Improving Insulation Methods in New and Existing Fabrication Processes

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Abstract

Silicon dioxide is widely used as a deposited insulator in a variety of fabrication processes for microelectronic devices and circuits. SiO_2 has a relatively low dielectric constant (3.9), is the native oxide of silicon and a natural choice for the silicon integrated circuit industry, and can be conveniently deposited with a variety of techniques. For this thesis, issues of insulator pinholes, edge/topology coverage, repeatable material parameters, and compatibility with liftoff processes are of particular importance. In this work, we focus primarily on the sputter deposition of silicon dioxide thin films, given the potential advantages typically offered by sputtering over the commonly used technique of evaporation for liftoff. An important additional thermal constraint in our work rules out PECVD or thermally grown silicon dioxide. The electrical and material properties of these films are in some cases essential to the intended devices, so the characterization of these thin films is an important aspect of this thesis. The optimization of the deposition method is also constrained by the fabrication process associated with the devices involved. A discussion of accompanying device processing improvements, including the resist etch-mask and liftoff processes for superconducting-insulator-superconducting (SIS) junctions, and the development of aerogel microelectrical-mechanical systems (MEMS) base devices with silicon dioxide capping layers will also be discussed. We find diode sputtered SiO_2 films to be superior to evaporated and magnetron films, where reduced pinhole density, superior edge coverage, low optical extinction coefficient, and a more repeatable dielectric constant is obtained with the diode deposited technique. With careful attention and adjustment of our fabrication processes, these diode sputtered SiO_2 films have been successfully incorporated into our existing superconducting circuits, replacing the SiO_x evaporation technique used in our devices for the past 25 years. The diode sputtered films were also successfully introduced into a newly developed single resist method for fabricating SIS junctions as well as for physical protection for aerogel thin film device insulation.

For Emily:
Home is whenever I'm with you.

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Everyone who kept the UVML running as smoothly as it did: Joe Beatrice, Alex Lobo, Harry Wade, and Tim Pernell. The way you keep all of the tools in the lab up is nothing short of amazing.

And finally my family for their never-ceasing love and support.

Chapter One: SIS Insulation Applications

Device insulation is an important component and a key area of research throughout the field of microfabrication. Electrical insulators can be used to protect more sensitive layers, block current flow, store charge, be an integral component of microstrip line elements, and provide other essential functions for proper circuit operation. Silicon dioxide is one of the most commonly used and studied insulators in this field with electrical and material properties that are highly dependent upon the deposition method (evaporation, sputtering, thermal growth, PECVD, etc.) and deposition parameters (pressure, initial material quality, deposition energy, etc.).

The electrical properties of insulators are very important as they affect circuit parameters including bandwidth and center frequencies for transmission lines. At higher frequencies circuit shunt capacitance, as determined by the dielectric constant of the insulator, becomes a non-trivial element that must be accounted for using circuit matching or by modifying the insulator parameters. For this work, the dielectric constant of the insulator must be taken into account when performing RF circuit design particularly in the placement of circuit elements like integrated tuning and coupling elements [1]. Having an unknown or run-to-run changing dielectric constant and/or dielectric loss due to process variation will impact performance by introducing additional error into the design via center frequency, bandwidth, and loss.

Issues of pinholes, edge/topology coverage, repeatable material parameters and compatibility with liftoff processes are of particular importance to this work. An important additional thermal constraint in our work rules out PECVD or thermally grown silicon dioxide. Evaporated SiO_x is frequently used in litoff processes due to its line of sight and low energy characteristics. However evaporated SiO_x often has an unknown stoichiometry due to its composition of free silicon, SiO, and SiO_2 that can vary run-to-run due to deposition parameters [2]. In this thesis we focus primarily on the sputter deposition of silicon dioxide thin films, given the potential material and electrical advantages typically offered by sputtering over the commonly used technique of evaporation for liftoff. However, numerous challenges exist to incorporate the sputtered film technology into our existing processes.

The terahertz frequency range is one of great importance to radio astronomers and superconductor-insulator-superconductor (SIS) devices are essential for sensitive heterodyne radio astronomy projects with frequencies up to ~1THz due to their low noise temperatures. These devices are fabricated in the University of Virginia Microfabrication Laboratories (UVML) cleanroom facility and many aspects of improving these devices for repeatability and reliability have been studied. Recent work our group has been involved in investigating includes alternative superconducting materials, tunneling barrier materials [3], beam leads, and an ultra-thin substrate architecture [4]. The properties of silicon dioxide films also play an important role in these devices as well. The quality of the sublimated (evaporated) silicon dioxide junction insulation used in SIS devices between the M1 base electrode and M3 wiring layer has always been a weakness that has been tolerated while pursuing other SIS performance

gains. This layer has been worrisome due to the use of evaporated SiO_x, as it is typically a poorly realized, silicon-rich stoichiometry with a significantly higher pinhole density than films deposited by other methods [5]. Since sublimated SiO_x is also a low energy process, the deposited film has insufficient step coverage that is necessary to robustly insulate SIS junctions, which will be discussed in depth in later sections. However, as SIS research continues to expand into device designs dependent on larger active areas of SiO_2 films, and on array applications where higher junction yields are important, improvements in the properties of this layer will be crucial.

The main process that this SiO_x film has to be compatible with is the Pentalevel junction insulation process [6]. The Pentalevel process is a self-aligning, five-level resist that allows for the precise definition of sub-micron SIS junction features using trilayer with a gold overlayer scheme as diagramed in Figure 1.1. This is the most critical processing step for creating SIS devices, requiring precise definition of the junction area, but it is also demanding of the SiO_2 layer.

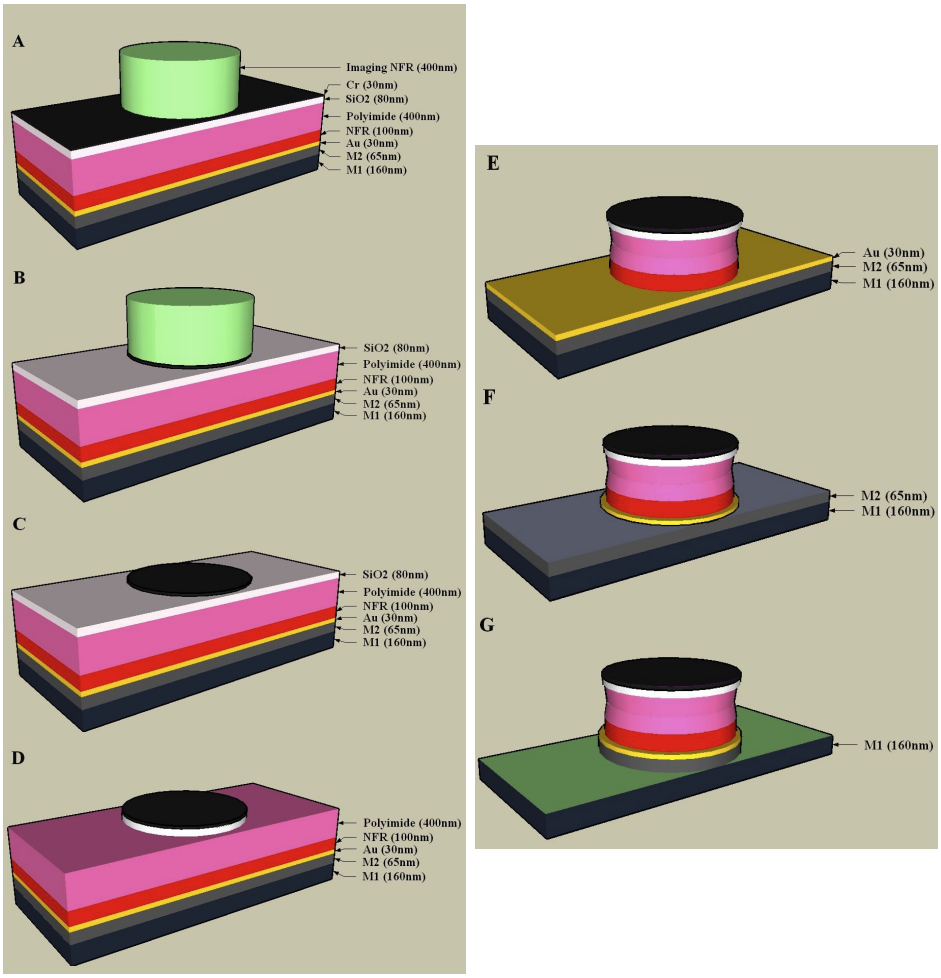


Figure 1.1: Pentalevel Process Flow Schematic [6]

The concept of using a multi-layer resist for creating junctions started for this group with the fabrication of micron sized Nb/Al-Al_2O_3/Nb Junctions with a trilevel resist liftoff

process [7,8]. This process replaced the previously used single resist approach that utilized a combination of anodized Nb_2O_5, formed from the exposed niobium, along with evaporated SiO_x for the insulation layer encircling the device junctions and between the M1 base electrode and M3 wiring layers. The yield of this anodization + SiO_x process was poor for junctions smaller than 3μm x 3μm. With smaller junctions becoming a necessity, a trilevel junction stack was developed.

One of the main deficiencies in the anodization + SiO_x single resist process was that the niobium junction etch was isotropic, resulting in a gap between the SiO_x junction insulation and the M2 junction counter-electrode the SiO_x was to have sealed. The idea of using a multilayer resist was conceived with the expectation that after performing the junction etch the organic sidewalls could be further shrunk with a high pressure oxygen plasma, revealing the perimeter of the niobium junction and hence allowing the subsequent SiO_x insulation to 'reach' and satisfactorily seal the edge of the niobium junction [9]. To mitigate these problems, the wafer was rotated and positioned ~7 degrees off-axis above the SiO_x source, to insure a line-of-sight deposition that would reach the edge of the M2 junction.

As defined in our group's previous work, "multi-layer resists typically are composed of thick bottom organic 'planarization' layer(s), a thinner inorganic 'barrier' layer(s) and a top imaging layer of photoresist." [6]. After all the layers are deposited onto the device wafer and the imaging resist is patterned, the barrier layer is etched. The barrier layer then serves as an etch mask for the subsequent oxygen based etch of the organic planarization layer. Immediately after that step, a reactive ion etch (RIE) is performed on the M2 Niobium counter electrode. After this etch, the SiO_x interlayer dielectric is deposited on the whole wafer and the Pentalevel stack subsequently removed via liftoff with a liquid resist stripper that attacks the organic planarization layer to remove the entire stack. The sidewalls of the SIS junction are now hopefully sealed by the dielectric insulator and only the top of the junction is exposed and is now ready to be connected by an M3 Niobium wiring layer.

In the first trilevel resist attempts a polyimide was used for the planarization layer, topped by a sputtered SiO_2 barrier layer, and a high resolution imaging resist. Though this process successfully realized SIS junctions, the barrier layer of SiO_2 etched in the fluorine based Niobium junction counter-electrode RIE. This made it difficult to control junction area sizes as they approached a 1μm diameter and additionally the process was very susceptible to debris and micromasking. A Quadlevel process was subsequently developed to address some of these issues [9], followed by the Pentalevel process. The final Pentalevel process uses a bi-layer NFR/polyimide planarization layer, SiO_2/Cr barrier layer, and high resolution imaging resist and is able to create SIS junctions with diameters down to 0.4μm in diameter [6].

In the Pentalevel process, the SIS trilayer is in-situ topped with a thin (30nm) gold overlayer. This gold is left atop the junction during the junction process, complicating the fabrication process. However, the advantage of this gold overlayer approach is that the gold prevents the formation of oxides on top of the junction, so that the subsequent wiring step can be performed without any in-situ physical clean. For regular trilayer junctions, a

sputter etch step is required before M3 wire deposition, and this physical clean tends to attack the SiO_x insulation coverage around the junctions and also open up pinholes in the SiO_x film. The gold overlayer allows one to avoid this deleterious physical clean. In the Pentalevel process after the oxygen etch of the organic planarization layers, the organic layers are modestly undercut with respect to the inorganic SiO_2/Cr barrier layers. The uncovered overlayer gold is then sputtered etched away, though the extent of the gold buttons left on the wafer follow the larger extent of the barrier layers and not the undercut organic layers. The subsequent Niobium RIE, which is now satisfactorily anisotropic, follows the gold pattern and leaves an Nb/Au junction button that extends beyond the perimeter of the organic layer. Such a feature provides excellent liftoff and it also permits the SiO_x junction insulation to overlap the perimeter of the Nb/Au button, providing improved sealing over earlier methods [6].

With the improvements seen from the Pentalevel process and gold overlayer, the SiO_x interlayer dielectric was targeted as the next necessary area of improvement. As mentioned earlier, the evaporated SiO_x currently used in this process is a silicon-rich film that allows leakage current stemming from pinholes in the film itself [5] and poor step coverage of the Pentalevel structure. However test capacitors used to determine the dielectric contact of the SiO_2 films from run to run were almost always found to be shorted from pinholes. These issues led to exploring different ways of depositing this insulating layer by means other than evaporation.

In changing the deposition method used for the junction SiO_x layer, the properties of this thin film will also be different and it has to remain compatible with the Pentalevel process. As with the silicon-rich sublimated films, the dielectric constant does not have to be the same as pure SiO_2 but it does need to be repeatable. The photolithography mask design process takes into account the thickness and dielectric constant of the insulating film and sizes the wiring interconnects and other structures appropriately. A certain minimum insulator thickness is needed to prevent 'cross-talk' between the base electrode and top wiring layer, necessary for proper device functionality. The SiO_x film must also seal the Pentalevel realized SIS junctions and provide adequate coverage for the entire device. Pinholes or other regions of poor coverage are a major concern and an adequate thickness and step coverage should be considered with any deposition method. A thicker SiO_x layer, from purely edge coverage and pinhole considerations would obviously be advantageous, but this must be balanced against the need for liftoff of the Pentalevel structures and also the impact of thicker SiO_x layers on circuit design. Liftoff can be a difficult process, especially with a thicker SiO_x layer.

The evaporated SiO_x currently used in the Pentalevel process sublimates solid SiO held in a baffled crucible heated by a high current source. The attraction of this method is the ease in liftoff processes as it is low-energy depositions that deposits in a line-of-sight manner that will not cover resist sidewalls. The resulting typically silicon-rich film has potential leakage current paths due to pinholes and the inability to fully seal the SIS junction are the weaknesses of this deposition method that has led to the exploration of using other tools for the interlayer dielectric.

The SiO_x deposition step is also constrained by temperature requirements. High energy and high temperature methods of insulator deposition like thermally growing or PECVD deposition of thin films have been shown to damage the thin insulator tunnel barrier in the SIS stack [10]. Interdiffusion between niobium and aluminum, changes in barrier composition, and oxygen diffusion from the counter electrode surface are all factors that degrade the properties of SIS junctions with oxide tunneling barriers at temperatures above 200-250° C and are also still significant for AlN SIS tunneling barriers. Some groups have developed low temperature PECVD tools for lower temperature deposition [11], but the UVML PECVD tool does not possess this capability and PECVD was eliminated as a SiO_x deposition method for this process.

Sputtering has advantages over evaporation as it is a higher energy method of deposition, allowing for more surface mobility to reduce the amount of pinholes in the deposited film. Sputter also uses a larger material source and operates at a higher pressure, allowing it to deposit in a non-line-of-sight manner. It therefore could be a candidate to ensure the junction insulator deposition is fully sealed, as seen in Figure 1.2. It is also thermally compatible with the SIS stack, as it does not require a high sample temperature and offers the potential to improve step coverage and reduce pinhole density in this process. However, earlier attempts at sputtering SiO_x were not compatible with the Trilevel process during the resist liftoff step. The physical sputtering plasma attacked the resist, leaving a ring of SiO_x around the junctions that had a different large grain size/irregular appearance than the SiO_x deposited in the fields between junctions. During liftoff, this malformed ring would typically liftoff leaving the niobium junction button unsealed. This led to the adoption of evaporation as the preferred method [8,12]. With multiple sputtering tools and the ability to test varied deposition parameters, it was decided to again investigate sputtering as a method to deposit junction SiO_x to take advantage of the beneficial properties of this deposition method.

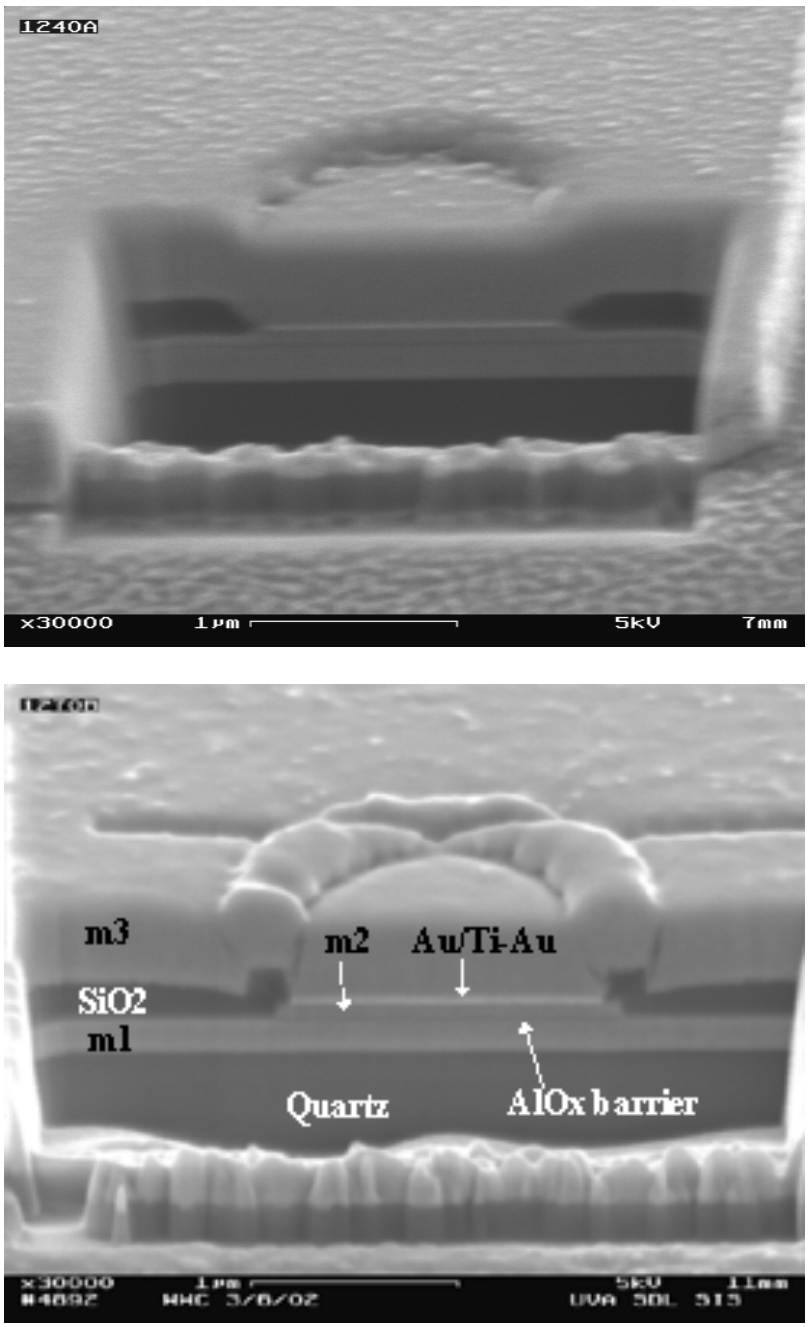


Figure 1.2: Edge Coverage for Evaporated (Top) and Sputtered (Bottom) SiO_x

Taking into account the intended use for the SiO_x film and the desired characteristics, experiments were conducted to compare the multiple deposition tools available in the UVML cleanroom. These systems included an RF diode sputtering system (used in previous attempts for sputtered SiO_x where liftoff was unsuccessful), a magnetron sputtering system with an eight-inch diameter gun, a magnetron sputtering system with a three-inch diameter gun, and an evaporation system. All of which are described further in Appendix A. The facility's PECVD system was not used because of the concerns

about SIS barrier damage. Also as a comparison, commercially purchased wafers with thermally grown SiO_2 were also evaluated.

The diode sputtering system and magnetron sputtering systems operate similarly, where a solid physical target composed of SiO_2 deposits a thin film of SiO_x onto the substrate by means of ion bombardment with a RF-induced plasma in a vacuum chamber with an argon working gas environment. Radio frequencies are required here (as opposed to DC sputtering) because of the need to deposit using a target composed of an insulator. Diode sputtering has a short separation of the target and substrate (less than 4cm), where magnetron sputtering uses an array of rare earth magnets to shape the electric fields and plasma in the system to concentrate the deposition and increase the separation length (12-23cm in our tools). Magnetron sputtering allows for higher deposition rates and lower operating pressures than diode sputtering, but both methods were considered due to of the availability of the tools.

To properly compare and analyze these different films, suitable metrology and characterization techniques were employed. A focus was placed on using ellipsometry and mercury probe techniques due to the non-destructive nature of these tests, quickness of these methods compared to other techniques, and the availability of newly-installed equipment in the UVML.

Ellipsometry was a readily available option for use in the UVML as a method of determining SiO_2 quality and thickness and was employed early on for metrology. This method measures the reflection of polarized light off of the sample surface, measuring the electric field waves from the light parallel to and perpendicular to the plane of incidence. The phase shift between these waves is defined as the parameter Δ and the ratio of the amplitudes ψ. These quantities are directly measured by the ellipsometer and are then used to determine material parameters like thickness using sample and material models [13].

The first property of the deposited SiO_x films that was examined was the thickness of the deposition. While other methods were available, the ease and non-destructive nature of ellipsometry made it an ideal candidate for discovering the thicknesses of the deposited SiO_x films and how the thickness varied when changing deposition parameters like power or pressure.

Another desired parameter from this tool was quality of the SiO_x film, determined in this case by the dielectric constant, lack of pinholes, etc. The static dielectric constant is a DC measurement or one at infinite wavelength. It could not be directly measured by the in-house ellipsometers, as they did not reach enough into the infrared wavelengths to give an accurate measurement. However, the dielectric constant of any film is directly related to the optical constants of that material, which could be modeled over the wavelengths available to our tools. These are defined as n, the index of refraction, and k, the extinction coefficient [13].

For insulators in the visible range of light used by this ellipsometer, the Cauchy function can be used to describe n as a function of wavelength and ignore k as it is essentially zero in this range:

$$n(\lambda) = A + B/\lambda^2 + C/\lambda^4 \quad [13]$$

This equation allows for a comparison of the measured index of refraction against other samples using different deposition methods or parameters. While it cannot give the static dielectric constant or directly indicate the presence of pinholes, it can show the quality of SiO_x thin films in relation to other samples.

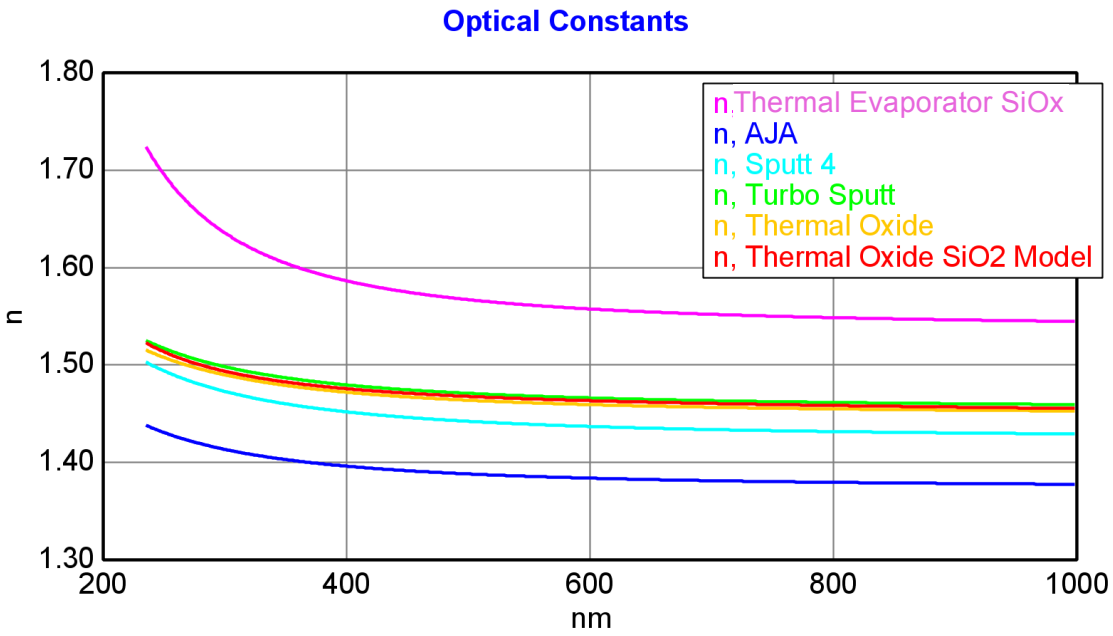


Figure 1.3: Ellipsometry Results for n, the Index of Refraction, Across All Available Tools

From Figure 1.3, it can be seen that the ellipsometry results from the Cauchy model graphing index of refraction, n, versus wavelength. Measuring the thermally grown SiO_2 gave a baseline to compare the other results. The model value for pure SiO_2 was also gave a curve for comparison. These show a much higher n for the evaporated SiO_x and a much lower n for the AJA system, a magnetron sputtering system. In contrast, the magnetron sputtered Sputt 4 film and diode sputtered Turbo Sputt films were relatively close to the thermal measurement. By expanding this model to also include the k, the extinction coefficient, it can be observed that the graph has a non-zero component for k for the evaporated and both magnetron sputtered SiO_x films in Figure 1.4. Having a non-zero k value means that the film is absorbing some light and that these films are silicon-rich since SiO_2 is a transparent film at these wavelengths. As a result, our focus was on the diode sputtering system.

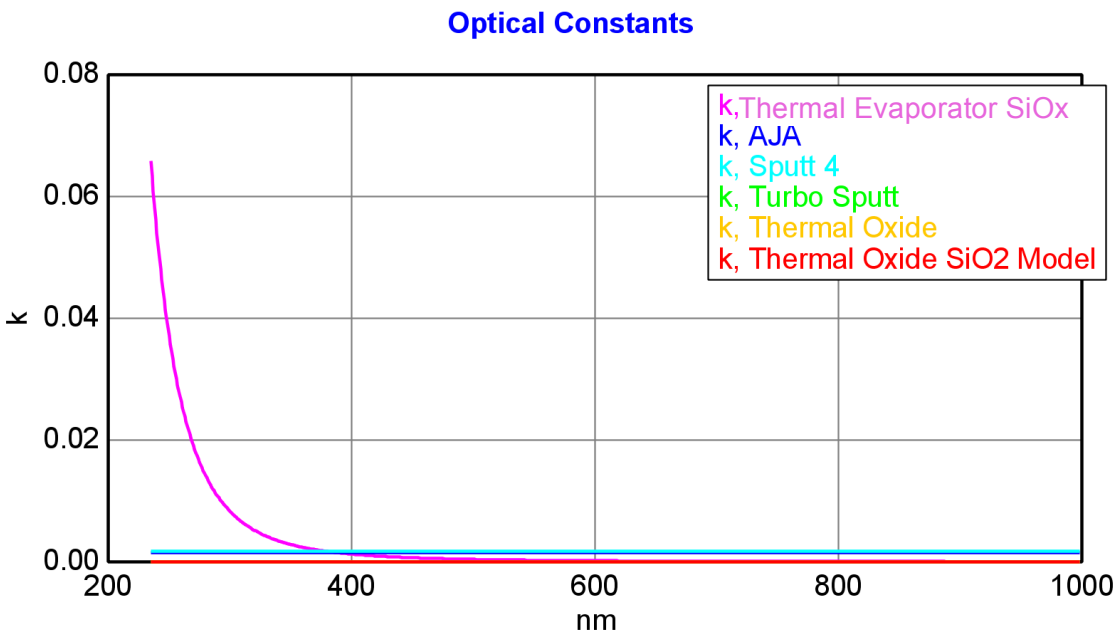


Figure 1.4: Ellipsometry Results for k, the Extinction Coefficient, for the Best Available Tools

To further test the quality of the deposited films, particularly from the tools highlighted by ellipsometry measurements, the film dielectric constant could be determined by creating capacitors. These devices could also provide for the detection of the amount of current leakage through the oxide and give a sense of the pinhole density of the film. Mike Cyberey designed a materials mask (Figure 1.5) to determine the properties of superconducting materials as well as interlayer dielectrics. While the cleanroom fabrication process is established for creating simple structures like capacitors, the time involved in deposition, lithography, etching, etc. takes an upwards of two weeks for each SiO_x deposition and is not a nimble way to study these thin films and how deposition parameters affect their quality. Early results from the capacitors constructed using magnetron sputtered films had a high leakage that prevented any meaningful C-V results for these films.

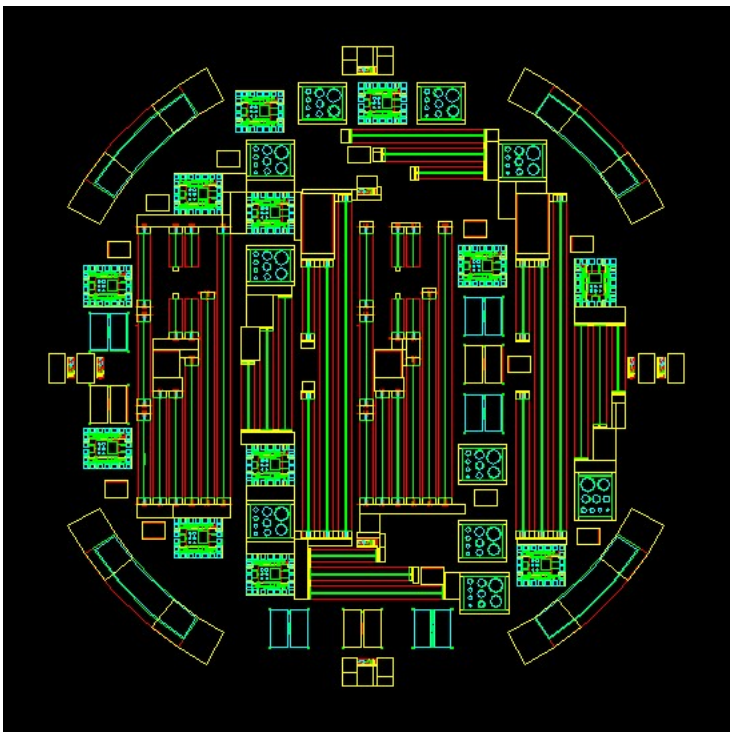


Figure 1.5: Materials Mask CAD Layout (Capacitors are the sets of 9 Blue Circles at Different Locations Across the Wafer)

A similar idea was then pursued to give a comparison of film quality between SiO_x deposition methods while reducing the amount of time necessary to produce an entire wafer using the materials mask set. A simple metal-insulator-semiconductor (MIS) capacitor could be created using a mercury probe system. This tool uses a small, well-defined (known diameter) drop of liquid mercury on top of a silicon/SiO_x wafer that is connected to a LCR meter and computer for measurement. This creates a structure that has been studied extensively in semiconductor devices and will result in measuring the dielectric constant of the material, as well as the leakage through the film that should reflect the amount leakage from pinholes in the SiO_x film.

Results from sending out wafers to Materials Development Corporation (MDC) for mercury probe testing showed that the evaporated oxides and magnetron sputtered oxides were very leaky and gave capacitances that were much higher than expected. The diode sputtered oxides showed low leakage with good I-V curves and reasonable permittivity values in Figures 1.6 and 1.7.

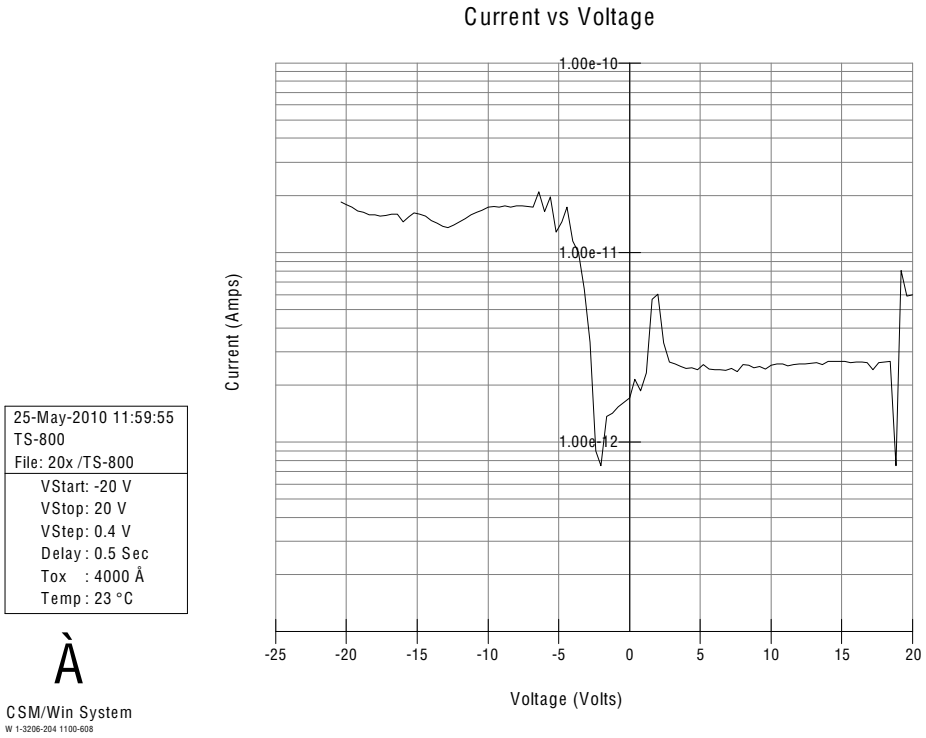


Figure 1.6: Diode Sputtered SiO_x I-V Curves via Mercury Probe

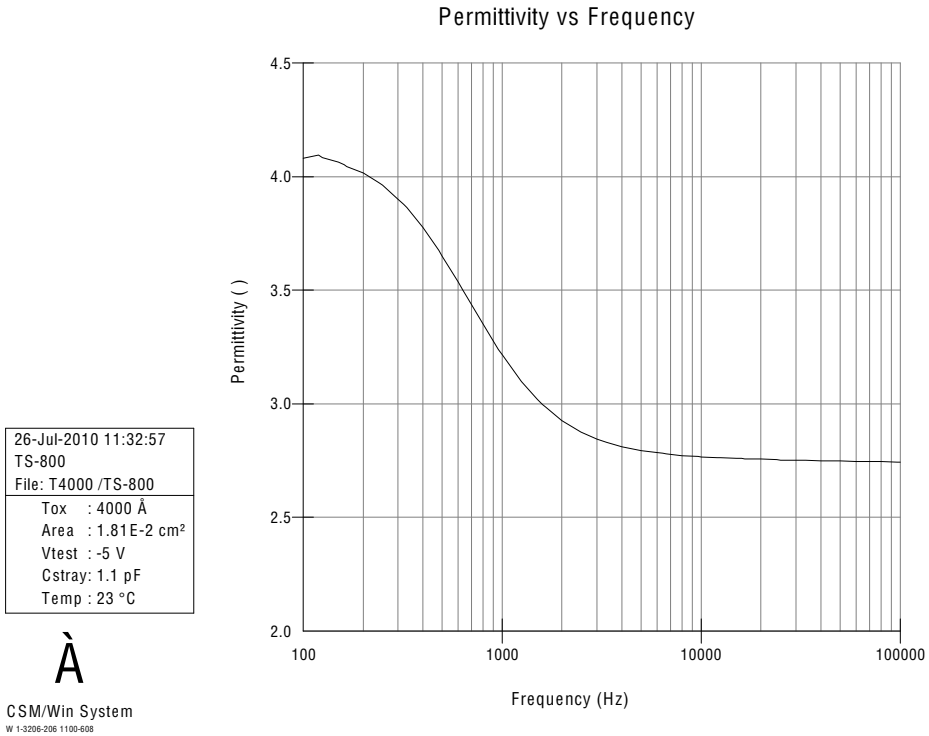


Figure 1.7: Diode Sputtered SiO_x Permittivity vs. Frequency Curves via Mercury Probe

The mercury probe results were backed up by capacitor measurements showing high leakage for magnetron sputtered films, but good numbers for diode sputtered films. Using all of this data, we have decided to move forward with testing diode sputtered SiO_x as the junction insulation in the full Pentalevel process as it has the best film qualities and provides the previously established advantages of sputtering over evaporation.

It is believed that the fact that the diode sputtered SiO_x films were of higher quality than the magnetron sputtered films can be explained at least in part by the geometry of the tools. The distance between target and substrate for the diode sputtering tool is about 4cm whereas the magnetron sputtering tools have throw distances at least three times larger. Constraining the sputtering plasma into a much smaller space means that higher energy sputtered particles will impact the wafer, allowing for increased surface mobility which allows the particles to move around and find an optimal place to settle.

While the above results focus on the optical properties, dielectric constant, and pinhole density of the deposited films, a high quality SiO_x film is of no value if it cannot be incorporated into our processes. Therefore SiO_x sputtered from the diode sputtering system onto the Pentalevel resist stack must properly cover the device geometry while allowing liftoff to occur. Earlier tests of diode sputtered SiO_2 films gave results where the sputtering process used (including a sputter etch step) attacked the resist in the Trilevel structures and left behind a damaged ring of SiO_x around the junction areas [12] and liftoff itself was problematic. Another requirement for testing sputtered SiO_x with the full Pentalevel process is to determine device parameters as some groups have experienced very high dielectric losses with sputtered SiO_x films [14].

The initial tests to determine diode sputtered SiO_x compatibility with the Pentalevel process began with putting down a much simpler, negative single resist on a scrap trilayer wafer, sputtering a relatively thick layer of SiO_x (~300nm) and then seeing if the resist could be removed via liftoff and using an SEM to examine the resulting structure. Built into the N-10 mask used for these lithography tests are arrays of different sizes of junction buttons from 4μm down to 0.6μm. These were used extensively to determine not only if liftoff of diode sputtered SiO_x was feasible, but also to determine the smallest sized junction that could be fabricated.

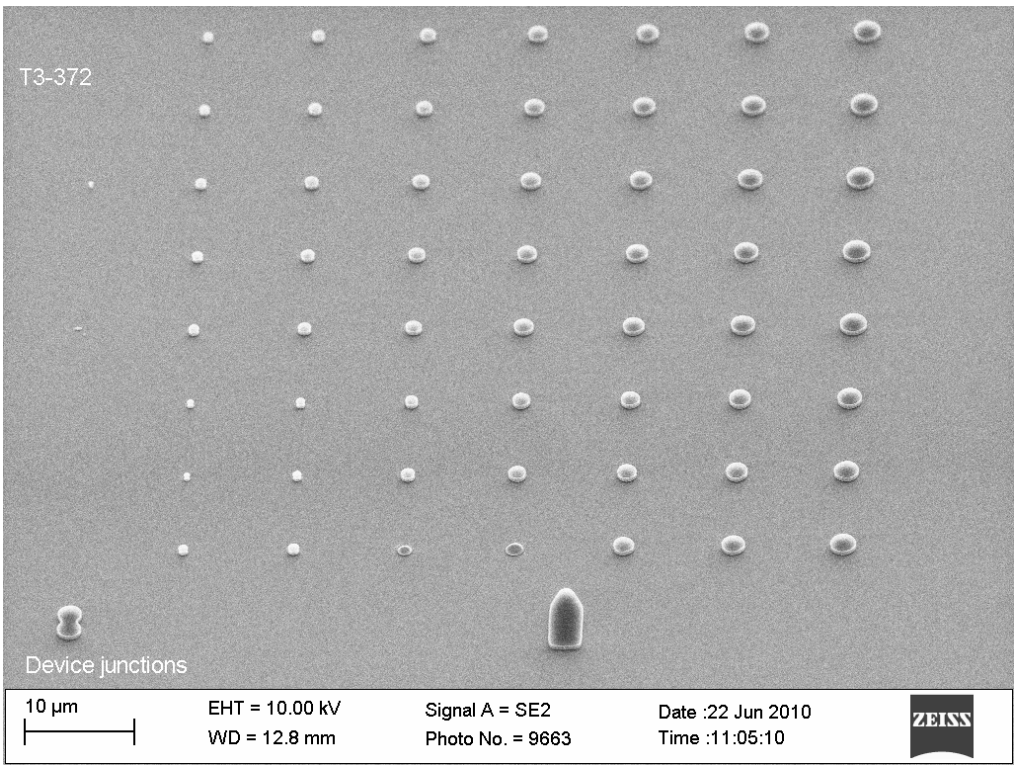


Figure 1.8: N-10 Junction Array SEM After Photolithography, Before SiO_x Deposition

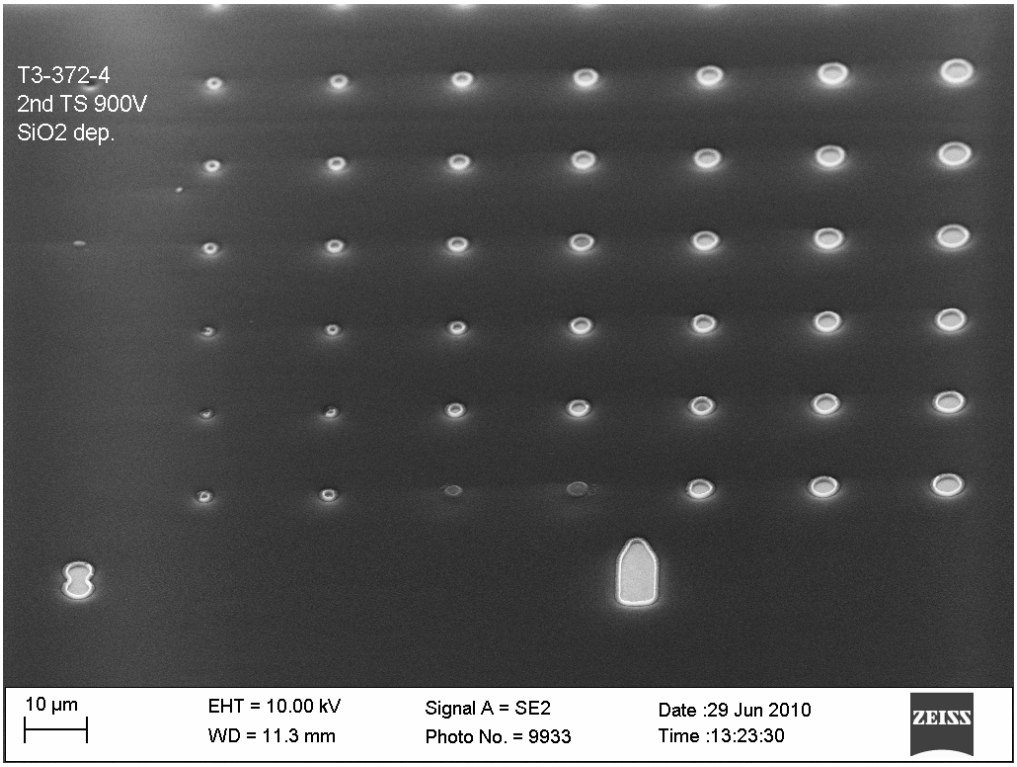


Figure 1.9: N-10 Junction Array SEM After SiO_x Diode Sputtered Deposition and Liftoff

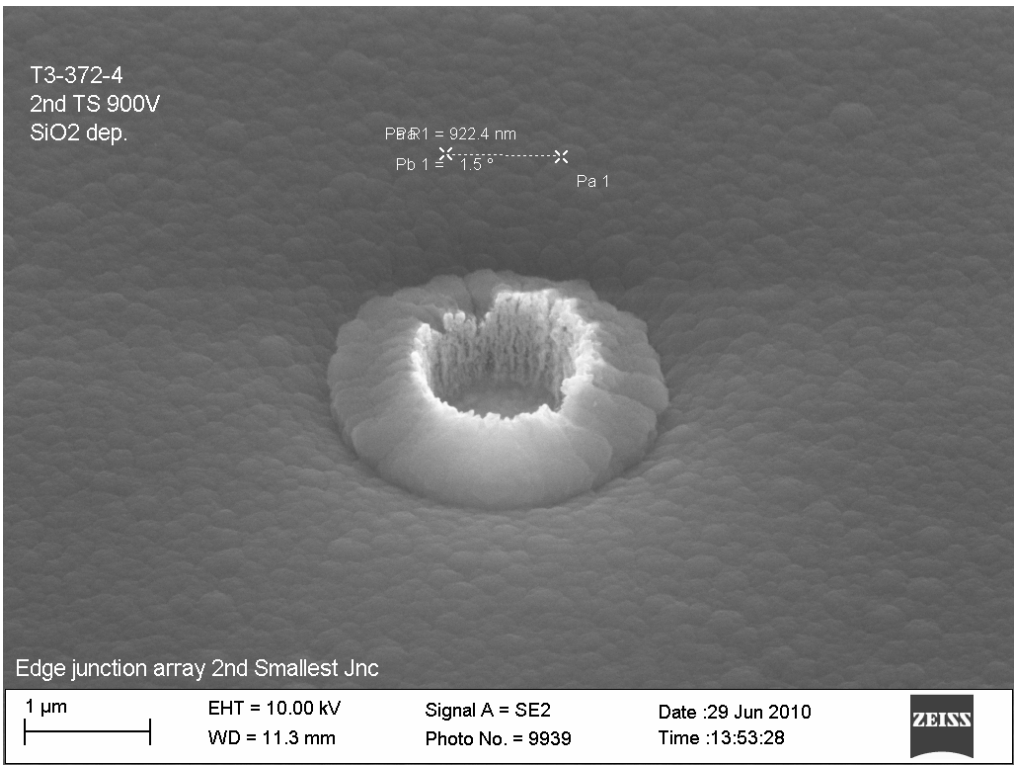


Figure 1.10: Individual Junction Array Button SEM After SiO_x Diode Sputtered Deposition and Liftoff with 922.4nm Diameter

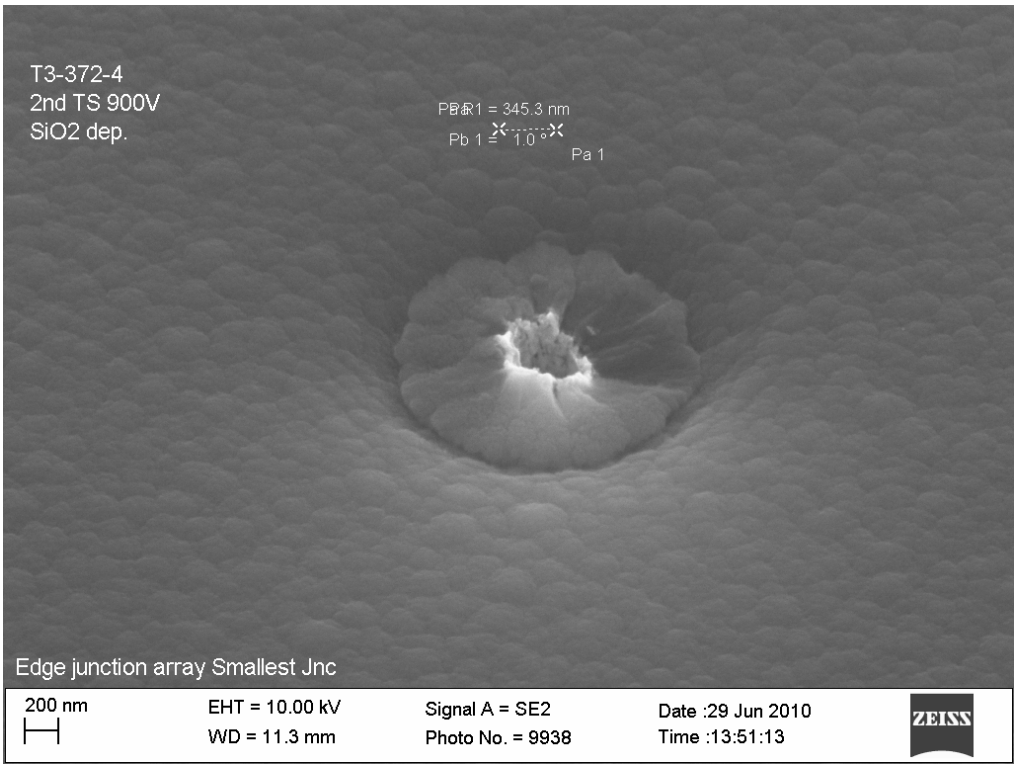


Figure 1.11: Individual Junction Array Button SEM After SiO_x Diode Sputtered Deposition and Liftoff with 345.3nm Diameter

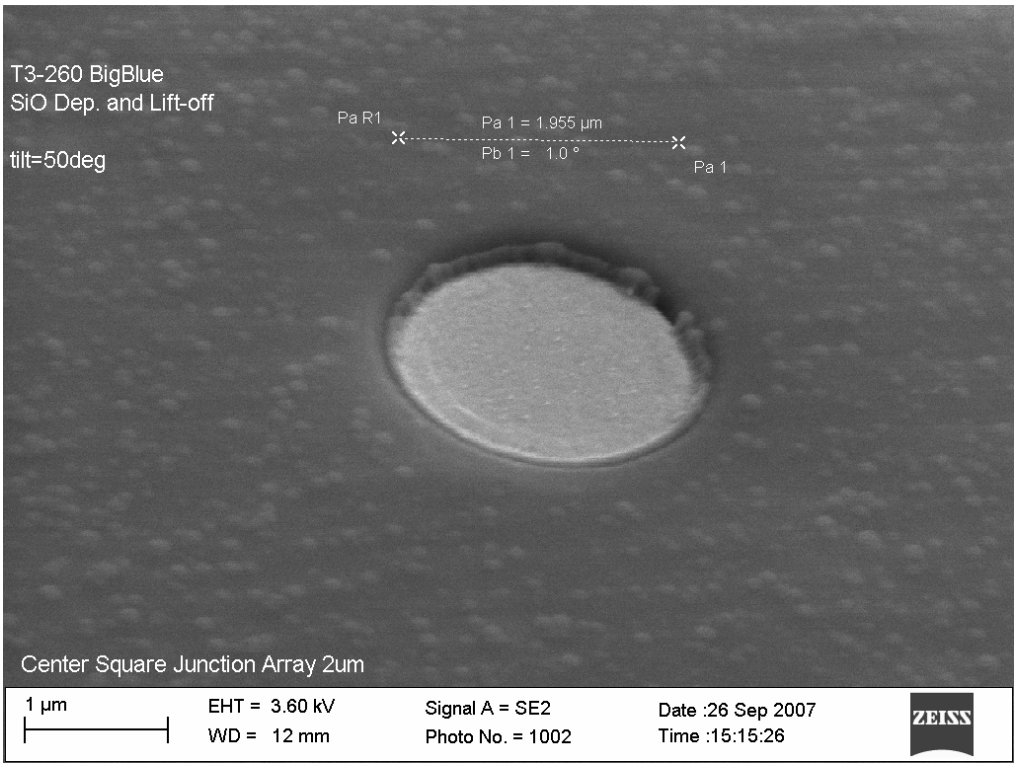


Figure 1.12: A Real SIS Device Junction SEM with Evaporated SiO_x After Liftoff

It was clear from the SEM images of the wafers before and after diode sputtering SiO_x in Figures 1.8 through 1.11 that a realistic insulator thickness could be deposited and the resist would still be able to liftoff afterwards. The next step would be to fabricate actual Pentalevel device wafers and use their results to determine if this process change would give improved insulation in the fabricated SIS devices. Comparing the sidewall coverage of diode sputtered to evaporated SiO_x (Figure 1.2) via SEM revealed the expected improvements from the higher energy deposition as well.

This result did not clarify why this process was successful while previous attempts years ago at using sputtered SiO_2 failed. However, further tests revealed that the sputter clean was at least to blame for hardening the resist and inhibiting liftoff. In diode sputtering, if the polarities of the parallel plate platters are reversed, the ionized gas particles are attracted to the sample holder and physically bombard the sample. This in-situ ion bombardment is often used prior to thin film sputter deposition to clean the surface of any moisture or unwanted thin oxide to ensure good film adhesion to the substrate, this step also hardened the patterned resist and kept it from dissolving during liftoff. By not including a sputter clean step in the new process flow, consistently liftoff of both the single resist and Pentalevel structures after SiO_x sputtering was possible. It is therefore also possible that the nLOF resist used for this work additionally less affected physically by the sputtered SiO_x. Emboldened with this success, the next test was using diode sputtered SiO_x in a Band 3 processes for both 1st and 2nd SiO_x shown after the M3 wiring layer etch in Figure 1.13. The resulting dip test I-V curves showed the Band 3 wafers had good

electrical characteristics (Figure 1.14) and subsequent mixer tests by Herzberg Institute of Astrophysics met the ALMA Band 3 specifications.

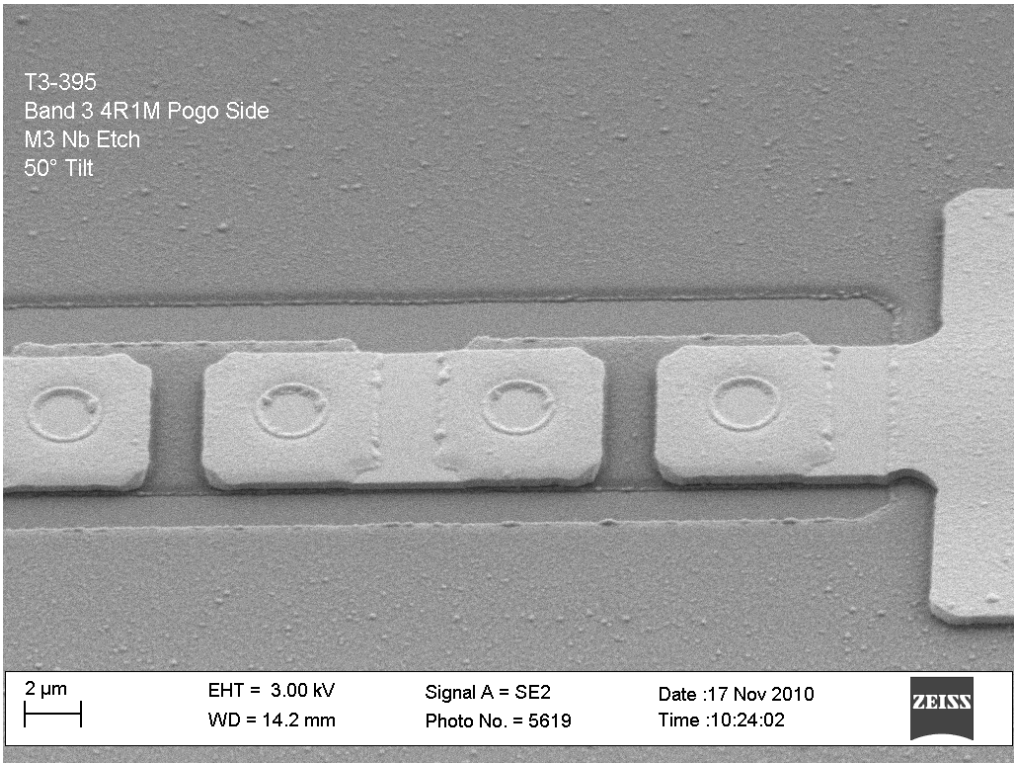


Figure 1.13: Band 3 Wafer SEM with Diode Sputtered SiO_x After Niobium M3 Etch

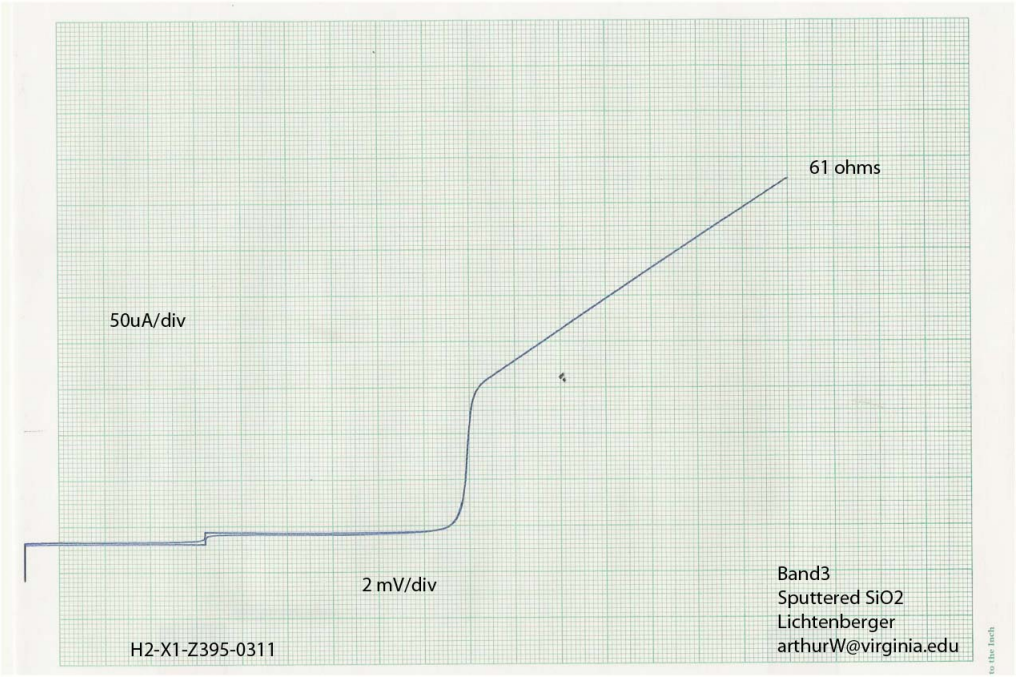


Figure 1.14: Superconducting Dip Test I-V Curves for the Band 3 Wafer with Diode Sputtered SiO_x

This result is a very important one as ellipsometry, mercury probe, and SEM results also show that diode sputtered SiO_x is the best option for high quality sputtered films. It is therefore important to note that since this result, sputtered SiO_x has been used as the junction insulation in all of our SIS device processing, replacing the long standing evaporation process of over 25 years.

Future work on this project includes ensuring our group has a single purpose tool to deposit diode sputtered SiO_x. The current diode sputtering tool has many users and targets of different materials; tool downtime and film repeatability are therefore concerns with the current system. One of the magnetron sputtering systems used in this study, Sputt 4, has been converted into a diode sputtering system by removing the rare earth magnets in the sputtering gun and modifying the electrical connections to handle increased current from the power supply. Target to substrate spacing, power per unit area, and deposition pressure have been matched to the other system to try and recreate the successful oxide films with this new dedicated tool for SiO_x deposition. Characterization work is ongoing to be able to adjust deposition parameters to achieve a high quality SiO_x. Figures 1.15 through 1.17 show ellipsometry measurements for varied DC biases and pressures, but mercury probe testing and capacitors fail to show a film that has a low enough leakage to get good dielectric constant measurements out of and Pentalevel junction insulation testing will not start until this leakage is reduced. Reactive sputtering is also of interest as the AJA magnetron sputtering system is equipped with a O_2 + Ar gas line to maintain the proper stoichiometry for sputtered SiO_2.

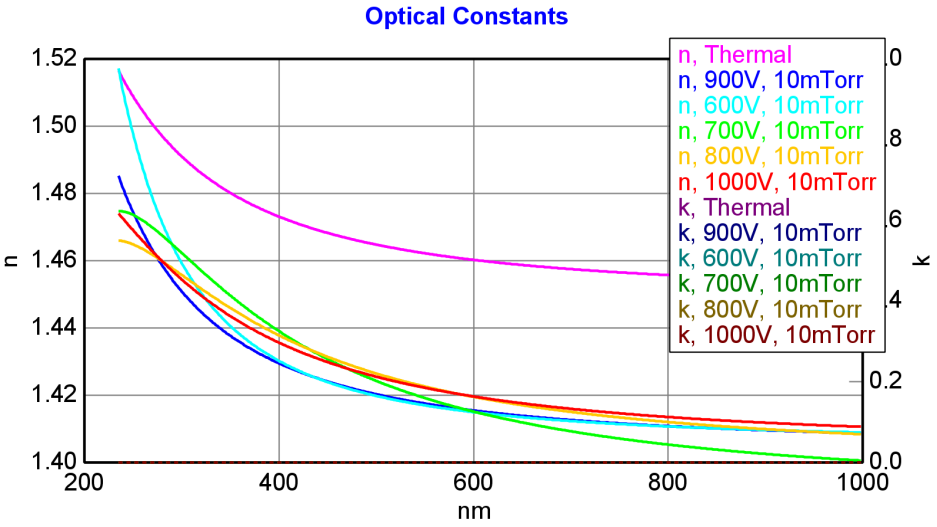


Figure 1.15: Diode Sputtered Ellipsometry Results at 600V-1000V DC Bias, 10mTorr

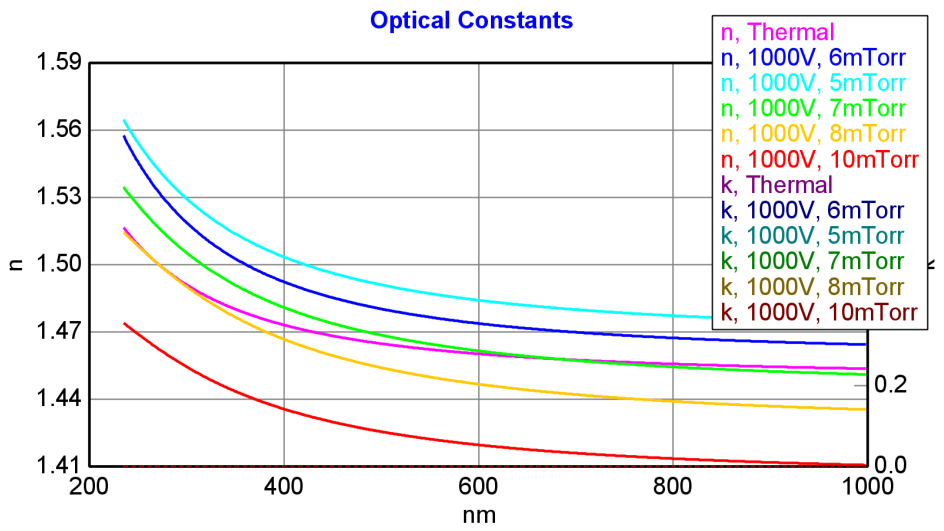


Figure 1.16: Diode Sputtered Ellipsometry Results at 1000V DC Bias, 6-10mTorr

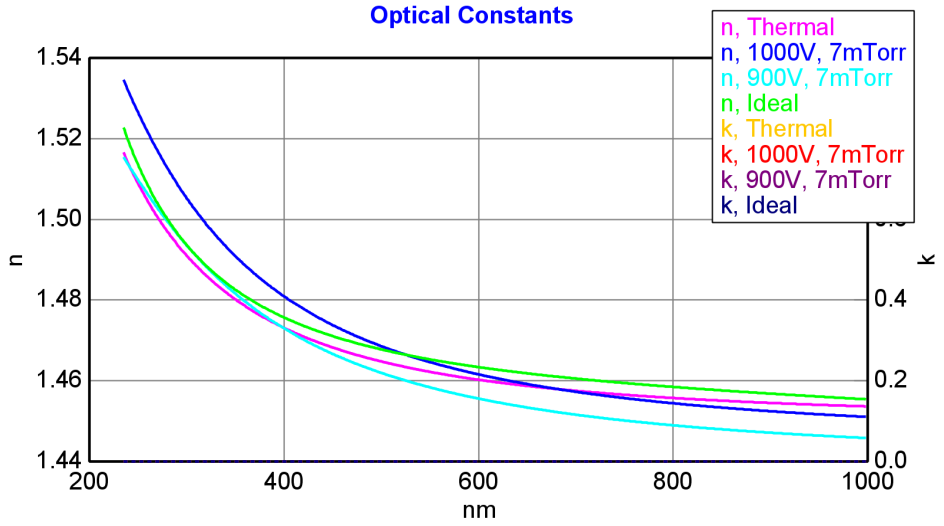


Figure 1.17: Best Diode Sputtered Ellipsometry Results

Chapter Two: Single Resist Processing

In developing an improved method for SIS device insulation, the amount of time required to fabricate a complete SIS device prevented agile feedback of the electrical characteristics of evolving fabrication and trilayer deposition processes. Any major improvement to the Pentalevel junction process will require fabrication of multiple wafers using the whole process to study the effects of these experiments. With each test wafer taking more than a month to fabricate, a significant amount of time will be required to fully understand the impact of any process changes. This will impact the study of alternative methods for depositing SiO_x films, but also the study of new superconducting films or barrier materials for the trilayer stack. While information on the properties of any of these materials can be obtained from direct measurement of the film using metrology tools, only in the construction of full SIS devices and their resulting superconducting I-V curves and critical current density and resistance measurements can it be determined if these process changes are beneficial. Chapter One is an example of the necessity of the construction of SIS devices with our new SiO_x deposition method, as ellipsometry and mercury probe tests cannot determine the compatibility of sputtered SiO_x with liftoff.

A single resist process would be the preferred candidate over the Pentalevel junction process for reducing the processing time of a single test wafer from over a month to less than two weeks. Potentially, there will also be drawbacks to this method: less precise control of junction area, increased difficulty in both defining sub-micron sized junctions and SiO_x insulation lifting off, etc. However for specific prototyping purposes, a single resist process would be a major benefit. A single resist process was previously developed before at UVA [7], but was for junctions larger than 3μm in size and used evaporated SiO_x. As a testing method, and not as a means of producing SIS devices for real applications, the yield and device area are less critical so long as working junctions are created with a known diameter. However for most of our current research with higher current density junctions (>10kA/cm^2), junction sizes must be less than 2μm to avoid self-heating affects of the junction M2 superconductor.

In order to use only a single resist layer, this photoresist must be able to withstand a variety of processing techniques and still be able to liftoff afterwards. As mentioned in Chapter One, a previous attempt at developing a single resist process failed because the physical sputtering plasma attacked the resist, leaving a ring of SiO_x around the junctions that had a different large grain size/irregular appearance than the SiO_x deposited in the fields between junctions. During liftoff, this malformed ring would typically liftoff leaving the niobium junction button unsealed. That single resist process used just a 'simple' SIS trilayer stack. Our current SIS trilayer, as described earlier, has an additional gold overlayer to ensure electrical connectivity of the niobium M3 metal wiring layers by preventing any niobium oxide growth on the junction counter electrode (M2) that would otherwise require a physical in-situ clean (e.g., sputter etch or ion mill) in the subsequent wiring process. Such a physical clean can damage the insulating SiO_x layer, particularly around the junction, and lead to micro-shorts in the circuit [15]. To maintain the benefits of the gold overlayer process, the new process must also be able to define a

properly sized junction and keep its shape during the gold etch to define the junctions. The resist must hold up to the following niobium M2 counter-electrode etch. After the etches are complete, SiO_x is deposited either by evaporation or sputtering, as described in the previous chapter, and the resist then has to lift off to give a well-defined and sealed junction.

The development of a new single junction resist method began with an established nLOF negative resist stack used in other processes for SiO_x liftoff (Band-6 2nd SiO_x) of larger sized features. An experiment was set up to prove the feasibility of lifting off small resist junction buttons (~1 micron in diameter) by first spinning diluted NFR as an adhesion layer followed by nLOF 2020, a negative resist designed for use in liftoff processes, onto a 50mm diameter silicon wafer that had a surface thin film coating of evaporated chromium to provide a good layer for the resist to adhere to and a contrast material for SEM images of the final results. The resists were patterned using the UVML's EVG contact mask aligner. An SEM of the subsequently developed nLOF pattern is shown in Figure 2.1. The total thickness of these resists was determined to be 1.39μm when measured by profilometer. A SiO_x thin film was the next deposited onto the wafer using the diode sputtering system, avoiding the sputter etch step. We were able to successfully liftoff the junction resist patterns after the SiO_x deposition and show through SEM that even some of the smallest resist features (~250nm at the base of the resist profile) in the mask test array were well defined after liftoff (Figures 2.2 and 2.3).

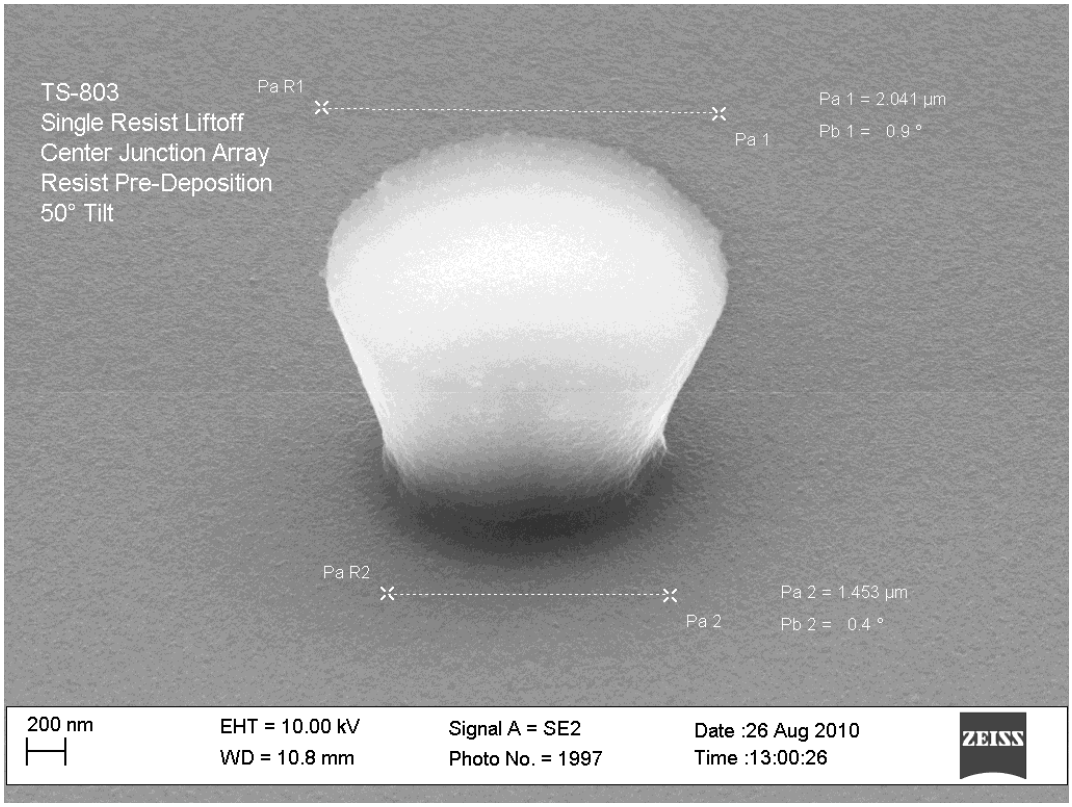


Figure 2.1: Single Resist on Cr SEM Before SiO_x Deposition and Liftoff

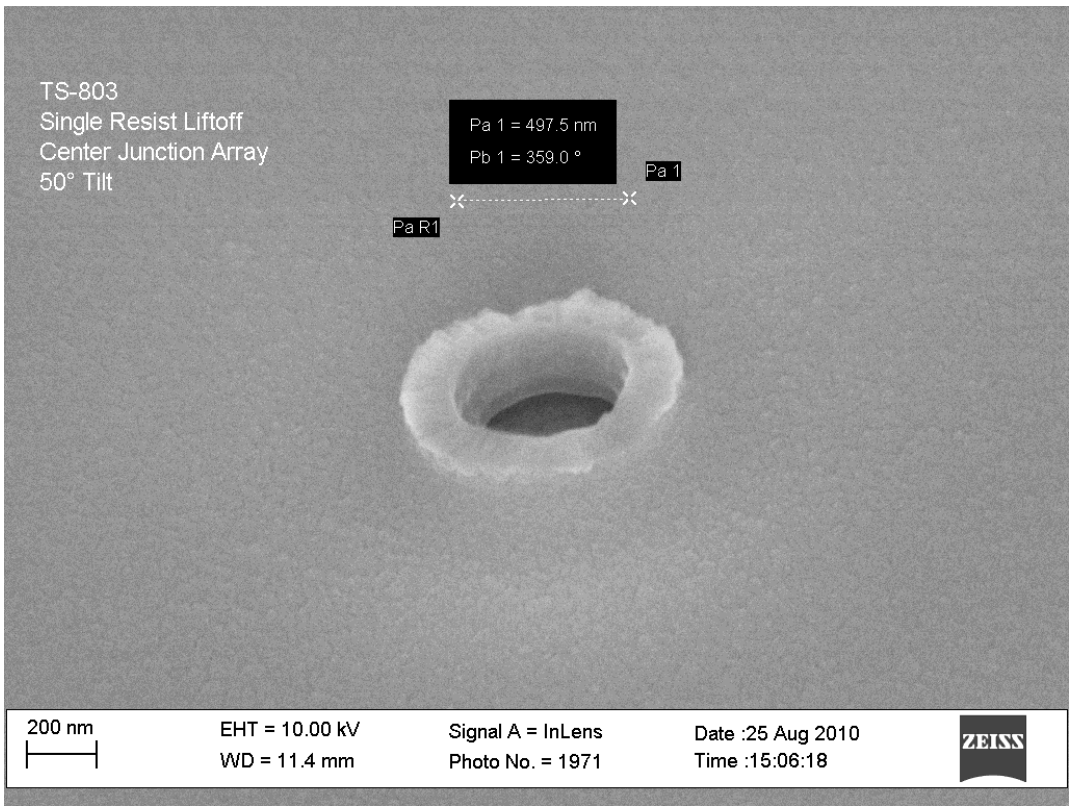


Figure 2.2: Tilted SEM Image of a Successful Single Resist Liftoff

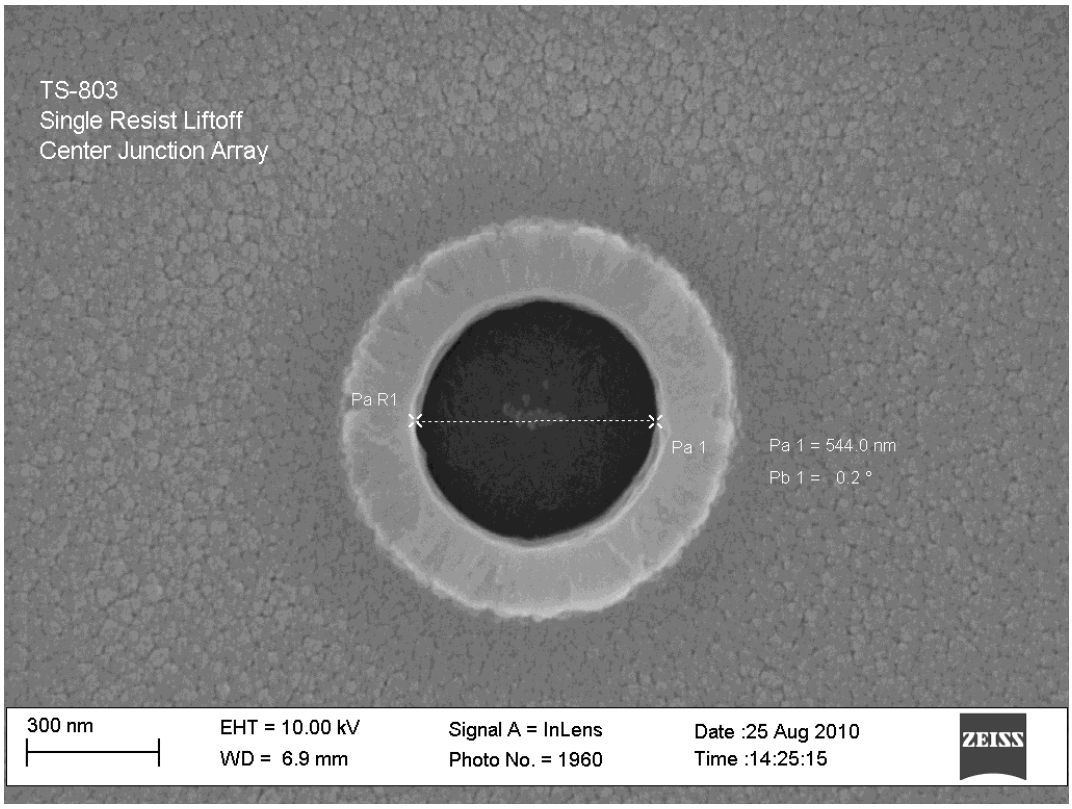


Figure 2.3: Top Down SEM Image of a Successful Single Resist Liftoff

The next step in this process was to use a silicon wafer with sputtered niobium (170nm) and gold (25nm) to simulate a trilayer wafer with a gold overlayer. The same NFR + nLOF 2020 resists were spun onto the wafer as before. Using a scanning electron microscope allowed measurement of the cross sectional diameter of the photolithography defining the critical resist junctions, both at the top and bottom of the feature and also qualitatively observe the structure of the resist junctions. This was informative in that using a negative resist with suitable exposure and sufficient over-development, a taper that starts with a wider top of the cylindrical structure and ends at a narrower bottom which allows for ease in liftoff is expected. Figures 2.4 and 2.5 are SEM images that show this tapered effect for all sizes of resist junction lithography with the smallest ones exhibiting excessive overdevelopment for their bake and exposure combination. The taper also affects the ability to seal the junctions and to liftoff the resist in future steps and can be adjusted by varying the resist thickness with spin speed, exposure duration, resist bake duration, development duration and nLOF resist thickness series. It is important to also add that the resist profile/taper has an important role in the junction etch process, as will be discussed later in this chapter. These resist SEM images before SiO_x deposition and liftoff also serve as a starting point to visually compare how the single resist looks before the various etches and liftoff processes performed later in this chapter.

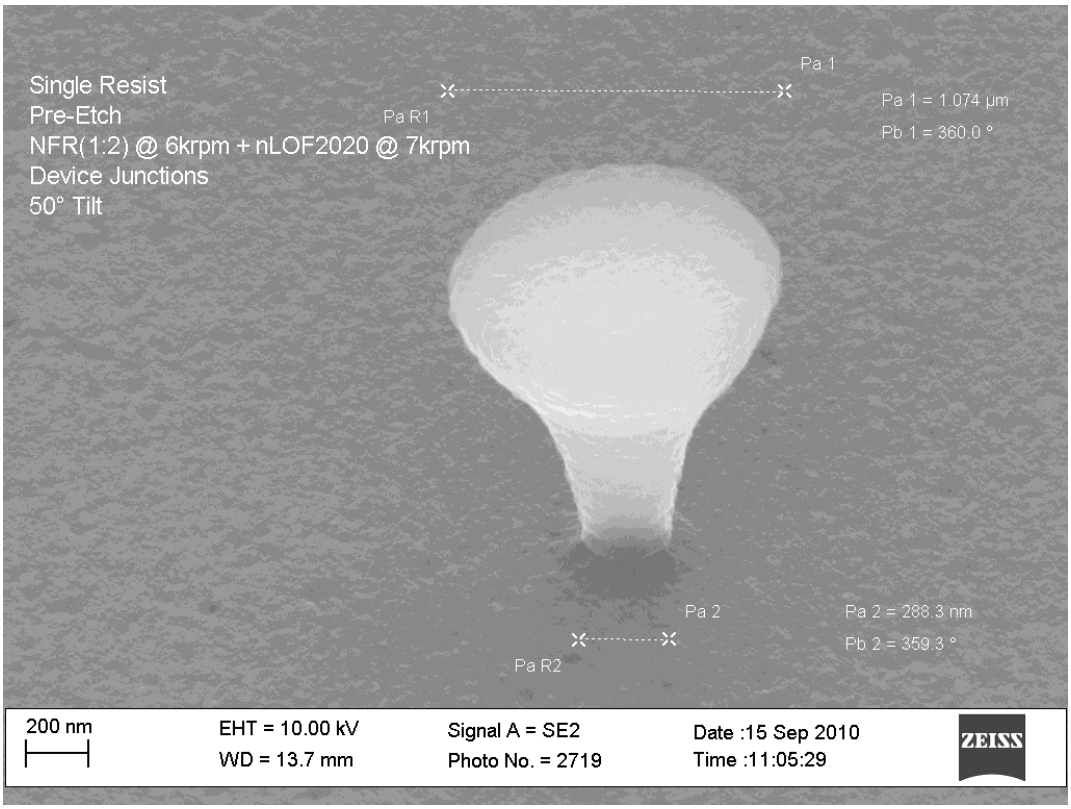


Figure 2.4: SEM Image of a Single Resist Process on Test Trilayer

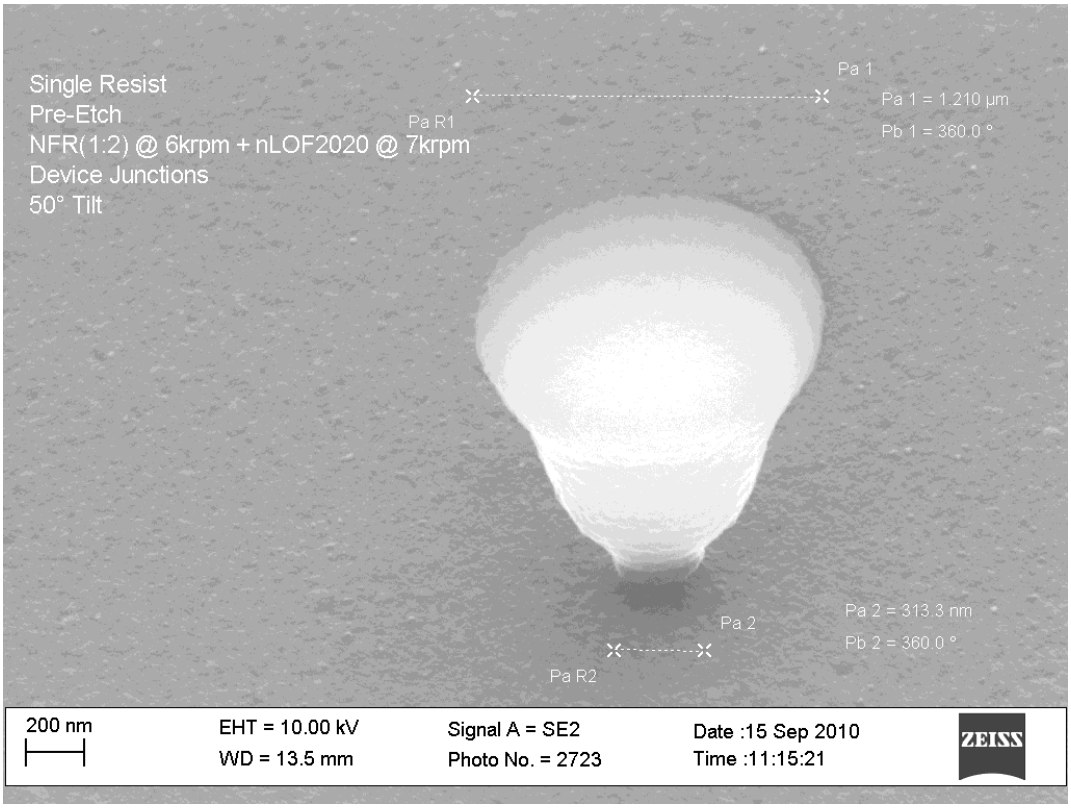


Figure 2.5: SEM Image of a Single Resist Process on Test Trilayer

This same silicon wafer with sputtered niobium and gold overlayer and single resist structures was then used to determine if the gold overlayer could be etched without damage to the resist buttons defining the device junctions. An iodine-based wet etch (HG-800) was initially proposed. A previous trilevel resist process was able to realize 2um sized junctions with a gold wet etch, but used a Cr-Au over layer which wet etches more uniformly than pure gold. The Cr-Au material was subsequently replaced with a gold target during the development of the Pentalevel junction process because of micro masking affects due to the chromium in the dry etch of the Pentalevel process. In the interest of being thorough, a gold wet etch approach was attempted, but the etch completely removed the smaller junction resist buttons. Previous attempts to improve the wet etch for use with etching the gold overlayer included UV hardening of the resist after patterning (though this makes liftoff less likely to succeed) and varying of the gold wet etch chemistry by diluting the solution and decreasing its ethanol content; however, such methods again failed to create any substantial improvements. A gold wet etch approach was therefore abandoned.

Next, a physical etch of the gold overlayer was performed using a sputter etch in a parallel plate Axic RIE. In this tool, a physical bombardment of argon atoms was used to etch the top gold layer using the same resists and patterning as the previous experiment. This method is currently used to etch the gold overlayer with the Pentalevel process. Our results revealed an etched profile that for the most part followed the top of the resist structure and not the resist feature size at the wafer surface. The gold directly underneath the top of the resist, however, looked to be tapered and 'chewed up' on the perimeter

leading to potential damage to the junction itself. Gold was also backsputtered onto the resist, leaving a thin gold film conforming to the resist sidewalls. This thin gold side layer is a concern in that it may make liftoff difficult or create additional 'wing' artifacts and debris when the resist structure is removed during liftoff. The test wafers that experienced the gold dry etch were then diode sputtered with 300nm of SiO_x, a worst-case thickness scenario, then placed in NMP for liftoff of the nLOF 2020 resist. The remaining NFR was removed with an oxygen ash and the resulting SEM images show successful liftoff of the resist with resist opening diameters of ~300nm in Figures 2.6 and 2.7. While the gold sputter etch did not damage or harden the nLOF resist enough to prevent it from lifting off, the inner region of the SiO_x (immediately surrounding what would be the junction) that is responsible for sealing the junctions is malformed exhibiting a thin cylindrical ring or shell around the perimeter of the opening, rising above the height of the deposited SiO_x as seen in Figure 2.7. This raised cylindrical shell is believed to be from interaction between the resist sidewalls, backsputtered gold onto the resist column and deposited SiO_x where some combination of this material matrix remains after liftoff.

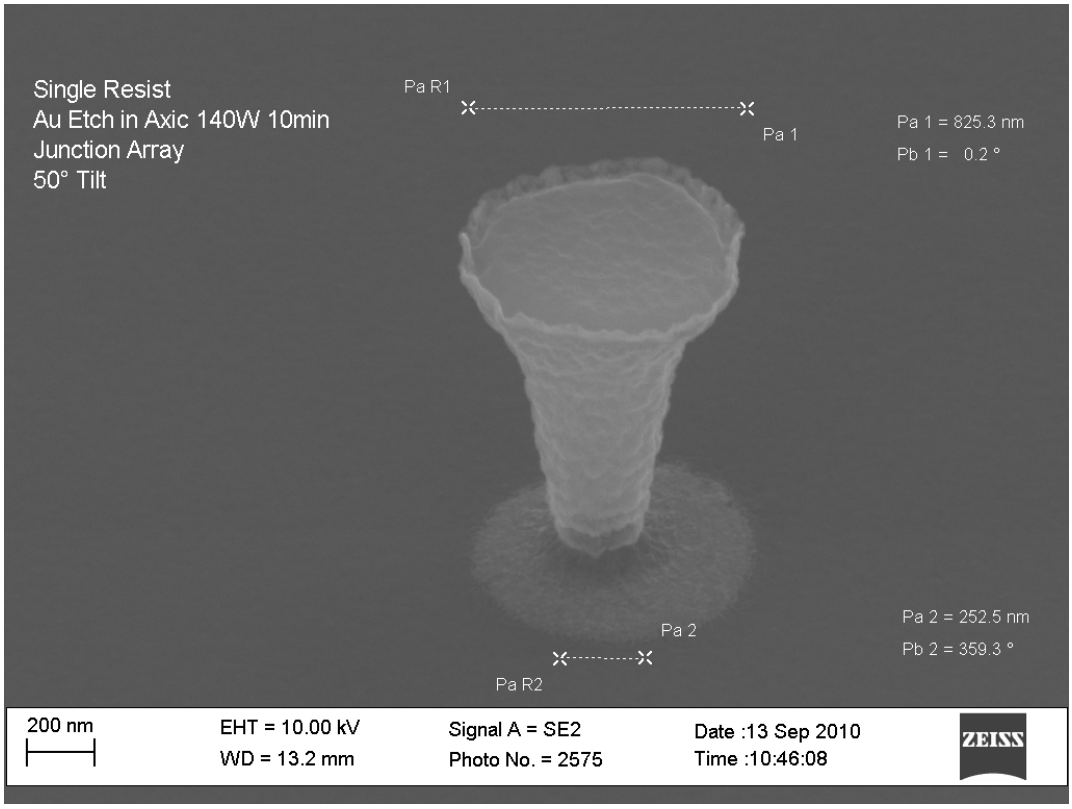


Figure 2.6: Single Resist SEM After Gold Sputter Etch with Backsputtered Gold

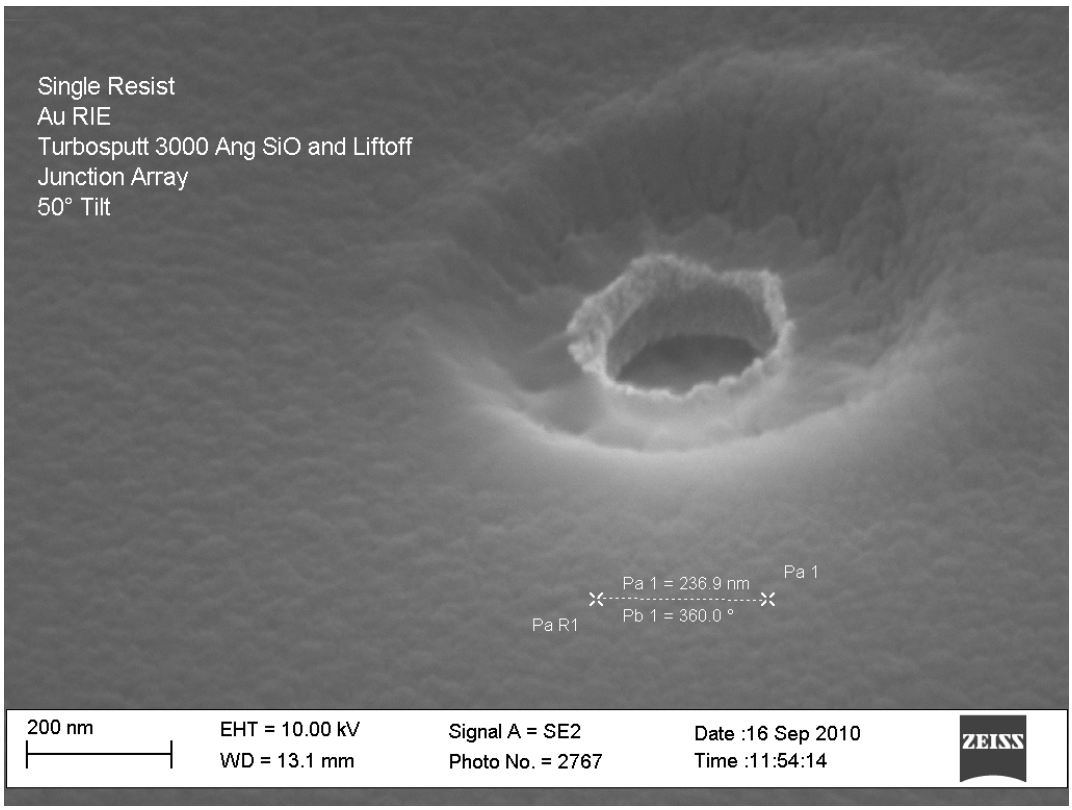


Figure 2.7: Single Resist SEM After Gold Sputter Etch, SiO_x Deposition, and Liftoff

While these results are encouraging, the non-optimal gold etching and the cylindrical shell artifacts are not acceptable for an actual junction process. It was suspected that these aspects of the process were due, at least in part, to the overly exaggerated overhand profile of the resist where the bottom profile of the resist is much smaller than required. Improving this resist profile to obtain a more modest undercut profile was therefore desired. Additionally, the inclusion of the niobium junction etch step into these tests was also needed to more fully test out this single resist process.

The next experiment was therefore set up to evaluate how the single resist would also hold up to the M2 niobium RIE etch (Oxford Instruments Plasmalab-100) used in etching the counter electrode underneath the gold overlayer. An nLOF 2035 resist was used instead of the nLOF 2020 resist to see how a thicker single resist would hold up in the RIE processing with the N10 (Band 6) junction mask on a Si/SiO_2 wafer with 200nm of niobium. An SF_6 + Ar recipe was used with an RF power of 30W and 50W. SEM images below show that with the 30W etch, the resulting M2 etched button follows the bottom of the resist, while with the 50W etch, the M2 perimeter corresponds to the top of the resist.

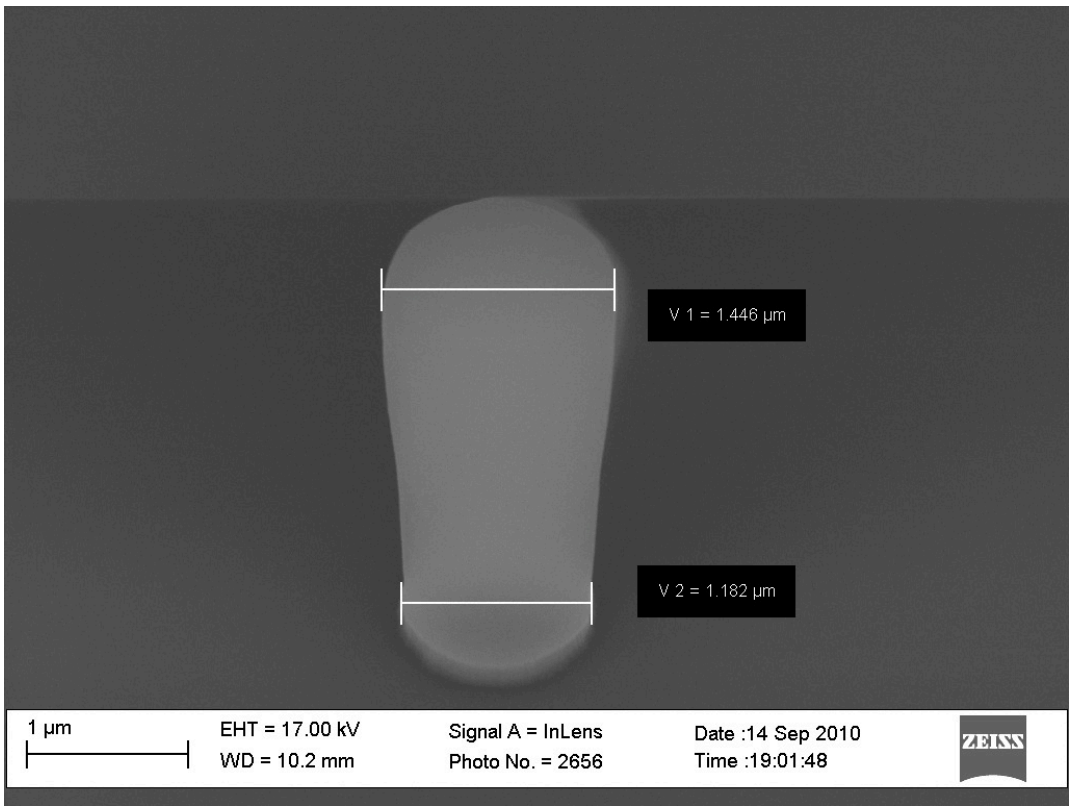


Figure 2.8: Single Resist SEM After 30W Niobium RIE

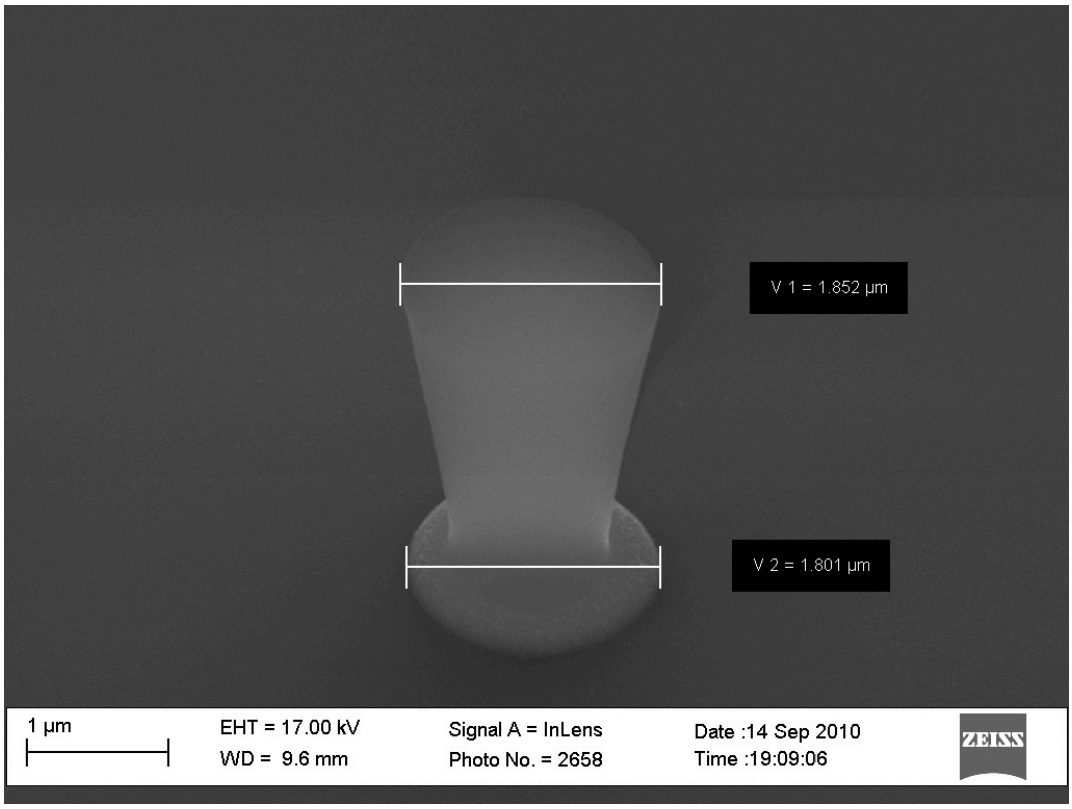


Figure 2.9: Single Resist SEM After 50W Niobium RIE

For a non gold-overlayer process, a niobium etch that follows the perimeter of the top of the resist, without damaging the exposed niobium below the resist structure, will allow the later SiO_x deposition to better insulate and properly seal the junction, contacting not only the sidewall of the niobium junction but covering part of the top perimeter surface as well. For gold overlayer processes, where size of the argon RIE defined gold button typically follows the diameter of the top of the resist (e.g. Quadlevel and Pentalevel resists), the subsequent M2 etched button follows the perimeter of the immediately overlying gold button, even with a 30W niobium etch.

Then the gold sputter etch and the niobium RIE were combined, using a new version of the nLOF resist series (nLOF 5510) that was specifically designed to realize sub-micron liftoff resist structures. The NFR/nLOF-5510 bilayer was patterned and then followed by a gold etch in the Axic RIE tool and then finally received a 30W niobium RIE in the Oxford system using the SF_6 + Ar chemistry (electing to use the same 30W niobium RIE conditions used in the Pentalevel junction process). SEM images in Figures 2.10 through 2.12 show a junction element after lithography, niobium etching and liftoff. Figure 2.11, which is an SEM after niobium etching, appears to show a well-formed gold button that roughly follows the diameter of the top of the resist, with the niobium button slightly undercut with respect to the gold perimeter. Also evident in this SEM is the backsputtering of a gold shell onto the sidewall of the resist as well as the extension of this back-sputtered shell above the full height of the resist. However, Figure 2.12, taken after SiO_x liftoff, shows a misshapen gold pad that is smaller in diameter than the niobium button and is physically abraded, particularly at its perimeter. This is in great contrast to the result of argon etching of gold in the Pentalevel process. Looking back at Fig 2.11 (after niobium etching) it is possible that the sidewalls of the niobium in the niobium etch not only undercut the gold button, but that the etch also progressed further toward the center of the junction between the interface of the Nb/Au bilayer. This would leave the perimeter of the gold button unsupported, causing this region of it to crumble during liftoff, leaving the misshapen gold pad. It is also possible that the Argon etch was less anisotropic as believed with this resist, thinning the gold layer under the 'shadow' of the resist overhang. Figure 2.12 also shows that the SiO_x after liftoff did not overlap the top of the M2 electrode, along the perimeter, at all. It is not even clear if the SiO_x sufficiently seals against the sidewall of the M2 niobium junction button to prevent electrical shorting of a subsequent M3 electrode to the M1/Al layer.

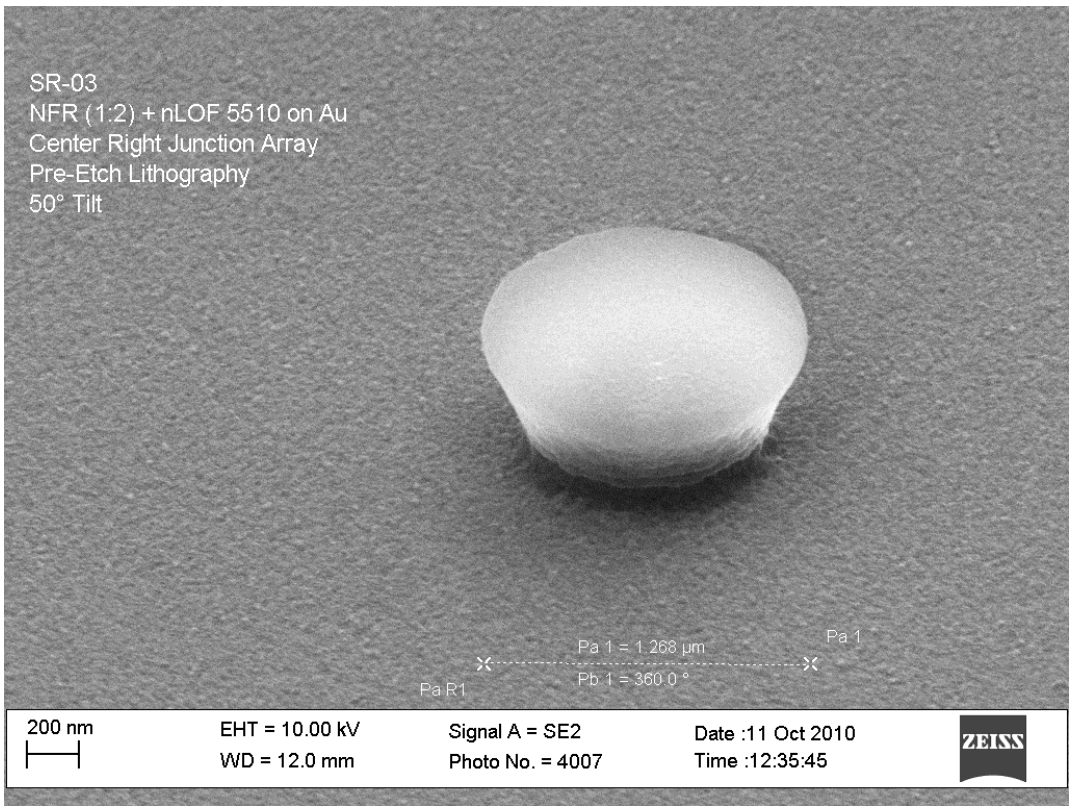


Figure 2.10: Single Resist SEM on Gold Surface Before Etching

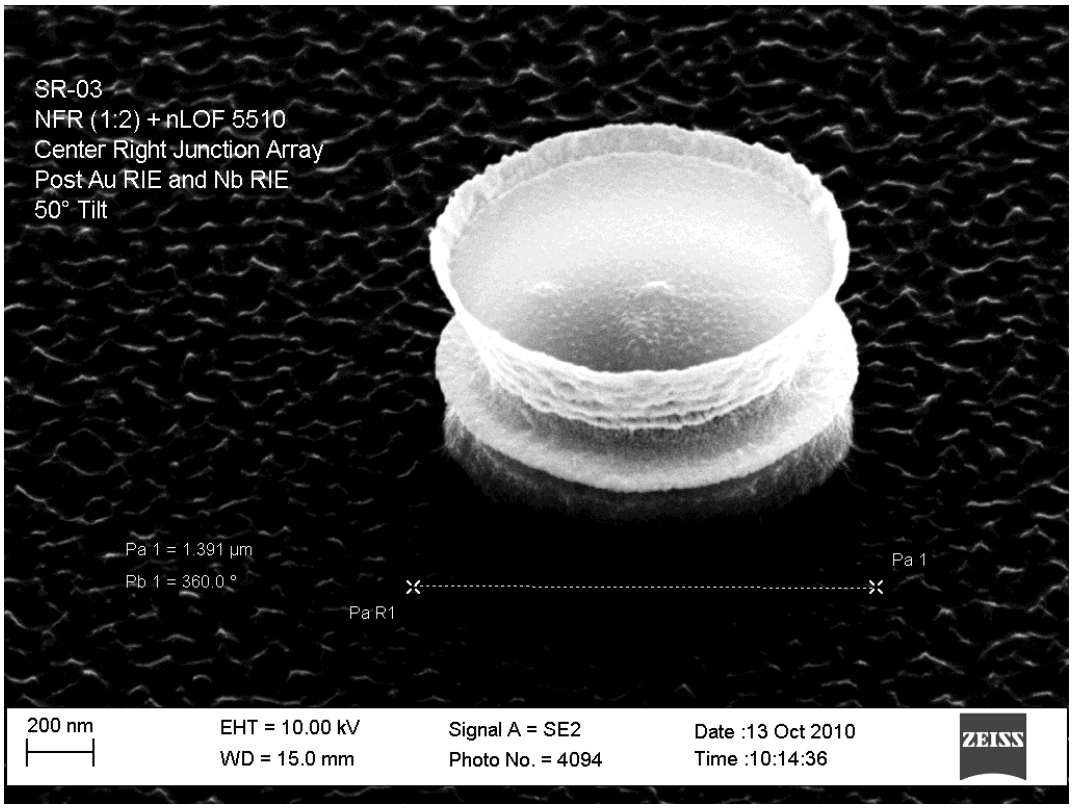


Figure 2.11: Single Resist SEM After Gold Sputter Etch and Niobium RIE

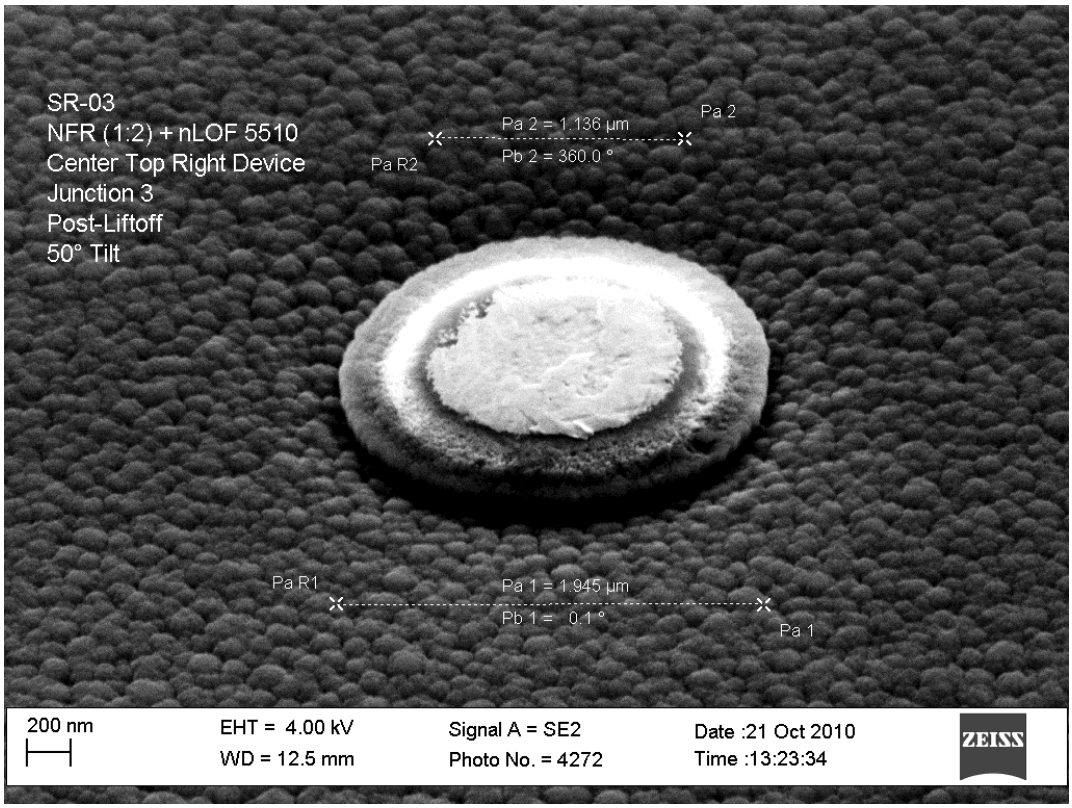


Figure 2.12: Button SEM After SiO_x Deposition and Liftoff

Because of the misshapen definition of the gold pad and the poor SiOx sealing of the junction, it was decided to investigate the use of an ion mill to etch the gold overlayer using an ion gun mounted at 45 degrees in a UVML sputtering tool (Sputt 3). Much earlier work had explored using an ion mill to etch a Cr-Au overlayer with a different single layer resist, but concluded that while effective in etching the gold, it created debris on the wafer surface and hardened the resist too much to liftoff [12]. However, this experiment was repeated using this different nLOF series resist and a gold overlayer material.

To explore the feasibility of an ion milling process, a test was devised using a single resist of nLOF 2020 and a test mask with a junction array to see the effect of the angled ion mill on a variety of different-sized junctions with diameters ranging from 4.0 µm down to 0.5 µm. The sample was heat sunk with Apiezon L-grease to a large metal block to ensure the resist would be reasonably heat sunk during the ion milling. The ion mill was run for 15 minutes at 300V beam voltage. SEM images of the sample show that the exposed gold was successfully removed. Clearly with an angled ion beam the resulting gold button will be quite different than that obtained from the customary normal incidence argon RIE ion flux (where the diameter of the gold button is the same as the largest diameter of the etch mask). One would instead expect the gold bottom to exactly follow the bottom 'foot' of the resist feature. Generally this is the result that was obtained, however as can be seen in Figures 2.13 and 2.14, the junction gold was found to protrude marginally beyond the bottom foot of the resist button after the ion mill. As the ions are impinging on the sample

at 45°, it is believed they are not only etching the gold surface and top of the resist but also the sidewalls of the resist. The leading edge of the etched gold thus slightly trails the receding edge of the resist etch mask.

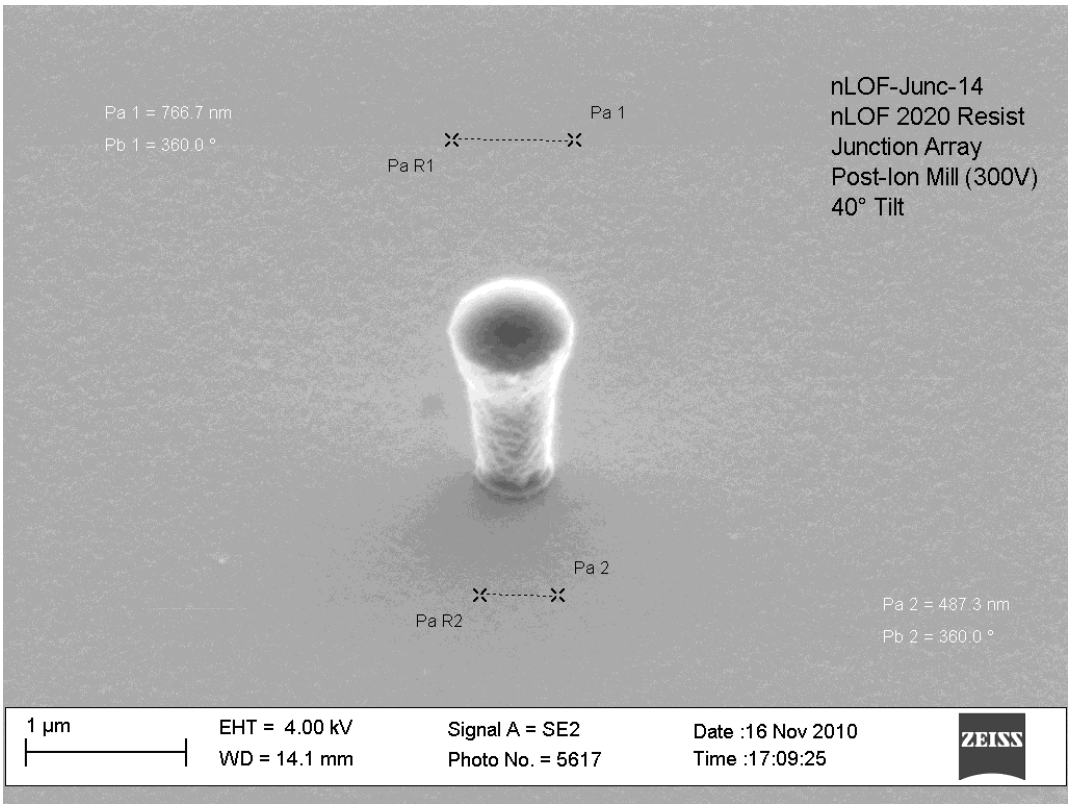


Figure 2.13: Single Resist SEM After Gold 45° Ion Mill

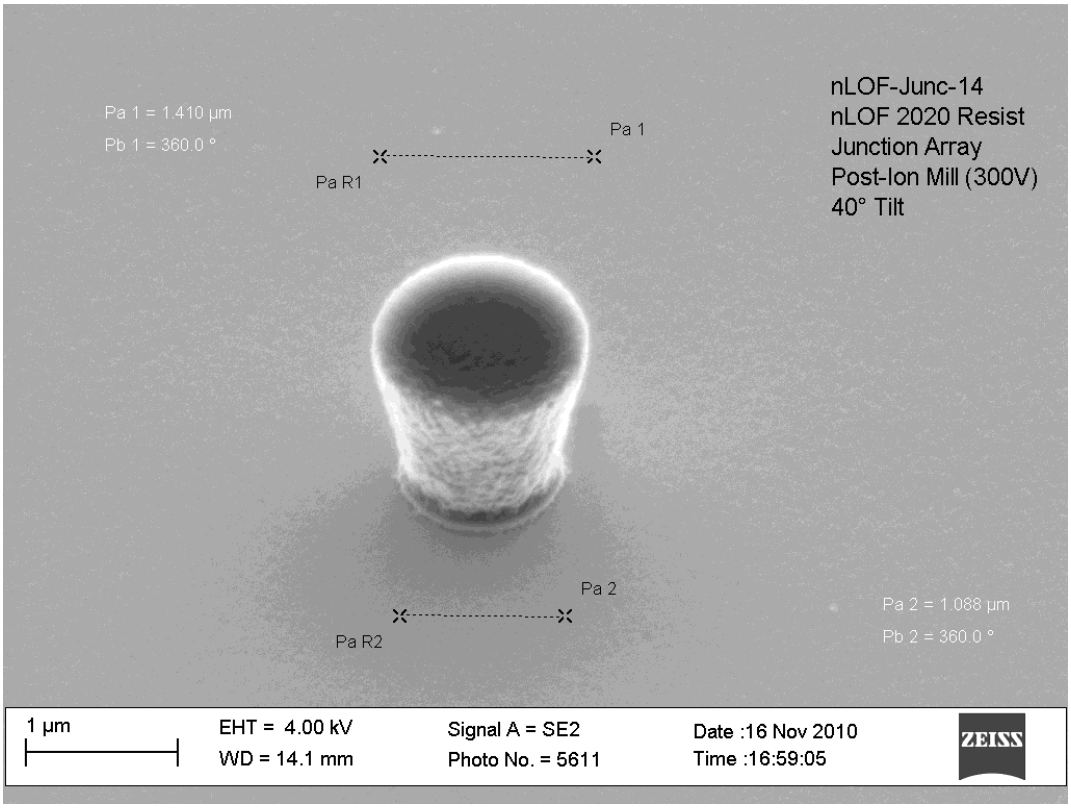


Figure 2.14: Single Resist SEM After Gold 45° Ion Mill

The next step in this process was to evaluate the full single resist process including junction etch and SiO_x deposition and liftoff. If these additional steps could be successfully completed, the single resist process with a gold ion mill could be useful as a replacement for the current Pentalevel process, at least as a faster method for prototyping test devices. The same sample used in the preceding gold ion mill steps (nLOF-junc-14) was processed through the remaining steps. The sample was degreased and loaded into an Oxford Instruments Plasma-100 system on a Si/SiO_2 carrier wafer to perform the necessary M2 junction etch, a niobium RIE at 50W with a SF_6 + Ar chemistry. The SEM images after the niobium etch (Figures 2.15 through 2.16) show that the single resist has held up nicely and the niobium etch nominally followed the top of the resist as discussed previously.

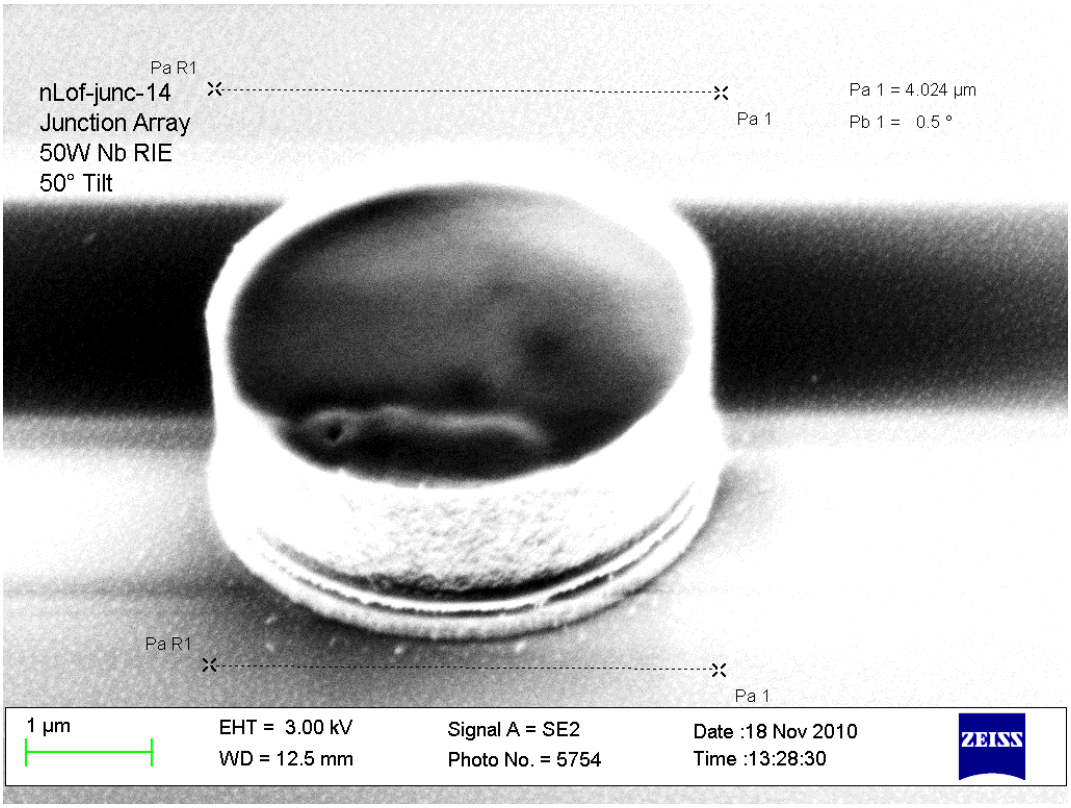


Figure 2.15: Single Resist SEM After Gold Sputter Etch and Niobium RIE

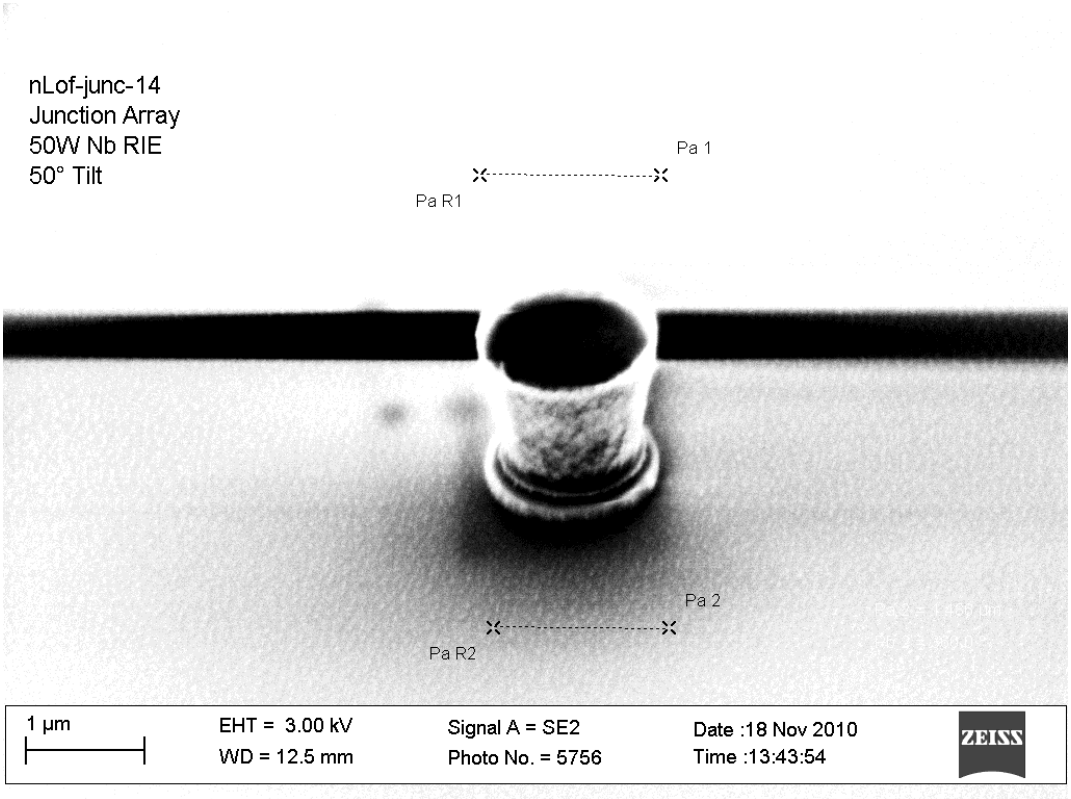


Figure 2.16: Single Resist SEM After Gold Sputter Etch and Niobium RIE

Following the niobium etch, the sample (nLOF-junc-14) was loaded into the diode sputtering chamber for the SiO_x deposition step. As described in a Chapter One, while the use of diode sputtered SiO_x is a new development, it proved to be the best insulation deposition option moving forward. A final concern with developing a single-resist process is that the ion mill and RIE will harden the resist and prevent it from proper liftoff. This was a major setback in earlier experiments [12]. 300nm of SiO_x was deposited on the sample as a worst-case thickness scenario using the diode sputtering tool. Liftoff was performed in a 120°C NMP bath for two hours followed by an oxygen ash to remove any remaining resist and the sample was inspected via SEM.

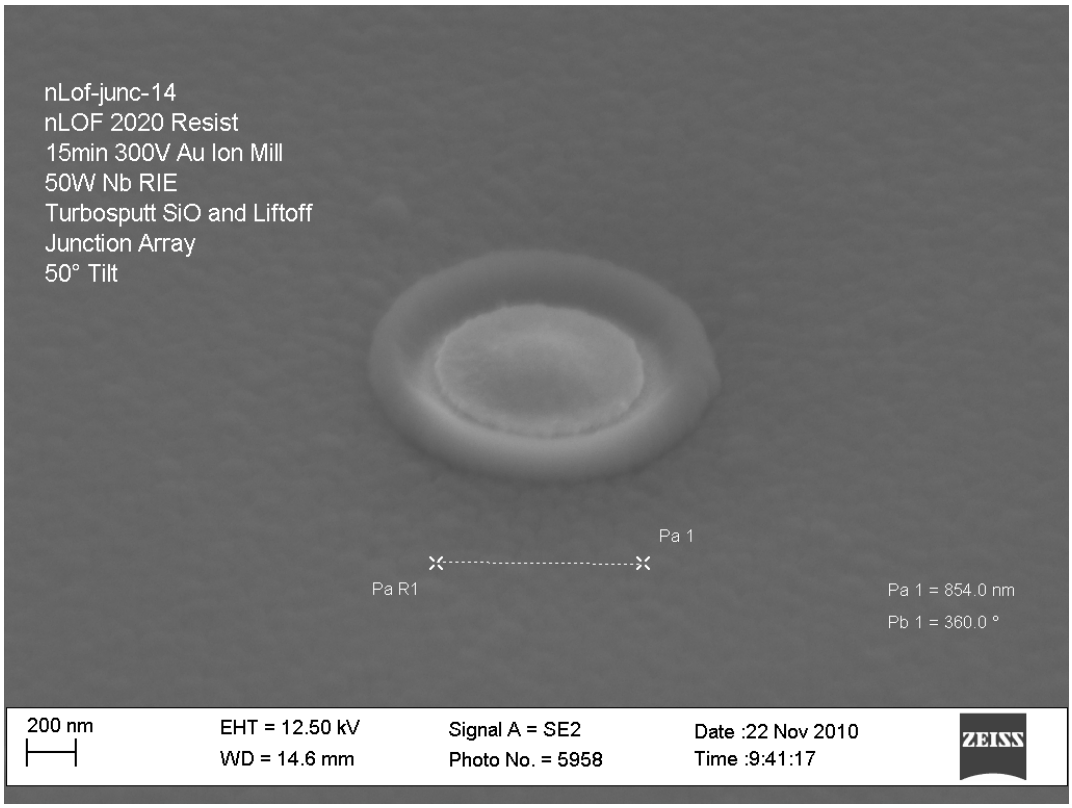


Figure 2.17: SEM Image of Single Resist Liftoff and Sealed Junction

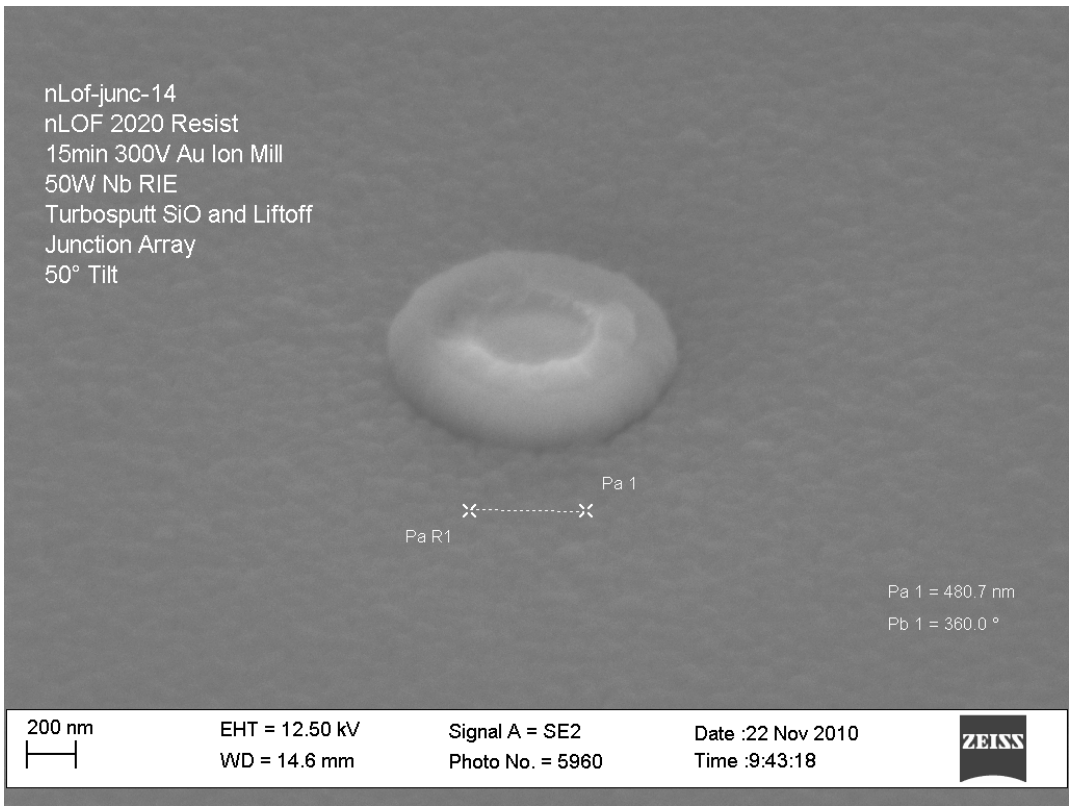


Figure 2.18: SEM Image of Single Resist Liftoff and Low Quality SiO_x

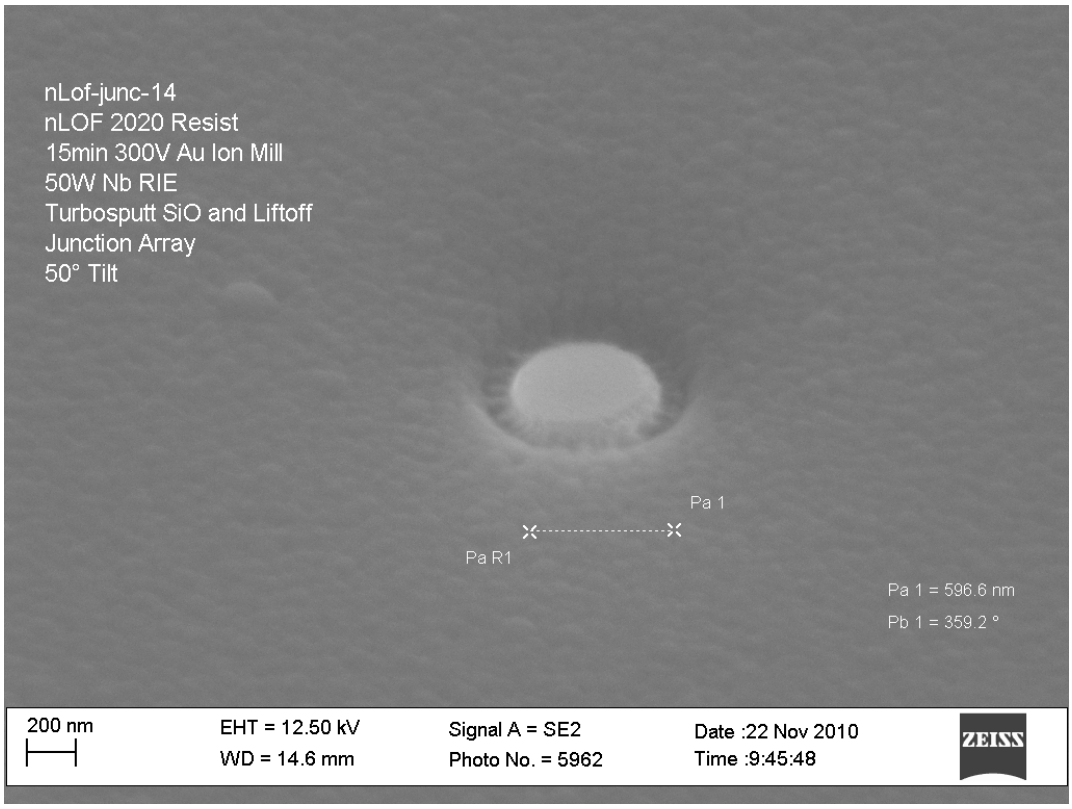


Figure 2.19: SEM Image of Single Resist Liftoff and Missing SiO_x Coverage

Sample images of the wafer after the liftoff process, seen in Figures 2.17 through 2.19, showed atypical SiO_x patterns at the junction sites. Sometimes junctions are obtained that are fully sealed, as is shown in Figure 2.18, where the SiO_x overlaps the perimeter of the gold button. Sometimes an inner ring of insulation is removed, as is shown in Figure 2.17, where the gold button is now fully exposed, but the SiO_x still overlaps the perimeter of the niobium junction button. Both of these results would be acceptable in regards to the SiO_x electrically insulating the junction for the subsequent niobium wiring step. However sometimes the entire fillet of SiO_x is removed, as shown in Figure 2.19, and concerns arise about the quality of the SiO_x film near the junction. It is expected that before liftoff, all the junctions are fully sealed by the SiOx, however during liftoff the junction insulation at the junction sites is sometimes partially or fully removed.

Further SEM imaging showed that all junctions larger than 800nm lost most of the inner ring of SiO_x around the gold button (like in Figure 2.17). Junctions smaller than 800nm typically retained the entire inner ring of SiO_x (like in Figure 2.18). And occasionally junctions of any size would lose all of their insulation, as occurred in Figure 2.19. A theory was developed that the SiO_x deposited around the junction is of inferior quality due to interaction with the resist feature.

The SiO_x immediately surrounding the junction is believed to be of inferior quality and related to the increased roughness of the sidewalls of the resist, caused primarily in the ion-milling step. An additional factor could be that the resist is inadequately hardened and therefore interacts with the initial deposition of SiO_x. This different textured, poorly formed SiO_x comes off more easily during liftoff than the SiO_x that is not interacting with the resist. The smaller junctions typically retained more portions of this SiO_x ring because their size allowed for increased structural integrity. An attempt to use a short oxygen ash after the ion milling step to smooth out the sides of the resist showed no noticeable difference in resist appearance, so the proposed solution to this problem was a higher temperature sample bake after patterning the resist but prior to the ion-milling step to harden the resist sufficiently to prevent it from interacting with the deposited SiO_x. This involved a tradeoff though, as the bake schedule must harden the resist sufficiently to keep the sidewalls from being textured in the ion-milling step while not deforming the resist profile or hardening the resist too much to prevent successful liftoff in the subsequent steps.

After some experimentation, a 160° C, 5 minute hot plate bake before the ion-milling step was added to the process flow. SEM images (Figure 2.20 below) after the gold ion mill and niobium RIE steps, showed the resist qualitatively looks much smoother than before (Figures 2.13, 2.14 above). The sample next had a sputter deposition of SiO_x and liftoff of the single resist structures. The resulting junction buttons was improved over earlier attempts, as shown in Figures 2.20 through 2.22, with no fillets of SiO_x missing. This sample bake schedule was found experimentally to acceptably harden the resist to keep it from interfering with the SiO_x deposition while still allowing resist/SiO_x liftoff after processing.

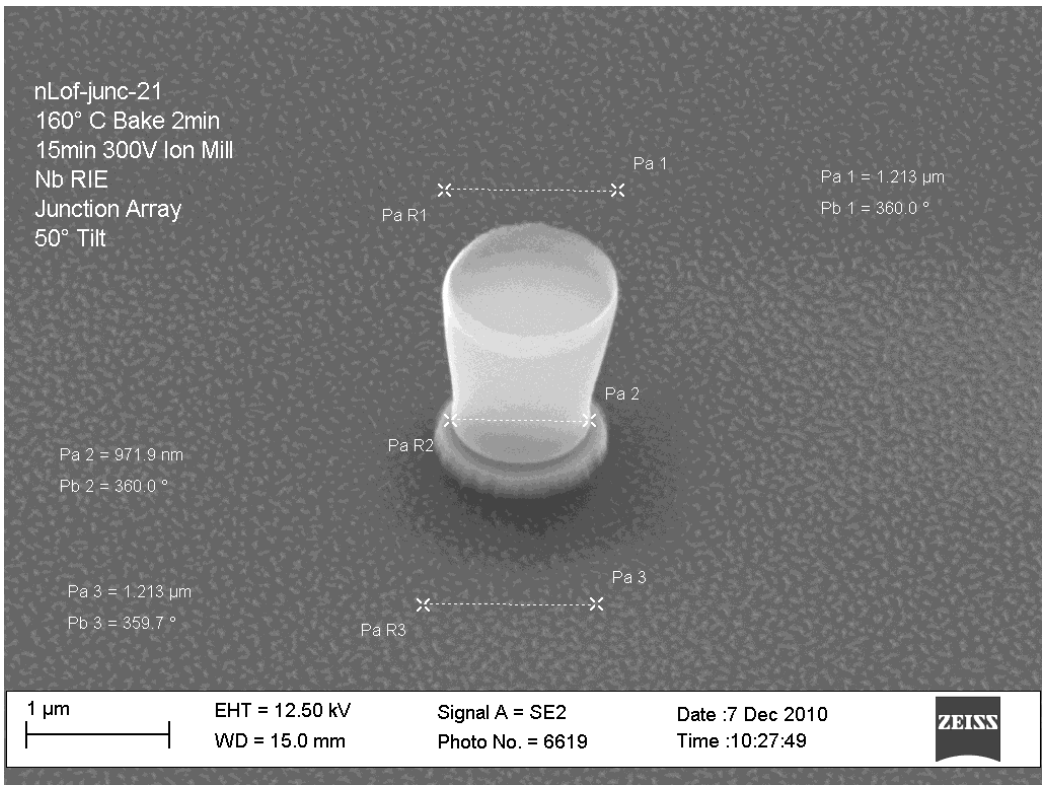


Figure 2.20: Single Resist SEM with Extra Bake Followed by an Ion Mill and Niobium RIE

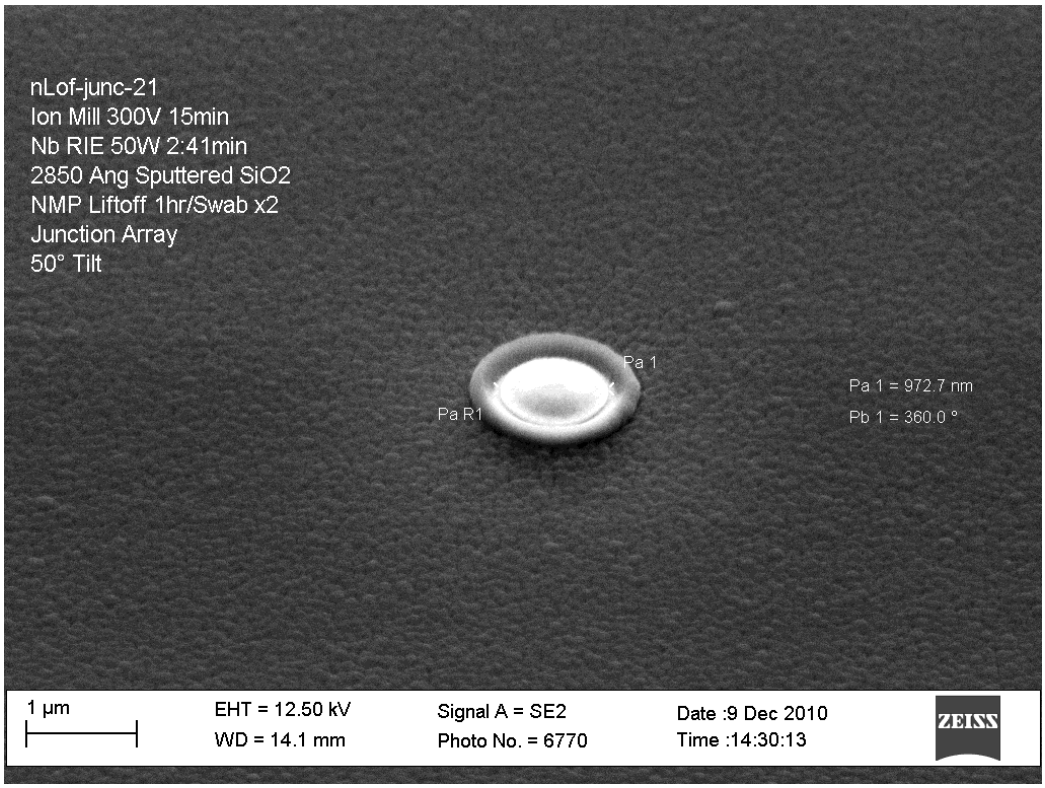


Figure 2.21: Junction Button SEM After SiO_x Deposition and Liftoff

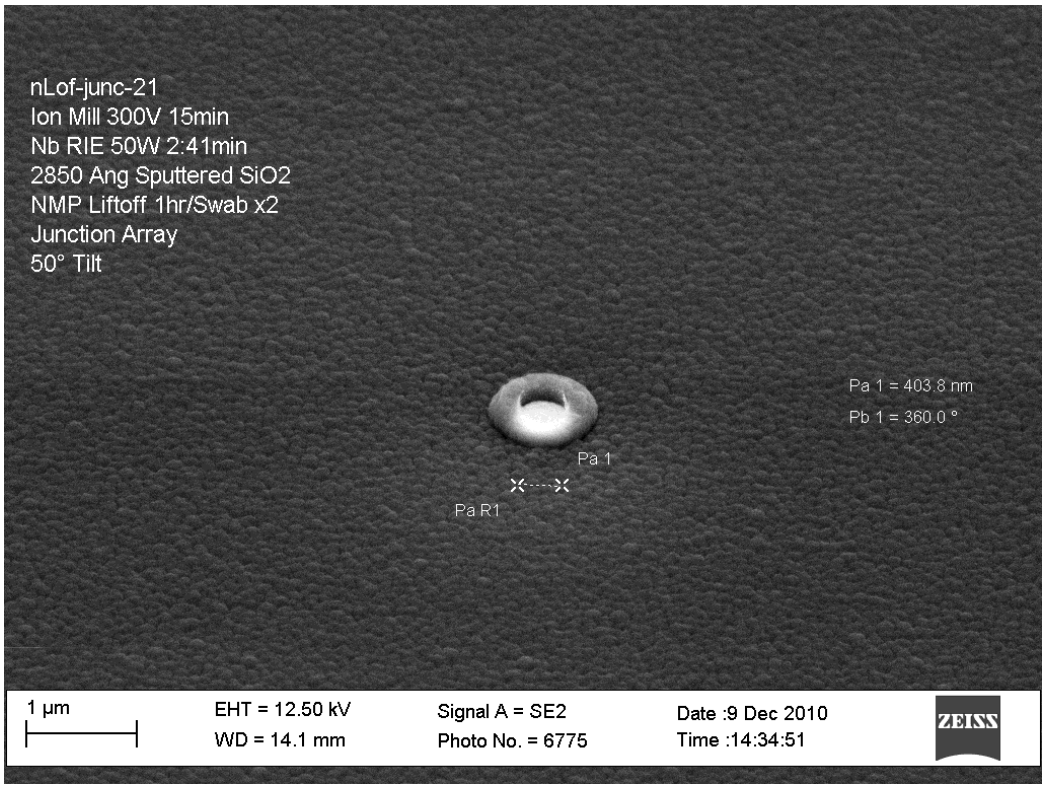


Figure 2.22: Junction Button SEM After SiO_x Deposition and Liftoff

Taking all of these process developments, Mike Cyberey was able to use a real trilayer wafer (T3-588) of Nb/Al-AlN/Nb/Au to create test junctions with the single resist process. Figures 2.23 through 2.25 show the junctions through the processing stages with Figure 2.25 showing a sealed junction with the SiO_x around the junction fully intact.

Upon completion of the device processing for this wafer, the electrical quality of the junction was electrically tested using a dip testing method. Figure 2.26 below shows the I-V characteristics of a junction with a critical current of 4kA/cm^2. This single resist process was able to create junctions > 1.5µm diameter with proper electrical results and is therefore a feasible option for creating test SIS junctions for prototyping applications. However, smaller area junctions generally did not results in acceptable SIS characteristics. Our best explanation for why single resist processing worked now after being abandoned for a multi-layer resist process before can be attributed to the photoresists used in processing. The current process succeeds using a negative resist, optimized for high temperature use and liftoff, whereas the single resist used in the past was a resist modified with a chlorobenzene dip to create an overhang preferable for liftoff [7].

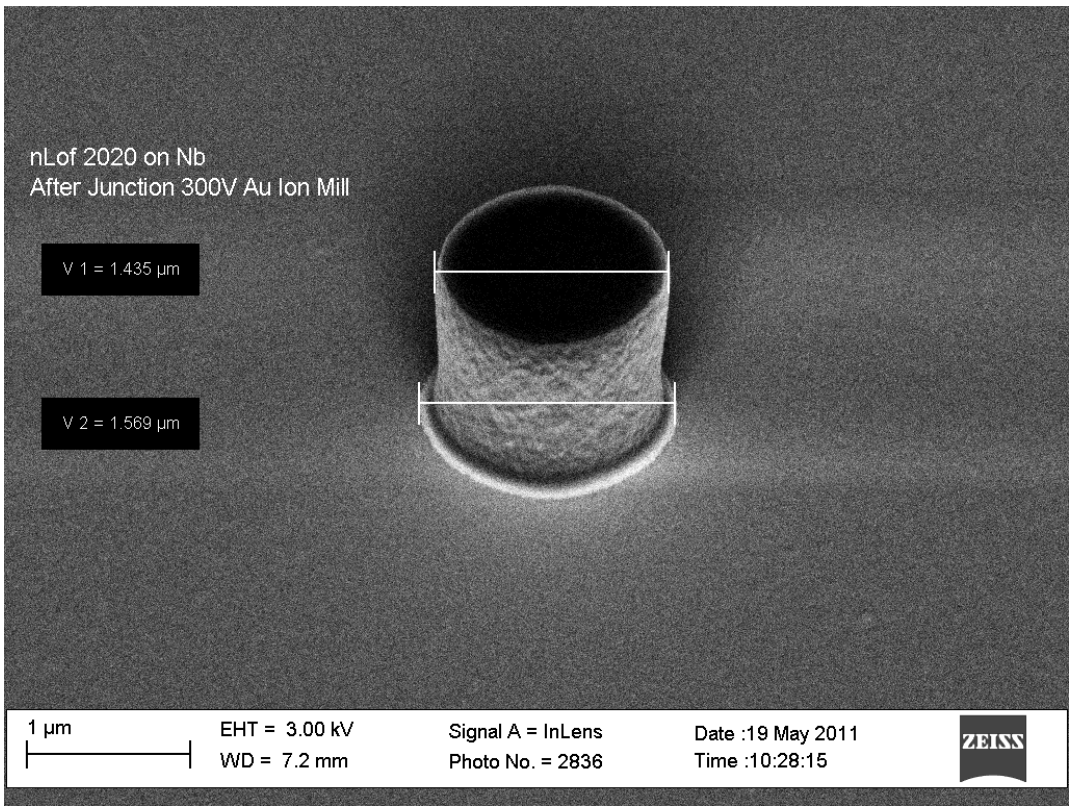


Figure 2.23: T3-588 Single Resist SEM After Gold Ion Mill

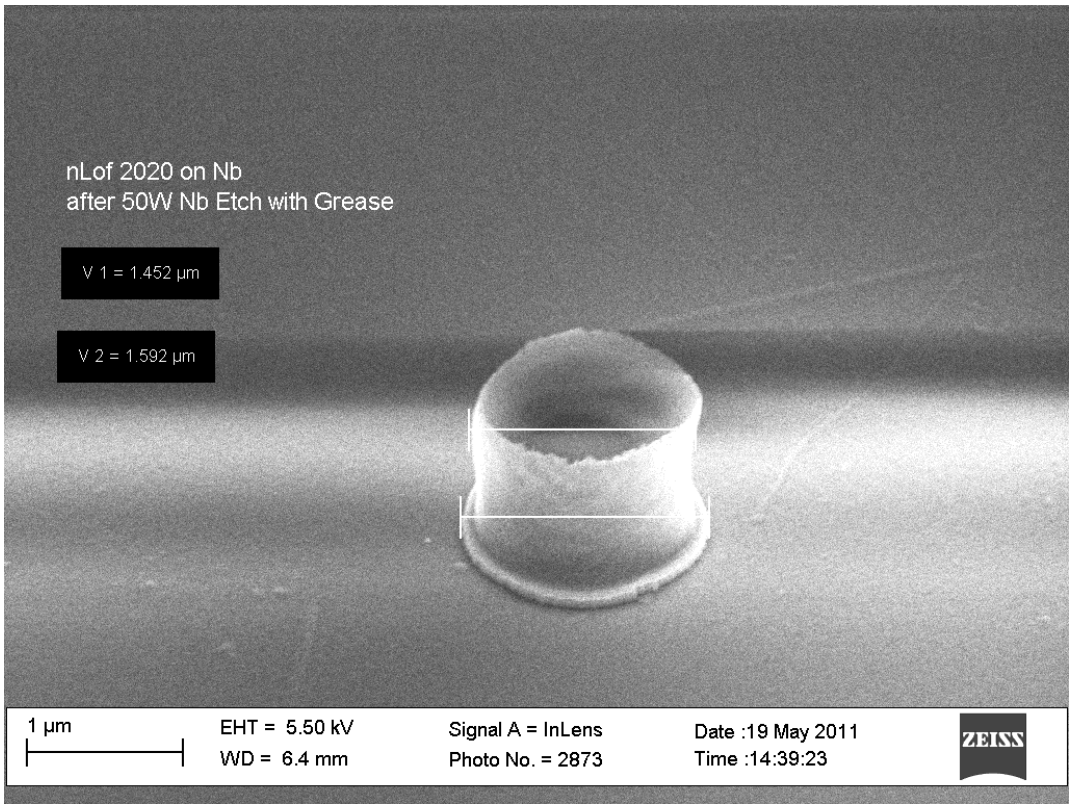


Figure 2.24: T3-588 Single Resist SEM After 50W Niobium RIE

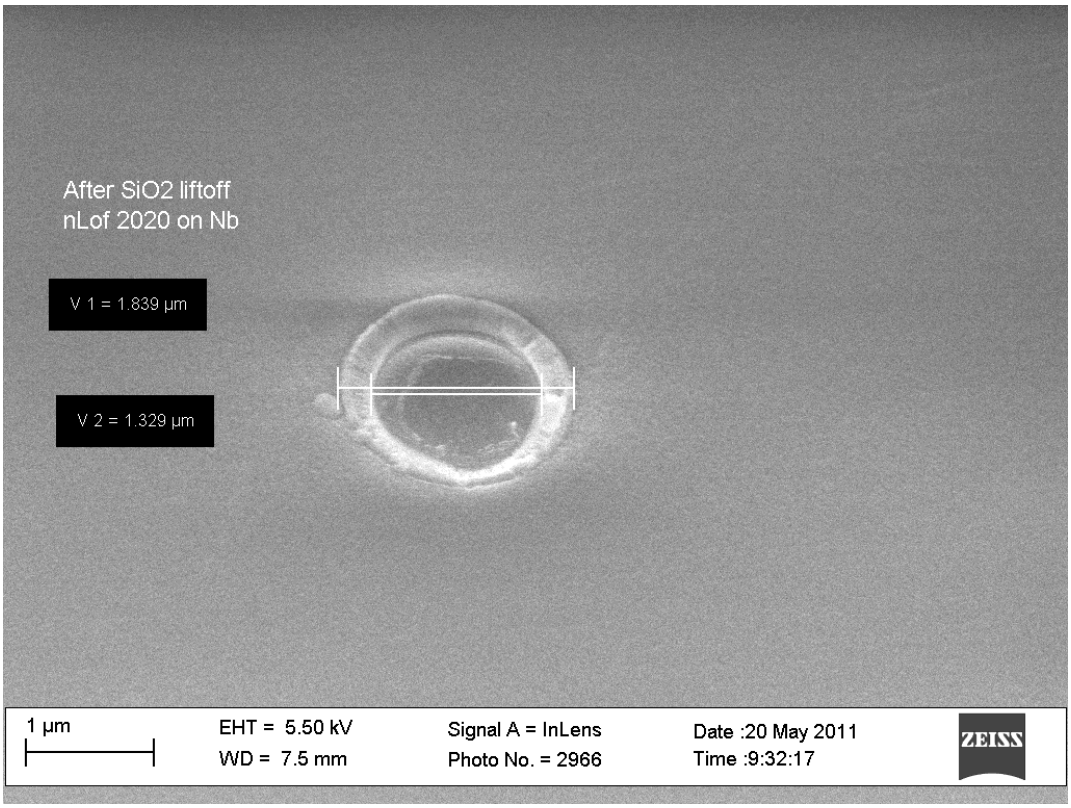


Figure 2.25: T3-588 Junction SEM After SiO_x Sputter Deposition and Liftoff

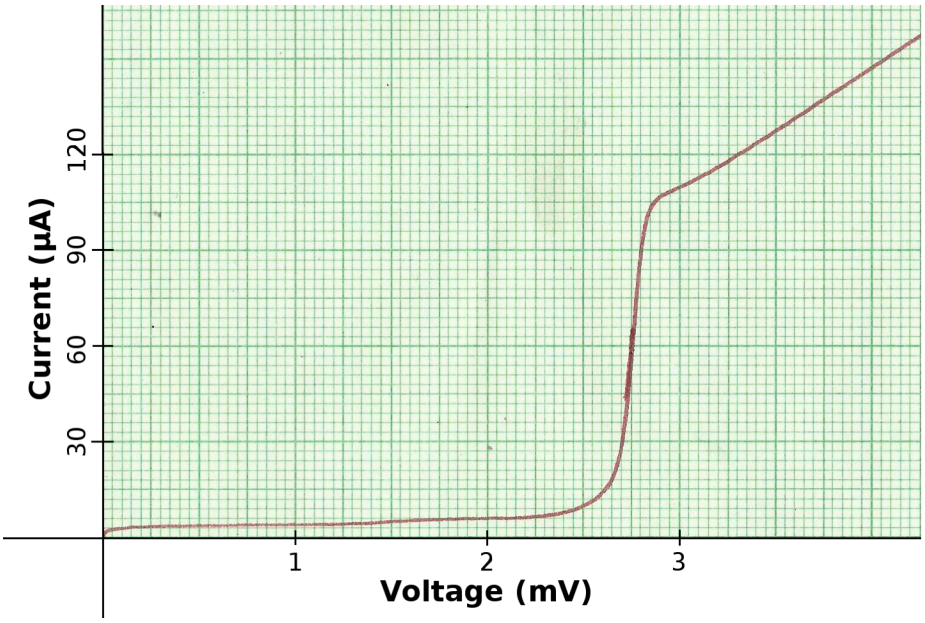


Figure 2.26: T3-588 I-V Curve

The question of why elements smaller than ~1.5µm have resistive or point contact electrical characteristics remains unsolved at this time. One possible explanation may be related to the niobium M2 junction being defined by the top of the resist profile that

overhangs the M2 electrode in space. With the Pentalevel process, a gold button is defined by the SiO_2/Cr top of the Pentalevel structure that overhangs/shadows the gold electrode. The entire surface of the resulting niobium M2 junction button is in turn masked/defined by the gold button that resides physically immediately on top of the M2 electrode. In contrast, for the single resist process, during the niobium M2 RIE, low energy ions can come in contact with the ring of niobium not covered by gold, on the surface of the junction electrode. The gold button is smaller than the final M2 junction size because the angled ion beam defines the gold button. A closer look at Figure 2.9 suggests that this exposed surface ring of niobium is actually rounded at the edge of the button. This could plausibly result in a perimeter ring of niobium with deteriorated superconducting quality. This effect would be more pronounced for smaller junctions where the relative ring area to total junction area ratio increases. Further resolution of this problem is beyond the constraints of this master's thesis, however below we have highlighted some areas for future work to improve this process.

One aspect that may have a significant impact is the choice of thickness of the gold overlayer, currently at 30nm. If this layer can be made thinner, it may be possible to realize a successful argon sputter etch process (similar to the Pentalevel process, and discussed earlier in this chapter) with decreased back sputtering of material against the sidewalls of the resist (using a thinner resist may also help realize a more anisotropic sputter etch). Such an argon RIE approach would avoid the exposed ring of surface niobium in the present angled ion-mill approach. However, if the gold overlayer is too thin, niobium oxides will form below the gold overlayer and interfere with the electrical connections of the SIS junctions, leading to poor device characteristics. XPS measurements of the wafer surface would be a useful tool to determine the presence of these niobium oxides. Other groups have reported using gold overlayer thicknesses as small as 15nm for other device types [16-18].

One could also conceive a return to a non-gold overlayer process, given the potentially more robust sputtered SiO_x films over the evaporated SiO_x that would be damaged when using an ion mill to clean the niobium oxides off the junction buttons before the M3 wiring deposition. For this approach the lithography should be biased to give as vertical a resist profile as possible. Other improvements to this process could also include optimizing the M2 niobium RIE, using apiezon L-grease for effective heat sinking and varying the temperature of the etch to both ensure an anisotropic etch and to possibly more fully freeze out the effect of low energy fluorine ions on the exposed surface ring of niobium.

Chapter Three: Aerogel Thin Film Insulators

Thin film aerogel is a new technology that has the potential to be used as an embedded thermal and electrical insulating film for microfabricated devices such as microelectrical-mechanical systems (MEMS). Aerogels are created by forming a gel, usually out of silicon dioxide, and removing the water within it while preventing the structure of the gel from collapsing in order to create a micro-porous material that can be composed of up to 99% air with a low density and high surface area [19,20]. Originally developed by Kistler and Caldwell in 1931 [21] and first used as thin films by Prikash, Brinker, and Hurd in 1991 [22], the concept to use thin film aerogels as insulators for MEMS devices was first proposed by Honeywell International who approached Pam Norris about the idea and was supported through a DARPA seedling grant in collaboration between her Mechanical Engineering group at UVA for aerogel creation and device testing, the UVML for microfabrication, and Honeywell who provided technical insight as well as performing their own separate microfabrication and testing.

The interest in using thin film aerogels for MEMS is fairly straightforward. Many types of MEMS structures including heaters, detectors, and sensors require electrical and thermal isolation. Currently, the best-known technology to provide thermal isolation for MEMS involves a combination of vacuum-sealing individual circuits after processing to prevent thermal convection and the use of nitride diaphragms suspended above the substrate to reduce conduction of heat. This method has found many applications in industry, however, using a nitride diaphragm has its drawbacks: the silicon pillars etched and designed to support the nitride membranes act as heat sinks, providing a pathway for heat to escape the system and an uneven temperature distribution across the device. Minimizing the number of support pillars is desirable, but this limits the size of the device that can be supported by the nitride diaphragm to no larger than 1mm for acceptable operation since the larger the device, the more mechanical support the diaphragm needs and the more pillars that are required. More pillars reduces the benefits of suspending the device on such a membrane [19].

A surface aerogel thin film architecture could meet or exceed the performance of nitride diaphragms by providing a continuous film with the potential of a lower thermal conductance than nitride diaphragms [19], since bulk (not thin film) aerogel has been shown to have a thermal conductance that is an order of magnitude less than air [20]. Such a device would also have a more uniform temperature distribution, could support larger MEMS structures and could still be vacuum-sealed to prevent convection if needed. Uses for aerogel thin films as electrical insulators would also be of interest as the electrical insulation provided by these films would be unique should the limitations of device processing with aerogels be overcome.

Utilizing this material to its fullest extent requires modifications to the means in which the aerogel is created and applied as well as to the processing methods used to build MEMS devices around it. The former research was undertaken by Casey Bauer who was able to

fabricate different aerogels for testing with modifications of previous aerogel processing techniques. The latter was the focus of this thesis's work in the UVML. The challenge in incorporating aerogel into MEMS fabrication processes comes from the fragility of a material that is comprised almost entirely of air. This material is sensitive to physical etches and very reactive to certain solvents. Our research therefore initially involved experiments to see what processes were possible with the material and to use that information to develop a method for MEMS construction incorporating aerogels.

Aerogel properties can be tailored to the users needs by modifying their chemical composition, deposition, and drying methods. Multiple aerogels samples were tested in the microfabrication process, each aerogel with different chemistries and drying methods [19]. A processing method for a testing structure could not be developed without having to submerge the sample in deionized water. However, if exposed to water, the aerogel structure would collapse and cease to provide proper insulation if it were not chemically modified to ensure it was hydrophobic [20]. In addition to water, there was a concern that other solvents would also damage the aerogel used for insulation, whether or not the gel was hydrophobic. The first test to see if aerogels could be used in MEMS device processing was to expose bulk aerogel (large monoliths of the gel created not as thin films but allowed to dry in large pieces), to chemicals used in device processing: water, methanol, TCE, photoresist, etc. Figure 3.1 showed that qualitatively there was no interaction between the aerogel and most of the chemicals. However, standard positive AZ photoresists did soak into the bulk aerogel and interact with it. Processing without photoresist would be very difficult, so a thin-film capping layer is necessary to protect the underlying aerogel.

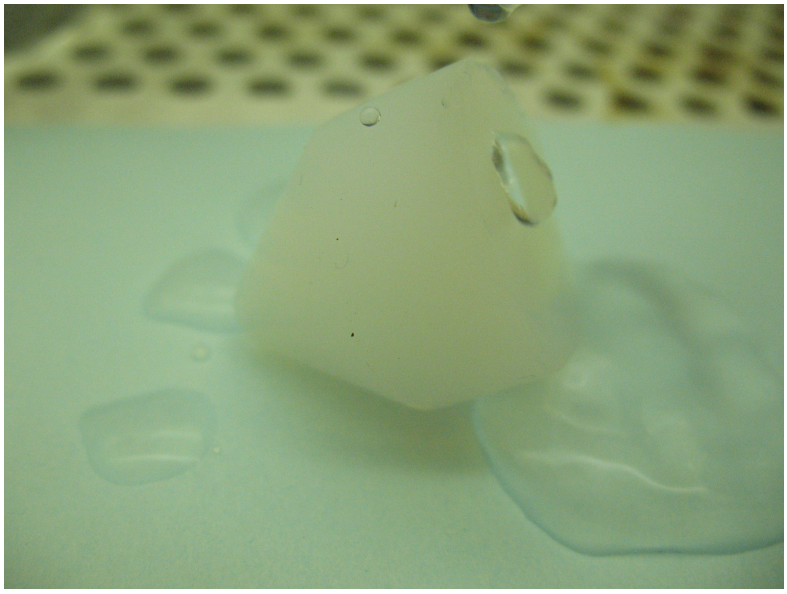


Figure 3.1: Testing Photoresist Developer with Bulk Aerogel

The next step in this investigation was to deposit the aerogel onto the surface of a wafer as a thin film. Dip coating was the most familiar method for the Bauer group and their initial depositions started with a process that would involve mixing the aerogel precursor materials and dipping the wafer into the solution at a set time before the chemicals have

gelled, slowly pulling the wafer out of the solution, and finishing gelling on the wafer surface by letting them dry in the ambient atmosphere or in an overnight chemical wash at elevated temperatures [19]. However, dip coating has significant limitations due to the resulting uneven aerogel film thickness and the aerogel being deposited on both sides of the wafer [20].

Spin coating was another technique used that closely resembles photoresist spin deposition and was developed to give a deposition technique compatible with MEMS processing. However, solvent evaporation during this process would result in the porous structure of the aerogel collapsing and ruining its insulating properties [19]. To prevent this from occurring in the spin coating process, an ethanol environment had to be maintained in the bowl of the spinning tool. Therefore a method to feed ethanol into the spinning chamber had to be engineered as well as a nitrogen feed into the bottom of the spinning tool near the motor to prevent any possibility of spark from the motor igniting the alcohol-saturated environment. While spinning aerogel thin films itself is not a novel technique [23], the use of an ethanol environment is new and important in our process for creating thin film aerogels. Aerogel thin films spun with this technique overcame the problems presented by dip coating, resulting in uniform thin film aerogels on a single side of the wafer. This spin technique was therefore used for most of our later processes.

Other techniques such as using an optically flat salt tablet as a planarization press to realize an aerogel film of uniform thickness, or using a squeegee to ensure the aerogel covers the wafer and fills any wells were considered, but were not fully explored after the success with the spin deposition of the aerogel.

An initial processing test circuit was selected for this work with an existing mask that requires easily accessible tools for deposition and lithography. The aerogel was deposited on a 50mm diameter silicon wafer with dip coating and sealed with a magnetron sputtered 200nm silicon dioxide capping layer in a custom vacuum chamber. Next, a thin (5-10nm) seed layer of titanium was deposited using a custom four gun off axis dc magnetron sputtering vacuum chamber, immediately followed by a 30nm layer of gold to simulate a metal structure for a MEMS device on top of the aerogel. A simple photolithography process with positive photoresist and an existing mask were used to create a pattern of serpentine lines across the wafer (images). This photoresist protects the desired metal structures during the etching process. A chemical wet etch was selected for its ease of use with gold. The process involves a 45 second etch in an iodine-based solution for the gold, followed by a 15 second etch in a 10:1 buffered hydrofluoric solution (BOE) to remove the titanium layer uncovered by the gold etch. The second etch was a concern as the solution is a known etchant of silicon dioxide and aerogel, but an attempt was made to minimize the time that the SiO_x capping layer was exposed to BOE so that the amount of SiO_x etched would be small compared with the total thickness such that the aerogel underneath would remain intact.

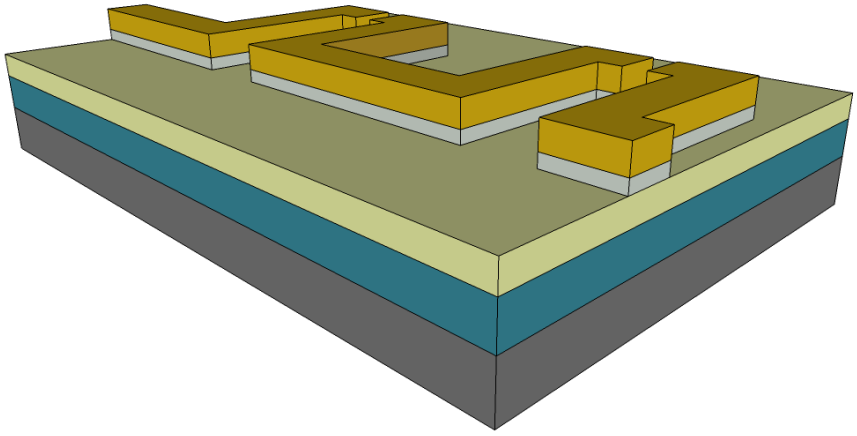


Figure 3.2: Test Pattern Diagram

This etch removed the unpatterned gold and titanium but while watching for an etch completion 'flash' of the titanium, the areas that had SiO_x and aerogel became discolored across portions of the wafer as seen in Figure 3.5. Not all of the aerogel appeared to be affected during this wet etch (Figures 3.3 and 3.4), but significant portions of the wafer were affected.

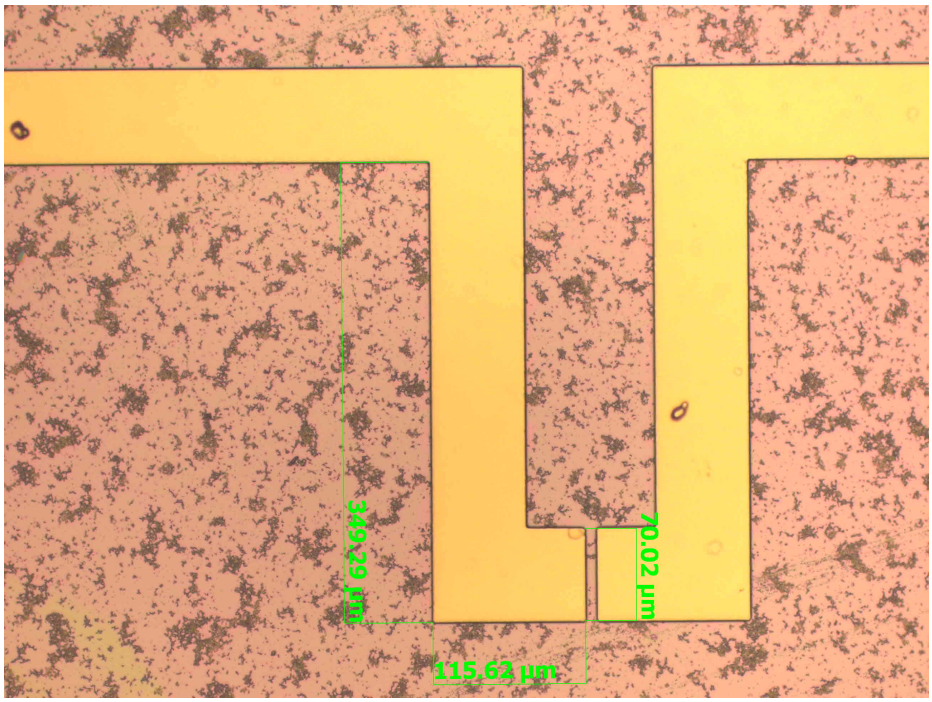


Figure 3.3: Test Pattern Fabrication Optical Microscope Image

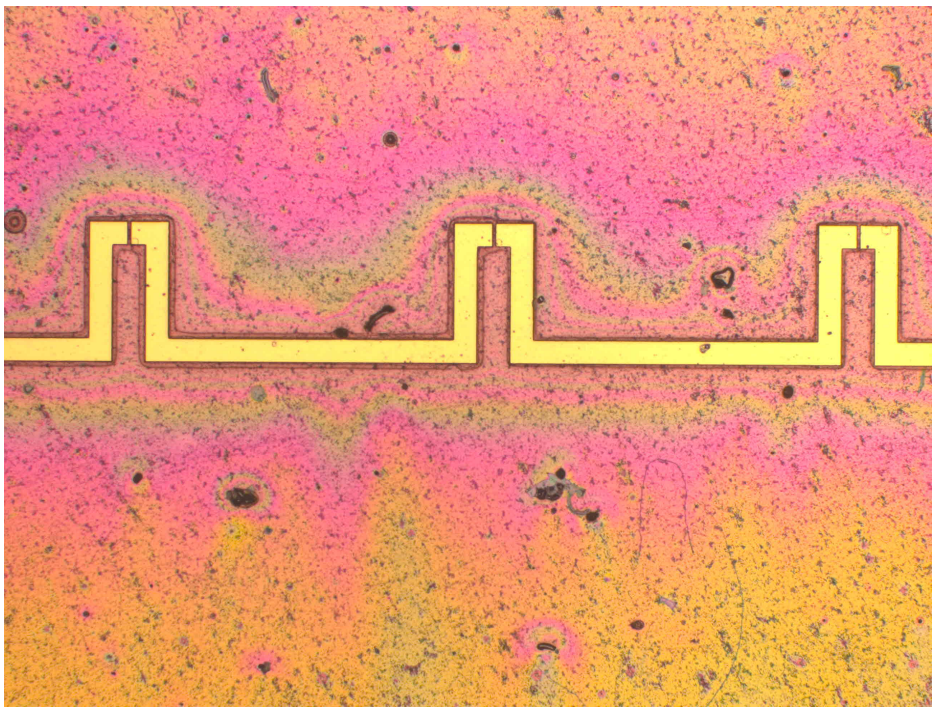


Figure 3.4: Test Pattern Fabrication Optical Microscope Image

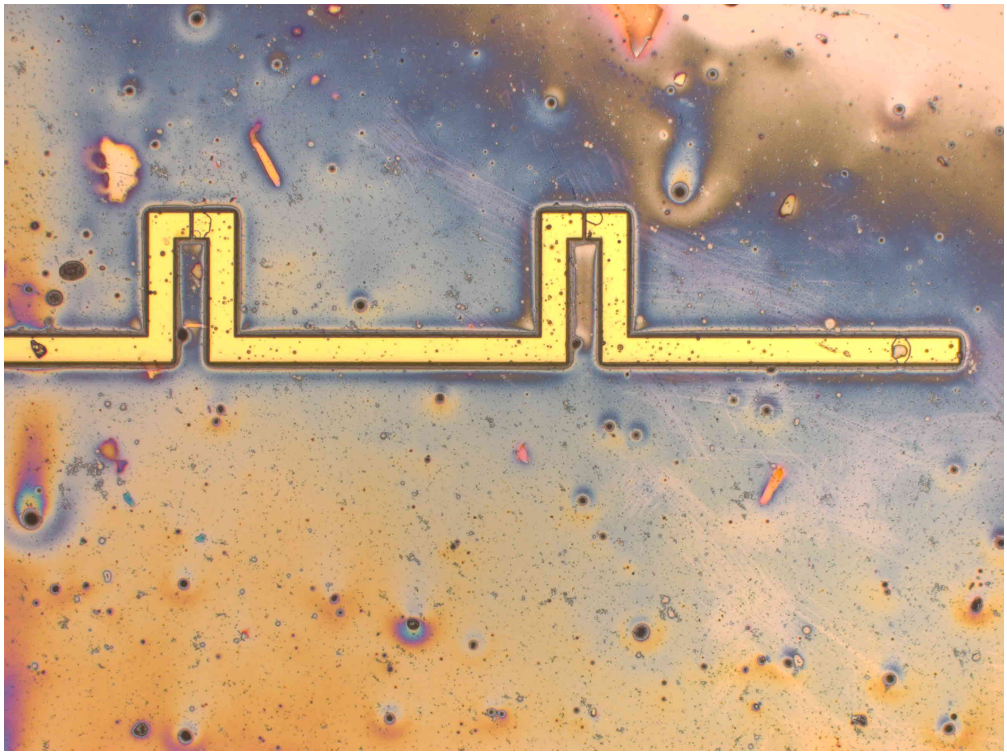


Figure 3.5: BOE Etching Through the Capping Layer and Damaging the Aerogel Optical Microscope Image

It is believed that the BOE etchant, at weaker points in the SiO_x film (most likely pinholes) was able to penetrate all the way through the protective layer and start to etch

the fragile aerogel underneath very quickly. This result would not be acceptable for any MEMS processing with aerogel thin films. Alternatives for depositing and defining metallization layers or other materials include the use of different seed layers for metallization layers, other deposition methods like liftoff, or changing etching techniques and using a sputter etch, RIE, or ion mill.

Another concern from this experiment involves the capping layer. It would be effective in sealing the top of the aerogel film from solvent damage provided a BOE etch was avoided, but would still leave the edges of the material stack exposed as seen in Figure 3.2. The proposed solution to this problem was to fabricate samples large enough to prevent any damage to the interior of the film where the aerogel was being measured and limit any aerogel damage to the perimeter of the sample.

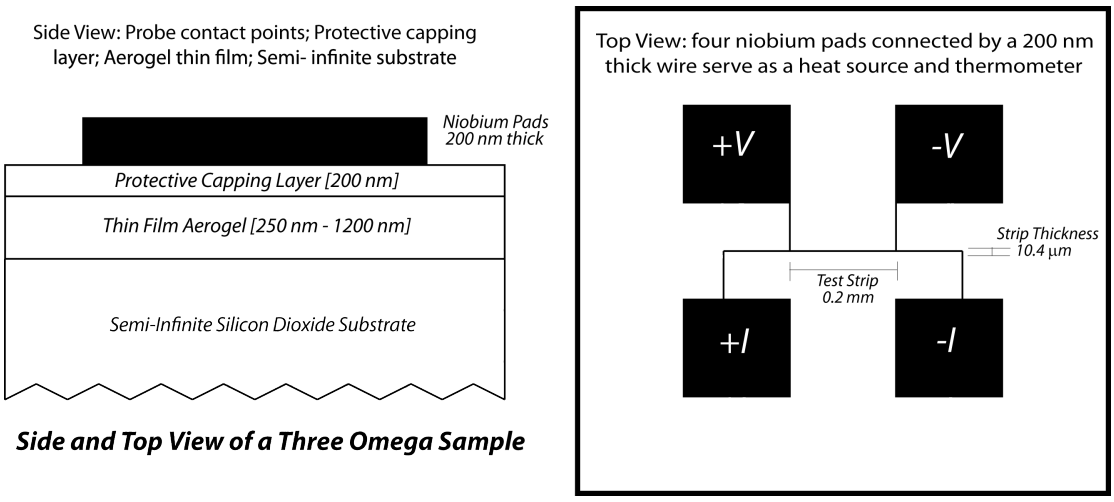
Experiments continued to define a metallization layer on top of the aerogel films, but while selecting different metals and/or etch chemistries to avoid damaging the SiO_x capping layer was possible, we were hesitant to use an approach that would fully submerge the wafer in any liquid etching. Liftoff, as described in previous chapters, would require suspending the wafer in a heated bath of resist stripper for hours at a time and might require additional physical scrubbing on the wafer surface. To minimize wafer and aerogel contact with etching or developing solutions, it was therefore decided to explore the use of dry etches as an alternative.

Of the available dry etching techniques, ion milling and argon sputter etching have been described in previous chapters where physical bombardment of argon ions is used to remove material from the wafer surface. These methods could both be effective where the wet etch failed, etching through the metallization layers without catastrophically damaging the aerogel through pinholes in the capping layer. However these methods also provide little selectivity and overetching would need to be minimized to prevent significant etching of the capping layer underneath the metal pattern enough to alter the geometry of the 3ω testing pattern and thereby alter the testing assumptions of a planar capping layer that the heat is transmitted through.

With concerns about etch selectivity, a reactive ion etch (which employs both physical and chemical etching) was considered. It can potentially provide more selectivity than the other dry etches with an etching chemistry appropriately selected for removing the desired material at a significantly higher rate than the capping layer. To be able to use the potential advantages of RIE for etching the metallization layers, it was necessary to select a suitable metal material as there are no RIE chemistries that selectively etch gold. Niobium was a good candidate for future tests as it has multiple RIE chemistries, well characterized deposition methods in the UVML cleanroom sputtering tools, and good adhesion to the SiO_2 capping layer. It also has thermo-resistive linearity over low temperatures [20], which is important for the subsequent 3ω tests. Using niobium would be acceptable for low temperature testing, but not high temperatures as this metal is easily oxidized, with the resulting surface oxides potentially inhibiting a low resistance contact. Probes brought into contact with the niobium pads would have to be tested to ensure electrical contact for testing at room temperature or below, but at high temperature such contact would be even more difficult.

To be able to test the feasibility of using niobium for the test structure and the use of an RIE to etch it, designing a photolithographic mask that is compatible with the testing process was necessary to proceed. The thermal properties of the different aerogel films would be tested using the 3ω process, selected for "its sensitivity to individual layers in multilayer structures, high accuracy and repeatability, and its ability to eliminate convective as well as radiative error." [19]. This method uses a lock-in amplifier to generate a first harmonic (1ω) signal that generates second harmonic (2ω) joule heating in the thin niobium wire that are measured with the third harmonic (3ω) voltage oscillations that serve as a thermometer. The thermal conductivity of all of the individual layers can then be determined mathematically.

The 3ω technique used for thermally testing samples involves defining a thin metal line with four contact pads for measurement on top of the sample as shown in Figure 3.6. A wafer was first diced into 19mm^2 samples to fit into the testing apparatus. Next, aerogel was deposited onto those samples, followed by the sputtering of a SiO_x capping layer. The test structure was completed with the definition of the niobium pattern that included the 10μm wide niobium line. To ensure proper mask contact across the wafer and to accurately realize the 10μm line, a burn-off mask was created as well to remove edge bead build-up of photoresist on the perimeter and particularly the corners of the wafer. Alignment of the subsequent wire pattern onto the center of the remaining resist square was non-critical so long as the pattern was not too close to the edge.



Side and Top View of a Three Omega Sample

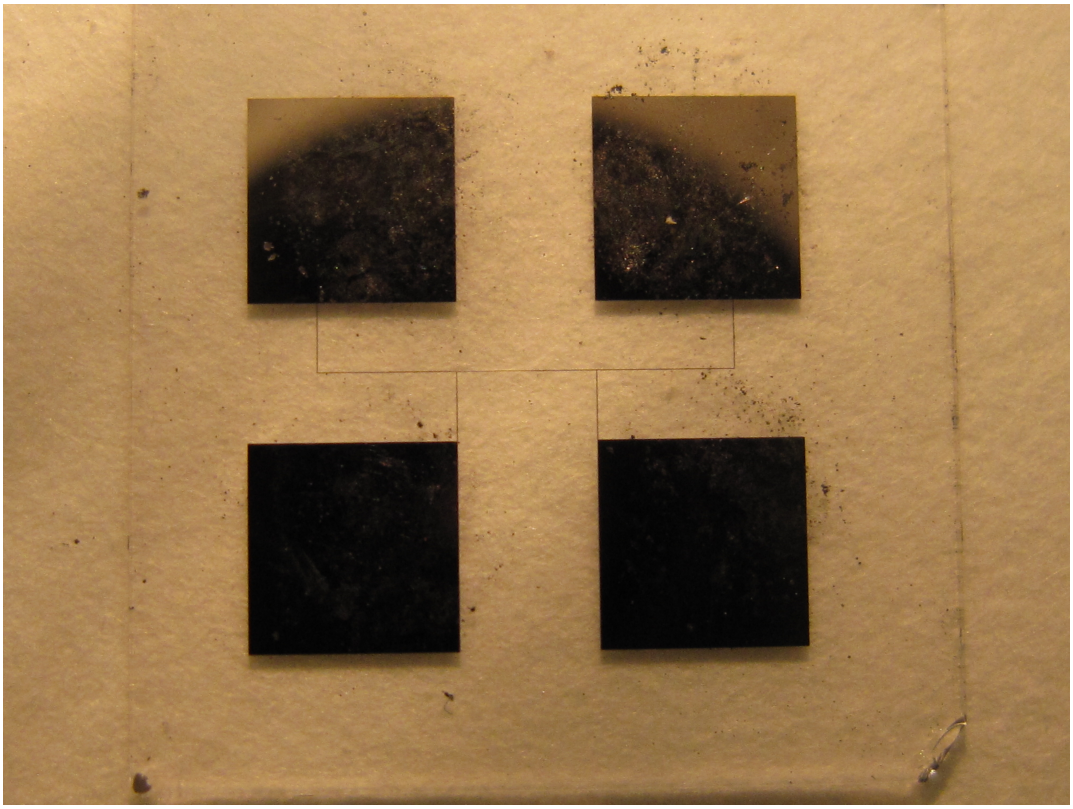


Figure 3.6: 3ω Sample: a) Schematic of Side View b) Schematic of Top View c) Photograph of 3ω Sample

It is important to note that the decision to dice the wafers before circuit processing came after noting on aerogel wafers that had been diced, some damage to the aerogel near the cut lines. This was due to the high-pressured cooling water utilized during dicing, shown in Figures 3.7 through 3.9. The alternative approach of dicing bare wafers first, while reducing throughput greatly, also allowed for depositing the different aerogels onto individual samples and was preferable for the initial processing. For future processing,

however, a scheme to improve throughput for future work was developed by spinning a protective coating resist, AZ Electronic Materials AZ-PC, on top of the wafer before dicing that prevented damage to the underlying layers. After dicing, this protective coating is easily removed with an oxygen ash.

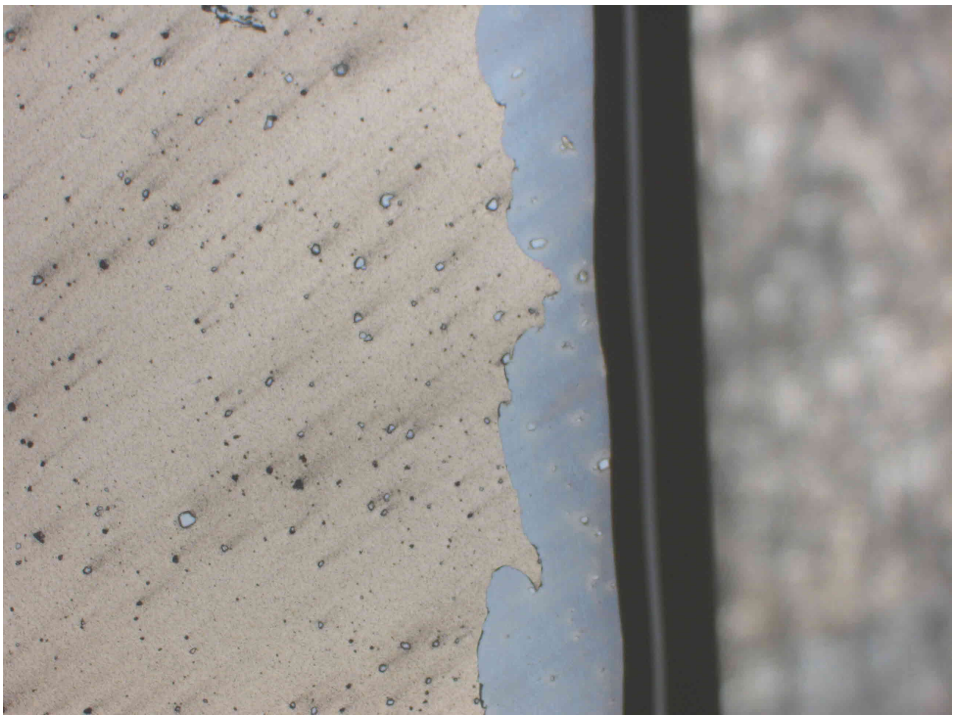


Figure 3.7: Cooling Water Damage During Dicing Optical Microscope Image

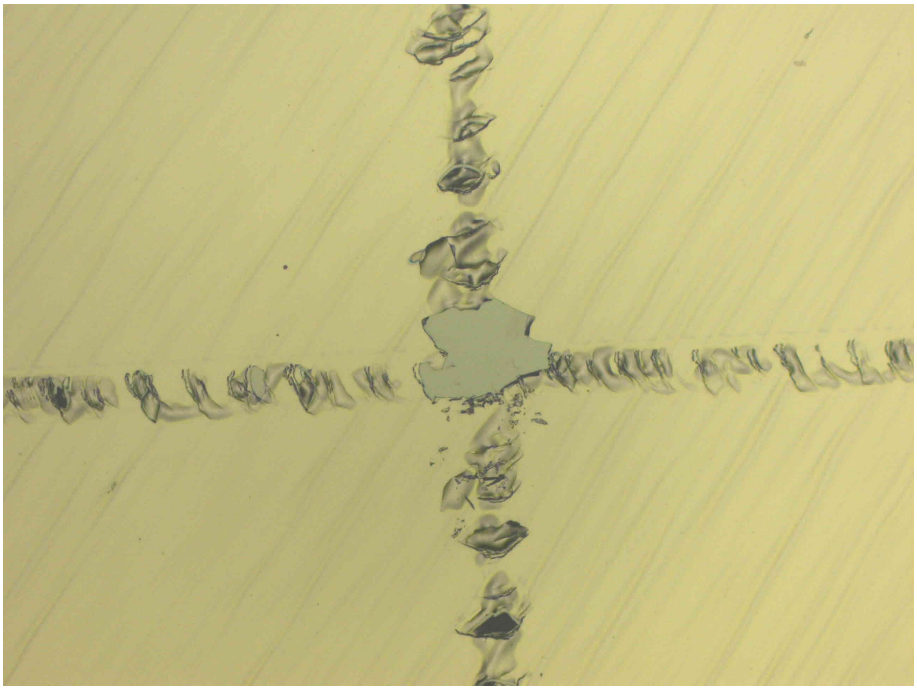


Figure 3.8: Cooling Water Damage During Dicing Optical Microscope Image

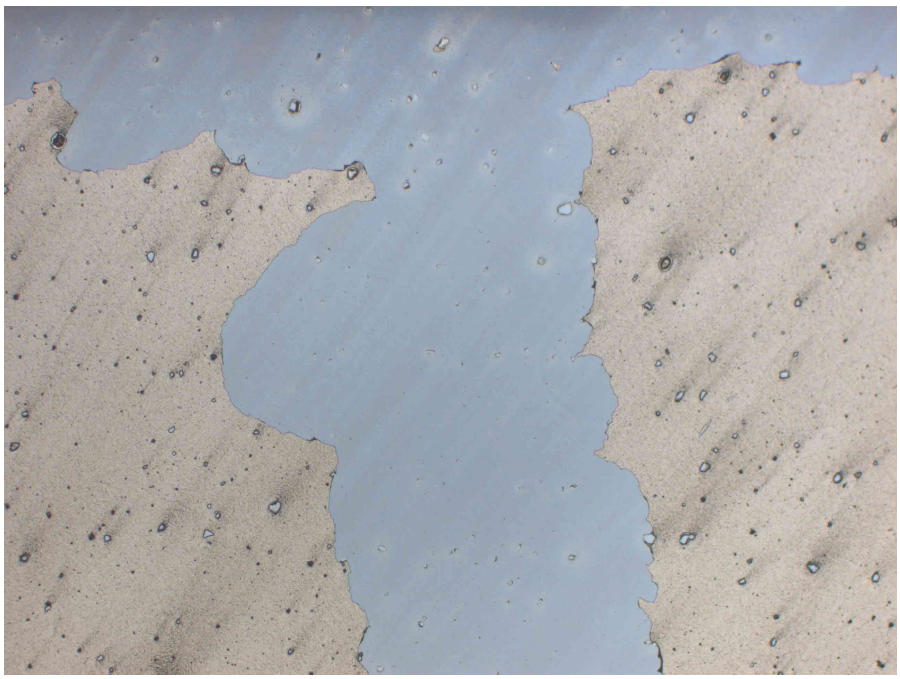


Figure 3.9: Cooling Water Damage During Dicing Optical Microscope Image

The diced silicon samples had a variety of aerogels deposited onto them and then were returned to the UVML, where the SiO_2 capping layer was deposited via magnetron sputter deposition using Sputt 4 at 300W and 4mTorr (see Appendix A). While the vacuum chamber was equipped with Ar^+ sputter clean capability, this was not used in order to avoid potentially damaging the exposed aerogel. A SiO_x thickness of 200nm was deposited, similar to the earlier test runs and to match the thickness of the capping layer used for the Honeywell samples. Tests to determine the minimum required thickness for this capping layer were discussed, but not continued due to time constraints. The heat transmitted through the SiO_x capping layer could be modeled and understood so long as the thickness of the layer was well known. This was possible due to calibration of the Sycon quartz microbalance and side-on SEM images of devices after testing that confirm the thickness of all layers: aerogel, capping, and metal.

Next, a 200nm of low-stress niobium metal layer was deposited at 500W in a 4.70 mTorr argon environment in Sputt 3 (see Appendix A), preceded by a non-physical cleaning step using electrons from a filament to enhance the niobium adhesion to the SiO_2 surface of the sample. The sample was then prepared for photolithography with a solvent spin clean and oxygen ash before a hot plate bake and the spin application of a positive resist (AZ Electronic Materials 4110). Pattering to define the wire lithography was accomplished using a Suss MicroTEC MJB4 contact mask aligner with the newly designed mask for both the burnoff and wire exposures.

With the wire and contact pad resist patterns defined, the sample was loaded into an Oxford Instruments PlasmaLab-100 system for the Reactive Ion Etch step of the wire layer. A SF_6 + Ar chemistry was selected for this process due to its established etch rate and anisotropy. To minimize subsequent etching of the underlying SiO_2 capping layer,

laser endpoint detection was used to terminate the etching process so as not to significantly alter the 3ω structure and to help maintain the assumption of an ideal line source heater in the testing results. Again, without the sputtered SiO_2 capping layer, even the short over etching time used to ensure the niobium was completely removed would damage the fragile aerogel. A gentle 100W oxygen ash was used to remove the photoresist after etching.

Samples were produced using this process both with and without an aerogel thin film to give a control sample for comparison during testing. Once completed, these samples were brought to the 3ω testing setup that was developed by Matt Bauer and Mike Fish. During initial testing, a problem with the silicon samples occurred where they exhibited a strong capacitive effect and reliable measurements were unable to be obtained. This was traced back to using a semiconductor as a substrate with a frequency sweep between 10 and 10,000Hz so the process was modified to use a 254μm thick double-side polished quartz substrate. There was no capacitive effect with the quartz substrate and all subsequent samples were fabricated on quartz, which was more fragile than silicon but was compatible with all of the MEMS processing steps defined above.

In parallel with this effort, similar structures were also fabricated at Honeywell Inc in a separate process at their facilities. Honeywell supplied 100cm wafers to UVa, where aerogel was spun on using the same processes as mentioned before. Similarly, a capping layer of 200nm of SiO_2 was deposited at UVa onto the wafer as a protective layer for the delicate gel. These wafers were then returned to Honeywell to allow them to use their expertise and processing methods to create a test pattern with a proprietary material to provide additional thermal testing data.

A proprietary material stack that included platinum heater wires was deposited on the supplied wafers via evaporation to ensure an excellent temperature coefficient of resistance (TCR) for testing results. Honeywell selected an ion-milling process to remove excess material where a SiO_2 hard mask was used to define the testing pattern. In Figure 3.10 one can see the oxide hard mask on top of the platinum wire. As mentioned earlier, ion milling is not a selective etching process and requires knowledge of material etch rates, otherwise the capping layer and potentially the sample aerogel will be damaged and or exposed for future processing steps. A Honeywell processing issue occurred when all of the platinum on one sample was etched through due to a misjudgment of the ion milling rate or stack thickness. Additionally, the oxide hard mask was required for their process as the photoresist is hardened from excessive heat and ion bombardment during the ion mill step. Honeywell had no capability of removing photoresist after the ion mill: standard wet stripping techniques cannot remove hardened resist, non-standard wet stripping techniques may damage the aerogel, and an oxygen plasma ash would damage their equipment and contaminate the process chamber. A second ion mill was instead performed through the SiO_2 masking layer to create vias for contact to the platinum heater lines, where gold pads were then defined by liftoff.

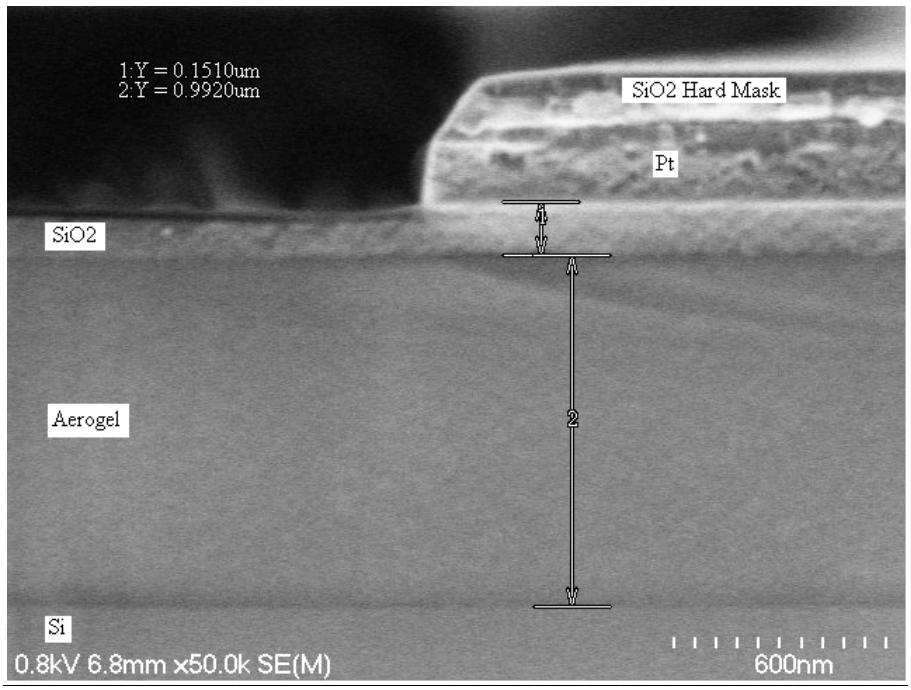


Figure 3.10: SEM of a Honeywell Sample Showing Layer Thicknesses

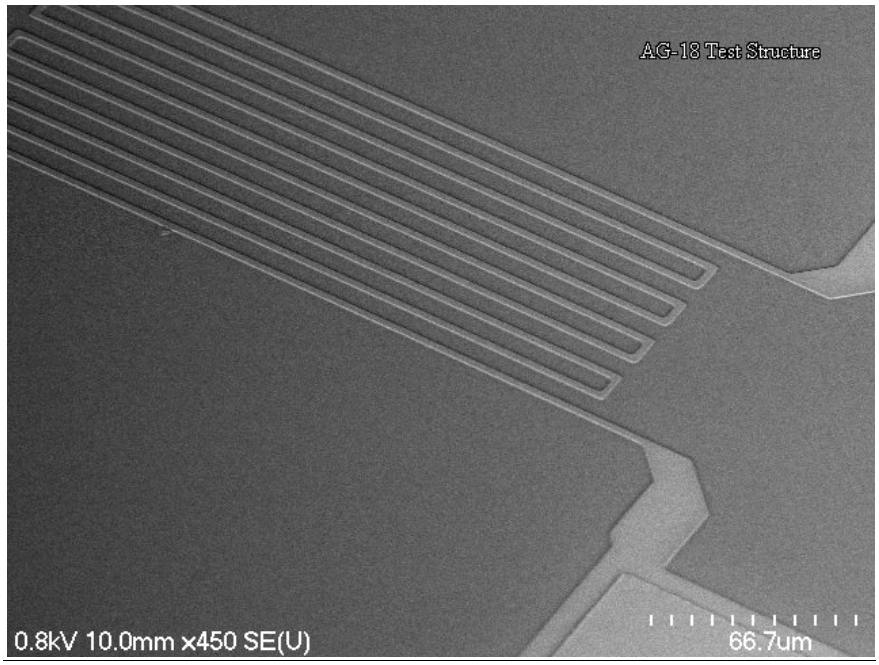


Figure 3.11: SEM of the Honeywell Resistor Structure Used for Testing

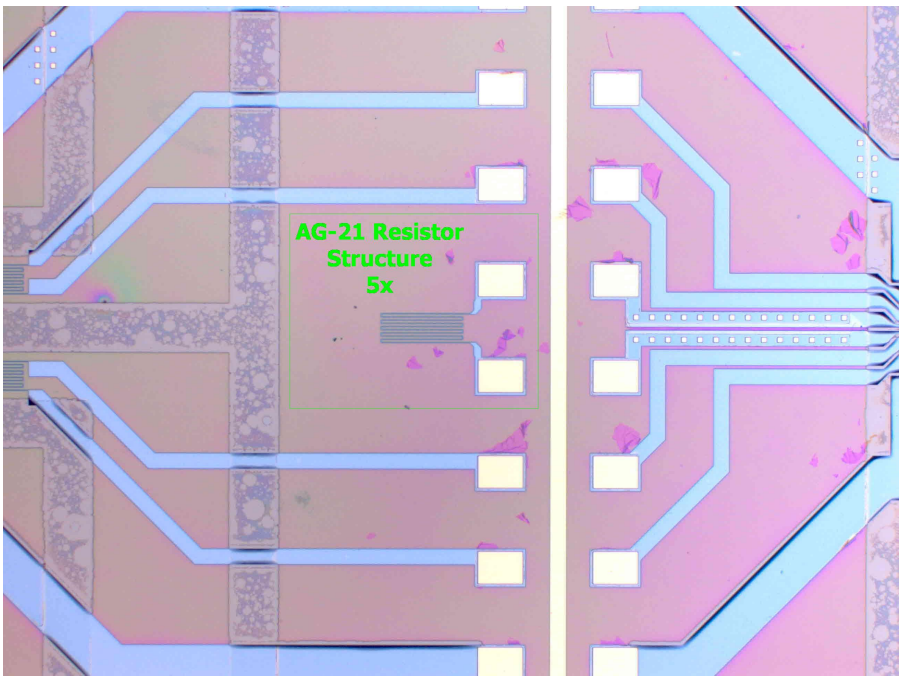


Figure 3.12: The Honeywell Resistor Structure Used for Testing Optical Microscope Image

Multiple methods of determining the characteristics of the aerogel films were explored as well. White light interferometry, physical profilometry, ellipsometry, and reflectometry were all investigated as means with which to determine aerogel thickness after deposition, but each encountered difficulties in determining the correct thickness of the aerogels. Physical profilometry, when used on the fragile aerogel surface, would not follow the surface of the aerogel but instead break through it, damaging the film itself and making any results useless. A measurement could be made of the aerogel + capping layer stack, but this would involve creating an aerogel + capping layer free area of the samples with lithography and etching methods, a challenge that was not addressed in this study. White light interferometry would provide a non-destructive method to measure the aerogel thickness, but would also require an area free of aerogel. Ellipsometry and reflectometry were investigated as means with which to determine aerogel thickness and porosity as well, but communication with Horiba Jobin Yvon, a UVML ellipsometer supplier, to determine a materials model that could be used to determine the aerogel thickness was unsuccessful despite attempts to modify current models. Other attempts to use an ellipsometer constructed by students in the Norris group did not match with the expected values of aerogel determined by SEM imaging. These SEM images (seen in Figures 3.13 through 3.15) were the best method of determining aerogel thickness and would also allow confirmation of the capping layer and metal line thickness. These were destructive in nature however and were a time consuming method of determining aerogel thickness due to the requirement that the sample had to be fabricated, tested, cleaved in half, and measured in the SEM edge-on in a non-trivial measurement.

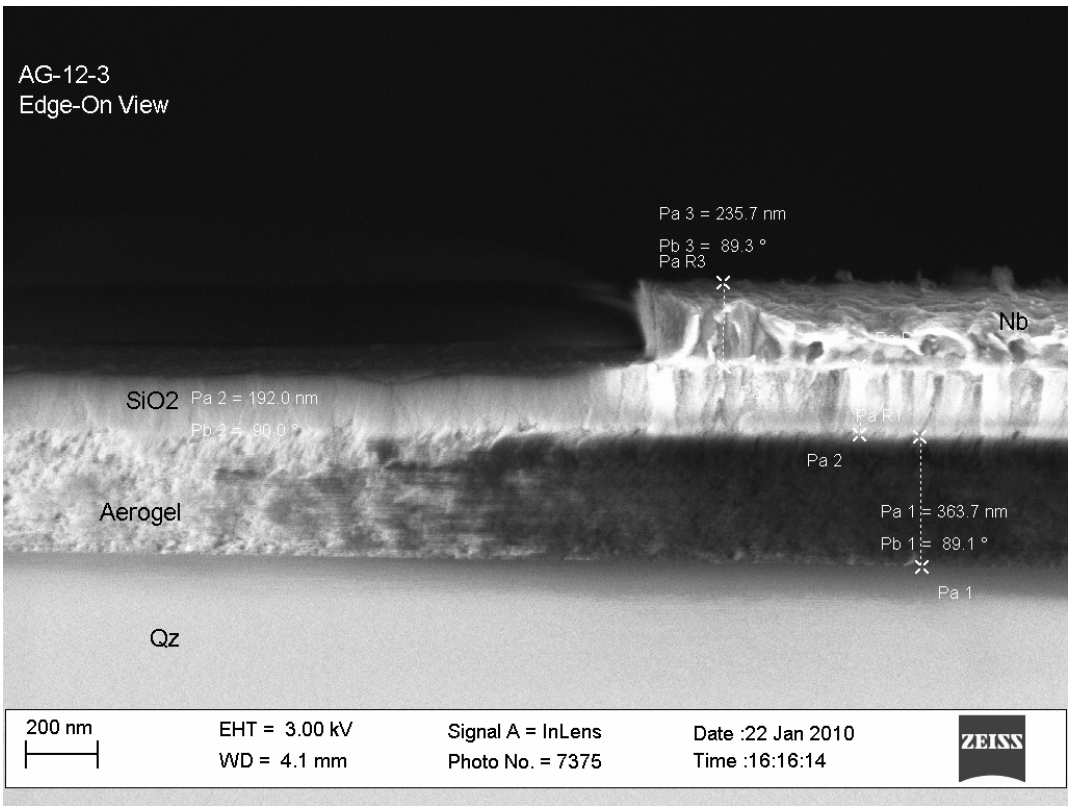


Figure 3.13: SEM of Aerogel Stack Showing Layer Thicknesses

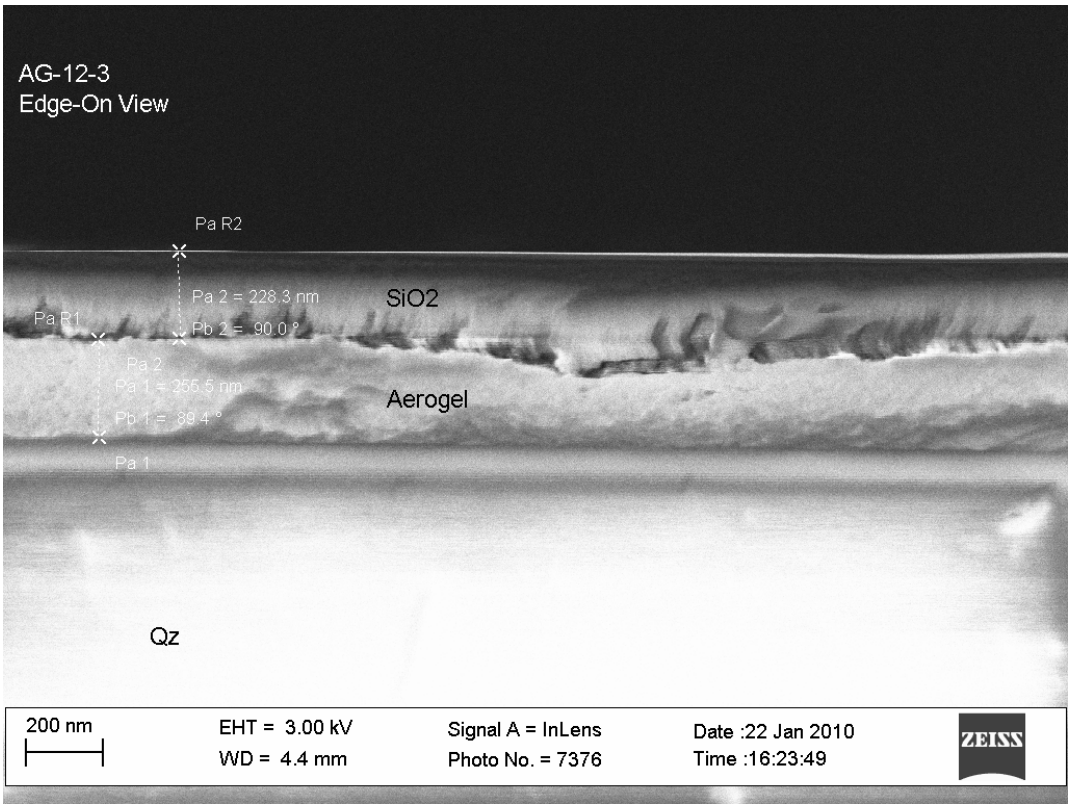


Figure 3.14: SEM of Aerogel Stack Showing Layer Thicknesses

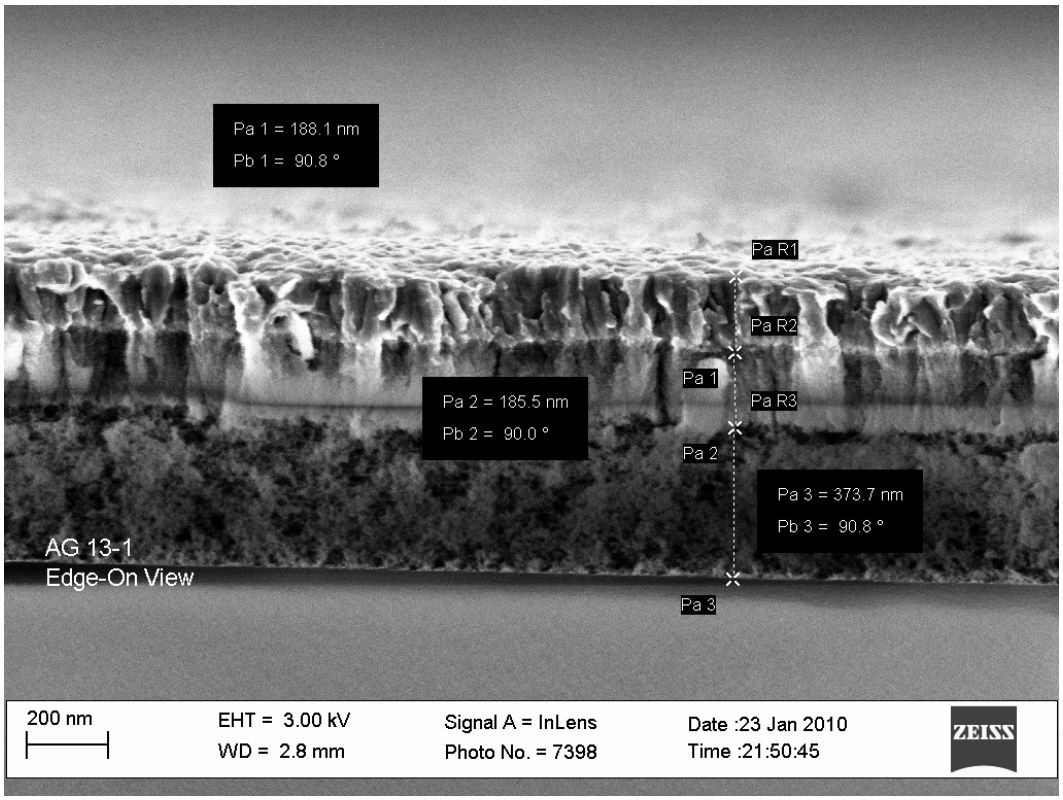


Figure 3.15: SEM of Aerogel Stack Showing Layer Thicknesses

The testing results from the 3ω process are summarized in Table 3.1. The thermal conductivity (k) was determined using the temperature shifts, ΔT_{film}, measured with the 3ω method and the film thickness determined via SEM imaging. Included in the testing is a control sample, where the niobium 3ω pattern was deposited and patterned on a quartz substrate without an aerogel or capping layer. The thermal conductivity of this control sample at 295K was measured to be 1.22 W/m-K with an experimental uncertainty of less than 6%, which agrees well with literature [19]. The thermal conductivities of the aerogel samples were one to two orders of magnitude less than this control sample.

Aerogel type	Thickness (nm)	k_{film} (W/m-K)	Estimated error (W/mK)
A	1280	0.24	±0.05
B	250	0.067	±0.01
B-pyrolyzed	370	0.024	±0.005
C	300	0.33	±0.07
C	620	0.29	±0.06

Table 3.1: Thermal Testing Results [20]

Honeywell's results came from using the relationship between power and thermal conductivity, where the steeper slopes of the curves in Figure 3.16 show a lower thermal conductivity. One can see that the aerogel samples show an improvement over the control sample again but fail to reach the thermal conductivity of the nitride diaphragms.

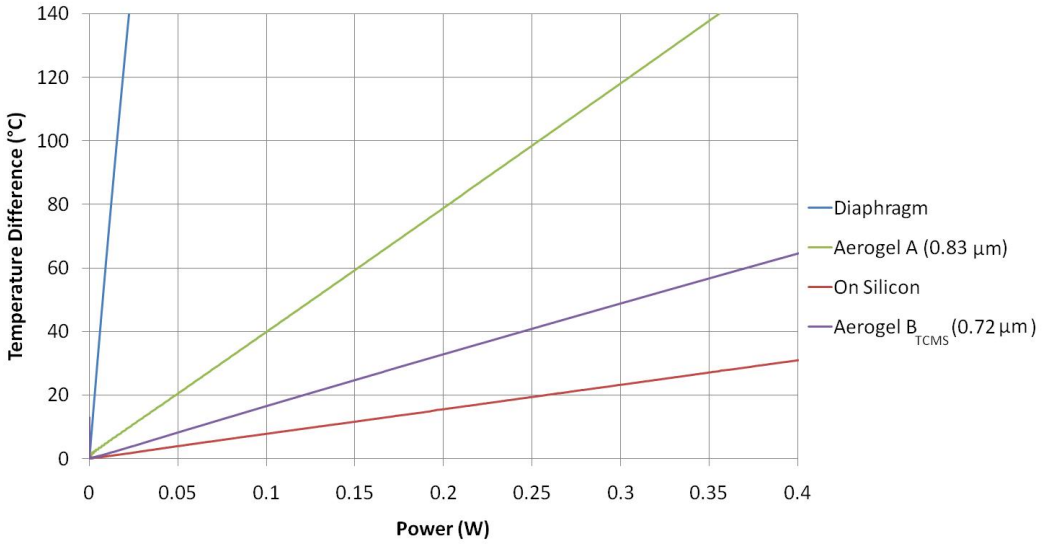


Figure 3.16: Temperature difference across various samples as function of applied power. The slope of the each curve measures the total thermal resistance of the sample with steeper slope signifying higher thermal resistance.

Figure 3.16 also provides a method to compare against the industry standard nitride diaphragms. The aerogel samples created did not perform as well as the diaphragms, but by using modeling to explore alternative sample thickness or by modeling aerogel with a lower thermal conductivity, it can be seen that better thermal insulation could potentially be achieved (Table 3.2). This shows that while the performance of the current aerogel thin films and geometry does not exceed that of nitride diaphragms, improvements could be possible by improving the quality of the aerogel deposited onto the samples or by modifying the spinning technique to increase the thickness of the film and Aerogel B-

pyrol could match the performance of the nitride diaphragms with a reasonable thickness of aerogel.

Aerogel	Thermal Conductance (kW/m^2K)	Necessary Thickness (μm)
A	188	20
B	268	5.6
B-pyrol	64.9	2
C (300)	1100	29
C (620)	468	24
Diaphragm	12	-

Table 3.2: Calculated thermal conductance of the samples tested compared to the industry standard diaphragm. Also shown is the thickness each sample would have to reach, assuming its conductivity remained constant, in order to match the diaphragm's thermal conductance. Note the two Aerogel C samples tested are denoted by their respective thicknesses.

The original DARPA proposal for this project included investigating a selective deposition technique. The reason for this experiment was to explore if thin aerogels films could be limited to only the necessary portions of the wafer within wells or channels to provide the insulation required of the project without having to deposit aerogel over the entire surface of the wafer. A concept depiction of this is shown in Figure 3.17. Chemical treatment of silicon surfaces could be used to encourage aerogel to adhere to the surface or prevent good adhesion depending on the chemicals used for surface treatment [20]. A process was developed that the surface of the entire wafer could be treated to prevent aerogel from adhering to the surface and photoresist spun onto the wafer and patterned such that the aerogel wells were defined while protecting the areas of the wafer that needed to retain the surface treatment to reject aerogel. The exposed silicon was then etched and then treated to encourage aerogel adhesion in the newly created well within the wafer. During this second treatment, the photoresist still on the surface of the wafer had to hold up to this chemical bath in order to ensure the surface of the wafer would still prevent aerogel from adhering to it. The second treatment had to be tested, as most of these chemicals were strong bases and would remove the photoresist and make the entire wafer receptive to aerogel bonding [20]. The removal of the photoresist also had to make sure not to alter the surface treated to reject aerogel or the wells treated to encourage aerogel formation. A solution was found to be compatible with photoresist, but this process could not be incorporated into the final thermal testing of devices due to time constraints and would be one area of future work to pursue. This method could also be a potential solution to the problem of having an exposed sidewall of aerogel integrated into devices where extra space to prevent damage to the interior insulation is not an available luxury.

Figure 3.17: Aerogel Deposition into Silicon Wells with Surface Treatment Schematic

Further pursuit of characterization techniques, particularly non-destructive ones like ellipsometry and white light reflectometry, is another area of future work that will be required to improve working with aerogel. This would allow for characterizing simple quantities like thickness will help make thermal measurements more reliable and precise. These measurements can then give rapid feedback on the quality of the aerogel produced as well as the integrity of the aerogel after processing. More complex concepts like index of refraction can also be determined by ellipsometry, which can then determine the porosity of the aerogel, a key parameter in defining the quality of the film. The use of commercial ellipsometers was hampered by the difficult to properly model aerogel. Pam Norris's group had already pioneered a technique for measuring aerogels using a custom-built ellipsometry setup [24]. Unfortunately the modeling results from this technique did not match other thickness measurements nor did the system always result in realistic indices of refraction and these discrepancies could not be rectified in our research.

Fabrication throughput is a concern that was considered throughout developing a process for working with aerogel but most of this work was not optimized for increasing throughput as samples were created on an individual basis. This work would involve applying aerogel to entire wafers and not small samples. This would be followed by the processing techniques established above, but with photoresist masks scaled up to put as many devices on one sample as possible followed by dicing the wafer into individual samples. For work with 3ω testing, an example of the benefit of making multiple samples out of one wafer would be to vary the width of the metal line used for testing to determine the anisotropy of the heat transfer through the sample.

While not matching the thermal insulation that a nitride diaphragm can, thin film aerogels have been shown to be compatible with MEMS processing techniques and provide a number of benefits over diaphragms that lead the authors to believe that this process is worth further pursuit. A situation where diaphragms and aerogels are combined can be visualized as well, though insulation gains are not known and would need to be pursued further. Such gains in size, potential improved heat resistance, and mechanical stability provided the initial inspiration to pursue thin film aerogels and with early success in fabrication and processing should provide more impetus to pursue using thin film aerogels in lieu of or in combination with nitride diaphragms.

Conclusions

Properties of insulating films play an important role in numerous devices. In this work SiO_x sputter deposited films were successfully incorporated into our SIS fabrication process, replacing the previous inferior method of evaporation. Ellipsometry, mercury probe tests, and capacitors were used to evaluate the quality of SiO_x thin films from a thermal evaporator and multiple sputter tools. Results showed the diode sputtering system was superior to the other tools, however oxide quality is only one criteria of this study – compatibility with the SIS Pentalevel junction process for creating is also crucial. In this work diode sputtered SiO_x films were also successfully adapted to the Pentalevel process with which we were able to create SIS devices that had good electrical characteristics. Subsequent mixer tests on ALMA Band 3 met receiver specifications, further verifying the new process. These diode sputtered films are now the standard for the UVML's SIS junction and 2nd SiO_2 insulation replacing evaporation, used for the past 25 years.

During the development of sputter deposited SIS junction insulation, initial single resist liftoff tests showed that a single resist junction process would be feasible and worth pursuing. Replacing the Pentalevel process with a single resist would significantly reduce processing time, though with tradeoffs in junction area control and processing difficulty. Work on comparing methods for etching the gold overlayer, the M2 niobium counterelectrode, and SiO_2 deposition coverage of the junction resulted in incorporating a 45° ion mill to etch the gold followed by a 50W SF_6 + Ar niobium RIE. The final addition of a 160° C bake before the etching process sufficiently hardened the resist, preventing the formation of an artifact ring without inhibiting liftoff. This process was used to create SIS devices where junctions larger than 1.5μm with good electrical characteristics were measured.

Incorporating aerogel into MEMS devices completed this thesis on SiO_2 films. Creating insulating layers with this unique and fragile thin film aerogel material that were compatible with device processing was a challenge. A novel spinning technique was developed to deposit the aerogel into uniform thin films onto wafers. The next experiments were then developed to determine the processing techniques necessary to create test structures on this film without damaging it. A sputtered SiO_x capping layer was deposited onto the surface of the aerogel to protect the top surface of the film. Niobium was selected for the metallization layer and was defined via photolithography and RIE to minimize solvent exposure and overetching. This process was used to create 3ω test samples that could then be tested to determine the quality of the aerogel compared to industry standard nitride diaphragms used for insulation. While no aerogel sample was more insulating than the diaphragms, some of the aerogel types were on order of the same quality as the diaphragms. The knowledge gained from this aerogel fabrication process that was developed to withstand processing techniques required to create simple devices allows aerogels to be considered for use as an insulating technique.

Appendix A: UVML Tools

Sputt 3

A custom vacuum system equipped with a load lock for a reduced pump down time and to maintain a clean sputtering chamber. This system has four dc magnetron sputtering guns and one ion gun.

The chamber is set up in such a way that the three-inch niobium gun is attached to a port that allows for straight on sputtering (perpendicular to the substrate). The other 2.5-inch sputtering guns are equipped with gold, titanium, and chromium targets and are off axis at a 45-degree angle to the substrate.

The ion gun is also situated 45 degrees to the substrate. Its uses include cleaning the substrate prior to deposition for enhanced adhesion and etching. The ion gun can be used to either create ions to bombard the surface and physically etch it or it can generate electrons from a filament for a gentler substrate clean than the ion bombardment.

Sputt 4

A custom vacuum chamber originally equipped with an eight-inch diameter RF magnetron sputtering gun from AJA Instruments with a variable throw distance from 12-23cm. It is also equipped with the ability to apply RF to the substrate itself for an Ar^+ sputter clean capability used to clean the surface of the substrate.

Experiments from this thesis also required modifications to this system to make it into an RF diode sputtering system. To accomplish this, the rare earth magnets were removed from the sputtering gun and the matching network was connected directly to the gun via copper rods instead of a cable to be able to handle the increased current flow. The throw distance of the gun was reduced to 8.89cm to match the Turbo Sputt system and the sputtering dc biases used were matched to attempt to create similar films.

Thermal SiO_x Evaporator

A SiO_x evaporating/sublimating tool that uses a heated, baffled crucible with solid SiO material to perform a low-energy deposition onto an off-axis (~7°), rotating substrate for improved step coverage.

Turbo Sputt

A custom-built, multi-user RF diode sputtering tool equipped with a single interchangable target and used for sputtering SiO_x in our experiments. It has a throw distance of 8.89cm and is equipped with a sputter-etching capability.

AJA

A custom-designed sputtering tool, built by AJA International. This tool has two chambers (one hot and one cold deposition chamber) as well as a load-lock to minimize pumping times. Each chamber is equipped with five sputtering guns for different materials arrainged with one directly beneath the sample and the others at an angle around it, including an RF magnetron sputtering target in the cold chamber for SiO_x deposition. Sputtering gasses available for this system include inert argon as well as reactive gasses oxygen and nitrogen. Performing reactive sputtering was outside the scope of this thesis, but it is an option for future deposition work.

Oxford

Oxford Instruments PlasmaLab-100 system was used for reactive ion etching (RIE) of substrates. This system has the capability of using multiple etch chemistries including fluorine and chlorine based etches and has an available inductively coupled plasma (ICP) unit. Liquid nitrogen allows the system to achieve low etching temperatures. It is also equipped with laser endpoint detection to determine the stopping point for etches based on material reflectivity.

Axic RIE

A reactive ion etching (RIE) tool with a parallel plate setup. This tool was primarily used for sputter etching inert metals using the physical bombardment of argon ions.

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