Laser Processing and Rapid Thermal Annealing of High-Efficiency c-Si Photovoltaic Devices

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In partial fulfillment

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Doctor of Philosophy

Charles L. Brown Department of Electrical and Computer Engineering

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By

Arpan Sinha

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APPROVAL SHEET

This Ph.D. dissertation is submitted in partial fulfillment of the requirements

for the degree of

Doctor of Philosophy (Electrical and Computer Engineering)

Arpan Sinha

This Ph.D. dissertation has been read and approved by the Examining Committee:

Professor Mool C. Gupta, Advisor (ECE)

Professor Jon F. Ihlefeld, Committee Chair (ECE & MSE)

Professor Andreas Beling (ECE)

Professor Avik Ghosh (ECE & Physics)

Professor Kyusang Lee (ECE & MSE)

Accepted for the School of Engineering and Applied Science:

Professor Jennifer West, Dean, School of Engineering and Applied Science

December 2023

To

My parents, Alokesh and Sanchita Sinha

and

ParaBrahman

'All this is Brahman. Everything comes from Brahman, everything goes back to Brahman, and everything is sustained by Brahman. One should therefore quietly meditate on Brahman.' Chandogya Upanishad 3.14.1

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Abstract

Recent developments in the c-Si photovoltaic (PV) solar cells based on inter-digitated back-contact heterojunctions (IBC-HJ) and carrier selective layers have resulted in record power conversion efficiencies. Multiple photolithography steps, high-temperature masked deposition, and furnace annealing are employed to fabricate these high-efficiency devices. Unfortunately, such conventional methods increase the thermal budget and technical complexity, affecting the levelized cost.

This thesis describes a comprehensive scientific investigation of laser processing and rapid thermal annealing (RTA) in improving solar cell device performance and circumventing the limitations of conventional fabrication methods. Different materials, optical, and electrical characterization techniques were employed to support the scientific investigations.

This work has investigated: (1) the selective laser ablation of top sacrificial a-Si:H layers without damaging underneath the passivation layer in IBC-HJ solar cell, (2) the use of RTA under different temperatures and atmosphere for B-doped p-TOPCon solar cell fabrication, (3) the effects of RTA thermal and cooling cycles on the passivation quality in B-doped p-TOPCon solar cells, (4) the thermal annealing behavior of transition metal oxide based PV devices, and (5) the use of laser heat for selective KOH etching of Si without any laser-induced damages.

The main results are (1) the achievement of high carrier lifetime and open circuit voltage after optimized nanosecond pulsed laser ablation, (2) the use of Essential MacLeod simulated color charts to determine the laser ablation depth accurately, (3) the effect of RTA treatment on the reduction in the hydrogen-induced blister formation, enhancement of the passivation quality, increased dopant activation and effect of SiN_x capping layer on B-doped p-TOPCon PV devices,

(4) Optimized longer cooling times to achieve good passivation quality and dopant activation in B-doped p-TOPCon solar cells, (5) the optimization of ALD Al_2O_3, TiO_x and PVD MoOx and successful laser annealing to fabricate bifacial TMO-based CSPC solar cells, and (6) the feasibility of selective laser-assisted chemical etching using a μs-pulsed laser to create patterns on Si surface without any laser-induced defects and has potential applications in a wide variety of Si devices.

This work shows the successful implementation and limitations of laser processing and RTA in fabricating high-efficiency silicon photovoltaic devices. A fundamental understanding of the laser material interaction and RTA in high-efficiency silicon photovoltaic devices is provided. Both IBC-HJ and TOPCon c-Si devices are expected to dominate the future photovoltaic market, so the presented results will be helpful in the advancement of both technologies.

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List of abbreviations

ALD	Atomic layer Deposition
CIE	International Commission on Illumination
CSPC	Carrier Selective Passivated Contacts
CW	Continuous Wave
DASH	Dopant-free Asymmetric Hetero-contacts
EDS	Energy-dispersive X-ray spectroscopy
ETL	Electron Transport Layer
FGA	Forming Gas Annealing
FIB-SEM	Focused Ion Beam Scanning Electron Microscopy
FTIR	Fourier Transform Infrared Spectroscopy
FWHM	Full Width Half Maximum
HAZ	Heat Affected Zone
HTL	Hole Transport Layer
IBC-HJ	Interdigitated Back Contact Heterojunction
iV_{OC}	Intrinsic Open Circuit Voltage
LHICE	Laser Heat-Induced Chemical Etching
LPCVD	Low-Pressure Chemical Vapor Deposition
MCL	Minority Carrier Lifetime
PECVD	Plasma Enhanced Chemical Vapor Deposition
PL	Photoluminescence
POLO	Polysilicon on oxides
PR	Photoresist
PVD	Physical Vapor Deposition
PV	Photovoltaics
QSSPC	Quasi Steady State Photoconductance
RTA	Rapid Thermal Annealing
SRH	Shockley-Read-Hall

TMO	Transition Metal Oxides
TOPCon	Tunnel Oxide Passivated Contacts
UV	Ultraviolet
XPS	X-ray photoelectron spectroscopy

CHAPTER 1: Introduction and Motivations

The increase in global energy demands has been met by excessive consumption and exploitation of non-renewable fossil fuel resources such as crude oil, natural gas, and coal. Regrettably, these resources are inherently unsustainable and finite. Consequently, the depletion of these resources has resulted in significant price increases.

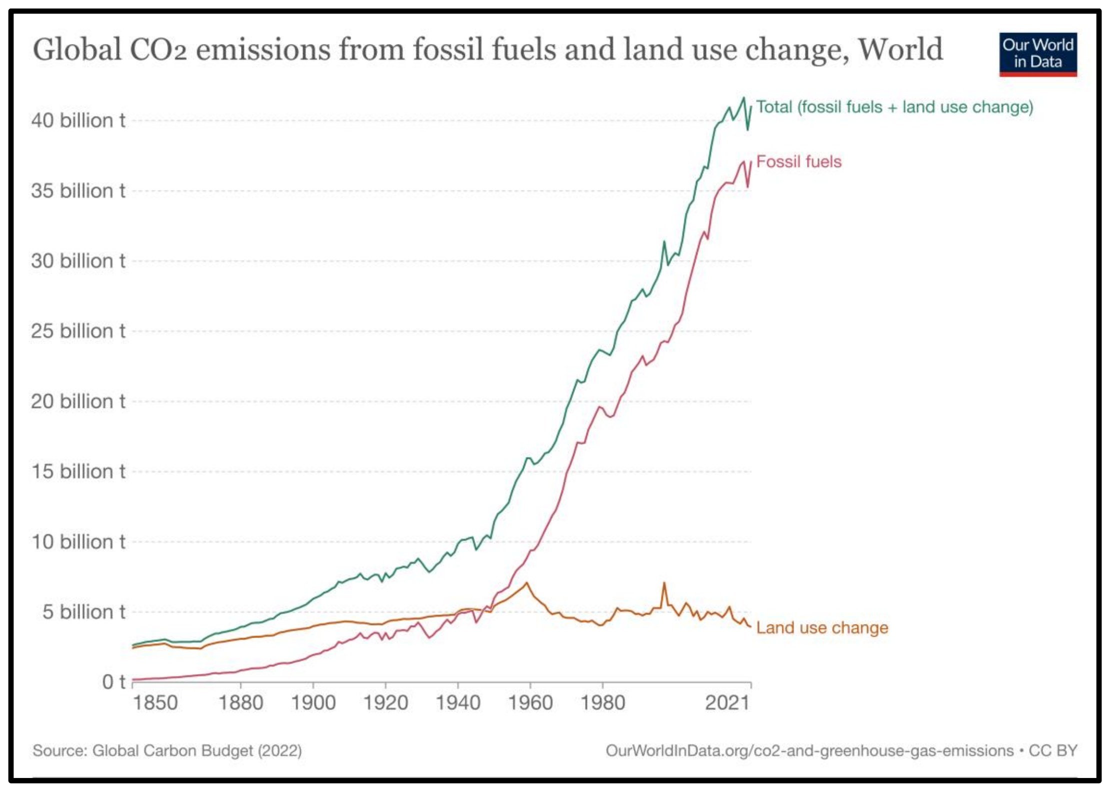


Fig. 1. 1 Data from the Global Carbon Budget 2022 shows the Global CO_2 emission from fossil fuels. (Reproduced from ref. [1] with permission of the Copernicus Publications, Earth System Science Data, and Our World in Data.).

According to reports from MET Group energy company and substantiated by the Energy Institute (EI) as of 2020, the reserves-to-product (R/P) ratio for coal is estimated to last for 139 years, while oil reserves are expected to sustain for 57 years, and gas reserves for 49 years [2][3].

In addition to these economic and energy reserve challenges, anthropogenic climate changes, including global warming, CO_2 emissions, pollution, ocean acidification, and land degradation, have substantially damaged the world's ecosystems. The Global Carbon Budget 2022 report, as shown in Fig. 1.1., states that the combined global impact of oil, coal, and gas resulted in approximately 35 billion tons of CO_2 emissions in 2021, with coal consumption being the primary contributing factor [1]. Furthermore, the toxic spills and waste generated from fossil fuel usage further harm the environment. Managing these toxic byproducts also increases labor costs, expensive infrastructure requirements, and health concerns. Therefore, such ongoing global issues can be tackled by advocating the use of renewable energy resources as an alternative.

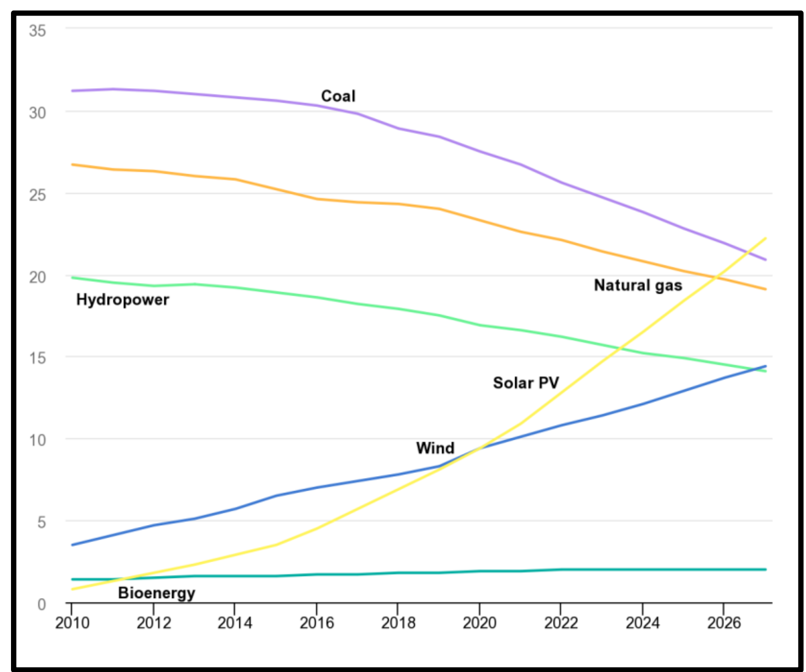


Fig. 1. 2. Data from IEA 2023 shows the increasing dominance of solar PV technology over all other energy resources. (Reproduced from ref. [4] with permission of the IEA, under creative commons attribution License: [CC by 4.0])

Renewable energy resources encompass sustainable options such as solar photovoltaics (PV), wind power, air energy, geothermal energy, biofuels, and hydropower. These represent vast, sustainable reserves that not only reduce carbon emissions but also avoid the production of harmful byproducts. According to the International Energy Agency's (IEA) International Energy Outlook 2019 (IEO2019) and the Annual Energy Outlook 2022 (AEO2022), renewables are expected to collectively contribute to 49% of global electricity generation and 44% of U.S. electricity by the year 2050 [5][6]. Solar PV technology is anticipated to experience the most rapid growth among renewable sources. In the renewable energy sector, solar PV technology has emerged as a formidable contender, challenging the dominance of wind technology in renewable capacity and commercialization. In fact, the International Energy Agency (IEA) reported that the cumulative power capacity of solar PV generation surged to 12.8% in 2022, as shown in Fig. 1.2., surpassing wind technology for the first time [4]. Solar PV's appeal is further enhanced by its advantages, including predictability, space efficiency, low maintenance requirements, flexible scalability, rapid deployment, modularity, and positive environmental impacts. As a result, investing in scientific research and development of PV technology has become increasingly important to drive global PV capacity growth even further.

The economic dimension of achieving maximum electrical power generation while minimizing expenses is pivotal in sustaining the global dominance of PV technology within the renewable energy market. This economic consideration, often quantified through the Levelized Cost of Energy (LCOE), expresses the cost-effectiveness as the cost per kilowatt-hour ($/kWh). Lai *et al.* define LCOE as an economic evaluation of the total cost of constructing and operating a power-generating asset over its lifespan, divided by the total energy output produced by that asset over the same period [7]. Consequently, ensuring the systematic and cost-efficient utilization of

resources and reducing LCOE becomes essential for advancing PV technology. Recent findings from Lazard indicate a declining trend in the LCOE for unsubsidized solar PV cells, signifying a decrease in the overall cost and a positive trajectory for PV technology in the renewable energy market [8]. This reduction in LCOE can be achieved through two principal approaches: (1) lowering fabrication costs and production time and (2) enhancing power conversion efficiency.

The major shares of the total production expenses associated with PV technology are attributed to fabrication costs and production time. Solar cell fabrication typically involves a series of intricate and time-intensive processes that not only impede overall scalability and efficiency but also contribute to increased expenditure. Additionally, using heavy equipment and managing toxic waste further contribute to the overall cost and time requirements. Photolithography, for instance, entails a sequence of time-consuming steps, including applying toxic photoresists through spin-coating, creating costly masks, alignment processes, development, and chemical etching. High-temperature furnace annealing, carried out over extended durations, can inadvertently damage the underlying layers within solar cell structures, raising the overall thermal budget. Furthermore, during furnace annealing, there is limited control and flexibility regarding heating, holding, and cooling times.

To address these shortcomings in the PV fabrication process, laser processing has emerged as a recognized alternative to traditional methods. Laser processing has proven to be a highly effective tool, offering advantages such as patterning flexibility, precise spatial and depth resolution, exceptional selectivity, and the ability to control temperature precisely. Additionally, various laser parameters, including wavelength, pulse width, repetition rate, peak pulse energy, and fluence, can be tailored to match the material's absorption depth and the specific requirements of the laser processing task [9]. Consequently, systematic research and scientific investigations are

imperative to comprehensively understand laser-material interactions and optimize the diverse applications of laser processing to develop cost-effective and manufacturable solar PV cells.

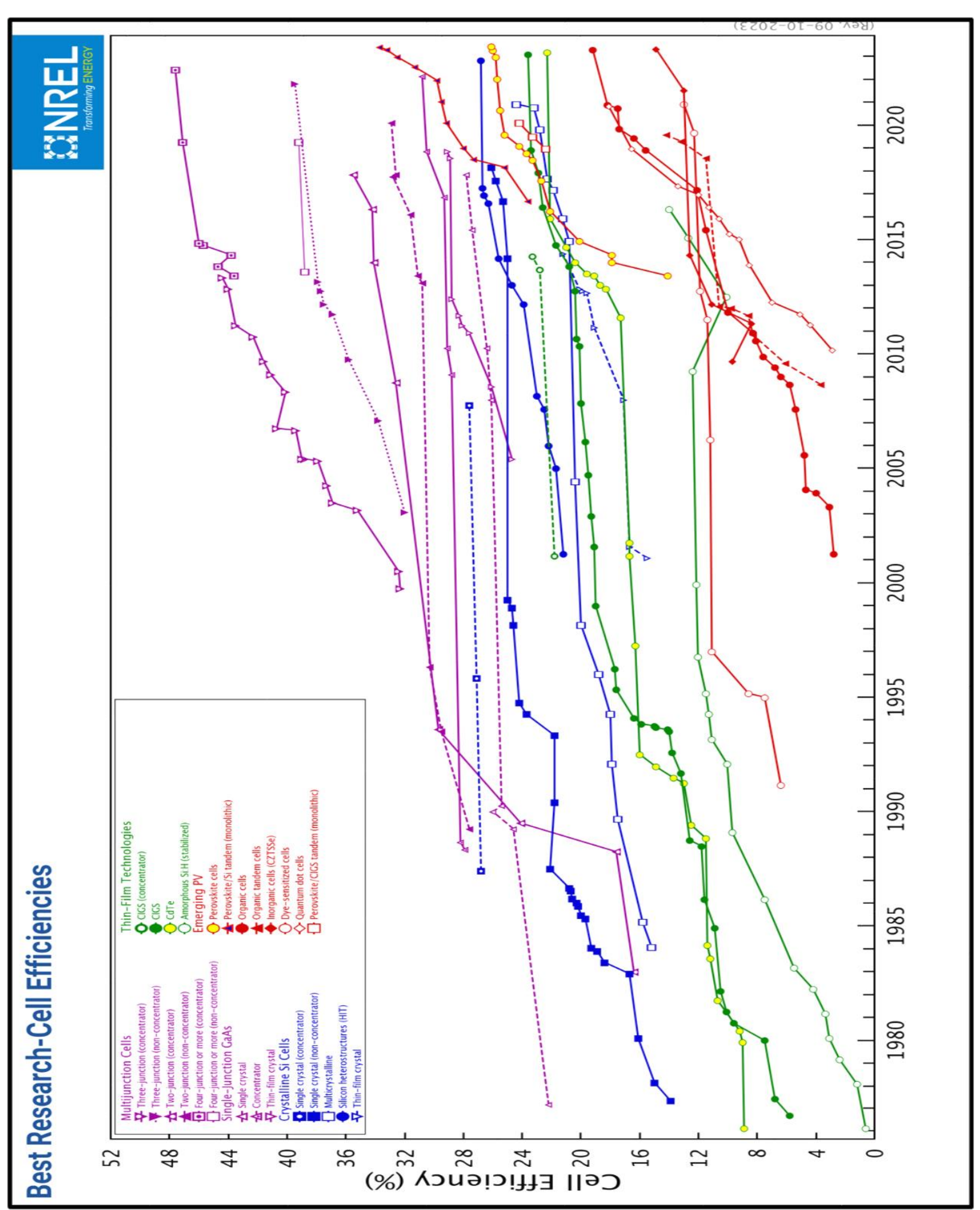


Fig. 1.3. Data from NREL shows the R&D timeline of global solar PV technology to date. (Reproduced from ref. [10] with permission of the NREL).

Photovoltaics (PV) operates on the fundamental principle of converting incident solar energy into useful electrical energy. Thanks to its limitless availability and a broad range of wavelengths, solar energy can be efficiently captured and harnessed by engineering solar PV device structures. According to the most recent NREL Best Research-Cell Efficiency Chart, as shown in Fig. 1.3., the highest laboratory-based efficiencies are achieved by multi-junction solar cells with four or more junctions (concentrator) developed by FhG-ISE, reaching an impressive 47.6%, and three-junction solar cells (non-concentrator) by NREL, achieving 39.46% efficiency [10]. Crystalline silicon (c-Si) based solar cells dominate the global PV market, claiming a staggering 95% share. Among these, monocrystalline Si holds the lion's share, accounting for 70% of all c-Si modules manufactured in 2019 [11]. Noteworthy c-Si based solar cell architectures like the Interdigitated Back Contact Heterojunction (IBC-HJ) and carrier-selective Tunnel Oxide Passivated Contacts (TOPCon) have achieved record laboratory-based efficiencies exceeding 26% [12]. In contrast, commercially available c-Si solar cells typically exhibit 17% to 20% efficiencies. Consequently, there is a compelling need to bridge the efficiency gap between commercial and laboratory-based c-Si solar cells and approach the theoretical limit of 33%, as defined by the Shockley-Queisser limit [13].

The IBC-HJ modules, a prominent design among crystalline silicon (c-Si) solar cell architectures, are projected to capture more than 50% of the global market share by 2030, with the current cost for this technology reduced to $0.30 per watt [14][15]. This architecture has gained significant traction due to its advantages, including minimal shading loss, reduced series resistance, higher power output per unit surface area, a smaller temperature coefficient, and the

ability to optimize optical and electrical properties independently. However, the drawbacks of the IBC-HJ architecture include its high fabrication complexity and production cost. The manufacturing process involves intricate steps, including lithography, masking, UV exposure, Chemical Vapor Deposition (CVD), selective chemical etching, and complex interdigitated multi-stack heterojunction layers for n+ and p+ emitters diffusion. Mask-metallization and the management of waste chemicals further contribute to the total fabrication time, expenses, and operational and maintenance costs. Laser patterning is a promising alternative to certain lithography-based fabrication stages in this context. Laser ablation, which can be optimized to achieve controlled depths, followed by straightforward selective wet chemical etching, can potentially replace some of these stages. To unlock these possibilities, comprehensive investigations into the physics governing laser-material interactions are required to facilitate the development of laser patterning techniques for IBC-HJ silicon solar cells.

Among crystalline silicon (c-Si) solar cells, another popular category is the carrier-selective passivated contacts (CSPC) solar cells, which can be divided into two major subtypes: TOPCon and transition metal oxide (TMO)-based Si solar cells. The TOPCon technology is a formidable contender and is expected to capture over 70% of the global market share in production by 2027, indicating a significant industry shift towards TOPCon [16]. This preference for TOPCon can be attributed to its advantages, including stability during high-temperature fabrication, straightforward manufacturing steps for emitter layers, flexibility in doping, and suitability for screen-printing processes. One crucial but time-consuming step in present TOPCon production involves tube-furnace annealing at temperatures between 800 and 900 ℃. This annealing step enhances passivation at tunneling interfaces, activates dopants, induces poly-crystallization carrier selectivity, and overcomes Schottky barriers in metallization. However, furnace annealing has

limitations, such as limited control over annealing atmospheres, heating, holding, and cooling times, as well as operational and maintenance costs. On the other hand, novel TMO-based CSPC Si solar cells feature asymmetric band offsets, high work functions ranging from 3.5 eV to 7 eV, carrier mobility, and selective tunneling properties at the bulk–contact interface through electron transport layers (like TiO_x), hole transport layers (like MoO_x), and tunneling dielectric layers (like AlO_x, SiO_x). This architecture eliminates the need for dopants, involves low-temperature processing, employs simpler and cost-effective deposition techniques, minimizes parasitic losses, enhances optical transparency, and aligns well with industrial production processes [17]. However, the drawback is the requirement for furnace annealing at temperatures ranging from 100 to 350 ºC after each intermediate deposition step. To overcome the limitations associated with furnace annealing and reduce the overall thermal budget for both CSPC Si device structures, laser annealing and rapid thermal annealing (RTA) hold immense potential. Conducting comprehensive investigations into laser annealing and RTA techniques can significantly enhance the development of high-efficiency CSPC silicon solar cells.

This dissertation studies using RTA, pulsed laser ablation, and heating to improve the performance of major c-Si PV devices like IBC-HJ, CSPC, and TMO solar cell technology. This approach addresses the limitations of traditional furnace annealing and provides a fundamental understanding of laser processing applied to photovoltaic devices. A basic understanding of laser-induced defects is essential for developing improved carrier-selective contacts.

CHAPTER 2: Theoretical background of the operation principles of Si solar cells and laser-material interactions

2.1. Silicon solar cells

A solar cell is a semiconductor optoelectronic device that absorbs the incident solar energy and converts it into usable electrical energy following the principle of photovoltaic effect. If an external load is connected to the solar cell, the electrons will flow through the load, creating an electric current. The amount of current that flows through the load depends on the solar cell's voltage, incident light intensity, and the load's resistance.

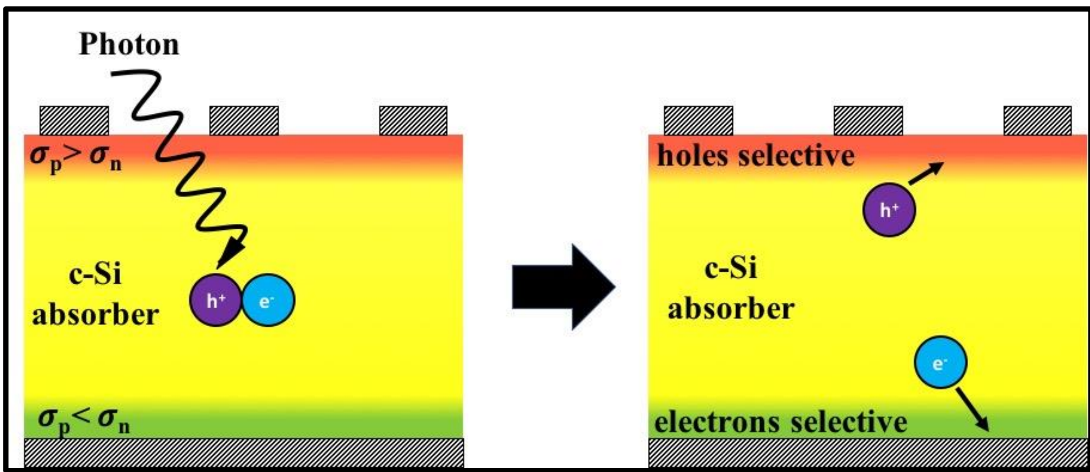


Fig. 2.1. Schematic diagram of the photogeneration of e^--h^+ pair due to a single light photon followed by separation and extraction of e^--h^+ pair.

In the Si solar cell architecture, the regions of excess carriers like holes and electrons are created by doping Si substrate with Group III elements (like Boron) and Group V elements (like Phosphorus), respectively, leading to a p-n junction. When an incident light photon energy is absorbed, an electron (e^-) is excited to the higher conduction band, leaving a hole (h^+) in its lower

valence band and generating an e^--h^+ pair. Due to the built-in potential and electric fields across the p-n junction, the e^--h^+ pair gets separated, which needs to be extracted by metal contacts before any recombination. Fig. 2.1. shows the schematic of generating and extracting e^--h^+ pairs in a bifacial Si solar cell. For optimal performance, it is essential to minimize series resistance and ensure a sufficiently high shunt resistance.

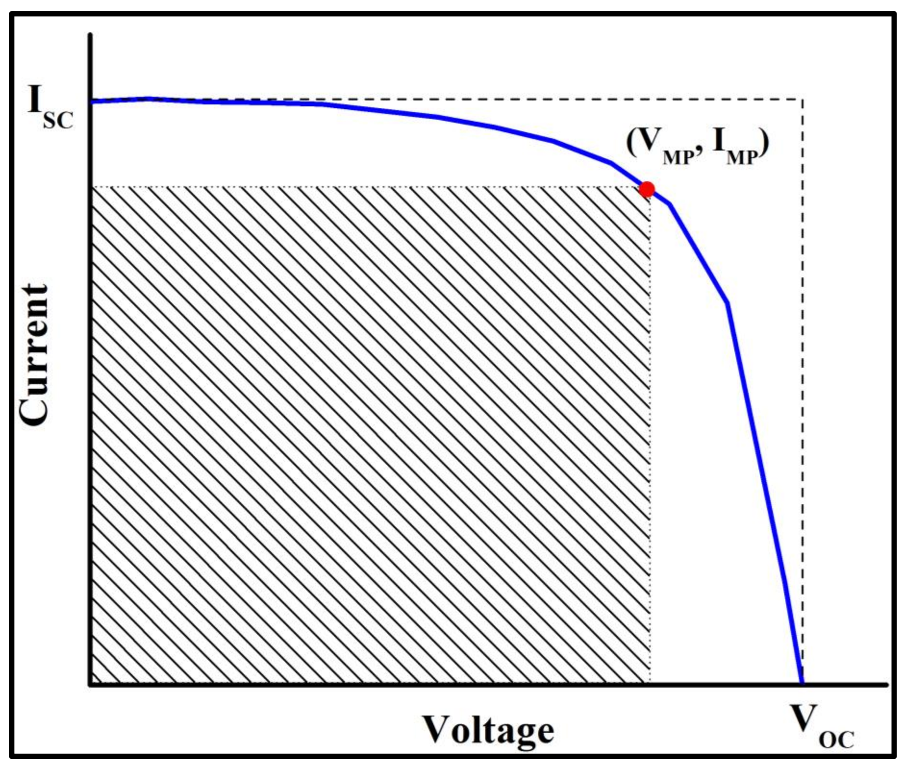


Fig. 2.2. The current-voltage (I-V) characteristics of a non-ideal solar cell under light exposure.

The solar cell performance is experimentally measured under dark and 1-sun (1000 W/m^2) calibrated illumination conditions at constant room temperature (300 K) and AM1.5 conditions. The resultant current-voltage (I-V) characteristic curve, as shown in Fig. 2.2., is used to evaluate the open-circuit voltage (V_{OC}), short-circuit current (I_{SC}), fill factor (FF), and power conversion efficiency (η).

The open-circuit voltage V_{OC} is defined as the maximum voltage output of a solar cell, occurring when there is no current flow, and it results from the inherent forward bias caused by the presence of light-generated current. The equation is as follows:

$$V_{OC} = \frac{nkT}{q} \ln\left(\frac{I_L}{I_0} + 1\right)$$

where n is the ideality factor, k is the Boltzmann constant, T is the temperature in Kelvin, q is the electronic charge, I_L is the photocurrent, and I_0 is the dark "leakage" current.

The short circuit current I_{SC} is defined as the current through the solar cell when the voltage across the solar cell is zero (i.e., when the solar cell is short-circuited), and it is equal to the photocurrent I_L magnitude in short circuit condition. The fill factor (FF) is the ratio of the maximum power (P_{MP}) from the solar cell to the product of V_{OC} and I_{SC}. The equation is stated as follows:

$$FF = \frac{P_{MP}}{V_{OC} \times I_{SC}} = \frac{V_{MP} \times I_{MP}}{V_{OC} \times I_{SC}}$$

The power conversion efficiency η is defined as the fraction of incident power converted to electricity and expressed as the ratio of the product of FF, V_{OC}, and I_{SC} to the input power P_{in}. The equation is as follows:

$$\eta = \frac{V_{OC} \times I_{SC} \times FF}{P_{in}}$$

A theoretical limit of the maximum efficiency that a single p-n junction solar cell can attain under ideal conditions is called the Shockley-Queisser limit [18]. The Shockley–Queisser limit for single junction solar cells is 29.4-33.7%, depending on the bandgap. All the practical c-Si solar cells have failed to achieve this limit due to the optical and electrical losses.

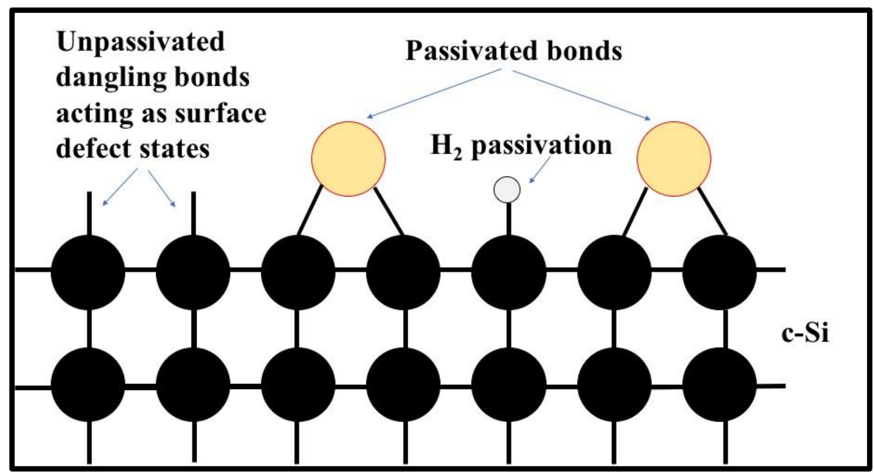


Fig. 2.3. Schematic diagram of the unpassivated surface dangling bonds, passivated surface bonds, and hydrogenated surface on a c-Si substrate.

Recombination losses are caused by the unwanted recombination of electrons and holes before reaching metallic contacts. There are four major types of recombination: radiative, Shockley-Read-Hall (SRH), Auger, and surface states [19]. In c-Si solar cells, high defect density and dopant concentration cause SRH and Auger recombination. Lastly, the dangling bonds at the terminated Si surface act as surface defect states for recombining charge carriers. Passivation of these surface states by dielectrics (e.g., oxides) and external hydrogenations (e.g., forming gas annealing) increases the minority carrier lifetime (MCL) and diffusion length, resulting in inhibition of the recombination process, as shown in Fig. 2.3. Good passivation at the surfaces and interfaces leads to higher MCL and higher efficiency of the Si solar cells. Lee *et al.* have provided the exponential relation between the lifetime τ_{eff} and iV_{OC}, which is as follows [20]:

$$\tau_{eff} = \frac{n_i^2 \exp\left(qV_{OC}/kT\right)}{J_{ph}(N + \Delta n)/qW}$$

where J_{ph} is the photo-generated current density, N is the dopant density, Δn is the excess carrier density, n_i is the intrinsic carrier concentration, q is the elementary charge, k is Boltzmann's constant, W is the wafer thickness, and T is the absolute temperature in Kelvin.

The Sinton Instruments WCT-120 Silicon Wafer Lifetime Tester is a widely used commercial instrument to characterize the performances of solar cells in terms of photoconductance and other solar cell performance parameters like implied open circuit voltage (iV_{OC}), effective minority carrier lifetime (τ_{eff}), effective surface recombination velocity (S_{eff}), sheet resistance and fill factor (FF) are calculated. This apparatus operates on the principle of a time of flight experiment. The apparatus consists of three primary components: a xenon flash lamp mounted on a stand, a sample platen containing a radio frequency (RF) assembly, and computer containing a National Instruments data acquisition card. The system is controlled through Microsoft Excel. The setup picture and the block diagram of the Sinton lifetime tester is shown in Fig. 2.4.

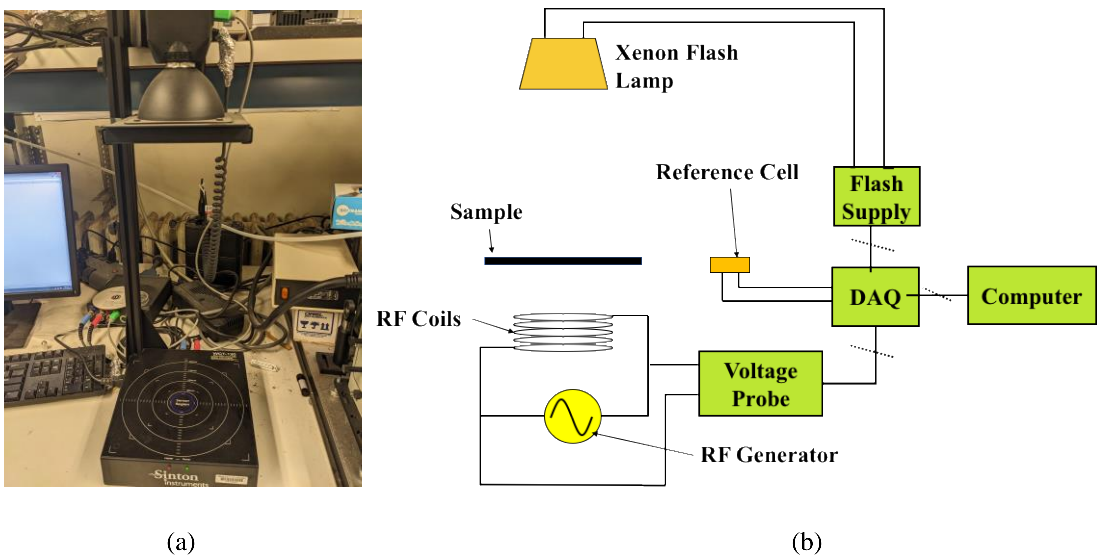


Fig. 2.4. (a) Setup and (b) block diagram of Sinton lifetime tester to measure minority carrier lifetime and iV_{OC}.

After the pulsed flash lamp exposure, the photo-induced carriers increase the photoconductance (σ) in the sample device under test (DUT) and this change is converted to a voltage signal by electromagnetic induction in the RF coils which is as follows:

$$\sigma = aV^2 + bV + c$$

where a, b and c are the calibrated constants. The resistance is calculated from the reciprocal of σ.

The induced excess carrier density (Δn) is calculated by the following equation:

$$\Delta n = \frac{\Delta\sigma}{qW(\mu_n + \mu_p)}$$

where Δσ is the photoconductance difference between light and dark conditions, W is the device thickness, q is the charge and $(\mu_n + \mu_p)$ is the combined mobilities of electrons and holes.

A reference solar cell synchronizes the conductivity measurement with the light pulse. The decay rate of the light pulse (reference solar cell voltage) is compared to that of the RF coil voltage to determine the effective carrier lifetime in the following generalized form:

$$\tau_{eff} = \frac{\Delta n(t)}{G(t) - \frac{d\Delta n}{dt}}$$

where G(t) is time-dependent generation rate of carriers. Under the quasi-steady state (QSS) illumination conditions, $\frac{d\Delta n}{dt}$ tends to be zero. Hence, in our typical carrier lifetime measurements, the details of the sample DUT like thickness, resistivity, dopant type, minority carrier density, illuminated area fraction and optical constant were provided manually.

Optical losses result from front metal contacts shadowing and reflection from the front surface and contacts. Such losses are minimized by adopting front and back surface micro-texturing, IBC architecture, and anti-reflection coatings (ARC) of dielectrics like SiN_x and SiC. The refractive index of ARC is calculated to be the geometric mean of refractive indices of two

adjacent material media. Electrical losses arise from the resistances of the electrical contacts and busbars, where the contact dimensions and material have to be optimized for maximum collection of carriers without introducing additional shadowing losses. Moreover, the metal-semiconductor Schottky barrier and Fermi level pinning can be overcome by employing heavy doping regions or carrier selective regions near the patterned contacts. Such strategies are usually used in IBC-HJ, TOPCon, and TMO-based Si solar cells.

2.2. Interdigitated Back Contact Heterojunction (IBC-HJ) Si solar cells

The IBC-HJ architecture utilizes the advantages of IBC and silicon heterojunction (SHJ) architectures. This concept was first developed at the Institute of Energy Conversion (IEC) at the University of Delaware [21]. The fabrication steps involve a lower thermal budget of ~250 ºC compared to conventional diffused homojunction cells and contacts at ~800 ºC, which causes warping and cracking of thin Si wafers. Moreover, employing PECVD over the dopant-diffusion method makes controlling the p- and n-doped regions more accessible. Consequently, the shunt resistance between the emitter and the base increases favorably.

The IBC structure permits the larger active area of light absorption by moving the front emitter and contacts to the rear side of the solar cell, thus eliminating the metal contact shadowing. It also integrates rear-side texturization for enhanced light-trapping and simplified inter-metal fingers and busbar connections. As a result, higher iV_{OC} and I_{SC} are achieved with less optical and electrical losses.

The SHJ structure utilizes the low-temperature depositions of thin layers of hydrogenated intrinsic amorphous silicon (a-Si:H(i)) on a crystalline silicon (c-Si) substrate. The structure progresses with the deposition of highly doped (p^+ and n^+) a-Si:H layers and ITO/ metallic

contacts. Due to its larger band gap (1.5-2.0 eV) and amorphous structure, the thin a-Si:H(i) layer provides good passivation to the c-Si surface, which increases the V_{OC} without significant parasitic absorption [22][23][24][25].

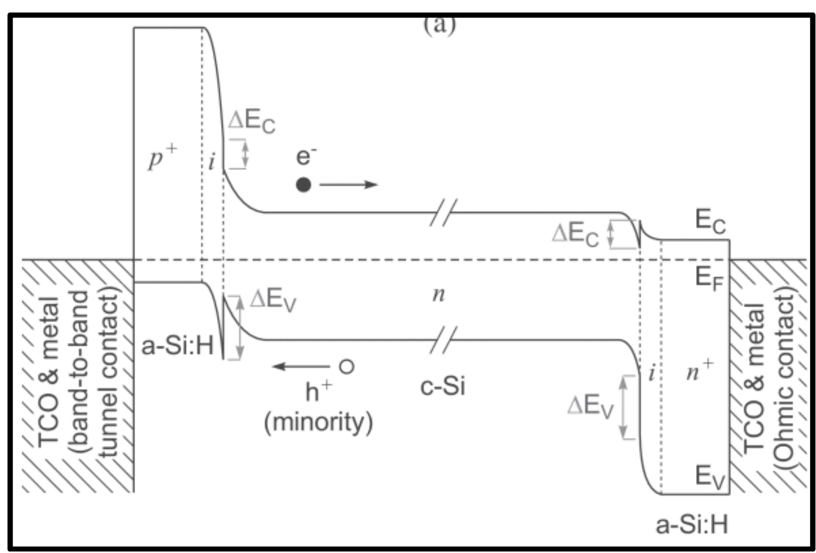


Fig. 2.5. Energy band diagram of SHJ on (n)c-Si (Reproduced from ref. [22], with the Copyright © 2013, IEEE JPV).

The energy band diagram of SHJ on (n)c-Si is showed in Fig. 2.5. Due to high doping p^+ and n^+ a-Si:H regions and thin a-Si:H(i), strong band bending in c-Si induces strong inversion layer at its surface which causes unequal energy band offsets ($\Delta E_V > \Delta E_C$). Hence, minority carriers are attracted to the surface, but majority carriers are repelled. The fill factor gets moderately affected. One such popular example using SHJ architecture is heterojunction with thin intrinsic layer (HIT) Si solar cells.

2.3. Carrier Selective Passivated Contacts (CSPC) Si solar cells

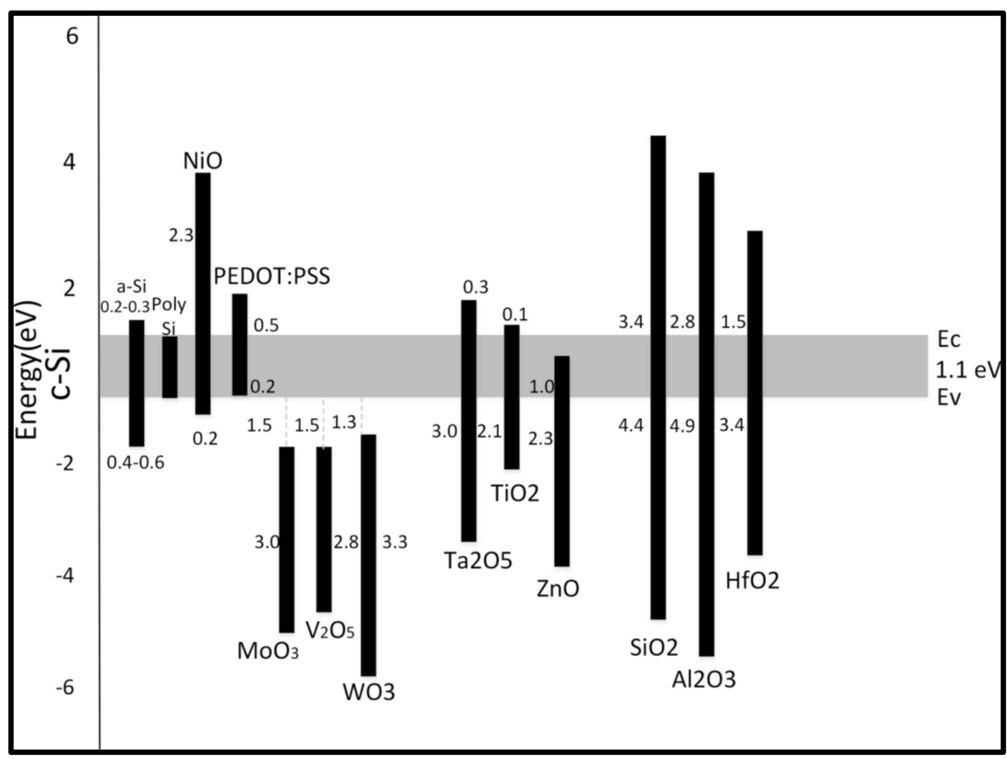


Fig. 2.6. Energy band diagram of SHJ on (n)c-Si (Reproduced from ref. [17] with the permission of Springer Link).

The carrier selective passivated contacts architecture employs asymmetric band offsets, gradient of quasi-Fermi levels, different mobilities of e^--h^+ pairs, and tunneling for charge carrier transport and separation without the actual need for an electrical field across p-n junctions [26]. It also incorporates a thin dielectric passivation layer to inhibit surface defect states and Fermi level pinning and simultaneously allow conductivity of all charge carriers [27][28]. The schematic energy band offsets of different materials' potential for CSPC Si solar cells are shown in Fig. 2.6. The CSPC Si solar cells can be broadly classified into two groups: dopant-dependent (like TOPCon) and dopant-free (like TMO-based Si solar cells).

2.3.1. Dopant-dependent TOPCon Si solar cells

The TOPCon or Polysilicon on oxides (POLO) structure implements an ultrathin interface SiO_2 layer (~1.5 nm) between highly doped poly-Si layers and c-Si substrates. The details of the TOPCon structure and fabrication process have been discussed in Chapter 5. The schematic energy band diagram of POLO contacts is shown in Fig. 2.7.

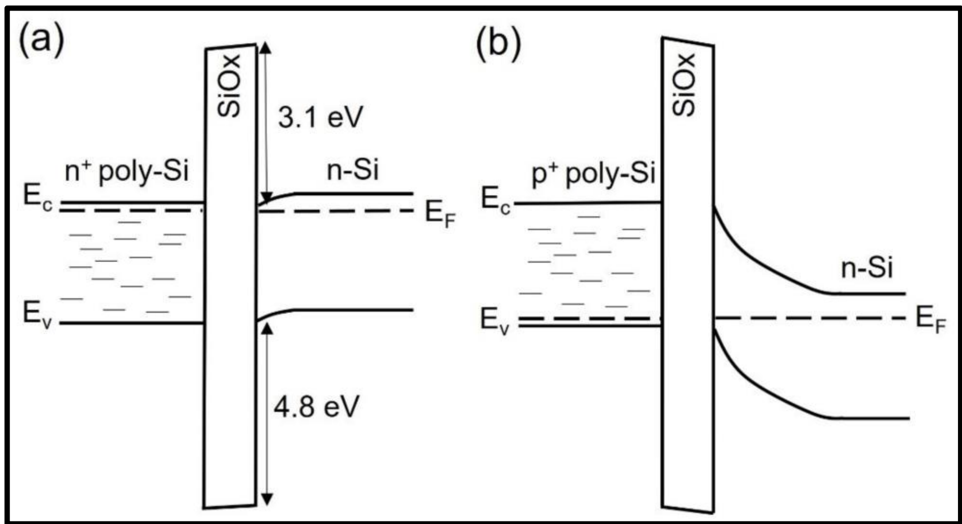


Fig. 2.7. Schematic energy band diagram of (a) n^+ poly-Si/SiO_x/c-Si and (b) p^+ poly-Si/SiO_x/c-Si POLO contacts (Reproduced from ref. [29], with the permission of MDPI Photonics).

The doped poly-Si layer allows selective conductivity of one type of carrier by inducing strong energy band bending at the c-Si surface. Such structure has high-temperature stability and undergoes traditional furnace annealing at 800-900 ºC for poly-Si crystallization, high dopant activation, and sheet resistance reductions. The dopant activation participates in charge carrier generation and provides field-induced passivation [30]. The excellent quality of the ultrathin oxide layer ensures stronger passivation and inhibits the Fermi level pinning at the direct poly-Si and c-Si interface. Moreover, the charge transport mechanism through the ultrathin oxide layer is hypothesized by two major theories: (1) quantum tunneling of charge carriers based on tunneling

layer thickness and band offsets and (2) localized current flow through oxide pinholes and non-uniform oxide thinning formed upon thermal annealing of the poly-Si/c-Si junctions [31]. Although the quantum tunneling hypothesis helps to understand the charge transport mechanism in n^+ poly-Si/SiO_x/c-Si in Fig. 2.7. (a), the pinholes hypothesis helps to understand the charge transport mechanism in p^+ poly-Si/SiO_x/c-Si in Fig. 2.7. (b).

2.3.2. Dopant-free Transition Metal Oxides (TMO) based Si solar cells

The TMO Si solar cell structure implements a dopant-free strategy where an ultrathin dielectric like AlO_x or SiO_2 layer (~1.5 nm) interface layer is employed for passivation and quantum tunneling of charge carriers and wide band gap transition metal oxides of extreme work functions (3.5 to 7 eV) for carrier-selective transport. These structures are low-temperature devices with deposition and annealing temperatures limited to 350 ºC. These layers have excellent stability, transparency, and resistance to parasitic losses. The TMO layers are classified into two major categories: (1) electron selective layer (ESL) and (2) hole selective layer.

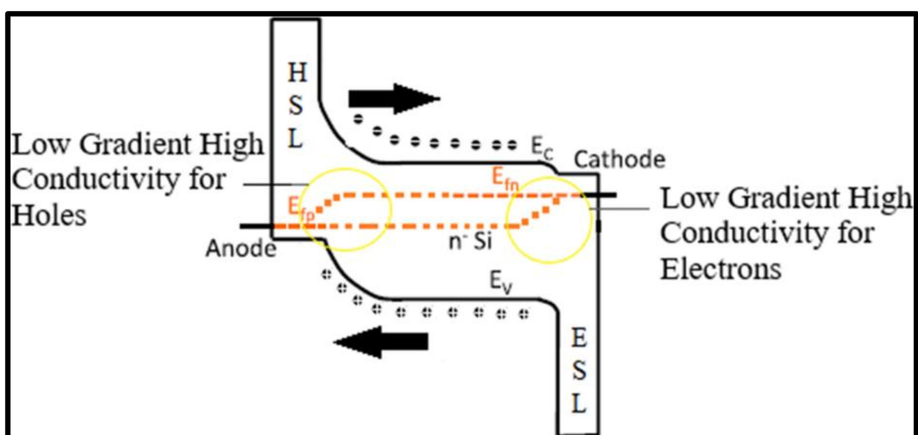


Fig. 2.8. Schematic energy band diagram of the charge separation and transport in a CSPC Si solar cell using ESL and HSL (Reproduced from ref. [17], with the permission of Springer Link).

The schematic energy band diagram of the charge separation and transport in a CSPC solar cell using ESL and HSL is shown in Fig. 2.8. The ESL uses low work function materials like TiO_x which causes downward band bending at ESL/c-Si interface, low conduction band offset (ΔE_C), higher valence band offset (ΔE_V) and large charge mobility, leading to efficient selective electron collection despite low gradient of Fermi energy. On the other hand, the HSL uses high work function materials like MoO_x, which causes upward band bending at the ESL/c-Si interface, higher conduction band offset (ΔE_C), low valence band offset (ΔE_V), and lesser charge mobility, leading to efficient selective hole collection despite less gradient of Fermi energy. The oxide sub-stoichiometry is essential to modify the atomic structures for maintaining carrier selectivity. Apart from TMOs, organic materials such as PEDOT:PSS, TAPC, and alkaline metal salts like LiF_x have also been identified as potential candidates for ESL and HSL [32][33].

2.4. The methodology of laser processing

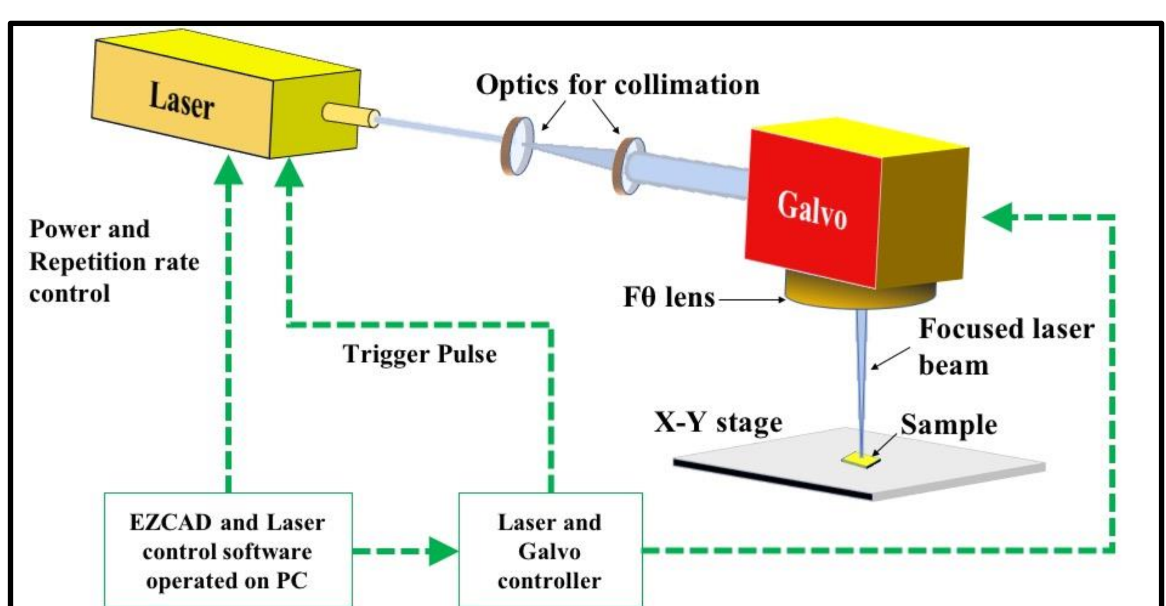


Fig. 2.9. Schematic diagram of a laser processing experimental setup.

Laser processing involves the application of high-power lasers with the help of opto-mechanical systems such as galvo scanners, translational X-Y stages, and modulation of laser light propagation by optics alignments. Fig. 2.9. shows the schematic diagram of a typical laser processing setup. The laser wavelength, pulse width, repetition rate, average and peak pulse power, beam spot size and shape, and laser fluence are some basic parameters that can be chosen according to the type of laser processing and the material. It is a versatile method of patterning, ablation, removal, cutting, drilling, melting, vaporization, and annealing materials, allowing high flexibility and spatial resolution. Fig. 2.10. shows the schematic diagram of the interaction of a focused laser beam resulting in the laser-treated region on a thin-film coated c-Si substrate.

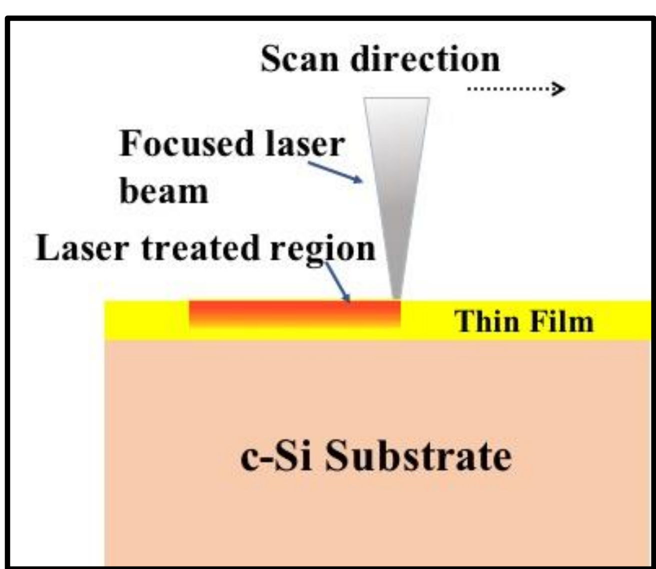


Fig. 2.10. Schematic diagram of the focused laser beam on the thin film-coated c-Si substrate.

Material properties like absorption coefficient, heat diffusion coefficient, thermal stress, nature of surface topology, and chemical state determine the process flow of the laser-material

experiments. Using beam shaper optics based on refraction, diffraction, and homogenization, the laser beam can be shaped into Gaussian, flat top-hat, or other Hermite-Gaussian modes. Single-mode laser beams can be easily collimated and focused to a tighter spot size than multi-mode laser beams. A tighter beam spot size is used at the focused position for higher laser fluence, which causes intense laser effects (like ablation and removal) and a widespread heat-affected zone (HAZ). The defocusing strategy is generally used to control and moderate laser heat effects like melting and annealing. The term' laser fluence', the ratio of laser energy (in Joules) to the spot size area (in cm^2), is used universally to quantify the amount of energy delivered per unit area of the material. Tighter spot size at focus results in higher laser fluence. Typically, collimated laser beams (~10 mm diameter) are modulated and fed to galvo scanner systems or optics setup and converged to tightly focused laser beams (20-200 μm diameter) with a 5-30 cm working distance.

The optomechanical systems of galvo scanners and translational stages help to draw intricate patterns and shapes accurately. Galvo scanners are used for patterning stationary material devices at a stage, whereas the translational stages are used for material devices under movement. They control parameters like scan speed, percentage overlap (intra-line and interline) of laser spots, and number of scans. Two basic equations are used in laser processing, which are as follows:

$$Scan\ Speed\ \left(\frac{mm}{s}\right) = (1 - Intraline\ overlap\%) \times Spot\ Size\ (\mu m) \times Repetition\ rate\ (Hz)$$

$$Interline\ Overlap\% = \left(1 - \frac{Scan\ lines\ spacing\ (\mu m)}{Spot\ size\ (\mu m)}\right) \times 100$$

Generally, continuous wave (CW) lasers are used for annealing purposes where the localized phase change in the material properties becomes the goal of the laser processing. Previously, Beyer *et al.* provided a few theoretical models and equations for simple laser annealing

setup for single film on the substrate and using a CW laser with a Gaussian beam profile to characterize the temperature in the laser spot [34]. Pulsed lasers with picosecond to microsecond pulse width have been considered for localized ablation, material removal, interfacial debonding, and many more applications with a controlled HAZ.

CHAPTER 3: Literature Review

Presently, there are two popular c-Si solar cell architectures, namely Interdigitated Back Contact Heterojunction (IBC-HJ) and Carrier Selective Passivated Contacts (CSPC), with a growing domination in the commercial c-Si PV market [14][15][16]. Depending on the presence of dopants, CSPC device architectures are divided into two sub-categories: Tunnel Oxide Passivated Contacts (TOPCon) based on dopant and dopant-free transition metal oxides (TMO) based devices. The working principles, including carrier selectivity and related materials, have already been explained in Chapter 2 of the thesis. Additionally, laser-induced selective chemical etching of Si wafers can be helpful in fabricating different Si-based devices, and it can be extended to a wide variety of materials.

3.1. Investigation of laser processing in the fabrication of IBC-HJ Si solar cells

The improvement in solar power conversion efficiency and reduction in manufacturing costs will enhance the competitiveness of silicon solar cells compared to other renewable energy sources. Among the two primary approaches, carrier selective contacts and the interdigitated back contact-heterojunction (IBC-HJ) architecture have yielded the highest efficiencies [35]. The IBC-HJ design represents a rear-contact crystalline silicon (c-Si) solar cell structure featuring strategically patterned, doped hydrogenated amorphous silicon (a-Si:H) layers, creating localized heterojunctions on the rear side [36].

In the past, traditional methods such as conventional lithography and shadow masking were employed to fabricate IBC-HJ solar cells. These methods led to increased overall manufacturing costs and introduced technical complexities [37][38][39]. In recent times, both the scientific and

industrial communities have shifted towards a more cost-effective approach, utilizing direct laser patterning with ultrashort picosecond (ps), femtosecond (fs), and short-pulsed nanosecond (ns) lasers for the fabrication of IBC c-Si solar cells. This transition has been driven by several advantages, including mask-free and contactless patterning, precise micrometer-level control over spatial and depth resolution, enhanced flexibility in pattern design, and improved production throughput [40]–[44]. It is anticipated that incorporating specific laser processing steps from this approach will significantly streamline the manufacturing process of IBC-HJ solar cells [45][46]. Nevertheless, recent reports suggest that the use of ultrashort femtosecond (fs) laser processing lead to more damage and result in decreased V_{OC}, fill factor, and efficiency when compared to nanosecond (ns) laser processing [47][48]. Furthermore, producing heterojunction (HJ) structures necessitates utilizing low-temperature processing and annealing [37].

Lately, numerous studies have examined the varying impacts of laser ablation parameters, including pulse duration and wavelength. However, these investigations have not delved into a comprehensive understanding of the thermal effects induced by lasers on each layer within the IBC architecture. Although previous reports show the electrical characterizations conducted on ns-pulsed laser processed of IBC-HJ solar cells, there is a lack of a holistic perspective on the morphological, structural, and chemical compositional aspects underlying the consequences of ns laser processing on passivation or the alterations in the IBC-HJ layers [42], [48]–[50]. Qi *et al.* explored the influence of ns pulse lasers on amorphous silicon without referencing the impact on the passivation layer [51].

While carrying out laser processing on an IBC-HJ solar cell, there is a risk of causing undesired damage and crystallization of the a-Si layer, which can substantially reduce the carrier lifetime and power conversion efficiency. Laser-induced damage results in increased

recombination losses over a considerably broader area than the actual size of the laser spot. This phenomenon occurs due to lateral carrier transport within IBC-HJ solar cells [52]. Consequently, it leads to a substantial decrease in the iV_{OC} and the MCL. This research also applies to mc-Si PERC solar cell fabrication, where high-power ps/ns pulsed lasers are used to make openings in a dielectric layer [53][54].

3.2. Investigation of the role of RTA in the fabrication of p-TOPCon Si solar cells

The Tunnel Oxide Passivated Contacts (TOPCon) Si solar cell is one of the most competitive c-Si solar cell architectures. It is known for its simple architecture, easy fabrication, high thermal stability, and resilience to post-metallization annealing. The TOPCon structure typically involves a layered structure comprising heavily doped (either B-doped or P-doped) polycrystalline silicon (poly-Si) layers and ultra-thin SiO_2 oxide layers on the doped c-Si substrate. Although the term "TOPCon" was originally coined with the assumption of tunneling current as the primary charge transport mechanism in these selective contacts, several publications have also demonstrated that the dominant current transport occurs through the pinholes that form during the annealing process [55][56]. Recent breakthroughs in research laboratories have achieved remarkable efficiencies for both p-TOPCon (based on p-type Si wafers) and n-TOPCon (based on n-type Si wafers) solar cells, with records of 26.1% and 25.8%, respectively [40][57][58].

Numerous factors and constraints in the fabrication process impact a solar cell's intrinsic open-circuit voltage (iV_{oc}) and efficiency. One of the essential steps in the fabrication of TOPCon solar cells is thermal annealing, which is necessary for dopant activation, crystallization, lower c-Si/SiO_x interfacial defects, and lower sheet resistance. Generally, annealing is performed at high temperatures (800 ℃ to 900 ℃) using traditional tube furnace anneal and conveyor belt-furnace

anneal under an inert atmosphere like N_2 [59]–[62]. Thermal processing with heating durations of tens of minutes is widely used in photovoltaic device fabrication and even in some industrial processes for $POCl_3$ diffusion. Previously, the traditional tube-furnace annealing was used for thermal annealing of n- and p-TOPCon at high temperatures under inert atmospheres, such as N_2 [59], [63]–[68]. The disadvantages of furnace annealing are an enormous thermal budget, longer annealing time, less flexibility, and lower throughput.

Due to its several advantages like choices of annealing atmosphere, better control of the annealing durations (from a few seconds to several minutes), and flexible ramping rates of heating and cooling, rapid thermal annealing (RTA) has emerged as an alternative cost-effective, high-yield processing tool for dopant activation and crystallization for n- and p-TOPCon device fabrication [69][70]–[72]. Borden *et al.* reported a RTA firing process of 30 s for their poly-Si contacts and metallization [73]. Yang *et al.* reported using RTA over the furnace to achieve 23.04% efficient Al_2O_3-capped P-doped n-TOPCon c-Si solar cells with iV_{oc} as high as 727 mV [71]. Similar studies are needed to fabricate highly efficient p-TOPCon c-Si solar cells comparable to n-TOPCon c-Si solar cells. Moreover, the RTA has been used to perform forming gas annealing (FGA) for external hydrogenation [74]. Since RTA shows such promising results, it is crucial to understand the technical hurdles at the thin-film interface level and the physics behind the thermal cycle dynamics of RTA processing to achieve optimized results equivalent to the traditional furnace annealing for p-TOPCon c-Si solar cells. It will also help understand and optimize fast laser processing for p-TOPCon c-Si fabrication since laser processing involves fast heating and cooling rates [75].

A pinhole formation mechanism has been proposed for the improvement of TOPCon device performance under furnace annealing. As the annealing temperature increases during

heating, poly-Si, ultrathin SiO_x, and c-Si substrates expand. Due to the higher thermal expansion coefficients, c-Si and poly-Si expand more than ultrathin SiO_x, which produces compressive stress in the substrate and tensile stress in the ultrathin SiO_x. This tensile stress causes concave distortion and fracture in the SiO_x, forming pinholes to relieve the accumulated tensions. On the contrary, cooling induces more inward shrinkage of both c-Si and poly-Si compared to ultrathin SiO_x, causing tensile stress in the substrate and compressive stress in the SiO_x, eventually increasing pinholes. The highly B-doped poly-Si layer on top of the ultrathin SiO_x layer provides additional field-effect passivation, provided the thickness of SiO_x is < 1.6 nm for tunneling to occur. At annealing temperatures < 850 ºC, the charge carrier transport occurs through the quantum tunneling effect as pinhole formation is minimal. At temperatures beyond 850 ºC, more pinholes form, and charge conduction through pinholes dominates the tunneling mechanism. The pinholes created in the SiO_x layer act as a gateway for the B-dopant to diffuse into the bulk Si. This diffused layer further enhances the electrical field to maximize the field-effect passivation. On the other hand, excess dopant diffusion into the bulk Si causes more considerable Auger recombination, which cannot be compensated by the enhanced field-effect passivation and leads to passivation degradation [76][30]

Yang *et al.* recently reported the heating and cooling effects of furnace annealing on TOPCon structures using the pinhole creation mechanism [77]. Hollemann *et al.* showed that significant temperature gradients increase mechanical stresses and the density of defect states at the SiO_x/c-Si interface during tube furnace annealing of P-doped poly-Si-based n-TOPCon devices [78][79]. Earlier reports also stated that cooling times influence the severity of thermal stress more than heating times [80]. Although this pinhole mechanism finding provides a good understanding of tube-furnace annealing effects, an understanding of RTA effects is still lacking as the overall

heating, holding, and cooling methodologies differ. Moreover, similar findings on the effects of slower RTA cooling rates on the minority carrier lifetime and defect densities were demonstrated in the fabrication of n^+-p-p^+ Si and p-type mc-Si devices. Still, optimization of heating rates and holding times remained unexplored [81]–[83]. It has also been suggested that the high radial-temperature nonuniformity in Si substrates causes stresses beyond its yield point due to the one-sided heating in the RTA system [84]. Earlier, Yang *et al.* had described the optimization of more prolonged RTA holding and cooling times of n-TOPCon devices, and Shou *et al.* had used similar optimization for annealing their TOPCon devices [71][85]. However, their findings were limited to PECVD P-doped n-TOPCon devices with a total RTA processing duration of ~27 min (similar to traditional tube furnace annealing durations), and the effects of heating times were not discussed. So, there is a need to understand the effects of RTA heating and cooling rates and holding time on the surface passivation quality, dopant activation, crystallization, and defect states in B-doped poly-Si-based p-TOPCon devices.

Additionally, the blister formation has been considered an important bottleneck in the fabrication of TOPCon architectures. Under intense dehydrogenation pressure, the physical rupturing of ultrathin SiO_x and poly-Si layers occurs during the tube-furnace annealing. This results in the degradation of the passivation quality [59]. Ingenito *et al.* addressed the blister formation issue during RTA processing [86]. Yang *et al.* reported blister formations during the RTA of n-TOPCon solar cells [71]. Although earlier studies have been on suppressing blisters, there is a lack of a comprehensive study on blister formation under the RTA and the role of different atmospheres, such as air versus nitrogen, for p-TOPCon structures [86][87].

In the RTA chamber, the poly-Si layer in the TOPCon device faces direct exposure to the intense lamp light and heat for the whole period of rapid annealing. In such circumstances, the

effect of intense light intensity under heat during RTA needs to be investigated. Different dielectric capping layers of SiN_x:H and Al_2O_3 and thermal annealing steps are excellent hydrogenation sources for passivating TOPCon structures using tube furnaces [88]–[92]. Moreover, dielectric layers protect TOPCon structures from spiking and damage during screen-printing metallization [93]. Therefore, it is also necessary to investigate the utility of using the dielectric SiN_x:H layer.

3.3. Fabrication of dopant-free TMO-based bifacial CSPC Si solar cells

Recent developments show that dopant-free TMO-based devices have gained attention lately in the global PV community. Such TMO devices can be classified as (i) electron-selective, (ii) hole-selective, or (iii) dopant-free asymmetric hetero-contacts (DASH), which is a combination of both electron- and hole-selective layers [94]. Yang *et al.* demonstrated 20.5% and 21.6% efficient Si solar cells based on TiO_2 as an electron-selective layer [95][96]. Dreon *et al.* and Geissbühler *et al.* reported 23.5% and 22.5% efficient HJ Si solar cells based on MoO_x as hole-selective layers, respectively [35][97]. Bullock *et al.* reported 20.7% efficient DASH Si solar cells using TiO_x and MoO_x as carrier-selective layers [98]. Hence, detailed investigations for low-cost, high-efficiency dopant-free TMO-based CSPC Si solar cells are required to continue further improvements.

The high negative charge density and higher hydrogen content make Al_2O_3 a good candidate as a passivation and hole-selective layer [99][100]. However, using Al_2O_3 in CSPC architectures comes with a trade-off between the passivation quality and tunneling ability [101]. Its thickness needs to be optimized to < 2 nm for the tunneling of charge carriers. Although there had been other earlier reports of using Al_2O_3 despite the trade-off of passivation and tunneling layer with TiO_x and MoO_x, a better understanding of the relation between the passivation quality

and tunneling phenomena in the context of CSPC devices is required to optimize the thickness of all these functional layers [102][103][104][105].

The electron-selective layer TiO_x is partially responsible for improving the passivation quality at the Si surfaces and interfaces. A thicker passivation Al_2O_3 layer makes the effect of TiO_x on the surface passivation at the c-Si interface weaker [106]. Moreover, it has been claimed that negative charges are formed in Al_2O_3/ TiO_x interfaces, which also influence the passivation quality. Titova *et al.* reported V_{OC} of 652 mV in TiO_x /SiO_2-based devices, but there was a lack of understanding of the effects of tunneling SiO_2 layer thickness on the passivation and carrier selectivity [107]. One of the best results was reported by Yang et al., who showed a high V_{OC} of 676 mV in a TiO_x /SiO_2-based device [96]. Since all these developments have been based on the SiO_2 passivation/tunneling layer, there is a need for scientific inquiry in CSPC devices based on the Al_2O_3 layer.

The holes-selective layer MoO_x has also been shown to partially improve the passivation quality at the Si surfaces and interfaces. It has been demonstrated that the stack SiO_x/ Al_2O_3 passivates the oxygen vacancy defects within the bandgap of the MoO_x [108]. Gerling et al. showed that direct passivation using MoO_x on c-Si substrate led to the iV_{OC} of 637 mV [109]. Thus, there is a need to investigate the effects of introducing Al_2O_3 for better passivation and tunneling capability. Chowdhury *et al.* reported an iV_{OC} of 726 mV in an Al_2O_3/ MoO_x contact-based CSPC device [104]. However, the carrier selectivity was overlooked since the thicknesses of Al_2O_3 layers were above 3 nm, which is not in the tunneling regime. Hence, there is a need to investigate the dynamics of Al_2O_3/MoO_x to achieve optimizations in thickness and annealing for better passivation and carrier selectivity.

Moreover, there is a lack of work on fabricating CSPC device structures employing TiO_x and MoO_x together on the Al_2O_3 layer in a single device structure. Mehmood et al. showed a simulation model using TiO_x and MoO_x on intrinsic a-Si:H layers and predicted $V_{OC} > 700$ mV [110]. Although Davis et al. had earlier shown the optimization works on Al_2O_3/ TiO_x and Al_2O_3/ MoO_x-based CSPC devices separately, no independent study was followed up for a complete CSPC device structure, combining both TiO_x as electron selective and MoO_x as hole-selective layers on Al_2O_3 passivation layer [102][103].

Lastly, these CSPC devices mentioned earlier have used furnace/ thermal annealing in their fabrication steps in N_2 or forming gas. As a result, the thermal budget and the total annealing time will increase the manufacturing cost and complexity of CSPC devices, defeating the purpose of fabricating low-cost, high-efficiency CSPC Si solar cells. Fortunately, laser processing may prove to be the game changer and overcome these limitations. The usefulness of laser processing has been discussed in Chapter 2 of the thesis. So, a scientific investigation is needed to study and optimize the laser processing method to replace furnace annealing steps in fabricating CSPC Si solar cell devices.

3.4. Investigation of laser heat-induced chemical etching (LHICE) of Si in KOH

In 2017, crystalline silicon PV modules held a dominant market share of approximately 90% in the global PV solar cell industry [1]. Recent works have reported that the laser ablation patterning method has been used to achieve recent breakthroughs in the fabrication of POLO-IBC solar cells with reported efficiency of 26.1% and IBC-HJ crystalline silicon (c-Si) solar cells with 26.3% efficiency [40][111]. However, a key challenge associated with laser processing for Si solar cell manufacturing is the emergence of laser-induced defects and thermal stress within the silicon

lattice, ultimately reducing the effective MCL and, consequently, the conversion efficiency. As a result, the widespread commercialization of high-efficiency Si solar cells hinges on the development of a cost-effective laser-patterning technique that minimizes laser-induced damage. In the semiconductor industry, a commonly employed method for isotropic etching of c-Si involves using a mixture of HF (49%) and HNO_3 (69%) in a 1:19 volume ratio [112]. Additionally, to create an anisotropic-etched micro-texture surface on c-Si, potassium hydroxide (KOH) and tetramethylammonium hydroxide (TMAH) are widely utilized [113]–[117].

Recent findings indicate that the utilization of ultrafast lasers with femtosecond (fs), picosecond (ps), and nanosecond (ns) pulse durations, in conjunction with anisotropic chemical etching employing KOH and TMAH solutions, SF_6 or HCl gases, or stain etchants such as HF–HNO_3, NH_4HF_2–H_2O, NH_4HF_2–$NaMnO_4$, has enabled the creation of diverse micro- and nano-scale structures and textures in c-Si through laser ablation processes [118]–[123] These structures encompass pores, pillars, porosified pillars, macro-pores, pin-holes, and polygonal pits. They have found application in various domains, including the production of photoluminescent porous Si (Poro-Si), enhancement of hydrophobicity and light-trapping mechanisms in c-Si solar cells and self-cleaning c-Si microelectronic devices, control of reflectance, absorbance, and emissivity in Si-based optical devices. Poro-Si has also been employed in diverse applications, such as Li-ion battery anodes and other devices sensitive to carrier traps and defect density, such as photodetectors, thin-film transistors, and LEDs [124]–[127]. Importantly, these micro- and nano-structures have broader implications beyond c-Si-based solar cells and microelectronics, extending to materials-based devices for novel purposes like achieving super-hydrophobic surfaces, manipulating wettability [128][129], producing unique reflected colors [130], affecting tribological behaviors [131], and preventing bacterial biofouling [132]. Notably, when the energy

delivered by the laser to c-Si exceeds the phase explosion threshold (>0.9 Tc, where T_c = 7925 K represents the thermodynamic critical temperature of silicon), it triggers an explosion-like release of ionized surface material due to explosive stress, resulting in the formation of micropores on the silicon surface, as described by Ji *et al.* [120]. However, these processes introduce significant defects to both the surface and bulk of c-Si wafers or substrates due to extensive laser ablation and high-temperature chemical etching. In fact, the direct interactions between the laser and crystalline silicon appear to have a more pronounced effect than the interactions involving laser-assisted chemical etching. Insufficient characterization of laser-induced damage and inadequate investigation into the preservation of MCL have been noted in previous studies. Furthermore, the role of microsecond (µs) pulse width lasers in low-temperature laser-assisted KOH etching of c-Si and their impact on MCL alteration remain poorly understood. While some studies have reported laser-assisted photochemical wet etching methods where exposure to specific laser wavelengths with optimized intensities selectively enhances the photochemical etch rate at localized regions, this approach is limited to semiconductor materials like c-Si and GaAs, as it relies on the generation of electron-hole pairs and necessitates the use of toxic etchants like HF [133][134].

In the realm of semiconductor processing, it is a well-established fact that the etching rate of KOH increases significantly as the temperature rises, following an exponential pattern described by the Arrhenius equation. The most favorable temperature range for this process typically falls between 80-100 °C. To illustrate, when employing a 30 wt% concentrated KOH solution, the etching rate of c-Si (100) at 20 °C is approximately 1.44 µm/hour (equivalent to 24 nm/min). However, at 80 °C, the etch rate escalates to around 79 µm/hour (equivalent to 1316 nm/min) [115]. The mechanism behind silicon etching with KOH involves a two-step sequential oxidation

and etching reaction. During the initial, rate-determining oxidation step, H-terminated Si atoms on the surface undergo oxidation, transforming into OH-terminated Si atoms due to the presence of OH- ions from the KOH aqueous solution. In the presence of H_2O, this process induces polarization and weakens the chemical bonds between silicon and oxygen. Consequently, Si atoms are removed in the form of $Si(OH)_4$ complexes. The rate of this oxidation process can be enhanced within the optimal temperature range of 80-100 °C. Furthermore, KOH is a highly advantageous silicon etchant due to its non-toxic nature, cost-effectiveness, widespread use, straightforward etching setup requirements, ability to achieve high silicon etch rates, significant anisotropy, moderate Si/SiO_2 etch rate ratio, and the generation of minimal surface roughness during the etching process.

Traditionally, the primary objective when creating surface textures and pyramidal shapes on c-Si surfaces has been to enhance light trapping, a process commonly achieved using alkaline etchants like KOH, NaOH, and TMAH to reduce surface reflectivity to as low as 6% [135]. Importantly, the KOH etching and texturizing of c-Si do not inflict significant damage on the surface quality. Additionally, the surface passivation of the etched or textured c-Si can be further improved by depositing stack layers of SiO_2/Al_2O_3 and SiN_x/Al_2O_3 [136]–[138]. In the context of fabricating interdigitated back-contact (IBC) solar cells, surface passivation can also be accomplished by depositing a plasma-enhanced chemical vapor deposition (PECVD) stack consisting of a-$Si/SiO_2/SiN_x$ (aSON) layers onto the textured c-Si, leading to the attainment of effective surface recombination velocities (SRVs) below 1 cm/s [139].

Notably, Zielke *et al.* reported measuring a very low saturation current density of (174 ± 11) fA/cm² on PERC cells after KOH pyramidal texturization, followed by the deposition of atomic-layer-deposited AlOx, indicating improved contact passivation [140]. Werner *et al.*'s

study demonstrates the achievement of a low SRV below 2.9 cm/s with a 10 nm thick Al_2O_3 layer, deposited through a spatial atomic layer deposition (ALD) process, on KOH-etched n-type (Cz) silicon [141]. Therefore, it is crucial to maintain an optimal temperature range (80°C to 100°C) to facilitate KOH etching and texturization effectively. Laser-induced KOH etching can facilitate the etching process on the c-Si surface at a higher control and selectivity. Fast laser processing expedites temperature rise within a small spatial resolution, which allows pattern control at a higher throughput.

Furthermore, a similar approach of laser-assisted temperature-selective micro-etching and texturization can be applied to various materials. For instance, controlled etching of steel in a mixture of $FeCl_3$ and aqueous solution containing $FeCl_3/HCl/HNO_3$ can be used to achieve super-hydrophobicity, manipulate wettability, and produce surface-reflected colors [129], [130], [142], [143]. This technique can also be employed on Ni–Co alloys on steel in a 30% v/v HCl/ethyl alcohol etchant to improve tribological properties [131][144], among other applications. Moreover, this methodology has the potential to surpass the extensive electrochemical etching process in Poro-Si texturization, which often leads to a reduction in carrier lifetime [145].

CHAPTER 4: Laser processing of Interdigitated Back Contact Heterojunction (IBC-HJ) Si Solar cells

In this chapter, we describe the results of a thorough investigation and characterization of the impact of ns laser processing parameters on the various layers of an IBC-HJ architecture. The n- and p-layers for the IBC-HJ structure were selectively patterned with minimal laser-induced damage. The laser ablation of the top sacrificial a-Si:H (p and i) layers on top of SiN_x and a-Si:H (n) layers was carried out, exposing the SiN_x layer underneath. The exposed SiN_x layer was later chemically etched away, exposing the a-Si:H (n) layer. This allowed the deposition of metal contacts on the a-Si:H (n) layer. Different analytical techniques such as micro-photoluminescence (μ-PL), quasi-steady-state photoconductance MCL (QSSPC MCL), optical imaging and ellipsometry, Essential Macleod optical simulations, surface and cross-section morphology by scanning electron microscopy (SEM) and focused ion beam (FIB) SEM, surface elemental and chemical characterizations using energy-dispersive X-ray spectroscopy (EDS), Raman spectroscopy, and high-resolution X-ray photoelectron spectroscopy (HR-XPS) have been used for this study. The simulated color chart based on optical interference was generated to be a reliable, independent scientific tool to identify the variation in thickness of individual layers because of laser processing in an IBC-HJ architecture. The efficacy of the approach of indirect laser patterning using UV-laser lithography, photoresists, and selective chemical etching was investigated.

4.1. Experimental

A. Fabrication of IBC-HJ Si Solar cells

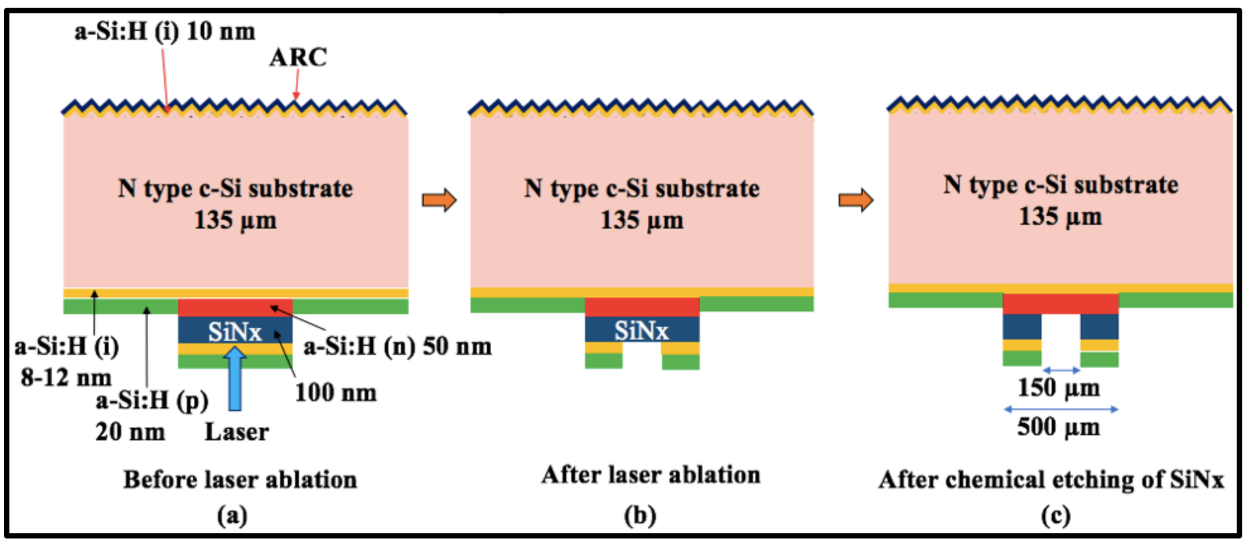


Fig. 4.1. Schematic diagram of laser processing steps comprising of (a) starting IBC-HJ test device structure before direct laser ablation, (b) after laser ablation of top sacrificial a-Si:H layers, and (c) after chemical etching of underlying SiN_x layer.

Fig. 4.1. illustrates the diagram of the laser processing steps performed on the rear side of the test structures, which were used in our study to simulate the effects on an IBC-HJ device. In Fig. 4.1. (a), a cross-sectional schematic of the IBC-HJ test structure used in our study is depicted. The upper layers of a-Si:H (p and i) are laser-ablated, exposing the SiN_x layer beneath them. Subsequently, the SiN_x layer is chemically etched to reveal the a-Si:H (n) layer underneath, facilitating the deposition of metal contacts onto the a-Si:H (n) layer through a mask. The development of such a structure with minimal laser damage is crucial for achieving high-efficiency laser-processed IBC-HJ cells [52][46]. These structures were manufactured on 135 μm n-type Cz Si wafers with a <100> orientation and a resistivity ranging from 1 to 8 Ω·cm. Before texturization, the wafers underwent cleaning using a standard procedure described in our previous work [146].

The pyramidal textures on the front side of the wafer were created using anisotropic silicon etchant tetra-methyl-ammonium-hydroxide (TMAH). To prevent texturization on the rear side intended for laser processing, a silicon nitride encapsulation layer was applied. The wafers featured a passivating intrinsic amorphous silicon (a-Si:H) layer with a thickness of 10 nm on the front side and varying thicknesses of 8–12 nm on the rear side, achieved using DC-plasma-enhanced chemical vapor deposition (DC-PECVD), as detailed elsewhere [147]. Table 4.1. provides information on the different a-Si:H (i) thicknesses used in all the samples. To minimize reflection losses at the front surface, SiN_x (80 nm)/SiC (20 nm) layers were deposited as the antireflection coating. On the semi-polished rear side, 50 nm of n-doped a-Si:H (n layer) and 100 nm of SiN_x layers were deposited in a finger pattern using a Si shadow mask. A thin layer of deposition was observed beneath the shadow mask due to plasma leakage during the PECVD process. This unintentional deposition of a-Si:H (n) layer caused by plasma leakage was selectively removed using 25% TMAH or 45% KOH (see Table 4.1) and followed by the final deposition step of the blanket layer stack consisting of a-Si:H (i) (10 nm)/a-Si:H (p) (20 nm).

In the case of the indirect approach of laser patterning of IBC-HJ devices, 1.4 µm thick positive photoresist (PR) AZ5214 was spin-coated on the devices at 4000 rpm. The goal of this experiment was the patterning of the PR layer by UV laser-exposure, which would be succeeded by resist development using AZ 400K solution, selective chemical etching of top sacrificial a-Si:H and SiN_x:H layers, and finally, removal of the remaining PR by AZ 100 remover. The a-Si:H and SiN_x:H layers were selectively etched by (1:100 v/v) HNA etch for 10 sec and 2% HF for 5 sec, respectively.

Table 4.1. Data for iV_{OC} and MCL after laser processing

Sample	Thickness of a-Si:H (i) layer deposited	Type of etchant	Laser Fluence (J/cm^2)	MCL before laser	iV_{OC} (mV) before laser	MCL (µs) after laser	iV_{OC} (mV) after laser
01	8 nm	KOH	0.254	332	660	302	657
02	8 nm	TMAH	0.254	807	682	786	682
03	10 nm	TMAH	0.254	1141	702	1131	701
04	10 nm	KOH	0.61	997	699	473	680
05	10 nm	TMAH	0.254	1563	707	1255	705
06	12 nm	TMAH	0.254	2190	720	1955	719

B. Laser parameter optimization

The laser setup consisted of a ytterbium fiber laser (YLP-G-10, IPG Photonics) aligned with the galvanometer scan head (SCANcube 14, SCANLAB), and scan patterns were designed in EZCad (Beijing JCZ Technology Co. Ltd). The specifications were 532 nm wavelength, pulse duration of 1.3 ns, average power of 10 W, 30 kHz repetition rate, and a Gaussian beam profile. The test samples were processed at the full-width half-maximum (FWHM) spot size of 20 µm at the focal plane, and the fluences were varied from 0.427 to 1.27 J/cm^2. The laser fluences were calculated by directly measuring its energy at different laser powers using Thorlabs energy/power meter and the laser spot size at FWHM. For each laser fluence, the scan pattern consisted of 13 mm of ~150 µm width laser ablation regions, comprising 0% overlap between laser spots.

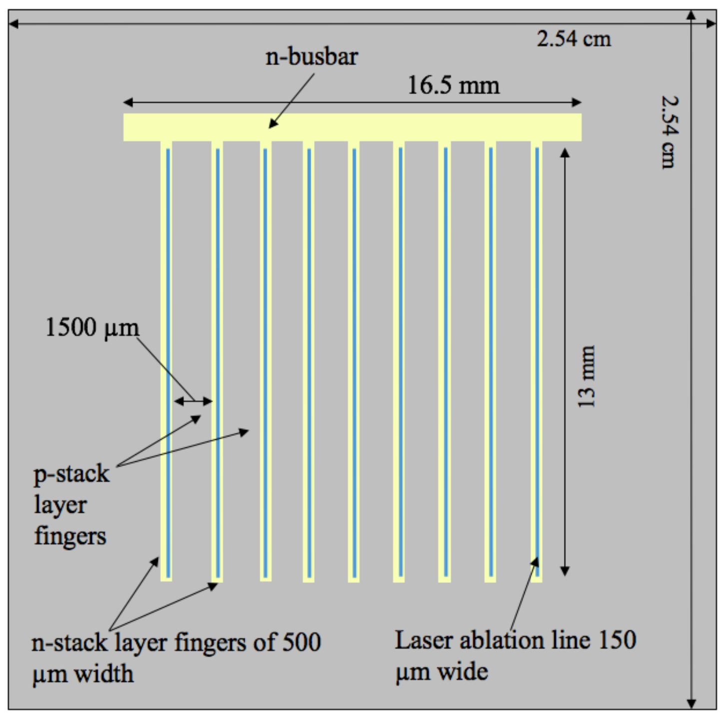


Fig. 4.2. Schematic diagram of the rear side of the laser patterned samples (top view).

The schematic diagram of the top view of a laser-patterned sample is shown in Fig. 4.2. The n-busbar connects all the n-stack layer fingers, and the rest of the isolated region acts as the p-stack layer fingers and p-busbar.

In the case of the indirect approach of laser patterning of photoresist-coated IBC-HJ devices, the UV 355 nm laser parameters were optimized to 50 kHz repetition rate, 80% overlap pulse-to-pulse, and ~150 µm line widths at the focus. The processing fluence window was optimized to 0.12-0.14 J/cm^2 for exposure.

C. Characterization Techniques:

The µ-PL configuration employed a 532 nm continuous wave (CW) laser, Melles Griot, as an excitation source, featuring an approximate spot size of 80 µm. This excitation laser's output

power was finely tuned to 70 mW using neutral density (ND) filters and quartz glass reflection to ensure precise μ-PL measurements while not impacting the sample device. The spectrometer, a Horiba Jobin Yvon iHR320, operated by SynerJY v3.5 software, along with an InGaAs detector and an SR830 DSP lock-in amplifier (Stanford Research Systems), were integral components of the setup.

Both MCL and iV_{OC} measurements were conducted through a WCT-120 Silicon Wafer Lifetime Tester from Sinton Instruments. The input of sample thickness was manually set as 0.028 cm with 3.5 Ω-cm resistivity, n-type dopant, 0.7 optical constant and generalized analysis mode. The surface morphology and elemental analysis using SEM/EDS were performed on an FEI Quanta 650 Field Emission SEM. Additionally, cross-sectional morphology characterization was accomplished using the Thermo Fisher Scientific Inc. Helios UC G4 Dual Beam FIB-SEM.

A Renishaw InVia Confocal Raman Microscope equipped with a 405 nm wavelength laser and a spot size of 1.8 μm was employed for Raman spectroscopy. The Raman scattering data were derived from an average of 15 scans, each spanning 25 sec of acquisition time, taken at specific locations on each laser-ablated spot. The high-resolution (HR) XPS, aimed at quantitative surface chemical and elemental composition analysis, was conducted using the PHI Versaprobe III Scanning X-ray Photoelectron Spectrometer, featuring an approximate spot size of 50 μm. To determine the optical constants of the device layers, a J. A. Woollam Company M-2000 Ellipsometer was employed, utilizing a focused light beam with a spot size of approximately 130 μm at a 70° incidence angle.

Before any optical images were captured, the optical microscope was calibrated in its bright-field mode following standard white balancing and color default procedures by using white

calibration disc, shown in Fig. 4.3. The white balancing was done to nullify the effects of optical artefacts introduced by the microscope itself. The light intensity was always kept constant.

Fig. 4.3. The white calibration disc used for white-balancing the optical microscope before any optical experiments conducted.

Based on the extracted experimental ellipsometry optical constant data for c-Si, a-Si:H and SiN_x:H, the simulation and forecasting of the reflected light's color chart were executed using Thin Film Center Inc.'s Essential Macleod software. Modeling of the stack layers of c-Si/a-Si:H (~60 nm)/ SiN_x:H (~100 nm)/ a-Si:H (~30 nm) was accomplished similar to the actual n-stack dimensions in Fig. 4.1. The thickness of each layer of the stack model were modified to represent the removal of each of the stack layers. The simulation additionally furnished a color chart spanning an incidence angle ranging from 0° to 70° for each layer. The choice of the illuminant source was D65, representing average daylight while adhering to the observer response defined in the CIE 1931 standard [148]. D65, as specified by the International Commission on Illumination

(CIE), serves as a standard white light illuminant characterized by a correlated color temperature (CCT) of 6504 K. The color-mapping function CIE 1931, known as the standard colorimetric observer, captures the typical chromatic response of an average human within a 2° arc within the fovea. These simulated colors were compared to the calibrated white-balanced optical images. Later, the reflectance spectrum of the complete n-stack layers was simulated, which was later compared to the experimental reflectance data from spectrophotometry.

4.2. Results and discussion

In the IBC-HJ architecture, a-Si:H (i) serves as a passivation layer for the device, providing protection and enhancement. However, any laser-induced damages, such as the generation of defects and crystallization during ns pulsed laser patterning, can potentially decrease the Minority Carrier Lifetime (MCL) and the implied open-circuit voltage (iV_{OC}). Various characterization techniques, including carrier lifetime measurement, optical imaging, surface morphology assessment, and chemical composition analysis, offer both qualitative and quantitative insights into the impact of laser processing on the different layers within the IBC-HJ test structure.

Following the laser processing step, the uppermost layer of a-Si:H is removed, exposing the underlying SiN_x. This SiN_x layer is selectively chemically etched using a 10% HF solution for a duration of 6 minutes. A dry resist layer is applied to safeguard the front Anti-Reflective Coating (ARC) during HF etching, which is subsequently eliminated using 1-methyl-2-pyrrolidone (NMP).

With the underlying a-Si:H (n) layer now accessible for contact purposes, an interdigitated pattern of p and n metals is formed using a shadow masking technique and e-beam evaporation of aluminum (Al) with a thickness of 1 μm. This final step completes the process of transforming the test structure into a fully realized IBC-HJ solar cell.

A. Passivation quality characterization

It is well known that impurities, dangling bonds, atomic vacancies, and imperfections on the non-passivated silicon surface create intermediary trap levels for electron-hole pairs (e^{-}-h^{+}). Similar defects emerge during laser processing, impacting the overall performance of IBC-HJ solar cells. The effectiveness of passivation can be assessed through measurements of quasi-steady-state photoconductance (QSSPC) carrier lifetime and the use of the μ-PL technique. These techniques serve as dependable means to quantify the extent of passivation quality.

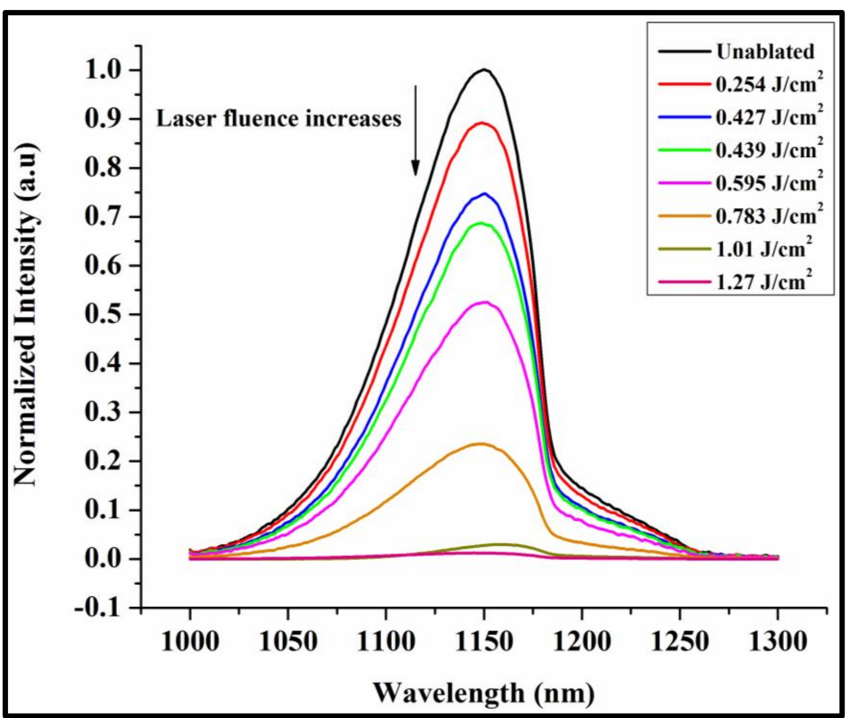


Fig. 4.4. μ-PL data for different laser fluence ablations. Each of the measurements was an average of over 20 scans.

For passivated c-Si substrates with texturing on both sides, photoluminescence (PL) is emitted around the wavelength range of 1150–1170 nm [149]. Fig. 4.4. illustrates the μ-PL data at

various laser fluences. The PL signal attenuated as the laser fluence was elevated from the unablated state to a condition of 1.27 J/cm². All the actual IBC-HJ solar cell test samples, except for sample #04, were processed at the laser fluence of 0.254 J/cm². In Table I, it can be observed that there was a slightly marginal reduction in both implied open-circuit voltage (iV_{OC}) (~3 mV) and Minority Carrier Lifetime (MCL). These measurements were taken at a minority carrier density (MCD) of 1×10^{15} cm^{-3}. Sample #04 underwent laser processing at a higher fluence, 0.61 J/cm², resulting in a notable decrease of 19 mV in iV_{OC} and a reduction of approximately 500 μs in MCL.

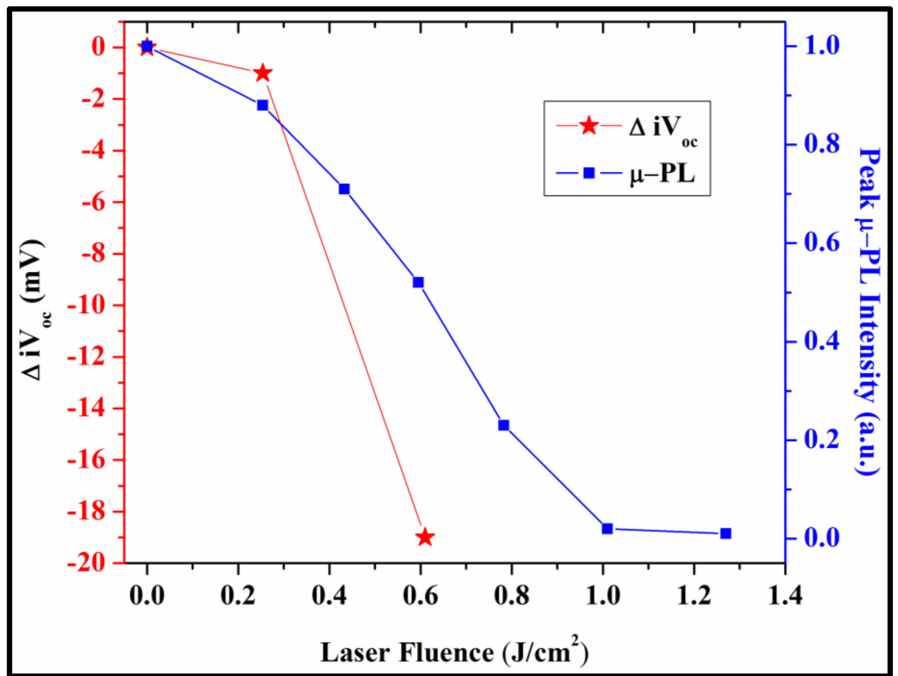


Fig. 4.5. Peak μ-PL intensity and ΔiV_{OC} versus laser fluence.

While QSSPC characterization is commonly employed for accurate lifetime and iV_{OC} assessments in IBC devices, a recent report has suggested potential artifacts influencing lifetime results at MCD exceeding 1×10^{15} cm^{-3} due to lateral inhomogeneity in the IBC structures [150].

The μ-PL technique was effectively conducted to identify the optimal laser processing condition for IBC-HJ solar cell production. Fig. 4.5. demonstrates a relationship between μ-PL intensity and the change ΔiV_{OC} with each incremental rise in laser fluence. As the fluence increased, both the peak μ-PL intensity and iV_{OC} experienced a decline.

B. Optical characterization

The optical characterizations, including optical imaging, ellipsometry, and spectrophotometry, offer valuable perspectives into absorption depth, reflectance, and transmittance alterations for each layer at specific wavelengths. Consequently, they enhance our comprehension of surface modifications following laser processing. A noteworthy facet of these analyses is the utilization of a color identification chart, which serves as a reliable, independent method for gauging adjustments in layer thickness and optical properties during laser processing.

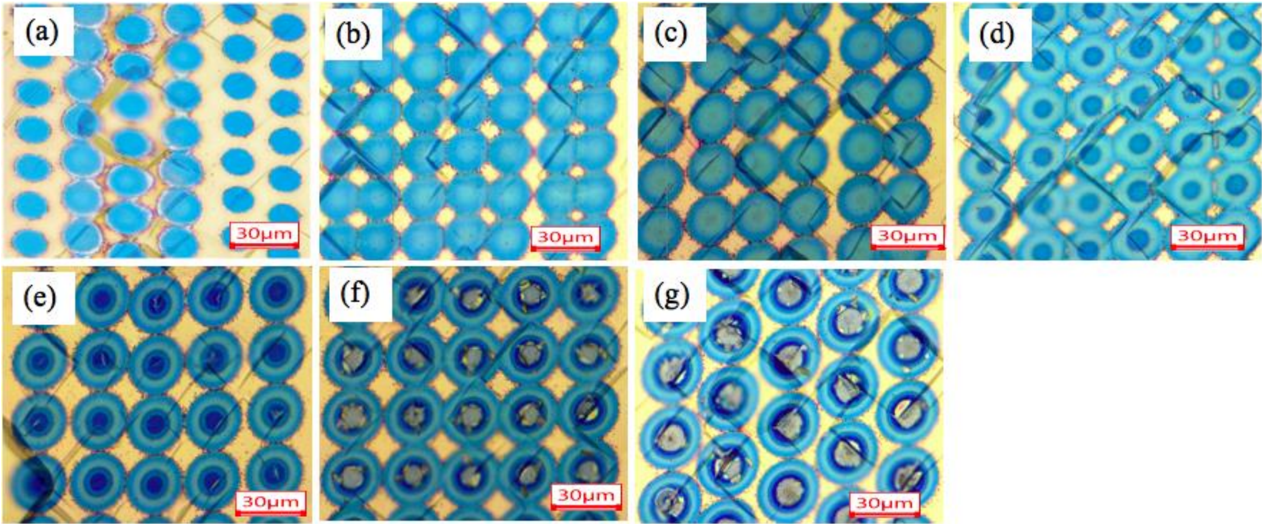


Fig. 4.6. Optical images of different laser processed regions at different laser fluences (a) 0.254 J/cm^2, (b) 0.427 J/cm^2, (c) 0.439 J/cm^2, (d) 0.595 J/cm^2, (e) 0.783 J/cm^2, (f) 1.01 J/cm^2 and (g) 1.27 J/cm^2. All the pictures were taken with a scale of 30 μm.

The various surface modifications and shifts in color resulting from distinct laser fluence processing settings are shown in Fig. 4.6. Notably, the SiN_x layer exhibited more pronounced concentric fringe formation as the laser fluence increased from 0.254 to 1.27 J/cm². Moreover, the extent of laser-induced damage at the focal point of the laser-ablated spots became more conspicuous with higher fluence levels.

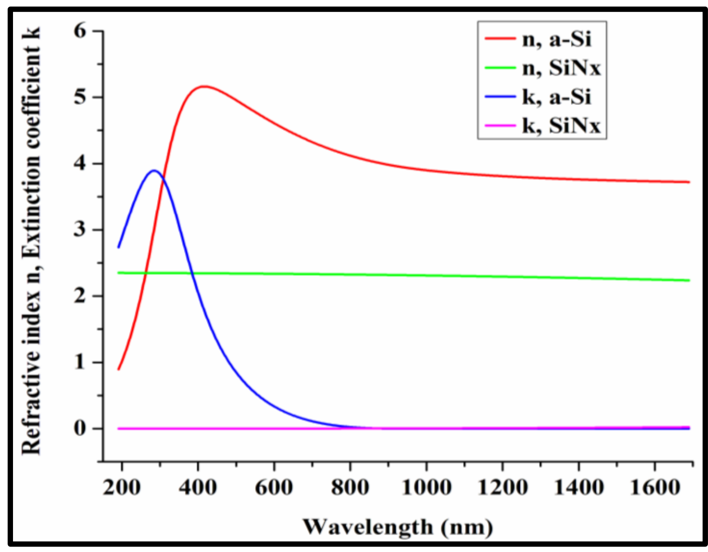


Fig. 4.7. Optical constants n, k vs. wavelength (nm) curve of the IBC-HJ test structure.

The quantitative foundation for designing and interpreting characteristics in multilayer stacks and tandem-structure devices is based on the intrinsic material optical constants. The optical constants, refractive index (n), and extinction coefficient (k) are instrumental in simulating the reflections from various stack layers, aiding in determining approximate thicknesses for laser-ablated and etched layers. The optical constants were precisely determined using an optical ellipsometer, accounting for a roughness of 5 nm and employing a 70° incidence angle. The results are depicted in Fig. 4.7. The acquired n and k values were then integrated into Essential Macleod software, facilitating simulations of normalized reflectance and color representation. Through this

simulation, the overall thickness of the uppermost a-Si:H layers was calculated to be approximately 26 nm, notably close to the anticipated 30 nm thickness for a-Si:H layers deposited via PECVD. The optical reflectance measurements were carried out using an optical spectrophotometer. Although both the experimental and simulated normalized reflectance curves closely align, as evidenced in Fig. 4.8., differences in the magnitudes of normalized reflectance stem from the semi-polished textured surface. Notably, the simulations were conducted with the assumption of a smooth surface.

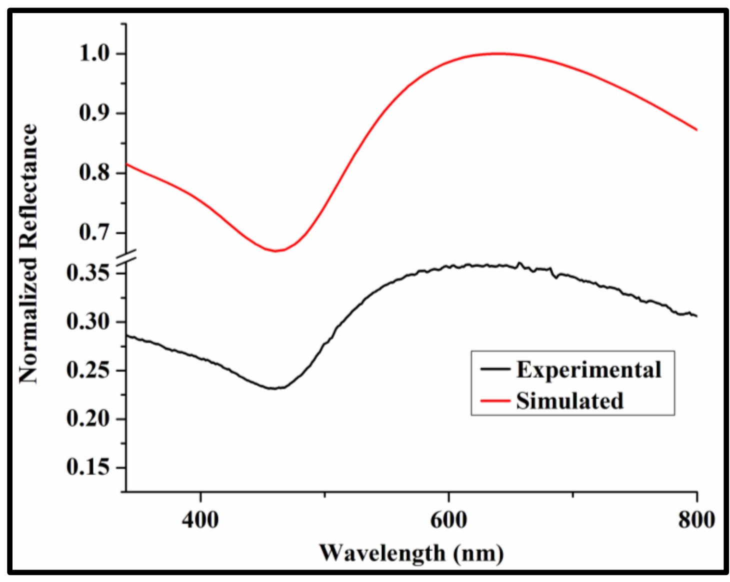


Fig. 4.8. Normalized reflectance versus wavelength (nm) curve for IBC-HJ test structure.

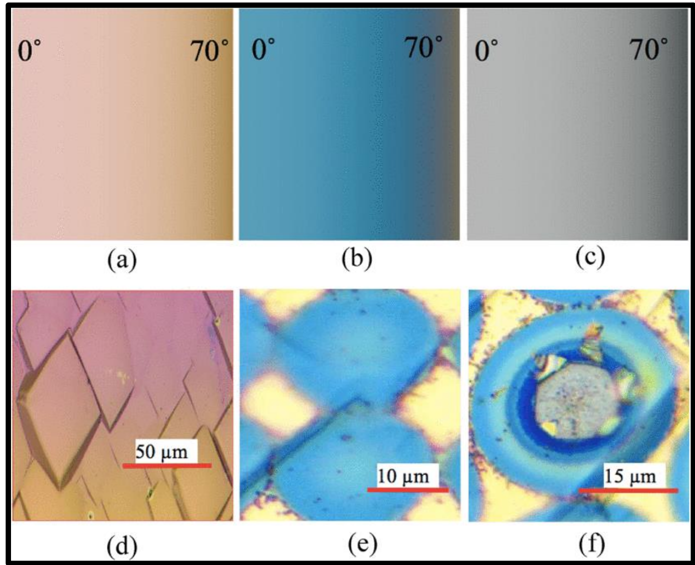


Fig. 4.9. Simulated colors for test structures (a) before any laser ablation, (b) after laser-ablation of sacrificial layers which expose SiN_x layer, and (c) underlying c-Si exposed due to the higher laser fluence, and (d) to (f) their respective optical images of IBC-HJ test structure.

The optical color chart simulations were carried out after reflectance simulation. In Fig. 4.9. (a)–(c), the simulated colors (at incidence angles of 0°–70°) for the IBC-HJ test structure are presented: firstly, prior to any laser ablation; secondly, following the laser ablation of sacrificial layers exposing the SiN_x layer; and thirdly, due to the higher laser fluence, uncovering the underlying c-Si. Correspondingly, Figures 4.9. (d)–(f) display the actual optical images of these scenarios. Remarkably, the predicted colors closely align with the actual optical colors. By comparing the distinct projected colors with the observed optical colors, it becomes feasible to deduce alterations in the thickness of laser-processed layers. Thus, the color identification chart emerges as a dependable tool for estimating the thickness of specific layers, identifying their removal and controlling the laser fluence.

C. Surface topology and cross-sectional morphology characterization

Utilizing high-resolution SEM imaging enables the analysis of surface topography, structure, and composition modifications resulting from laser interactions. This further corroborates the optical images and color chart findings discussed earlier. The top-view SEM images were captured using a secondary electron (SE) mode at a beam energy of 15 kV.

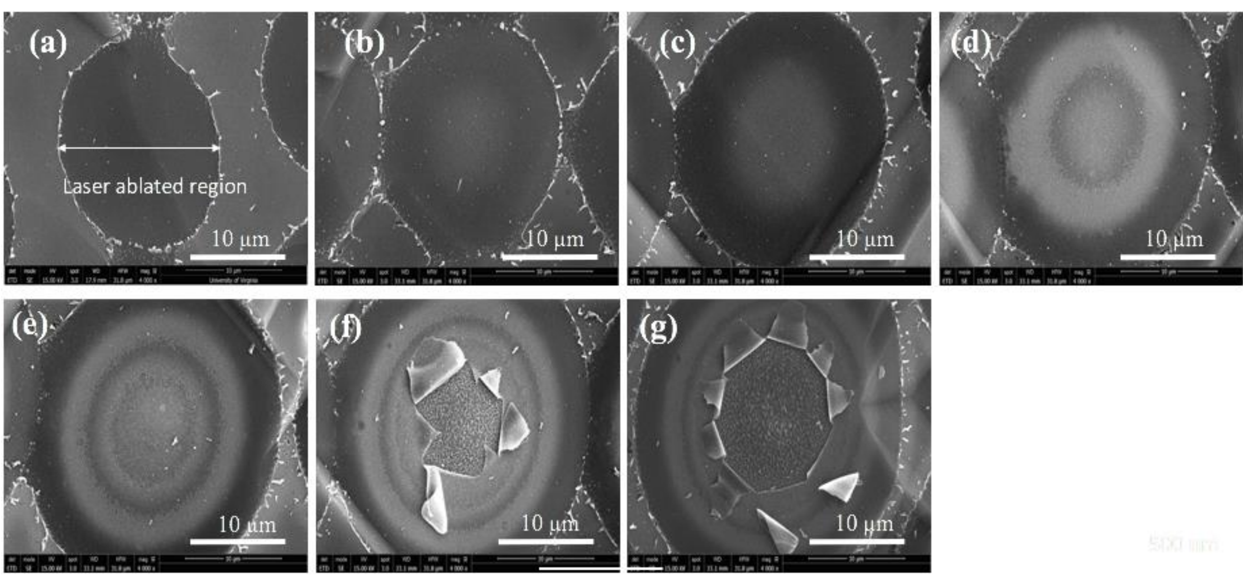


Fig. 4.10. Top-view SEM images of ablations at different laser fluences of (a) 0.254 J/cm^2, (b) 0.427 J/cm^2, (c) 0.439 J/cm^2, (d) 0.595 J/cm^2, (e) 0.783 J/cm^2, (f) 1.01 J/cm^2 and (g) 1.27 J/cm^2.

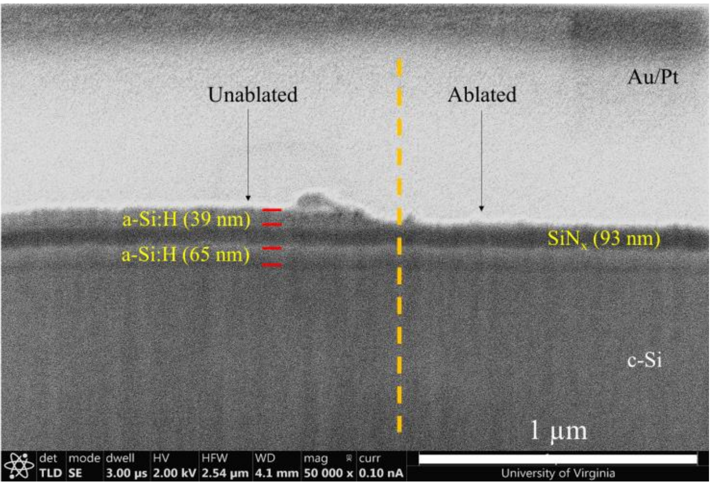


Fig. 4.11. FIB-SEM image of the cross-section at the edge of an ablated spot at the fluence 0.254 J/cm^2.

In Fig. 4.10., these top-view SEM images illustrate the emergence of circular ring patterns on the SiN_x layer relative to the laser fluence. For fluences surpassing 1.01 J/cm^2, the uppermost SiN_x layers experience ruptures and detachment at the central region of laser impact, an observation subsequently confirmed by our EDS analysis. Given that SiN_x is transparent to the 532 nm laser, the fluence aligns with the threshold at which Si undergoes melting [151][152]. In this context, at the core of the laser beam, the subjacent a-Si:H (n and i) layers attain a molten liquid state for a duration sufficient to enable the accumulation and release of H_2 gas pressure [153], potentially accompanied by a-Si vapor. This localized melting of a-Si is a consequence of the laser-induced heat, leading to the melting of the surrounding a-Si in proximity to the laser spot.

Fig. 4.10. (a) depicts a minimal removal of the upper sacrificial a-Si:H layer at a fluence of 0.254 J/cm^2. A more pronounced laser-based removal of the a-Si:H thin film is illustrated in Fig. 4.10. (b) at a laser fluence of 0.427 J/cm^2, with a reduced debris formation. As the laser fluence is incrementally raised, discernible ring fringes appear on the surface, as evidenced in Fig. 4.10. (c) and (d). With higher laser fluences, the top sacrificial a-Si:H layer is ablated, and the n-layer beneath the SiNx absorbs a portion of the laser energy. The SiN_x layer's transparency to the 532 nm laser wavelength results in predominant light absorption within the n-layer [154]–[156]. This absorption leads to the heating, melting, and vaporizing of the n-layer, accompanied by the liberation of H_2. The vapor absorbs a fraction of the laser energy, attaining elevated temperatures that induce ionization and the formation of plasma [157][158]. Fast localized heating due to laser action, along with plasma creation, triggers an expanding shockwave, generating visible fringes upon the solidification of the material. The presence of the SiN_x overlayer significantly amplifies the generated pressures compared to scenarios without the overlayer. At

even higher laser fluences, the plasma pressure intensifies, ultimately leading to the rupture of the SiN_x layer, as depicted in Fig. 4.10. (f) and (g). This interpretation is further substantiated through EDS and XPS characterization methods.

The FIB-SEM imaging allows the characterization of the cross-section morphology after removing materials by the ion-milling process. The gallium source was used for ion milling, and the device was coated with 10 nm of Au and a ~1.5 μm thick layer of Pt prior to imaging. In Fig. 4.11., the FIB-SEM image shows the cross-section of the laser-ablated region at the fluence of 0.254 J/cm^2.

D. Surface elemental and chemical characterization

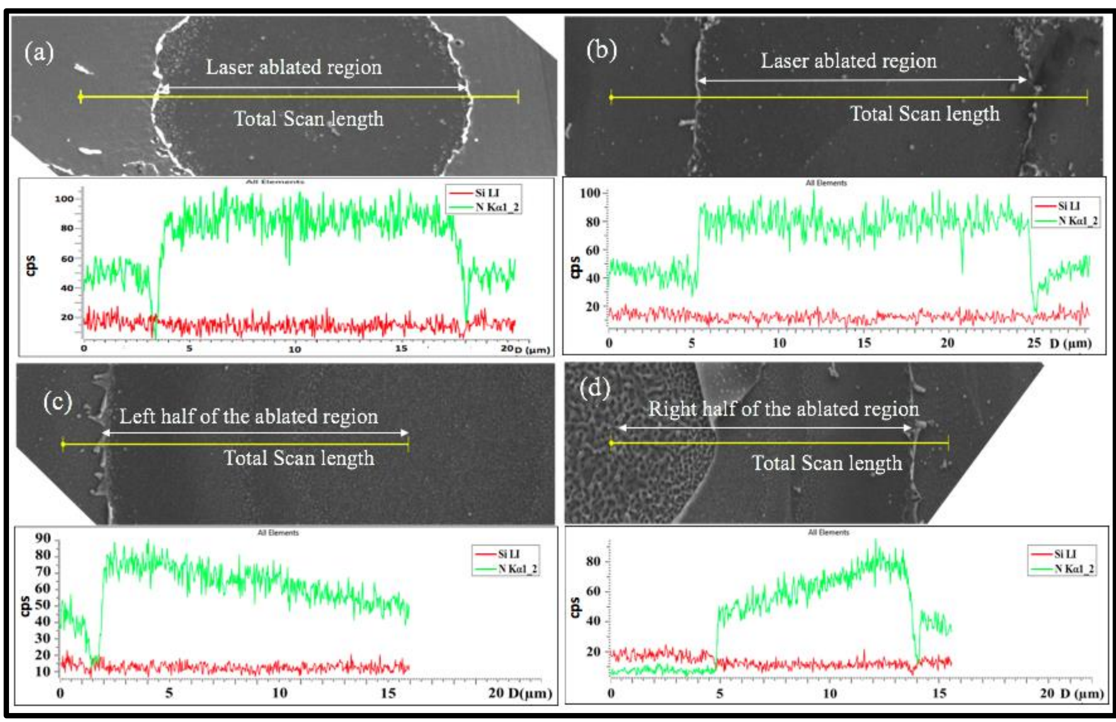


Fig. 4.12. Line-map EDS spectra for N Kα1 at different laser fluences of (a) 0.254 J/cm^2, (b) 0.427 J/cm^2, (c) 0.595 J/cm^2, and (d) 1.01 J/cm^2. The green spectrum denotes N (Kα), and the red spectrum denotes Si (LI).

It's important to highlight that line-mapping EDS spectra were acquired at a beam energy of 5 kV. This choice was deliberate to exclusively capture the nitrogen element N (Kα1) (depicted by the green-colored spectrum) along the scan length D, corresponding to the presence of the SiN_x layer. In Fig. 4.12. (a)–(d), an observable trend emerges: an increase in laser fluence correlates with a noticeable dip in the N-peak situated at the center of the laser impact, signifying a reduction in the SiN_x layer's thickness. Notably, at laser fluences of 0.254 and 0.427 J/cm² (as demonstrated in Fig. 4.12. (a) and (b)), the N (Kα1) profiles display considerable similarity, indicating the removal of the upper a-Si:H layer and the exposure of the underlying SiN_x layer. Subsequently, as depicted in Fig. 4.12. (c) and (d), where laser fluences of 0.595 and 1.01 J/cm² were utilized, the line mapping was restricted to half of the laser spot area. Notably, the N peak gradually diminishes, ultimately plummeting at the center. This observation signifies the thickness of the exposed SiN_x tapers as one progresses toward the spot's central region. This finding indicates that, for fluences exceeding 0.427 J/cm², a distinct gradient in SiN_x thickness manifests, ultimately leading to its rupture.

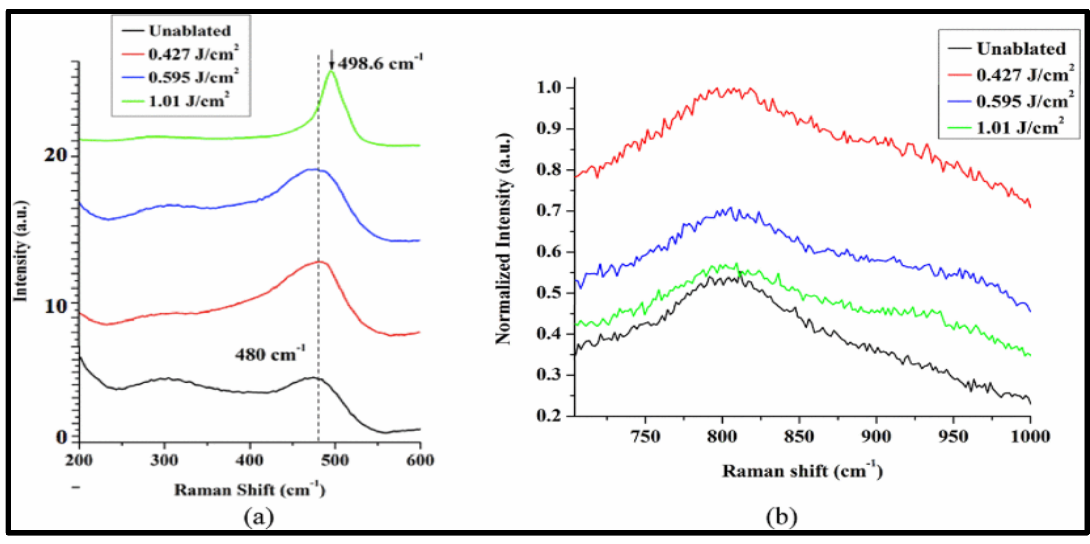


Fig. 4.13. (a) Raman spectra of underneath a-Si:H passivation layer undergoing amorphous to polycrystalline phase under various laser fluences. (b) Raman spectra of decreasing SiN_x under different laser fluence conditions.

Employing the refractive index values (n and k) extracted from Fig. 4.7., the computed absorption depth for the 405 nm blue wavelength Raman excitation laser in the a-Si:H layer (n = 5.155; k = 1.954) is approximately 16.49 nm. Correspondingly, for the SiNx layer (n = 2.344; k = 0.0003), the calculated absorption depth is approximately 54.9 µm. This translates to roughly 16% of the incident blue light intensity traversing through the uppermost 30 nm of the sacrificial a-Si layer and reaching the SiN_x layer. In Fig. 4.13. (a), we present the Raman scattering data originating from the underlying a-Si:H layer, which undergoes phase transitions from an amorphous to a polycrystalline state at different laser fluences. Evidently, a broad Raman peak centered around ~480 cm^{-1}, in line with the literature, signifies the presence of the a-Si:H layer [159]. A slight shift in the a-Si:H peak is observable with the increasing laser fluence. Notably, at a laser fluence of 1.01 J/cm^2, a distinct sharp peak emerges at 498.6 cm^{-1}, approaching the crystalline Si peak. Moving to Fig. 4.13. (b), a discernible decline in the broad peak at ~800 cm^{-1} is depicted, correlating with an increase in laser fluences. This peak is attributed to the presence of SiN_x [160][161]. Under conditions of non-ablation, the Raman scattering stems from both the upper sacrificial a-Si:H layers and the underlying SiN_x, with only approximately 16% of the incident blue light reaching the a-Si:H/SiN_x interface. Consequently, the broad SiN_x Raman peak at ~800 cm^{-1} exhibits the lowest intensity counts. Contrastingly, under ablation conditions, the total intensity counts of the SiN_x peak increase as the remaining amount of a-Si:H layer becomes negligible. As the laser fluences rise, a reduction in the peak's intensity is observed. This trend can be attributed to the diminishing presence of the underlying SiN_x due to ablation, resulting in

reduced Raman scattering. The EDS spectra validate the phenomenon of thinning out of the SiN_x layer.

Table 4.2. Data of Si:N ratio at various laser fluence

Fluences (J/cm^2)	Intensity of Si (2p) (a.u.)	Intensity of N (1s) (a.u.)	Si(2p): N(1s) Ratio
Unablated	37.1	0.4	92.8
0.427	22.57	2.89	7.8096
0.595	22.93	3.62	6.3342
1.01	25.6	2.1	7.0718

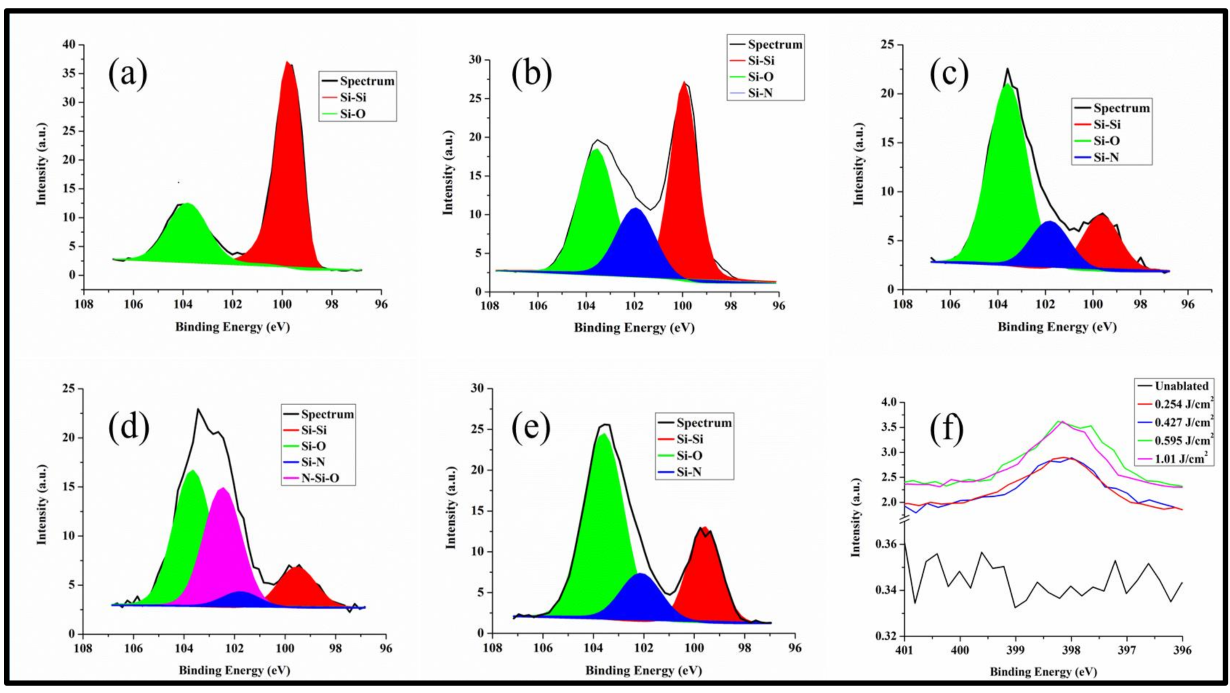


Fig. 4.14. XPS Si(2p) spectra of (a) unablated, (b) 0.254 J/cm^2, (c) 0.427 J/cm^2, (d) 0.595 J/cm^2, (e) 1.01 J/cm^2 fluences and (f) N(1s) spectra of all the laser fluences. The average measurement error across all elements was found to be ~10.7%.

High-resolution XPS (HR-XPS) measurements were conducted with a spot size of 50 μm, resulting in an average signal obtained over two laser spots with a 20 μm beam diameter. The error bars in all XPS measurements were within ± 0.2 eV. The XPS spectra were calibrated to the C (1s) peak at 284.8 eV following ASTM/NIST guidelines [162]. The collective measurement error across all elements, computed from five distinct XPS measurements in the unablated region, was approximately 10.7%. Table 4.2. highlights a declining Si(2p): N(1s) ratio as the laser fluence increases, indicative of an augmented exposure of the SiN_x layer after removing the sacrificial a-Si:H layers. A marginal upswing in the Si(2p): N(1s) ratio is evident at laser fluences surpassing 1.01 J/cm², attributed to the emergence of underlying c-Si at the laser spot centers. Within Fig. 4.14. (a)–(e), the presence of a Si (2p) peak at 99.4 eV signifies the existence of Si-Si bonds within both the a-Si:H and c-Si layers. A Si-O peak at 103.5 eV indicates the formation of SiO_2, corroborating findings by He *et al.* [163]. The Si-N peak at 101.84 eV and a potential N-Si-O complex peak at 102.64 eV under a fluence of 0.595 J/cm² align with existing literature [164]–[166]. Fig. 4.14. (a) portrays the presence of the upper a-Si:H layer and its inherent oxide during unablated conditions. In Fig. 4.14. (b), the Si-N peak confirms the targeted ablation of the upper a-Si:H layer, leading to SiN_x exposure. A comparable peak structure is evident in Fig. 4.14. (c). In Fig. 4.14. (d), at a fluence of 0.595 J/cm², the robust emergence of the N-Si-O peak indicates the conversion of the SiN_x layer into a silicon oxy-nitrile (N-Si-O) complex at the laser spot center due to the Gaussian beam profile. Fig. 4.14. (e) displays the disappearance of the N-Si-O peak, aligned with the peel-off phenomenon observed at the laser spot centers. Lastly, Fig. 4.14. (f) showcases the absence of the N (1s) peak in the unablated sample and the emergence of the N (1s) peak at 397.9 cm^{-1}, substantiating the presence of the SiN_x layer owing to the N-Si bond [167].

Hence, the comprehensive XPS and Raman investigation collectively demonstrates that the a-Si:H layer can be laser ablated to uncover the underlying SiN_x layer through ns laser processing, all while preserving passivation.

E. Comparison with lithography patterned devices

The novelty of using a photoresist (PR) coating on IBC-HJ sample devices was that the selective UV laser exposure of the top sacrificial PR layer coating would create patterns without any direct laser-induced heat damaging the device. Later, after the development of the laser-exposed areas, selective chemical etching was conducted, followed by stripping off the remaining PR layer. This concept needs no complex masking and ensures flexible spatial-resolved patterning. The positive PR used in this experiment was AZ5214.

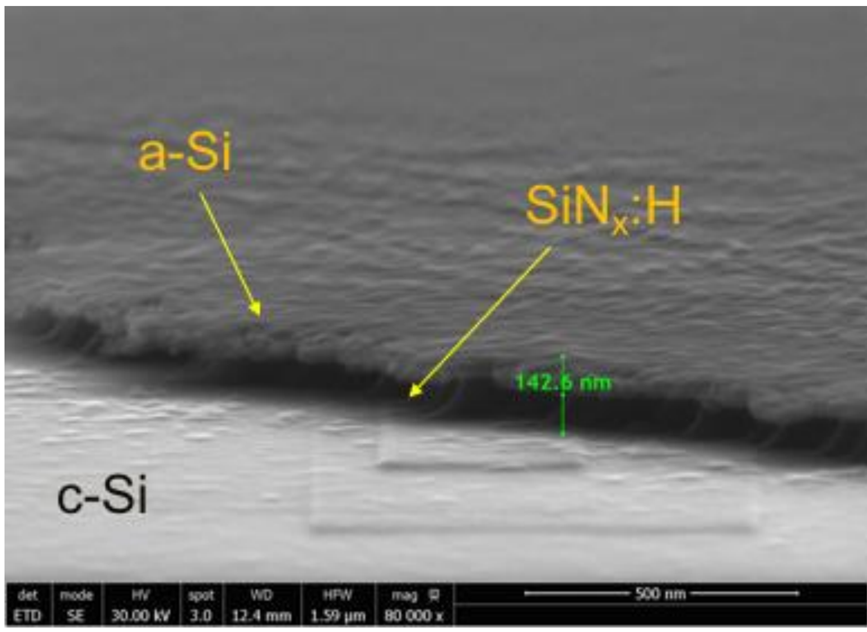


Fig. 4.15. Cross-sectional SEM image of IBC device after laser exposure of photoresist and selective chemical etching of top sacrificial a-Si:H and SiN_x:H layers.

Table 4.3. MCL and iVoc before and after laser exposure of the photoresist layer

Sample	Laser Fluence (J/cm^2)	1.4 µm thick Photoresist	Before laser exposure		After laser exposure and selective chemical etchings	
			MCL (µs)	iV_{OC} (mV)	MCL (µs)	iV_{OC} (mV)
01	0.14	AZ5214	679	699	573	693
02	0.12	AZ5214	1280	721	1227	720

The cross-sectional SEM images, shown in Fig. 4.15., showed the success of this approach. A negligible drop in iV_{OC} (< 7 mV) and in MCL (~4.1% decrease), shown in Table 4.3., was observed after laser exposure and selective chemical etchings. Hence, optimized UV laser exposure to the PR layer induced negligible damage to the IBC solar cell devices. This indirect laser patterning has proved to be a potential method of fabricating IBC devices at high throughput and lower complexity.

4.3. Conclusion

The ns pulsed laser patterning for fabricating IBC-HJ solar cells is demonstrated. The laser fluence required for the removal of the top sacrificial a-Si:H layer was found to be 0.254 J/cm^2. At this laser fluence, minimal effect on carrier lifetime and a change of iV_{OC} of only ~5 mV was observed. At these laser fluences, the a-Si: H sacrificial layer gets ablated, and the SiN_x layer is exposed. With the increase in laser fluence, the removal of the SiN_x layer was observed because of the laser light absorption in the underneath layers and the development of vapor pressure. The underneath a-Si:H (i and n) layers, acting as passivation and dopant layers, convert to the polycrystalline phase as laser fluence is increased beyond 0.595 J/cm^2. At laser fluences greater

than 1.01 J/cm^2, direct laser crystallization was observed and resulted in the rupturing of the SiN_x layer at the center of the laser spot. The presence of the SiN_x layer because of the laser ablation of the a-Si:H layer was confirmed by line-mapping EDS and Raman measurements. The Raman data also showed gradual crystallization at the laser spot and a decrease of the underlying SiN_x layer with increased laser fluence. The XPS measurements showed the growth of SiO_2, SiN_x, a complex N-Si-O at the surface (at 0.595 J/cm^2), and a decrease in the Si/N ratio after laser processing. The optical constants of the layers were measured using ellipsometry, and it helped to generate color charts, which can be reliably used to identify the changes in layer properties under different laser processing parameters. Such a method can also be used for multilayer identification in different thin-film devices. The ns pulsed lasers optimized in this work can successfully fabricate IBC-HJ solar cells with no significant degradation of iV_{OC} by the proper selection of laser fluence. Lastly, the indirect laser patterning of IBC devices using photoresists and selective chemical etchings gave high-performance results of iV_{OC} as high as 720 mV, similar to optimized direct laser patterning of IBC-HJ devices.

CHAPTER 5: Rapid Thermal Annealing (RTA) of p-TOPCon Si Solar cells

In this chapter, the feasibility and efficacy of RTA processing in the fabrication of in-situ B-doped p-TOPCon solar cells have been thoroughly investigated and optimized. We started our scientific investigation on the low-temperature (530 ºC) LPCVD TOPCon devices. Here, we present the results of RTA under air versus N_2 and the effect of high-intensity light under heat on in-situ B-doped p-TOPCon solar cells. The mechanism of passivation degradation was investigated through various measurements, such as surface morphology, carrier lifetime, crystallinity, chemical compositional changes, electrical sheet resistances, and oxidation state of SiO_x. The results of SiN_x:H coating under RTA conditions were also characterized.

Later, we continued this scientific investigation for the high-temperature (588 ºC) LPCVD TOPCon devices. Here, we used the prior optimizations of RTA processing and studied the effects of RTA heating, holding, and cooling times on the passivation quality, iV_{oc}, and dopant activation. The impacts of B-doped poly-Si and pulsed RTA were also explored. The device characterizations were conducted using photoluminescence (PL), QSSPC, and 4-point probing. This detailed study of RTA processing helps in understanding the effects of fast heating-cooling cycles during annealing and optimization of the potential use of laser processing of p-TOPCon devices.

5.1. Experimental

A. Fabrication of the p-TOPCon test structure

The p-TOPCon architecture employed in this study utilizes an in-situ B-doped poly-Si/SiO_x stack on n-type c-Si wafers. The in-situ boron doping method offers multiple advantages over ex-situ methods, including simplicity, independence from dopant pre-deposition processes, higher throughput, the increased deposition rate of the poly-Si layer, elevated boron concentration, enhanced field-induced passivation, and a reduced optimal annealing temperature [168]–[170].

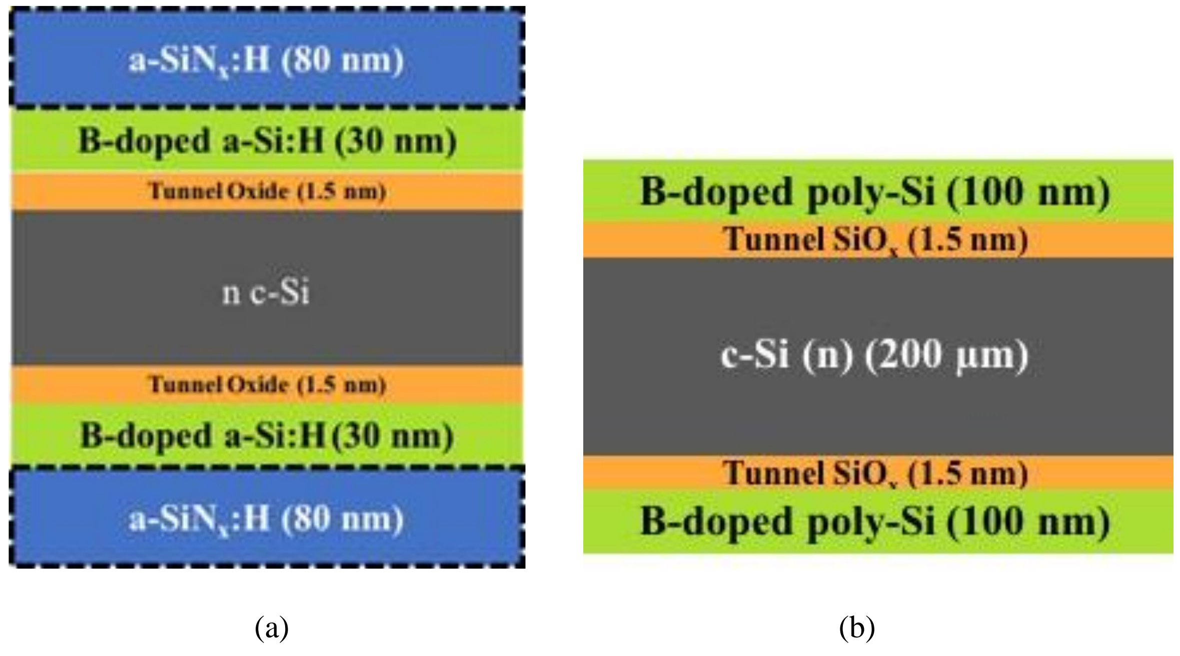


Fig. 5.1. Schematic diagram of a fabricated TOPCon test structure fabricated at (a) lower LPCVD temperature 530 ºC and (b). higher LPCVD temperature of 588 ºC. The dotted a-SiN_x:H layers are considered when the test structure is TOPCon/ SiN_x:H

Fig. 5.1. presents the schematic diagrams of the symmetric TOPCon test structure and the SiNx:H layer (dotted). These test structures were fabricated on 200 µm thick n-type monocrystalline Cz-type <100> silicon wafers with a 3.2 Ω·cm bulk resistivity. Saw damage was eliminated by subjecting the wafers to a 9% wt. KOH solution at 80 °C for 12 minutes, resulting in a semi-planarized surface. The wafers were meticulously cleaned in a sequence involving

piranha solution (96% wt. H_2SO_4: H_2O_2: DI :: 1:1:2) and SC-2 solution (38% wt. HCl: H_2O_2: DI :: 1:1:2), with oxide removal (5% wt. HF solution) performed between each step and at the process conclusion. The temperature of the solutions ranged between 50 and 60 °C. Following this, an ultrathin layer of SiO_x (~1.5 nm) was grown on both sides of the silicon using 70% wt. electronics grade HNO_3 at 100 °C for 15 minutes. The subsequent step involved the growth of in-situ boron-doped polysilicon on both sides of the wafer using a Tystar tube low-pressure chemical vapor deposition (LPCVD) system using silane and diborane precursor gases. Two sets of test samples were fabricated, where the first set had a polysilicon layer grown at 530 °C and the second set of test samples at 588 ºC for 27 minutes. The resulting thickness of the polysilicon layers in the first set of samples, as shown in Fig. 5.1. (a), was approximately 30 nm, and in the second set of test samples, the thickness was ~100 nm, as shown in Fig. 5.1. (b). Furthermore, some samples from the first set were coated with an 80 nm layer of SiN_x:H on both sides in a Centrotherm plasma-enhanced chemical vapor deposition (PECVD) reactor to achieve improved passivation through hydrogenation. The furnace-annealed sample underwent annealing in nitrogen at 875 °C for 30 minutes in a Centrotherm tube furnace with a ramp-up from 600 °C at approximately 10 °C/min. The reason for growing the second set of samples at 588 ºC was to enhance the polycrystallinity compared to lower samples grown at lower temperatures.

Before any subsequent processing steps, 1 cm × 1 cm dimension samples were cut from a singular 6-inch test wafer to serve as the test samples for all material characterization except carrier lifetime measurements. Quasi-steady-state photoconductance (QSSPC) carrier lifetime measurements were conducted on test samples of size 1 in^2. The QSSPC sensor coil exhibited a diameter of 4 cm. For each thermal annealing test, a total of three samples were meticulously prepared. The film thickness variation across a 1 cm length was determined to have a maximum

deviation of ±5%. It is important to note that the homogeneity of boron concentration was not assessed.

Both rapid thermal annealing (RTA) and forming gas annealing (FGA) were conducted within the AnnealSys rapid thermal processing (RTP) system, employing various processing gas environments such as ultrapure N_2 and forming gas (composed of 5% H_2 and 95% Ar) from Praxair. The surrounding air was used for air annealing, with the room's humidity recorded at 40%–42%. It is worth noting that the temperature range for breaking Si-H bonds and dehydrogenation spans from 300 to 550 °C, and a slower heating rate is employed to prevent the formation of blisters [171].

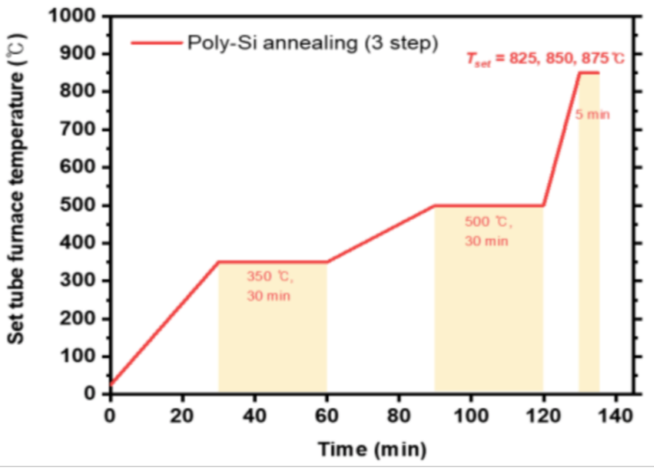


Fig. 5.2. Schematic diagram of the RTA temperature profile conducted for the first set of test samples with lower temperature (530 ºC) LPCVD poly-Si layer. (Adapted from [87], with the permission of MDPI, *Energies*.)

In the case of the first set of test samples with lower temperature (530 ºC) LPCVD poly-Si, all RTAs consisted of a three-step process, as shown in Fig. 5.2. The three-step approach was adapted from Lee *et al.*'s work, though their study was confined to tube-furnace annealing [87]. The first step involved a 30-minute ramp-up from room temperature to 350 °C, followed by a 30-

minute dwell. Subsequently, a 30-minute ramp-up to 500 °C was carried out, followed by a 30-minute dwell. The final step comprised a 10-minute ramp-up to specific annealing temperatures, such as 625, 750, 825, and 875 °C, with a 5-minute dwell time. Both N_2 and air atmospheres were used for these RTAs. The cooling rate during RTA was about 300 °C/min, compared to about 3 °C/min in the tube furnace. The rapid cooling rate underscores the expeditious nature of our RTA processing. For the FGA process, the annealing treatment occurred at 425 °C, forming gas for 1 hour. To investigate potential light-induced damage from the tungsten-halogen lamp in the RTA system, a 500 µm thick p-type c-Si wafer cover with a 1.05″ × 1.05″ area was placed over the test samples during all annealing procedures, regardless of the annealing atmosphere. The avoidance of physical contact between the Si wafer cover and the test sample was ensured using small Si spacers. The test samples were subjected to direct light exposure using the three-step RTA process at 825 °C in N_2 and air to assess the impact of light-induced degradation. Furthermore, a few selected test samples from the first set (of LPCVD 530 ºC) with a SiN_x:H layer underwent direct RTA at 825 °C in N_2, followed by FGA.

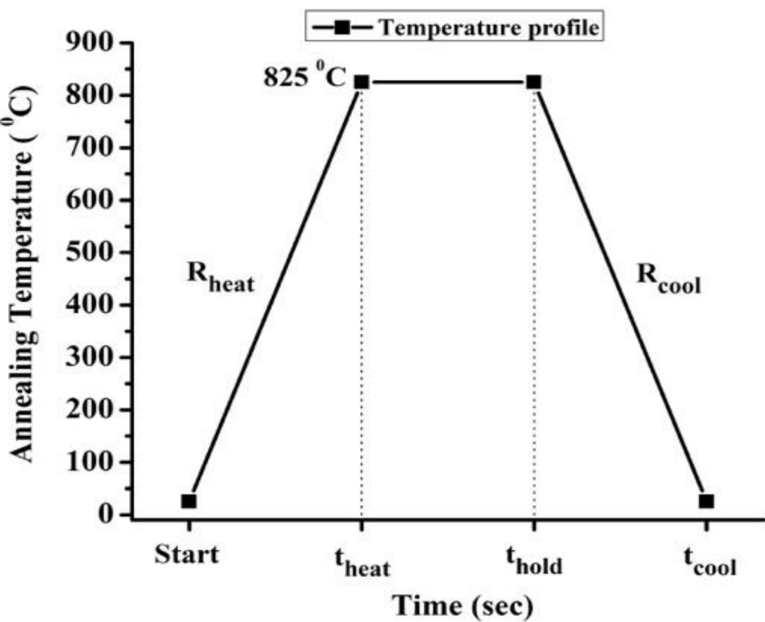


Fig. 5.3. Schematic diagram of the RTA temperature profile conducted for the second set of test samples with higher temperature (588 ºC) LPCVD poly-Si layer.

In the case of the second set of test samples with higher-temperature (588 ºC) LPCVD poly-Si, the variations were made in the RTA heating time (30 sec to 150 sec), holding time (10 sec to 150 sec) and cooling time (30 sec to 300 sec) in N_2. The temperature profile of the RTA process is depicted in Fig. 5.3. The pulsed form of RTA, as shown in Fig. 5.4., was also used to study the passivation quality under a series of pulsing heating, holding, and cooling times. Only t_{hold} was varied as 10 sec or 60 sec. All other time frames, including time between any 2 pulses at 550 ºC, consisted of 60 sec. Such a design was formulated to relieve thermal stress.

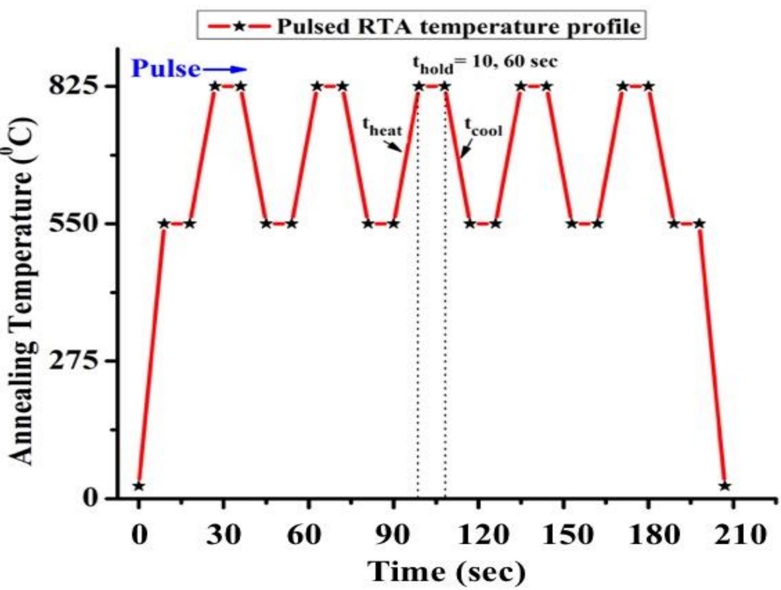


Fig. 5.4. Schematic diagram of the 5-pulses RTA temperature profile.

To investigate the effect of the B-doped poly-Si layer on the passivation quality and the extent of the boron dopant diffusion at the SiO_x/Si interfaces, four test samples of 1 cm × 1 cm

area, including the starting and the reference furnace anneal samples were selected. The B-doped poly-Si layer was selectively etched using 20% wt. KOH at 40 ℃ for 250 sec at an etch rate of ~0.4 nm/s. The first sample was as-prepared (starting), the second was furnace annealed, the third was KOH etched, and the fourth went through RTA and then KOH etched. The KOH etching kept the SiO_x layer on the silicon wafer.

B. Characterization techniques

Except for the QSSPC iV_{OC} measurements, all characterization studies were conducted on test samples with an area of 1 cm². The surface morphology was examined using a 15° stage tilt in an FEI Quanta 650 Field Emission Scanning Electron Microscope. The QSSPC iV_{OC} measurements were executed on test samples with an area of (1″ × 1″) using the WCT-120 Silicon Wafer Lifetime Tester from Sinton Instruments. The input of sample thickness was manually set as 0.02 cm with 2.8 Ω-cm resistivity, n-type dopant, 0.7 optical constant and generalized analysis mode. These iV_{OC} measurements were performed under 1 Sun conditions.

For passivation characterization using photoluminescence (PL), an experimental setup was used comprising a continuous-wave laser (Melles Griot) with a wavelength of 532 nm and power of 2 W as the excitation source. The spot size was approximately 1 mm. The spectrometer was a Horiba Jobin Yvon iHR320 operated by SynerJY v3.5 software, coupled with an InGaAs detector and an SR830 DSP lock-in amplifier from Stanford Research Systems. To prevent detector saturation, minimize heating of test samples, and ensure a high signal-to-noise ratio, the laser power was reduced to 70 mW using neutral density filters and quartz glass reflection. Each PL spectrum reading was an average of 10 scans. The absolute PL intensity values are arbitrary but can be used to compare the passivation quality. The PL intensity peak at ∼1150 nm was due to the

c-Si bandgap of ~1.1 eV [172]. Micro-PL measurements were also performed to assess and differentiate passivation quality on the blister and non-blister regions. This μ-PL measurement had a spot size of approximately 150 μm. The PL data carried an approximate intensity error of around ±2.6%.

For crystallinity measurements using Raman spectroscopy, a Renishaw InVia TM Confocal Raman Microscope was utilized with a 405 nm excitation wavelength laser and a spot size of 1.8 μm. Each Raman scattering data point was an average of ten scans, each with a 15-second acquisition time. A reference sample was used prior to measuring the test samples to account for factors such as optics, mounting effects, and crystallinity changes.

Sheet resistances were determined using a Jandel four-point probe station for electrical characterization. Chemical compositional characterization was done using Fourier transform infrared (FTIR) spectroscopy on a Thermo Scientific Nicolet iS50 FT-IR instrument. Each FTIR reading comprised an average of 256 scans, with background readings averaged over 200 scans.

X-ray photoelectron spectroscopy (XPS) characterization was employed to ascertain quantitative surface chemical and elemental composition, depth profiling, and oxidation state determination. This was carried out on a PHI Versaprobe III scanning X-ray photoelectron spectrometer with a spot size of around 200 μm and an Al monochromatic X-ray source. The pass energy was set at 280 eV with a 0.5 eV acquisition step. For the XPS spectra of TOPCon structures, the C(1s) peak was calibrated to 284.8 eV following ASTM/NIST standards [162]. For the TOPCon/SiN_x:H samples, the N(1s) peak was calibrated to 397.86 eV [173]. The XPS measurements for SiO_x oxidation states carried an error bar of approximately 0.2 eV.

5.2. Results and discussion

The experimental findings and characterization results are discussed in this section. We investigated the effects of RTA atmospheres, high-intensity lamplight environment, and SiN_x:H coatings on the first set of test samples with lower temperatures (530 ºC) LPCVD poly-Si. They have been discussed in sub-sections 5.2.A. to 5.2.C. The scientific findings from this study led us to a newer approach of increasing the LPCVD temperature to 588 ºC and a thicker poly-Si layer for the second set of test samples. We continued our detailed scientific investigation into understanding and optimizing the effects of RTA heating, holding, and cooling times, the effects of B-doped poly-Si layers on passivation quality, and the pulsed form of RTA. These results have been discussed in sub-sections 5.2.D. to 5.2.I.

A. Study of the effects of RTA atmospheres

1. Surface morphology

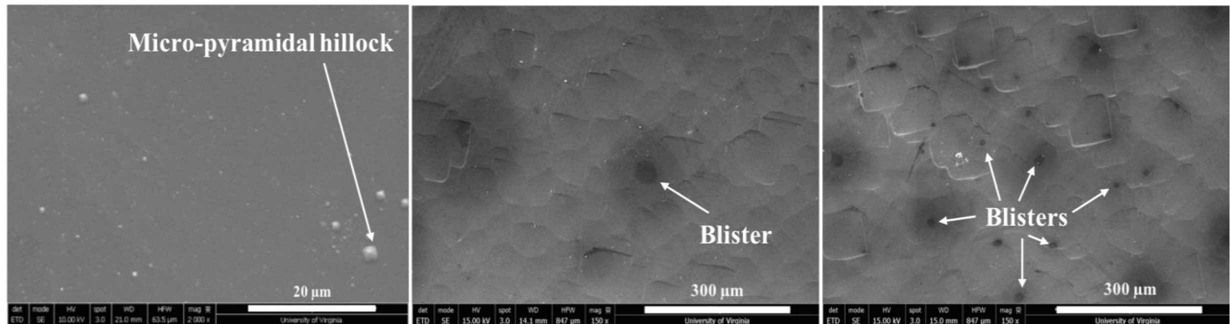


Fig. 5.5. Top-view SEM images of (a) as-deposited sample, (b) blisters (black areas) after RTA at 875 °C in air, and (c) blisters (black areas) after RTA at 875 °C in N_2.

Fig. 5.5. (a) presents a top-view image of the samples in their as-deposited state. No blistering was detected, though octahedral pyramidal features were evident on the surface. These structures resulted from KOH etching during the semi-planarization process and remained

unaffected by variations in annealing temperatures and durations. A study by Schröder *et al.* [174] has previously discussed the observation and potential mechanism behind such pyramidal features during the KOH etching of Si. Fig. 5.5. (b) showcases the top-view SEM image of blisters observed on samples air-annealed at 875 °C. Notably, a higher density of similar blisters was observed in N_2-annealed samples at 875 °C, as depicted in Fig. 5.5. (c). These blisters covered approximately 1% of the total surface area for air-annealed samples, while in N_2-annealed samples, they covered roughly 3%–4% of the total surface area. The morphology of samples annealed in the tube furnace is not shown, as no discernible changes were identified.

The elevated-temperature annealing induced the separation of Si-H bonds, leading to the liberation of atomic hydrogen within the poly-Si/SiO_x/c-Si structure. These atomic hydrogens aggregated to form molecular H_2, which then escaped under its considerable pressure, causing the rupture of the polysilicon layer and manifesting as blisters [175]. The implementation of a three-step procedure involving lower-temperature annealing served to mitigate the formation of blisters. Additionally, samples annealed in the furnace exhibited a diminished presence of blisters, potentially attributed to the slower heating rates compared to the rapid thermal annealing (RTA) process.

2. Surface passivation quality

Fig. 5.6. illustrates the iV_{OC} variation with the RTA temperatures under N_2 and air atmospheres. An optimal annealing temperature range emerged around 825 °C, with iV_{OC} declining beyond this threshold. This trend might be attributed to potential degradation affecting the SiO_2 passivation layer at higher temperatures.

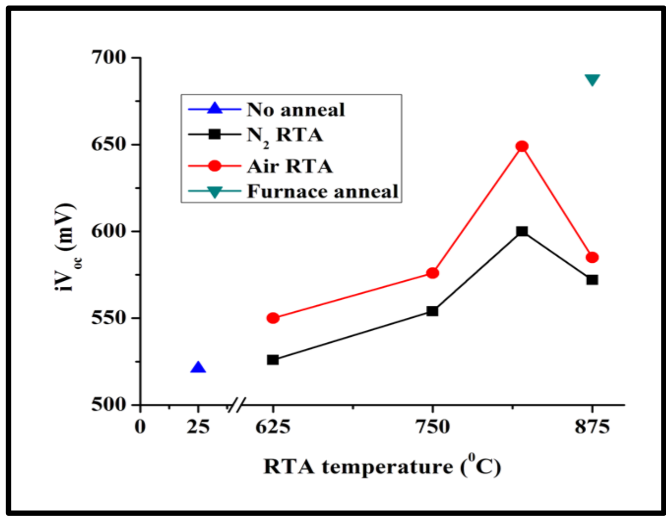
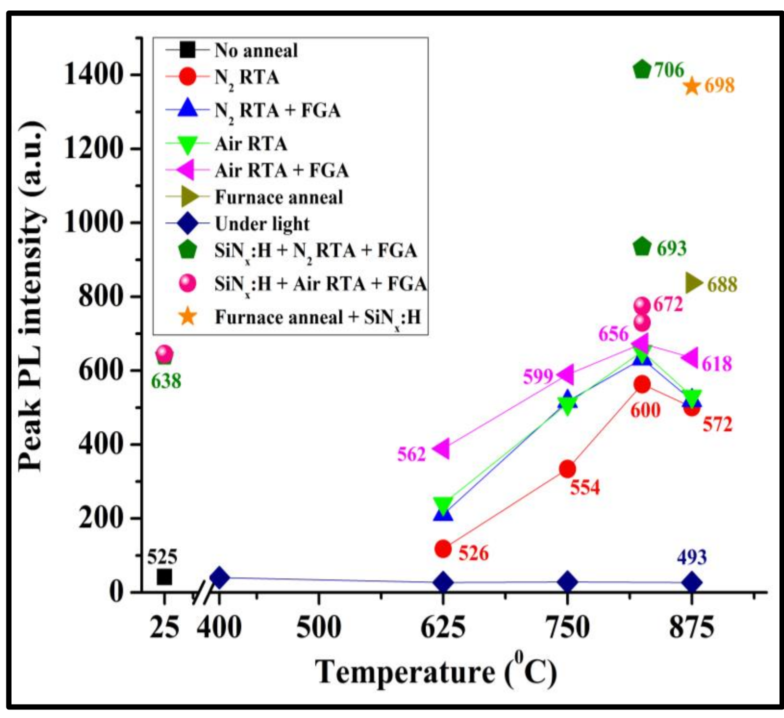


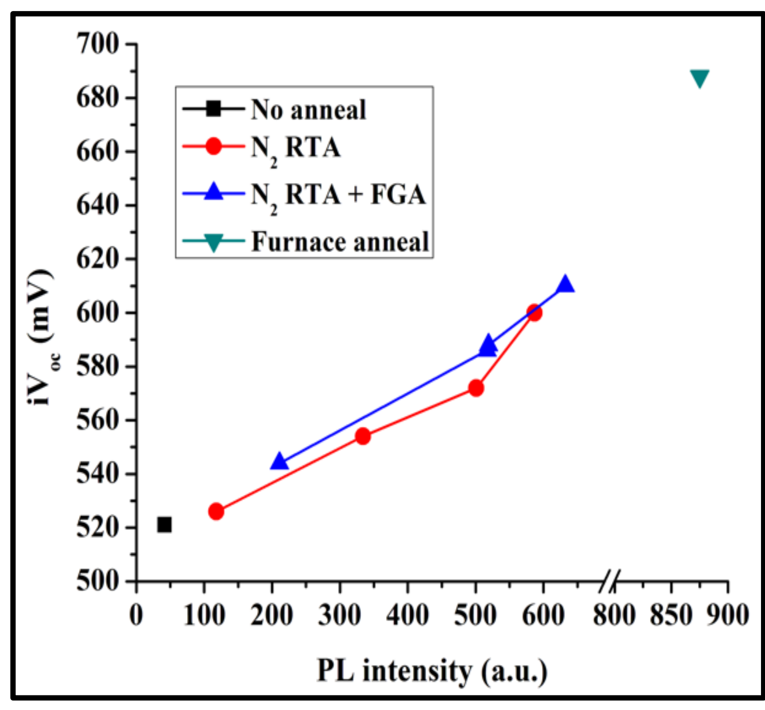
Fig. 5.6. Graph showing the dependence of iV_{OC} on the RTA temperatures. The data are given for RTA both in N_2 and air atmospheres. The graphs also show the iV_{OC} value for the sample without and after furnace annealing.

Notably, the iV_{OC} peak value proved higher in an air environment (649 mV) compared to N_2 (600 mV). Given that the in-situ B-doped poly-Si layers within these test samples were formed through the LPCVD process at a relatively lower temperature of 530 °C, a substantial initial hydrogen content was present, which increased the likelihood of blister formation. Notably, the iV_{OC} value of the RTA sample did not reach the level observed in the tube-furnace-annealed sample (688 mV). This discrepancy may be attributed to the higher blister density associated with the RTA process, potentially leading to the degradation of passivation quality.

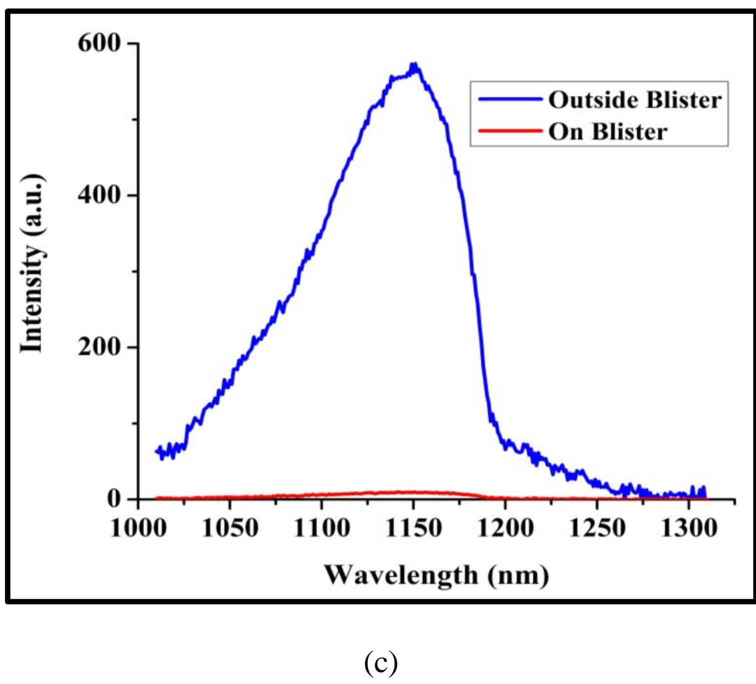
3. Photoluminescence



(a)



(b)



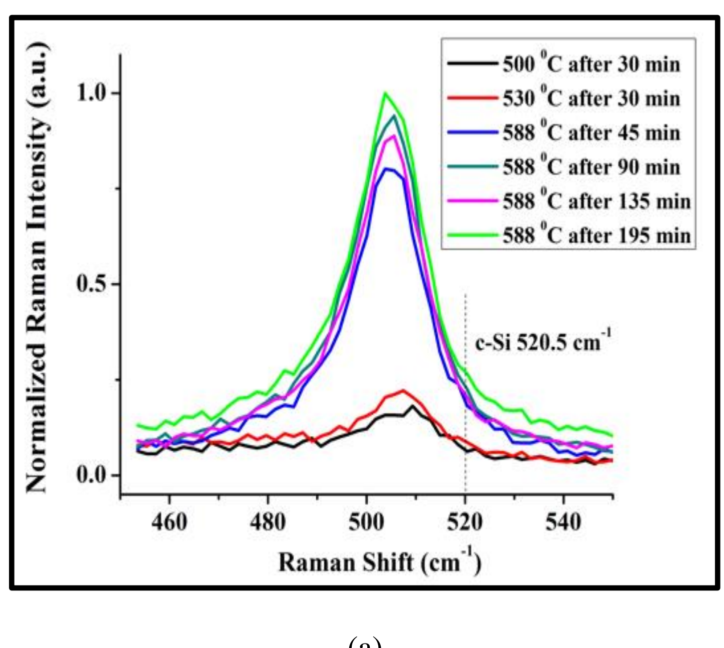
(c)

Fig. 5.7. (a) Qualitative dependence of peak PL intensity on the RTA temperatures for various annealing conditions. The iV_{OC} (in mV) numbers are provided on the graph, and (b) the dependence of iV_{OC} on the peak PL intensity. The data are given for RTA in N_2 and subsequent FGA only, and (c) PL intensity on and outside blister areas.

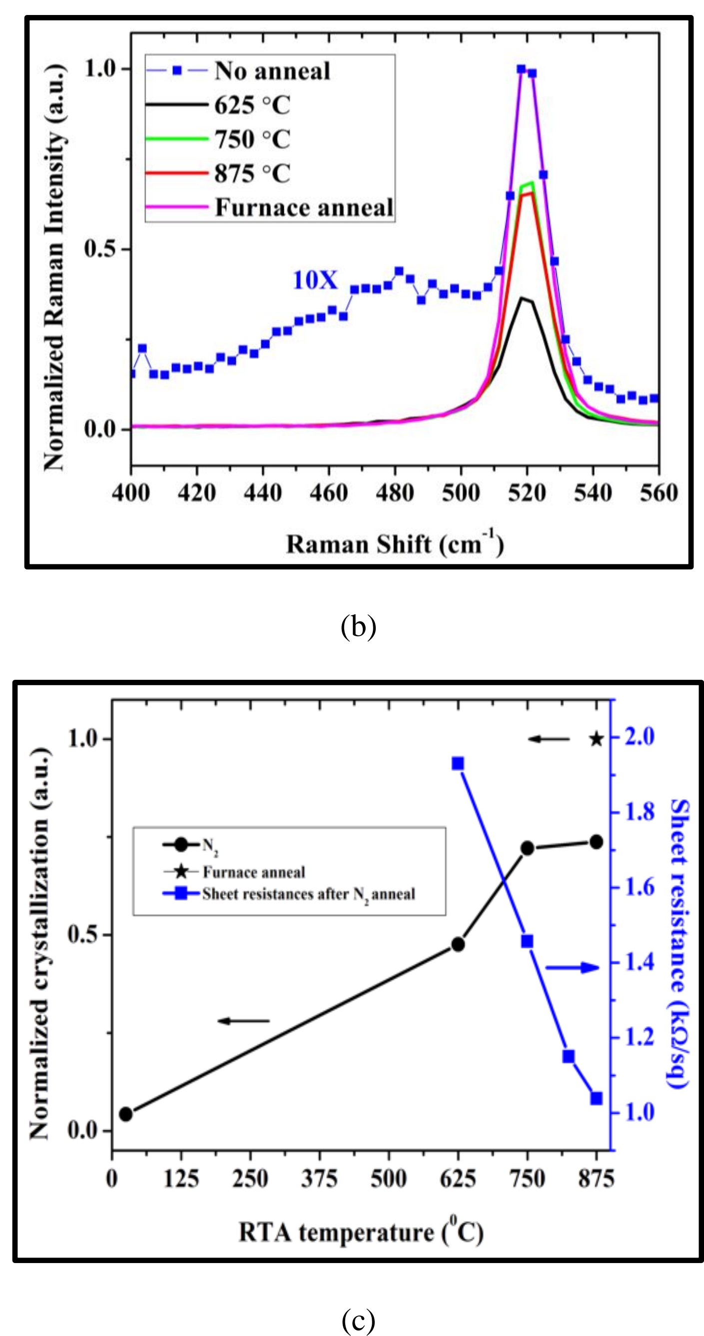
Fig. 5.7. (a) shows the trend of peak PL intensity with respect to RTA temperatures within N_2 and air atmospheres, as well as FGAs. Notably, the optimal annealing temperature of 825 °C yielded the highest peak PL intensity, further enhanced by FGA. Within the N_2-annealed test sample, the peak PL intensity reached 563 a.u., while FGA propelled it to 632 a.u. Similarly, for air annealing, the highest peak PL intensity achieved was 652 a.u., and FGA facilitated a rise to 673 a.u. Comparatively, the furnace-annealed sample exhibited an even higher peak PL intensity. These findings underscored the superior passivation quality of air-annealed samples compared to their N_2 counterparts. In Fig. 5.7. (b), the observed connection between iV_{OC} and peak PL intensity is displayed. Notably, while a logarithmic relationship is anticipated in the presence of a junction [176], this case demonstrates a linear relationship. This discrepancy is attributed to the interplay

of factors such as oxidation, enhanced crystallinity, and a decrease in defect density, all of which influence the change in PL. Fig. 5.7. (c) highlights the μ-PL intensity discrepancy between the blistered and non-blistered regions. Remarkably, the blister region displayed a peak PL intensity of 9 a.u. compared to the approximately 570 a.u. observed outside the blister region in an air-annealed test sample at 825 °C. This stark contrast indicated that blisters led to considerable passivation degradation within the tested samples.

4) Crystallinity determination



(a)



(b)

(c)

Fig. 5.8. (a) Raman spectra for the dependence of crystallization of a-Si:H on the anneal time duration while the sample was kept at a hot stage at various temperatures, (b) Room temperature Raman spectra for the dependence of crystallization on the RTA temperature, anneal time was 5 minutes and curves are normalized to furnace anneal. The as-deposited sample curve is magnified 10X due to lower Raman intensity, and (c) the growth of crystallinity (area under the curve) as a function of temperature.

In Fig. 5.8. (a), the Raman peak intensity corresponding to the polycrystalline phase is plotted against the annealing temperature and duration in the N_2 atmosphere. Choi *et al.* [59] previously emphasized that the deposition temperature of LPCVD poly-Si should be above 580 °C to ensure a reduced hydrogen content that prevents the formation of blisters. Enhanced crystallinity became apparent starting from 588 °C, as indicated by the Raman peak at 508 cm^{-1}, and this enhancement further progressed with extended annealing times. These measurements were performed within a heated N_2-filled chamber. The typical Raman peak of room temperature c-Si at 520.5 cm^{-1} is slightly shifted to 508 cm^{-1} due to the high-temperature measurement conditions [177]. The as-deposited in-situ B-doped poly-Si film displayed a composite of amorphous and polycrystalline phases.

Fig. 5.8. (b) showcases the transition of the a-Si:H peak Raman peak at 480 cm^{-1} towards the crystalline phase at 519.1 cm^{-1} as RTA temperatures rose from 625 to 875 °C within the N_2 atmosphere. Similar phenomena were observed when the test samples underwent RTA in an air atmosphere (not depicted here). In Fig. 5.8. (c), the increase in the "area under the curve" of the Raman curve with respect to RTA temperatures in the N_2 atmosphere signifies the increased crystallinity. The degree of crystallinity in the in-situ B-doped TOPCon structure is contingent on RTA temperatures and annealing time, independent of annealing atmospheres or post-anneal FGAs. At room temperature, the Raman peaks for poly-Si and the c-Si substrate occur at 520.5 cm^{-1}. The Raman peak of poly-Si is notably broader due to its polycrystalline nature. Given the 405 nm Raman excitation wavelength, the transmission through a 30 nm poly-Si layer is approximately 12% based on the optical n and k values. Consequently, the contribution of the c-Si substrate to the Raman peak was minimal.

5) Chemical composition

Fig. 5.9. (a) presents the FTIR absorbance spectra of c-Si, the as-deposited film, TOPCon structure annealed at 825 °C in N_2 and air atmospheres, and furnace annealed in N_2. The absorbance peak at 1107 cm^{-1} typically corresponds to the vibrational stretching mode of Si-O, signifying the presence of interstitial oxygen and native oxide [178][179]. The shift of this peak towards the 1080 cm^{-1} peak aligns with the stretching mode of Si-O-Si, indicating the formation of conventional thermal SiO_2 on the surface after air annealing [180][181]. Notably, the peak at 455.6 cm^{-1} observed in the air-annealed sample corresponds to the rocking-mode vibration of Si-O bonds, further corroborating the creation of SiO_2 [182]. Moreover, a vibrational state linked to the Si–Si bond was discernible at 611.7 cm^{-1} [183].

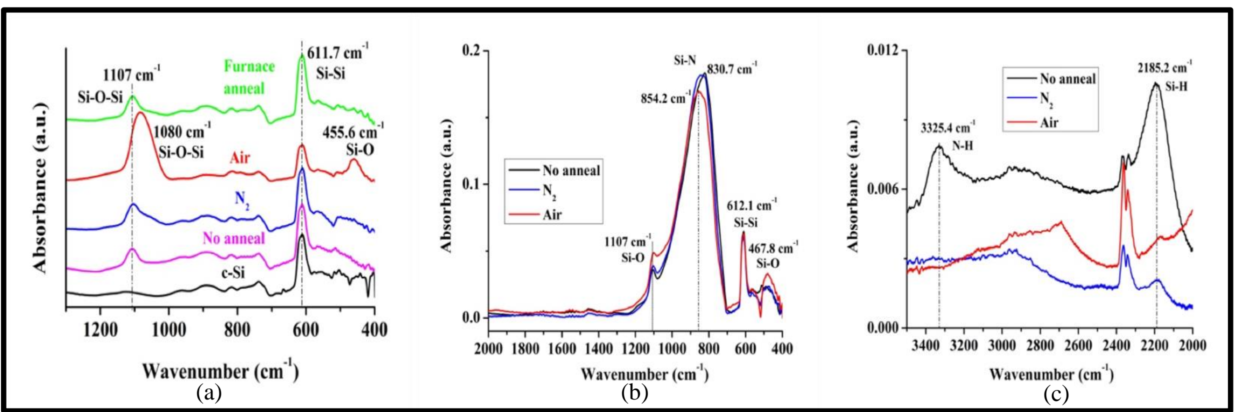


Fig. 5.9. (a) FTIR spectra for c-Si, TOPCon samples annealed at 825 ºC in N_2 and air and results are compared with furnace annealed sample, (b) FTIR spectra for TOPCon/SiN_x:H samples as-deposited and annealed at 825 ºC in N_2 and air, (c) FTIR spectra for TOPCon/SiN_x:H samples from 3400-2000 cm^{-1} wavenumber region. All the samples were FGA-treated before FTIR.

The distinct positions of these peaks imply that air annealing led to the transformation of the upper portion of the poly-Si layer into the SiO_2 layer. In contrast, under N_2 RTA and furnace annealing conditions, notable SiO_2 formation did not occur, except for the growth of native oxide.

6) Sheet resistance

The transformation of the a-Si:H layer into poly-Si improves lateral carrier transport, dopant activation, and passivation efficiency. As demonstrated in Fig. 5.8. (c), sheet resistances were measured across various annealing temperatures within an N_2 environment, along with an assessment of crystallinity. Notably, sheet resistances as low as those achieved through furnace annealing were attainable [0.9 kΩ/sq, not depicted in Fig. 5.8. (c)]. For the non-annealed sample, the sheet resistance exceeded 1 MΩ/sq. It's worth noting that the RTA atmospheres, including air, had a negligible impact on the sheet resistance of in-situ B-doped poly-Si when measured at a constant annealing temperature of 875 °C.

7) Oxidation state and elemental composition

The depth-profiling XPS composition spectra depicting test samples after RTA in both air and N_2 environments at 825 °C are presented in Fig. 5.10. (a) and (b), respectively. Considering the expected sputtering rate of SiO_2 to be approximately 8.9 nm/min and a Si/SiO_2 sputter rate ratio of about 1.1, it is essential to acknowledge that the precise positions of the surface oxide, poly-Si, and buried ultrathin oxide layers may contain some level of uncertainty due to the indeterminate sputter rate across the poly-Si layer [184]. A thicker oxide layer was observed atop the remaining poly-Si layer for the air-annealed case. This observation supports the notion that oxygen from the surrounding air diffused through the surface oxide layer onto the poly-Si. The

presence of an ultrathin oxide layer is indicated by increased oxygen concentration and decreased Si concentration beneath the poly-Si layer. Past the interface of the ultrathin oxide/c-Si, the concentration ratio of Si to O increased. In contrast, N_2 annealing led to the identification of a very thin surface oxide along with a broader peak representing Si and oxygen concentrations at the ultrathin oxide region. This suggests a higher oxygen concentration within the ultrathin oxide layer in air-annealed samples. Due to its relatively low concentration, boron detection was not possible. The as-deposited sample exhibited an exceedingly thin surface native oxide layer with an intact poly-Si/ultrathin oxide/c-Si structure (not shown here), reaffirming our FTIR findings.

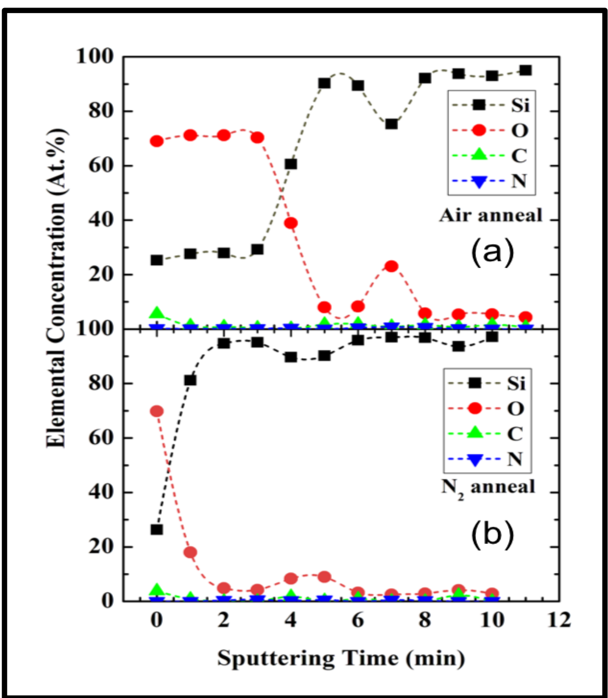


Fig. 5.10. Depth-profiling XPS spectra showing the atomic percentage profile of (a) air-annealed and (b) N_2-annealed samples based on the atomic concentrations of Si (2p), O (1s), C (1s), and N (1s).

In Fig. 5.11., the XPS spectra of the ultrathin passivating SiO_2 layer are displayed subsequent to the removal of polysilicon through a chemical etching process for distinct annealing conditions at 825 °C. The XPS spectra display a peak at 99.8 eV arising from the Si–Si bond and

another peak at 103.8 eV due to the presence of the SiO_x layer. Deconvolution of the Si-O peak unveiled the prominent oxidation states of Si^{3+} and Si^{4+} [185]. The minimal discrepancies in SiO_x/SiO_2 ratios and their respective peak positions indicate that the RTA atmosphere (air or N_2) did not profoundly influence the chemical composition of the ultrathin silicon oxide. Only furnace annealing led to a noticeable shift in the Si-O peak. Furthermore, the silicon peak's area increased following thermal annealing, indicating an increase in elemental Si [186]. Notably, a decrease in SiO_2 concentration was observed, possibly attributed to Si incorporation into the oxide layer [187].

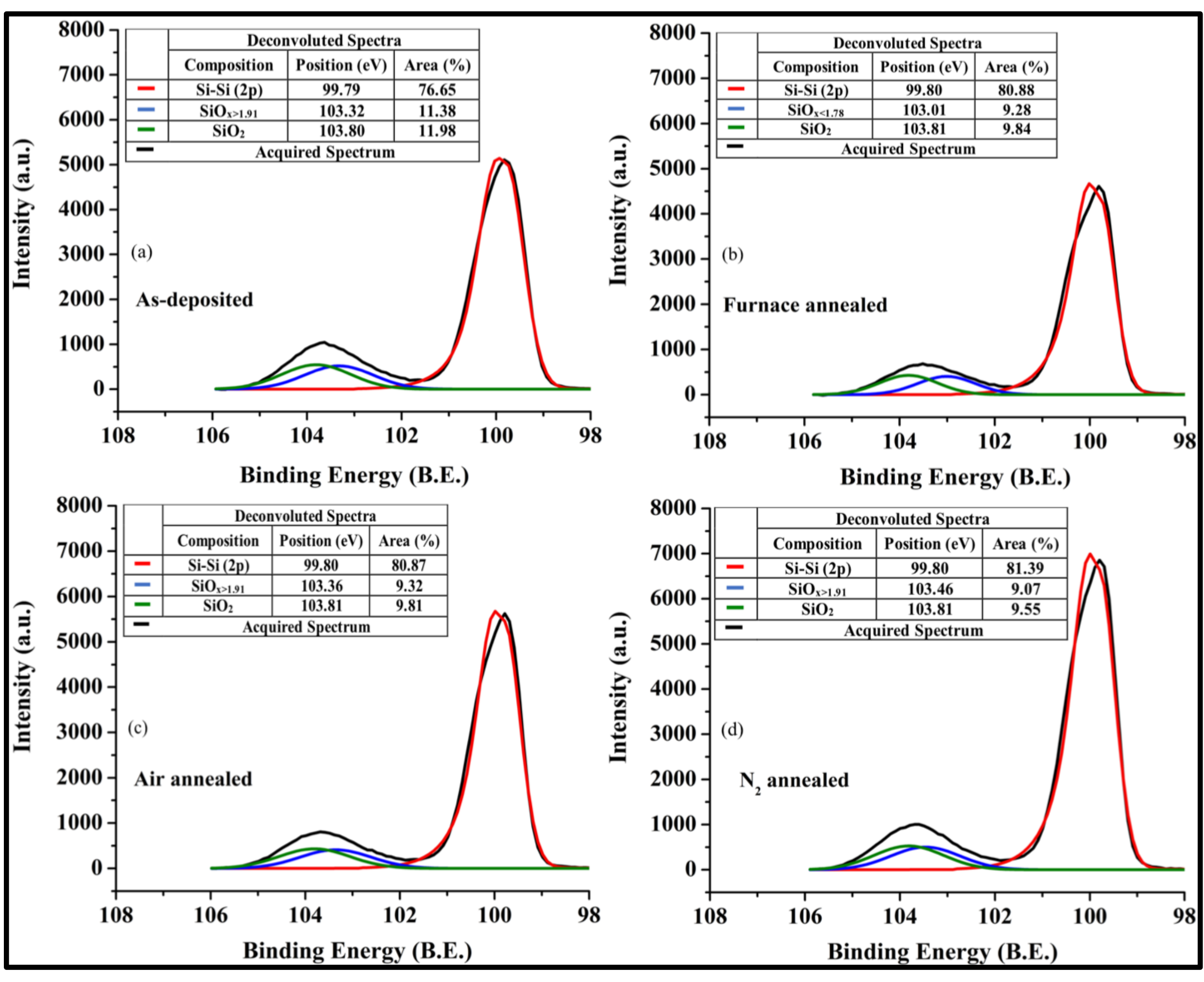


Fig. 5.11. Surface XPS spectra of ultrathin SiO_2 layer of TOPCon test structures for (a) as-deposited, (b) furnace, (c) air, and (d) N_2 annealing conditions.

B. Effects of high-intensity light environment

Initially, the RTA-treated samples exhibited subpar photoluminescence (PL) intensity and notably low iV_{OC} values. It became evident that this performance deterioration was linked to the exposure of the samples to both intense light and heat within the RTA setup for sample heating. To investigate this, we conducted experiments with samples subjected to the high-intensity light of the RTA process alongside samples that were effectively shielded by a Si wafer cover.

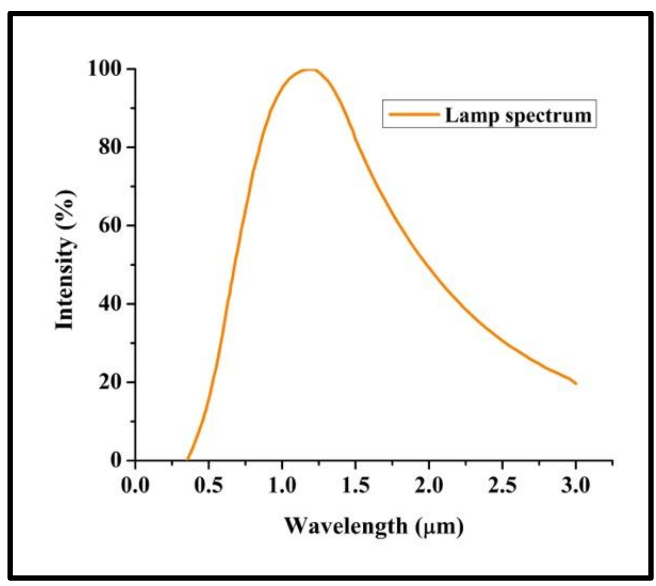


Fig. 5.12. Spectrum of the RTA lamp used in this study.

The spectral composition of the halogen IR lamp utilized in the RTA investigations is presented in Fig. 5.12. The RTA durations were approximately 5 minutes at elevated temperatures, a duration sufficient to achieve thermal equilibrium. Around 88.9% of the underlying 4-inch Si wafer received the full spectrum of radiation from the RTA lamp, given that the test samples only occupied 11.1% of the total area. Consequently, the base wafer temperature was anticipated to be

similar to an uncovered setup. The Si wafer cover absorbed all visible light emitted by the lamp, consequently emitting heat towards the test samples. Additionally, the temperature measurement obtained from the thermocouple in contact with the base Si wafer indicated the sample's temperature.

Table 5.1. The effects of high-intensity RTA lamplight on the PL intensity and iV_{OC} of TOPCon structures at 875ºC.

Sample		Before FGA		After FGA	
		PL (a.u.)	iV_{OC} (mV)	PL (a.u.)	iV_{OC} (mV)
As fabricated		41	525	107	537
Without a Si wafer cover	N_2	28	491	37	~520
	Air	27	493	45	~520
With Si wafer cover	N_2	501	572	517	588
	Air	519	585	642	618

Fig. 5.7. (a) depicts the light-induced degradation of peak PL intensity, measured at approximately 1150 nm, without the presence of a Si wafer cover (labeled as "underlight" in the legend) for both N_2 and air atmospheres at varying annealing temperatures. All other data points were recorded utilizing a Si wafer cover to prevent light exposure. The summarized data from Fig. 5.7. (a) are presented in Table 5.1. Under high RTA temperatures without the Si wafer cover, it was observed that degradation in iV_{OC} occurred. Subsequent post-anneal FGAs facilitated recovery from this loss of passivation, restoring the initial passivation quality. However, further improvement in iV_{OC} beyond its original value was not achieved. By utilizing the Si wafer cover during both RTA and post-anneal FGAs, it was possible to achieve enhanced iV_{OC} values. Notably, this light-induced degradation was observed regardless of the RTA atmosphere, specifically occurring only at elevated temperatures surpassing 625 °C.

C. Effect of RTA on SiN_x:H coated TOPCon structure

1) Effect on surface morphology

Subjecting a TOPCon sample coated with SiN_x:H to RTA at 825 °C in an N_2 atmosphere resulted in blister formation on the SiNx:H layer, as seen in the top-view SEM image in Fig. 5.13. These blisters emerged due to the elevated hydrogen pressure during the RTA procedure. Notably, fragments of broken SiN_x:H material are visible in proximity to the blister. The assessment revealed that blisters covered approximately 7–9% of the total surface area. If effective measures could be implemented to minimize blister formation, this would likely increase the iV_{OC} value.

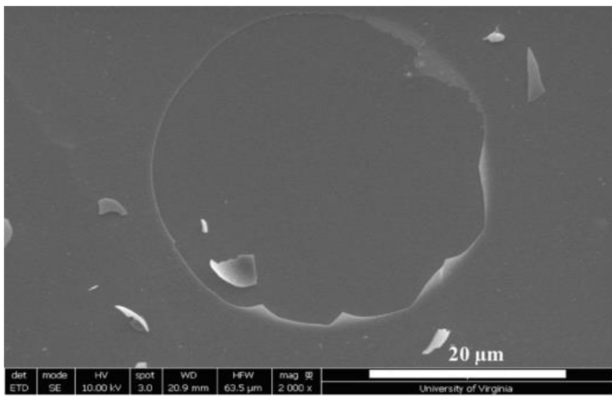


Fig. 5.13. Top-view SEM image showing a blister formed on the SiN_x:H layer after RTA at 825 ºC in N_2.

2) Effect on passivation quality

Table 5.2. Effects of SiN_x:H coating on the PL intensity and iV_{OC} of TOPCon structures under different RTA atmospheres at 825 ºC.

Sample	**Before FGA**		**After FGA**	
	PL (a.u.)	**iV_{OC} (mV)**	**PL (a.u.)**	**iV_{OC} (mV)**
As fabricated	638	622	678	634

RTA in N_2	935	693	1414	706
RTA in Air	730	659	775	672

Fig. 5.7. (a) illustrates the peak PL intensity of TOPCon/SiN_x:H test structures following the three-step annealing process at 825 °C under N_2 and air atmospheres and subsequent FGAs. All pertinent data have been concisely summarized and organized in Table 5.2. The highest iV_{OC} value of 706 mV was attained through N_2 annealing. For context, the furnace-annealed p-TOPCon structure reached an iV_{OC} of 688 mV without SiN_x:H and 698 mV with SiN_x:H coating. This underscores the efficacy of employing the SiN_x:H layer for passivation. The optical n and k values of the as-deposited SiN_x:H film were determined via ellipsometry and were found to be 2.108 and 0.00001, respectively, at 532 nm. The SiN_x:H layer serves as an antireflection coating, facilitating enhanced excitation laser light transmission and augmenting the PL intensity. However, it's important to note that our research focus lies in contrasting the change in PL intensity between unannealed and annealed samples. The assumption is that the absorption properties of SiN_x:H remain unchanged following thermal annealing. Consequently, its influence on the PL measurement is negligible, except for the enhancement of the absolute PL signal by approximately 30%, as computed based on light interference calculations.

3) Effect on SiN_x:H stoichiometry

Fig. 5.9. (b) and (c) depict the FTIR absorbance spectra of the TOPCon/SiN_x:H structures subjected to N_2 and air annealing at 825 °C, juxtaposed with the spectra of the as-deposited film. In Fig. 5.9. (b), the observation reveals an increase in the wagging mode peak at 1107 cm^{-1} and the bending mode peak at 467.8 cm^{-1} associated with Si-O bonds after air annealing, indicating the formation of a greater quantity of Si-O complexes [188]. Additionally, the absorbance peak

situated at 612.1 cm^{-1} corresponds to the Si–Si bond, while the broad peak centered around 840 cm^{-1} is generally attributed to the presence of the Si-N bond. The spectral range spanning 830.7 to 854.2 cm^{-1} signifies the presence of asymmetric stretching modes of Si-N, which undergo stoichiometric shifts, likely transitioning from Si_3-Si-N to Si_2-(H)Si-N configurations [189].

In Fig. 5.9. (c), the discernible presence of stretching modes corresponding to N-H and Si-H peaks at 3325.4 cm^{-1} and 2185.2 cm^{-1}, respectively, in the as-deposited samples indicates a high level of hydrogenation [190]. Subsequently, these peaks vanish after RTA due to the process of dehydrogenation.

4) Effect on the chemical composition of SiN_x:H

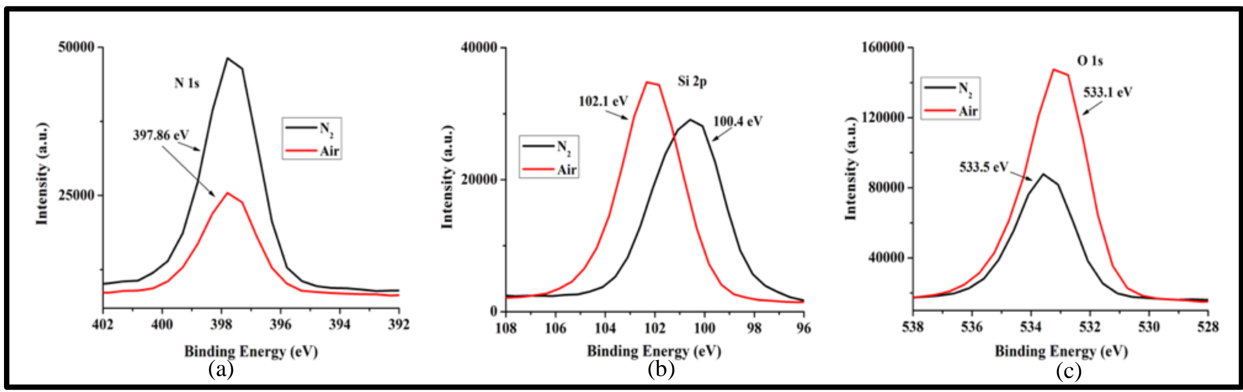


Fig. 5.14. XPS spectra of (a) N 1s peaks, (b) Si 2p peaks, and (c) O 1s peaks of the TOPCon/SiN_x:H samples after RTA at 825 °C under N_2 and air atmospheres.

Fig. 5.14. shows the compositional XPS spectra of the TOPCon/SiN_x:H stack annealed at 825 °C both in N_2 and air. In Fig. 5.14. (a), it was observed that there was a comparatively lower count of the N (1s) peak at 397.86 eV in the air-annealed sample than in N_2 annealed. This suggested a decrease in the Si-N bond in the top region of the SiN_x:H layer film after air annealing compared with the N_2 annealing. This is due to the possible Si-O bond formation on the SiN_x:H

surface. In Fig. 5.14. (b), it was observed that there was a Si (2p) peak at 100.4 eV in N_2 annealing and 102.1 eV in air. The XPS peak at 100.4 eV, observed after N_2 annealing, is attributed to the presence of the Si-Si_3N_1 complex, and the peak at 102.1 eV, observed after air annealing, is attributed to the formation of SiO_x complexes [191][192][193][194]. The Si-N peak is expected to be located at 101.7 eV, and the SiO_2 peak to be at 103.5 eV, but peak positions are sensitive to stoichiometry [195]. Finally, after air annealing, the O (1s) peak intensity at 533.1 eV was higher than N_2 annealing, as shown in Fig. 5.14. (c). This proved that more surficial SiO_2 and stoichiometric changes occurred during the air annealing, as previously shown by Miller and Linton [196] and Lin and Hwu [197].

The results on crystallinity property determination by Raman spectroscopy, chemical changes by FTIR and XPS, and electrical property changes by sheet resistance measurement have been presented. As the annealing temperature increases, the poly-Si crystalline fraction and iV_{OC} increase, implying lower charge-carrier recombination. The FTIR measurements were not sensitive enough to detect the passivation quality; however, it detects dehydrogenation in SiN_x:H capped samples. The depth-profiling XPS measurements show a higher oxygen concentration in the ultrathin oxide after air annealing, which could lead to higher iV_{OC} than N_2 for uncapped samples. The surface morphology shows the blister formation affecting the carrier selectivity and, hence, the surface passivation.

The disadvantages of lower temperature LPCVD of poly-Si at 530 ºC have been observed, which led us to opt for a higher temperature of 588 ºC LPCVD. In the upcoming sub-sections, the scientific findings have been described for the second set of test samples with LPCVD poly-Si deposited at 588 ºC and a thicker poly-Si layer.

D. Effects of heating time t_{heat}

Fig. 5.15. shows the variation of peak PL intensity and the sheet resistances w.r.t. the RTA heating time t_{heat} at constant t_{hold} = 300 sec and t_{cool} = 300 sec. At t_{heat} = 10 sec or heating rate R_{heat} = ~80 ºC/s, the peak PL intensity dropped from 450 a.u. to 110 a.u. As the time t_{heat} was increased from 60 sec to 300 sec (or $R_{heat} \leq$ ~13 ºC/s), the peak PL intensity climbed back and saturated at the PL intensity of the starting sample. The FGA recovered the peak PL intensity of test samples treated only at $t_{heat} \geq 60$ sec to a saturated value of ~1525 a.u., comparable to the furnace annealed reference sample (~2100 a.u.), and the fast heated t_{heat} = 10 sec sample did not recover. This showed that a fast heating rate (R_{heat} = ~80 ºC/s) irreversibly degraded the surface passivation quality beyond recovery, and FGA could not improve it further. The optimized value of t_{heat} is ≥ 60 sec.

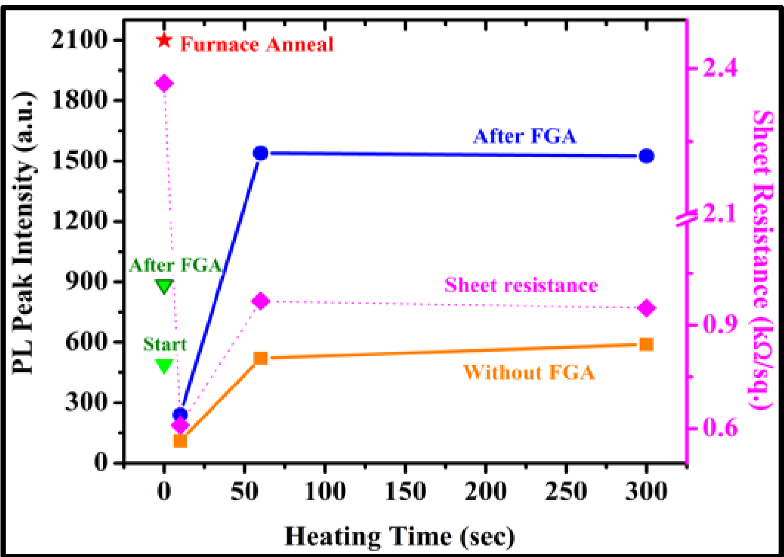


Fig. 5.15. The dependence of peak PL intensity counts and sheet resistance on RTA heating times. The data for as-prepared (start), after FGA treatment of as-deposited sample, and furnace annealed are also shown.

The sheet resistance dropped significantly and saturated at 0.9-1.1 kΩ/sq. at fast heating rate R_{heat} = ~80 ºC/s which is comparable to furnace anneal. The dip at t_{heat} = 10 sec should be treated as within the error bar. This proved that a fast heating rate of ~80 ºC/s generates significant dopant activation but degrades iV_{OC}.

E. Effects of holding time t_{hold}

Fig. 5.16. shows the variation of peak PL intensity and the sheet resistances w.r.t. the RTA holding time t_{hold} at constant t_{heat} = 60 sec and t_{cool} = 300 sec. From t_{hold} = 10 sec to 100 sec, the peak PL intensity showed an increasing trend w.r.t. the starting condition. At t_{hold} > 100 sec, PL intensity counts saturate. After FGA, both test samples under t_{hold} = 60 sec and 300 sec showed a significant jump in the peak PL intensity and saturated at ~1800 a.u. The test sample with the shortest hold time of 10 sec did not recover the PL intensity. This showed that a short holding time of 10 sec caused irreversible degradation to the surface passivation quality beyond recovery, and FGA could not improve it further. The optimized condition for the value of t_{hold} starts from 60 sec.

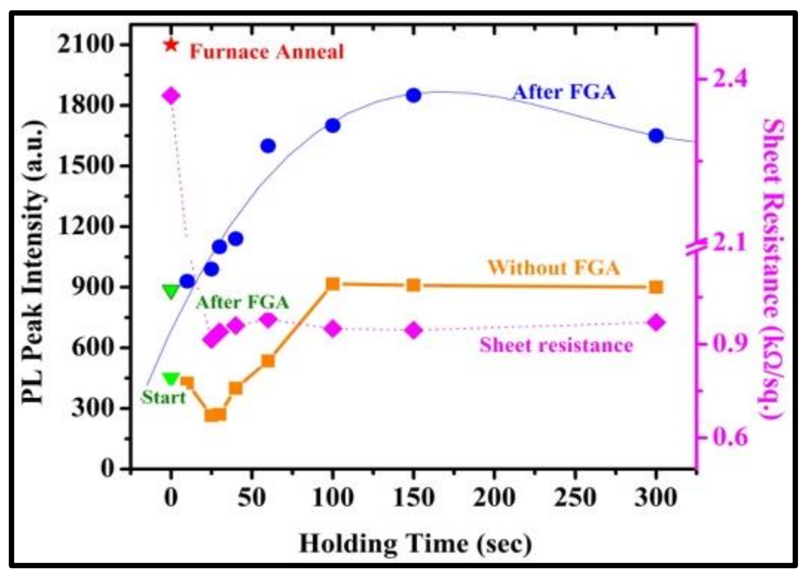


Fig. 5.16. The dependence of peak PL intensity counts and sheet resistance on RTA holding times. The data for as-prepared (start), after FGA treatment of as-deposited sample, and furnace annealed are also shown.

The sheet resistance dropped significantly and saturated at 0.9-1.1 kΩ/sq., starting at a short holding time of 10 sec, comparable to furnace anneal. Hence, dopant activation occurs at 10 sec or longer hold time.

F. Effects of cooling time t_{cool}

Fig. 5.17. shows the variation of peak PL intensity and the sheet resistances w.r.t. the RTA cooling time t_{cool} at constant t_{heat} = 60 sec and t_{hold} = 300 sec. At t_{cool} = 10 sec or cooling rate R_{cool} = ~80 ºC/s, the peak PL intensity dropped from 450 a.u. to 12 a.u. As the time regime of t_{cool} was increased from 60 sec to 300 sec (or $R_{cool} \leq$ ~13 ºC/s), the peak PL intensity climbed back gradually to the starting sample PL intensity counts. The peak PL intensity of the test sample treated under the shortest cooling time t_{cool} = 10 sec did not recover after FGA. On the other hand, the FGA regained the peak PL intensity of test samples treated at t_{cool} = 60 sec to a value of ~800 a.u., and the highest peak PL intensity rise to 1550 a.u. was recorded at t_{cool} = 300 sec comparable to furnace annealed reference sample (~2100 a.u.). It was observed that a fast quenching/ cooling rate (R_{cool} = ~80 ºC/s) irreversibly degraded the surface passivation quality beyond recovery, and FGA could not improve it further. The optimized value of t_{cool} is ≥ 300 sec.

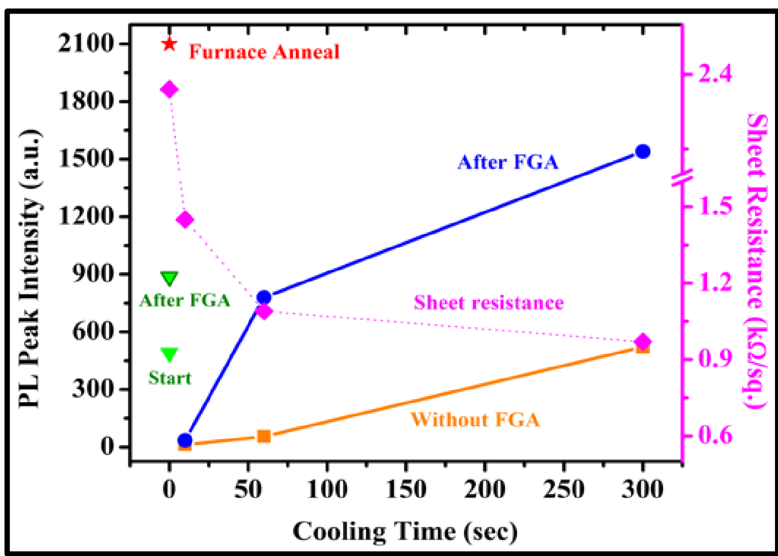


Fig. 5.17. The dependence of peak PL intensity counts and sheet resistance on RTA cooling times. The data for as-prepared (start), after FGA treatment of as-deposited sample, and furnace annealed are also shown.

Sheet resistances decreased gradually as the cooling rate fell, which showed that the dopant activation was affected moderately with a fast cooling rate.

G. Optimization of RTA parameters

For better device performance, the optimized RTA heating, holding, and cooling times were 60 sec, 60 sec, and 300 sec. Table 5.3. shows some of the optimized performances of p-TOPCon devices after RTA.

Table 5.3. Carrier lifetime, iV_{oc}, and sheet resistance after optimized RTA

No.	RTA timing conditions (sec) at 825 °C/ N_2		τ (μs)	iV_{OC} (mV)	Sheet resistance (kΩ/sq.)
1	t_{heat}= 60; t_{hold}= 100; t_{cool}= 300	Starting	15	573	1.0-1.1
		After RTA	56	602	
		After FGA	97	628	
2	t_{heat}= 60; t_{hold}= 150; t_{cool}= 600	Starting	11	571	0.9-1.0

		After RTA	78	607	
		After FGA	112	633	
3	t_{heat}= 150; t_{hold}= 150; t_{cool}= 600	Starting	14	571	0.9-1.0
		After RTA	72	609	
		After FGA	133	638	

The reference furnace anneal sample had sheet resistance of 0.9-1.0 kΩ/sq., a lifetime of ~300 μs, and an iV_{OC} of 688 mV. Post-anneal FGA further enhanced the overall performances. The sheet resistances were reduced to ~0.9 kΩ/sq, which showed that complete dopant activation was achievable under RTA conditions. Using longer RTA durations may probably increase the iV_{OC} and lifetime, but it will defeat the purpose of "rapidity" of our RTA processing.

H. Effect of B-doped poly-Si layer on passivation quality

Fig. 5.18. shows the dependence of PL intensity counts on the presence of boron-doped poly-Si layer. The test samples were treated under the RTA conditions t_{heat} = 60 sec, t_{hold} = 100 sec, and t_{cool} = 300 sec at 825 ºC in N_2. To evaluate the effect of boron diffusion into Si during the furnace and RTA annealing process, the doped poly-Si layer was chemically etched away after annealing, and the PL was measured. These results were compared with the samples that did not have a doped poly-Si layer but went through RTA and furnace annealing under similar conditions.

The peak PL intensity counts derived from Fig. 5.18. have been tabulated in Table 5.4. Comparing Cases 1 and 2, it is observed that the RTA enhanced the passivation quality of the ultrathin SiO_x layer. Comparing Cases 1 and 3, it is observed that the presence of a poly-Si layer provides additional passivation in the absence of RTA. In case 4, it is observed that the RTA moderately improved the overall passivation quality. Case 5 shows the best passivation quality was obtained after furnace annealing.

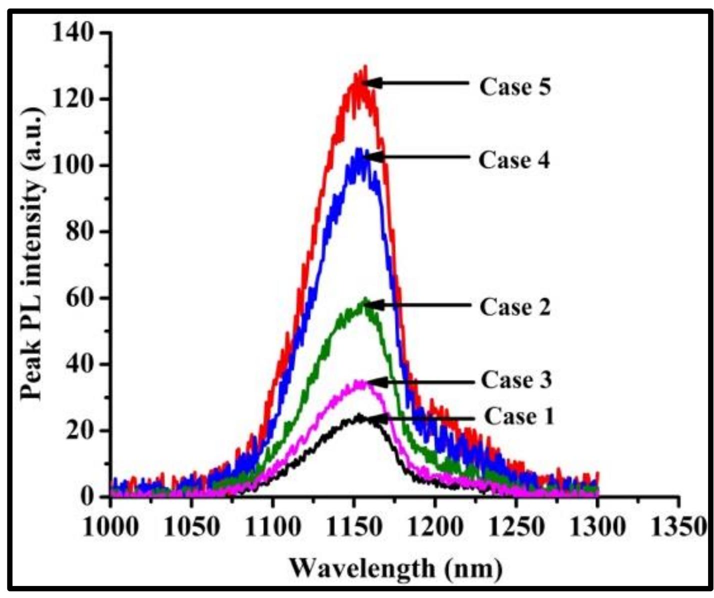


Fig. 5.18. The dependence of PL intensity counts on the presence of boron-doped poly-Si layer.

Table 5.4. Peak PL intensity of the effects of B-doped poly-Si layer on the passivation quality

Case	RTA at 825 ºC t_{heat}= 60 s, t_{hold}= 100 s, t_{cool}= 300 s	Peak PL Intensity (a.u.)
1	SiO_x deposited on Si	25
2	After the RTA of SiO_x deposited on Si	57
3	After poly-Si deposition on SiO_x/Si	33
4	After RTA of poly-Si deposition followed by its chemical etch	108
5	After Furnace anneal of poly-Si deposition followed by its chemical etch	127

In the case of RTA with a poly-Si layer, the boron dopants could diffuse through the pin-holes in the SiO_x layer into bulk Si and also through the ultrathin SiO_x layer. This diffused layer will provide additional field-effect passivation, exhibiting higher PL counts even after removing the poly-Si layer. The furnace-annealed samples showed the best performance due to the slower

boron diffusion in bulk Si under a longer duration of heating and cooling times. In the case of RTA with a poly-Si layer, over-diffusion of boron might have caused Auger recombination, which lowered the passivation quality. This might also explain the cause of the discrepancy in the iV_{OC} between optimized-RTA and reference furnace anneal samples. The performance lag of p-TOPCon compared to the n-TOPCon could possibly be due to lower improvements in interface properties and the amount of boron diffusion in Si. It has been reported that boron diffusion is much faster under RTA compared to slow furnace annealing [198].

I. Effects of pulsed RTA processing

This study aimed to investigate the effects of a series of short pulses of RTA on the dopant activation and passivation quality of p-TOPCon devices. The results have been tabulated in Table 5.5.

Table 5.5. iV_{oc} and sheet resistance after optimized pulsed RTA. Both heating and cooling times were fixed at 60 sec.

Pulsed RTA Holding time (sec)	Number of RTA pulses	Starting sample peak PL intensity counts (a.u.)	After RTA peak PL intensity counts (a.u.)	After FGA peak PL intensity counts (a.u.)	Sheet resistance (kΩ/sq.)
10	1	410	120	330	1.9
	5		380	1200	1.45
	10		410	1350	1.35
60	1		100	570	1.8
	5		450	660	1.6
	10		390	1100	1.4

At both holding times (10 and 60 sec), the number of pulses varied from 1 to 10. There was a preliminary decrease in PL intensity after RTA for each holding time, which improved after multiple pulses. This confirmed that the PL intensity counts increased as the cumulative holding

times increased, and the passivation quality improved, reaching back to the starting sample condition. An increasing trend in PL intensity counts was observed with the increase in the number of pulses, which was further improved by post-anneal FGA. It is to be noted that the cooling time of each of the RTA pulses is the most influential aspect, as it eradicates any sort of defects formed during the heating and holding times of each RTA pulse. If we compare the results based on different holding times, the changes in PL intensity counts were similar within the error bar and suggested no significant difference in the final PL intensity counts.

In the case of sheet resistance measurements, a gradual decrease was observed with the increase in the number of RTA pulses. This suggested that the first RTA pulse started the dopant activations process, and the sheet resistance decreased from 2.4 kΩ/sq. to 1.9 kΩ/sq. Later, this trend saturated as the number of pulses increased. It is possible to lower the sheet resistance further by increasing the cumulative holding time and the number of RTA pulses, but it will defeat the purpose of "rapidity" in our RTA processing. Our results show that the RTA process for p-TOPCon does not improve the iV_{OC} at the same level as furnace annealing for n-TOPCon. This possibly could be due to higher boron diffusion under the RTA process.

5.3. Conclusion

This study delved into several aspects of RTA of in-situ B-doped poly-Si-based p-TOPCon solar cells and explored the impact of the RTA atmosphere on various characteristics. Firstly, the investigation encompassed surface morphology, surface passivation, alterations in polysilicon crystallinity, compositional changes, sheet resistance, and the determination of oxidation states in the ultrathin SiO_2 passivation layer under RTA. Additionally, the study revealed that intense light exposure during RTA had a substantially detrimental effect on surface passivation quality, leading

to a decline in iV_{OC}. Moreover, it was discovered that employing a single-step RTA process after depositing a SiN_x:H layer on top of the polysilicon yielded a notably high iV_{OC} value of 706 mV.

To ensure optimal passivation, efforts were directed towards minimizing hydrogen-induced blister formation during annealing, as confirmed by PL measurements indicating their negative impact on surface passivation. Notably, air-based RTA yielded a higher iV_{OC} than nitrogen for SiN_x:H-uncapped samples. It was necessary to avoid UV and visible light radiation exposure during high-temperature RTA to prevent degradation. The Si-O bond transitioned from wagging to stretching mode under annealing at 875 °C. The sheet resistance, as low as 0.9 kΩ/sq, could be achieved for a 30 nm in-situ B-doped polysilicon film under RTA.

The findings emphasized that RTA at around 825 °C maximized the fraction of the polycrystalline phase, and N_2-based RTA for SiN_x:H-coated polysilicon film resulted in higher iV_{OC} values than uncoated films. Addressing the initial hydrogen content during the as-deposited TOPCon structure formation is crucial to minimize blister formation. Additionally, LPCVD of in-situ B-doped a-Si:H should be performed at 588 °C to curtail hydrogen incorporation and enhance the poly-crystalline fraction.

The effects of heating, holding, and cooling time on the passivation quality and dopant activations during RTA processing (at 825 ºC/ N_2) in-situ boron-doped p-TOPCon solar cells were investigated. These test samples had poly-Si layers deposited at 588 º C. Fast heating and cooling rates (≥ 80 ºC/s) damaged the passivation quality irreversibly, beyond any post-anneal FGA recovery. Slower heating (≤ 13.3 ºC/s) and cooling (≤ 2.6 ºC/s) rates provided the best PL intensity results. The start of the dopant activation process required at least 10 sec of holding time, which was determined by the decreasing trend in the sheet resistance. The RTA parameters were optimized at a heating time of 60 sec, a holding time of 60 sec, and a cooling time of 300 sec. At

optimized parameters, considerable improvements in peak PL intensity counts and passivation quality of the test devices were observed, which further improved with the external FGA hydrogenation. The best performances were recorded as carrier lifetime of 133 μs, iV_{OC} of 638 mV, and sheet resistance of ~0.9 kΩ/sq., at a heating time of 150 sec, a holding time of 150 sec, and a cooling time of 600 sec. The RTA processing of the etched poly-Si layer proved that the boron dopant diffusion could provide additional field-effect passivation. An over-diffused dopant profile creates Auger recombination and is detrimental to the overall passivation quality. The pulsed RTA processing showed the potential to create dopant activation and passivation adequately, and longer cumulative holding times can give better results.

CHAPTER 6: Fabrication of dopant-free bifacial TMO-based CSPC Si solar cells

In this chapter, a preliminary study was conducted to fabricate complete dopant-free bi-facial CSPC Si solar cell devices consisting of transition metal oxides (TMO) as carrier-selective layers, passivation, and tunneling interlayers on c-Si substrates. Here, the term 'complete' refers to the fabrication until pre-metallization step in this preliminary study. The effects of pre-deposition HF etch, growth of SiO_x, optimizations of ALD of Al_2O_3 and TiO_x, thermal evaporation and deposition of MoO_x, consequences of post-deposition FGA, and the potentiality of using short wavelength CW laser annealing have been investigated to improve the passivation quality, carrier lifetime and iV_{OC} of the test CSPC Si devices. The test device samples were characterized using photoluminescence (PL) for passivation quality and quasi-steady state photoconductance (QSSPC) minority carrier lifetime measurements. The results showed a successful approach toward laser processing.

6.1. Experimental

A. Fabrication of the TMO CSPC test structure and characterization

Fig. 6.1. gives an overview of the fabrication steps of the bifacial CSPC device structure. The double-side polished phosphorus-doped FZ c-Si <100> type wafers with a thickness of 280 µm and 1-5 Ω.cm resistivity were used for the experiments. The c-Si wafers were cut into 1-

inch × 1-inch samples and then treated with RCA cleaning. The removal of native oxides on the selected Si wafer substrates using 2% HF solution for 2 minutes was not performed.

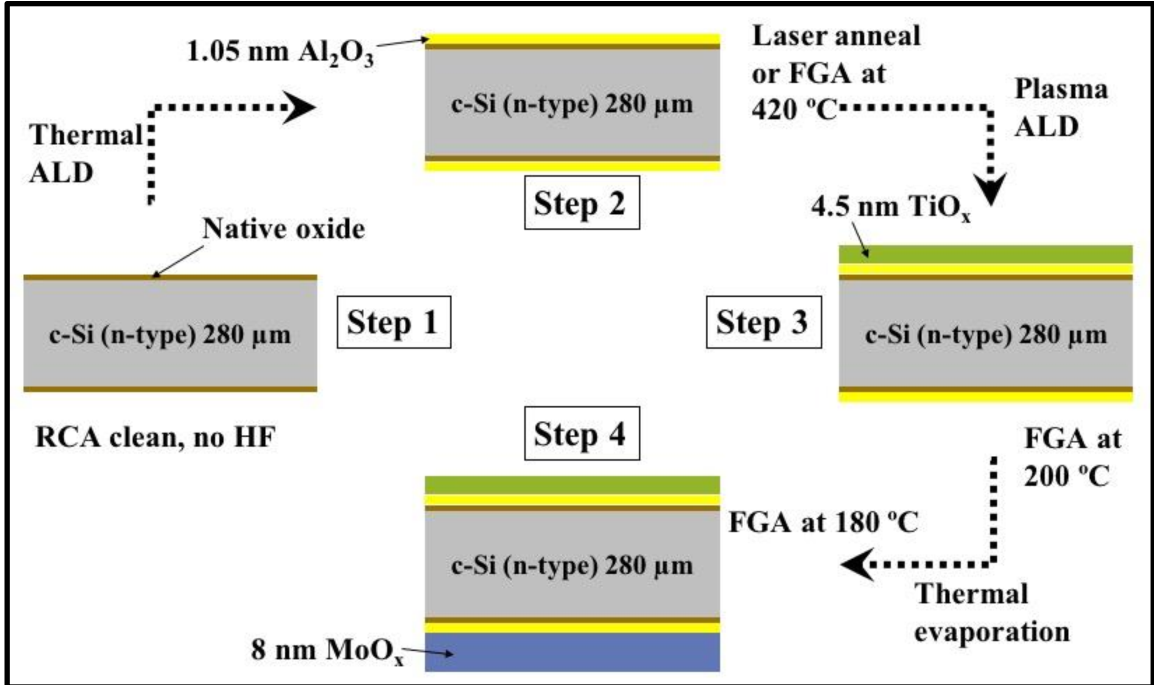


Fig. 6.1. Schematic diagram of the fabrication steps of the bifacial TMO-based CSPC Si solar cells. Step 1 involves the RCA cleaning and keeping native oxide intact without HF etch. Step 2 requires the thermal ALD of 1.05 nm Al_2O_3, followed by either laser annealing or FGA at 420 ℃ for 5 min. Step 3 entails the plasma ALD of 4.5 nm TiO_x as ETL, followed by FGA at 200 ℃ for 10 min. Finally, step 4 involves the 8 nm of MoO_x deposition by thermal evaporation of MoO_x, followed by FGA at 180 ℃ for 5 min.

All the ALD processes were done in the Oxford FlexAL™ system. The optimization study of the passivation/tunneling Al_2O_3 layers was done in two modes: plasma and thermal. A thickness of 1.05 nm of plasma ALD Al_2O_3 was deposited at 200 ℃ and 80 mTorr pressure at the rate of 1.2 Å/cyc. The precursor materials were TMA and O_2 plasma. Similar thicknesses of thermal ALD Al_2O_3 were also deposited at 200 ℃ and 80 mTorr pressure at the rate of 1.0 Å/cyc. The precursor materials were TMA and H_2O. The electron transport layer (ETL) of TiO_x of 4.5 nm thickness was

deposited using plasma ALD process at a low temperature of 170 ºC and 40 mTorr pressure and at a rate of 0.5 Å/cyc using the precursors TDMAT and O_2 plasma. Due to the unavailability of ALD precursors and recipes, ~8 nm thick hole transport layer (HTL) of MoO_x was deposited in a thermal evaporator using MoO_3 pellets on Mo boat at a pressure of 10^{-5} Torr at the rate of 10 Å/min. For the comparison study of SiO_x and Al_2O_3 as a passivation layer, 1.5 nm of SiO_x were grown on the HF-treated Si substrates using 70% wt. electronics grade HNO_3 at 100 °C for 15 minutes. To study the effect of the furnace annealed SiO_x passivation layer, a Centrotherm tube furnace was used for annealing at 875 ºC in N_2 for 30 minutes, similar to the TOPCon fabrication [74]. The forming gas annealing (FGA) was conducted in the AnnealSys rapid thermal processing (RTP) system in forming gas (5% H_2: 95% Ar) from Praxair. The FGA temperatures were varied from 180 ºC to 420 ºC, according to the need for optimization at different fabrication steps.

The laser annealing was done using a continuous wave (CW) multi-mode laser from NUBURU (AO-150 model) with a wavelength of 450 nm and a maximum average power of 150 W. The laser beam was focused to a spot size of ~100 µm, and the laser power was optimized at ~18 W. The test samples were mounted on the translational X-Y stage. The scan velocity was set at 3 mm/s, and the overall overlap between the laser spots was 50%.

The photoluminescence (PL) characterization was accomplished using a 532 nm excitation laser at 70 mW power, and the spot size was ~150 µm. The peak PL intensity counts were determined at a wavelength of 1145 nm within ± 25 a.u. error bar. The QSSPC iV_{OC} measurements were conducted on (1″ × 1″) area test samples using a WCT-120 Silicon Wafer Lifetime Tester made by Sinton Instruments. The input of sample thickness was manually set as 0.025 cm with 3.5 Ω-cm resistivity, n-type dopant, 0.7 optical constant and generalized analysis mode. The iV_{OC} and the minority carrier lifetime data were generated at 1 Sun condition at the minority carrier

density of 1×10^{15} cm^{-3}. The error bars in the lifetime and iV_{OC} measurements were ~15 μs and 2 mV, respectively.

6.2. Results and discussions

A. Optimization of pre-ALD HF treatment of Si wafers

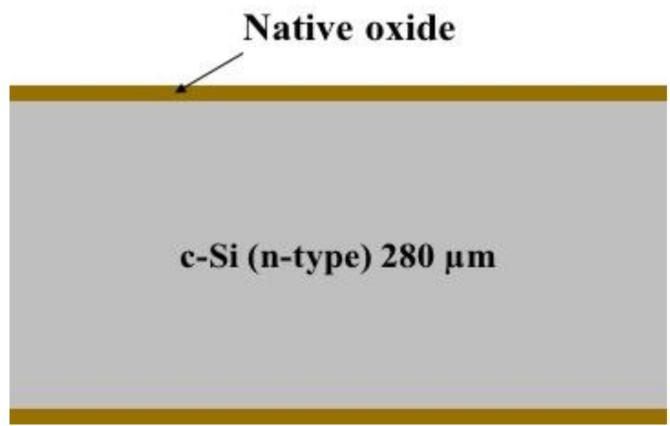


Fig. 6.2. Schematic diagram of the symmetric bifacial TMO-based CSPC Si device where the native oxide is kept intact without HF etch.

The effect of HF treatment before the commencement of ALD of Al_2O_3 on Si wafers has been investigated. The schematic diagram of the CSPC device with native oxide is shown in Fig. 6.2. Due to its very high selective etch rate of SiO_2 over Si, HF etching was conducted to remove the native oxide. The thickness of native oxide is said to vary from 1.9 to 7.6 Å [199]. Each case result represents an average of three test samples. Later, all these test samples were symmetrically coated with 1.05 nm of thermal ALD Al_2O_3 layers. The peak PL intensity count was measured at a wavelength of 1145 nm.

Table 6.1. Optimization based on the effects of HF etching of native oxide. All samples were symmetrically coated with 1.05 nm thick Al_2O_3. The FGA was conducted at 420 ℃ for 5 minutes.

Case	Condition	Before FGA			After FGA		
		PL (a.u.)	τ (µs)	iV_{OC} (mV)	PL (a.u.)	τ (µs)	iV_{OC} (mV)
1	HF etching of native oxide	15	10	547	200	90	556
2	No HF etch	25	33	562	610	180	583

The results have been tabulated in Table 6.1. It was observed that in case 1, the test samples did not have native oxides due to HF etching, and the Al_2O_3 was directly deposited on the RCA-terminated Si wafer surface, which resulted in lower PL intensity counts, carrier lifetime, and iV_{OC}. After the administration of external hydrogenation by FGA, the PL intensity increased 13 times, carrier lifetime 9 times, and the final iV_{OC} reached 556 mV. On the other hand, in case 2, the test samples had both native oxide and Al_2O_3 layers, which resulted in higher starting PL intensity counts, carrier lifetime, and iV_{OC}. FGA improved the overall performances and resulted in an iV_{OC} of 583 mV, 4.85% higher than case 1. This showed that the presence of native oxide was essential for better passivation quality in addition to field-induced passivation of the Al_2O_3 layer, and FGA improved further by passivating interface defects. This finding is also in agreement with the results reported by Getz *et al.* [200].

B. Optimization of ALD Al_2O_3 layers

The effects of two modes of ALD, namely plasma and thermal, for Al_2O_3 deposition on Si/native oxide substrates, have been investigated. Plasma ALD involves low-temperature plasma-based activation of a wide variety of precursor materials into reactive radicals, which get

chemisorbed onto the substrate surface. Thermal ALD involves higher temperatures for activating and vaporizing limited precursor materials, which get chemisorbed onto the substrate surface.

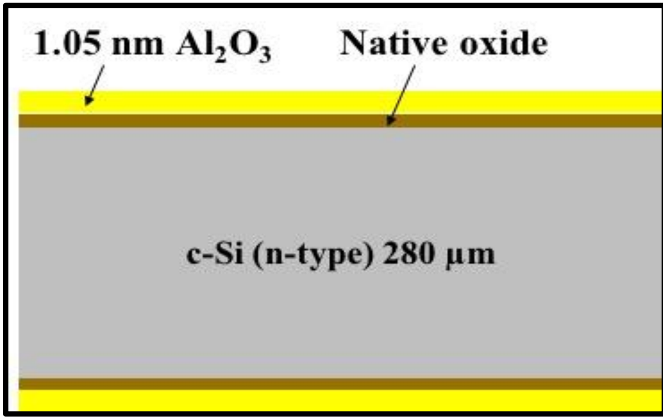


Fig. 6.3. Schematic diagram of the symmetric bifacial TMO-based CSPC Si device where the thermal ALD of 1.05 nm Al_2O_3 was done on the native oxides.

Considering the negatively charged field-effect passivation and charge carrier-specific tunneling effect of Al_2O_3 and the thickness of native oxide, the thickness of Al_2O_3 was decided to be kept at 1.05 nm. This ensured that the final passivation and tunneling capabilities of the test devices were not affected by their cumulative thickness. The post-deposition anneal required for ALD Al2O3 is 673-723 K or ~400-450 ℃ [201][202]. The schematic diagram of a symmetric bifacial CSPC device with native oxide and thermal ALD Al_2O_3 is shown in Fig. 6.3.

Table 6.2. Optimization based on the effects of type of ALD process for 1.05 nm of Al_2O_3 deposition. All the samples had native oxide and did not go through HF etching. The FGA was conducted at 420 ℃ for 5 minutes.

Case	Type of ALD	Before FGA			After FGA		
		PL (a.u.)	τ (μs)	iV_{OC} (mV)	PL (a.u.)	τ (μs)	iV_{OC} (mV)
1	Plasma at 200 ºC	9	12	535	603	173	581
2	Thermal at 200 ºC	124	65	578	604	176	583

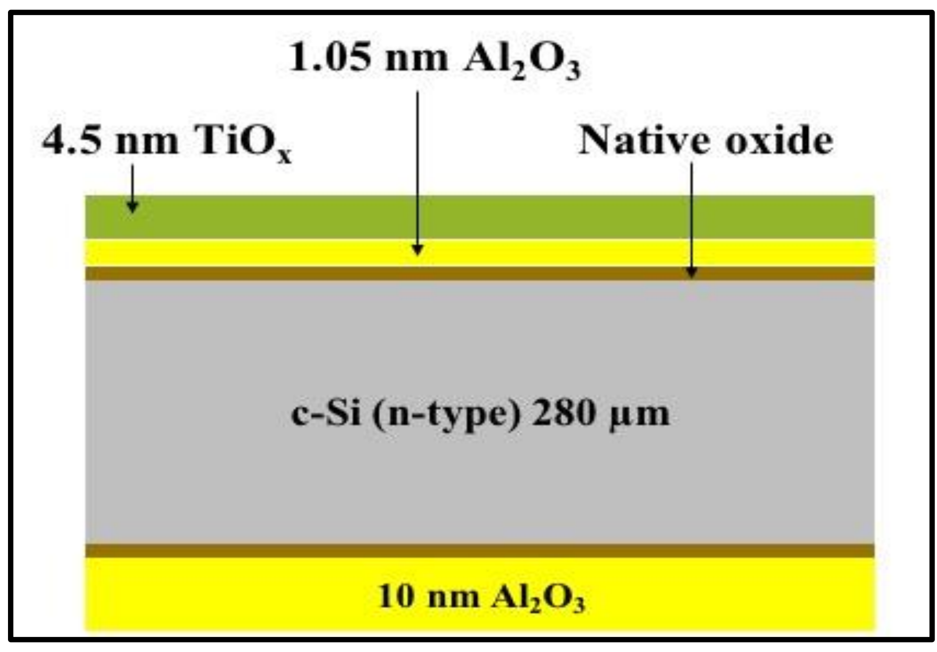
Table 6.2. shows the ALD process optimization results for 1.05 nm Al_2O_3 for symmetric test samples. Each case represents the averaged data of 4 samples. In case 1, the samples had symmetric structures of native oxide and plasma ALD of Al_2O_3 layers. In case 2, the samples had symmetric structures of native oxide and thermal ALD of Al_2O_3 layers. Comparing both cases, it was observed that although the thermal ALD had better starting performance than plasma ALD samples, both modes of ALD caused a similarly high level of surface passivation quality and iV_{OC} of 580-583 mV after FGA.

These results indicate that there should have been a higher hydrogen content in thermal ALD, which improved the passivation quality compared to plasma ALD. Additionally, the in-situ annealing during thermal ALD might have improved passivation quality and iV_{OC}. The saturation in hydrogen content during FGA possibly caused similar performances in thermal and plasma ALD samples. These results coincide with the earlier findings of Dingemans *et al.*, who reported that thermal ALD has 3.6 at.% more hydrogen content than plasma ALD [203]. The thermal ALD approach was undertaken henceforth for the fabrication of CSPC devices.

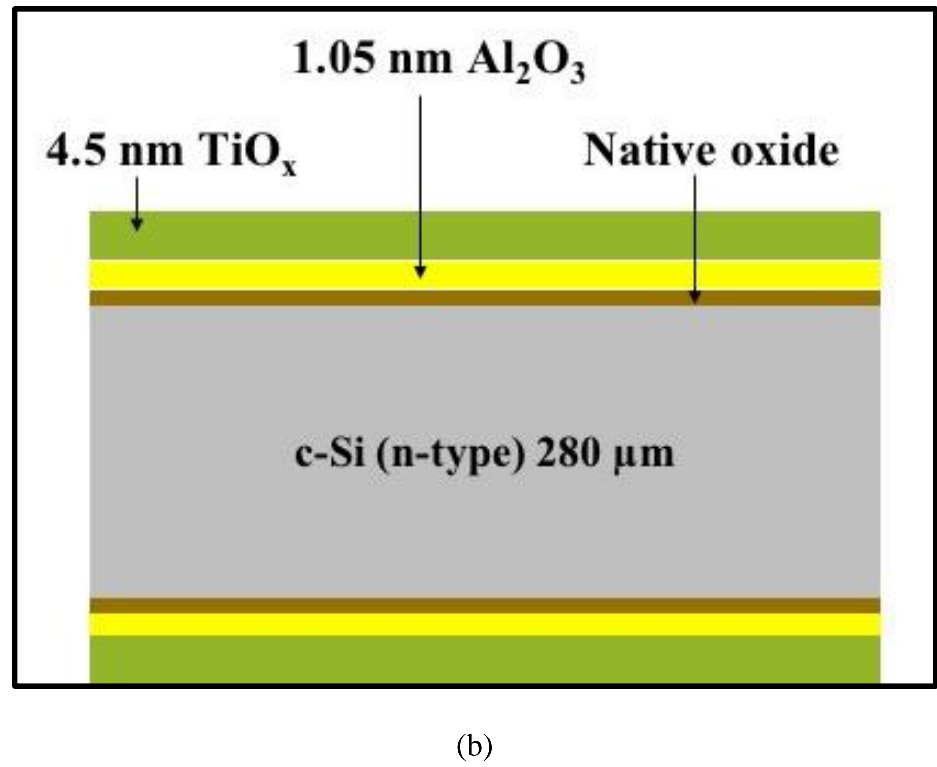
C. Optimization of ALD TiO_x as electron transport layer (ETL)

The effects of adding ALD TiO_x as ETL on the carrier lifetime and iV_{OC} of the asymmetric structures with thicker Al_2O_3 layer and symmetric structures of c-Si/Native oxide/Al_2O_3 (thermal ALD) test devices have been investigated. The TiO_x was deposited at a low temperature of 170 ºC

using Plasma ALD mode. Two test samples were fabricated to study the effectiveness of single-side deposition of TiO_x, where the other side of the test samples was highly passivated by 10 nm of ALD Al_2O_3 layer. The thickness of TiO_x was chosen to be 4.5 nm following the reports made by Yang et al. [95]. Post-deposition FGA was used at a lower temperature of 200 ℃ for 10 minutes to avoid the anatase phase, film cracking, and lifetime degradation [204]. This ensured that the non-stoichiometric oxygen vacancies and crystalline phase of TiO_x were not affected, which is generally considered essential for the electron transport property [205].



(a)



(b)

Fig. 6.4. Schematic diagrams of the bifacial TMO-based CSPC Si solar cells with (a) thermal ALD of 10 nm Al_2O_3 on the rear side to understand the passivation effects of TiOx as ETL and (b) thermal ALD of 1.05 nm Al_2O_3.and 4.5 nm TiOx on the native oxide symmetrically. The front sides had native oxide, thermal ALD of 1.05 nm Al_2O_3, and 4.5 nm TiO_x.

Table 6.3. Optimization based on the effects of ALD of 4.5 nm TiO_x on asymmetrically structured devices is shown in Fig. 6.4. (a). The ALD 10 nm of Al_2O_3 passivated the rear side of the samples to study the passivation effect of TiO_x. The FGA was done at 200 ºC for 10 min.

Sample	**Conditions**	**Before 4.5 nm TiO_x**		**After 4.5 nm TiO_x on single-side**		**After FGA**	
		τ (µs)	**iVoc (mV)**	**τ (µs)**	**iVoc (mV)**	**τ (µs)**	**iVoc (mV)**
1	c-Si/Nat.ox/ 10 nm Al_2O_3	192	601	216	616	319	629
2	c-Si/Nat.ox/ 10 nm Al_2O_3	193	606	198	609	302	628

Table 6.3. shows the tabulated results of optimizing the ALD TiO_x layer in two separate asymmetric test devices shown in Fig. 6.4. (a). This experiment aimed to understand the passivation effects of TiO_x as ETL. It was observed that the 10 nm Al_2O_3 layer caused a high starting iV_{OC} and carrier lifetime due to its superb passivation on one side. This allowed us to investigate the effects of TiO_x on the overall performances of the CSPC devices. The TiO_x layer improved the iV_{OC} by 15 mV to reach 616 mV, which increased further to a final ~629 mV after FGA. The deposition of the TiO_X layer has a minimal improvement in iV_{OC}, so it is not contributing much to the passivation as 10 nm Al_2O_3 was found to be sufficient. Moreover, the FGA should have possibly constructively contributed to the molecular rearrangements at the interfaces and inhibition of defects by hydrogenation without hampering the non-stoichiometric nature of TiO_x.

The investigation was continued by fabricating a symmetric architecture of c-Si/native oxide/Al_2O_3/TiO_x devices, as shown in Fig. 6.4. (b), employing all our previous optimization results. The results have been tabulated in Table 6.4. It was observed that the best result achieved was iV_{OC} of 625 mV of a symmetric structure employing TiO_x as ETL. It was observed that the passivation due to Al_2O_3 was stronger than that of TiO_x.

Table 6.4. Performances of symmetric CSPC device structures, shown in Fig. 6.4. (b), using TiO_x as ETL.

Sample	**Conditions**	**Before 4.5 nm TiO_x**		**After 4.5 nm TiO_x**		**After FGA**	
		τ (μs)	**iV_{OC} (mV)**	**τ (μs)**	**iV_{OC} (mV)**	**τ (μs)**	**iV_{OC} (mV)**
1	Symmetric c-Si/Nat.ox/ 1.05 nm Al_2O_3	178	582	191	601	283	625
2	Symmetric c-Si/Nat.ox/ 1.05 nm Al_2O_3	167	579	183	591	269	621

D. Investigation of the effects of the deposition of MoO_x as a hole transport layer (HTL)

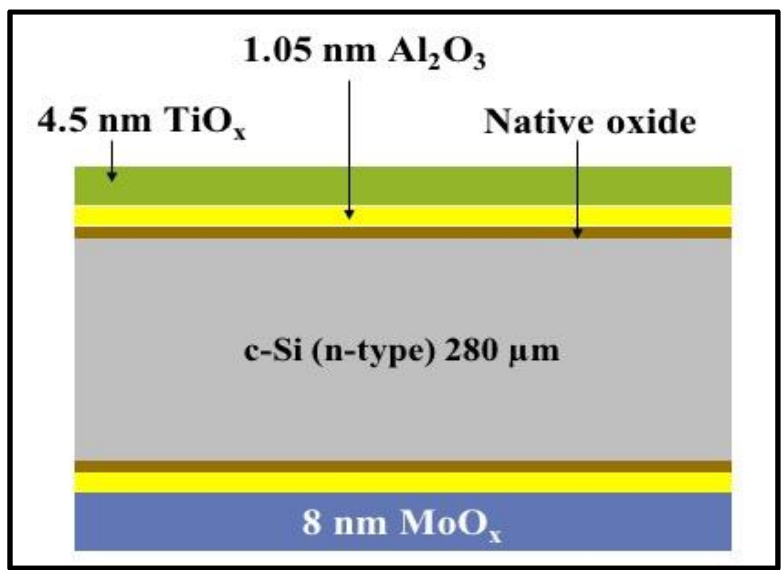


Fig. 6.5. Schematic diagram of the complete bifacial TMO-based CSPC Si solar cell. After 8 nm of MoO_x deposition by thermal evaporation, FGA was done at 180 ºC for 5 min.

Two complete test device architectures employing symmetric structures of native oxide, 1.05 nm thermal ALD Al_2O_3, were used. Both these test device samples had optimized 4.5 nm Plasma ALD TiO_x as ETL and thermally evaporated MoO_x as HTL. The schematic of a complete bifacial CSPC solar cell is shown in Fig. 6.5. Due to the unavailability of ALD infrastructure for MoO_x, physical vapor deposition (PVD), also known as thermal evaporation, was used for the deposition of MoO_x. The thickness of the MoO_x layer was chosen to be ~8 nm, according to the earlier optimization study done by Wu *et al.* [206]. The results of two completely fabricated CSPC devices have been tabulated in Table 6.5.

Table 6.5. Performances of complete CSPC device structures using TiO_x as ETL and MoO_x as HTL. The FGA was done after Al_2O_3 and TiO_x depositions for 5 and 10 minutes, respectively. The FGA was done after MoO_x for 5 min.

Sample	Before 8 nm MoO_x		After 8 nm MoO_x		FGA temperature	After FGA	
	τ (μs)	iV_{OC} (mV)	τ (μs)	iV_{OC} (mV)		τ (μs)	iV_{OC} (mV)
1	276	626	283	627	180 ℃	286	629
2	256	621	249	625	250 ℃	188	614

It was observed that the best result achieved was iV_{OC} of 629 mV with a minority carrier lifetime of 286 μs after the administration of FGA at 180 ℃ for 5 min. The results of annealing at 250 ℃ coincide with the earlier findings by Gregory *et al.*, who showed that temperature above 200 ℃ caused degradation in MoO_x quality and overall passivation quality [207]. High-temperature annealing causes additional SiO_x interlayer growth under Al_2O_3, increases the total interlayer thickness, and decreases the tunneling effect and passivation [208]. The deposition of TiO_x and post-deposition annealing should precede the MoO_x deposition since the thermal stability of MoO_x is lower than that of TiO_x.

E. Comparison with laser annealing methodology

The feasibility of laser annealing in the fabrication of complete CSPC devices has been investigated. The laser annealing was accomplished only after the thermal ALD of Al_2O_3 but did not replace the other FGA steps in the fabrication process. Table 6.6. shows the best results of laser annealing of complete CSPC device structures. The laser power used for annealing was optimized to 18 W.

Table 6.6. Results of laser annealing of complete CSPC device structures using TiO_x as ETL and MoO_x as HTL. The laser annealing was done at 18 W after Al_2O_3 ALD. The FGA was done after TiO_x and MoO_x depositions for 10 and 5 minutes, respectively.

Sample	After Native oxide and 1.05 nm Al_2O_3 deposition		After laser anneal		After 4.5 nm TiO_x and FGA at 200 ºC		After 8 nm MoO_x and FGA at 180 ºC	
	τ (µs)	iV_{OC} (mV)	τ (µs)	iV_{OC} (mV)	τ (µs)	iV_{OC} (mV)	τ (µs)	iV_{OC} (mV)
1	153	580	206	611	254	622	282	627
2	161	584	188	606	266	624	267	625

It was observed that the laser annealing was helpful in the partial improvement of the iV_{OC} and the passivation quality at the interface. The laser annealing helped significantly increment iV_{OC} by 20-30 mV. Given the ultrathin thickness of native oxide and Al_2O_3 and their respective absorbance spectra, it can be safely assumed that these layers were practically transparent to the laser wavelength of 450 nm and all the laser light was absorbed by the Si substrate [209][210]. The CW mode of laser annealing modified the atomic arrangements at the interfaces of the Si substrate while eliminating interfacial defects and improving the overall passivation. Ideally, a deep UV laser in CW mode will be helpful in directly annealing these ultrathin native oxides and Al_2O_3 layers.

It is essential to calculate the temperature induced by the CW laser so that the laser processing parameters can be optimized to replicate the thermal annealing conditions. Far deviation from these annealing conditions will fail laser annealing. Beyer *et al*. provided the theoretical model to calculate the maximum dynamic temperature rise (ΔT_M^d) during the CW laser annealing of thin films and substrates [34]. The equation is as follows:

$$\Delta T_M^d = \frac{P^*/\kappa 2\pi^{0.5}\, r_0}{1 + z^2 r_0\, v/8D_S}$$

where P^* is the laser power, κ is the heat conductivity, r_0 is the radius of the laser spot, v is the laser scan velocity, D_S is the heat diffusivity, and z is the heat diffusion length in multiples of r_0. In the

case of c-Si, κ is 1.42-1.56 W(cm.°K)$^{-1}$, D_S is ~0.8 cm^2/s, and z = 1 as the heat diffusion length had been assumed to be contained in laser spot radius [211][212]. The other parameters were r_0 = 0.005 cm (since the spot size was ~100 μm), and the scan velocity was 0.3 cm/s. The incident laser power was 18 W. The maximum dynamic temperature rise was calculated to be 651-715 °K (or 378-442 °C) for κ ranging from 1.42-1.56 W(cm.°K)$^{-1}$, close to the FGA conditions.

The other FGA processes after each deposition of TiO_x and MoO_x layers were done, and the best result achieved was around 627 mV, similar to the results achieved without laser annealing shown in Table 6.5. This showed the efficacy and potentiality of using laser annealing instead of thermal annealing to get satisfactory performances.

F. Comparison with SiO_x as the passivation layer

The effects of replacing ALD Al_2O_3 with SiO_x layer as the passivation/tunneling interlayer on the passivation quality and iV_{OC} have been investigated. Two test device samples were considered for this experiment. The 1.5 nm SiO_x was grown on each HF-treated Si substrate using 70% wt. electronics grade HNO_3 at 100 °C for 15 minutes. One of the test samples was treated with optimized 450 nm CW laser annealing with ~18 W power, and the other test sample was treated with tube furnace anneal at 875 °C in N_2 for 30 minutes, similar to the TOPCon fabrication. There was no ALD Al_2O_3 since the cumulative interlayer thickness would defeat the purpose of tunneling. The rest of the fabrication steps, like the ALD of TiO_x and the thermal evaporation of MoO_x and FGA, were kept the same. The results have been tabulated in Table 6.7.

Table 6.7. Results of laser annealing of complete CSPC device structures using TiO_x as ETL and MoO_x as HTL. The laser annealing was done at 18 W after growing SiO_x. The FGA was done after TiO_x and MoO_x depositions for 10 and 5 minutes, respectively.

Sample	After 1.5 nm SiO_x growth in HNO_3		Annealing condition	After annealing		After 4.5 nm TiO_x and FGA at 200 ºC		After 8 nm MoO_x and FGA at 180 ºC	
	τ (μs)	iV_{OC} (mV)		τ (μs)	iV_{OC} (mV)	τ (μs)	iV_{OC} (mV)	τ (μs)	iV_{OC} (mV)
1	167	583	Laser	166	593	234	623	250	624
2	155	579	Furnace	175	597	211	620	261	626

It was observed that the laser annealing improved iV_{OC} by ~10 mV, but this improvement was smaller compared to the laser annealing of Al_2O_3. This is possibly due to the more significant influence of the negative fixed charge in Al_2O_3 on the overall passivation quality compared to SiO_x [213]. On the other hand, the furnace annealing resulted in a comparatively better improvement in iV_{OC} by 18 mV, as such thermal treatment is common in TOPCon fabrication. Ultimately, the overall iV_{OC} value saturates at an average value of 625 mV.

It is to be noted that the performances of all our test devices saturated within a maximum iV_{OC} value of 629 mV. This may be attributed to the lack of further optimization in the thickness, precursor materials, deposition recipes, and architecture novelty for TiO_x and MoO_x, which can be a future research subject. Moreover, the lower quality and functional characteristics of the thermally evaporated MoO_x compared to ALD might also contribute to this saturation of iV_{OC}. Additionally, the cleaning process of the Si substrate wafer at the beginning can also affect the outcome.

G. Comparison of iV_{OC} performances between test devices and literature

The comparisons in Table 6.8., have been made to present an overview between our preliminary results from our test devices and some literature review. All the listed iV_{OC} are recorded post-deposition annealing.

Table 6.8. Comparison of iV_{OC} performances between our test samples and some of the iV_{OC} values reported in the literature.

Case	Name of the fabrication step	iV_{OC} of our test samples	iV_{OC} extracted from literature	Comments on literature	Ref.
1	After ALD Al_2O_3 + Anneal	583 mV	~650 mV	Only 2 nm ALD Al_2O_3	[214]
			640-645 mV	Thickness > 2 nm and no tunneling	[202]
2	After ALD TiO_x on Al_2O_3 + Anneal	625-629 mV	698 mV	High iV_{OC} without Al_2O_3; Rear side passivated by Al_2O_3/ SiN_x/ metal	[95]
3	After PVD MoO_x on Al_2O_3 + Anneal	629 mV	676-685 mV	Symmetric SiO_x/Al_2O_3/ MoO_x; ALD is better than PVD.	[105], [207]

It can be observed that in case 1, there is a lag in our test samples by ~70 mV in iV_{OC}, which suggests that the Al_2O_3 deposition is critical and demands more scientific involvement in understanding the c-Si and Al_2O_3 interfacial properties and optimizing deposition recipes. Moreover, the investigation of tunneling is as crucial as passivation quality. In cases 2 and 3, the performances of our test devices saturated at iV_{OC} of 629 mV and lagged by 50-70 mV compared to some of the reported values in the literature. This shows a need for further optimization in TiOx and MoOx stack combination with Al_2O_3. Moreover, cleaning wafers should play a big role in overall performance since it will significantly affect the interfacial defect density.

6.3. Conclusion

The fabrication of transition metal oxides (TMO) based carrier selective passivated contacts (CSPC) Si solar cells have been investigated by optimization at every step based on the passivation

quality, minority carrier lifetime measurements, and the calculation of iV_{OC}. The presence of the native oxides on the Si substrates, without HF treatment, provided the best starting passivation quality. Thermal ALD of 1.05 nm Al_2O_3 at 200 ºC provided additional hydrogen and in-situ heating on the native oxide-coated Si substrates. The cumulative thickness of the native oxide and Al_2O_3 was kept within the tunneling regime of < 2 nm. After FGA, the resultant iV_{OC} reached ~580 mV. Using low-temperature plasma ALD at 170 ºC, optimized 4.5 nm of TiO_x was deposited as ETL, and after FGA treatment, the average resultant iV_{OC} was 629 mV. Similar optimization experiments were carried out for the PVD of MoO_x as HTL for a completely fabricated CSPC device. After FGA at 180 ºC, the best result of iV_{OC} of 627 mV was achieved. In our test samples, TiO_x and MoO_x did not improve iV_{OC} significantly, though the carrier selectivity was allowed. Hence, the improvement of Al_2O_3 deposition becomes the critical step. The feasibility of laser annealing of the Al_2O_3 /SiO_x stack structure was investigated, and the iV_{OC} was ~30 mV higher than the FGA results. The optimized CW 405 nm laser annealing with 18 W power, a spot size of ~100 µm, a scan velocity of 3 mm/s, and 50% overlap were used. After laser annealing, the iV_{OC} improved and reached 611 mV, whereas after FGA, the iV_{OC} saturated at ~580 mV. Using theoretical calculations, it was shown that the laser annealing produced an annealing temperature similar to FGA. Further optimization in the thickness, precursor materials, deposition recipes, and architecture novelty for Al_2O_3, TiO_x, and MoO_x could further improve the iV_{OC}, tunneling, and overall passivation quality.

CHAPTER 7: Conclusion and Future Work

A. Conclusion

This thesis investigates the fast laser processing and RTA for the device fabrication of low-cost, high-efficiency c-Si solar cells like IBC-HJ and carrier-selective (p-TOPCon and TMO-based) solar cells. The implications of the laser-material interactions and the rapidity of the RTA processing have been investigated and optimized with the help of diverse material, chemical, optical, and electrical characterization techniques. These scientific methods helped build a comprehensive understanding of the passivation quality, minority carrier lifetime, dopant activation, crystallinity, surface morphology changes, chemical constitution modifications at the c-Si, and different thin film interfaces in solar cell devices.

In the case of IBC-HJ c-Si solar cells, the effects of nanosecond (ns) pulsed lasers of wavelength 532 nm and 355 nm were investigated and optimized for selective laser ablation and material removal for the interdigitated back contact device fabrication. A laser fluence of 0.254 J/cm^2 was sufficient to effectively ablate the top sacrificial a-Si:H layer, achieving carrier lifetime and iV_{OC} as high as ~2 ms and 719 mV, respectively. This showed the feasibility of ns-pulsed laser processing for selective and localized material removal without causing laser heat-induced crystallization and damage to the underneath heterojunction passivation layer. Higher laser fluences resulted in the accumulation and egression of hydrogen gas under immense localized pressure, which caused ruptures in the SiN_x layer with concentric rings after completely removing the top sacrificial a-Si:H layer. Additionally, unwanted poly-crystallization of the a-Si:H (n and i) layer and irreversible degradation to the passivation quality occurred. The chemical constitutions changed due to the laser heat, which led to an N-Si-O complex formation at the center of the

Gaussian laser ablation spots. All these findings were supported by the characterization results from μ-PL, SEM, FIB-SEM, line-mapping EDS, Raman, and X-ray spectroscopy. Using the optical constants calculated from ellipsometry and Essential MacLeod simulation to model color charts, an innovative approach was also made to characterize the laser-induced effects on multi-thin film layer structures. The optimization of selective ns-pulsed laser ablation in an IBC architecture was shown without compromising the laser heat-induced damages to the passivation quality of a heterojunction. This method not only cut down the complexity of lithography and the required masking in the IBC structures but also increased fabrication throughput of such devices. Compared with white-light microscopy, the potentiality of using Essential MacLeod color chart modeling was established as a stand-alone independent technique to accurately characterize laser ablation depths in multi-thin film layer structures.

In the case of carrier selective boron-doped poly-Si-based p-TOPCon c-Si solar cells, the effects of RTA temperature and atmosphere on the passivation quality, iV_{OC}, crystallinity, dopant activation, and oxidation state at the SiO_x/c-Si interface and the addition of SiN_x coating were investigated. Also, a separate scientific investigation was conducted on the effects of high-intensity lamp light exposure at high temperatures on p-TOPCon device structures. The high-intensity RTA lamp light-induced passivation degradation was prevented by using a thicker Si wafer cover. The RTA conducted in the air resulted in fewer blisters, thicker oxide formation at the expense of the poly-Si layer, and higher passivation quality. The application of SiNx coating improved the iV_{OC} to 706 mV and acted as an additional hydrogenation source for higher passivation quality. Higher LPCVD temperature at 588 ℃ produced higher poly-Si crystallinity, dopant activation, and less hydrogen content to minimize blisters. Optimal RTA temperature and time improved dopant activations and lowered sheet resistance. The longer RTA cooling time was the most significant

factor that influenced the p-TOPCon device performances. Shorter heating, holding, and cooling time should be avoided to prevent irreversible passivation quality damage. The unique aspect of the presence of poly-Si layer and boron activation after RTA was the positive contribution towards field passivation and increment in peak PL intensity. Over-diffusion of boron was expected to cause more Auger recombination and reduced passivation quality. An innovative approach was the use of pulsed cycles of RTA processing, and it was found that the dopant activation was achieved to lower the sheet resistance. These scientific findings have a broader impact on the fabrication of p-TOPCon and n-TOPCon devices using thermal annealing and fast laser annealing methods. The fundamentals of the RTA affecting the dopant behavior and device-structures were understood and will help us in the overall process development and optimization. Thus, the PV community will be able to improve the lagging performances of the boron-doped p-TOPCon devices and compete with the dominating phosphorus-doped n-TOPCon devices in the market.

Lastly, the preliminary investigation and optimization of ultrathin ALD, thermal evaporated TMOs, and laser annealing were accomplished, and the fabrication of complete bifacial CSPC Si solar cells was demonstrated. The passivation quality, minority carrier lifetime, and iV_{OC} at every fabrication step were determined for the optimization. The presence of the native oxide and the thermal ALD of Al_2O_3, with a cumulative thickness < 2 nm, was beneficial for high passivation quality and tunneling of charge carriers. FGA was helpful in hydrogenation and annealing externally, which improved the passivation quality and iV_{OC}. Due to its lower thermal threshold and propensity towards crystallization and changes in stoichiometry, MoO_x deposition should be done after the FGA of the TiO_x layer. The feasibility of laser annealing methodology and the potential replacement of thermal annealing of the Al_2O_3 layer was demonstrated and compared to furnace thermal annealing, supported by theoretical calculations. The CW laser

annealing was accomplished using optimized 18 W power, a spot size of ~100 μm, scan velocity of 3 mm/s, and 50% overlap. The laser annealing improved the iV_{OC}, reaching 611 mV, compared to thermal annealing, where iV_{OC} saturated at ~580 mV. Although the devices with an Al_2O_3 passivation layer started with a higher iV_{OC} performance than those using SiO_x, the final iV_{OC} reached ~630 mV. This proved that mechanisms undergoing at the interfaces of c-Si, native oxide, and Al_2O_3 are critical and demand more investigative attention. The research work has a broader impact on the identification of the technical factors influencing the passivation quality, tunneling, and deposition conditions of the dopant-free CSPC Si devices. This will help to improve the iV_{OC} performances of such devices beyond 720 mV, without compromising the tunneling properties. Moreover, the significance of controlled CW laser annealing will help in overcoming the interfacial defects and compete with other carrier-selective devices like TOPCon in terms of device performances and throughput in the PV market.

The summary of all the major accomplishments and novelty of results is provided in Table 7.1.

Table 7.1. Summary of the accomplishments and novelty of results in this thesis work.

Si solar cells structures	**Fabrication Problems**	**Solution to the problems**	**Novel approach and results**
(1) IBC-HJ	♦ Requires complex lithography process. ♦ fs- & ps-pulsed laser-induced damages; iV_{OC} loss = $\underline{-40\ mV}$ [47].	♦ Use of pulsed laser patterning, and selective removal of a-Si:H (i) and (p) layers. ♦ Use of ns-pulse width laser.	♦ Optical thin-film interference simulation to control laser fluence, allowing minimization of laser-induced damage. ♦ Achieved insignificant laser-induced damages: iV_{OC} loss $\underline{\leq -3\ mV}$, resulting in high iV_{OC} ~719 mV.

(2) p-TOPCon	♦ Use of long duration of furnace annealing (875 ºC/ 30min) to achieve high iV_{OC} (~688 mV) and dopant activation. ♦ Lack of flexibility. ♦ High thermal budget	♦ Use of RTA with flexibility in the choice of annealing atmosphere; controlling heating, holding and cooling times; and temperature.	♦ RTA at optimal 825 ºC/ 7-15 min was achieved. ♦ Lower thermal budget accomplished. ♦ Air RTA+FGA (iV_{OC} ~656 mV), with fewer blisters and thicker surface oxide, is better than N_2 RTA+FGA (iV_{OC} ~630 mV). ♦ N_2 RTA of SiN_x-coated devices resulted in the highest iV_{OC} ~706 mV. ♦ Light-induced degradation was avoided by using Si wafer cover. ♦ Dopant activation and lower sheet resistance were achieved. ♦ Slower cooling time (≥ 300s) was found critical for the best performance.
(3) TMO-based CSPC	♦ Use of long duration of furnace annealing (425 ºC/ 30min). ♦ Lack of flexibility. ♦ High thermal budget	♦ Use of CW laser annealing to improve the c-Si/nat.ox. /Al_2O_3 interfacial quality.	♦ The interfacial quality of c-Si/nat.ox. /Al_2O_3 was improved and iV_{OC} was increased by 2.6% using CW 450 nm laser annealing at 18 W, compared to furnace anneal. ♦ Lower thermal budget achieved. ♦ Presence of native oxide, and use of Thermal ALD Al_2O_3 and Plasma ALD

			TiO_x were good as deposition conditions. ♦ Best performance was iV_{OC} ~629 mV.

B. Future Work

In the case of IBC-HJ Si solar cells, we have demonstrated using nanosecond pulsed laser processing for selective ablation without damaging the passivation layer. This accomplishment opens new possibilities for investigating ultrafast picosecond and femtosecond lasers for selective ablations without laser-induced heat on HJ solar cells using similar characterization techniques, including Essential Macleod thin-film modeling. Such simulation modeling can also be used for laser isolation to avoid plasma leakage problems [215]. A laser beam of the top-hat profile will be a good start for a future endeavor of uniform ablation as it will avoid the difficulty of laser spots with a Gaussian profile. The extension of fast laser processing from 1-inch to 6-inch devices within an optimized timescale can also be a future area of interest.

In the case of carrier-selective p-TOPCon Si solar cells, we demonstrated the implications of variable heating, holding, and cooling cycles, anneal atmospheres, lamp light-induced degradations, hydrogen content in poly-Si depositions, blistering, and presence of SiN_x:H coatings under RTA. Future work can be extended to investigating CW and microsecond pulsed laser annealing in small vacuum chambers. Study of interface study based on the energy band bending by EELS, cathodoluminescence, atomic bonding by STEM, and dopant profile by SIMS can be a starting point for a detailed study. The application of selective laser annealing can be optimized for a future research endeavor in solar cell architectures using both IBC and TOPCon. Later,

extending fast laser processing from 1-inch to 6-inch devices within an optimized timescale can also be a future area of interest.

In the case of carrier-selective TMO-based CSPC Si solar cells, we conducted a preliminary study on the deposition and optimization of SiO_x, Al_2O_3, TiO_x, and MoO_x and demonstrated complete bifacial CSPC Si devices, supported by FGA and CW laser annealing. The future areas of interest can be improving the c-Si/native oxide/ Al_2O_3 interfacial defects and deposition optimizations to balance the need for good passivation quality and tunneling. TiO_x and MoO_x 's carrier selectivity can be considered an independent optimization work that can be pursued based on various material and electrical characterization. Investigation of the CW deep-UV laser processing will benefit the PV community in fabricating dopant-free CSPC devices at high throughput and low expenditure. Lastly, converting bifacial to IBC architectures using masked-ALD of ETL and HTL and metallization can be an innovative topic of interest for future research.

Appendix A: Additional work on laser processing and solar cells.

A1. Microscale patterning of semiconductor c-Si by selective laser-heating induced KOH etching

In this chapter, we present a novel approach for achieving highly localized micron-resolution patterning using a microsecond (μs) pulsed laser, a technique based on the laser heating-induced chemical etching (LHICE) process that preserves carrier lifetime. The core principle of this methodology involves elevating the temperature in specific areas irradiated by the laser, thereby enhancing the forward reaction rate of temperature-dependent chemical etching on crystalline silicon (c-Si). By carefully selecting laser processing parameters, we successfully patterned c-Si without the need for direct laser ablation. This temperature range was chosen to be both low and safe for the fabrication of silicon solar cells, effectively minimizing direct laser-induced defects and thermal stresses in the c-Si lattice.

Following the microsecond pulse-width laser-heated KOH etch patterning of c-Si, we conducted a comprehensive analysis of its impact on minority carrier lifetime (MCL). Our characterizations involved various analytical techniques, including optical microscopy, scanning electron microscopy (SEM), Sinton QSSPCD MCL measurement, white-light Zygo optical profilometry, and LCPSim simulation, to gain a comprehensive understanding of the laser-assisted chemical etching process.

This cost-effective, low-temperature patterning method holds promise for diverse applications in solar cell designs, encompassing both inorganic and organic materials. Its availability for high-efficiency solar cell fabrication is expected to significantly benefit the solar

industry. Furthermore, this approach has the potential to extend its applicability to a wide range of other materials, including metals, ceramics, and semiconductors.

A1.1. Experimental

I. Laser processing setup

The experimental setup utilized an IPG Photonics YLR-150/1500-QCW-AC-Y11 laser emitting at a wavelength of 1070 ± 5 nm, operating in quasi-continuous mode. The laser delivered pulse energy of approximately 1.5 J with a maximum peak power of 1500 W, and a constant repetition rate of 500 Hz was maintained. To investigate the impact of duty cycles on Laser Heating-Induced Chemical Etching (LHICE), various laser pulse widths were employed: 100 μs, 150 μs, 200 μs, and 250 μs, resulting in corresponding duty cycles of 5%, 7.5%, 10%, and 12.5%, respectively. The effects of laser scan speeds on LHICE were also examined, with scan speeds set at 10 mm/s, 15 mm/s, and 50 mm/s. Laser power variations were also studied, utilizing average laser powers of 14.1 W, 16.4 W, 18.6 W, and 21 W. The laser spot size remained constant at approximately 430 μm at FWHM (Full Width at Half Maximum), and the total number of scans was kept at 4.

The experiments employed a double-side polished n-doped FZ c-Si <100> type wafer with a thickness of 300 μm and a resistivity ranging from 1 to 5 Ω cm. This c-Si wafer was cut into 1 × 1-inch samples and thoroughly cleaned using methanol and HF solutions to eliminate surface contaminants. A total of nine straight parallel lines, similar to those used in the pattern by Sinha *et al.* [172], were patterned on the wafer. Each line was 13 mm long with gaps of approximately 500 μm in between. The wafer was immersed in a 30 wt% KOH alkaline solution in a polystyrene

petri dish. The KOH solution was maintained at a level of approximately 1 mm above the wafer's surface.

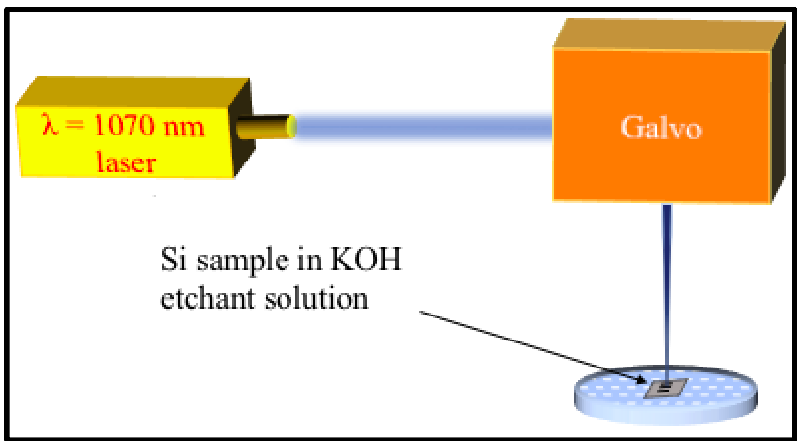


Fig. A1.1. Schematic diagram of the experimental setup for LHICE of silicon.

Fig. A1.1. illustrates the schematic diagram of the experimental setup. Measurements of Minority Carrier Lifetime (MCL) were taken before and after laser processing using a chemical passivation technique involving a 0.08 mol l^{-1} of I_2-methanol solution [216]. The investigation included optical microscopy, Scanning Electron Microscopy (SEM), white-light Zygo optical profilometry, and LCPSim simulation [217]. Optical images were captured using a Hirox 3D Digital Microscope. The MCL was determined using the WCT-120 Silicon Wafer Lifetime Tester by Sinton Instruments. Surface morphology was analyzed using an FEI Quanta 650 Field Emission Scanning Electron Microscope, and depth profiles were obtained using the Zygo NewView 7300 white-light optical profilometer.

A1.2. Results and discussion

I. Influence of laser processing parameters, surfactant, and solution stirring

It is crucial to comprehend how different laser processing parameters, such as laser scan speed, duty cycle, and power, influence surface morphology to optimize laser patterning. Additionally, the impact of using a surfactant and the process of solution stirring were investigated. To characterize the depth profiles of the laser-assisted etched groove lines under these varying conditions, non-destructive white-light Zygo optical profilometry was employed.

I.1. The effect of laser scan speed variation.

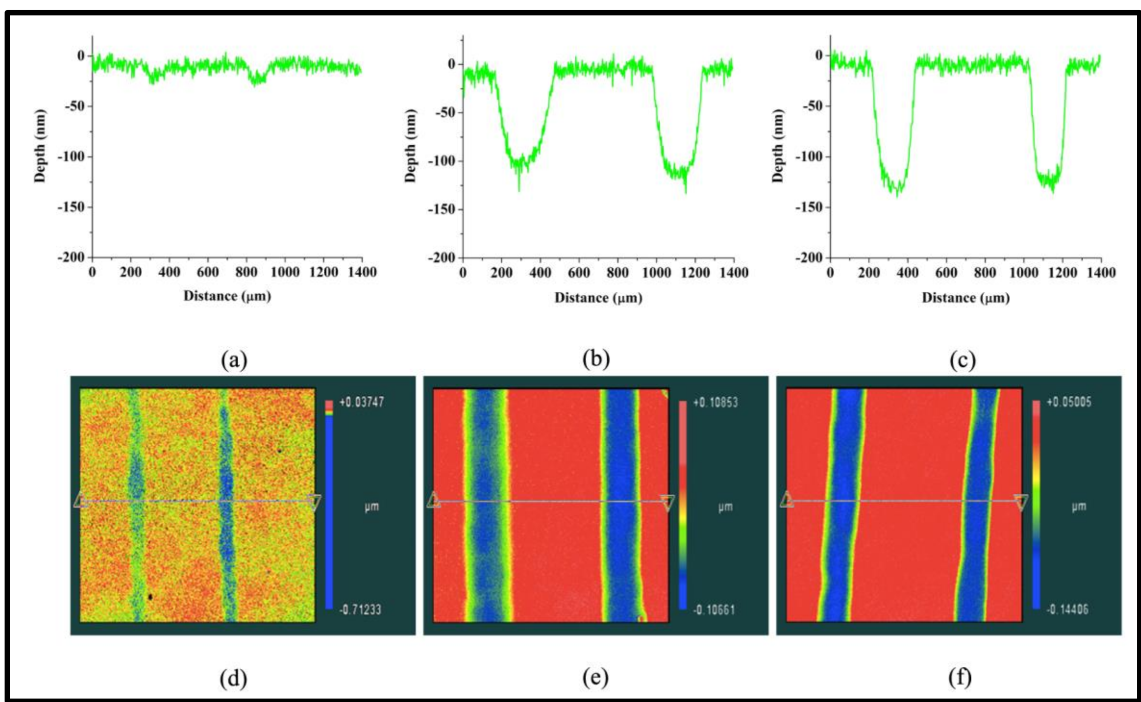


Fig. A1.2. Zygo profilometry showing the surface profile of laser-induced KOH etched lines on the c-Si substrate at scan speed (a) 50 mm s^{-1}, (b) 15 mm s^{-1}, and (c) 10 mm s^{-1}, respectively, while keeping other parameters constant. The figures (d)–(f) show the depth-color mapping images of the lines corresponding to the scan speeds of 50, 15, and 10 mm s^{-1}, respectively.

We investigated the influence of laser scan speed on LHICE. As seen in Fig. A1.2. (a)–(c), when maintaining a constant average power of 18.6 W and a 5% duty cycle, we observed that the etch depth increased from approximately 25 nm to 135 nm as the scan speed decreased from 50 mm/s to 10 mm/s. Lower scan speeds resulted in a higher number of laser pulses, leading to increased heating and, consequently, deeper etching. The depth-color maps clearly illustrate the development of distinct groove features with the reduction in scan speed, as depicted in Fig. A1.2. (d)–(f).

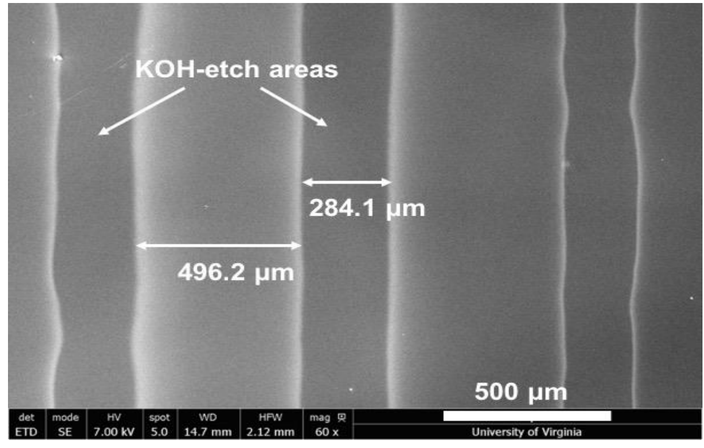


Fig. A1.3. Top-view SEM image of the laser-induced KOH etched lines obtained under the scan speed 15 mm s^{-1}.

However, when the scan speed dropped below 10 mm/s, excessive heating occurred, causing the direct evaporation of KOH and laser-induced ablation of the c-Si. The color map also confirms that the impact remained negligible outside the desired etched region, emphasizing the high spatial localization of the process. It's important to note that laser processing in a liquid etchant medium differs from laser processing in air or vacuum. Literature suggests that the lattice thermal conductivity of c-Si (~5.1 W/(m K)) surpasses that of 30 wt% KOH (~0.727 W/(m K)) and air (~0.02–0.03 W/(m K)) [218]–[220]. Consequently, most laser-induced heat is redistributed within the c-Si lattice, with only a small portion dissipating into the adjacent liquid etchant. This leads to the heating of the liquid surrounding the laser-irradiated c-Si region.

Fig. A1.3. displays a top-view SEM image of a laser-assisted KOH-etched line on the c-Si substrate at a scan speed of 15 mm/s. The etched groove line exhibited an average width of approximately 280 ± 10 µm. The SEM results confirm that the localized laser-induced heat was responsible for forming the KOH-etched groove and not direct laser ablation or stress. The laser power was sufficiently low to prevent the silicon surface from melting. Some minor disturbances and boiling of the etchant liquid near the Si surface did result in slightly irregular groove boundaries. It's worth noting that excessive laser power would lead to silicon melting, substantial bubble formation, vaporization, and uncontrolled etching.

I.2. The effect of laser duty cycle.

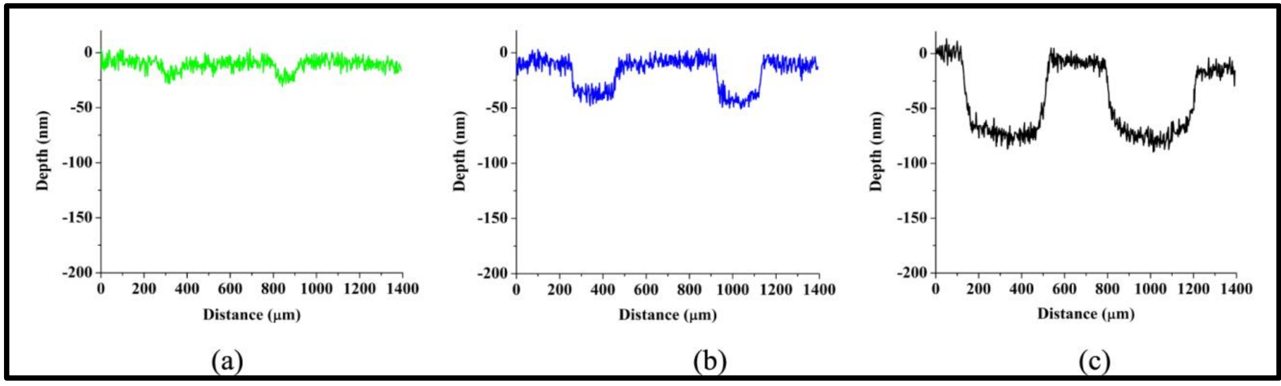


Fig. A1.4. Zygo profilometry showing the surface profile of the KOH-etched groove lines at various laser duty cycles (a) 5%, (b) 7.5%, and (c) 10% while keeping average power (18.6 W) and scan speed (50 mm s^{-1}) constant.

Fig. A1.4. (a)–(c) depict a progressive increase in etch depth, ranging from approximately 25 nm to 80 nm, and an expansion in groove line width, from around 150 µm to 350 µm, as the duty cycle was raised from 5% to 10%. In cases where laser average power and scan speed remained constant, the shorter pulse width led to higher peak energy per pulse, resulting in limited etching despite the elevated temperature induced by the laser. With the increase in the duty cycle,

the pulse width also increased, extending the duration of heating. Consequently, this prolonged heating period allowed more time for the KOH chemical reaction to occur, resulting in deeper etch depths and wider groove lines. Consequently, it becomes evident that the duty cycle plays a significant role in influencing the LHICE process. This observation aligns with the findings from the LCPSim simulation model, discussed in a subsequent section, which underscores the importance of extended heating durations and larger duty cycles.

I.3. The effect of laser power variation.

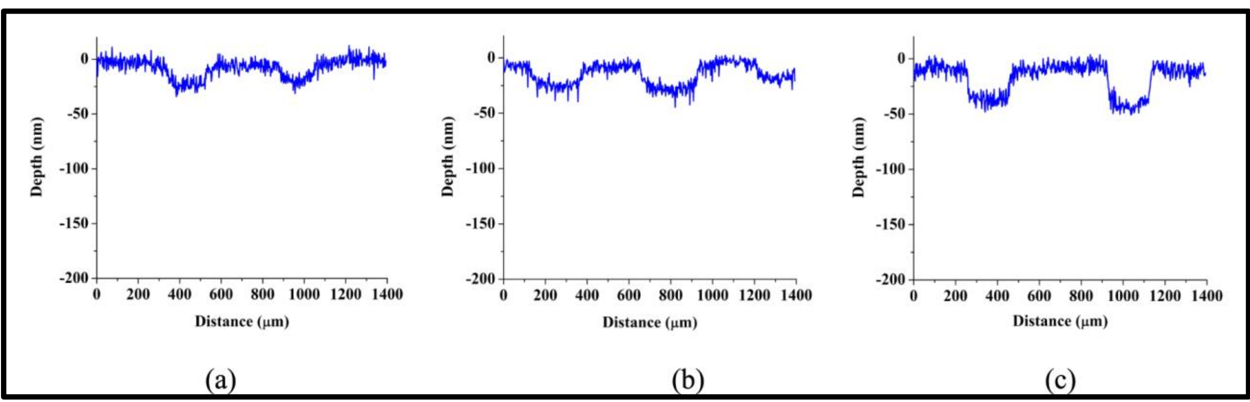


Fig. A1.5. Zygo profilometry showing the surface profile of the KOH-etched groove lines at various average laser powers (a) 14.1 W, (b) 16.4 W, and (c) 18.6 W while keeping other parameters constant (duty cycle = 7.5% and scan speed = 50 mm s^{-1})

The results illustrating the impact of varying the average laser power while maintaining a 7.5% duty cycle and a scan speed of 50 mm/s are presented in Fig. A1.5. (a)–(c). When the average laser power was raised from 14.1 W to 18.6 W, there was a slight increase in etch depth. Although this increase in etch depth was not particularly pronounced, the groove lines did widen. It's worth noting that average power levels below 14.1 W did not result in the formation of any etch grooves, while average power levels exceeding 18.6 W led to the direct laser ablation of silicon, as

illustrated in Fig. A1.6. Consequently, it was concluded that etch depth in LHICE cannot be determined solely by the average power.

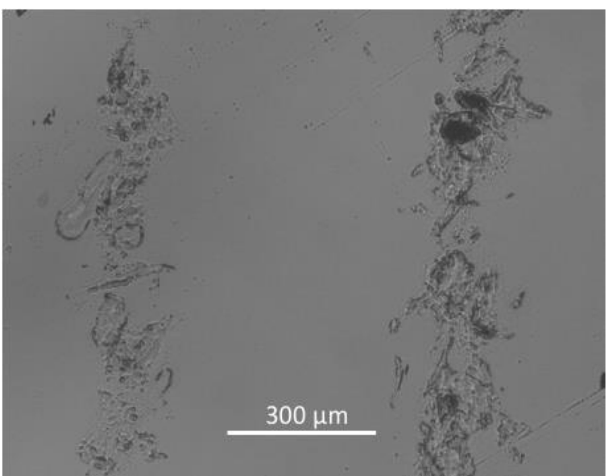


Fig. A!.6. Optical image showing the laser-induced ablation at an average power of 21 W.

I.4. The effect of using surfactant and solution stirring.

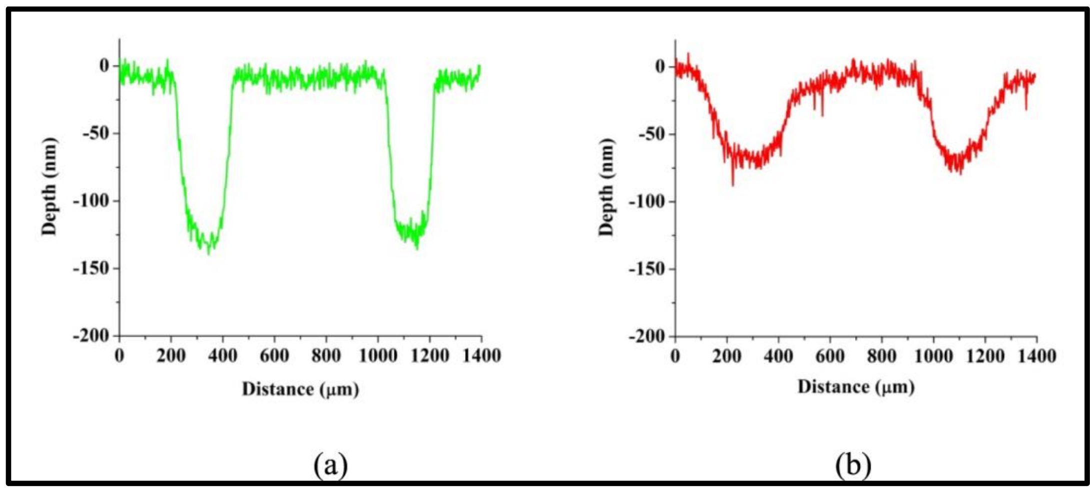


Fig. A1.7. Zygo profilometry showing the surface profile of the KOH-etched groove lines (a) without Triton X-100 and (b) with Triton X-100 while keeping all laser parameters constant (duty cycle = 5% and scan speed = 10 mm s^{-1})

Triton X-100, a common surfactant, is typically employed to enhance surface wetting during the KOH etching of c-Si. This study introduced 100 ppm of Triton X-100 into a 30% KOH solution. Fig. A1.7. (a) & (b) depict the etch depth for samples subjected to KOH solution with

and without the surfactant. When maintaining a constant average power of 18.6 W, a 5% duty cycle, and a scan speed of 10 mm/s, it was observed that the sample etched with Triton-containing KOH exhibited a shallower etch depth (~75 nm) compared to the one etched with KOH alone (~130 nm). It was evident that the etching rate was slower in the case of Triton-added KOH etching, but the average roughness improved from 36 nm to 20 nm. These results align with prior research by Rola *et al.*, which also demonstrated lower etch rates and a smoothening effect resulting from adding Triton to the KOH etchant [221].

Efforts were made to mitigate bubble formation during heating by stirring the solution using a magnetic stirrer rotating at speeds ranging from 50 to 100 rpm. However, this liquid stirring induced undesired turbulence on the liquid surface, leading to irregularities in etch depth due to increased scattering of the laser beam.

I.5. Reproducibility and scalability.

Reproducibility and scalability play pivotal roles in assessing a process's reliability and industrial applicability. Three identical samples were subjected to etching under identical laser parameter conditions in this context. As depicted in Fig. A1.8., it is evident that when employing an average power of 18.6 W, a 5% duty cycle, and a scan speed of 15 mm/s, consistent etch depth (~110 ± 10 nm) and width (~300 ± 20 nm) were achieved. This observation underscores the reproducibility and reliability of the LHICE process.

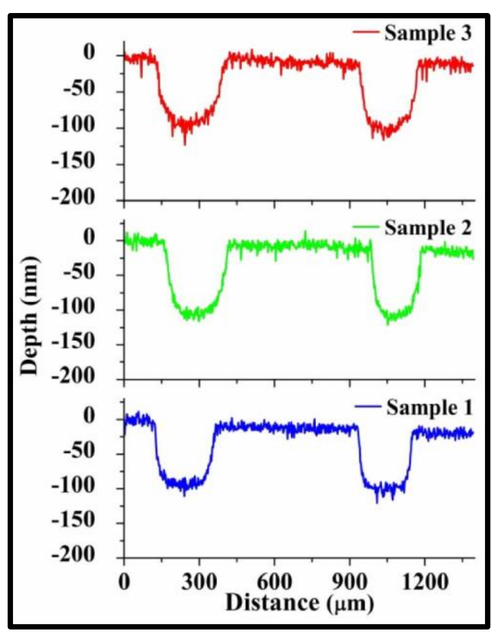


Fig. A1.8. Zygo profilometry shows the reproducibility of the etch depths in three different 1 × 1 inch c-Si samples using the same laser parameters: average power of 18.6 W, 5% duty cycle, and scan speed of 15 mm s^{-1}.

I.6. The effect of laser-assisted chemical etch time.

The concentration of KOH and the temperature influences the etching rate of silicon. Our study maintained the KOH concentration at a constant 30 wt%. It's worth noting that the etching rate initially increases with concentration and then begins to decrease. This suggests that selecting a higher KOH concentration might be advantageous as it can elevate the boiling point of the solution and reduce etching in areas untreated by the laser [222].

The practicality of the LHICE process should meet the criterion of being time-efficient to achieve high throughput in the solar cell industry. In the commercial sector, 6 × 6-inch silicon solar cells hold a dominant position, making it imperative for selective laser-assisted KOH etching of 6 × 6-inch c-Si wafers to be a time-efficient procedure.

The approximate time required to pattern four scans of a single 13 mm straight line, resulting in a ~110 ± 10 nm groove depth, was 1.65 seconds. Consequently, the total time needed

to pattern nine parallel patterns of this nature amounted to 14.85 seconds. The time taken for the complete selective laser-assisted KOH etching of c-Si samples can be enhanced through an optimized combination of factors such as multiple-beam systems, spot size, KOH concentration, average laser power, pulse width, laser wavelength, and the number of laser scans. Thus, to create a single line pattern of 6 inches (i.e., 152.4 mm) on a 6-inch wafer with four scans and achieve a similar groove depth, it would require 18.9 seconds. For each etched line with a depth of ~20 nm, the time would be approximately 4 seconds. The choice of etched depth can be tailored to meet industry requirements. Utilizing a multiple-beam system has the potential to further reduce processing time for large areas. Rather than circular laser beams, one-dimensional line beams can be employed to generate faster and more uniform line patterns. Employing higher-power lasers can extend the length of the focused laser beamline, enabling significantly faster throughput compared to what was used in our experiments.

II. QSSPCD carrier lifetime characterization of semiconductor c-Si

The Quasi-Steady-State Photoconductance Decay (QSSPCD) characterization tool is invaluable for assessing the extent of damages and defects present on both the surface and within the bulk of the c-Si substrate following laser processing. Fig. A1.9. illustrates the QSSPCD MCL (Minority Carrier Lifetime) data compared to carrier density measurements taken before and after the LHICE process. For this analysis, we utilized three separate c-Si substrates, each measuring 1×1 inch, which was previously employed for investigating etch-depth reproducibility, as discussed in the section 'Reproducibility and scalability'. Each measurement was conducted with a minority carrier density of 1×10^{15} cm^{-3}, and an average of three measurements was taken.

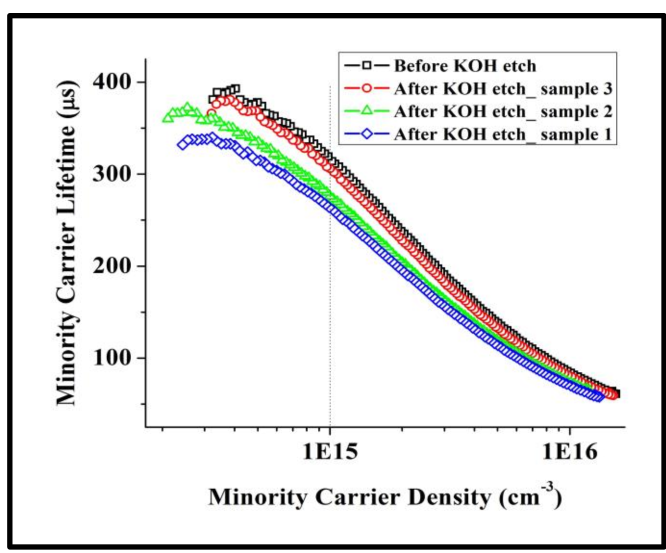


Fig. A1.9. QSSPCD carrier lifetime measurements before and after LHICE for three different 1 × 1 inch c-Si samples showing its reproducibility. The temporary passivation for lifetime measurement was made by the iodine–methanol passivation method.

Table A1.1. QSSPCD measurements to show the reproducibility of the LHICE process on c-Si samples.

Sample	Laser parameters	Before LHICE		After LHICE		Percentage change (%)
		MCL (µs)	iV_{OC} (mV)	MCL (µs)	iV_{OC} (mV)	
The average of all 3 starting samples	-	320	640	-	-	-
Sample 1	18.6 W, 5% D.C. and 15 mm/s.	-	-	265	632	ΔMCL= -17.1 ΔiV_{OC} = -1.25
Sample 2	-do-	-	-	285	635	ΔMCL= -10.9 ΔiV_{OC} = -0.78
Sample3	-do-	-	-	301	639	ΔMCL= -5.93 ΔiV_{OC} = -0.15

The impact of LHICE on c-Si substrates was evaluated based on the MCLs and implied open-circuit voltages (iV_{OC}), both summarized in Table A!.1. In the context of silicon solar cell

manufacturing, the minor decreases observed in MCL (-17.1%) and iV_{OC} (-1.25%) have minimal, if any, profound effects on performance. These negligible reductions in carrier lifetime and iV_{OC} demonstrate our successful execution of localized laser-assisted KOH etching while minimizing the detrimental effects of laser-induced stress and ablation damage on the c-Si substrate. Direct laser ablation would have resulted in a significant reduction in carrier lifetime due to the introduction of defects and damage within the bulk of the material. Wilkes has previously demonstrated that laser processing in an atmospheric environment generally leads to a decrease in carrier lifetime and damages the silicon, although the 1070 nm wavelength is not typically favored for surface micro-patterning on silicon [223].

III. Modelling and simulation for wavelength and power optimizations

III.A. LCPSim simulation.

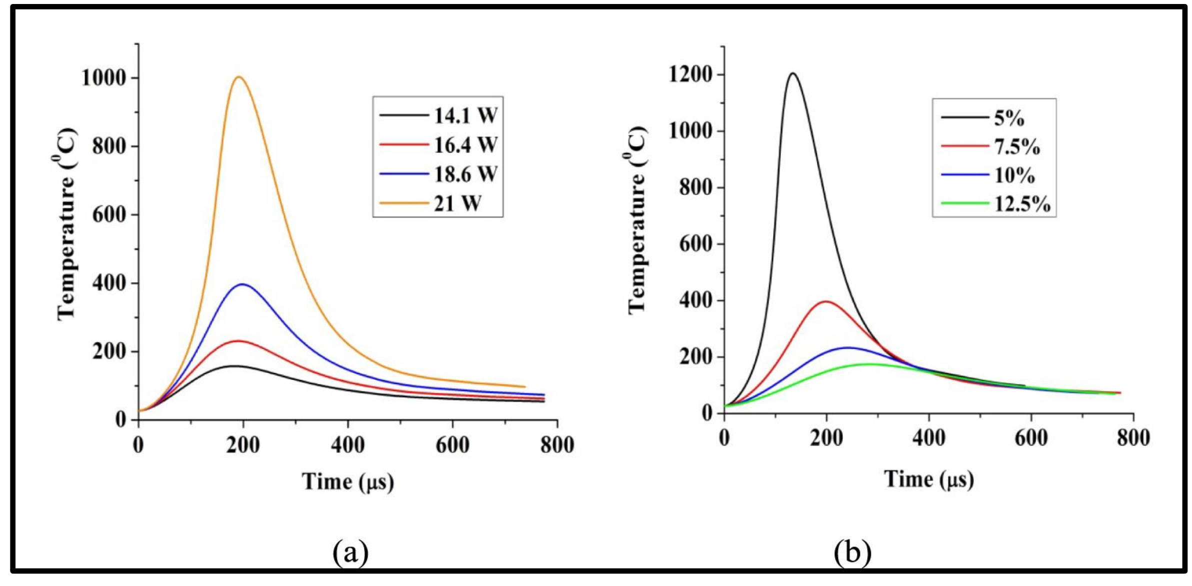


Fig. A1.10. LCPSim simulation results of a single 1064 nm laser pulse showing (a) the maximum temperature profile with respect to time at different average laser powers while other laser parameters are constant and (b) the maximum temperature profile with respect to time at different duty cycles while other laser parameters are constant.

We utilized the Fraunhofer ISE simulation software LCPSim 1.3, developed by Fell *et al.*, to generate simulation results that predict the relationship between laser power and temperature on the surface of c-Si [217]. Due to the limited options for wavelength and medium selection within the simulation program, we opted for a Near-Infrared 1064 nm wavelength laser and considered air as the medium for the simulations while maintaining all other physical and laser parameters constant. The simulation process parameters mirrored those of our experimental conditions. The laser spot size was consistently maintained at approximately 430 µm.

The LCPSim simulations were conducted to illustrate the impact of a single 1064 nm laser pulse on c-Si. Fig. A1.10. (a) illustrates the escalation in simulated peak temperature with an increase in average laser power, ranging from 14.1 W to 21 W. All other laser parameters remained constant, such as the duty cycle (7.5%) and scan speed (50 mm/s). The simulations reveal that peak temperatures fall from approximately 140 °C to 1000 °C. As average power increased, the temperature curves' Full Width at Half Maximum (FWHM) also expanded. A broader FWHM indicates a longer duration of heating. After 800 µs, all the temperature curves reached saturation, registering above approximately 50 °C.

Fig. A1.10. (b) presents the impact of laser duty cycles on LHICE, with all other laser parameters, such as average power and scan speed, held constant at 18.6 W and 50 mm/s, respectively. Two key observations arise from the simulation: (a) lower laser duty cycles result in increased peak temperatures, and (b) higher duty cycles lead to an expansion of the FWHM. In this context, lower duty cycles offer insufficient time for the KOH chemical reaction to generate significant etch depth. Consequently, very shallow grooves are produced, as shown in Fig. A1.4.

(a). Additionally, the narrower FWHM corresponds to a shorter timeframe, further explaining the shallow etch depth observed at lower duty cycles.

It is reasonable to assume that using a liquid medium (KOH/water) resulted in lower peak temperature simulation results due to the higher thermal conductivity of the KOH solution compared to air. Consequently, the simulation outcomes align with our experiments on localized laser-assisted KOH etching of c-Si. The localized temperature was elevated sufficiently to facilitate the KOH etching mechanism while avoiding the direct melting or ablation of the c-Si substrate.

III.B. The effect of laser wavelength.

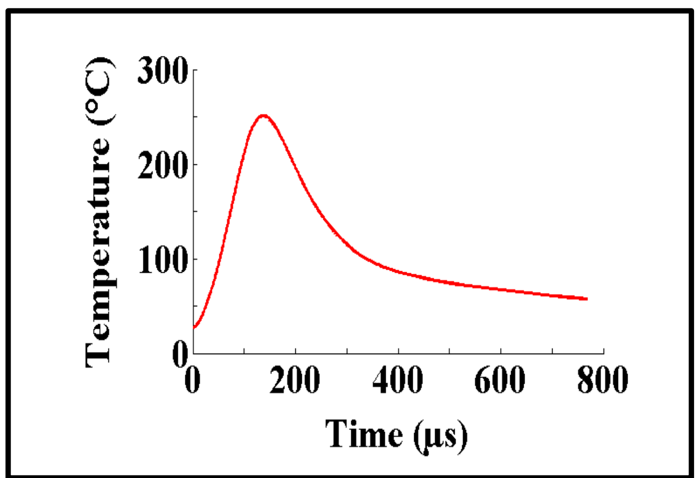


Fig. A1.11. LCP Sim simulation results for a single laser pulse of spot size 25 μm with the wavelength 355 nm, pulse-width of 25 ns, repetition rate of 50 kHz, and average power of 0.05 W.

Near-surface heating is generally preferred when fabricating devices with low defect-density. In the context of laser-assisted chemical etching, near-surface heating ensures that laser energy is primarily absorbed at the interface between the KOH solution and the c-Si surface, where the actual chemical etching occurs. Bulk heating of the device can potentially induce thermal

stress-related defects within the material due to heat accumulation. The depth of laser heating can be controlled by carefully selecting laser fluence, wavelength, spot size, and other related process parameters. According to Beer's law, the choice of laser wavelength determines the depth at which light is absorbed within a particular material. Shorter wavelengths, such as UV wavelengths, are suitable for achieving near-surface heating of c-Si due to their shallow absorption depth. For instance, the absorption depth of UV light with a wavelength of 355 nm in c-Si is approximately 10 nm, whereas for a wavelength of 1070 nm, it extends to about 0.1 cm [224].

Fig. A1.11. illustrates an LCPSim simulation aimed at achieving a maximum temperature of approximately 250 °C with a single laser pulse at a wavelength of 355 nm. The simulation employed laser parameters, including a spot size of 25 µm, a pulse width of 25 ns, a repetition rate of 50 kHz, and an average power of 0.05 W. It took approximately 0.045 µs to reach the peak temperature, followed by a rapid decrease to 50 °C within 0.2 µs. From this, it can be inferred that utilizing nanosecond-pulse-width UV light with a wavelength of 355 nm would be advantageous for LHICE without significant heat diffusion into the bulk of the material. However, shorter heating times may result in shorter chemical etching times and shallower etch depths. One can opt for lasers with higher repetition rates to achieve higher etch rates.

IV. Direct applicability of LHICE process to diverse semiconductor device fabrication

The laser-assisted spatially localized temperature-selective method is applicable for diverse materials, which include semiconductors, dielectrics, metals and alloys, glass, and polymers using different etchants. A few such examples are shown in Table A1.2.

The LHICE process can be applied to etch holes and grooves required for various device fabrication purposes. In the case of Passivated Emitter and Rear Cell (PERC) and Aluminum Back Surface Field (Al-BSF) solar cells, previous attempts involved direct laser drilling of lOCal openings in layers such as Al, AlO_x, SiO_2/SiN_x, and AlO_x/SiN_x stacks, resulting in some laser-induced defects and passivation damages. These local openings can be achieved through selective laser patterning of SiN_x in H_3PO_4, AlO_x, and Al in KOH, as well as SiO_2 in KOH [225]–[227]. Additionally, Wu et al. demonstrated the KOH etching process for bulk micromachining of a 100 mm diameter (100) silicon substrate, SiO_2, and SiN_x passivation layers for the fabrication of high-temperature pressure sensors based on polycrystalline and single-crystalline 3C-SiC piezo resistors [228]. This functionality is also attainable by selectively chemical-etching using laser patterning in KOH and H_3PO_4 solutions. The LHICE process proves useful in fabricating microfluidic devices based on glass and silicon, where channel grooves/holes are typically created using photoresists or a-Si masks [229]. Furthermore, the LHICE process can replace conventional etching methods for soda-lime glass in fabricating high aspect ratio microfluidic channels, as previously demonstrated by Lin *et al.* [230]. Finally, in the production of Micro-Electro-Mechanical Systems (MEMS) devices, the removal of Parylene C layers on silicon and silicon oxide substrates is typically achieved through processes like piranha solution (a 7:3 mixture of H_2SO_4 and H_2O_2) and chloronaphthalene or benzyl benzoate, or wet KOH etching [231], all of which can be implemented using the LHICE process. Consequently, it is evident that this method holds applicability in other fields of thin-film and MEMS device fabrication not discussed here, where flexible localized laser patterning can enable high throughput without introducing defects into the devices.

Furthermore, incorporating fluorescent dyes (both water- and IPA-soluble) into the etchant solution can enhance the absorption of a specific laser wavelength. This approach exclusively heats the KOH solution, accelerating the etching reaction without causing thermal effects on c-Si. Water-soluble dyes such as BBT-mPEG, benzothiopyrylium pentamethine cyanines, and commercial fluorescent dyes like CFTM dyes and LUWSIR4 dyes, known for their diverse wavelength absorption-sensitivities, can be employed in the LHICE process [232]–[235].

Table A1.2. Etching rates of different etchants on various materials at higher operating temperatures.

Materials & description	**Etchant**	**Etch rate at a lower temperature**		**Etch rate at a higher temperature**		**Ref.**
Au	Transene Au-etchant TFA	~ 30 Å/s	20 ºC	~ 150 Å/s	60 ºC	[236]
AlN	Photoresist developer AZ400K.	~ 50 nm/min	40 ºC	~ 600 nm/min;	75 ºC	[237]
Boron-doped c-Si (100)	Ethylene diamine-pyrocatechol-water (EDP)	167 nm/min	66 ºC	~ 500 nm/min	110 ºC	[238]
Monel-400 alloy	$FeCl_3$, $CuCl_2$	6 µm/min	40 ºC	12.5 µm/min	80 ºC	[239]
Polyimide polymer	2 M NaOH + 50 % ethylene diamine	0.1 µm/min	30 ºC	~ 0.9 µm/min	80 ºC	[240]
$Si_{0.8}Ge_{0.2}$	25 % TMAH	5 nm/min	~ 50 ºC	19 nm/min	~ 75 ºC	[241]
SiN_x (Low refractive index)	30-40 wt% KOH	Negligible	25 ºC	0.67 nm/min	80 ºC	[242]
Si_3N_4	BOE	2 nm/min	40 ºC	62 nm/min;	90 ºC	[243]
Si_3N_4	94.5 % H_3PO_4	0.6-3 nm/min	140 ºC	11.5-20 nm/min;	180-200 ºC	[244]–[246]
SiO_2	BOE	0.2 nm/min	40 ºC	0.6 nm/min;	90 ºC	[243]
SiO_2	5 wt% TMAH	100 Å/hr	60 ºC	> 400 Å/hr	76 ºC	[247]

Soda-lime glass	BOE / HCl mixture	1.5 µm/min	5 ºC	~5.5 µm/min	55 ºC	[248]
TiO_2	H_2O_2:NH_4OH:H_2O (1:1:5 by vol.)	0.29 ± 0.09 nm/min	25 ºC	15 ± 1.4 nm/min	65 ºC	[249]

A1.3. Conclusion

A new method of laser patterning using localized laser-heating induced KOH etching of c-Si substrates with minimal impact on electronic properties has been demonstrated. The effect of various processing parameters such as laser scan speed, duty cycle, average power, and other factors like the addition of surfactant, solution stirring, etchant concentration, and etching time was investigated. LCPSim simulations were done to calculate the laser-generated temperature and provided an understanding of the laser-induced heating of KOH.

The etching depth was found to increase as the laser scan speed was reduced from 50 mm s^{-1} to 10 mm s^{-1}. The scan speed, faster than 50 mm s^{-1}, did not induce any observable etching, and slower than 10 mm s^{-1}, introduced direct laser-induced damage to c-Si. The increase in laser pulse width from 100 µs to 200 µs increased etching depth. A longer pulse width provided more laser heating and higher KOH chemical etching reaction times. No noticeable etching was observed at an average laser power of 14.1 W, whereas greater than 18.6 W induced damage to the c-Si. The etching depth was found to increase steadily as the laser power was increased. Both average laser power and pulse width can be optimized for the desired etch depth. The addition of surfactant Triton X-100 slowed down the KOH etch rate, resulting in shallower etch depths compared to the condition without surfactant. The surface roughness was reduced with the presence of the surfactant. The solution stirring proved unreliable in driving away bubbles in the liquid etchant as it impacted the incident laser beam.

The reproducibility and scalability of LHICE were examined using three identical samples and measurement of etching depth and MCL. The QSSPCD lifetime measurement observed an insignificant drop in carrier lifetime (~55 μs) and less than a few percent change in implied open-circuit voltage. Such changes are insignificant for solar cell devices. The optical and SEM images showed smooth etched grooves with no visible damage outside the etched region, which proved the high selectivity and localization. The laser-generated groove boundaries were slightly irregular due to minor turmoil and bubbles in the liquid KOH medium, which could be improved by further optimization of laser parameters. The width of the grooves was found to be approximately ~300 ± 10 μm, and the highest depth was ~130 ± 20 nm using a laser spot diameter of ~430 μm. The throughput of chemical etching can be improved further using an optimized combination of KOH etchant concentration, multiple laser beam systems, 1D line beams, and laser processing parameters. Higher KOH concentration will increase the boiling temperature of the liquid and would have less effect on untreated laser areas on the substrate.

The LCPSim simulation software was used to simulate the maximum temperature reached at the center of the laser beam as a function of time for a single laser pulse of different pulse-width and average powers of 14.1–21 W and a wavelength of 1064 nm. The temperature gradient on the c-Si surface was also determined at different times. The simulated peak temperature and the temperature gradient showed the required temperature range of KOH-etch operation at localized regions without reaching the melting point of c-Si. A smaller laser wavelength, like 355 nm, could be used for more surface-oriented etch.

The demonstrated temperature-dependent localized laser-assisted etching methodology could be equally applicable to various kinds of bulk and thin-film materials like semiconductors, metals, dielectrics, polymers, and glasses, which can find applications in surface-enhanced super-

hydrophobicity, wettability, tribology, bacterial anti-fouling, solar cells, photodetectors, light emitters, and diverse micro-device fabrication.

A2. NASA Terahertz Heterodyne Spectrometer for In-Situ Resource Utilization (THSiRU) Project

NASA has planned future human missions to the moon and techniques to extract water and fuel to sustain future habitats on the harsh lunar terrain. Thus, it has become essential to invent lightweight and compact systems to detect and identify H_2O and hydroxyl group molecules in the lunar rocks and regolith. Such compact systems include heterodyne spectrometers and lasers to enable elemental and molecular detections. This project was accomplished in collaboration with Dr. Berhanu Bulcha, NASA Goddard Space Flight Center and other group members.

Our work was based on investigations on controlled olivine rock samples using FTIR and the destructive Laser-induced Breakdown Spectroscopy (LIBS) method to detect H_2O and -OH molecules. The 1064 nm wavelength pulsed laser was used to perform LIBS. These experiments were conducted in small vacuum chambers where the coatings of materials were deposited on the sapphire window during LIBS after short periods. The feasibility of using the same laser to clean the window was demonstrated by decreasing the laser fluence to clear the window for laser light transmission. This showed the potentiality of using the same laser to conduct LIBS and glass cleaning autonomously.

A3. 2018 NASA Big Idea Challenge Competition

The goal of the 2018 NASA Big Idea Challenge was to demonstrate novel ideas for designing autonomous systems comprising lightweight structures, compact storage, and high-efficiency photovoltaics to ensure sustained electrical power generation during potential human missions to Mars in the 2030s. The major design aspects addressed using advanced ultra-lightweight materials, high-efficiency solar cells, packaging, deployment, retraction, and dust-abatement strategies in the harsh Martian climate conditions and terrain. This was a team effort.

The design name was Photovoltaic Balloon for Autonomous Energy Generation on Mars (MEGA-PB). Our proposed design was based on deploying a giant spherical Kapton-Kevlar balloon, which would be inflated by pumping in from the Martian CO_2 atmosphere. The top of the balloon would house a 1000 m^2 area of high-efficiency GaAs PV solar cells. By heating the CO_2 inside, the balloon would gain altitude and ensure the PV systems are free from Martian dust accumulation. The balloon would be prevented from flying away by grounding it in a storage device filled with Martian sand. The electrical power generated from the solar cells would be transferred to this storage device as a power source.

A detailed report can be found on this link: https://bigidea.nianet.org/wp-content/uploads/2018/03/2018-BIG-Idea-Final-Paper_UVA-1.pdf

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List of peer-reviewed journal publications, conference proceedings and technical reports

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As a first author

1. **A. Sinha**, A. Soman, U. Das, S. Hegedus, and M. C. Gupta, "Nanosecond pulsed laser patterning of interdigitated back contact heterojunction silicon solar cells," *IEEE J. Photovoltaics*, Vol. 10, no. 6, pp. 1648-1656, 2020, DOI: 10.1109/JPHOTOV.2020.3026907
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As a co-author

1. A. Soman, U. Das, N. Ahmed, **A. Sinha**, M. C. Gupta, S. Hegedus, "Process-induced losses by plasma leakage in lithography-free shadow masked interdigitated back contact silicon heterojunction architectures", *J. Mat. Sci. Semicon. Proc.*, Vol. 166, 2023, DOI: 10.1016/j.mssp.2023.107762.
2. A. Soman, U. Das, **A. Sinha**, U. Nsofor, L. Zhang, M. C. Gupta, S. Hegedus "Understanding V_{OC} loss in lithography-free shadow-masked laser ablated interdigitated back contact silicon heterojunction solar cells". Presently under review in the Journal of Solar Energy.

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1. **A. Sinha**, A. Soman, U. Das, S. Hegedus, and M. C. Gupta, "Interdigitated Back Contact (IBC) Heterojunction (HJ) Si Solar Cell Fabrication by Laser Patterning," *2020 47th IEEE Photovoltaic Specialists Conference (PVSC)*, 2020, pp. 0502-0505, doi: 10.1109/PVSC45281.2020.9300857
2. **A. Sinha**, S. Dasgupta, A. Rohatgi, and M. C. Gupta, "Rapid Thermal Annealing (RTA) of Hydrogenated Poly-Si under Air and Nitrogen and Blister Formation," *2022*

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Collection of published works

Nanosecond Pulsed Laser Patterning of Interdigitated Back Contact Heterojunction Silicon Solar Cells

Arpan Sinha, Anishkumar Soman, Ujjwal Das, *Member, IEEE*, Steven Hegedus, *Senior Member, IEEE*, and Mool C. Gupta, *Fellow, IEEE*

***Abstract*—Careful control of the laser patterning for the fabrication of an interdigitated back contact heterojunction (IBC-HJ) solar cell is needed to avoid laser-induced defects and heat-induced crystallization, which can produce higher carrier recombination and lower power conversion efficiency. The results of nanosecond laser patterning of an IBC-HJ test structure are reported, and it was shown that optimized laser ablation conditions using a sacrificial layer eliminates laser-induced damage of the underlying passivation layer. A rigorous set of characterizations, comprising of minority carrier lifetime, spatially resolved μ-photoluminescence, optical microscopy, ellipsometry, Essential Macleod program simulations, scanning electron microscopy, line-mapping energy-dispersive X-ray spectroscopy, X-ray photoelectron spectroscopy, and Raman spectroscopy, were undertaken to provide a deeper understanding of the nanosecond laser processing under a wide range of laser fluence. The evolving changes in surface morphologies of top sacrificial a-Si and SiN_x and the use of color chart simulation for ablation-depth analysis were investigated. The μ-photoluminescence, carrier lifetime, and crystallinity in the passivation layer were evaluated. The trend in the change in the surface chemical constituency was determined in terms of Si/N ratio. Finally, the minimum laser fluence for the IBC-HJ test structure was determined and a negligible change in the implied open-circuit voltage was demonstrated.**

***Index Terms*—Interdigitated back contact (IBC) solar cells, laser patterning, photovoltaics, silicon.**

I. Introduction

THE enhancement in solar power conversion efficiency and lowering of the manufacturing cost will make silicon solar cells more competitive with other renewable energy sources. The two major methodologies—carrier selective contacts [1] and interdigitated back contact-heterojunction (IBC-HJ) architecture—have provided the highest efficiency. The IBC-HJ structure is a back-contact c-Si solar cell architecture with patterned doped hydrogenated amorphous silicon (a-Si:H) layers, thereby forming local heterojunctions at the rear side [2]. Recently, a record 26.1% efficiency polycrystalline on oxide junction IBC (POLO-IBC) solar cell and 26.3% efficiency IBC-HJ c-Si solar cell have been reported [3], [4].

Previously, conventional lithography and shadow masking [5] had been used for the fabrication of IBC-HJ solar cells which increases the total manufacturing cost and added technical complexity [6], [7]. In recent years, the scientific and industrial communities have reported cost-effective direct laser patterning using ultrashort picosecond (ps), femtosecond (fs), and short-pulsed nanosecond (ns) lasers for the fabrication of IBC c-Si solar cells because of its several advantages such as mask-free and contactless patterning, micrometer-level spatial and depth resolution, high flexibility in the pattern design, and high throughput [3], [8]–[11]. Implementation of some of these laser processing steps is envisaged to significantly simplify the fabrication process of IBC-HJ solar cells [12]–[14].

However, recent reports suggest that ultrashort fs-laser processing causes more damage and lowers the V_{oc}, fill factor, and efficiency more than ns laser processing [15], [16]. The processing of HJ structures requires low-temperature processing and annealing [5].

Recently, several investigations have been reported on the varying effects of laser ablation parameters such as the pulse duration and wavelength, but they do not provide an understanding of laser-induced thermal effects on each layer in IBC architecture. For example, in their previous reports, Franklin *et al.* [9], De Vecchi *et al.* [16], Hermann *et al.* [17], and Desrues *et al.* [18] had discussed about the ns laser processing of IBC-HJ solar cells in terms of electrical characterizations only. They do not provide a comprehensive knowledge on the morphological, structural, and chemical compositional aspects behind the effects of ns laser processing on passivation and changes in the IBC-HJ layers. In the paper by Qi *et al.* [19], the effect of ns pulse laser on amorphous silicon has been discussed with no reference to the effect on the passivation layer.

During the laser processing of an IBC-HJ solar cell, unwanted damages and crystallization could be induced, which will significantly lower the carrier lifetime and power conversion efficiency. The laser-induced damage has been found to introduce higher recombination loss in a much wider region than the physical dimension of the laser spot because of lateral carrier transport in IBC-HJ solar cells [20]. Consequently, this leads to a significant loss in iV_{oc} and minority carrier lifetime (MCL). The goal of this article is to selectively achieve patterned n- and p-layers for IBC-HJ cell with minimal laser-induced damage. The laser

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Arpan Sinha and Mool C. Gupta are with the University of Virginia, Charlottesville, VA 22904 USA (e-mail: as2ag@virginia.edu; mgupta@virginia.edu).

Anishkumar Soman, Ujjwal Das, and Steven Hegedus are with the Institute of Energy Conversion, University of Delaware, Newark, DE 19711 USA (e-mail: aksoman@udel.edu; ukdas@udel.edu; ssh@udel.edu).

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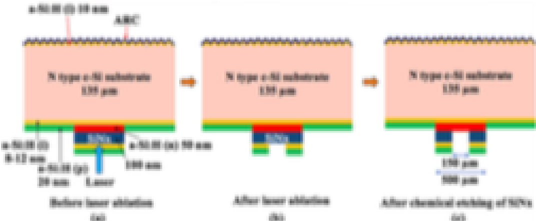

Fig. 1. Schematic diagram of laser processing steps comprising of (a) starting IBC-HJ test device structure before direct laser ablation, (b) after laser ablation of top sacrificial a-Si:H layers, and (c) after chemical etching of underlying SiN_x layer.

ablation of top sacrificial a-Si:H (p and i) layers on top of SiN_x and a-Si:H (n) layers was carried out, exposing the SiN_x layer underneath. The exposed SiN_x layer was later chemically etched away, exposing the a-Si:H (n) layer. This allowed the deposition of metal contacts on the a-Si:H (n) layer. In this article, we describe the results of a thorough investigation and characterization of the impact of ns laser processing parameters on the various layers of an IBC-HJ architecture. Different analytical techniques such as microphotoluminescence (μ-PL), quasi-steady-state photoconductance MCL (QSSPC MCL), optical imaging and ellipsometry, Essential Macleod optical simulations, surface and cross-section morphology by scanning electron microscopy (SEM) and focused ion beam (FIB) SEM, surface elemental and chemical characterizations using energy-dispersive X-ray spectroscopy (EDS), Raman spectroscopy, and high-resolution X-ray photoelectron spectroscopy (HR-XPS) have been used for this study. The simulated color chart based on optical interference was generated to be a reliable independent scientific tool to identify the variation in thickness of individual layers because of laser processing in an IBC-HJ architecture. This research will also be applicable to mc-Si PERC solar cells fabrication where high power ps/ns pulsed lasers are used for making openings in a dielectric layer [21], [22].

II. Experiment Setup

A. Architecture of the IBC-HJ Test Structure

The schematic diagram of the laser processing steps on the rear side of the test structures used in our study to simulate the effects on an IBC-HJ device is shown in Fig. 1. The antireflection coating (ARC), passivation layer of a-Si:H (i), and the texturization at the front side of the devices are not shown in the diagram. In Fig. 1(a), the cross-sectional schematic of the IBC-HJ test structure used for our study is shown. The top a-Si:H (p and i) layers are laser-ablated, exposing the SiN_x layer underneath. The SiN_x layer was then chemically etched to expose the a-Si:H (n) layer underneath. This allows the mask-deposition of metal contacts on the a-Si:H (n) layer. The development of such structure with minimum laser damage is essential to achieve high-efficiency laser-processed IBC-HJ cells [12], [13]. The structures were fabricated on 135 μm n-type Cz Si wafer having <100> orientation and resistivity of 1–8 Ω·cm. Before texturization, the wafers were cleaned using a standard procedure mentioned in our previous work [23]. The pyramidal textures on the front side of the wafer were formed by anisotropic silicon etchant tetra-methyl-ammonium-hydroxide (TMAH). The rear side to be used for the laser processing was prevented from texturization using a silicon nitride encapsulation layer. The wafers had a deposition of a passivating intrinsic amorphous silicon (a-Si:H) layer of 10 nm thickness on the front side and varying thickness of 8–12 nm on the rear side using DC-plasma enhanced chemical vapor deposition (DC-PECVD), the details of which are mentioned elsewhere [24]. Table I shows the different a-Si:H (i) thicknesses used in all the samples. To prevent reflection losses at the front surface, SiN_x (80 nm)/ SiC (20 nm) layers were deposited as the ARC. A 50 nm of n-doped a-Si:H (n layer) and 100 nm of SiN_x layers were deposited in a finger pattern on the semipolished rear side using a Si shadow mask. A thin layer of deposition is observed underneath the shadow mask because of plasma leakage during the PECVD process. This plasma leakage induced deposition of a-Si:H (n) layer was removed selectively by 25% TMAH or 45% KOH (see Table I) and followed by the final deposition step of the blanket layer stack of a-Si:H (i) (10 nm)/a-Si:H (p) (20 nm).

B. Laser

The laser used in the study was a 532 nm wavelength, 10 W average power ytterbium fiber laser (YLP-G-10, IPG Photonics) with 1.3 ns pulse duration, 4.48 μJ pulse energy, 30 kHz repetition rate, and has a Gaussian beam profile. The galvanometer scan head used was a SCANcube 14, SCANLAB, with a scan pattern designed in EZCad (Beijing JCZ Technology Co. Ltd). The laser was used at a 30 kHz repetition rate with a full-width half-maximum (FWHM) spot size of 20 μm at the focal plane at different fluences from 0.427 to 1.27 J/cm^2. The laser fluences have been calculated by directly measuring its energy at different laser powers using Thorlabs energy/power meter and the laser spot size at FWHM. For each laser fluence, the scan pattern consisted of 13 mm of ~150 μm width laser ablation regions, comprising of 0% overlap between laser spots. The schematic diagram of the top view of a laser-patterned sample is shown in Fig. 2. The n-busbar connects all the n-stack layer fingers and the rest of the isolated region acts as the p-stack layer fingers and p-busbar.

C. Characterization

The μ-PL setup consists of a 532 nm 2 W continuous wave (CW) laser (Melles Griot) to be an excitation source with a spot size of ~80 μm, a spectrometer Horiba Jobin Yvon iHR320 operated by SynerJY v3.5 software, an InGaAs detector, and a SR830 DSP lock-in amplifier (Stanford Research Systems). The output power of this excitation laser was optimally reduced to 70 mW by neutral density (ND) filters and quartz glass reflection for μ-PL measurement without affecting the sample device. The MCL and iV_{oc} were measured using WCT-120 Silicon Wafer Lifetime Tester made by Sinton Instruments. The Essential Macleod software from Thin Film Center Inc. was used for simulation and prediction of the color chart of the reflected light

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TABLE I
DATA FOR iV_{OC} AND MCL AFTER LASER PROCESSING AT MINORITY CARRIER DENSITY OF 1×10^{15} cm^{-3}

Sample	Thickness of a-Si:H (i) layer deposited	Type of etchant	Laser Fluence (J/cm^2)	MCL (µs) before laser	iV_{oc} (mV) before laser	MCL (µs) after laser	iV_{oc} (mV) after laser
01	8 nm	KOH	0.254	332	660	302	657
02	8 nm	TMAH	0.254	807	682	786	682
03	10 nm	TMAH	0.254	1141	702	1131	701
04	10 nm	KOH	0.61	997	699	473	680
05	10 nm	TMAH	0.254	1563	707	1255	705
06	12 nm	TMAH	0.254	2190	720	1955	719

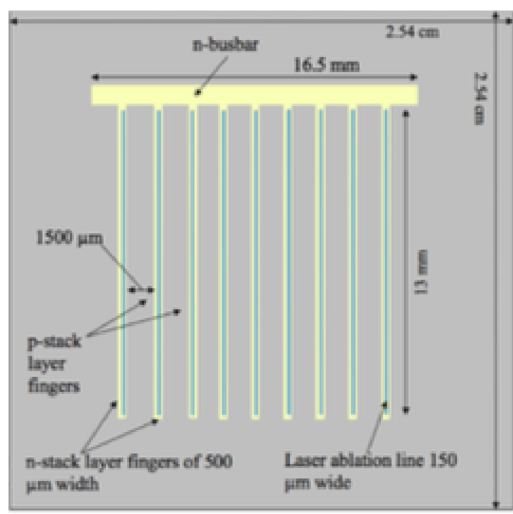

Fig. 2. Schematic diagram of the rear side of the laser patterned samples (top view).

using experimental optical constant data. The SEM/EDS surface morphology and elemental analysis were done using FEI Quanta 650 Field Emission SEM. The cross-sectional morphology characterization was done using Thermo Fisher Scientific Inc. Helios UC G4 Dual Beam FIB-SEM. The Raman spectroscopy was done on Renishaw InVia Confocal Raman Microscope with a 405 nm wavelength laser and spot size of 1.8 μm. All Raman scattering data had been taken to be an average of 15 scans with each of 25 s of acquisition time at a particular location on each laser-ablated spot. The high-resolution (HR) XPS for quantitative surface chemical and elemental composition analysis was done on PHI Versaprobe III Scanning X-ray Photoelectron Spectrometer with a spot size of $\sim$50 μm. The measurement of the optical constants of the device layers was done on J. A. Woollam Company M-2000 Ellipsometer with a focused light beam of $\sim$130 μm spot size at 70° incidence angle.

III. RESULTS AND DISCUSSION

In the IBC-HJ architecture, the a-Si:H (i) acts as a passivation layer for the device. Any laser-induced damages such as defects generation and crystallization during the ns pulsed laser patterning will reduce the MCL and implied open-circuit voltage (iV_{oc}). Different characterizations such as carrier lifetime, optical imaging, surface morphology, and chemical composition provide us both qualitative and quantitative insights to the effects of such laser processing on the various stack layers of IBC-HJ test structure. After the laser processing is done, the ablated top a-Si:H layer exposes the underlying SiN_x, which would be chemically etched selectively using 10% HF solution for 6 min. The front ARC is protected by a dry resist during HF etching, which would be later removed using 1-methyl-2-pyrrolidone (NMP). Now, since the underlying a-Si:H (n) layer is opened up for contact purpose, the interdigitated p and n metal pattern could be made using shadow masking e-beam evaporation of 1 μm thick Al. This is how the test structure could be eventually made into a complete IBC-HJ solar cell.

A. µ-PL and Carrier Lifetime Measurements

The impurities, dangling bonds, atomic vacancies, and defects in unpassivated Si surface generate intermediate e^--h^+ trap levels. Similar defects arise during laser processing, which affect the overall performance of IBC-HJ solar cells. The passivation quality can be characterized by photoconductance carrier lifetime measurement and μ-PL technique. The μ-PL is a reliable tool to measure the degree of passivation at a spatial resolution in micrometers.

In the case of both-side-textured passivated Si substrates, the radiative recombination emits PL at around 1150–1170 nm wavelength [25]. The μ-PL data for different laser fluences are shown in Fig. 3. There is a drop in the PL signal as laser fluence increases from the unablated to 1.27 J/cm^2 condition. For all IBC-HJ solar cell fabrication, laser fluence at 0.254 J/cm^2 was used except for sample# 04 and an insignificant decrease in both iV_{oc} ($\sim$3 mV) and MCL was observed, as shown in Table I, measured at minority carrier density (MCD) of 1×10^{15} cm^{-3}. The sample# 04 was laser processed at a higher laser fluence, 0.61 J/cm^2, and a significant drop of 19 mV in iV_{oc} and $\sim$500 μs in MCL was observed. Although the QSSPC characterization is generally used for reliable lifetime and iV_{oc} measurements for IBC devices, there has been a report suggesting QSSPC artifacts influencing the lifetime results at MCD greater than 1×10^{15} cm^{-3} because of lateral inhomogeneity in the IBC structures [26]. The μ-PL method was successfully used to determine the optimum laser processing condition for IBC-HJ

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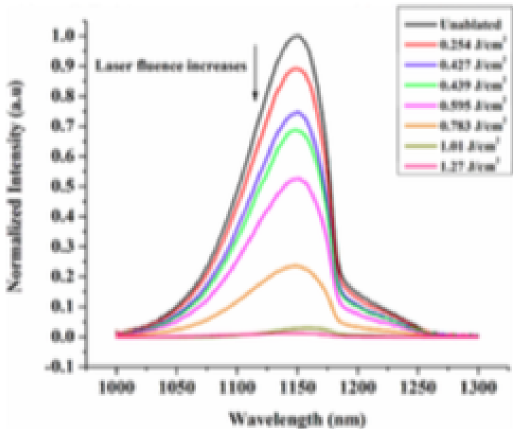

Fig. 3. μ-PL data for different laser fluence ablations. Each of the measurements was an average over 20 scans.

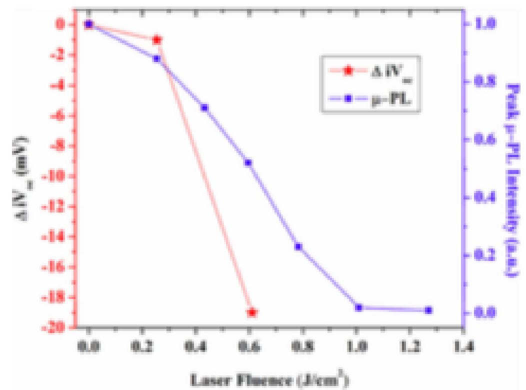

Fig. 4. Peak μ-PL intensity and ΔiV_{OC} versus laser fluence.

solar cell fabrication. Fig. 4 provides a correlation between the μ-PL intensity and ΔiV_{oc} for every increase in laser fluence. As the fluence increases, the peak μ-PL intensity decreases along with the decrease in the iV_{oc}.

B. Optical Characterization

The optical characterizations, such as optical imaging and ellipsometry, provide very useful insights on the changes in absorption depth, reflectance, and transmittance from each layer at a particular wavelength. Thus, it becomes easier to understand the surface features after laser processing. One important aspect of such characterizations is the color identification chart which can serve as a reliable stand-alone tool for determining changes in layer thickness and optical constants under laser processing.

In Fig. 5, we show different surface morphologies and color changes because of different laser fluence processing conditions. The images were obtained using an optical microscope. Prior to optical microscopy, standard white balancing and color default were performed. The formation of fringes in SiN_x layer becomes prominent as the laser fluence increases from 0.254 to 1.27 J/cm^2. In addition, the laser-induced damage at the center of the laser-ablated spots increases with the increase in the fluences.

The material optical constants form the quantitative basis of the design and allows the interpretations of properties of multilayer stack and tandem-structure devices. We can use these optical constants to simulate the reflections from the different stack layers to find the approximate thickness of the laser-ablated and etched layers. The optical constants, refractive index n and extinction coefficient k, were measured using an optical ellipsometer with 5 nm roughness consideration at a 70° incidence angle. The results are shown in Fig. 6. The measured n and k values were fed into Essential Macleod software for simulations of normalized reflectance and color chart. From the simulation, the total thickness of top blanket a-Si:H layers was calculated to be ~26 nm, which is close to the expected thickness of 30 nm for a-Si:H layers deposited by PECVD. The optical reflectance was measured by an optical spectrophotometer. Although both the normalized experimental and simulation curves closely match each other as shown in Fig. 7, the difference in the magnitude of normalized reflectance is because of the semipolished textured surface, while the simulations were made on the assumption of a smooth surface.

The simulation also provides the color chart for a range of incidence angle from 0° to 70° for each layer. The illuminant source is chosen as D65 for average daylight and the observer response as defined in CIE 1931 standard [27]. The International Commission on Illumination (CIE) defines D65 to be a standard white light illuminant source with a correlated color temperature (CCT) of 6504 K. The color-mapping function CIE 1931 is termed as the standard colorimetric observer to represent an average human's chromatic response within 2° arc inside the fovea. In Fig. 8(a)–(c), we show the simulation colors (0°–70° incidence) of IBC-HJ test structure before any laser ablation, after laser-ablation of sacrificial layers which expose SiN_x layer, and underlying c-Si because of the higher laser fluence, respectively. Fig. 8(d)–(f) shows their respective actual optical images. The colors do closely match. The different predicted colors could be compared with the actual optical colors, thus allowing the determination of the changes in the laser-processed layer thicknesses. Hence, the color identification chart can be a reliable tool to know the thickness of a particular layer and its removal.

C. Surface and Cross-Section Morphology

High-resolution SEM imaging allows the characterization of the laser-induced changes in surface topology, morphology, and composition. The optical images and the color chart results in the previous section can be further validated here. The top-view SEM images were taken in a secondary electron (SE) mode at 15 kV beam energy. In Fig. 9, the top-view SEM images show the formation of rings on the SiN_x layer as a function of laser fluence. At fluence greater than 1.01 J/cm^2, the top SiN_x layers rupture and peel off at the laser spot center, which has been

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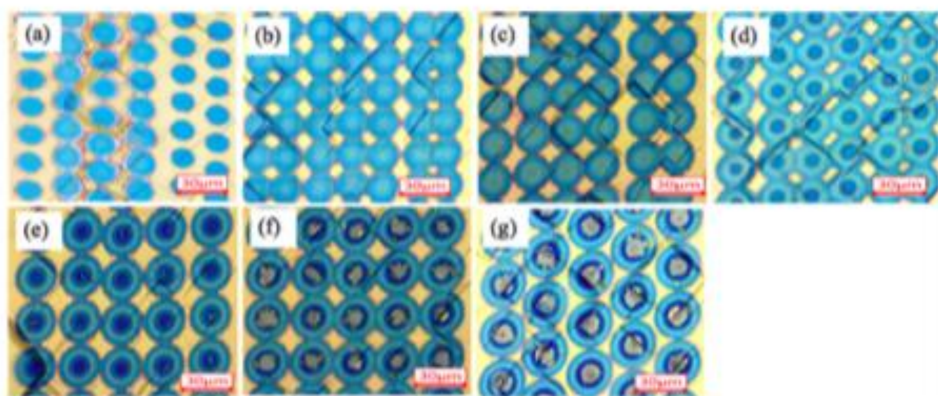

Fig. 5. Optical images of different laser processed regions at different laser fluences (a) 0.254 J/cm^2, (b) 0.427 J/cm^2, (c) 0.439 J/cm^2, (d) 0.595 J/cm^2, (e) 0.783 J/cm^2, (f) 1.01 J/cm^2, and (g) 1.27 J/cm^2. All the pictures were taken with a scale of 30 μm.

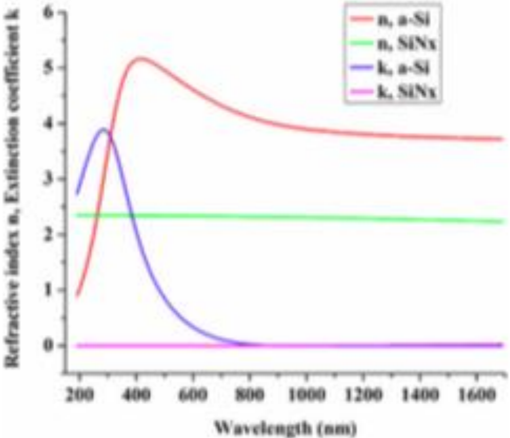

Fig. 6. Optical constants n, k versus wavelength (nm) curve of the IBC-HJ test structure.

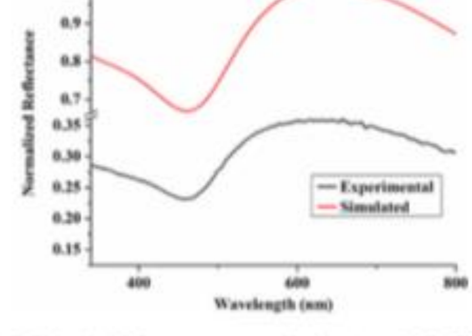

Fig. 7. Normalized reflectance versus wavelength (nm) curve for IBC-HJ test structure.

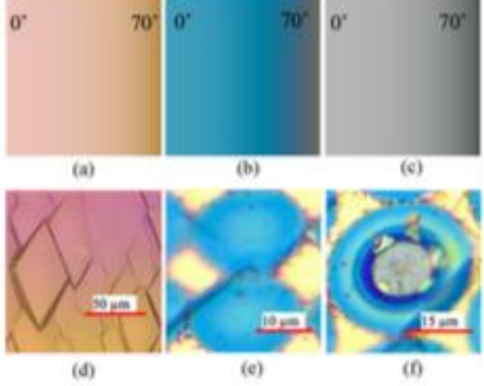

Fig. 8. Simulated colors for test structures (a) before any laser ablation, (b) after laser-ablation of sacrificial layers which expose SiN_x layer, and (c) underlying c-Si exposed due to the higher laser fluence, and (d) to (f) their respective optical images of IBC-HJ test structure.

verified later with our EDS results. Since SiN_x is transparent to 532 nm laser, the laser fluence coincides with the melting threshold of Si [28], [29]. At the center of the laser beam, the underlying a-Si:H (n and i) layers are in the molten liquid state for a long enough time for H_2 gas pressure to build up and escape [30] along with possible a-Si vapor. Because of the laser heat, the surrounding a-Si melts all around the laser spot.

Fig. 9(a) shows a minimum removal of top sacrificial a-Si:H layer at fluence 0.254 J/cm^2. Fig. 9(b) shows a more significant laser removal of a-Si:H thin film at a laser fluence of 0.427 J/cm^2 and less debris are formed. As the laser fluence is increased further, some fringe formation can be observed on the surface as seen in Fig. 9(c) and (d). At higher laser fluence, the top sacrificial a-Si:H layer is ablated away and some of the laser light is absorbed by the n-layer underneath the SiN_x. The SiN_x

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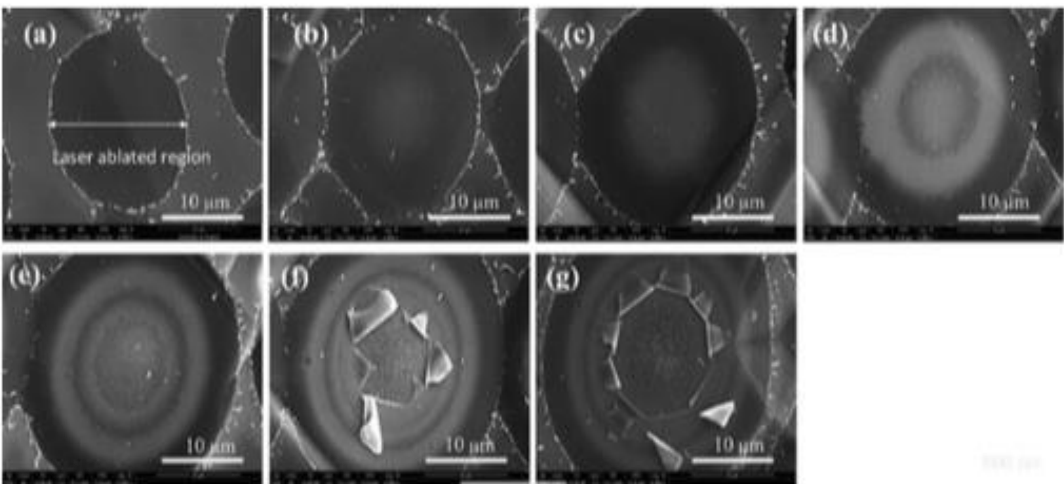

Fig. 9. Top-view SEM images of ablations at different laser fluences of (a) 0.254 J/cm^2, (b) 0.427 J/cm^2, (c) 0.439 J/cm^2, (d) 0.595 J/cm^2, (e) 0.783 J/cm^2, (f) 1.01 J/cm^2, and (g) 1.27 J/cm^2.

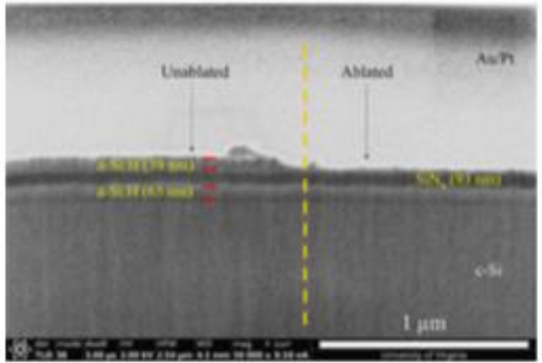

Fig. 10. FIB-SEM image of the cross section at the edge of an ablated spot at the fluence 0.254 J/cm^2.

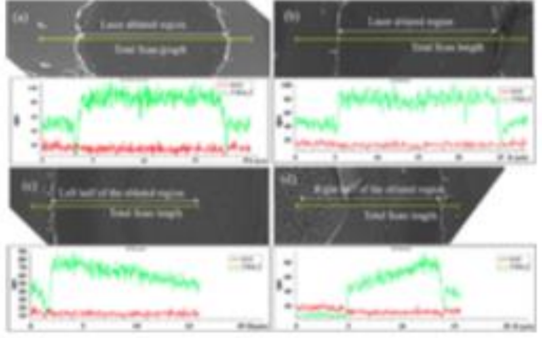

Fig. 11. Line-map EDS spectra for N Kα1 at different laser fluences of (a) 0.254 J/cm^2, (b) 0.427 J/cm^2, (c) 0.595 J/cm^2, and (d) 1.01 J/cm^2. The green spectrum denotes N (Kα) and the red spectrum denotes Si (L1).

layer is essentially transparent to 532 nm wavelength of the laser so that most of the light absorption occurs in the n-layer [31]–[33]. The laser light absorption causes heating, melting, and vaporization of the n-layer along with the release of H_2. The vapor absorbs part of the laser energy and reaches high temperatures. The high temperature causes ionization of the vapor and forms plasma [34], [35]. The rapid laser heating in a localized region and formation of plasma generates a shock wave as it expands. Because of the presence of an overlayer of SiN_x, the generated pressures are much higher than without the overlayer. The generated shock wave gives rise to the observed fringes as the material solidifies after laser heating. As the laser fluence is increased further, the generated plasma pressure becomes higher and the rupture of the SiN_x layer occurs as observed in Fig. 9(f) and (g). This interpretation was further validated by EDS and XPS characterization.

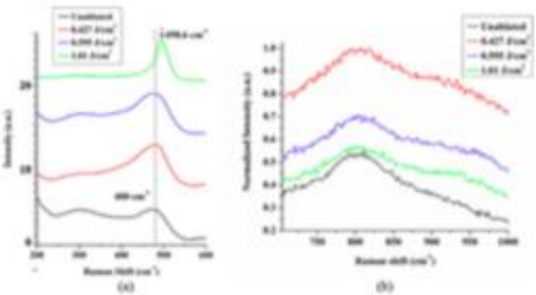

Fig. 12. (a) Raman spectra of underneath a-Si:H passivation layer undergoing amorphous to polycrystalline phase under various laser fluences. (b) Raman spectra of decreasing SiN_x under different laser fluence conditions.

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TABLE II
DATA OF Si:N RATIO AT VARIOUS LASER FLUENCES*

Fluences (J/cm2)	Intensity of Si (2p) (a.u.)	Intensity of N (1s) (a.u.)	Si (2p): N (1s) Ratio
Unablated	37.1 ± 3.96	0.4 ± 0.04	92.8 ± 19.11
0.254	27.2 ± 2.91	2.9 ± 0.31	9.3793 ± 2.00
0.427	22.57 ± 2.41	2.89 ± 0.30	7.8096 ± 1.64
0.595	22.93 ± 2.44	3.62 ± 0.38	6.3342 ± 1.34
1.01	25.6 ± 2.73	2.1 ± 0.22	7.0718 ± 1.49

* The average measurement error across all elements was found to be ~10.7%.

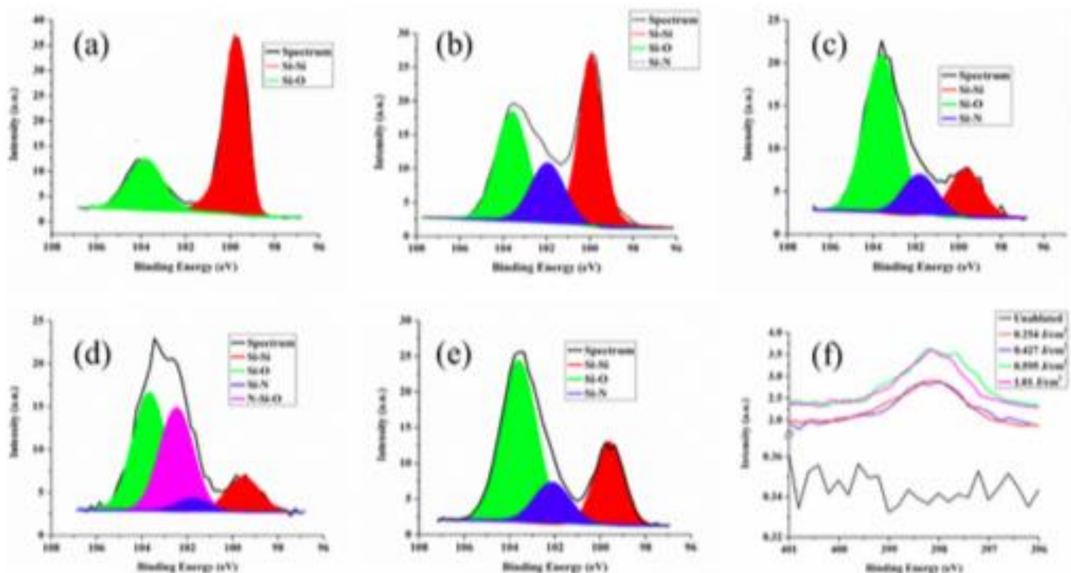

Fig. 13. XPS Si(2p) spectra of (a) unablated, (b) 0.254 J/cm^2, (c) 0.427 J/cm^2, (d) 0.595 J/cm^2, (e) 1.01 J/cm^2 fluences, and (f) N(1s) spectra of all the laser fluences. The average measurement error across all elements was found to be ~10.7%.

The FIB-SEM imaging allows the characterization of the cross-section morphology after removing materials by ion-milling process. The gallium source was used for ion-milling and the device was coated with 10 nm of Au and ~1.5 μm thick layer of Pt prior to imaging. In Fig. 10, the FIB-SEM image shows the cross section of the laser-ablated region at the fluence of 0.254 J/cm^2.

D. Surface Elemental and Chemical Characterization

Note that the line-mapping EDS spectra acquisition was made at 5 kV beam energy so as to only measure the nitrogen element N (Kα1) (denoted by green color spectrum) along the scan length D which corresponds to the existence of SiN$_x$ layer. From Fig. 11(a)–(d), we can see that with the increase in laser fluence, a dip in N-peak at the center of the laser spot was observed, which indicates the decrease in the SiN$_x$ layer thickness. At laser fluences 0.254 and 0.427 J/cm^2, as shown in Fig. 11(a) and (b), the N (Kα1) profiles were quite similar, which indicated the removal of top a-Si:H layer and exposure of the SiN$_x$ layer underneath. In Fig. 11(c) and (d), at a laser fluence of 0.595 and 1.01 J/cm^2, respectively, the line mapping was done for half of the laser spot area. Note the gradual decline in the N peak, which ultimately plummets down at the center. This shows that the exposed SiN$_x$ thickness tapers towards the spot center. This concludes that at fluences greater than 0.427 J/cm^2, a gradient in SiN$_x$ thickness was observed, ultimately leading to rupture.

Using n and k values from Fig. 6, the calculated absorption depth for 405 nm blue wavelength Raman excitation laser in a-Si:H layer ($n = 5.155$; $k = 1.954$) is ~16.49 nm and for SiN$_x$ layer ($n = 2.344$; $k = 0.0003$), it is ~54.9 μm. Hence, ~16% of incident blue light intensity gets transmitted through 30 nm of the top sacrificial a-Si layer and reaches the SiN$_x$ layer. In Fig. 12(a), we show the Raman scattering data of the underlying a-Si:H layer undergoing phase changes from amorphous to polycrystalline form at different laser fluences. Here, we can see

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that there is a broad Raman peak centered at ~480cm^{-1} which signifies the presence of a-Si:H layer according to literature [36]. There is a slight shift of a-Si:H peak with an increase in laser fluence. At 1.01J/cm^2, there is an observable sharp peak at 498.6cm^{-1} approaching toward crystalline Si peak. In Fig. 12(b), we show the decreasing trend of a broad ~800cm^{-1} peak with an increase in laser fluences, which is assigned to the presence of SiN_x [37], [38]. Under the unablation regime, the Raman scattering is because of the light scattering from both top sacrificial a-Si:H layers and underlying SiN_x and merely ~16% of the incident blue light is reaching the a-Si:H/ SiN_x interface. Hence, the broad SiN_x Raman peak at ~800 cm^{-1} has the lowest intensity counts. Under ablation conditions, there is an increase in total intensity counts of SiN_x peak since there is an insignificant amount of a-Si:H layer remaining. With the increase in the laser fluences, a decreasing trend in the peak has been observed. The reason can be attributed to the fact that the quantity of underlying SiN_x gets ablated out, and hence, less Raman scattering occurs. This fact of thinning out of the SiN_x layer has already been validated by EDS spectra.

The HR-XPS measurements were done with 50 μm spot size; therefore, the signal gives an average over two laser spots of 20 μm beam diameter with a ± 0.2eV error. The XPS spectra have C (1s) peak calibrated to 284.8 eV according to ASTM/ NIST [39]. The average measurement error across all the elements, calculated from five different XPS measurements at the unablated region, was found to be ~10.7%. From Table II, we can see the decreasing trend in Si(2p): N(1s) ratio with an increase in laser fluence, indicating an increasing exposure of the SiN_x layer after sacrificial a-Si:H layers' removal. The slight increase in Si(2p): N(1s) ratio at a laser fluence of greater than 1.01 J/cm^2 is seen because of the underlying c-Si getting exposed at the laser spot centers, which account for the sudden increase in Si (2p) count, as discussed earlier in Sections III-A and III-C. In Fig. 13(a)–(e), the presence of a Si (2p) peak at 99.4 eV indicates the presence of Si-Si bond in a-Si:H and c-Si layers. A Si-O peak at 103.5eV indicates SiO_2 formation, as reported by He *et al.* [40]. The Si-N peak at 101.84 eV, as well as, possible N-Si-O complex peak at 102.64 eV under 0.595 J/cm^2 fluence are found to coincide with the literature [41]–[43]. Fig. 13(a) shows the presence of top a-Si:H layer and its natural oxide for unablated condition. Fig. 13(b) shows the presence of Si-N peak, which proves the selective ablation of top a-Si:H layer and exposure of SiN_x. Fig. 13(c) shows peak structure formation similar to Fig. 13(b). Fig. 13(d), at fluence of 0.595 J/cm^2, the new strong N-Si-O peak indicates that the SiN_x layer had been converted into silicon oxy-nitrile (N-Si-O) complex at the ablation spot center because of the laser Gaussian beam profile. Fig. 13(e) shows the disappearance of N-Si-O peak because of the peel-off observed at the laser spot centers. Fig. 13(f) shows the absence of N (1s) peak in unablated sample and N (1s) peak at 397.9cm^{-1} because the N-Si bond shows the presence of the SiN_x layer, as shown in [44]. Hence, the overall XPS study and Raman reveals that the a-Si:H layer can be laser ablated to expose the underlying SiN_x layer using ns laser processing without affecting the passivation.

IV. Conclusion

The ns pulsed laser patterning for the fabrication of IBC-HJ solar cells is demonstrated. The laser fluence required for the removal of the top sacrificial a-Si:H layer was found to be 0.254J/cm^2. At this laser fluence, minimal effect on carrier lifetime and a change of iV_{oc} of only ~5 mV was observed. At these laser fluences, the sacrificial layer of a-Si:H gets ablated, and the SiN_x layer is exposed. With the increase in laser fluence, the removal of the SiN_x layer was observed because of the laser light absorption in the underneath layers and the development of vapor pressure. The underneath a-Si:H (i and n) layers, acting as passivation and dopant layers, convert to the polycrystalline phase as laser fluence is increased beyond 0.595 J/cm^2. At laser fluences greater than 1.01 J/cm^2, direct laser crystallization was observed and resulted in the rupturing of SiN_x layer at the center of the laser spot. The presence of the SiN_x layer because of the laser ablation of the a-Si:H layer was confirmed by line-mapping EDS and Raman measurements. The Raman data also showed the gradual crystallization at the laser spot and decrease of the underlying SiN_x layer with an increase in laser fluence. The XPS measurements showed the growth of SiO_2, SiN_x, a complex N-Si-O at the surface (at 0.595 J/cm^2), and a decrease in the Si/N ratio after laser processing. The optical constants of the layers were measured using ellipsometry and it helped to generate the color charts which can be reliably used to identify the changes in layer properties under different laser processing parameters. Such a method can also be used for multilayer identification in different thin-film devices. The ns pulsed lasers optimized in this work can be successfully used for the fabrication of IBC-HJ solar cells with no significant degradation of iV_{oc} by the proper selection of laser fluence.

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Rapid Thermal Annealing of p-Type Polysilicon Passivated Contacts Silicon Solar Cells

Arpan Sinha, *Graduate Student Member, IEEE*, Sagnik Dasgupta, *Graduate Student Member, IEEE*, Ajeet Rohatgi, *Life Fellow, IEEE*, and Mool C. Gupta, *Fellow, IEEE*

***Abstract*—The carrier selective contacts Si solar cells based on tunnel oxide passivated contact (TOPCon) have provided an efficiency of over 25%, and the large-scale production is planned. One of the crucial steps in TOPCon solar cells fabrication is furnace annealing at around 875 °C. We have investigated the rapid thermal annealing (RTA) for TOPCon solar cells. We discovered that the RTA carried out in air showed much fewer hydrogen-induced blisters than in the N_2 atmosphere. Second, the optical radiation and heat generated in RTA had a significant effect on the degradation of iV_{oc}. The RTA with a SiN_x:H layer on top of polysilicon generated iV_{oc} of 706 mV. The mechanism of degradation under air versus nitrogen atmosphere and the effect of high-intensity light during the annealing process were inferred through various characterizations, such as surface morphology, surface passivation, crystallinity determination, chemical compositional changes, electrical sheet resistances, and oxidation state of ultrathin SiO_x. The TOPCon after air RTA performed better than in nitrogen, optimally at 825 °C. Forming gas annealing further improved the iV_{oc}. Crystallization and sheet resistance were dependent on the annealing temperature and time.**

***Index Terms*—Annealing, blister, polysilicon, rapid thermal annealing (RTA), solar cells, tunnel oxide passivated contact (TOPCon).**

I. Introduction

THE architecture of high-efficiency c-Si-solar cells based on tunnel oxide passivated contact (TOPCon) generally consists of stack layers of heavily doped (B-doped or P-doped) polycrystalline silicon (poly-Si) layer and ultrathin oxide SiO_2 on the doped c-Si substrate. Although the term TOPCon was coined under the assumption of tunneling current as the charge transport mechanism in these selective contacts, several publications show that the dominating current transport mechanism is through the pinholes formed during the annealing process [1], [2]. There are many parameters and constraints in the fabrication steps that influence the intrinsic open-circuit voltage (iV_{oc}) and efficiency of a solar cell.

The recent research laboratory record-breaking efficiencies of p-TOPCon (based on p-type Si wafer) and n-TOPCon (based on n-type Si wafer) solar cells are 26.1% and 25.8%, respectively [3], [4]. The thermal annealing is a very important fabrication step required for achieving polycrystallization dopant activation and minimizing interfacial defects by improved passivation, thus enhancing the iV_{oc} and efficiency of a TOPCon solar cell.

Previously, the traditional tube-furnace annealing was used for thermal annealing of n- and p-TOPCon at high temperatures under inert atmospheres, such as N_2 [5], [6], [7], [8], [9], [10] [11]. The thermal processing with heating durations of tens of minutes is widely used in photovoltaic device fabrication and even in some of the industrial processes for $POCl_3$ diffusion. The firing process of the metallization, which includes heating, dwell, and cooling, is done in tens of seconds. Borden et al. [12] reported a firing process of 30 s for their poly-Si contacts. The blister formation is an important bottleneck in the fabrication of TOPCon architectures as under intense dehydrogenation pressure, the physical rupturing of ultrathin SiO_x and poly-Si layers occurs. This results in the degradations of the passivation quality [6]. Ingenito et al. [13] described even faster processes while addressing the minimization of the blistering formation issue. Recent reports have shown that the rapid thermal annealing (RTA) has been used for annealing purposes in n- and p-TOPCon fabrication [14], [15], [16]. Rapid annealing is focused on time duration from a few seconds to several minutes. RTA has a fundamental advantage of a short period of annealing time as compared with tube-furnace annealing. Yang et al. [15] reported blister formations during RTA of n-TOPCon solar cells. Although earlier studies have been on suppressing blisters, there is a lack of a comprehensive study on blister formation under the RTA and the role of different atmospheres, such as air versus nitrogen, for p-TOPCon structures [13], [17].

In the RTA chamber, the a-Si:H layer in the TOPCon device faces direct exposure to the intense lamp light and heat for the whole period of rapid annealing. In such circumstances, the effect of intense light intensity under heat during RTA needs to be investigated.

Different dielectric capping layers of SiN_x:H and Al_2O_3 and thermal annealing steps have been known to be excellent hydrogenation sources for passivating TOPCon structures using tube furnaces [18], [19], [20], [21], [22]. Moreover, dielectric layers protect TOPCon structures from spiking and damage during

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Arpan Sinha and Mool C. Gupta are with the Department of Electrical and Computer Engineering, University of Virginia, Charlottesville, VA 22904 USA (e-mail: as2ag@virginia.edu; mgupta@virginia.edu).

Sagnik Dasgupta and Ajeet Rohatgi are with the School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332 USA (e-mail: sdasgupta@gatech.edu; ajeet.rohatgi@ece.gatech.edu).

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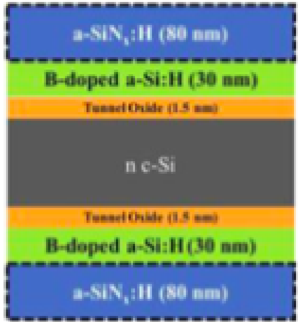

Fig. 1. Schematic diagram of a fabricated TOPCon test structure. The dotted a-SiN_x:H layers are considered when the test structure is TOPCon/SiN_x:H.

screen-printing metallization [23]. Therefore, it is necessary to investigate the utility of using the dielectric SiN_x:H layer.

In this article, we present the results of RTA under air versus N_2 and the effect of high-intensity light under heat on *in situ* B-doped p-TOPCon solar cells. The mechanism of passivation degradation was investigated through various measurements, such as surface morphology, carrier lifetime, crystallinity, chemical compositional changes, electrical sheet resistances, and oxidation state of SiO_x.

II. Experiment

A. Fabrication of the p-TOPCon Test Structure

The p-TOPCon architecture used here is based on the type of poly-Si layer (*in situ* B-doped poly-Si/SiO_x stack) on n-type c-Si wafers. The *in situ* boron doping has several advantages over *ex situ* boron doping, such as simplicity, independent of dopant predeposition process, higher throughput, higher deposition rate of poly-Si layer, higher boron concentration, higher field-induced passivation, and lower optimal annealing temperature [24], [25], [26]. Fig. 1 shows the schematic diagram of the TOPCon test structure and with SiN_x:H layer (dotted). These test structures were fabricated on 200 μm thick n-type monocrystalline Cz-type <100> silicon wafers with a bulk resistivity of 3.2 Ω·cm. Saw damage was removed in 9% wt. KOH at 80 °C for 12 min resulting in a semiplanarized surface. Wafers were cleaned in piranha solution (96% wt. H_2SO_4: H_2O_2: DI :: 1:1:2) and SC-2 (38% wt. HCl: H_2O_2: DI :: 1:1:2) along with oxide removal (5% wt. HF solution) between each step and at the end. The solution temperature was between 50 and 60 °C. Subsequently, an ultrathin (~1.5 nm) layer of SiO_x was grown on both sides of Si in 70% wt. electronics grade HNO_3 at 100 °C for 15 min. *In situ* boron-doped polysilicon was then grown on both sides of the wafer in a Tystar tube low pressure chemical vapor deposition (LPCVD) system at 530 °C for 27 min using precursor gases of silane and diborane resulting in a thickness of approximately 30 nm. A selected sample was annealed in nitrogen at 875 °C for 30 min in a Centrotherm tube furnace to improve crystallinity and activate dopants. Additionally, some samples were coated with 80 nm of SiN_x:H layer on both sides in a Centrotherm plasma enhanced chemical vapor deposition (PECVD) reactor for improved passivation due to hydrogenation.

The samples were cut into a 1 cm × 1 cm area from a single 6-in test wafer before the start of any further processing. The quasi-steady-state photoconductance (QSSPC) measurements were done on 1 in^2 test samples. The QSSPC sensor coil diameter was 4 cm. Three samples were prepared for each thermal annealing test. The maximum film thickness variation over 1 cm length was found to be ±5%. The boron concentration homogeneity was not measured.

Both the RTAs and forming gas anneals (FGAs) were done in the AnnealSys rapid thermal processing (RTP) system under different processing gas environments, such as ultrapure N_2 and forming gas (5% H_2: 95% Ar) from Praxair. In the case of air annealing, the surrounding air was used with no pumping. The humidity recorded in the room was 40%–42%. The temperature regime for breaking Si-H bonds and dehydrogenation is from 300 to 550 °C, and a slower heating rate is beneficial to avoid blister formations [27]. All the RTAs were done using the three-step process, where the first step of annealing started with a 30-min ramp-up from room temperature to 350 °C and dwelling for further 30 min, followed by the second step of a 30-min ramp-up to 500 °C and dwell there for further 30 min. Subsequently, the final step was a 10-min ramp-up to different annealing temperatures, such as 625, 750, 825, and 875 °C, for a 5-min dwell time. The RTAs were done both in N_2 and air atmospheres. The three-step method was adapted from Lee et al.'s article [17], but their study was limited only to the tube-furnace annealing. The reference samples were annealed in the tube furnace at 875 °C for 30 min in N_2 with a ramp-up from 600 °C at the rate of ~10 °C/min. The cooling rate in the RTA was ~300 °C/min as compared with ~3 °C/min in the tube furnace. This fast cooling rate emphasizes the rapidity of our RTA processing. The FGA process consisted of annealing treatment at 425 °C in forming gas for 1 h. To investigate the light-induced damaging effects due to the direct exposure from the tungsten-halogen lamp in the RTA system, a 500 μm thick p-type c-Si wafer cover of 1.05″ × 1.05″ area was placed over the test samples during all the annealing, irrespective of the anneal atmospheres. It was ensured that there was no actual physical contact between the Si wafer cover and the test sample by using small Si spacers. Test samples were annealed with direct exposure to the light using the three-step process of RTA at 875 °C both in N_2 and air in order to investigate the effect of light-induced degradation. The sample with SiN_x:H layer was directly annealed in RTA at 825 °C in N_2, followed by FGA.

B. Characterizations

Except for the QSSPC iV_{oc} measurements, all the characterization studies were accomplished using 1 cm^2 area test samples. The SEM surface morphology was characterized using a 15° stage tilt in FEI Quanta 650 Field Emission Scanning Electron Microscope. The QSSPC iV_{oc} measurements were conducted on (1″ × 1″) area test samples using WCT-120 Silicon Wafer Lifetime Tester made by Sinton Instruments. The iV_{oc} data were generated at 1 Sun condition. The photoluminescence (PL) setup for passivation characterization consisted of a 532 nm wavelength and 2 W continuous-wave laser (Melles Griot) as an excitation source with a spot size of ~1 mm, a spectrometer Horiba Jobin Yvon iHR320 operated by SynerJY v3.5

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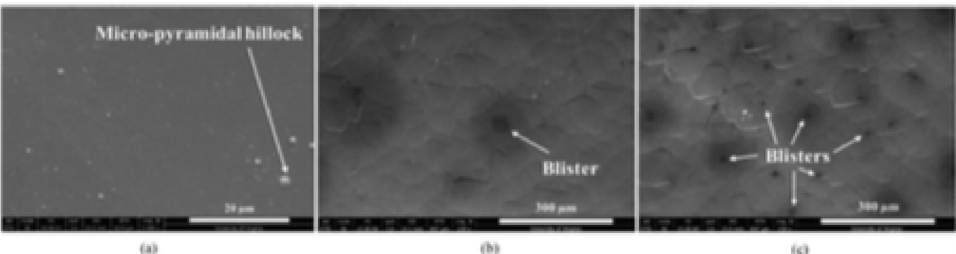

Fig. 2. Top-view SEM images of (a) as-deposited sample, (b) blisters (black areas) after RTA at 875 °C in air, and (c) blisters (black areas) after RTA at 875 °C in N_2.

software, an InGaAs detector, and an SR830 DSP lock-in amplifier (Stanford Research Systems). The excitation laser power was reduced to 70 mW by neutral density filters and quartz glass reflection so that it does not saturate the PL detector, does not heat the test samples significantly, and provides a high S/N ratio. Each PL spectrum reading consisted of an average of ten scans. The absolute PL intensity values are arbitrary but can be used for a relative comparison of the passivation quality. The PL intensity has a peak value at ~1150 nm due to the c-Si bandgap of ~1.1 eV [28]. The μ-PL measurement (with a spot size of ~150 μm) was also done to characterize and differentiate the passivation quality on the blisters and outside-the-blister region. The PL data had an approximate intensity error of ~2.6%. The Raman spectroscopy for crystallinity measurements was done on Renishaw InVia TM Confocal Raman Microscope with a 405 nm excitation wavelength laser and spot size of 1.8 μm. All Raman scattering data had been taken as an average of ten scans with each of 15 s of acquisition time. To calculate the Raman peak "area under the curve," a reference sample was used every time before making measurements on test samples to account for the changes due to optics, mounting effects, crystallinity, etc. The sheet resistances were measured by Jandel four-point probe station for electrical characterization. The Fourier transform infrared (FTIR) spectroscopy was done in Thermo Scientific Nicolet iS50FT-IR for chemical compositional characterization. Each FTIR reading was taken as an average of 256 scans, and the background readings were taken as an average of 200 scans. All these characterizations had an error of ~5%. The X-ray photoelectron spectroscopy (XPS) characterization was done for quantitative surface chemical and elemental composition, depth profiling, and oxidation state determination on PHI Versaprobe III scanning X-ray photoelectron spectrometer with a spot size of ~200 μm and Al monochromatic X-ray source. The pass energy was 280 eV with a 0.5 eV acquisition step. All the XPS spectra for TOPCon structures had C (1s) peak calibrated to 284.8 eV according to ASTM/NIST [29]. The XPS spectra for the TOPCon/SiN_x:H samples had N(1s) peak calibrated to 397.86 eV [30]. The error bar of XPS measurements for oxidation states of SiO_x was approximately 0.2 eV.

III. Results and Discussion

We present the results of the RTA of p-TOPCon with and without SiN_x:H layer under N_2 versus air and the effects of high-intensity light environment.

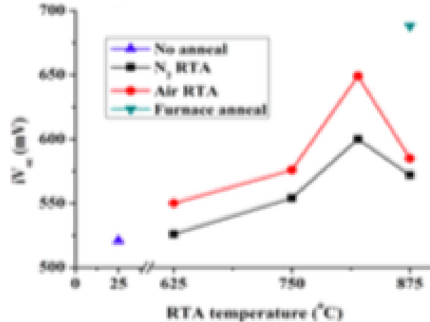

Fig. 3. Graph showing the dependence of iV_{OC} on the RTA temperatures. The data are given for RTA both in N_2 and air atmospheres. The graphs also show the iV_{OC} value for the sample with no annealing and after furnace annealing.

A. Study of the Effects of RTA Atmospheres

1) Surface Morphology: Fig. 2(a) shows the top-view image of as-deposited samples. No blisters were observed except for the octahedral pyramidal features on the surface. The pyramidal structures were caused due to the KOH etching during the semiplanarization process, and they were unaffected by annealing temperatures and time conditions. Schröder et al. [31] have reported the observation and possible mechanism of such pyramidal features during the KOH etching of Si. Fig. 2(b) shows the top-view SEM image of blisters on the air-annealed samples at 875 °C. A higher number density of such similar blisters was observed in the N_2-annealed test samples at 875 °C, as shown in Fig. 2(c). The blisters covered ~1% of the total surface area of air-annealed samples, whereas the blisters covered ~3%–4% of the total surface area of N_2-annealed samples. The morphology of samples annealed in the tube furnace is not shown here as no change was noted.

The high-temperature annealing caused the dissociation of Si-H bonds, which resulted in the release of atomic hydrogen in the poly-Si/SiO_x/c-Si stack. These atomic hydrogens combined to form molecular H_2 under its own immense pressure and consequently escaped while rupturing through the polysilicon layer in the form of blisters [32]. The three-step process of lower temperature annealing minimized the formation of blisters. The furnace-annealed samples showed fewer blisters possibly due to slower heating rates compared with the RTA.

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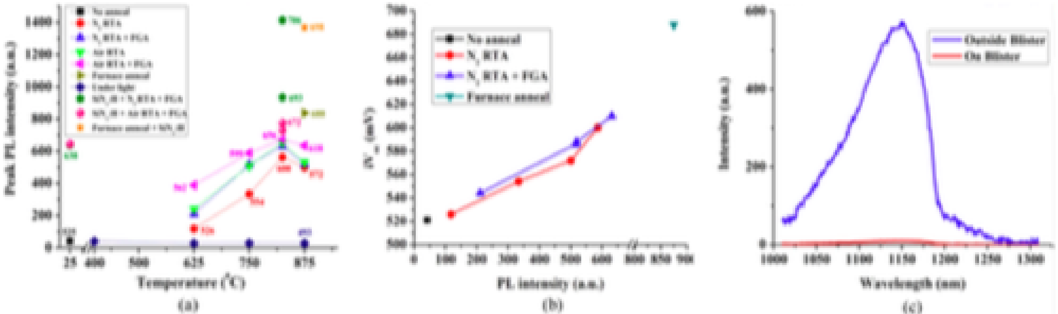

Fig. 4. (a) Qualitative dependence of peak PL intensity on the RTA temperatures for various annealing conditions. The iV_{OC} (in mV) numbers are provided on the graph and (b) dependence of iV_{OC} on the peak PL intensity. The data are given for RTA in N_2 and subsequent FGA only, and (c) PL intensity on and outside blister areas.

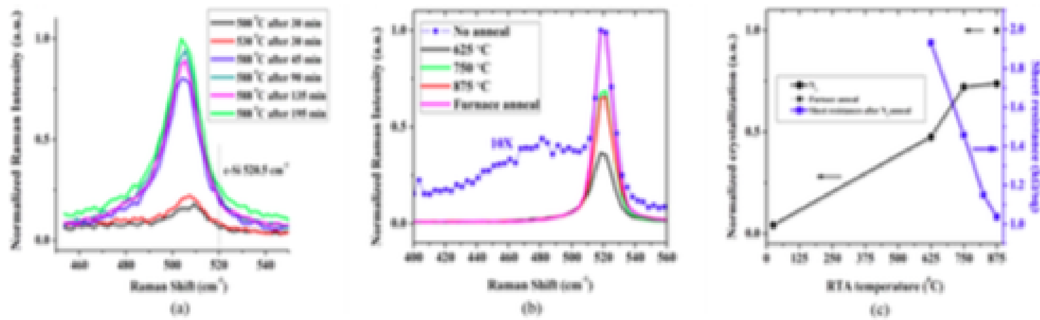

Fig. 5. (a) Raman spectra for the dependence of crystallization of a-Si:H on the anneal time duration while the sample was kept at hot stage at various temperatures. (b) Room temperature Raman spectra for the dependence of crystallization on the RTA temperature, anneal time was 5 min and curves are normalized to furnace anneal. The as-deposited sample curve is magnified ten times due to lower Raman intensity and (c) growth of crystallinity (area under curve) as a function of temperature.

2) Surface Passivation Quality: Fig. 3 shows the variation of iV_{oc} with the RTA temperatures under N_2 and air. The optimal regime of annealing temperature was found to be near 825 °C, and the iV_{OC} started decreasing at temperatures beyond 825 °C. This could be due to the possible degradation to the SiO_2 passivation layer. The iV_{oc} peak value was higher in the air (649 mV) than in N_2 (600 mV). Since the *in situ* B-doped poly-Si layers of these test samples were fabricated by the LPCVD process at a lower temperature of 530 °C, there was a significant starting amount of hydrogen, which increased the chances of blister formations. The RTA sample did not reach the tube-furnace-annealed sample iV_{oc} value of 688 mV, possibly due to the higher density of blisters leading to the passivation degradation.

3) Photoluminescence: Fig. 4(a) shows the variation of peak PL intensity w.r.t. RTA temperatures in the N_2 and air atmosphere and FGAs. It was observed that the annealing temperature of 825 °C provided the highest PL intensity, and FGA improved it further. In N_2-annealed test sample, the highest PL intensity was 563 a.u. and FGA pushed it to 632 a.u. Similarly, in the case of air anneal, the highest PL intensity was 652 a.u. and FGA helped to reach 673 a.u. The furnace-annealed sample had a higher peak PL intensity. This showed that the passivation quality of air-annealed samples was better than that of N_2. Fig. 4(b) shows the observed relationship between iV_{oc} and peak PL intensity. Note when the junction is present, a logarithmic relationship is expected [33]. However, in this case, the PL change occurs due to the oxidation, crystallinity increase, and decrease in defect density. Therefore, it shows a linear relationship.

Fig. 4(c) shows the μ-PL intensity between the blister region and outside the blister region. It was found that the peak PL intensity at the blister region was 9 a.u. as compared with ~570 a.u. outside the blister region of an air-annealed test sample at 825 °C. This showed that the blisters caused extensive passivation degradation in the test samples.

4) Crystallinity Determination: Fig. 5(a) shows the Raman peak intensity of the polycrystalline phase w.r.t. anneal temperature and time duration in the N_2 atmosphere. Choi et al. [6] reported that the deposition temperature of LPCVD poly-Si should be above 580 °C to ensure lower hydrogen content that prevents blister formation. An increase in crystallinity was observed starting at 588 °C, shown by the Raman peak at 508 cm^{-1}, and it increased further as the annealing time was increased. These measurements were carried out in a heated chamber filled

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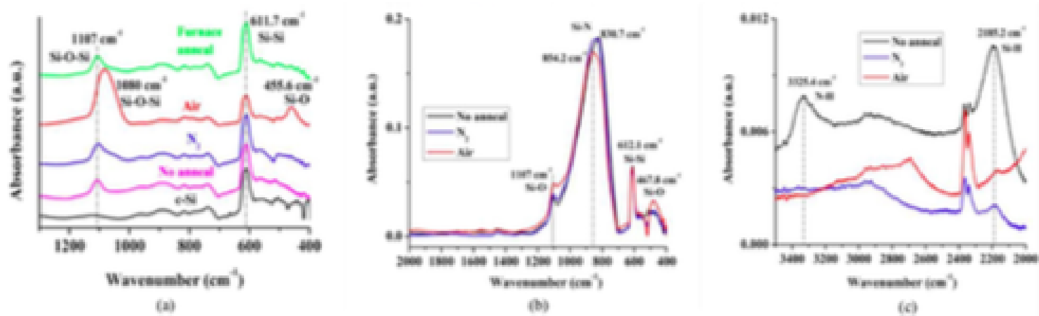

Fig. 6. (a) FTIR spectra for c-Si, TOPCon samples annealed at 825 °C in N_2 and air and results are compared with furnace-annealed sample. (b) FTIR spectra for TOPCon/SiN_x:H samples as deposited and annealed at 825 °C in N_2 and air. (c) FTIR spectra for TOPCon/SiN_x:H samples from 3400 to 2000 cm^{-1} wavenumber region. All the samples were FGA treated before FTIR.

with N_2. The standard room temperature Raman peak of c-Si at 520.5 cm^{-1} is shifted to 508 cm^{-1} due to the measurements done at the high temperature [34]. The as-deposited *in situ* B-doped poly-Si film was a mixture of amorphous and polycrystalline phases. Fig. 5(b) shows the change of a-Si:H peak Raman peak at 480 cm^{-1} toward the crystalline phase at 519.1 cm^{-1} as the RTA temperature increased from 625 to 875 °C in the N_2 atmosphere. Similar phenomena were observed when the test samples were subjected to RTA under an air atmosphere (not shown here). Fig. 5(c) shows the increase of the "area under the curve" of the Raman curve w.r.t. RTA temperatures in the N_2 atmosphere, indicating the increase in crystallinity. The degree of crystallinity in the in situ B-doped TOPCon depends on RTA temperatures and annealing time, not on anneal atmospheres or postanneal FGAs. At room temperature, the Raman peaks for poly-Si and c-Si substrate both occur at 520.5 cm^{-1}. The Raman peak of poly-Si is much broader than that of c-Si due its polycrystalline nature. At the Raman excitation wavelength of 405 nm, the transmission through 30 nm poly-Si is only ~12% based on the optical n and k constants, and therefore, the contribution to the Raman peak from the c-Si substrate was very small.

5) Chemical Composition: Fig. 6(a) shows the FTIR absorbance spectra of c-Si, as-deposited film, TOPCon structure annealed at 825 °C in N_2 and air, and furnace annealed in N_2.

In Fig. 6(a), the absorbance peak at 1107 cm^{-1} generally corresponds to the presence of the vibrational stretching mode of Si-O, indicating the presence of interstitial oxygen and native oxide [35], [36]. The shift of this peak toward the 1080 cm^{-1} peak corresponds to the stretching mode of Si-O-Si and indicates the formation of typical thermal SiO_2 on the surface after air annealing [37], [38]. The peak at 455.6 cm^{-1} for the air-annealed sample corresponds to the rocking-mode vibration of Si-O bonds, which also indicates the formation of SiO_2 [39]. The vibrational state of the Si–Si bond was observed at 611.7 cm^{-1} [40].

The different peak positions indicated that the air annealing converted the top part of the poly-Si layer into the SiO_2 layer. Under the N_2 RTA and furnace annealing, there was no significant SiO_2 formation except native oxide growth.

6) Sheet Resistance: The conversion of the a-Si:H layer to poly-Si will enhance lateral transport of carriers, dopant activation, and passivation. Fig. 5(c) shows the sheet resistances measured at different annealing temperatures in N_2 along with a degree of crystallinity. It was possible to achieve sheet resistances as low as furnace anneal test samples [0.9 kΩ/sq, not shown in Fig. 5(c)]. The sheet resistance of the nonannealed sample was > 1 MΩ/sq. The RTA atmospheres, such as the air, had a negligible effect on the sheet resistance of *in situ* B-doped poly-Si, measured at a constant annealing temperature of 875 °C.

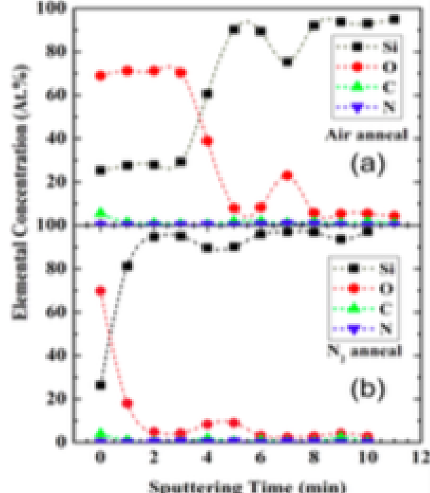

Fig. 7. Depth-profiling XPS spectra showing the atomic percentage profile of (a) air-annealed and (b) N_2-annealed samples based on the atomic concentrations of Si (2p), O (1s), C (1s), and N (1s).

7) Oxidation State and Elemental Composition: The depth-profiling XPS composition spectra of test samples after RTA both in air and N_2 at 825 °C are shown in Fig. 7(a) and (b), respectively. The sputtering rate of SiO_2 is expected to be ~8.9 nm/min, and the Si/SiO_2 sputter rate ratio was ~1.1 [41]. Hence, the exact locations of the surface oxide, poly-Si, and buried ultrathin oxide layers are prone to some error due to the

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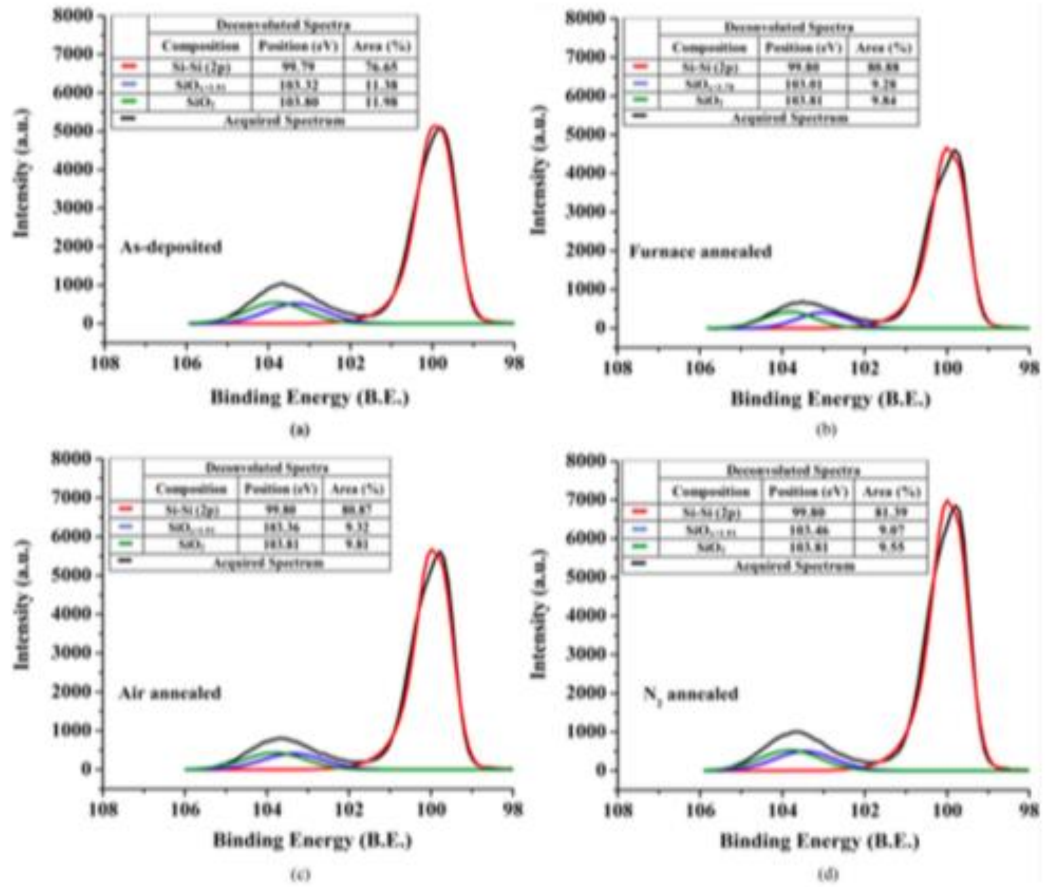

Fig. 8. Surface XPS spectra of ultrathin SiO_2 layer of TOPCon test structures at (a) as-deposited, (b) furnace, (c) air, and (d) N_2 annealing conditions.

undetermined sputter rate through the poly-Si layer. In the case of air annealing, a thicker oxide layer was observed on the top of the remaining poly-Si layer. This proved that the oxygen from air diffused through the surface oxide layer on poly-Si. An increase in oxygen concentration and a decrease in Si concentration under the poly-Si layer is due to the presence of an ultrathin oxide layer. Past the ultrathin oxide/c-Si interface, the Si/O ratio concentration increased. In the case of N_2 annealing, a very thin surface oxide was observed along with the broader peak of Si and oxygen concentrations at the ultrathin oxide region. This shows higher concentration of oxygen present in the ultrathin oxide layer in air-annealed samples. The boron was not able to be detected due to its relatively low concentration. The as-deposited sample had a negligibly thin surface native oxide layer with an intact poly-Si/ ultrathin oxide/c-Si structure (not shown here). This also reiterated our findings from the FTIR study. Fig. 8 shows the XPS spectra of the ultrathin passivating SiO_2 layer after the removal of polysilicon by the chemical etching process for different annealing conditions at 825 °C. XPS spectra show a peak at 99.8 eV due to the Si–Si bond, and another peak at 103.8 eV is due to the presence of the SiO_x layer. The Si-O peak was deconvoluted and showed the two major oxidation states of Si^{3+} and Si^{4+} [42]. The negligible differences in SiO_x/SiO_2 ratios and their respective peak positions suggested that the RTA atmosphere (air or N_2) did not significantly affect the chemical composition of the ultrathin silicon oxide. Only for furnace anneal, there was a visible shift in the Si-O peak. In addition, the area of silicon peak was higher after thermal annealing, indicating the increase in elemental Si [43]. The decrease in SiO_2 concentration was noted, possibly which can come from the incorporation of Si into the oxide layer [44].

B. Effects of High-Intensity Light Environment

Initially, the RTA samples showed poor PL intensity and very low iV_{oc} value. It was discovered that the source of poor performance is related to the exposure of samples to the presence of high-intensity light and heat in RTA for sample heating. We

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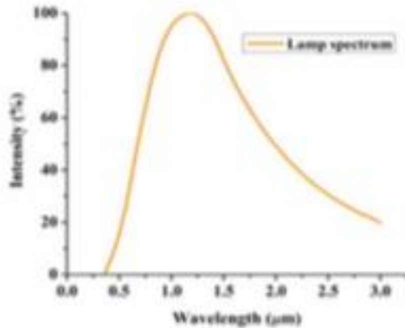

Fig. 9. Spectrum of the RTA lamp used in this study.

TABLE I
EFFECTS OF HIGH INTENSITY RTA LAMPLIGHT ON THE PL INTENSITY AND iV_{OC} OF TOPCON STRUCTURES AT 875 °C

Sample		Before FGA		After FGA	
		PL (a.u.)	iV_{oc} (mV)	PL (a.u.)	iV_{oc} (mV)
As fabricated		41	525	107	537
Without Si wafer cover	N_2	28	491	37	~520
	Air	27	493	45	~520
With Si wafer cover	N_2	501	572	517	588
	Air	519	585	642	618

carried out experiments with samples exposed to RTA intense light along with the samples that were covered with Si wafer cover.

Fig. 9 shows the spectrum of the halogen IR lamp used in the RTA studies. The RTA durations were about 5 min at high temperatures, which was long enough to generate the thermal equilibrium. Approximately, 88.9% of the base 4-in Si wafer received the full spectrum of the RTA lamp radiation, as the test samples only occupied 11.1% of the area. Therefore, the base wafer temperature would be expected to be similar to the one without cover. The Si wafer cover absorbed all of the visible light from the lamp and radiated heat to the test sample. In addition, the temperature readout from the thermocouple touching the base Si wafer indicated the sample temperature.

Fig. 4(a) shows the light-induced degradations of peak PL intensity measured at ~1150 nm without Si wafer cover (denoted by "underlight" legend) for both N_2 and air at different annealing temperatures. The rest of the data were recorded using an Si wafer cover without light exposure. The data from Fig. 4(a) have been summarized and tabulated in Table I. It was observed that under high RTA temperature without the Si wafer cover, there were degradations of iV_{oc}. Later, the post-anneal FGAs recovered from this passivation loss back to the starting passivation quality. It did not improve the iV_{oc} further from the original value. By using the Si wafer cover during RTA and postanneal FGA, it was possible to get higher iV_{oc}. This light-induced degradation occurred irrespective of RTA atmospheres at only high temperatures above 625 °C.

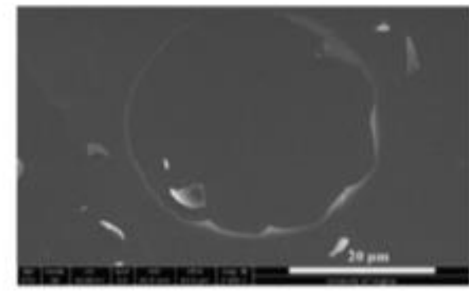

Fig. 10. Top-view SEM image showing a blister formed on the SiN_x:H layer after RTA at 825 °C in N_2.

TABLE II
EFFECTS OF SiN_X:H COATING ON THE PL INTENSITY AND iV_{OC} OF TOPCON STRUCTURES UNDER DIFFERENT RTA ATMOSPHERES AT 825 °C

Sample	Before FGA		After FGA	
	PL (a.u.)	iV_{oc} (mV)	PL (a.u.)	iV_{oc} (mV)
As fabricated	638	622	678	634
RTA in N_2	935	693	1414	706
RTA in Air	730	659	775	672

C. Effect of RTA on SiN_x:H Coated TOPCon Structure

1) Effect on Surface Morphology: An SiN_x:H coated TOPCon sample went through RTA at 825 °C in an N_2 atmosphere. The top-view SEM image in Fig. 10 shows one of the blisters observed on the SiN_x:H layer due to high hydrogen pressure under RTA. The broken SiN_x:H fragments can be observed lying surrounding the blister. The area fraction of blisters was measured as 7%–9% of the total surface area. If the blister formation can be minimized, that would lead to higher iV_{oc} value.

2) Effect on Passivation Quality: Fig. 4(a) shows the peak PL intensity of TOPCon/SiN_x:H test structures annealed by the three-step process at 825 °C under both N_2 and air environments and the subsequent FGAs. All the related data have been summarized and tabulated in Table II. The highest iV_{oc} of 706 mV was achieved after N_2 annealing. For reference, the iV_{oc} of the furnace-annealed p-TOPCon structure reached 688 mV without SiN_x:H and 698 mV with SiN_x:H coating. This displayed the usefulness of using the SiN_x:H layer for passivation purposes. The optical n and k values for as-deposited SiN_x:H film were measured by ellipsometry and were 2.108 and 0.00001, respectively. The SiN_x:H layer would act as an antireflection layer, allowing higher transmission of the excitation laser light and would enhance the PL intensity. However, we are comparing the change in PL intensity between unannealed and annealed samples. The absorption properties of SiN_x:H are assumed to be unchanged after thermal annealing. Therefore, it does not impact

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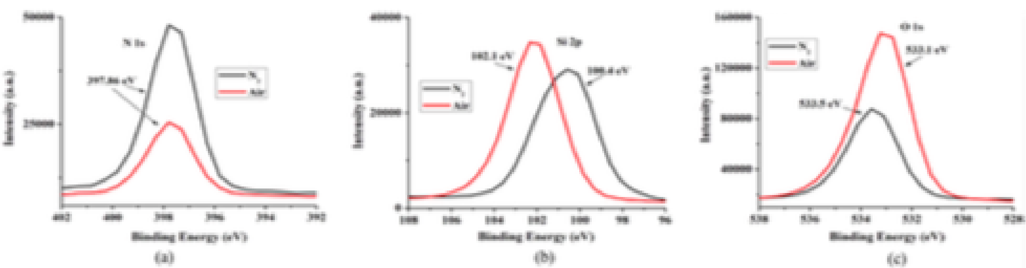

Fig. 11. XPS spectra of (a) N 1s peaks, (b) Si 2p peaks, and (c) O 1s peaks of the TOPCon/SiN_x:H samples after RTA at 825 °C under N_2 and air atmospheres.

the PL measurement, except in the enhancement of absolute PL signal by ∼30% based on the light interference calculations.

3) Effect on SiN_x:H Stoichiometry: Fig. 6(b) and (c) shows the FTIR absorbance spectra of the TOPCon/SiN_x:H structures under N_2 and air annealing at 825 °C and compared with as-deposited film. In Fig. 6(b), it was observed that the wagging mode 1107 cm^{-1} and bending mode 467.8 cm^{-1} peaks of Si-O bond increased after air annealing, which indicated a greater amount of Si-O complexes being formed [45]. The absorbance peak at 612.1 cm^{-1} corresponds to the Si–Si bond. The broad peak centered at 840 cm^{-1} is generally attributed to the presence of the Si-N bond. The spectra from 830.7 to 854.2 cm^{-1} denote the presence of the asymmetric stretching modes of Si-N, which underwent stoichiometric changes likely from Si_3-Si-N to Si_2-(H)Si-N [46]. In Fig. 6(c), it was observed that the presence of the stretching modes of N-H and Si-H peaks at 3325.4 cm^{-1} and 2185.2 cm^{-1}, respectively, in the as-deposited samples showed that they were highly hydrogenated [47]. Later, these peaks disappeared after RTA, which is due to the dehydrogenation.

4) Effect on Chemical Composition of SiN_x:H: Fig. 11 shows the compositional XPS spectra of the TOPCon/SiN_x:H stack annealed at 825 °C both in N_2 and air. In Fig. 11(a), it was observed that there was a comparatively lower count of the N (1s) peak at 397.86 eV in the air-annealed sample than in N_2 annealed. This suggested that there was a decrease in the Si-N bond in the top 3–5 nm thickness of the SiN_x:H layer film after air annealing compared with the N_2 annealing. This is due to the possible Si-O bonds formation on the SiN_x:H surface. In Fig. 11(b), it was observed that there was an Si (2p) peak at 100.4 eV in N_2 annealing and at 102.1 eV in air. The XPS peak at 100.4 eV, observed after N_2 annealing, is attributed to the presence of the Si-Si_3N_1 complex and the peak at 102.1 eV, observed after air annealing, is attributed to the formation of SiO_x complexes [48], [49], [50], [51]. The Si-N peak is expected to be located at 101.7 eV, and the SiO_2 peak to be at 103.5 eV, but peak positions are sensitive to stoichiometry [52]. Finally, after air annealing, the intensity of O (1s) peak at 533.1 eV was higher as compared with N_2 annealing, as shown in Fig. 11(c). This proved that there were more surficial SiO_2 and stoichiometric changes that occurred during the air annealing, as previously showed by Miller and Linton [53] and Lin and Hwu [54].

The results on crystallinity property determination by Raman spectroscopy, chemical changes by FTIR and XPS, and electrical property changes by sheet resistance measurement have been presented. As the annealing temperature increases, the poly-Si crystalline fraction and iV_{oc} increase, implying lower charge-carrier recombination. The FTIR measurements were not sensitive to detect the passivation quality; however, it detects dehydrogenation in SiN_x:H capped samples. The depth-profiling XPS measurements show higher concentration of oxygen in the ultrathin oxide after air annealing, which could lead to higher iV_{oc} compared with that of N_2 for uncapped samples. The surface morphology shows the blister formation affecting the carrier selectivity and, hence, the surface passivation.

IV. Conclusion

In this article, the effect of RTA atmosphere on surface morphology (blister formation), surface passivation, changes in polysilicon crystallinity, composition, sheet resistance, and determination of oxidation state of ultrathin SiO_2 passivation layer in *in situ* B-doped poly-Si-based p-TOPCon was investigated. Second, it was discovered that the high-intensity light exposure during RTA significantly degraded the surface passivation quality and, hence, iV_{oc}. Third, first depositing an SiN_x:H layer on top of polysilicon and carrying out a single step of RTA provide a high iV_{oc} value of 706 mV. In summary, this article shows the following.

1) During annealing, hydrogen-induced blisters must be minimized as confirmed by the PL measurements in which they lead to the loss of surface passivation.
2) A higher iV_{oc} was observed under air RTA compared with nitrogen in SiN_x:H-uncapped samples,
3) UV and visible light radiation during high-temperature RTA induces degradation and its exposure must be avoided during the annealing process.
4) The Si-O bond changes from wagging mode to stretching mode under annealing at 875 °C.
5) The RTA can provide low sheet resistance value of 0.9 kΩ/sq for a 30 nm *in situ* B-doped polysilicon film.
6) Under RTA, the fraction of polycrystalline phase maximizes at around 825 °C.
7) RTA in N_2 of SiN_x:H coated polysilicon film provided the higher iV_{oc} compared with uncoated film.
8) RTA can provide iV_{oc} value similar to the furnace annealing.

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The initial hydrogen content in the as-deposited TOPCon structure should be minimized to avoid blister formation, and the LPCVD of *in situ* B-doped a-Si:H should be done at 588 °C to minimize hydrogen incorporation as well as to obtain a higher poly-crystalline fraction.

Acknowledgment

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Microscale patterning of semiconductor c-Si by selective laser-heating induced KOH etching

Arpan Sinha and Mool C Gupta*

Department of Electrical and Computer Engineering, University of Virginia, Charlottesville 22904, VA

E-mail: mgupta@virginia.edu

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Abstract

Laser patterning has been used for the micro-scale fabrication of semiconductor devices like solar cells, photodetectors, LEDs, and also for modification of surfaces for wettability, reflected colors, initial bacterial adhesion, etc, due to its several advantages of patterning flexibility, spatial resolution, and mask-free operation over complex conventional lithography. Currently, laser-induced ablation is a promising patterning method in silicon solar cell fabrication; however, laser-induced defects, and thermal stresses remain a significant concern. In this paper, we demonstrate a laser ablation-free method for patterning c-Si based on the observation that the anisotropic etching of c-Si by KOH is highly temperature-dependent as the etching rate is about 100 times faster at 80 °C compared to room temperature. The laser heating-induced chemical etching (LHICE) of crystalline silicon can help alleviate such laser-induced damage by providing the necessary low temperature on the localized area(s) on the silicon substrate. We investigated the micro-second pulsed laser-assisted chemical etching of c-Si substrate for microscale patterning and showed that laser-induced damage could be eliminated as indicated by the minority carrier lifetime preservation. We also present results of the effect of laser processing parameters such as laser power, scan speed, and duty cycle on etching depth and surface morphology. The optical, surface morphology, depth profile, and LCPSim simulation results are also presented to optimize and understand the LHICE process. This versatile methodology of temperature-selective chemical etching could be applied to various thin-film and bulk materials used in diverse device fabrication.

Keywords: KOH etching, laser heating-induced etching, microsecond pulsed laser, silicon

(Some figures may appear in colour only in the online journal)

1. Introduction

As of 2017, the crystalline silicon PV modules accounted for about 90% of the world PV solar cell market share [1]. Currently, the interdigitated back-contact hetero-junction (IBC-HJ) silicon solar cells and the passivated emitter rear contact (PERC) silicon solar cells are very popular for commercial applications due to their higher efficiency and lower manufacturing costs [2–4]. Recently, a record 26.1% efficiency for polycrystalline on oxide junction interdigitated back contact (POLO-IBC) solar cell and 26.3% efficiency for IBC-HJ c-Si solar cell have been reported [4, 5] utilizing a laser ablation patterning method. One of the major issues in using laser processing for Si solar cell fabrications lies in the occurrence of laser-induced defects and thermal stress in the lattices, which eventually lowers down the effective minority carrier lifetime (MCL) and hence, conversion efficiency. Hence, the widespread commercialization of high-efficiency IBC and PERC solar cells depends on the availability of a

* Author to whom any correspondence should be addressed.

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low-cost laser-patterning method, which ensures minimum laser-induced damage. The isotropic etching of c-Si can be achieved using a mixture of HF (49%) and HNO_3 (69%) in the ratio of 1:19 by volume and is widely used in the semiconductor industry [6]. Potassium hydroxide (KOH) and tetramethylammonium hydroxide (TMAH) are widely used to create an anisotropic-etched micro-texture surface on c-Si [7–11].

Recent reports show that by using ultrafast femtosecond (fs), picosecond (ps) lasers, and nanosecond (ns) pulse width lasers combined with anisotropic chemical etching (using KOH and TMAH aqueous solutions), SF_6 or HCl gases, or stain etchants (using HF–HNO_3, NH_4HF_2–H_2O, NH_4HF_2–$NaMnO_4$), it has been possible to produce various kinds of micro-and nano-sized structures and microtextures like pores, pillars, porosified pillars, macro-pores, pin-holes and polygonal pits in c-*Si* using laser ablation process [12–16]. These micro-/nano-structures have been made for the fabrication of photoluminescent porous Si (Poro-Si) [13, 16]; better hydrophobicity and enhanced light-trapping mechanism in c-*Si* solar cells and self-cleaning c-*Si* microelectronic devices [14]; controlled reflectance, absorbance, and emissivity of *Si*-based optical devices [15, 17]. A few other applications of Poro-Si are Li-ion battery anodes [18] and other minority carrier devices like photodetectors, thin-film transistors, and LEDs, etc, where their performances degrade due to carrier traps and defect density [19–21]. But the advantages of such micro- and nano-structures are not just limited to the c-Si based solar cell and micro-electronics devices but also to various materials-based devices for novel purposes like surface super-hydrophobicity and wettability [22, 23], reflected colors [24], tribological behaviors [25], bacterial anti-biofouling [26], etc. According to Ji *et al*, when the accumulation and transfer of energy from the laser to c-Si reach the phase explosion conditions (>0.9 T_c, $T_c = 7925$ K, it is the thermodynamic critical temperature of silicon), it leads to an explosion splash of ionized surface material caused by explosive stress, leaving micropores on the silicon surface [14]. Obviously, there were significant defects formed to the surface and bulk of c-*Si* wafers/ substrates due to the extensive laser ablation process and high-temperature chemical etch in all these processes. As a matter of fact, the effects of the direct laser-crystalline silicon interactions seemed to be dominant over the laser-assisted chemical etch interaction effects. The laser-induced damages were not characterized adequately, and the preservation of MCL was not previously investigated. Additionally, there is a lack of understanding of the role that micro-second (μs) pulse width lasers play in low-temperature laser-assisted KOH etching of c-Si and how it influences the change in the MCL. Several works on laser-assisted photochemical wet etching methods have been reported where the exposure of a particular laser wavelength with an optimized intensity selectively enhances the photochemical etch rate at a localized place and does not depend on the laser heating. However, such a method is limited to only semiconductor materials like c-Si, GaAs since the etching rate depends on the formation of e^-h^+ pairs and requires toxic etchants like HF [27, 28].

From semiconductor processing, it is well known that the KOH etching rate increases exponentially above the room temperature as described by the Arrhenius equation, and the optimum temperature range lies within 80 °C to 100 °C. The 30 wt% concentrated KOH etch rate of c-*Si* (100) at 20 °C is $\sim$1.44 μm h^{-1} (=24 nm min^{-1}) whereas at 80 °C, the etch rate becomes $\sim$79 μm h^{-1} (=1316 nm min^{-1}) [9]. The mechanism of silicon etching by KOH is a two-step sequential oxidation and etching reaction. During the rate-limiting process of oxidation, H-terminated Si atoms at the surface get oxidized to OH-terminated Si atoms due to OH^- ions from KOH aqueous solution. In the presence of H_2O, polarization and weakening of the back bonds occur due to differences in electronegativity between Si and O. Consequently, etching (removal) of Si atoms occurs in the form of $Si(OH)_4$ complexes [29]. The rate-limiting oxidation process can be accelerated by an optimal temperature range from 80 °C to 100 °C. Moreover, it is a non-toxic, economical, and commonly used alkali metal hydroxide silicon etchant, which requires a simple etch setup and provides high silicon etch rate, a high degree of anisotropy, moderate Si/SiO_2 etch rate ratio, and low etched surface roughness.

Generally, the prime goal of creating textures and pyramidal shapes on a c-Si surface has been to enhance light trapping, using alkaline KOH, NaOH, and TMAH, ensuring surface reflectivity as low as 6% [30]. The KOH etching/ texturizing of c-Si does not cause any major damage to the surface quality, and the surface passivation on the etched/textured c-Si can be further improved by the deposition of SiO_2/Al_2O_3 and SiN_x/Al_2O_3 stack layers [31–33]. The surface passivation, as in IBC solar cell fabrication, can also be done by depositing the PECVD stack of a-Si /SiO_2 /SiN_x (aSON) layers on the textured c-Si to obtain effective surface recombination velocities (*SRV*s) below 1 cm s^{-1} [34]. Zielke *et al* reported that a very low saturation current density of (174 ± 11) fA cm^{-2} was measured on the PERC cells after KOH pyramidal texturization, followed by atomic-layer-deposited AlO_x, indicating better contact passivation [35]. The report by Werner *et al* shows that it has been possible to achieve a low *SRV* below 2.9 cm s^{-1} with a 10 nm thick Al_2O_3 layer, deposited by spatial ALD process, on a KOH-etched n-type Czochralski-grown (Cz) silicon [36]. Hence, an optimum temperature range (80 °C to 100 °C) has to be achieved, which would suffice for KOH etching/texturization. Similar laser-assisted temperature-selective micro-etch/ texturization is quite feasible for controlled etching steel in etchant $FeCl_3$ and aqueous solution mixture of $FeCl_3$/ HCl/ HNO_3 for super-hydrophobicity, wettability and surface-reflected colors [23, 24, 37, 38], Ni–Co alloys on steel in etchant 30% v/v HCl/ethyl alcohol for tribological properties [25, 39] and many more. Moreover, such methodology can also overtake the extensive electrochemical etching for Poro-Si texturization, which eventually lowers down the carrier lifetime [40].

In this paper, we describe a highly localized micron-resolution patterning using a micro-second (μs) pulsed laser based on the laser heating-induced chemical etching (LHICE)

process, where the carrier lifetime is preserved. This methodology's fundamental approach lies in the increase in the temperature at localized areas irradiated by laser and enhancing the forward reaction rate of temperature-dependent chemical etching of c-Si. Hence, by proper selection of laser processing parameters, the patterning of c-Si was achieved, and no direct ablation by laser was required. Such a temperature regime was considered low and safe for silicon solar cell fabrication. Consequently, the direct laser-induced defects and thermal stresses in the c-Si lattice were minimized.

After using microsecond pulse-width laser-heated KOH etch patterning of c-Si, we investigated the effect on MCL. Analytical techniques like optical microscopy, scanning electron microscopy (SEM), Sinton QSSPCD MCL measurement, white-light Zygo optical profilometry, and LCPSim simulation were used for characterizations to understand the laser-assisted chemical etching process. This low-cost, low-temperature patterning method will find other applications in a variety of solar cell designs based on inorganic and organic materials, and the availability of such a method for the fabrication of high-efficiency solar cells will greatly help the solar industry. It will also be applicable to a variety of other materials like metals, ceramics, and semiconductors.

2. Experimental

The laser used in the experiment was IPG Photonics YLR-150/1500-QCW-AC-Y11 with a wavelength of 1070 ± 5 nm operating at quasi-continuous mode. The pulse energy was ~1.5 J with a maximum peak power of 1500 W. The laser repetition rate was kept constant at 500 Hz. To study the effects of duty cycles on LHICE, the laser pulse widths were 100 μs, 150 μs, 200 μs, and 250 μs. Hence, the corresponding duty cycles were 5%, 7.5%, 10% and 12.5% respectively. In order to study the effects of the laser scan speeds on LHICE, the scan speeds of 10 mm s^{-1}, 15 mm s^{-1}, and 50 mm s^{-1} were used. To investigate the effect of laser power, the average laser powers of 14.1 W, 16.4 W, 18.6 W, and 21 W were used. The laser spot size was fixed at ~430 μm at FWHM at the focal plane, and the total scan number was kept constant at 4.

The double-side polished n-doped FZ c-Si <100> type wafer with a thickness of 300 μm and 1–5 Ω cm resistivity was used for the experiments. The c-Si wafer was cut into a 1 × 1 inch size sample and then cleaned with methanol and HF solutions to get rid of surface contaminants. A total of nine straight parallel lines were patterned, quite similar to the pattern used by Sinha *et al* [41], each 13 mm long and separated by gaps of ~500 μm in between while keeping it immersed in a 30 wt% concentration of KOH alkaline solution in a polystyrene petri dish. The petri dish was filled up to 1 mm in the height of the KOH solution above the wafer. The schematic diagram of the experimental setup is shown in figure 1. The MCL was measured before and after the laser processing using a chemical passivation technique of 0.08 mol l^{-1} concentration of I_2-methanol solution [42]. The investigative analysis was further carried out using optical microscopy, SEM, white-light Zygo optical profilometry, and LCPSim simulation [43].

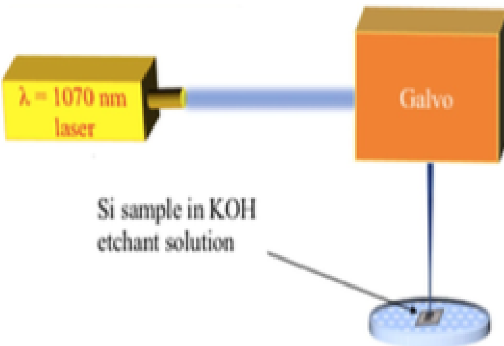

Figure 1. Schematic diagram of the experimental setup.

The optical images were taken using a Hirox 3D Digital Microscope. The QSSPCD MCL was measured using WCT-120 Silicon Wafer Lifetime Tester made by Sinton Instruments. The surface morphology was characterized using an FEI Quanta 650 Field Emission Scanning Electron Microscope, and the depth profiles were measured using the white-light optical profilometer Zygo NewView 7300.

3. Results and discussions

3.1. *Influence of laser processing parameters, surfactant, and solution stirring*

The understanding of the effects of various laser processing parameters like laser scan speed, duty cycle, and laser power on the surface morphology is essential for laser-patterning optimization. In addition to that, the effects of the usage of surfactant and solution stirring process were examined. The non-destructive white-light Zygo optical profilometry was used for the characterization of all the depth profiles of the laser-assisted etched groove lines under these different conditions.

3.1.1. The effect of laser scan speed variation. The effect of laser scan speed on LHICE was investigated. From figures 2(a)–(c), it was observed that at a constant average power of 18.6 W and 5% duty cycle, the etch depth increased from ~25 nm to 135 nm as the scan speed was reduced from 50 mm s^{-1} to 10 mm s^{-1}. Lower scan speed corresponded to the higher number of laser pulses, and hence, more heating occurred, which resulted in deeper etchings. The depth-color maps show distinct groove features with increasing etch depth as the scan speed was reduced, as shown in figures 2(d)–(f). But as the scan speed was reduced below 10 mm s^{-1}, excessive heating occurred, which resulted in direct evaporation of KOH and laser-induced ablations of the c-Si.

The color map also proves that there is negligible impact outside the desired etched region, and the process was highly spatially localized. Laser processing in a liquid etchant medium is different from laser processing in air/vacuum. From the literature, it is known that the lattice thermal conductivity

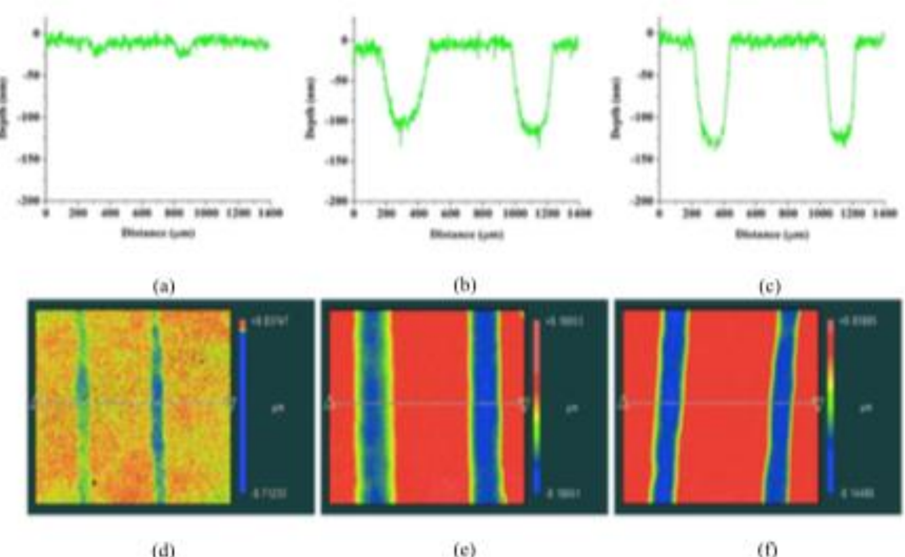

Figure 2. Zygo profilometry showing the surface profile of laser-induced KOH etched lines on the c-Si substrate at scan speed (a) 50 mm s^{-1}, (b) 15 mm s^{-1}, and (c) 10 mm s^{-1}, respectively while keeping other parameters constant. The figures(d)–(f) show the depth-color mapping images of the lines corresponding to the scan speeds of 50, 15, and 10 mm s^{-1}, respectively.

of c-Si (~5.1 W (m K)$^{-1}$) is greater than the thermal conductivities of 30 wt% KOH (~0.727 W (m K)$^{-1}$) and air (~0.02–0.03 W (m K)$^{-1}$) [44–46]. Hence, much of the laser-induced heat is redistributed within the c-Si lattice and a small amount of the heat gets dissipated out to an immediate liquid etchant medium. This results in the heating of the liquid surrounding the laser-irradiated region on c-Si. Figure 3 shows the top-view SEM image of a laser-assisted KOH etched line on the c-Si substrate at a scan speed of 15 mm s^{-1}. The average width of the etched groove line was found to be ~280 ± 10 μm. The SEM results indicate that the localized laser-induced heat was responsible for the KOH-etched groove and not the direct laser ablation and stress. The laser power was low enough not to cause direct melting of the silicon surface. Minor turmoil and boiling of the etchant liquid near the Si surface caused the groove boundaries to be slightly irregular. Too high a laser power will cause melting of silicon, a significant amount of bubble formation and vaporization and would lead to uncontrolled etching.

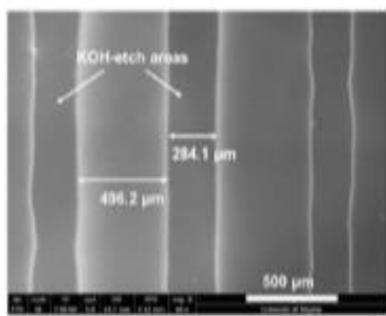

Figure 3. Top-view SEM image of the laser-induced KOH etched lines obtained under the scan speed 15 mm s^{-1}.

3.1.2. The effect of laser duty cycle. Figures 4(a)–(c) show an increasing etch depth from ~25 nm to 80 nm and groove line-width increase from ~150 μm to 350 μm as the duty cycle was increased from 5% to 10%. For constant laser average power and scan speed, the shorter pulse-width caused higher peak energy per pulse, resulting in limited etching even though the laser-induced temperature was quite high. As the duty cycle increased, the pulse-width increased, which caused a longer heating duration. Consequently, more time was available for KOH chemical reaction to occur, resulting in deeper etch depth and wider groove lines. Thus, the duty cycle was found to be an important factor influencing the LHICE method. The LCPSim simulation model, discussed in the later section, also proved the importance of a longer duration of heating and a larger duty cycle.

3.1.3. The effect of laser power variation. The results of the influence of varying average laser power while keeping 7.5% duty cycle and a scan speed of 50 mm s^{-1} are shown in figures 5(a)–(c). As the average laser power was increased

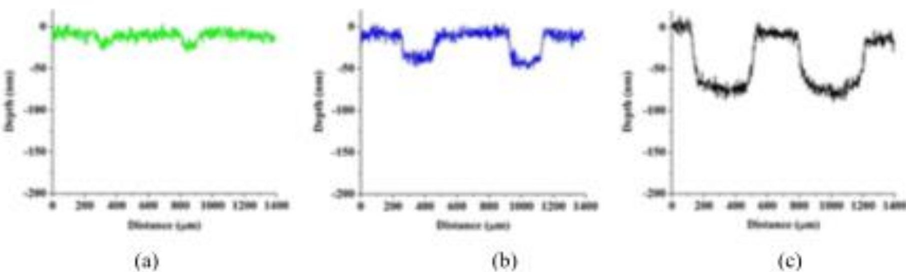

Figure 4. Zygo profilometry showing the surface profile of the KOH-etched groove lines at various laser duty cycles (a) 5%, (b) 7.5%, and (c) 10% while keeping average power (18.6 W) and scan speed (50 mm s^{-1}) constant.

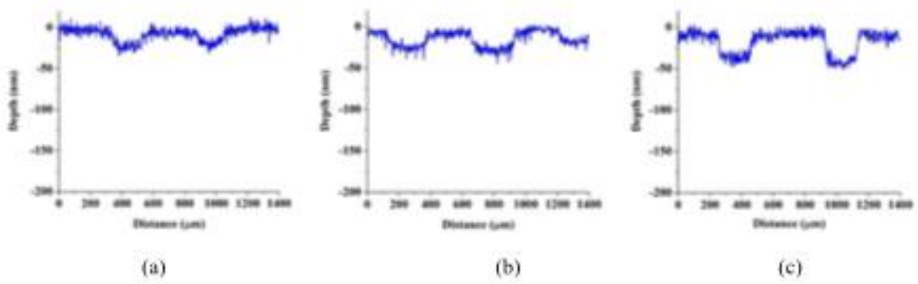

Figure 5. Zygo profilometry showing the surface profile of the KOH-etched groove lines at various average laser powers (a) 14.1 W, (b) 16.4 W, and (c) 18.6 W while keeping other parameters constant (duty cycle = 7.5% and scan speed = 50 mm s^{-1}).

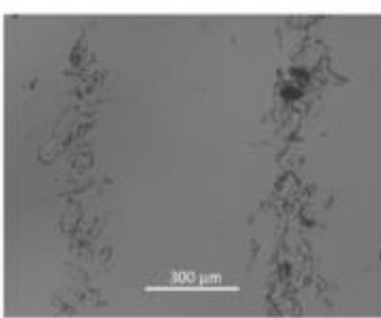

Figure 6. Optical image showing the laser-induced ablation at an average power of 21 W.

from 14.1 W to 18.6 W, there was a small increase in the etch depth. Although the etch depth increase was not that significant, but the groove lines widened. Average power lower than 14.1 W did not create any etch grooves and average power higher than 18.6 W caused direct laser ablation of silicon, as shown in figure 6. So, it was concluded that the average power solely could not determine to etch depth in LHICE.

3.1.4. The effect of using surfactant and solution stirring. The surfactant Triton X-100 is generally used for improving surface wetting during KOH etching of c-Si. A 100 ppm of Triton X-100 was added to 30% KOH solution. Figures 7(a) and (b) show the etch depth for KOH solution with and without surfactant. It was found that under constant average power of 18.6 W, 5% duty cycle, and a scan speed of 10 mm s^{-1}, the sample etched with Triton containing KOH had shallower etch depth (~75 nm) than the one etched with only KOH (~130 nm). The etching rate was found to be slower in the case of Triton-added KOH etch, but the average roughness improved from 36 nm to 20 nm. Similar lower etch rates and smoothening effects of Triton addition to KOH etchant had been shown earlier by Rola *et al* [47].

In order to remove bubbles formed during heating, solution stirring was attempted using a magnetic stirrer, rotating at 50–100 rpm. The liquid stirring caused an increase in unwanted turbulences on the liquid surface. This led to the irregularity in etch depth due to the higher scattering of the laser beam.

3.1.5. Reproducibility and scalability. Reproducibility and scalability are the important factors that determine its reliability and industrial application. Three identical samples were etched using the same laser parameter conditions. From figure 8, it is observed that using average power of 18.6 W, 5% duty cycle and a scan speed of 15 mm s^{-1}, similar etch depth (~110 ± 10 nm) and width (~300 ± 20 nm) were obtained. So, the LHICE process is reproducible and reliable.

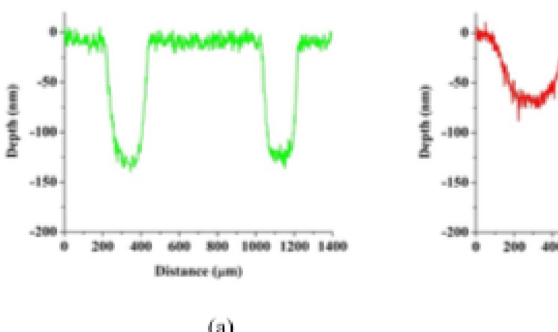

Figure 7. Zygo profilometry showing the surface profile of the KOH-etched groove lines (a) without Triton X-100 and (b) with Triton X-100 while keeping all laser parameters constant (duty cycle = 5% and scan speed = 10 mm s^{-1}).

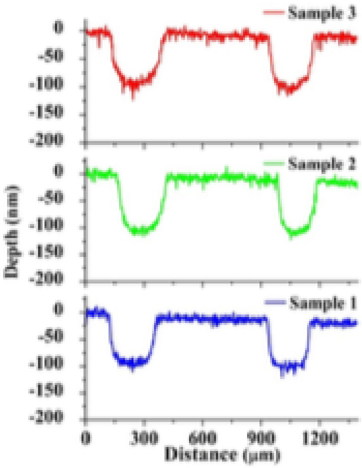

Figure 8. Zygo profilometry showing the reproducibility of the etch depths in three different 1 × 1 inch c-Si samples using the same laser parameters: average power 18.6 W, 5% duty cycle, and scan speed of 15 mm s^{-1}.

3.1.6. The effect of laser-assisted chemical etch time. The silicon etching rate is dependent on KOH concentration and temperature. In our study, KOH concentration was fixed at 30 wt%. The etching rate initially increases with concentration and then decreases. So, it may be possible to choose higher KOH concentration which will allow increase in the boiling point of the solution and lower etching of the laser untreated area [48].

The applicability of the LHICE process should fulfill the short time criterion to achieve high throughput in the solar cell industry. Commercially, 6 × 6 inch silicon solar cells are quite dominant in the market, and hence, selective laser-assisted KOH etching of 6 × 6 inch c-Si wafers must be a time-efficient process.

The approximate time taken to pattern four scans of a single 13 mm straight line was 1.65 s to obtain ∼110 ± 10 nm groove depth. Hence, the total time taken to pattern nine such parallel patterns was 14.85 s. The time taken for a complete selective laser-assisted KOH etching of c-Si samples can be improved by an optimized combination of multiple-beam systems, spot size, KOH concentration, average laser power, pulse width, laser wavelength, and the number of laser scans. So, to draw a single 6 inches (i.e. 152.4 mm) line pattern on a 6 inch wafer with four scans and similar groove depth, it would take 18.9 s. To create each etched line of ∼20 nm etch depth, it would take approx. 4 s. The amount of etched depth can be chosen according to the industry needs. By using a multiple beam system, it is possible to shorten the large-area processing time further. Instead of using circular laser beams, one-dimension line beams can be used to generate faster uniform line patterns. By using higher power lasers, the focused laser beamline length can be made longer than used in our experiments, which will allow much faster throughput.

3.2. QSSPCD carrier lifetime characterization of semiconductor c-Si

QSSPCD characterization tool is useful to investigate the extent of damages and defects on the surface and bulk of the c-Si substrate after the laser processing. Figure 9 shows the QSSPCD MCL data vs. carrier density measured before and after the LHICE process. The lifetime was measured for three separate c-Si substrates, each of dimension 1 × 1 inch, which were used for etch-depth reproducibility earlier, as discussed in section 3.1.5. Each of the measurements was done at the minority carrier density of 1 × 10^{15} cm^{-3} over an average of three measurements. The effect of LHICE on c-Si substrates had been investigated based on the MCLs and implied open-circuit voltages (iV_{oc}), which are tabulated in table 1. From the point-of-view of silicon solar cell fabrication, such decrease in MCL and iVoc do not affect the performance profoundly. Such insignificant decreases in the carrier lifetime (−17.1%) and iV_{oc} (−1.25%) shows our successful attempt at localized

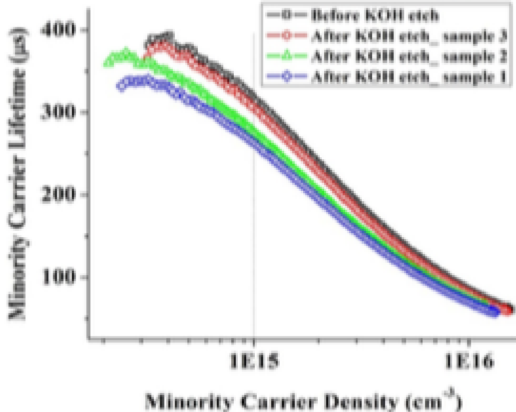

Figure 9. QSSPCD carrier lifetime measurements before and after LHICE for three different 1 × 1 inch c-Si samples showing its reproducibility. The temporary passivation for lifetime measurement was made by the iodine–methanol passivation method.

laser-assisted KOH etching and minimizing the laser-induced stress and ablation damage on a c-Si substrate. The direct laser ablation would significantly reduce the carrier lifetime due to defects and damage in bulk. Wilkes has shown that laser processing in the air generally causes lifetime reduction and damage to the silicon, although the 1070 nm wavelength is not generally favored for surface micro-patterning on silicon [49].

3.3. Modelling and simulation for wavelength and power optimizations

3.3.1. LCPSim simulation. Using the Fraunhofer ISE simulation software LCPSim 1.3 designed by Fell *et al*, we had been able to generate simulation results to predict the relation between the laser power and the temperature on the c-Si surface [43]. Due to the limited scope in wavelength and medium selection in the simulation program, Near-Infrared 1064 nm wavelength laser was chosen as the laser wavelength and air as the medium for simulations, keeping all other physical and laser parameters constant. The process parameters for simulation were similar to the experimental conditions. The laser spot size was kept constant at ∼430 μm. The LCPSim simulations were done to show the effect of a single 1064 nm laser pulse on c-Si. Figure 10(a) shows the increase in the simulated peak temperature as the average laser power was increased from 14.1 W to 21 W. All other laser parameters like duty cycle (7.5%) and scan speed (50 mm s^{-1}) were kept constant. The simulations show that the peak temperatures lie in the range from ∼140 °C to 1000 °C. As the average power increased, the FWHM of temperature curves increased. The wider FWHM of the curves implies longer heating duration time. At 800 μs, all the temperature curves saturated to above ∼50 °C.

Figure 10(b) shows the effect of laser duty cycles on LHICE while all other laser parameters like average power and scan speed were kept constant at 18.6 W and 50 mm s^{-1}, respectively. There are two major observations from the simulation: (a) lower laser duty cycle increased the peak temperature, and (b) higher duty cycle led to the increase in the FWHM. At lower duty cycles, KOH chemical reaction time was too short of producing significant etch depth. As a result, very shallow grooves were observed, as shown in figure 4(a). Also, the FWHM width was narrow over a short time span which also explains the shallow etch depth at lower duty cycles.

It can be safely assumed that the liquid (KOH/water) medium must have resulted in a lower peak temperature simulation result due to the higher thermal conductivity value of the KOH solution compared to air. Hence, the whole simulation result coincides with our experiments on localized laser-assisted KOH etching of c-Si. The localized temperature was raised enough for KOH etch mechanism but not for the direct melting/ ablation of the c-Si substrate.

3.3.2. The effect of laser wavelength. Near-surface heating is generally favored for fabricating low defect-density devices. The near-surface heating in laser-assisted chemical etching would ensure to limit the laser energy absorption at the interface of the KOH solution and the c-Si surface where the actual chemical etching would take place. The bulk heating of the device could induce thermal stress-related defects within the bulk due to heat accumulation. The laser heating depth can be controlled by a proper selection of laser fluence, wavelength, spot size, and other related process parameters. According to Beer's law, the choice of laser wavelength determines the absorption depth of light propagating through a particular material. Shorter wavelengths like UV wavelengths can be opted for near-surface heating of c-Si due to its near-surface absorption depth. The absorption depth of UV 355 nm wavelength in c-Si is ∼10 nm, and for 1070 nm, the wavelength is ∼0.1 cm [50]. Figure 11 shows the LCPSim simulation of achieving a maximum temperature of ∼250 °C for a single laser pulse of wavelength 355 nm. The laser parameters used were spot size of 25 μm, pulse-width of 25 ns, a repetition rate of 50 kHz, and average power of 0.05 W. It took approx. 0.045 μs to reach the peak temperature and eventually plummeted down to 50 °C within 0.2 μs. It can be concluded that using nano-second pulse-width UV 355 nm would be beneficial for LHICE without any enormous heat diffusion in bulk. However, the short heating times would lead to lower chemical etching times and would produce much shallower etch depths. Higher etch rates could be achieved by using higher repetition rate lasers.

3.4. Direct applicability of LHICE process to diverse semiconductor device fabrication

The laser-assisted spatially localized temperature-selective method is applicable for diverse materials, which includes semiconductors, dielectrics, metals and alloys, glass, and polymers using different etchants. A few such examples are shown in table 2.

Table 1. QSSPCD measurements to show the reproducibility of LHICE process on c-Si samples.

Sample	Laser parameters	Before LHICE MCL	Before LHICE iV_{oc}	After LHICE MCL	After LHICE iV_{oc}	Percentage change
Average of all three starting samples	—	320 μs	640 mV	—	—	—
Sample 1	18.6 W, 5% D.C. and 15 mm s^{-1}.	—	—	265 μs	632 mV	ΔMCL = − 17.1% $\Delta iV_{oc} = -1.25\%$
Sample 2	-do-	—	—	285 μs	635 mV	ΔMCL = − 10.9% $\Delta iV_{oc} = -0.78\%$
Sample3	-do-	—	—	301 μs	639 mV	ΔMCL = − 5.93% $\Delta iV_{oc} = -0.15\%$

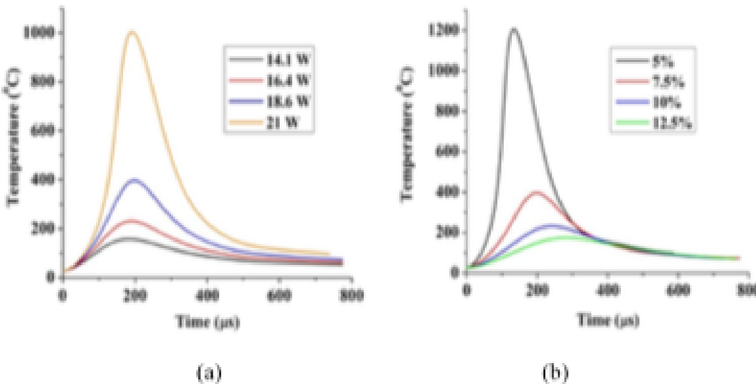

Figure 10. LCPSim simulation results of a single 1064 nm laser pulse showing (a) the maximum temperature profile with respect to time at different average laser powers while other laser parameters constant and (b) the maximum temperature profile with respect to time at different duty cycles while other laser parameters constant.

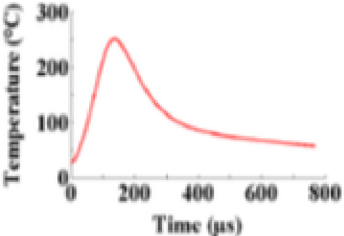

Figure 11. LCP Sim simulation results for a single laser pulse of spot size 25 μm with the wavelength 355 nm, pulse-width of 25 ns, the repetition rate of 50 kHz, and average power of 0.05 W.

The LHICE process is implementable for etching holes and grooves required for diverse device fabrication. In PERC and Al-BSF solar cells, direct laser drilling of local openings in Al, AlO_x, SiO_2/SiN_x, and AlO_x/SiN_x stack layers had been previously attempted with some laser-induced defects and passivation damages. Such local openings can be made by selective laser patterning of SiN_x in H_3PO_4, AlO_x and Al in KOH, and SiO_2 in KOH [65–67]. Wu *et al* showed the KOH etching process for bulk micromachining of 100 mm diameter (100) silicon substrate, SiO_2, and SiN_x passivation layers for the fabrication of high-temperature pressure sensors based on polycrystalline and single-crystalline 3C-SiC piezo-resistors [68], which are also achievable by selectively chemical-etching by laser patterning in KOH and H_3PO_4 solutions. Such LHICE process is also useful even in the fabrication of microfluidic devices based on glass and silicon where the channel grooves/holes are created using photoresists or a-Si masks [69]. The LHICE process can replace the conventional etching method of soda-lime glass for the fabrication of high aspect ratio-microfluidic channels, which had been previously shown by Lin *et al* [70]. Lastly, in the fabrication of MEMS devices, removal of Parylene C layers on silicon and silicon oxide substrates is accomplished by piranha solution (7:3 mixture of H_2SO_4 and H_2O_2) and chloronaphthelene or benzyl benzoate, wet KOH etching [71], which can be fabricated using LHICE process. So, it is quite evident that such a method will find its applicability in many other thin-film and

Table 2. Etching rates of different etchants on various materials at higher operating temperatures.

Materials & description	Etchant	Etch rate at a lower temperature		Etch rate at a higher temperature		Reference
Au	Transene Au-etchant TFA	~30 Å s^{-1}	20 °C	~150 Å s^{-1}	60 °C	[51]
AlN	Photoresist developer AZ400K.	~50 nm min^{-1}	40 °C	~600 nm min^{-1};	75 °C	[52]
Boron-doped c-Si (100)	Ethylene diamine-pyrocatechol-water (EDP)	167 nm min^{-1}	66 °C	~500 nm min^{-1}	110 °C	[53]
Monel-400 alloy	$FeCl_3$, $CuCl_2$	6 μm min^{-1}	40 °C	12.5 μm min^{-1}	80 °C	[54]
Polyimide polymer	2 M NaOH + 50% ethylene diamine	0.1 μm min^{-1}	30 °C	~0.9 μm min^{-1}	80 °C	[55]
$Si_{0.8}Ge_{0.2}$	25% TMAH	5 nm min^{-1}	~50 °C	19 nm min^{-1}	~75 °C	[56]
SiN_x (low refractive index)	30–40 wt% KOH	Negligible	25 °C	0.67 nm min^{-1}	80 °C	[57]
Si_3N_4	BOE	2 nm min^{-1}	40 °C	62 nm min^{-1};	90 °C	[58]
Si_3N_4	94.5% H_3PO_4	0.6–3 nm min^{-1}	140 °C	11.5–20 nm min^{-1};	180 °C–200 °C	[59–61]
SiO_2	BOE	0.2 nm min^{-1}	40 °C	0.6 nm min^{-1};	90 °C	[58]
SiO_2	5 wt% TMAH	100 Å h^{-1}	60 °C	>400 Å h^{-1}	76 °C	[62]
Soda-lime glass	BOE/HCl mixture	1.5 μm min^{-1}	5 °C	~5.5 μm min^{-1}	55 °C	[63]
TiO_2	H_2O_2:NH_4OH:H_2O (1:1:5 by vol.)	0.29 ± 0.09 nm min^{-1}	25 °C	15 ± 1.4 nm min^{-1}	65 °C	[64]

MEMS device fabrication fields, which are not discussed here, where flexible localized laser patterning will make it possible for achieving high throughput without creating any defects in the devices.

The fluorescent dyes (both water- and IPA-soluble) may be added into the etchant solution for better absorption of a particular laser wavelength. This approach will only heat the KOH solution and accelerate the etching reaction without any thermal effects on c-Si. The water-soluble dyes like BBT-mPEG, benzothiopyrylium pentamethine cyanines, and commercial fluorescent dyes like CFTM dyes and LUWSIR4 dyes having a wide range of diverse wavelength absorption-sensitivities can be used for the LHICE process [72–75].

4. Conclusion

A new method of laser patterning using localized laser-heating induced KOH etching of c-Si substrates with minimal impact on electronic properties has been demonstrated. The effect of various processing parameters such as laser scan speed, duty cycle, average power, and other factors like the addition of surfactant, solution stirring, etchant concentration, and etching time was investigated. LCPSim simulations were done to calculate the laser-generated temperature and provided an understanding of the laser-induced heating of KOH.

The etching depth was found to increase as the laser scan speed was reduced from 50 mm s^{-1} to 10 mm s^{-1}. The scan speed, faster than 50 mm s^{-1}, did not induce any observable etching, and slower than 10 mm s^{-1}, introduced direct laser-induced damage to c-Si. The increase in laser pulse width from 100 μs to 200 μs led to an increase in etching depth. A longer pulse width provided more laser heating time and higher KOH chemical etching reaction time. At an average laser power of 14.1 W, no noticeable etching was observed, whereas greater than 18.6 W induced damage to the c-Si. The etching depth was found to increase steadily as the laser power was increased. Both average laser power and pulse width can be optimized for the desired etch depth. The addition of surfactant Triton X-100 slowed down the KOH etch rate, resulting in shallower etch depths as compared to the condition without surfactant. The surface roughness was reduced with the presence of the surfactant. The solution stirring proved unreliable to drive away bubbles in the liquid etchant as it impacted the incident laser beam.

The reproducibility and scalability of LHICE were examined using three identical samples and measurement of etching depth and MCL. From the QSSPCD lifetime measurement, an insignificant drop in carrier lifetime (~55 μs) and less than a few percent change in implied open-circuit voltage were observed. Such changes are insignificant for solar cell devices. The optical and SEM images showed the smooth etched grooves with no visible damage outside the etched region, which proved the high selectivity and localization. The laser-generated groove boundaries were slightly irregular due to minor turmoil and bubbles in the liquid KOH medium, which could be improved by further optimization of laser parameters. The width of the grooves was found to be approximately ~300 ± 10 μm, and the highest depth was ~130 ± 20 nm using a laser spot diameter of ~430 μm. The throughput of chemical etching can be improved further by using an optimized combination of KOH etchant concentration, multiple laser beam system, 1D line beams, and laser processing parameters. Higher KOH concentration will

increase the boiling temperature of the liquid and would have less effect on untreated laser areas on the substrate.

The LCPSim simulation software was used to simulate the maximum temperature reached at the center of the laser beam as a function of time for a single laser pulse of different pulse-width and average powers of 14.1–21 W and a wavelength of 1064 nm. The temperature gradient on the c-Si surface was also determined at different times. The simulated peak temperature and the temperature gradient showed the required temperature range of KOH-etch operation at localized regions without reaching the melting point of c-Si. Using smaller laser wavelength like 355 nm could be used for more surface-oriented etch.

The demonstrated temperature-dependent localized laser-assisted etching methodology could be equally applicable on various kinds of bulk and thin-film materials like semiconductors, metals, dielectrics, polymers, glasses, which can find applications in surface-enhanced super-hydrophobicity, wettability, tribology, bacterial anti-fouling, solar cells, photodetectors, light emitters, and diverse micro-device fabrication.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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Credit authorship contribution statement

Arpan Sinha: Methodology, Software, Formal analysis, Investigation, Writing—Original Draft, Writing—Review & Editing, Validation.

Mool C Gupta: Conceptualization, Supervision, Project administration, Funding acquisition, Technical discussion, Writing—Review & Editing.

ORCID iDs

Arpan Sinha https://orcid.org/0000-0002-5459-5949
Mool C Gupta https://orcid.org/0000-0002-1782-5354

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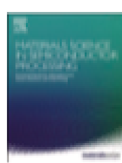

Process-induced losses by plasma leakage in lithography-free shadow masked interdigitated back contact silicon heterojunction architectures

Anishkumar Soman [a,b,*], Ujjwal K. Das [b], Nuha Ahmed [a,b], Arpan Sinha [c], Mool C. Gupta [c], Steven S. Hegedus [a,b]

[a] Department of Electrical and Computer Engineering, University of Delaware, Newark, DE, 19716, USA
[b] Institute of Energy Conversion, University of Delaware, Newark, DE, 19716, USA
[c] Department of Electrical and Computer Engineering, University of Virginia, Charlottesville, VA, 22904, USA

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ABSTRACT

Silicon (Si) Heterojunction (HJ) solar cells with interdigitated back contact (IBC) are considered a promising candidate for next-generation silicon photovoltaics due to the highest efficiency on a single junction device achieved by this architecture. However, the complex fabrication process involving photolithography has limited its prospect for commercial scalability and adoption by the industry. To overcome this challenge, we have investigated a lithography-free process for HJ IBC using in-situ shadow masking during the deposition of doped layers to form an interdigitated pattern combined with laser ablation for contact formation. However, this process resulted in poor open-circuit voltage (V_{OC}). Lifetime measurements, Photoluminescence (PL), and electroluminescence (EL) studies showed that this does not originate from passivation loss. We investigated this phenomenon using back junction (BJ) test structures with rear architecture similar to our IBC cells to isolate the emitter. A detailed characterization using optical microscopy, EL and current density-voltage (J-V) analysis revealed the plasma leakage during the process resulted in shunts, a barrier to injection, and resistive losses. To mitigate this process-induced loss, we developed a uniform controllable wet-etch method to remove the plasma leaked layer. This resulted in improving V_{OC} in the HJ IBC cells by greater than 300 mV, thereby validating the detrimental effect of plasma leak and its significance in developing a low-cost, manufacturable and scalable process for high-efficiency Si HJ IBC solar cells.

1. Introduction

Solar Photovoltaics is the third largest renewable electricity source globally, currently contributing to 3.6% of the global electricity production [1] and has reached the terawatt scale [2,3]. The way forward for the market-dominant silicon (Si) photovoltaics is to develop lower-cost industrially manufacturable processes retaining higher efficiency to reduce the cost per watt. The world record efficiency of 26.81% for single junction silicon solar cell is held by silicon heterojunction (HJ) by LONGi [4]. The interdigitated back contact (IBC) architecture, which was introduced by Schwartz and Lammert for solar concentration application [5], was first combined with the HJ structure by our lab in 2007 [6] to demonstrate the HJ-IBC concept. The HJ-IBC concept combines the high open-circuit voltage (V_{OC}) of HJ, which comes from the superior interface passivation by intrinsic amorphous silicon (a-Si:H) and higher short-circuit current density (J_{SC}) of IBC, originating from the absence of front metal shading loss since both the emitter and the back surface field are shifted to the rear surface. The HJ-IBC concept also helps achieve simpler cell interconnection, increases active module area, and improves the aesthetics of the solar panel. However, despite these many advantages, the Si HJ IBC solar cell has been unsuccessful to find commercial market penetration due to the complexity of its fabrication process and the involvement of lithography steps to fabricate the interdigitated pattern [7,8]. Though companies like Maxeon/Sunpower have shown commercially scalable IBC, they remain one of the most expensive modules in the market, and also the technology hasn't been translated for commercial success in silicon heterojunction solar cells, hence a method for low-cost patterning would be beneficial. It is interesting to note even after a decade of IBC being commercialized there haven't been any competitors to this technology, the reason has been assumed to be the complexity and cost of IBC manufacturing. Additionally, there is ambiguity in the exact steps

* Corresponding author. Department of Electrical and Computer Engineering, University of Delaware, Newark, DE, 19716, USA.
E-mail address: aksoman@udel.edu (A. Soman).

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followed for the fabrication of IBC in the industry, most laboratory scale cell fabrication relies on multiple lithography steps using resists which not only inhibits scaling but also introduces contaminants that can affect the doped layers. They also require an expensive and slow mask alignment process. Such challenges can be overcome by using a simplified patterning process without lithography. There are multiple methods in the literature that uses non-lithographic methods for patterning the rear side of IBC structures, such as inkjet printing [9], hard masking [10], direct laser writing [11], screen printing [12] and ion-implantation [13] to name a few. Though all these approaches show promising results and avoid the complexities of multi-step photolithography, they all have inherent limitations. Using hard masks like silicon oxide [14] or dielectric mirrors [15] can provide a well-defined emitter pattern, however, the lift-off with chemical etch is not scalable for the industry. Additionally, the dielectric mirror hard mask mentioned previously requires multiple bilayers of dielectric layers using rf-PECVD [16], for acting as a selective reflector to laser light to prevent damage to the bottom passivation layer during laser ablation, which could make the entire process costlier for large area applications. Inkjet and screen printing, though industrially relevant, still require to etch resists and resist stripping by lift-off, which inhibits their manufacturing capability for IBC cells. Direct laser writing can help achieve high throughput for patterning; however, the quality of the interface passivation, post-transfer process, and the adhesion of these layers to the surface is still a topic of concern. In our previous work, our group [17] demonstrated that although laser-firing localized metal contacts that had been deposited through a single shadow mask was viable, it resulted in low Fill Factor (FF) due to high series resistance and low V_{OC} coming from the laser damage. Ion-implantation can offer well-defined, controlled, and repeatable patterning; however, it requires a very large capital cost for equipment and a high-temperature defect anneal step, which is incompatible with low-temperature a-Si layers.

In recent years there has been an increased interest in the shadow masking approach for patterning interdigitated back contact [18–21] which has shown promising results for fabricating viable HJ-IBC solar cells. In this work, we present an approach to obtain interdigitated pattern by using shadow masking in-situ while depositing the doped layer in a plasma enhanced chemical vapor deposition (PECVD) chamber and making the contact opening using laser ablation. This process gives the advantage of developing the patterned doped layers in-situ with no additional equipment cost. Also, using laser ablation only for opening the contacts reduces the possibility of large area laser-induced damage, which could severely impact the V_{OC} [22]. But using a mask in the PECVD deposition introduces plasma leakage at the edge of the mask [23,24], which can result in edge recombination due to the lateral spread of the doped layers as well as shunting of the p- and n-fingers. We have found that this approach drastically affects the V_{OC} in spite of having superior passivation before metallization. The reason for this V_{OC} loss is investigated here using a novel approach: creating patterned back junction test structures. Methods to mitigate this loss are discussed for its widespread application to fabricate Si HJ IBC solar cells. Thus, our work will pave the way for low-cost scalable manufacturing processes for HJ IBC solar cells by discussing methods to mitigate the process-induced losses.

2. Experimental section

2.1. Fabrication

The Si HJ IBC solar cells are fabricated on n-type one-inch square Czochralski (Cz) silicon wafers having a resistivity of 1–10 Ω-cm, <100> orientation, and thickness of 140 μm. The process flow for the fabrication of the cell is given in Fig. 1. The substrate initially undergoes a standard cleaning procedure [25] and single-sided texturization using tetramethylammonium hydroxide (TMAH) for light trapping [26]. After texturization, the intrinsic (i-layer) a-Si:H is deposited on both sides of the wafer using a direct current (d.c.) PECVD system. The i-layer deposited at 200 °C at a rate of ~1 Å/s has a thickness of 10 nm, and the detail of its deposition is given in our previous work [27,28]. The front anti-reflection coating (ARC) consists of a bilayer of amorphous silicon nitride (a-SiN_x:H or SiN) and amorphous silicon carbide (a-SiC:H or SiC) which is deposited after the i-layer. The a-SiN_x:H is deposited at a rate of ~2.5 Å/s in a separate rf-PECVD chamber at a temperature of 300 °C, pressure of 1000 mTorr, and power of 40 W. Since the electrode area of the chamber is 1188 cm^2 (33 cm × 36 cm), so the power density for a-SiN_x:H deposition is 34 mW/cm^2. The a-SiN_x:H deposition uses silane (SiH_4), hydrogen (H_2), and ammonia (NH_3) as precursor gases in the ratio 3:10:6 respectively. This is followed by a a-SiC:H deposition at 200 °C using dc-PECVD at a pressure of 700 mTorr and current of 60 mA. For this deposition SiH_4, H_2 and methane (CH_4) are used as precursor gases at a flow rate of 5 sccm, 60 sccm, and 28 sccm respectively. The Front i-layer/a-SiN_x:H/a-SiC:H stack is optimized for superior passivation from the i-layer combined with anti-reflection properties of a-SiN_x:H, whereas a-SiC:H acts as an etch barrier for the downstream processes.

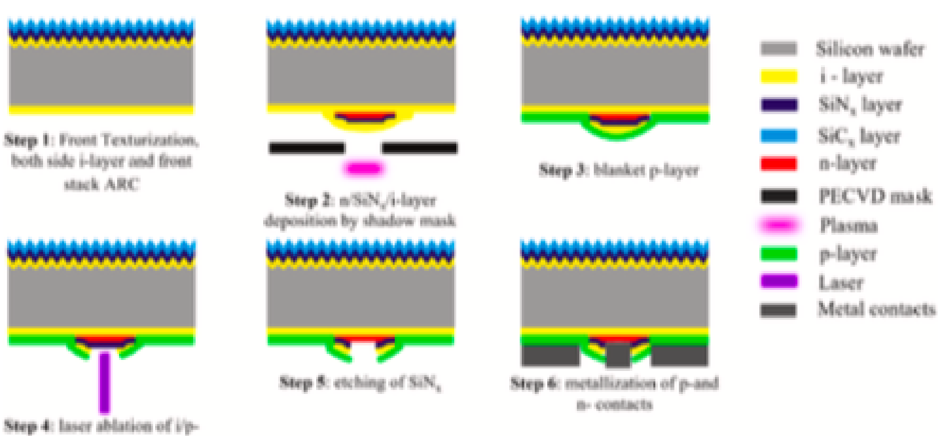


Fig. 1. Schematic of process steps to fabricate PMLP IBC solar cells.

Next, we deposit a stack of n-layer [a-Si:H(n)], a-SiN_x:H, and i-layer through the shadow mask of n-finger. The blocking shadow mask is in intimate contact to the samples to minimize the gap between the sample and the mask. The n-layer [a-Si:H(n)], a-SiN_x:H, and i-layer has thicknesses of 50 nm, 160 nm, and 10 nm respectively. The n-layer [a-Si:H (n)] is deposited at 250 °C, 1.75 Torr, and a current of 60 mA using 20 sccm SiH_4, 120 sccm H_2 and 10 sccm phosphine (PH_3) [2% diluted in hydrogen]. The capping a-SiN_x:H over n-finger is done at a similar condition as the front ARC except the SiH_4:H_2:NH_3 ratio is 6:17:10. This change is to make the a-SiN_x:H layer a better etch barrier by changing its stoichiometry as against the front a-SiN_x:H which is only used as an ARC layer. After the stack layers, we deposit a 20 nm blanket p-layer [a-Si:H (p)] on the entire rear surface. The p-layer [a-Si:H(p)] is deposited at a temperature of 200 °C using 20 sccm SiH_4, 120 sccm H_2 and 15 sccm diborane (B_2H_6) [2% diluted in hydrogen] at a pressure ranging from 1.25 Torr to 1.75 Torr and current ranging from 60 mA to 120 mA. It is important to note that the intrinsic, p- [a-Si:H(p)] and n-layers [a-Si:H (n)] are deposited in different chambers of the PECVD system to prevent cross-contamination. The laser ablation of the i/p layer is done using either a 355 nm (Ultraviolet) or 532 nm (Green) nanosecond pulsed laser, the details of which are given elsewhere [29,30]. After the laser ablation, the exposed a-SiN_x:H is etched using 2% hydrofluoric acid (HF). Following the etch, the interdigitated p and n fingers are metalized with 3 μm Aluminium (Al) by electron beam (e-beam) evaporation using a shadow mask aligned with the n- and p-fingers. The contact resistivity of the Al/a-Si:H interface is reduced by a heat treatment at 150 °C for 15 min in ambient air which results in interdiffusion of Al & Si forming partially crystallized aluminium silicide alloy at the interface.

2.2. Characterization

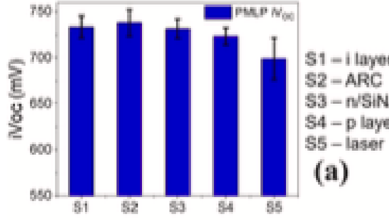
At each stage of the device fabrication, the injection level dependent minority carrier lifetime (τ_{eff}) was measured using Sinton quasi-steady-state photoconductance (QSSPC) tool WCT-100 which helps understand the loss in passivation quality. The implied V_{OC} (iV_{OC}) at 1-sun illumination estimated from τ_{eff} is used as the figure of merit to determine passivation quality. The iV_{OC} provides an estimate of the upper limit of V_{OC} after each step of the process. EL measurements were taken using a germanium-silicon (Ge-Si) detector held at −80 °C with a thermo-electric cooler. The sample was placed on a vertical stage that could move along the X–Y direction. To provide the injection current, a source meter was used in a 4-wire mode. The camera and stage were placed inside a dark box with cooling fans housed in the camera enclosure to ventilate the dark box. In addition to the dark frame subtraction provided by the camera, a dark frame (no current image at the same EL condition) was subtracted from each image to further eliminate the dark signal. The emission intensity for each image was normalized to exposure times, so that images could be compared directly. The detector array size is 480 × 640 pixels, and the resolution of the system is ~25 μm. The camera sensitivity is in the 300–1600 nm wavelength range. EL images were taken without active thermal control of the sample. PL measurements were taken using a 690 nm continuous wave (CW) laser diode with a power of 30 mW. The laser beam diameter is about 1 mm, and a beam expander has been coupled to the laser, so the beam diameter roughly covers a region of 3 mm on the device. A long pass filter (830 nm) was placed between the sample and detector to ensure only emission light from the device reaches the detector and to prevent any laser light that might be reflected off the solar cell from reaching the camera. The current density-voltage (J-V) characteristic of the device was measured using a class AAA AM1.5 simulator from Optical Association Incorporated (OAI). The cells were measured under a light intensity of 100 mW/cm^2 with the cell temperature maintained at 25 °C using a cooling fan underneath the stage for standard testing conditions (STC). A Keithley source-meter (SMU 2400) was used as the voltage source as well as the current measurement unit. An in-depth analysis of the solar cells was carried out using the diode analysis described elsewhere [31].

3. Results and discussion

3.1. Fabrication of Plasma Masked Laser Processed (PMLP) HJ-IBC solar cells

To design an IBC architecture which could be commercially scalable, it is important to eliminate complex steps like lithography and avoid using resists that could contaminate the active layers. We propose an architecture in which the interdigitated pattern of doped layer is achieved by using shadow masks during the PECVD process, and the contacts are formed by creating an opening on the fingers by laser ablation. We used d.c. PECVD method to deposit our intrinsic and doped layers, this has a commercial advantage due to its simpler design assisting in easier industrial implementation and does not need a complex impedance matching network. This combined with a non-lithographic masking step for patterning and laser ablation for contact formation assists in low-cost, high-throughput, manufacturable silicon heterojunction IBC solar cells. The schematic of one possible process flow and the resulting architecture is given in Fig. 1. We call this proof-of-concept structure the 'Plasma Masked Laser Processed' (PMLP) IBC solar cells. The process involves one shadow mask step for making n-layer [a-Si:H(n)] pattern and one self-alignment step to deposit the metal using an interdigitated metallization mask. Though in this work we have used wet etching method to form contacts after laser ablation to demonstrate the proof-of-concept, it could be replaced by dry etching techniques which are more amenable to low-waste manufacturing [32]. Other groups have already shown the use of Nitrogen trifluoride (NF_3)/Argon (Ar) [14] and sulfur hexafluoride (SF_6) [33] to etch a-Si:H. The process step for PMLP IBC solar cells starts with single-sided texturization of the front, deposition of a-Si:H on both sides of the substrate followed by a deposition of Anti Reflection Coating (ARC) on the front. From Fig. 1, the second step involves the deposition of a-Si:H (n), a-SiN_x:H and a-Si:H fingers using a shadow mask. This is followed by the third step of blanket a-Si:H (p) deposition on the entire rear side. Later in the text, we will introduce an additional etch step between steps 2 and 3, the details of which will be elucidated in the result section. Step 4 consists of laser ablation of the i/p layer over the n-finger followed by the etching of the exposed a-SiN_x:H layer. The last step involves metallization of the p and n fingers using a self-aligned mask. Thus, from the process flow shown in Fig. 1, we can see that a combination of in-situ masking during PECVD combined with laser ablation can result in a simple non-lithographic, high throughput, and industrially relevant method for HJ-IBC cells.

To understand the loss of passivation due to each step of the process flow we have measured the iV_{OC} of 8 cells before metallization as shown in Fig. 2(a). The iV_{OC} of 733 ± 12 mV after both side i-layer passivation increases to 738 ± 14 mV after adding the high temperature a-SiN_x:H (ARC) deposition process that acts as an annealing step. After deposition of the rear surface n/SiN/i finger through the shadow mask of width 350 μm we see a slight drop in iV_{OC} to 732 ± 11 mV. A further drop in iV_{OC} to 723 ± 9 mV is observed after the p-blanket [a-Si:H(p)] layer deposition due to passivation degradation phenomenon observed previously [34]. Another drop in iV_{OC} happens after the laser ablation layer where the iV_{OC} drops to 699 ± 22 mV. The large variation in standard deviation for this step arises from the fact that different laser conditions were applied to optimize the iV_{OC} loss for our initial trials. A large iV_{OC} drop (> 20 mV) has been considerably reduced to < 5 mV by optimizing the laser conditions. However, despite having cells which gave an iV_{OC} > 700 mV before metallization, the final cells after metallization only had a V_{OC} of ~300–400 mV, as shown in Fig. 2(b) by plotting J-V curve of a representative cell. We have previously shown [35] that V_{OC} drops significantly due to an increase in interface defect states (D_{it}) and therefore an increased surface recombination velocity (SRV) indicative of poor passivation. To make sure the severe drop in V_{OC} after metallization does not come from loss in passivation, we etched the Al contacts



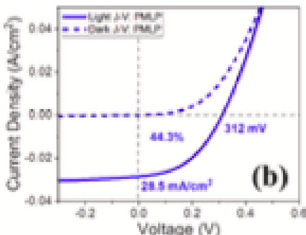


Fig. 2. (a) iV_{OC} at different steps of PMLP HJ-IBC fabrication process flow namely – after both side i-layer (S1), front ARC (S2), rear masked n/a-SiN_x:H/i layers (S3), rear p-layer [a-Si:H(p)] (S4) and after laser ablation (S5) (b) Light and Dark J-V characteristics of PMLP HJ IBC solar cell.

of the cells having low V_{OC} and re-measured their iV_{OC}. We found that the same cells which gave low V_{OC} after metallization had iV_{OC}>700 mV close to their initial iV_{OC} values before metallization. The results of this study are elaborated in detail below.

In order to understand the origin of the low V_{OC} in PMLP HJ-IBC solar cells, we performed a study in which the implied V_{OC} (iV_{OC}) of the devices were measured using a Sinton WCT-100 QSSPC tool before and after metallization. To confirm that the low V_{OC} was not due to surface damage caused during the e-beam evaporation of aluminium (Al) for metal contacts, a few PMLP HJ-IBC cells had the Al etched off and iV_{OC} was remeasured. The first measurement involved measuring the iV_{OC} of the devices just before metallization after all the processing steps including laser ablation and silicon nitride (SiN) etch. The second measurement involved measuring the actual V_{OC} of the device after metallization. Finally, for the last measurement Al was etched off and the iV_{OC} of the devices were remeasured, the results are shown in Table 1. The iV_{OC} values from Table 1 show that the PMLP HJ-IBC devices recovered to nearly the original value of their iV_{OC} before metallization, over 300 mV higher than the measured V_{OC}. This confirms that the low V_{OC} problem is not due to recombination or poor passivation due to surface damage, but due to the injection of current at V_{OC}.

This result indicates that the low V_{OC} observed in the final metalized devices was not due to a loss in passivation.

To understand this poor performance and confirm the above hypothesis, we measured the EL and PL of one of the cells, to probe a V_{OC} loss (ΔV_{OC}) of −400 mV, as shown in Fig. 3. For PL imaging we selected a cell having a high iV_{OC} of 739 mV after i-layer deposition but showed a poor final V_{OC} of approximately 400 mV after metallization. For the PL imaging, we have etched the metal contacts of the final devices and used PL as a method to investigate any loss of passivation during the contact formation. The PL image in Fig. 3(a) after the rear metal etch shows high emission spatially over most regions of the device, corresponding to the high implied V_{OC} we observed while remeasuring the iV_{OC} of the devices after etching the metal contacts. The non-uniformity in the PL comes from the limitation in the beam expander to expand the laser light onto the entire cell area. This verifies that the loss of V_{OC} is not due to loss of passivation, as for example, some have reported it can come from the sputtering damage due to ion bombardment or the radiation damage during the e-beam deposition of contacts [36,37]. After device processing, with the proposed non-lithography technique, the actual measured V_{OC} dropped to <400 mV (>45% decrease in V_{OC}), much less than the implied V_{OC}. The EL emission shown in Fig. 3(b) has

Table 1
iV_{OC} and V_{OC} of PMLP HJ-IBC solar cells at different stages of processing.

Sample	iV_{OC} before metallization (mV)	Measured V_{OC} after metallization (mV)	iV_{OC} after metal etch (mV)
Device 1	710	366	705
Device 2	720	355	711

non-uniform low intensity where the reduced intensity could either be due to non-radiative recombination of minority carriers or a barrier to injection for minority carriers. For this EL study, the minority carriers (holes) were injected through the p-strip busbar while the majority carriers (electrons) were injected through the n-strip busbar, both at the back. Holes then recombine with electrons in the bulk of the device and photons are emitted. EL which is equivalent to the rate of spontaneous emission is directly proportional to the minority carrier concentration in the device [38]. The pattern of non-uniform EL over the p-strip (wider) and the n-strip (narrower) corresponds to the minority carrier concentration in the corresponding regions of the device. The n-fingers appear darker due to a phenomenon called electrical shadowing [39] where the minority carriers generated over the n-fingers get recombined with the majority carriers resulting in no emission. Also, the EL injection current was 160 mA/cm^2 (− 4 times J_{SC} of the device) to obtain a visible emission profile across the active cell area. For well-behaved devices, considerable emission is readily obtainable at an injection current that is below the J_{SC} of the device. The need to go to a higher injection current is due to the very low V_{OC}, which is indicative of either the high non-radiative recombination rate or barrier to minority carriers [40].

3.2. Back Junction test structures with rear IBC pattern to understand the origin of low V_{OC} in PMLP architecture

From the discussion above, we can infer that the loss of V_{OC} does not originate from the loss of passivation resulting from a high surface recombination velocity. This is reinforced by the PL images which show high intensity even after etching the metal. To probe this loss, we look into the fabrication process and find that during the deposition of the doped layer using a shadow mask, there is a lateral spread of the doped layer into the emitter region shaded by the mask, as can be visualized from the schematic in Fig. 4(a). To verify this, we have taken the optical image of the doped layer deposited on glass with a thickness of −50 nm as seen in Fig. 4(b), and a thickness profile of this leakage is shown in Fig. 4(c).

In the PECVD reactor, the precursor gases enter the chamber through the showerhead below the substrate holder, and the plasma is generated in the gap between the two. Because of this geometry, the deposition is upwards on the substrate, which is covered using a shadow mask. The shadow mask is mechanically kept in contact with the wafer, and there is no additional force that holds the mask to the wafer. Since the shadow mask under the wafer is suspended by gravity, the open ends of the mask near the busbar are pulled in the downward direction resulting in a greater spread of the leakage near the busbar as seen in Fig. 4(b). To overcome this bottleneck, we even substituted the mechanical mask with a magnetic mask however, plasma leakage was observed at the edges of the patterned deposition by this method as well. The silicon wafers we use to fabricate cells are not mirror-polished and have a high surface roughness of the order of a few microns which results in a gap between the shadow mask and the substrate, for the plasma species to percolate. As we can see in the graphic illustrated in Fig. 4(a), the plasma

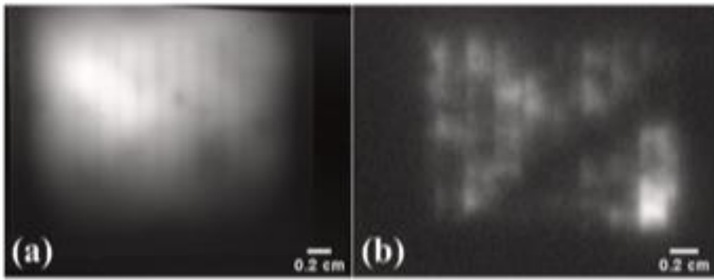


Fig. 3. (a) Photoluminescence (PL) image of PMLP cell after metal etch that had an initial iV_{OC} = 739 mV after i-layer deposition (b) Electroluminescence (EL) image of PMLP cell with a V_{OC} = 400 mV at an injection current of 160 mA/cm^2.

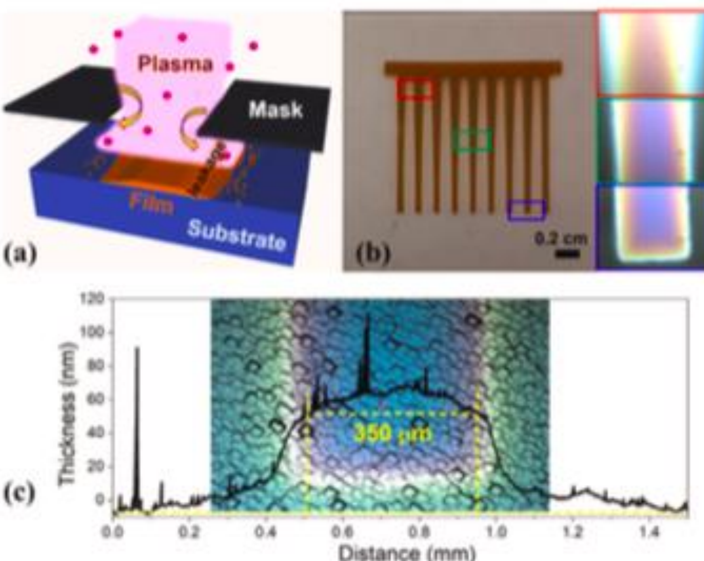


Fig. 4. (a) Graphical illustration of plasma leakage through the edge of the shadow mask during the PECVD process (b) Optical micrograph of n-layer [a-Si:H(n)] deposited through n-finger shadow mask on glass with zoomed inset image of different regions of the finger showing the extend of plasma leakage. The brownish film is deposited through the openings in the shadow mask, the bottom part of the finger which is attached to the mask has more defined pattern (blue square) as against the top part, where the tip of the mask is free floating (red square). (c) Thickness profile of the patterned doped layer showing leakage superpositioned over the optical image of n-finger on silicon.

radicals seep under the edges of the mask between the gap due to the imperfect contact, leading to the spreading of the doped layer under the masked region, resulting in n-type contamination along the covered p-strip. To understand the spreading of the doped layer, we deposited the doped amorphous film through the same mask on a glass sample, as shown in Fig. 4(b). We can observe from the optical image that the spread of the film is wider towards the busbar whereas it tapers towards the bottom. Also, Hartenstein et al. has observed similar spreading of the dopant radicals [33] while shadow masking due to the low sticking coefficient of the doped species on the growth surface. This phenomenon along with the leak due to the gap in the mask, give rise to the spreading of the radicals resulting in a Gaussian tail as observed from the profile of the deposition along the edge of the films in Fig. 4(c).

In order to investigate if the origin of loss in V_{OC} of the device stems from plasma leakage, we fabricated back junction (BJ) solar cells having p-type a-Si:H emitter on the rear side of the wafer. Along with the reference BJ cell, we also fabricated test structures that had the n-finger pattern similar to the PMLP structure to mimic the rear side of PMLP IBC structures, as shown in Fig. 5(a). The intrinsic and doped layers used for this study have the same deposition conditions as our PMLP cells. We fabricated 2 batches of BJ test structures, one in which the cells underwent plasma leak etch (PLE) and the other had no PLE. For the PLE samples, etch was performed after the a-Si:H(n)/a-SiN_x:H finger deposition through the mask to remove the plasma leakage before the deposition of p-layer [a-Si:H(p)]. The PLE of BJ cells having n-finger leak of a-SiN_x:H/n-layer [a-Si:H(n)] is done by dipping it in hydrofluoric acid (2% HF) to remove a-SiN_x:H leak followed by an approximately 5 min etch either in potassium hydroxide (45% KOH) or 25% TMAH to remove n-layer [a-Si:H(n)] leakage. Additionally, a non-optimized BJ cell with the same condition having no rear pattern was fabricated for reference, as shown in Fig. 5(a). The reference cell has 10 nm i-layer on both sides followed by 30 nm n-layer at the front and 20 nm p-layer at the back. This is followed by 80 nm ITO layer by sputtering on the top as ARC. Then the cells are metalized with 50 nm Nickel with 3 µm Al grid at the front and 500 nm Al blanket layer at the rear. The front layer stack is kept the same between the reference BJ cell and BJ test structures with n-finger patterning described above. The schematic of the rear patterned BJ test structures and the reference cell can be seen in Fig. 5(a). The dark and light J-V characteristics of the different cells are given in Fig. 5(b). The J-V plot shows BJ cells having no PLE has the worst performance

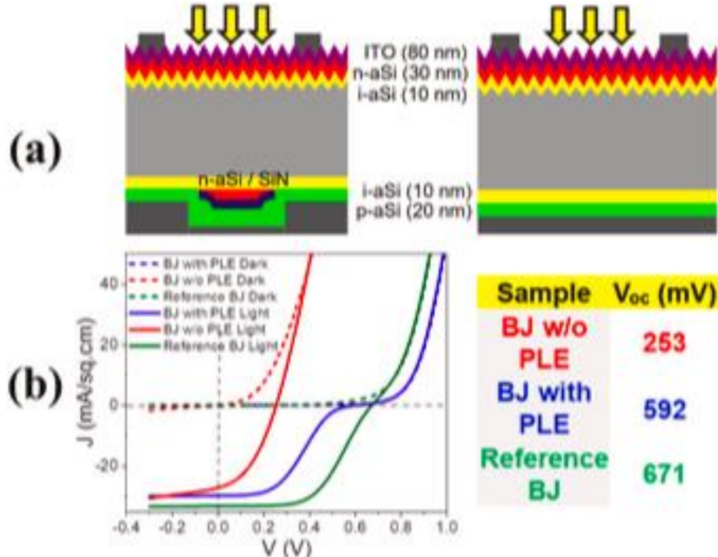


Fig. 5. (a) Schematic of back junction (BJ) test structures with and without rear n-finger pattern (b) Dark and Light J-V characteristics of 3 different BJ cell structures – reference (green), with (blue) & without (red) plasma leak etch (PLE).

with a V_{OC} of 253 mV. But after PLE the V_{OC} improves considerably to 592 mV. Though the V_{OC} shows improvement, nevertheless, the cell has poor performance due to the 'S-shaped curve' which originates in a Schottky rectifying barrier typical in HJ cells where the extraction of carriers is limited due to the barrier. As against this, the reference cell had a V_{OC} of 671 mV, which is close to the iV_{OC} of ~700 mV for the cells after doped layers. This difference arises from the non-optimized conditions of the reference BJ cell, which can be clearly seen in the J-V characteristics. Nevertheless, the trend shows the severity of the effect of plasma leakage on the V_{OC} of the device and the overall performance in general.

To better understand the performance of these BJ test structures we have analyzed their EL imaging. In this experiment, the BJ reference cell has a p-blanket [a-Si:H(p)] layer at the back and an n-layer [a-Si:H(n)] at the front. Whereas the BJ test structures have rear n/SiN fingers by masked deposition with a blanket p-layer [a-Si:H(p)] over it, thus forming interdigitated p and n doped fingers at the rear similar to the PMLP IBC rear side. The reference BJ cell in Fig. 6(a) shows uniform and high EL emission image corresponding to high optical and electronic properties [41]. The EL emission in Fig. 6(a) shows no major localized regions where emission is lower due to high non-radiative recombination of minority carriers. Unlike the IBC device discussed in the previous section, the p-region in the BJ reference cell in Fig. 6(a) makes up the whole rear side; hence EL emission is uniform. In the all-back junction test structures in Fig. 6(b) and (c), minority hole carriers are injected through the back p strip and majority carriers are injected through the front metal grids into the front ITO and then into the base region of the device. The EL emission in Fig. 6(a) is measured under an injection current comparable to the J_{SC} of the device which indicates this device has better performance, compared to the PMLP IBC devices described in Fig. 3(b) which had poor performance. However, the EL of the BJ device with the a-SiN_x:H/n-layer [a-Si:H(n)] strips without etching the plasma leakage (no PLE) in Fig. 6(b) shows significantly lower emissions than the reference BJ device discussed previously in Fig. 6(a). Injection

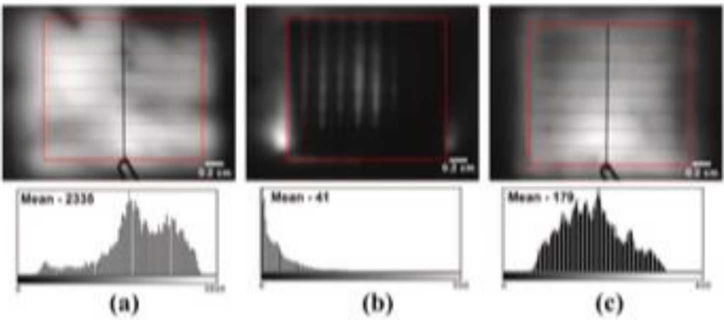


Fig. 6. Electroluminescence images of back junction solar cells along with their intensity histograms for (a) Reference with no rear pattern at 28 mA/cm^2 injection current (b) cell with no plasma leak etch (no PLE) at 400 mA/cm^2 injection current (c) cell with PLE of the rear pattern at 28 mA/cm^2 injection current. The red square shows the active area defined by the ITO on front. The grid pattern on front is also visible since it blocks EL emission.

current of EL had to be increased by more than an order of magnitude to achieve an EL image with high enough contrast to be compared to the EL of the reference device. The EL of the reference device in Fig. 6(a) is measured at 28 mA/cm^2 (70 mA) which is comparable to its J_{SC} of 32.1 mA/cm^2. J_{SC} of the device in Fig. 6(b) without PLE is 23.6 mA/cm^2, while its injection current was 400 mA/cm^2 (1 A). Thus, we can infer that it takes ~14 times more injection current for the BJ cell without PLE as compared to a reference BJ cell to get images of similar contrast. Also, the EL emission for the BJ cell without PLE is non-uniform as can be seen in Fig. 6(b). It is interesting to see the pattern of EL observed in Fig. 6(b) resembles the pattern seen in Fig. 4(b) thereby confirming that its the region of plasma leakage which acts as a region of low emission. It is important to note that the n-finger showing leakage pattern in Fig. 6(b) is flipped as compared to Fig. 4(b) thus it is the i/n region that has lower EL emission. The low EL emission indicates either a region of high recombination or a barrier to injection of minority carriers. Thus, it is plausible that the plasma leakage results in a barrier to injection causing V_{OC} loss in the device. This barrier can cause the minority carriers injected into the back p-strip to not be able to recombine radiatively with the majority carriers in the bulk of the device. For the case where the plasma leakage has been etched in Fig. 6(c), EL shows a much more uniform emission as compared to no PLE with no reduced intensity. The possible barrier to minority carrier injection seems to have been significantly decreased by etching the leakage. Emission is mostly uniform and hence shows that the detrimental effect of plasma leakage is reversible to a considerable extent by etching. The EL emission after PLE is significantly increased as compared to no PLE. The EL in Fig. 6(c) is measured at an injection current of 28 mA/cm^2 that is comparable to the J_{SC} of the device and is the same current used to measure the reference BJ cell. The EL emission in Fig. 6(c) shows slight regions to the side where the etching might not have been uniform and the effective EL emission compared to that of the reference BJ cell is about ~8%. We speculate that EL emission is not restored to initial values as the reference BJ cell due to the formation of a barrier between the a-Si:H p- and i-layers due to the remnant plasma leakage after etching which can be deduced from the S-shaped light J-V curve seen in Fig. 5(b). This barrier will hinder the injection of minority carriers and will result in a decreased EL emission compared to the reference cell emission. Both reference BJ and BJ with PLE devices show similar contrast for an injection current of 28 mA/cm^2 as against BJ without any PLE showing poor contrast even at an injection of 400 mA/cm^2. This hints at the role of plasma leakage as a barrier to injection. Thus, the EL results are indicative of the fact that plasma leakage is detrimental to device performance which can be improved by etching the leakage.

The dark J-V analysis of the test structures discussed in Fig. 5 is presented in Table 2. It shows that for a BJ cell that has not undergone PLE has high series resistance (R_S) of 2.12 Ω cm^2 which decreases to 1.13 Ω cm^2 after PLE but does not reach as low as the reference cell having R_S of 0.89 Ω cm^2. We can also find that BJ cells without PLE have shunt paths due to the n-leakage extending into the p region resulting in R_{Sh} of 0.18 kΩ cm^2 which is more than two orders of magnitude smaller than 20.8 kΩ cm^2 after PLE. However, R_{Sh} of reference remains much higher at 140.5 kΩ cm^2 hinting at further scope of improvement to optimize the etching to remove any shunt effect. The recombination current (J_0) also shows considerable improvement after PLE, from 0.94 mA/cm^2 to 1.8 × 10^{-6} mA/cm^2, further reinforcing the significance of removing plasma leak to obtain better device performance. Thus, the diode analysis along with the EL results highlights the deleterious effect of plasma leakage and supports our argument that eliminating process-induced plasma leak can significantly improve device performance by reducing resistive losses, injection barriers, and shunt paths.

Table 2
Dark J-V analysis of BJ test structures.

Sample	R_s (Ω.cm^2)	R_{sh} (Ωcm^2)	J_0 (mA/cm^2)
BJ with PLE	1.13	20829	1.80 × 10^{-6}
BJ w/o PLE	2.12	189	0.94
Reference BJ	0.89	140450	2.27 × 10^{-4}

3.3. Process optimization to mitigate the losses due to plasma leakage in the fabrication of HJ-IBC cell architectures

Though the plasma leak can be etched either by a dry or wet etching process, in this work, we have focused on wet etching methods. After understanding the effect of plasma leak removal in the test structures we fabricated a series of PMLP cells with and without plasma leak etch. This additional step of etching plasma leakage has been introduced between step 2 and step 3 shown in Fig. 1. In our initial trial of etching the leak, we used a mixture of 10% HF with Nitric acid (HNO_3) in the ratio 1:100 as a single step etch. We avoided the KOH etch method used for our test structures to avoid metal ion contamination in the IBC cells. However, the HF + HNO_3 mixture had a high etch rate limiting the etch time to ~5 s making it difficult to have a controllable etch process. Moreover, the etch was non-uniform and resulted in major constraints to obtaining a reproducible etch profile. To overcome both of these limitations, we performed a 'triple etch' method as against a 'single etch'. After forming the n/SiN/i stack n-fingers through the masking step, we first etch the i-layer leak using a short 5% TMAH etch for 5 min, followed by a 2% HF etch for 150 s to remove the a-SiN_x:H leak. This is followed by a longer 5% TMAH etch for 15 min which assists in the complete removal of the rear i-layer along with the n-layer [a-Si:H(n)] leak. Then a new i-layer is redeposited as a blanket layer to re-passivate the rear before depositing the blanket p layer in step 3. Since 5% TMAH has a slow etch rate, it helps in developing a controllable process for leak removal. From Fig. 7 it can be observed that the triple etch method results in a uniform etch profile and results in sharper edges of the n-finger. The light and dark J-V results of the fabricated PMLP cells are shown in Fig. 8. We can observe that even a single etch step introduced in the fabrication process can considerably improve the cell performance. The cell with no plasma leak etch has a V_{OC} of 312 mV consistent with the unetched baseline cell in Fig. (2). The V_{OC} improves to 537 mV after 'single etch' step despite having a non-uniform etch profile. With a more controllable and defined 'triple etch' method the device shows further improvement in V_{OC} to 637 mV. The trend in the increase in V_{OC} after the leak etch in Fig. 8 is in agreement with the improvement in V_{OC} observed in BJ test structures after plasma leak etch thereby verifying the detrimental effect of process-induced leak and how its removal can significantly improve device performance.

The dark and light J-V curves of the cells from Fig. 8 were analyzed. The dV/dJ versus 1/J plot of the PMLP cells after etch in Fig. 9 shows a linear trend in the dark which is expected for a single diode. However, in the light we see a peak indicating that there is a barrier to hole collection which validates our hypothesis presented during the EL results. Such inflection attributed to blocking behavior in solar cells has been reported in detail elsewhere [31]. Also, the parameters extracted from the diode analysis in Table 3 show that the etch process helps in reducing the shunt paths in the IBC cells due to the plasma leak. The R_{sh} in the dark improves considerably from 0.49 kΩ cm^2 for cells with no etch to 3.3 kΩ cm^2 for single etch cells to 5.4 kΩ cm^2 for triple etched cells. The etch also reduces the series resistance by reducing the resistive losses coming from the dielectric plasma leak in the current collection path. J_0 also considerably decreases due to etching the plasma leak, hinting at reduced recombination loss. Thus, we can see that plasma leak removal can improve the V_{OC} of the devices by > 300 mV, though these devices need further optimization to improve the uniformity of etch either by dry etch methods or developing alternative masking methods to reduce V_{OC} loss and obtain values close to the implied V_{OC} of ~700 mV after all the process. It is also interesting to note that the laser process for contact formation is a viable approach for the fabrication of HJ devices as the iV_{OC} only decreased by <5 mV. In a subsequent paper, simulations have been performed of the band alignment to identify barriers and will

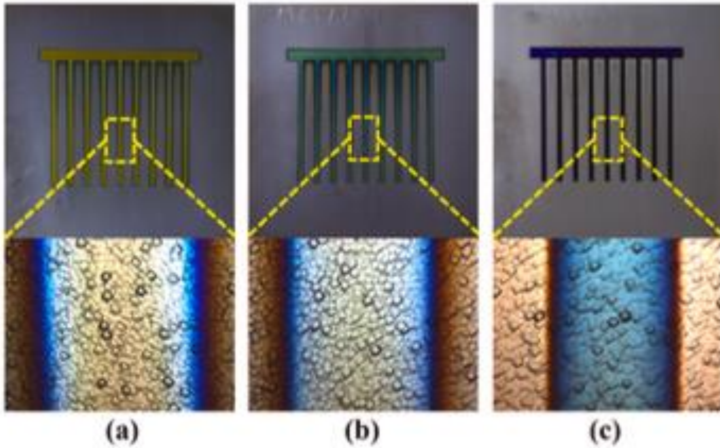


Fig. 7. Optical image of n-finger consisting of n/SiN/i-layer stack along with the magnified images of the finger showing the leak removal process during triple etch method (a) before etch (b) after 5% TMAH etch (c) After 5% TMAH + 2%HF + 5% TMAH triple etch. We can see the gradual progression of leak removal and sharper edges of the fingers after each step of the process along with a reduction in film thickness.

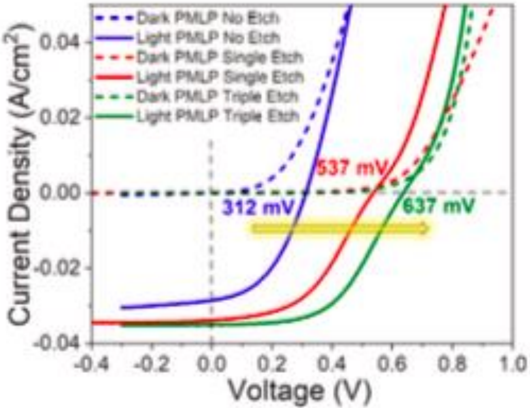


Fig. 8. Light and dark J-V characteristics of PMLP cells under no etch, single etch and triple etch.

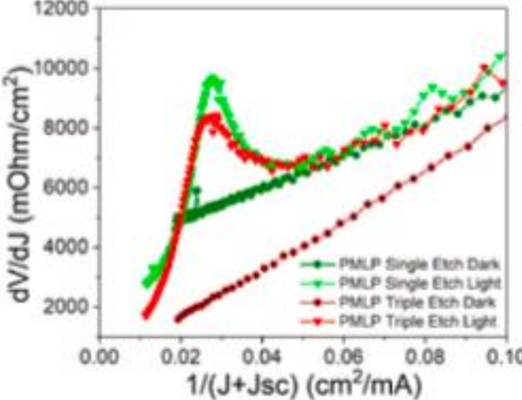


Fig. 9. Plot of the first derivative of voltage with respect to current density (dV/dJ) versus the inverse of current density (1/J) for both 'single etch' and 'triple etch' PMLP IBC cells in light and dark.

present the results of applying these methods to improve the performance of actual IBC-HJ cells.

4. Conclusion

In summary, we have developed a novel non-lithographic process for heterojunction IBC architecture using in-situ shadow masking combined with laser ablation as a path towards a low-cost manufacturable process to replace lithography with an industrially-friendly process. Our initial results showed poor V_{OC} of < 400 mV. Investigation using a combination of minority carrier lifetime measurements, photoluminescence and electroluminescence revealed the loss in V_{OC} does not come from the loss of passivation. To investigate the origin of this loss, we designed and fabricated back junction cells with the same rear architecture as our IBC cells. A detailed characterization of these devices revealed the loss originates in the plasma leakage during the shadow masking process while depositing the patterned doped layer by PECVD. The chemical etching of the leakage considerably improved the V_{OC} as well as reduced shunt channels and resistive loss in the device. Using the insights from these results as a guideline, we fabricated HJ IBC cells incorporating the plasma leak chemical etch step. We developed a controllable uniform etch method which significantly improved the V_{OC} of the device by >300 mV from ~300 to 637 mV. Thus, we showed the proof-of-concept of a novel manufacturable process which can be commercially viable wherein mitigating the process-induced losses can improve the device performance. We plan to further optimize this process to fabricate high-efficiency heterojunction IBC solar cells having higher V_{OC} in our future

Table 3
J-V analysis of PMLP HJ-IBC cells in dark conditions.

Samples	R_{sh} (Ω.cm²)	R_s (Ω.cm²)	J_0 (mA/cm²)
PMLP (no etch)	485	3.81	7.00×10^{2}
PMLP (single etch)	3344	2.48	5.13×10^{4}
PMLP (triple etch)	5399	0.89	3.10×10^{3}

work.

CRediT authorship contribution statement

Anishkumar Soman: Writing – review & editing, Writing – original draft, Visualization, Validation, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **Ujjwal K. Das:** Writing – review & editing, Conceptualization, Formal analysis, Funding acquisition, Methodology, Project administration, Supervision. **Nuha Ahmed:** Data curation, Formal analysis. **Arpan Sinha:** Investigation, Validation, Writing – review & editing. **Mool C. Gupta:** Writing – review & editing, Conceptualization, Funding acquisition, Resources. **Steven S. Hegedus:** Supervision, Resources, Project administration, Methodology, Funding acquisition, Formal analysis, Conceptualization, Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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Appendix A. Supplementary data

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