A Microwave On-Wafer Probe with Micromachined Replaceable Tip

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The thesis

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Abstract

On-Wafer testing is a critical part of the integrated circuit industry and an important technique for research and development. On wafer probes allow for circuit characterization prior to dicing, or mounting. Defective circuits can be removed prior to packaging, with the result of reducing time and costs. Probe stations can be automated, allowing for a large number of measurements to be done efficiently and quickly. On wafer probes can have DC bias capabilities, and can provide accurate RF measurements of integrated circuits with proper calibration.

This work presents the design, simulation, and measurement of a 0-50 GHz on wafer probe with a replaceable tip. The replaceable tip provides the ability to change the probe to a different pitch, or replace a damaged probe tip. Without this feature, a new probe would need to be purchased, or sent to the manufacturer for repair. The replaceable tip is realized using silicon micromachining techniques.

Contents

1 Introduction

The RF and microwave on wafer probe market consists primarily of two major companies, GGB Industries Inc.,and Cascade Microtech Inc. [1, 2]. These companies offer on-wafer probes operating to 60 GHz with coaxial inputs, and probes operating in wave standard waveguide bands from 33-1,100 GHz. Coaxial cables and connectors are limited by an upper cutoff frequency, which is the point where the first higher order mode is able to propagate. The lowest order mode on a coaxial line is a TEM wave. Higher order TE and TM modes are possible, and the wavelengths of the TE modes can be found with the approximate formula:

$$\lambda_c \approx \frac{2\pi}{n}\left(\frac{r_o + r_i}{2}\right),\ n = 1, 2, 3, ... \tag{1}$$

[3]

Where $r_o$and r_i are the outer and inner radii of the coaxial cable. The lowest-order TE mode (first higher order mode) will propagate at $\lambda_c$when n=1 in formula 1 [3]. To extend the operating band, the dimensions of the coaxial line can be made smaller, however commercially-available coaxial connectors generally range from 1.0-3.5 mm diameter. Shrinking the coaxial cable is limited by loss from the skin effect. At higher frequencies the skin depth is smaller, which causes current crowding leading to increased resistance [3]. For 1.0 mm coax, 110 GHz is the maximum frequency where higher order modes can be avoided. Beyond 110 GHz, rectangular waveguide is used,

where the dimensions of the waveguide can be scaled to provide single mode operation to the terahertz range. Waveguide probes are available down to WR22 (33-50 GHz) as well. In addition to having an upper cutoff frequency, waveguide designed for single mode propagation has a lower cutoff frequency where a half wavelength equals the length of the broad wall of the waveguide. However, because rectangular waveguide cannot support a TEM mode, it does not reach DC and therefore a separate DC bias must be applied 1.

1.1 Micromachined On-Wafer Probes

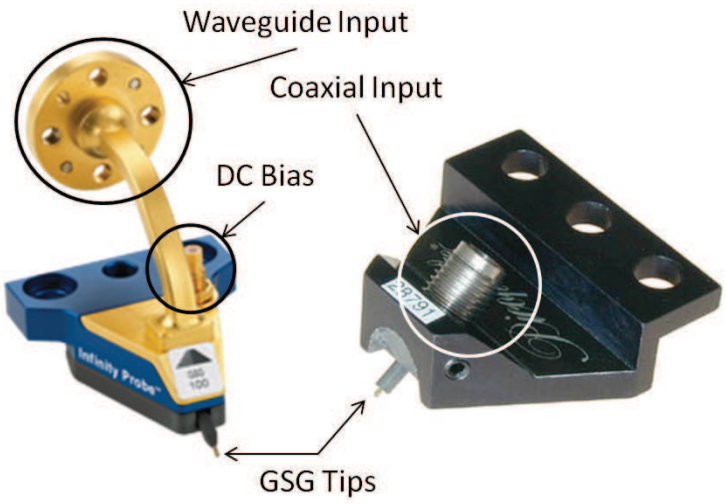

Figure 1: (Left) Cascade Infinity Probe[2] (Right) GGB Model 40A [1]

A major drawback, that on-wafer probes have traditionally faced, is that after many contacts the tips may become damaged to the point where they cannot be used. A study performed by Chen found probe failure after 6,000

contacts with 15 mN of force applied. The failure is due to the displacement of the gold at the probe tips, as well as the wear and deformation of the silicon [4]. To minimize the gold displacement, different metal alloys can be used to harden the tip, including adding cobalt-hardened gold or nickel [5, 6, 4]. It is important to note that this failure mode cannot be mitigated by repairing the probe, and a new tip is required.A major issue with probes manufactured by GGB Industries and Cascade Microtech is that failure necessitates purchase of a new probe, or the probe must be sent back to the company for refurbishment. One approach to address this drawback is to engineer a replaceable probe tip. The past research by Zhang [7], Reck [7, 8], Bauwens [5], and Chen [4] on designing a micromachining process to produce submillimeter on-wafer probes, provides a foundation for realizing microwave probes with replaceable tips. Not only could removable tips be used to replace damaged tips, but they could also allow for users to change probe tip pitch to meet differing measurement needs.

The micromachined on-wafer probe developed at the University of Virginia, consists of two parts. First a probe block housing manufactured by CNC milling with precision of $\pm$ 2.5 μm provides the accuracy necessary for 1 THz waveguide channels and self aligning recesses. The recesses permit probe chips to be placed and aligned without adhesives [5]. Second, a microfabrication process for ultra-thin silicon chips is used to make the probe chips tailored to fit the probe housing. This process uses Silicon-on-Insulator (SOI) as a base material to produce chips that can have metallization on

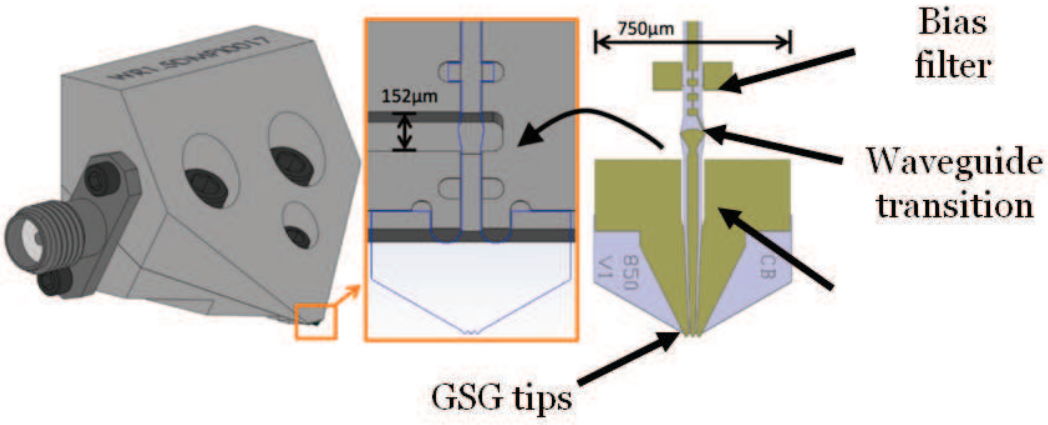

Figure 2: Micromachined Probe [5]

both sides, and be as thin as 1.6 µm [9, 10]. The micromachining process also defines the chip geometry using microfabrication techniques that allow the chip architecture to be etched within an accuracy of ± 2 µm [10].

Subsequent work following the initial demonstration of micromachined probes utilizing the SOI process, added metallized vias to connect ground planes on either side of the chip [8]. The tight tolerances of the micromachining process allow the probe chips to be dropped into the probe block, and are self aligning. The chip is then clamped in place when the two halves of the block are mated (Fig.2). The assembly process utilizes only the block and micromachined chip without the need for adhesives and using minimal hand alignment. Thick plated gold in the clamp regions ensure the chip is held tightly in place.

In contrast to the micromachined probe approach, probes manufactured by GGB Industries and Cascade Microtech employ a more complex process,

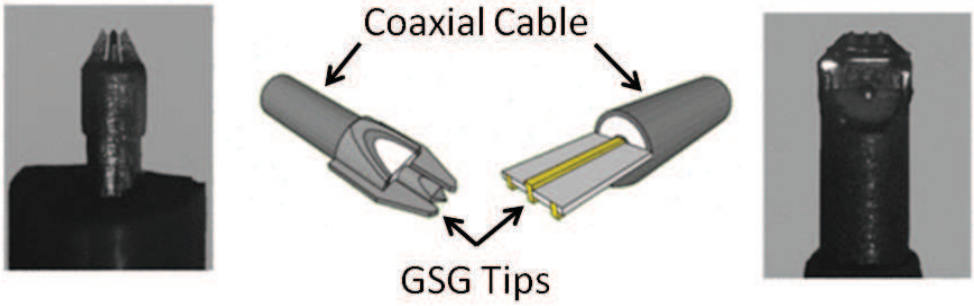

Figure 3: (Left) GGB Probe Tip (Right) Cascade Probe Tip[11]

particularly in probe tip formation. GGB probe tips utilize a coaxial transmission line, and adds ground and signal tabs made from Beryllium Copper through hand assembly. Cascade on the other hand, defines their tips with a microfabrication process applied to a polymide film. However the contact tips are attached subsequently using adhesives (Fig. 3)[11].

1.2 Outline of the Thesis

The goal of this research is to provide a proof-of-concept demonstration for a microwave probe operating from 0-50 GHz with a replaceable tip. This work, based on micromachining, addresses the issues of commercial probes in this frequency range that are not readily amenable to replacing damaged tips, and changing probe pitch. This work includes a new version of the micromachined probe developed by Zhang [7], Reck [7, 8], Chen [4], and Bauwens [5] that interfaces to a coaxial connector instead of a waveguide port. This thesis is divided into four parts.

1. Chapter 2 details the probe concept, including the design of the transitions required to engineer a low frequency micromachined probe. An RF test structure is developed to assess and verify the most critical transition in the design

2. Chapter 3 details the design of the RF transitions for the complete probe concept. This work includes a full simulation of the probe, including the SMA connector and DUT. The design of the probe block, as well as the photolithographic masks for fabricating the probe components are also included.

3. Chapter 4 describes the assembly of the probe, as well as calibration and test results.

5. Chapter 5 summarizes the work completed, and discusses possible future work that builds upon this thesis.

2 Probe Geometry and Design Considerations

Micromachined Probe Concept

GGB Industries Inc.,and Cascade Microtech Inc. both market a 0-40 GHz on wafer probe with insertionloss less than 2 dB and return loss greater than 18 dB across the band (Fig. 4) [1, 11]. A goal of this work is to replicate comparable performance with a micromachined probe featuring an easily replaceable contact tip. To accomplish this, the probe must be capable of interfacing to a commercial Vector Network Analyzer (VNA) which performs the RF measurements and applies the error correction algorithms for calibration. Network analyzers typically employ coaxial interfaces, and consequently the probe developed in this work will feature a coaxial launcher.

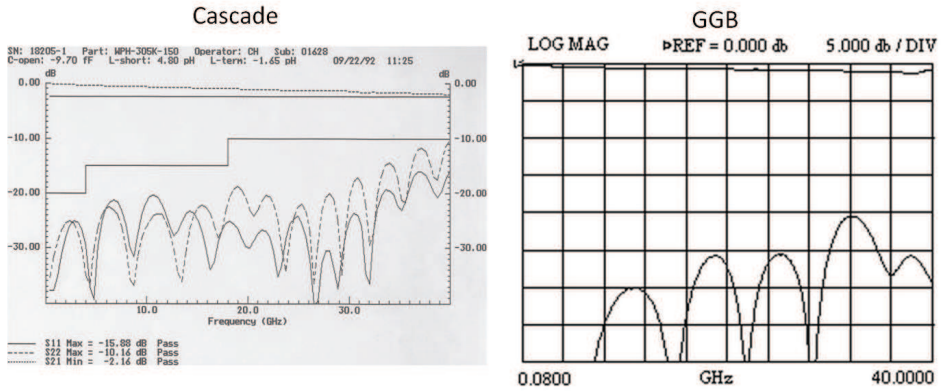

Figure 4: Insertion and return loss of 40 GHz models: Cascade WPH-305K (Left) [11],GGB 40A (Right) [1]

The past work with micromachined probes employed a design with a replaceable tip. However, replacement requires skill in assembling submillime-

ter waveguide components and mounting of thin chips . An objective of this work is demonstration of a probe tip that can be replaced by a non-specialist RF test engineer or techinician. Therefore, the chips must be larger, more robust, and easily handled. The probe will employ the standard Ground Signal Ground (GSG) configuration at the tip. Commercially available probe tip pitches range from 25 μm to 1.25 mm. For this work the design pitch will be 100 μm as our lab has commercial probes with this pitch that will serve as a basis for comparison. The pitch of a probe tip is the distance from a ground tip to the center conductor tip. Commercial probes in this frequency range have a coaxial adapter that interfaces to a coaxial transmission line inside the block. This coaxial transmission line extends through the block, exits the housing, and then transitions to a coplanar launcher at the tip (Fig.1). This transition provides a good field of view for the user. To utilize the advantages of the micromachining process, a different transmission line architecture will be used. The micromachining process utilizes thin silicon chips for the probe tips, which are not easily interfaced to a coaxial line.

In previous micromachined probes, the probe chip couples from a waveguide probe transition to a microstrip line on the chip [5, 6]. CPW ground planes are brought in to form the probe tips (Fig. 5). This probe should supply DC for biasing, which cannot be accomplished directly using a waveguide, as it cannot support a TEM mode. To address this transition, an SMA connector is included to contact onto a permanent thick silicon piece with integrated microstrip, stripline, or CPW transmission line as the in-block

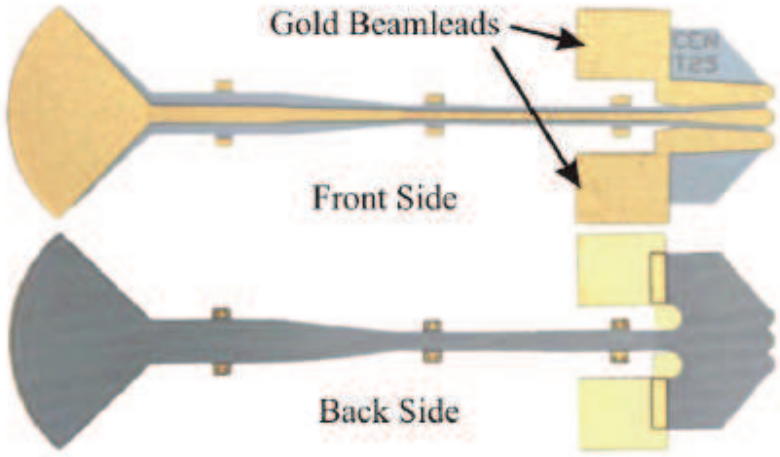

Figure 5: Micromachined wafer probe chip on 15 μm Si [6]

transmission line. This transition will be permanent and attached to the housing with adhesive. Near the front edge of the block, the probe chip's RF circuitry interfaces to the RF circuitry of the permanent silicon piece, and extends beyond the housing so that it can contact a DUT. The chip must be clamped securely to allow a DC connection, and to hold the chip in place during measurement. This chip must also have GSG tips at the contact end to allow interface with coplanar components.

While this project focuses on the design of a first order prototype, it has the opportunity to be commercialized, and therefore trade-offs of cost are also considered. The probe chips will be the replaceable part, while the housing and thick silicon component will be permanent. The housing, and permanent pieces that reside in the housing, should be designed to endure multiple replacement tips. The housing comprises the majority of the costs,

but as it is permanent, lasting over the lifetime of tens or hundreds of probe chips would allow the ≈$2,000 machining cost to be commercially viable. The $2,000 dollar cost per block was the quoted price for 2 blocks, and if more were ordered the price would decrease. The cost of the precision milling required for a probe chip recess (± 2.5 μm accuracy) dominates the cost of the housing. The tolerances in the lateral directions could be increased to ± 25 μm accuracy while keeping return loss to 13 dB. The precision for shaping the probe chips is done using the microfabrication process, which is essentially included in the costs of the process to make the chip. If the alignment of the chips could be done by the microfabrication process, the blocks could be made much cheaper. Another trade-off to consider is in the size of the probe chips. A goal is that the chip is large and robust enough to be replaced by the technician or engineer using the probe. Conversely the smaller the chips are, the more that can be fabricated per wafer lowering the cost per chip. Other costs to note are the use of high resistivity silicon, which increases the price. The use of 50 μm silicon, which is not a standard thickness, also increases cost. There are also costs for the connector as well as fabrication and assembly.

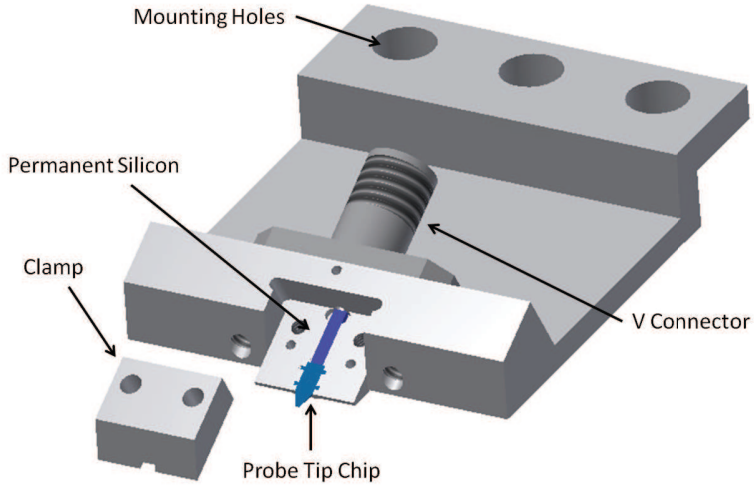

Figure 6: Probe Block

Probe Components

2.1 Overview of Probe Architecture

An overview of the probe is shown in Fig. 6. The probe assembly includes a two part aluminum housing, a coaxial launcher (V-connector), a permanent silicon chip, and a probe tip chip. The following sections will go into detail on each piece and how they interface with one another.

2.1.1 Coaxial Connector to Block Transmission Line

The initial RF transition is realized through a coaxial launcher connector that couples the TEM mode of a coaxial cable to a quasi-TEM mode on a planar transmission line inside the housing. In this case, a V-connector,

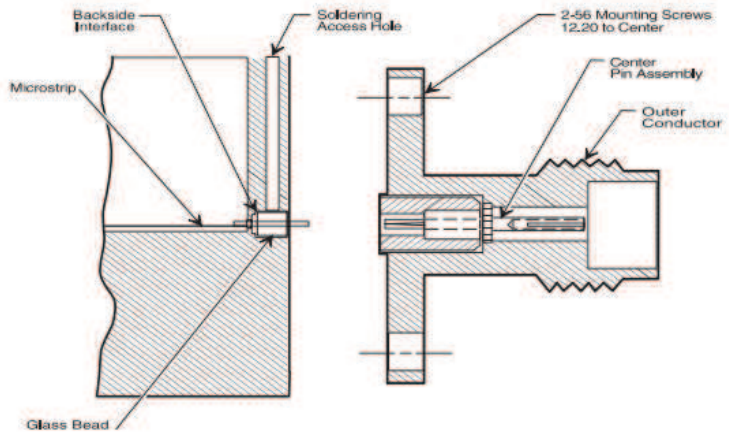

Figure 7: V-connector diagram [12]

which is manufactured by Anritsu Inc. [13], was chosen as the launcher. The V-connector has a 1.85 mm outer conductor diameter, which will allow single mode propagation up to 65 GHz with the geometry seen in Fig. 7. The prototype in this work has a design frequency of 40 GHz, however the V-connector operation up to 65 GHz will allow testing of the probe beyond this operating band. This can give insight into scaling future probes designed for higher frequency operation. The focus of this transition is to ensure that the V-connector can be integrated into the housing and contact a transmission line inside the block with high return and low insertion loss. It can be seen in Fig. 7 that a glass bead is permanently soldered to the housing to provide the direct contact to a transmission line inside the block. The female flange connector that is screwed onto the housing then provides the interface to a coaxial cable.

2.1.2 Block Transmission Line to Probe Chip Transition

Following the coaxial transition, inside the block is the transmission line fabricated on a permanent piece of high-resistivity silicon. This transmission line then contacts a transmission line on a probe chip. This chip to chip transmisssion line transition is reported in a patent by Cascade Microtech [14]. The patent describes a transition between CPW and inverted CPW on the replaceable tip. A significant issue is the potential misalignment of the two chips. To account for this, the shape of the overlap should be designed to allow for variations in alignment Fig.8[14]. The current work will utilize the precision accuracy of the micromachining process to provide the necessary alignment.

2.1.3 Probe Tip Geometry

The replaceable probe chip with GSG contact tips will extend from the block to enable contact with the DUT. The shape of the probe chip and tips will be defined lithographically in the fabrication process to fit into an alignment structure in the block. This structure will have recesses for the chip to be dropped into, so that it is self aligning. The contact resistance with a test substrate must be on the order of a few ohms to allow DC biasing and measurements. To achieve this, a contact force of 15 mN is generally considered sufficient [5]. An angle representing a reasonable trade-off between RF performance and visual clarity between the probe tip and test substrate has been found in previous work to be 30^{o} [6]. The thickness and length

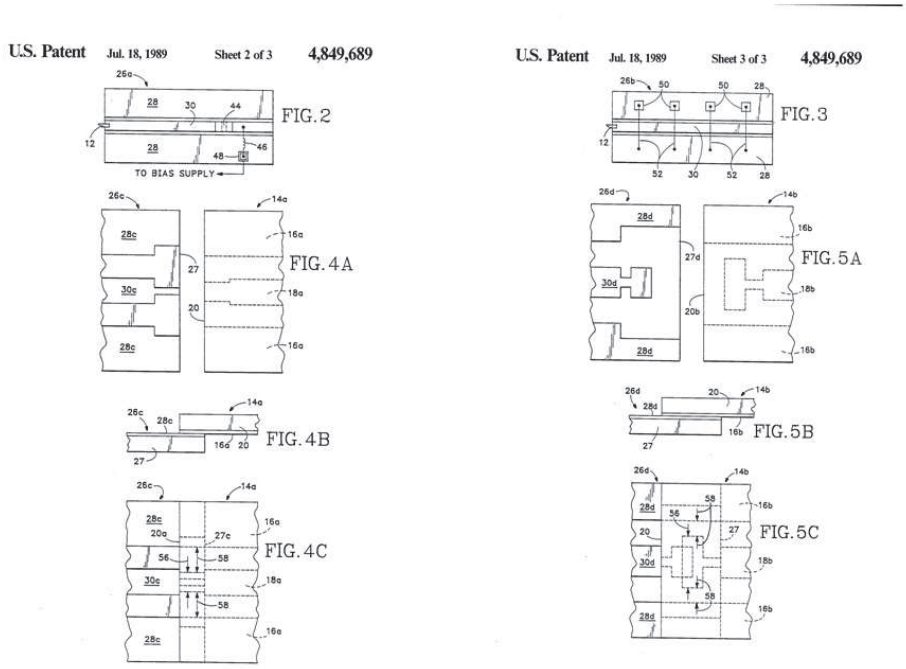

Figure 8: CPW to inverted CPW transition designed to permit variations in alignment[14]

of the chip must then be chosen to reach the substrate, without excessive flexing when 15 mN is applied. To ensure that the probe block does not touch the substrate when the probe chip flexes, at least 110 μm of clearance should exist between the bottom of the block and the test substrate [6].

2.2 Probe Block Design

The split probe block is a CNC milled aluminum housing. The housing includes a standard 3 hole RF probe mount to attach to the test station.

The V connector has holes for the mounting screws as well as for a glass bead that sits inside the block. This glass bead has a conductor in the center that touches the transmission line on the permanent piece of Si. Recesses are milled for the permanent piece of Si and for the probe chip. The tolerances of these recesses utilize the $\pm$ 2.5 μm accuracy of the milling process to ensure the optimal alignment for the drop in chip. The permanent piece of Si is epoxied into the block, while the probe chip will be held down by a separate aluminum clamp piece. The clamp will be screwed down, and is aligned by dowel pins.

2.3 RF Transition Test Structure

The RF transition, from an underlying piece of Si with metallization on the top, to a separate covering piece with metallization on the bottom, could have unanticipated issues with contact and alignment. There may be difficulties in obtaining electrical contact between transmission lines on the two pieces that may not be perfectly smooth surfaces after fabrication. Simulation can include surface roughness, however it cannot take into account all the variances of fabrication and testing in a lab. To assess the performance of this transition and the integrity of the electrical contact, a test structure consisting of a back-to-back RF transition was developed to evaluate both its RF performance and mechanical robustness. The structure includes a flipped silicon chip that bridges an air gap between two separate silicon chips (Fig. 14).

Transitions with a flipped chip have been tested before with a goal of integrating high performance, but costly III-V semiconductors with silicon wafers. Previous flip chip designs used metallic bumps to ensure a DC connection between the transmission lines [4]. To align the flipped chip with the base chip, SU-8 was employed to form a mechanical structure that interlocked the two chips [4].

The current work utilizes a flip chip, however the goal is not to integrate a separate type of semiconductor, but to ensure a reliable DC and RF transition to the probe chip. In the test structure there will also be an air gap below the flipped chip instead of a substrate to simulate the tip extending past the block into air, prior to coming in contact with a DUT. The issues of alignment, and impedance matching still apply. Track and channel, as well as indent alignment techniques were considered in this work, and are detailed in 2.3.2.

The characteristic impedance of a transmission line is determined by the geometry and the substrates involved. Microstrip has a characteristic impedance:

$$Z_o = \frac{60}{\sqrt{\varepsilon_{eff}}} ln(8\frac{H}{W} + 0.25\frac{W}{H}) \ when \frac{W}{H} < 1 \tag{2}$$

$$else \ \ Z_o = \frac{120\pi}{\sqrt{\varepsilon_{eff}}} \left(\frac{1}{\frac{W}{H} + 1.393 + 0.677 * ln\left(\frac{W}{H} + 1.444\right)} \right) \tag{3}$$

[15]

where H is the height of the substrate, W is the width of the conductor, and ε_{eff} is the effective permittivity which takes into account the permittivity of the substrate and the air. The characteristic impedance of CPW line, after taking into account ε_{eff} and the height, is determined by the ratio $\frac{W}{G}$where W is the width and G is the gap between the center conductor and the ground planes. Impedance matching is necessary to maximize the power transfer between the different sections of transmission line. The reflection coefficient given by:

$$\Gamma=\frac{Z_L - Z_o}{Z_L + Z_o} \tag{4}$$

[3]

where Z_o is the characteristic impedance of the line and $Z_L$is the load impedance. With two sections of transmission line in succession, there will be a mismatch between the lines that must be compensated for. When dealing with overlapped chips, ε_{eff} will change and so the dimensions of the transmission line must be adjusted to match the impedance, minimizing reflections.

500 μm thick silicon with a resistivity greater than 10 kΩ was chosen for the two bottom pieces in the test structure. High resistivity silicon is used to minimize dielectric loss. For the bridge piece, 15 μm silicon on insulator (SOI) was chosen. This substrate has been used for past probe chips for its robustness due to its high modulus of resilience [6]. The SOI structure

also allows for frontside and backside processing, therefore beam-leads and backside metal can be fabricated.

2.3.1 Simulation Results

The simulated S-parameters of the proposed RF transition test structure can be seen in Fig. 9. In simulation the back-to-back RF transition is expected to have close to 0 dB of insertion loss across the band. The return loss is expected to be greater than 18 dB across the band. This can be attributed to good impedance matching, and assuming perfect alignment.

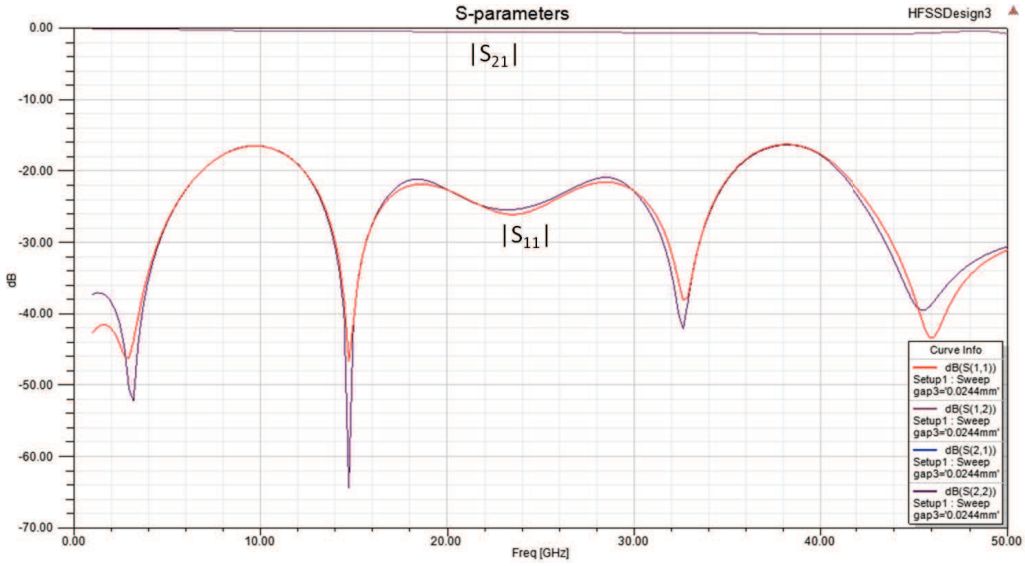

Figure 9: Simulated S-parameters of back to back test structure

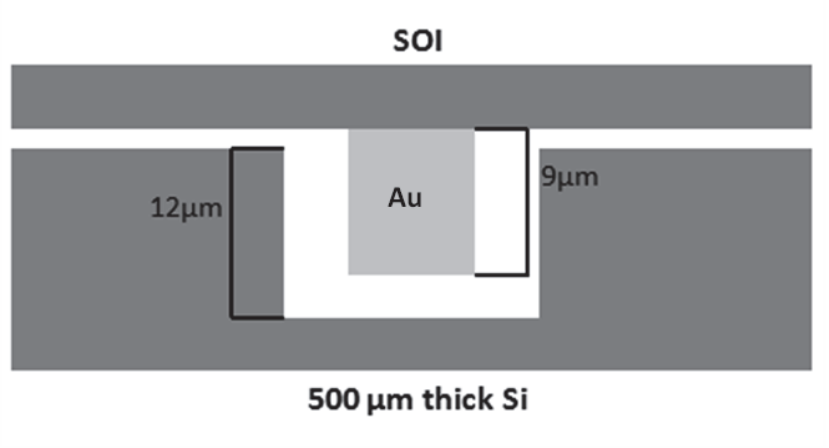

Figure 10: Track and Channel Alignment

2.3.2 Alignment Techniques

The first alignment technique for the test structure was a track and channel system Fig. 10. This would allow for alignment in one dimension. The idea is to etch channels into the 500 µm thick silicon that are at least 12 µm deep. Then metal would be plated to a sufficient thickness on the SOI bridge piece to create a track that would fit into the channel. In the fabrication phase, nLOF 2070 resist was used instead of metal. . nLOF, a negative resist, was spun to a thickness of 9 µm. It was hard baked at 225°C without reflow.

The second alignment technique to be tested was an indent method as shown in Fig.11. 15 µm silicon was chosen for the bridge in the test structure, since that had previously been used for probe chips. The indent in the 500 µm silicon chip must be deep enough to allow for alignment, however some of the chip must remain above the surface of the 500 µm silicon to allow for

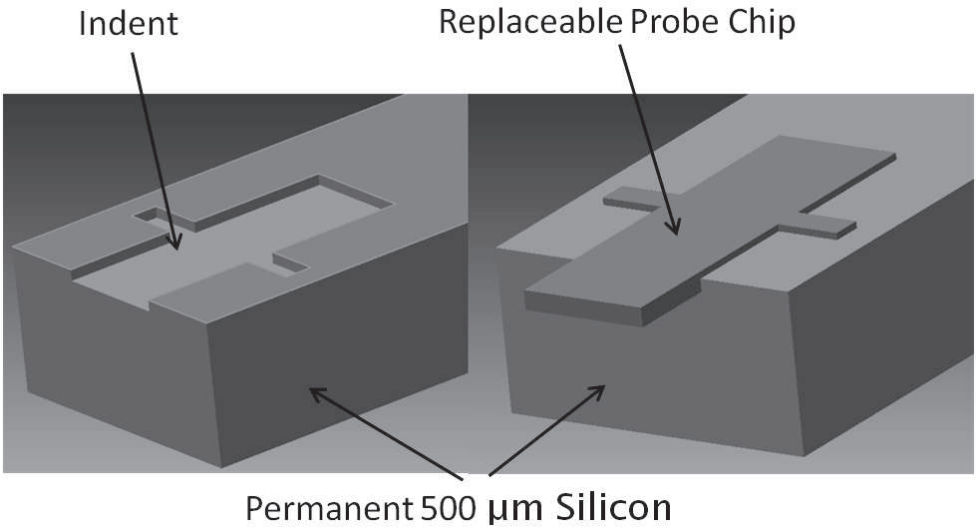

Figure 11: Indent Alignment

clamping. This led to a designed indent etch of 7-8 µm. The indent would allow for alignment in 2 dimensions.

2.3.3 Test Structure Block Design

A simple block was machined for the test structure, to test the RF transition between the permanent transmission line and probe chip. The insets for the silicon pieces, and the air gap to be bridged can be seen in Fig.12. This insets will allow for rudimentary alignment of the chips. The block allows the use of on wafer probes to test the back to back transition by leaving space for contact at either end. The depth of the deeper inset was made to ensure that there would be contact between the Si pieces. The block provides rudimentary alignment, however alignment marks on the silicon chips were

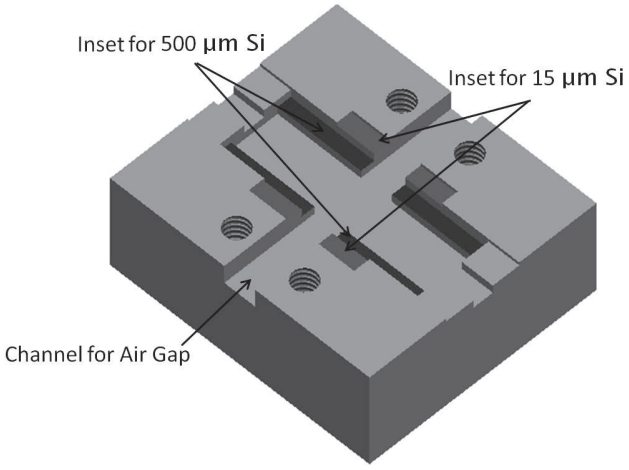

Figure 12: Test Structure Block

used for finer alignment. This was done to reduce the cost of milling the block, because smaller tolerances are more expensive.

2.3.4 Test Structure Mask Design

Two mask sets are required for the test structure. The 500 µm silicon pieces required two masks, and the 15 µm SOI piece required 6 masks. To ensure proper alignment, visual alignment marks were added to both mask sets.

Fabrication of the 500 µm silicon piece began with a silicon etch. This was used to etch either the indent, or the channel for the different alignment techniques to be tested. The second mask defined where the metal would be located for the CPW lines. There were also metal circles and rectangles used for the visual alignment.

Fabrication of the 15 µm thick silicon began with a via etch. This process

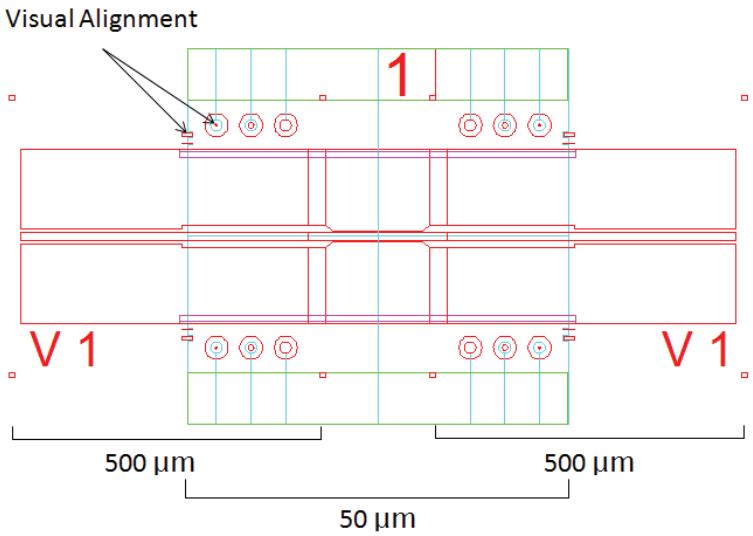

Figure 13: Mask of 500 µm and 50 µm pieces showing the overlap Visual alignment

etched vias through the 15 µm device layer silicon piece which allowed for alignment to frontside features when backside processing was done. The second mask defined where the metal on the frontside was plated for the transmission lines. The third mask defined the nLOF resist tracks which would fit into the channels for alignment. The fourth mask defined the metal on the backside of the wafer. The fifth mask defined the shape of the chip for the extents etch. The sixth mask was used to remove the edge bead, which is excess photoresist on the edge of a wafer after the resist has been spun. The detailed fabrication process will be found in section 4.1, and the full mask designs can be found in Appendix B.

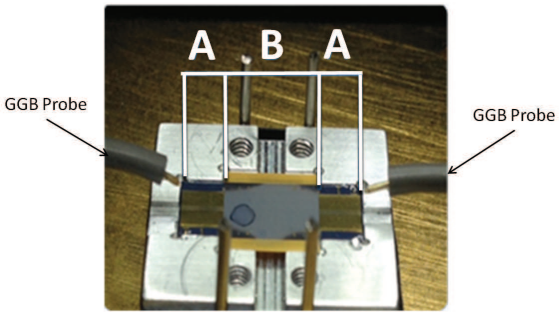

Figure 14: Test Setup

2.4 RF Transition Results

After the 500 μm silicon features had been fabricated, the chips were diced out of the wafer to fit the aluminum block. The 15 μm silicon chips had their shape defined lithographically with the SOI extents etch. The 500 μm chips were held in the block using vacuum grease, while a 15 μm chip was placed on top, bridging the transmission lines.

The 8510 C VNA was used for measurement. GGB probes were used to contact the test structure. The VNA was calibrated at the probe tips using TRL (Thru, Reflect, Line) calibration standards that had been fabricated on the same wafer as the 500 μm chips. More detail on the calibration process will be found in chapter 4.2. The measurement setup can be seen in Fig. 14. Sections "A" are CPW transmission line on the 500 μm Si. Section "B" includes the overlapped regions of 500 μm and 15 μm Si, as well as the 15 μm Si bridging an air gap.

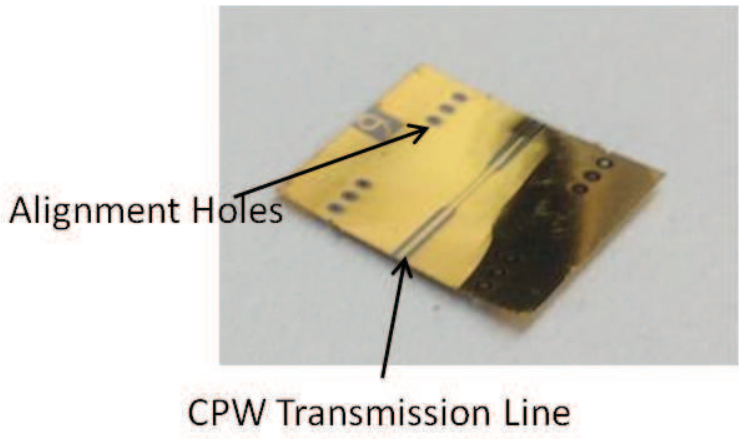

Figure 15: Warped 15 μm chip

2.4.1 Chip Warping

The test structure described above revealed an issue of warping of the thin SOI chips (Fig.15). The 15 μm silicon is used in the higher frequency probes, however the dimensions of those chips are around 3x1 mm. In contrast the chips for this test structure are approximately 5 x 5 mm. It appears that compressive stresses in the plated gold have enough force to warp the 15 μm chips. This made testing the alignment techniques impossible as the visible warping of the chips was much greater than the 8 to 9 μm deep tracks, or indents.

2.4.2 Corrected Measurements

The measured S-parameters are shown in Fig. 16 and indicate significant degradation in return and insertion loss above 20 GHz. The insertion loss for

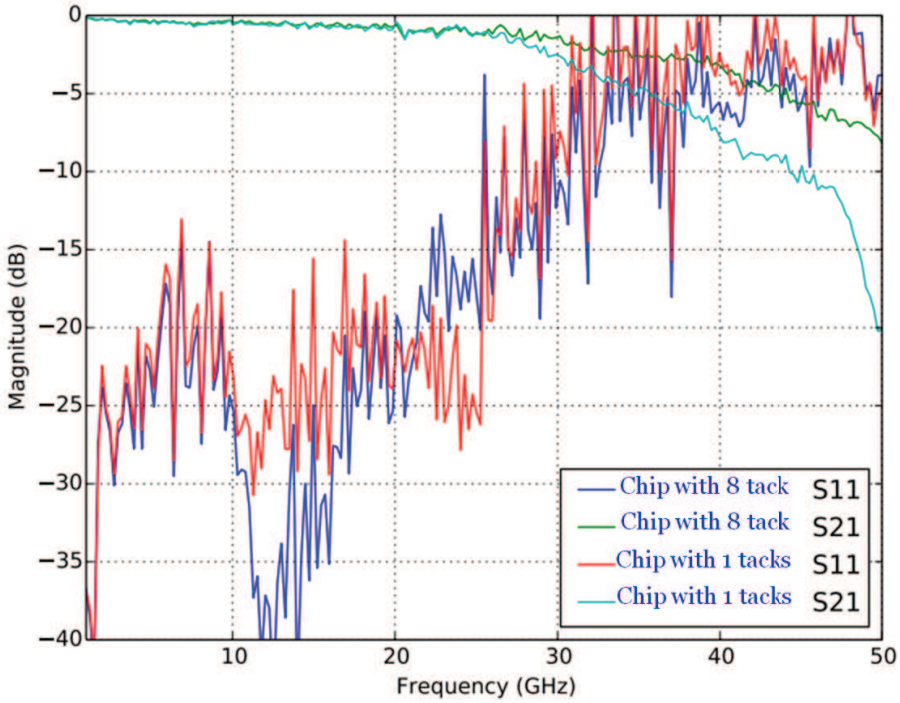

Figure 16: Measured S parameters

two different measurements are denoted by the light blue and green lines. The return loss for two separate measurements is denoted by the dark blue and red lines. The poor response is attributed to the large amount of warping in the chips. No signal transmission was measured when the 15 μm chip rested on top of the 500 μm chips with no applied force, because the center conductor was not in contact. The heat and ultrasonic force of a wire-bonder was used to tack down the 15 μm chips for measurement. It is important to note the difference between the insertion losses. The blue line was measured

when the ground planes and center conductor were only tacked down once on each side. The green line shows improved insertion loss when the chip was tacked down at least 8 times on both sides. This indicates that there was a physical gap between the 15 μm and 500 μm chips due to the warping. It was not possible with the wire-bonder to evenly flatten and bond the chip across the whole structure.

The final probe chips will be much smaller, to avoid any issues of warping, a design change was made, and 50 μm thick Si chips were used. Moving forward the alignment techniques in the fabrication were abandoned for alignment solely from recesses in the block. While the fabrication alignment techniques may work with a flat chip, ensuring better prototype performance with a similar alignment technique used in other micromachined probes was chosen.

3 Final Probe Design

Mechanical Design

Mechanical simulations were completed to ensure that the probe chip could handle the stresses endured during testing without fracture or excessive flexing. To accurately simulate the stresses, a 3D model of the probe block clamping down on a probe chip was implemented in Solidworks. A force of 10 mN was applied (3.3 mN per tip). The displacement and stress profile of this simulation can be seen in Fig. 17, where areas of high stress and displacement are displayed in red. With 10 mN applied the highest stress measured was 64.5 MPa, which is 1.3% of the yield strength of Si (approximately 5 GPa) [16].

RF Transitions

With satisfactory mechanical simulations , EMF simulations of the probe are required to complete the RF design. This section details the full HFSS simulation of the final probe. This includes the glass bead of the V-connector, all the way to a test substrate.

3.1 V-Connector to Shielded Microstrip Transition

The initial RF transition includes the glass bead of the V-connector which is a coaxial transmission line with a characteristic impedance of 50 Ω. The

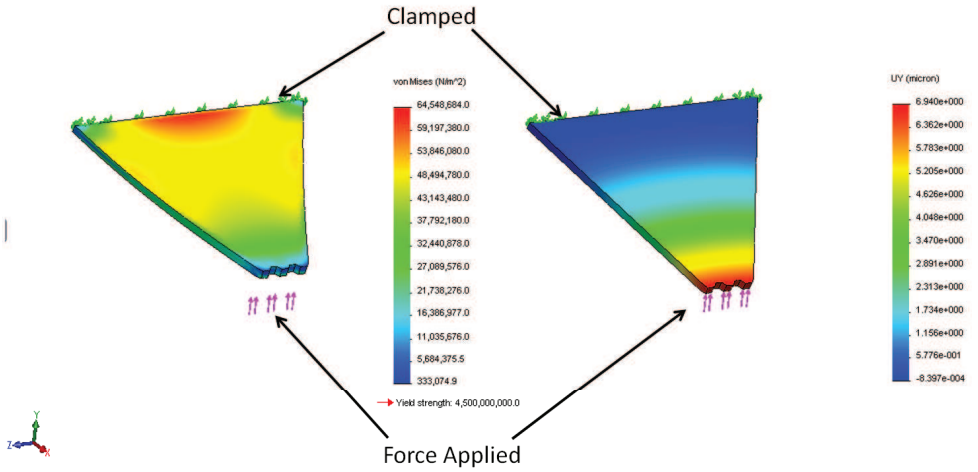

Figure 17: Mechanical simulation with 10 mN applied at the probe tip (Left) displacement (Right) stress profile

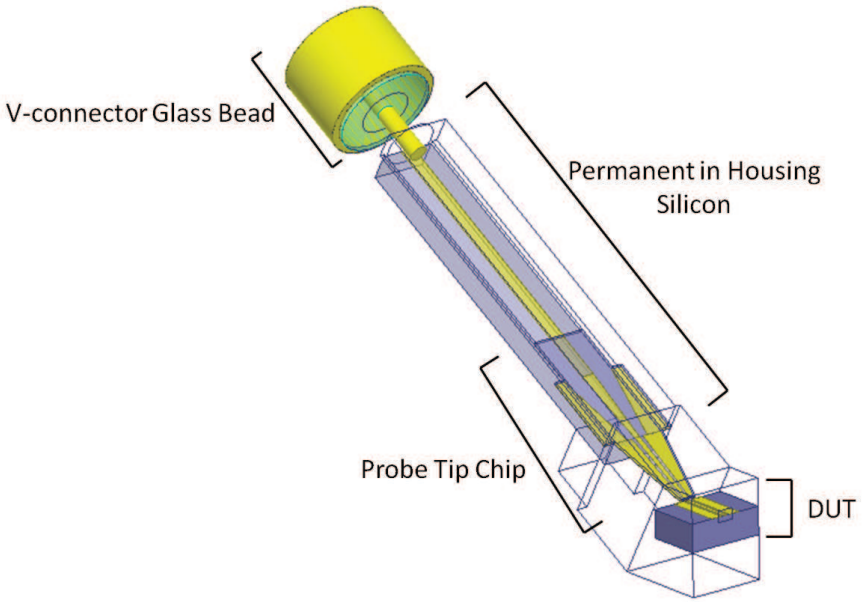

Figure 18: EMF simulation from SMA connector to test substrate

diameter of the center conductor, outer conductor and the permittivity of the glass in between determines this impedance. The next section is where the center conductor reaches through a hole drilled in the aluminum block. This is also a coaxial transmission line with air as the dielectric which is why the diameter of the hole is smaller than that of the bead, to match a 50 Ω impedance. The next section is a shielded microstrip, on the 500 μm silicon chip, that exists inside the block. The large amount of metal of the V-connector pin, causes an impedance mismatch where it overlaps the microstrip. Some overlap is necessary to ensure a connection however, the longer the overlap, the larger the reflections from this transition. To minimize reflections below 15 dB at this junction, the overlap was reduced to 200 μm.

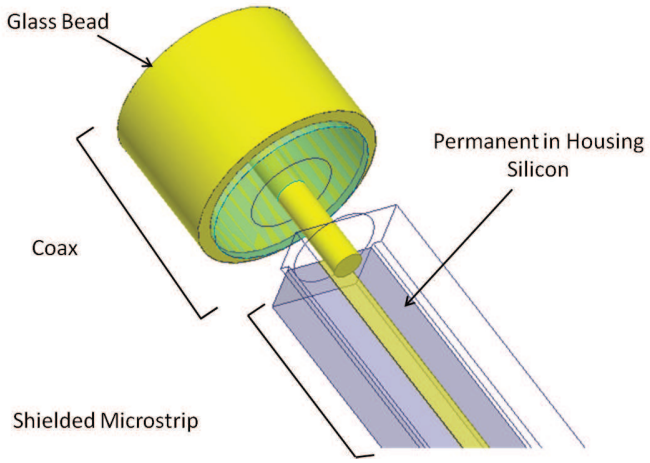

Figure 19: V-connector to shielded microstrip transition

Microstrip was chosen over CPW for this section since it exhibits lower loss.

3.2 Shielded Microstrip to Stripline Transition

The next transition occurs where the 50 μm silicon chip overlaps the microstrip on the 500 μm silicon in the block. At this point the transmission line becomes stripline. To match to 50 Ω, with the change in permittivity surrounding the transmission line, the conductor width was decreased approximately 10 μm. The effective permittivity has increased, and if we look at equation 2, the width must be decreased to keep the same characteristic impedance.

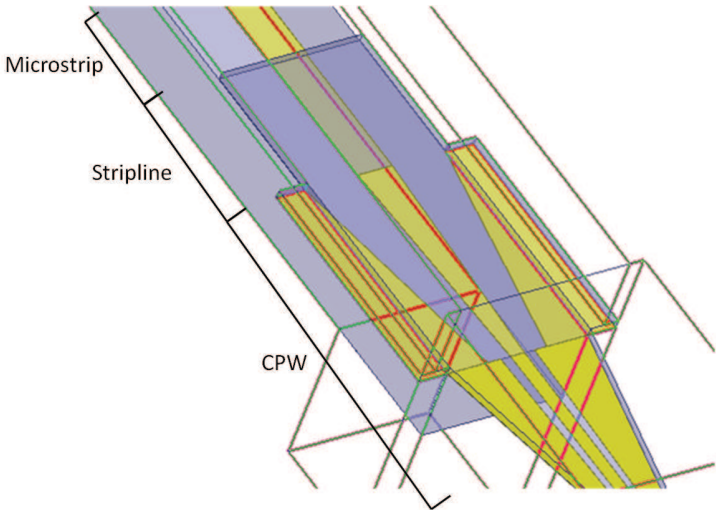

Figure 20: 500 μm silicon and 50 μm silicon overlap

3.3 Stripline to Coplanar

The next transition involves another change in transmission line type. The probe tips must be GSG, so at this point the transition to CPW is made Fig. 20. The grounds are transitioned in from tabs that are clamped down by the block, to ensure that they are grounded. As the ground planes are transitioned in from the side walls, the center conductor is tapered down to continue impedance matching to 50 Ω.

The transition at the edge of the block is more difficult to design than the previous transitions. There is a drastic and abrupt change in the effective permittivity of the medium surrounding the transmission line. Not only has the chip left the shielding of the block but the 500 μm silicon piece is no longer beneath the probe chip. There is a trade off between an "S" taper

and a discontinuity at this transition. An "S" shaped taper could be used to smoothly transition to the new dimensions of the CPW line, however due to the abrupt change in the dielectric there will be an impedance mismatch. An abrupt change in the dimensions of the CPW line can be made to avoid an impedance mismatch, however this will result in a physical discontinuity which will also cause reflections. Through simulation of both options, it was found that the reflections caused by the discontinuity provided a better return loss than reflections from a tapered impedance mismatch. Specifically the taper had a return loss of 12-13 dB past 39 GHz while the discontinuity had return loss below 15 dB till 45 GHz. The alignment of the two pieces has been designed to be within 10 μm in the lateral directions from the tolerances of the CNC milling of the block. These tolerances could be increased to allow for ± 25 μm, however the return loss will reach 12 dB at places across the band.

3.4 Tip Definition

The last RF transition is at the probe tips. The CPW dimensions are tapered to reach the desired 100 μm pitch while matching 50 Ω. It is important to note that this is the stage where the taper could most easily be adjusted to accommodate different pitches. The chip is tapered in to provide a better field of view, and the tips are also defined to ensure contact of the gold tips, and not the silicon in between. This shape is possible, since the chip will be etched with a silicon etch, with the extents being lithographically defined.

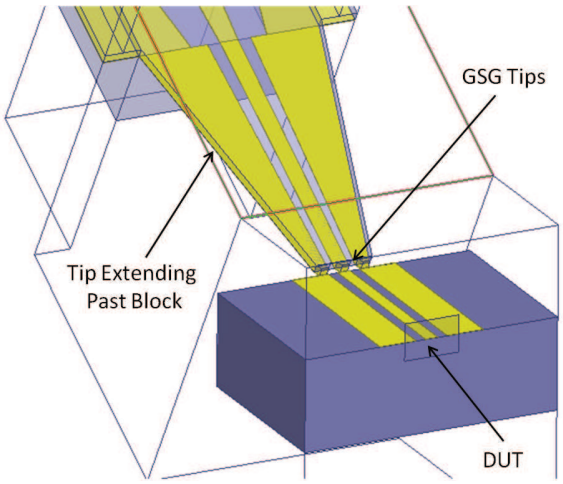

Figure 21: Probe tip chip extending out of block to DUT

3.5 Simulation Results

The results of the full simulation with a coaxial port on the glass bead of the V-connector and a wave port on the test substrate is shown in Fig. 22. It can be seen that the insertion loss is less than 1 dB across the band from 0 to 40 GHz, and increases to 1.2 dB at 50 GHz. The return loss is better than 15 dB across the band except for one point at 13.5 GHz where it is 14.5 dB. Beyond 40 GHz, the probe can still be used, however the return loss reaches 10 dB and the dynamic range will be reduced. Higher order modes also begin to propagate past 44 GHz. The periodic reflections from the discontinuity at the edge of the block can be seen in the return loss. The approximately 8 GHz periodicity matches the electrical distance from the discontinuity to the glass bead of the V-connector. The conductivity of gold used for these simulations was 4.1 E7 S/m. Simulations assuming plated gold

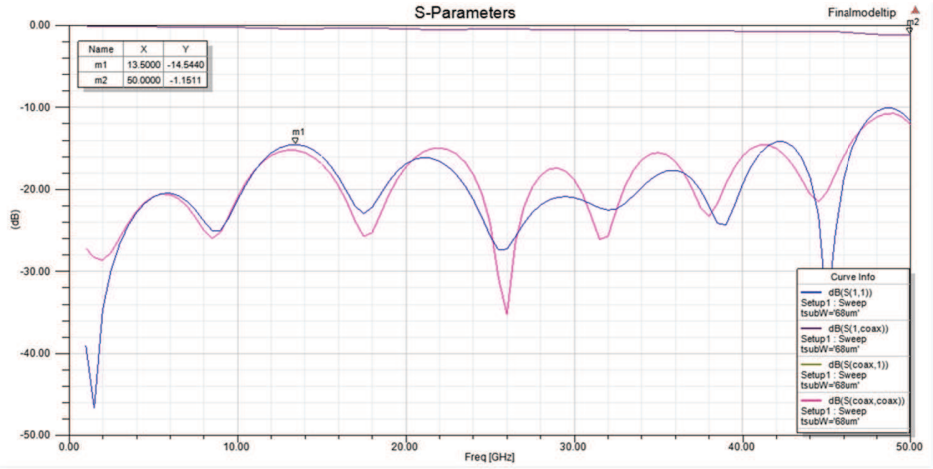

Figure 22: Simulated S parameters from V-connector bead to test substrate with perfect alignment of the 500 μm and 50 μm chips

had a conductivity of 3.0 E7 S/m increased insertion loss to 2 to 3 dB across the band, and return loss reached up to 12 to 13 dB at its peaks.

3.6 Block and Mask design

3.6.1 Block Design

The final probe block design is shown in Fig. 23 and detailed machine drawings can be found in Appendix A. There are three holes for the mounting of the V-connector, and three overlaid holes of different diameters to accommodate the glass bead. There is a hole on the top of the housing for solder to be dripped in to bond the bead to the housing. There are two holes to mount the clamp, with two dowel pins to align the clamp piece to within ±12.7 μm. To ensure that the permanent piece of silicon touches the probe chip, the

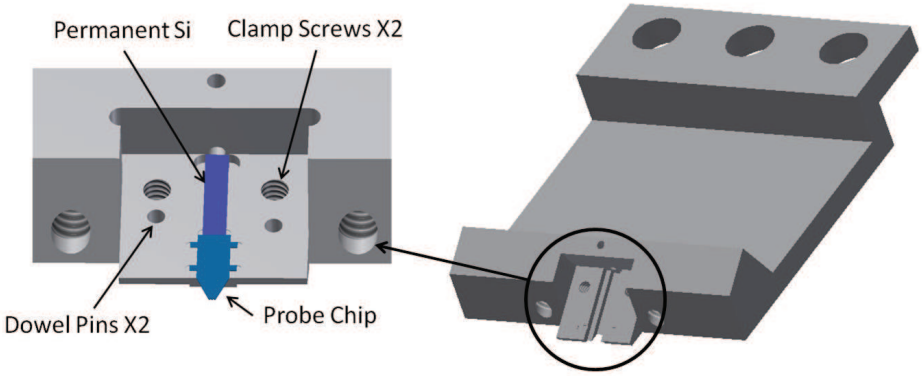

Figure 23: Final Probe Block

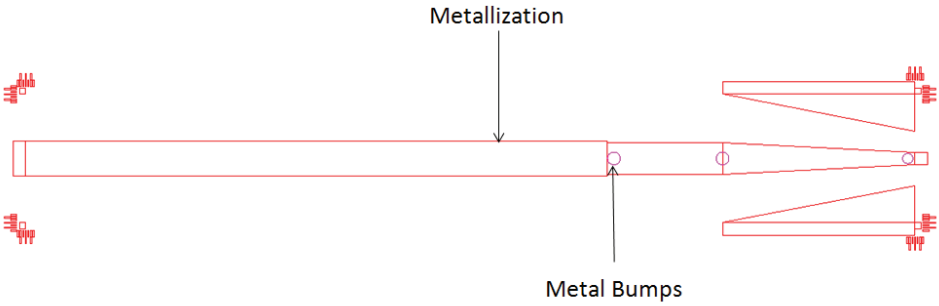

Figure 24: 500 μm Mask

block recess for this piece must be shallower than the 500 μm silicon, so the recess was milled 495 μm deep. To ensure that the recess for the probe chip was deep enough for alignment, but not too deep to prevent clamping, this recess was milled 35 μm deep.

3.6.2 500 μm Mask Design

The mask set for the 500 μm silicon can be seen in Fig. 24. The first mask defines the metallization of the transmission line in red. The change in dimensions can be seen as the transmission line changes from microstrip, to stripline, and CPW. Metal squares define where the piece should be diced to fit the block. Due to variances in the dicing, and tolerances in the block dimensions, a vernier scale was added to adjust where the dicing saw will cut, to have the most snug fit in the block. The second mask is for metal bumps to be plated higher than the rest of the metal. If there is an issue with planarity between the silicon chips, the bumps should ensure a good DC contact. It was found in the assembly stage that the bumps were not necessary. The only variation in the first mask is in removing the ground planes on some chips, as they should only be necessary on the 50 μm silicon chip. The variations in the second mask are in the size, amount, and placement of the metal bumps.

Calibration and verification circuits were also added to the 500 μm mask set. The calibration circuits are short, open, through, and four additional lengths of line to improve the accuracy of the TRL calibration. These sections are at 100 μm pitch with 50 Ω characteristic impedance. The verification circuits included two different impedance lines, one being 25 Ω and the other being 72 Ω. There is also a low pass filter at the top with a design cutoff frequency of 10 GHz and more than 12 dB rejection by 20 GHz.

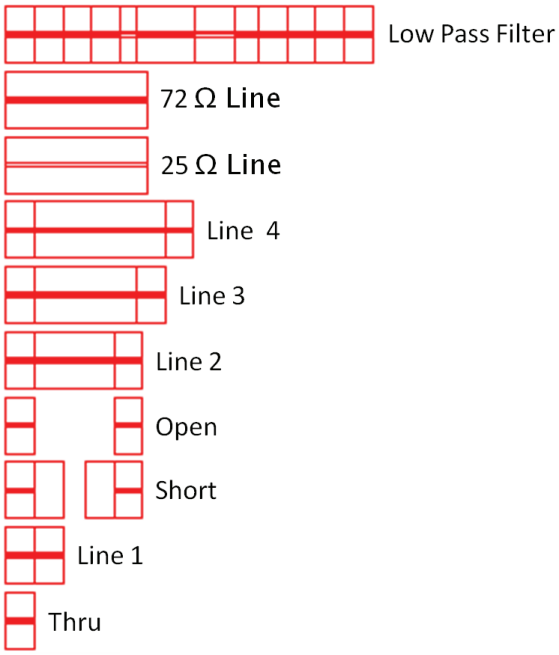

Figure 25: Calibration and Verification Circuits

3.6.3 50 μm Mask Design

The layout for the 50 μm silicon tip is shown in Fig. 26. The first mask is the via etch, which will create vias for backside alignment as well as in the ground planes. The clamp will apply pressure to this chip on the sides on the backside. These vias are necessary to ensure that the grounds at the tip are touching the ground of the probe block. The second mask is the extra-via. The purpose of this mask is to remove any photoresist that may reside in the via holes to ensure that full metal contact will connect the frontside and backside of the chip. The third mask is the frontside metal, which can be seen in red. This defines the metal for the transmission line, as well as beam

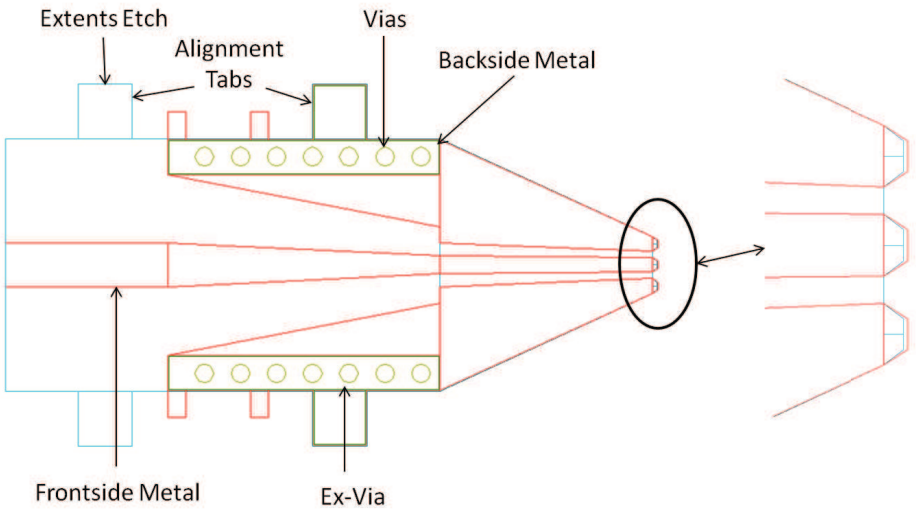

Figure 26: Mask for micromachined silicon tip

leads. Some of the chips have four 150 μm rectangular beam leads extending from the side of the chip. If there are issues in contacting the ground planes for DC connection due to problems with the vias, these could be bonded to the block to ensure ground connection. There are also 5 μm beam leads at the probe tips seen on the right of Fig. 26. These will ensure that there is gold all the way at the edge of the tips when contacting a substrate. After flipping the chip, backside processing will be done. First there is the backside metal mask which can be seen in bright green. This will ensure that the frontside metal grounds, connected by the vias, will have backside gold to contact the clamp. The backside gold will also be the region that is clamped down, and is therefore only at the front of the chip. this ensures that the chip does not get separated from the 500 μm silicon when the tip contacts a wafer. The final

mask is the extents etch seen in light blue. The final silicon etch will define the shape of the chip. This includes the 300 x 300 μm tabs for alignment in the block, as well as the definition of the probe tip. The variations in this mask set include chips that are ± 10 μm in their outer dimensions to ensure the tightest fit in the block. Some chips do not have the side beamleads as well.

4 Assembly and Results

4.1 Fabrication

4.1.1 500 μm Silicon

The permanent pieces of silicon that will reside in the block only requires two masks for the fabrication process. First a seed layer of Ti (100 Å) Au (200 Å) is deposited using an E-beam evaporator. Photolithography defines the shape of the metal to be plated up. First the transmission lines are defined, and 2 μm of Au are electroplated. Another photolithography step then defines where metal bumps will reside to ensure DC contact. 10 μm of Au are electroplated for the bumps. After all resist has been removed, a pottasium iodine based Au wet etch removes the seed layer of Au. The seed layer of Ti is removed using a 2 minute reactive ion etch (RIE) flowing SF_6, CHF_3, and N_2. The wafer is then diced according to vernier alignment marks defined by Au squares on the surface. The pieces can be diced at slightly different lengths and widths to ensure the best fit in the block.

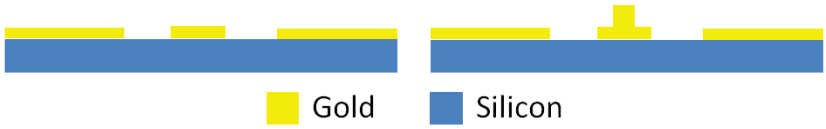

Figure 27: Fabrication process for in block silicon chips

4.1.2 50 μm Silicon

There is a major difference between the fabrication of these probe chips and those for the back to back test structure. The test structure utilized 15 μm device layer silicon, a 1 μm SiO_2 etch stop layer, and a 500 μm silicon handle. 50 μm device layer SOI was not available for purchase, and instead free standing wafers, which are fragile, are used. There is also not an etch stop layer. To remedy this, the first step is to sputter 4 μm of Al to not only strengthen the wafer, but to also provide an etch stop (step i). The wafer is then flipped and attached to a silicon carrier using Apiezon-W black wax. Via holes are then etched using using an ICP-RIE process flowing C_4F_8 and SF_6. The via holes are necessary for backside alignment, and to connect the frontside and backside CPW ground planes. It is important to note that in this photolithography step, the photoresist will not last through our 50 μm silicon etch unless it is approximately 15 μm thick. Prior to this photolithography step, 3,000 Å of aluminum was evaporated onto the frontside of the wafer. AZ 4330 resist spun at 2,700 rpm provides a thickness of approximately 5 μm. After the resist is patterned, a Transene Type-D aluminum etch is used, which realizes a hard mask on the surface of the silicon. The silicon etch will remove the resist after 30-45 minutes, however, the aluminum etches at only 20 Å/min and will last through the silicon etch without issue. Post etch, the hard Aluminum mask is removed in the Ttransene Type-D aluminum etch (step ii). Next, a seed layer of Ti (100 Å) Au (200 Å) is deposited. The Ex-Via mask is used to remove all resist

from the via holes so that plated gold will have a DC connection through the vias. The frontside transmission lines are defined with photolithography, and the gold is plated 2 μm in these regions. After seed layer removal, the frontside processing is completed (step iii). The wafer is then flipped and bonded to another carrier using Wafer Bond and epoxy (step iv). The first carrier is then thinned through dicing until approximately 70 μm remains. The remaining silicon is etched with the ICP-RIE etch. The Al etch stop is now removed using the transene aluminum etch. With the backside of the silicon now visible, seed layers of Ti and Au are deposited, and the backside metal areas are defined with photolithography. Backside gold is then plated 5 μm high (step v). After seed layer removal, an extents etch is completed using the ICP-RIE silicon etch. This etch defines the shape of the probe chips and will etch down to the Wafer Bond (step vi). The Wafer Bond is then removed using a TCE bath which will release the probe chips.

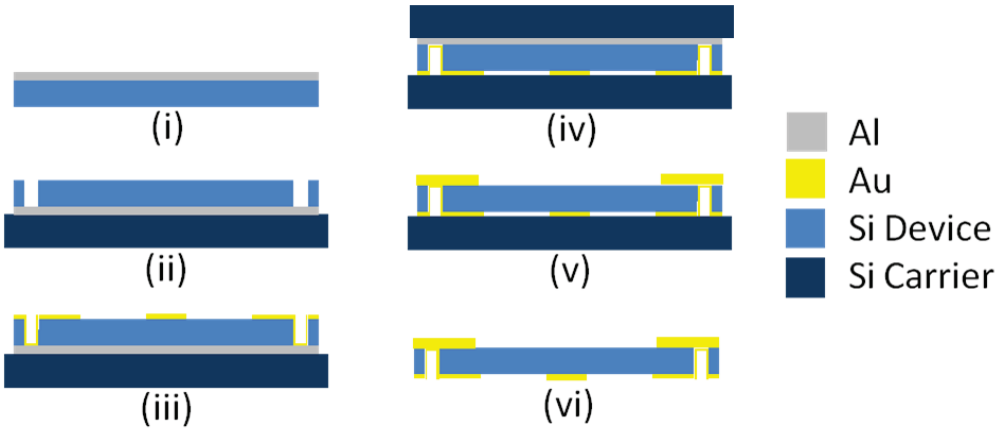

Figure 28: Fabrication process for probe chips

4.2 Calibration

Details on calibrating an RF measurement system can be found at reference [17]. The calibration method used in this research is TRL (thru, reflect, line). At a minimum this method requires two separate known lengths of line, and a reflect (open, short). This method is the most precise, since redundant standards can be used to increase the accuracy of the calibration. The on wafer standards for this project have five lengths of line, an open, and a short to improve calibration accuracy. Calibration programs, such as Wincal, require the physical length and phase velocity estimates for each standard. With this information, it can accurately remove the systemic error to calibrate the VNA at the probe tips. The disadvantages of TRL is that at low frequency, lines of significant electrical length can be very long, taking up valuable wafer space. The different lengths of line also require the movement of the probes in two dimensions, lengthening the calibration process.

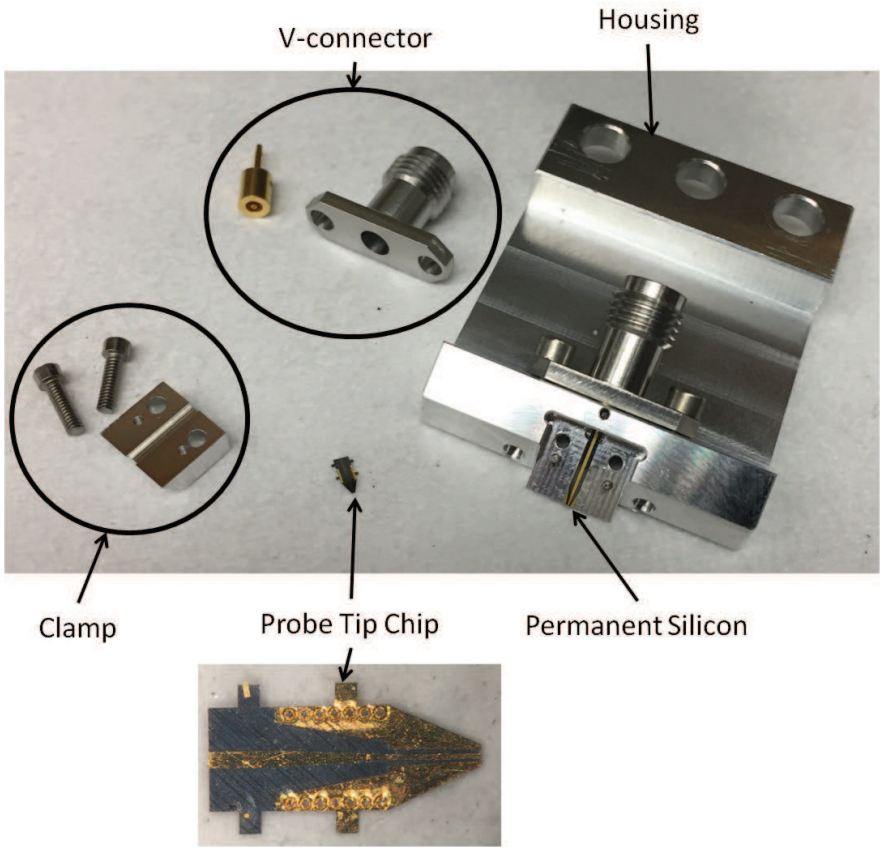

Figure 29: Disassembled Probe

5 Conclusion

The final chapter will detail the assembly of the micromachined probe. All of the parts necessary to make the probe can be seen in Fig. 29. Following probe assembly the S-parameters of two completed micromachined probes are found, and compared to commercial GGB probes. A force versus displacement curve was also found to determine the spring constant of the micromachined silicon. Finally future work for the project is considered.

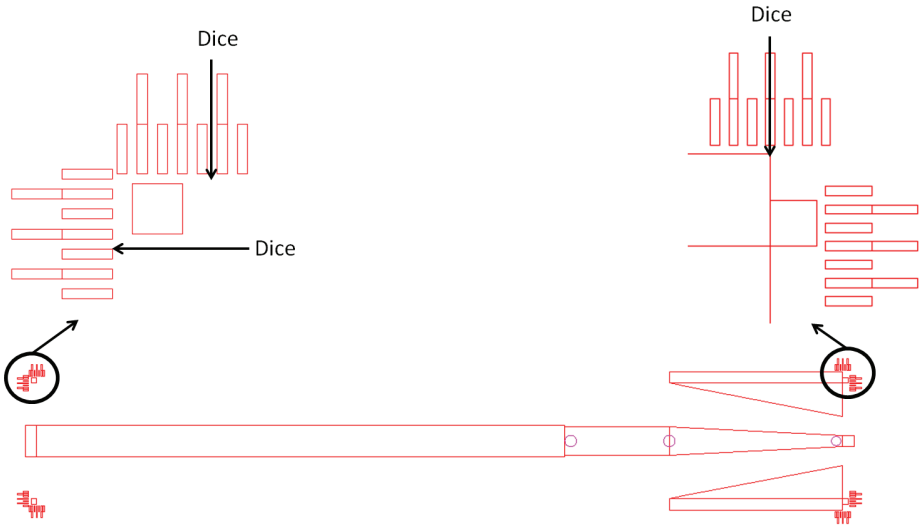

Figure 30: Where to dice the 500 μm chips to fit in housing

5.1 Probe Assembly

The first step in assembling the probe is to dice out the 500 μm chips to epoxy into the block. The exact lines on which to dice can be seen in Fig. 30. Following these marks is vital to ensure that the piece will fit in the housing, and that the piece will align with the probe tip chip. Note that the lines denoting where to dice are not for the center of the saw blade, as the thickness of the cut can vary. The mark denotes where the innermost edge of the blade, in reference to the chip, should be. The horizontal dicing line should be mirrored when doing the longways cut on the otherside.

The diced out piece of silicon must then be epoxied into the housing. We do not want epoxy under the piece as it will raise the height inside housing,

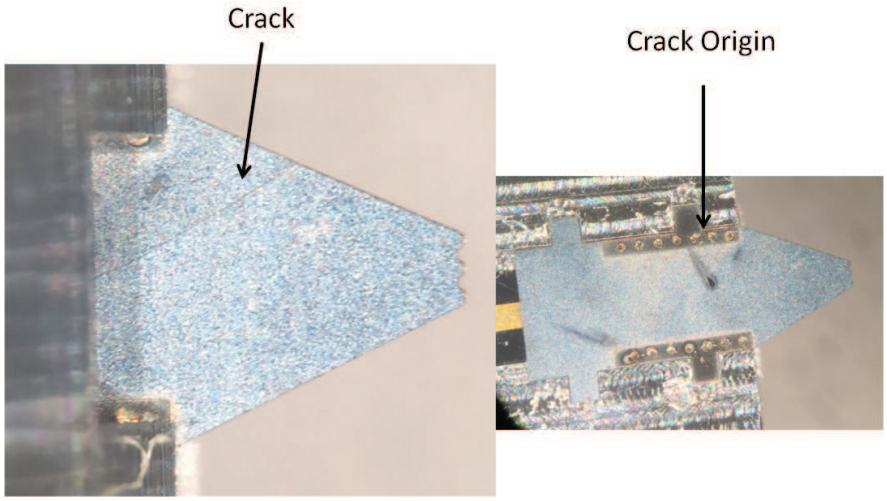

Figure 31: Cracked Probe Chip

possibly preventing alignment of the probe tip chip. The diced out piece should be placed inside the housing until it sits completely inside the block. It should be inspected with a microscope to ensure that it is flat and nothing is trapped underneath. Two small dots of Norland Optical Adhesive should be placed at the back of the chip in two recesses on the side (Fig. 29). 30 seconds of ultraviolet light should cure the epoxy.

Next, the glass K-bead (with liquid flux) must be inserted into the block (longer conductor end first); Fig. 7 helps illustrate this. Solder should then be applied through the hole at the top of the block, and cut when it is flush with the surface. A soldering iron can then be touched to the hole on top, and to the outer conductor of the K-bead to liquify the solder. It should be noted that aluminum specific flux was not used in this step. The V-connector can then be screwed on.

The last and most critical step of assembling the probe, is the attachment of the tip. When first assembling, it was found that the alignment recess in the housing worked, by sliding the probe tip along the surface until it came to rest in the recess. An issue that was not seen in modeling was the cracking of the probe chip when the clamp applied pressure. Mechanical simulations had been done to see if a force applied at the tip would cause cracking, however the possibility of cracking at the alignment tabs was overlooked. The cracked chip can be seen in Fig. 31 and while it may be difficult to tell, the crack originates at the sharp inner corner of the alignment tab. Five chips were cracked at different times during the assembly of two probes, and in every case the crack originates at a sharp corner of one of the two front alignment tabs. To minimize bending at the alignment tabs, small amounts of silver epoxy were placed in each recess. The chip was then placed in position, and the clamp was brought down until light pressure was applied to the chip. The entire probe was then placed on a hotplate to cure the epoxy which provides stress relief for the alignment tabs.

5.2 Testing and Results

The testing setup can be seen in Fig. 32. The probe station is a Cascade Microtech Inc. PA-200 probe station. A Keysight Technologies PNA-X was used to measure the S-parameters. Prior to measuring the S-parameters, it was important to test the DC contacts inside the block. A multimeter is connected to the coaxial connector on the micromachined probe to measure

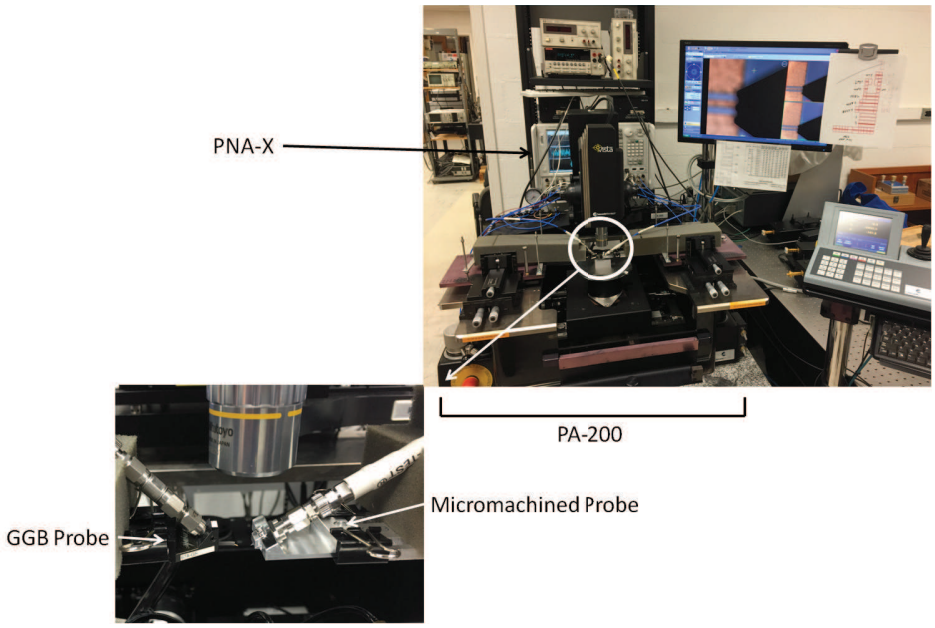

Figure 32: Test Setup

the DC connections. Without a probe tip chip in the block, the resistance should be on the order of a few mega-ohms. The resistance seen is that of the in housing silicon. With a probe tip chip clamped inside the housing, the resistance measured should be around 0.2 mega-ohms. The resistance seen is that of the CPW gap on the probe tip chip. To ensure that both ground planes on the chip are connected to the ground of the block, the tip must be brought into contact with gold plated substrate. Micromachined probe 1 has a resistance of 0.61 Ω and probe 2 has a resistance of 1.6 Ω. It is also important to make sure that both ground planes are DC connected which can be tested by contacting 2 points of the tip on the substrate. Probe 1 had resistances of 0.96 Ω and 1.1 Ω, while probe 2 had resistances of 4.8 Ω and

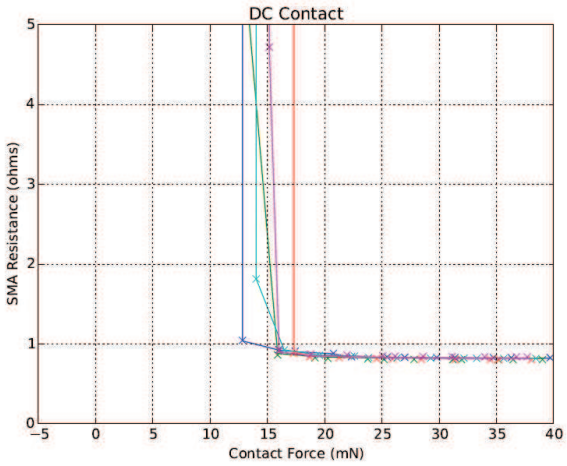

Figure 33: DC Contact vs. Force

1.9 Ω. A load cell was used to determine the force necessary to obtain DC contact with a substrate and Fig. 33 shows the probe requires between 13 and 17 mN.

In order to measure the S-parameters of the probe itself, a two tier calibration is necessary. First a calibration to the tips of the probes is done with the TRL substrate fabricated. The error network includes the probes, the connectors, the cables, and the VNA. Then a SOLT calibration is done at the end of the coaxial cables, producing error networks including the cables, connectors, and the VNA. By multiplying the error networks of the first tier calibration, by the inverse of the error networks from the second tier calibration, the S-parameters of the probes can be de-embedded.

5.2.1 Probe S-Parameters

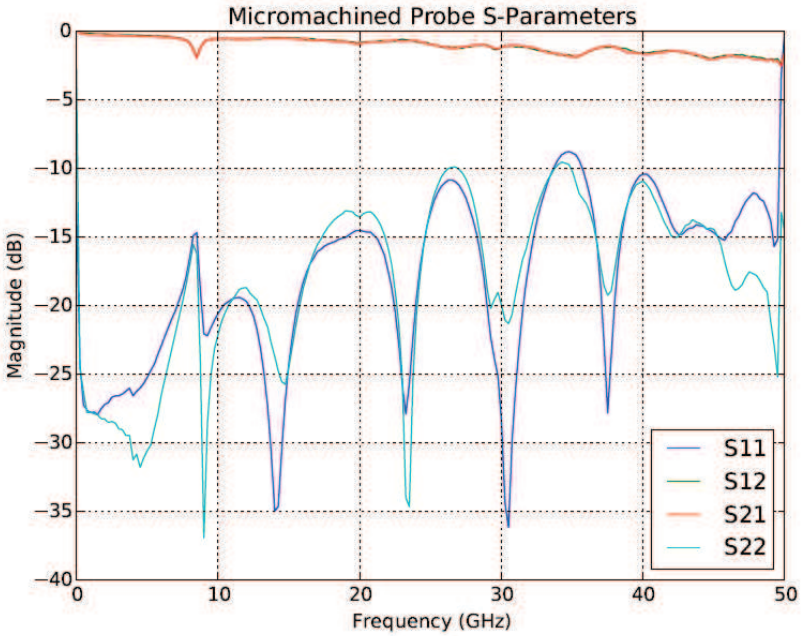

Figure 34: Micromachined S-parameters Probe 1

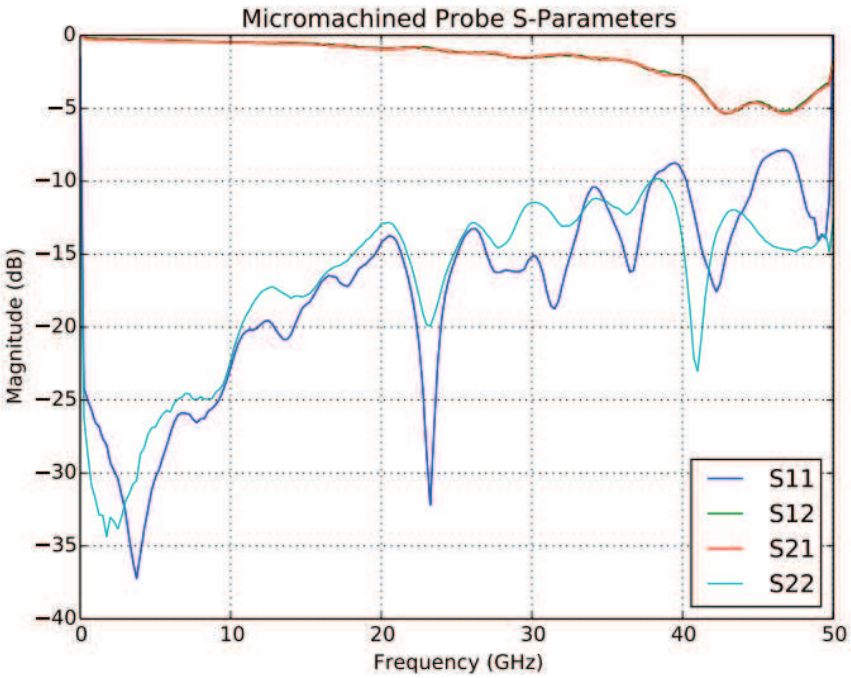

Figure 35: Micromachined S-parameters Probe 2

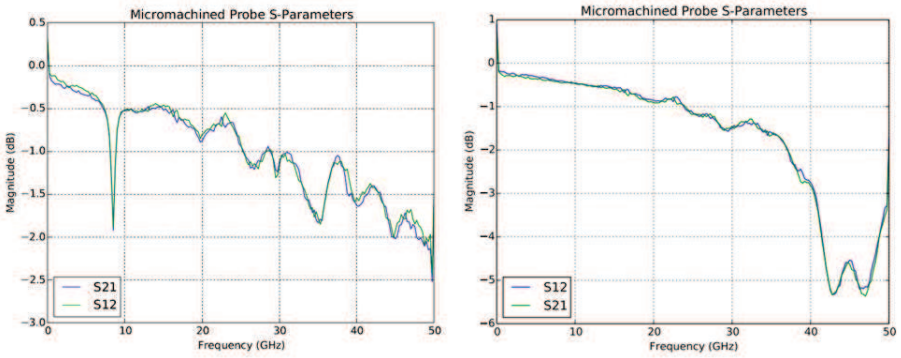

Figure 36: Insertion loss comparison of two micromachined probes

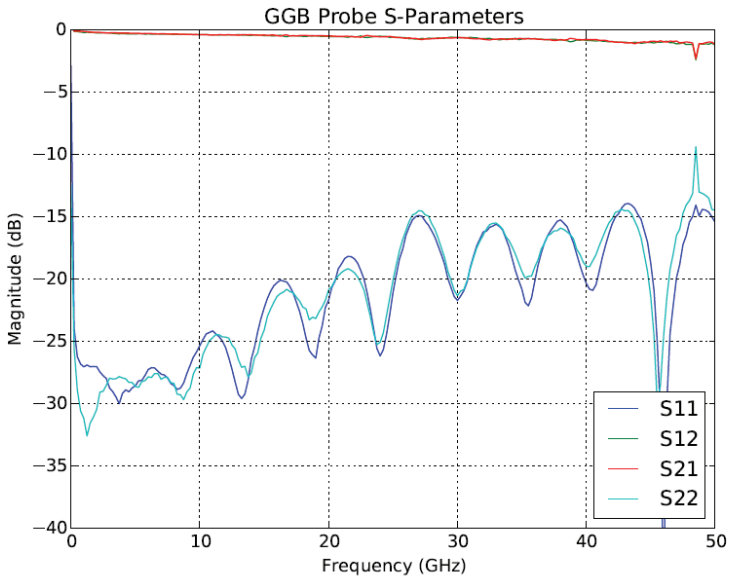

Figure 37: GGB S-parameters

The S-parameters of two micromachined probes and a commercial GGB probe can be seen in the figures 34 to 37. The micromachined probes were comparable to the GGB probe. The insertion loss was 1 to 1.5 dB higher for the micromachined probes across most of the band. The return loss reached 10 dB compared to 15 dB for the GGB probe. There was variability between the two micromachined probes which is best seen in Fig. 36. The most notable differences are a resonance at 8 GHz in probe 1, and a higher insertion loss beyond 40 GHz in probe 2.

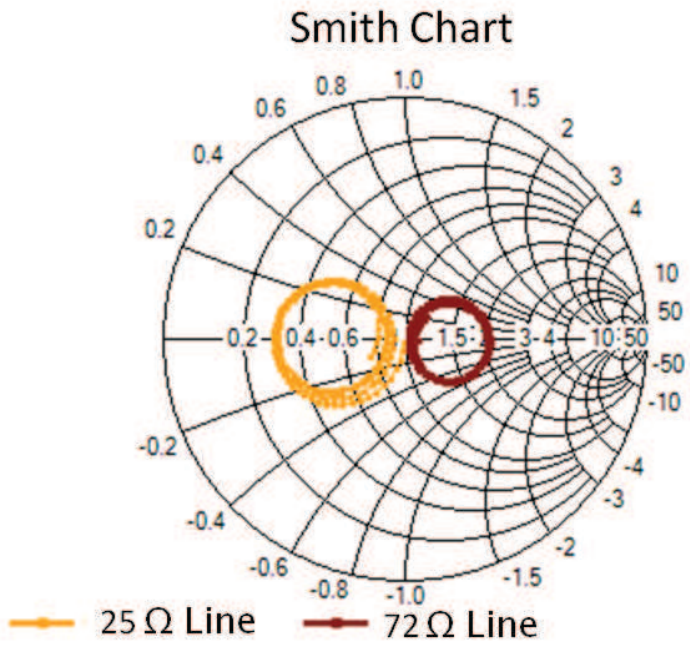

Figure 38: Measurement of 25 Ω and 72 Ω Lines

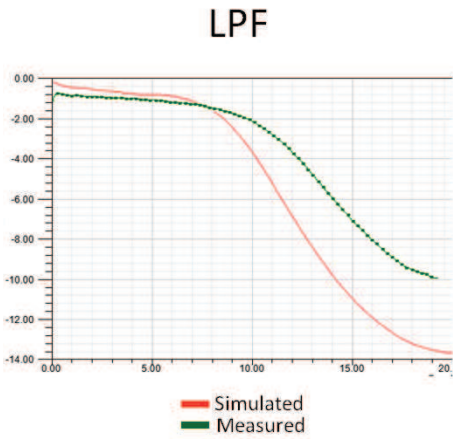

Figure 39: S21 Low Pass Filter Simulation vs. Measurement

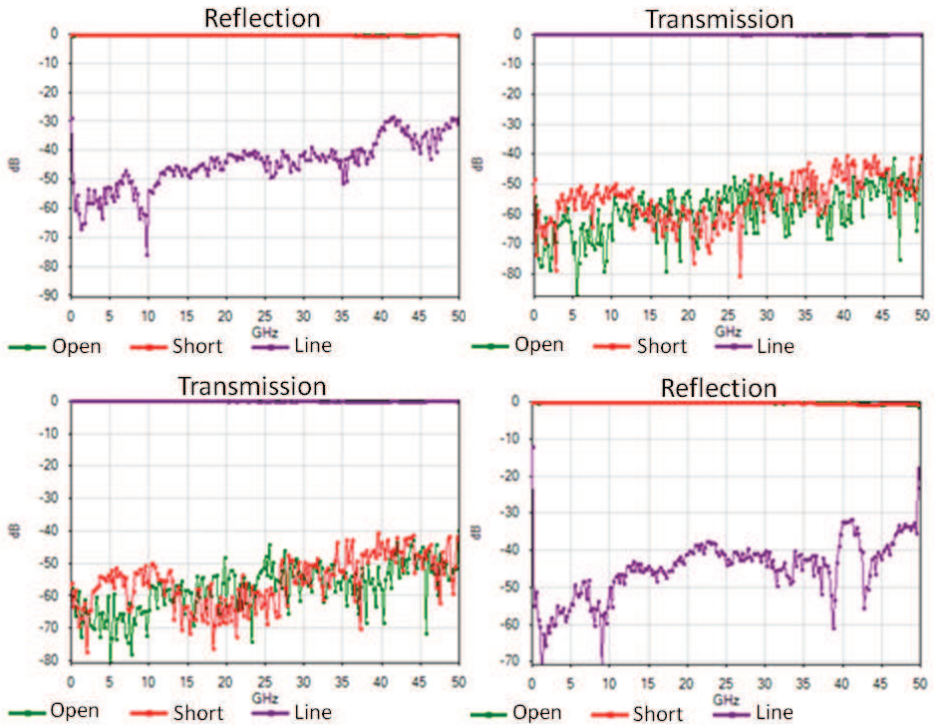

Figure 40: Dynamic range of calibrated measurement system using two micromachined probes

5.2.2 Device Under Test (DUT) Measurement with GGB Comparison

After calibration the verification circuits on the calibration substrate were measured. Fig. 38 shows the calibrated measurement of a 25 Ω and 72 Ω line on a smith chart. Fig. 39 compares the simulation of the low pass filter (LPF) with the measured LPF.

Measurement of the open, short, and line standards were done with a pair of micromachined probes (Fig. 40) and a pair of GGB probes (Fig. 41).

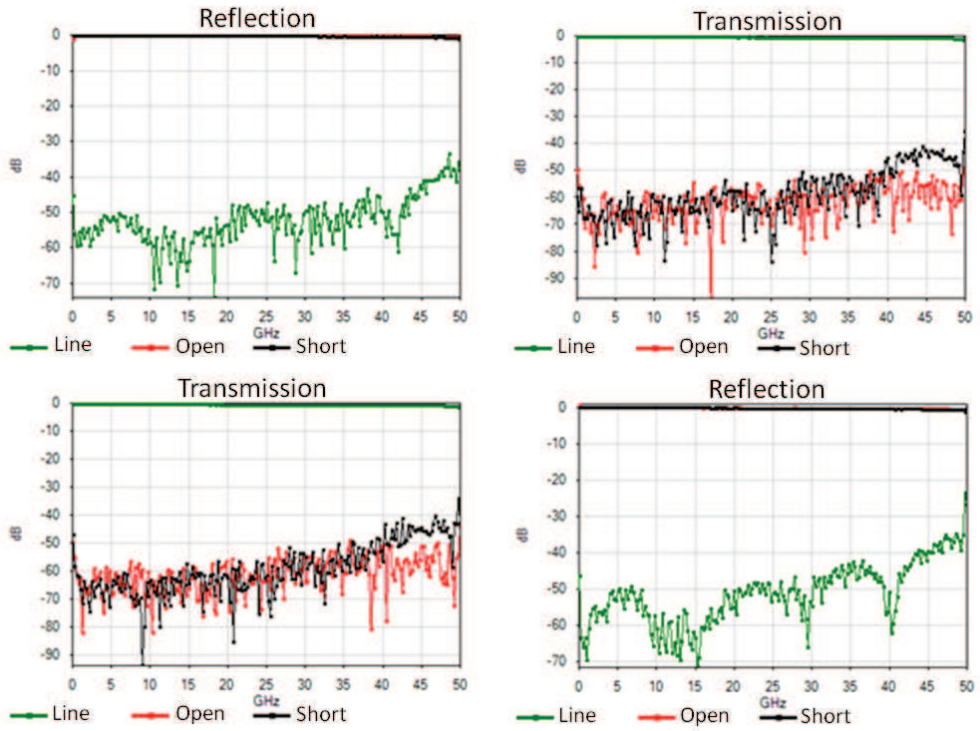

Figure 41: Dynamic range of calibrated measurement system using two GGB probes

What they represent is the calibrated dynamic range for this measurement setup with either sets of probes. The micromachined probes are comparable to the commercial GGB probes with a calibrated dynamic range of 40 dB up to 40 GHz.

5.2.3 Spring Constant of Probe Chip

The spring constant of the probe chip can be calculated by:

$$k = \frac{Ew}{4cos^2(\theta)} \left(\frac{t}{l}\right)^3 \tag{5}$$

[5]

Where E is Young's modulus of silicon, t is thickness, l is length, w is width, and θ is the angle of the probe with the substrate. This formula gives a spring constant of 1.34 mN/μm. The spring constant can be found in testing by the formula:

$$k = \frac{F_{contact}}{d_{overtravel}}, \ where \tag{6}$$

$$d_{overtravel} = d\, cos(\theta) \tag{7}$$

[5]

Using Fig. 42 the spring constant was found to be 1.36 mN/μm. The mechanical simulation of the probe chip using solid works yielded a spring constant of 1.44 mN/μm.

5.3 Future Work

The issue of cracked chips must be addressed. The same block can be used, however adjustments must be made to the extents etch, and backside gold masks. the sharp corners at the alignment tabs should be rounded so the the stress of clamping is distributed. Another mask should also be added to

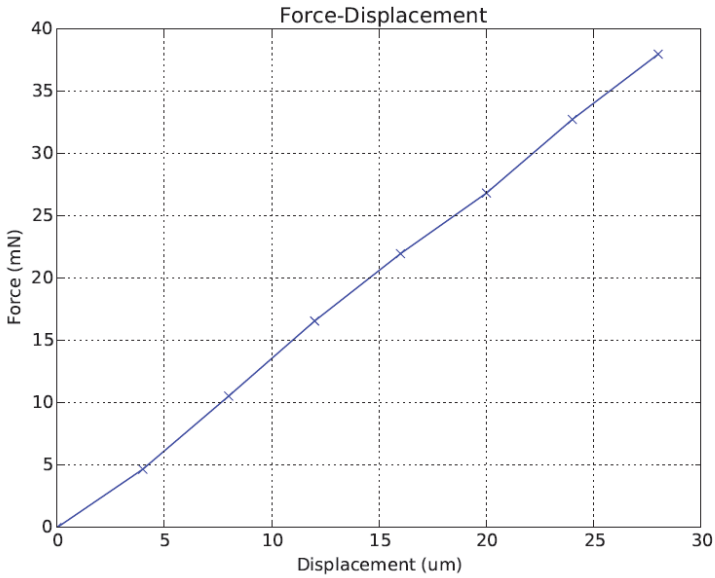

Figure 42: Force vs. Displacement

plate nickel at the tips. This will allow for a repeated contact study to be completed, to learn how many contacts the chip can handle before failure.

It would be useful to revisit the fabrication alignment techniques mentioned in the back to back test structure. The 50 μm chips do not warp and the techniques could have been successful in the final probe. If the fabrication could be used for the alignment the high tolerances of the recesses in the block could be removed, lowering costs.

An option for future work mentioned in 3.4 was to test the probes ability to handle different pitched tips. This would most easily be done in the probe tip chip, specifically after the chip is extending past the block. At this point there is a taper to the designed 100 μm pitch, and it would be important to

study what range of pitches can be reached by adjusting this taper. This is an important selling point of the prototype as a commercial product as consumers would have the ability to change the pitch of their probe without buying a new one.

Another area of future work would be the possibilities of scaling the probe to higher frequencies. 1 mm SMA allows single mode operation up to 110 GHz. It would be interesting to see if the prototype could be scaled to these frequencies by adjusting the geometries of the transmission line, and changing the thickness of the silicon substrates.

The most intriguing possibility for this prototype may be the prospect of integrating a 6-port reflectometer into the probe. With some adjustments to the housing, and to the permanent piece of silicon, commercial silicon diodes could be added to sample the power along the transmission line in the housing. The probe would then have the potential for an integrated network analyzer, meaning consumers would only need the probe and an RF source to measure S-parameters.

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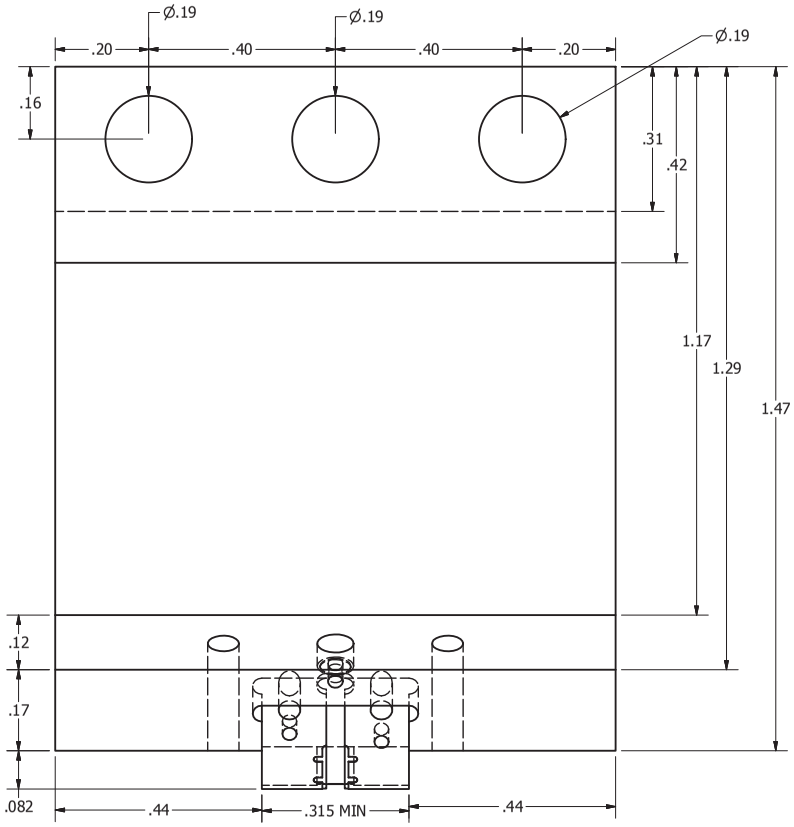
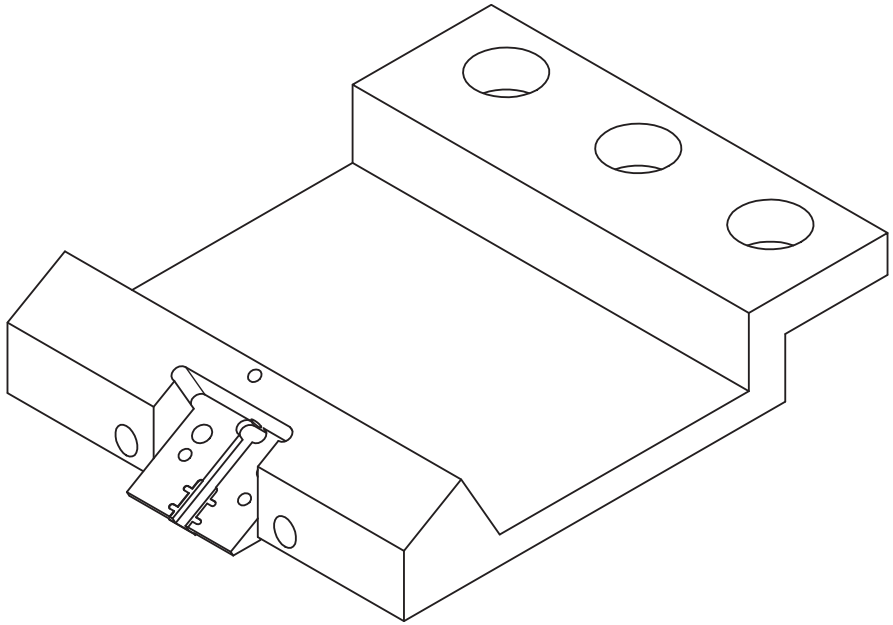
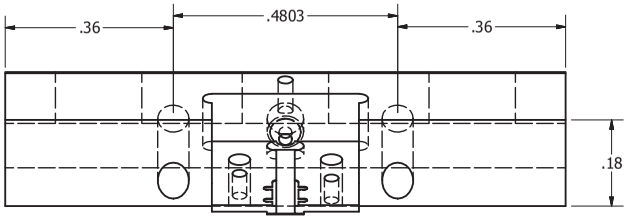
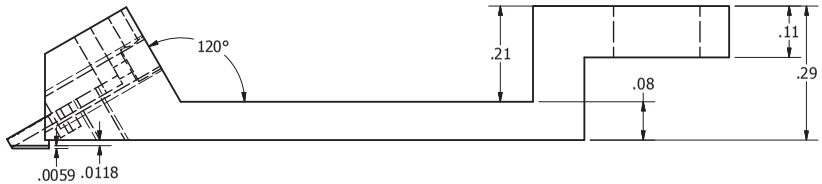
Appendix A Block Machine Drawings



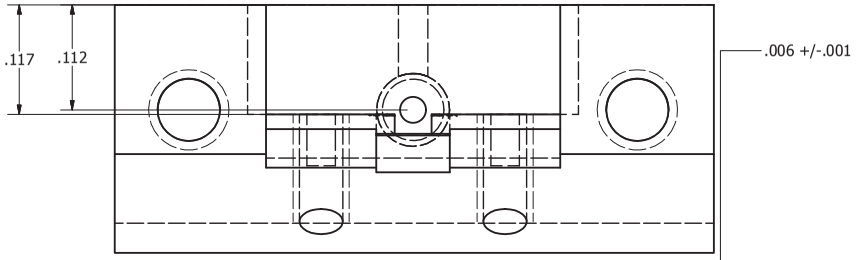




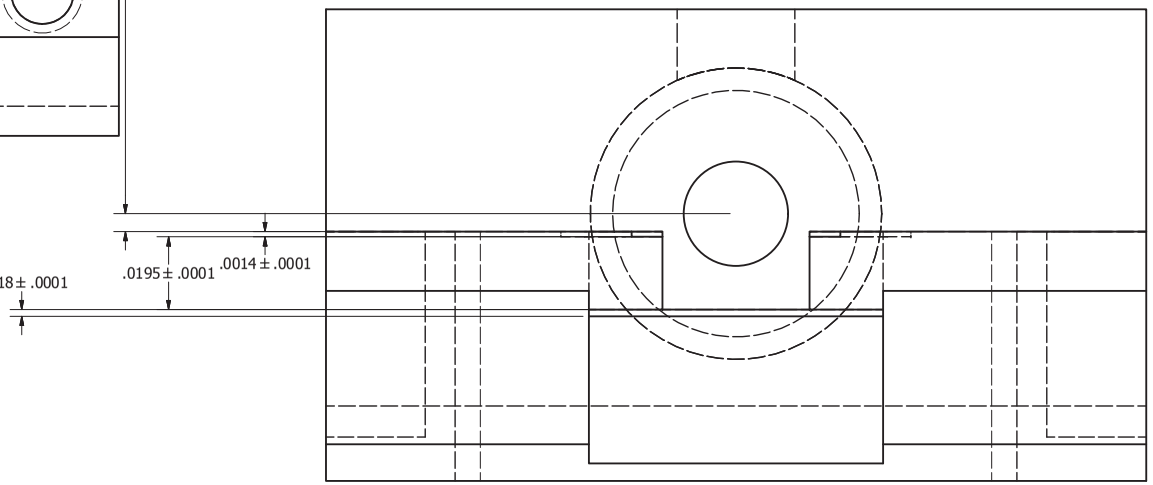


Tolerances unless otherwise specified
.XX +/- .01
.XXX +/- .005
.XXXX +/-.0005

DRAWN HFSSMachine	1/20/2015		
CHECKED		TITLE	
QA			
MFG			
APPROVED		SIZE C	DWG NO base_overall / REV
		SCALE 5 to 1	SHEET 1 OF 1

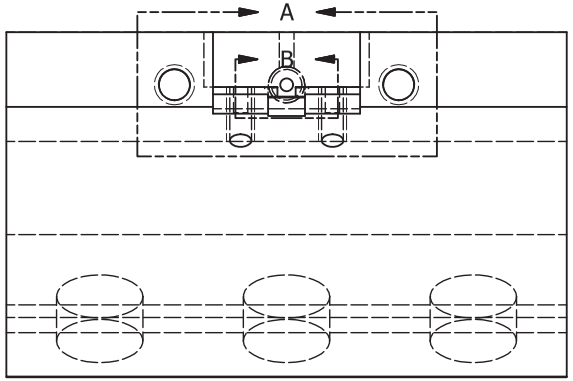


I have changed this dimension from .0048 +/-.0005 to .006 +/-.001
please let me know if this is possible



DETAIL A
SCALE 10 : 1

DETAIL B
SCALE 40 : 1



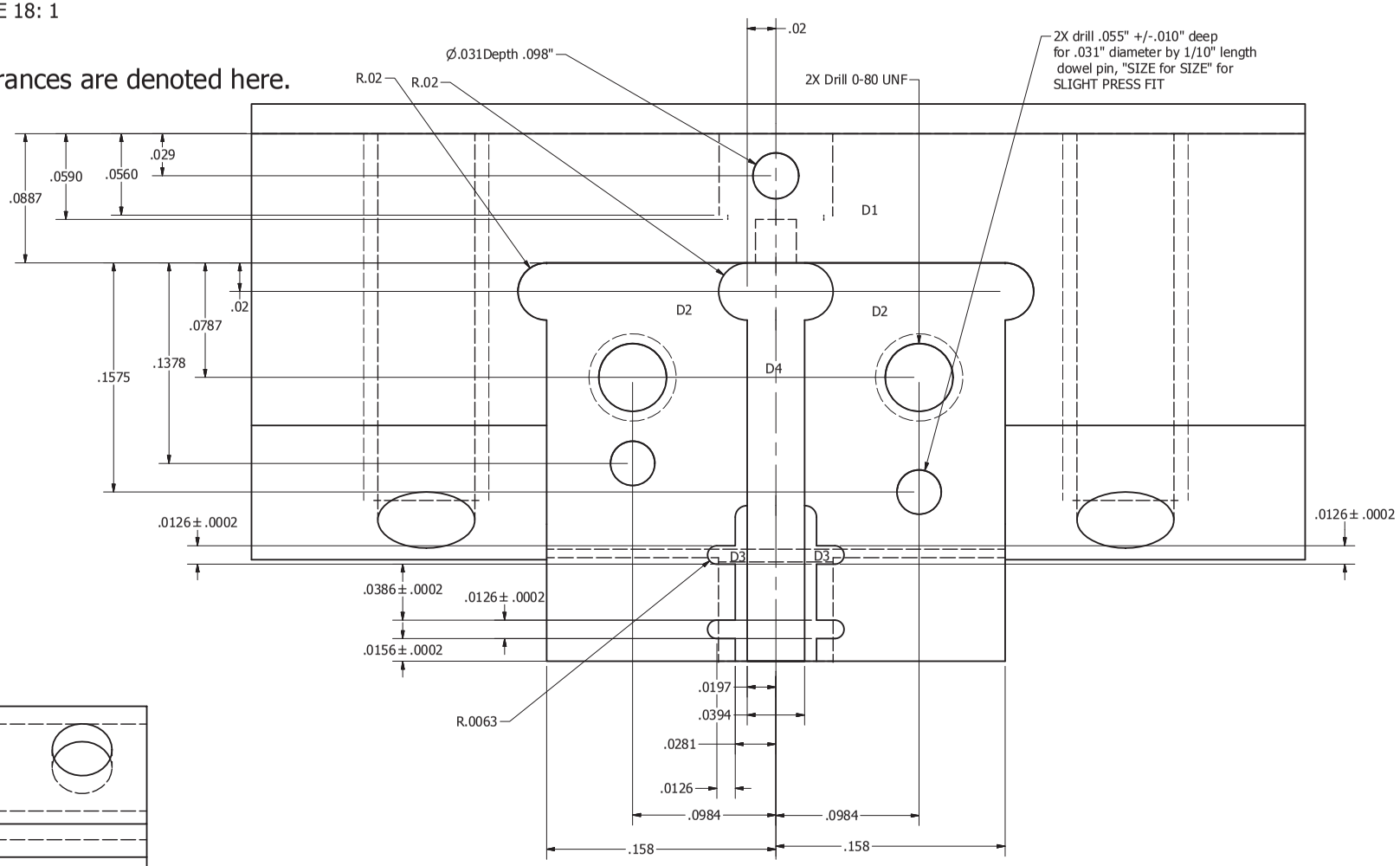
Tolerances unless otherwise specified

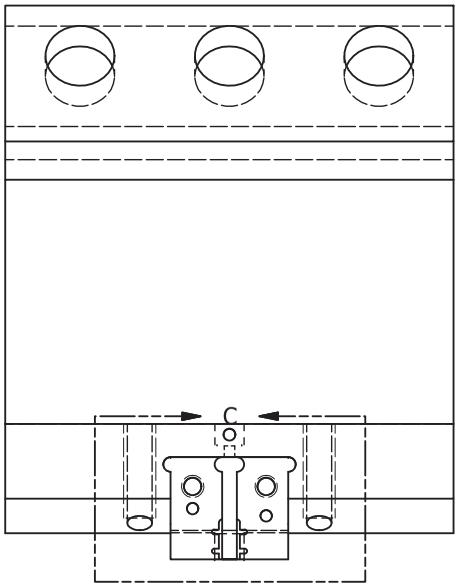
.XXX +/- .005
.XXXX +/-.0005

DRAWN HFSSMachine	1/21/2015			
CHECKED		TITLE		
QA				
MFG				
APPROVED		SIZE C	DWG NO channel depth to pill hole dimension	REV
		SCALE 5 to 1	SHEET 1 OF 1	

DETAIL C
SCALE 18: 1

Hole depths and tolerances are denoted here.



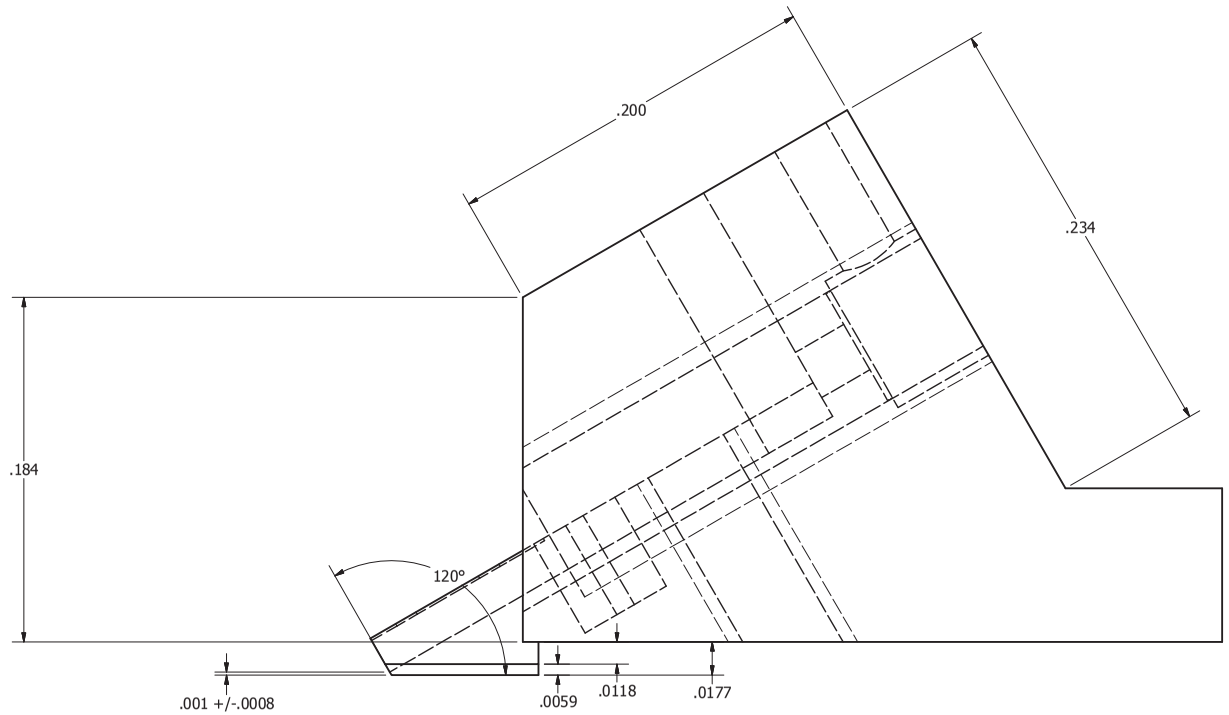


DEPTHS
D1-0.0
D2-.117 +/- .001
D3-.1187 +/- .0001
D4-.1381 +/- .0001

While i did give depths here in relation to the top of the block, they are not important, and should not have been given. The important depths are in reference to the bottom of the channel.

Tolerances unless otherwise specified
.XX +/- .01
.XXX +/- .001
.XXXX +/-.0005

DRAWN HFSSMachine	1/20/2015	
CHECKED		TITLE
QA		
MFG		
APPROVED		
SIZE C	DWG NO hole depth tolerances	REV
SCALE 4 to 1	SHEET 1 OF 1	

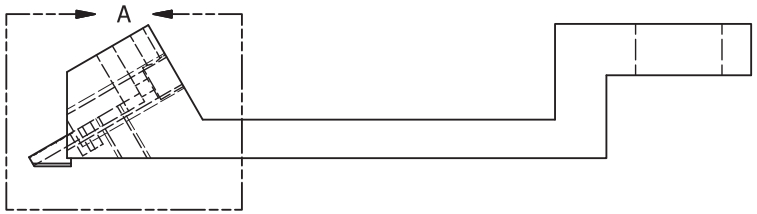


I have changed this dimension from .0016 +/-.0001 to .001 +/- .0008.
The depth below this channel is not important as long as it is as thin as possible, however due to the necessity of the probe chip needing to contact the surface, I need it to be equal to or less than the maximum size possible with this tolerance of .0018 inches

DETAIL A
SCALE 20 : 1

Tolerances unless otherwise specified

.XXX +/- .005
.XXXX +/-.0005



DRAWN HFSSMachine	1/21/2015			
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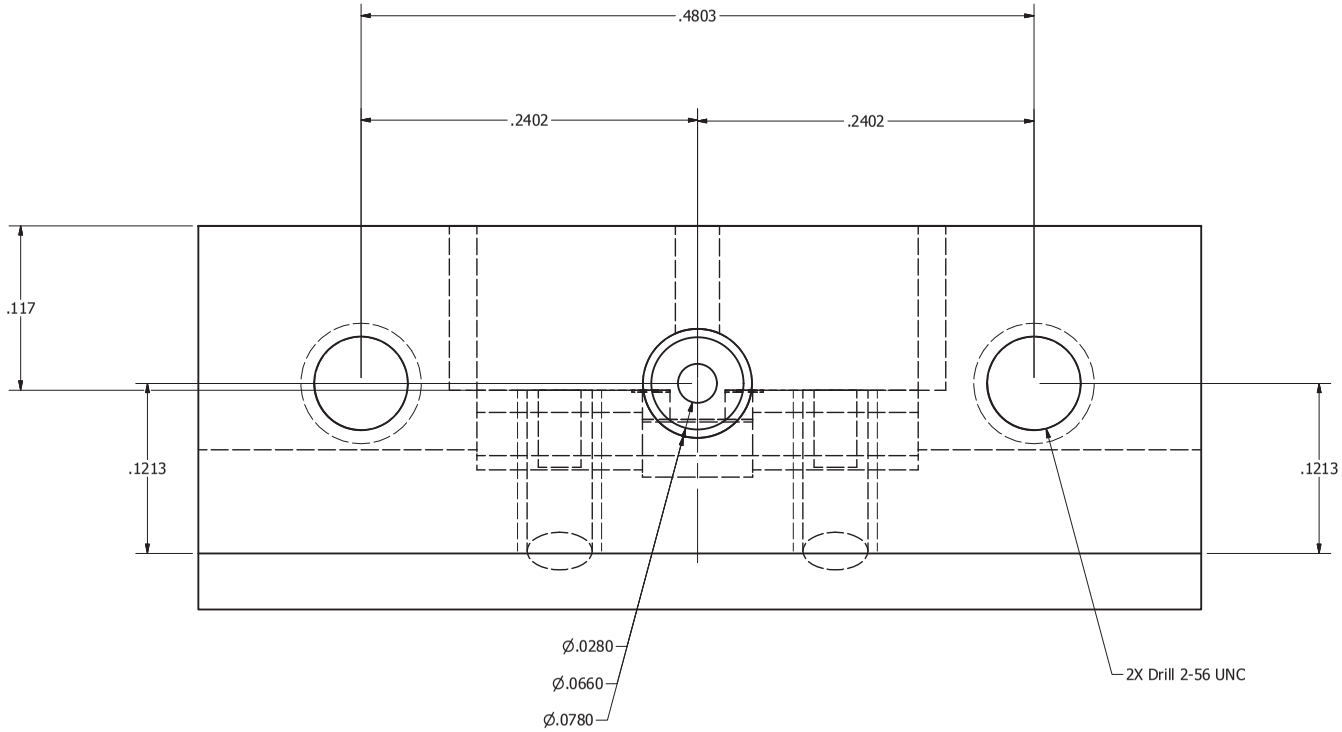
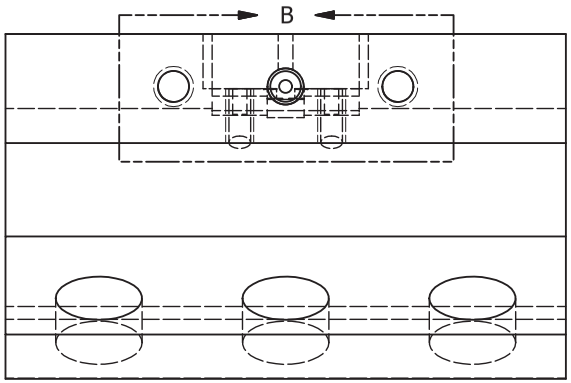
QA				
MFG				
APPROVED		SIZE C	DWG NO depth below channel clarification	REV
		SCALE 5 to 1	SHEET 1 OF 1	

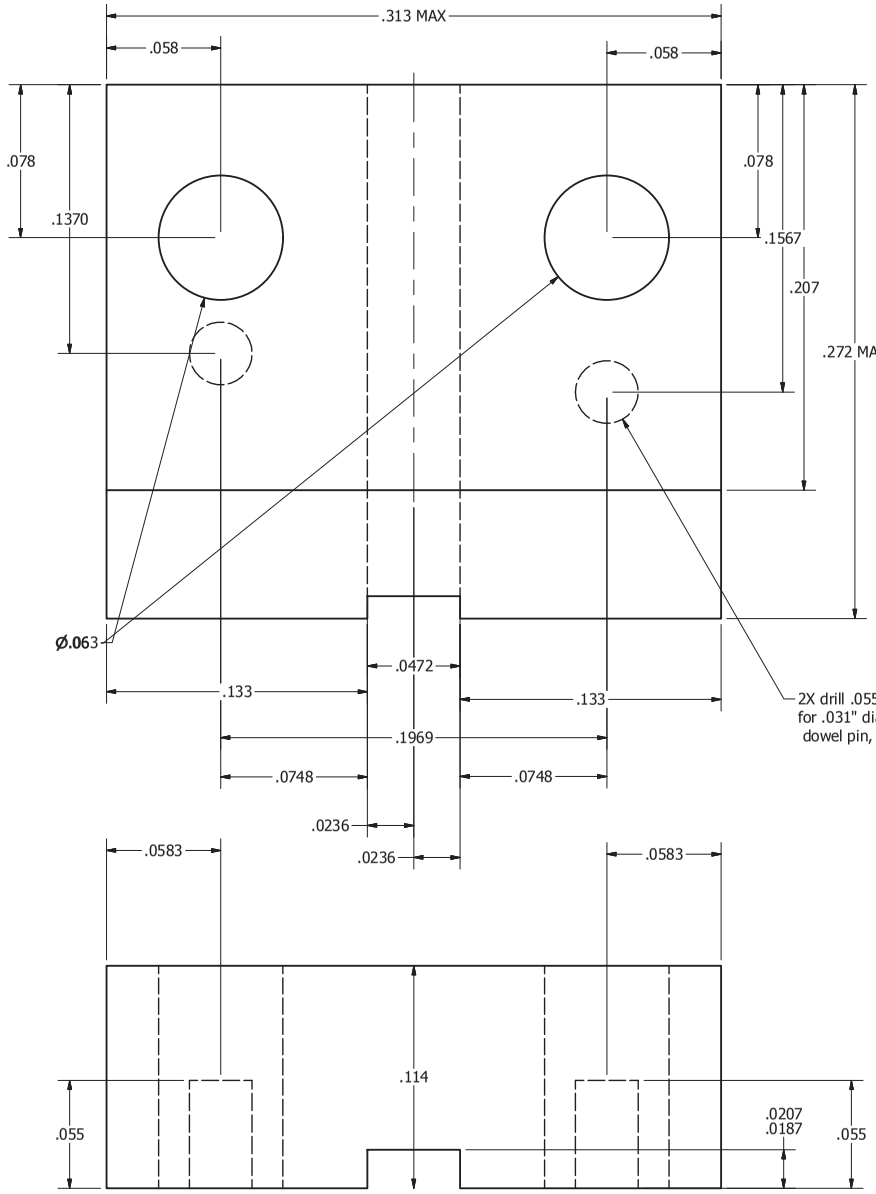


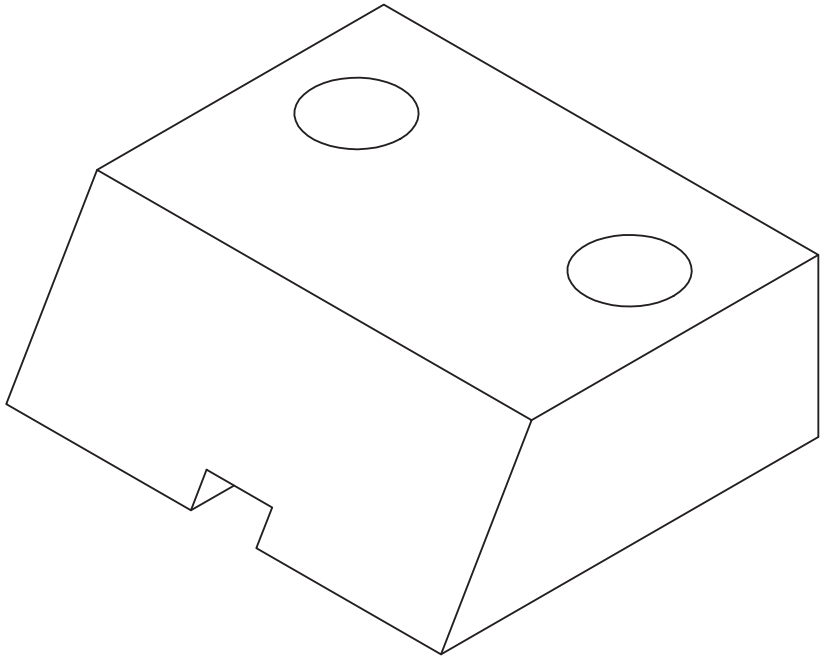
DETAIL B
SCALE 15 : 1

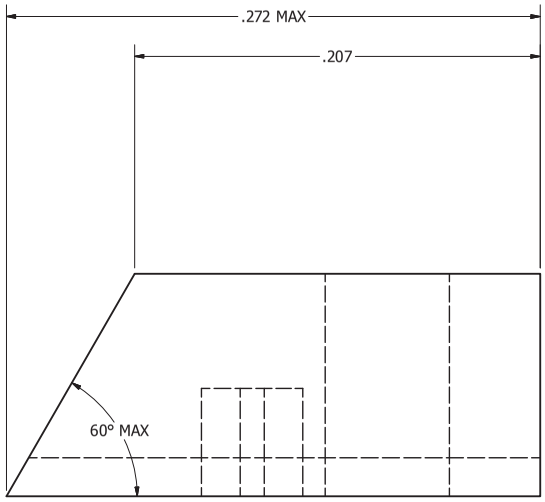


Tolerances unless otherwise specified
.XX +/- .01
.XXX +/- .001
.XXXX +/-.0005

DRAWN HFSSMachine	1/20/2015			
CHECKED		TITLE		
QA				
MFG				
APPROVED				
		SIZE C	DWG NO vconnectorholes	REV
		SCALE 5 to 1	SHEET 1 OF 1	







Tolerances unless otherwise specified
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.XXXX +/-.0005

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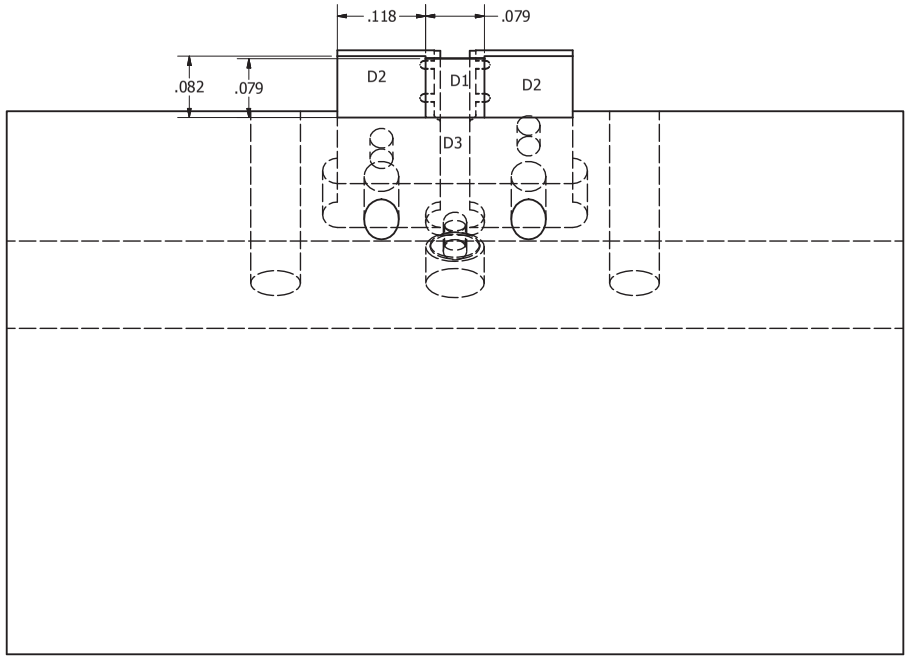
QA		TITLE Gonzalez, Ben: Clamp	
MFG			
APPROVED			
		SIZE C	DWG NO clamp / REV
		SCALE 21 to 1	SHEET 1 OF 1

DEPTHS
D1-0.0
D2-.0059 +/-.0005
D3-.0118 +/-.0005
Tolerances unless otherwise specified
.XXX +/- .001
.XXXX +/-.0005



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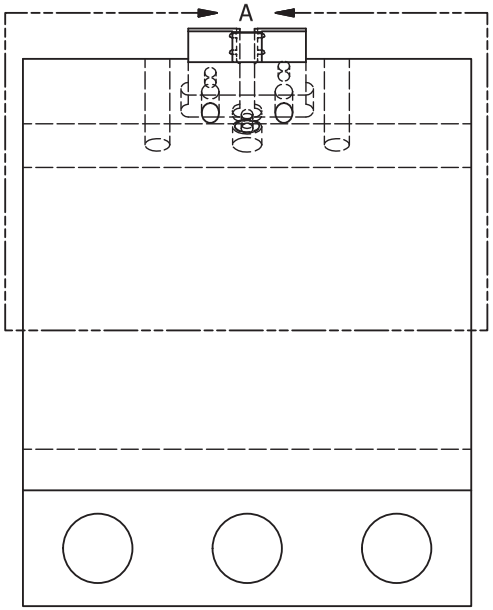

DRAWN HFSSMachine	1/21/2015		
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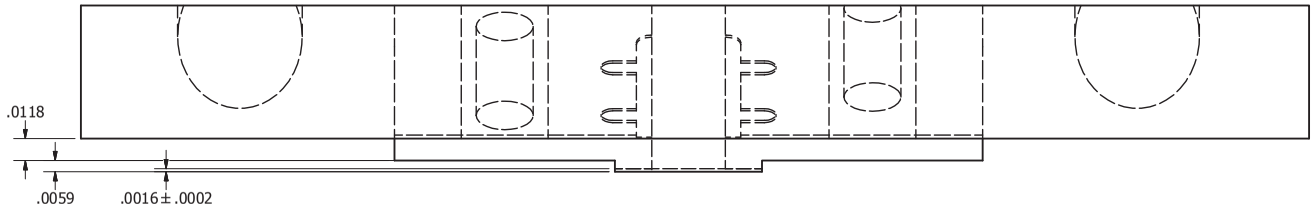
QA			
MFG			
APPROVED		SIZE C	DWG NO bottom_view REV
		SCALE 4 to 1	SHEET 1 OF 1



DETAIL A
SCALE 20 : 1

Tolerances unless otherwise specified
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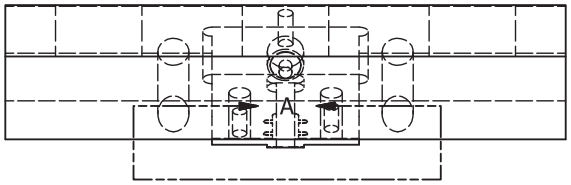
.XXX +/- .005
.XXXX +/-.0005



DRAWN HFSSMachine	1/21/2015			
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QA				
MFG				
APPROVED		SIZE C	DWG NO back_view	REV
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Appendix B Mask Layouts

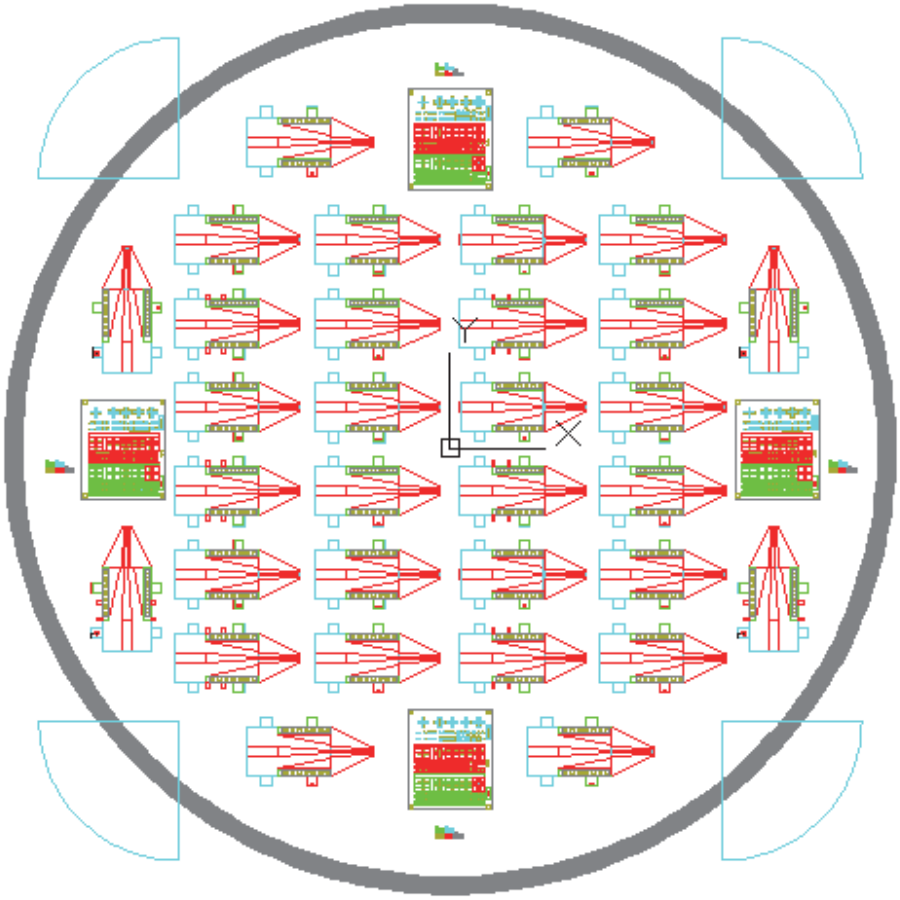

Figure 43: 50 μm Silicon Mask Set

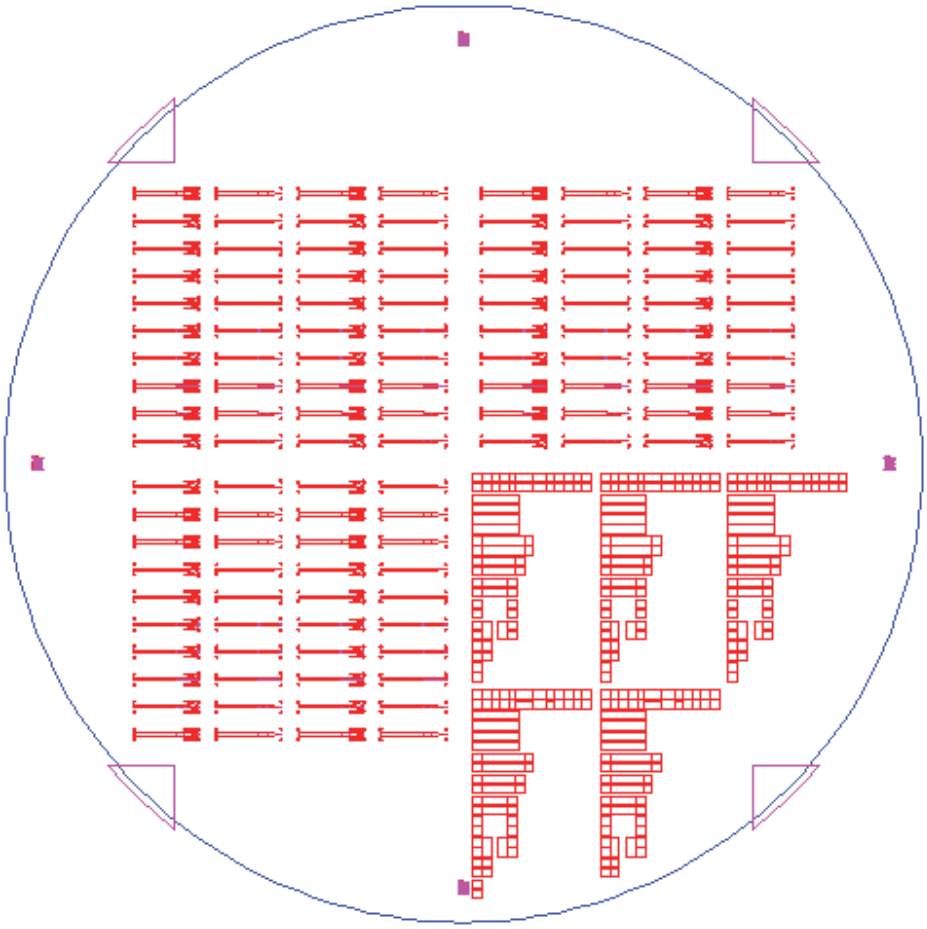

Figure 44: 500 μm Silicon Mask Set