A high precision and low energy Tunable On-Chip Clock Design for In-Textile Computing

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A

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Abstract

The growing demand for wearable electronics within textiles presents unique challenges that require advanced data collection and processing systems embedded in textiles. This requires precise time-stamping among sensor and processing units while ensuring power efficiency. These timing solutions require precise, low-power, and adaptable clock sources essential to support real-time processing and data synchronization across multiple integrated devices. This research introduces a tunable on-chip current-starved ring oscillator, specifically optimized in precision tuning steps and running at sub-threshold weak inversion to achieve ultra-low power for textile applications, addressing the need for power efficiency, accuracy, and adaptability in fabric-based electronics. The oscillator consumes only 170 femtojoules per cycle, a level of efficiency critical for resource-constrained environments such as wearable fabrics.

Operating at 1.1V, the proposed oscillator achieves a frequency range of 88.35 KHz to 108.7 KHz with a tuning step size of 80 Hz (0.08%), providing versatile performance to accommodate a variety of dynamic sensing, processing, and communication tasks inherent to textile-integrated systems. This capability enables adaptive tuning of the clock frequency and resolution to match the changing demands of embedded systems within the fabric, ensuring clock stability and efficiency without compromising power consumption. Demonstrated through integration within an ARM Cortex M0+ SoC, this clock design meets the stringent timing requirements of advanced textile-based wearable applications. The successful implementation of this clock as part of a multi-chiplet SoC system enables robust synchronization of embedded sensors, paving the way for new applications in wearable technology that require precise timing control for complex, fabric-based computing environments.

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Acronyms

$V_{\mathbf{th}}$ Threshold Voltage of Transistor.

BJT Bipolar Junction Transistor.

CAC Central Access Controller.

CMOS Complementary Metal-Oxide-Semiconductor.

COTS Commercial Off Chip Components.

CSRO Current Starved Ring Oscillator.

FLL Frequency Locked Loop.

FVC Frequency to Voltage Converter.

IoT Internet Of Things.

LDO Low Dropout Regulator.

LF Low pass Filter.

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor.

PEX Post-layout parasitic extraction.

PGLA Pattern Generator Logic Analyzer.

PLL Phase Locked Loop.

RO Ring Oscillator.

RTC Real Time Counter.

RXO Relaxation Oscillator.

SoC System-On-Chip.

VCO Voltage-Controlled Oscillators.

VD Voltage Detector.

XO Crystal Oscillator.

Chapter 1

Introduction

In the rapidly evolving field of wearable technology, textile electronics represent a fusion of textile engineering and microelectronics, enabling the seamless integration of electronic functions within fibrous substrates. Textile electronics encompass a wide range of components such as sensors [1], actuators, heaters, coolers, generators, solar cells, LEDs, microfluidic devices, and Microelectromechanical systems (MEMS) [2]. These components, traditionally found in conventional electronic designs, are now being adapted into textile forms, allowing fibers or fiber assemblies to interact with their surroundings through stimuli sensations, actuation delivery, thermal management, energy harvesting and storage, decision making, display, communication, and calculation.

The convergence of textile technologies and electronic engineering has led to the development of textile electronic systems that maintain the inherent characteristics of textiles while enhancing the functionality and performance of integrated electronics. This integration has resulted in wearable electronics that are not only flexible and breathable but also durable and washable, making them suitable for various applications in wearable technology, soft robotics, and extended reality [3]. The initial stages of textile electronics involved the attachment of bulky electronic components to textiles, which compromised their flexibility and comfort. However, advancements in miniaturization and lightweight electronics have enabled the integration of sophisticated electronic functionalities into textiles without sacrificing their comfort [4].

The development of textile electronics involves two primary approaches: processing functional

materials into textile-structured electronic devices [5] and the heterogeneous integration of commercial microelectronics into conventional textiles [6]. This integration has driven innovation in electronic joining and packaging technologies, as well as textile decorative techniques and conductive path printing methods. The result is a seamless blend of textiles and electronics with improved performance and quality, achieved through industrial textile processes such as weaving, knitting, braiding, and nonwoven techniques [3].

On the other hand, the evolution of textiles has been closely linked to the progression of human civilization. From primitive leaf-based clothing to natural fibers like silk and cotton, and eventually, to synthetic materials, textiles have significantly improved human well-being and comfort [7]. In recent years, the demand for high-quality textile products has spurred the development of smart textiles, which possess advanced functionalities such as energy collection, color tuning, health monitoring, shape memory, and heat storage [8]. These smart textiles are classified into passive smart textiles, which sense external conditions; active smart textiles, which respond to external conditions; and ultra-smart textiles, which can sense, react, and adapt to their environment [9].

Smart textiles have found applications in various fields, including medical and health, environmental protection, military, and aerospace. Examples include clothing that regulates temperature, controls muscle vibrations and releases medication or moisturizer into the skin. The continuous advancement in science and technology has enabled the development of more sophisticated smart textiles, which integrate functionalities from disciplines such as artificial intelligence, biotechnology, and information theory. These advancements have led to wearable textile-based personal systems that monitor health, provide protection and safety, and promote a healthy lifestyle [10].

1.1 Historical Context

The integration of technology with textiles, commonly known as E-textiles or textile computing, dates back to the 1850s. Early explorations combined technology with clothing items like corsets and belts [11, 12], laying the foundation for modern E-textiles. Significant progress was made in 1955 with the development of the first wearable computer, sparking interest in embedding

electronic functionalities within clothing [13]. By the early 1990s, advancements in electronics and textile engineering shifted the focus from attaching devices to garments to directly integrating technology within the fabric. Steve Mann, often called the "father of wearable computing," explored both the technological and social implications of this integration, envisioning wearables as essential to daily attire [14]. This evolution has led to advanced smart textiles that extend digital interactivity beyond traditional uses of clothing.

In [4] the evolution of the field of textile computing has been categorized in three phases. The first phase focused on wearable computing, where electronic devices were simply attached to clothing, establishing a foundation for more complex integration. In the second phase, textiles themselves became active components of electronic systems, turning fabric into an integral part of devices. The third phase marked the advent of fiber-level smart textiles, embedding electronic capabilities directly within fibers, as discussed by Cheneral and van Pieterson [15]. This shift toward smaller, more integrated technology suggests a future where fabrics monitor health, respond to environmental changes, and interact with other devices. Stoppa and Chiolerio [16] highlight the need for multidisciplinary collaboration in e-textiles due to the distinct expertise of electronics and textile producers, emphasizing the importance of human comfort and safety.

While wearable computing began in the 1960s, it faced challenges due to the bulkiness of early devices. Advances in miniaturization and conductive fibers, like silver and carbon, allowed sensors, actuators, and microprocessors to be embedded in fabrics, enabling clothing to sense and respond to environmental or wearer needs [17]. By the early 2000s, prototypes of smart garments with heart rate monitors and temperature sensors showcased E-textiles' potential to transform healthcare, fitness, and fashion. Today, modern E-textiles can generate energy, change color, and even self-repair, redefining the role of clothing as an active extension of the wearer [18].

1.2 Advancements in E-textiles

E-textiles, or electronic textiles, represent a significant advancement in integrating electronics with fabrics, enabling clothing to perform functions such as sensing information, storing energy,

and even heating or cooling. Previously distinct engineering domains are now combined into wearable garments that serve applications in healthcare, military, sports, and beyond. The advancement of electronics deployment in textile can be described in sections represented in [19]. The components that build up the E-textile can be categorized as shown in 1.1.

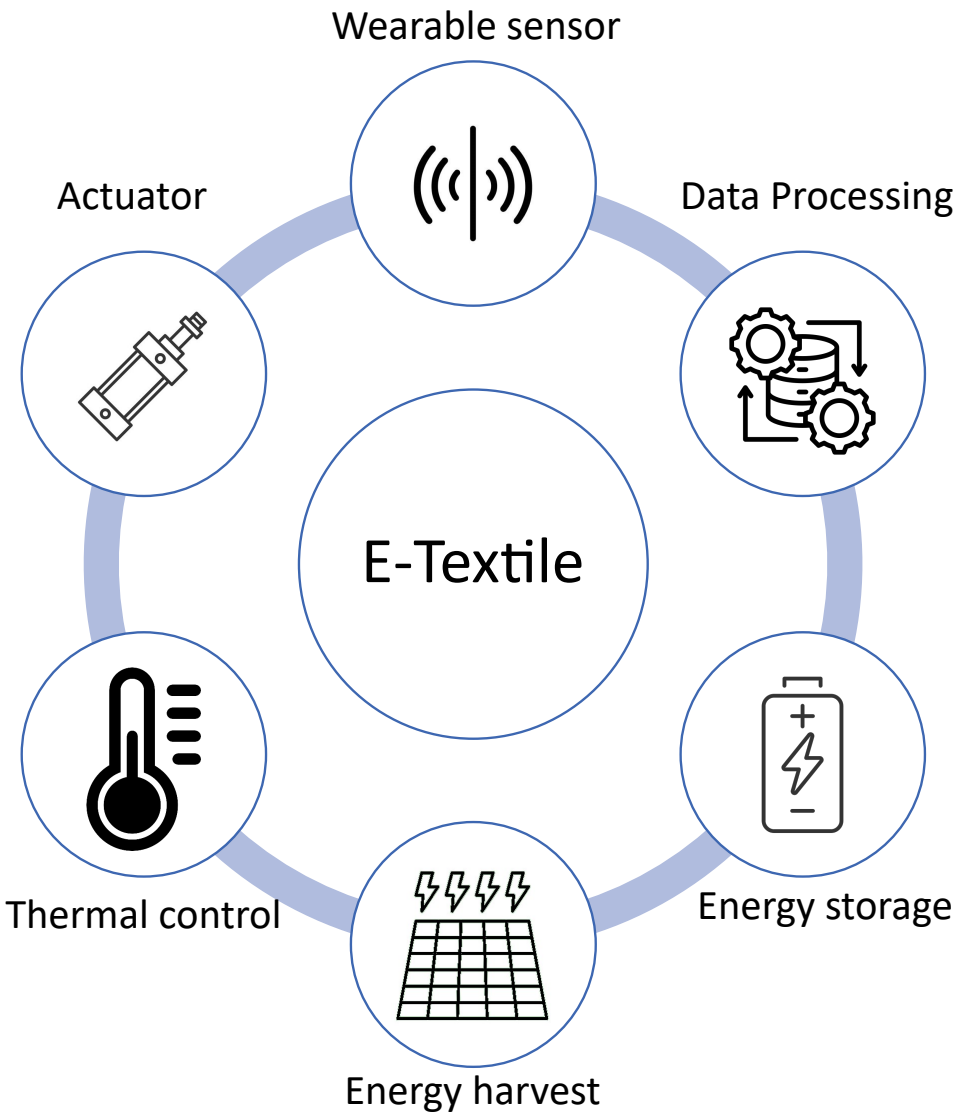


Figure 1.1: Components of E-textile

- **Wearable Sensors:** Specialized sensors embedded within E-textiles are used to detect and monitor various physiological and environmental parameters. Often seamlessly integrated

into the fabric, these sensors operate without being noticed by the wearer. Capable of measuring metrics such as heart rate, body temperature, muscle activity, and sweat chemistry, these sensors utilize conductive fibers to transmit signals through the fabric to small computing devices for analysis.

- **Data Processing:** Data gathered by the sensors must undergo processing to provide meaningful information. This transformation of raw sensor signals into actionable insights is managed by miniaturized computers and processors incorporated within the fabric. Advanced algorithms are employed to analyze data, offer feedback, or activate specific fabric functions. Additionally, data can be wirelessly transmitted to external devices, such as smartphones or computers, for further analysis.

- **Actuators:** Actuators within E-textiles create movement or alter the fabric's shape, enabling functions such as haptic feedback for virtual reality or mobility assistance in medical applications. Actuators can also regulate pressure in therapeutic garments, adapting to the wearer's needs.

- **Energy Storage:** Energy storage solutions, including flexible batteries and supercapacitors, are integrated into E-textiles to power embedded features. These storage solutions are designed to be lightweight and flexible, addressing the limited energy budgets in wearable fabrics.

- **Thermal Control:** Thermal control capabilities are embedded within E-textiles to provide heating or cooling. Heating elements can provide warmth in cold environments or for medical use, while cooling mechanisms utilize specialized materials to dissipate heat, enhancing comfort for the wearer.

- **Energy Harvesting:** E-textiles reduce reliance on external power sources by harvesting energy from the environment. Integrated solar panels harness sunlight, and specialized materials generate power from movement, such as walking or running, enabling continuous operation with minimal external power dependence.

1.3 Motivation

In the requirement for fabrics to be wearable breathable and comfortable while being functional and washable e-textile is moving towards replacing bulky components with miniaturized multi-chip network systems. In multi-chip fabric systems for wearable sensors, precise timing is crucial for accurate time-stamping and synchronization between sensors and processing units across a network. A reliable timing solution is needed in System-On-Chip (SoC) based implementation, especially for SoC-to-SoC and SoC-to-sensor synchronization.

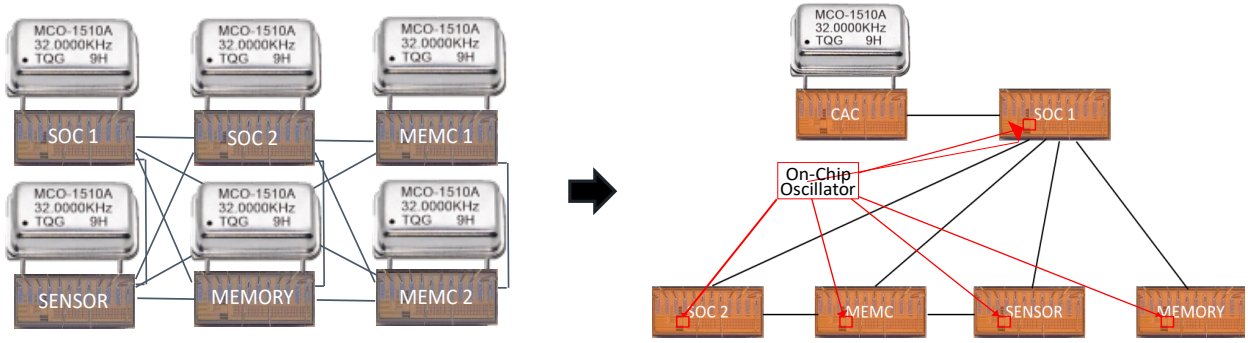


Figure 1.2: Proposed multi-chip network system on fabric.

A 32-bit timer can provide 6 hours of data with 10 μs intervals, leading to the oscillator's frequency on the SOC timer needing to be 100KHz. While commercial crystal oscillators provide stable oscillations resilient to environmental changes, their size (COTS SMD 100kHz component size 3.2mm * 1.5mm [20]) limits their integration into each chip within a compact fabric system. This necessitates a synthesized timing solution.

As on-chip oscillator frequency drifts over time from the target frequency they need to be calibrated for proper time-stamping. Along with that in a multi-chip network, all chips need synchronization for the proper execution of tasks. Using a COTS crystal oscillator for a multichip network becomes obsolete for its bulky size and for which this thesis proposes a system where only one SoC has a crystal oscillator and other SoCs contain on-chip oscillators and they maintain synchronization.

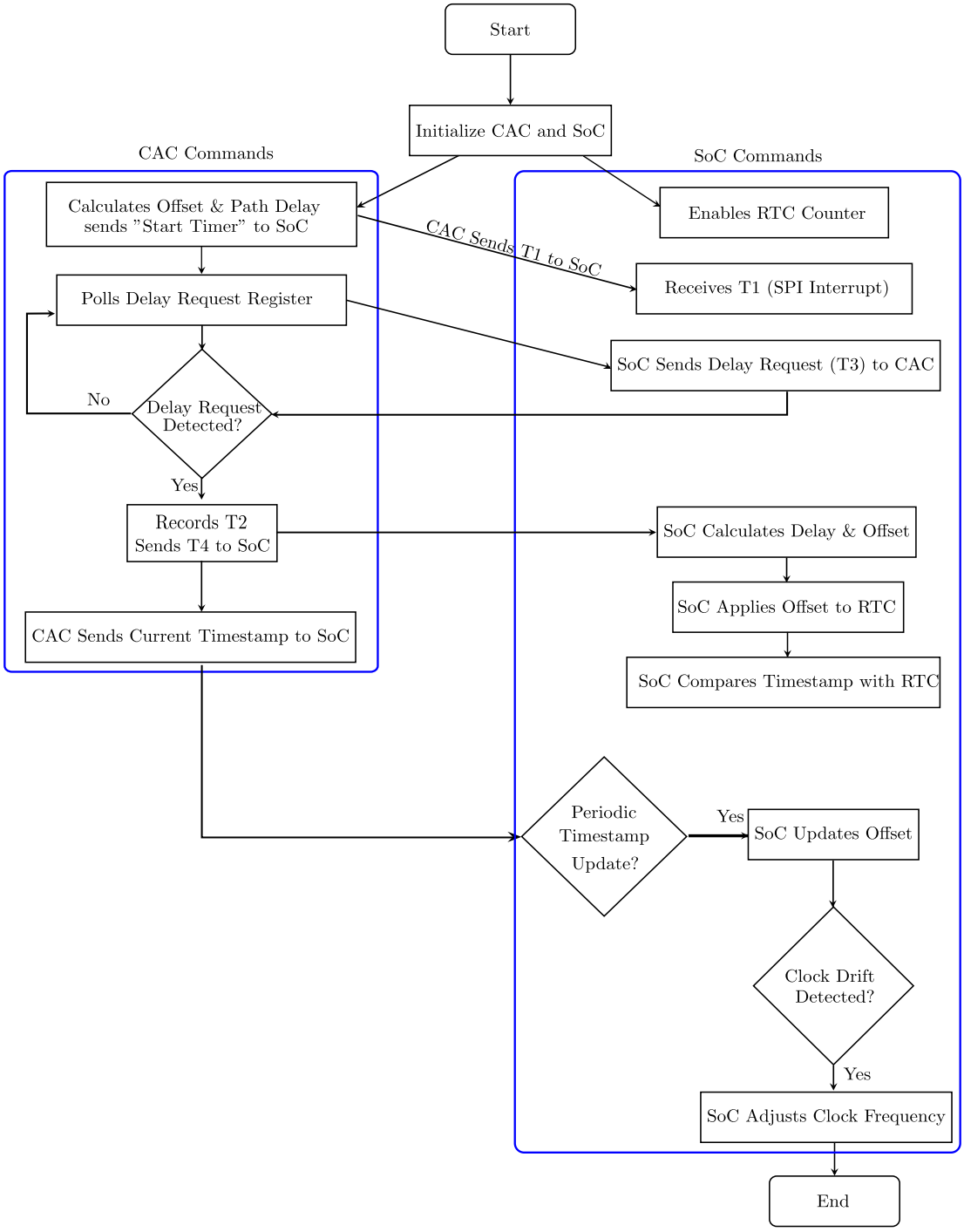


Figure 1.3: Flowchart of timing synchronization

This thesis presents a fabric-integrated timing synchronization system with a central command SoC chip as Central Access Controller (CAC) and other individual SoC's for different purposes. The CAC, operating at 32KHz using COTS, provides timing synchronization to connected SoCs and sensors. Each SoC is equipped with an on-chip oscillator that is controlled by Cortex ARM M0+ digital core and 32kB SRAM, ensuring lightweight operation within the fabric.

The synchronization system flow between CAC and SoC is shown in 1.3. It maintains the SoC's timer within ±100 microseconds of the CAC's clock. During setup, CAC calculates initial timing offsets and path delays. Upon establishing a connection over a 3-wire SPI interface, CAC sends a "Start your timer" command to activate the SoC's Real Time Counter (RTC). This is managed through the RTC control register (RTCCR), and data transfer occurs over an AHB-to-APB bridge. With the RTC active, CAC sends an initial timestamp (T1), prompting the SoC to log it, send a delay request, and exchange timestamps (T1, T2, T3, and T4) for calculating initial delay and offset.

Over time, clock drift may arise due to environmental factors. To counteract this, CAC periodically sends updated timestamps, allowing the SoC to detect and calculate drift. Rather than direct RTC adjustments, the SoC applies an offset based on observed drift to maintain alignment. If persistent drift is detected, the SoC fine-tunes its clock frequency through minor adjustments, compensating for drift without interrupting operations and preserving the ±100-microsecond precision target. So a design that has 1% tuning resolution can suffice a timing synchronization every 100 ms. The objective of this thesis is to fulfill these requirements and provide a compact solution.

1.4 Thesis Statement

1. Design a tunable oscillator that fulfills the key requirements outlined in the 1.3 addressing configurable frequency, low power consumption, and compact area, making it suitable for the in-textile computing application.

2. Analyze the oscillator's relevant metrics to evaluate its performance

3. Assess the oscillator's performance across varying operational conditions to verify its relia-

bility and effectiveness in practical applications.

4. Integrate the oscillator within a System-On-Chip (SoC) to assess its suitability for real-time, time-sensitive applications requiring precise frequency control.

1.5 Evaluation Matrices

Upon addressing the key requirements outlined in the 1.3, the design specification and evaluation matrices are needed to be chosen. This calls upon the requirement for analyzing previous works done in tunable oscillator design.

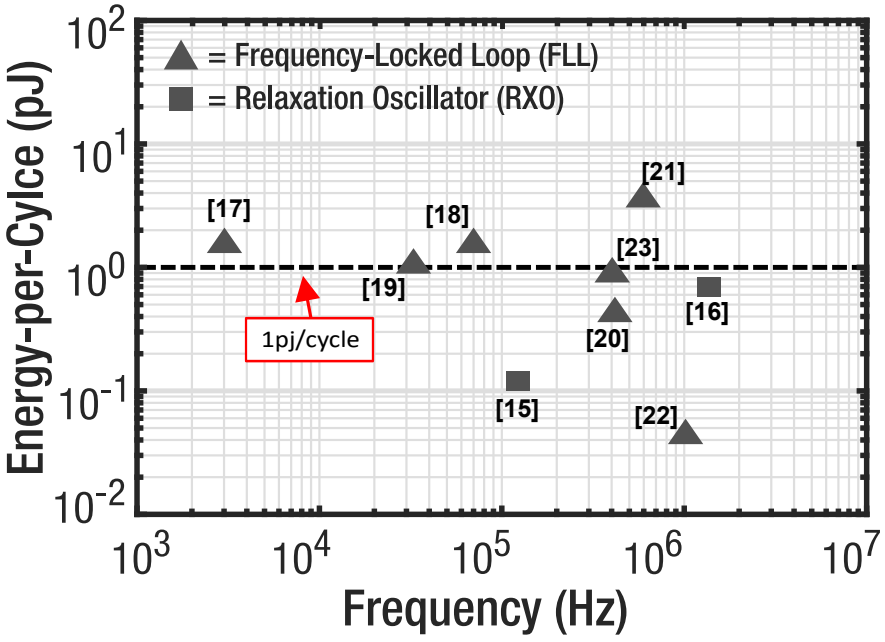


Figure 1.4: Previous work: Energy per cycle (pj/cycle) vs Frequency (Hz).

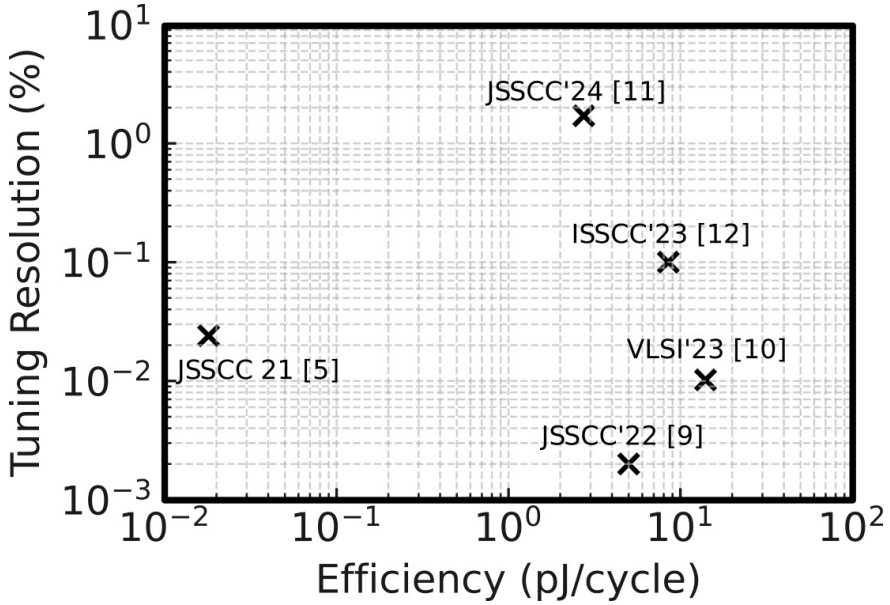


Figure 1.5: Previous work: Tuning resolution vs energy efficiency.

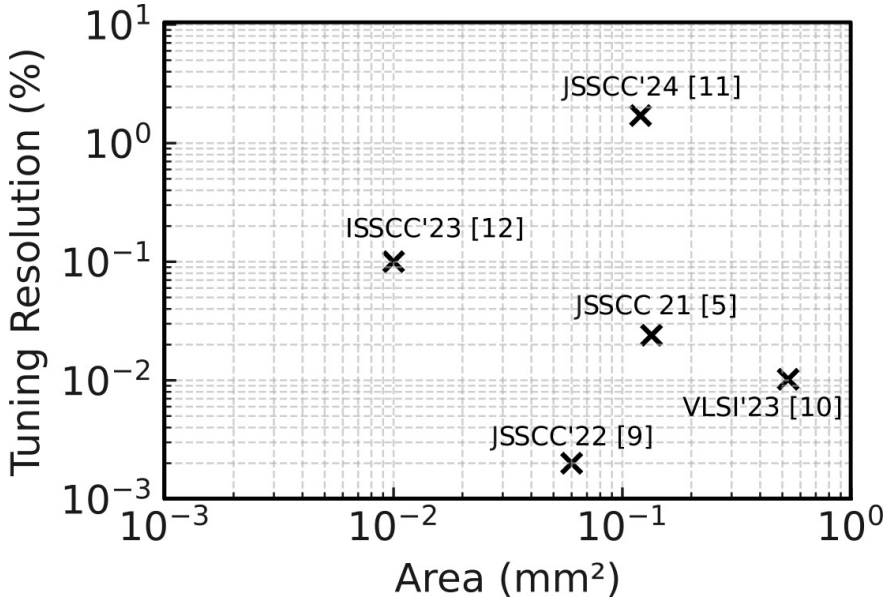


Figure 1.6: Previous work: Tuning resolution vs Area (mm^2).

From Figure 1.4 [21–29], we can see most of the previous works have targeted achieving 1pj/-cycle energy efficiency. From Figures 1.5 and 1.6 [30–34], we observe that adding tunability to an on-chip oscillator increases area and power consumption. To address the requirements of this

thesis, the following specifications have been targeted for the design.

Design	VDD (V)	Frequency Max (kHz)	Frequency min (KHz)	Tuning step resolution in %	Power consumption (nW)	Energy per cycle (pj/cycle)
Spec	1.1-1.2	>100	<100	<0.1	<100	<1

Table 1.1: Targeted design spec.

Chapter 2

Literature Review

Before exploring the design of the tunable on-chip oscillator, it is essential to provide a theoretical overview of foundational circuit components and oscillator architectures. This discussion will cover the principles of current mirror circuits and examine a range of oscillator types, including Crystal Oscillator (XO), Voltage-Controlled Oscillators (VCO), RC Oscillator, LC oscillators, Relaxation Oscillator (RXO), Frequency Locked Loop (FLL), and Ring Oscillator (RO). By establishing a strong grasp of these components, this overview aims to enhance understanding of the fundamental building blocks that play a critical role in oscillator design. Furthermore, it will assist in evaluating and selecting the most suitable architecture for achieving the desired characteristics in a tunable on-chip oscillator, ensuring both performance and efficiency in the final design. Different types of oscillators are categorised below.

2.1 Different types of Oscillators

2.1.1 Crystal Oscillator

Crystal oscillators are among the most widely used oscillators, known for their excellent frequency stability, precision, and low phase noise. They operate based on the mechanical resonance of a quartz crystal, which vibrates at a highly predictable frequency when an electric field is ap-

plied. Due to this natural resonance, crystal oscillators maintain a stable oscillation frequency, which is ideal for applications requiring highly accurate timing, such as in clocks, communication systems, and microprocessors. For crystal oscillators, the oscillation frequency f is determined by the crystal's natural resonance frequency (f), which can be approximated as:

The Series Resonant Frequency f_S of a crystal can be writen as [35]:

$$f_S = \frac{1}{2\pi\sqrt{L_S C_S}} \tag{2.1}$$

where:

- L_S is the equivalent inductance of the crystal,
- C_S is the equivalent capacitance of the crystal.

The parallel resonance frequency, f_p, occurs when the reactance of the series LC leg equals the reactance of the parallel capacitor, C_p, and is given as [35]:

$$f_p = \frac{1}{2\pi L_S\sqrt{\frac{C_p C_S}{C_p+C_S}}} \tag{2.2}$$

However, despite their high stability, crystal oscillators face challenges when it comes to integration and tunability. Quartz crystals are typically external components, making them less compatible with monolithic integration into standard Complementary Metal-Oxide-Semiconductor (CMOS) technology. This limitation restricts their use in applications where compact, on-chip solutions are preferred, particularly in highly integrated electronic devices and SoC.

2.1.2 Voltage-Controlled Oscillators (VCO)

Voltage-controlled oscillators are another popular type, where the oscillation frequency is tuned by varying a control voltage. VCOs are commonly used in applications requiring frequency agility, such as Phase Locked Loop (PLL)s, frequency synthesizers, and communication systems where frequency adjustment is necessary.

In VCOs, the output frequency f is a function of the control voltage V_{control}. For a simple linear VCO, this relationship can be expressed as:

$$f = f_{\text{min}} + K_v \cdot V_{\text{control}} \tag{2.3}$$

where:

- f_{min} is the minimum oscillation frequency,
- K_v is the VCO gain, representing the frequency change per unit of control voltage (H_z/V).

VCOs typically offer a broader tuning range than crystal oscillators, providing a measure of frequency flexibility. However, achieving high-frequency stability in VCOs can be challenging, as they are sensitive to power supply variations, temperature fluctuations, and inherent circuit noise. While integration into CMOS is more feasible with VCOs than with crystal oscillators, maintaining high stability across a wide tuning range requires additional design complexity and sometimes compromises stability for tunability. To explore the suitability and applications of various oscillators as on-chip solutions, the following subsections will provide a detailed analysis of different on chip oscillators in integrated circuit design.

2.1.2.1 RC Oscillator

RC Oscillator use resistors and capacitors to set their oscillation frequency and are often used when moderate frequency accuracy and low-cost integration are priorities. A few examples include the Wien bridge and phase-shift oscillators, which can be fully integrated into CMOS technology. RC Oscillator while simple and cost-effective, face challenges in precision tuning due to component variations, limited tuning resolution, and temperature sensitivity. These limitations stem from their reliance on resistors and capacitors, which are prone to manufacturing tolerances and environmental influences. In contrast, Ring Oscillator (RO), built with digital logic gates, offers advantages in precision tuning. Their voltage-controlled nature allows for fine-grained frequency adjustments, while their digital implementation provides better stability and easier integration with

digital control systems. This makes ring oscillators well-suited for applications demanding precise and stable frequency control, despite potential drawbacks like higher phase noise and power consumption.

For RC Oscillator, the oscillation frequency f is determined by the resistor and capacitor values. In the case of a simple Wien Bridge Oscillator, the frequency is similar to equation 2.1. In a Phase-Shift RC Oscillator, where three RC stages are used in series, the oscillation frequency can be expressed as:

$$f = \frac{1}{2\pi RC\sqrt{2N}} \tag{2.4}$$

RC Oscillator face notable limitations in integration and efficiency, especially in CMOS technology. RC oscillators typically suffer from higher phase noise due to the inherent instability in resistor-capacitor networks, making them less ideal for applications requiring low noise and precise timing. Additionally, achieving higher frequencies in RC oscillators often leads to increased power consumption since a higher current is required, limiting their suitability for low-power applications. In contrast, CSROs provide more efficient power management through current regulation, maintaining both low power and stable performance. Furthermore, RC oscillators demand significant chip area due to large capacitors at lower frequencies, and achieving tight resistor tolerances is challenging in CMOS processes, complicating precise frequency control. These issues can be mitigated using a CSRO however, which is more compact, easily integrable in CMOS, and allows for finer frequency adjustment through current regulation, making them a more space-efficient and adaptable choice for highly integrated circuits.

2.1.2.2 LC Oscillators

LC oscillators use inductors (L) and capacitors (C) to generate oscillations based on resonance, offering good frequency stability and low phase noise, especially useful in RF applications. Although more integrable than crystal oscillators, LC oscillators are still less compact and power-efficient than ring oscillators because inductors consume significant chip area. Achieving fully integrated LC oscillators in CMOS can be challenging, especially as applications demand more compact designs. The frequency is similar to equation 2.1.

2.1.2.3 Relaxation Oscillator (RXO)

Relaxation oscillators generate oscillations based on the charging and discharging of a capacitor and are often used in low-frequency applications. A basic relaxation oscillator typically consists of a reference current source, a load capacitor, and a comparator with feedback connected to the load capacitor as a reset mechanism. The equation of the frequency can be depicted as:

$$F_{\text{out}} = \frac{1}{2 * R_{\text{ref}} * C_L} \tag{2.5}$$

Where R_{ref} is the reference resistor used in the biasing current generator and CL is the load capacitor. However, using a Relaxation Oscillator (RXO) is less efficient for designs in the KHz-MHz range due to its high reference current requirements in the biasing circuit, which increases power consumption. Additionally, if the biasing circuit includes an amplifier, the comparators delay further impacts the frequency, adding complexity to the design. In contrast, a Current Starved Ring Oscillator (CSRO) can generate similar frequencies with significantly lower power consumption, making it a more efficient alternative.

2.1.2.4 Frequency Locked Loop (FLL)

Frequency Locked Loop (FLL) are specialized oscillators used for maintaining frequency stability by locking onto an external reference frequency, adjusting the oscillator's frequency to match the reference which is generally used for frequency synthesis. With certain modifications, such as implementing voltage error detection and a frequency-to-voltage converter instead of a frequency reference, an output frequency can be generated using an on-chip voltage reference.

Figure 2.1 depicts the architectures of a FLL which are comprised of Frequency/Voltage error detection (Frequency to Voltage Converter (FVC),Voltage Detector (VD)), Low pass Filter (LF), VCO (RO, RXO etc) and Frequecy divider ($1/N$, N=divider number).

FLL generally provide strong frequency stability and control; however, they are less commonly integrated into fully CMOS-based designs due to their complexity. Additionally, reliance on an external reference limits their use in fully autonomous systems where external signals are not available. FLLs without a reference frequency face significant challenges in frequency generation

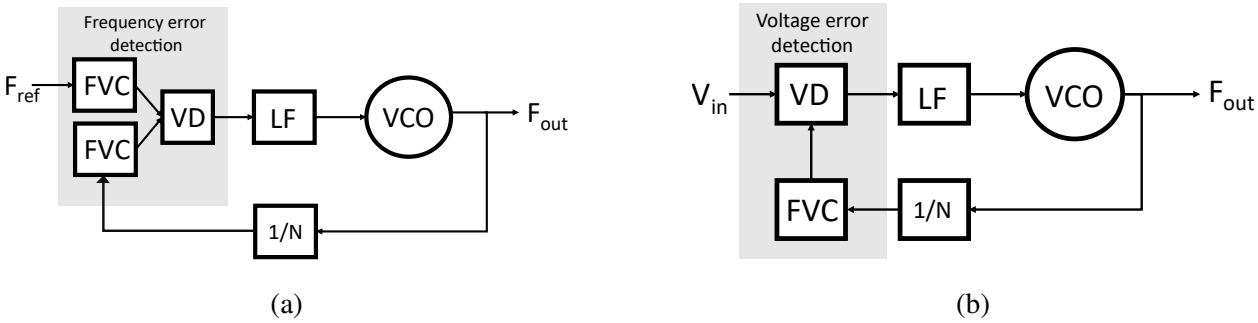


Figure 2.1: (a) Frequency-Locked Loop (FLL) architecture for frequency synthesis. (b) Frequency-Locked Loop for frequency generation

compared to ring oscillators. FLLs often require complex compensation and calibration circuitry, adding to power consumption and system costs. Their lock time is also typically longer, limiting their use in applications needing quick frequency response. Additionally, without a reference, FLLs are more sensitive to noise, leading to further instability. In contrast, ring oscillators provide a simpler, faster, and more power-efficient solution, especially in applications where absolute frequency stability isn't critical.

2.1.2.5 Ring Oscillator (RO)

Ring Oscillator (RO) come in various forms, including single-ended ring oscillators, Differential ring oscillators, Multiphase ring oscillators, and Current Starved Ring Oscillator (CSRO). Among these, CSRO are often the preferred choice due to their superior frequency control and power efficiency. By regulating current in each stage, CSRO allow for precise tuning while significantly reducing power consumption and minimizing sensitivity to power supply fluctuations. This makes them particularly well-suited for applications that demand both efficient power usage and high-frequency stability.

2.2 Comparison between different oscillators

In table 2.1 a comprehensive comparison table is shown. The table shows that the Current Starved Ring Oscillator (CSRO) is ideal for on-chip applications due to its high tunability, low power consumption, and compact area. By controlling the current at each stage, it achieves efficient frequency adjustments without large components, making it highly space-efficient. This design enables fine-tuning of frequency over a broad range, which is essential for applications needing adaptable timing.

Additionally, its low power operation makes it particularly suitable for battery-powered and energy-sensitive devices, such as E-textile systems. Overall, the current-starved ring oscillator offers a reliable and efficient solution for applications that demand both compact design and low power consumption. Building on these advantages, this thesis will focus on designing a tunable Current Starved Ring Oscillator (CSRO) that meets specific performance criteria outlined in the initial requirements.

Oscillator Type	Frequency Stability	Power Consumption	Phase Noise	Area Consumption	Tunability	Advantages	Disadvantages
Crystal Oscillator	Very High	**Low**	Very Low	High	**Low**	High accuracy and stability	High area consumption, **Low tunability** , Slow start-up.
RC Oscillator	Low	**Low**	Moderate to High	Low	**Moderate**	Simple, low-cost	Larger Component Size, **Limited Tuning Capability,** Higher Power Consumption.
LC Oscillator	Moderate to High	**Medium**	Low to Moderate	High	**Moderate**	Good phase noise performance	Bulky and high area consumption, **Power consumption** , Limited tuning range.
Relaxation Oscillator	Low	**Very Low**	High	Low	**Low**	Simple design, very low power	Higher Noise and Jitter, **Very limited tunability** , Limited precision for low power.
Frequency Locked Loop (FLL)	High	**Medium to High**	Low	High	**High**	Excellent frequency stability with feedback	High area consumption, **High power consumption, Complex tuning requirements** .
Ring Oscillator (Current-Starved)	Moderate	**Low**	Moderate to High	Very Low	**High**	Compact, **highly tunable,** low area **and power**	Sensitive to temperature, Moderate phase noise.

Table 2.1: Comparison of different types of oscillators

Through targeted modifications, the proposed design aims to achieve high precision in tuning steps, providing adjustable frequency control without compromising power efficiency. This approach ensures that the oscillator can adapt to application demands, maintaining both energy efficiency and accuracy, which are essential for resource-constrained environments like textile computing systems.

2.3 Design Principles of CSRO

Current Starved Ring Oscillator (CSRO) is comprised of 3 section which can be seen in 2.2. First is reference current generation, secondly ring oscillator stages and third is buffer. Usually the bias is offen referenced from a precise biasing circuit such as Bandgap reference circuit or LDO. Using difference current mirror techniques the reference is distributed for different purposes in the oscillator such as tuning control and current control of the Ring Oscillator (RO) inverter bruches.

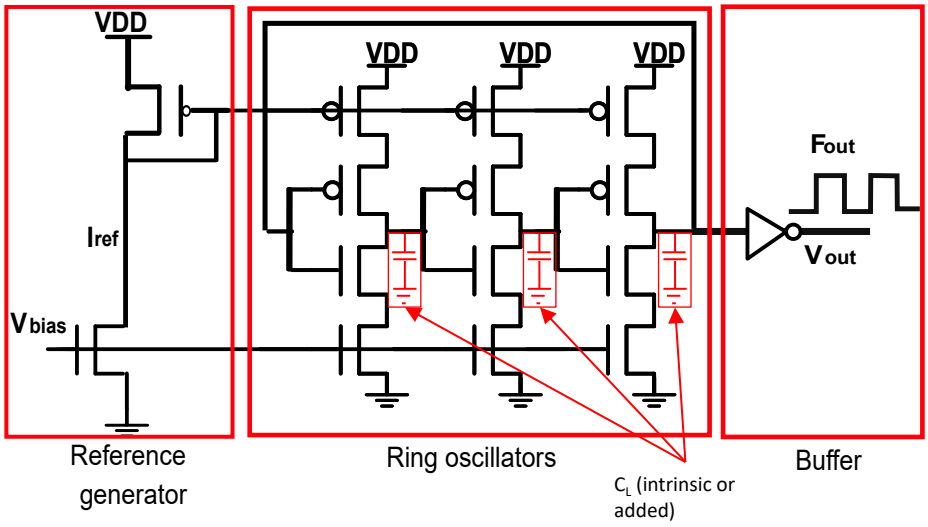


Figure 2.2: Basic Current Starved Ring Oscillator design

2.3.1 Current mirror

Current mirrors are fundamental building blocks in analog circuit design, providing a stable and replicable current source across various electronic applications. They are widely utilized for biasing and as active loads in differential amplifiers, voltage references, and Operational Transconductance Amplifiers (OTA). This section reviews the development, principles, and types of current mirrors, emphasizing their importance in modern analog design.

2.3.1.1 Basic Principles of Current Mirrors

A current mirror is a circuit configuration that replicates (mirrors) an input current at an output node, maintaining a constant current over a range of load conditions. The basic current mirror consists of two matched transistors, typically acrfullmosfet or Bipolar Junction Transistor (BJT). The fundamental principle is that if two identical transistors are kept at the same gate-source voltage (MOSFET) or Base-emitter voltage (BJTs), the current flowing through them will be equal. The behavior of current mirrors can be described for two main operating regions: Saturation (strong inversion) and Subthreshold (weak inversion).

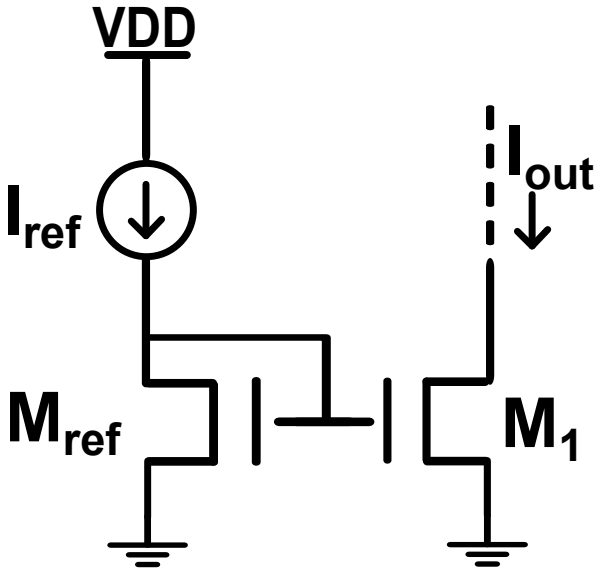


Figure 2.3: Current Mirror Circuit using NMOS transistors

Current Mirrors in Saturation (Strong Inversion)

In a MOSFET-based current mirror, the output current I_{out} is designed to match the input current I_{ref}, assuming ideal conditions. The key equation governing the behavior of a MOSFET current mirror can be expressed as:

$$I_D = \frac{1}{2}\mu_n C_{\text{ox}} \frac{W}{L}(V_{\text{GS}} - V_{\text{th}})^2 \tag{2.6}$$

where:

- μ_n is the electron mobility,
- C_{ox} is the gate oxide capacitance per unit area,
- W and L are the channel width and length of the MOSFET,
- V_{GS} is the gate-source voltage, and
- V_{th} is the threshold voltage.

If we assume that two transistors (M_{ref} and M_1 in Figure 2.3) are identically matched and operate at the same gate-source voltage, we can assume the relationship to be:

$$I_{D1} \propto I_{REF} \cdot \left(\frac{W}{L}\right) \tag{2.7}$$

From this by eliminating identical parameters and simplify them to:

$$I_{D1} = \left(\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_{\text{REF}}}\right) I_{\text{REF}} \tag{2.8}$$

where:

- $\left(\frac{W}{L}\right)_1$ is the width-to-length ratio of the output transistor,
- $\left(\frac{W}{L}\right)_{\text{REF}}$ is the width-to-length ratio of the reference transistor.

This equation highlights that the output current is proportional to the reference current, scaled by the aspect ratios of the two transistors. For accurate current mirroring, precise matching of the transistor parameters (W/L ratios) is crucial. Any mismatch can lead to variations in the output current, which affects the performance of the entire circuit.

Current Mirrors in Subthreshold (Weak Inversion)

In the subthreshold region, where the gate-source voltage V_{GS} is below the threshold voltage V_{th}, the drain current exhibits an exponential dependence on V_{GS}. The drain current I_D in this region is described by [35–37]:

$$I_D = I_{D0} \exp\left(\frac{V_{GS}}{\eta V_T}\right) \tag{2.9}$$

where:

- I_{D0} is a pre-exponential factor dependent on process and device parameters,
- V_T is the thermal voltage (approximately 26 mV at room temperature),
- η is the subthreshold slope factor, where η is typically greater than 1 and denoted as ,

$$n = 1 + \frac{C_{\text{dep}}}{C_{\text{ox}}} \tag{2.10}$$

where:

- C_{dep} is the depletion layer capacitance,
- C_{ox} is the oxide capacitance.

So, for non-identical transistors (different W/L ratios), the relationship adjusts to:

$$I_{D1} = \left(\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_{\text{REF}}}\right) I_{\text{REF}} \tag{2.8}$$

The equation solves to the same equation 2.8 for saturation region which shows that even in the subthreshold region, the current mirror operates with a proportional scaling based on the

aspect ratios. The exponential relationship allows for ultra-low-power operation, which is useful in applications such as low-power analog circuits and subthreshold digital systems. The operation of current mirrors in the subthreshold region emphasizes low leakage and efficient current scaling.

2.3.1.2 Types of Current Mirrors

Over the years, several variations of current mirrors have been developed to improve performance in terms of accuracy, output impedance, and temperature stability. Key types include:

Simple Current Mirror

The simplest current mirror consists of two identical MOSFETs, which is described in section 2.3.1.1. While this configuration is easy to design and implement, it suffers from limitations such as finite output impedance and sensitivity to transistor mismatch. The output impedance can be expressed as [36]:

$$r_{\text{out}} = \frac{1}{g_{ds}} \tag{2.11}$$

where g_{ds} is the conductance of the MOSFET. Higher output impedance is desirable as it enables better current replication.

Cascode Current Mirror

To address the limitations of the simple current mirror, the cascode current in Figure 2.4 mirror introduces an additional pair of transistors to increase the output impedance, thereby reducing the dependence on the output voltage.

Wilson Current Mirror

The Wilson current mirror (Figure 2.5) adds a feedback mechanism to compensate for transistor mismatches, improving current matching and reducing the error. This configuration also boosts the output impedance, which can be approximated as [36]: While effective, the design can be more complex and may introduce stability concerns, especially in high-frequency applications.

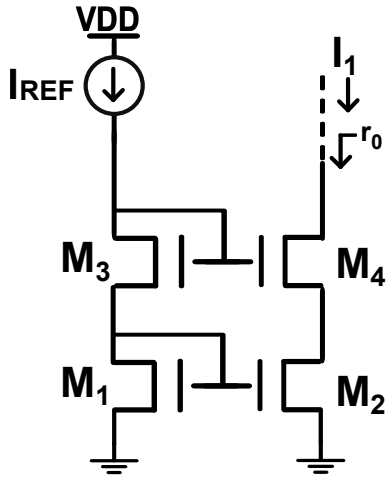


Figure 2.4: Cascode current mirror

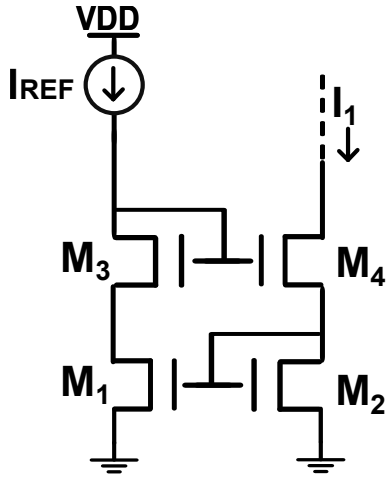


Figure 2.5: Wilson current mirror

Current Steering

Current steering is a technique commonly used in analog circuits to distribute or control current across multiple branches. By leveraging the properties of current mirrors, designers can guide current into different paths, making this technique essential for digital-to-analog converters (DACs), mixers, and other applications where precise current control is necessary.

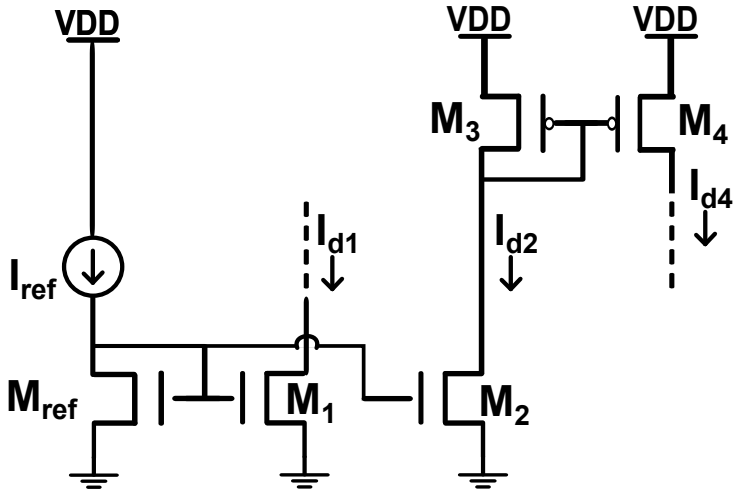


Figure 2.6: Current Steering circuit

In a multi-branch current steering configuration, a reference current IREF is replicated and steered into four separate branches using current mirrors. This allows for precise control over the currents I_1 , I_2, I_3, and I_4 flowing in each branch. The currents in the four branches can be defined as:

$$I_1 = \alpha_1 I_{\text{REF}}, \quad I_2 = \alpha_2 I_{\text{REF}}, \quad I_3 = \alpha_3 I_{\text{REF}}, \quad I_4 = \alpha_4 I_{\text{REF}} \tag{2.12}$$

where:

- α_1, α_2, α_3, and α_4 are scaling factors that determine how much of the reference current is steered into each branch. These factors are typically determined by the width-to-length ratios (W/L) of the transistors in each branch.
- If the transistors are matched but have different (W/L) ratios, the scaling factors can be expressed as:

$$\alpha_i = \frac{\left(\frac{W}{L}\right)_i}{\left(\frac{W}{L}\right)_{\text{REF}}} \tag{2.13}$$

where i denotes each of the branches (1, 2, 3, 4). This means the current in each branch is directly proportional to the reference current and the design of each individual transistor.

$$I_i = \frac{\left(\frac{W}{L}\right)_i}{\left(\frac{W}{L}\right)_{\text{REF}}} I_{\text{REF}}, \quad \text{for } i = 1, 2, 3, 4 \tag{2.14}$$

So in Figure 2.6, the equation for I_{D4} becomes:

$$I_{D4} = \frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_4} \times \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_{\text{ref}}} I_{\text{REF}} \tag{2.15}$$

In this way, current steering provides flexibility in analog designs, allowing for dynamic control of currents by varying the (W/L) ratios or by switching on/off different branches. It can also be used to implement complex analog functions like multiplication, mixing, and waveform generation.

2.3.2 Design Challenges and Considerations

The accuracy of a current mirror is affected by factors such as channel length modulation, mismatch in threshold voltages, and process variations. For instance, the effect of channel length modulation introduces a dependence of I_{D1} on the drain-source voltage V_{DS}, deviating from the ideal behavior. Due to channel length modulation, the drain current becomes sensitive to changes in the drain-source voltage ΔV_{DS}. This effect can be described by introducing a parameter λ, which captures the variation:

$$I_{D1} + \Delta I_{D1} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_{\text{REF}}} I_{\text{REF}} \left(1 + \lambda \Delta V_{DS}\right) \tag{2.16}$$

where:

- ΔI_{D1} represents the change in the drain current due to channel length modulation,

- λ is the channel length modulation parameter, and
- ΔV_{DS} is the variation in the drain-source voltage.

The parameter λ reflects how the output current I_{D1} is no longer perfectly constant but increases with higher V_{DS}. This deviation can lead to inaccuracies in the mirrored current, especially in circuits where the transistor output operates over a wide range of voltages. In short channel weak inversion, perfect matching can not be achieved if *L* is varied. So keeping *L* constant for all mosfet and incorporating equation 2.16 with equation 2.15 we get:

$$I_{D4} = \frac{W_3}{W_4} \cdot \frac{(1 + \lambda V_{DS_3})}{(1 + \lambda V_{DS_4})} \cdot \frac{W_2}{W_{\text{ref}}} \cdot \frac{(1 + \lambda V_{DS_2})}{(1 + \lambda V_{DS,\text{ref}})} \cdot I_{\text{REF}} \tag{2.17}$$

To mitigate these effects, designers may use techniques such as increasing the channel length L, which reduces the value of λ and, consequently, the sensitivity to V_{DS}. Additionally, employing cascode configurations can significantly increase the output impedance, effectively minimizing the influence of V_{DS} variations and providing a more stable current mirror output.

2.3.3 Architecture of Current Starved Ring Oscillator (CSRO)

The oscillation frequency of a CSRO depends on the delay through each inverter stage. The design of a CSRO must carefully consider the number of stages, current control, and supply voltage.

The fundamental frequency f_{osc} of a CSRO with N stages and a per-stage delay τ is given by:

$$f_{\text{osc}} = \frac{1}{2 \cdot N \cdot \tau} \tag{2.18}$$

where the per-stage delay τ depends on the controlled current I_{ctrl} as:

$$\tau = \frac{C_L \cdot V_{DD}}{I_{\text{ctrl}}} \tag{2.19}$$

where C_L is the load capacitance, V_{DD} is the supply voltage, and I_{ctrl} is the tunable current.

Substituting the delay into the frequency equation gives:

$$f_{\text{osc}} = \frac{I_{\text{ctrl}}}{2 \cdot N \cdot C_L \cdot V_{DD}} \tag{2.20}$$

Frequency Tuning Mechanism of CSRO

The frequency of a CSRO can be adjusted by modifying I_{ctrl}, controlled by an external voltage V_{ctrl}. The relationship between I_{ctrl} and V_{ctrl} (assuming MOSFET operation in saturation) is same as 2.6 with $I_{\text{ctrl}} = I_d$ and $V_{\text{ctrl}} = V_{\text{ds}}$.

Power Consumption of CSRO

The dynamic power consumption P_{CSRO} of a CSRO, is:

$$P_{\text{CSRO}} = \frac{N \cdot C \cdot V_{DD} \cdot I_{\text{ctrl}}}{2} \tag{2.21}$$

This equation highlights the dependence of power consumption on N, C, V_{DD}, and I_{ctrl}. Reducing N or V_{DD} can minimize power consumption, while tuning I_{ctrl} maintains frequency control.

Temperature and Process Variations of CSRO

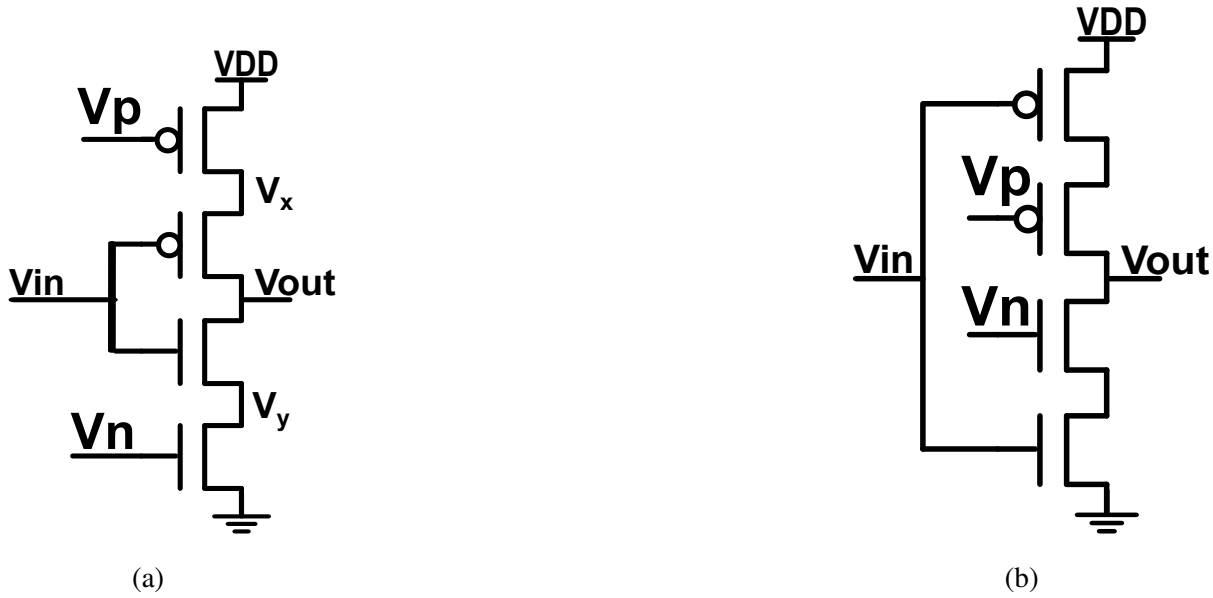
The Current Starved Ring Oscillator (CSRO)'s performance is sensitive to temperature and process variations, which affect parameters like V_{th} and μ_n. The temperature coefficient α_T, representing the change in frequency with temperature, is given by:

$$\alpha_T = \frac{1}{f_{\text{osc}}} \cdot \frac{\partial f_{\text{osc}}}{\partial T} \tag{2.22}$$

2.3.4 Previous work on CSRO

Various CSRO architectures have been explored in the literature [38–40], each employing distinct biasing circuit designs to optimize performance for specific applications. An output-switch-based CSRO architecture is described in [41], which leverages a switching mechanism at the output stage to enhance control over oscillation frequency. In a different approach, [42] introduces a CSRO configuration utilizing only NMOS current sources and forgoing the typical bias circuit.

This streamlined design aims to reduce circuit complexity and minimize power dissipation, making it an efficient alternative for power-sensitive applications. Furthermore, [43] presents a technique involving the addition of delay elements within the CSRO structure to effectively reduce oscillation frequency, allowing for finer control over timing characteristics. in [44], 4 different



(a) (b)

Figure 2.7: (a) Conventional CS inverter. (b) Output switch scheme inverter

strategies of biasing MOSFET placement has been explored for performance analysis. Each of these architectures showcases unique strategies to balance performance, power, and simplicity, underscoring the versatility of CSRO designs across various application contexts.

However, in [41] from conventional CS inverter (shown in Figure 2.7(a)) using control transistors connected to the output terminal (shown in Figure 2.7(b) & [41]) provides more control over transient current suppression and achieves higher frequency than the conventional design. As the switching scene, inverter provides more control over frequency and power consumption, the design will be leveraging this technique.

Chapter 3

Tunable clock design

This chapter details the design of a tunable on-chip oscillator. The design process leveraged Cadence Virtuoso for schematic capture and layout within the SOC system. Performance was rigorously evaluated using pre and post-layout simulations.

3.1 Overview of Design

The Current Starved Ring Oscillator (CSRO) is a vital component in this system, consisting of multiple inverter stages connected in a loop. Each inverter stage is ”starved” of current by additional transistors, which allows precise control over the oscillator’s frequency. By adjusting the current fed into each stage, the oscillator can be fine-tuned to meet specific frequency requirements. These additional transistors are designed to respond to signals from an external controller, which sets the current flowing into each inverter stage. As previously discussed, controlling the current through each stage allows for meticulous frequency adjustments, enabling the system to dynamically tune the oscillator’s frequency in response to feedback.

In the picture below Figure 3.1, the SoC is integrated with a Central Access Controller (CAC), which provides real-time input to either increase or decrease the oscillator’s frequency. This control mechanism is implemented by setting predetermined registers, known as coreMMR, within the Cortex M0+ SoC, as shown in Figure 3.1. These registers interface directly with the Current

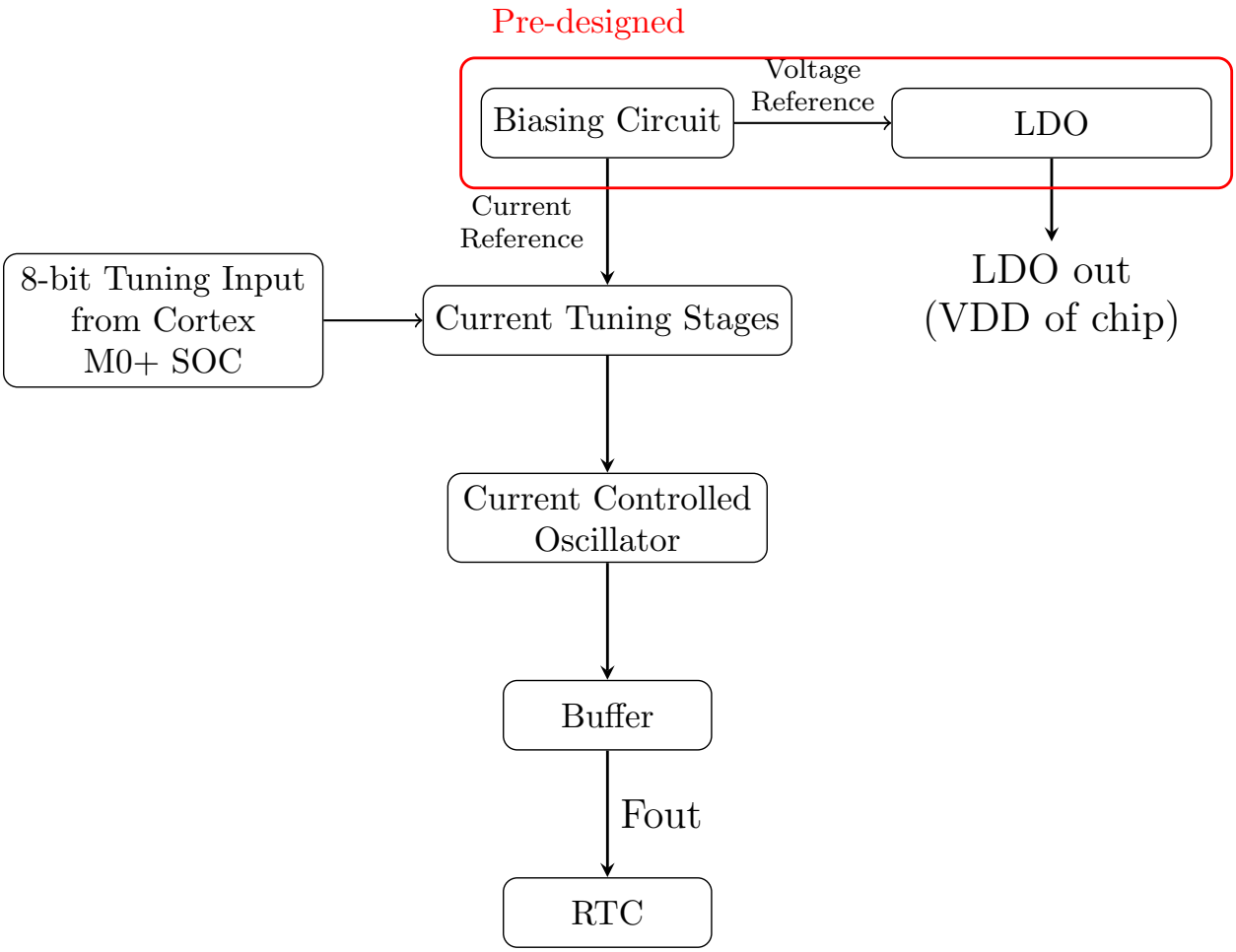


Figure 3.1: Flowchart of the design

Tuning Stage, feeding it with the necessary input to adjust the oscillator frequency. This feedback-based tuning architecture enables the SoC to achieve optimized frequency control, enhancing the system's adaptability and efficiency.

The Current Tuning Stage is a sophisticated arrangement of switches and current mirrors. This block's core function is to regulate the current driving the oscillator, and it is key to achieving precise control over the frequency output. An 8-bit tuning input from the M0+ provides a digital signal that adjusts the current. This input corresponds to a micro controller unit (MCU) or similar processor, offering 256 distinct tuning states (2^8), thus allowing fine-grained frequency control. This digital-to-analog interface forms a crucial aspect of the system, enabling the SoC to modulate

the current with high precision based on real-time conditions. The Current Tuning Stage mirrors a reference current generated by the Biasing Circuit. The biasing circuit provides a foundational current that ensures consistent operation across the system, serving as a reliable current source. In this design, a Constant-gm current reference circuit is employed within a Low Dropout Regulator (LDO), which regulates the system's 1.8V supply voltage down to a stable 1.1V operating voltage. This setup is essential for maintaining stable performance and ensuring that current variations do not disrupt the oscillator's tuning.

To maintain the integrity of the oscillator's output, Buffer is incorporated. Buffers ensure that signals are transmitted cleanly between different stages in the integrated circuit, preventing signal degradation due to loading effects. Here, the buffer strengthens and stabilizes the oscillator's output before sending it to the next block, designated as (F_{out}). This process ensures that the clock signal remains robust and interference-free when it reaches the Real Time Counter (RTC). Finally, the RTC forms a critical part of the SoC, where it serves as the real-time clock for timestamping sensor data. With a stable, tunable clock input provided by the CSRO, the RTC can deliver accurate timing information essential for time-sensitive applications. By enabling the SoC to adjust the oscillator frequency as needed, this design supports efficient, adaptable timing control, enhancing the overall performance and reliability of the system.

3.2 Design requirement for oscillator

The design specifications define a high-precision, low-power oscillator tailored for applications requiring stable, adjustable clock signals. The system is required to achieve a target frequency of 100 kHz with a stable operating voltage of 1.1V. An 8-bit tuning resolution allows 256 precise adjustment steps, ensuring fine-grained frequency control between CAC and SoC within 100us accuracy. Designed for ultra-low power consumption, the system aims to stay below 100 nanowatts which makes the energy per cycle requirement to be less than 1pj/cycle, highlighting the system's efficiency. For precise tuning of the oscillator, the mechanism requires frequency adjustments with small steps, offering highly precise control. These specifications collectively underscore the system's focus on precision, efficiency, and adaptability for applications requiring a tunable, low-power clock source.

3.3 Schematic design of Tunable CSRO

The design has been constructed using **TSMC 65nm PDK (process design kit)**. The diagram is shown in Figure 3.2. The V_{ref} is connected to a 20nA branch of the biasing circuit used in the LDO, which generates the V_{DD}. Using the current steering method of a current mirror, the I_{tune} and I_{N} currents are generated.

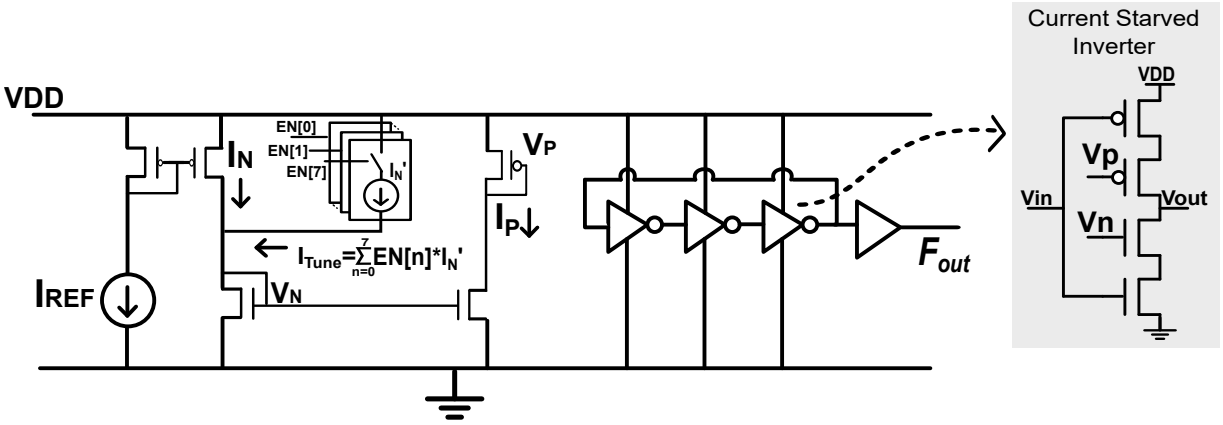


Figure 3.2: Schematic design of Current starved ring oscillator

In this architecture, the current I_N acts as the base current to generate the minimum frequency while driving the current-starved ring oscillator. A key aspect of the design is the regulated current I_{Tune}, which is governed by the value of the tuning bits $E_n[7:0]$. The tuning stage switching transistors are sized in exponentially with respect to corresponding E_n pin connection. The expression can be written as:

$$W_N = 2^N * W_0 \tag{3.1}$$

The switches associated with these tuning bits are strategically distributed across eight branches. Each branch is connected in series with transistors responsible for mirroring the bias current I_{ref} which is also sized following 3.1.

The bias current I_{ref} serves as a reference that is mirrored across these eight branches, enabling consistent regulation of the currents in each. As the tuning values encoded in $E_n[7:0]$ are altered, they dynamically regulate the currents through each branch. This adjustment directly influences the total current exerted through each branch, which is then added to the base current I_N. The resulting sum of currents leads to a modulation in V_N, a key control voltage within the system.

The voltage V_N, after being modulated by the combined currents, is ideally mirrored to V_P. This mirroring ensures that any changes in V_N are precisely reflected in V_P. Both V_P and V_N play a crucial role in controlling the current flowing through the inverter branches of the ring oscillator. By adjusting the currents, these voltages effectively determine the oscillation behavior of the ring oscillator.

The control of V_P and V_N directly affects the frequency F_{out} produced by the ring oscillator. Since the oscillator is current-starved, the amount of current allowed through the inverters dictates how fast the oscillator can switch, thus controlling the output frequency. When the currents are higher, the oscillator can switch more quickly, leading to a higher frequency F_{out}. Conversely, reducing the currents slows down the oscillator, lowering the frequency. The buffered F_{out} is then brought out for further use in external circuits or systems.

3.4 Schematic simulation result

The schematic has been tested under various conditions across voltage, temperature, and corner cases. Additionally, the Monte Carlo simulation results have been analyzed. Figure 3.3 shows the pre-layout frequency vs. tuning value simulation results for the tunable CSRO, aiming to achieve a frequency of 100 kHz within the oscillator's tuning range. The schematic design was tested under a temperature variation from 0 to 80°C with VDD voltages of 1.1V and 1.2V. The simulation results

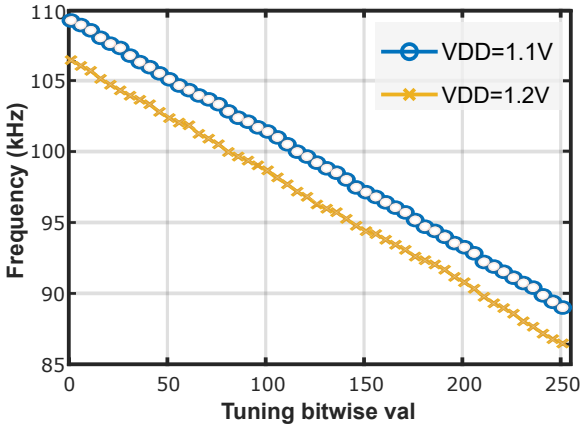


Figure 3.3: Frequency vs Tuning value change at LDO output 1.1V and putting VDD at 1.2V

for frequency vs. tuning value indicate that, across each case of temperature and voltage change, the design can achieve a frequency of 100 kHz within the 8-bit tuning range (EN[7:0]).

Leakage current effects can be observed in Figure 3.4, where the oscillator frequency increases or decreases proportionally with temperature. The increased leakage current at higher temperatures raises the static current consumption, affecting the base current that sets the minimum frequency when EN[7:0] = 255. Additionally, the dynamic power consumption also increases with temperature. Figure 3.5 is attributed to the current rise in the tuning stage and current mirror branches. Figure 3.5 presents the power consumption changes concerning tuning value variations, with curves representing the results across temperature and frequency changes. The results show that power consumption increases with rising temperatures. As noted in 2.22, the ring oscillator is susceptible to temperature variations. With increasing temperature, the V_{th} of transistors decreases, resulting

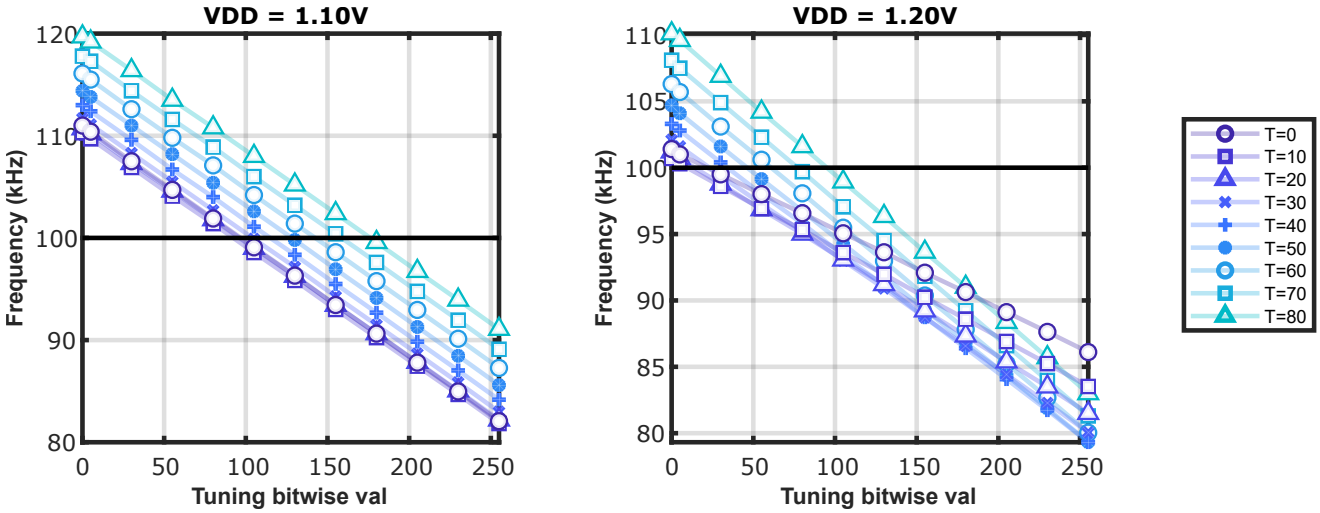


Figure 3.4: Frequency vs tuning value result across temperature change for VDD=1.1 & 1.2

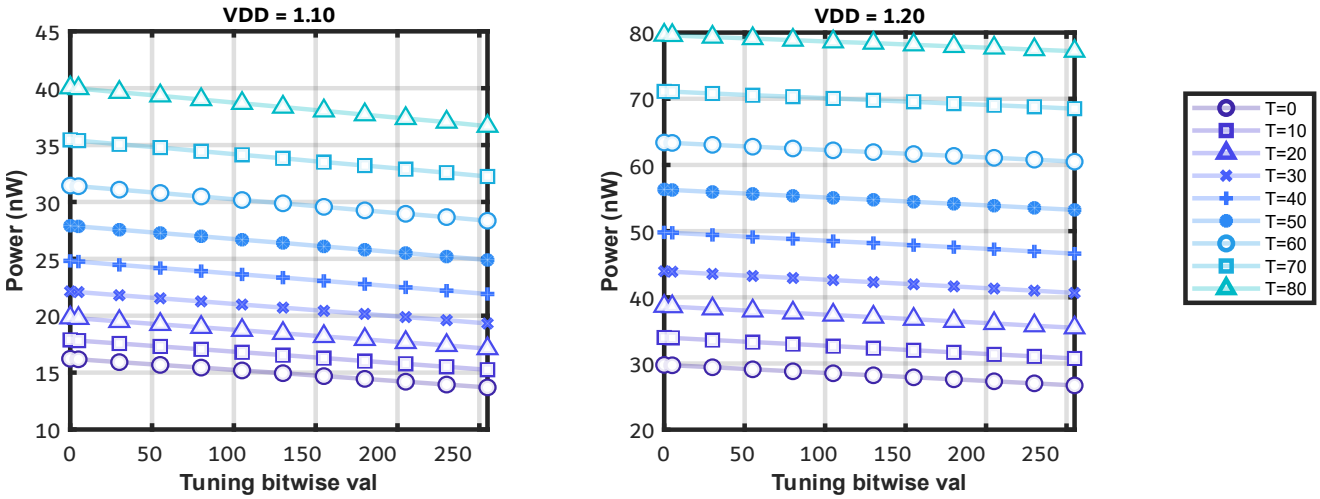


Figure 3.5: Power consumption vs tuning value result across temperature change for VDD=1.1 & 1.2

in higher leakage power consumption.

Energy per cycle is a critical metric for oscillators, quantifying performance across different frequencies and enabling comparisons with other oscillator designs. Ideally, the energy per cycle of an oscillator should be less than 1 pJ/cycle. In Figure 3.6, the maximum energy per cycle at 1.1V is 0.45 pJ/cycle, while at 20°C, it is only 0.17 pJ/cycle. Using a V_{DD} of 1.2V, the maximum increases to 0.9 pJ/cycle, which remains below 1 pJ/cycle despite being obtained at high temperatures. At

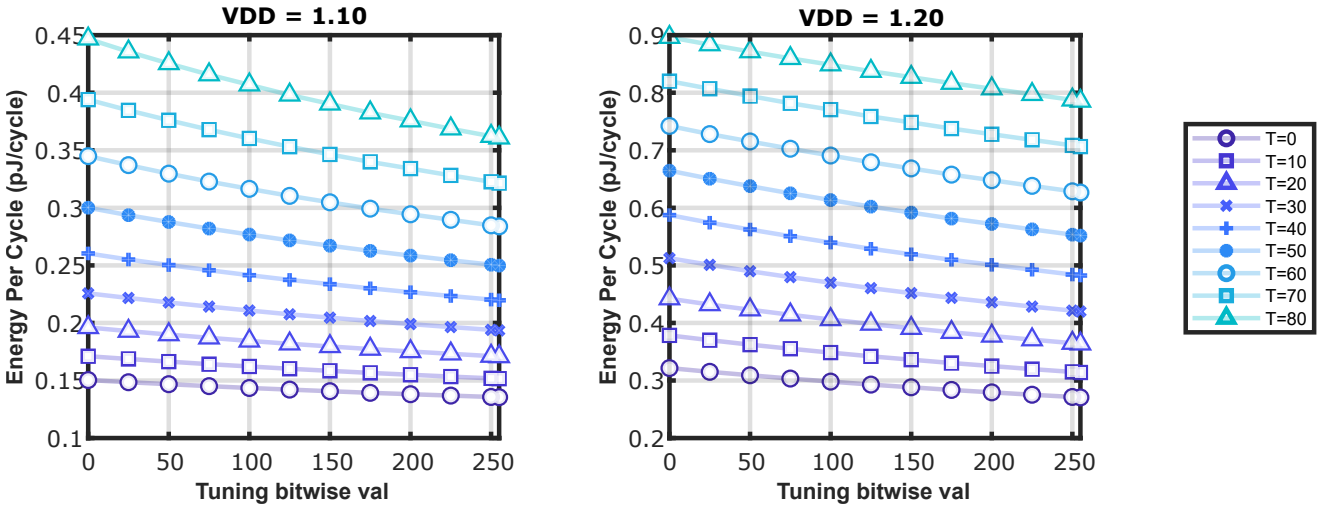


Figure 3.6: Energy Per Cycle vs tuning value result across temperature change for VDD=1.1 & 1.2

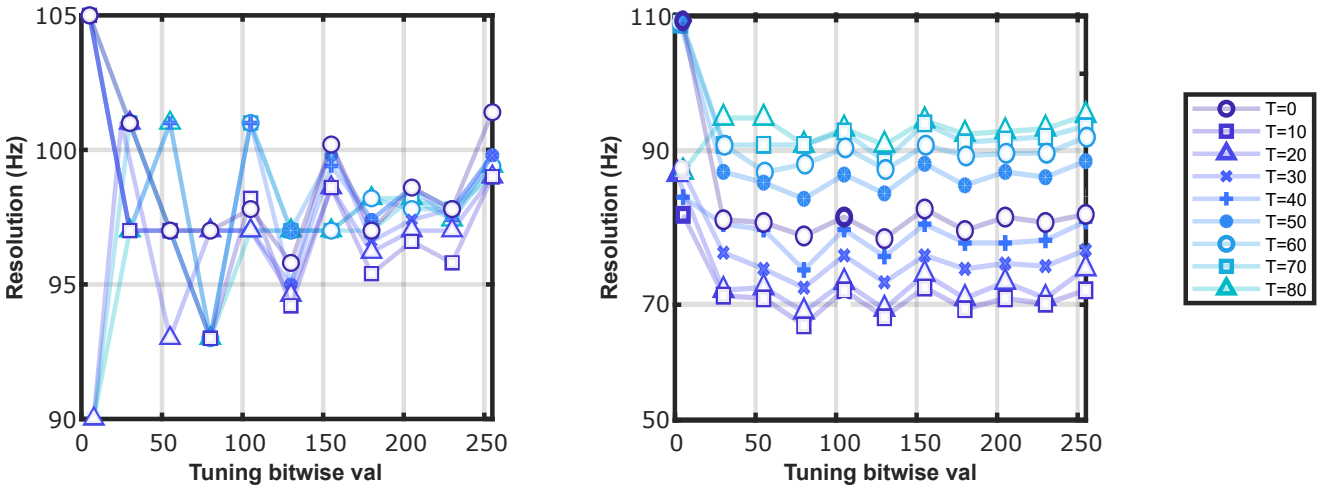


Figure 3.7: Tuning step Resolution vs tuning value result across temperature change for VDD=1.1 & 1.2

20°C, the design reaches 0.45 pJ/cycle. This energy increase is due to higher power consumption in the current mirror and tuning stages, which are sensitive to leakage current increases under temperature and voltage variations.

The primary objective is to achieve a high-frequency tuning resolution in the oscillator with changes in the tuning value. At a system voltage of $V_{\mathrm{DD}} = 1.1\mathrm{V}$, the design achieves a nearly constant tuning resolution ranging from 95 to 100 Hz in schematic simulations, which is also ob-

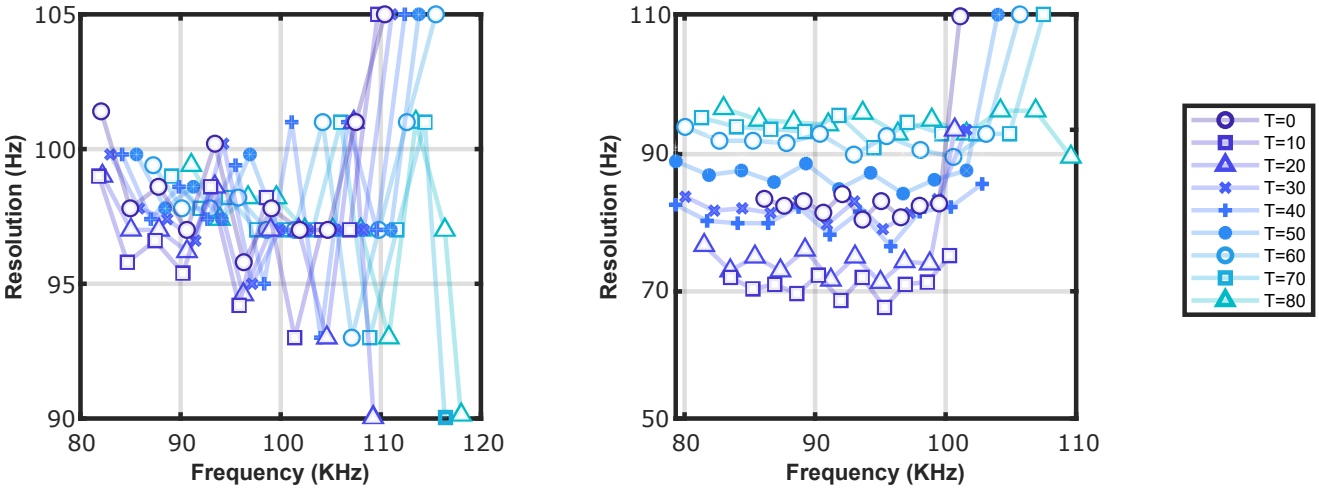


Figure 3.8: Tuning step Resolution vs Oscillation Frequency across temperature change for VDD=1.1 & 1.2

served at $V_{\text{DD}} = 1.2\text{V}$ (Figure 3.7 & 3.8. However, at lower temperatures, the frequency range and resolution decrease due to the high threshold of transistors. The elevated threshold voltage delays MOSFET turn-on, resulting in a lower frequency output from the ring oscillator. Therefore, although the base current for minimum frequency generation remains unchanged at lower temperatures, the oscillator's frequency output is lower than at nominal temperatures.

In Figure 3.4 for $V_{\text{DD}} = 1.2V$ (external supply) we can observe that with temperature increase the frequency changing slope is higher than lower frequency which can be explained using Figure 3.7 where we can see that if $V_{\text{DD}} = 1.2V$, the tuning resolution (change in frequency per tuning value) increases with temperature. this effect is not present if $V_{\text{DD}} = 1.1V$ and at high temperatures also the tuning resolution remains the same.

3.5 Post layout simulation results

For implementing the oscillator with the SoC in silicon, the Cadence Layout XL suite was used. The CSRO occupies an area of 53.69 x 41.65 μm^2, totaling 2236.12 μm^2. Following successful mitigation of DRC and LVS errors, Post-layout parasitic extraction (PEX) was conducted, and PEX simulation results were subsequently obtained.

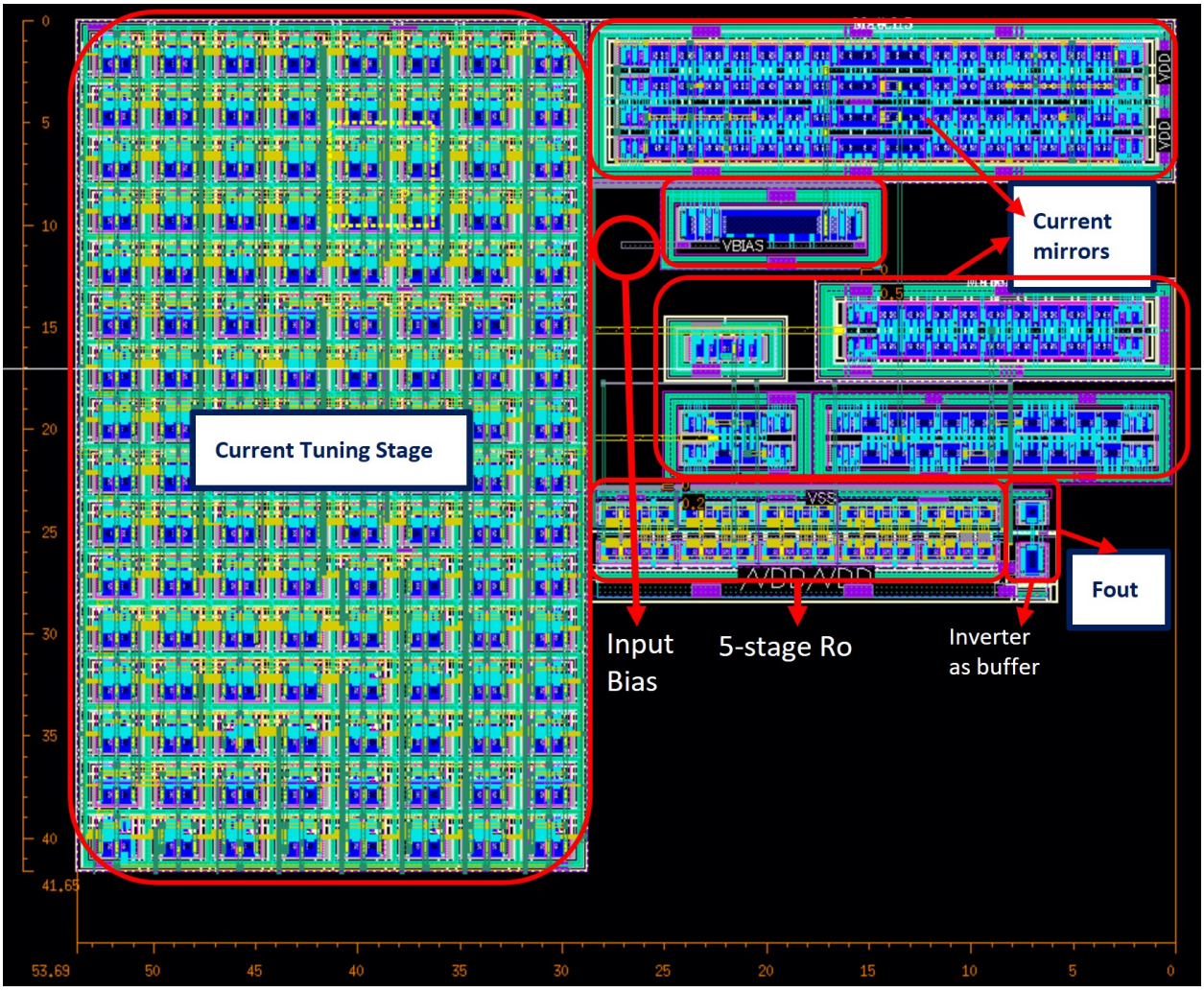


Figure 3.9: Layout design of the Proposed Current Starved Ring Oscillator (CSRO)

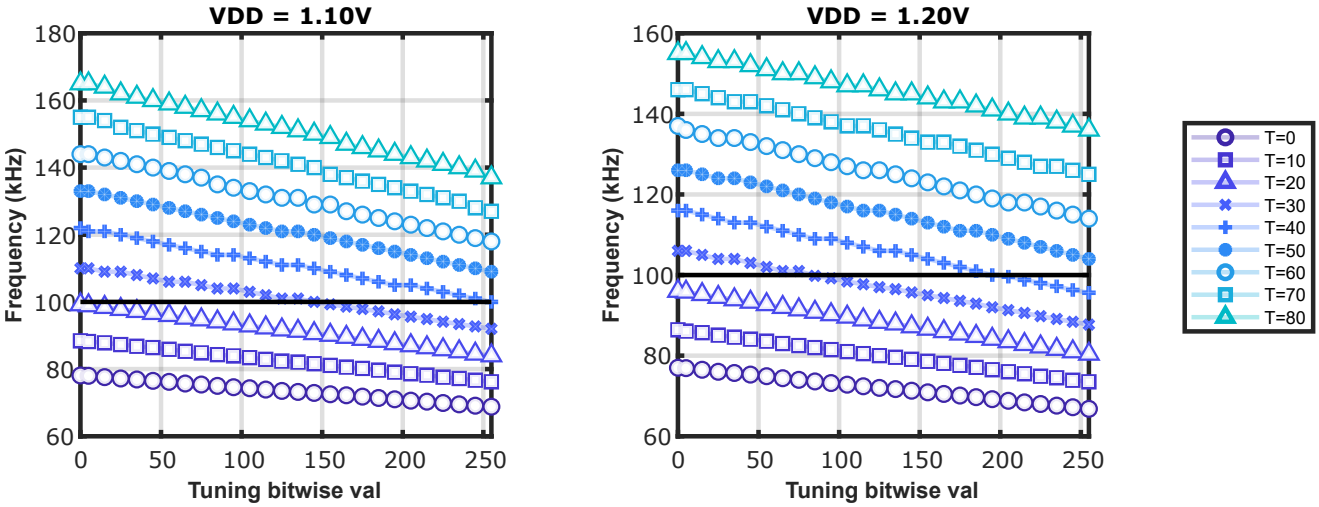


Figure 3.10: PEX simulation result of Frequency vs tuning value result across temperature change for VDD=1.1 & 1.2

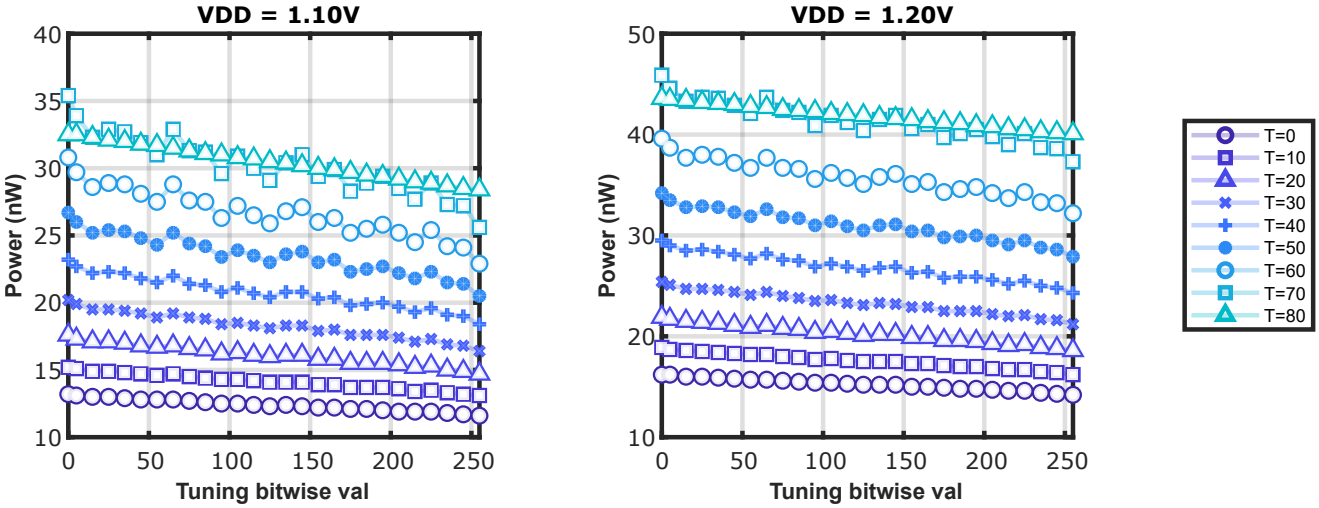


Figure 3.11: PEX simulation result of Power consumption vs tuning value result across temperature change for VDD=1.1 & 1.2

Figure 3.10 shows the PEX simulation results, illustrating frequency changes of the oscillator as tuning values vary. At $T = 20$, 30, and 40°C, the system achieves the target frequency of 100 kHz. However, in comparison with simulation results shown in Figure 3.4 at higher temperatures, parasitic effects degrade performance, causing significant variations in the oscillator's minimum

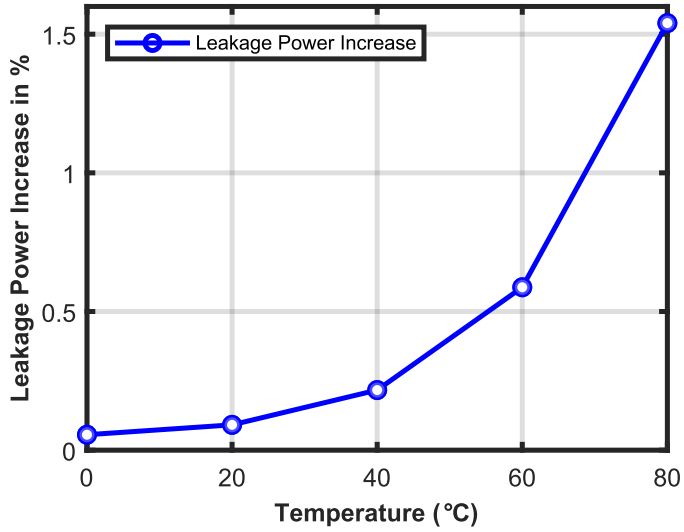


Figure 3.12: Percentage of leakage power increase w.r.t actual power across temperature for an inverter

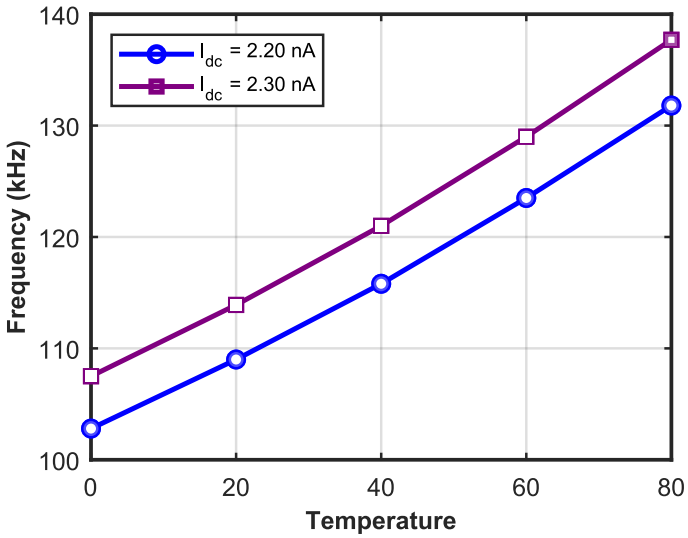


Figure 3.13: Small change in bias current effect in Ring oscillator output frequency

and maximum frequencies. This degradation is primarily due to increased leakage current w.r.t temperature increase and mismatches in the transistors layout matching within the current mirrors, which lead to deviations from the intended design target. As the temperature increases in layout the

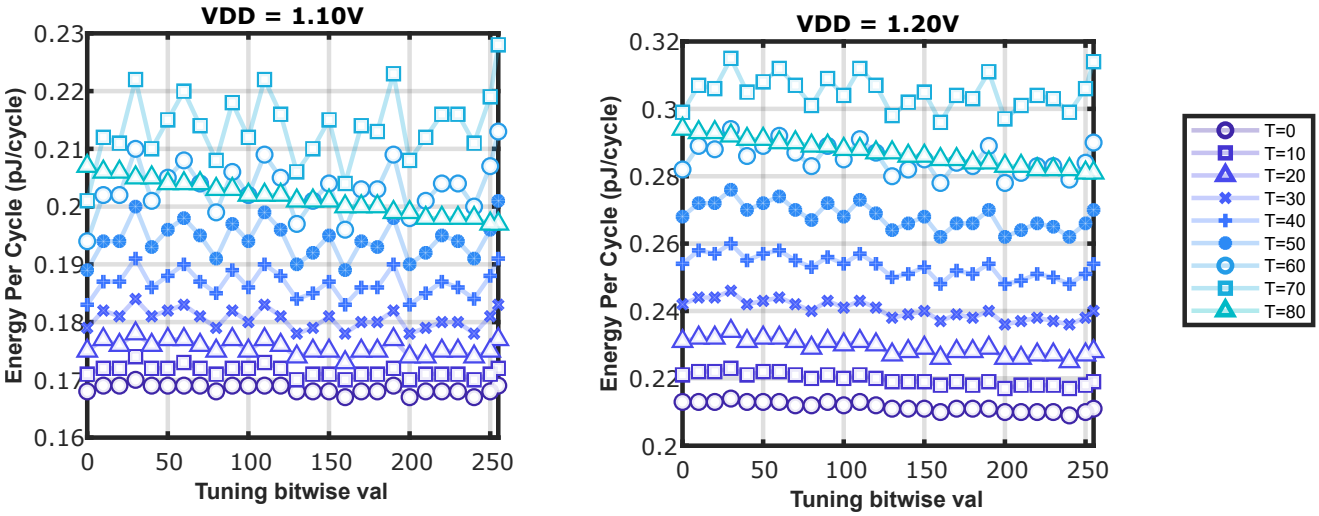


Figure 3.14: PEX simulation result of Energy Per Cycle vs tuning value result across temperature change for VDD=1.1 & 1.2

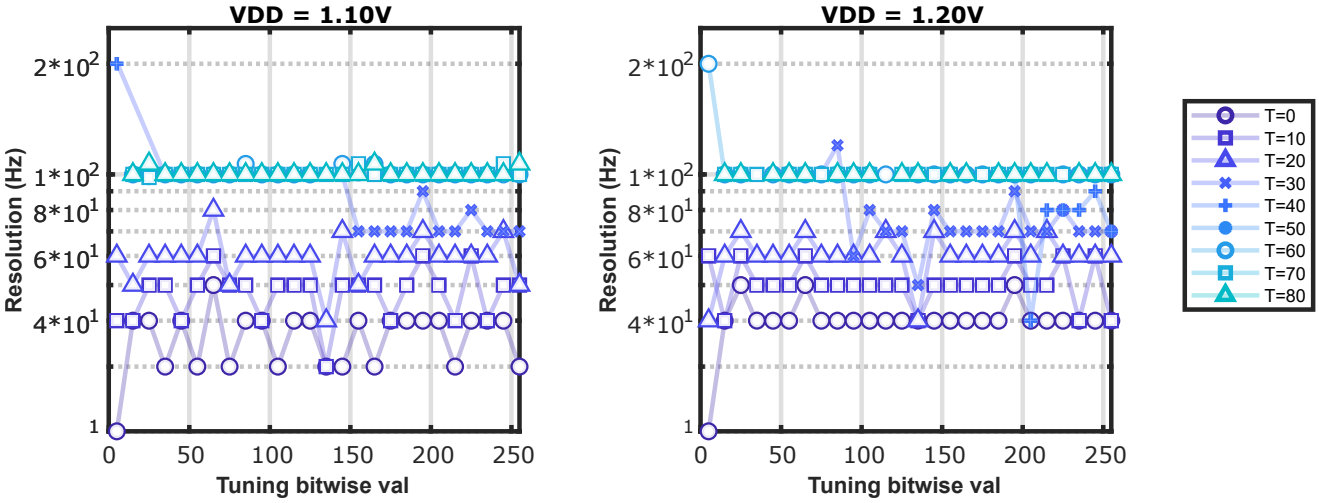


Figure 3.15: PEX simulation result of Tuning step Resolution vs tuning value result across temperature change for VDD=1.1 & 1.2

performance of the current mirrors degrades in matching the brunch currents in different current regulation stages which is increasing eventually thus increasing the brunch current in the oscillators that are set in schematic simulations leading to a gradual increase in the oscillation frequency of the CSRO.

The figure also shows that, at 1.2 V, the oscillator's frequency decreases compared to its perfor-

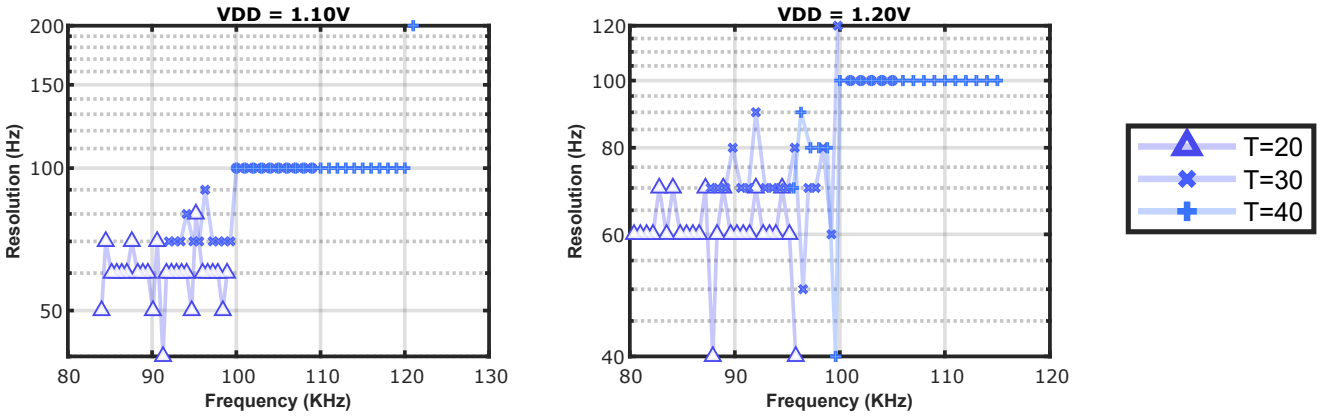


Figure 3.16: PEX simulation result of Tuning step Resolution vs Oscillation Frequency across temperature change for VDD=1.1 & 1.2

mance at 1.1 V across all temperatures. Thus, in addition to adjusting tuning bit values, controlling V_{DD} provides another means to reduce the oscillator frequency for high-temperature applications, aiding in frequency stabilization.

The power consumption (Figure 3.11) and energy per cycle (Figure 3.14) performance in the PEX simulation closely match the schematic simulation, and even improve upon, the initial design specifications. Notably, the maximum power consumption at $T = 80°C$ is 45 nW at $V_{DD} = 1.2V$ compared to 80nW in figure 3.5, significantly lower than in the initial simulation results. This reduced power consumption demonstrates the energy efficiency of the design under high-temperature conditions regardless of frequency mismatch from schematic to layout results.

The frequency and power consumption increase mismatch between simulation and PEX results can be explained with figure 3.12 & 3.13. Figure 3.12 illustrates the increase in leakage power compared to actual dynamic switching power for a single inverter. This power rises to 1.6% at high temperatures for a single inverter's pull-up/pull-down transistor. This effect accumulates across all MOSFETs in the RO and tuning stage, collectively increasing leakage power up to 10 nW at high temperatures. This leakage current pushes the frequency of the design to exceed the target frequency.

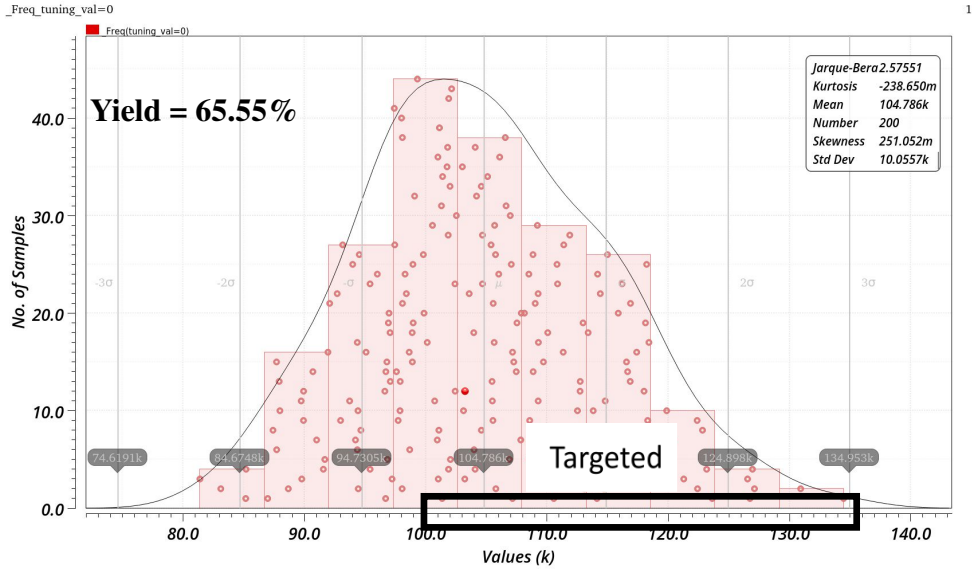
The output frequency of the Current Starved Ring Oscillator (CSRO) is regulated by controlling the branch currents of the inverter stages. However, achieving frequency stability also requires

maintaining current stability in biasing the oscillator. Figure 3.13 shows that a small 0.1 nA change in the biasing current of the post-layout PEX simulated inverter results in a significant frequency increase.

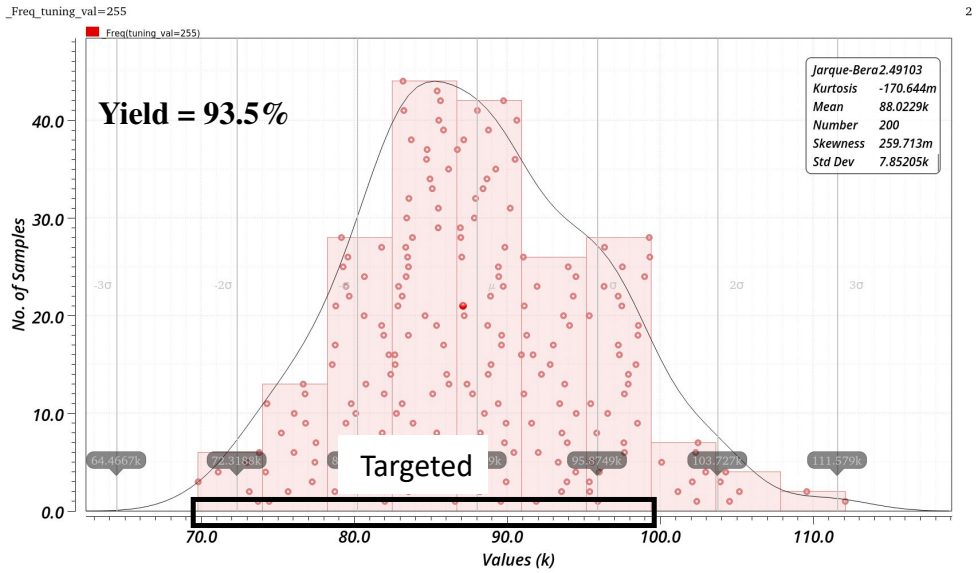
The tuning resolution performance (Figure 3.15-3.16) of the design aligns closely with the simulation results. At higher temperatures, the resolution reaches 100 Hz. However, at nominal and lower temperatures, for both 1.1V and 1.2V V_{DD}, the resolution peaks at 80 Hz with an average resolution of 60 Hz. Compared to the results from simulation in 3.7-3.8 which is higher. This consistency across operating conditions demonstrates stable tuning performance across various temperature and voltage levels.

The design requirements specify a tuning resolution sufficient for a 40 ms synchronization time. In the resolution vs. frequency plot, data from the 20–40°C range demonstrates that the simulation maintains a frequency range within 100 kHz. With a maximum tuning resolution of 100 Hz, the minimum achievable synchronization interval is 10 ms.

3.6 Monte Carlo Simulation Result



(a)



(b)

Figure 3.17: Monte Carlo simulation results with $V_{\mathrm{DD}} = 1.1V$, nominal temperature and global corner for (a) Maximum frequency for tuning value 0, (b) Minimum frequency for tuning value 255

.

Monte Carlo simulation is a statistical technique used to model the probability of different outcomes in processes with inherent uncertainty. Running numerous random trials, it provides insights into system behavior under various scenarios, helping predict and analyze performance variations across design parameters like voltage V_{th}, temperature, etc. This approach helps assess reliability and stability by simulating real-world variations that may affect performance. The figure illustrates the frequency variability across chips at the extremes of the tuning range (Tuning value = 0 for maximum frequency and Tuning value = 255 for minimum frequency), as simulated using the Monte Carlo simulation method. Within the 3σ confidence interval, we observe a spread in the minimum achievable frequency from 70 kHz to 111 kHz with a yield of 93.5% (yield= % of points $<$100KHz) and in the maximum achievable frequency from 83 kHz to 134 kHz with and yield of 63.5% (yield= % of points $>$100KHz). This range indicates potential inter-chip variations where some chips may only reach frequencies as low as 70 kHz at the minimum tuning level and top out at 83 kHz at the maximum tuning level, missing the target frequency of 100 kHz entirely. Conversely, another subset of chips might start at 111 kHz and reach up to 134 kHz, again bypassing the 100 kHz mark.

Chapter 4

Real chip experimented results

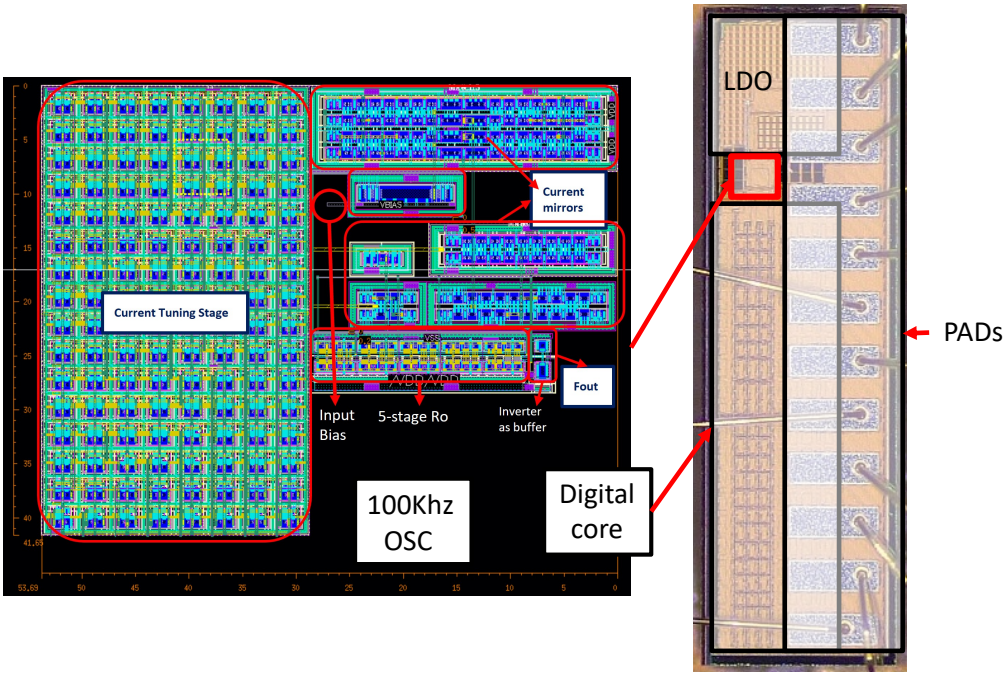


Figure 4.1: Die picture with 100Khz oscillator.

The design GDS has been fabricated at **TSMC 65nm** technology with **cortex M0+** SoC chip and this section will analyze the chip results. The Figure4.2 shows the testing setup. The SoC chip size is 0.6mm*2.15mm (containing oscillator silicon area 53.69 μm * 41.65μm).

The chip is tested using Pattern Generator Logic Analyzer (PGLA) and the output frequency is

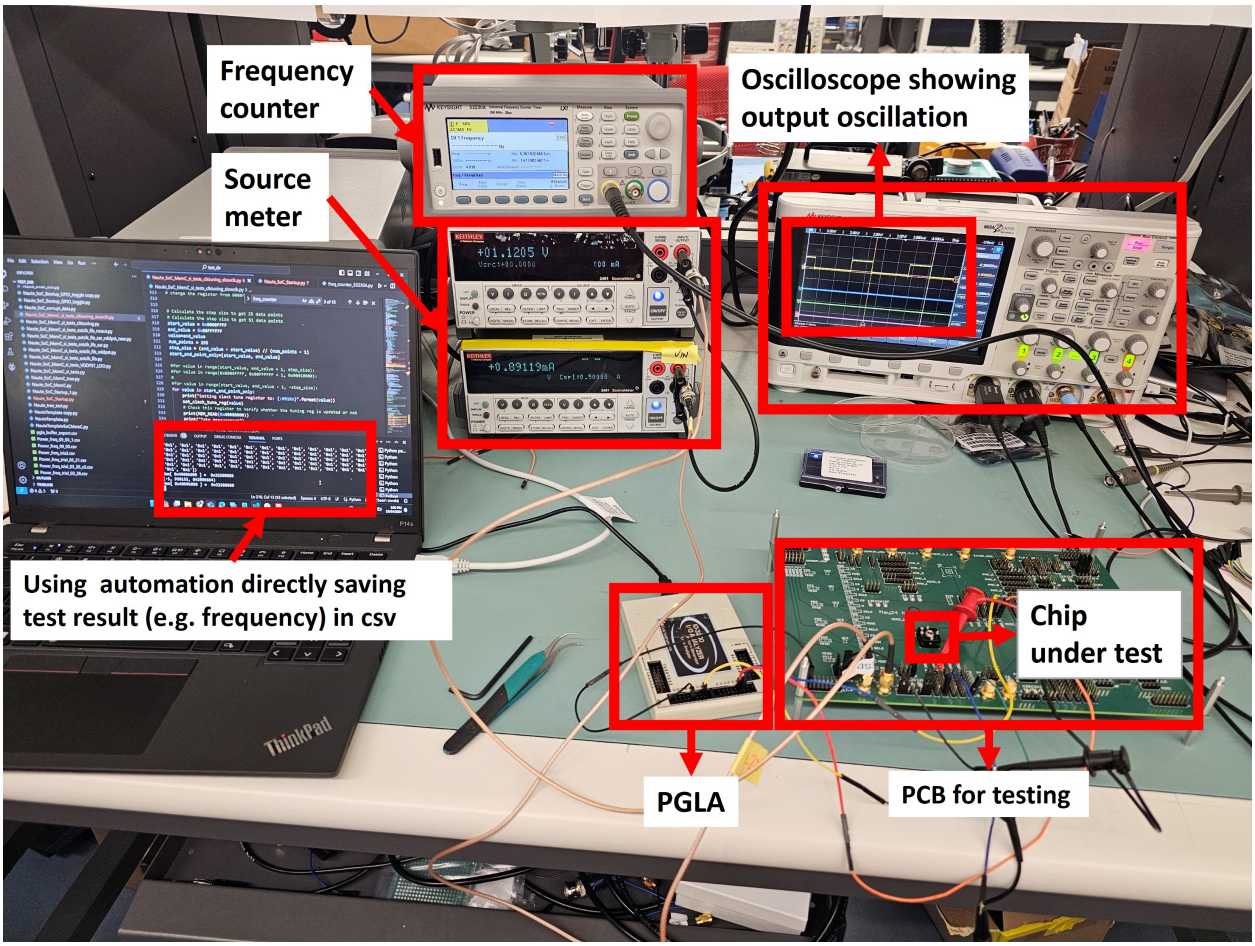
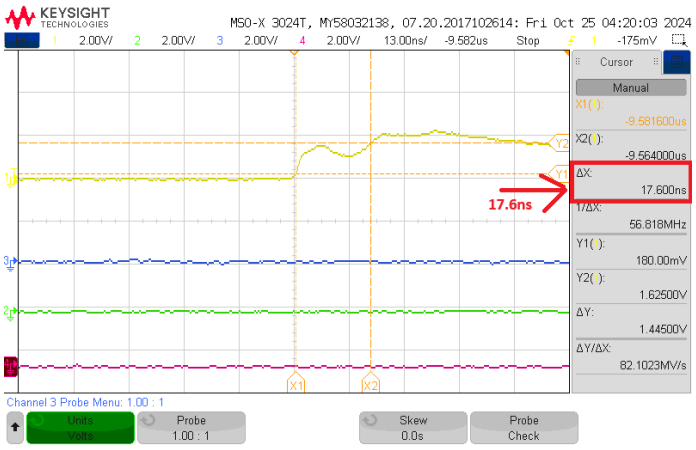


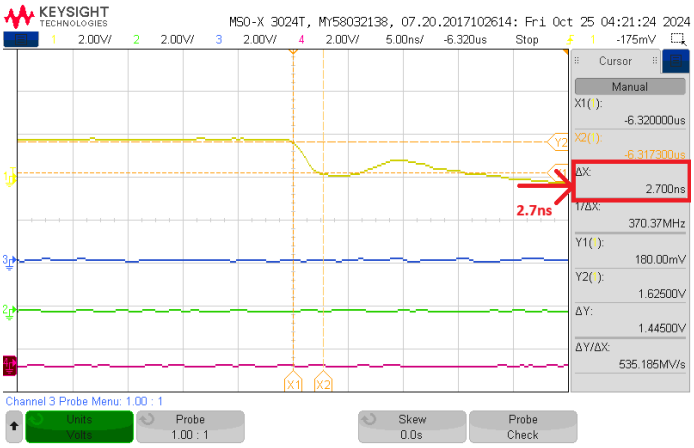
Figure 4.2: Testing Setup of the chip

measured by the Frequency counter. The 2 source meters are used for supplying 1.8 V, measuring the on-chip LDO output, and also supply 1.2 V bypassing LDO when testing under $V_{DD} = 1.2V$ supply. An automation code is setup in Python which can control the source meters and frequency counter to change and measure voltages, currents, and counted frequency and store all of them in a CSV altogether.

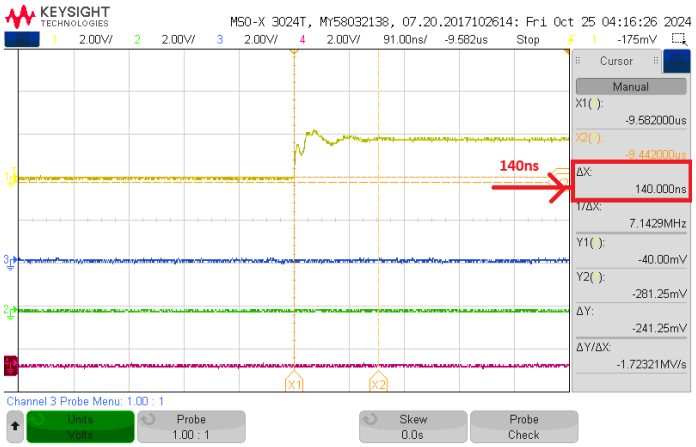
The oscillator demonstrates (Figure 4.3(c)) a settling time of 140 ns, with a rise time (Figure 4.3(a))of 17.6 ns and a fall time(Figure 4.3(b)) of 2.7 ns. For a 100 kHz oscillator, these values correspond to 1.4% for settling time, 0.176% for rise time, and 0.027% for fall time relative to the oscillation period.



(a) Rise time



(b) Fall time



(c) Settling time

Figure 4.3: a) Rise time, b) Fall time, c) Settling time of the oscillator

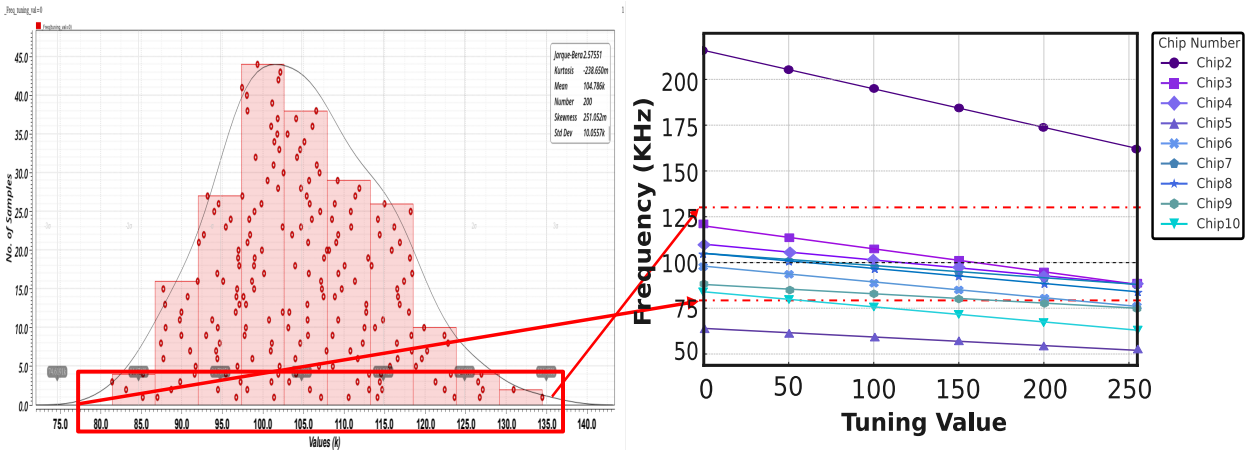


Figure 4.4: Silicon result of Oscillator for Frequency vs Tuning Value across chip and comparison with Montecarlo result

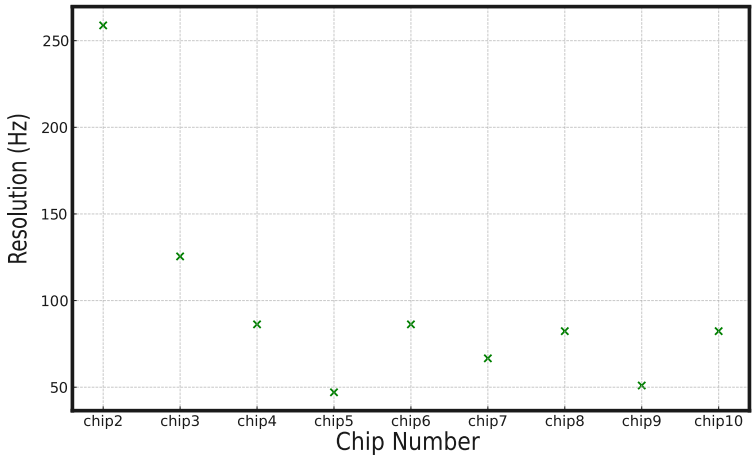


Figure 4.5: Silicon result of Oscillator for Resolution(Hz) for the chips

Figure 4.4 illustrates chip-to-chip performance variation due to process differences along with comparison with 3.6. Chips 3, 4, 6, 7, and 8 successfully reach the 100 kHz target frequency, with data collected at an LDO output voltage of 1.1 V serving as V_{DD}. Due to inherent voltage error, the LDO output spans from 1.12 V to 1.18 V across chips, impacting the oscillator's frequency output. A refined V_{DD} could address this issue, improving yield by reducing frequency variability.

A comparison with the Monte Carlo simulation results shown in Figure 3.17 is essential to assess chip-to-chip variation. As outlined in Section 3.6, the performance within a 3σ range indicates that the chip's maximum and minimum frequencies can span from 83–134 kHz and 70–111 kHz, respectively, at nominal temperature. Among the tested chips, all but chip 2 and chip 5 fall within this range, supporting the Monte Carlo simulation results. Future work should aim to broaden this range, ensuring that the maximum frequency exceeds 100 kHz and the minimum frequency falls below 100 kHz within a 3σ range. This enhancement would help ensure that the majority of chips achieve a center frequency of 100 kHz within their tuning range.

The plot 4.5 shows the tuning resolution (in Hz) for each chip, represented by chip numbers on the x-axis and resolution values on the y-axis. Each point represents the average tuning resolution for a specific chip, illustrating variation in resolution across different chips.

From the graph 4.5, we can see that Chip 2 has the highest resolution at approximately 250 Hz, while the other chips exhibit lower resolutions, mostly clustering between 50 and 100 Hz. This variation suggests that some chips achieve finer tuning steps than others, which may result from process variation and minor differences in component behavior from chip to chip. However, this shows a stable performance range across the set, indicating reliable tuning resolution despite variations in individual chips.

As shown in Figure 4.4, chip-8 exhibits the closest match to the simulation results, and therefore, further analysis and testing were conducted using chip-8. Figure 4.6 presents frequency sweeping in response to changes in tuning values. The design successfully achieves the target frequency of 100 kHz within its tuning range, with a maximum frequency of 108 kHz and a minimum frequency of 87 kHz. When compared with the results in Figure 3.10 at $T = 30°C$, which represents the nominal temperature, both cases show that the frequency reaches 100 kHz within their respective tuning ranges. Both plots also exhibit similar results for the maximum and minimum frequency ranges achieved. The PEX simulation indicates a f_{max} of 110 kHz at $T = 30°C$, and silicon data supports this result when V_{DD} is at 1.1V.

Although in figure 4.6 the plots look liner, from figure 4.7 & 4.9 we can see the actual variation between each points. The chip demonstrates a high tuning resolution, with an average step size of

84 Hz and a maximum of 89 Hz across different tuning values, as shown in figures 4.7 and 4.8. When compared with the PEX simulation results in Figures 3.15 and 3.16 at $T = 30°C$, the tuning resolution is consistent. For both $V_{DD} = 1.1V$ and $V_{DD} = 1.2V$, the resolution is close to 80 Hz. Given the importance of tuning precision for accurate timing in the SoC, these results demonstrate the high tunability of the design, ensuring consistent and reliable performance within the specified operational range.

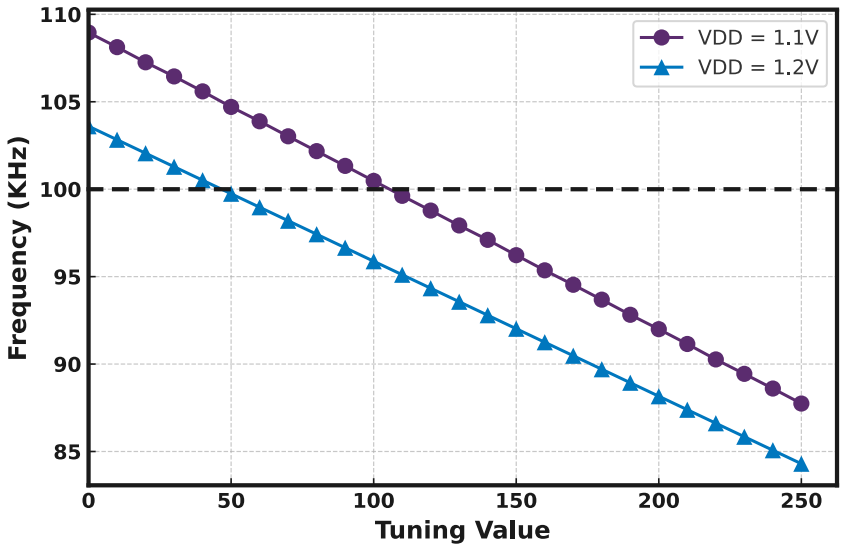


Figure 4.6: Silicon result of Oscillator for Frequency vs Tuning Value

Figure 4.9 displays the chip's performance across varying temperatures. The silicon test results confirm that the chip maintains the target frequency of 100 kHz within its tuning range from 20°C to 50°C. At 60°C, the oscillator remains close to 100 kHz, while at 70°C, an increase in V_{DD} from 1.1 V to 1.22 V allows it to achieve 100 kHz. However, at 80°C, even raising V_{DD} to 1.3 V does not achieve the target frequency, suggesting that further increases in V_{DD} may be needed to stabilize frequency performance at this higher temperature.

The design specifications require a tuning resolution sufficient to support small synchronization intervals. In the Resolution (Hz) vs. Chip Number plot, the data in figure 4.5 shows that only for 1 chip a maximum resolution of 250 Hz. Most chips exhibit even finer tuning resolutions, with some chips reaching as low as 50 Hz while most of the chips provide an average resolution of 80 Hz.

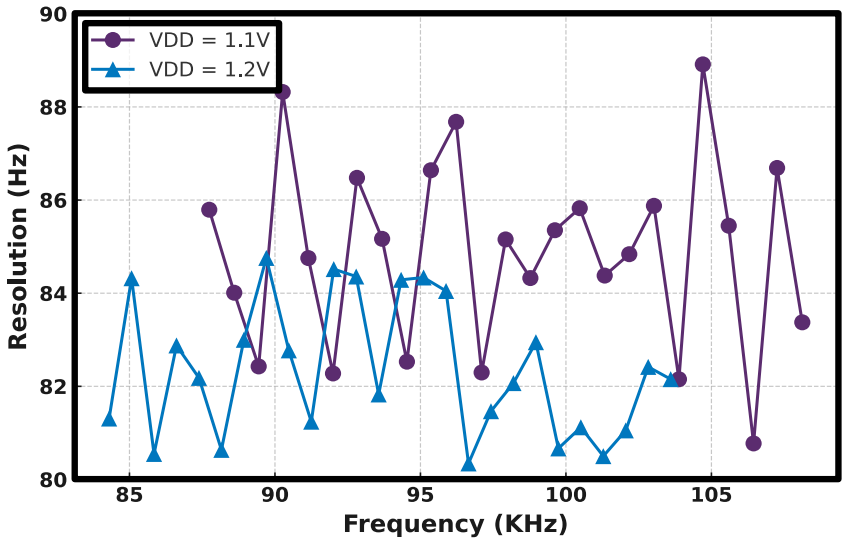


Figure 4.7: Silicon result of Oscillator for Resolution(Hz) vs Tuning Value

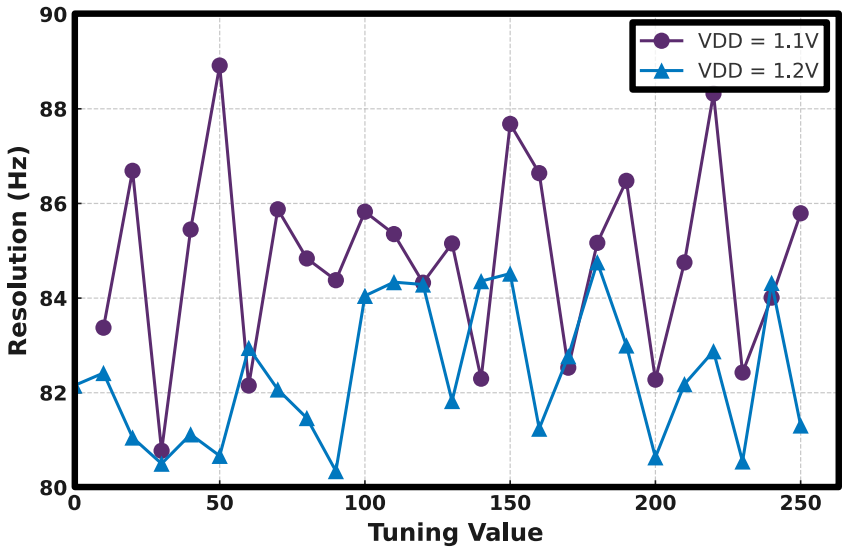


Figure 4.8: Silicon result of Oscillator for Resolution(Hz) vs Frequency

Given that a tuning resolution of 1 kHz corresponds to a 1 ms synchronization capability, the observed average resolution of 80 Hz implies that the system can support a synchronization interval as low as 12.5 ms. A 0.1% tuning resolution means that the timer errors will be kept below 100 μs as long as synchronization occurs every 100 ms. This design provides a tuning resolution of

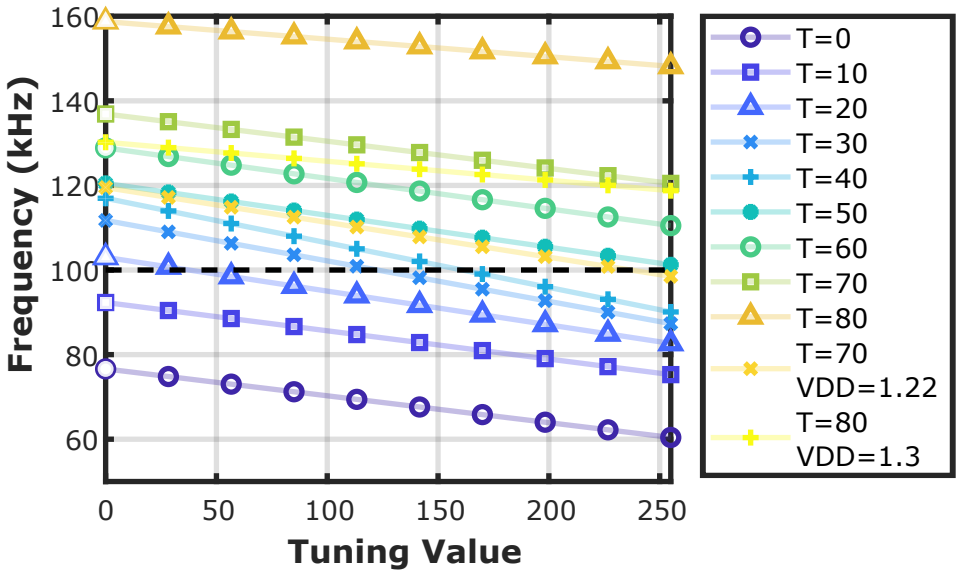


Figure 4.9: Silicon result of Oscillator for Frequency vs Tuning Value across temperature variation

0.08%, which is much lower than the desired threshold. Therefore, this analysis quantitatively confirms that the design not only meets but significantly exceeds the synchronization performance criteria, providing a substantial margin of robustness in real-world applications.

4.1 Design Summary

The complete summary of the design for schematic simulation, Layout Pex simulation, and fabricated chip (Chip-8 in Figure 4.4,4.5) silicon result at nominal temperature is tabulated in 4.1.

Design	**VDD**	**Frequency Max (kHz)**	**Frequency min (KHz)**	**Tuning range (KHz)**	**Average Tuning step size (Hz)**	**Tuning step resolution in %**	**Power consumption (nW)**	**Energy per cycle (fj/cycle)**
Spec	1.1-1.2	>100	<100	<25.6	<100	<0.1	<100	<1000
Silicon result	1.1V	108.95	87.74	21.21	82.85	0.082	Unable to measure	
	1.2V	103.6	82.3	21.3	83.2	0.083		
PEX Simulation	1.1V	110	92.7	17.3	67.57	0.067	18.3	183
	1.2V	106	87.7	18.3	71.48	0.071	23.2	202
Schematic Simulation	1.1V	120	87.5	32.5	126.95	0.127	17.5	175
	1.2V	112	83.5	28.5	111.32	0.111	38	380

Table 4.1: Design Summary of 100 KHz tunable CSRO for Chip-8

Here in 4.1, the power consumption of the chip can not be measured due to the CSRO is implemented in SoC and the digital core is always operating along with the oscillator. So acquiring the CSRO power consumption is not possible. From observing the simulation and PEX result it can be assumed that the power consumption should be $<$20 nw which would be $<$200 fj/cycle.

Incorporating these results into the previous work in Figure 1.4,1.5,1.6, we can further evaluate the performance of the design.

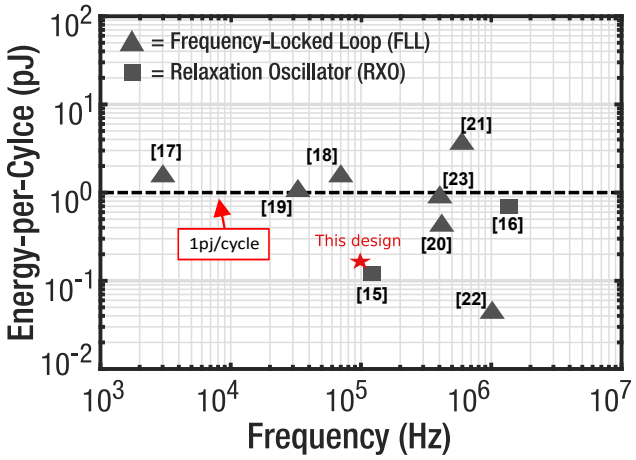


Figure 4.10: Comparison with previous work: Energy per cycle (pj/cycle) vs Frequency (Hz).

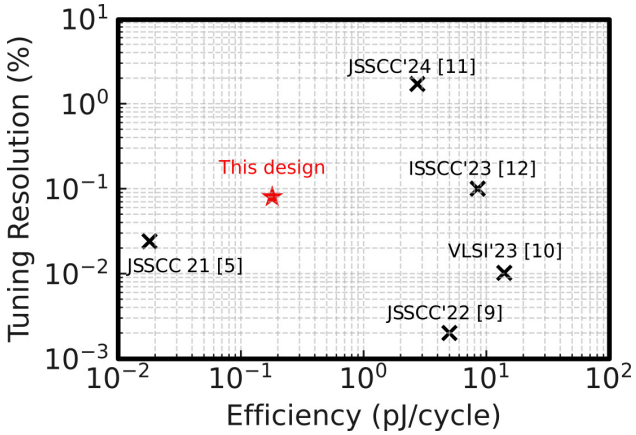


Figure 4.11: Comparison with previous work: Tuning resolution vs energy efficiency.

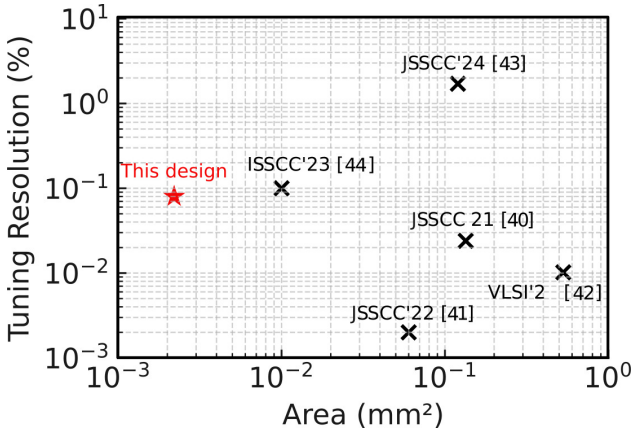


Figure 4.12: Comparison with previous work: Tuning resolution vs Area (mm^2).

Chapter 5

Conclusion

This thesis has introduced the design and implementation of a tunable on-chip current-starved ring oscillator, specifically optimized for ultra-low power consumption and high-precision tuning in textile-integrated wearable applications. Driven by the increasing demand for wearable electronics embedded within fabrics, this research addresses the need for precise, adaptable, and low-power clock sources that can support real-time data processing and synchronization across multiple integrated devices. Operating in the sub-threshold weak inversion region at 1.1V, the proposed oscillator achieves a frequency range from 22KHz from 87.74 kHz to 108.9 kHz which can be seen in table 4.1 and achieves a fine-tuning step size of 82.86 Hz (0.08%). This precise control ensures accurate time-stamping among sensor and processing units, enabling efficient synchronization in power-constrained environments such as wearable textiles.

Demonstrated through integration within an ARM Cortex M0+ SoC, the oscillator successfully meets the stringent timing requirements of advanced textile-based wearable systems, providing stable and adaptive timing solutions for dynamic sensing, processing, and communication tasks. With an energy efficiency of assumed $<$200 femtojoules per cycle, the oscillator ensures that clock stability and accuracy are maintained without compromising on power consumption—a critical feature for resource-limited applications. The chip has a maximum frequency of 108 kHz and a minimum of 87 kHz.

Despite being sensitive to temperature and process variations, the hypothesis of using optimiza-

tion technique of precise current control—to achieve high-precision tuning steps while maintaining low energy consumption in a Current Starved Ring Oscillator (CSRO) circuit has been validated. This confirms its capability to operate across a versatile range, adapting to the varied demands of textile-based electronics.

5.1 Future work

5.1.1 Temperature Compensation Techniques

- **Exploring Different Architectures**: Different temperature compensation methods can be explored to stabilize the oscillator's frequency across various temperatures. One potential approach is a temperature-compensated Current Starved Ring Oscillator (CSRO), where the circuit automatically adjusts to maintain a stable output despite temperature fluctuations. A combination of Frequency Locked Loop (FLL) and CSRO techniques could be explored to leverage the strengths of both architectures, thereby mitigating vulnerabilities to temperature and process variations. Additional circuitry could be incorporated to sense temperature and adjust the oscillator's current or voltage accordingly, helping to achieve consistent frequency output.

- $V_{\mathbf{DD}}$ **Voltage Regulation**: As temperature changes affect VDD stability, implementing a voltage regulation mechanism for VDD could improve frequency consistency. Given that the Low Dropout Regulator (LDO) showed output variations across temperature and from chip to chip—impacting the CSRO output—a stable VDD supply would ensure that the oscillator's performance remains unaffected by minor fluctuations in power supply, which often accompanies environmental temperature changes.

5.1.2 Adaptive Power Scaling

Developing adaptive power scaling techniques that enable the oscillator to adjust its power consumption dynamically based on application requirements. Introducing a feedback mechanism

could allow the oscillator to modify its frequency range in response to real-time processing and power needs, which would be highly beneficial for wearable applications with limited power resources. This approach ensures that the clock operates at high power only when high-performance processing is needed, thus extending battery life.

5.1.3 Multi-Sensor Network Integration

Extending the oscillator's application by exploring its use in synchronized multi-sensor networks embedded within textiles is a vital next step. By integrating the clock with wireless communication modules and examining synchronization techniques across distributed sensor nodes, this oscillator could support advanced monitoring and data collection within fabric-based structures. This application would be particularly useful in real-time health monitoring, environmental sensing, and seamless human-computer interactions within wearable textile systems.

5.1.4 Expanded Frequency Range for Broader Applications

Investigate the possibility of expanding the oscillator's frequency range to accommodate a wider set of applications beyond textiles. Modifying the circuit design and control mechanisms could allow the oscillator to support different frequency ranges, making it suitable for a broader range of low-power, precision-dependent IoT applications. This would open up potential use cases in healthcare, environmental monitoring, and consumer electronics, where compact, low-power clocks are essential.

5.1.5 Enhanced Tuning Resolution for Fine-Grained Control

Exploration of methods to further refine the tuning resolution, enabling even finer frequency adjustments is needed for extending the application of this oscillator. This could involve redesigning the control circuitry or implementing novel techniques to achieve sub-Hz tuning granularity. Such an enhancement would provide more precise control, making the oscillator adaptable to applications requiring very high accuracy. Improved tuning resolution would increase the versatility

of the oscillator, allowing it to meet the stringent timing demands of advanced applications.

Each of these directions presents a pathway to further enhance the performance and adaptability of the tunable ring oscillator, ensuring that it meets the evolving requirements of next-generation wearable and IoT applications.

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