Size Reduction Techniques for AC-DC Converters

A

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Abstract

AC-DC converters allow electronic devices that operate with low DC voltage to utilize the reliable and ubiquitous high voltage AC mains as their power supply. Small-sized converters are preferred by customers because of their portability, compatibility, and space-saving features. However, conventional converters use many discrete components, which occupy a large area of the printed circuit board (PCB). Additionally, several large components, such as capacitors and transformers, also lead to bulky size. Recently, many scholars focus on increasing the switching frequency of the converters to reduce the size of transformers or inductors [1–5]. However, the increase in switching frequency is limited to the efficiency requirement and the switching component's performance.

To further reduce the size, we investigated three strategies: (1) IC (integrated circuit) Implementations; (2) Active Capacitors; (3) Voltage-Drop Rectifiers. In this design, we applied a flyback converter structure to explore the IC Implementations and Active Capacitors methods. Furthermore, we searched for opportunities to replace the transformer with smaller voltage-drop rectifiers. An additional requirement is that the output voltage ripple ratio needs to be smaller than 2% to maintain the performance of the load device.

First, IC Implementation Technique is investigated to merge as many discrete components as possible. This strategy is estimated to save 10% of the space of the whole flyback converter with a 1.57% ripple ratio. Next, to further reduce the size, we need to shrink the size of the bulky components. One method to achieve that is replacing one of the big components with small elements. In this design, the large output capacitor is replaced with an active capacitor, and the total volume is expected to be reduced from 22.4 cm^3 to 10.41 cm^3 and the ripple ratio is around 1.87%. Finally,

we explored voltage-drop rectifiers to find opportunities to remove the transformer of the flyback converter. We found that one kind of voltage-drop rectifiers, the capacitor-fed rectifier, occupies only approximately 40% of the normal transformer's original physical size. A DC-DC converter is implemented after the capacitor-fed rectifier to suppress the output voltage ripple. Overall, these methods are effective to shrink the volume while maintaining the output voltage ripple small.

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Chapter 1

Introduction

1.1 Size Reduction of an AC-DC Converter

The various AC main sources around the world range from 90 to 240Vrms, leading to a need for international AC-DC converters for travelers and global electrical products. Compared with batteries, AC-DC converters provide more stable and trustable power for devices because of the almost infinite capacity and low dropout of the mains [1, 6, 7]. Large power converters are often bulky and heavy, making them difficult to carry around, especially for traveling. Additionally, a huge power converter is challenging to be implemented as a DC voltage supply for a physically small low-power system. As a result, reducing the size of the AC-DC converter is significant. However, three main difficulties get in the way of achieving that.

First, conventionally, many discrete components of the AC-DC converter systems, such as resistors, capacitors, and amplifiers, often need to be placed far apart on the printed PCB board to achieve the desired performance. In contrast, integrated circuits (ICs) combine multiple ingredients into a single package, occupying a smaller area of the PCB board. Consequently, customized integrated circuits are applied to shrink the size [1, 6–35].

Second, the requirement of giant input and output capacitors makes size reduction challenging.

The size of the passive capacitors is enormous because a certain amount of dielectric material is needed that limits their miniaturization. The total volume will be diminished if the colossal passive capacitor can be replaced with several small components and an IC. This device is called an active capacitor [36–40].

Third, the transformer of a flyback converter normally occupies a large proportion of the size. That is because a huge voltage gap between the high-voltage input and low-voltage output requires large turns ratio of the transformer. In other words, more coils are needed to be wound on the magnetic core. That requires a large magnetic core to place a large number of coils and thick insulation materials to isolate the input and output of the transformer. To realize the function of the transformer to transfer the high voltage to low voltage, we investigated voltage drop-down rectifiers (including capacitive-voltage divider rectifier [41] and capacitor-fed rectifier [42]) to search for a smaller substitute.

Among various AC-DC converters, the Flyback converters are commonly used for low-power energy conversion because of their simple structure, low cost, and low standby power consumption characteristics [43]. As a result, the flyback converter module designed by the University of South Carolina team, which transfers 90-240Vrms with 50Hz/60Hz AC input to a 5V/5W DC output, is adopted in the research of IC implementations and the Active Capacitor. Because the flyback converter's transformer typically occupies the most considerable proportion of the size, the possibility of replacing the bulky transformer with voltage-drop rectifiers to bridge the high voltage gap between AC input and DC output is explored.

1.2 Flyback Converter

Because the flyback converter is implemented as the main module of our IC implementation and Active Capacitor research, its introduction is necessary.

1.2.1 The Structure of Flyback Converter

The structure of a flyback converter is shown in Fig.1.1. The basic circuit includes an AC source, a rectifier, an input capacitor, a transformer, a switching device (e.g., MOSFET or GaNFet), a secondary-side diode, an output capacitor, and a control circuit with its feedback loop. The structure of the flyback converter is similar to a buck converter, and the difference is a transformer is exploited in the flyback converter instead of an inductor [30]. In the first phase, when the switch turns on, the input voltage is applied to the primary winding of the transformer, and the energy is stored in the transformer's magnetic field. In the second stage, the switch is turned off, and the energy stored in the transformer is rectified by the secondary-side diode and transferred to the output side. One part of the energy offers stable voltage for the output load, and the other part of the energy is stored on the output capacitor to supply a stable voltage when the primary side switch turns on again. The output capacitor is also essential for filtering and reducing the ripple of the output voltage.

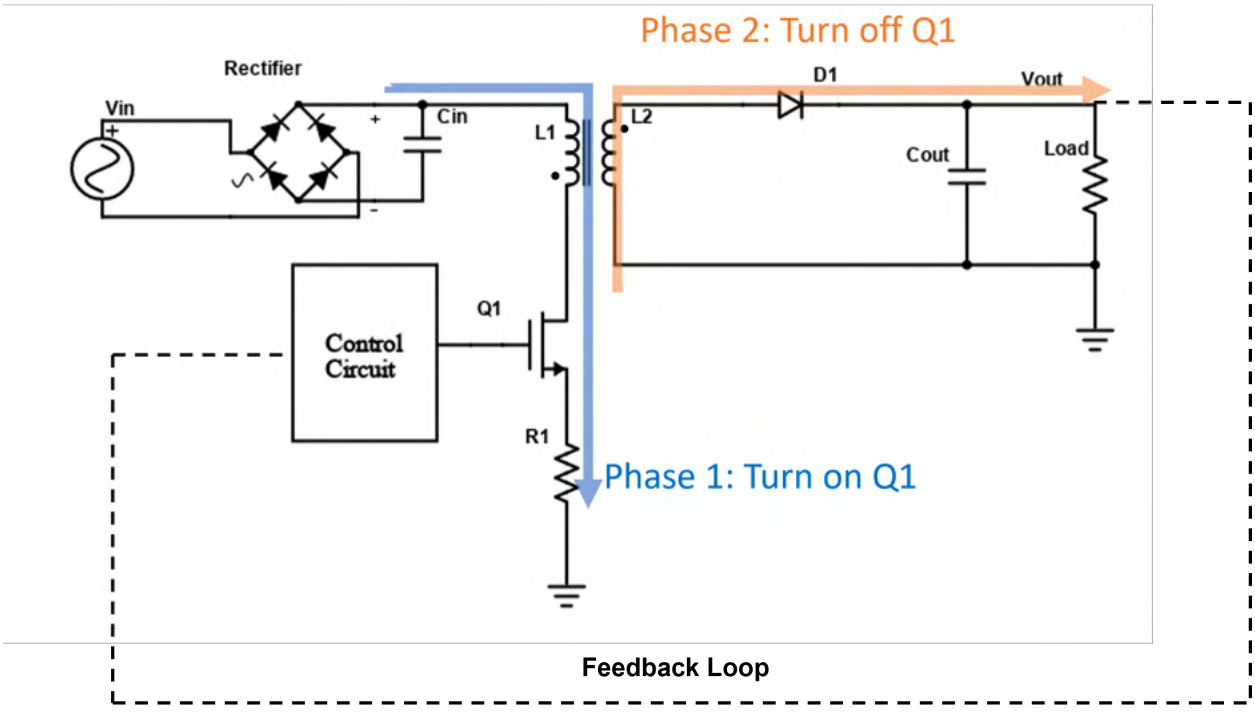

Figure 1.1: Basic Structure of a Flyback Converter

1.2.2 PWM Control Modes for the Control Circuit

As for the control circuit, there are two kinds of pulse width modulation (PWM) control strategies for flyback converter: Peak Current Mode (PCM) Control and Voltage Mode (VM) Control.

The structure of the peak current control mode is shown in Figure 1.2. The peak current mode control senses current flows through the primary winding of the transformer by detecting the voltage across the resistor R_{sense}. The obtained voltage V_s is feedback to the negative input of the PWM comparator. The positive input of the PWM comparator is the Error Amplifier output, which detects the voltage difference between the reference and output voltage. When V_s reaches V_{sensor}, the comparator generates the reset signal to the latch. A clock generator is connected to the set (S) input of the latch. The rising edge of the clock triggers a high voltage level of the latch; then, the latch waits for the reset signal from the PWM comparator to return to a low level. The output of the latch controls the switching of the GaNFet, which ultimately controls the output voltage.

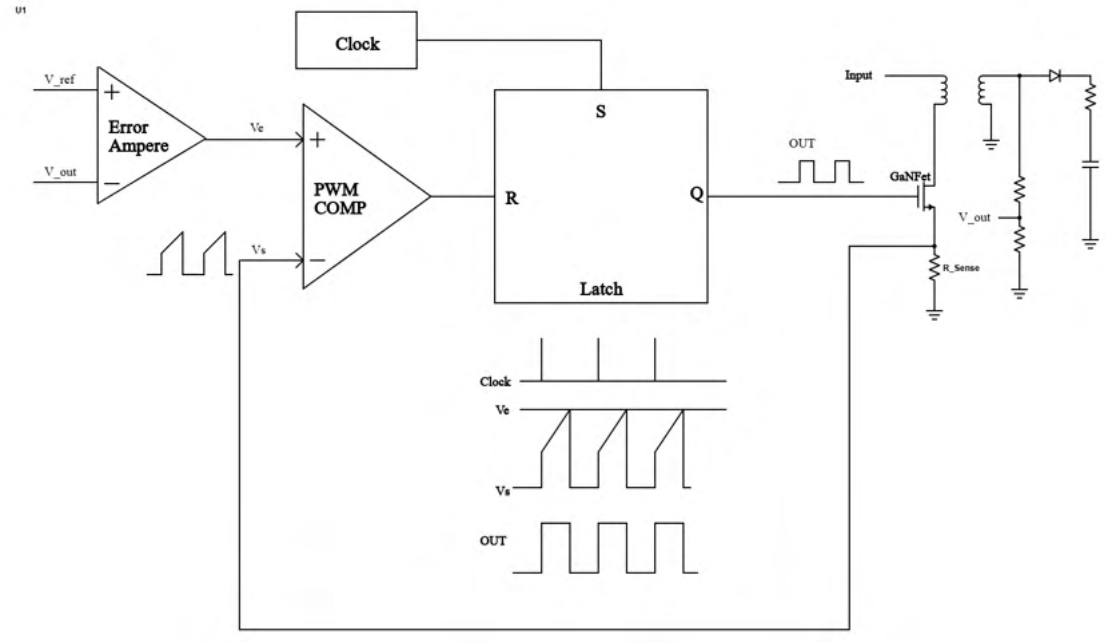

Figure 1.2: Peak Current Mode PWM Control

As shown in Figure 2.9, the voltage mode control detects the output voltage or voltage at a tertiary

winding of the transformer and feeds it back to the PID controller. The output of the PID controller is compared with a ramp voltage by going through the PWM comparator. If the PID controller output voltage V_e is higher than the ramp voltage V_r, the OUT voltage is high; otherwise, the OUT voltage is low.

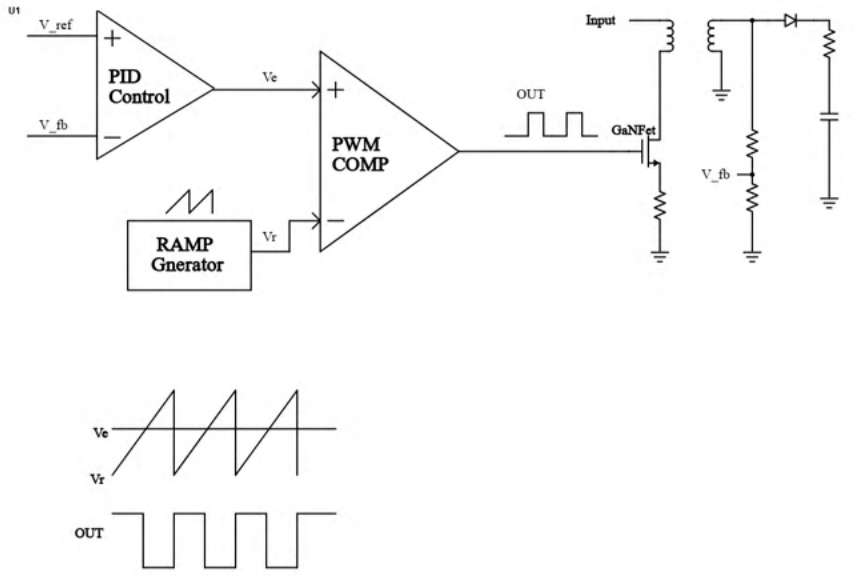

Figure 1.3: Voltage Mode PWM Control

Peak current mode control has two feedback loops: the current feedback loop and the voltage feedback loop. This dual-loop control can reduce the response delay since the primary side switch is under control. In comparison, the voltage mode control only has one feedback loop to control the output voltage at the secondary side of the transformer, which increases the latency. As a result, we used the peak current mode control for the analog integrated controller. However, if we implemented peak current mode control to the digital integrated controller, the dual loop means two analog signal need to be transferred to digital data through analog-to-digital converters (ADC). Two ADCs increase the complexity of the design, as well as power consumption. Consequently, we explored the voltage control mode for the digital integrated controller. The details of controlling the flyback converter with the peak current mode control are demonstrated in Section 2.2.1. Moreover, the digital control with Voltage mode can be found in Section 2.1.1

1.3 State-of-the-art Designs of Flyback Converters

After reviewing the recent work related to flyback converter designs [1, 6–35], a number of important metrics, including size, output voltage ripple ratio, efficiency, and transient time, are organized and analyzed. In this thesis, size reduction is the priority of the design. The second important metric is the small output voltage ripple because the converter needs to supply a stable DC voltage for the load devices. On the other hand, efficiency is less important compared with size and ripple.

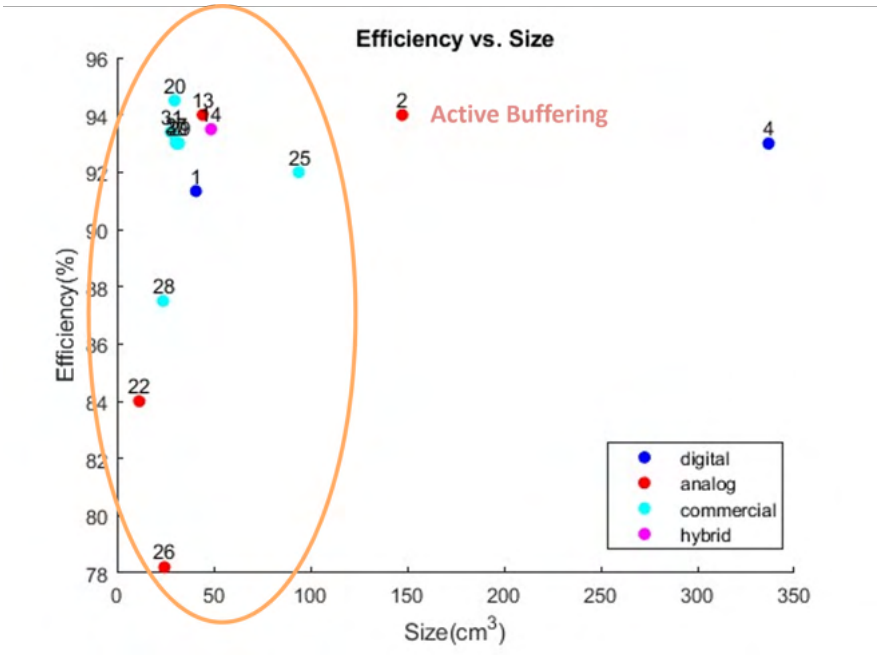

Figure 1.4: Efficiency vs. Size

First of all, Figure 1.4 and 1.5 present the efficiency of the flyback converters versus their size. Figure 1.4 includes data of reference [1, 6–35], and Figure 1.5 is the zoom in of the designs whose size smaller than 100cm^3. The plot 1.5 shows that all the IC implementation designs' data points fall within 70cm^3 [17, 18, 24, 26, 29–35]. However, the size of [1] is also smaller than 70cm^3, which indicates that the high switching frequency helps with size reduction. Compared with other methods, e.g., active buffering (147.42cm^3) [6] and implementing discrete components (336.72cm^3) [8], the IC implementation can significantly shrink the size (smaller than 70cm^3).

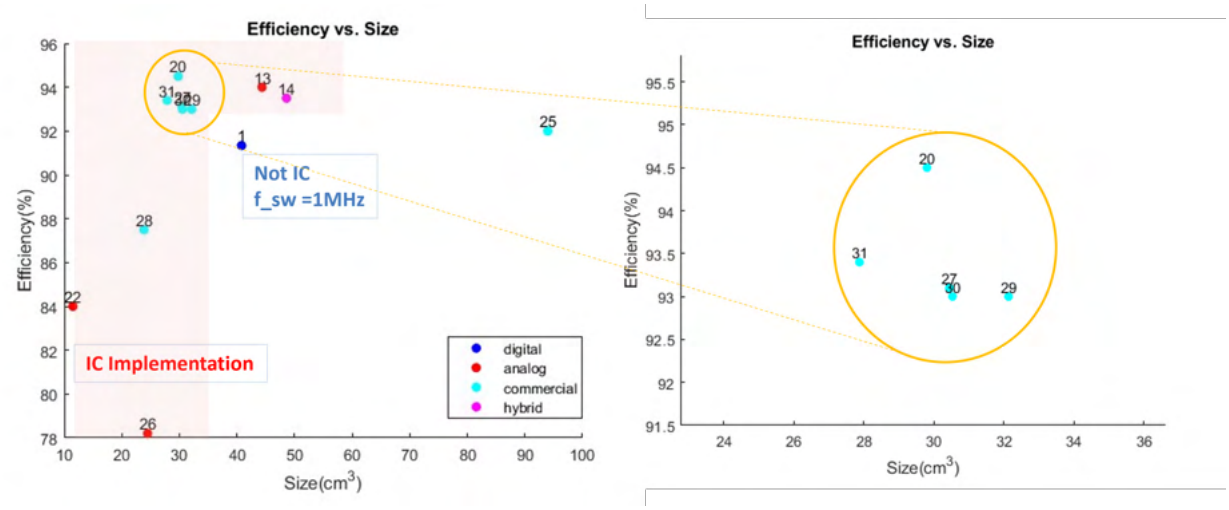

Figure 1.5: Efficiency vs. Size (Zoom in)

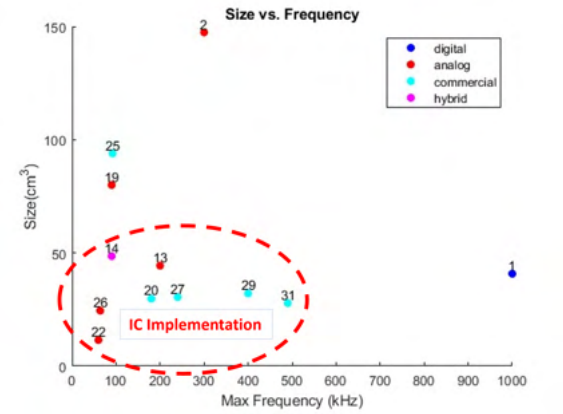

Figure 1.6: Size vs. Maximum Switching Frequency

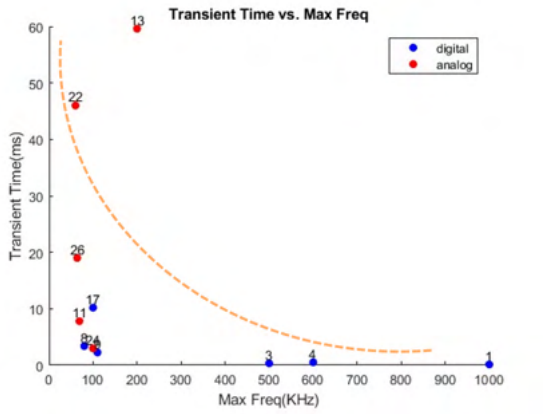

Figure 1.7: Transient Time vs. Maximum Switching Frequency

Furthermore, Figure 1.6 demonstrates the relationship between the size and the maximum switching frequency. The plot indicates that as switching frequency increases, size tends to decrease. Nevertheless, references [13-14, 20, 22, 26, 27] are under the line because the IC integration technique is implemented. For reference [2], even though its switching frequency is higher than many other designs, its size is the largest. For reference [1], it has the highest switching frequency (1MHz). Although smaller than many designs with low switching frequencies, its size is still larger than several IC designs. In conclusion, increasing the maximum switching frequency is a valid method to minimize the size of the flyback converters, but it is less effective than the IC implementation technique.

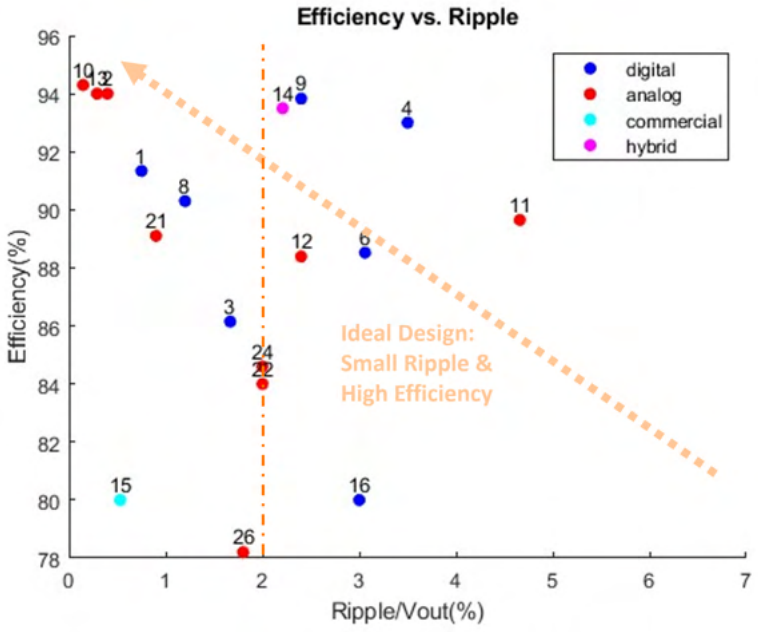

Figure 1.8: Efficiency vs. Ripple Ratio

Next, as shown in Figure 1.7, transient time reduces with the increase of the maximum switching frequency. In Figure 1.7, high-frequency design tends to use digital control strategies. As Figure 1.6 shows that a high switching frequency contributes to decreasing the size, exploring an integrated digital controller is meaningful.

Finally, Figure 1.8 explores the small output ripple because it is the second important metric.

Figure 1.8 presents the Efficiency vs. Ripple of the state-of-art flyback converter designs. Both analog and digital control can make a ripple ratio of less than 2%: 63.6% of them are analog control, and 27.3% are digital control. Overall, analog control's ripple is smaller than digital control's. Consequently, an analog integrated controller is required to be studied for the ripple requirement.

In summary, an effective approach to reducing the size of the flyback converter is IC implementation according to the analysis of Figure 1.4 and Figure 1.5. Another less influential method is increasing the switching frequency, which is commonly used for digital controlled flyback converters. (Figure 1.6) Finally, the analog controlled flyback converter is more likely to meet the ripple requirement based on the data from Figure 1.8. As a result, both digital and analog controlled flyback converters with ICs are explored in Chapter 2.

1.4 Active Capacitor

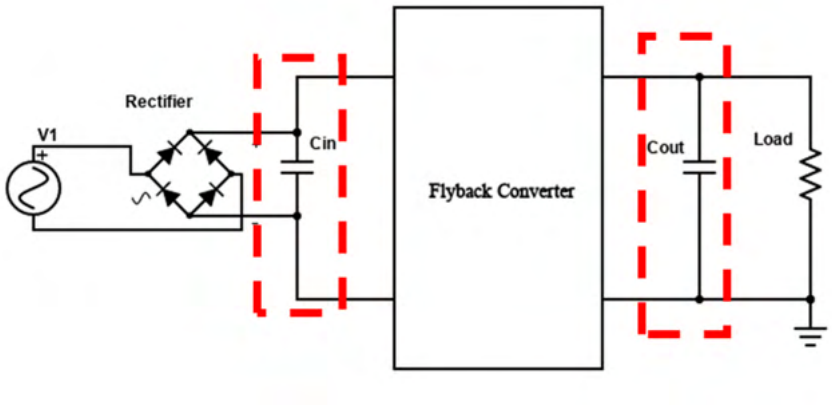

Figure 1.9: Input and Output Capacitors of a Flyback Converter

For an AC-DC converter, capacitors are essential for producing a DC voltage at the output terminal. As shown in Figure 1.9, conventionally, a large input capacitor is needed to maintain a small-ripple voltage at the output of the rectifier to transfer to the flyback converter. Additionally, the bulky output capacitor is parallel with the load to keep the output voltage constant. However, a big capacitor

means a vast size occupant. To reduce the size of the converter, instead of implementing the large passive capacitor, several smaller components are used to make the converter more compact.

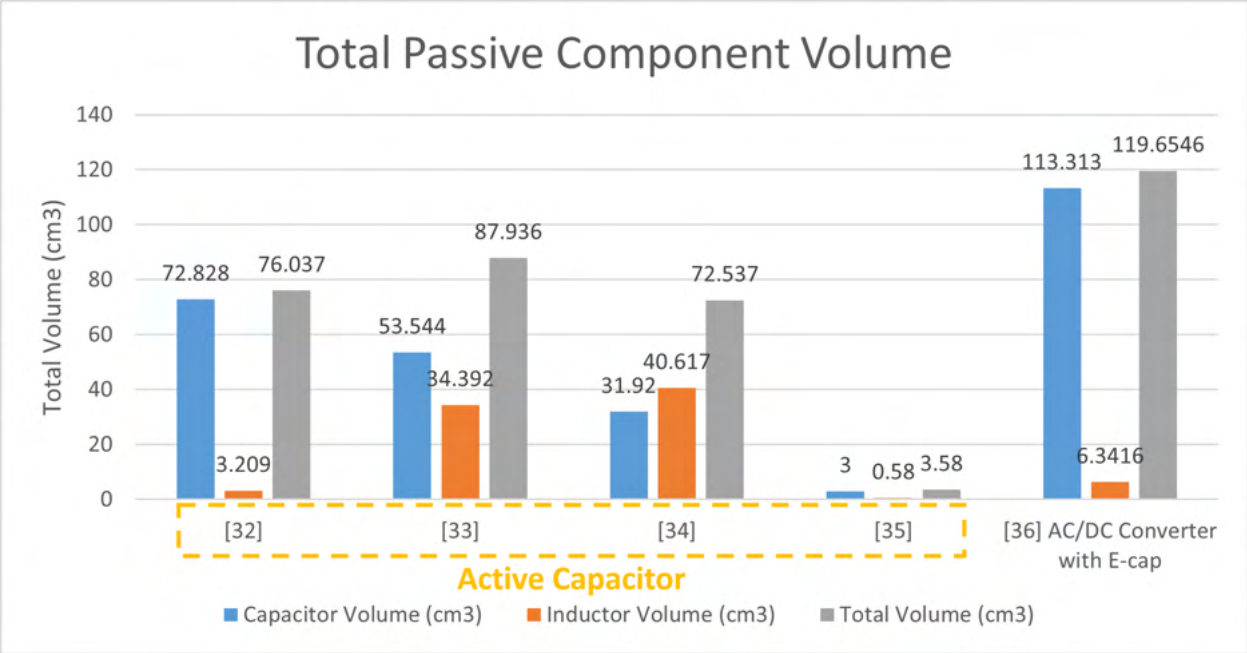

Figure 1.10: Total Passive Component Volume of Active Capacitors

The active capacitor is formed with an auxiliary capacitor and a bidirectional converter. The bidirectional converter could be a buck, boost, buck-boost, or half-bridge converter. [36] Figure 1.10 shows that compared with conventional flyback converters with an electrolytic capacitor (E-cap), the active capacitor structure effectively decreases the total volume of the passive components. The total volume of passive components for a flyback converter with an E-cap is 119.6546 cm^3 [40]. However, the total volume of the most giant active capacitor is 87.936 cm^3, which is around 73.5% of the volume of conventional design [37]. More interestingly, the smallest active capacitor's total volume is 3.58cm^3, approximately 3% of the traditional design [39]. In the [39], the input passive capacitor of a flyback converter is replaced by the active capacitor, and the volume of the input capacitor is reduced from 15.63 cm^3 to 3.58 cm^3. Because the required capacitance is effectively reduced, the size of the AC-DC converter is diminished. Because [39] is the tiniest active capacitor, its structure is explored in Capture 3 for replacing both the input and output capacitors of a flyback

converter.

1.5 Voltage-Drop Rectifiers

One challenge of AC-DC converter design is how to bridge the massive gap between high-voltage AC input (90-240Vrms) and low-voltage DC output (5V). As shown in Figure 1.11, there are three methods to deal with this issue [42]. A transformer (Figure 1.11 (a)) can adjust the turn ratio of windings to convert a high voltage to a low level, such as increasing the turns on the primary side or decreasing the turns on the secondary side. A well-designed transformer can achieve high levels of efficiency. However, typically, transformers are large and heavy, which motivates us to replace them with other structures. Figure 1.11 (c) demonstrates a resistive voltage divider. The power density of the resistive voltage divider is higher because the size of the resistors is smaller than capacitors and transformers. The trade-off is its power consumption decreases the efficiency of the converter. If the input voltage Vin is large, the power consumption is enormous, which leads to an ultra-low efficiency. As shown in Figure 1.11 (b), the capacitive voltage divider is a reasonable choice to replace the bulky transformer. Even though it occupies more area than a resistive divider, the conversion efficiency is almost unit for ideal capacitors. Suppose the capacitive voltage divider's input can be connected to the AC source and its output to the rectifier. In that case, the voltage can be dropped down in the initial stage, and the transformer and fewer high-voltage devices are needed. This structure is named capacitive voltage divider rectifier, as shown in Figure 1.12 [44].

Figure 1.12 displayed that the Capacitive Voltage Divider Rectifier is formed with a protective resistor (R_{in}), a capacitive voltage divider (C_{ac_1} and C_{ac_2}), and a rectifier (D_1-D_4). The capacitive divider helps step the input voltage down according to the equation 1.1. The rectifier regulates the AC voltage to a DC voltage with significant fluctuation (V'_{in}). Then its output is connected to the DC-DC converter to suppress the ripple and provide a smooth DC voltage to the load.

$$V_{br} = V_{in} \times \frac{C_{ac_1}}{C_{ac_1} + C_{ac_2}} \tag{1.1}$$

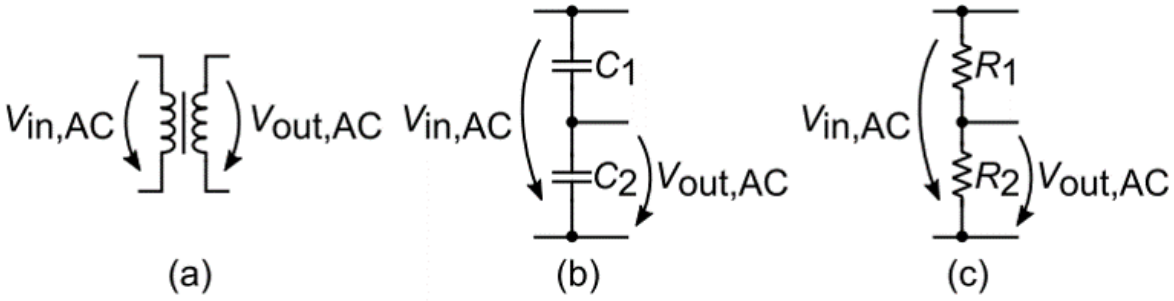

Figure 1.11: Three methods of converting a high voltage to a lower level: (a) a transformer, (b) a capacitive divider, (c) a resistive divider

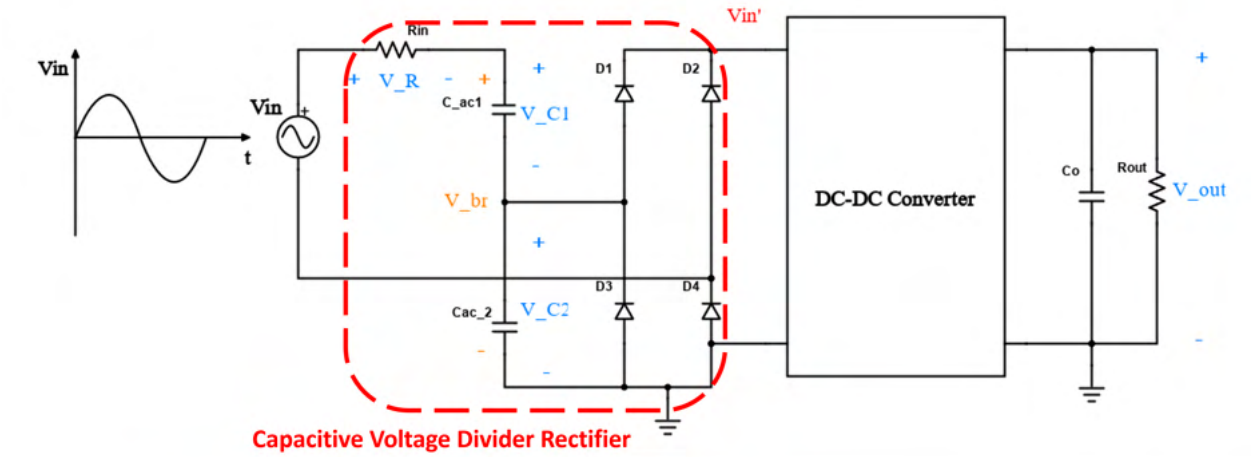

Figure 1.12: Capacitive Voltage Divider Rectifier

Even if the capacitive voltage divider generates a low voltage V_{br}, two high-voltage capacitors are required, and their size is colossal. For example, a 60uF AC capacitor, which can withstand 240Vac, is 367 cm^3 (THAS600M400AA0C). Instead of two capacitors, the voltage can be divided by one capacitor with the capacitor-fed rectifier, which is known as the capacitor-fed rectifier [41]. Its structure is shown in Figure 1.13. The capacitor-fed rectifier is similar to the capacitive voltage divider rectifier, which includes a protective resistor (R_{in}), a capacitor (C_{ac}), and a rectifier (D_1-D_4). Compared with a capacitive voltage divider rectifier, its benefit is the reduction of area occupation. Its drawback is that the heavy load can influence V_{br}, even worse if it affects the AC input source. In this research, size reduction is the priority of the design, and the load is light; the exploration is focused on the capacitor-fed rectifier. An example of converting a 120Vrms AC voltage to a 30V DC voltage with a capacitor-fed rectifier is demonstrated in Chapter 4.

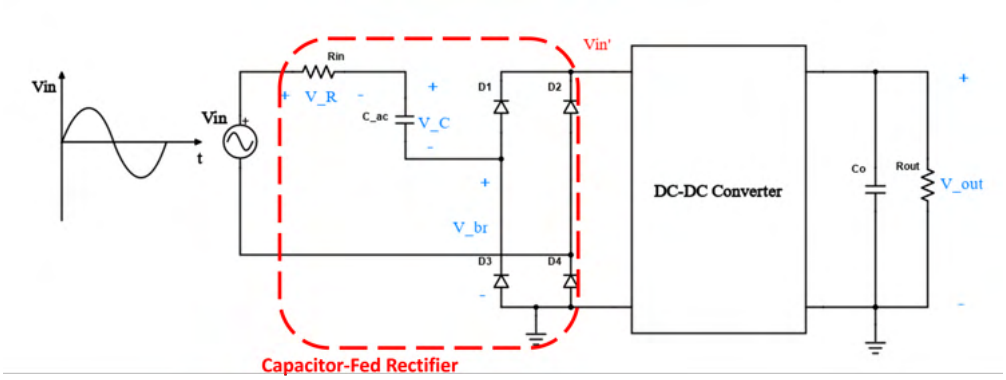

Figure 1.13: capacitor-fed Rectifier

1.6 Thesis Statement

1. Size reduction of AC-DC converters is the priority of this research because its portability feature allows customers to carry them around conveniently, such as for traveling. Small converters can also be the DC voltage supply for size-limiting devices, such as Internet of Things (IoT) devices, to obtain power from ubiquitous mains AC sources.

2. The second goal of our design is to suppress the output voltage ripple smaller than 100mV (ripple ratio is smaller than 2%). The reason is that a nice performance of an electronic circuit load needs a stable and constant voltage supply, especially for a voltage-sensitive device.

1.7 Outline of the Thesis

In conclusion, the structure of this thesis is summarized in Figure 1.14.

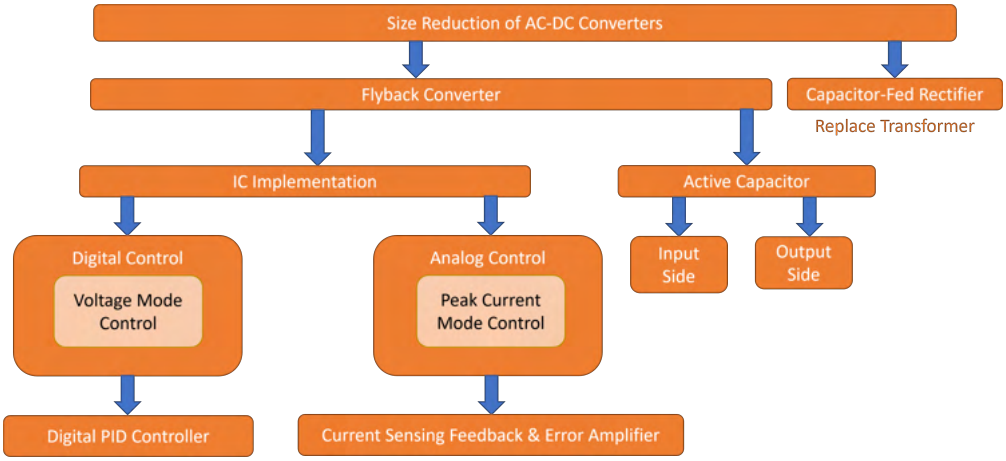

Figure 1.14: Outline of the Thesis

In this thesis, these three types of size reduction techniques are discussed: (1) IC Implementations; (2) Active Capacitors; (3) voltage-drop Rectifiers. The flyback converter is the fundamental structure for IC Implementation and Active Capacitor explorations. The capacitor-fed rectifier is investigated for the potentiality of replacing the bulky transformer. At first, integrating as many discrete components as possible on chips to minimize the area of the PCB board is introduced in Chapter 2; Next, the process of replacing the output capacitor of the flyback converter with an active capacitor is presented in Chapter 3; Then, voltage-drop rectifiers are explored to eliminate the usage of the giant transformer and reduce the number of high-voltage components to shrink the size in Chapter 4; Finally, the thesis is summarized and concluded in Chapter 5.

Chapter 2

IC Implementation for Flyback Converter

According to the literature review analysis in Section 1.3, exploring the IC Implementation technique for size reduction of the flyback converters is worthwhile. Because discrete components occupy much more area of the PCB board than the chip, the more parts of the converter integrated into chips, the smaller the size will be. However, not all components of the flyback converter can be integrated on-chip. For instance, the diodes of the rectifier need to withstand 240Vrms input voltage, which is much higher than the maximum volt that the chip PDK components can bear with. Another example is that the capacitance of the output capacitor is too large (around 100uF) to be fabricated on small silicon material. As a result, the decision to choose the parts to be integrated is essential.

The integration requirement is: (1) The voltage across the components should be lower than the IC maximum voltage. (2) The value of these components (e.g., capacitance, inductance) must be smaller than the maximum value of the chip components. The feedback control loop is the flyback converter's segment that can fulfill the conditions mentioned above.

In this Chapter, digital and analog integrated controllers are investigated. The control strategy of the digital circuit is voltage mode PWM control, and that of the analog circuit is peak current mode PWM control, as mentioned in Section 1.2.2.

2.1 Digital Integrated Controller

2.1.1 Voltage Mode Control

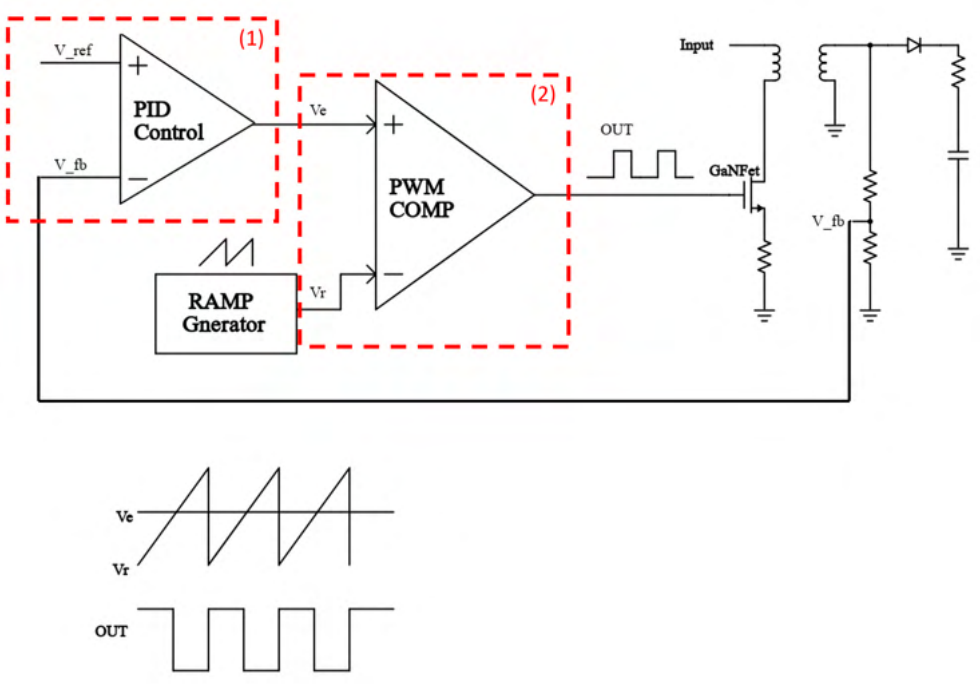

Figure 2.1: The Structure of Voltage Mode Control

Control Strategy of Voltage Mode

The voltage mode PWM control structure is presented in Figure 2.1 [45]:

1. The PID controller detects the feedback voltage from the converter's output side or the transformer's tertiary winding to form the closed-loop control. Then the PID controller generates the control signal V_e by operating the input reference voltage and feedback voltage.

2. The PWM comparator compares the V_e with ramp voltage from the ramp generator. When $V_e < V_r$, the output of the PWM comparator OUT is 1. When $V_e > V_r$, the result of

the PWM comparator is 0. The signal OUT governs the switching of the GaNFet, which ultimately determines the output voltage.

3. If the feedback voltage is low than the reference voltage, signal V_e will increase. This causes a more extensive duty cycle of the OUT signal, and GaNFet turns on for longer. This means more energy is transferred to the output side, which helps raise the output voltage higher and closer to the reference voltage. Vice versa, the control loop can also reduce the output voltage if it is higher than the reference voltage.

Advantages of Voltage Mode Control

1. There is only one feedback loop, making circuit analysis easier.
2. A large-amplitude ramp waveform provides a good noise margin for a stable modulation process.

Disadvantages of Voltage Mode Control

1. Any change in line or load must first be sensed as an output change and then corrected by the feedback loop. This usually means a slow response.
2. There are two poles of the control loop [45]. Compensation is further complicated by the fact that the system is second-ordered.

2.1.2 Digital PWM Controller

Figure 2.2 demonstrates the structure of the designed digital PWM controller. The input of the PWM controller is the feedback voltage (V_{fb}), which is obtained from the feedback loop or output voltage. The analog-to-digital converter (ADC) detects the feedback voltage with the frequency f_{ADC} and transferred this analog signal to the digital data ($V_{fb(k)}$). As one of the digital PID

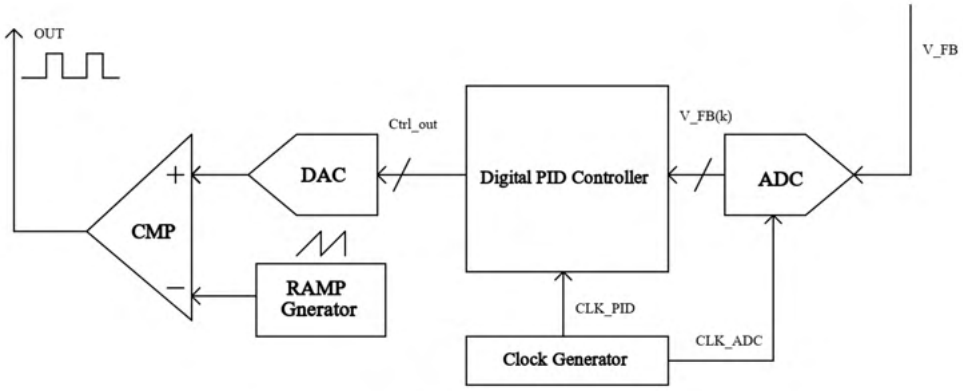

Figure 2.2: Digital PWM Controller

controller's inputs, it will be compared with the reference voltage and calculated to get the digital control output signal. The function of the digital PID controller is going to be described in Section 2.3. The clock generator offers clock signals for both the digital PID controller and ADC. The digital-to-analog converter (DAC) changes the control output to the analog voltage Ve. According to the voltage mode PWM control, the Ve and the ramp voltage are the comparator's inputs, and the comparator's output is the control wave of the primary GaNFet.

2.1.3 Digital PID Control

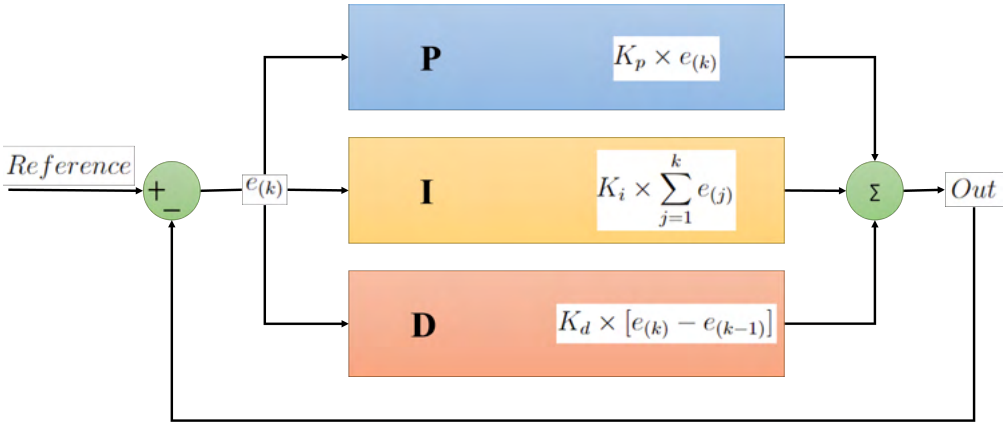

Figure 2.3: Digital PID Control

The PID control is formed with proportional, integral, and derivative units, as presented in Figure 2.3. It has become the core controller in this system due to its simple structure, good stability, reliable operation, and convenient adjustment [46]. The following is the explanation of the PID algorithm. K_p, K_i, and K_d are the proportional, integral, and derivative coefficients separately. The signal $e_{(k)}$ is the error between the reference and feedback voltage. The sum of $e_{(j)}$ is the sum of the errors from the first to k^{th}. And $e(k-1)$ is the previous error. From this algorithm, the PID control's equations are:

(1) Proportional unit:

$$P = K_p \times e_{(k)} \tag{2.1}$$

(2) Integral unit:

$$I = K_i \times \sum_{j=1}^{k} e_{(j)} = K_i \times e_{(k)} + K_i \times \sum_{j=1}^{k-1} e_{(j)} = K_i e_{(k)} + prevIntegral \tag{2.2}$$

$$prevIntegral = K_i \times \sum_{j=1}^{k-1} e_{(j)} \tag{2.3}$$

(3) Derivative unit:

$$D = K_d \times [e_{(k)} - e_{(k-1)}] \tag{2.4}$$

(4) The output of the PID control is:

$$Out = P + I + D = K_p \times e_{(k)} + K_i \times \sum_{j=1}^{k} e_{(j)} + K_d \times [e_{(k)} - e_{(k-1)}] \tag{2.5}$$

According to the PID control theory, the Digital PID Controller is constructed as Figure 2.4. [47] The reference voltage and digital feedback voltage signal are input to the controller's subtractor. The error $e_{(k)}$ is generated from the subtractor and sent to proportional, integral, and derivative units for further operation. For the proportional unit, the $e_{(k)}$ times the proportional coefficient K_p to get the proportional result. For the integral unit, first, the $e_{(k)}$ times integral coefficient K_i, then add the previous integral signal to get the output. For the derivative unit, error $e_{(k)}$ is subtracted by the previous error $e_{(k-1)}$, and the error difference is multiplied by the derivative coefficient K_d to gain the derivative output. The sum of the results of proportional, integral, and derivative units

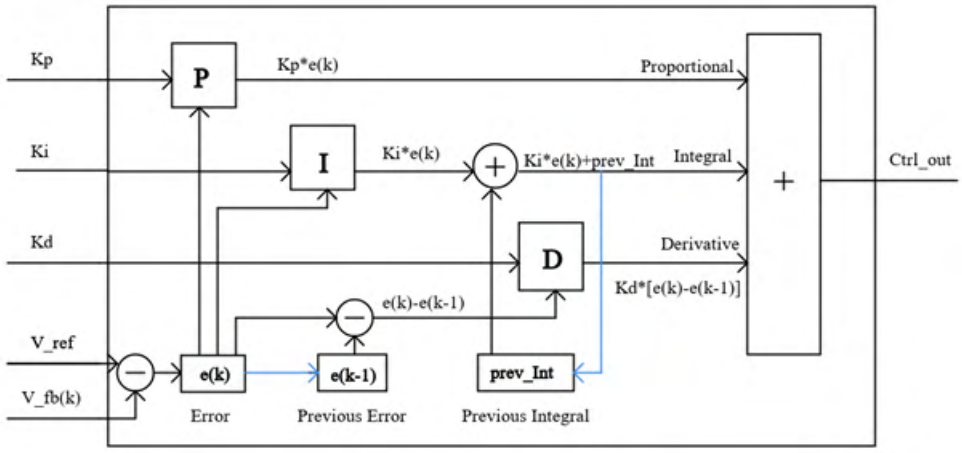

Figure 2.4: Digital PID Controller Strucutre

is the control output of the Digital PID Control. In the next clock period (labeled by blue arrows), the error $e_{(k)}$ and temporary integral $tempIntegral$ will be separately stored in the previous error and previous integral registers.

This digital PID controller is verified with a flyback converter model, which converts 120Vrms input to a 5V output. The switching frequency of the flyback converter is 500KHz. The sampling frequency of the ADC of the DPID controller is 1MHz, and the internal clock frequency of the DPID controller is 2MHz. The simulation testbench is displayed in Figure 2.5.

The simulation result of the output voltage of the flyback converter is shown in Figure 2.6. The output voltage achieves 5V after 2.943ms start-up time. The range of the output voltage is from 4.951V to 5.05V. In other words, the output voltage ripple is 99.32 mV, and the ripple ratio is 2%. From this simulation, the efficiency of this flyback converter system is also measured as 90.86%.

2.1.4 ADC Sampling Frequency and PID Operation Frequency

During the simulation process, we found that two metrics affect the output ripple to a large extent: ADC Sampling Frequency and PID Operation Frequency. Ripple is one of the most significant characteristics, and exploring how to suppress it is crucial. First, we fixed the PID operation

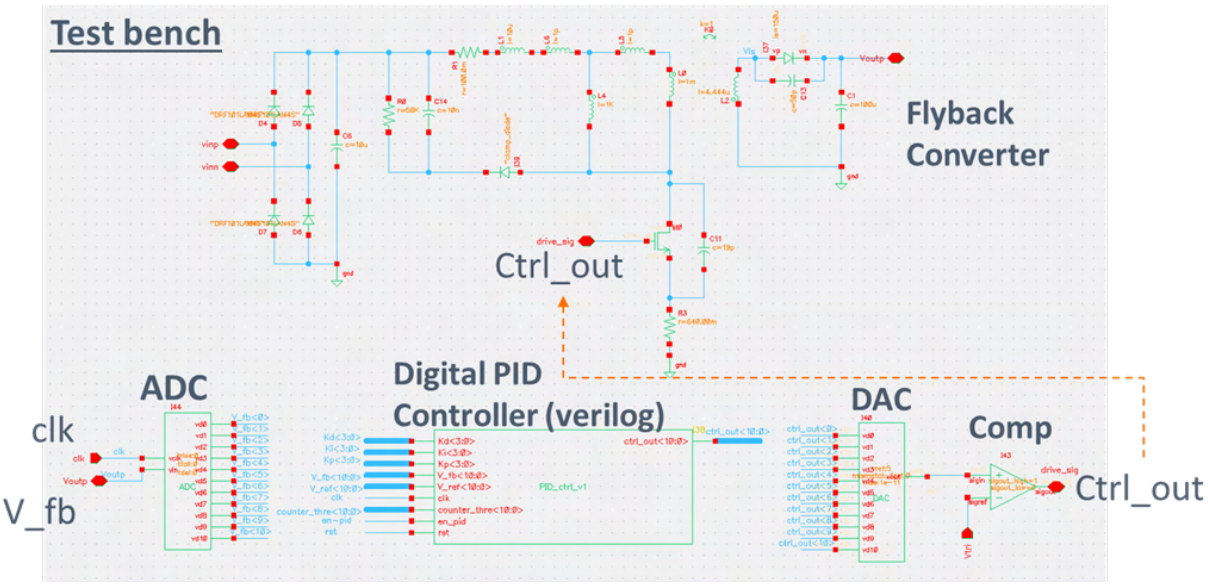

Figure 2.5: Testbench of the Flyback Converter with DPID Controller

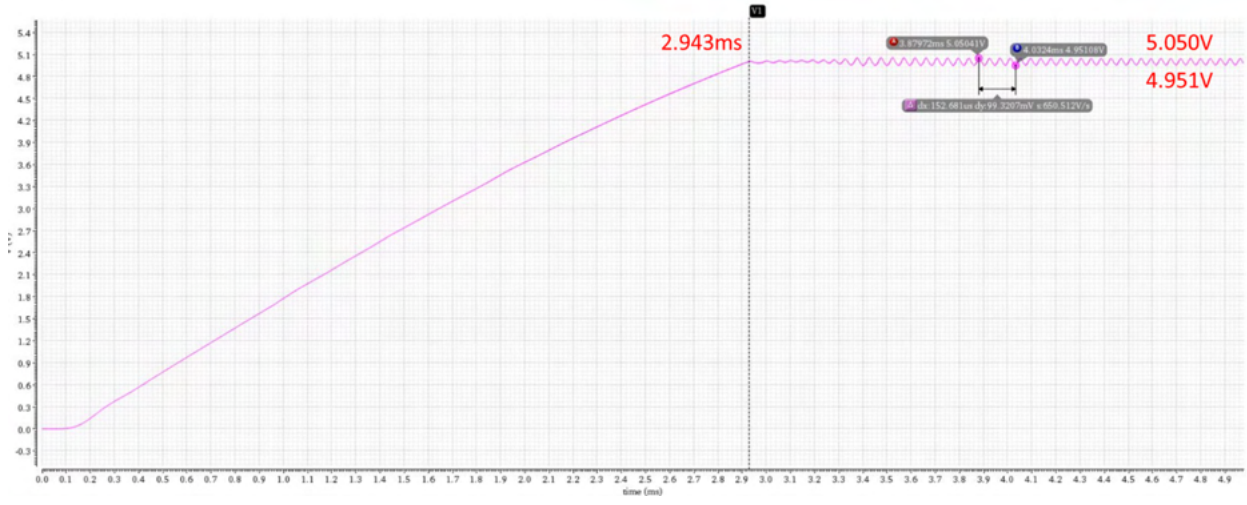

Figure 2.6: Output Voltage of Flyback Converter with DIPD Controller

frequency at 4MHz, swept the ADC sampling frequency from 200KHz to 2MHz, and observed the output voltage ripple. Next, the ADC sampling frequency was set as 1MHz, and the PID operation frequency varied from 500KHz to 4MHz.

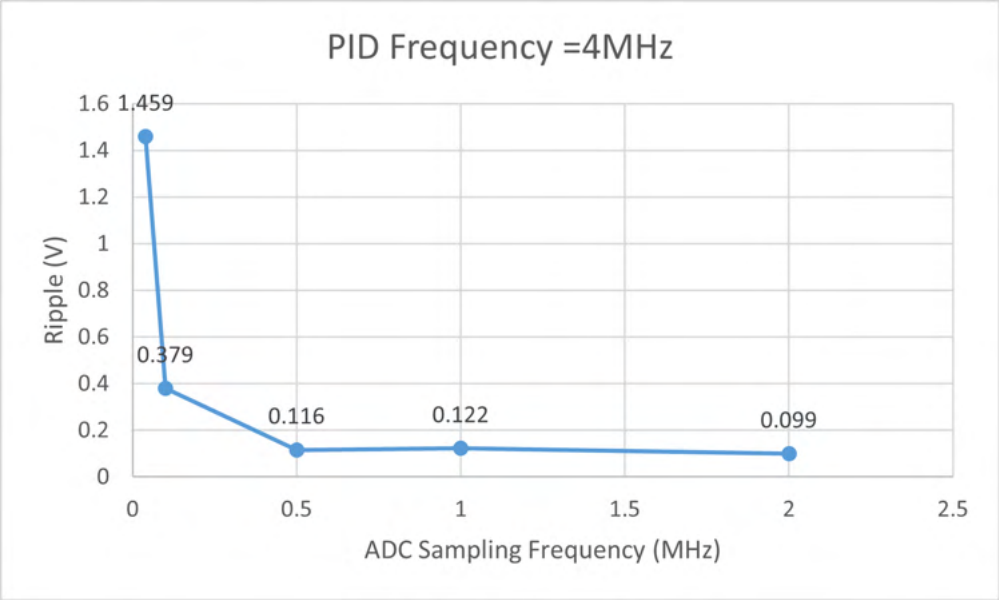

Figure 2.7: Output Voltage Ripple vs. ADC Frequency

As shown in Figure 2.7, there is a trade-off between the voltage ripple and ADC sampling frequency. The increase of the ADC sampling frequency leads to a decrease in ripple. This is because the time between two sampling points is shorter, and more detecting data are transferred to the controller, which makes the control more precise. Nevertheless, the slope of the ripple decrease becomes slower due to the limitation of the fixed operation frequency of the PID controller (4MHz). Even though more data are transmitted to the controller, due to the extended operation period of the digital controller, there needs to be more time for the digital controller to deal with such an amount of data and generate output control signals in time. The reduction of the ripple is mitigated. However, raising the PID operation frequency could further reduce the ripple.

Increasing the ADC sampling frequency is beneficial for reducing the ripple. However, there are several trade-offs. First, the increase in the sampling frequency leads to a large switching power consumption on ADC. Second, a high frequency will likely cause ADC's functional errors,

especially for a high-resolution one. Third, the cost will increase because reducing the ripple requires not only the ADC sampling frequency but also the PID operation frequency to be high.

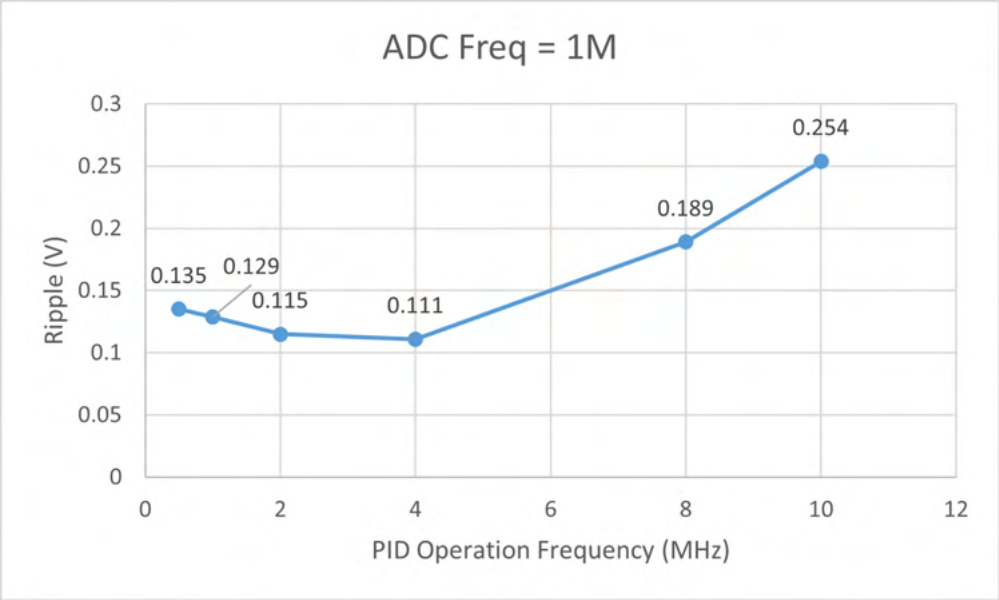

Figure 2.8: Output Voltage Ripple vs. PID Operation Frequency

Figure 2.8 shows that when the ADC sampling frequency is fixed at 1MHz, the ripple decreases with the increase of PID operation frequency from 500kHz to 4MHz. The reason for this is that the rise of the controller's speed can contribute to improving the control signal updating speed. But the ripple increase when the PID operation frequency is higher than 4MHz. This is because the data input speed is much slower than the operation speed, and sampled data is out-of-date for the PID controller. The output control signal would be less accurate because of the over-calculation. As a result, the PID operation frequency needs to be decided based on the ADC sampling frequency.

2.1.5 Design Challenges

1. High-Frequency ADC Design

As analyzed in Section 2.1.4, the sampling frequency of the ADC should be large enough to update the input data of the digital PID controller quickly. In order to minimize the output voltage ripple,

an ADC with a high sampling frequency is required. However, it is complex to design a high-speed ADC because the signal integrity is difficult to maintain with a high sampling frequency due to factors such as parasitic capacitor distortion and signal attenuation [48]. Another reason is that high-frequency sampling tends to insert noises and make the measurement less accurate. Consequently, the high sampling frequency ADC design is one challenge of designing the digital PWM controller.

2. High-Resolution ADC Design

A higher resolution ADC means the sampled data is closer to the original signal. For accurate control, the precision of the input signal is essential. However, it is challenging to design a high-resolution ADC because of the quantization noise, linearity, and speed limitations. [49]

According to the reference [1], the resolution of ADC needs to be determined by the maximum allowed variance or ripple of the output voltage, as shown in the equation 2.6.

$$\Delta V_o \geq \Delta V_{o-ADC} = \frac{V_{A/D}}{2^{n_{A/D}}} \times \frac{1}{H}, (H = \frac{V_{ref}}{V_o}) \tag{2.6}$$

V_{ref} is the reference voltage, $V_{A/D}$ is the full range of ADC, $n_{A/D}$ is the bit number of ADC, and H is the output voltage sensor gain.

In this design, the output voltage ripple ratio requirement is limited to 2% (lower than 100mV for 5V output), which also means a small ΔV_o. According to the equation 2.6, the ways to mitigate this trouble are to reduce the full range of ADC ($V_{A/D}$) and increase the output voltage sensor gain (H).

2.2 Analog Integrated Controller

2.2.1 Peak Current Mode Control

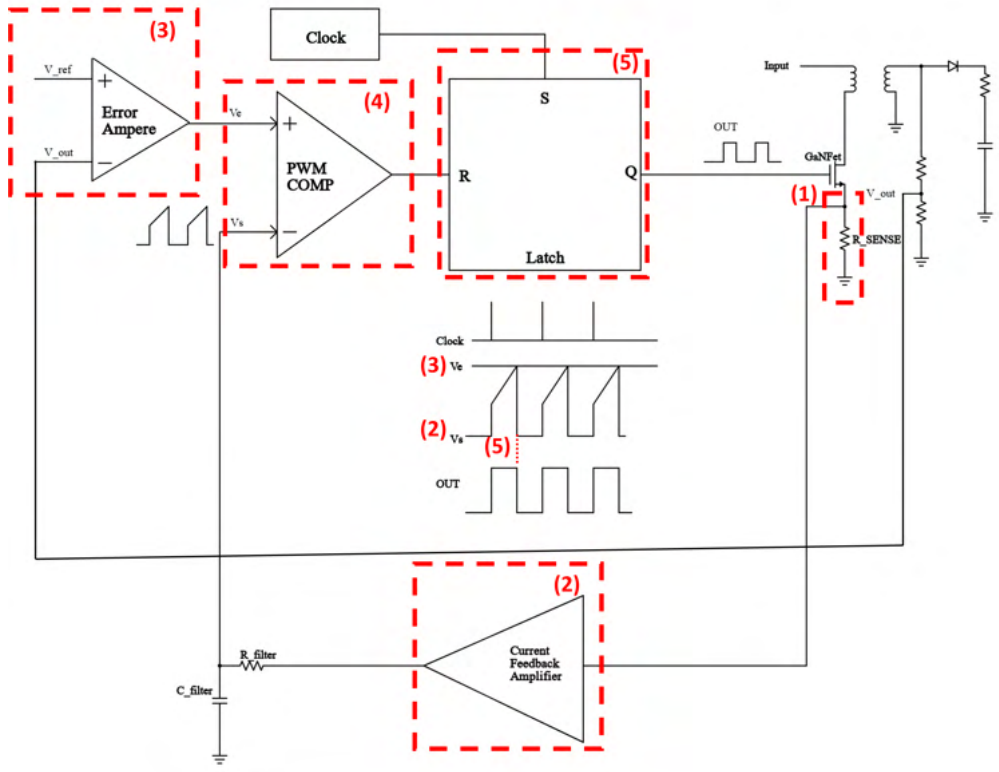

Figure 2.9: Peak Current Mode Control

The peak current mode control structure is presented in Figure 2.9 [50]. This is a dual loop control: current feedback loop and voltage feedback loop. The current feedback loop detects current flowing through the primary winding of the transformer, and the voltage feedback loop measures the voltage at the output side or the feedback voltage from the tertiary winding of the transformer. The peak current mode control can transfer a second-ordered system to a first-ordered one [45].

Control Strategy of Peak Current Mode

1. The resistor R_{SENSE} transfers current flowing through the primary side winding to a voltage signal. Then this signal is sent to the Current Feedback Amplifier to amplify its amplitude.

2. The Current Feedback Amplifier boosts the small signal V_s then an RC filter removes the leading-edge spike noises to get the voltage V_s.

3. The Error Amplifier sensed the output voltage and compared it with the reference voltage. The error is amplified and sent to the PWM comparator.

4. PWM Comparator compares sensing voltage V_s with the error amplifier's output voltage V_e. When V_s is smaller than V_e, the output of the comparator is 0, and the reset signal of the PWM latch is 0. When vs is equal to V_e, the output of the comparator is 1, and the reset signal is 1.

5. PWM Latch is the component that generates the control signal. The set input S of the Latch is the clock signal from the clock generator. The clock triggers the latch output to be high, and the transistor turns on. Then the current flows through the inductor and V_s rises. No reset signal exists when V_s is lower than V_e, so the latch output stays high. When V_s reaches V_e, the PWM comparator generates the reset signal, the latch output becomes low, and the transistor is turned off. Then there is no current flow through R_{SENSE}, and V_s becomes zero.

6. Over-current protection: because V_e is limited by the error amplifier, and V_s cannot be higher than V_e as mentioned above, the amplitude of the sensing current is restricted. This provides the protection of the transformer and GaNFet.

7. When the output voltage is lower than the reference voltage, the error amplifier's output increases. It takes a longer time for V_s to reach V_e, which also means a longer time for turning on the GaNFet. More energy is transited to the transformer and then the output side. Finally, the output voltage will increase closer to the reference voltage. The condition of the output voltage higher than the reference voltage is similar.

Advantages of PCM

1. Improving stability and dynamics of voltage regulators because the peak current mode control is a dual-loop control: the current and voltage feedback loop. The current feedback loop reduces the system's order, making the compensator's design easier.

2. The delayed response is mitigated compared with voltage mode control since the current loop could directly sense the line voltage changes.

3. Better short current protection: As Section 2.2.1 mentioned, the current flowing through the inductor and transistor is limited. Consequently, this offers over-current protection.

Disadvantages of PCM

1. Two feedback loops make circuit analysis more difficult.

2. The control loop becomes unstable at duty cycles above 50% unless slope compensation is added.

3. The leading-edge current spike is a particularly troublesome noise source, typically caused by transformer winding capacitance and output rectifier recovery current. An RC filter or an active filter can remove this noise.

2.2.2 Current Feedback Amplifier

One design challenge for the inner current feedback loop is eliminating the leading-edge current spikes caused by the switching of the GaNFet. These noises' amplitude is higher than the sensing current. If these noises are transited to the input of the comparator, the output of the comparator would be determined by these noises rather than the desired sensing current. (Figure 2.10)

An RC filter could effectively remove leading-edge current spikes. However, the output signal of the filter is attenuated. To boost the detected signal, an operational amplifier (op-amp) is applied

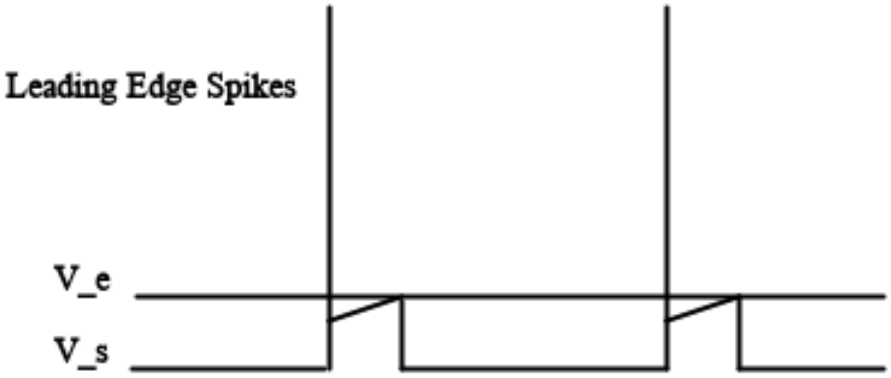

Figure 2.10: Leading-Edge Current Spikes

before the RC filter. The structure of the current feedback loop is shown in Figure 2.11.

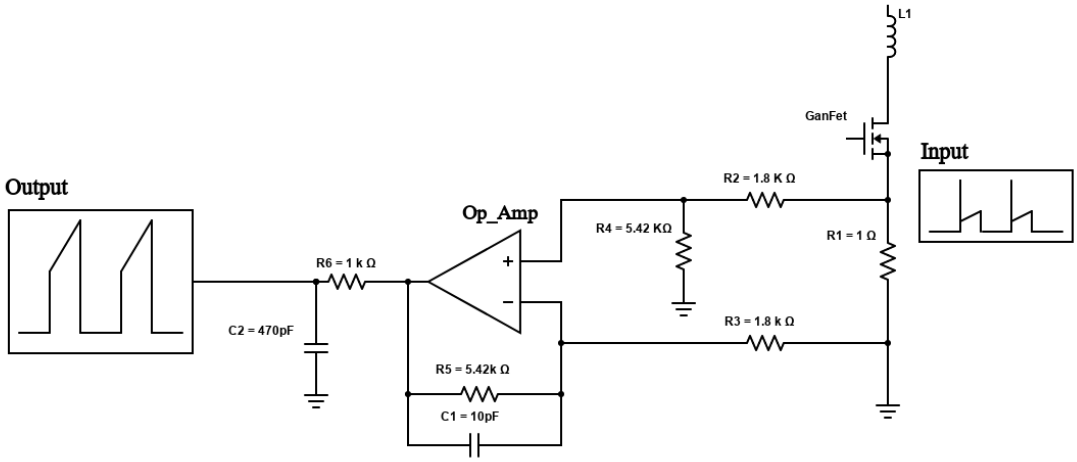

Figure 2.11: Current Feedback Loop

As Section 2.2.1 mentions, a resistor R_1 helps transform current sensing to voltage sensing. The signal is raised after passing the op-amp, and resistors (R_2 - R_5) help adjust the amplifier's closed-loop gain. An RC low pass filter is added in the last stage. In summary, the output signal is amplified by three times, and the leading-edge current spike noises are filtered.

An essential component of the current feedback loop is the operational amplifier. To guarantee the functionality of the current feedback loop, the targets of the op-amp design are:

(1) The gain needs to be higher than 40 dB: The high gain allows our op-amps to detect small fluctuations in their input and maintain the close loop gain of the feedback loop.

(2) The pass band is more than to 500kHz: The switching frequency of the control signal is 500KHz, we need this signal to pass the low pass filter and not be attenuated.

(3) The phase margin is about 45 degrees: This phase margin can maintain the stability of the op-amp.

(4) The supply Voltage (V_{dd}) is 5V: The supply voltage is from the tertiary winding of the transformer.

(5) The reference current is 150uA, and the input voltage is about 0.2V: The input voltage is determined by the previous current sensing stage.

The details of the design of the Op-Amp are demonstrated in Section 2.2.4.

2.2.3 Error Amplifier

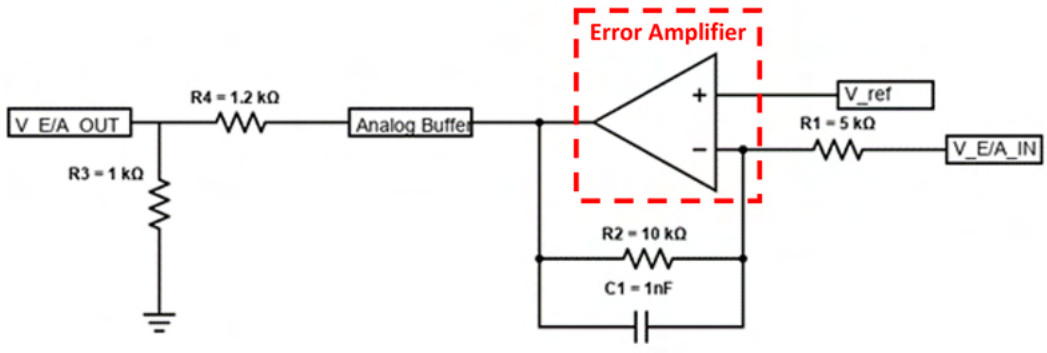

Figure 2.12: Error Amplifier Loop

The error amplifier (E/A) tests and amplifies the difference between the feedback and reference voltage. (Figure 2.12) In this design, the feedback voltage is from the tertiary winding of the

transformer. The output of the error amplifier would be compared with the feedback current signal to adjust the duty cycle of the control signal.

The requirements of the Op-Amp for error amplifier are the same as the current feedback amplifier, EXCEPT that the reference voltage of the E/A is 1.6V, and the reference current is 100uA. The structure of the op-amp for E/A is similar to that of the current feedback loop, so the design process is going to display sparingly. Nevertheless, its closed-loop Bode Plot is presented in Section 2.2.4 to show that those requirements are met.

2.2.4 Operational Amplifier

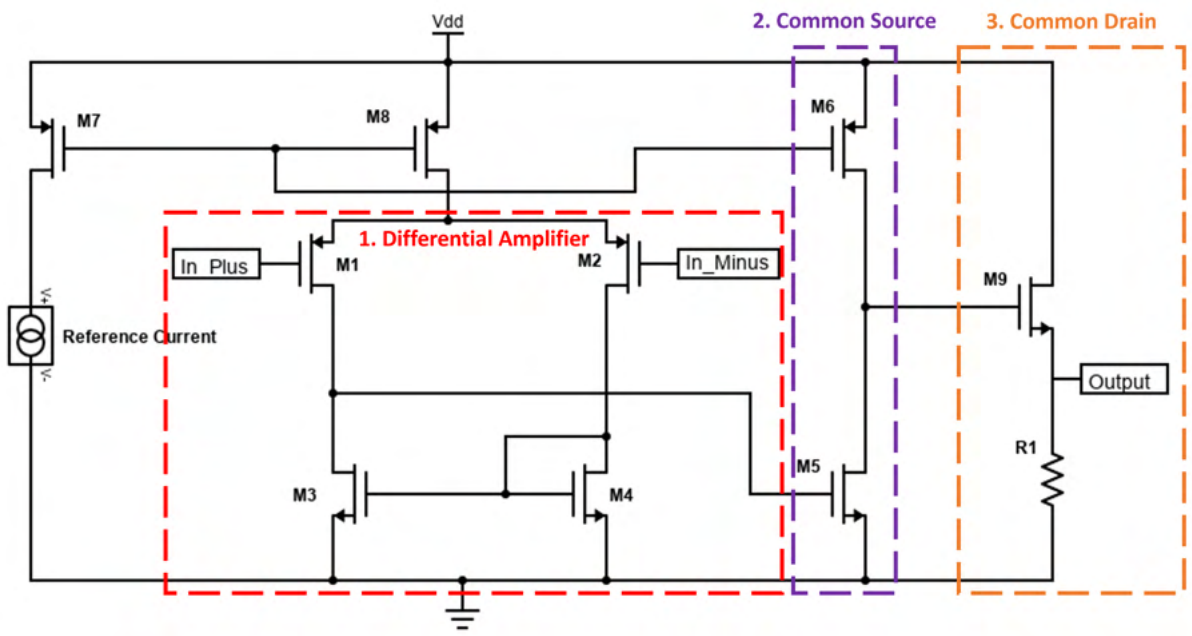

Figure 2.13: Structure of the Operational Amplifier

Figure 2.13 demonstrates the structure of the Op-Amp. It is formed by three stages. The first stage is a differential amplifier. Due to the input voltage amplitude of 0.2V for the current feedback amplifier and 1.2V for E/A being below the threshold voltage for the NMOS differential amplifier type, the PMOS type is being used. The second stage is a common source amplifier to increase the

gain. Finally, the last stage is a common drain amplifier to separate the amplifying stages from the resistive load. The reference current is replicated in each stage with a current mirror.

The design analysis is separated into 1. Amplifying Stage (Differential Amplifier and Common Source Amplifier). 2. Common Drain Stage. Because the amplifying stage is more relative to enhancing the gain, its design is important.

1. DC Analysis

The amplifying function needs all the transistors working in the saturation section. To achieve that, a DC analysis is required. Figure 2.14 presents the final DC Analysis results, and the design details are demonstrated as follows.

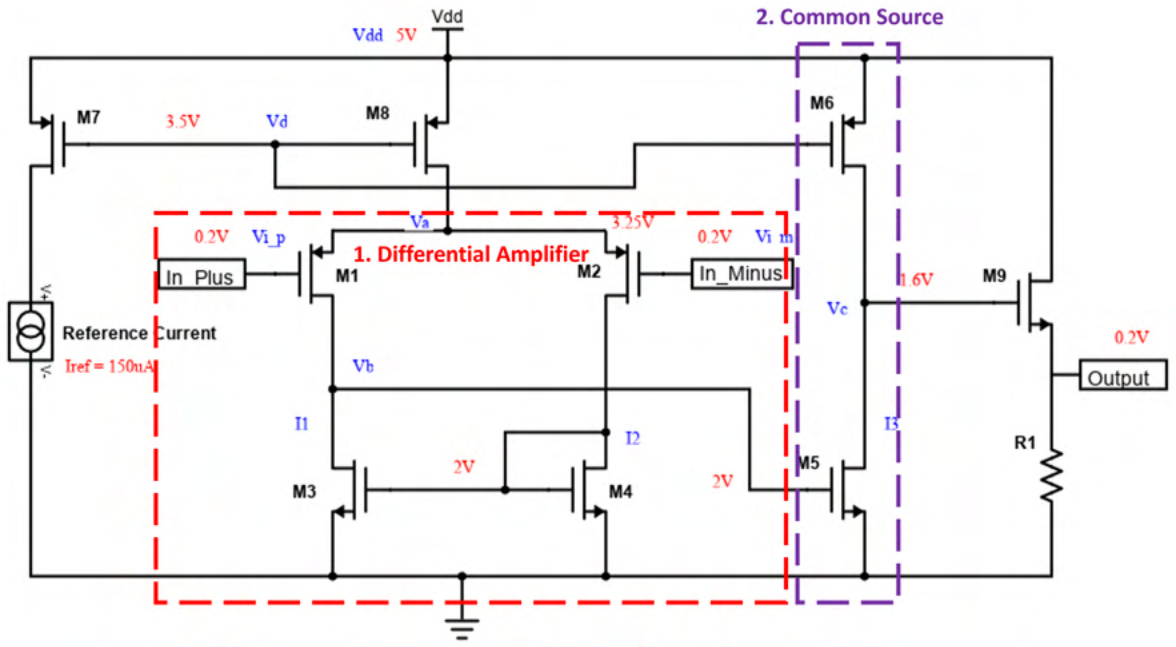

Figure 2.14: The DC Analysis of Op-Amp

The MOSFETs work in the saturation region when inequality 2.7 and 2.8 are satisfied. To get this target, we listed V_{gs}, V_T, and V_{ds} for every MOSFET in amplifying stage and choose appropriate

DC operation points to find the answer for the inequality groups. The list can be found in Section 6.1.

$$|V_{gs}| > |V_T| \tag{2.7}$$

$$|V_{gs} - V_T| < |V_{ds}| \tag{2.8}$$

The drain current for an NMOS is equation 2.9, and that for PMOS is equation 2.10. According to these equations and DC operation points, the ratio of width over length (W/L) can be found. (Table 2.1)

$$I_d = k'_n \times (W/L)_n \times \frac{(V_{gs} - V_T)^2}{2} \tag{2.9}$$

$$I_d = k'_p \times (W/L)_p \times \frac{(V_{gs} - V_T)^2}{2} \tag{2.10}$$

Table 2.1

Devices	W/L
M1, M2	3
M3, M4	1.61
M5	3.22
M6, M7, M8	14

2. AC Analysis

The small signal model of the amplifying stage is presented in Figure 2.15.

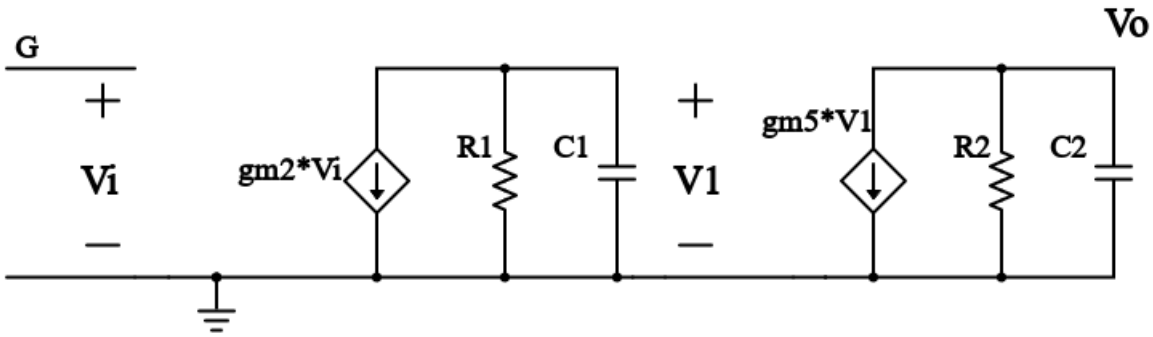

Figure 2.15: The AC Analysis of Amplifying Stage

The resistance of the differential amplifier is the parallel of r_out of M2, M4:

$$R_1 = r_{O2}//r_{O4}$$

The resistance of the common source amplifier is the parallel of r_out of M5, M6:

$$R_2 = r_{O5}//r_{O6}$$

The capacitance of the differential amplifier is the parallel drain-bulk capacitance of M2, M4, and gate capacitance of M5 ($C_{gg5} >> C_{db2}, C_{db4}$):

$$C_1 = C_{db2} + C_{db4} + C_{gg5} \approx C_{gg5}$$

The capacitance of the differential amplifier is the parallel drain-bulk capacitance of M5, M6, and gate capacitance of M9 ($C_{gg9} >> C_{db5}, C_{db6}$):

$$C_2 = C_{db5} + C_{db6} + C_{gg9} \approx C_{gg9}$$

The gain of the amplifying stage is V_o/V_i

$$\frac{V_O}{V_i} = \frac{V_O}{V_1} \times \frac{V_1}{V_i}$$

In the differential amplifier stage:

$$\frac{V_1}{\frac{1}{sC_1}} + \frac{V_1}{R_1} = -gm_2 \times V_i$$

In the common source amplifier stage:

$$\frac{V_O}{\frac{1}{sC_2}} + \frac{V_O}{R_2} = -gm_5 \times V_1$$

The transfer function of the amplifying stage is

$$\frac{V_O}{V_i} = \frac{gm_2 gm_5 R_1 R_2}{(sC_1R_1 + 1)(sC_2R_2 + 1)}$$

The gain of the amplifying stage is

$$A_1 = gm_2 gm_5 R_1 R_2$$

The small signal model of the common drain stage is shown in Figure 2.16

The output voltage of the common drain stage is

$$V_o = gmV_{gs}R_s$$

The input voltage of the common drain stage is

$$V_i = V_o + V_{gs}$$

The gain of the common drain stage is V_o/V_i

$$A_2 = \frac{gmR_s}{gmR_s + 1}$$

The gain of the whole op-amp is

$$A = A_1 \times A_2$$

3. Bode Plot of Current Feedback Amplifier

The Bode Plot of the current feedback amplifier is shown in 2.17. The gain achieves 43.287 dB, and the pass band is 918.4KHz. The phase margin is 44.79 degrees with Miller Compensation (25fF capacitance between the differential amplifier and common source amplifier).

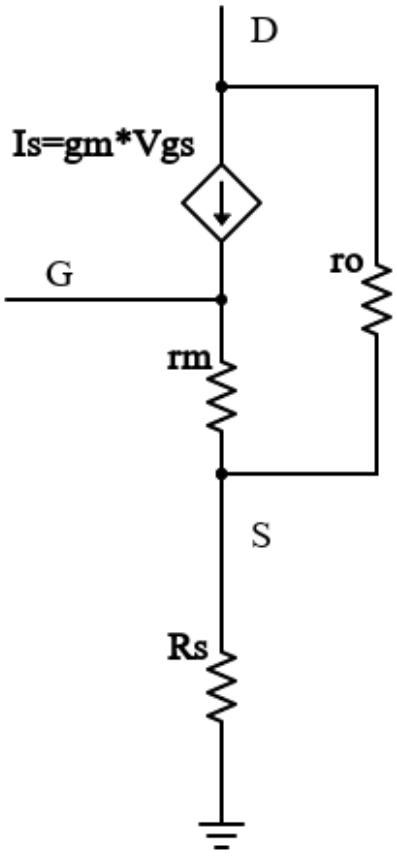

Figure 2.16: The AC Analysis of Common Drain Stage

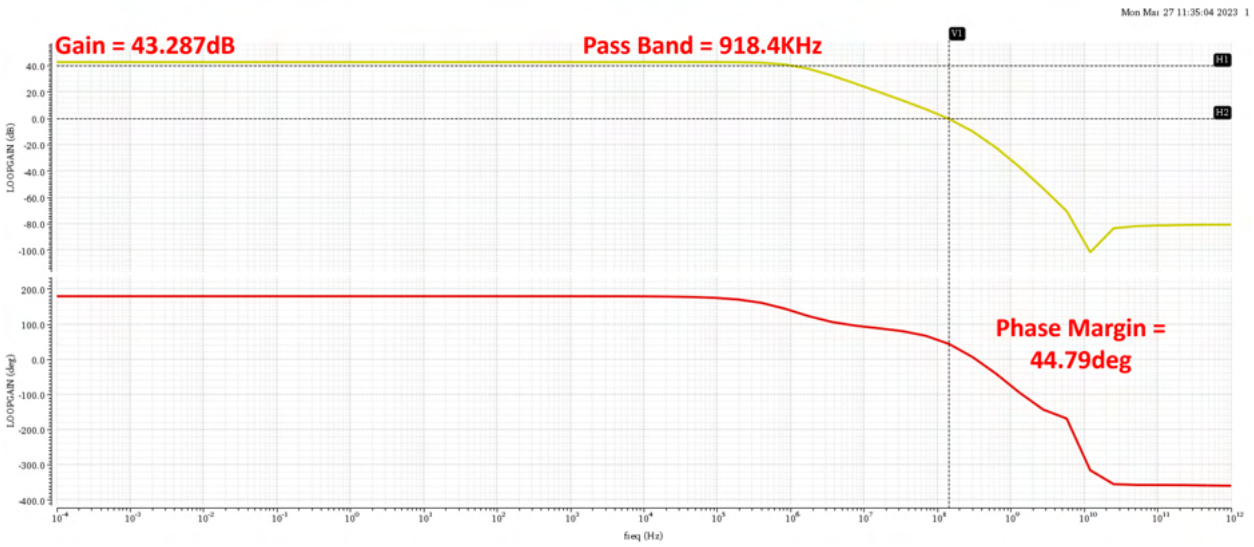

Figure 2.17: Bode Plot of the Current Feedback Amplifier

4. Bode Plot of Error Amplifier

The Bode Plot of the Error Amplifier is shown in 2.18. The gain achieves 46.515 dB, and the pass band is 1.437Hz. The phase margin is 43.565 degrees with Miller Compensation (10fF capacitance between the differential amplifier and common source amplifier).

5. Transient Response of Current Feedback Amplifier

After integrating the current feedback amplifier with other analog IC controller components and testing with the flyback converter model, its transient response is shown in Figure 2.19. The figure shows that the input signal is successfully amplified. The leading-edge spikes are eliminated, as well as other high-frequency noises. The flyback converter system operates stably with this designed current feedback amplifier.

Figure 2.20 presents the output voltage and current of the flyback converter with the analog integrated controller. The output voltage is from 5.05 to 5.128V, and the ripple is 78.37mV.

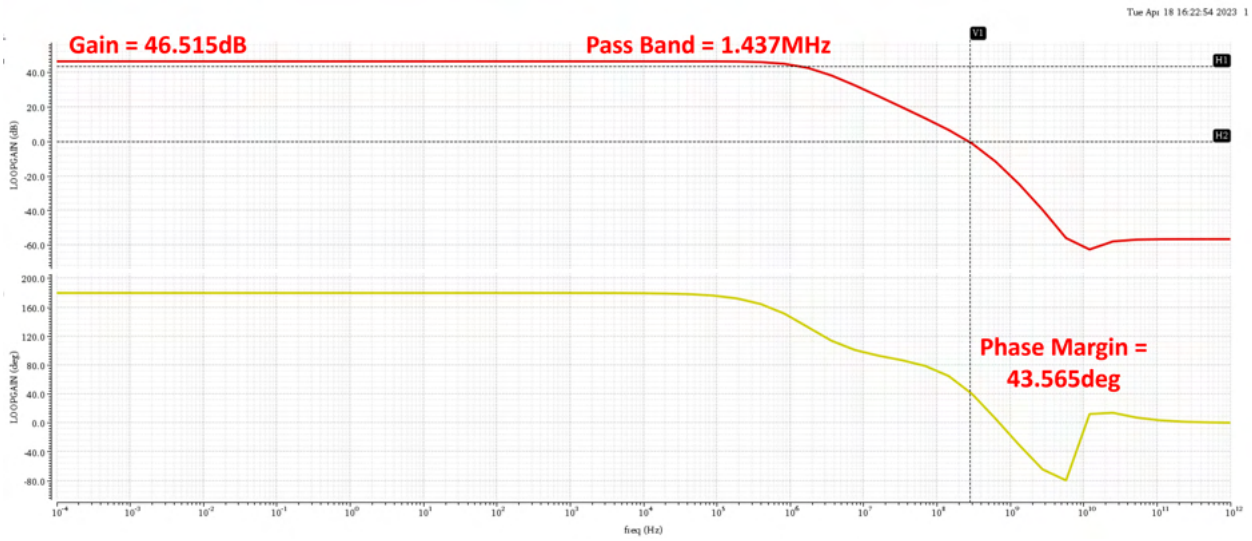

Figure 2.18: Bode Plot of Error Amplifier

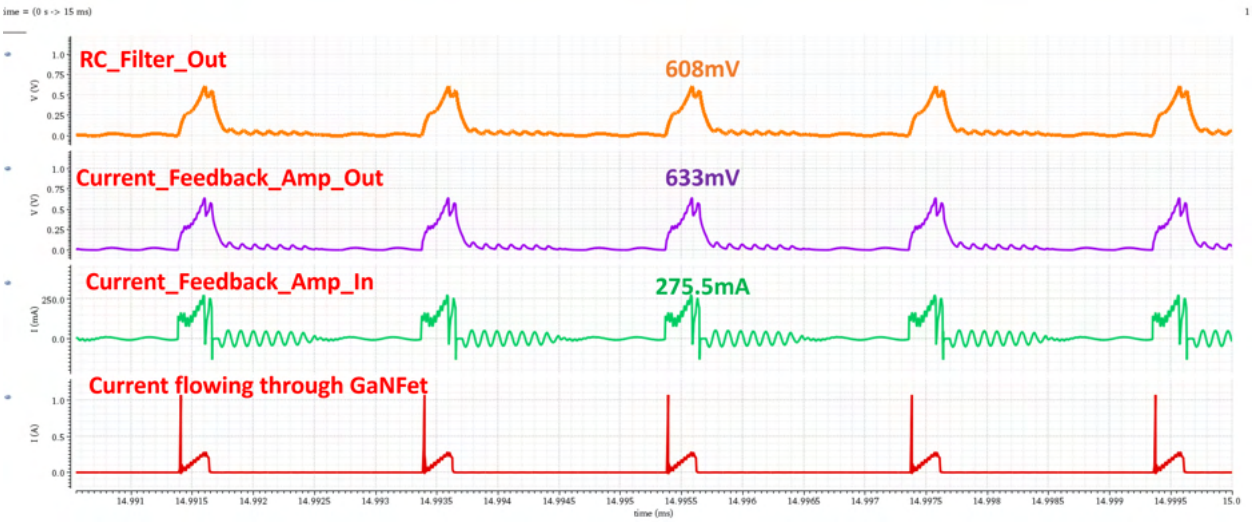

Figure 2.19: The Transient Response of the Current Feedback Amplifier

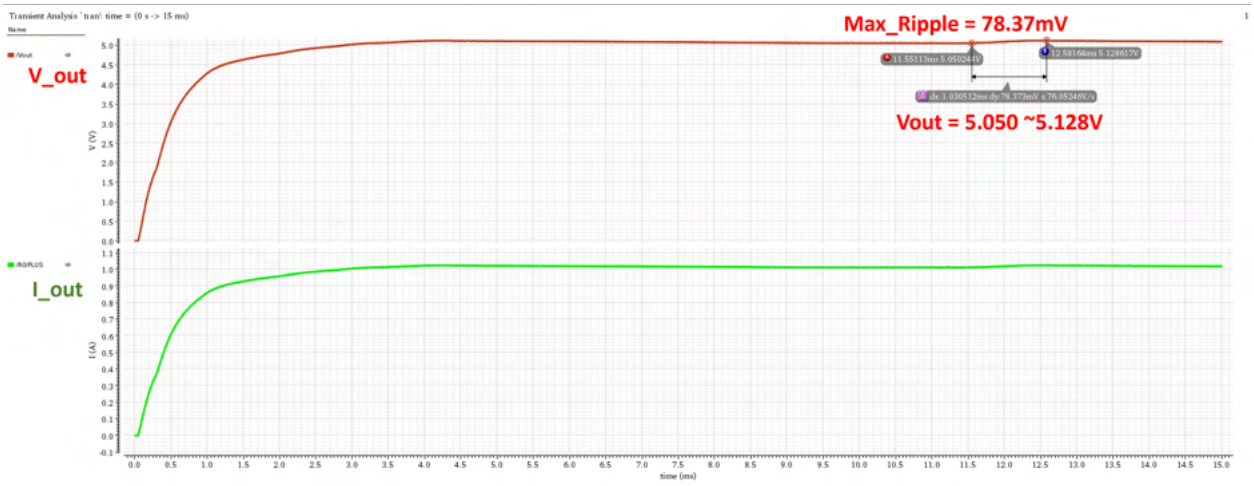

Figure 2.20: The Output Voltage and Current of the Analog Control Flyback Converter

Chapter 3

Active Capacitor

3.1 Active Capacitor at Input Side

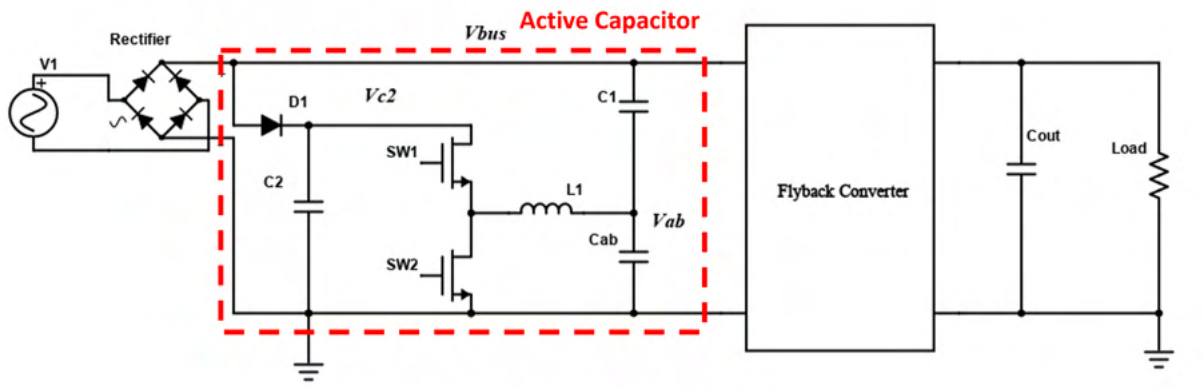

Figure 3.1: The Active Capacitor at Input Side

As introduced in Section 1.4, the input capacitor that connects the rectifier and flyback converter is significant because it determines the ripple of the input voltage of a flyback converter. The larger capacitance means more energy can be stored in the capacitor, so the valley voltage across the capacitor is higher. As shown in Figure 3.2, the larger capacitance means a minor wave but also represents a large size. If the input capacitor is tiny, the valley value of V_{bus} will influence the

performance of the flyback converter and lead to a large ripple at the load terminal. To break up this capacitance-ripple trade-off, an active capacitor is implemented to absorb ripple.

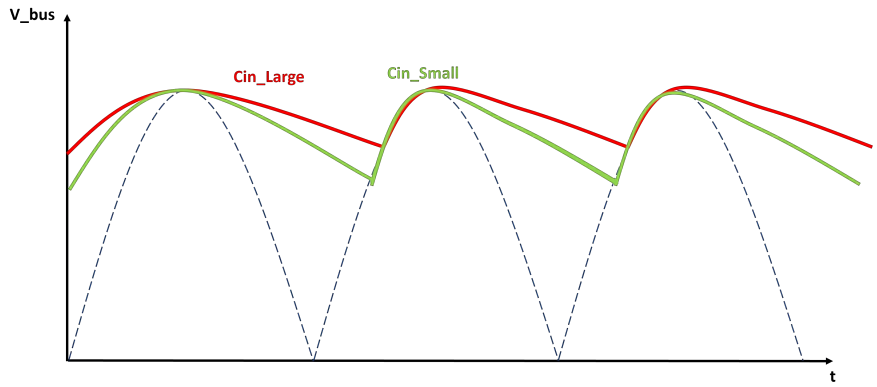

Figure 3.2: The Influence of the Input Capacitor

Figure 3.1 presents the structure of the active capacitor replacing the input capacitor. By controlling the voltage V_{ab}, the ripple of the V_{bus} can be partly canceled out. [39]

The PSIM simulation result is shown in Figure 3.3. The input voltage of the flyback converter is 120Vrms and the output voltage targets 5V. The V_{ab} is regulated by the control circuit to be negatively proportional to voltage V_{C2}, and the waveform of V_{ab} is reversed symmetrically to the voltage V_{C1}. Because $V_{bus} = V_{C1} + V_{ab}$, the output voltage of the active capacitor V_{bus} is flat. The output of the flyback converter with an input active capacitor is 5V with the maximum ripple at 74mV.

Nevertheless, there are a few limitations related to this structure. First, if the converter's load is light, the capacitance of the input capacitor is small. Even though two smaller capacitors replace it, other components (including switches, the diode, and the inductor) are massive because they need to withstand a high voltage. If the capacitance of the original passive capacitor is extremely small, the total volume of the active capacitor could be larger than the passive one. Second, when the input AC voltage source changes, the parameters of this active capacitor have to be renewed, and capacitors (C1 and C2) also need to be replaced. As a result, using it for international power adapters is challenging. Third, the control methodology is complicated. Because the duty cycle

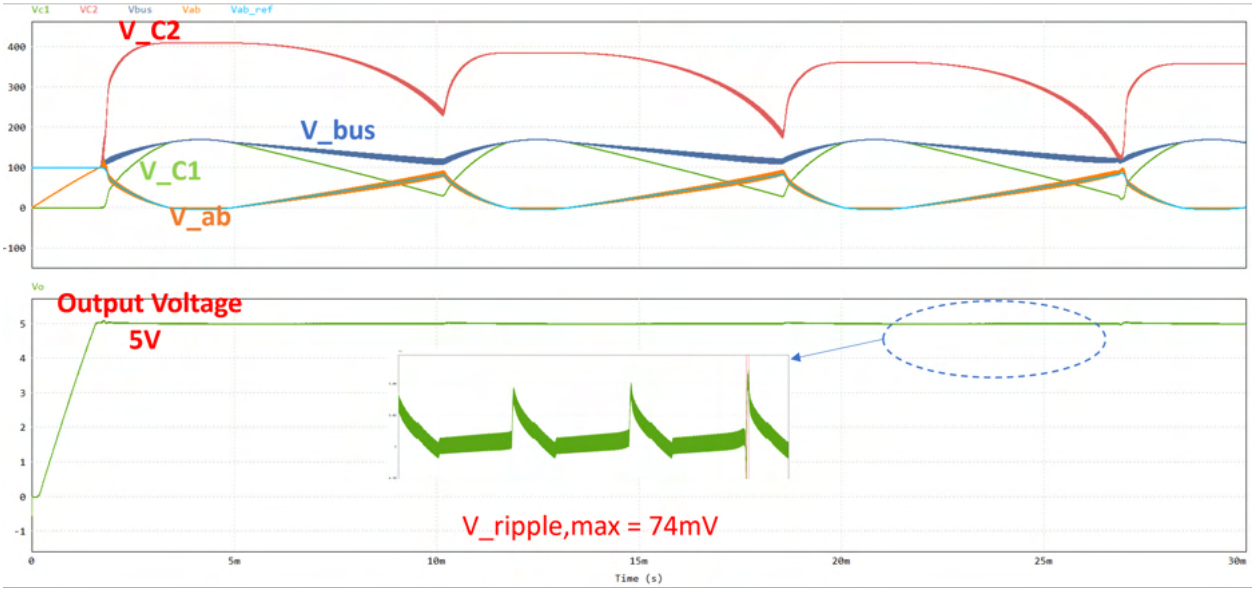

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Figure 3.3: The Simulation Results of Active Capacitor at Input Side

in the control circuit is changed in an extensive range, transferring the duty cycle to square wave signals to control two switches is difficult. To mitigate these problems, an active capacitor replaces the output capacitor instead of the input capacitor.

3.2 Active Capacitor at Output Side

3.2.1 Structure

The structure of the active capacitor replacing the output passive capacitor is shown in Figure 3.4. The active capacitor at the output side is formed with a diode, two Mosfet switches, an inductor, and three capacitors (C1, C2, and Cab). The diode keeps the current flow into the active capacitor and avoids the current flowing back into the flyback converter. The capacitor C2 is the first stage of storing energy from the flyback converter. It is implemented to keep the V_{C2} high. Two transistors and an inductor form a half-bridge converter, which helps control V_{ab} to make it follow V_{ab-ref}.

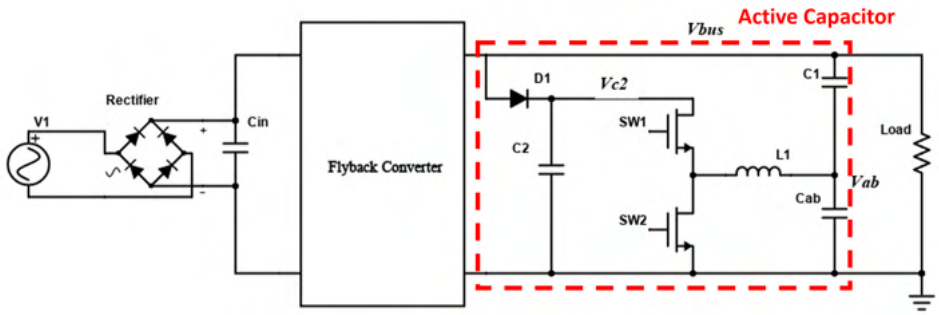

Figure 3.4: The Active Capacitor at Output Side

Finally, two capacitors, C1 and C2, are placed in series to be charged and discharged to keep the output voltage constant.

3.2.2 Control Circuit

For better understanding, the half-bridge structure is simplified as two impedances in a series. (Figure 3.5) [39] The current flows through Z_{C1} and Z_{ab} are the same. It could be represented as equation 3.1.

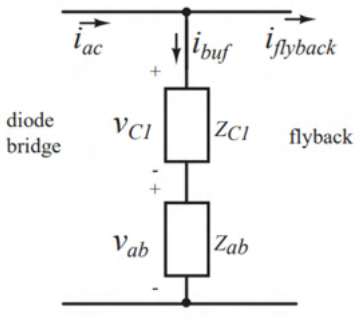

Figure 3.5: The Simplified Structure of the Active Capacitor

$$i_{buf} = \frac{\Delta V_{ab}}{Z_{ab}} = \frac{\Delta V_1}{Z_1} \tag{3.1}$$

The voltage ΔV_{ab} can be controlled with the control circuit, and we set it as equation 3.2.

$$\frac{Z_{ab}}{Z_{C1}} = \frac{\Delta V_{ab}}{\Delta V_1} = -k.(0 < k < 1) \tag{3.2}$$

According to Figure 3.5,

$$Z_{eq} = Z_{ab} + Z_{C1} \tag{3.3}$$

After combining the equation 3.1, 3.2, and 3.3,

$$Z_{eq} = (1 - k) \times Z_{C1} \tag{3.4}$$

Consequently, the capacitance of the active capacitor is (1-k) smaller than the passive one. (Equation 3.5)

$$C_1 = (1 - k) \times C_{eq} \tag{3.5}$$

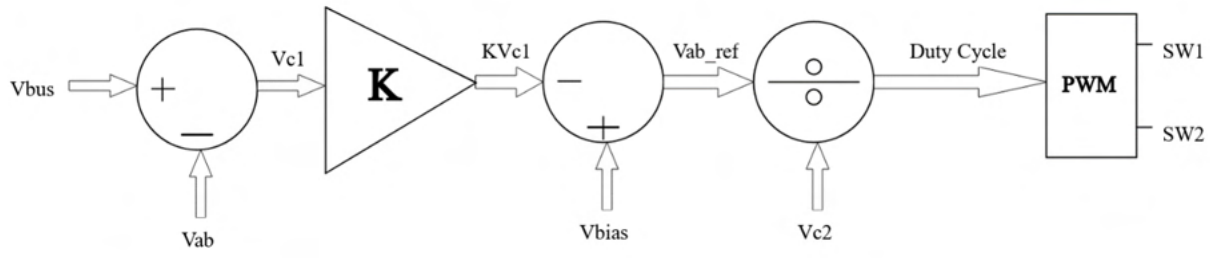

Figure 3.6: The Control Circuit of the Active Capaictor

Figure 3.6 displays the control circuit of the active capacitor. Because the V_{C1} is floating, it is hard to detect its value directly. A subtractor is used for $V_{bus} - V_{ab}$ to obtain V_{C1}. Then the V_{C1} needs to be scaled by a parameter -k ($0 < k < 1$). We hope $-k * V_{C1}$ is the ripple at V_{ab} to offset the ripple at the output side. To keep V_{ab-ref} nonnegative, we need to add a bias voltage V_{bias}. $V_{bias} - k * V_{C1} = V_{ab-ref}$. V_{ab} needs to follow V_{ab-ref}. To do that, V_{ab-ref}/V_{C2} gets the duty cycle. After the PWM control, the duty cycle is transferred to the square wave signals to control switches Q1 and Q2. Then the active capacitor could absorb ripple and keep a constant output voltage.

3.2.3 PSIM simulation result

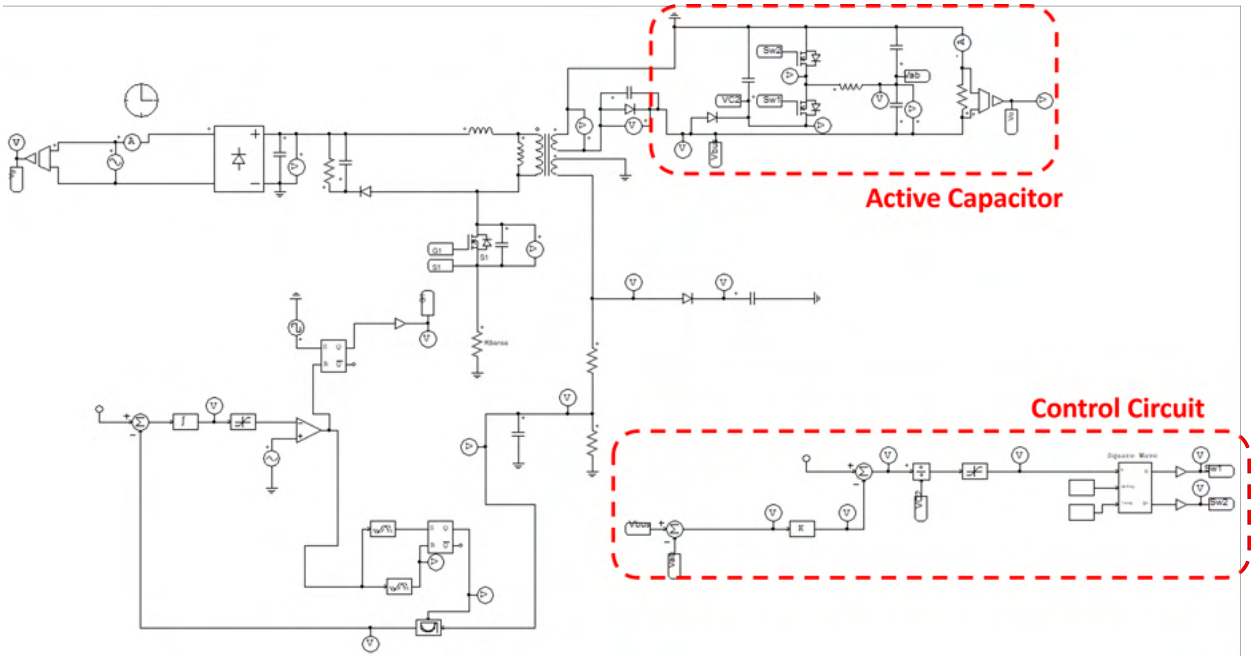

Figure 3.7: The Simulation Testbench of Active Capacitor at Output Side

Figure 3.7 shows the testbench of flyback converter system with the active capacitor at the output side. The flyback converter aims at converting the 120/240V AC input to a 5V/1A output. The original passive output capacitor is 100uF, replaced with the active capacitor whose total capacitance is 67.79uF.

The simulation result of the active capacitor at the output side with 120Vrms 60Hz input voltage is presented in Figure 3.8. The output voltage of the active capacitor is 5V. The ripple of the output is 93.47mV, which means the ripple ratio is 1.8%. When the input voltage is 240Vrms, the simulation result is shown in Figure 3.9. The output voltage of the active capacitor is 5V. The ripple of the output is 77.27mV, which means the ripple ratio is 1.4%. The total capacitance of the active capacitor is 67.8% of the original passive capacitance. The volume is estimated to be reduced to 49% of the original passive capacitor.

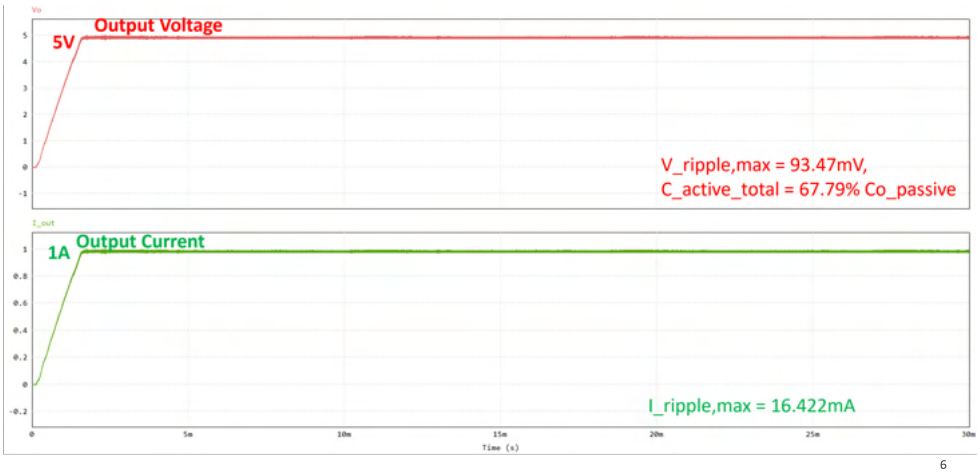

Figure 3.8: The Simulation Result of Active Capacitor at Output Side with 120Vrms Input

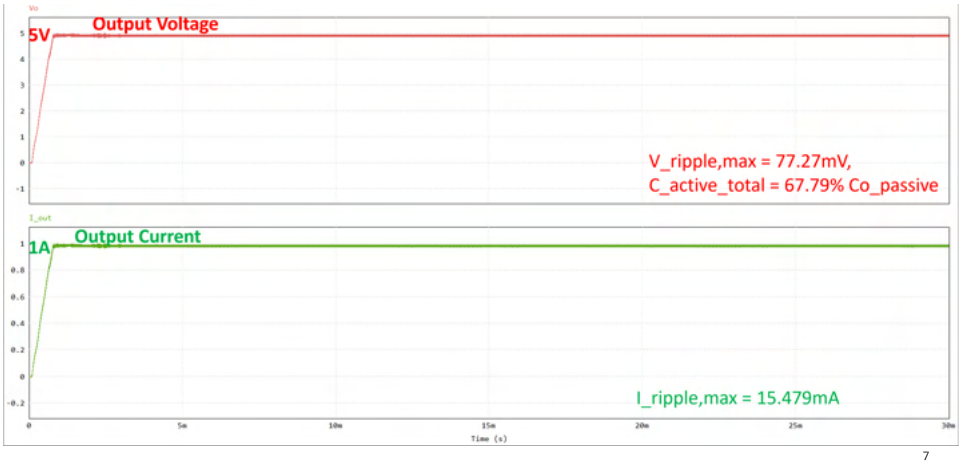

Figure 3.9: The Simulation Result of Active Capacitor at Output Side with 240Vrms Input

3.2.4 Trade-offs

1. Ripple vs. C_{total}

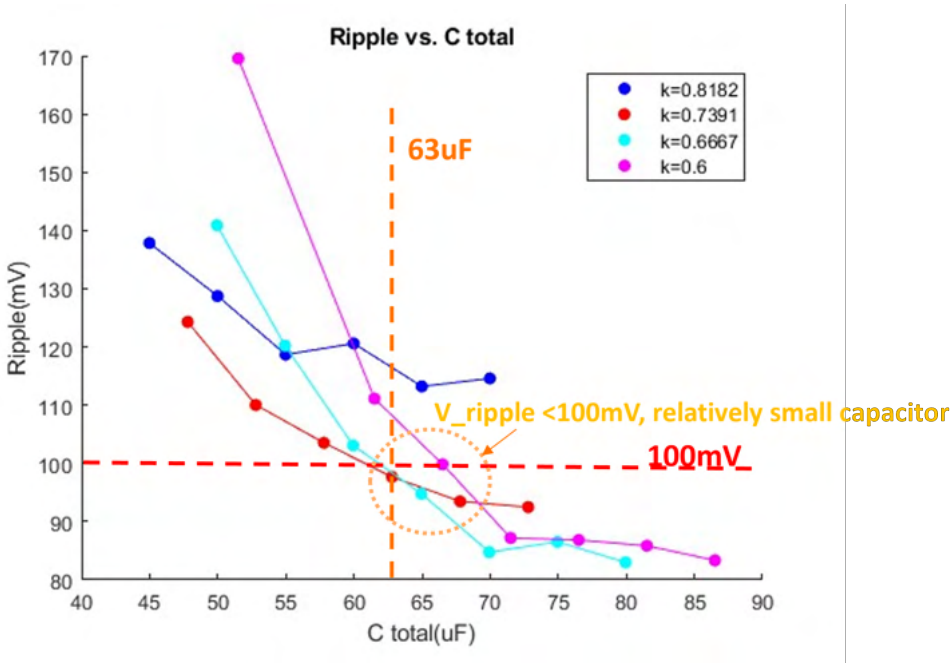

Figure 3.10: The Trade-off Between Ripple and C_{total}

As Equation 3.2 shows, the ripple of the $V_{ab-ref} = -k * V_{C1}$, so the ripple of V_{bus} is $(1-k) * V_{C1}$. If k is close to 1, we can keep the output voltage ripple small. However, V_{ab} is not precisely the same as V_{ab-ref}. How close V_{ab} follows V_{ab-ref} depends on the capacitor Cab. If the Cab is too small, the high-frequency noise cannot be filtered out, and it will influence the wave of the V_{ab}. The larger Cab makes V_{ab} closer to V_{ab-ref} but also makes the size bigger. Consequently, there is a trade-off of the size and ripple, as shown in Fig 3.10. The ripple is decreased with the C_{total} increase. The parameter k will influence the slope of the decline. If the ripple is required to be lower than 100mV, from the simulation results, the total capacitance needs to be more than 63uF. To meet the ripple requirement and shrink the size, the data points in the circle on the plots can be good choices.

2. Size of MOSFET vs. Control Performance

As explained in Section 3.2.2, the variation of V_{ab} (dV_{ab}) is the parameter needed to be controlled.

$$I_{ab} = C_{ab} \times \frac{dV_{ab}}{dt} \tag{3.6}$$

According to the equation 3.6,

$$dV_{ab} = \frac{I_{ab}}{C_{ab}} \times dt \tag{3.7}$$

The current flow through Cab is

$$I_{ab} = I_{C1} + I_L.$$

I_{C1} depends on the design of the converter. It is the current charging the capacitor to store the energy from the secondary side transformer. I_L is the control current. It flows from the energy stored on V_{C2} to achieve

$$V_{ab} = d \times V_{C2} \tag{3.8}$$

d is the duty cycle of the control circuit.

According to this specific flyback converter, the peak output current is 5A. If the I_L is too small, the proportion of the I_L to I_{ab} is too low to control V_{ab}. The current of I_L mainly depends on the size of the transistor. If the width of the transistor is smaller than the minimum current (1.5A in this design), the V_{ab} cannot follow the V_{ab-ref} well. As a result, there is a tradeoff between size and control performance.

3.3 Challenges

1. Balancing the Trade-off Between the Size and Ripple

The size of the active capacitor is related to the C_{ab} and the width of two transistors, and those two metrics greatly determine the control of V_{ab}. If Cab is too small, high-frequency noise will affect

the waveform of the V_{ab}. And if the width of transistors is too tiny, V_{ab} cannot follow the V_{ab-ref} well, and the feedback control is less effective.

2. Power consumption of the active capacitor.

Because the current flow through the active capacitor is large, the power consumed by the transistors, inductors, and two capacitors is significant. The power consumption will lead to a voltage drop at the output side. As a result, power consumption must be considered while implementing the whole AC-DC converter system.

Chapter 4

Voltage-Drop Rectifier

The motivation for exploring voltage-drop rectifiers is to replace the bulky transformer with smaller circuit structures. The main effect of the transformer of a flyback converter is stepping down the high-level input voltage to a low-level output voltage. As a result, a capacitive voltage divider structure is applied with a rectifier to form the capacitive divider rectifier. However, the size of two high-voltage capacitors is enormous. Instead of dividing voltage by two capacitors, we split it with a capacitor and the rectifier. This structure is known as the capacitor-fed rectifier. To explain the operation of these two voltage-drop rectifiers, the example of converting a 120Vrms input voltage to 30V DC voltage is presented for both. The simulation results are also shown in this chapter.

4.1 Capacitive Divider Rectifier

The schematic view of the capacitive divider is shown in Figure 4.1. The capacitive divider rectifier is formed with a protective resistor R_{in}, two AC capacitors C_{ac1}, C_{ac2}, and a rectifier. V_R is the voltage across R_{in}, V_{C1} and V_{C2} are the voltage across the C_{ac1}, C_{ac2}, V_{in}' is the output voltage of the capacitive divider rectifier and the input voltage of the DC-DC Converter. V_{o-max} is the maximum voltage of V_{C2}.

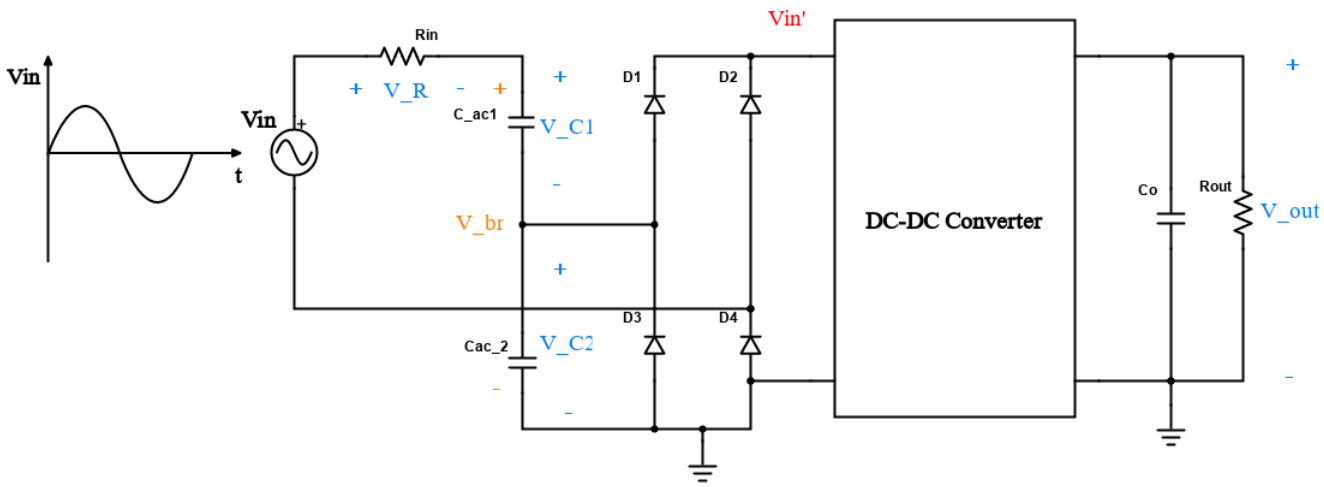

Figure 4.1: Capacitive Divider Schematic View

In most cases, the forward voltage drop of the diode is 0.7V; to leave enough margin, we assume that the forward voltage drop is 2V. The V_{o-max} is

$$V_{o-max} = V'_{in} + 2; \tag{4.1}$$

$$V_{br} = V_{o-max} + V_{C1}; \tag{4.2}$$

Combine capacitors C_{ac1}, C_{ac2} as an integral part and symbol it as X.

$$X = \frac{1}{\omega C} \tag{4.3}$$

$$C = C1 + C2 \tag{4.4}$$

The resistance of X is ([41])

$$|X| = \frac{2R_{DC-Conv}}{\pi} * \frac{V_{o-max} - V_{in'} - V_D}{V'_{in}} \tag{4.5}$$

$R_{DC-Conv}$ presents the equivalent input resistance of the DC-DC Converter.

Because current flows through the R_{in} C_{ac1} and C_{ac2} is almost the same,

$$C1 = \frac{V_{o-max}}{V_{br}} C \tag{4.6}$$

The value of the protective resistor can be obtained from the equation (4.7)

$$\frac{R_{in}}{X1 + X2} = \frac{\sqrt{2}V_{in} - V_{br}}{V_{br}} \tag{4.7}$$

From these equations, the value of each component can be obtained from the calculation.

The capacitive divider rectifier's input voltage and current waveform are shown in Figure 4.2.

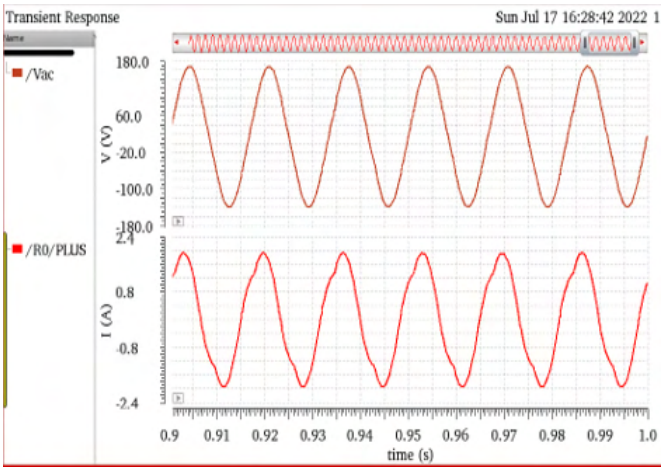

Figure 4.2: Capacitive Divider Rectifier V_{in} I_{in}

Figure 4.3 demonstrates the example of the output voltage targeting at 30V. The output current of the capacitive divider rectifier is 904.993mA. The voltage ripple is 433.6mV, and the current ripple is 14.8mA.

Even though the capacitive divider rectifier successfully drops the voltage down, its size is bulky due to the two high-voltage AC capacitors. To further shrink the size, the next investigation is focused on the capacitor-fed rectifier.

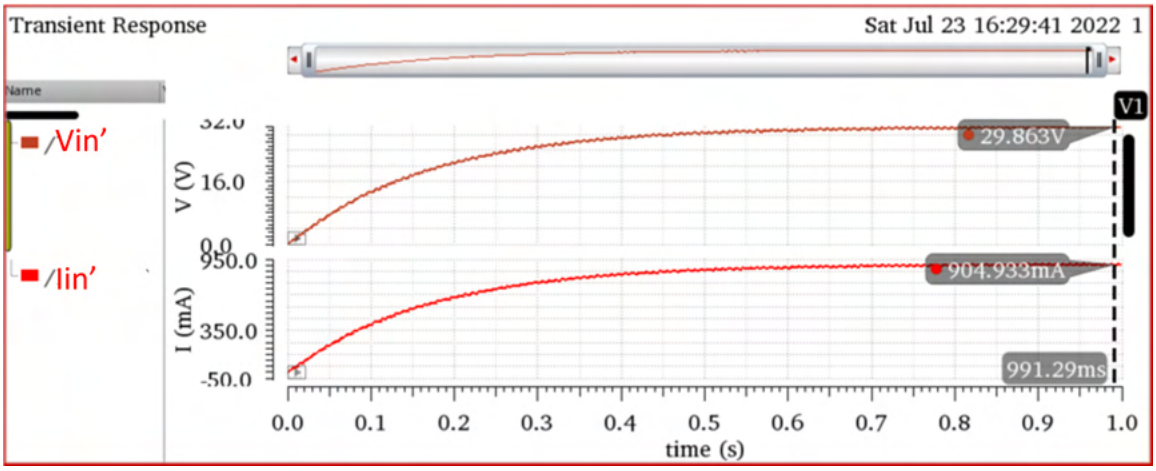

Figure 4.3: Capacitive Divider Rectifier's Output Voltage and Current

4.2 Capacitor-Fed Rectifier

4.2.1 Analysis of Capacitor-Fed Rectifier

The Schematic View of the Capacitor-Fed Rectifier is shown in Figure 4.4. It is constructed by a protective resistor R_{in}, an AC capacitor C_{ac}, and a rectifier$D_1 - D_4$. V_R is the voltage across R_{in}, V_C is the voltage across the C_{ac}, V'_{in} is the output capacitor-fed rectifier and the input voltage of the DC-DC Converter.

Capacitive voltage divider rectifier divides input voltage with two AC capacitors as introduced in Section 4.1. However, two high-voltage capacitors have a large volume. Instead of using two capacitors, the capacitor-fed rectifier divides voltage with one capacitor and the rectifier. As shown in Figure 4.5,V_{in} is the 120Vrms input voltage, V_{Cac} is the voltage across the AC capacitor and its protective resistor, and V_{rect} is the voltage across the rectifier. From this analysis, we can obtain that

$$V_{in} = V_{Cac} + V_{rect} \tag{4.8}$$

The positive half of the V_{rect} is V_{br} shown in Figure 4.6. We can observe that the peak voltage

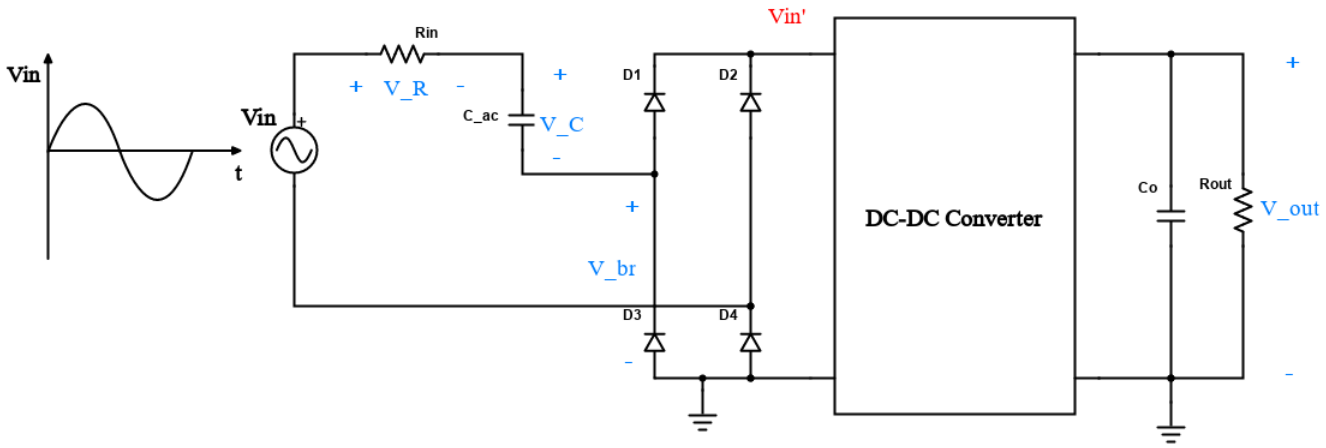

Figure 4.4: Capacitor-Fed Rectifier Schematic View

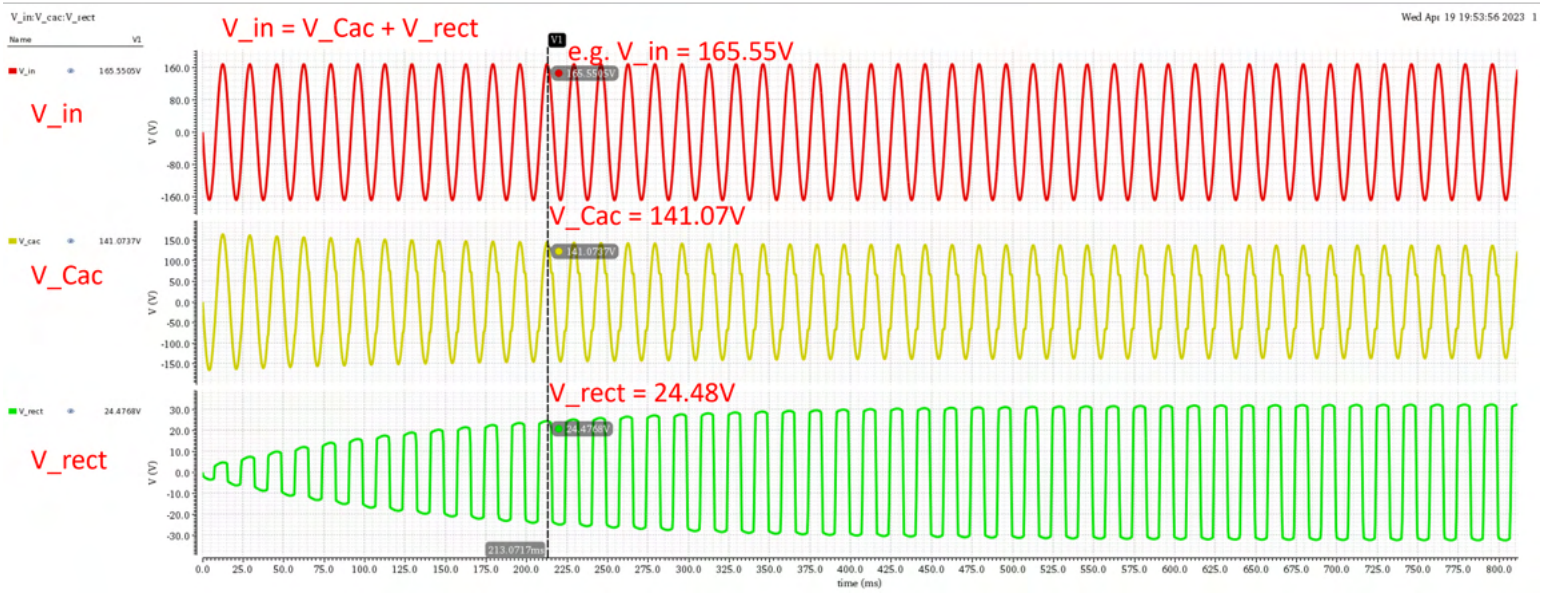

Figure 4.5: Capacitor-Fed V_{in}, V_{Cac}, and V_{rect}

of V_{br} when it becomes stable is the targeting voltage of V'_{in} (around 30V) plus the forward bias voltage of diodes in the rectifier V_D.

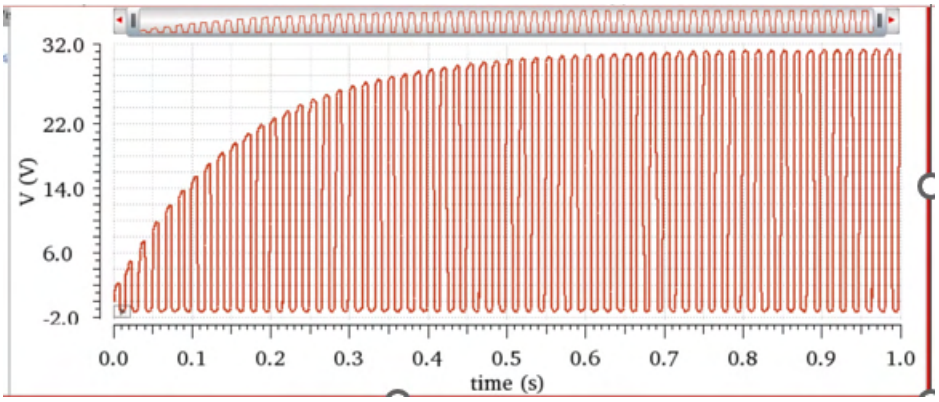

Figure 4.6: Capacitor-Fed V_{br}

The input capacitor in the DC-DC converter helps maintain the amplitude of voltage V'_{in} and current I'_{in} and filter noises. The voltage ripple is 325mV, and the current ripple is 10mA. The rising wave of the ripple is caused by discharging C_{ac} and energy is transferred to the input capacitor of the DC-DC converter. The falling wave of the ripple is due to the energy consumption of the DC-DC converter and the load.

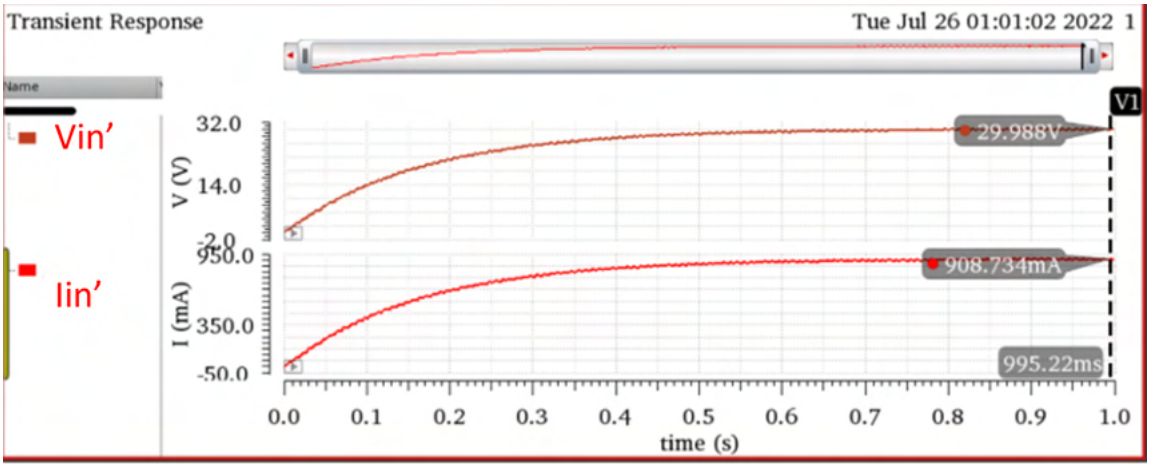

Figure 4.7: Capacitor-Fed V_{out} I_{out}

4.2.2 Replacing High Voltage AC Capacitor

In the capacitor-fed rectifier, the component with the largest volume is the AC capacitor. That is because the AC capacitor is always charged and discharged because of the oscillation of the AC input. Besides holding the high voltage, the AC capacitor also requires dissipating the heat caused by the current flowing. The AC capacitor should be large for better heat dissipation and voltage isolation. [51]. For example, the size of a 60uF film capacitor withstood 240V AC voltage is 366.999 cm^3. (SFC24T60K391B-F).

In contrast, the size of the high-voltage DC capacitor is tinier. For instance, the size of a 60uF 400V_{DC} Aluminum Electrolytic Capacitor (THAS600M400AA0C) is 8.598cm^3, 2.34% of the high voltage AC capacitor of the same capacitance.

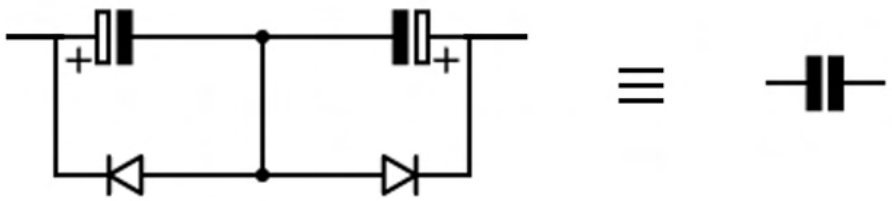

Figure 4.8: Replace AC Capacitor with DC Capacitors

Based on this characteristic, the high-voltage AC capacitor must be replaced with DC capacitors. The replacement structure is shown in Figure 4.8. The negative poles of these two DC capacitors are connected, and their positive poles are connected to the AC input. Two diodes are added to prevent the reverse current. The AC capacitor, for example, can be replaced with two 120uF DC capacitors and two diodes. The list of them is in the following Table. The total volume is 16.02cm^3, which is 4.36% of the AC capacitor.

Device	Type	Capacitance	Voltage	Volume
DC Capacitors	LDQ2G121MERYGA	120uF	400V_{DC}	16cm^3*2
HV Diodes	S1G		400V_{DC}	0.02cm^3*2

4.2.3 Reduce the Number of High-Voltage Components

A capacitor-fed rectifier can decrease the voltage and regulate it to a fluctuating DC signal. In the secondary DC-DC stage, the components' size will be considerably more minor than the high-voltage ones because thick isolation materials and large conductive are not in demand. For instance, as mentioned in the above subsection, a 60uF 400V_{DC} Aluminum Electrolytic Capacitor (SFC24T60K391B-F) is 8.598cm^3. For a 100uF 35V capacitor, however, the volume is 0.165cm^3. As a result, fewer HV components included help with size reduction.

4.2.4 Capacitor-Fed Rectifier vs. Transformer

The volume of a 115V - 30V transformer is 79.238 cm^3. (XFRMR LAMINATED 4.5VA CHAS MOUNT). As shown in the table, the total passive volume of a capacitor-fed rectifier is 32.04 cm^3, which is about 40% of the transformer.

However, the capacitor-fed rectifier cannot isolate the low-voltage output side from the high-voltage input side. This brings risks to the security of customers. In [9], a customized transformer is implemented, which can maintain the advantage of a transformer for isolation and shrink the size.

Chapter 5

Conclusion

The AC-DC converters transfer high-voltage AC sources to the low-voltage DC output to supply power for electronic devices. The small-sized AC-DC converters are popular among customers because they are portable, compatible, and space-saving. The priority of this research is the size reduction. In addition, another essential target is suppressing ripple, which will influence the performance of the output load. A 120/240 Vrms input, 5V/1A output flyback converter module is utilized for this size reduction exploration.

From the previous state-of-the-art designs explored in Chapter 1, many converters with IC Implementations can significantly reduce their size. Additionally, the active capacitors replace the colossal passive capacitors with several smaller components to occupy less space. At last, a design of voltage-drop rectifiers is potentially able to replace the giant transformer.

In Chapter 2 (IC Implementations), the strategy is integrating tiny components as many as possible into the chips. Both digital and analog integrated controllers are investigated. After implementing IC controllers, about 10.69% of the size is estimated to be reduced, as shown in Figure 5.1. The digital controller can suppress the ripple to 99.32mV. For the analog controller, the ripple is 78.37 mV.

The active capacitor is introduced in Chapter 3 (Active Capacitor). The 100uF output capacitor of

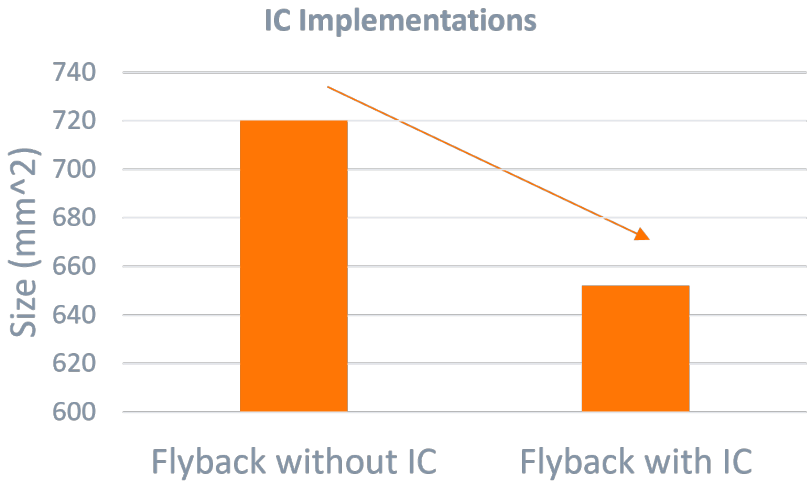

Figure 5.1: Size Reduction of IC Implementations

the flyback converter is replaced with a 67.79uF active capacitor. Figure 5.2 shows that the size of the output capacitor is expected to be reduced from 22.4cm^3 to 10.264cm^3. The ripple of the output voltage is 90mV. The total volume of the active capacitor is 45.8% of the original passive capacitor.

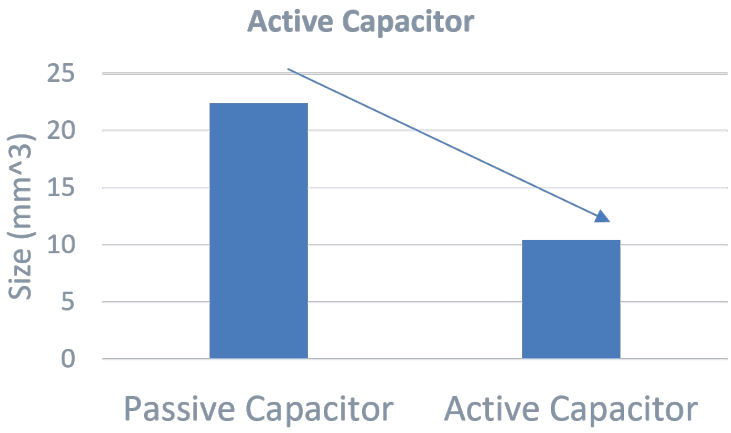

Figure 5.2: Size Reduction of Active Capacitor

Chapter 4 (Voltage-Drop Rectifier) demonstrates two kinds of rectifiers: capacitive divider and capacitor-fed rectifier. The capacitor-fed rectifier successfully steps the 120Vrms input voltage

down to a 30V DC voltage for the next stage DC-DC converter. The size of the capacitance is 32cm^3, and an 79.2cm^3 transformer can be replaced. (Figure 5.3) In other words, 60% volume of the bulky transformer can be decreased.

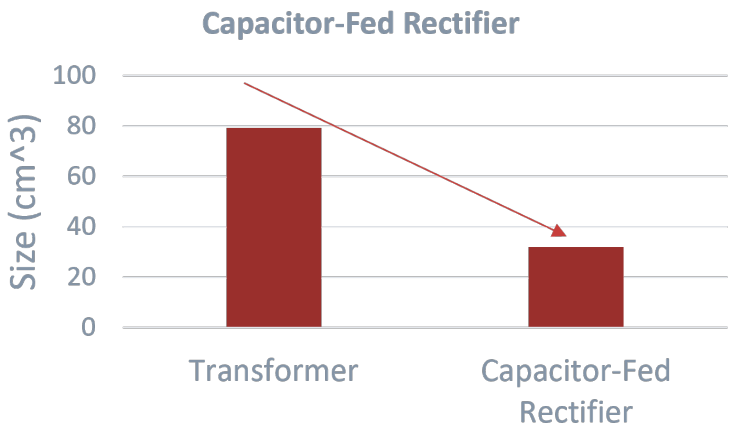

Figure 5.3: Size Reduction of Capacitor-Fed Rectifier

Chapter 6

Appendix

6.1 Op-Amp: DC Operation Points

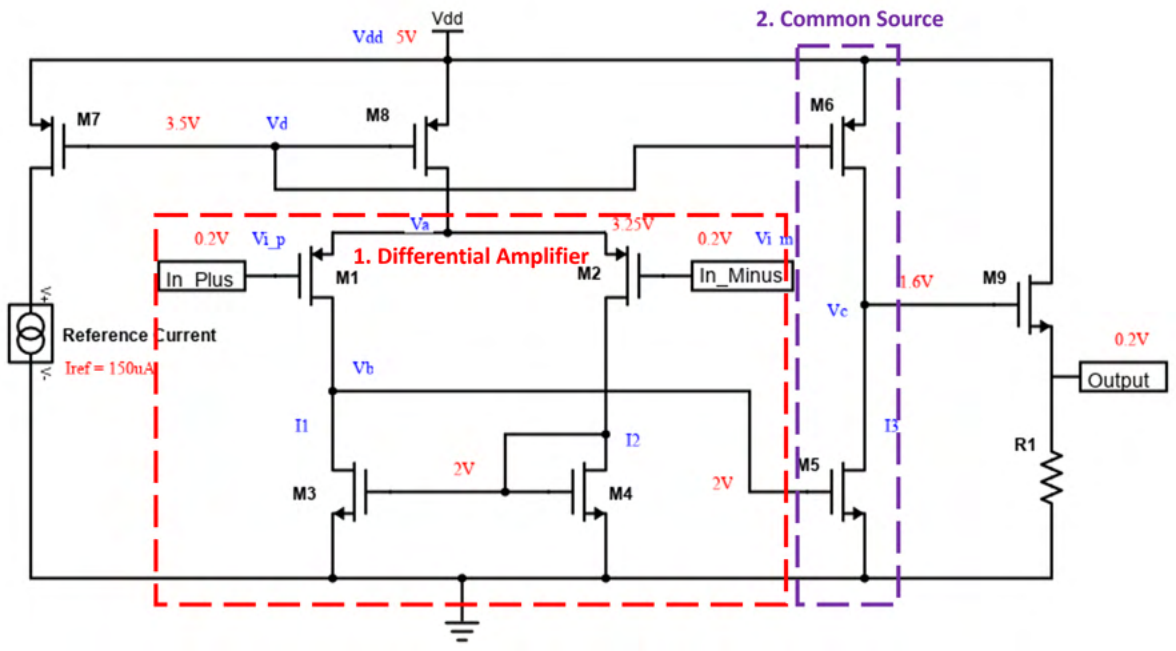

Figure 6.1: The DC Analysis of Op-Amp

(a) M1, M2

$V_{gs} = V_i - V_a$

$V_T = V_{T0} + \gamma_p(\sqrt{|-2\Phi_F + V_{SB}|} - \sqrt{|-2\Phi_F|})$

$V_{sb} = V_a - V_{DD}$, $\Phi_F = -0.3$

$V_{ds} = V_b - V_a$

(b) M3, M4

$V_{gs} = V_b$

$V_T = V_{T0}$

$V_{ds} = V_b$

(c) M5

$V_{gs} = V_b$

$V_{ds} = V_c$

$V_T = V_{TN0}$

(d) M6

$V_{gs} = V_d - V_{DD}$

$V_{ds} = V_c - V_{DD}$

$V_T = V_{TP0}$

(e) M7, M8

$V_{gs} = V_d - V_{DD}$

$V_{ds} = V_a - V_{DD}$

$V_T = V_{TP0}$

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