Development of Single-ended and Balun Integrated Probes for THz Applications

A Dissertation

Presented to

The faculty of the School of Engineering and Applied Science

University of Virginia

In Partial Fulfillment

Of the requirements for the degree of

Doctor of Philosophy of Electrical Engineering

By

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August 2014

To my families,

who have always supported and encouraged me.

Abstract

A number of new devices and components are being developed in the terahertz spectrum for applications such as radio astronomy, medical and surveillance imaging. However, these development efforts are hampered by difficulties in the characterization processes. Typically, terahertz modules fabricated on semiconductor material need to be diced into individual chips, and assembled to a precision micromachined block for test. This time-consuming and arduous characterization process adds to the complexity and cost. The on-wafer probe solves these problems by providing a tool to characterize the terahertz DUT on-wafer, in large volumes and with higher precision.

In this dissertation, a new fabrication technology is first developed to fabricate a single-ended probe with GSG probe tips. The improved fabrication processes have been used to realize on-wafer probes up to 1.1 THz, which is the first reported THz probe in the community. Further tests on these probes demonstrate that they can maintain electrical repeatability over long term usage.

In the second part of this work, a prototype balun integrated probe at W-band is developed to enable on-wafer characterization for differential circuits. Detailed design considerations, as well as test results, are shown in this work. Just as with the GSG probes, the GSGSG design has the potential to be scaled to higher frequencies. The balun integrated probe can be used to provide a convenient way to characterize the emerging differential MMIC devices with better accuracy and lower cost.

Acknowledgements

First of all, I'd like to extend my heartfelt gratitude to my advisor Arthur Lichtenberger, whose long term support and encouragement has been an essential part of my PhD experience. He encouraged freedom in the pursuit of academic researches, and provided a lot of valuable insights and help along the way, without which the successful completion of my PhD degree is impossible. His philosophy of mentoring young graduate students will continue to inspire me after I graduate.

I would also like to extend my same appreciation to Prof. Robert Weikle and Prof. Scott Barker for their continual support and guidance. Through regular research meetings, they both have advised me a lot in terms of doing researches, and helped me accomplish much in every way.

Additionally, I'd like to thank other fellow graduate students in our research group, including former students Theodore Reck, Lihan Chen, Alex Arsenovic, Michael Cyberey, and current students Matthew Bauwens, who have always been ready to offer assistance when there is a need. Other fellow students and co-workers, including Jianzhong Zhang, Jie Wang, Greg Stronko and Qiang Yu, have also been very helpful everytime I ask. My thanks also go to Alex Lobo and Joe Beatrice for their hard work in keeping the cleanroom running.

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Chapter 1

Introduction

1.1 Terahertz Technology and Applications

Terahertz radiation, also called submillimeter radiation, refers to microwave radiation with frequencies ranging from 300 GHz to 3 THz, or wavelengths in air from 0.1mm to 1mm. It has been an area of focused scientific research for the past few decades and has found many important applications in areas such as radio astronomy, terahertz spectroscopy, imaging and telecommunication. For example, NASA launched the Submillimeter Wave Astronomy Satellite (SWAS), using UVa mixer diodes, in December 1998 to detect the interstellar clouds and research the way these clouds collapse to form stars and planets, which could reveal insights into star formation[20]. Terahertz spectroscopy is also a powerful tool for biological researchers to study the vibrational modes of many biological and chemical molecules, such as the twisting and deformation of the double helix structure of the DNA[21]. Because of the non-ionizing properties of the terahertz radiation, as well its sensitivity to water concentration and transmissivity through dry fabric materials, terahertz imaging technology has been developed for skin cancer imaging[22] and non-destructive imaging of concealed explosives, weapons and drugs[23, 24]. In addition to all these applications, the electronics industry's quest for faster and more powerful computers and wireless communication has been constantly driving up the clock frequencies, making terahertz frequency a potential answer to keep up with the Moore's Law[25].

Despite all these promising applications for terahertz technology, devices and components in this frequency range are still rare and difficult to make. Until recently, available systems in this frequency range were still based on either waveguides or quasi-optics. It is thus highly desirable to develop integrated circuits in this frequency region to reduce the size, weight, and eventually cost of terahertz components. Recent years have seen siginificant advancement of Submillimeter-wave and Millimeter-wave Monolithic Integrated Circuits (S-MMIC and MMIC), using InP based High Electron Mobility Transistors (HEMTs) and Heterojunction Bipolar Transistors (HBTs)[26, 27, 28, 29, 30, 31, 32].

The development of differential S-MMIC and MMIC devices is of special interest to industry because of differential circuits' excellent noise immunity and the elimination of ground plane parasitics. For amplifiers especially, the differential configuration could improve linearity and allow for a double voltage swing under a given voltage supply, which is highly desired for high indensity integrated circuits. There has been a lot of interest in differential amplifiers below 100 GHz, using various technologies such as Si CMOS, SiGe, and InP HBT[33, 34, 35]. More importantly, there has also been reports of differential amplifiers working above 100 GHz in the past few years[36, 37], shedding light on the future of differential S-MMIC and MMIC.

1.2 On-wafer Characterization

Calibrated on-wafer measurement which is widely adopted in the industry at lower frequencies (< 300 GHz), can be used to characterize integrated circuits without the use of waveguide test fixtures. At frequencies where on-wafer probing is not available, device characterization becomes considerably more difficult. Individual chips must be diced out and placed into waveguide blocks for measurement. Such post processing fixturing is time consuming and costly. Additionally, it usually does not allow the setting reference planes close to the device-under-test (DUT) for more precise device

characterization. Thus, on-wafer probes are highly desirable in the terahertz industry to provide means for on-wafer characterization at these frequencies. They significantly reduce the testing time and cost. Additionally, by setting the reference planes right next to the DUT, more accurate device measurements can be achieved, enabling measurement-based device models.

There are previously two primary vendors that offer on-wafer probing solutions up to 500 GHz - GGB Industries and Cascade Microtech, with the new addition of Dominion MicroProbes, whose products are based on a new type of on-wafer probes described in this dissertation. The development of on-wafer probes at the University of Virginia started with a prototype probe at the WR-10 waveguide band (75 to 110 GHz)[38, 19], which has since been scaled to even higher frequencies[3, 39]. Shown in Fig 1.1 is a comparison of on-wafer probes from the GGB Industries, Cascade Microtech and the University of Virginia.

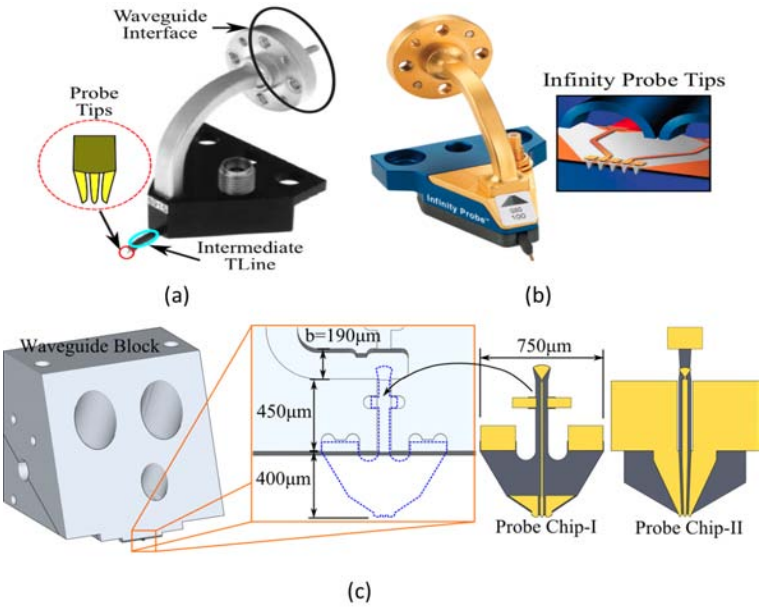

Figure 1.1: On-wafer probes available from (a) GGB Industries Model 120 Picoprobe[1], (b) Cascade-MicroTech Waveguide Infinity Probe[2], (c) University of Virginia micromachined on-wafer probe at WR1.5 waveguide band[3].

For differential MMIC and S-MMIC design and characterization, the ability to perform on-wafer probing is also very important. There are a few ways to achieve this

goal in the lower frequency realm (typically below 67 GHz), as will be discussed below. Other than being either very expensive or potentially less accurate, these methods are very difficult to be extended to higher frequencies. A high frequency balun probe, where the balun circuitry is integrated onto the probe itself, is thus highly desirable to facilitate on-wafer differential circuits characterization at terahertz frequency range.

1.3 Organization of The Dissertation

Chapter 2 of the dissertation starts with an introduction to the capabilities as well as the limitations of the semiconductor processing tools at the University of Virginia Microfabrication Lab (UVML). The development of new fabrication techniques are described for on-wafer probe fabrication on $15\mu m$ thick Silicon-on-Insulator (SOI) wafers. Two fabrication process flows are developed with detailed analysis comparing the pros and cons of the two. Improvement on one of the fabrication process flows is discussed. Test results on a WR1.5 waveguide band (500 - 750 GHz) on-wafer probe are shown to demonstrate the repeatability and reliability of the probe.

Chapter 3 of the work focuses on the theoretical background of differential MMIC. Arguments in favor of differential MMIC are first presented that demonstrate the advantages of using a differential configuration. Then the fundamentals of differential MMIC characterization, including the mixed-mode S-parameters and the characterization methods, are discussed. Balun integrated probes are proposed to help facilitate differential MMIC characterization and the characterization uncertainties using this method is evaluated. From this characterization uncertainties simulation, the target performance of the balun integrated probe is proposed.

Chapter 4 of this dissertation concerns the design considerations of the balun integrated probes. An overview of different balun implementations are first given to introduce the coupled line based balun design that will be employed in this work.

Then the design methodologies for three reported balun variations based on coupled lines, the uncompensated balun, the compensated balun and the Marchand balun, are explored. The Marchand balun is preferred over other balun designs because of its low phase and amplitude imbalance, its broadband nature, and the ease of implementation. Detailed design considerations to integrate the Marchand balun with the on-wafer probe are also given.

In Chapter 5, the fabrication and characterization of the balun integrated probes are presented. Step-by-step fabrication processes of the balun integrated probe are discussed. The balun test structures to validate the design approach are first characterized. The measurement results demonstrate a functional balun although discrepancies between the measured and the simulated results exist, primarily due to uncertainties brought about by the characterization practice. The on-wafer probes are then characterized using dual delayed short standards. Good agreement between the measured and simulated results are obtained. The S-parameters of the balun integrated probe have achieved the proposed target performance.

In Chapter 6, conclusions are drawn for this on-wafer probe project. Future work is discussed including the characterization of high frequency resistors and the potential of scaling this prototype balun integrated probe to higher frequencies.

Chapter 2

SOI Processing techniques for On-wafer Probe Fabrication

2.1 Introduction to Si Fabrication Technology

Si fabrication technology generally refers to an array of methods and processing techniques to fabricate large scale integrated circuits on Si wafers. It typically involves many complicated and precisely controlled fabrication steps such as semiconductor crystal growth, ion implantation, photolithography, thermal oxidation growth, thin film deposition, dry etching and wet etching, etc. These steps can be combined to create miniaturized integrated circuits on an enormous scale. For example, it is common place today to have a 4GB memory chip about the same size as a quarter, which means there are about 10^{10} CMOS devices packaged in that single chip.

Si fabrication technology is also evolving at a very rapid pace. According to the Moore's Law, the density of transistors in a large scale integrated circuit doubles approximately every 18 months. This is enabled by the relentless miniaturization of semiconductor processing capabilities. With the capability to fabricate smaller semiconductor devices, more functional components can be integrated into a single chip, giving rise to greater computational capabilities for today's electronics. It is said that the bulky computer system deployed in Apollo 11 mission to put man on the moon was not as capable as a pocket computer today.

This section of the dissertation will give a brief introduction to germane Si fabrication technologies, with special focus on the capabilities and limitations of the tools at the UVML. In later sections of this chapter, these fabrication capabilities will be explored to develop and improve SOI processing techniques that have been used to fabricate various on-wafer probes.

Among the many steps involved in the fabrication of on-wafer probes, the lithography step is the major source of fabrication limitations. There are two deep UV aligners for photolithography at UVML, the EVG aligner and the MJB4 aligner. While both aligners are used for the fabrication of on-wafer probes, the two tools offer different capabilities. First, the EVG aligner can be used in either front-side alignment mode or backside alignment mode, while the MJB4 is only capable of the former. The initial fabrication processes took advantage of EVG's backside alignment capability to achieve alignment between front-side and backside metallization features on $15\mu m$ thick Si film. However, an issue with the EVG control software was later discovered, revealing that the backside alignment precision could be severely jeopardized under certain circumstances. As a result, new fabrication processes were proposed to avoid the use of backside alignment functionality of the EVG tool, as will be discussed in later sections. Second, the EVG aligner offers slightly higher alignment precision when used in the front-side alignment mode. The mechanics of the EVG tool is designed to have minimum shift when the wafer is brought into close contact with the mask for exposure. When the wafer is brought into contact for lithography with the MJB4 tool, it has been observed that there is a slight shift between the wafer and mask. This has limited the alignment precision with the MJB4 tool. However, the EVG aligner also suffers from a few drawbacks as will be discussed later.

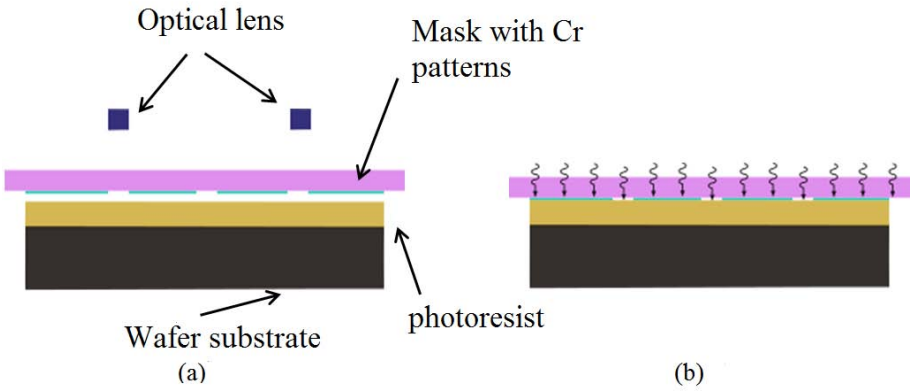

Figure 2.1: The lithography steps, (a) separation mode for wafer to mask alignment, (b) contact mode for UV exposure.

Shown in Fig 2.1 are the two alignment steps involved in lithography. The wafer, which is first spin coated with photoresist, is brought into close proximity with a quartz mask that is pre-fabricated with high resolution chrome patterns. This step is in aligner's separation mode to allow for wafer-to-mask alignment. When the alignment is satisfactory, the wafer is brought into contact with the mask. The operator could then apply vacuum adhesion between the wafer holder and the mask for vacuum contact (only available on EVG), or provide an upward push with nitrogen for hard contact, or do both for vacuum plus hard contact. The purpose of these contact modes is to level out the wafer surface and provide a good contact for UV exposure. The UV light source then moves forward and shines collimated light on the mask. The exposed wafer is then developed in diluted AZ400K solution to complete the lithography step.

A number of issues could impact the quality of the photolithography process. The first is when the alignment is finished and the contact force is being applied, the wafer can shift. This is especially a problem for the MJB4 aligner due to poorer mechanical components. In oder to alleviate this problem, the MJB4 aligner does have an option for alignment check before exposure. This alignment check option brings the wafer into full contact with the mask, applying necessary contact force

according to the contact mode setting (vacuum contact, hard contact or both), and allows the operator to inspect the final alignment. The operator can then choose to proceed to UV exposure if the alignment is still satisfactory, or go back to separation mode for re-alignment if mis-alignment is out of tolerance.

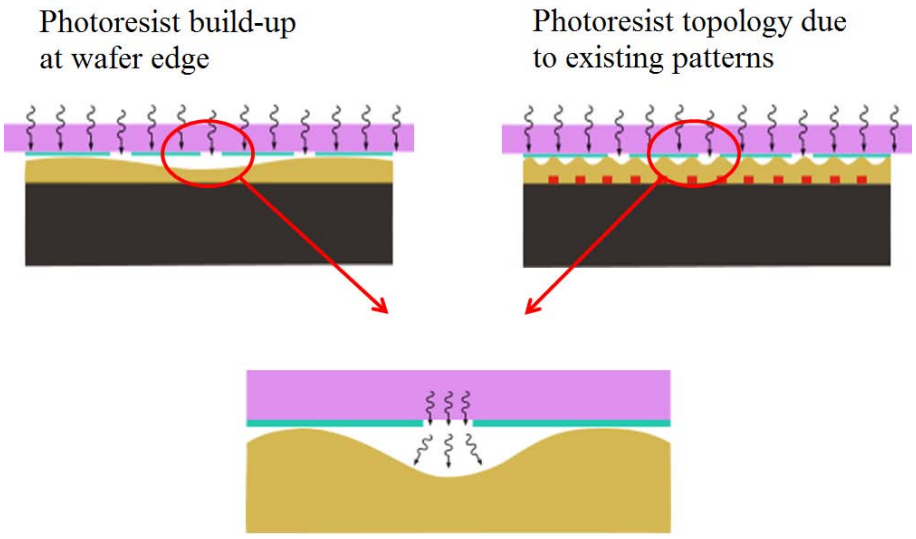

Figure 2.2: Light diffusion causes expanded transferred patterns.

Other issues that could impact the quality of photolithography include the photoresist edge bead and photoresist surface topology. Photoresist tends to build up at the edge of the wafer during the spin coating process, which makes the edge of the wafer higher than the center of the wafer. Or, if the wafer is already patterned with features of a few microns thickness, the spin coated photoresist will have a surface topology following the topology of the wafer patterns. Both issues create an uneven photoresist surface that will be a problem for the following lithography process. During UV exposure, the regional variations in surface height cause contact gaps that allow for more diffracted light during the exposure, as illustrated in Fig 2.2. This diffracted light will cause the sidewall of the photoresist to be exposed and developed by diluted AZ400K. If this lithography step defines the shape for Au plating, the end result will be larger Au circuit patterns than desired.

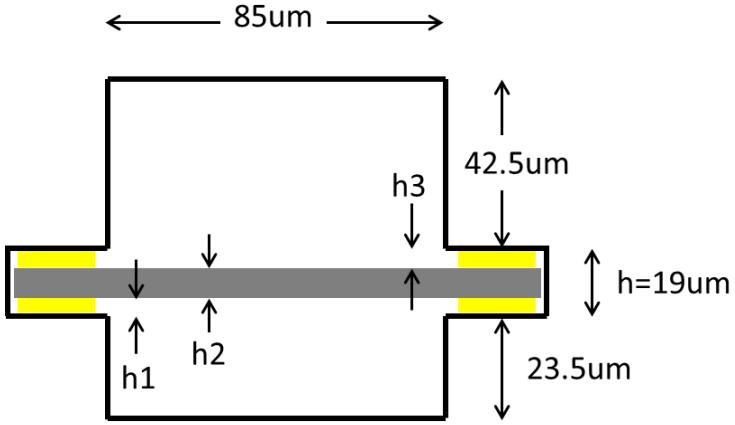

Figure 2.3: Cross section view of the probe channel when the probe is assembled.

Apart from these intrinsic issues with the aligner tool, the photoresist also has a role in determining the lithography fabrication limits. For example, the specific photoresist to be used in the Au plating lithography for this on-wafer probe project is determined by the thickness of the desired gold patterns. The consideration for plated Au thickness is that the on-wafer probe is designed to be clamped by a waveguide block, as shown in Fig 2.3 for a W-band block design. In order to achieve this goal, the sum of the thickness for front-side metal h_1, Si beam h_2, and backside metal h_3, must be greater than the clamp recess depth h plus $5\mu m$ machining tolerance, or $h_1 + h_2 + h_3 \geq h + 5\mu m$. Since the SOI thickness (ignoring fabrication tolerances) $h_2 = 15\mu m$ and the block recess depth $h = 19\mu m$, the minimum thickness for front-side and backside gold should have $h_1 + h_3 \geq 9\mu m$.

For W-band on-wafer probes, the front-side and backside gold thickness is chosen to be around $5\mu m$ each. AZ4620 photoresist is used for lithography processes, which typically gives around $6.2\mu m$ thickness at 4 krpm spin speed, and has a resolution limit of about $6\mu m$ for minimum achievable line width. For higher frequency on-wafer probes, a new mask is introduced to plate extra gold on the probe clamp region and avoid plating thick gold for both front-side and backside circuit. As a result, the thickness requirement posed by clamping conditions can be relaxed. Both front-side

and backside gold thickness is thus chosen to be around $3\mu m$. AZ4330 photoresist can be used for both front-side and backside lithography. It gives about $3.3\mu m$ thick photoresist at 4krpm spin speed and can work with finer features. As shown in Fig 2.5, minimum line width of $4\mu m$ and gap of $2\mu m$ has been achieved under good contact conditions.

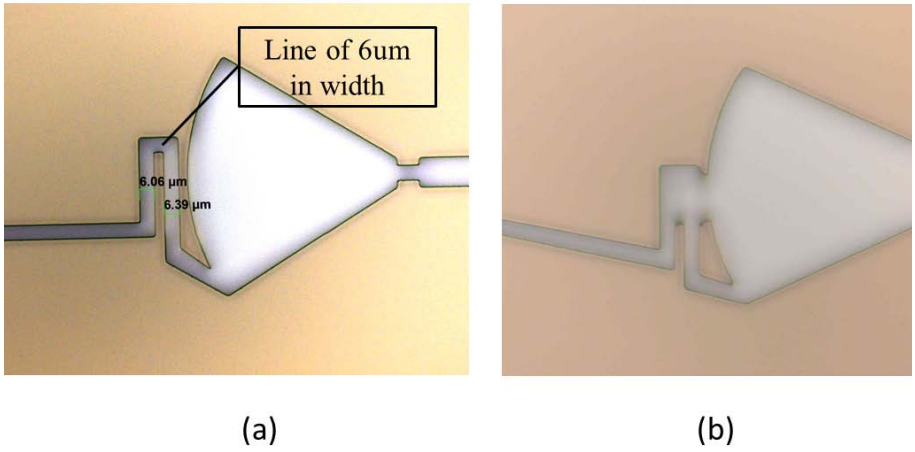

Figure 2.4: Lithography results for critical features as small as $6\mu m$ in width achieved with AZ4620 photoresist, (a) a successful lithography with precise pattern transfer, and (b) a failed lithography that gives expanded transferred patterns.

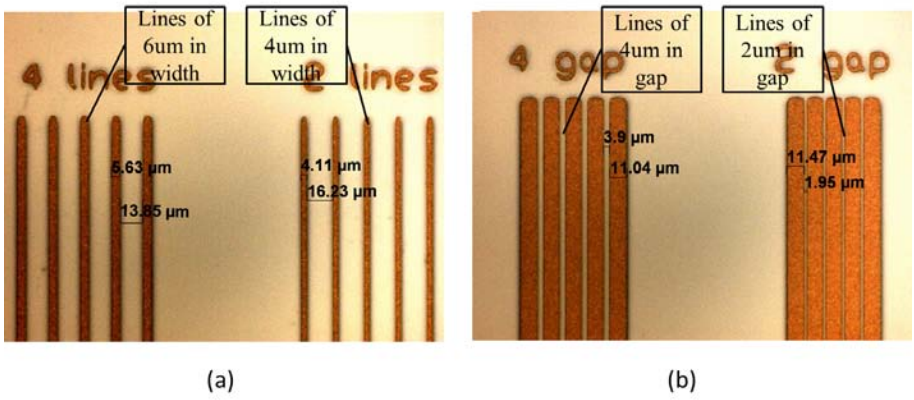

Figure 2.5: Gold plating results for (a) critical features as small as $4\mu m$ in width, and (b) critical features as small as $2\mu m$ in gap, achieved with AZ4330 photoresist.

Besides photolithography, other important Si processing techniques used for on-wafer probe fabrication include metallic thin film sputter deposition, electrical plating,

dry and wet etching. Shown in Fig 2.6 is the process flow to fabricate plated gold patterns on Si wafer, using the mentioned techniques.

In order to minimize RF loss, the Si substrate used for on-wafer probe is high resistivity Si specified to be greater than $10,000\,Ohm \cdot cm$. Additionally, plated gold does not adhere well to bare Si substrate, and it is also not possible to plate gold film directly on top of a Si wafer. Therefore, a sputtered metallic seed layer for electrical plating has to be employed. The chosen seed layer consists of a Ti/Au/Ti tri-layer, each layer approximately 50nm thick, as shown in Fig 2.6(b). The bottom Ti layer helps improve adhesion between sputtered gold and Si substrate, and the top Ti is used to avoid plating gold, under the photoresist plating mask at the perimeter of the features.

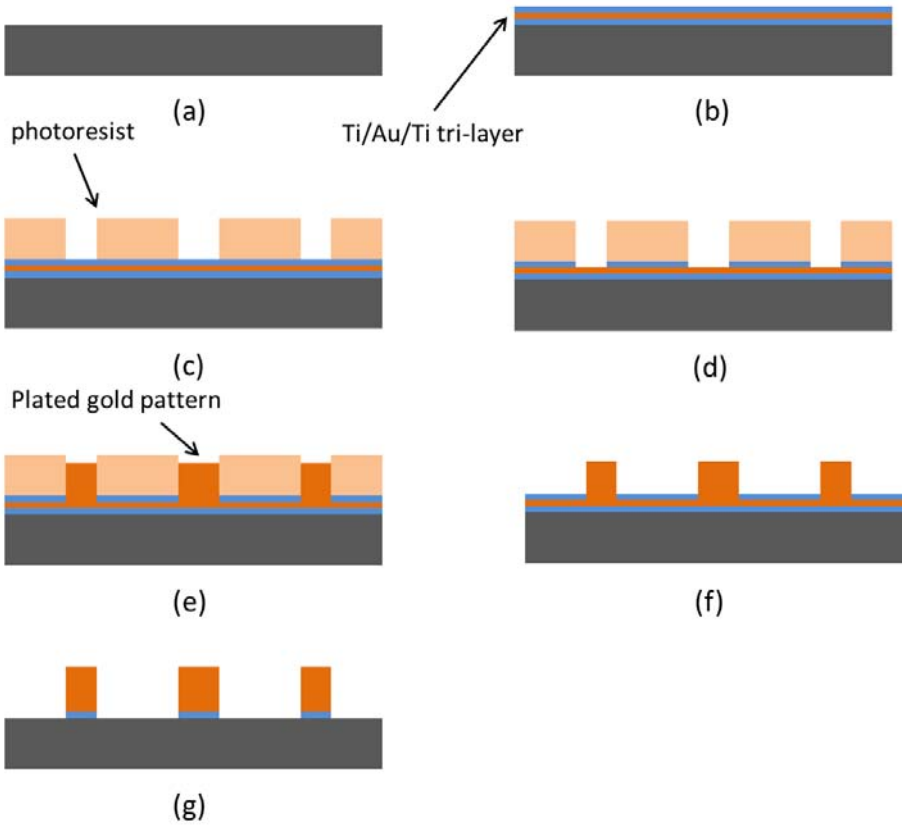

Figure 2.6: Gold plating fabrication process flow. (a) wafer clean, (b) Ti/Au/Ti seedlayer deposition, (c) lithography, (d) etch top Ti, (e) gold plating, (f) resist strip, (g) seedlayer removal.

After the Si wafer is coated with a Ti/Au/Ti seed layer, it is then patterned with photoresist. The area to be plated with gold is UV exposed and developed to become photoresist openings, which is shown in Fig 2.6(c). To define the perimeter plating barrier of Ti, the top Ti at the plating area needs to be removed. A dry etch process in a Semigroup 1000-TP RIE etch tool is employed to achieve anisotropic Ti etch using etchant gas species SF_6. It has 20sccm of SF_6 flow, 5sccm of CHF_3 flow and 0.6sccm of O_2, at pressure of 30mTorr and RF power of 80W. The step for top Ti removal is shown in Fig 2.6(d).

After the unmasked top Ti layer is removed, the revealed Au layer is open for electrical plating, as shown in Fig 2.6(e). A prolonged Ti dry etch (more than 10 minutes) is found to be able to remove the sputtered Au layer too, but a timed etch (2 minutes) has consistently left enough Au on wafer for electrical plating. It is also found that performing a 'similar' Ti etch in a different tool can produce unexpected results. Performing this Ti etch with similar conditions in the Oxford etching tool, more gold particles tend to be re-sputtered on to adjacent photoresist features due to the different etching environment. This results in plated gold build up around the photoresist. However, it is expected that a successful Ti etch recipe in the Oxford tool, using lower RF power, could be obtained with further experimentation.

When the gold plating is completed, the photoresist can be removed. The Ti/Au/Ti seed layers beneath the plating photoresist should also be removed since they are for plating protection purpose only, not for electrical connection. This is done by sequentially performing a Ti dry etch, gold wet etch and Ti dry etch. What remains on the wafer are plated gold patterns as defined by lithography, as shown in Fig 2.6(g).

2.2 Deep Si Etch and Backside Alignment for SOI Processing

This section will focus on two important techniques for on-wafer probe fabrication, the deep Si etch and backside alignment. Over the years of development, the technologies

of plasma etching for semiconductor materials have become mature techniques for wide spread industry applications. The pseudo Bosch process described here is one of the Si etch processes developed for high aspect ratio Si etch. It is realized at the UVML using the commercially available Oxford Instrument Plasmalab System 100 ICP-RIE etch tool, as shown in Fig 2.7.

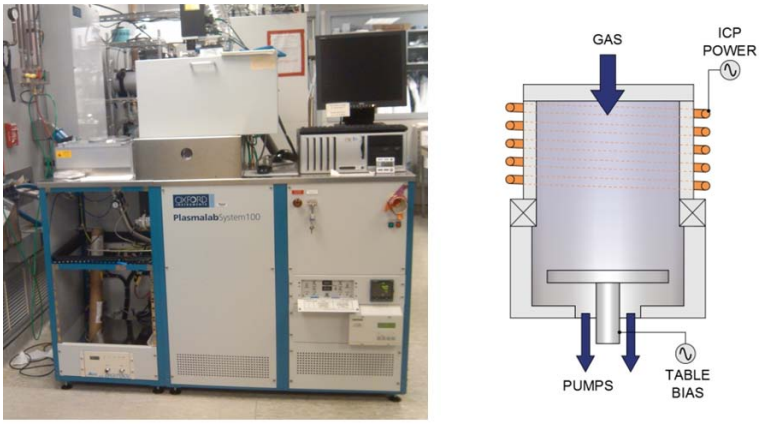

Figure 2.7: The Oxford Instrument Plasmalab System 100 ICP-RIE etch tool for deep Si etch.

As is indicated by its name, the Oxford Instrument ICP-RIE tool involves two components in its hardware, the Inductively Coupled Plasma technology (ICP) and the Reactive Ion Etching (RIE) techonology. The ICP power is used to generate a time-varying magnetic field inside the coils, which then through the Maxwell-Faraday equation induces a circulating electrical field in the plane perpendicular to the coils. This electrical field causes electrons to be accelerated and collide with the slowly moving molecules, contributing to the low energy ionization of the gas. By changing the ICP power delivered to the coil, the plasma density can be controlled.

The plasma generated from the ICP process diffuses into the chamber for vertical acceleration. An RF power is applied to the substrate platter to generate a time-varying electrical field in the chamber. This time-varying electrical field allows for more plasma generation by accelerating the light weight electrons to collide with and thus further ionize gas molecules. The massive ions, on the other hand, are less mobile

and not able to move as far in the rapidly oscilating electrical field. If the anode plate (the substrate holder table in Fig 2.7) is isolated from DC ground with a capacitor, negative charges will accumulate on the anode plate, resulting in a DC bias voltage. The positive ions of the gas spieces are then attracted by the negatively charged table plate and are accelerated toward it. Thus, the RIE power supply provides the gas ions with a vertial momentum and determines the energy of the ions when they reach the table plate. By allowing relatively independent control of both plasma density and directional kinetic energy, the Oxford Instrument ICP-RIE tool provides a powerful means for dry etch.

The pseudo Bosch etch process uses the Oxford ICP-RIE tool to fabricate high aspect ratio Si structures. The process uses two gas species SF_6 and C_4F_8 for the deep Si etch. The SF_6 is the primary gas etchant that becomes ionized in the chamber to provide fluorine ions to actively etch the Si. The C_4F_8, though also releasing fluorine, is the passivation gas species that helps create a polymer chain deposited on the Si surface to protect it from chemical reactive etching. However, with sufficient RF power, the directionality of the accelerated fluorine ions supplied by the ICP-RIE tool means that the fluorine ions are able to physically remove the polymer chain at the horizontal planes of the Si surface. If the polymer growth is sufficiently robust and the energy of laterally scattered ions is sufficiently low, the polymer will remain on the vertical sidewalls. As a result, the etch process occurs at the horizontal planes but is greatly reduced at the sidewalls. The resulting process outcome can be very vertical sidewalls for patterns etched in Si, as shown below in Fig 2.8.

Although using the same etchant gas species and sharing a lot of similarities in the etching and passivation processes, the pseudo Bosch process is different from the Bosch process that is widely employed in the semiconductor industry. The Bosch process repeatedly alternates between the etching mode and the passivation mode, with only one purpose served at a time. This results in a wave like sidewall surface from the cycling between the two modes. The pseudo Bosch process, however, is

continuous for both the etching and the passivation. The sidewall of the etched structures can be much smoother because of this continual process, as demonstrated in Fig 2.8, but the etch rate is much lower than that of the Bosch process.

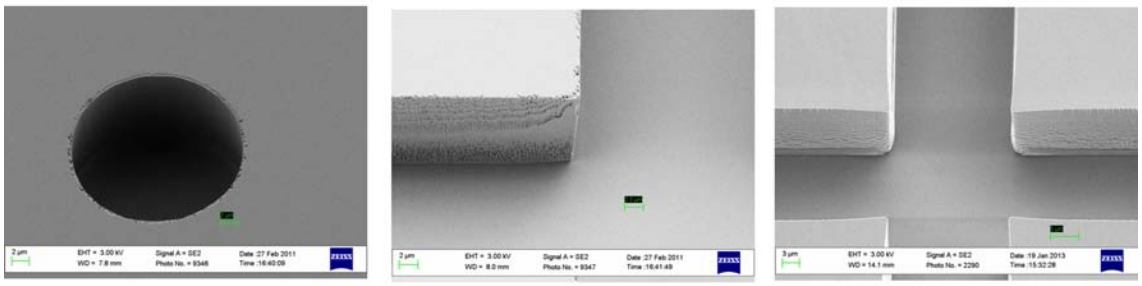

Figure 2.8: Sidewalls of Si patterns etched using pesudo Bosch deep Si etch process.

The pseudo Bosch process for deep Si etch has been well studied and documented in the literature[40]. Initial tests were performed at the UVML to find a working recipe for on-wafer probes fabrication. The tests were done at 500W ICP power, 40W RIE power, at $0°C$ degrees table temperature under 15mTorr chamber pressure. The gas flow rates for SF_6 and C_4F_8 are varied to study their impact on the etching rate and etched Si profiles. It is found that with greater SF_6 to C_4F_8 ratio, the etching rate becomes faster with a compromise of increased sidewall surface roughness.

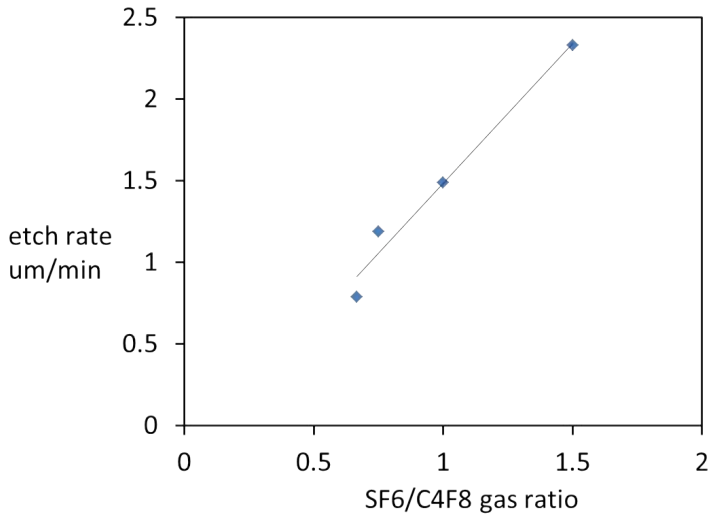

Figure 2.9: Si etch rate for various SF_6/C_4F_8 gas ratios.

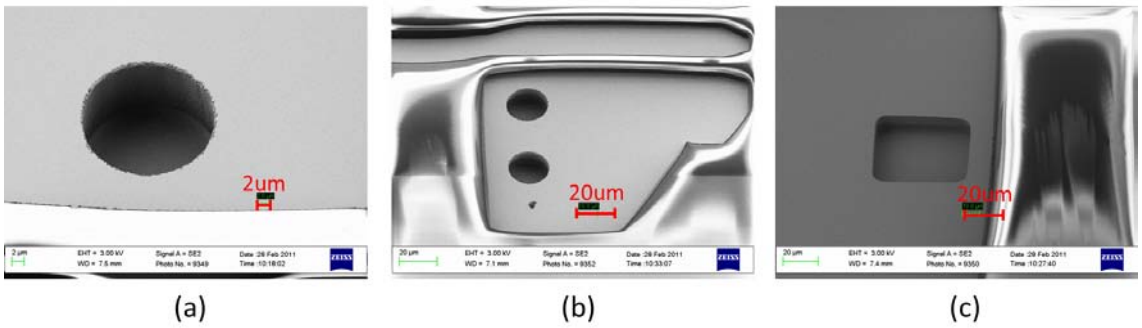

Figure 2.10: (a) Si via holes etched using the pseudo Bosch process, and (b) and (c) the photoresist patterns around the via holes after a lithography step.

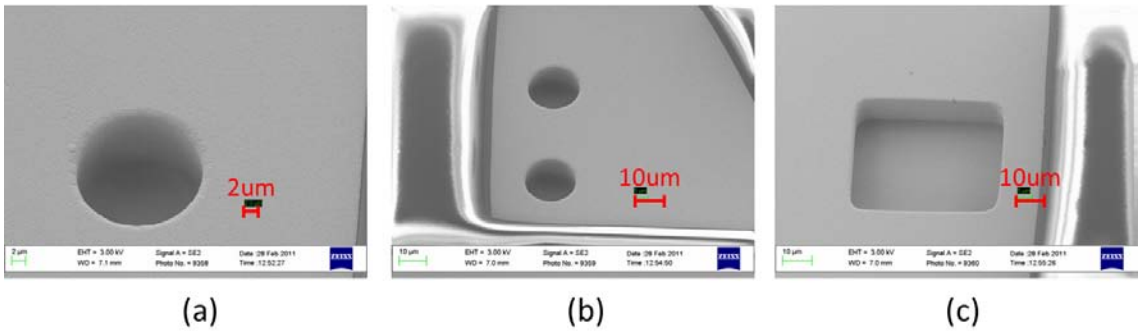

Figure 2.11: (a) and (b), Gold being plated inside the via holes of $20\mu m$ diameter, and (c) gold being plated inside the rectangular via hole of $60\mu m \times 45\mu m$ dimension.

The via holes are designed to make electrical connection between the front-side and backside gold circuits. Gold plating inside the via holes is crucial for the proper functioning of the probe. Tests and fabrication experience show that it is possible to plate gold in the vias, as demonstrated in Fig 2.10 and 2.11. The shiny features around the via holes in the SEM figures are photoresist not yet stripped from the wafer, which looks bright because of regional charge accumulation. The plating gold builds up at the bottom as well as the sidewalls of the via holes as small as $20\mu m$ in diameter. This is ensured by the seedlayer deposition step in the gold plating process described in Fig 2.6. During the Ti/Au/Ti seed layer deposition, both the Ti and the Au molecules are arriving at an angle to the wafer surface. The simultaneous rotation

of the wafer leads to successful seed layer deposition at the sidewalls and the bottom planes of the via. Gold plating can therefore occur on the sidewalls and bottom of the vias, resulting in a shell of Au inside the via.

Another important technique for on-wafer probe fabrication is the backside alignment for SOI wafers. The SOI wafer has a layered silicon-insulator-silicon substrate in place of conventional silicon substrate. The wafer has the $15\mu m$ thick high resistivity device layer, the $1\mu m$ oxide layer and the $450\mu m$ handle layer. Detailed processes flow for on-wafer probe fabrication using SOI wafers will be discussed in later sections. Here the discussion will be focused on the two processing techniques developed to achieve backside and front-side patterns alignment. These two processing techniques are named the true backside alignment and via-aided alignment in the following sections.

For the true backside alignment scheme, the front-side plated gold patterns, including alignment markers for all subsequent backside lithography steps, have to first be fabricated on a SOI wafer. The wafer is then mounted upside down to a quartz carrier wafer using epoxy and wafer bond. After backside mounting, the handle layer is removed using a combination of dicing and dry etching, and the oxide layer is removed using wet etch, to arrive at the backside of the $15\mu m$ thick device layer of the SOI wafer. The next step is the backside lithography where true backside alignment is needed.

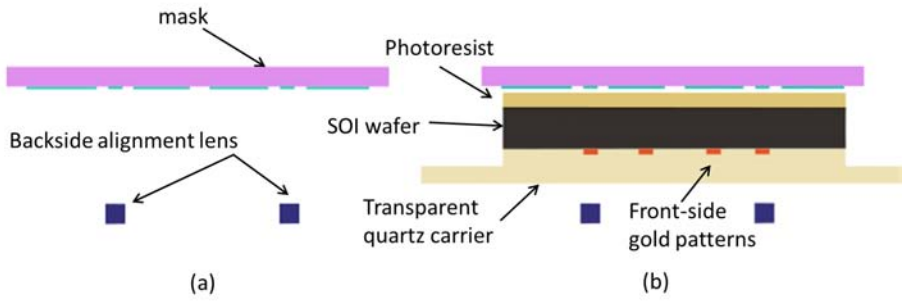

Figure 2.12: True backside alignment process steps, (a) the backside alignment lens takes a picture of the alignment markers of the mask and fixes their positions thereafter, (b) the wafer is aligned to the on-screen images of mask alignment markers.

The true backside alignment is carried out on the EVG aligner in two steps, as shown in Fig 2.12. There are two optical lens in EVG that are dedicated to backside alignment, and can look upward through the glass substrate holder. When the mask is mounted to the mask holder, the operator can move the optical lenses around to find the alignment markers at the two sides of the mask. After loading the mask, the computer records the position readings of the two optical lenses and takes pictures of the alignment markers on the mask. The mask and the optical lens are then locked into their current positions and are not freely movable. Then the wafer with spin coated photoresist is loaded into the aligner and brought into small separation 'contact' with the mask. Before the contact force is applied, there is still a gap separation between the wafer and the mask that allows for free movement of the wafer. Through the glass substrate holder and the transparent quartz wafer carrier, the optical lens can see the front-side patterns of the SOI wafer, but not the mask since the view is blocked by the nontransparent Si wafer. The creative design of the EVG tool allows the operator to move the wafer around and align the wafer to the captured, but displayed on-screen images of the mask alignment markers taken in the previous step. This completes the second step of the backside alignment process. Then UV light is shone onto the mask to expose the wafer.

Although the true backside alignment techniques for SOI processing have been successfully applied to on-wafer probe fabrication, there are a few intrinsic problems with the EVG tool. The first is that there are some issues with the control software of the EVG tool. The digital images from the backside alignment lenses sometimes freezes halfway during the lithography step, disrupting all ongoing alignment efforts. The second, which is potentially more detrimental, is that the control software is not able to read the exact position of the backside alignment lens with precision better than $10\mu m$. Slightly inadvertently shifted position of the lenses, unnoticed by the control software, could cause significant misalignment across the wafer. The third is that the on-screen images of the via features taken by the digital camera in EVG are

not as sharp as that seen through optical lens with other aligners, further increasing the difficulty for high precision alignment.

As a result of these intrinsic issues with the backside alignment, a new fabrication alignment process is proposed. The new processing technique employs the via alignment markers etched using the deep Si etch process to improve the alignment precision. Fabrication experiences show that the via hole etch can achieve sufficiently straight sidewalls to serve as alignment markers for both front-side and backside lithography, as shown in Fig 2.13 (with a tilted view of the etched sidewall). Also shown in Fig 2.14 are front-side and backside views of the alignment markers. Seen from the backside, the alignment markers are bright enough to be seen clearly under the aligner microscope for alignment purposes. A new fabrication scheme is thus proposed to avoid the problems with the true backside alignment mode and to improve alignment precision.

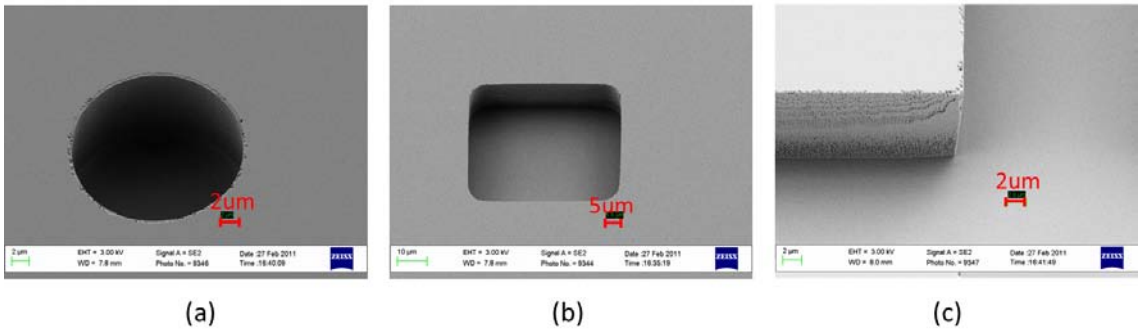

Figure 2.13: Tilted SEM view of the sidewalls of the etched Si structures.

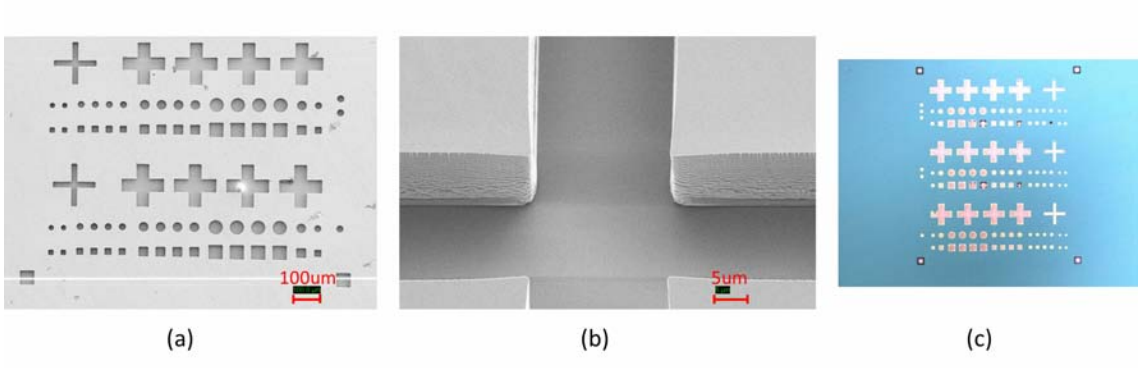

Figure 2.14: The etched alignment markers seen from the front-side and backside. The left and the middle images are taken in an SEM, while the right is taken with a table microscope.

With this new via-aided alignment scheme, via holes including alignment markers are first etched. For subsequent lithography processes, either at the front-side or backside, the mask is aligned to the via hole alignment markers as if performing a front-side alignment. This greatly reduces alignment difficulties while improving alignment precision. This new SOI processing technique has been employed to successfully fabricate various on-wafer probes from 140 GHz to 1.1 THz.

2.3 SOI Processing Techniques Using True Backside Alignment

As mentioned in previous section, two processes have been developed at UVML for on-wafer probe fabrication, the true backside alignment and the via-aided backside alignment. In this section, the fabrication processes using true backside alignment with the EVG aligner will be discussed.

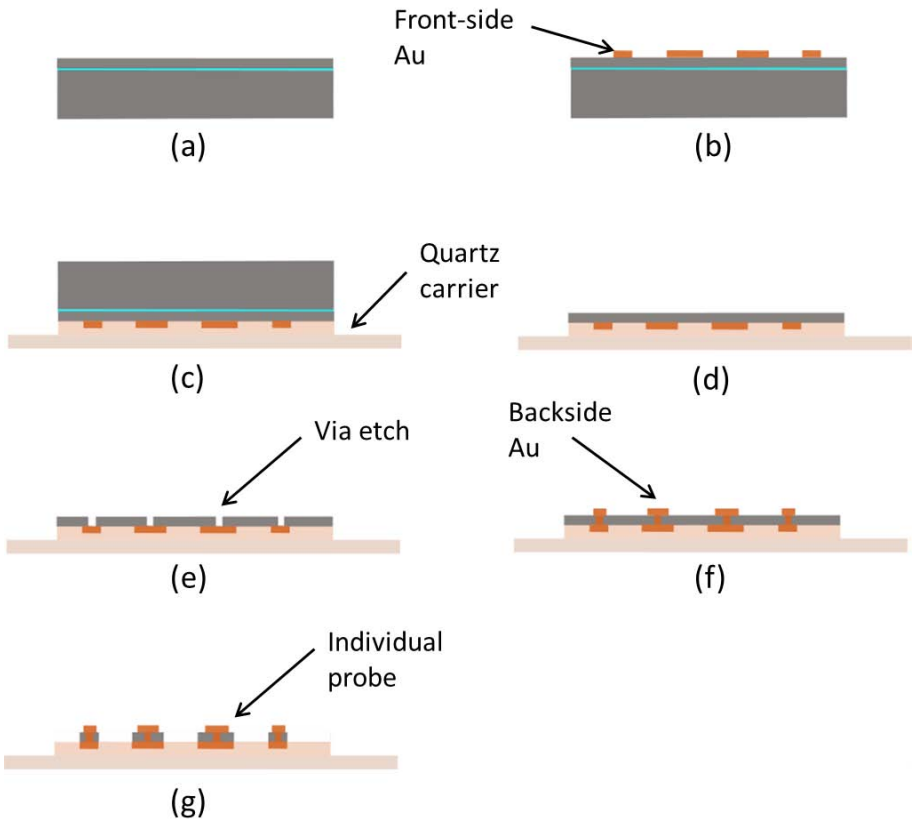

Figure 2.15: The on-wafer probe fabrication process flow using true backside alignment. (a) wafer cleaning, (b) front-side plating gold circuit definition, (c) backside mounting of the SOI wafer, (d) the handle and the oxide layer removal, (e) via hole etch, (f) backside plating gold circuit definition, (g) extents etching for probe contour definition.

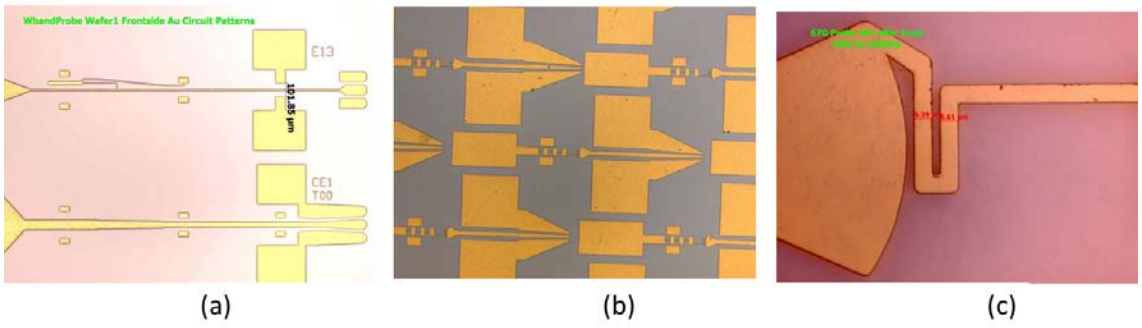

Figure 2.16: Typical front-side plated gold patterns.

Shown in Fig 2.15 is the process flow using true backside alignment. These fabrication processes have been used to fabricate on-wafer probes at W-band (75 to 110

GHz) and W1.5 waveguide band (500 to 750 GHz). It starts with thoroughly cleaning the wafer surface. Then the wafer is patterned with front-side gold features using the gold plating processes outlined in Fig 2.6. Shown in Fig 2.16 are a few figures after the front-side gold plating for W-band and WR1.5 waveguide band on-wafer probe fabrication.

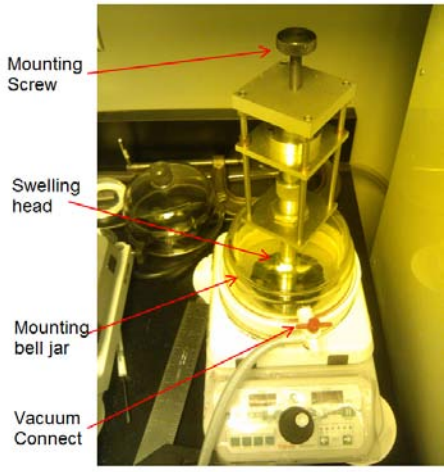

Figure 2.17: The backside mounting jig.

When front-side patterns are finished, the next step is to mount the wafer upside down onto a carrier wafer for backside processing. This is achieved using a homemade backside mounting jig shown in Fig 2.17. The wafer surface is first spin coated with wafer bond, a sticky adhesion layer that dissolves in TCE. The wafer is then placed on a $150°C$ hotplate in vacuum environment for at least 25min to remove air bubbles and the majority of the solvents in wafer bond. At the same time, an epoxy mixture is also prepared and placed in a vacuum bell jar for 30min to remove air bubbles. When both are prepared, a handheld microdispenser is used to dispense the epoxy to the center of a 3inch quartz carrier wafer. The SOI wafer to be mounted is attached to a swivelling head of the mounting jig using Apiezon L-grease, and placed upside down over the center of the quartz wafer where the viscous epoxy fluid sits. The bell jar of the mounting jig is placed on top of the hotplate, and is connected to vacuum supply. The whole mounting system is kept in vacuum condition with hotplate turned off

for another 30min to help remove any air bubbles trapped in epoxy and wafer bond. Then the screw on top of the bell jar pushes the SOI wafer down to be in contact with the carrier, modestly squeezing out excessive epoxy. The hotplate is then turned on at $100°C$. After curing the epoxy for 5min, the wafer stack is taken out and slided off the mounting jig, and is cleaned of excessive grease and epoxy using TCE (C_2HCl_3, a common solvent used by the semiconductor industry) and methanol. The previous 5min cure at $100°C$ results in an epoxy just viscous enough for wafer handling, but can still be easily removed with methanol. After cleaning, the wafer is placed under a commercial pressing jig, using a silicone sheet to distribute the load, to provide a constant pressure between the SOI wafer and the carrier until the epoxy permanently cures at $100°C$.

When the backside mounting is finished, the SOI wafer is now mounted upside down to a quartz carrier, and the backside processing for the SOI wafer can begin. The first step is to remove the $450\mu m$ thick handle layer, which is achieved by a combination of dicing and RIE plasma etching. The dicing tool uses a 0.5mm wide blade to dice across the whole SOI wafer cut by cut, removing up to $420\mu m$ thickness of the handle layer. Then the wafer is etched using an RIE only Si etching recipe to remove the remaining 20-40μm of the handle silicon. The RIE only Si etch is very selective between Si and silicon oxide and will stop at the oxide layer. Etching tests show that an hour of over-etch, which is typically longer than the time required to remove the remaining Si, is not able to etch through the $1\mu m$ thick oxide layer. After the handle layer is thoroughly removed, the wafer is soaked in BOE for about 20min to strip the oxide layer. Similarly, the BOE wet etch is highly selective between silicon oxide and Si. The result of the oxide strip is a nicely clean Si surface at the backside of the $15\mu m$ thick device layer.

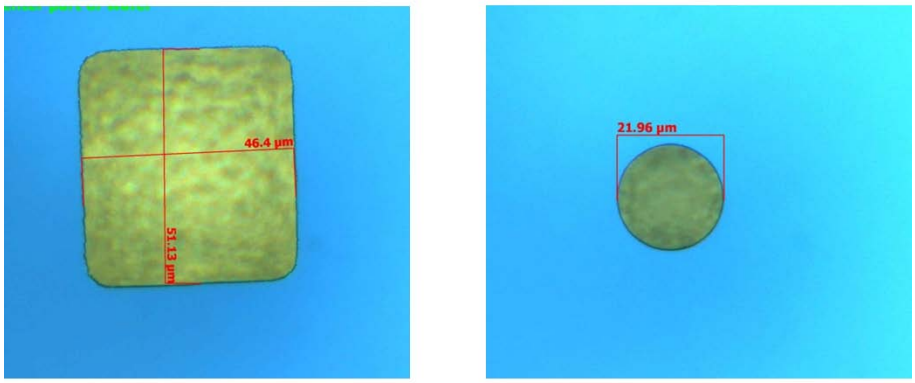

Figure 2.18: Microscope images of etched via holes at the backside of the device layer, the front-side gold can be seen at the bottom of the etched vias (blurred because the focus point is at the edge of the Si).

With the revealing of the backside of the device layer, the next step is the via hole etch to make electrical connection between front-side and backside gold features. This step is achieved using true backside alignment on the EVG aligner as discussed in the previous section. After the via hole lithography is performed, the photoresist is baked and UV cured to make it more durable during the subsequent dry etch. The via hole etch is performed in the Oxford Instrument Plasmalab System 100, using the deep Si etch recipe discussed in the previous section. The photoresist is then stripped after the via hole etch, using an oxygen plasma followed by liquid photoresist stripper. Shown in Fig 2.18 are a few figures after the via hole etch.

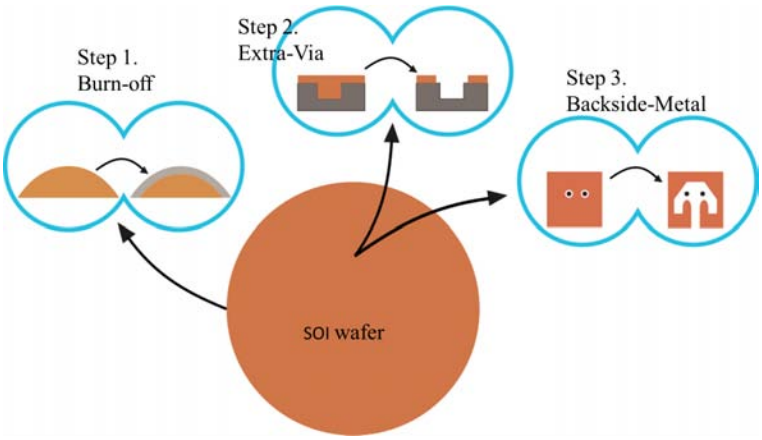

Figure 2.19: The three lithography steps to pattern backside gold plating features.

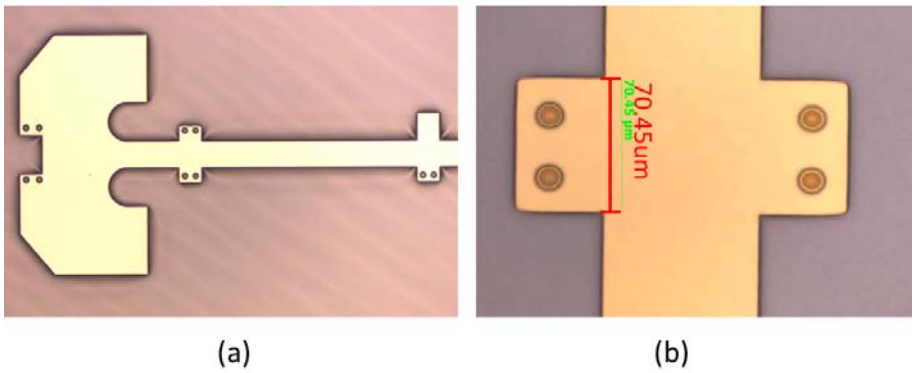

Figure 2.20: Microscope images of the backside gold plating lithography, (a) after backside metal lithography, (b) after gold plating.

After the via hole etch, the next step is backside gold plating. The whole wafer is first sputtered with a Ti/Au/Ti seed layer, which also covers the sidewalls of the via holes for gold plating. The backside gold plating lithography is complicated by the photoresist surface topology due to the presence of the via holes. Three individual lithography steps are performed one after another using different masks to pattern the backside gold plating features, as shown in Fig 2.19. The first is the burn-off mask, which exposes the edge of the wafer, taking away excessive photoresist build-up at the ring edge of the wafer. After development, the second lithography step is used to provide extra UV light exposure to the via regions because there is considerably more photoresist filling the via holes. It is found by trial and error that approximately two times the normal exposure dosage is sufficient to expose the photoresist in the via holes well. When the wafer is then developed in diluted AZ400K solution, light ultrasonic vibration is used to help the develop solution find its way into the via holes and dissolve the photoresist inside, until the photoresist around the via holes are developed. When extra via exposure and development is done, the backside plating mask is then used to define gold plating patterns. This lithography can now be performed with relatively good contact and visibility.

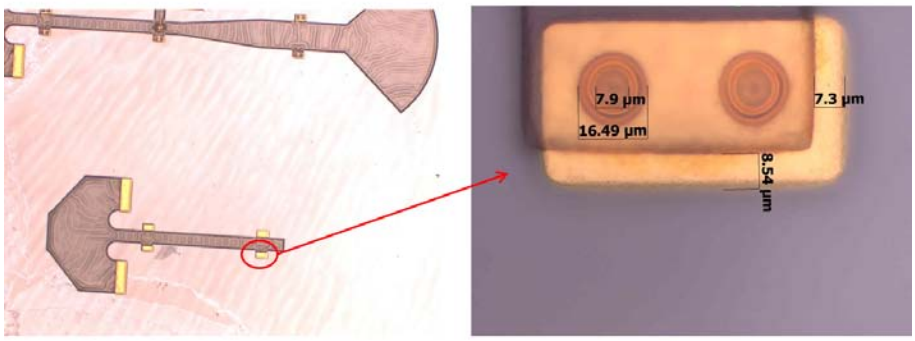

Figure 2.21: After the extents lithography, the probe contour is defined to prepare for subsequent Si etch.

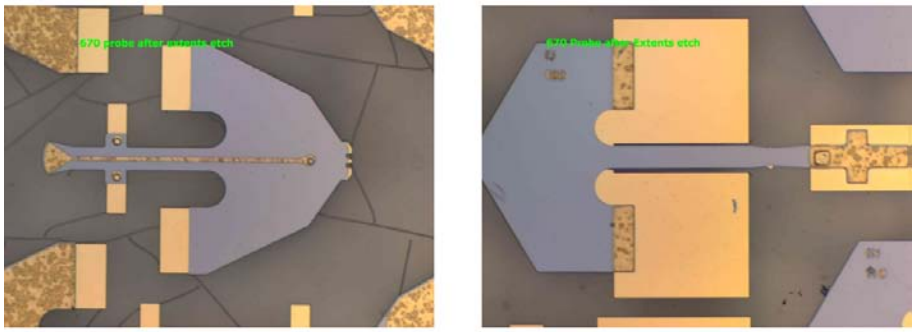

Figure 2.22: After extents etch, individual probes stay on the carrier wafer.

After backside gold plating is the extents lithography and etch. These step define the Si probe contour using photoresist, as shown in Fig 2.21(a). The area covered with photoresist is protected from etching in the subsequent anisotropic Si etch, while the rest of the Si is etched, leaving individual probes on the carrier. In order to improve the photoresist durability for a prolonged Si etch, the photoresist is hardened by UV treatment, which gives the ripple effect to the photoresist surface as shown in Fig 2.21(a). The Si etch is again performed in the Oxford Instrument Plasmalab System 100 using the deep Si etch recipe. The result of the Si etch are individual probes still attached to the carrier wafer, as shown in Fig 2.22. The wafer is then soaked in TCE

solution to dissolve the wafer bond beneath the probes and to release the individual probes from the carrier.

2.4 SOI Processing Techniques Using Via-aided Alignment

In the previous section, SOI processing techniques using the true backside alignment with the EVG aligner have been developed for on-wafer probe fabrication. Although these processing techniques have been applied to the fabrication of W-band (75 to 110 GHz) and W1.5 waveguide band (500 to 750 GHz) on-wafer probes, a few problems have emerged that revealed the limitations of these fabrication processes. In order to address these issues, fabrication processes using a via-aided backside alignment scheme are proposed. This section is devoted to the discussion of these new fabrication processes and the improvement associated with them.

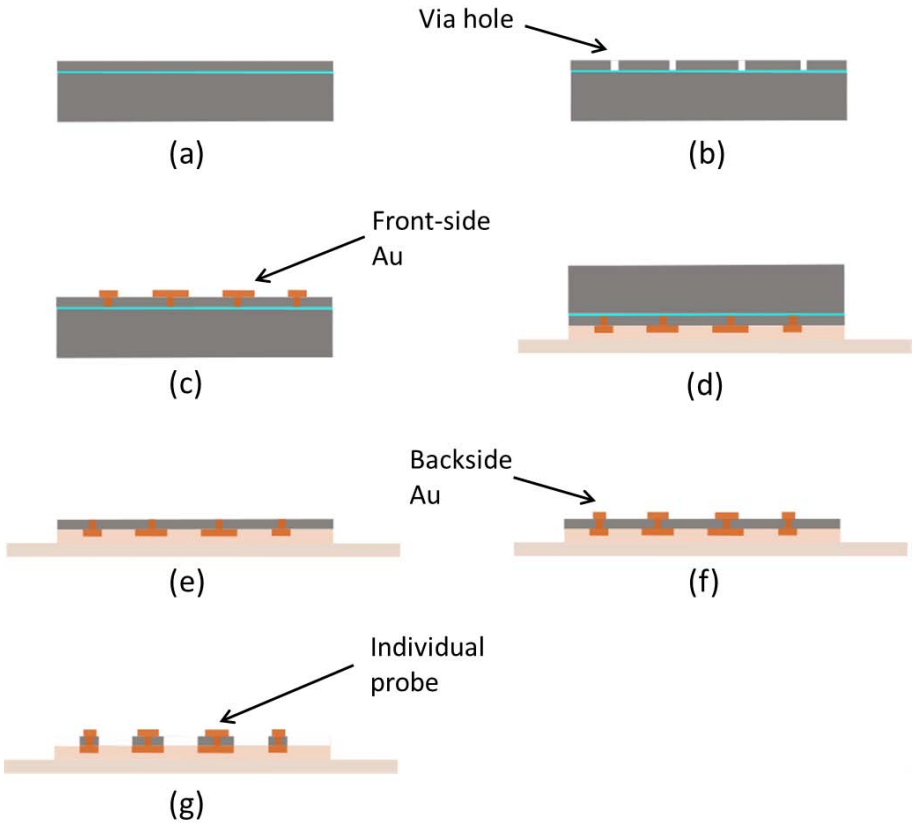

Figure 2.23: On-wafer probe fabrication processes flow using via-aided alignment scheme. (a) wafer cleaning, (b) via hole etch, (c) front-side plating gold circuit definition, (d) backside mounting of the SOI wafer, (e) the handle and the oxide layer removal, (f) backside plating gold circuit definition, (g) extents etch for probe contour definition.

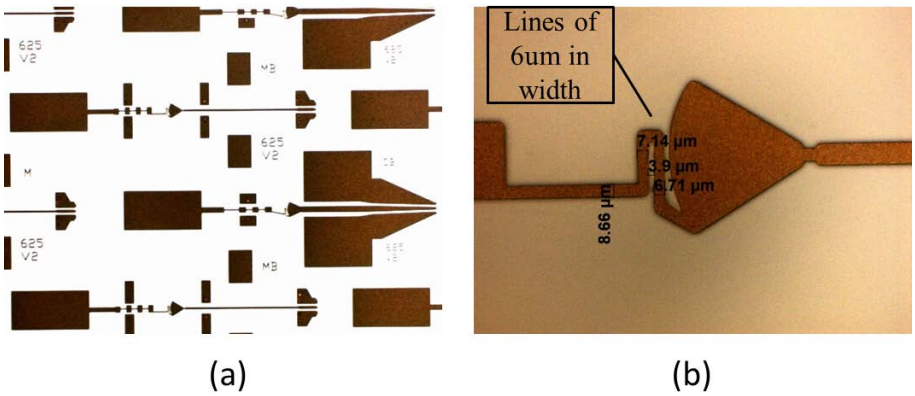

Figure 2.24: The plated front-side gold patterns using the via-aided alignment scheme.

Shown in Fig 2.23 is the new fabrication processes flow using etched via structures as alignment markers. On a clean SOI wafer, the via holes as well as alignment markers are first etched. The sidewall profiles shown in Fig 2.13 and 2.14 are typical of the etched vias and alignment markers. After seed layer deposition in Sputter3, the front-side plating lithography is then performed and gold features are plated as shown in Fig 2.24.

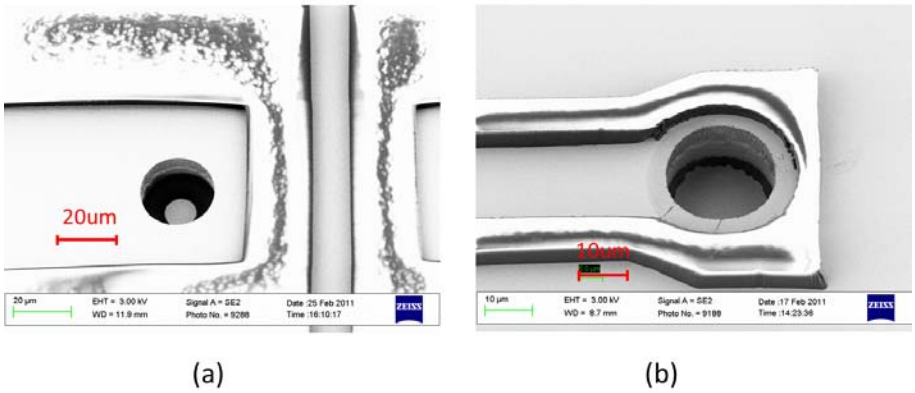

Figure 2.25: Residue photoresist inside via holes after front-side gold plating lithography.

As is similar to the backside gold plating lithography in the previous section, the front-side gold plating lithography with this new alignment scheme is complicated by the presence of the via holes. These via holes introduce regional variations in spin coated photoresist thickness, and make the extra photoresist inside the via holes not able to be developed by a normal dosage of UV exposure. Additionally, the front-side gold plating lithography has to resolve critical features as small as $6\mu m$ in width. These issues are again addressed by performing the lithography in three steps. The first step exposes and develops away photoresist at the edge of the wafer and over the alignment marker regions. The second step provides extra exposure to the via hole regions and develops away photoresist inside the vias with the aid of ultrasonic vibration. The third step defines the photoresist patterns for the front-side plating gold circuit. Shown in Fig 2.25 is the residue photoresist inside the via holes after the lithography, which has also been observed in backside gold plating lithography

with true backside alignment scheme. This residue photoresist can be cleaned by an oxygen plasma in the March cleaning tool. The front-side plated gold features typically come out well aligned to the via holes.

When the front-side processing is finished, the wafer is similarly mounted upside down to a carrier wafer. The wafer then goes through handle layer dicing, Si etch and oxide layer wet etch until the backside of the device layer is reached. It's now ready to start the backside processing.

Before the backside processes are started, a few comments can be made in regards to the via holes. As shown in Fig 2.14, the via holes seen from the backside are bright and shiny gold features in contrast to the darker Si background. The sharp images seen from optical lens greatly help with alignment. Additionally, the backside wafer surface is flat with the absence of $15\mu m$ deep vias and trenches, improving contact between the wafer substrate and the mask. A few images for backside gold plating lithography and the plated gold features are shown in Fig 2.26, which indicate excellent alignment being achieved.

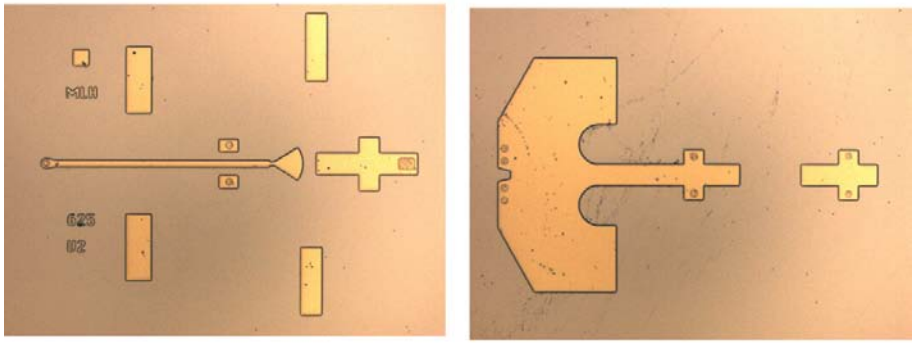

Figure 2.26: Backside plated gold features with via-aided alignment scheme.

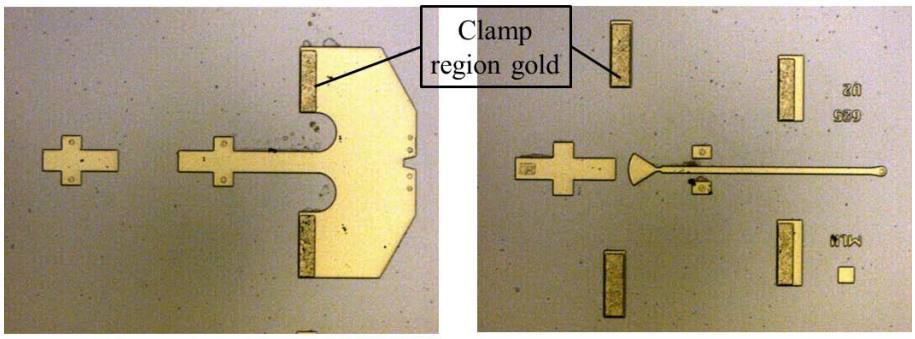

Figure 2.27: The plated clamp gold (dark rectangles on bright gold of the probes) that adds extra gold at the clamp regions.

A new step, the clamp gold plating, although not intrinsically connected to this new alignment process, is included in the processes flow for this new fabrication scheme. Experience with the previous on-wafer probes reveals that the two halves of the probe block does not fully close as designed. The probe inside the block is not firmly clamped by the block and moves slightly during the probing process. The clamp gold is designed to provide extra plated gold to the clamp regions to solve this issue, as well as to avoid thick gold features for both front-side and backside RF circuitry. They are large rectangular patterns on top of the backside gold features for mechanical clamping purposes, as shown in Fig 2.27. They provide enough thickness of gold in the clamp regions for the probe to be firmly clamped by the probe block when assembled.

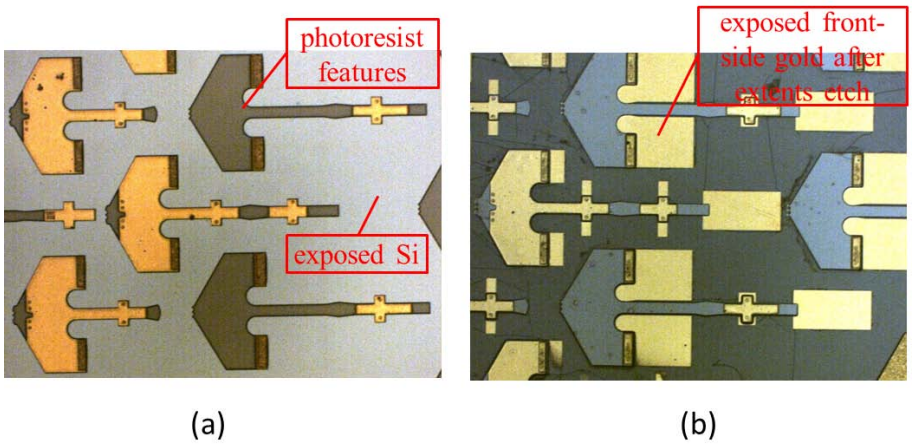

Figure 2.28: (a) Extents lithography that defines the probe contour and (b), (c) individual probes remaining on carrier wafer after the extents etch.

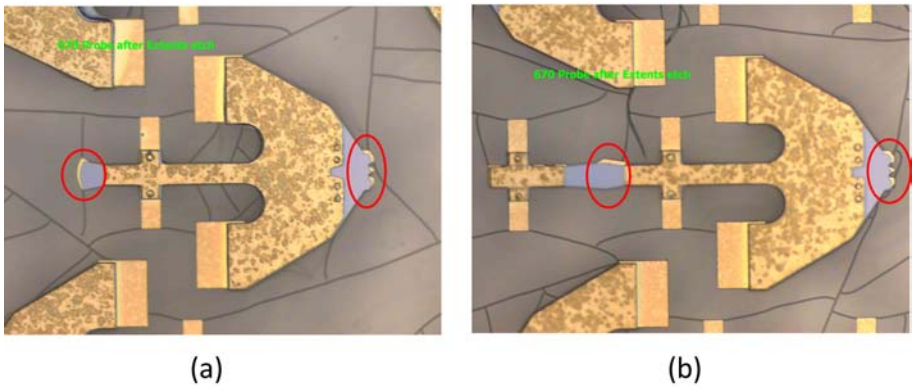

Figure 2.29: Feature distortion caused by misalignment between via etch lithography, extra via lithography and backside gold plating lithography with the true backside alignment scheme.

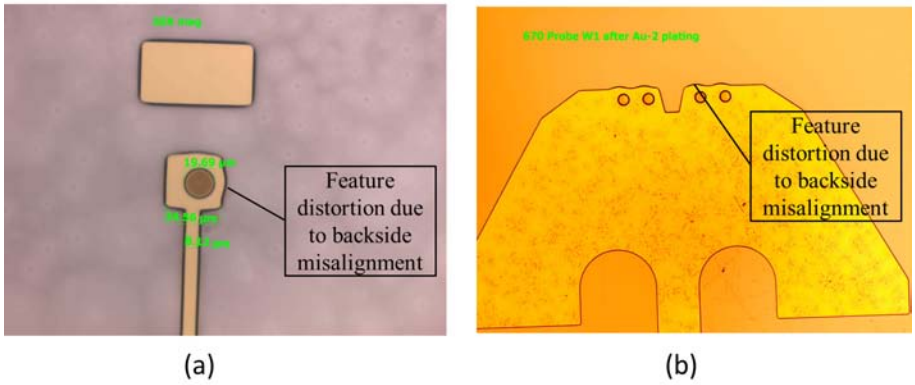

Figure 2.30: Misalignment between the front-side and backside features with the true backside alignment scheme.

The extents lithography is performed to define the probe contour using photoresist as the etch mask. After photoresist postbake and UV hardening, the wafer is then etched using the deep Si etch recipe. Individual probes remain on the wafer as shown in Fig 2.28. They are then released from substrate using TCE.

By switching to the via-aided backside alignment scheme for probe fabrication, a few important improvements are made. These improvements have greatly enhanced probe alignment precision as well as fabrication throughput. The first improvement is a significant reduction in backside processing difficulties by moving the via etch step to front-side. When the via hole etch is moved to the front-side of the wafer, fabrication difficulties are moved to the front-side processing. More time and efforts could potentially be saved if the wafer failure occurs at the front-side.

Another advantage brought about by moving the via etch to the front-side is the significant improvement in alignment precision for backside processes. As mentioned in previous section, the true backside alignment with the EVG tool suffers from unexpected misalignment uncertainties, as shown in Fig 2.29 and 2.30 for some typical backside alignment results. They include misalignment between via etch lithography, backside gold plating lithography, extents etch lithography and front-side features.

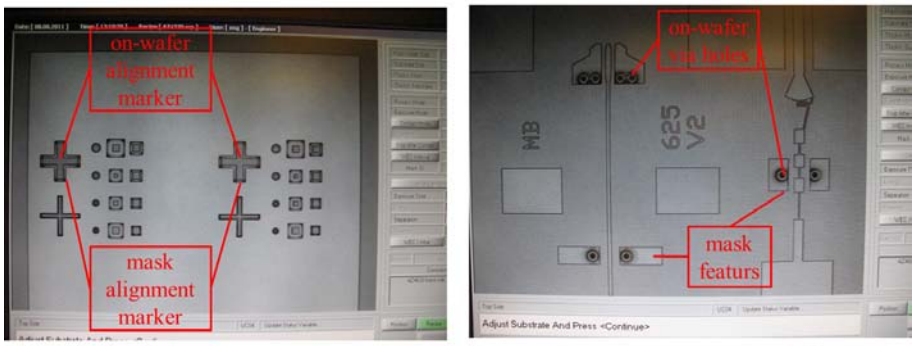

Figure 2.31: Images of alignment markers and wafer patterns seen through aligner's microscopes with via-aided alignment scheme.

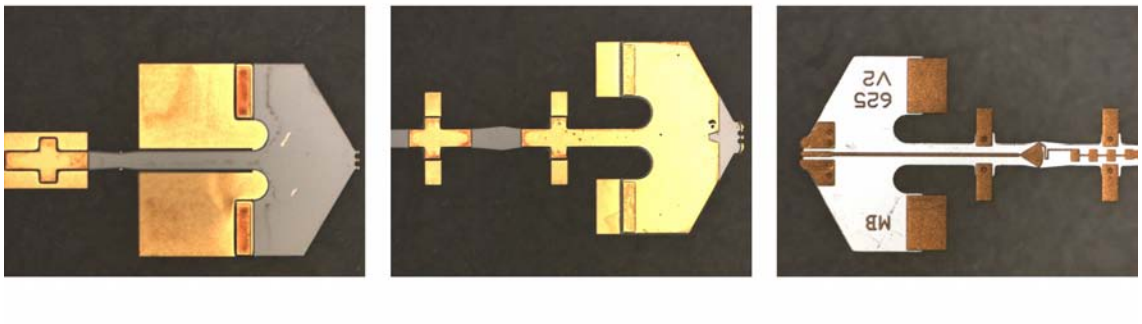

Figure 2.32: Typical alignment precision for front-side and backside features achieved with via-aided alignment scheme.

By using the via-aided alignment scheme, the front-side and backside alignment precision has been greatly improved. This is because either at the front-side or the backside of the SOI wafer, the lithography is performed effectively as a front-side alignment to the via holes. Additionally, the optical lens' positions are not fixed as required by the true backside alignment using the EVG aligner. This allows the operator to move the lens around and inspect alignment precision before UV exposure, as shown in Fig 2.31. By aligning to the via holes for each lithography, very good alignment between front-side patterns and backside patterns have been achieved, as demonstrated in Fig 2.32.

One additional important aspect about using the via-aided alignment scheme is that it does not require the use of transparent quartz carrier. During the first few

rounds of fabrication with the via-aided alignment scheme where a quartz carrier is still used, it is found during backside lithography that it's not possible to precisely align features at both edges of the wafer to the mask at the same time. Further tests reveal that the SOI wafer surface is bowed by a thermal mismatch between the quartz carrier wafer and the SOI wafer during backside mounting, which is the major factor for the radial misalignment seen later on. This problem is addressed by replacing the quartz carrier with a thick Si carrier wafer ($650\mu m$ to 1mm thickness being used). When a SOI wafer is mounted to the thick Si carrier wafer, its surface bow is reduced to $10\mu m$ height difference between wafer edge and wafer center point, from about $60\mu m$ when mounted to a quartz carrier. This has greatly improved overall alignment across the wafer. Reduction in the SOI wafer surface bow has also improved the overall alignment.

Shown in Tab 2.1 are the tabulated values of typical misalignment achieved using the two different alignment schemes. As can be seen from the tabulated values, the alignment precision has been greatly enhanced with the improved via-aided alignment scheme. When the lithography masks are being designed and fabricated, the misalignment tolerances between the backside features are typically set to be $5\mu m$, and the misalignment tolerances between the backside gold features and the via holes are set to be $10\mu m$. The typical misalignment values achieved by the true backside alignment scheme are exceeding the design tolerances, which is the primary reason for misalignments shown in Fig 2.21 and 2.30. The alignment precision is greatly enhanced with the improved via-aided alignment fabrication processes. The misalignment between the front-side and backside features are typically below $5\mu m$, caused by accumulation of misalignment when both the front-side and backside features are aligned to the via holes within a certain precision level. When the front-side features are aligned within $1\mu m$ precision to the via holes and the backside features are aligned within $2\mu m$ precision to the via holes, the accumulated misalignment between the front-side and backside features could accumulate to be $3\mu m$. The residual curvature of the SOI

wafer surface caused by thermal mismatch during the backside mounting, although has been greatly improved by switching to Si carrier from the previous quartz carrier, also contributes to a few microns of radial misalignment. The alignment precision can be further improved by improving alignment precision at the backside (using EVG aligner for better alignment precision, reducing photoresist topology to get better alignment contact, etc.) and reducing the SOI wafer surface curvature after the backside mounting (try lower temperature for epoxy curing, using even thicker Si carrier wafer, etc.).

True Backside Alignment Scheme		Via-aided Alignment Scheme	
Between front-side and backside features	between backside features	Between front-side and backside features	between backside features
$10\mu m$	$10\mu m$	$5\mu m$	$2\mu m$

Table 2.1: Typical misalignment values for fabricated on-wafer probes using two different alignment scheme.

2.5 Repeatability and Reliability of On-wafer Probes

In previous sections, SOI processing techniques are described and improved to fabricate on-wafer probes at various waveguide bands. On-wafer probes covering frequencies ranging from 140 GHz to 1.1 THz have been made commercially available by this fabrication technology[39, 41]. These on-wafer probes are assembled in a micromachined metallic split block[38, 19], which houses an E-plane split-waveguide connected to the waveguide output of the VNA. The probe chip is dropped in the micromachined channel for assembly, using the channel as well as the clamp regions to realize probe-to-block alignment, as shown in Fig 2.33. When the two halves of the blocks are assembled, the probe is firmly clamped by the probe block.

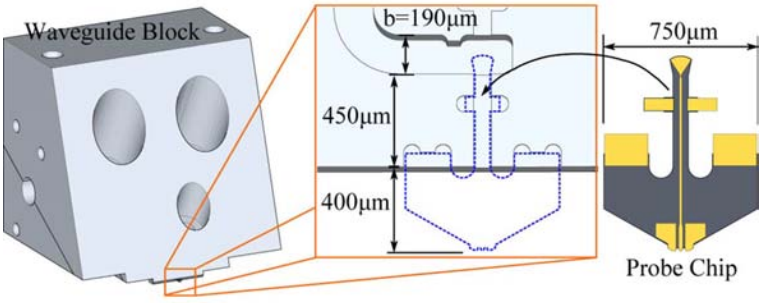

Figure 2.33: On-wafer probe being assemble in the metallic block[3].

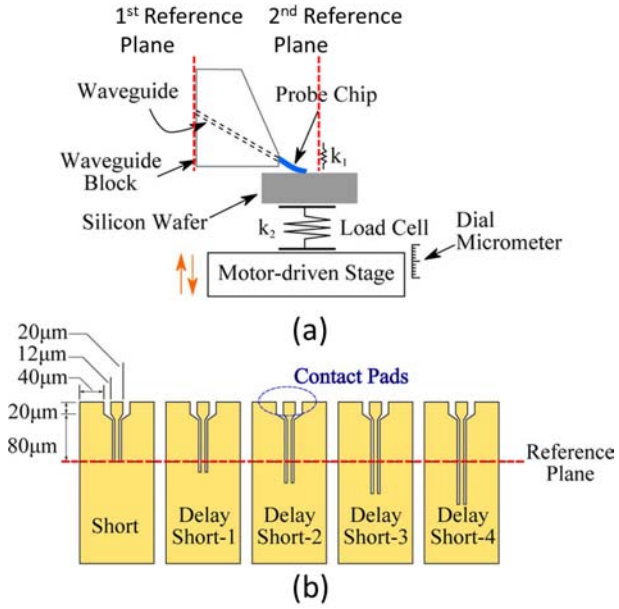

Figure 2.34: (a) A schematic of the probe station being used for WR1.5 waveguide band on-wafer probe characterization, (b) delayed short standards for WR1.5 waveguide band on-wafer probe characterization[3].

After probe assembly, the block is attached to the waveguide port of the VNA (Rohde Schwarz ZVA-40 with VDI WR1.5 VNAXTXRX frequency extender). A pre-fabricated calibration substrate is used to characterize the RF performance of the on-wafer probe. The calibration substrate is placed on a spring load cell (FUTEK model FSH0234) that sits on the motor driven stage (Newport MFA-CC model motor stage) to move horizontally and vertically. The motor driven stage moves the calibration substrate up into contact with the probe tips, bending the probe to generate

a contact force that can be read by the load cell. In order to overcome rotational misalignment between the probe tips and the substrate, an overdue contact force of 20mN is typically used to ensure good electrical contact. A schematic of the probing system is shown in Fig 2.34(a).

The on-wafer probe is characterized in two steps. The first step is a waveguide calibration putting the reference plane to the waveguide output port of the VNA. The second step is on-wafer calibration putting the reference plane a distance away from the CPW contact pads, as shown in Fig 2.34(b) for WR1.5 waveguide band probe calibration substrate. The one-port, two-tier calibration algorithm can be used to compute the S-parameters of the on-wafer probe[3, 19].

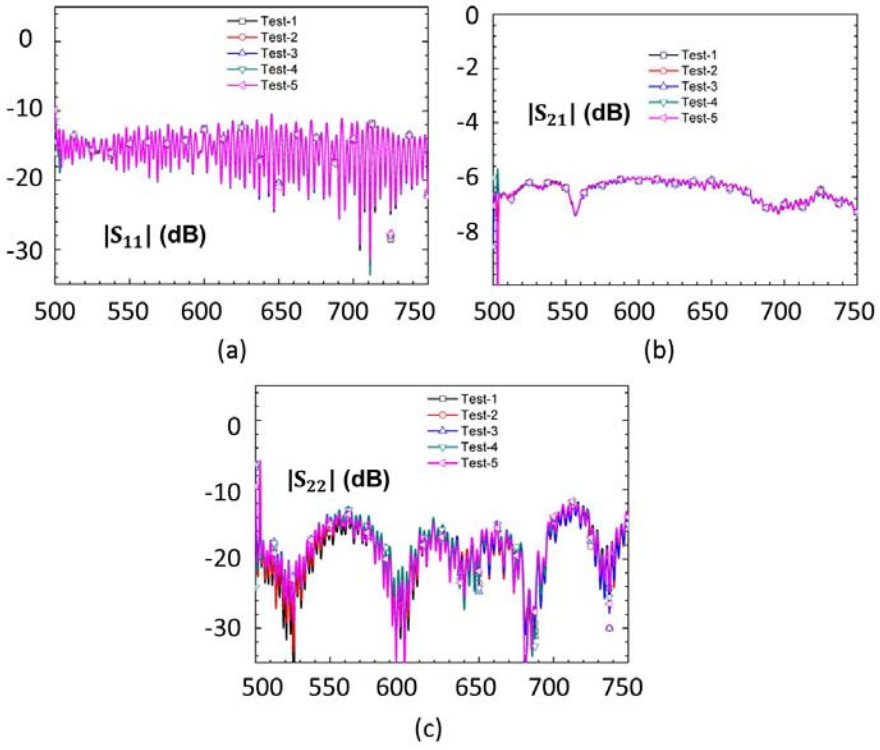

Figure 2.35: Measured S-parameters of the same probe five separate times. (a) Magnitude of S_{11} (waveguide port). (b) Magnitude of S_{21}. (c) Magnitude of S_{22} (CPW port)[3].

With the experimental setup and mathematical algorithm ready for on-wafer probe characterization, the repeatability and reliability of the probe RF performance is evaluated for the WR1.5 waveguide band probe[3]. These tests were performed as a

collaborative teamwork with former PhD student Lihan Chen, with results published in [3]. For the repeatability test, the probe is first used to measure each of the calibration standards five different times. Then the probe S-parameters can be computed five different times using these measurements. The characterized S-parameters are plotted in Fig 2.35. This repeatability test evaluates the impact of the landing positioning errors on the characterized results of the probe. The oscillation in S_{11} is due to a waveguide mismatch at the block waveguide interface. Overall, the characterized S-parameters from these five independent measurements track each other very tightly. The difference in the magnitude of S-parameters caused by probe positioning uncertainty is very low.

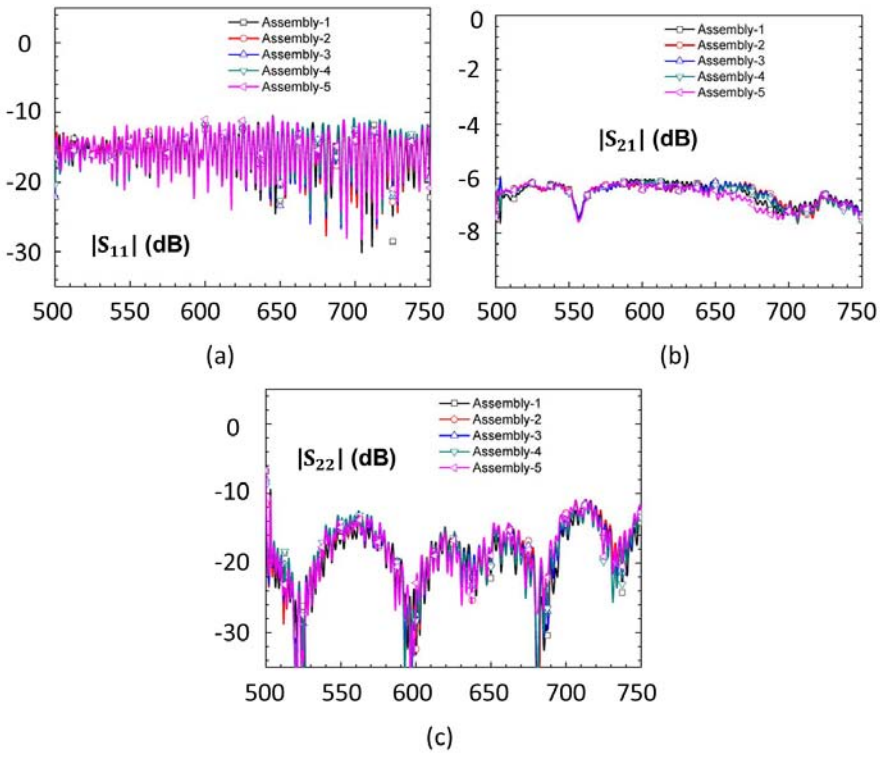

Figure 2.36: Measured S-parameters of the same probe assembled in the same metallic block five separate times. (a) Magnitude of S_{11} (waveguide port). (b) Magnitude of S_{21}. (c) Magnitude of S_{22} (CPW port)[3].

The same probe chip is then assembled in the metallic block five different times, and the S-parameters of the probe after each assembly is independently characterized.

This process evaluates the impact on probe RF performance brought about by the probe-to-block alignment uncertainty during each assembly. The precision machining tolerance for the metallic block is $\pm 5\mu m$. This gives the probe ample room to adjust itself when dropped in the channel for assembly. The slight difference in probe-to-block alignment for each assembly will result in changes in the probe S-parameters. As is demonstrated in Fig 2.36, the discrepancy in the S-parameters of the on-wafer probes from each assembly is significantly larger than that shown in Fig 2.35. This probe RF performance difference among different assemblies will not affect DUT measurement uncertainty if the probe is characterized after each assembly.

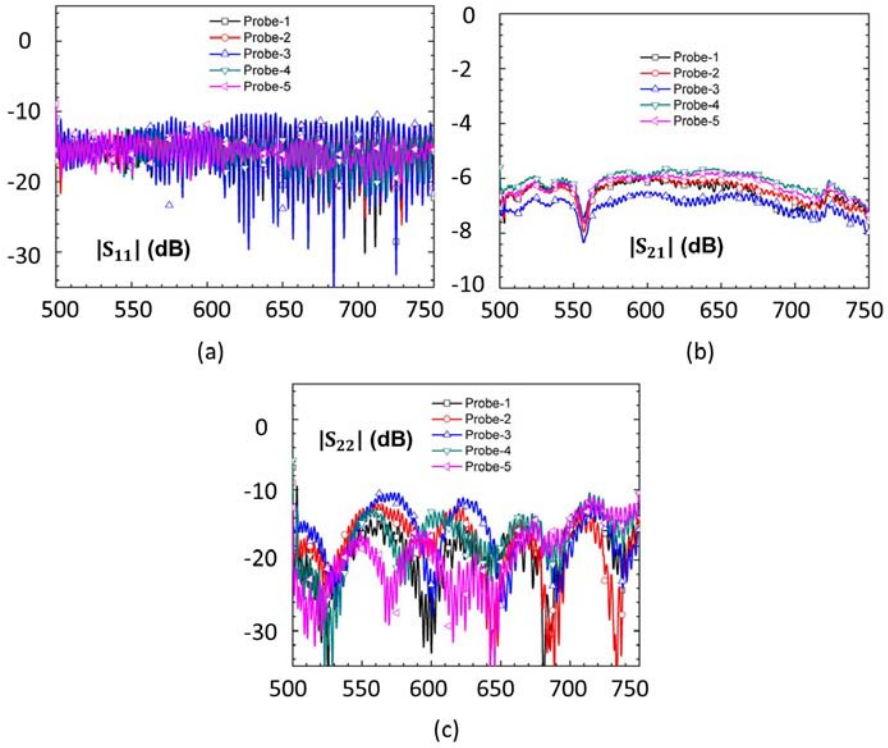

Figure 2.37: Measured S-parameters of five different probes. (a) Magnitude of S_{11} (waveguide port). (b) Magnitude of S_{21}. (c) Magnitude of S_{22} (CPW port)[3].

The last part of the probe repeatability test is to evaluate the variation in RF performance for probes fabricated in the same run. Five probes of the same design and from the same fabrication run are assembled to the same block and characterized, with the S-parameters plotted in Fig 2.37. The discrepancy in S-parameters between

different probes is significantly larger than that in previous figures. This extra discrepancy is caused by probe variations during fabrication processes. Nevertheless, the probe has consistently achieved better than 10dB for return loss. The variation of the insertion loss is below 1dB. This probe RF performance difference among different probes will not affect DUT measurement uncertainty neither, if the probe is characterized after each new probe assembly.

Pobe reliability test is also performed to evaluate the degradation of probe RF performance over usage wear. In order to do this, the probe is brought into contact with the substrate at 20mN contact force for multiple times by the automated motor stage. After each 1,000 contacts, the probe is characterized using the delayed short standards. SEM images of the probe tips area are also taken. With these measurements and images, the degradation of probe RF performance as well as the dilapidation of mechanical structure can be tracked.

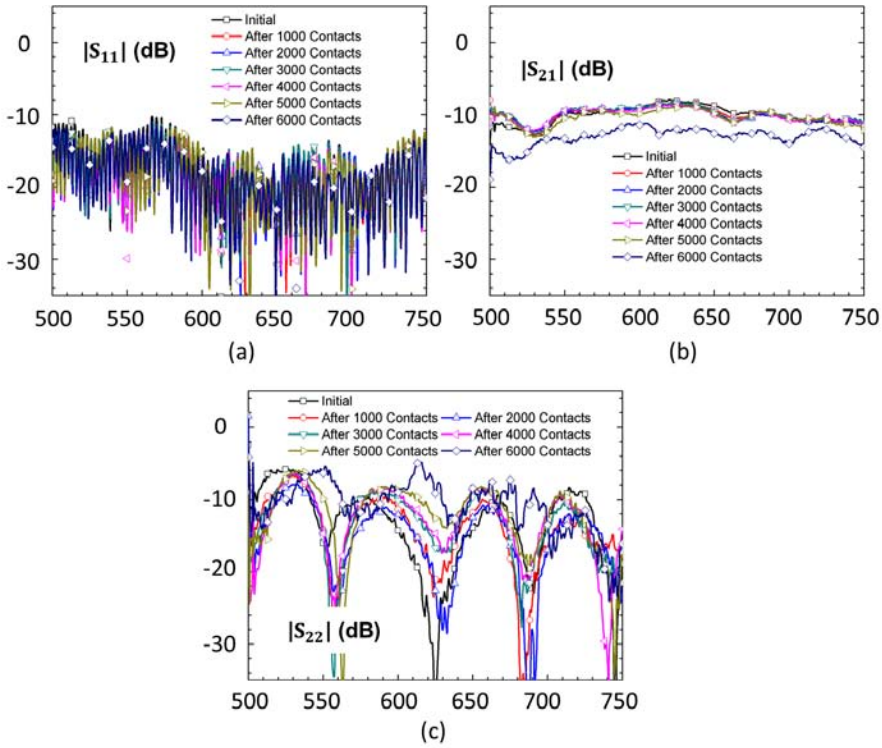

Figure 2.38: Measured S-parameters for a probe with soft gold tips after different number of contacts. (a) Magnitude of S_{11} (waveguide port). (b) Magnitude of S_{21}. (c) Magnitude of S_{22} (CPW port)[3].

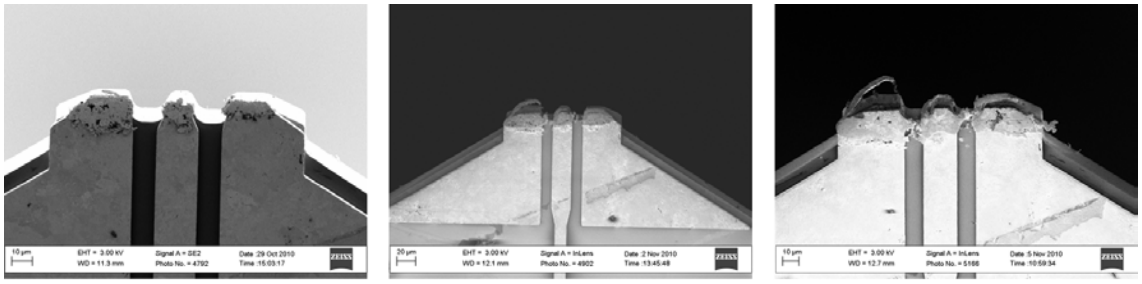

Figure 2.39: SEM images of the probe tip area for a probe with soft gold tips after different number of contacts, (a) 10 contacts, (b) 3,000 contacts, (c) 6,000 contacts[3].

The reliability test is first performed with soft gold probes contacting with soft gold substrate (plated gold on Si substrate). High purity gold is typically used as electrical interconnect in the semiconductor industry for its superior electrical conductivity and chemical inertia to oxidation. However, probe tips plated with high purity gold are relatively soft and delapidate quickly. The soft gold material at the probe tips quickly deforms as contact cycles continue, accumulates in the gaps of the CPW transmission line and eventually leads to probe failure when enough gold debris in the gaps causes electrical short. This electrical and mechanical degradation process is shown in Fig 2.38 and 2.39.

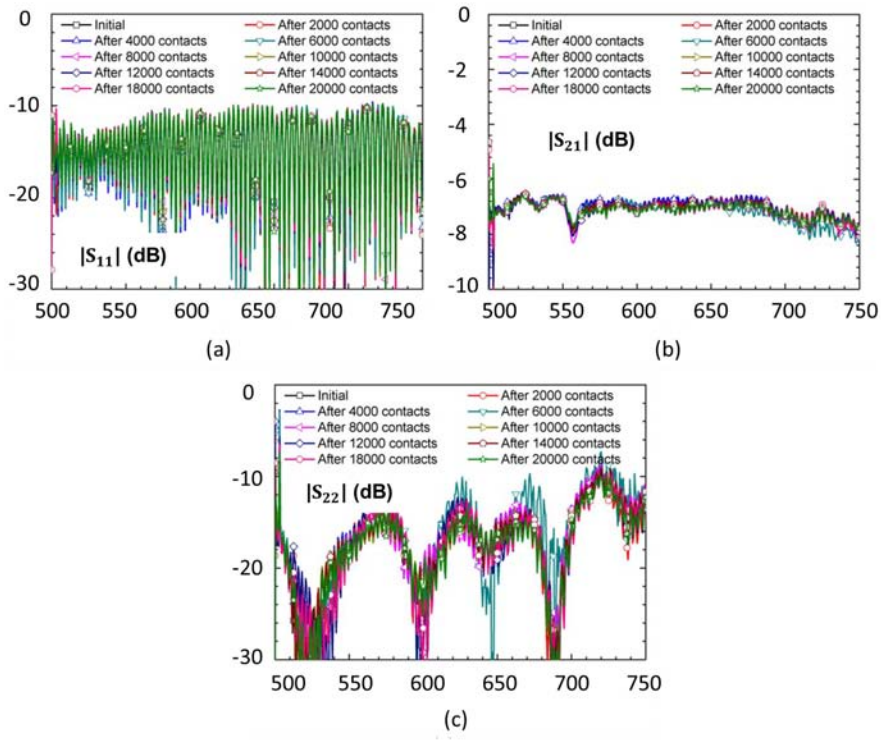

Figure 2.40: Measured S-parameters for a probe with hard gold tips after different number of contacts. (a) Magnitude of S_{11} (waveguide port). (b) Magnitude of S_{21}. (c) Magnitude of S_{22} (CPW port)[3].

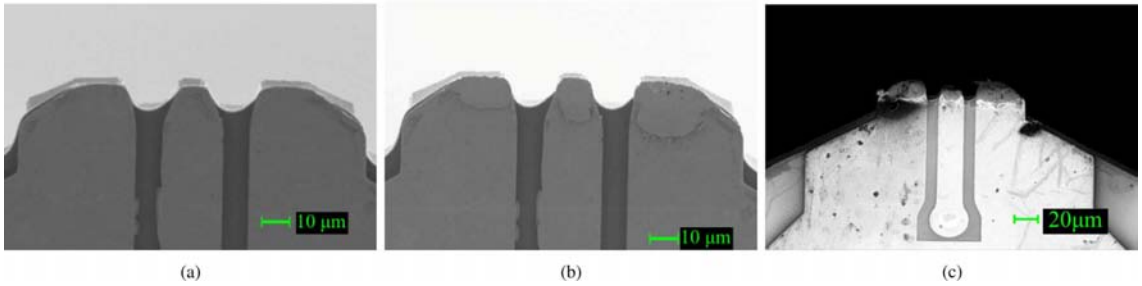

Figure 2.41: SEM images of the probe tip area for a probe with hard gold tips after different number of contacts, (a) 10 contacts, (b) 2,000 contacts, (c) 20,000 contacts[3].

Technic Inc offers hard gold plating solution Orosene 990 HS that adds cobalt dopant to the high purity gold. It has better than twice the hardness of the soft gold material, and can significantly improve the mechanical durability of the gold material. In order to improve the probe lifetime, hard gold is plated to the front-side of the probe, including the probe tips. Then the reliability test is performed with the hard gold probe by bringing it into contact with quartz carrier wafer at 20mN contact

force for multiple times. The hard gold probe has demonstrated superior longevity in the reliability test, and is not seen to degrade much mechanically or RF-wise after 20,000 contact cycles, as shown in Fig 2.40 and 2.41.

In this chapter, SOI processing techniques are described for the fabrication of GSG on-wafer probes. Significant improvements have been been made to enhance alignment precision and fabrication throughput. The on-wafer probes fabricated using these techniques demonstrate superior electrical and mechanical properties. They have been tested to exhibit repeatable RF characteristics. Further improvement in manufacturing procedures has also improved their lifetime for on-wafer characterization applications. Based on this fabrication technology developed in this dissertation, on-wafer probes have been extended to wider frequency ranges and are now commercially available from 140 GHz to 1.1 THz[41].

With this success in GSG on-wafer probes, a balun integrated probe for differential circuits on-wafer characterization is proposed. This will be the focus of discussion for the following few chapters.

Chapter 3

Fundamental Theories for Microwave Differential Circuits

3.1 Benefits of Using Differential Configuration for MMIC

Balanced transmission lines have found important applications in telecommunication industry and audio systems for a long time. They compose of two identical lines that are twisted together to transimit differential signals. Electrical noises that deteriorate the sound clarity of acoustic signals usually affect both of the signal lines in the same way, inducing a common mode noise signal. This common mode noise is eventually removed when the signals are fed into a differential amplifier by taking the difference of the two. These twisted pair balanced transmission lines offer superior performance in rejecting common-mode noise and maintaining good sound quality.

With the rapid advancement of the semiconductor industry and the ever-increasing density of devices on a single wafer chip, differential circuits are also gradually finding their ways in applications in the microwave and terahertz integrated circuits. In recent years, there have been a myriad of Millimeter-wave Monolithic Integrated Circuit (MMIC) and Submillimeter-wave Monolithic Integrated Circuit (SMMIC) being implemented in differential configurations, including differential attena, amplifier, LNA, mixer and VCO[33, 34, 35, 36, 37]. They are preferred over similar devices of single-ended configuration because of a few important reasons.

The first reason is that differential circuits offer superior performance in terms of noise rejection, for the same reason it is used in telecommunication and audio systems. External noises typically affect both branches in the same way when the differential circuit is properly designed with good symmetry. The common mode signal induced by external noises will be eventually removed as the difference of the signals is used. This particular feature with differential circuits has made it especially popular in Low Noise Applifier (LNA) design.

The second benefit of the differentially configured devices is that they offer superior immunity to ground plane variations caused by interconnect discontinuities. As today's high speed electronics is being scaled to higher and higher frequencies, the electromagnetic wavelength is becoming smaller and smaller. This poses a great problem for microwave integrated circuits designers in that the interconnect discontinuities such as wire bonding and ball soldering have an unnegligible electrical length. For conventional single-ended circuits, these interconnect discontinuities will lead to variations in the voltages of the ground plane that is difficult to simulate. In a differential system, however, the signals can be referenced to the symmetry point as a virtual ground, with no need to incorporate an actual ground plane that is affected by unknown factors. This advantage with the differential circuits greatly alleviates the difficulties brought about by interconnect discontinuities in designing higher frequency devices.

Another obvious benefit brought about by the differential configuration is the 6 dB increase in output power level at a given operating voltage. Power efficiency requirements in today's digital integrated circuits are pushing down the operating voltage of the circuits, but the power consumption and operating voltage of relevant analog circuits can not be simply scaled down similar to digital circuits. A decrease in the voltage of analog circuits must be compensated by an increase in the circuit current to keep a constant power level fed into a given load. Converting the single-ended circuit into differential configuration offers the opportunity to decrease the

operating voltage by a factor of two under the same current. In applications where voltage scaling down is not preferred, the double swing of the voltage offers higher dynamic range for the system.

Another less referenced advantage with differential circuits is improved nonlinear even-order distortion, as illustrated in Fig 3.1[42]. A differential amplifier can be seen as composed of two identical single-ended amplifiers with a differential input signal. For each single-ended amplifier, the output signal is a nonlinear function of the input signal that can be written in the following harmonic terms, as shown in Fig 3.1, under Taylor series expansion. The output differential signal takes the difference of the two output branches, canceling out the even-order terms. This leads to an improved even-order distortion.

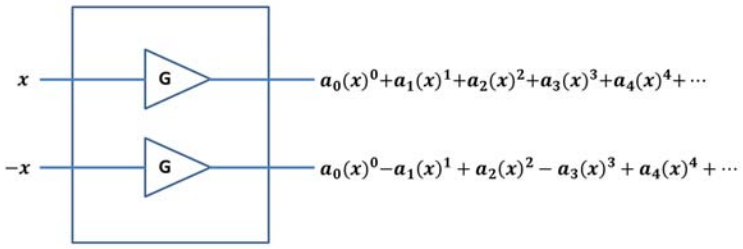

Figure 3.1: Nonlinear even-order improvement with differential circuits.

3.2 Mixed-mode S-parameters and Differential Circuits Characterization

Differential circuits are typically described using mixed-mode s-parameters developed in the mid 1990s. Like the conventional single-ended s-parameters, the mixed-mode s-parameters can be used to describe linear relationships between the electrical stimuli at multiple ports. Unlike the conventional single-ended s-parameters, the mixed-

mode s-parameters have one extra dimension for the mode specific excitations at the differential ports. For typical 3 port and 4 port differential circuits, shown below in Fig 3.2, the corresponding mixed-mode s-parameters are shown in Eq 3.1 and 3.2[42].

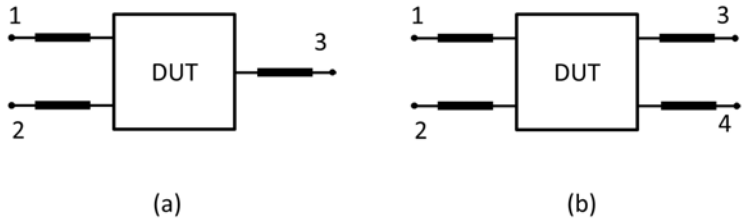

Figure 3.2: (a) A three port differential network, (b) a four port differential network.

$$\begin{pmatrix} b_d \\ b_s \\ b_c \end{pmatrix} = \begin{pmatrix} S_{dd} & S_{ds} & S_{dc} \\ S_{sd} & S_{ss} & S_{sc} \\ S_{cd} & S_{cs} & S_{cc} \end{pmatrix} \cdot \begin{pmatrix} a_d \\ a_s \\ a_c \end{pmatrix} \tag{3.1}$$

$$\begin{pmatrix} b_{d1} \\ b_{d2} \\ b_{c1} \\ b_{c2} \end{pmatrix} = \begin{pmatrix} S_{dd11} & S_{dd12} & S_{dc11} & S_{dc12} \\ S_{dd21} & S_{dd22} & S_{dc21} & S_{dc22} \\ S_{cd11} & S_{cd12} & S_{cc11} & S_{cc12} \\ S_{cd21} & S_{cd22} & S_{cc21} & S_{cc22} \end{pmatrix} \cdot \begin{pmatrix} a_{d1} \\ a_{d2} \\ a_{c1} \\ a_{c2} \end{pmatrix} \tag{3.2}$$

A linear relationship exists between the conventional single-ended s-parameters and mixed-mode s-parameters. For a 3 port and 4 port network, the linear transform relationship is shown below in Eq 3.3 and 3.4[42].

$$\begin{pmatrix} S_{dd} & S_{ds} & S_{dc} \\ S_{sd} & S_{ss} & S_{sc} \\ S_{cd} & S_{cs} & S_{cc} \end{pmatrix} = \begin{pmatrix} \frac{(S_{11}-S_{12}-S_{21}+S_{22})}{2} & \frac{(S_{13}-S_{23})}{\sqrt{2}} & \frac{(S_{11}+S_{12}-S_{21}-S_{22})}{2} \\ \frac{(S_{31}-S_{32})}{\sqrt{2}} & S_{33} & \frac{(S_{31}+S_{32})}{\sqrt{2}} \\ \frac{(S_{11}-S_{12}+S_{21}-S_{22})}{2} & \frac{(S_{13}+S_{23})}{\sqrt{2}} & \frac{(S_{11}+S_{12}+S_{21}+S_{22})}{2} \end{pmatrix} \tag{3.3}$$

$$\begin{pmatrix} S_{dd11} & S_{dd12} & S_{dc11} & S_{dc12} \\ S_{dd21} & S_{dd22} & S_{dc21} & S_{dc22} \\ S_{cd11} & S_{cd12} & S_{cc11} & S_{cc12} \\ S_{cd21} & S_{cd22} & S_{cc21} & S_{cc22} \end{pmatrix} =$$

$$\begin{pmatrix} \frac{(S_{11}-S_{21}-S_{12}+S_{22})}{2} & \frac{(S_{13}-S_{23}-S_{14}+S_{24})}{2} & \frac{(S_{11}-S_{21}+S_{12}-S_{22})}{2} & \frac{(S_{13}-S_{23}+S_{14}-S_{24})}{2} \\ \frac{(S_{31}-S_{41}-S_{32}+S_{42})}{2} & \frac{(S_{33}-S_{43}-S_{34}+S_{44})}{2} & \frac{(S_{31}-S_{41}+S_{32}-S_{42})}{2} & \frac{(S_{33}-S_{43}+S_{34}-S_{44})}{2} \\ \frac{(S_{11}+S_{21}-S_{12}-S_{22})}{2} & \frac{(S_{13}+S_{23}-S_{14}-S_{24})}{2} & \frac{(S_{11}+S_{21}+S_{12}+S_{22})}{2} & \frac{(S_{13}+S_{23}+S_{14}+S_{24})}{2} \\ \frac{(S_{31}+S_{41}-S_{32}-S_{42})}{2} & \frac{(S_{33}+S_{43}-S_{34}-S_{44})}{2} & \frac{(S_{31}+S_{41}+S_{32}+S_{42})}{2} & \frac{(S_{33}+S_{43}+S_{34}+S_{44})}{2} \end{pmatrix} \quad (3.4)$$

There are a few different methods for differential DUT characterization. The first way is to take the differential circuit as a multiport single-ended network and measure the s-parameters without applying true mixed mode signals. The measured single-ended s-parameters will then be mathematically converted into mixed mode s-parameters using Eq 3.3 and 3.4. This approach for differential circuit characterization is relatively easy and does not require any advanced testing equipment. However, it has the inherent drawback that no truly differential or common mode signal is applied at the DUT testing ports, which is different from the way the DUT is designed to operate. In most applications, especially in the characterization of passive linear circuits such as differential filters, attenas and baluns, this approach is precise enough. However, there has been concerns when this approach is applied to active devices such as differential VCOs, mixers and LNAs, especially for large signal measurements at their nonlinear region. The differential active device's response to single-ended stimuli can be drastically different from that of a differential stimuli, as shown in Fig 3.3[4].

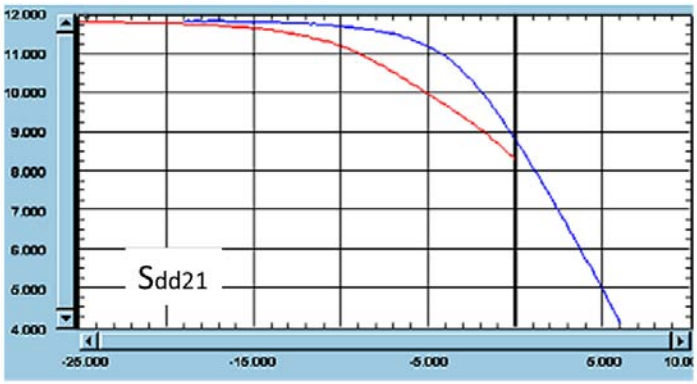

Figure 3.3: Power sweep measurement results for a differential amplifier using true mode (blue) and single-ended (red) measurement techniques. Horizontal axis represents input power, vertical axis represents differential gain[4].

A second method for differential circuit testing at frequencies below 110 GHz is to use the four-port dual-source VNA that is commercially available from Rohde & Schwarz and Agilent Technologies. These four-port VNA models come with dual sources installed and have the capability of tuning the phase and amplitude differences between these two sources at very high accuracy. By calibrating to the test ports' reference planes, the phase and amplitude mismatch at the test ports can be automatically adjusted to achieve truly differential and common mode signals, or any arbitrary phase and amplitude difference as desired. But the issue with dual-source four-port VNA is that they are available only up to 110 GHz for balanced measurements. The VNAs themselves can be used at higher frequencies up to terahertz with additional external frequency extenders, but these frequency extenders require connection to both sources of the VNA, eliminating the availability of an independent second source. Thus the balanced measurement capability is lost with the use of frequency extenders. There are also issues with residue phase errors. The VNA is able to automatically adjust for phase errors caused by port mismatches, but is not able to eliminate the residue phase errors coming from the frequency synthesizers, as shown in Fig 3.4 (the horizontal axis in Fig 3.4(b) should be GHz, as confirmed by Agilent technical expert). This inherent drawback in the hardware becomes more

severe at higher frequencies and limits the precision of achievable truly differential or common mode signal[5].

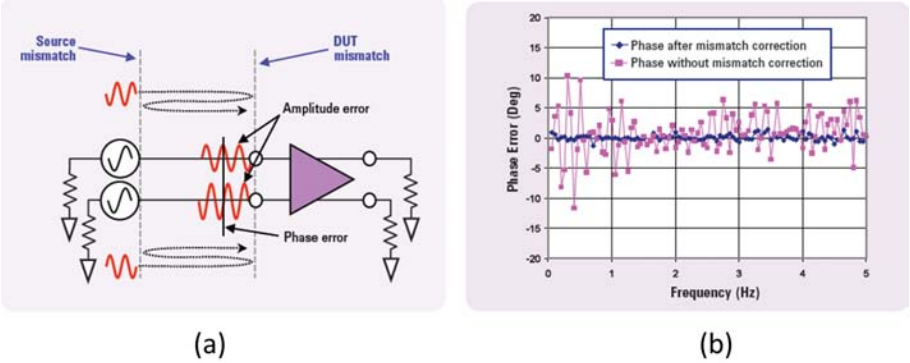

Figure 3.4: (a) Amplitude and phase imbalance caused by port mismatch, (b) mismatch correction functionality built in Agilent PNA-X series for reducing phase errors[5].

The third option for balanced measurements is to construct a pure mode VNA (PMVNA) using external phase shifting components[6, 43]. A typical PMVNA employs a waveguide switch and magic T to switch between differential and common mode operation, as demonstrated in Fig 3.5. The differential or common mode signal generated from the magic T is then passed through phase shifters that are used to cancel any additional phase imbalances before being fed into a GSGSG configurated dual probe. While offering the capability of fully characterizing both the differential and common mode components of the differential DUT, this method has found limited applications because of the bulky overhead, expensive upfront investment, and limited bandwidth. The apparatus shown in Fig 3.5 also lacks the capability to adjust for amplitude imbalance caused by asymmetry in waveguide connections in the two signal paths.

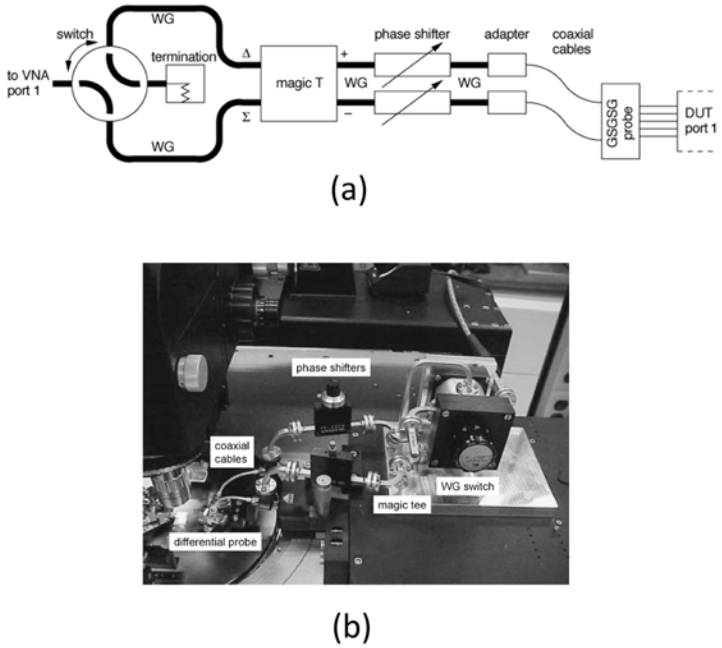

Figure 3.5: (a) Schematic of a pure-mode VNA, (b) a fully constructed pure-mode VNA[6].

A more recent development to provide an easy-to-operate, affordable, high precision and broad band characterization approach for differential DUT is to use the balun-integrated probes. A balun is a three port structure that converts a single-ended signal into differential signal, or vice versa. A balun-integrated probe can thus eliminate the bulky waveguide devices required for a pure mode VNA, reducing operational cost and upfront investment. A balun-integrated probe converts a single-ended signal from the VNA to a differential mode signal at probe tips, which is then applied on-wafer to DUT's reference planes directly, avoiding the extra amplitude and phase imbalances due to additional connections and transitions. Fig 3.6 illustrates how balun probes are used to perform a two-port characterization of a differential DUT. A single-ended signal from VNA port 1 is fed into the balun probe and is converted into a differential signal, which is applied on the DUT input port. The reflected differential signal from the DUT is picked up by the same balun probe, converted back into the single-ended signal and measured by the VNA. Another balun probe

on the right picks up the output differential signal at the other port of the DUT, and converts it into single-ended signal to be measured by the VNA. By performing such two-port measurements, the differential component of the DUT can be characterized. However, this also introduces another issue with respect to characterization uncertainty. This balun-integrated probe approach ignores common mode and cross mode signal paths which will contribute to characterization uncertainty. Its impact will be discussed in the following section.

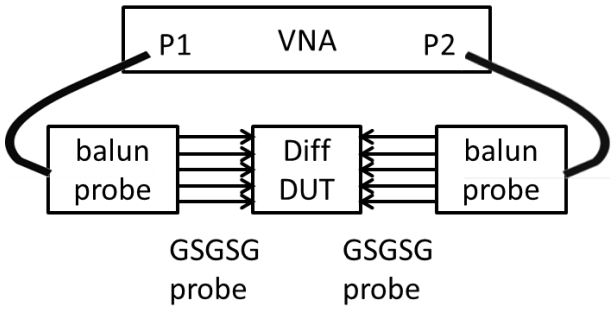

Figure 3.6: Balun-integrated probes for differential DUT characterization.[7]

An electrically repeatable and mechanically robust GSG probe for high frequency on-wafer characterization has been demonstrated in the previous chapter, fabricated using a novel SOI processing technique developed at the UVML. The aim of the following sections is to integrate a wide band balun structure with the current W-band GSG probe. The balun integrated probe can be used to facilitate differential microwave integrated circuits characterization.

3.3 Balun Integrated Probe Measurement Uncertainties

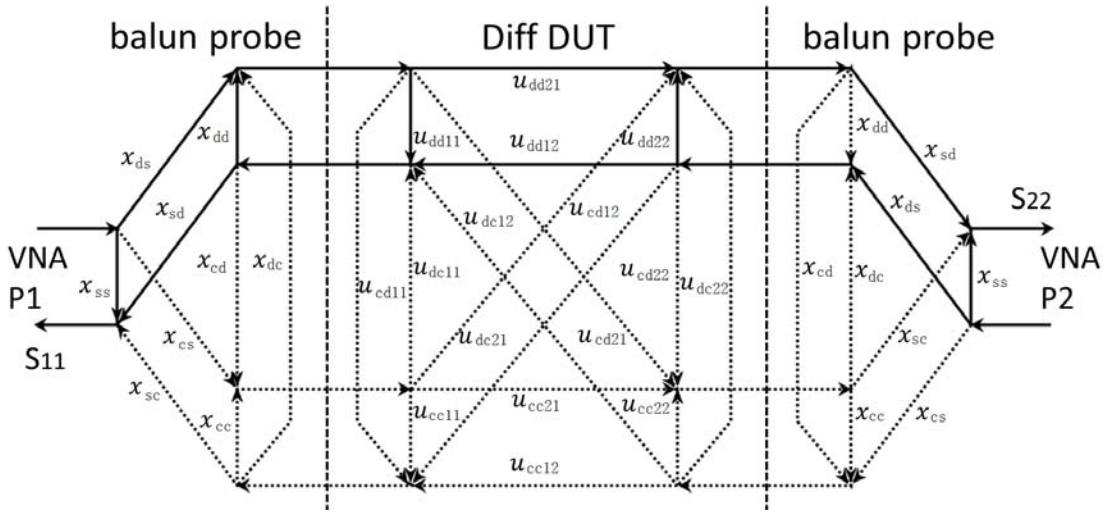

Figure 3.7: The signal flow graph of differential DUT characterization.

The balun integrated probe provides an easy, fast and cost effective way to characterize the differential devices. However, what comes with these advantages is a compromise in characterization accuracy. With the balun probe, only the 2×2 differential component s-parameters are characterized, instead of the full 4×4 s-matrix. Shown in Fig 3.7 is the signal flow diagram for differential DUT characterization using two identical balun probes, with the dominant differential branch of signal flow highlighted by dark lines. The balun integrated probe characterization method effectively assumes that the signal will go completely through the differential path, ignoring the common mode and cross mode signal flow branches in grey. In reality however, the signal will go through all possible paths in the diagram. Besides, the balun integrated probe is imperfect in that a small amount of common mode signal is generated together with the dominant differential mode signal. This undesirable common mode signal will further contribute to signal flow in the common mode and cross mode branch. Failure to include this into consideration causes measurement uncertainties that can not be backed out in the posterior mathematical manipulation.

As a result of the intrinsic drawback of using balun integrated probes for differential DUT characterization, the characterization accuracy is compromised. Measurement uncertainty simulation is performed to evaluate how the balun probe's performance could affect the characterization errors for a given differential DUT characterized by given balun probes. For the signal flow graph shown in Fig 3.7, a two port measurement can be performed by the VNA that is calibrated to the single-ended ports of the balun probes, with measurements $[S]$ (2×2 matrix $\begin{pmatrix} S_{11} & S_{21} \\ S_{12} & S_{22} \end{pmatrix}$). These measured results are mathematically related to the s-parameters of the balun probes $[X_{mm}]$ (3×3 matrix) and the differential DUT $[U_{mm}]$ (4×4 matrix). When all signal flow pathes are considered, the relationship is given by

$$[S] = f_1([X_{mm}],\ [U_{mm}]) \tag{3.5}$$

where f_1 is a nonlinear function given in [7]. When the common mode and cross mode signal flow pathes are neglected, the equation above can be simplified to,

$$[S] = f_2([X_{mm}],\ [U_{dd}]) \tag{3.6}$$

which can be used to compute the $[U_{dd}]$ (2×2 matrix) from known $[S]$ and $[X_{mm}]$. A Monte Carlo simulation is thus performed based on these two equations. With given $[X_{mm}]$ and $[U_{mm}]$, Eq 3.5 is used to compute the expected measured results by the VNA, $[S]$. With already known $[X_{mm}]$ and $[S]$, Eq 3.6 is then used to compute the differential mode s-parameters of the DUT $[U_{dd}]$. The discrepancies between the $[U_{dd}]$ and the differential components of $[U_{mm}]$ are characterization errors caused by neglecting the common mode and cross mode signal flow pathes. During the Monte Carlo simulation, the amplitude and phases of the common mode and cross mode components of $[U_{mm}]$ are randomly assigned, to evaluate the distribution of

characterization errors. The individual s-parameter of the balun probe $[X_{mm}]$ is also varied to study how it impacts the characterization errors. The procedures of the Monte Carlo simulation are outlined below.

1. The 3×3 s-matrix of the balun integrated probe is assigned as $[X_{mm}]$ in Eq 3.7, and the amplitude of the 4×4 s-matrix of the differential DUT is assigned as $[U_{mm}]$ in Eq 3.8.

2. Three random variables are generated. They are then assigned to $[U_{mm}]$ so that $S_{dd\,12}$, $S_{dd\,21}$ and $S_{dd\,22}$ have arbitrary phase values.

3. Another set of 24 random variables are generated. They are assigned to the remaining 12 terms of $[S_{dc}]$, $[S_{cd}]$ and $[S_{cc}]$ so that they have arbitrary amplitude values smaller than what is assigned to them respectively in step 1, and arbitrary phase values. This fully defines the $[X_{mm}]$ and $[U_{mm}]$.

4. Using the already defined s-matrixes $[X_{mm}]$ and $[U_{mm}]$, the expected two-port measurement results $[S]$ are computed using Eq 3.5, which takes into consideration all possible signal flow paths.

5. The 2×2 differential mode s-parameters $[U_{dd}]$ are calculated from $[X_{mm}]$ and $[S]$, using Eq 3.6.

6. Step 3 to 5 is repeated 1000 times for the Monte Carlo simulation. The $[U_{dd}]$ obtained each time is then compared to the actually assigned differential components of $[U_{mm}]$ to evaluate the measurement uncertainities.

$$X_{mm} = \begin{pmatrix} S_{dd} & S_{ds} & S_{dc} \\ S_{sd} & S_{ss} & S_{sc} \\ S_{cd} & S_{cs} & S_{cc} \end{pmatrix}$$

$$= \begin{pmatrix} -0.1681 + 0.0977i & 0.7761 + 0.3666i & S_{dc} \\ 0.7761 + 0.3666i & -0.0131 + 0.0657i & S_{sc} \\ S_{cd} & S_{cs} & S_{cc} \end{pmatrix} \tag{3.7}$$

$$U_{mm} = \begin{pmatrix} S_{dd11} & S_{dd12} & S_{dc11} & S_{dc12} \\ S_{dd21} & S_{dd22} & S_{dc21} & S_{dc22} \\ S_{cd11} & S_{cd12} & S_{cc11} & S_{cc12} \\ S_{cd21} & S_{cd22} & S_{cc21} & S_{cc22} \end{pmatrix}$$

$$= \begin{pmatrix} 0.314 & 0.1 & 0.174 & 0.1 \\ 4 & 0.56 & 0.174 & 0.174 \\ 0.174 & 0.1 & 0.314 & 0.1 \\ 0.174 & 0.174 & 2 & 0.314 \end{pmatrix} \tag{3.8}$$

The pre-assigned X_{mm} and U_{mm} is illustrated in Eq 3.7 and 3.8. The choice of amplitude values of U_{mm} is based on the measured s-parameters of a typical differential amplifier[44]. The choice of X_{mm} is based on the simulation results of a balun device, but the actual values of each s-parameter in X_{mm} is changed during the uncertainty simulation to study how the performance of the balun affects the final measurement uncertainties. The simulation results are shown in Fig 3.8 and 3.9. The scattered blue dots represent the distribution of the computed U_{dd} matrix using the parameters assigned in Eq 3.7 and 3.8. The more scattered the blue dots are around the center point, the greater the characterization uncertainty. The scattered red dots are obtained when the S_{cs} (or S_{sc}) and S_{cd} (or S_{dc}) terms are made 0 while other terms in X_{mm} remain the same. These scattered red dots represent the characterization uncertainty using a perfect balun that generates no common mode signals. The characterization errors with such balun probes are from the reflected common mode signals when the DUT is applied with differential excitation. For the given U_{mm} matrix, it is shown that S_{cs} (or S_{sc}) and S_{cd} (or S_{dc}) have a great impact on the measurement uncertainty. They should be kept strictly below -20dB to improve measurement accuracy. Simulation also shows that for a lossless balun that requires S_{cc} to be almost 0 dB because of the conservation of microwave energy, measurement accuracy does not improve proportionally with the improvement of S_{cs} (or S_{sc}) and

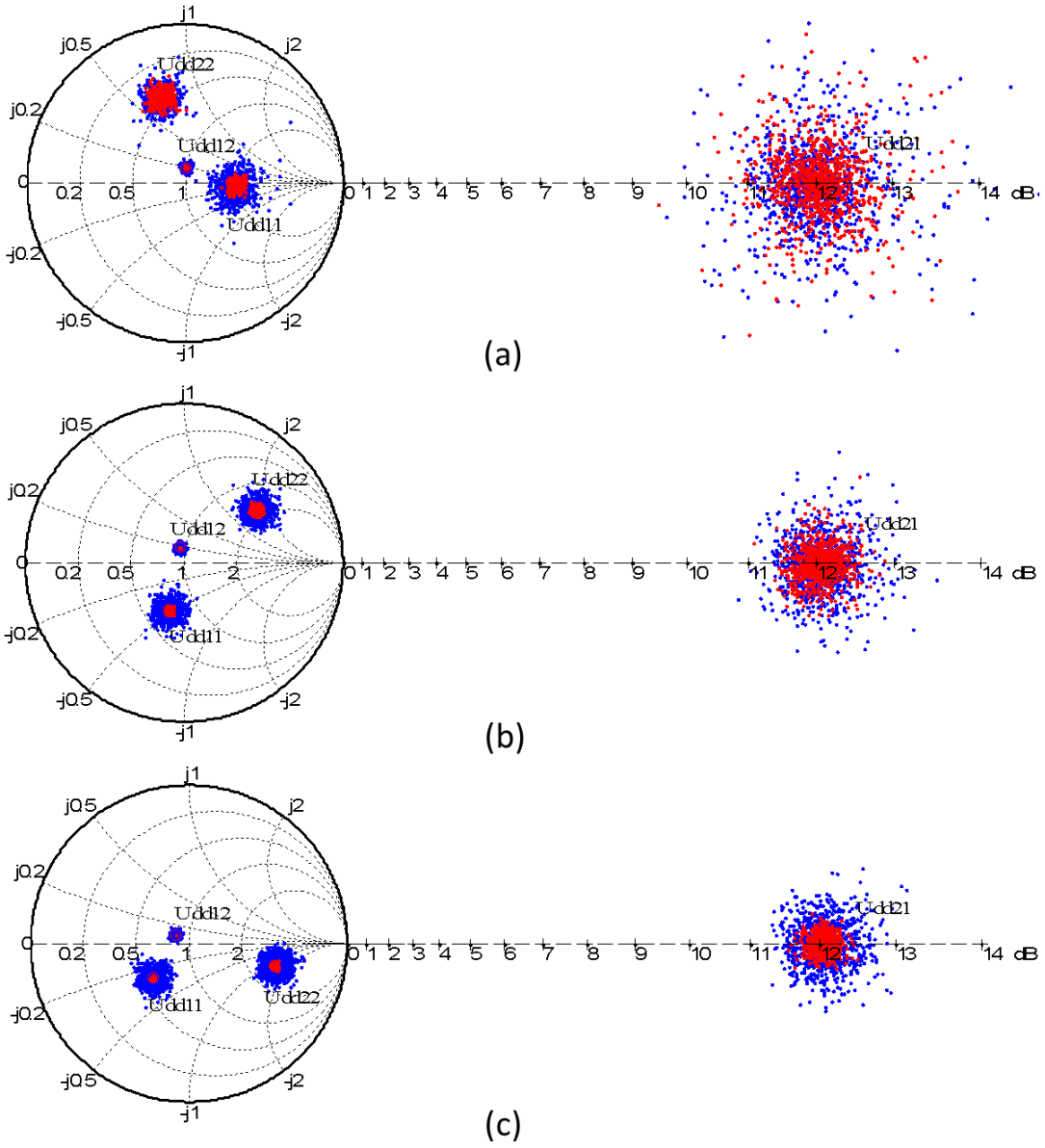

Figure 3.8: Measurement uncertainty of a differential DUT when (a) balun probe $S_{cc} = 0dB$, S_{dc} (S_{cd}), S_{sc} $(S_{cs}) = -20dB$ (blue), and S_{dc} (S_{cd}), S_{sc} $(S_{cs}) = 0$ (red), (b) balun probe $S_{cc} = -5dB$, S_{dc} (S_{cd}), S_{sc} $(S_{cs}) = -20dB$ (blue), and S_{dc} (S_{cd}), S_{sc} $(S_{cs}) = 0$ (red), and (c) balun probe $S_{cc} = -10dB$, S_{dc} (S_{cd}), S_{sc} $(S_{cs}) = -20dB$ (blue), and S_{dc} (S_{cd}), S_{sc} $(S_{cs}) = 0$ (red).

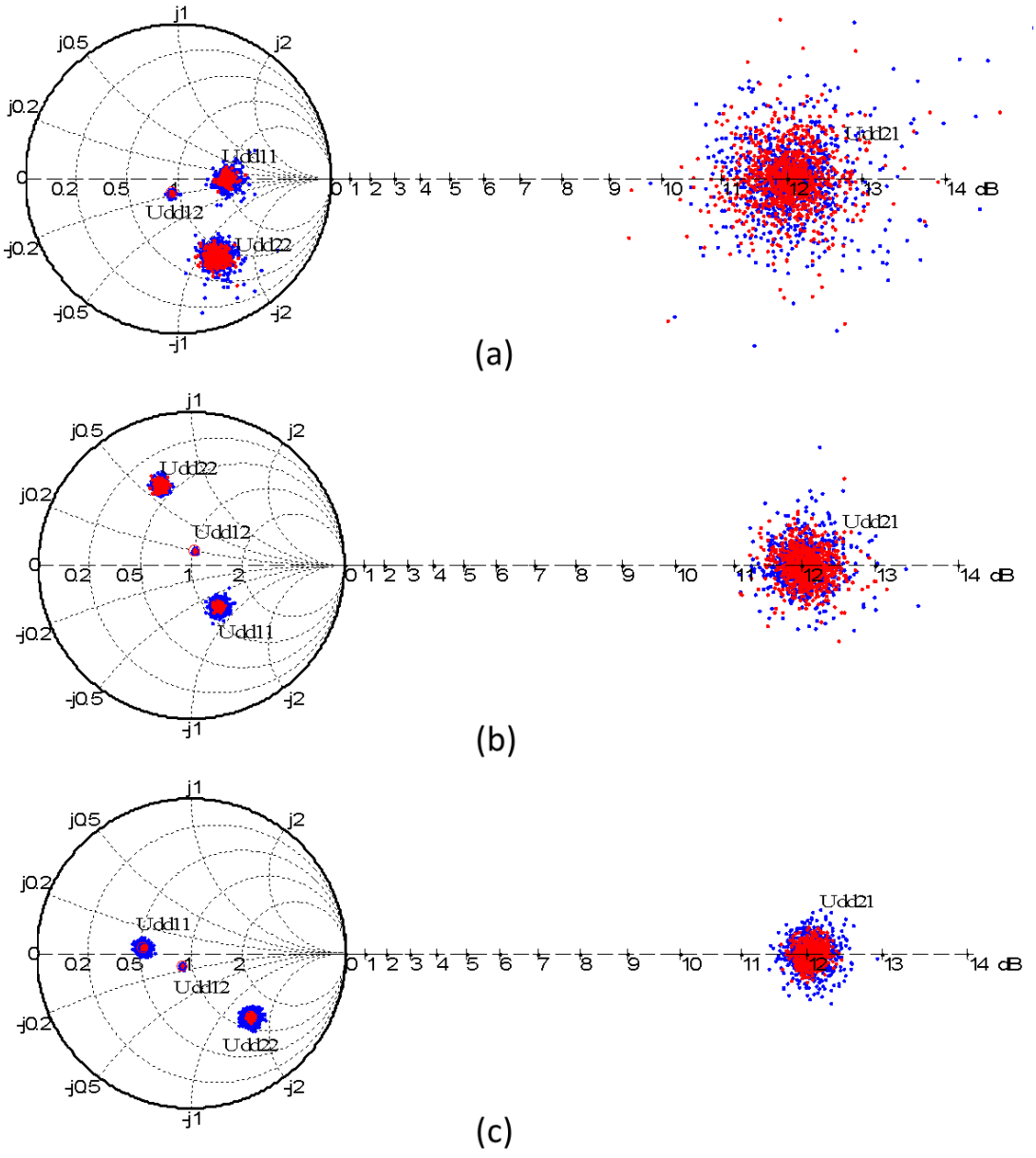

Figure 3.9: Measurement uncertainty of a differential DUT when (a) balun probe $S_{cc} = 0dB$, S_{dc} (S_{cd}), S_{sc} (S_{cs}) $= -25dB$ (blue), and S_{dc} (S_{cd}), S_{sc} (S_{cs}) $= 0$ (red), (b) balun probe $S_{cc} = -5dB$, S_{dc} (S_{cd}), S_{sc} (S_{cs}) $= -25dB$ (blue), and S_{dc} (S_{cd}), S_{sc} (S_{cs}) $= 0$ (red), and (c) balun probe $S_{cc} = -10dB$, S_{dc} (S_{cd}), S_{sc} (S_{cs}) $= -25dB$ (blue), and S_{dc} (S_{cd}), S_{sc} (S_{cs}) $= 0$ (red).

S_{cd} (or S_{dc}). It is only when S_{cc} is kept below -5 dB that efforts to reduce S_{cs} (or S_{sc}) and S_{cd} (or S_{dc}) start to reap the benefits.

Based on this measurement uncertainty simulation, the target performance for the balun probe is proposed. The common mode match term S_{cc} should be -5 dB or lower, while the mixed mode coupling S_{cs} (or S_{sc}) and S_{cd} (or S_{dc}) should be -20 dB or lower. It is important to note that this network is no longer a lossless network and a common mode loss mechanism has to be introduced in order to realize such a network.

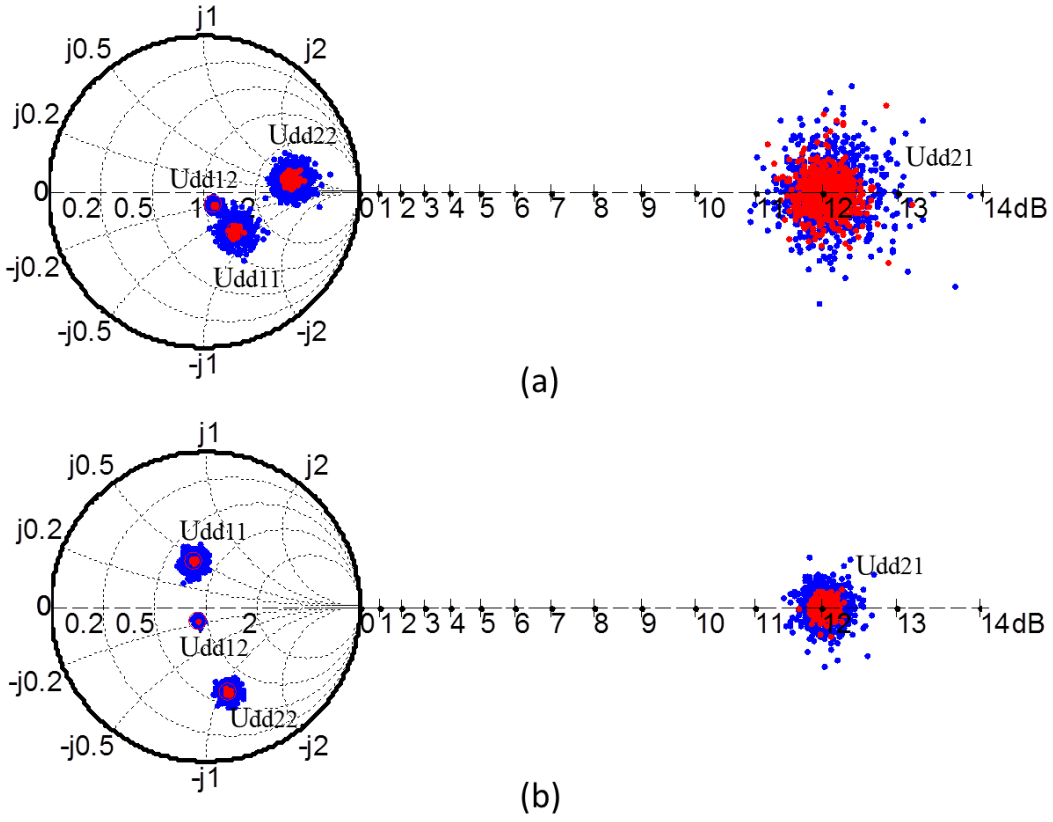

Figure 3.10: Measurement uncertainty of a differential DUT with balun probe $S_{cc} = -5dB$, S_{dc} (S_{cd}), S_{sc} (S_{cs}) $= -20dB$ (blue), and S_{dc} (S_{cd}), S_{sc} (S_{cs}) $= 0$ (red), when the 8 s-parameters in the S_{dc} and S_{cd} components of the differential DUT are (a) -15dB, (b) -20dB.

Another important issue using the balun probe is that the differential DUT also has an important role in determining the DUT characterization uncertainty. This effect is evaluated by setting the balun probe performance to be the target performance level

(S_{cc} is -5dB, S_{cs} (or S_{sc}) and S_{cd} (or S_{dc}) are -20dB), while changing the s-parameters of the differential DUT in Eq 3.8. It is found that the 8 s-parameters in the S_{cd} and S_{dc} components of Eq 3.8 have greater impacts on the characterization uncertainty than the rest of the s-parameters. The simulation results are shown in Fig 3.10 when all the 8 s-parameters in the S_{cd} and S_{dc} components of Eq 3.8 are reduced from -15dB to -20dB, while the rest of the s-parameters are kept the same. The characterization accuracy significantly improves with the reduction in the S_{cd} and S_{dc} components of the DUT. This also sets a limit for the differential DUT when it is characterized by a balun probe with the proposed target performance. The limit is that the S_{cd} and S_{dc} components of the differential DUT have to be below -15dB. This requires a well balanced differential DUT during the design and fabrication processes.

Chapter 4

Design of Balun Integrated Probes

4.1 Overview of Balun Design and Coupled Line Theories

A balun is an important electrical device in differential circuits that converts between differential signals and a single-ended signal. The name balun itself is derived from its functionality of achieving 'balanced-to-unbalanced' signal conversion. In the past few decades, there have been a myriad of different balun implementations being proposed and studied. In this section, an overview of the most commonly seen balun implementations will be discussed with special attention given to planarly implemented baluns. The fundamental theory of coupled lines will also be studied, to introduce the balun design equations that will subsequently be used in the next section.

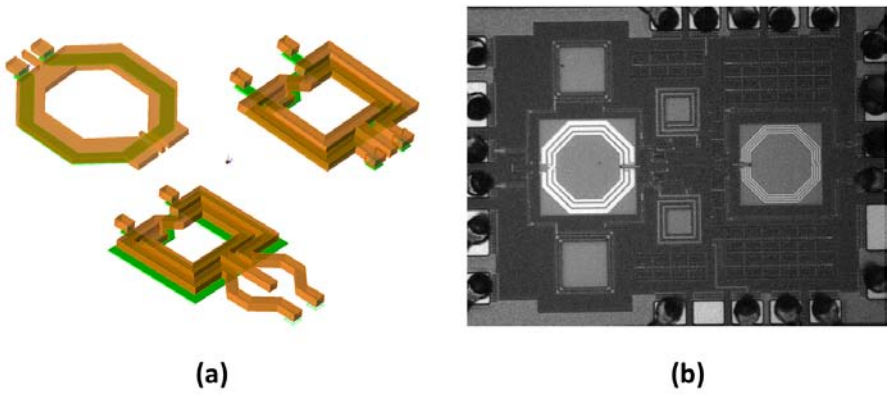

Figure 4.1: Spiral Inductor based transformer baluns[8, 9].

Shown in Fig 4.1 are some inductor-based transformer balun implementations[8, 9]. They employ magnetic coupling between the primary and secondary coils to achieve strong coupling and generate differential signal output from single-ended input. The high frequency electromagnetic signal passes through the primary coil, generating a varying magnetic field that induces electric signals of the same frequency in the secondary coils. These spiral inductor based transformer baluns are widely used in today's MMIC industry. However, as the working frequency of MMIC is raised, it becomes increasingly difficult to design and fabricate high-quality factor inductor based baluns because of the substrate loss, limited coupling and parasitics in via interconnections. Shown in Fig 4.1(b) is the die chip of a CMOS differential LNA operating from 3 - 5 GHz, with the two spiral inductor baluns taking up a large region of the die area[9].

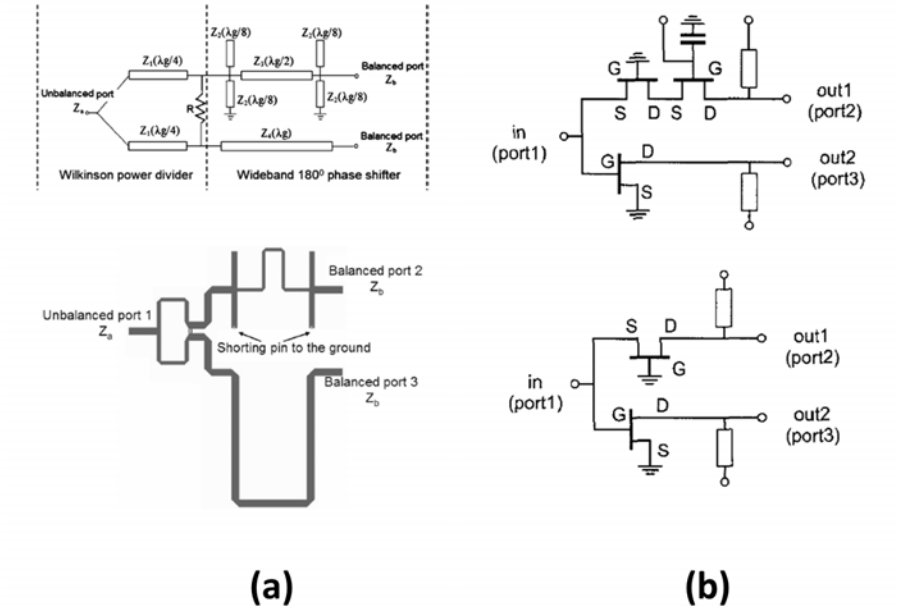

Figure 4.2: (a) Balun implementation based on a powder divider, (b) active balun[10, 11].

Apart from the commonly seen spiral inductor based balun, there are other novel balun implementations that have been proposed. For example, shown in Fig 4.2(a) is a planar balun implemention derived from a Wilkinson power divider[10]. The power

divider divides the input RF power into two branches where a 180° phase difference is added to the two branches by using a wide band phase shifter. Although there have been quite a few different implementations proposed for the 180° phase shifter, the Wilkinson power divider based balun generally suffers from a limited bandwidth, and high amplitude and phase imbalance due to assymetrical paths between the two branches. Also shown in Fig 4.2(b) is an active balun[11]. The CMOS based active balun is much more complicated to design and fabricate, but can be conveniently integrated with the process flow of CMOS based devices such as an LNA. However, it also suffers from the cutoff frequency as limited by CMOS technology.

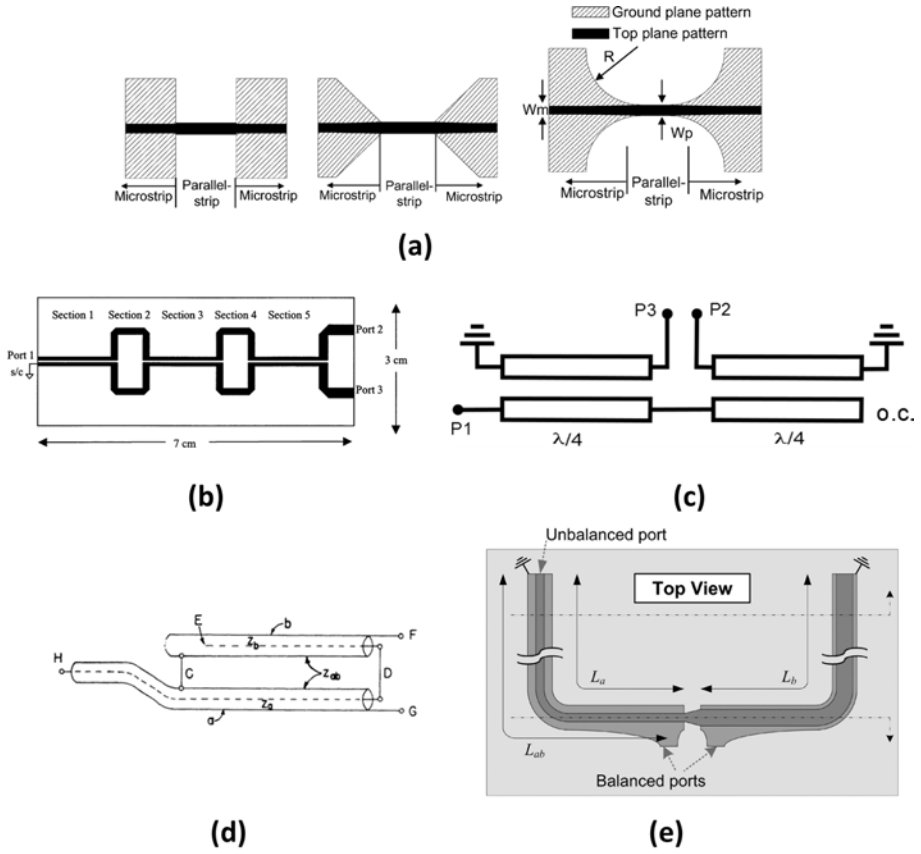

Figure 4.3: (a) Uncompensated balun implementation using microstrip to strip line transition[12, 13], (b) multisection coupled line based balun[14], (c) compensated balun using tight couplers, (d) original Marchand balun implemented in coaxial transmission line[15], (e) planar Marchand balun[16, 17].

There has been a growing interest in the industry to develop coupled line based planar baluns, as shown in Fig 4.3. A few different implementations as well as analytical approaches and design equations have been proposed. Shown in Fig 4.3(a) are three 'back-to-back' connected uncompensated balun structures[12, 13]. The single-ended signal from the microstrip line input is transitioned into differential mode signal output at the symmetric broadside-coupled parallel-plate strip lines. A successful mode conversion is largely dependent on the smooth transition between microstrip and strip line as well as the strength of coupling between the broadside-coupled strip lines. For occasions where sidewall-coupled lines are used as shown in Fig 4.3(b), the coupling is usually not strong enough to satisfy the stringent requirement of the balun. Cascaded multisection coupled lines are thus used to improve mode conversion and reduce reflection at the input port[14].

Shown in Fig 4.3(c) is the circuit diagram of a compensated balun. Although being commonly dubbed 'Marchand balun', and usually used interchangably in the academia, the compensated balun follows a distinguishably different analytical approach and design equations as will be discussed in the next section. It poses a much looser requirement on the coupling coefficient than the uncompensated balun. However, the design approach still presents a challenge for obtaining a high coupling coefficient, making it difficult for most sidewall coupled planar structures to meet this criteria.

The requirement on tight couplers is further relaxed with the Marchand balun design approach by employing novel coupling structures. The original Marchand balun is implemented in coaxial transmission line as shown in Fig 4.3(d)[15]. A planar implementation with analysis approaches is introduced in [16, 17], as shown in Fig 4.3(e). Asymmetrical coupled lines are used instead of symmetrical couplers. More tuning parameters are allowed, such as the impedances as well as the electrical lengths of the coupled lines, as will be discussed later. This gives the circuit designer

a lot more options in optimizing the balun performance. The planar Marchand balun has also demonstrated a very wide bandwidth.

In order to introduce the balun design equations in the next section, coupled line theories will initially be discussed in this section. The mathematic equations presented here apply to the general case of two uniform asymmetrically coupled lines. The wave equations describing the forward and backward power waves propagating along the coupled lines will be derived from the Telegraph Equations and their mode characteristics will be discussed. The mode characteristics for symmetrically coupled lines will be obtained from that of the asymmetrically coupled lines as a special case.

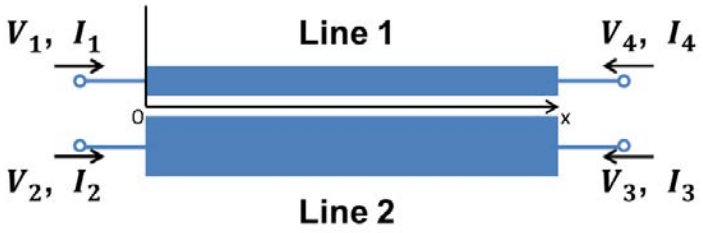

Figure 4.4: Asymmetrically coupled lines.

Shown in Fig 4.4 are two asymmetrically coupled lines with defined port voltages and currents. The Telegraph Equations that describe the wave propagation of the voltages and currents along the lines are shown below[45],

$$\begin{cases} \frac{dv_1(x)}{dx} = -Z_1 \cdot i_1(x) - Z_m \cdot i_2(x) \\ \frac{dv_2(x)}{dx} = -Z_m \cdot i_1(x) - Z_2 \cdot i_2(x) \\ \frac{di_1(x)}{dx} = -Y_1 \cdot v_1(x) - Y_m \cdot v_2(x) \\ \frac{di_2(x)}{dx} = -Y_m \cdot v_1(x) - Y_2 \cdot v_2(x) \end{cases} \tag{4.1}$$

where Z_1, Z_2 and Z_m is unit length self impedance of line 1, 2 and mutual impedance between line 1, 2 respectively, and Y_1, Y_2 and Y_m is unit length self admittance of line

1, 2 and mutual admittance between line 1, 2 respectively. By canceling i_1 and i_2 in the equations, two differential equations regarding the voltages are obtained,

$$\begin{cases} \frac{d^2\, v_1(x)}{d\, x^2} = a_1 \cdot v_1(x) + b_1 \cdot v_2(x) \\ \frac{d^2\, v_2(x)}{d\, x^2} = a_2 \cdot v_1(x) + b_2 \cdot v_2(x) \end{cases} \tag{4.2}$$

where $a_1 = Y_1 Z_1 + Y_m Z_m$, $a_2 = Y_2 Z_2 + Y_m Z_m$, $b_1 = Y_m Z_1 + Y_2 Z_m$, $b_2 = Y_m Z_2 + Y_1 Z_m$ are constants only determined by the line characteristics, and are independent of x position for uniform lines. By further canceling v_2 in the equations above, the fourth order differential equation for v_1 is obtained,

$$\frac{d^4\, v_1(x)}{d\, x^4} - (a_1 + a_2) \cdot \frac{d^2\, v_1(x)}{d\, x^2} - (a_1 a_2 - b_1 b_2) \cdot v_1(x) = 0 \tag{4.3}$$

Based on differential equations theories, fourth order differential equations can be solved by first obtaining the eigenvalues shown below,

$$\gamma^4 - (a_1 + a_2) \cdot \gamma^2 + (a_1 a_2 - b_1 b_2) = 0 \tag{4.4}$$

which gives the solutions as $\gamma = \pm\gamma_c, \pm\gamma_\pi$, where $\gamma_c = \frac{1}{2}(a_1 + a_2) + \frac{1}{2} \cdot \sqrt{(a_1 - a_2)^2 + 4 b_1 b_2}$ and $\gamma_\pi = \frac{1}{2}(a_1 + a_2) - \frac{1}{2} \cdot \sqrt{(a_1 - a_2)^2 + 4 b_1 b_2}$. The subscripts c and π correspond to two different modes of propagation, the in-phase c mode and anti-phase π mode. For each mode, there are two possible values for the propagation constant γ, one positive and the other negative, which represents the forward propagating and backward propagating wave respectively. The wave equations for the voltages and currents can be described as,

$$\begin{cases} v_1(x) = v_{1c}^{+} \cdot e^{-\gamma_c x} + v_{1c}^{-} \cdot e^{\gamma x} + v_{1\pi}^{+} \cdot e^{-\gamma_\pi x} + v_{1\pi}^{-} \cdot e^{\gamma_\pi x} \\ v_2(x) = R_c \cdot (v_{1c}^{+} \cdot e^{-\gamma_c x} + v_{1c}^{-} \cdot e^{\gamma x}) + R_\pi \cdot (v_{1\pi}^{+} \cdot e^{-\gamma_\pi x} + v_{1\pi}^{-} \cdot e^{\gamma_\pi x}) \\ i_1(x) = Y_{1c}(v_{1c}^{+} \cdot e^{-\gamma_c x} - v_{1c}^{-} \cdot e^{\gamma x}) + Y_{1\pi}(v_{1\pi}^{+} \cdot e^{-\gamma_\pi x} - v_{1\pi}^{-} \cdot e^{\gamma_\pi x}) \\ i_2(x) = R_c Y_{2c} \cdot (v_{1c}^{+} \cdot e^{-\gamma_c x} - v_{1c}^{-} \cdot e^{\gamma x}) + R_\pi Y_{2\pi} \cdot (v_{1\pi}^{+} \cdot e^{-\gamma_\pi x} - v_{1\pi}^{-} \cdot e^{\gamma_\pi x}) \end{cases} \tag{4.5}$$

where $R_c = \frac{1}{2b_1}(a_2 - a_1) + \frac{1}{2b_1} \cdot \sqrt{(a_1 - a_2)^2 + 4b_1 b_2}$, $R_\pi = \frac{1}{2b_1}(a_2 - a_1) - \frac{1}{2b_1} \cdot \sqrt{(a_1 - a_2)^2 + 4b_1 b_2}$, $Y_{1\,c,p} = \gamma_{c,p} \cdot \frac{Z_2 - Z_m R_{c,p}}{Z_1 Z_2 - Z_m}$ and $Y_{2\,c,p} = \frac{\gamma_{c,p}}{R_{c,p}} \cdot \frac{Z_1 R_{c,p} - Z_m}{Z_1 Z_2 - Z_m}$ are constants determined by line characteristics. It can be seen that for any real values for a_1, a_2, b_1 and b_2, as determined in Eq 4.2, the term R_c is positive real, and the term R_π is negative real.

One crucial observation can be made with regard to the asymmetrically coupled lines. There are two modes being supported by the coupled lines, the in-phase c mode and anti-phase π mode. These two modes are named in-phase and anti-phase modes because of the phase relations between v_1 and v_2 for each mode, as can be seen from Eq 4.5 and the signs of R_c and R_π. For the in-phase mode, R_c is positive real and v_1 and v_2 always keep pace with each other in terms of phase difference. For the anti-phase mode, R_π is negative real and v_1 and v_2 always have opposite phase with each other.

These equations can also naturally simplify to the case for symmetrically coupled lines. Let $Z_1 = Z_2 = Z_s$ and $Y_1 = Y_2 = Y_s$, it is then easy to come to the result that the in-phase c mode becomes the even mode and the anti-phase π mode becomes odd mode,

$$\begin{cases} R_c = 1 \\ R_\pi = -1 \end{cases} \tag{4.6}$$

4.2 Analytical Approaches for Balun Design

Although there have been quite a few different proposed balun implementations, Marchand balun is popular for MMIC applications because of its planar structure, broad band feature and excellent performance in reducing common mode conversion. In this section, the discussion will be focused on the analytical approach and design equations of a coupled line based balun, including uncompensated balun, compensated balun and Marchand balun.

Uncompensated Balun

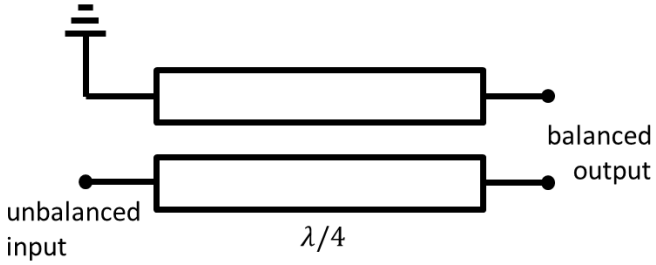

Figure 4.5: Equivalent circuit diagram of an uncompensated balun.

An uncompensated balun employs a section of symmetrically coupled lines for mode conversion. It can be analyzed using even and odd mode analysis, with the mode specific admittance Y_{0e} and Y_{0o}. Under the port matching conditions, the admittance matrix for the symmetric coupled lines computed from even and odd mode analysis is[46, 47],

$$Y =$$

$$\begin{pmatrix} -\frac{1}{2}j(Y_{0e}+Y_{0o})cot\theta & -\frac{1}{2}j(Y_{0e}-Y_{0o})cot\theta & \frac{1}{2}j(Y_{0e}-Y_{0o})csc\theta & \frac{1}{2}j(Y_{0e}+Y_{0o})csc\theta \\ -\frac{1}{2}j(Y_{0e}-Y_{0o})cot\theta & -\frac{1}{2}j(Y_{0e}+Y_{0o})cot\theta & \frac{1}{2}j(Y_{0e}+Y_{0o})csc\theta & \frac{1}{2}j(Y_{0e}-Y_{0o})csc\theta \\ \frac{1}{2}j(Y_{0e}-Y_{0o})csc\theta & \frac{1}{2}j(Y_{0e}+Y_{0o})csc\theta & -\frac{1}{2}j(Y_{0e}+Y_{0o})cot\theta & -\frac{1}{2}j(Y_{0e}-Y_{0o})cot\theta \\ \frac{1}{2}j(Y_{0e}+Y_{0o})csc\theta & \frac{1}{2}j(Y_{0e}-Y_{0o})csc\theta & -\frac{1}{2}j(Y_{0e}-Y_{0o})cot\theta & -\frac{1}{2}j(Y_{0e}+Y_{0o})cot\theta \end{pmatrix} \quad (4.7)$$

where the even and odd mode phase velocity is assumed to be the same, and the electrical length of the coupling section is $\theta = 90^\circ$ for a quarter-wave long coupler at band center. When port 1 is short-circuited ($V_1 = 0$), while the other three ports are terminated with matched loads, the s-parameters for the 3-port network can be obtained by converting the Y matrix into the S matrix as[46, 47]:

$$\begin{cases} S_{32} = \frac{j2Y_0Y_A}{Y_0^2+Y_A^2+Y_B^2} \\ S_{42} = \frac{-j2Y_0Y_B}{Y_0^2+Y_A^2+Y_B^2} \end{cases} \tag{4.8}$$

where $Y_0 = 1/Z_0$ is the source or load impedance and $Y_A = (Y_{0o} - Y_{0e})/2$, and $Y_B = (Y_{0o} + Y_{0e})/2$. From these two s-parameters it can be obtained that

$$S_{32}/S_{42} = -Y_A/Y_B = -(Y_{0o} - Y_{0e})/(Y_{0o} + Y_{0e}) = -(R-1)/(R+1) \tag{4.9}$$

where $R = Z_{0e}/Z_{0o}$ is the ratio of even mode and odd mode characteristic impedance. From Eq 4.9 it can be seen that the phase difference between S_{32} and S_{42} are 180° degrees at band center while the amplitude imbalance is determined by the R ratio. The higher the R ratio that is achieved for the coupled lines structure, the lower the amplitude imbalance across the desired frequency range. In order to assess uncompensated balun performance with respect to different R ratios, an ADS model for uncompensated balun using ideal coupled lines is setup as shown in Fig 4.6 that allows for arbitary assignment of even and odd mode impedance, as well as physical length and effective dielectric constant for the respective mode. By making the even and odd mode effective dielectric constants different from each other, the assumption of same even and odd mode phase velocity is relaxed, allowing for further examination of its impact on the balun performance.

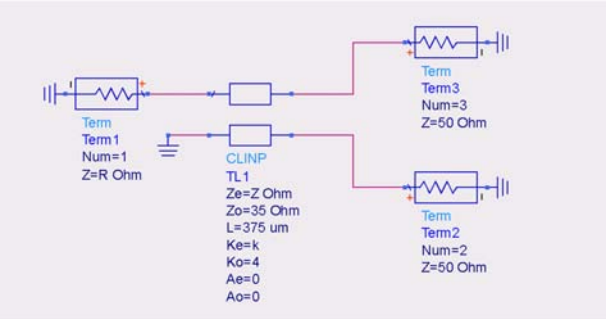

Figure 4.6: ADS model of uncompensated balun using ideal coupled lines models.

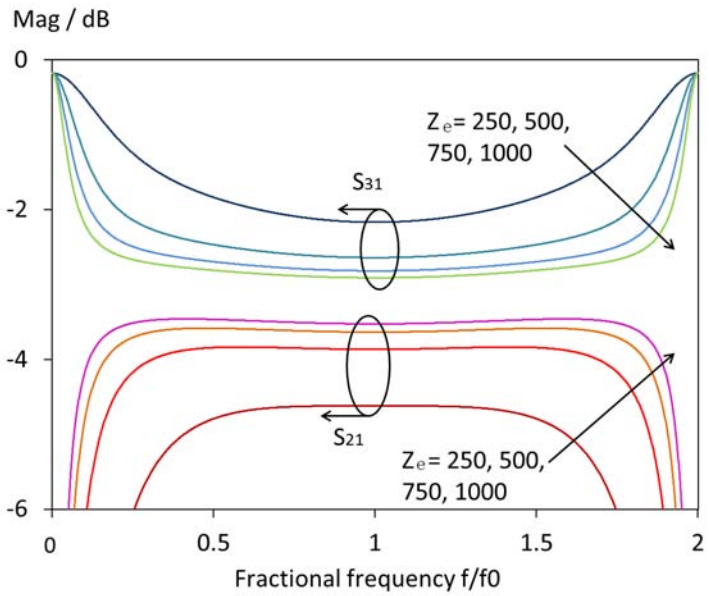

Figure 4.7: The amplitude imbalance of an uncompensated balun at different even mode impedances (odd mode impedance is 35 Ohm, odd mode and even mode effective dielectric constant is 4).

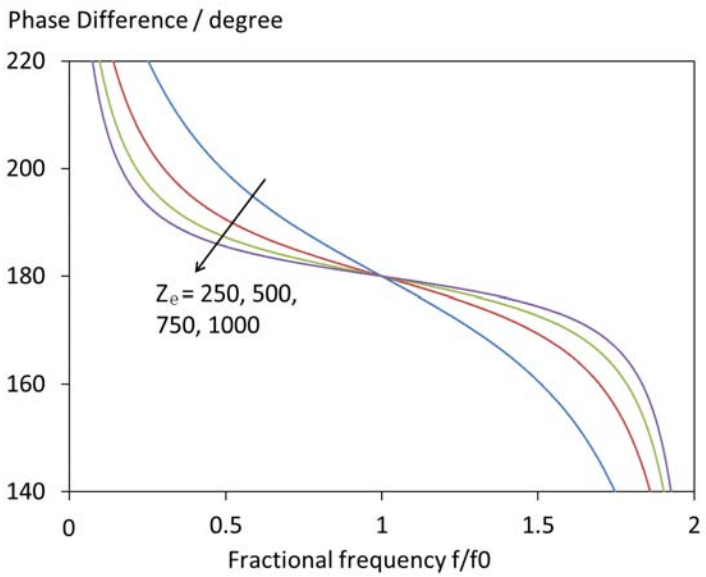

Figure 4.8: The phase imbalance of an uncompensated balun at different even mode impedance (odd mode impedance is 35 Ohm, odd mode and even mode effective dielectric constant is 4).

Shown in Fig 4.7 and 4.8 are the amplitude and phase imbalance for an uncompensated balun with different coupling factors as simulated in ADS. The odd mode impedance is set to be 35 Ohm, while the even mode impedance is varied from 250 to 1000 Ohm. As can be seen from these figures, the even mode impedance Z_{0e} has to be uncommonly large to achieve 1dB amplitude imbalance and +/-5 degree phase imbalance for a quarter-wave-long uncompensated balun. Baluns using cascaded coupled lines to achieve very high even mode impedance have been reported[48].

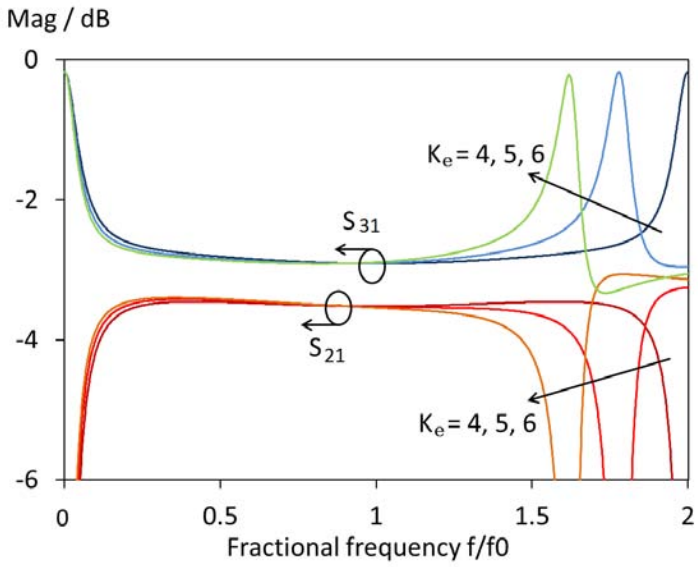

Figure 4.9: The amplitude imbalance of an uncompensated balun at different even mode effective dielectric constant (odd mode impedance is 35 Ohm, even mode impedance is 1000 Ohm, odd mode effective dielectric constant is 4).

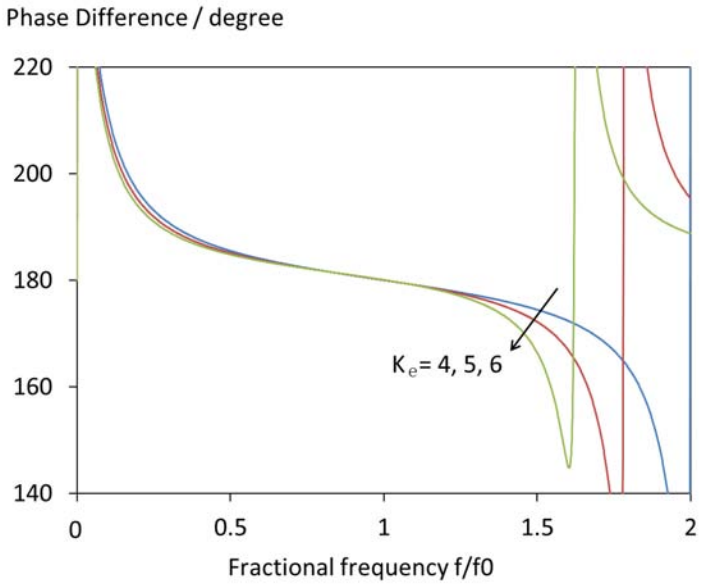

Figure 4.10: The phase imbalance of an uncompensated balun at different even mode effective dielectric constant (odd mode impedance is 35 Ohm, even mode impedance is 1000 Ohm, , odd mode effective dielectric constant is 4).

Different phase velocities for even and odd mode propagation is found to be another important factor limiting the bandwidth, although it does not significantly deteriorate balun performance at lower frequency, as shown in Fig 4.9 and 4.10.

Compensated Balun

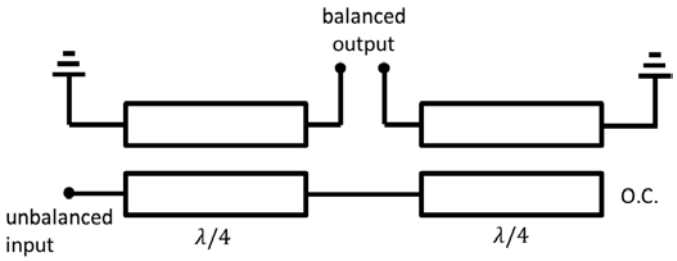

Figure 4.11: A compensated balun.

Shown in Fig 4.11 is a compensated balun which consists of two quarter-wave long tight couplers terminated as shown. By converting the four port Y matrix in Eq 4.7 into an s-matrix and applying signal flow graph analysis, the 3 port s-parameters for a compensated balun can be computed as[49]:

$$S = \begin{pmatrix} \frac{x^4-y^4-y^2}{1+y^2} & \frac{x^3y-xy^3-xy}{1+y^2} & -\frac{x^3y-xy^3-xy}{1+y^2} \\ \frac{x^3y-xy^3-xy}{1+y^2} & -\frac{x^2}{1+y^2} & \frac{-x^2y^2-+y^2+y^4}{1+y^2} \\ -\frac{x^3y-xy^3-xy}{1+y^2} & \frac{-x^2y^2-+y^2+y^4}{1+y^2} & -\frac{x^2}{1+y^2} \end{pmatrix} \tag{4.10}$$

where $x = \frac{\sqrt{1-C^2}}{\sqrt{1-C^2}\,cos\theta + j\,sin\theta}$, $y = \frac{j\,Ctan\theta}{\sqrt{1-C^2}\,cos\theta + j\,sin\theta}$, and $C = \frac{Z_{0e}-Z_{0o}}{Z_{0e}+Z_{0o}}$ is the coupling coefficient and θ is the electrical length for the coupled line under the assumption that even and odd mode phase velocities are the same.

In the more general case that the unbalanced and balanced port impedance Z_0 and Z_1 is different at port 1, port 2 and 3, the modified balun s-matrix can be obtained from the matrix manipulation shown in Eq 4.11[49].

$$[\,S\,]' = [\,A\,]^{-1} \cdot (([\,S\,] - [\,\Gamma\,]) \cdot ([\,I\,] - [\,\Gamma\,][\,S\,])^{-1}) \cdot [\,A\,] \tag{4.11}$$

where $[\,\Gamma\,] = \begin{pmatrix} 0 & 0 & 0 \\ 0 & \frac{Z_1-Z_0}{Z_1+Z_0} & 0 \\ 0 & 0 & \frac{Z_1-Z_0}{Z_1+Z_0} \end{pmatrix}$, $[\,A\,] = \begin{pmatrix} 1 & 0 & 0 \\ 0 & \frac{2\sqrt{Z_1Z_0}}{Z_1+Z_0} & 0 \\ 0 & 0 & \frac{2\sqrt{Z_1Z_0}}{Z_1+Z_0} \end{pmatrix}$.

Choose $\theta = 90^\circ$ for quarter-wave coupled lines, the modified s-matrix of an impedance transforming balun is computed to be,

$$S = \begin{pmatrix} \frac{1-C^2(\frac{2Z_1}{Z_0}+1)}{1+C^2(\frac{2Z_1}{Z_0}-1)} & j\frac{2C\sqrt{1-C^2}\sqrt{\frac{Z_1}{Z_0}}}{1+C^2(\frac{2Z_1}{Z_0}-1)} & -j\frac{2C\sqrt{1-C^2}\sqrt{\frac{Z_1}{Z_0}}}{1+C^2(\frac{2Z_1}{Z_0}-1)} \\ j\frac{2C\sqrt{1-C^2}\sqrt{\frac{Z_1}{Z_0}}}{1+C^2(\frac{2Z_1}{Z_0}-1)} & \frac{1-C^2}{1+C^2(\frac{2Z_1}{Z_0}-1)} & j\frac{2C^2\frac{Z_1}{Z_0}}{1+C^2(\frac{2Z_1}{Z_0}-1)} \\ -j\frac{2C\sqrt{1-C^2}\sqrt{\frac{Z_1}{Z_0}}}{1+C^2(\frac{2Z_1}{Z_0}-1)} & j\frac{2C^2\frac{Z_1}{Z_0}}{1+C^2(\frac{2Z_1}{Z_0}-1)} & \frac{1-C^2}{1+C^2(\frac{2Z_1}{Z_0}-1)} \end{pmatrix} \tag{4.12}$$

A few critical observation can be made from Eq 4.12. The first is that $S_{21} = -S_{31}$ is always ensured regardless of values of coupling coefficient C. This effectively means that a perfect balun can be achieved regardless of the coupler's coupling strength. The second is that unbalanced port return loss $S_{11} = \frac{1-C^2(\frac{2Z_1}{Z_0}+1)}{1+C^2(\frac{2Z_1}{Z_0}-1)}$ gives rise to the unbalanced port matching condition,

$$C_{match} = \frac{1}{\sqrt{\frac{2Z_1}{Z_0}+1}} \tag{4.13}$$

Eq 4.13 determines the optimum coupling coefficient, or even to odd mode impedance ratio, for a balun of a given port impedance transforming ratio. Unlike the uncompensated balun, the amplitude and phase imbalance of a compensated balun is not determined by the coupling coefficient as long as the assumption of same even and odd mode phase velocities holds true. The coupling coefficient only affects how well the ports are matched. Ideal port matching conditions require an optimum value for the coupling coefficient. It's also worth pointing out that a tight 3 dB coupler is not always preferred. The optimum coupling coefficient and even to odd mode impedance ratio for baluns of various port impedance transforming ratioes are tabulated in Tab 4.1 below.

Port Impedance Transforming Ratio	Z_1/Z_0	0.5	1	1.5	2
Coupling Coefficient / dB	C	-3	-4.8	-6	-7
Even to Odd Mode Impedance Ratio	Z_{0e}/Z_{0o}	5.8	3.7	3.0	1.5

Table 4.1: Optimum coupling coefficient and even to odd mode impedance ratio for baluns of different port impedance transforming ratioes.

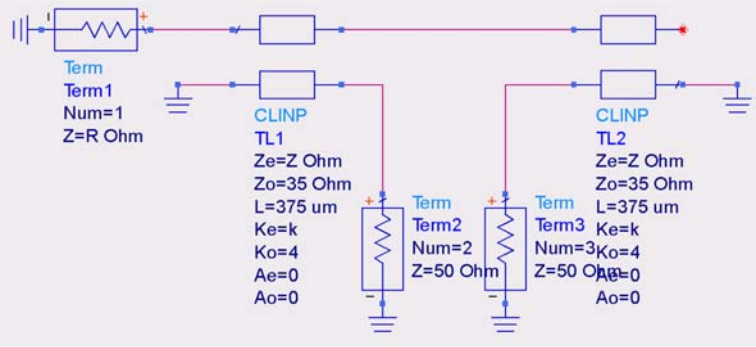

Figure 4.12: An ADS model of compensated balun using ideal coupling lines structures.

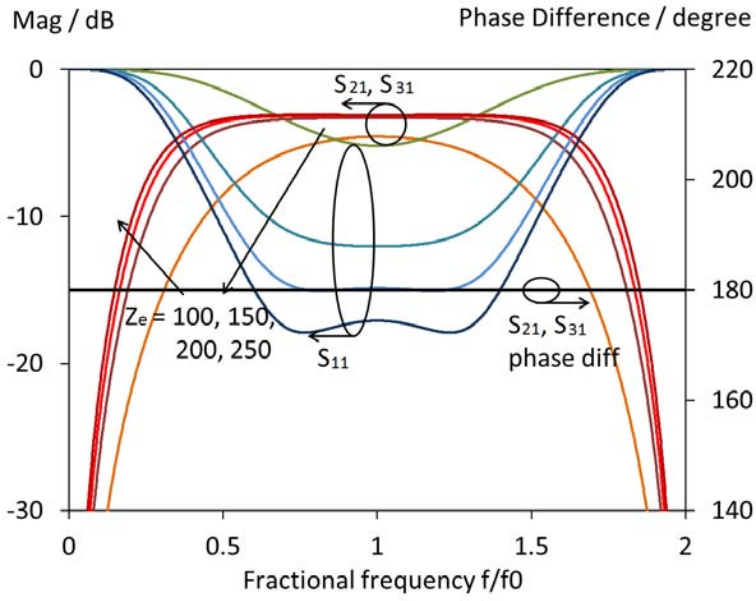

Figure 4.13: The magnitude and phase imbalance of a compensated balun for various even mode impedance values (odd mode impedance is 35 Ohm, odd and even mode effective dielectric constant is 4).

In order to verify these observations, as well as to identify sources of amplitude and phase imbalance, an ADS model for a compensated balun is setup as shown in Fig 4.12. The simulation results confirm the previous observations in this chapter.

As shown in Fig 4.13, phase and amplitude imbalance between port 2 and 3 is almost nonexistent for all different values of even mode impedance, when common and odd mode phase velocities are identical. Change in even mode impedance only affects unbalanced port match and the energy converted into the differential mode signal. Difference in even and odd mode phase velocities is found to be a major limiting factor for bandwidth, as shown in Fig 4.14 and 4.15.

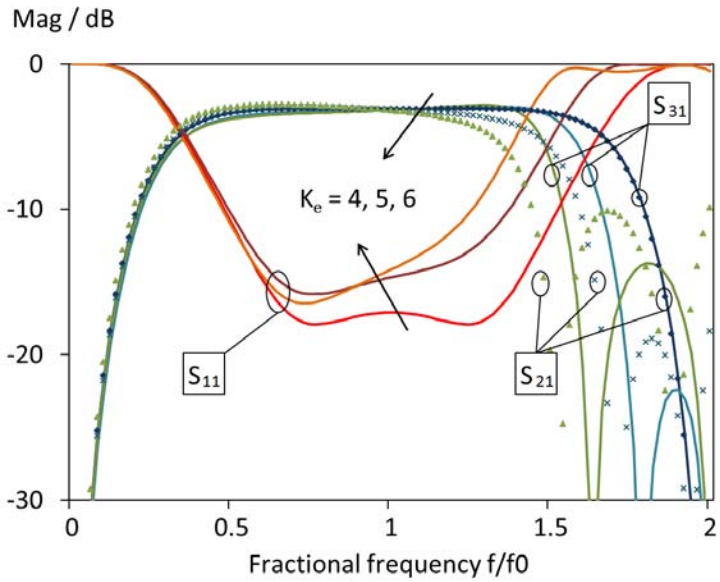

Figure 4.14: The magnitude imbalance of a compensated balun for various even mode effective dielectric constant (odd mode impedance is 35 Ohm, even mode impedance is 250 Ohm, odd mode effective dielectric constant is 4).

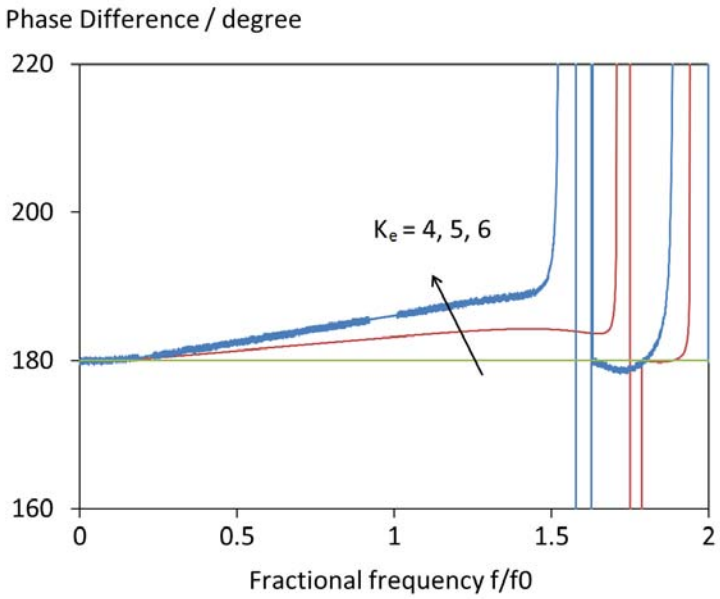

Figure 4.15: The phase imbalance of a compensated balun for various even mode effective dielectric constant (odd mode impedance is 35 Ohm, even mode impedance is 250 Ohm, odd mode effective dielectric constant is 4).

Marchand Balun

Although being structurally very similar to a compensated balun and commonly named interchangably with a compensated balun in most literature, the Marchand balun has a very different analytical approach and design equations. First conceived in the 1940s using coaxial transmission lines by Marchand and a few other researchers at Harvard Radio Research Laboratory, it was later reinvented by Roberts in the 1950s and implemented in planar circuit by R. Bawer and J.J. Wolfe in 1960[50, 51]. Its design and analysis has been extensively discussed and well documented in literature.

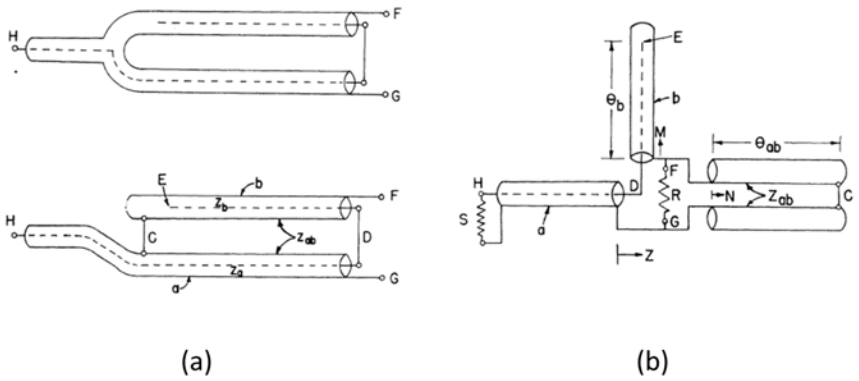

Figure 4.16: (a) Coaxial transmission line Marchand balun and (b) its equivalent circuit[18].

Shown in Fig 4.16 are two variations of Marchand baluns implemented in coaxial lines and its equivalent circuit[18]. The Marchand balun consists of two sections of shielded coaxial lines a and b, with characteristic impedances Z_a and Z_b, and electrical length θ_a and θ_b respectively. The inner conductors of the coaxial lines a and b are connected at point D, while the outer conductors are connect at point C. Additionally, the outer conductors of line a and b also have equal impedance Z_{ab} that is referenced to a ground plane not explicitly shown in Fig 4.16, and reaches out as differential ports at point F and G. It has been demonstrated that the Marchand balun has excellent performance in terms of common mode rejection and bandwidth.

As can been seen from the equivalent circuit in Fig 4.16(b), the unbalanced input port impedance is S and balanced port load between point F and G is R. The two line sections a and b are serial connected, while the balanced port load R and outer conductor impedance Z_{ab} is parallel connected to the circuit. The impedance looking into the circuit at the point D can thus be computed as,

$$Z = -jZ_b cot\theta_b + \frac{jRZ_{ab}tan\theta_{ab}}{R + jZ_{ab}tan\theta_{ab}} \tag{4.14}$$

Substituting $\theta_b = \theta_{ab} = \theta$ and simplifying Eq 4.14 gives,

$$Z = \frac{RZ_{ab}^2 + j(R^2(Z_{ab} - Z_b cot^2\theta) - Z_b Z_{ab}^2)cot\theta}{R^2 cot^2\theta + Z_{ab}^2} \tag{4.15}$$

In order to match Z to unbalanced port load S, the imaginary part of Z has to cancel out. As can be seen from Eq 4.15, the Marchand balun design allows for both Z_b and Z_{ab} to be tuned for optimum balun performance. There have been a few different optimization choices that lead to different balun performance. One of the optimization choices proposed by Roberts imposes the conditions that $Z_a = Z_b$ and $Z_{ab} = R$, which leads to a simplified expression for impedance Z to be[18, 51]

$$Z = R\,sin^2\theta + j(R\,sin^2\theta - Z_a)cot\theta \tag{4.16}$$

Making the imaginary component equal to 0 gives the matching condition for θ that is at two widely separated frequencies given by the solution

$$sin^2\theta = Z_a/R \tag{4.17}$$

Another reported optimization choice by D.A. Dunn, J.W. McLaughlin and R.W. Grow[51] imposes the condition that $\theta = 90$ at midband, Z_{ab} is chosen to be as large as possible and

$$Z_b = R^2/Z_{ab} \tag{4.18}$$

Apart from this coaxial transmission line balun, there are also a few planarly implemented Marchand baluns reported. Shown below in Fig 4.17 are planar Marchand baluns fabricated using multilayered organic thin films[16, 17]. Similar to the compensated baluns introduced in prior discussion, the planar Marchand balun has two sections of coupling lines connected serially and terminated in a similar fashion. However, there are a few major differences that clearly distinguish the planar Marchand balun from a compensated balun.

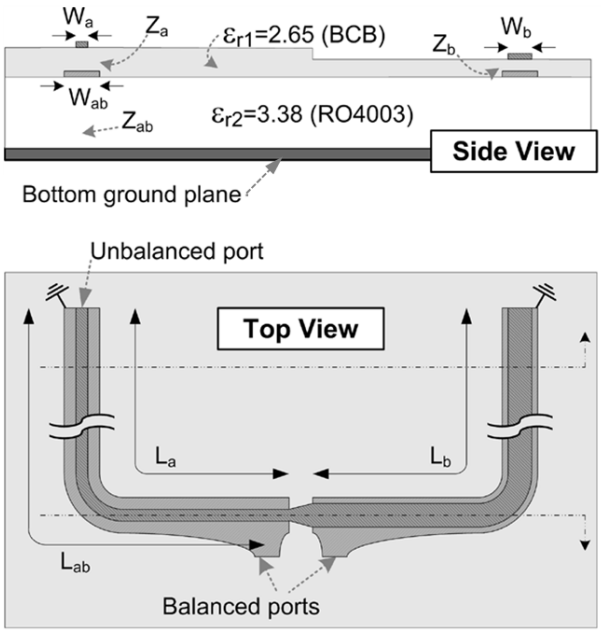

Figure 4.17: Planar Marchand baluns implementations[16].

First, the Marchand balun uses asymmetrical coupling structures rather than the typically employed symmetrical coupling structures for a compensated balun. The necessity of using asymmetrical coupling structures for a Marchand balun can be appreciated from the theoretical analysis for a coaxial transmission line balun. In the analysis for a coaxial transmission line balun, the impedance Z_a and Z_b are characteristic impedances of the inner conductors of lines a and b referenced to their outer conductors, while Z_{ab} is the characteristic impedance of the outer conductors of lines a and b referenced to a ground plane. In order to maintain this novel design approach and follow the same analysis procedures, asymmetrically coupled lines have to be used. It's also important to design the asymmetrically coupled lines' bottom metal strip wide enough to shield the field lines of the coupled lines' top metal strip away from the ground plane, just as the outer conductor of the coaxial line shields field lines of the inner conductor away from the ground plane. This design ensures the impedance Z_a and Z_b seen by the top metal strips is referenced to the coupled

lines' bottom metal strip, while the impedance Z_{ab} seen by the coupled lines' bottom metal strip is referenced to the ground plane.

Second, the planar Marchand balun has relatively relaxed requirements on the physical dimensions of the coupling structure compared to that for a compensated balun. The compensated balun is composed of two sections of quarter-wave long symmetrically coupled lines, whose physical dimensions are pretty much fixed after the even mode and odd mode impedances are chosen for a given dielectric medium. The Marchand balun, on the other hand, allows for more tuning parameters. With the aid of modern finite element simulation tools such as HFSS, the balun design can be more easily optimized to meet bandwidth, performance, structural limitations and other requirements or constraints.

4.3 W-band Balun Integrated Probe Design

A micromachined GSG probe at W-band has been previously fabricated and tested as part of this dissertation at the University of Virginia, as shown in Fig 4.18[52, 53]. The single-ended GSG probe has since then been scaled to higher frequencies, and more functionality has been added[39, 54]. The higher frequency probe tested exhibits excellent mechanical as well as electrical performance[3]. With the success of this GSG probe, a balun integrated probe is proposed in this dissertation to help facilitate the on-wafer characterization of differential MMIC and to improve differential circuit modeling and design. The prototype balun integrated probe is designed to be fully compatible with the existing probe blocks at W-band. The balun analysis approaches introduced in the previous sections are used to help with the realization of the first reported balun probe with common mode matching network at W-band.

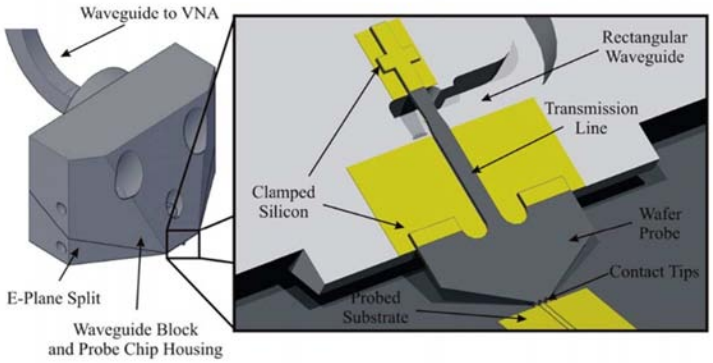

Figure 4.18: GSG probe at W-band, probe head width is $750\mu m$, length from clamp region to probe tip is $400\mu m$[19].

The GSG probe at W-band is fabricated on $15\mu m$ thick SOI wafer using backside alignment processing technique and is housed in a metallic probe block. In order to be compatible with the existing probe block, a few restricions apply for the design of the prototype balun integrated probe. First, the balun circuitry should be outside the block channel so that its RF performance will not be affected by probe alignment uncertainties as well as block micromachining tolerances when it is assembled in the probe block. Second, the width of the probe head area is fixed to $750\mu m$ to be physically clamped by the probe block at the beamlead region as well as to maintain proper stress distribution when the probe is in contact with substrate. While the length of the probe head can be increased from the original $400\mu m$ to accommodate the balun structure, probe stiffness will be affected. This will lead to a lower limit for maximum achievable contact force. Challenges for the design of a high performance balun integrated probe emerge from the Si material used, fabrication limitations, as well as the limited space available for balun circuitry at the probe chip head area.

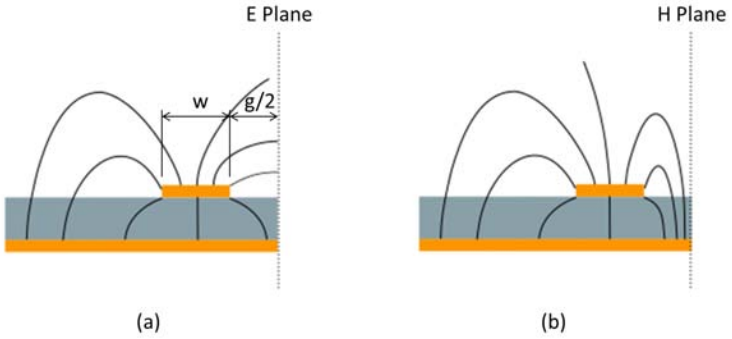

Figure 4.19: The electrical field lines for even and odd mode operation of symmetrically coupled microstrip lines.

The use of $15\mu m$ thick silicon film as probe mechanical support poses a significant challenge for the balun integrated probe design. If symmetrically coupled lines are used for the balun implementation, the performance requirement of the balun sets a bar on the coupling coefficient that can not possibly be achieved by sidewall coupled microstrip lines. According to Eq 4.13, as discussed in the previous section, for a balun with port impedance transformation ratio of 1, the coupled lines structure needs to achieve an even to odd mode impedance ratio of $Z_{0e}/Z_{0o} = 3.7$. An HFSS model of sidewall-coupled symmetrically coupled microstrip lines is setup to simulate the achievable Z_{0e}/Z_{0o} ratios, with the splitted half model shown in Fig 4.19. The line width w and gap g are varied with fabrication limitations in mind. As can be see from Tab 4.2, the achievable Z_{0e}/Z_{0o} ratio for the symmetrically coupled microstrip lines is well below the required value. Additionally, the even and odd mode operation of the symmetrically coupled lines has very different field line distribution patterns, as is shown in Fig 4.19. This difference in field line distribution leads to highly different even and odd mode effective dielectric constants due to the high dielectric constant value of Si, as is also shown in Tab 4.2. As a result, the even and odd mode group velocities will be different and the amplitude and phase imbalance of the balun will be affected.

		Z_{0e}/Z_{0o}			ϵ_e/ϵ_o		
		CPW gap g			CPW gap g		
		$6\mu m$	$10\mu m$	$14\mu m$	$6\mu m$	$10\mu m$	$14\mu m$
CPW width w	$6\mu m$	1.64	1.34	1.21	1.44	1.34	1.28
	$10\mu m$	1.59	1.33	1.21	1.44	1.34	1.29
	$14\mu m$	1.54	1.31	1.20	1.45	1.37	1.29

Table 4.2: The even to odd mode characteristic impedance ratios and dielectric constant ratios for different CPW gaps g and widths w.

Instead, the high performance balun is realized by constructing assymetrical coupled lines as shown in Fig 4.20. The input signal line from the single-ended port is the $10\mu m$ wide metal strip (labeled as A) on top of the Si beam. It is shielded away from the ground planes (labeled as C and D) by the $40\mu m$ wide metal strip (labeled as B) on the bottom, so that the input microstrip line characteristic impedance is referenced to metal strip B instead of the ground planes C and D. In order to facilitate a smooth transition to microstrip lines at the balanced outputs of the balun, the ground plane metal strip C is moved to the other side of the Si film, as shown in Fig 4.20(b).

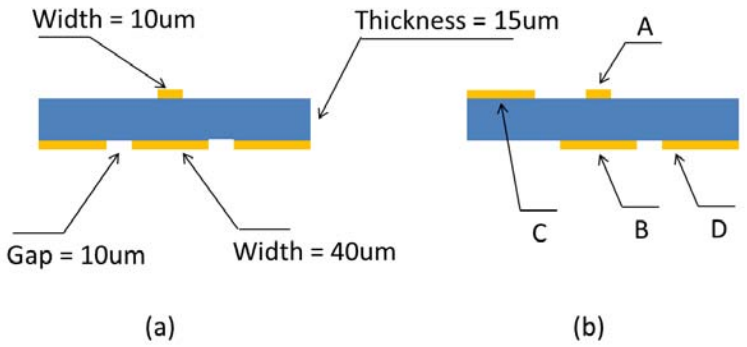

Figure 4.20: (a) Cross section of asymmetrically coupled line structure for Marchand balun, (b) cross section of modified coupled line structure with the metal strip C moved to other side of the Si film.

Another challenge for designing a balun integrated probe is the need for a common mode matching network. As has been discussed in previous sections, the target performance of the balun probe has to reach -5 dB or better for the common mode match term S_{cc}, and -20 dB or better for the common mode conversion S_{cs} (or S_{sc}) and

mixed mode reflection S_{cd} (or S_{dc}). It's clear that the energy conservation requirement for the s-matrix $\mid S_{cd} \mid^2 + \mid S_{cs} \mid^2 + \mid S_{cc} \mid^2 = 1$ no longer holds, which makes the balun probe a lossy three port network. A common mode signal dissipation mechanism has to be introduced, as shown below in Fig 4.21.

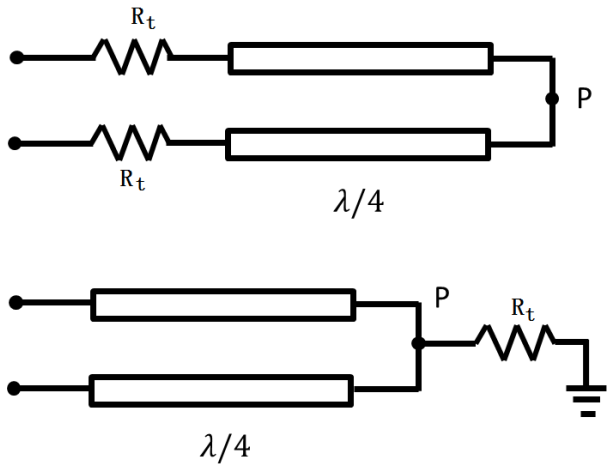

Figure 4.21: Two reported common mode matching network.

There have been a number of common mode matching network designs being reported, with two commonly seen designs shown in Fig 4.21. The first common mode matching network employs two sections of back-to-back connected transmission lines, each of which is connected to a serial resistor R_t. Under differential mode excitation, the point P acts as a virtual ground and provides an open circuit termination for the resistors. Under common mode excitation, the point P acts as a virtual open to provide short circuit termination for the resistors, thus dissipating the common mode energy at the input ports. At frequencies away from band center, the quarter-wave transmission line can no longer make perfect transformation between the virtual open and virtual short, posing unexpected uncertainties to the resistor termination. The second common mode matching network employs two back-to-back connected quarter-wave long shunt stubs, but with serial resistor termination R_t connected at symmetry point Q. Under differential mode excitation, the point Q is a virtual ground, providing an open circuit at the input ports. Under common mode excitation, the

point Q is a virtual open, the termination resistor R_t can be split into two parallel resistors of $2R_t$ serially connected with each stub. If R_t is chosen to be 25 Ohm for stubs of 50 Ohm line characteristic impedance, the resistors will provide a perfect match under common mode excitation and fully dissipate common energy present at the input ports. The second scheme for common mode match always has the symmetry point Q as virtual ground under differential excitation, which shields the termination resistor R_t away from the rest of the circuit, preventing any unnecessary differential mode energy dissipation. As a result, the second design scheme is preferred for common mode match.

Another major difficulty in balun integrated probe design is the integration of these important components into the limited probe chip head area. The aim is to design a balun integrated probe at W-band that is fully compatible with the existing metallic block, and has the potential to be scaled to higher frequencies. As shown in Fig 4.22, the radial stub and quasi-coaxial transmission line section of the probe, which stays inside the probe block channel, is physically similar to that of the GSG probe. What is different is the probe chip head area where the balun structure is housed.

The Marchand balun is realized using two sections of asymmetrically coupled lines as illustrated in Fig 4.23. It has front-side and backside metal strips labeled as A, B, C and D, corresponding to the asymmetrically coupled lines design in Fig 4.20. The singled-ended signal from the probe block channel is first transitioned into the microstrip line that is then fed into the balun probe. The balanced output ports of the Marchand balun are transitioned into GSGSG configured contact pads. The common mode matching network is connected in parallel to the balanced output ports of the Marchand balun.

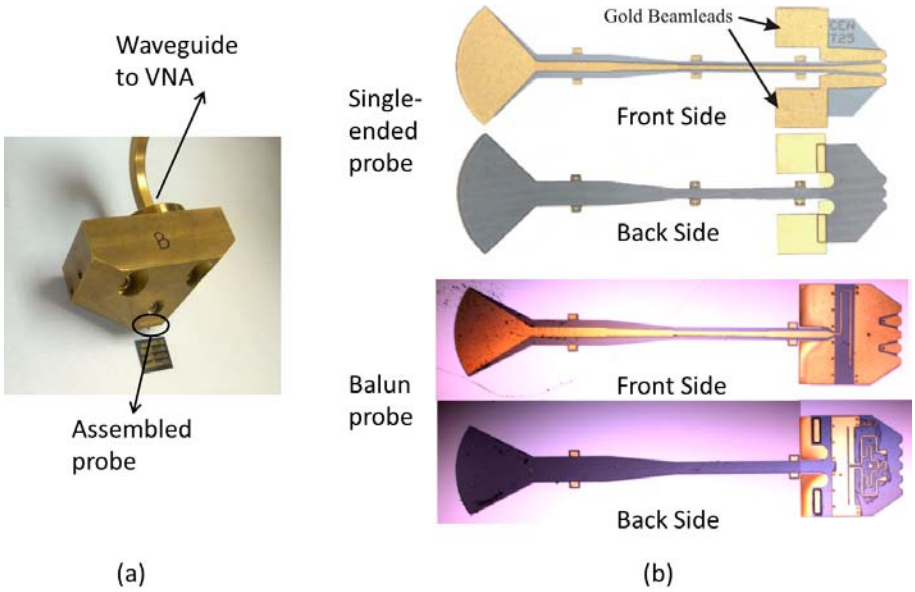

Figure 4.22: (a) The W-band probe block and (b) W-band GSG probe chips (top) and balun integrated probe (bottom).

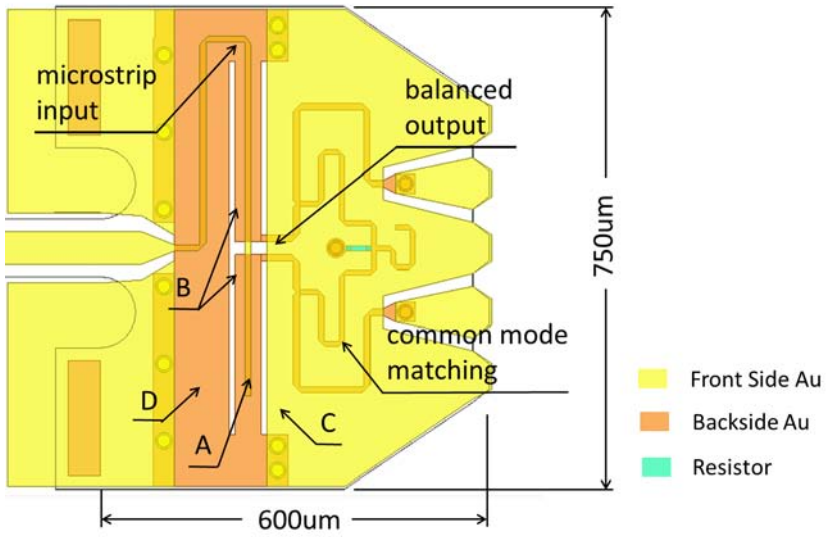

Figure 4.23: An overview of the balun probe head area.

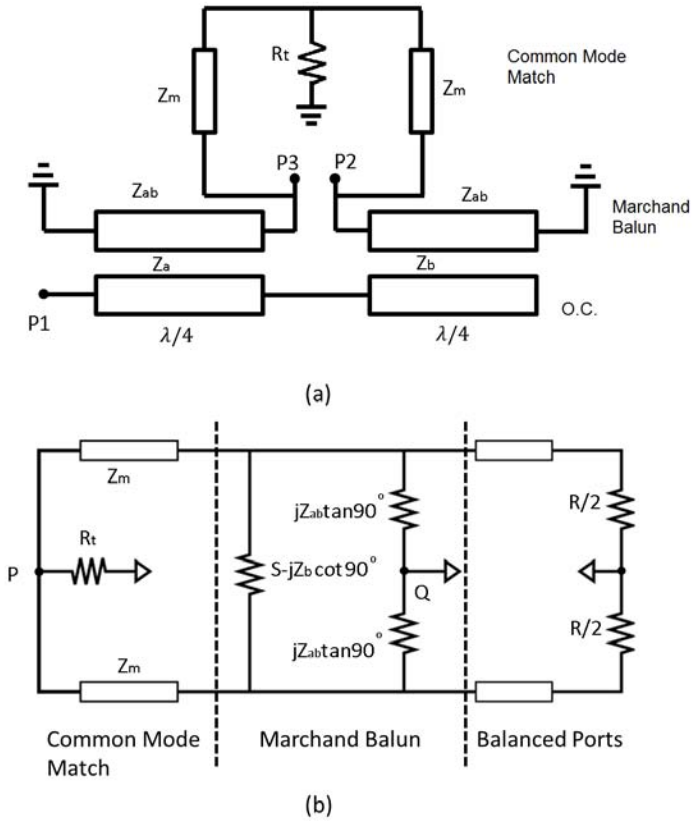

Figure 4.24: Equivalent circuit of Marchand balun with common mode matching network in (a) transmission line representation, (b) lumped element representation.

The equivalent circuit of the balun with common mode matching network is shown in Fig 4.24 for both transmission line representation and lumped element representation. P1 is the single-ended input port with load impedance S (named to keep consistancy with conventions) and a line characteristic impedance of Z_b referenced to the other signal line of the coupler. P2 and P3 are the differential output ports each with load impedance of $R/2$ and line characteristic impedance Z_{ab} referenced to actual ground plane. The common mode matching network consists of two quarter-wave-long transmission lines with a thin film resistor R_t terminated at the symmetry point.

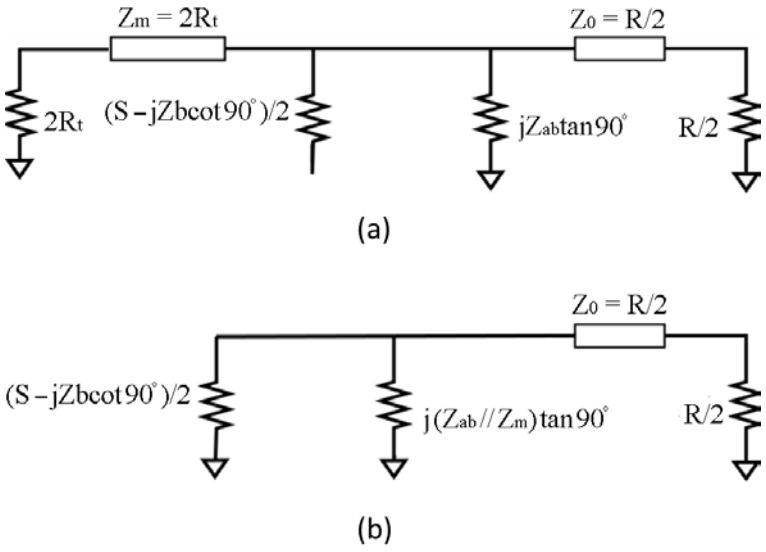

Figure 4.25: (a) The even mode and (b) the odd mode equivalent circuit of the Marchand balun with common mode matching network.

The equivalent circuit shown in Fig 4.24 can be analysed using even and odd mode analysis as shown in Fig 4.25. In the even mode configuration, the termination resistor R_t can be split into two parallel resistors of $2R_t$ to provide a perfect match to the common mode input signal. In the differential mode configuration, the symmetry point is a virtual ground, eliminating the effect of the resistor. This is important because the resistance of the thin film resistor tends to vary across the wafer due to thickness variations in the thin film deposition process used in this work. The circuit layout chosen will prevent variations in the thin film resistor from affecting the differential mode performance. The lines of Z_{ab} and Z_m become two shunt stubs of quarter-wave length that are short-circuited at one end. The differential port is matched to the single-ended port with a shunt stub tuning.

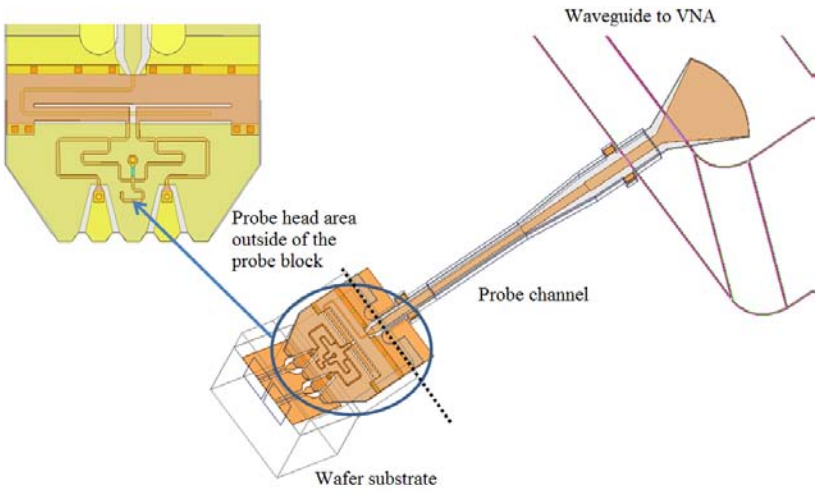

Figure 4.26: Full balun integrated probe model in HFSS.

Shown in Fig 4.26 is the full balun integrated probe model in HFSS. As is the case with a GSG probe, the balun integrated probe sits in a metallic block with a micromachined waveguide bend. The radial stub picks up the RF signal from the waveguide input and transitions into a quasi-coaxial mode of propagation along the channel of the probe block. The geometry of the radial stub and quasi-coaxial line is slightly different from that of the W-band GSG probe, due to different matching and optimization considerations. At the opening of the block channel, the quasi-coaxial line is transitioned into a microstrip line that is fed into the Marchand balun. The two microstrip outputs of the Marchand balun are then transitioned to the probe contact tips in a GSGSG configuration with $100\mu m$ pitch.

The simulation model takes into consideration the conductor loss due to the gold film roughness in the probe chip RF circuitry, as well as the finite conductivity of the brass material in the E-plane split-waveguide and probe channel. The conductivity of the gold film is set to 3.1×10^7 $siemens/m$ instead of the bulk conductivity 4.1×10^7 $siemens/m$, which has been found to account for conductor loss with reasonable accuracy for high frequency GSG probes. The walls of the waveguide as well as the probe channel inside the brass probe block are set to finite conductivity boundary

conditions instead of perfect E boundaries in HFSS simulator, with conductivity equal to that of the bulk brass.

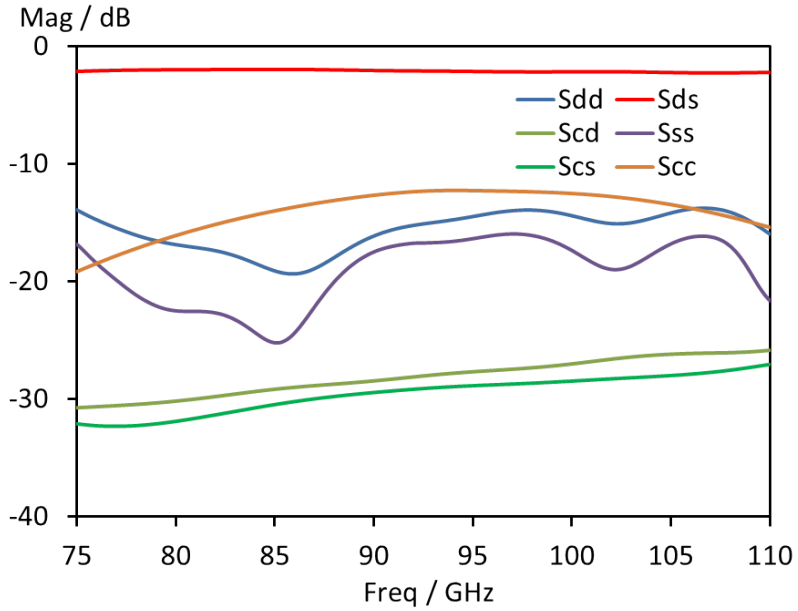

Figure 4.27: Simulated S parameters of a balun integrated probe in HFSS.

The balun integrated probe designed using the approach outlined above meets target performance, as shown in Fig 4.27 for simulated mixed-mode S-parameters from the waveguide port to on-wafer differential port. The single-ended and differential mode return loss S_{ss} and S_{dd} is better than 13dB across the W-band, and the common mode return loss S_{cc} is better than 11dB across the band. The coupling between the common mode and single-ended mode S_{sc}, as well as that between the common mode and differential mode S_{dc}, is better than -26dB across the band. It is also found from simulation that the balun integrated probe can tolerate resistor variations between 20Ω and 30Ω. When the resistance varies within this range, only the S_{cc} term changes significantly. At 25Ω resistor termination, the S_{cc} term is optimized below -10 dB across the frequency range, as shown in Fig 4.27. At 20Ω termination, the the S_{cc} term is better optimized at the lower frequencies. At 30Ω termination, the the S_{cc} term is better optimized at the higher frequencies.

Chapter 5

Balun Integrated Probes Fabrication and Characterization

5.1 Fabrication of Balun Integrated Probe

The balun integrated probe is fabricated using the same SOI processing technology that is used to fabricate a GSG probe. The fabrication process generally follows the process flow outlined in Chapter II with the addition of a resistor layer deposition. An outline of the fabrication process flow is shown in Fig 5.1.

The via-aided alignment scheme is employed for the fabrication of balun probes. On a spin-cleaned SOI wafer, the via holes are first defined and etched, with via alignment markers for both front-side and backside lithography patterning. The etched results are shown in Fig 5.2, with a tilted view of the etched cylindrical vias revealing the straightness of the sidewall. This completes the first step shown in Fig 5.1(a).

After the via hole etch, the front-side gold featured are plated up to $3\mu m$ thick, as shown in Fig 5.3. The SEM images confirm the successful build-up of plated gold inside the vias for electrical connection. This step is shown in Fig 5.1(b).

Then the wafer is flipped over and mounted to a carrier wafer with wafer bond and epoxy. The $450\mu m$ thick handle layer silicon is then removed with a combination of dicing and dry etching, with $1\mu m$ thick silicon oxide layer serving as the stop layer. This oxide layer is subsequently removed using a BOE chemical etch that is highly selective between silicon and silicon oxide, and leaves a clean surface at the revealed

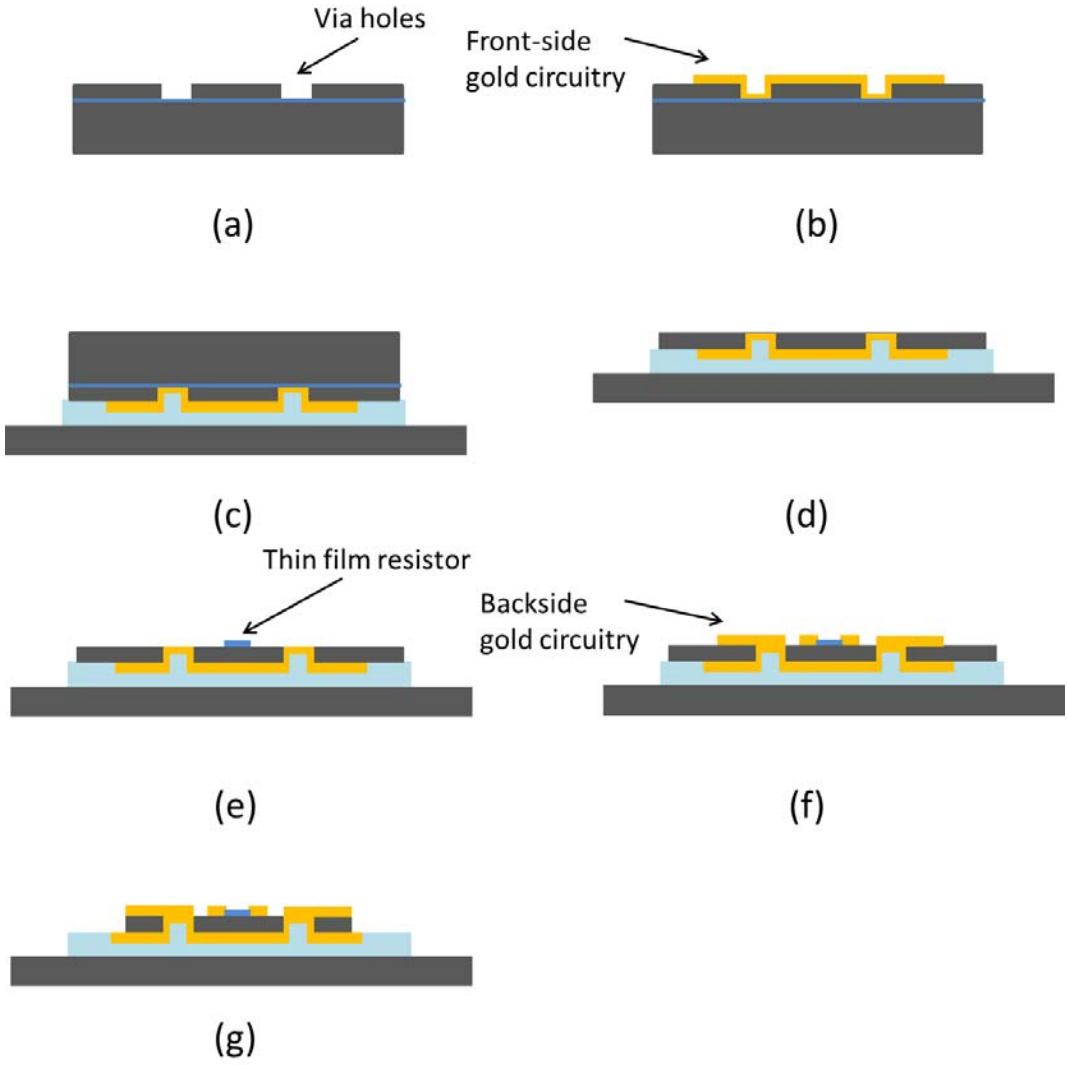

Figure 5.1: The fabrication process flow of a balun integrated probe. (a) via hole etch on clean SOI wafer, (b) gold plating for front-side circuitry definition, (c) SOI wafer backside mounting, (d) the handle and the oxide layer removal, (e) high frequency resistor definition, (f) gold plating for backside circuitry definition, (g) extents etch to define individual probes.

backside of the device Si for further processing. The alignment markers and the vias are clearly revealed at the backside of the device Si layer, as shown in Fig 5.4. These gold alignment markers in bright color can be used to effectively perform a front-side alignment for backside processing. These fabrication steps completes the processes shown in Fig 5.1(c) and (d).

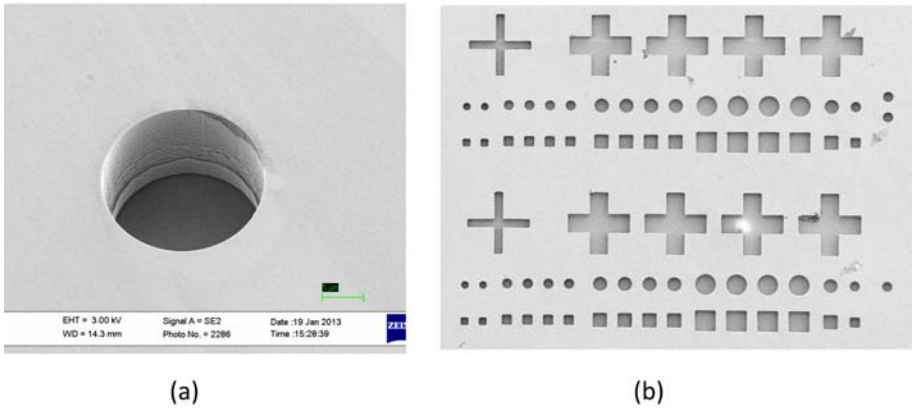

Figure 5.2: (a) Via holes after via hole etch step (front view), (b) via holes after via hole etch step (side view), and (c) via alignment markers.

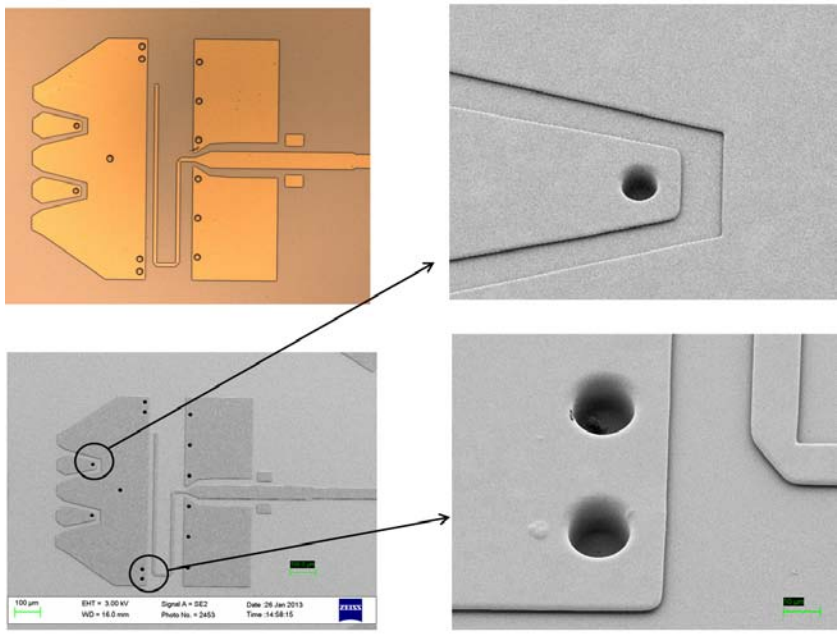

Figure 5.3: Via holes after front-side gold plating.

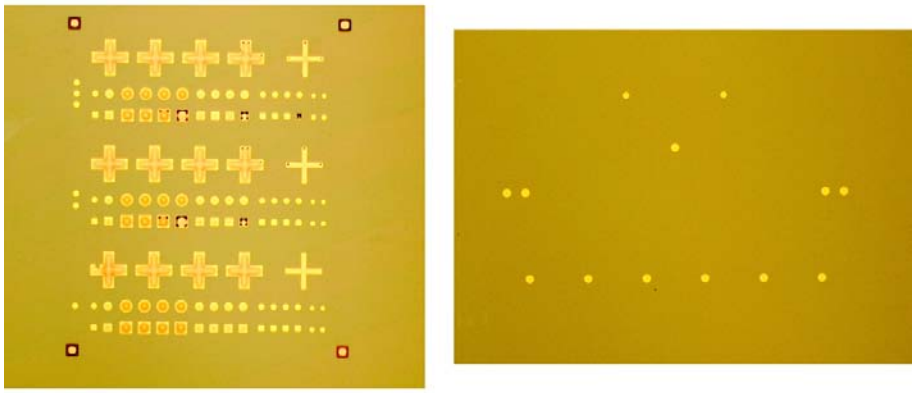

Figure 5.4: Alignment markers and via holes viewed from the backside of the wafer.

Most of the fabrication steps described up to now are the same steps used for fabricating the GSG single-ended probe. The next step is the high frequency thin film resistor definition that is unique to the balun probe fabrication. Prior to the fabrication of the balun integrated probes, a few tests of thin film resitors are performed to determine the correct parameters for fabricating these resistors.

There are two available methods to deposit a resistive thin film at the UVML: (i) a titanium thin film with sputtering deposition on the Sputter3 tool and (ii) a NiCr thin film with eletronic beam deposition. The electron beam tool uses accelerated high energy electrons to physically bombard an ingot of target deposition material. This kinetic energy from the electrons will be absorbed by the ingot through various inter-atomic interactions and be used to heat up the ingot under high vacuum conditions. The ingot can reach such high temperatures that the target material will be transformed into gaseous phase, and deposit on the rotating substrate. The sputtering tool, on the other hand, uses accelerated high energy ions, typically argon, in a target for the bombardment process. The argon ion has a much higher mass and is accelerated to a much higher energy than the electron. When the incoming argon ions' kinetic energy is much higher than the conventional thermal energy ($\gg 1\,eV$),

the atoms of the target deposition material will be ejected from the solid ingot, and get deposited on the wafer substrate.

The target value of the thin film resistor is 25Ω resistance for a resistor of aspect ratio (length/width) 2.5. In order to obtain the correct deposition thickness for the two resistive materials, a few test runs to fabricate DC test resistors are performed. The DC resistors are fabricated and measured using four point resistance measurement technique, the resistive material deposition time is then adjusted until the correct resistance is achieved. It is found that about 20min ebeam deposition of NiCr (approximately 120nm thickness with measured resistivity of $\rho = 1.5 \times 10^{-6}\,\Omega/m$), or 14min sputtering deposition of Ti (approximately 90nm thickness with measured resistivity of $\rho = 6.8 \times 10^{-7}\,\Omega/m$), gives the correct resistance range. The NiCr film is deposited in 3 times, each with 400sec deposition followed by 1hr cooling for the ebeam system. After these test runs with both tools, the Ti sputtering process is chosen for resistive material deposition. During the NiCr deposition with the ebeam tool, the prolonged deposition process produces flakes of NiCr material at the insides of the vacuum chamber, which will contaminate thin film deposition processes with other materials for future users. This is highly undesirable as the tool is shared with other researchers at UVML.

As a result, the resistors are fabricated as rectangularly shaped titanium films using the Sputter3 tool. The resistors definition is achieved with negative photoresist nLof2020 to leave the entire wafer covered with photoresist after the photolithography except for the intended resistor areas. The wafer is then loaded into the vacuum chamber of the Sputter3 tool for titanmium deposition. After titanium deposition, the whole wafer is soaked in a hot bath of NMP and proplyene-glycol solusion mixed in a 1-to-1 ratio and heated to $120°C$. The solution will actively attack the nLof2020 photoresist and break it away from Si substrate, leaving titanium rectangles where the photoresist was not present. This step is shown as Fig 5.1(e).

After the resistor films are deposited, backside gold features are plated to make backside RF circuitry, as well as electrical connection to the resistors. Ti/Au/Ti tri-layer is deposited across the wafer in Sputter3, with 1min deposition time in Sputter3 for each layer, to serve as seed layer for gold plating. The resistor Ti films already deposited on wafer see an in situ 7min ion gun cleaning immediately before the tri-layer deposition. After seed layer deposition, a lithography step is performed to define the backside palting gold features, and the top Ti after the lithography is etched away to expose the Au layer for gold plating. When the gold plating is done, the seed layer must be removed. The top Ti layer across the wafer is dry etched, and the Au layer is wet etched. Then another lithography using resistor definition mask is performed with positive photoresist, which leaves rectangular photoresist features covering the areas of the Ti resistor. The bottom Ti layer is subsequently etched away, with the resistor area covered and thus protected by the photoresist. However, a misalignment of about $1\mu m$ is typically observed between the photoresist and the resistor features. As a result, the resistors are partially exposed to the Ti etch. This misalignment could possibly contribute to the cross-wafer resistance variations if the Ti etch is not even across the wafer. Shown in Fig 5.5 and 5.6 are table microscope images of the balun probes and DC test resistors fabricated at the same time. These steps complete the backside circuitry definition process in Fig 5.1(e).

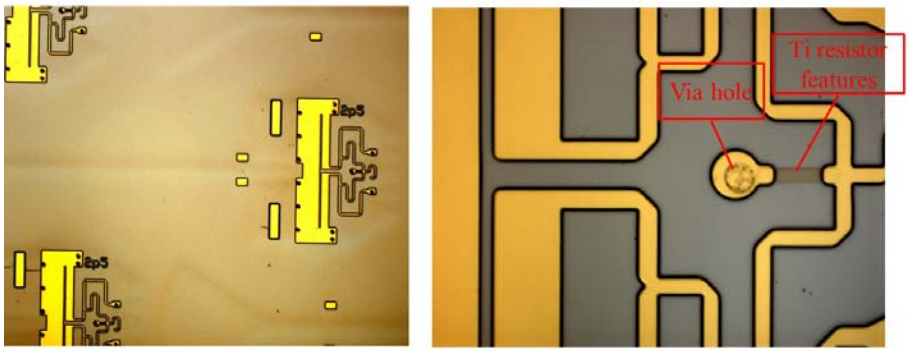

Figure 5.5: Plated backside gold circuit.

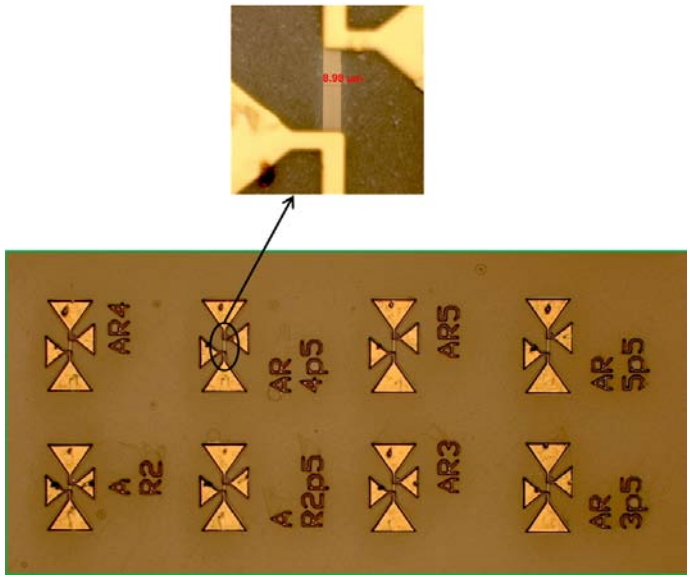

Figure 5.6: DC test resistors with aspect ratios ranging from 2 to 5.5.

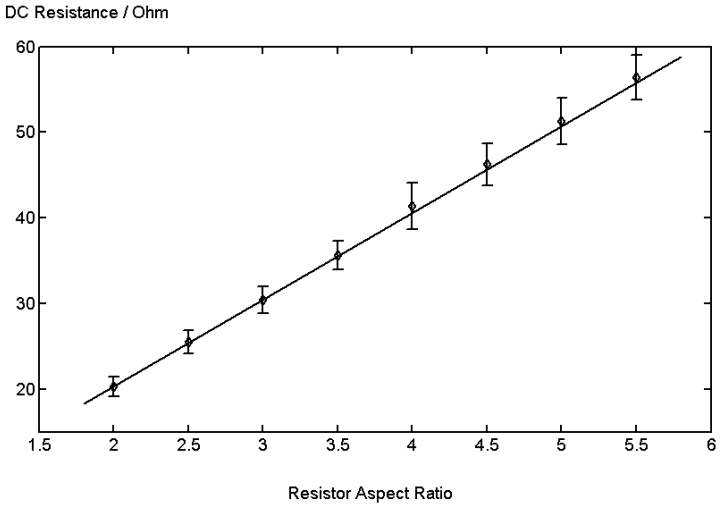

Figure 5.7: Measured resistance for DC test resistors of various aspect ratios with 14min Ti deposition in the Sputter3 tool. Diamond markers stand for the average measured values, error bars are the standard the deviation of the measured resistances at different locations of the wafer, and solid line is the intraplated line from the measurements.

In order to determine the correct deposition time for the target resistance values, DC test resistors of various aspect ratios are fabricated and characterized. There are also test resistors located at different places of the wafer to study the cross-wafer variation of the resistors. A desired DC resistance value of between 25Ω and 30Ω is

to be achieved for a resistor of aspect ratio 2.5 or 3. These resistors are fabricated with different deposition times (and thus different film thickness) and characterized using the four point measurement method. The Ti deposition times are then adjusted until the correct resistance is achieved. It is found that 14min Ti deposition with the Sputter3 tool on SOI wafer gives the desired resistance values, as shown in Fig 5.7. The diamond markers are the average measured resistance values of six differently located resistors, with the standard deviations represented by the error bars. The solid line is the interpolated line through origin. The cross-wafer resistance variation is found to be around 5% of the resistor's actual value.

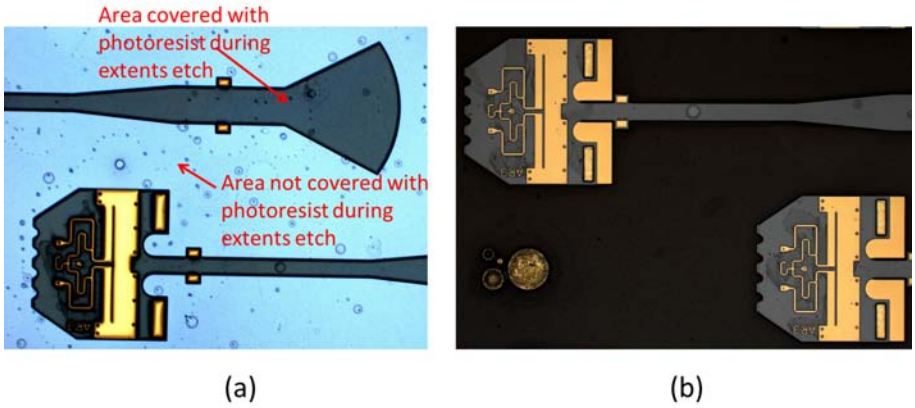

Figure 5.8: (a) After the probe extents lithography, and (b) after extents etch that defines the probe contour.

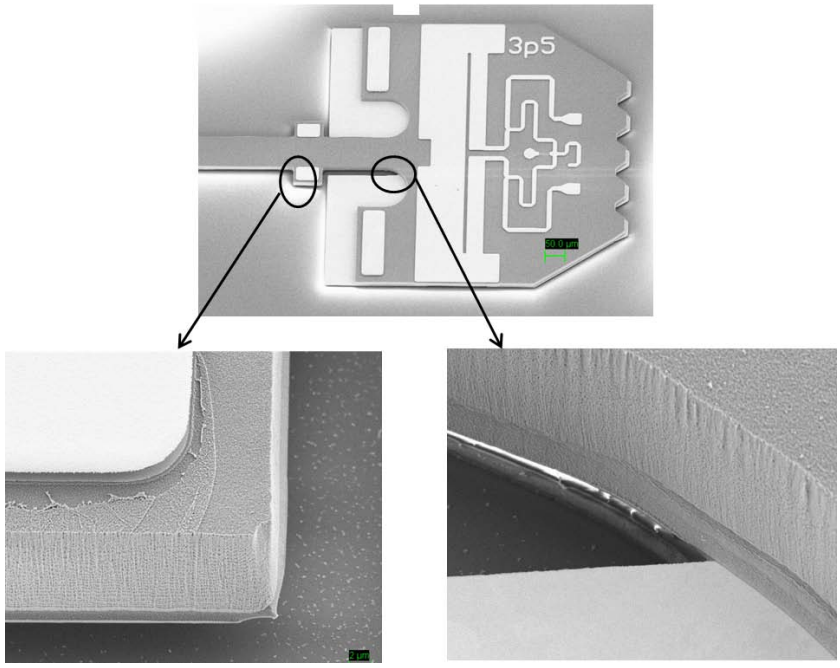

Figure 5.9: SEM images of balun integrated probe details after extents etch, which revealed the straightness of the extents etch.

After backside gold plating, the extents lithography is performed to define the contour of the probe. The probe area is covered with photoresist that will protect it from being attacked during the subsequent extents etch, while the area not covered with photoresist is completely cleaned of silicon during the etch. What remains on the wafer after the extents etch are clearly-defined individual probes ready to be dismounted, as shown in Fig 5.8. Shown in Fig 5.9 are SEM images of probe details after extents etch and photoresist removal. These SEM images confirm that the anisotropic silicon etch recipe for extents etch gives a straight and clean sidewall, as shown in Fig 5.9, which has been found to be important for ensuring probe longevity. The extents etch and the final release of the probe concludes the fabrication process of the balun probes, as shown in Fig 5.1(g).

5.2 Calibration of Terminated Balun Structure

In order to verify the design methodology of the balun circuitry, balun test structures are fabricated in the same wafer run with the balun integrated probes on $15\mu m$ thick Si film, as shown in Fig 5.10. These balun test structures are exactly the same as that on a balun integrated probe for the Marchand balun and common mode matching part, but have CPW output ports that allow for a two-port characterization. One of the balun's differential output ports is terminated with a known load to facilitate a two-port measurement on a three-port device. For each test structure, a total of four identical baluns are fabricated with different terminations (P1 terminated with Γ_1, P1 terminated with Γ_2, P2 terminated with Γ_1, and P2 terminated with Γ_2), so as to provide enough equations to solve for the S-parameters of the balun. TRL calibration standards are also included in the test structures, which set the reference planes right next to the microstrip to CPW transition.

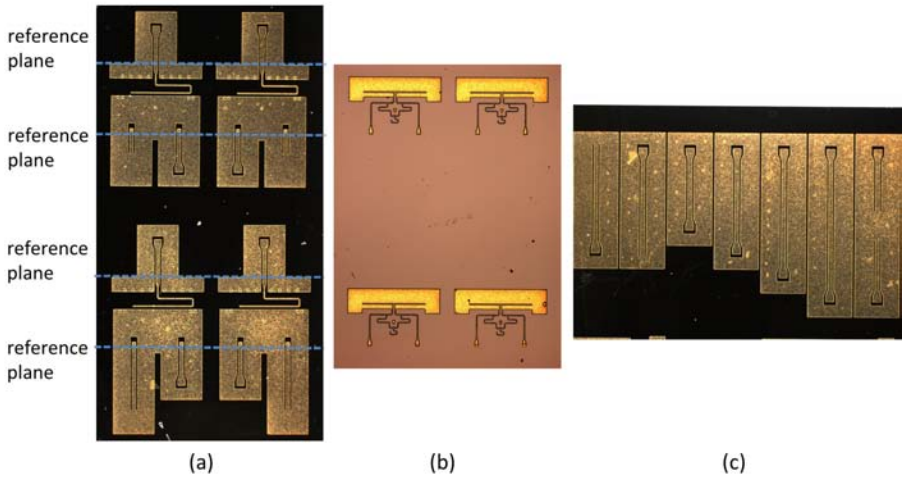

Figure 5.10: (a) Front-side and (b) backside of terminated balun structure, and (c) TRL calibration standards.

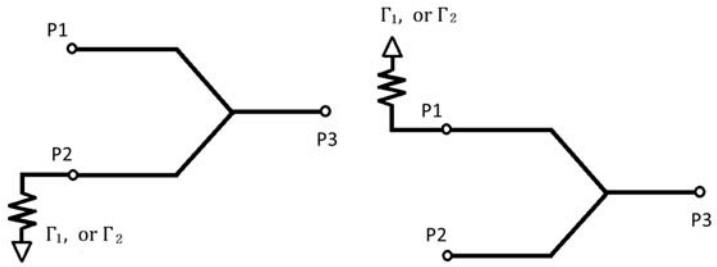

Figure 5.11: Equivalent circuits of the balun device's differential port being terminated with two different known loads.

Shown in Fig 5.11 are the simplified schemes for the four different terminations of the balun test structures. Each of the balun's differential ports, P1 and P2, is terminated with two known loads Γ_1 and Γ_2 once. Using the two-port VNA system, four sets of S-parameters $M^{(i)} = \begin{pmatrix} M_{11}^{(i)} & M_{12}^{(i)} \\ M_{21}^{(i)} & M_{22}^{(i)} \end{pmatrix}$ can be obtained from each measurement, where the superscript i=1, 2, 3 and 4 represent Port 2 being terminated with Γ_1, Port 2 being terminated with Γ_2, Port 1 being terminated with Γ_1 and Port 2 being terminated with Γ_2 respectively. Using the signal flow graph, it is determined that these measured results $M^{(i)}$ are related to the balun s-parameters in the following way,

$$M = \begin{pmatrix} M_{11} & M_{12} \\ M_{21} & M_{22} \end{pmatrix}$$

$$= \begin{pmatrix} S_{11} + \Gamma S_{12}S_{21}/(1-\Gamma S_{22}) & S_{13} + \Gamma S_{12}S_{23}/(1-\Gamma S_{22}) \\ S_{31} + \Gamma S_{32}S_{21}/(1-\Gamma S_{22}) & S_{33} + \Gamma S_{32}S_{23}/(1-\Gamma S_{22}) \end{pmatrix} \tag{5.1}$$

for the case of Port 2 being terminated. Similar equations can be obtained for the case of Port 1 being terminated by changing the subscripts for 1 and 2. It is thus clear that,

$$\begin{cases} M_{11}^{(1)} = S_{11} + \Gamma_1 S_{12} S_{21}/(1 - \Gamma_1 S_{22}) \\ M_{11}^{(2)} = S_{11} + \Gamma_2 S_{12} S_{21}/(1 - \Gamma_2 S_{22}) \\ M_{11}^{(3)} = S_{22} + \Gamma_1 S_{12} S_{21}/(1 - \Gamma_1 S_{11}) \\ M_{11}^{(4)} = S_{22} + \Gamma_2 S_{12} S_{21}/(1 - \Gamma_2 S_{11}) \end{cases} \tag{5.2}$$

By canceling the $S_{12}S_{21}$ term, a linear equations set can be obtained,

$$\begin{cases} (1 - \Gamma_1 M_{11}^{(3)}) \cdot S_{11} + (\Gamma_1 M_{11}^{(1)} - 1) \cdot S_{22} = M_{11}^{(1)} - M_{11}^{(3)} \\ (1 - \Gamma_2 M_{11}^{(4)}) \cdot S_{11} + (\Gamma_2 M_{11}^{(2)} - 1) \cdot S_{22} = M_{11}^{(2)} - M_{11}^{(4)} \end{cases} \tag{5.3}$$

The s-parameters of the balun S_{11} and S_{22} can thus be computed using the equations below,

$$\begin{pmatrix} S_{11} \\ S_{22} \end{pmatrix} = (A^T A)^{-1} \cdot A^T \cdot B \tag{5.4}$$

where $A = \begin{pmatrix} 1 - \Gamma_1 M_{11}^{(3)} & \Gamma_1 M_{11}^{(1)} - 1 \\ 1 - \Gamma_2 M_{11}^{(4)} & \Gamma_2 M_{11}^{(2)} - 1 \end{pmatrix}$, and $B = \begin{pmatrix} M_{11}^{(1)} - M_{11}^{(3)} \\ M_{11}^{(2)} - M_{11}^{(4)} \end{pmatrix}$.

Apply similar analysis to the M_{12} term, it can be obtained that,

$$\begin{cases} M_{12}^{(1)} = S_{13} + \Gamma_1 S_{12} S_{23}/(1 - \Gamma_1 S_{22}) \\ M_{12}^{(2)} = S_{13} + \Gamma_2 S_{12} S_{23}/(1 - \Gamma_2 S_{22}) \\ M_{12}^{(3)} = S_{23} + \Gamma_1 S_{21} S_{13}/(1 - \Gamma_1 S_{11}) \\ M_{12}^{(4)} = S_{23} + \Gamma_2 S_{21} S_{13}/(1 - \Gamma_2 S_{11}) \end{cases} \tag{5.5}$$

Canceling $S_{12}S_{23}$ and $S_{21}S_{13}$ term, the S_{13} and S_{23} terms can be solved as,

$$\begin{cases} S_{13} = \left(M_{12}^{(1)}(1-\Gamma_1 S_{22}) - M_{12}^{(2)}(1-\Gamma_2 S_{22})\right)/(\Gamma_2 S_{22} - \Gamma_1 S_{22}) \\ S_{23} = \left(M_{12}^{(4)}(1-\Gamma_2 S_{11}) - M_{12}^{(3)}(1-\Gamma_1 S_{11})\right)/(\Gamma_2 S_{11} - \Gamma_1 S_{11}) \end{cases} \tag{5.6}$$

And the S_{12} and S_{33} terms can be solved as,

$$\begin{cases} S_{12} = (M_{12}^{(1)} - S_{13})(1-\Gamma_1 S_{22})/(\Gamma_1 S_{23}) \\ S_{33} = M_{22}^{(1)} - \Gamma_1 S_{23}^2/(1-\Gamma_1 S_{22}) \end{cases} \tag{5.7}$$

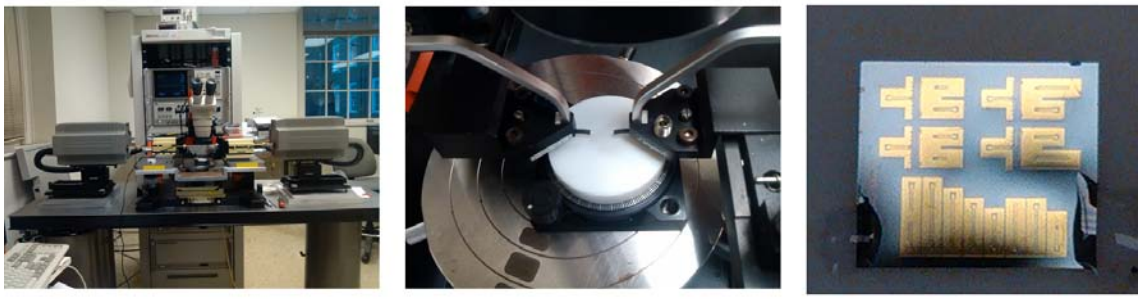

Figure 5.12: (a) HP 8510 two port VNA measurement system with two W-band frequency extender units, (b) closer look at the two GGB Model 120 single-ended probes, and (c) the calibration substrate being attached to teflon block with wax for measurements.

An HP 8510 two port VNA system with W-band frequency extender units (HP 85104A) is set up for the measurement. Two GGB single-ended probes are connected to the waveguide output ports of the frequency extenders to provide two-port on-wafer measurement capability, as shown in Fig 5.12(a) and (b). The balun test chip fabricated on $15\mu m$ thick thin film Si is waxed to a dielectric material stage for mechanical support and to prevent it from sliding during measurement. However, this poses one issue for the balun test structures. The balun test structures have exactly the same geometrical design as the baluns on the probe, which is optimized for it to function in air environment. By placing the test chips on top a dielectric

material stage, one side of the balun test structures is replaced with that dielectric material. This could cause material deviations for the RF response of the balun test structures if the dielectric material has a high dielectric constant compared to air. A teflon block is chosen to be the stage because it has a low dielectric constant $\varepsilon_r = 2.1$ and it's readily available in the cleanroom, as is shown in Fig 5.12(c). The simulation results shown in Fig 5.13 and 5.14 already take into consideration the fact that one side of the balun test structures is filled with teflon material rather than air.

Following the mathematical procedures outlined above, the two-port balun structures can be characterized. The measured results are shown in Fig 5.13 for the three matching S-parameters S_{ss}, S_{dd} and S_{cc}, and in 5.14 for the three mixed-mode S-parameters S_{cs}, S_{dc} and S_{ds}. Overall, the measured results demonstrate a functional balun structure, and agree with the simulated results. The single-ended and differential mode return loss S_{ss} and S_{dd} are both better than 15dB across the frequency band. The common mode return loss S_{cc} is better than 7dB across the frequency band, and is even better at the higher frequency end tracking the simulation results. For the mixed-mode S-parameters, the cross-mode coupling to common mode S_{cs} and S_{dc} are below -22dB across the frequency band, agreeing well with simulation results. The coupling between the differential mode and the single-ended mode is about $1 \backsim 2$dB across the frequency band.

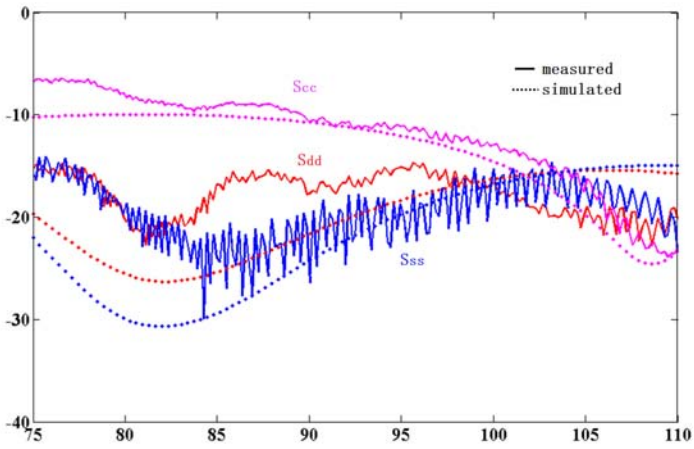

Figure 5.13: The single-ended port matching s-parameter S_{ss}, differential mode matching S_{dd}, and common mode matching S_{cc} of the test balun structure.

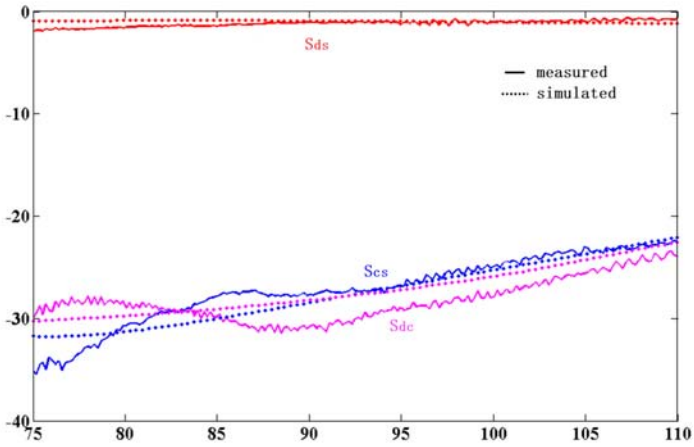

Figure 5.14: The single-ended to common mode coupling s-parameter S_{cs}, differential mode to common mode coupling S_{dc}, and single-ended to differential mode coupling S_{ds} of the test balun structure.

Despite the overall agreement between measured and simulated results, there is also an apparent difference between the two, especially in the lower and higher ends of the frequency band. One possible reason could be uncertainties brought about by placing the thin film chip of test structures on top of the teflon block for measurement. When the test chip is waxed to the teflon block at the edges, it is possible that there are air gaps trapped beneath the chip. This unknown air gap creates uncertainties

that is not captured in the simulation model. A sudden crash of the HP 8510 system prevented further efforts to investigate into this issue.

5.3 Calibration of Balun Integrated Probe

The balun integrated probe is characterized using the probing station shown in Fig 5.15 below, which is same as the setup used to characterize a WR1.5 GSG probe described in Chapter 2.5[3]. A first tier calibration to the waveguide output of the VNA (Rohde Schwarz ZVA-40 with OML V08VNA1-TR X2 90 to 140 GHz frequency extender) is first performed. Then the metallic block assembled with a balun probe is connected to the VNA waveguide output. The balun probe measures the RF response of multiple calibration standards on a substrate, which can be used to compute the S-parameters of the balun probe. The calibration substrate moves with step motors (Newport MFA-CC model motor stage) horizontally to be aligned to the probe tips, and vertically to be in contact and separation with the probe tips. A loadcell (FUTEK model FSH0234) is used to monitor the real-time contact force.

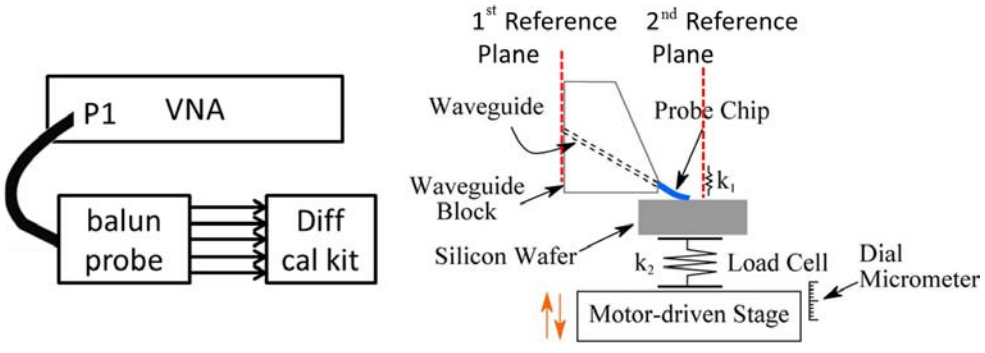

Figure 5.15: A schematic of the probing system and probing stage used for balun probe characterization.

The on-wafer calibration standards are specially designed for balun probe characterization. They compose of two CPW delayed short lines placed adjacent to each

other, as shown in Fig 5.16. The width of the center conductor for the CPW lines is $15\mu m$, and the gap is also $15\mu m$, which gives $50Ohm$ line impedance. These two CPW lines are placed $200\mu m$ next to each other and have very low coupling between the two lines. When the balun probe takes measurements of the calibration standard, the dual delayed short CPW lines can be seen as two independent terminations at the differential output ports of the balun probe. The electrical lengths of the dual delayed short standards are varied independently to provide multiple terminations for balun probe characterization, as shown in Fig 5.16 for the $175\mu m$ step increase in CPW line physical length which corresponds to about 45° for electrical length.

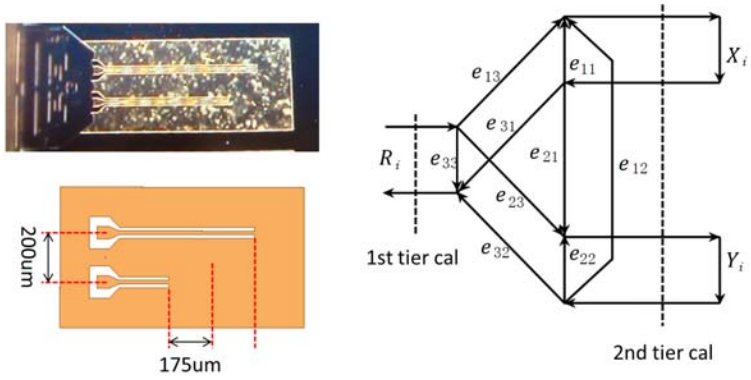

Figure 5.16: The on-wafer calibration standards for balun probe characterization (left) and the signal flow graph of a balun probe measuring the standards (right).

Also shown in Fig 5.16 is the signal flow graph of the balun probe being terminated with dual delayed short standards. The independent terminations at the differential ports are denoted as X_i and Y_i, while the measured reponse at the waveguide port is denoted as R_i. They are related through the S-parameters of the balun probe in the following equations[55],

$$R_i = e_{33} + \frac{e_{31}^2 \cdot X_i + e_{32}^2 \cdot Y_i + \begin{pmatrix} 2e_{32}e_{31}e_{21} \\ -e_{32}^2 e_{11} - e_{31}^2 e_{22} \end{pmatrix} X_i Y_i}{1 - e_{11} \cdot X_i - e_{22} \cdot Y_i + (e_{11}e_{22} - e_{21}^2)\, X_i Y_i} \tag{5.8}$$

where the error network (e_{ij}) is the S-parameters of the balun probe. For n independent measurements on different calibration standards, this equation can be transformed into a set of linear equations,

$$R = M \cdot E \tag{5.9}$$

where $R = \begin{pmatrix} R_1 \\ \vdots \\ R_n \end{pmatrix}$, $M = \begin{pmatrix} X_1R_1 & Y_1R_1 & 1 & Y_1 & X_1 & X_1Y_1R_1 & X_1Y_1 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ X_nR_n & Y_nR_n & 1 & Y_n & X_n & X_nY_nR_n & X_nY_n \end{pmatrix}$, and $E = \begin{pmatrix} e_{11} \\ e_{22} \\ e_{33} \\ e_{32}^2 - e_{22}e_{33} \\ e_{31}^2 - e_{11}e_{33} \\ e_{21}^2 - e_{11}e_{22} \\ \begin{pmatrix} 2e_{32}e_{31}e_{21} + e_{11}e_{22}e_{33} \\ -e_{32}^2e_{11} - e_{31}^2e_{22} - e_{21}^2e_{33} \end{pmatrix} \end{pmatrix}$. It can be seen that at least 7 different measurements have to been obtained to solve this linear equation set. These measurements are obtained using the calibration standards demonstrated in Fig 5.16 by varying the electrical lengths of each delayed short line independently.

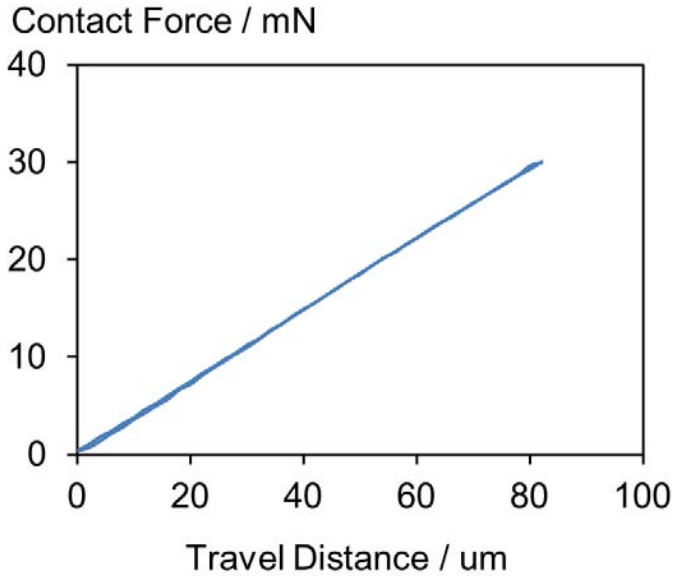

Figure 5.17: The measured contact force v.s. stage vertical travel distance for a typical balun integrated probe.

Using the same experimental setup shown in Fig 5.15, both the mechanical and the RF characteristics are obtained for the balun probes.

Before the RF performance of the balun integrated probe is characterized, the spring constant of the balun integrated probe is first measured. This is used to help determine whether the probe is firmly clamped by the waveguide block. The probe spring constant is obtained by moving the stage up in steps of $2\mu m$ and keeping track of the contact force at the same time. When the contact force reaches 30mN, the stage is then brought down in steps of $2\mu m$ while monitoring the contact force. Experiences with single-ended probes show that the plot for the measured contact force v.s. stage vertical travel distance is typically a straight line, as shown in Fig 5.17, when the probe is firmly clamped by the waveguide block. If the probe is not firmly clamped by the waveguide block, the probe can adjust itself in the probe channel as the contact force increases. This leads to a change in the slope of the force v.s. vertical displacement plot. Using different balun probes of the same mechanical design fabricated in the same run, the interpolated slopes of the force v.s. vertical displacement plot are

measured to be about $0.37\,mN/\mu m$ on average. This interpolated slopes can be seen as the combined effect of two series connected springs, the probe and the loadcell. With the spring constant of the loadcell measured to be $1.07\,mN/\mu m$, the spring constant of the probe can be computed using the following equation,

$$\frac{1}{k_{total}} = \frac{1}{k_{loadcell}} + \frac{1}{k_{probe}} \tag{5.10}$$

which gives the spring constants of the balun probe to be $0.57\,mN/\mu m$.

$400\mu m$-long GSG probe (measured)	GSG probe ANSYS simulation	$600\mu m$-long balun probe (measured)	Balun probe ANSYS simulation
$0.65mN/\mu m$	$0.56mN/\mu m$	$0.57mN/\mu m$	$0.45mN/\mu m$

Table 5.1: Comparison of probe spring constant.

The measured balun probe spring constant is lower than that of a $400\mu m$ long GSG probe [56] as shown in Tab 5.1. It is due to the balun probe's longer probe length, which allows the probe head to deflect more under the same contact force. There is a discrepancy between the measured probe spring constants and the simulated values for both GSG probe and balun probe. This is due to the slight difference in the Si film thickness (specified $\pm 0.5\mu m$ across the wafer for a SOI wafer with $15\mu m$ device layer thickness), which causes variations in the probe spring constants for the fabricated probes.

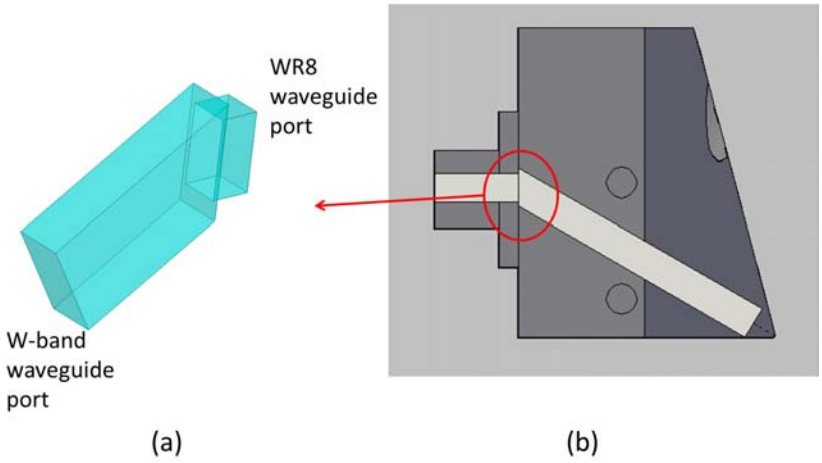

Figure 5.18: The waveguide mismatch from a tilted W-band waveguide interface to WR8 waveguide interface.

Because of the unavailability of W-band (75 to 110 GHz) frequency extenders, the RF performance of the balun integrated probes is characterized using an OML WR8 waveguide band frequency extender, with usable measurements up to 115 GHz due to the cutoff frequency for the W-band waveguide. The waveguide mismatch caused by connecting a W-band waveguide to a WR8 waveguide interface, as shown in Fig 5.18, contributes to the ripple effect in the differential mode and single-ended port reflection coefficient, and is included in the probe simulation model for Fig 5.19 and 5.20.

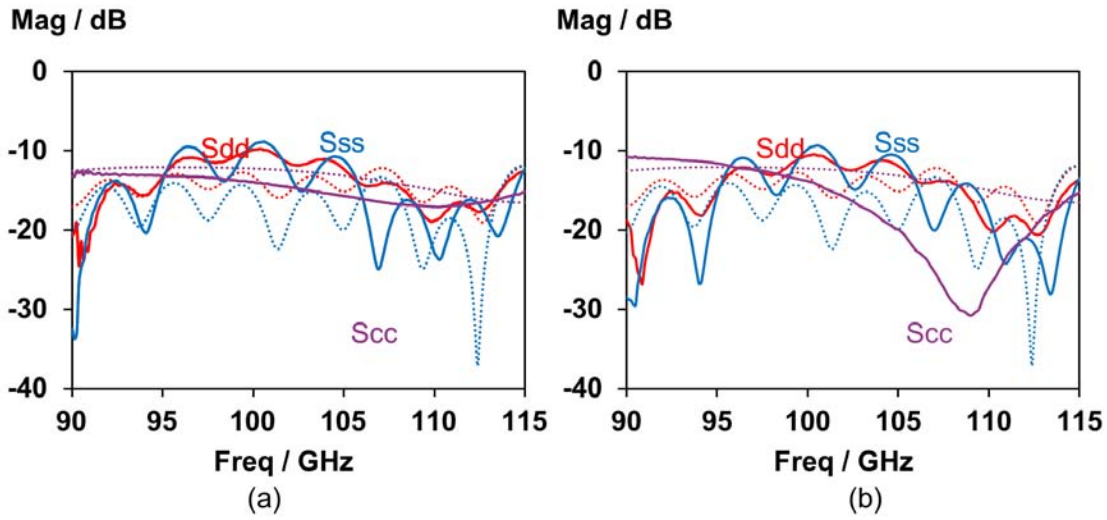

Figure 5.19: The measured return loss S-parameters for the (a) balun integrated probe with resistor aspect ratio of 2.5, and (b) balun integrated probe with resistor aspect ratio of 3. Dashed lines represent simulated results, solid lines represent measured results.

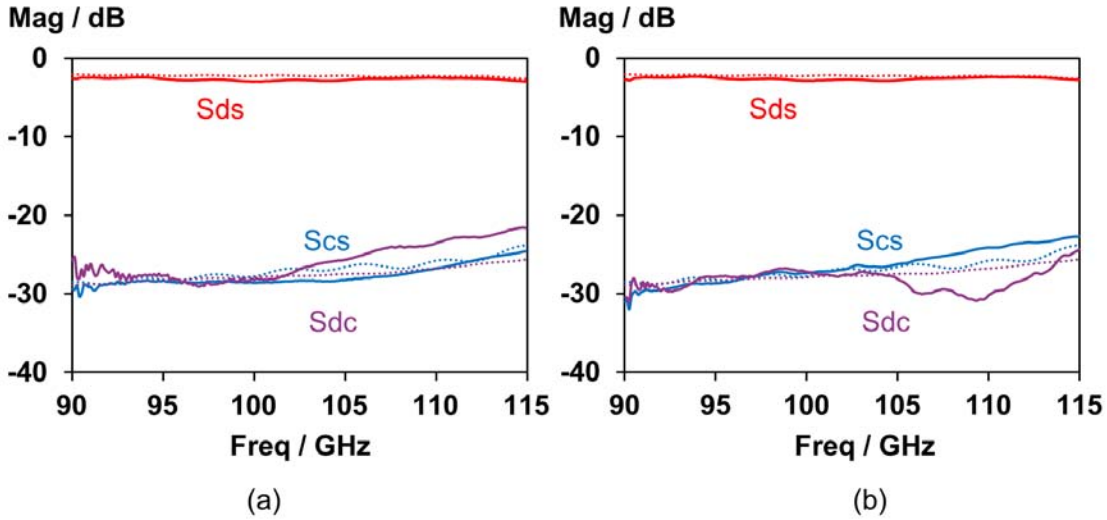

Figure 5.20: The measured cross-mode S-parameters for the (a) balun integrated probe with resistor aspect ratio of 2.5, and (b) balun integrated probe with resistor aspect ratio of 3. Dashed lines represent simulated results, solid lines represent measured results.

The measured RF performance of the balun integrated probe is shown in Fig 5.19 for the three return loss S-parameters, and in Fig 5.20 for the three cross-mode S-parameters. Shown in Fig 5.19(a) and 5.20(a) are the S-parameters for the balun integrated probe with resistor aspect ratio of 2.5 at approximately 25Ω measured

DC resistance. Shown in Fig 5.19(b) and 5.20(b) are the S-parameters for the balun integrated probe with resistor aspect ratio of 3 at approximately 30Ω measured DC resistance. The solid lines are the measured results while the dashed lines are simulated results.

There are a few things to point out from these figures. The measured return loss for the differential mode S_{dd} and the singled-ended port S_{ss} are better than 10dB for most of the frequency band, which fits with simulation. The differential mode match S_{dd} is also not seriously affected by the common mode termination resistor, as is expected from the common mode matching network design. The simulation predicts that the resistance of the termination resistor mainly affect the common mode return loss S_{cc}. This is clearly reflected in the measured results as shown in Fig 5.19. With approximately 30Ω resistor termination, the common mode return loss S_{cc} has a dip at the higher frequency end. When the termination resistor is reduced to approximately 25Ω, the S_{cc} term flatterns and becomes optimized across the frequency band. But the common mode return loss is always better than 10dB across the frequency band for both probes.

Discrepancies between the measured results and the simulated results are apparent. The measured S_{dd}, S_{ss} and S_{cc} terms have shifted in frequencies compared to simulation. This frequency shift is initially thought to be caused by probe tips landing position errors, as has also been seen in higher frequency GSG probes. But further simulation by moving the probe tips contact point forward or backward by $10\mu m$ on probe contact pads doesn't help much in explaining the frequency shift. It is possible that some defects on probe blocks could have contributed to these discrepancies. As is shown in Fig 5.21, there is a dent in the probe channel region of the probe block used, which is from previous usage. The defect in the block structure introduces uncertainties that are not captured in the HFSS simulation model.

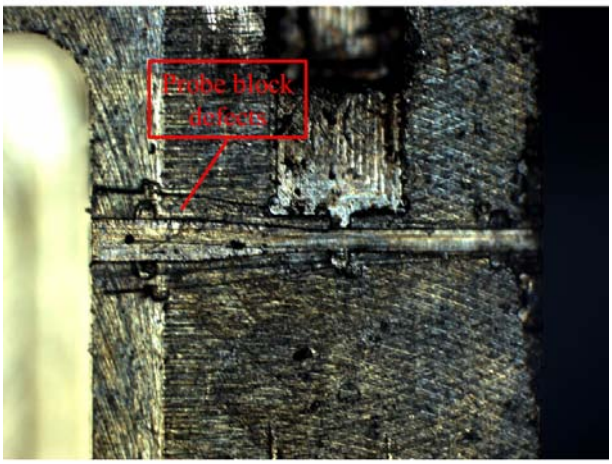

Figure 5.21: The probe block defects from previous usage.

The cross-mode S-parameters, which are more important indicators of balun performance, fit the simulated results very well. The measured coupling between the differential mode and the single-ended modeS_{ds} averages -2.7dB and -2.6dB for the two balun integrated probes, and is better than -3dB across the frequency band for both probes. The measured results have approximately 0.4dB higher loss than the simulated value (0.42dB for the balun probe with resistor aspect ratio 2.5, 0.34dB for the balun probe with resistor aspect ratio 3), however. This discrepancy may arises from the extra conductor loss due to rough metal surface.

The coupling between the common mode and the single-ended port S_{cs}, and the coupling between the common mode and the differential mode S_{dc}, fit the simulated results very well. Although there are discrepancies up to a few dBs between the measured results and the simulated results, the difference in magnitude is low given their small value. These S-parameters are below -25dB for most part of the frequency band, and below -21.6dB and -22.7dB respectively across the frequency range.

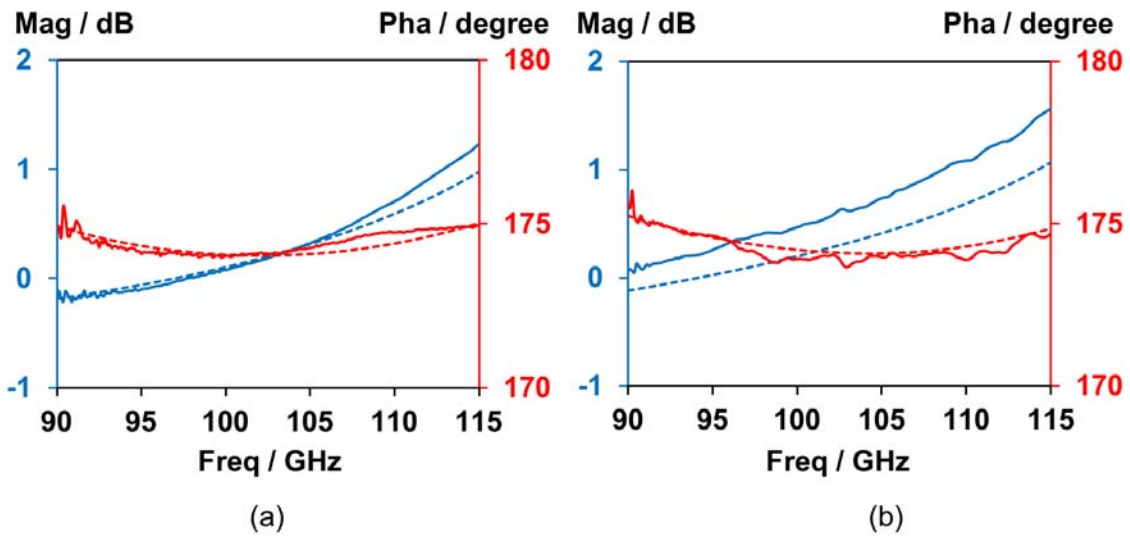

Figure 5.22: The measured amplitude and phase imbalance for the (a) balun integrated probe with resistor aspect ratio of 2.5, and (b) balun integrated probe with resistor aspect ratio of 3.

The performance of the balun integrated probe is sometimes quoted in the amplitude and phase imbalance between the differential signal generated from the probe. They are shown in Fig 5.22 for the balun integrated probes with resistor aspect ratio of 2.5 and 3. The solid lines are the measured magnitude and phase imbalances while the dashed lines are the simulated results. The measured amplitude imbalance is between -0.2dB and 1.23dB for the balun integrated probe with resistor aspect ratio of 2.5, and between 0 and 1.6dB for the balun integrated probe with resistor aspect ratio of 3. Compared to ideal baluns with 180° phase difference between the differential ports, the measured phase difference is between 174.0° and 175.5° for the balun integrated probe with resistor aspect ratio of 2.5, and between 173.7° and 176.0° for the balun integrated probe with resistor aspect ratio of 3. These magnitude and phase imbalances are caused by the geometric asymmetry in the two coupled line sections of the Marchand balun. They are the results of an overall optimization process to reduce generated common mode signal under good port matching conditions. During the design and optimization of the balun probe using HFSS, the probe geometry is varied to achieve lowest common mode signal generation (S_{cs} and S_{cd}) under port match-

ing conditions, which is equivalent to reducing the magnitude and phase imbalances in single-ended s-parameters representation. The measured magnitude imbalance for balun probe of resistor aspect ratio 3 is about 0.3dB higher than simulated results, probably due to slight geometrical difference between the differential branches during fabrication. In general, the measured results for the magnitude and phase imbalances agree well with simulated results.

Overall, the measured s-parameters of the balun probe have good agreement with the simulations, and have reached the proposed target performance. Shown below in Tab 5.2 is a performance comparison between the balun probe demonstrated in this dissertation and other reported works. Compared to a reported balun probe in [57], the balun probe described in this dissertation offers much higher working frequency, and better S_{cc}, S_{cs} and S_{dc} terms for more accurate on-wafer characterization applications. Compared to another reported balun probe in [58], the balun probe described in this dissertation is slightly better in terms of phase and amplitude imbalance, and is much better in terms of S_{cc} since the balun probe reported in [58] does not have a common mode matching network.

	Working Frequency	S_{cs} and S_{dc}	S_{cc}	phase imbalance	magnitude imbalance
Jung et al, IEEE, 2008[57]	3 - 9 GHz	below -20dB upto 7.5GHz	below -5dB	Not Specified	Not Specified
Kim et al, IEEE, 2008[58]	20 - 100 GHz	Not Specified	Not Specified	approx. $\pm 5°$	upto approx. 2dB
this work	90 - 115 GHz	below -22.7dB	below -10.7dB	upto$-6.3°$	upto 1.6dB

Table 5.2: Comparison of balun probe performance between this work and other reported works.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

The rapid development of today's integrated circuits industry is pushing for electronic devices and components at higher and higher frequencies. The capability of being able to perform on-wafer RF characterization is crucial in enabling the mass production and thus wide spread application of these technologies. The on-wafer probing practice not only reduces the time and capital cost needed to characterize microwave integrated circuits working at millimeter-wave frequency range, but also delivers measured results with higher precision and better reliability compared to taking measurements by assembling a die chip to a waveguide structure.

In this dissertation, SOI processing techniques were developed to fabriate novel on-wafer GSG probes using $15\mu m$ thick SOI wafers. These fabrication techniques were also improved over time to improve probe fabrication precision and throughput. The via-aided fabrication processes that is developed based on previous true backside alignment techniques has greatly reduced fabrication complexities and enhanced alignment precision. The fabricated probes have demonstrated excellent electrical repeatability and reliability for on-wafer testing applications. Probes covering frequencies from 140 GHz to as high as 1.1 THz have been fabricated employing the improved processing techniques, and are already commercially available.

With this success in GSG on-wafer probes, it is a well suited extension to the idea to integrate a balun into the existing probe structure. A balun integrated probe at terahertz frequency range provides the research community a convenient tool to characterize differential circuits at such high frequency range. The balun probe is highly desirable in the industry to facilitate design of terahertz differential amplifiers, VCO, LNA and other active components. However, the reported balun probes either work at frequencies lower than 10 GHz [57] or does not have a common mode matching network[49].

In this dissertation, a fully functional balun integrated probe is developed at W-band (75GHz to 110GHz). The balun probe is fully compatible with an existing W-band GSG on-wafer probe block and can be similarly dropped in the block to be assembled. Furthermore, the balun probe has a common mode matching network that is incorporated into the probe structure. The common mode matching network that dissipates reflected common mode signal from the differential DUT is found to be crucial in improving differential DUT characterization precision. The balun probe is fabricated and characterized using CPW dual delayed short standards fabricated on high resistivity Si. The measured S-parameters for the balun probe matches simulation results and reaches proposed target performance requirements. This novel W-band balun probe is scalable to higher frequency, as will be discussed in the next section.

6.2 Future Work

Higher Frequency Balun Probe

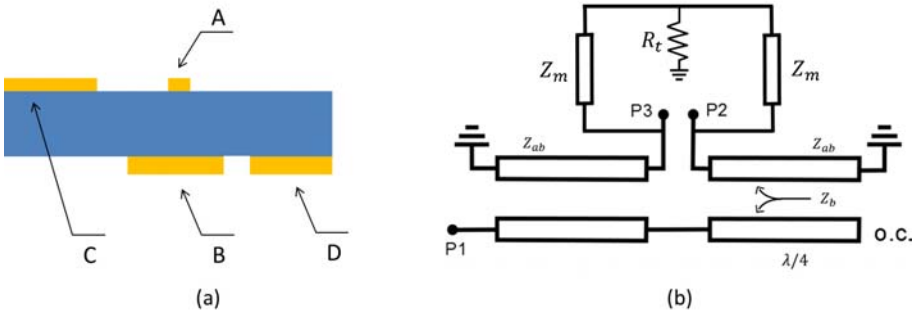

Figure 6.1: (a) Cross-sectional view of the asymmetrical coupled lines for Marchand balun, and (b) the equivalent circuit of the Marchand balun.

In the last few years, there have been quite a few differential amplifiers reported with working frequencies beyond 100GHz[59, 60, 61]. A balun integrated probe that could provide convenient on-wafer characterization for differential devices is thus highly desirable. The prototype balun integrated probe design at W-band, which is demonstrated in this dissertation, can be scaled to higher frequencies to meet this demand.

The core of designing a Marchand balun is to find the proper geometric structure for the asymmetrical coupled lines, as shown in Fig 6.1(a) for the cross-sectional view. Metal strip A is the microstrip input. The kernal of the design is that the metal strip B should be wide enough to shield electrical fields induced by metal A away from the actual ground planes C and D. As a result, the characteristic impedance of metal A (Z_b) is referenced to metal B, and the characteristic impedance of metal B (Z_{ab}) is referenced to actual ground planes C and D. The design process becomes tuning the impedances Z_b, Z_{ab} and their respective electrical lengths to achieve port matching conditions.

At higher frequencies, the novel asymmetrical coupled line structure shown in Fig 6.1(a) is still expected to be valid for the Marchand balun implementation. New optimization processes are needed to fine tune the impedances as well as the electrical lengths of each line. One of the main challenges for accurate simulation of the balun probe beyond W-band will be the thin film resistor modeling.

Thin Film Resistor Modeling

Thin film resistors are crucial for the proper functioning of a balun integrated probe. The common mode reflection term (S_{cc}) of the balun probe is especially susceptible to simulation uncertainties in the thin film resistor at higher frequencies. Additionally, they can be used as potential probe calibration standards complementary to existing delayed-short standards. An accurate simulation model for the thin film resistors at high frequency is thus of key importance to this project.

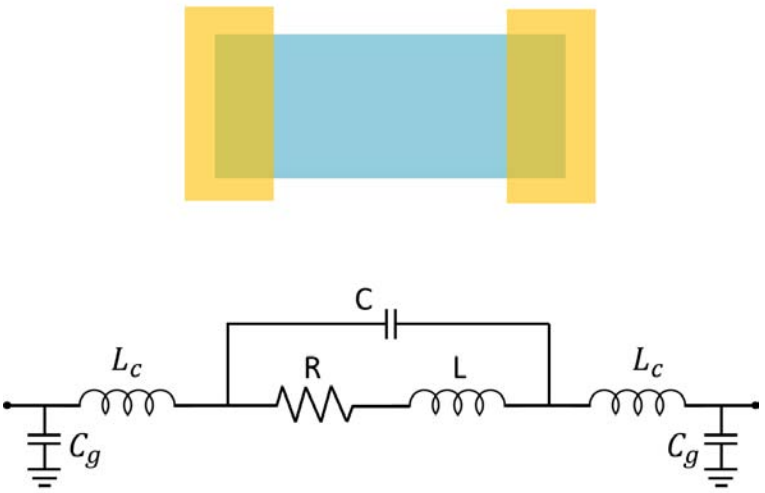

Figure 6.2: The thin film resistor and its equivalent circuit model at high frequencies.

The RF response of the thin film resistors at high frequency can be significantly different from that at lower frequencies. Shown in Fig 6.2 is the high frequency equivalent circuit model for the thin film resistor[62]. The resistor can be modeled using five parameters, the external connection inductance L_c, the external capacitance to ground C_g, the internal shunt capacitance C, the internal inductance L and the internal resistance R. The three parameters C, L and R are associated with the lossy transmission line, while the two parameters L_c and C_g are associated with the step discontinuity of the contact pads. These two parameters can be estimated using the equations provided in [62],

$$C_g = \frac{\frac{1}{2}\left(\frac{\sqrt{\varepsilon_{eff1}}}{c_0 Z_0} - \frac{\varepsilon_0 \varepsilon_r W_1}{h}\right) \cdot (W_1 - W_2)}{1 + \frac{Ah}{l} tanh(8l/h)} \tag{6.1}$$

where $A = exp(-0.1 \cdot exp(2.33 - 2.53W/h))$, ε_{eff} is the effective dielectric constant of the microstrip line contact, c_0 is the speed of light, Z_0 is the characteristic impedance of the microstrip line, W_1 is the width of the microstrip line, W_2 is the width of the resistor, l is the length of the resistor, and h is the thickness of the substrate.

$$L_c = (a(\alpha - 1) - blog(\alpha + c(\alpha - 1)^2))h\,[nH] \tag{6.2}$$

where $a = 40.5$, $b = 75$, $c = 0.2$, and $\alpha = W_1/W_2$.

From these two equations, the two parameters are estimated to be $C_g = 0.074\,fF$ and $L_c = 38.0\,fH$. At the frequency of 1 THz, their reactances are $Z_C = -2150.7j\,\Omega$ and $Z_L = 0.24j\,\Omega$. A series inductor or a parallel capacitor is not going to contribute much to the reactance of the thin film resistor in the frequency range for a scaled balun probe.

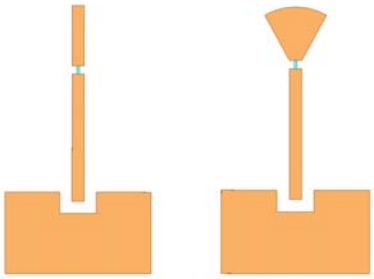

Figure 6.3: High frequency thin film resistors test structures.

At higher frequencies, the electrical length of the thin film resistor, as well as the short termination for the thin film resistor (via hole to the ground plane or open-circuit stub) will also contribute to the reactance part of the thin film resistor. High frequency thin film resistor structures shown in Fig 6.3 need to be designed and characterized to validate the modeling and fabrication consistency of these resistors. The measurement based thin film resistor model will help improve balun probe simulation accuracy.

These resistors are already fabricated with working frequency as high as 330GHz and are now waiting to be characterized.

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