SUB-MICROWATT POWER MANAGEMENT CIRCUITS AND SYSTEMS FOR SELF-POWERED INTERNET-OF-THINGS APPLICATIONS

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Abstract

Emerging trillions of wireless sensor nodes for Internet-of-Things (IoT) applications, such as wearable healthcare, structure health monitoring, and smart home and cities, are dramatically improving our life quality and productivity. To truly enable the IoT era, those sensor nodes need to be fully autonomous and deployable, which requires them to have ultra-low power consumption to increase life time, self-powered and batteryless capability to avoid frequent and a large number of battery change, and highly efficient power delivery train to enable deployment under a variety of environmental conditions.

To meet those requirements, the design of power management units (PMUs) including energy harvesting interface circuits and voltage regulators for self-powered system-on-chips (SoCs) is becoming critical and challenging. Especially, in recent years, with power consumption of different loading components gradually reducing from µW down to nW or even pW, and reduced energy from energy harvesters due to limited form factor and energy availability in the environment, PMUs need to be power efficient enough to deliver pW to nW output power from energy sources to loads, which requires them to have ultra-low quiescent power within sub-µW range and meanwhile maintain a high performance.

This dissertation aims to explore sub-µW, high-performance, and highly power-efficient architectures for power management circuits and systems, which includes two main categories and covers the entire power delivery train for self-powered IoT systems. The first category is from energy harvesting perspective looking into how to extract maximum energy from the environment. The potential approaches include using high performance energy harvesting interface circuits, highly efficient maximum-power-point tracking schemes, energy extraction from multi-modal energy sources, and single-stage power delivery architectures. By extracting more energy from the environment, it opens up more applications where energy limits the deployment of wireless sensor

nodes. The second category in this dissertation explores how to design voltage regulators to efficiently power nW loads, which requires voltage regulators themselves to consume nW or sub-nW quiescent power. In this category, we provide a complete sub-nW power management solution including low-dropout regulators and a bandgap voltage reference. To achieve the goals for these two categories, four research work has been conducted in this dissertation.

The first research explores a highly efficient piezoelectric energy harvesting system with maximum power-point tracking (MPPT). Piezoelectric energy harvesting interface can determine how much power can be extracted from transducers and a proper MPPT scheme needs to be used to match the transducer impedance with the impedance of interface circuits to extract maximum energy. In this work, a high-performance parallel synchronized-switch harvesting-on-inductor (SSHI) rectifier with >400% figure-of-merit (FOM) has been implemented together with a highly efficient MPPT scheme with >95% tracking efficiency. To achieve such high tracking efficiency, we used perturb & observe (P&O) algorithm for the MPPT and proposed an analog power monitor to implement the P&O algorithm.

The second work in the energy harvesting category is to design a multi-input single-inductor multi-output (MISIMO) energy harvesting and power management unit (EHPMU) with nW quiescent power. This MISIMO EHPMU can extract energy from thermal, solar and vibration energy simultaneously and provide four voltage outputs for loads, which greatly extends the energy extraction and power delivery capability. It also integrates a multi-modal cold start-up block and combines the energy harvesting interfaces and voltage regulators in one power stage to minimize the form factor and eliminate the cascaded power loss. Measurement results show the EHPMU achieves 32nA quiescent current, 1.2×10^5 dynamic range, and an 80% power efficiency at 1μW output power and can cold start from three different energy sources.

The next two research provides a sub-nW power management solution for nW IoT systems. The first work is to explore the design space of sub-nA low dropout regulators (LDOs), which

includes two designs, a digital LDO (DLDO) and an analog LDO (ALDO). The DLDO uses a hybrid synchronous and asynchronous control scheme and keeps an ultra-low quiescent power consumption, which achieves the lowest 745pA quiescent current with a widest 3.8×10^5 dynamic load range. It also supports a fast load transient response through the asynchronous path. As a comparison, a traditional fully integrated sub-nA ALDO using an analog feedback loop is also presented, which also achieves sub-nW power consumption and is well suited for powering analog and RF blocks in fully integrated nW IoT systems.

The final work is to design a sub-nW bandgap reference (BGR) with a wide input voltage range. By directly biasing the bipolar junction transistors (BJTs) with pA current and using an input charge pump with configurable gain to increase input voltage range, the proposed BGR achieves a 930pW power consumption at 0.45V and an input voltage range from 0.45V up to 3.3V in simulations. The designed sub-nW BGR can be used together with sub-nW voltage regulators to generate voltage supplies with a good stability against process, voltage and temperature (PVT) variation.

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Chapter 1

1. Introduction

1.1 Background

Internet-of-Things (IoT) devices with the capability of sensing, digital processing, and wireless communication are becoming an essential part of our daily lives [1], such as wearable healthcare, environmental monitoring, and smart home and cities. They are also playing an important role in industry and agriculture field. [2] Those IoT devices usually collect data from different types of sensors, process those data through digital processors, and transmit them to the cloud, as shown in Figure 1-1. According to latest survey and prediction, there are already nearly

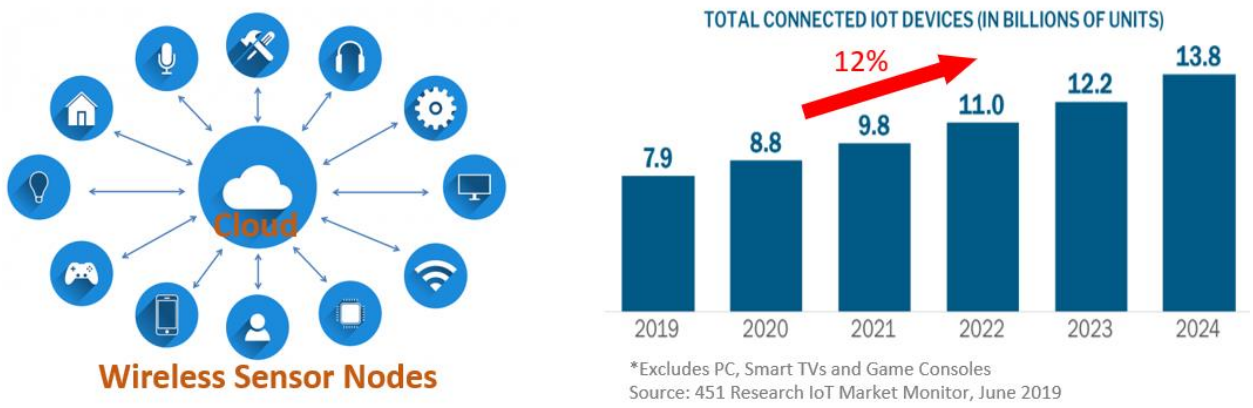


Figure 1-1 Wireless sensor nodes keeping a rapid growth rate in recent years.

8 billion IoT devices in 2019 and the growth rate is around 12% each year. Such large number of devices and rapid growth rate bring many challenges for IoT sensor node design and deployment in the real life, such as device miniaturization, effective wireless communication, power consumption reduction, etc.

Among all the challenges, how to manage the power delivery for those large number of IoT devices effectively is becoming very critical. Traditional IoT nodes heavily rely on the battery as the power source, so the main drawback is that they need frequent battery replacement, which is not practical for the incoming billions of sensor nodes deployed in the near future. Alternatively,

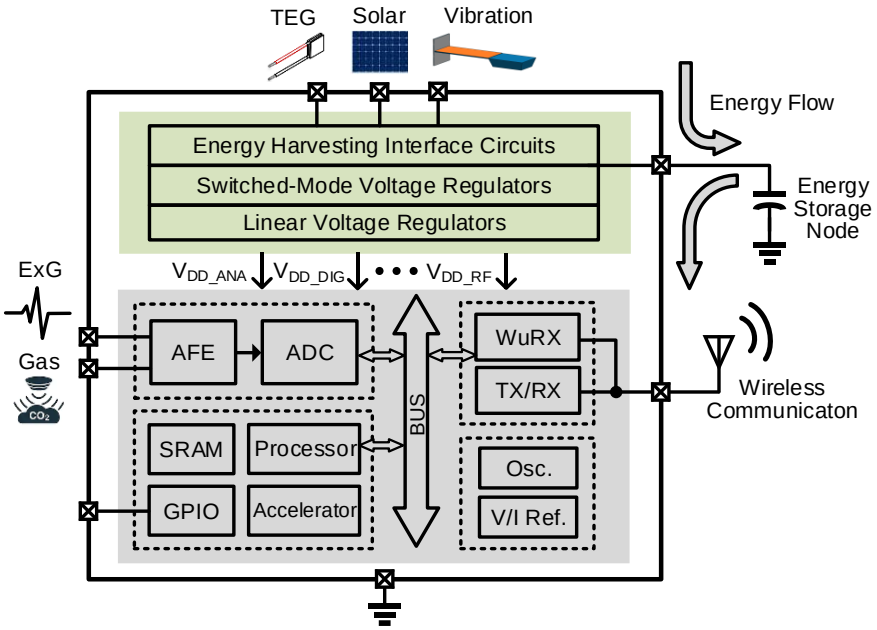


Figure 1-2 System block diagram of a typical self-powered IoT SoC.

self-powered and batteryless wireless sensor nodes [3]-[5] are becoming a solution for the next-generation IoT devices, which overcome the battery issue by using energy harvesting technology to extract energy directly from environment and store energy on supercapacitors. Energy harvesting devices eliminate the battery-replacement issue and also has the benefits of long cycle life and being environmentally friendly. To implement such a self-powered and energy harvesting

IoT devices, one of the critical blocks is the power management unit (PMU) including the energy harvesting interface circuits and voltage regulators.

Figure 1-2 shows a typical system block diagram of a self-powered IoT system-on-chip (SoC), which integrates all the necessary functions of a wireless senor node on chip. The signal processing path includes sensor interfaces for data sensing and collection, digital processors and memory for data processing and storage, RF transceivers for wireless communication, and other supportive blocks, such as voltage references and clocks. The power delivery path includes energy harvesting interfaces and different types of voltage regulators, and an off-chip energy storage node. In this dissertation, we will mainly focus on the components on the power delivery path.

1.2 Power Delivery Path in a Self-Powered System-on-Chip

There are many types of energy existing in the environment with different modalities. The common energy sources include thermal energy, solar energy, vibration energy, etc. Energy harvesting and power management unit (EHPMU) in a self-powered SoC is used to extract those energy from the environment to power load circuits, which includes the energy harvesting interfaces and voltage regulators shown in Figure 1-3. On the power delivery path, the energy harvesting circuits first extract the ambient energy from energy transducers and then the energy is stored on the energy storage node, such as a supercapacitor and allocated to the loads using different kinds of voltage regulators. Switched-mode voltage regulators, such as inductor-based regulators or switched-capacitor regulators, have a high power-efficiency, so they are usually used as the first stage to transfer the energy from high voltage to low voltage. Generally, linear voltage regulators, such as low dropout regulators (LDOs), are used as the last stage to provide a clean voltage and fast transient response for loads. In addition, voltage references are usually needed as a supportive block to provide an accurate voltage values to generate voltage supplies, which should have a good stability against temperature variation.

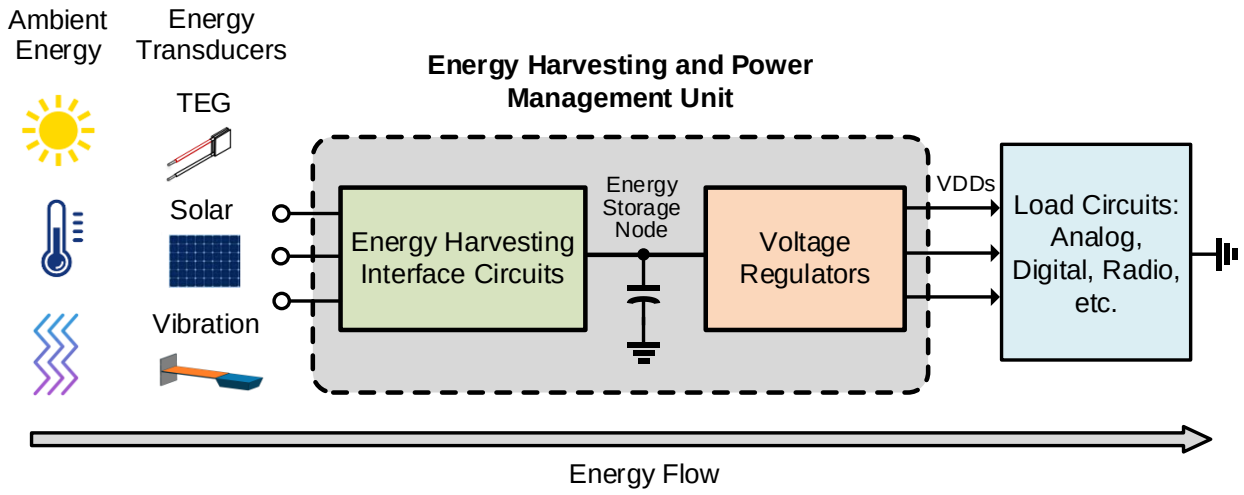
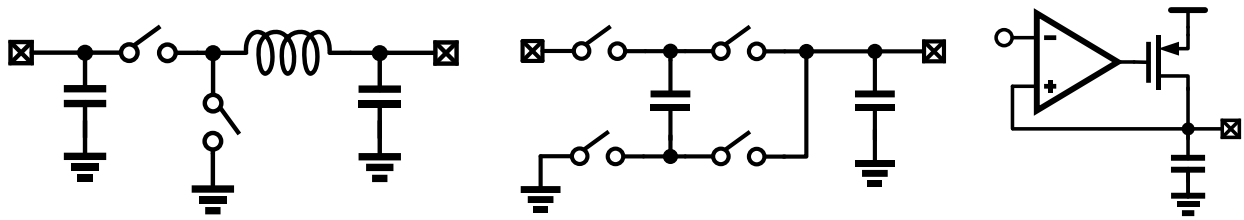


Figure 1-3 Illustration of energy flow and EHPMU for IoT SoCs.

1.2.1 Topologies of Power Converters

EHPMUs are essentially power converters, so to fully understand the EHPMU working principle, we need to look into the topologies of different power converters, which are shown in Figure 1-4. There are usually three power converter topologies, inductor-based, switched-capacitor-based, and linear voltage regulator. The inductor-based voltage regulators are widely used as the main converter at the first stage due to the advantages of high power-efficiency. Theoretically, the maximum efficiency could be up to 100 percent. However, it needs off-chip inductors, which means it has a high cost and increases the form factor. So, it is not suitable for fully integrated applications. The main advantage of switched-capacitor voltage regulator is that it can be fully integrated on chip, however the power efficiency is not as high as inductor-based regulator due to the intrinsic charge-redistribution power loss. It is also widely adopted as a local power-conversion circuitry, such as charge pumps for cold start-up circuits. The linear voltage regulator, such as a low dropout regulator (LDO), has a power efficiency related to the input and output voltage ratio, which means when the input voltage is much higher than output voltage, the power efficiency is very low. LDOs have the advantages of providing fast transient response and

clean voltage supplies to the loads, so it is usually used at the last stage on the power delivery path, especially for powering analog and radio-frequency (RF) circuits. Also, LDOs have a low design complexity and low cost compared with inductor-based or switched-capacitor based voltage regulators, so LDOs are usually used together with switching voltage regulators to provide voltage domains for different loads



(a) (b) (c)

Figure 1-4 Power converter topologies of (a) inductor-based voltage regulator; (b) switched-capacitor voltage regulator; (c) linear voltage regulator.

How to choose different power converter architectures for ultra-low-power (ULP) IoT systems depends on the characteristics, which are introduced above. Generally, either an inductor-based or switched-capacitor-based voltage regulator is used to down convert the high voltage from the supercapacitor. Then LDOs are used if there are multiple voltage domains are needs in the systems for different loads, such as analog, digital and RF circuits.

1.2.2 Design Considerations and Key Metrics

There are many design considerations for EHPMUs. Specifically, the energy harvesting (EH) side must convert energy from energy transducers to a usable voltage level for storage, so EH circuits need to manage maximum-power-point tracking (MPPT), cold start-up, a wide input power range, etc. The voltage regulator (VR) side deals with the output to the loads, which needs to manage a wide output power range, transient response, output voltage ripple, etc. Among all

those metrics, the EH conversion efficiency and voltage regulator power efficiency rank as highly important. Some of the common metrics for both of the EH and VR are listed and explained below.

- Power/Conversion Efficiency: This efficiency equals to P_{OUT} / P_{IN}, which stands for how much power delivered to output loads from input sources. A higher efficiency means lower power loss and a more effective power delivery.

- Quiescent Power: Quiescent power is the power consumption when a power converter works at steady state. For a switching voltage regulator or energy harvesting circuits, the lowest quiescent power is the power consumption when EH input power and VR output power are equal to zero, which means it does not have any power delivery, so the conduction and switching power loss is not included. For an LDO, the quiescent current is the steady-state current consumption of the whole LDO circuit.

There are also some metrics specifically for energy harvesting interface circuits.

- Cold start-up: When the energy storage node is totally out of charge, the EH needs initial energy and voltage to make itself start to work. The mechanism which makes the EH circuit boot is called cold start-up. One of the key metrics for cold start-up circuit is the minimum cold start-up voltage, which usually limits the minimum energy needed in the environment to make self-powered devices work.

- Maximum-power-point tracking (MPPT): According to maximum power transfer theorem, to extract the maximum energy, the input impedance of EH circuit has to equal to the output impedance of energy transducers. The mechanism of tracking the maximum power-point of the energy harvester is called MPPT.

- Energy-extraction improvement/gain for piezoelectric energy harvesters (PEHs): The energy-extraction improvement or gain, which is also called Figure of Merit (FOM) is defined in [6],

$$FOM_1 = P_{REC} \Big/ \left(C_P \cdot {V_{OC}}^2 \cdot f \right) \tag{1.1}$$

where P_{REC}, C_P, V_{OC} and f stand for rectifier output power, PEH parasitic capacitance, PEH open-circuit voltage, and vibration frequency. This FOM represents energy-extraction capability of the rectifier by normalizing its output power with the ideal full-bridge rectifier (FBR). There are a second FOM [7], which normalizes its output power with on-chip FBR, so in the comparison, it counts the FBR on-chip loss.

$$FOM_2 = P_{REC} \Big/ P_{FBR\_OC} \tag{1.2}$$

The following metrics are specifically for the voltage regulators including transient response, output ripple or noise, and dynamic range explained below.

- Transient Response: Transient response is the voltage supply response to the load step change, which presents how quickly the voltage supply can recover to its original value. It is characterized by several parameters, such as load step size, voltage droop, response time and settling time.
- Output Ripple/Noise: For some supply sensitive circuits, such as analog or RF blocks, the ripple and noise on the power supply could affect the sensitivity and signal quality. So, the output ripple/noise should always be minimized.
- Dynamic Range: The dynamic range is the output power range that voltage regulators can delivery to the loads. For a switching voltage regulator with pulse-frequency modulation (PFM), the highest boundary is limited by the maximum switching frequency and the lowest boundary is limited by the quiescent power and acceptable power efficiency.

There are multiple design tradeoffs between those parameters. For example, reducing quiescent power means slow bandwidth in the control loop, which leads to a slow transient response, but low quiescent power can help with the efficiency when output power is very low and it also increases

the dynamic range. So, one of the challenges to design ULP PMUs is to create circuit structures and control schemes to achieve better tradeoffs between those parameters.

1.3 Sub-microWatt Power Management Circuits and Systems

Reducing PMU quiescent power is critical to improve the total power efficiency of the whole power deliver train. Specifically, for modern nW-μW IoT devices, the PMU quiescent power should target for the sub-μW range to achieve a high efficiency. The power efficiency, η, of a switching voltage regulator is equal to the output power divided by output power plus total power loss.

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_Q + P_{SW} + P_{COND}} \tag{1.3}$$

where P_{IN}, P_{OUT}, P_Q, P_{SW}, and P_{COND} stand for the power converter input power, output power, quiescent power, switching loss and conduction loss. Figure 1-5 shows an illustration of power efficient versus output power, in which we can find when the output power is very high, the power efficiency is mainly limited by the conduction loss or switching loss depending on the modulation scheme and when the output power is reduced down to sub-μW level, the power efficiency is mainly limited by the quiescent power. As a result, reducing quiescent power dramatically increases the power efficiency at the low end and also helps increase the total dynamic range.

Reducing quiescent power and keeping a high efficiency at low output power means there are more power delivered to the loads, which relieves the requirement on minimum available energy in the environment to power self-powered IoT devices. Another benefit of reducing quiescent power is to increase system life time. Especially when the system is in the sleep mode or turned off and there is no power delivery in the PMUs, the quiescent power dominants the total power consumption of the system at this situation.

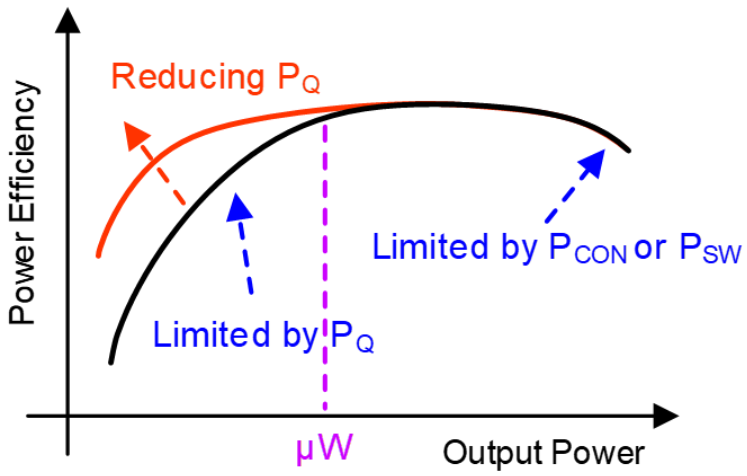


Figure 1-5 Illustration of power efficiency versus output power.

1.3.1 Highly Efficient Energy Harvesting System

As we already know, EHPMU essentially works as a bridge for power delivery between energy transducers at the input and load circuits at the output. From the input perspective, the power density of different energy transducers needs to be considered. As shown in Table 1-1, under normal conditions, the power density of thermal electric generate (TEG), photovoltaic (PV) cell, and piezoelectric energy harvester is from a few μW to tens of μW per square centimeter, which means, if under poor environmental conditions or using millimeter-size transducers, there is only a few μW or less power available, so reducing EHPMU quiescent power down to sub-μW helps keep a high conversion efficiency under those conditions.

Table 1-1 Power density of different types of energy harvesters [8] [9]

Energy Harvesters	Conditions	Power Density
PV Cells	Indoor	10's $\mu W/cm^2$
TEG	5°C gradient	100 $\mu W/cm^2$
Piezo	wearable	1's – 100's $\mu W/cm^2$

In addition to reducing quiescent power down to sub-µW range, many other energy harvesting techniques are also commonly used to extract as much energy from the environment as possible.

- Rectifiers for piezoelectric energy harvesters (PEHs): Due AC characteristics of PEH input, piezoelectric energy harvesting system usually needs a rectifier to convert the AC input power to DC output power. Different rectifiers have different energy extraction capability, which depends on how well the rectifiers can match the output impedance of the PEH. The energy extraction capability is quantified using the FOM, which is introduced in equations (1.1) and (1.2). By using a high FOM rectifier, more energy can be extracted from PEHs.

- Maximum-power point tracking: According to the maximum power transfer theorem, when load impedance equals to the impedance in the power source, the power delivered to the load is maximum. MPPT is a control scheme to adjust the input impedance of the energy harvesting circuitry to match the impedance of the energy harvesters. Commonly used MPPT methods include factional open-circuit voltage (FVOC) and perturb & observe (P&O) algorithm.

- Multi-modal energy harvesting: To extract maximum energy from the environment where multiple energy modalities exist, an effective way is to extract all those types of energy

simultaneously. This requires a multi-input power converter with interface adaptive to each energy source. Common energy sources include thermal energy, solar energy, and vibration energy and multi-input single-inductor multi-output (MISIMO) is a popular power converter architecture to fulfill this purpose.

- Single-stage power conversion: Traditional EHPMUs usually make energy harvesting interfaces and voltage regulators as two separate power converters. This two-stage structure increases the serial power loss and has a large form factor due to two inductors for two power converters. Single-stage power conversion is to directly delivery the energy from the harvesting input to the loads or to the energy storage node once the loads are fully charged. In this way, it eliminates the serial loss and minimized the form factor and cost.

By using those energy harvesting techniques together with reducing the quiescent power down to sub-µW range, there will be more energy delivered to the loads, which is one of the important tasks when designing EHPMUs for self-powered IoT devices.

1.3.2 Sub-nW Power Management Solution

After analyzing energy harvesting from the input side, next we will take a look at the load power at the output. One of the goals for designing voltage regulators is to maximize the power efficiency when delivery ultra-low output power to loads. Figure 1-6 shows the lowest power consumption of different types of loading components from 2009-2019 ISSCC/JSSC publications. As we can see, the lowest power consumption at 2009 is still hundreds of nW, but reduces down to pW at 2019. So, the power gradually decreases from µW, nW to pW during the past 11 years. With the trend of power reduction, how to power those loads efficiently is becoming very challenging, which also requires the quiescent power of EH-PMU has to be nW or even pW to maintain a high power-efficiency.

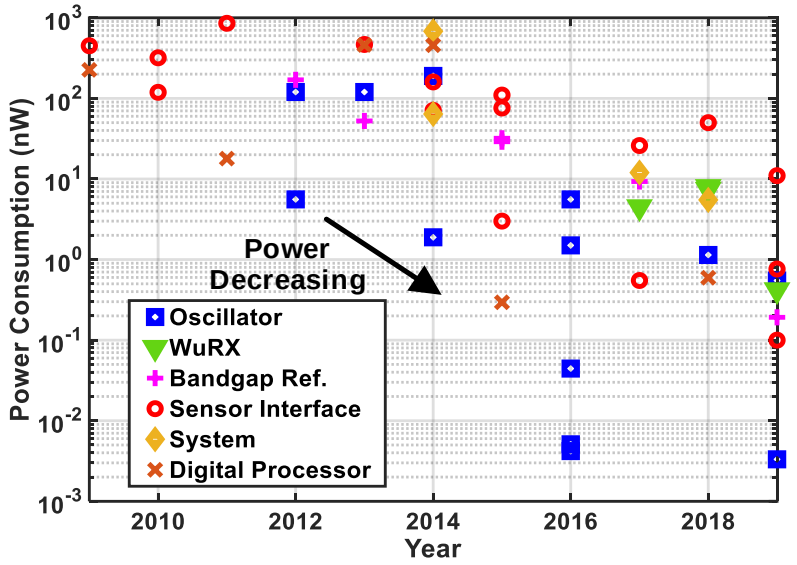


Figure 1-6 The lowest power consumption of different types of loading components from 2009 – 2019 ISSCC/JSSC publications. [10]

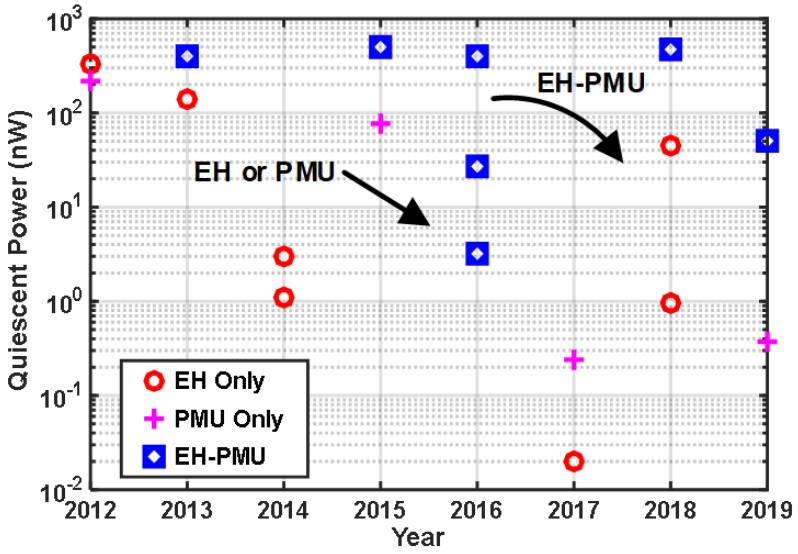


Figure 1-7 The lowest quiescent power of EHPMUs from 2012 – 2019 ISSCC/JSSC publications. [10]

Figure 1-7 shows the lowest quiescent power of EHPMUs from 2012-2019 ISSCC/JSSC publications. As we can see, the trend is almost the same as the trend of loads that the quiescent

power is gradually decreasing from nW down to pW. However, the power scaling for EHPMU system is not as fast as individual EH or PMU probably due to the system complexity.

To efficiently power modern nW or pW loading components, PMUs need to consume sub-nW quiescent power themselves, which is explained in the power efficiency equation (1.3). However, simply reducing the power consumption will sacrifice the performance such as loop transient response, so one of the main challenges is how to design sub-nW voltage regulators while keeping a high transient performance. One of the promising approaches is to optimize the control loop by using hybrid synchronous and asynchronous control schemes. Besides power delivery circuits, in order to generate stable voltage supplies for loads, voltage references are also needed to provides accurate voltage values. So sub-nW voltage references with good process, voltage and temperature stability are necessary in the power delivery path for ULP IoT systems.

1.4 Research Contribution and Organization

Power scaling from mW down to μW and nW enables energy harvesting and self-powered capability for IoT devices, which eliminates frequent and a large number of battery change and helps truly achieve the IoT era with billions of devices deployed in the near future. However, the power scaling down trend also brings unprecedented challenges for the SoC design, especially for the power delivery circuits including energy harvesting interfaces and voltage regulators. On the energy harvesting side, how to extract enough energy from the environment to power those IoT devices and on the voltage regulator side, how to maintain a high power-efficiency when delivering ultra-low output power to the loads are becoming critical and challenging.

The research in this dissertation focuses on the two main challenges for EHPMU design in self-powered IoT devices. First, from energy harvesting perspective, this dissertation explores how to extract more energy from the environment, which can potentially open up numerous applications where previously energy limits the device deployment. By investigating different

circuit architectures and design techniques including high-performance PEH rectifier, MPPT, and multi-modal energy harvesting, the designs in this research greatly enhance the energy extraction capability for energy harvesting interfaces. Second, from voltage regulator perspective, reducing PMU quiescent power down to sub-nW is the key to achieve high efficiency for powering nW or sub-nW loads. In this dissertation, we provide a complete sub-nW power management solution including voltage regulators and a bandgap voltage reference. Furthermore, given the general tradeoff between power consumption and performance, different kinds of design techniques and circuit architectures are explored and created to achieve a better optimization. The research in this dissertation achieves highly efficient energy harvesting and power delivery circuits for self-powered IoT nodes and helps enable IoT deployment even with limited energy in the environment to potentially open up many new applications. The dissertation is organized as follows.

In Chapter 2, we present a piezoelectric energy harvesting system, focusing on achieving the high-performance rectifier and maximum power point tracking simultaneously. In this work, a high-performance parallel synchronized-switch harvesting-on-inductor (SSHI) rectifier is implemented together with a highly efficient MPPT using perturb & observe (P&O) algorithm. We also proposed an analog power monitor to implement the P&O algorithm.

Chapter 3 is to design a multi-input single-inductor multi-output (MISIMO) energy harvesting and power management unit (EHPMU), which can extract energy from thermal, solar and vibration energy simultaneously and provide four voltage outputs for loads. It also integrates a multi-modal cold start-up block and combines the energy harvesting interfaces and voltage regulators in one power stage to minimize the form factor and eliminate the cascaded power loss.

The next two chapters provides a sub-nW power management solution. In Chapter 4, we explore the sub-nA LDO design using the advanced control techniques targeting for a wide dynamic range and fast transient response to power the nW or sub-nW load circuits, which includes two designs, a digital LDO (DLDO) and an analog LDO (ALDO). The DLDO uses a hybrid

synchronous and asynchronous control scheme and keeps an ultra-low quiescent power consumption while supporting a fast load transient response through the asynchronous path. As a comparison, a traditional fully integrated sub-nA ALDO using an analog feedback loop is also presented.

The final work is to design a sub-nW bandgap reference (BGR) with a wide input voltage range. By directly biasing the bipolar junction transistors (BJTs) with pA current and using an input charge pump to increase input voltage range, the proposed BGR achieves a sub-nW power consumption and a wide input voltage range from 0.45V up to 3.3V. The designed sub-nW BGR can be used together with sub-nW voltage regulators to generate voltage supplies with a good stability against process, voltage and temperature (PVT) variation.

Chapter 2

2. Piezoelectric Energy Harvesting System

2.1 Introduction

Energy exists everywhere in our lives with different modalities, such as thermal energy, solar energy, biochemical energy, etc. Those energy can be collected and stored to power electrical devices. Another widely existing energy is from mechanical vibration, which can be found everywhere from the engines in the factories, the tires on the vehicles, to the bridges among architectures, as shown in Figure 2-1. The energy generated by the vibration sources can also be collected and utilized to power our portable electronics, which is usually around μW level based on the vibration amplitude and transducer size. A piezoelectric energy harvester (PEH), which is an energy transducer, is commonly used to transform the vibration energy to electric energy. A major difference between vibration energy and other static energy source is that PEH outputs AC energy, which needs to convert to DC before using for powering the electric loads. This requires the energy harvesting interfaces to have the AC-DC conversion ability.

Figure 2-1 Application scenarios of energy harvesting from mechanical vibration.

A PEH is a type of energy transducer to convert the mechanical vibration energy to electric energy, which is usually made from two piezoelectric layer as shown in Figure 2-2. A tip mass can also be can be added to change the PEH characteristics, such as resonance frequency, open-circuit voltage, and output power. Figure 2-3 show a PEH model in mechanical and electrical domain [11] [12], where σ_{IN}, L_M, R_M, and C_M stand for a stress generator, mechanical mass, mechanical stiffness and mechanical losses.

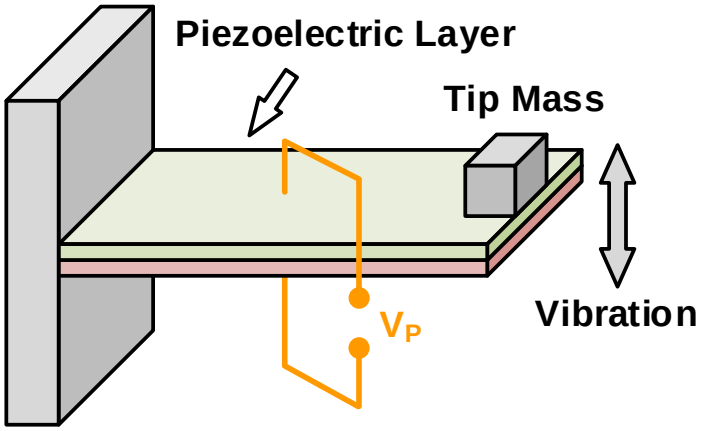


Figure 2-2 Illustration of a cantilever-beam-based PEH.

Converting the parameters from mechanical domain to electrical domain, we can get a fully electrical model of a PEH shown on the right side of Figure 2-3, where the parameters are explained below.

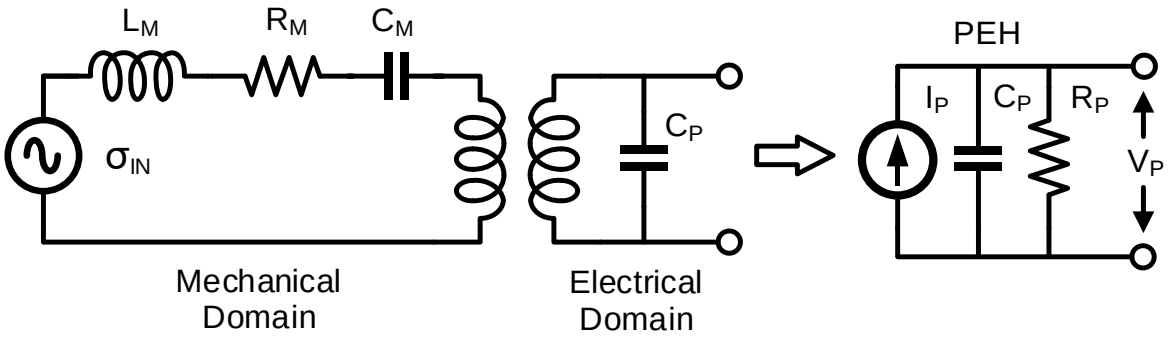


Figure 2-3 Electrical model of a piezoelectric energy harvester.

- V_P is the open circuit voltage of piezoelectric transducer and its typical value is 1V-10V which depends on vibration frequency and amplitude from vibration source and PEH characteristics, such as resonant frequency and parasitic capacitance.
- I_P stands for the equivalent AC current source. I_P frequency relies on vibration frequency, which has a typical value of 20-500Hz depending on the applications. I_P frequency could be PEH resonant frequency or off-resonant frequency and the amplitude of I_P depends on vibration strength of the energy source.
- C_P stands for the parasitic capacitance, which is usually very large with typical values of 10nF-200nF. C_P limits the maximum power that can be extracts by the energy harvesting interfaces, so during energy extraction, C_P should be compensated by using different kinds of circuit techniques.
- R_P is the equivalent dielectric loss resistance, which is usually extremely large at about MΩ level and sometimes can be ignored at high PEH output power.

2.2 Overview of PEH Interface Circuits

To extract the energy from a PEH and power the loading circuits, an interface circuit is needed shown in Figure 2-4, which includes an AC to DC rectifier and a DC-DC converter. A PEH

electrical model is usually used as the energy input during simulations. The main functions of the PEH rectifier are to convert AC energy to DC energy and extract as much energy as possible from the PEH, which can be characterized as energy-extraction improvement. For the DC-DC converter, first, it is used to adjust the intermediate voltage, V_{REC}, to make the rectifier work at the maximum power point. Second, if we want to store the maximum energy at the storage node, the DC-DC converter can transfer the energy from V_{REC} to V_{STORE} with a high efficiency. So, there are basically two main goals to design a PEH interface circuit, enhancing the rectifier energy-extraction capability and efficiently tracking the rectifier maximum power-point.

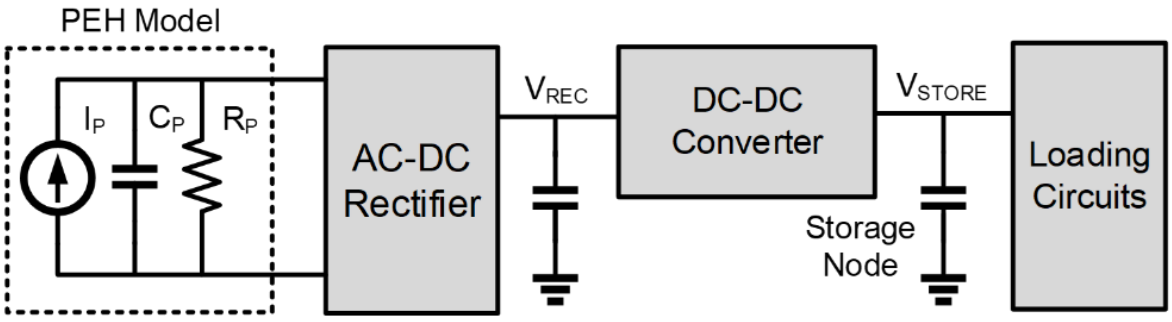


Figure 2-4 Block diagram of a general piezoelectric energy harvesting system. [13]

2.2.1 PEH Rectifiers

The AC-DC rectifier design for PEH is critical because it directly determines the energy-extraction ability. Although there are a lot of variants of rectifiers, the basic structure can be divided into three categories, full bridge rectifier (FBR), [14] synchronous-electric-charge extraction (SECE) rectifier, [15] [16] and parallel synchronized-switch harvesting-on-inductor (SSHI) rectifier [17] [18].

- The FBR directly converts the AC input power to DC power, so it is the simplest rectifier, which has a low energy-extraction gain, but it also has a low design complexity. The schematic with its operating waveform is shown in Figure 2-5. Every time the current I_P

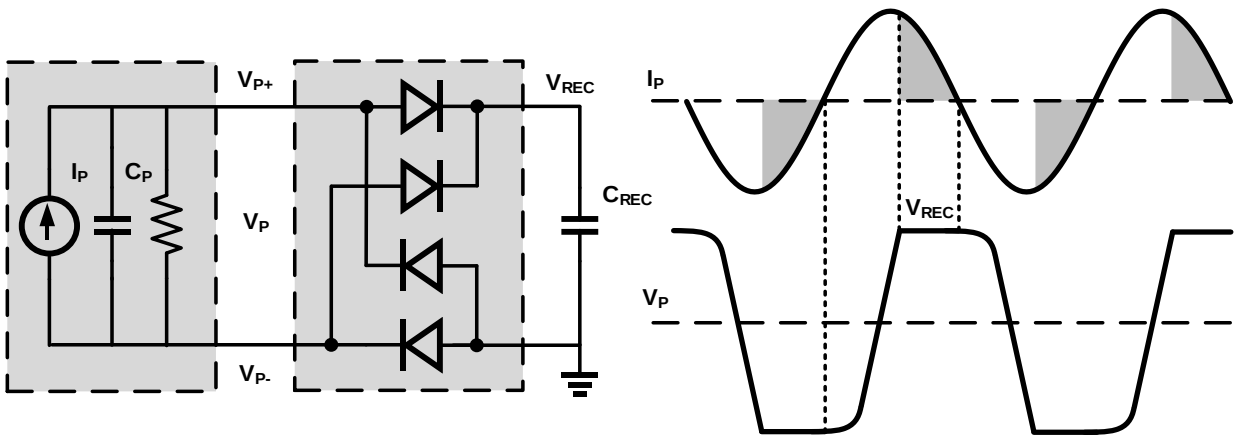


Figure 2-5 Block diagram and operating waveform of the FBR.

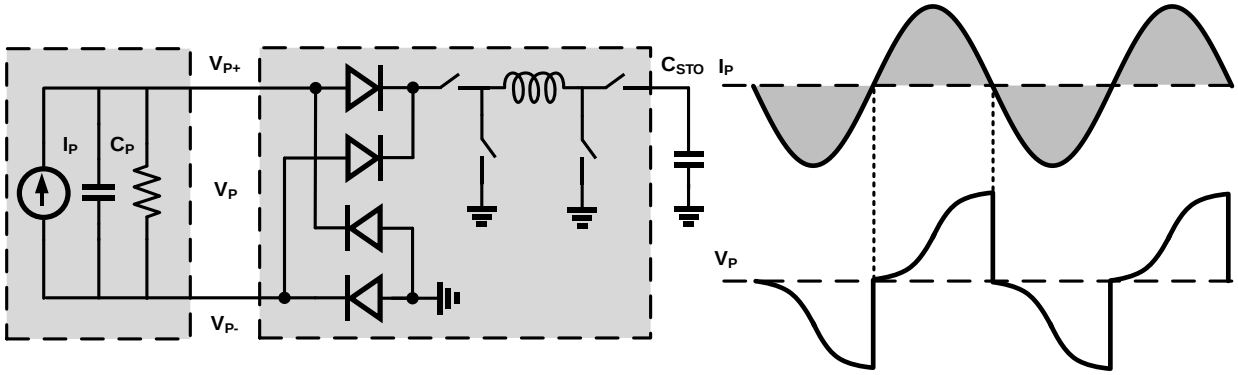


Figure 2-6 Block diagram and operating waveform of the SECE rectifier.

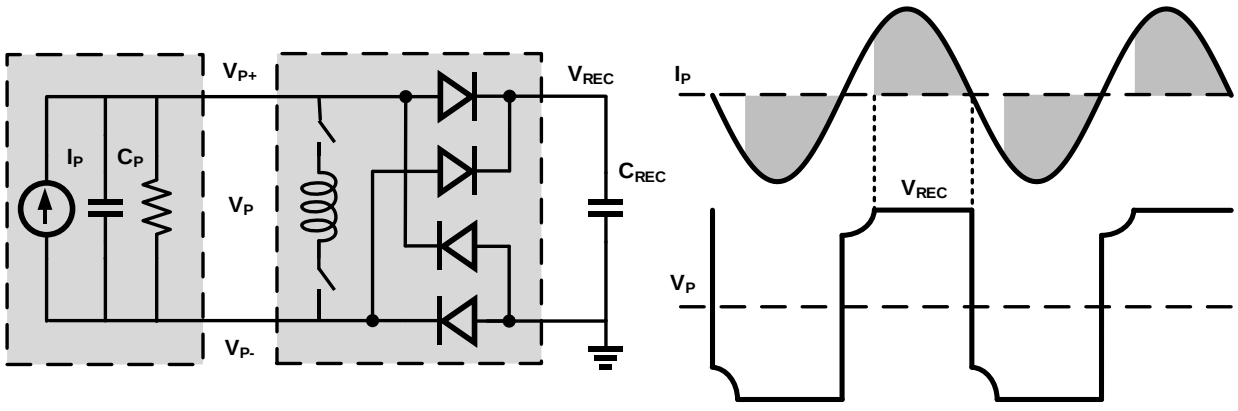


Figure 2-7 Block diagram and operating waveform of the parallel-SSHI rectifier.

reverses the charging direction, the PEH needs to discharge C_P first to zero voltage and recharge it again up to V_{REC}, so there is a lot of energy wasted by charging and discharging C_P and the FOM is very low due to high energy loss on C_P.

- Figure 2-6 shows the schematic and its operating waveform of a SECE rectifier, which consists of a full bridge rectifier and a DC-DC converter. The DC-DC converter extracts the energy from C_P every half vibration cycle once C_P is charged to its highest voltage. SECE rectifier improves the FOM by directly extracting energy stored on C_P, so there is no energy loss due to C_P discharging. SECE rectifier has a medium design complexity and a medium energy-extraction gain because it still needs to charge the C_P from zero voltage. Another benefit of SECE rectifier is that it includes the voltage regulation capability using the DC-DC converter, so it can transfer energy directly to the energy storage node.

- The parallel-SSHI rectifier is shown in Figure 2-7. Instead of extracting the energy on the capacitor, the parallel-SSHI rectifier flips the energy and voltage on C_P every half vibration cycle using an inductor, so the current generated from the PEH can directly go through the rectifier to an optimized voltage on capacitor C_{REC}, which greatly improves the energy-extraction capability. The parallel-SSHI rectifier has highest FOM, but it also increases the design complexity.

There are many other types of PEH rectifiers developed in recent years, such as synchronized-switch harvesting-on-capacitor (SSHC) [19] [20] or rectifier with energy-investing ability [21]. The working principle of SSHC rectifier is similar to parallel-SSHI rectifier. The main difference is that instead of using inductor to flip the energy on C_P, it uses capacitors to achieve the flipping functions. The energy-investing PEH rectifier injects energy from energy storage node to C_P to enhance the energy extraction capability.

2.2.2 MPPT Schemes for PEH

After discussing the rectifiers, next we will look at the MPPT schemes. For piezoelectric energy harvesting, many MPPT schemes are used for specific rectifiers because for different rectifiers, the maximum energy extracted from PEHs are usually different due to the impedance matching ability and the power loss of different rectifier structures. So, the selection of MPPT scheme need to adapt to the rectifier working mechanism. Common MPPT schemes for PEH rectifiers are listed below.

- Fractional open-circuit voltage (FVOC) is a very common MPPT scheme. [22] It detects the PEH open-circuit voltage V_{OC} and uses a fraction of V_{OC} to regulate the rectifier output. Although this MPPT scheme has a high tracking efficiency, the drawback is that it is only effective for FBR, so the rectifier energy extraction capability is low. The calculated open circuit voltage and MPP voltage for FBR are

$$V_{OC} = \frac{I_P}{\omega C_P} \tag{2.1}$$

$$V_{MPP} = \frac{I_P}{2\omega C_P} \tag{2.2}$$

  where ω is the angular frequency of the vibration. As we can see, the MPP at the output of a FBR is half of its open circuit voltage.

- A sense and set MPPT is proposed in [23], which can exactly track the AC energy signal and compensate the parasitic capacitance, C_P. It has the benefit of accurately tracking the PEH input impedance and the rectifier used with sense and set MPPT has a high energy-extraction capability. However, this MPPT method is only effective for low input power range, which is less than 17μW in the paper and also it does not count the power loss of the rectifier.

- Perturb and observe (P&O) MPPT is another commonly used MPPT scheme. This MPPT is based on the P&O algorithm [24] [25], which changes one parameter first, and observes the result to find the maximum or minimum value. The advantage of P&O algorithm is that it does not limited by any type of rectifiers due to its universality.

2.3 A Piezoelectric Energy Harvesting System with Highly Efficient MPPT

This research mainly investigates the design of a highly efficient piezoelectric energy harvesting system with a high FOM rectifier and MPPT. Parallel-SSHI rectifier can achieve high energy-extraction ability, but its MPP is related to the rectifier flipping efficiency and the characteristics of PEH and excitation source, which makes its MPPT very complicated. So how to achieve a high FOM rectifier together with a high efficiency and ultra-low-power MPPT is very challenging.

Figure 2-8 shows the architecture of the proposed piezoelectric energy harvesting system, [26] which includes a parallel-SSHI rectifier, a buck-boost converter, and a MPPT control loop. The buck-boost converter operates under discontinuous-conduction mode (DCM) and adopts ripple-based control with a hysteresis comparator. The control signal, SW_R, from the rectifier is used to synchronize the switching of the buck-boost converter with the PEH vibration cycles. The proposed PEH system includes the high-performance parallel-SSHI rectifier and P&O MPPT together to enhance the energy extraction capability. We also implement an analog power monitor to accurately estimate the output power for P&O algorithm.

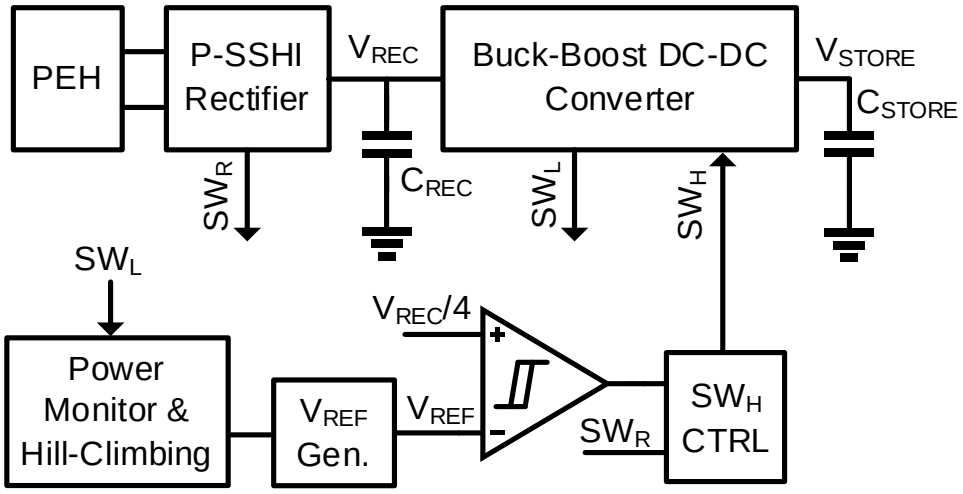
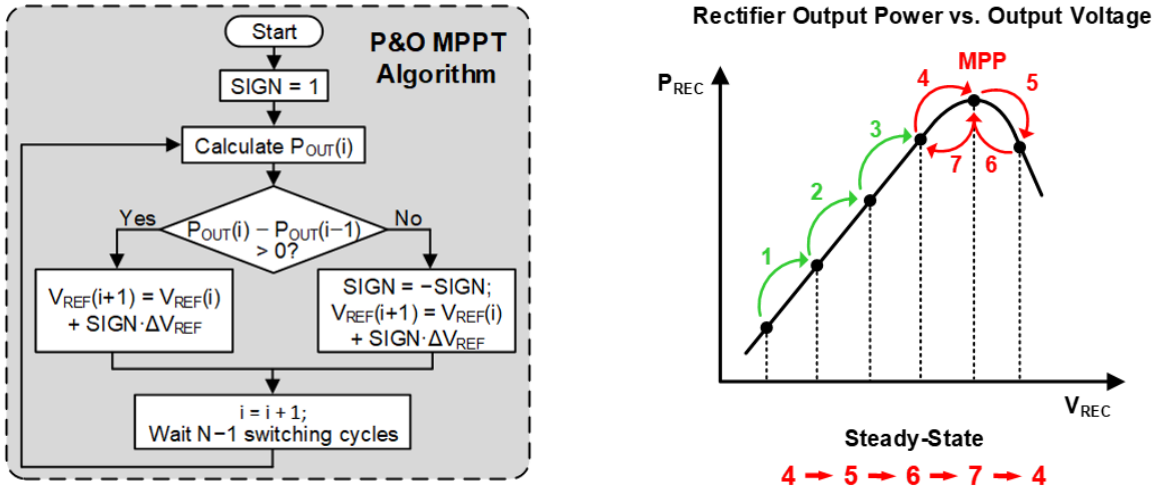


Figure 2-8 Architecture of the proposed piezoelectric energy harvesting system. [26]

2.3.1 P&O MPPT and Proposed Power Evaluation Algorithm

In this work, P&O algorithm is used for the MPPT together with the high performance parallel-SSHI rectifier. The biggest advantage of this MPPT algorithm is that it is independent from the harvester and circuit characteristics, which is suitable for the parallel-SSHI rectifier. The flow chart of this algorithm is shown in Figure 2-9 (a). First, the algorithm calculates the rectifier output power, P_{OUT}, and then compares the current power with the previous one. If the current value is higher than the previous one, V_{REC} keeps the same searching directions. Otherwise, it will reverse the direction. For example, in Figure 2-9 (b), V_{REC} keeps the same direction for step 1, 2, 3, and 4 since the current output power is higher than the previous power. For step 5, its current calculated value is lower than the previous one, so it reverses the searching direction. In such case, during steady state, V_{REC} keeps the searching loop from step 4 to 7 and maximize the rectifier output power.



(a) (b)

Figure 2-9 (a) Flowchart of the P&O MPPT algorithm; (b) Illustration of the P&O algorithm.

In all the procedures of this algorithm, the most challenging task is how to calculate the AC output power out of the rectifier accurately. To address this issue, we propose an output power evaluation method, which uses the parameters in the buck-boost converter shown in Figure 2-10. The basic ideal is the total output power equals to the energy transferred in the inductor divided by the switching cycle. SW_H and SW_L represent the switching control signals for the power switches in the buck-boost converter. For every switching cycle, the energy transferred through the inductor is:

$$\Delta E = \frac{1}{2} \cdot L \cdot I_{PEAK}^{\ 2} \tag{2.3}$$

where I_{PEAK} is peak current through the inductor. Assuming the conduction loss during the second transfer phase is negligible compared with the total transferred energy, I_{PEAK} equals to:

$$I_{PEAK} = \frac{V_{STORE} \cdot T_{SWL}}{L} \tag{2.4}$$

where T_{SWL} is the pulse width of SW_L and V_{STORE} is the voltage on the energy storage node.

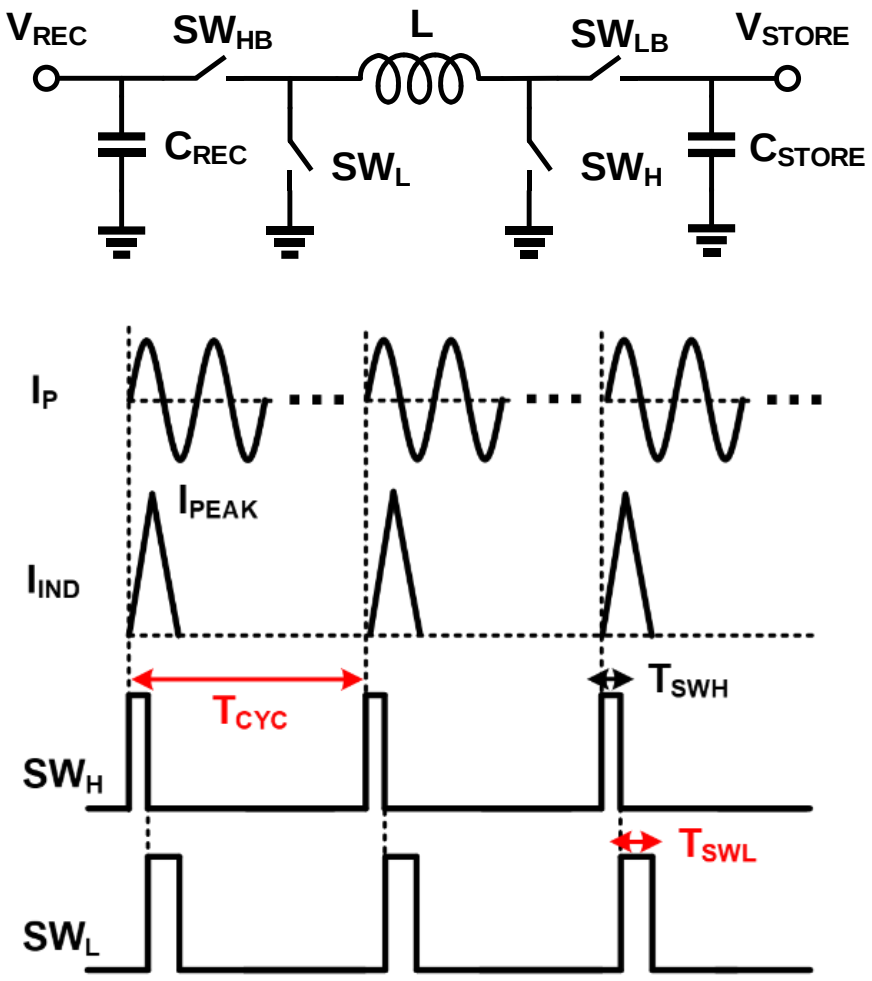


Figure 2-10 Structure of a buck-boost converter and its operating waveform.

Finally, P_{OUT} can be calculated by dividing the energy delivered during one switching pulse with its corresponding switching cycle. So, from (2.1) and (2.2), the P_{OUT} is:

$$P_{OUT} = \frac{\Delta E}{T_{CYC}} = \frac{V_{STORE}^{\ 2} \cdot T_{SWL}^{\ 2}}{2 \cdot L \cdot T_{CYC}} \tag{2.5}$$

where T_{CYC} is the SW_L switching period. Assuming V_{STORE} keeps constant during adjacent two comparison cycles due to the large storage capacitor of 4.7 mF used in this work, the variables in (2.5) are only T_{SWL} and T_{CYC}, both of which can be derived from the control signal SW_L.

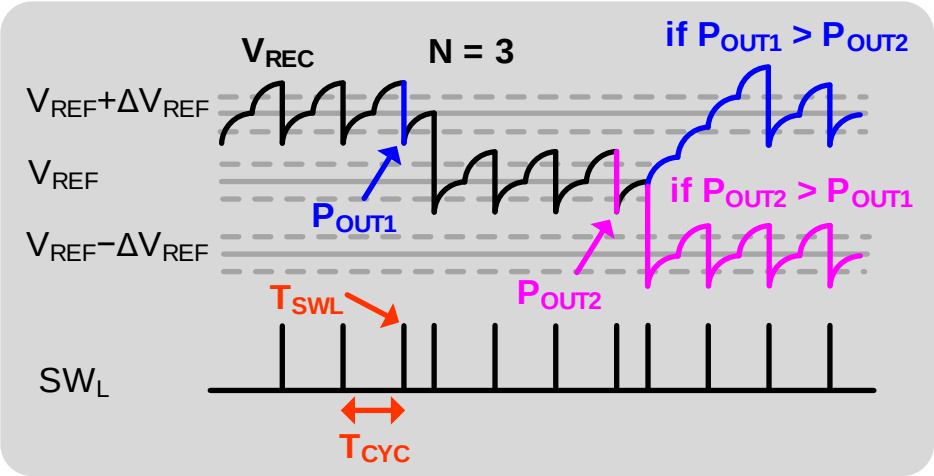


Figure 2-11 P&O MPPT operation timing diagram.

There are two things to notice for this power evaluation method. First, to get an average P_{OUT} and make the evaluation accurate, T_{CYC} should include integer number of vibration cycles, which needs the switching control of the buck-boost converter to be synchronized with the PEH rectifier. In a hysteresis control implementation, M is the number of minimum cycles that makes V_{REC} larger than the high threshold voltage, which depends on the hysteresis voltage value, PEH input power, and the value of C_{REC}. Second, because the proposed power evaluation calculates the power delivered to the storage node, this method not only considers the power loss of the rectifier, but also the power loss of the buck-boost converter.

The MPPT operation timing diagram in Figure 2-11 shows how V_{REC} works to find out the MPP with a voltage step of ΔV_{REC} and $M = 2$. After arriving at a new voltage level, V_{REC} needs to wait $N-1$ switching-cycles of the buck-boost converter to become steady state and evaluate P_{OUT} at the *N-th* switching pulse. N is programmable from 3 to 6 in this work. Larger N makes V_{REC} well settled on the new voltage level, which reduces the evaluation error but increases the tracking time. After power evaluation and comparison, V_{REC} will change to a new voltage level at the next half-vibration-cycle based on the comparison result.

2.3.2 Design Implementation

A detailed implementation of the piezoelectric harvesting system is shown in Figure 2-12, which includes a parallel-SSHI rectifier, a buck-boost converter with integrated P&O MPPT, and a bias generator and an inductor sharing block. The parallel-SSHI rectifier adopts an active rectifier (AR) scheme and consists of a negative voltage converter (NVC), an active diode and a flipping-time control block. SW_R is the comparator output of the active diode and SW_F is the control signal for the rectifier voltage flipping. Transistor M_S is used for the cold start-up of the rectifier. The inductor, $L_{R\text{-}M}$, is shared by the rectifier and the DC-DC converter to minimize the off-chip components and system volume through an inductor sharing block.

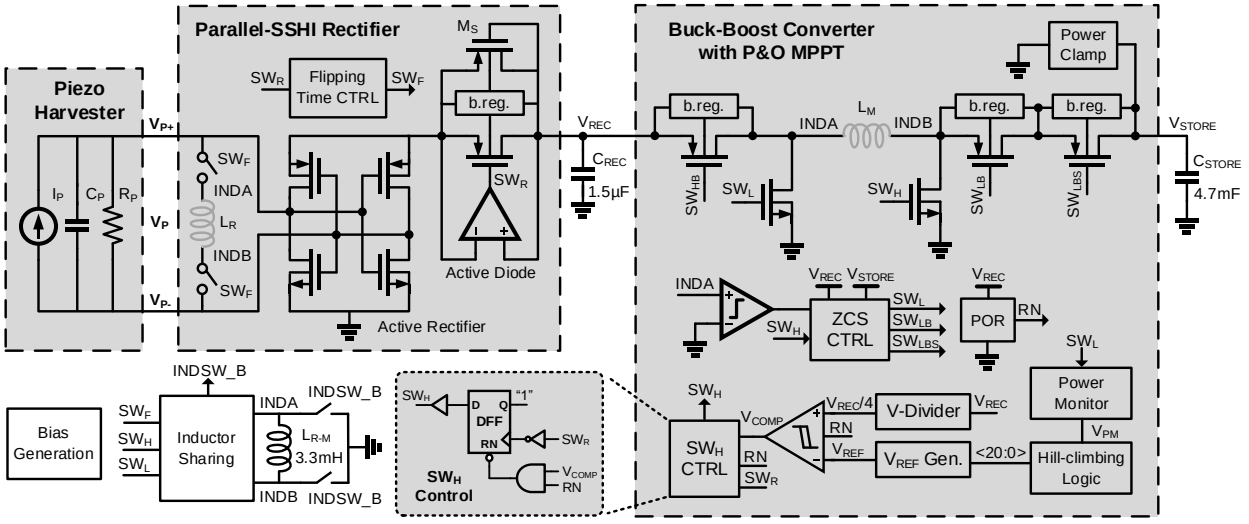


Figure 2-12 Implementation of the piezoelectric energy-harvesting system.

To implement the power evaluation algorithm derived in (2.5), we achieve a power monitor block in fully analog domain with sub-µA current consumption. First, time parameters in equation (2.5) need to be transformed to electrical parameters. So, T_{SWL} and T_{CYC} are converted to voltages using time-to-voltage converters (TVCs) and then to currents using V-I converters. The conversion equation for T_{SWL} is:

$$I_{SWL} = V_{SWL} / R_{SWL} = \frac{I_{BIAS} \cdot T_{SWL}}{C_{SWL} \cdot R_{SWL}} \tag{2.6}$$

The exponential characteristics of the MOSFET I-V curve under subthreshold (sub-V_T) region in (2.7) is utilized to compare P_{OUT}. If I_{SWL} and I_{CYC} flow through the sub-V_T transistors, the square and division in (2.6) will convert to addition and subtraction of the transistor gate-source voltage, V_{GS}. So, the difference of the two adjacent $logP_{OUT}$ is derived in (2.8).

$$I_D = I_0 exp\left(V_{GS} / \zeta V_T\right) \tag{2.7}$$

$$\begin{aligned} logP_{OUT,1} - logP_{OUT,2} &= \left(2logT_{SWL,1} - logT_{CYC,1}\right) - \left(2logT_{SWL,2} - logT_{CYC,2}\right) \\ &= A \cdot \left[\left(2V_{GS,SWL,1} - V_{GS,CYC,1}\right) - \left(2V_{GS,SWL,2} - V_{GS,CYC,2}\right)\right] \end{aligned} \tag{2.8}$$

where A is a constant number, $V_{GS,\,SWL}$ and $V_{GS,\,CYC}$ are the gate-to-source voltages of the sub-V_T transistors. Figure 2-13 shows the block diagram of the proposed power monitor, which includes a pulse generator, two time-to-voltage converters and voltage-to-current converters, a subthreshold power calculation block, a sample and hold block, and a comparator. The proposed power monitor achieves all the functions in the analog domain to keep the power very low.

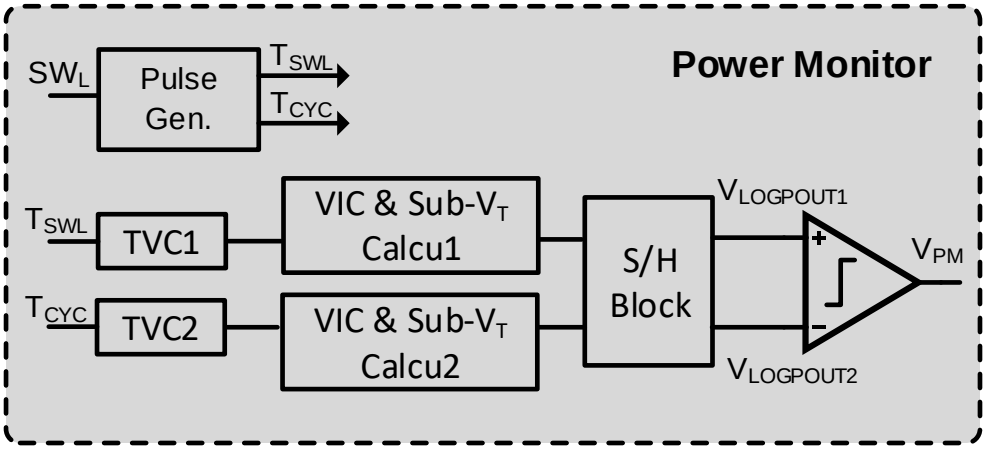


Figure 2-13 Block diagram of the proposed power monitor.

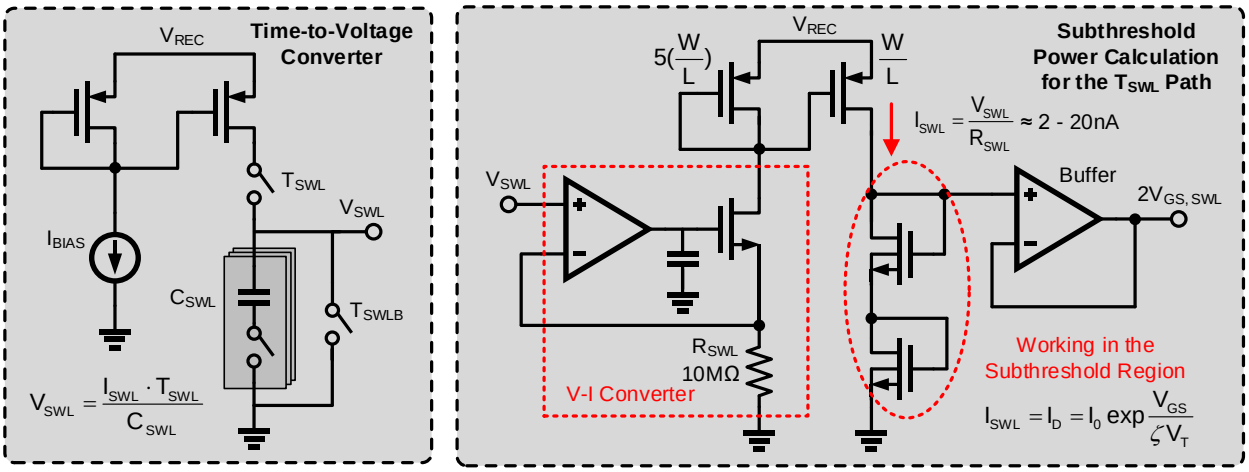


Figure 2-14 Schematic of the TVC and subthreshold power calculation block.

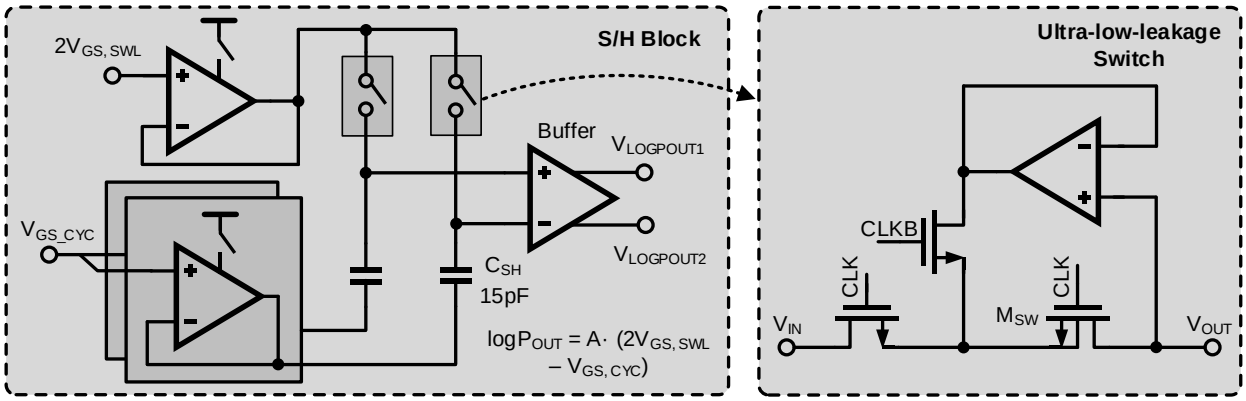


Figure 2-15 Schematic of the S/H block and ultra-low-leakage switch.

Figure 2-14 and Figure 2-15 show the detailed schematic of each block in the power monitor. TVC is implemented by using a current source to charge a capacitor and its output voltage is connected with a V-I converter followed by sub-V_T transistors. Figure 2-14 shows the branch for T_{SWL}. For T_{CYC}, it only needs one sub-V_T transistor. To reduce the voltage error on the capacitor in the sampling and hold (S/H) block, an ultra-low-leakage switch [24] is used in this work. When the switch is off, the amplifier makes the body and source of transistor M_{SW} the same voltage as the drain to reduce the leakage current through the transistor body and channel.

The schematics of the V_{REF} generator and the comparator for zero-current switching (ZCS) control are shown in Figure 2-16. V_{REF} is generated by making a current source going through a resistor array. During V_{REF} transition phase, the hill-climbing logic generates a one-hot code to choose one of the references from the resistor array, which is buffered and sampled onto a 9.6 pF on-chip capacitor. By changing the configuration of the hill-climbing logic, the resolution of the reference voltage can be set to either 100mV or 200mV. The P&O tracking range for V_{REC} is from 1.2V to 3.3V in this design. The continuous-time comparator is used for the ZCS of the buck-boost converter, which adopts a common-gate structure. The comparator is duty-cycled to reduce the average power consumption.

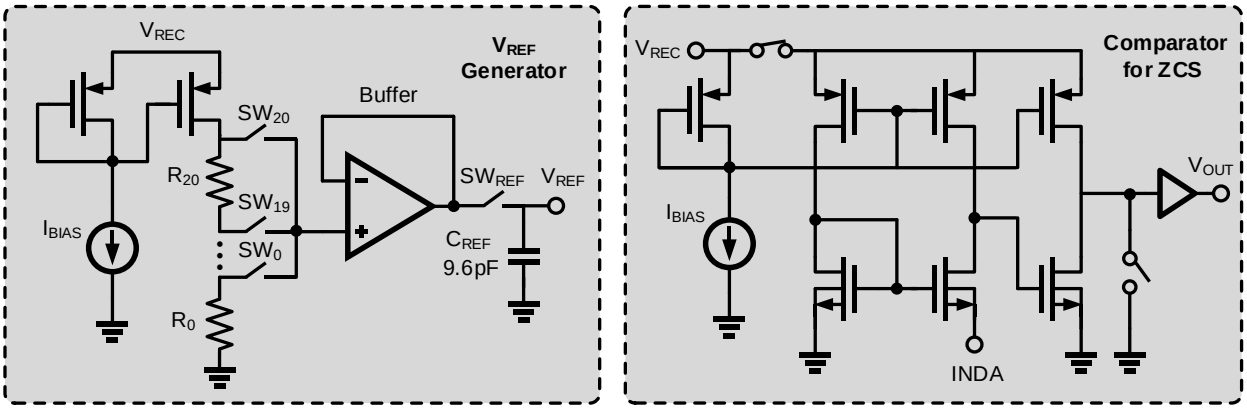


Figure 2-16 Schematic of V_{REF} generator and comparator for ZCS control.

2.3.3 Measurement Results

The piezoelectric energy-harvesting system is fabricated in 130-nm CMOS technology with an area of 1.07mm^2. Figure 2-17 shows the chip micrograph and simulated quiescent current breakdown of the piezoelectric system and its power monitor is shown in Figure 2-18. The simulated total current consumption for the whole system is 1.57μA and the proposed analog power monitor only consumes 430nA. For the measurement setup shown in Figure 2-19, a function generator (Agilent 33250A) sends the vibration waveforms to a power amplifier (B&K 4809)

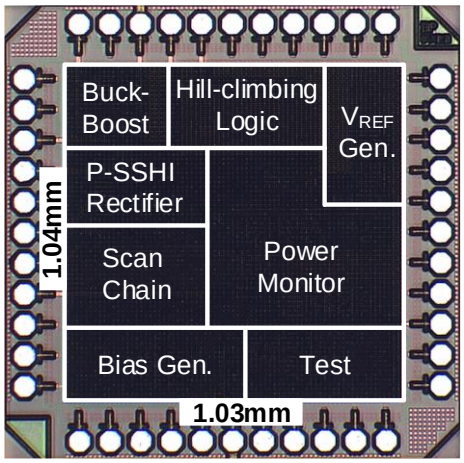
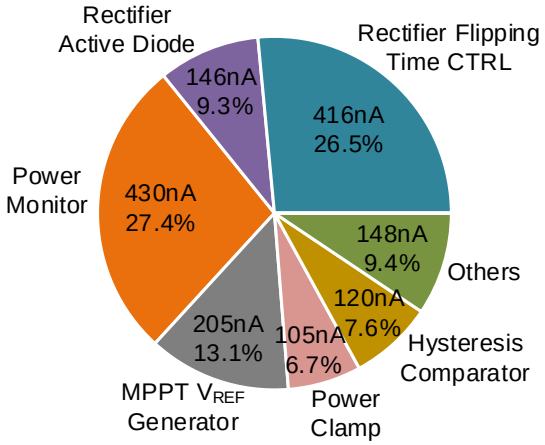


Figure 2-17 Chip micrograph. [26]



Power monitor	Quiescent Current (nA)
TVC	122.3
Sub-V_T calculation	184.2
S/H block	63.1
Comparator	0.53
Pulse Gen.	60
Total	430.13

Figure 2-18 Simulated quiescent current breakdown of the PEH system and power monitor.

which drives a mini shaker (B&K 4810). Two piezoelectric transducers, PPA-1021 and PPA-1011 from Mide Technology, are used for the measurements with parasitic capacitance of 22nF and 100nF and resonance frequency of 182Hz and 135Hz separately. Figure 2-20 shows the measured transient start-up waveform. As we can see, V_{REC} is charged first, and then the storage node V_{STORE} is charged slowly up to the maximum 3.3V voltage because of the large storage capacitor. After V_{STORE} charges to 3.3 V, it is regulated by the on-chip power clamp to protect the chip from over-voltage. During steady state, the flipping efficiency of the parallel-SSHI rectifier is 86%.

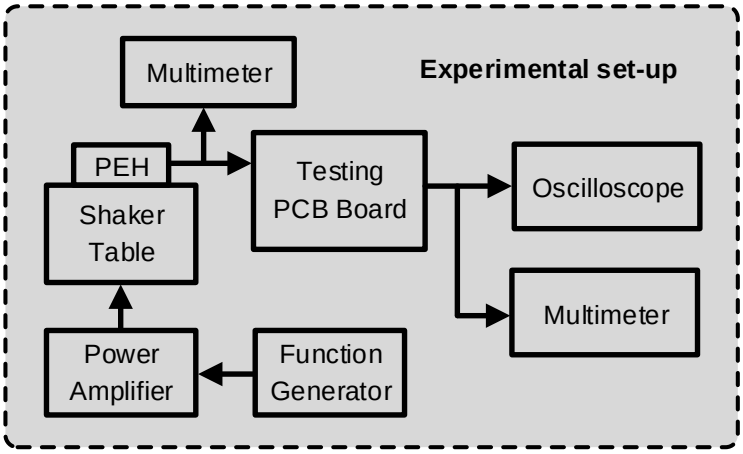


Figure 2-19 Experimental set-up for the PEH system measurements

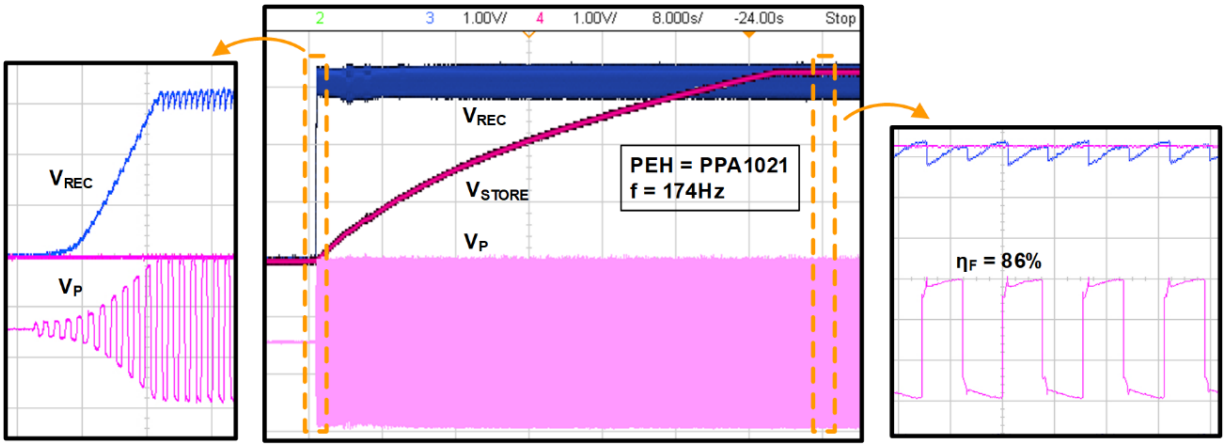


Figure 2-20 Measured transient start-up waveform of the piezoelectric system.

The measured inductor-sharing waveform is shown in Figure 2-21, which shows the rectifier flipping current and buck-boost switching current enabled by the control signal *INDSW*. When the inductor sharing is disabled, the two terminals of the inductor are shorted to the ground. The measured steady-state waveform of the MPPT in Figure 2-22 shows exactly the P&O waveform with an about 300mV voltage step. The two signals, $V_{LOGPOUT1}$ and $V_{LOGPOUT2}$, are the evaluated output power value stored on the capacitor in the S/H block. The measured rectifier output power with PPA-1021 under 143Hz and 1.6V V_{OC} is 30.53µW shown in Figure 2-23. However, the on-chip AR can only extract a maximum 6.9µW output power under the same setup. The parallel-

SSHI rectifier can extract 4.17× more energy than the ideal FBR, which means the energy-extraction improvement of the rectifier is 417%. The measured maximum buck-boost converter efficiency is 78% when V_{REC} and V_{STORE} are both set to 3V and the efficiency reduces at high P_{IN} due to higher conduction loss as shown in Figure 2-24.

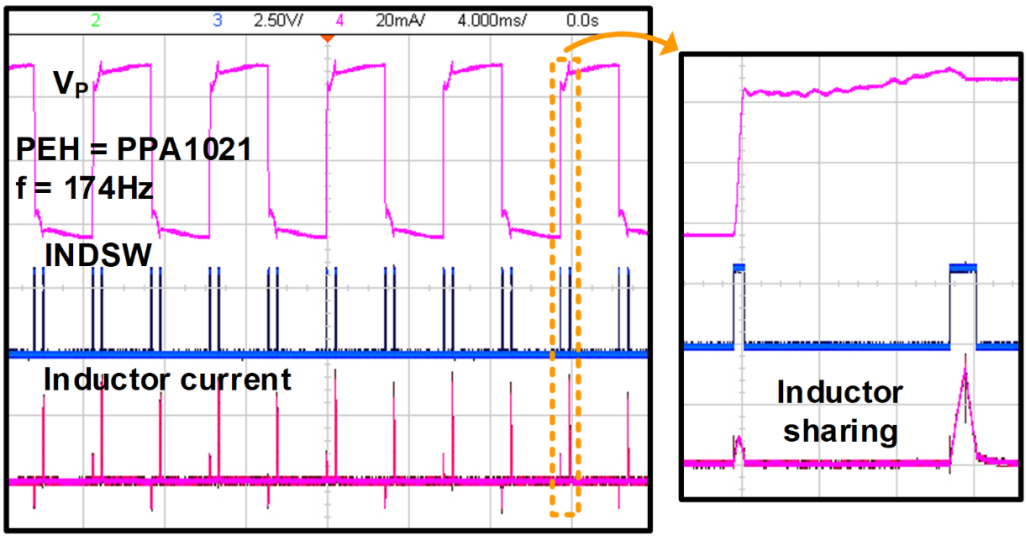


Figure 2-21 Measured V_P and inductor-sharing transient waveform.

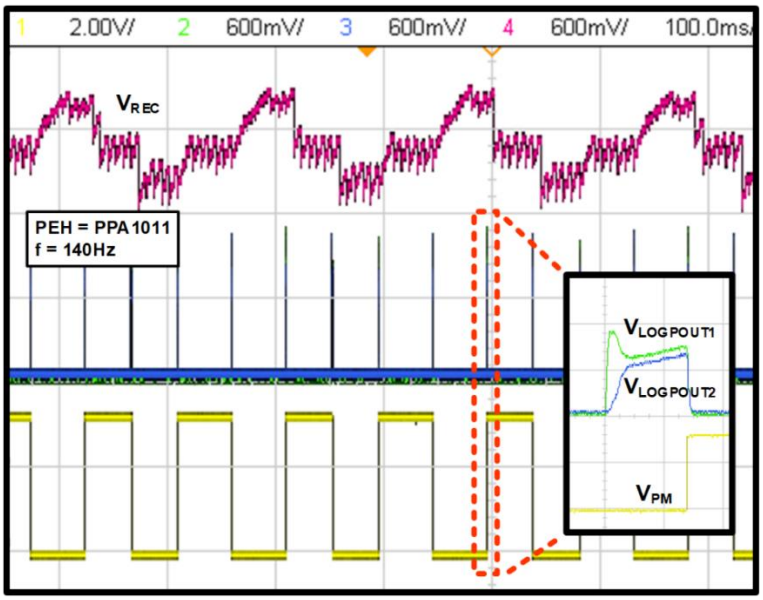


Figure 2-22 Measured MPPT steady-state waveform.

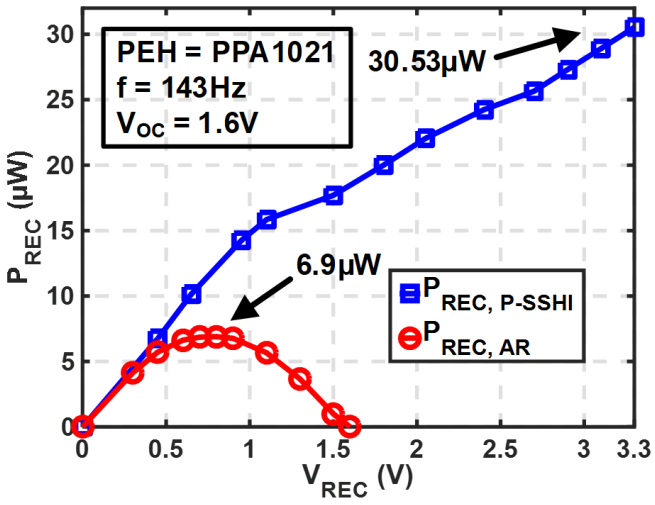


Figure 2-23 Measured rectifier output power P_{REC} vs. output voltage V_{REC}.

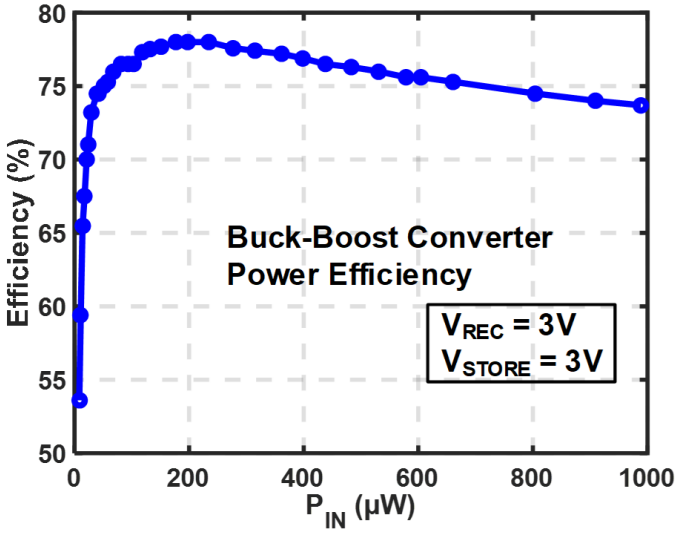


Figure 2-24 Measured power efficiency of the buck-boost converter.

Figure 2-25 and Figure 2-26 shows the tracking efficiency of the MPPT over V_{OC} and vibration frequency by comparing P_{OUT} when enabling MPPT under 100mV voltage step with the manually-tuned maximum P_{OUT}. The MPPT efficiency is larger than 90% across the range of 2.2V-4V V_{OC} and 100-142Hz excitation frequency.

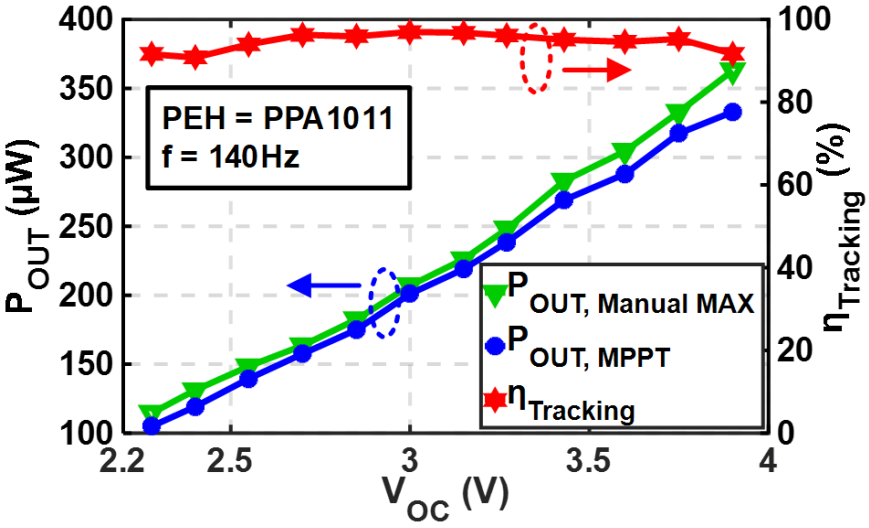


Figure 2-25 Measured tracking efficiency vs. V_{OC}.

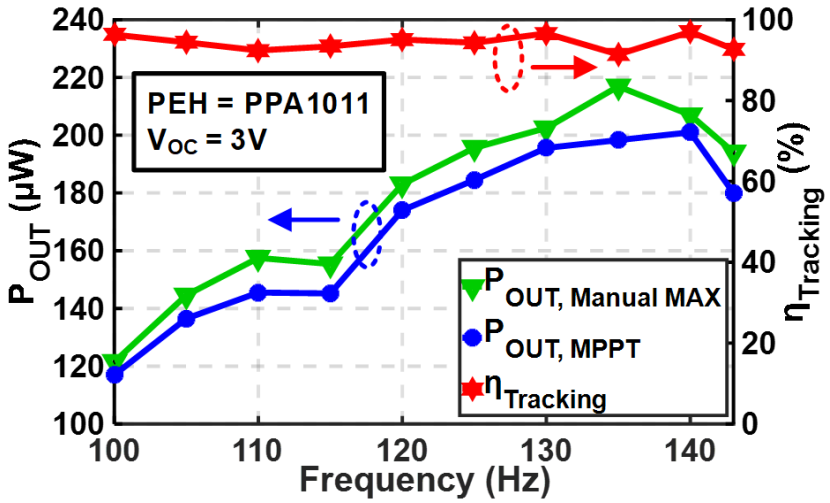


Figure 2-26 Measured tracking efficiency vs. excitation frequency.

The performance comparison with state-of-the-art PEH interfaces in Table 2-1 shows that our piezoelectric energy harvesting system achieves a 417% FOM rectifier, which is 4× higher than the FBRs used with other MPPTs, and a maximum 97% efficiency MPPT simultaneously thanks to the parallel-SSHI rectifier, perturb & observe MPPT and proposed power monitor, which has the benefit of high energy-extraction capability and high MPPT tracking efficiency.

Table 2-1 Comparison with state-of-the-art piezoelectric energy harvesting interface circuits

	This work	[22] ISSCC'14	[27] ISSCC'13	[18] ISSCC'16	[28] JSSC'14
Process	0.13μm	0.35μm	0.25μm	0.35μm	0.18μm
Harvester Type	Piezoelectric	Piezoelectric	Electrostatic	Piezoelectric	Piezoelectric
Piezoelectric Harvester	MIDE PPA1021 & PPA1011	MIDE V20W & V21BL	N/A	MIDE V21B & V22B	Custom MEMS
Harvester Capacitance (nF)	20 & 100	11	N/A	26, 20 & 9	8.5
Rectifier Scheme	Parallel-SSHI	FBR	Off-chip FBR	Parallel-SSHI	Parallel-SSHI
Operation Frequency (Hz)	100 - 180	N/R	N/R	134.6 - 229.2	155 & 419
MPPT	Yes	Yes	Yes	No	No
MPPT Algorithm	P&O	Fractional V_{OC}	VS-P&O	N/A	N/A
Flipping Efficiency	0.86	N/A	N/A	0.93	0.76**
Energy-Extraction Improvement (FOM*)	**417%**	**90%**	**< 100%**	**681%**	**266%****
Maximum MPPT Efficiency	**97%**	**99%**	**99.9%**	**N/A**	**N/A**
Rectifier (>400% FOM) + MPPT (>90% Efficiency)	**Yes**	**No**	**No**	**No**	**No**

N/A = Not Applicable; N/R = Not Reported; * FOM = $P_{REC}/(C_P \cdot V_{OC}^2 \cdot f)$; ** Calculated from the paper

2.4 Conclusions

In this work, a piezoelectric energy-harvesting system including a parallel-SSHI rectifier and integrated MPPT is presented. The P&O algorithm is adopted for the MPPT of the parallel-SSHI rectifier. Furthermore, an output power evaluation algorithm for the P&O MPPT is proposed and its detailed implementation in the full analog domain is analyzed. Fabricated in 130-nm CMOS, measurement results show the piezoelectric harvesting system achieves a 417% energy-extraction improvement for the rectifier and a maximum 97% tracking efficiency for the MPPT, which makes the system achieve high energy-extraction improvement and MPPT efficiency simultaneously.

Chapter 3

3. MISIMO Energy Harvesting and Power Management Platform

3.1 Introduction

One of the major objectives for designing energy harvesting circuits is to extract as much energy as possible from the environment. This goal can be achieved by using advanced rectifiers and MPPTs for PEH energy harvesting, as introduced in the last chapter. Another effective way is to extract energy from different energy sources with different modalities. Besides vibration energy, other common energy sources include thermal energy and solar energy. In this research, we will explore energy harvesting and power management design that can extract energy from all those three energy modalities and provide multiple outputs for loads using only one inductor. This EHPMU adopts multi-input single-inductor multi-output (MISIMO) architecture, which has only one power-delivery stage to minimize the form factor and reduce the serial power loss.

3.1.1 Thermal Electric Generator

A thermal electric generator (TEG) is an energy transducer that converts thermal energy in the form of temperature differences to electric energy. [29] [30] Figure 3-1 shows a physical structure of a TEG, which consists of an array of 2N pellets, conductors to connect the pellets, and two ceramic plates on the top and bottom. The 2N pellets are made of p-type and n-type materials, so based on the Seeback effect, TEG generates current flow from the warm side to the cold side of the ceramic plates.

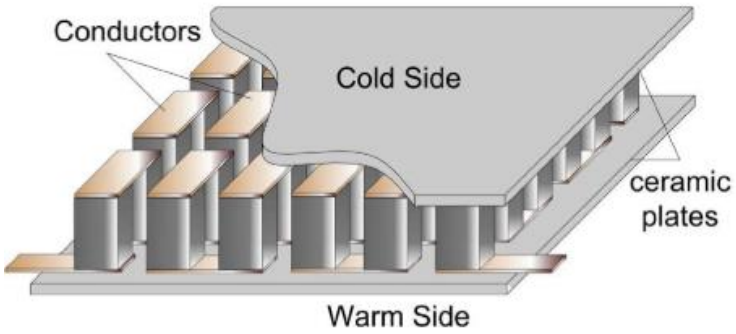


Figure 3-1 Physical structure of a TEG. [29]

Figure 3-2 show the equivalent electrical model of the TEG, where V_{TEG} is the TEG open circuit voltage and R_{TEG} is the internal resistance. V_{TEG} is proportional to the temperature difference between two sides of a TEG, which is given by

$$V_{TEG} = S \cdot \Delta T \tag{3.1}$$

where S is the Seeback coefficient and ΔT is the temperature difference. R_{TEG} depends on the number of serial pellets and is usually very small in a few ohms range. The generated V_{TEG} is also very small. For a wearable size TEG and temperature difference between human body and room temperature, V_{TEG} is only tens of mV. [31]

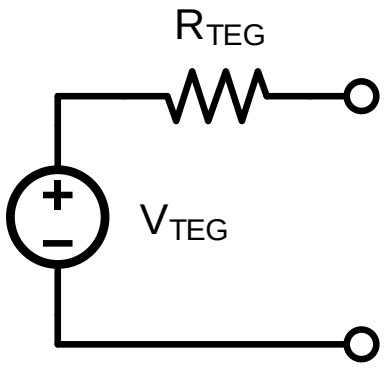


Figure 3-2 Electrical model of a TEG.

3.1.2 Photovoltaic Cell

Photovoltaic (PV) cell is an energy transducer that converts the energy of light directly to electricity based on the photovoltaic effect. Figure 3-3 show a structure of a PV cell, which is made of PN junctions, metal grids, and a metal base for connections.

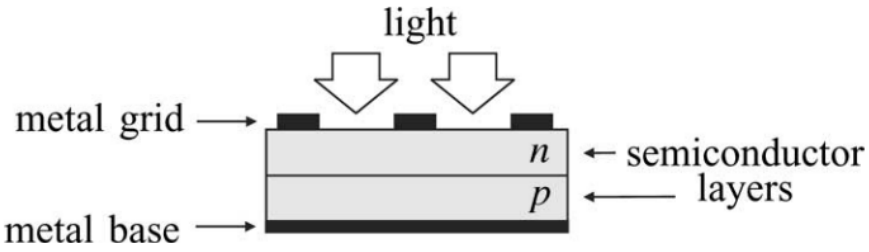


Figure 3-3 Physical structure of a PV cell. [32]

An equivalent electrical model of PV cell is shown in Figure 3-4, where I_{PV} is the photogenerated current, D_{PV} is the diode generated by the PN junction, and R_S and R_P are the series and parallel resistance due to the non-idealities of the PV cell. The origin of R_P could be the leakage around the edge of the PV cell and diffusion paths along boundaries. The series resistance R_S is due to resistance of metal contacts with the P-type and N-type materials and the resistance of the semiconductor layers and the metallic fingers. [33]

The I-V equation of the PV electrical model can be represented as

$$I = I_{PV} - I_0 \left[exp\left(\frac{V + I \times R_S}{a \times n_S \times V_T} \right) - 1 \right] - \frac{V + I \times R_S}{R_P} \tag{3.2}$$

where I_0 is the reverse saturation current of the diode, V_T is the thermal voltage, n_S is the number of PV cells in series, and a is the diode ideality factor. [32]

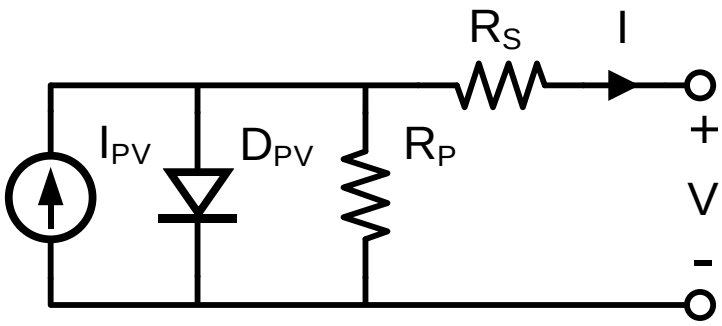


Figure 3-4 Electrical model of a PV cell.

3.1.3 Overview of EHPMU Architecture

Different EHPMU architectures have been developed in recent years, which mainly includes two kind of architectures. The first one separates the energy harvesting interface and DC-DC converter as shown in Figure 3-5. [34] The downsides are more power loss due to cascaded stage and two inductors needed which increases the cost and form factor. Combing the two blocks together, the one-stage power-delivery architecture is shown Figure 3-6, which has a higher conversion efficiency with fewer power transistors, but it suffers from cross regulation issue due to the inductor sharing scheme. [35]

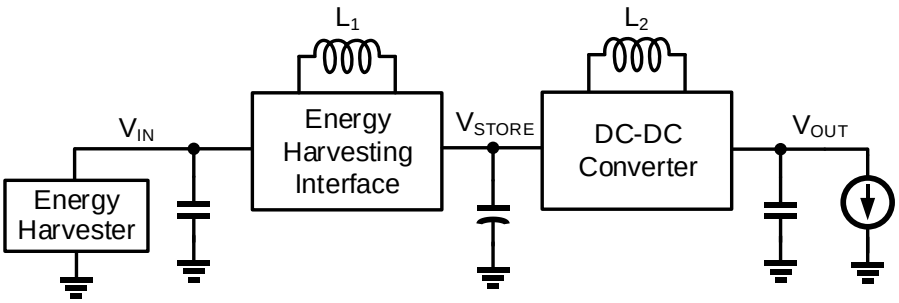


Figure 3-5 A traditional two-stage architecture for EHPMU.

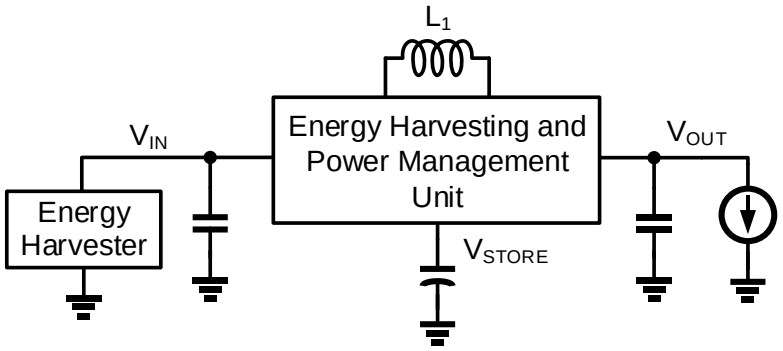


Figure 3-6 Improved EHPMU architecture with only one stage.

To extract energy from multi-modal energy harvesters and provide multiple voltage supplies for the loads, multi-input multi-output EHPMUs [36]-[39] are becoming prevalent in recent years. A classic architecture for the multi-input single-inductor multi-output (MISIMO) EHPMU is shown in Figure 3-7, which includes power switches, comparators, MPPT detection blocks, a zero-current detector (ZCD), and a digital controller. The comparator on the bottom left sets the output voltage of the energy transducers to V_{MPPT}, which is generated by the MPPT detector as the optimal voltage for power transfer. The comparators on the bottom right regulate each output voltage to its reference voltage, V_{REF}. Options for these comparators include a hysteresis comparator for asynchronous control or a clock-driven comparator for synchronous control, which uses time information as the hysteresis value for the regulation. For sub-μA designs, the power converters usually work in discontinuous-conduction mode (DCM) due to the ultra-light load at the output.

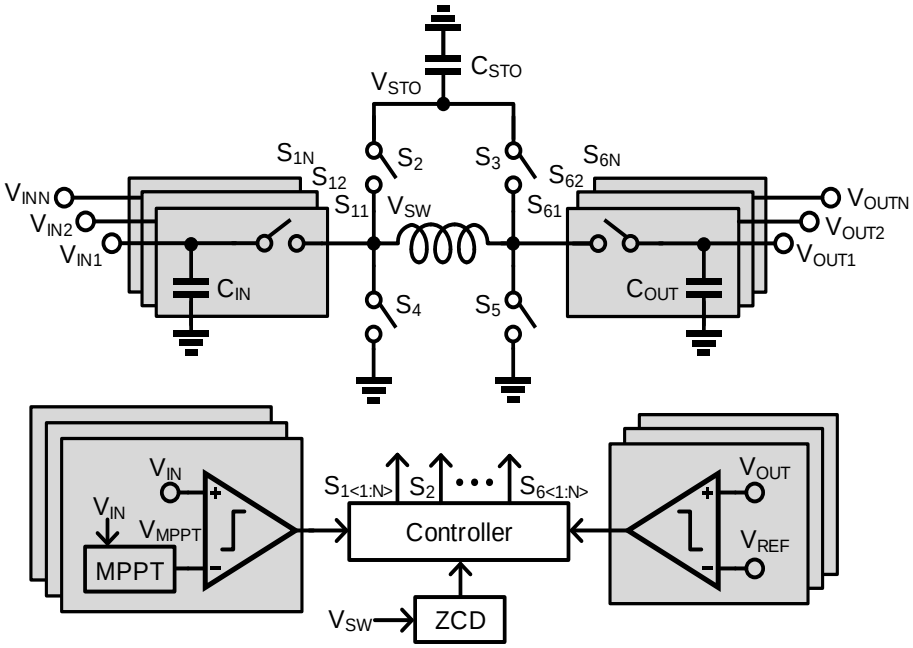


Figure 3-7 A classic architecture of a MISIMO EHPMU.

This MISIMO architecture has several advantages. First, it has a very low quiescent current, since most of the components are digital circuits including the digital control, comparators, and passives. Also, the hysteresis control works as pulse-frequency modulation (PFM). When the load is larger, the frequency of switching pulses increases, and when the load is reduced, the frequency reduces correspondingly. The controller can be improved to adaptively change the on-time of the switch, T_{ON}, as well as the switching frequency, F_{SW}. Second, it has a fast response to the load change since the output changes can be immediately detected by the hysteresis control. Whenever the output voltage is lower than its V_{REF}, it triggers the comparator and toggles the power transistors to send energy to the appropriate loads, which is not like a traditional analog feedback loop whose step response depends on the control loop bandwidth. Third, the low-complexity control only includes the comparators and digital logic, unlike an analog feedback loop, which is often used in high output power applications and needs a compensator for the loop stability [40]. Fourth, this structure has a high flexibility, which can be easily extended to any number of inputs and outputs, allowing connection with more energy harvesters and more power supplies for load circuits.

Besides the adaptive T_{ON} and F_{SW}, some other techniques have also been proposed to reduce the quiescent current and increase the power efficiency for this structure, like switch size modulation [36] and automatic source selection [39].

3.2 Prior Arts and Design Challenges

Due to the advantages introduced above, the MISIMO EHPMU is becoming popular in recent years and many architecture variants have been investigated and developed. The architecture proposed in [36] can extract energy from three DC energy sources and provide three outputs to loads. However, this structure does not include the MPPT block, cold start-up and voltage references, which prevent it from being fully autonomous and deployable. Also, it does not have the ability to extract energy from AC energy sources, like piezoelectric harvesters. Furthermore, the minimum load power is 1μA, so this design is not optimized for powering sub-μW loads, which is critical for the nW IoT SoCs. Another MISIMO EHPMU architecture is proposed in [37]. This architecture can extract energy from both DC and AC energy sources and includes cold start-up circuit, MPPT, and voltage references. However, it cannot cold start from the input of piezoelectric harvester, which prevents it from deploying in a purely mechanical vibration environment. Also, it does not have any power clamp for the energy store node to protect the circuits from over-voltage. So, this design is also not fully deployable. More importantly, to reduce the quiescent current, the control circuits for both input and output circuits have been highly reused, which can cause severe cross regulation issues and deteriorate the transient response performance.

To power the emerging nW self-powered IoT systems with different energy sources in the environment, the MISIMO EHPMU is a very effective solution, but it also has many design challenges, which are listed below.

- To make the IoT devices fully autonomous, the MISIMO EHPMU should include all the components for power delivery circuits, such as voltage references, MPPT, clock

generators, and cold start-up circuit, such that the IoT systems can be fully deployable and function as a “plug-and-play” device.

- For nW IoT systems, reducing the quiescent current of MISIMO EHPMU is critical to achieve a high efficiency when delivering ultra-low output power. So, how to design a EHPMU system with nanowatt power consumption with a high performance including wide dynamic load range and fast transient response is very challenging.
- To deploy IoT devices in all kinds of environment, the ability of cold start from multi-modal energy sources is necessary. So, another challenge is how to design a cold start-up circuit which can make the EHPMU system boost from all energy modalities.

3.3 Proposed MISIMO EHPMU Architecture

In this work, we propose a fully autonomous and deployable multi-modal EHPMU platform using the MISIMO architecture. The proposed EHPMU platform achieves power extraction from three different energy modalities (TEG/PV/PEH) and provides four voltage supplies to power different types of loads based on their specific requirements.

Figure 3-8 shows the system block diagram of the proposed multi-modal EHPMU platform, which includes the MISIMO power stage and the control blocks including the comparator detection circuits for each of the inputs and outputs, a source controller, a load controller, cold start-up circuits, and auxiliary blocks. The proposed EHPMU architecture has many advantages over traditional ones. First, it extracts energy from three energy modalities including DC and AC energy using only one single inductor and can power four custom loads with 3.3V for IO output, 1.2V for high analog and RF, 0.6V for low analog and 0.6V for digital separately. Second, the EHPMU integrates a multi-modal cold start-up circuit, which can startup from any of the three energy harvesters. The switches M_{L_1A} and M_{L_3A} are used for startup process and always keeps turn-on during normal operation. Third, the EHPMU integrates all the component it needs, so it is

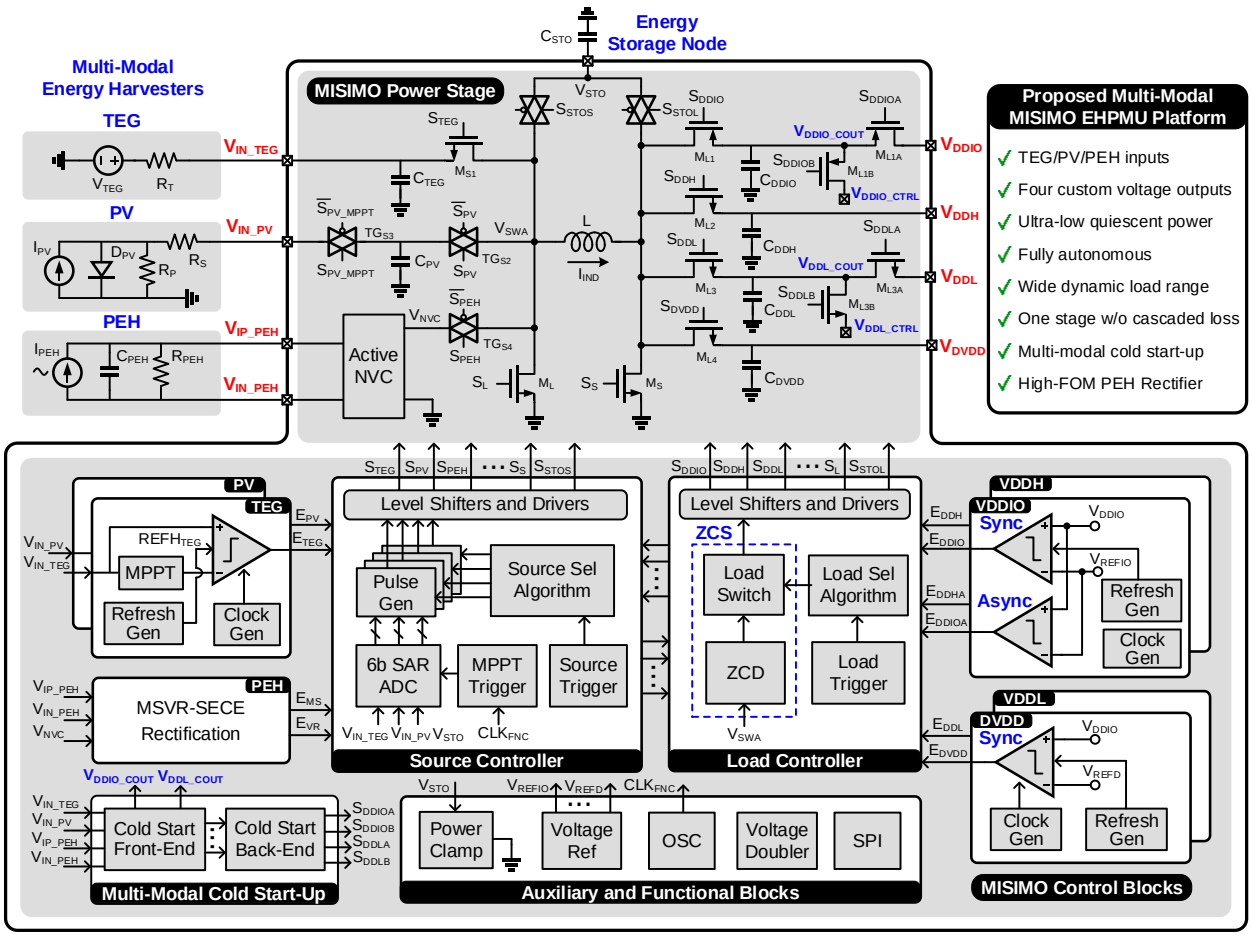


Figure 3-8 Architecture of the proposed MISIMO EHPMU.

fully autonomous and deployable. The platform has everything integrated on-chip except for the passive components, so it can be directly deployed in a variety of the environmental conditions Finally, this platform has the benefit of flexible configuration with the clock, comparator, and frequency modulation, and pulse generation for the each of the input and output. In such way the platform can be figured with any number of the inputs and outputs using the enable and disable control bits.

When delivering ultra-low power from energy sources to the loads, which is a common case for ULP IoT applications, the EHPMU quiescent power should be very low to keep a high conversion efficiency. To reduce the power consumption, several techniques have been adopted

in this design. First, two voltage domains have been used. All the control blocks except the voltage references are powered with a 0.6V low voltage, which is shared with the output voltage with EHPMU. The EHPMU drivers are connected with a 3.3V high voltage, which is shared with V_{DDIO} through level-shifters. Second, most of the structures are achieved in digital domain, which eliminates the constant current consumption. Third, each of the input and output has their own clock frequency and on-time control, which can minimize the power consumption according to their own power delivery situations.

3.4 Design Implementations

3.4.1 MISIMO Control Algorithm

The MISIMO EHPMU needs appropriate source and load control algorithms to guarantee a correct operation and keep a high performance. The control algorithm proposed in this work is shown in Figure 3-9. This algorithm starts with situations, in which any of the loads needs power delivery or any of the sources has the power extraction ready. In the source selection algorithm, first, the EHPMU will detect if the PEH needs to be regulated to prevent it from over voltage. Then it will detect if the load has any sudden voltage drop through the asynchronous path, which leads to the selection of the supercapacitor as the energy source. If not, the energy harvester is selected based on the priority of PEH, PV and TEG. If none of source is ready, then the supercapacitor will be selected as the energy source. In the load selection algorithm, it detects any event-driven signals for any large load steps. Then it detects the voltage outputs by their priority. V_{DDIO} and V_{DDH} have higher priority than V_{DDL} and V_{DVDD} due to potentially large load current step. If none of the outputs needs energy, then it selects the supercapacitor as the load to store the energy from inputs. This algorithm has several advantages over general first-come-first-serve algorithm. First, it includes the event-driven fast transient response by triggering the load asynchronous signals and

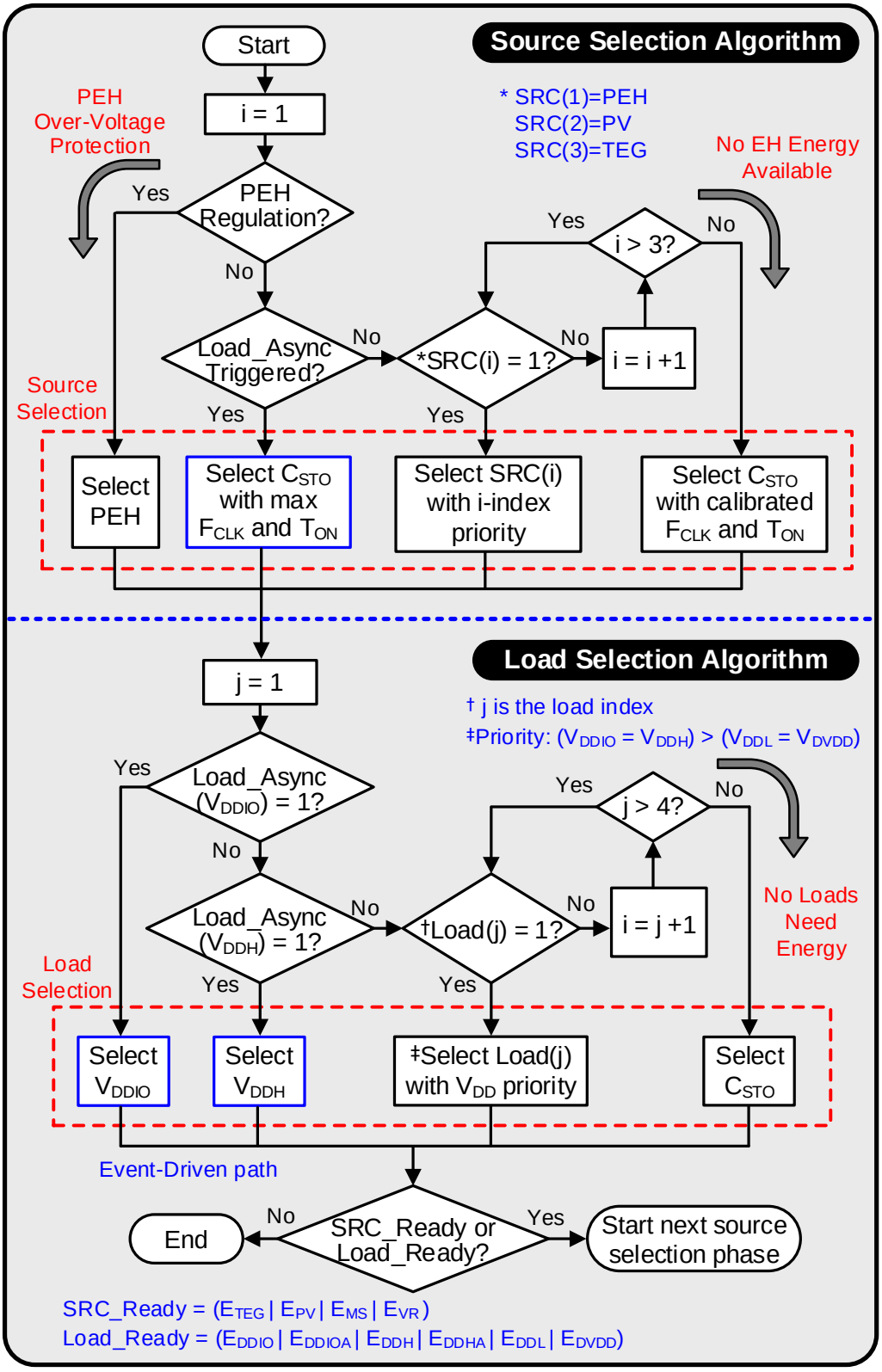


Figure 3-9 Flowchart of the source and load selection algorithm

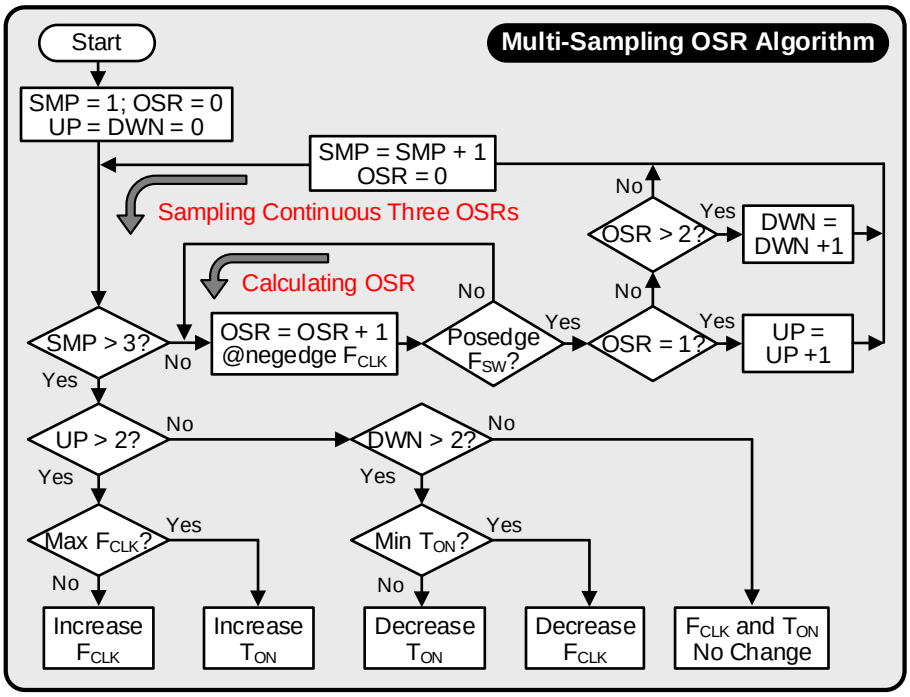


Figure 3-10 Flowchart of the multi-sampling OSR algorithm.

enabling the maximum F_{CLK} and T_{ON}. Second, the characteristics of PEH has been considered by regulating the PEH and protecting it from over-voltage. Third, the sources and loads are assigned with specific priorities which are based on the specific requirement and characteristics, which helps reduce the across regulation issue.

The adaptive F_{CLK} and T_{ON} are effective ways to scale quiescent power to the output power. Traditionally, for PFM control, the over-sampling ratio (OSR) of clock frequency, F_{CLK}, can directly change with the switching frequency F_{SW}. However, for the MISIMO architecture, it can introduce a severe cross regulation issue due to the unstable OSR. In this work, a OSR multi-sampling technique is proposed as shown in Figure 3-10, which samples continuous three OSR values. If two of them are larger than 2, then the F_{CLK} or T_{ON} would increase. If two of them are less than 1, then the F_{CLK} and T_{ON} would decrease. By sampling continuous multiple OSR values, the cross-regulation issue can be greatly relieved.

3.4.2 MSVR-SECE Rectifier

The PEH rectifier determines the energy-extraction gain of the piezo harvesting. The SECE rectifier includes a DC-DC converter, which is ideal for MISIMO architecture. However, there are mainly two issues for traditional SECE rectifier. First, the SECE needs a large inductor which is up to mH and is not compatible with the inductor for other energy harvesting interfaces. Second, when the input power is large, the voltage on the PEH can be larger than the process maximum voltages, so SECE input dynamic range is limited by the process maximum voltage. To address those issues, a multi-step voltage-regulating (MSVR) SECE is proposed in this work. The block diagram of the MSVR-SECE is shown in Figure 3-11, which includes an active negative voltage converter (NVC), a voltage-regulation control and a multi-step SECE control.

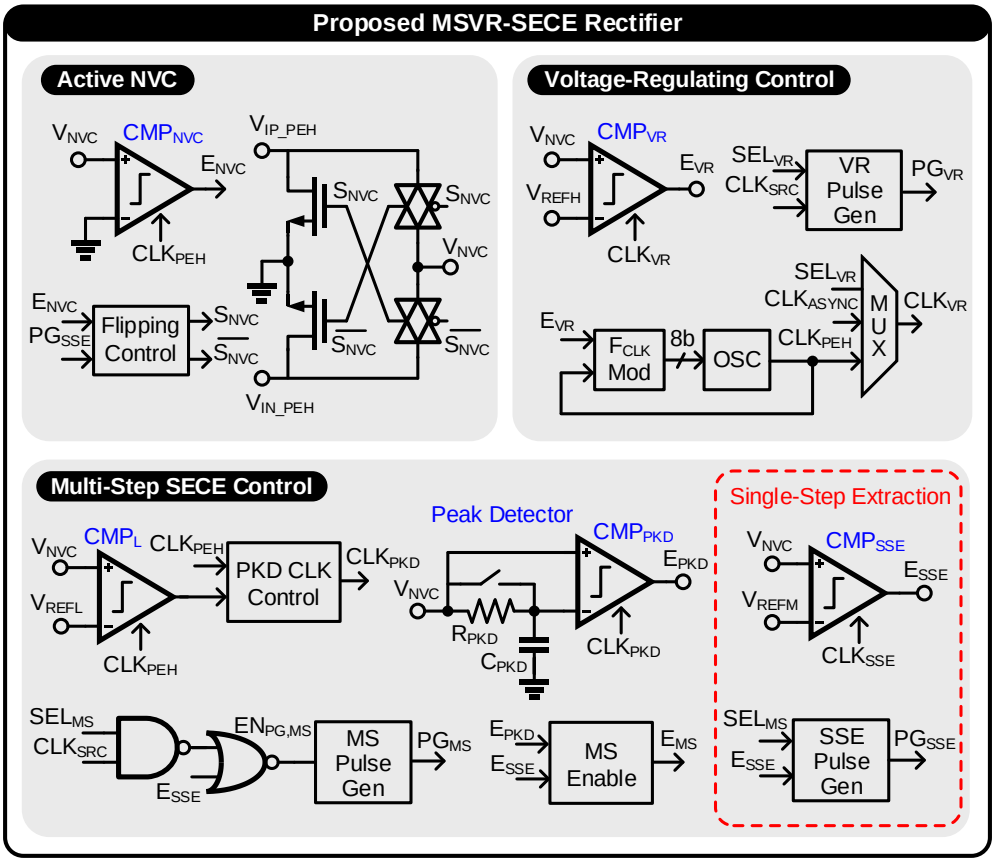


Figure 3-11 Schematic of the proposed MSVR-SECE rectifier.

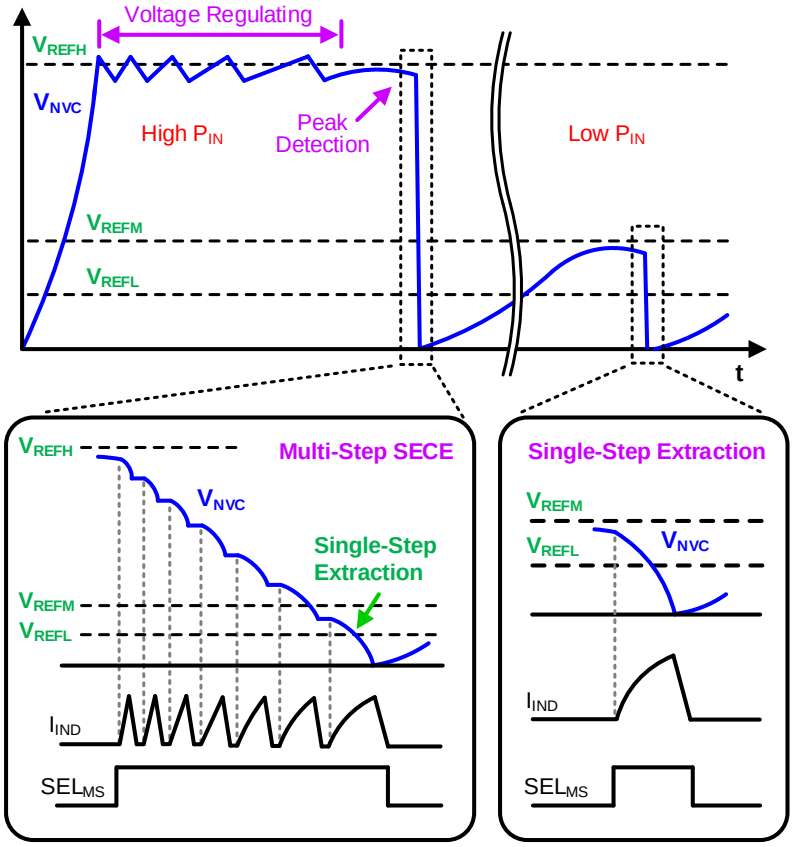


Figure 3-12 Operating waveform of the MSVR-SECE rectifier.

Figure 3-12 shows the operating waveform of the proposed MSVR-SECE rectifier. When the input power is larger than the rectifier high threshold, V_{REFH}, the rectifier will trigger the voltage regulating control, which limits the maximum voltage to V_{REFH} and protects the circuits from over-voltage. When the PEH current reverses the direction, it can be detected by the peak detector and then triggers the multi-step control. The step number is adaptive to the voltage on the PEH which can create a constant peak inductor current regardless the voltage change. When the voltage is lower than the medium threshold, V_{REFM}, it will trigger the single-step extraction phase, which finishes the multi-step extraction. When in the input power is lower than the medium threshold but higher than the low threshold, V_{REFL}, it just uses the single-step extraction for energy harvesting, which is the same as the traditional SECE rectifier.

3.4.3 Multi-modal Cold Start-up Circuit

Figure 3-13 shows the block diagram of the proposed multi-modal cold start-up circuits, which can cold start from any of the three energy harvesters. During cold start, instead of the charging the supercapacitor, the input charges the capacitors on V_{DDIO} and V_{DDL} rails, which are detected by the two voltage monitors. Once the capacitors, C_{DDIO} and C_{DDL}, are fully charged, the cold start-up block is turned off to save power. The cold start-up is enabled once the voltage on the supercapacitor is lower than around 0.6V. The cold start-up also generates the power-on-reset (POR) signal for the EHPMU and outputs enabling sequence to bring up the four voltage supplies.

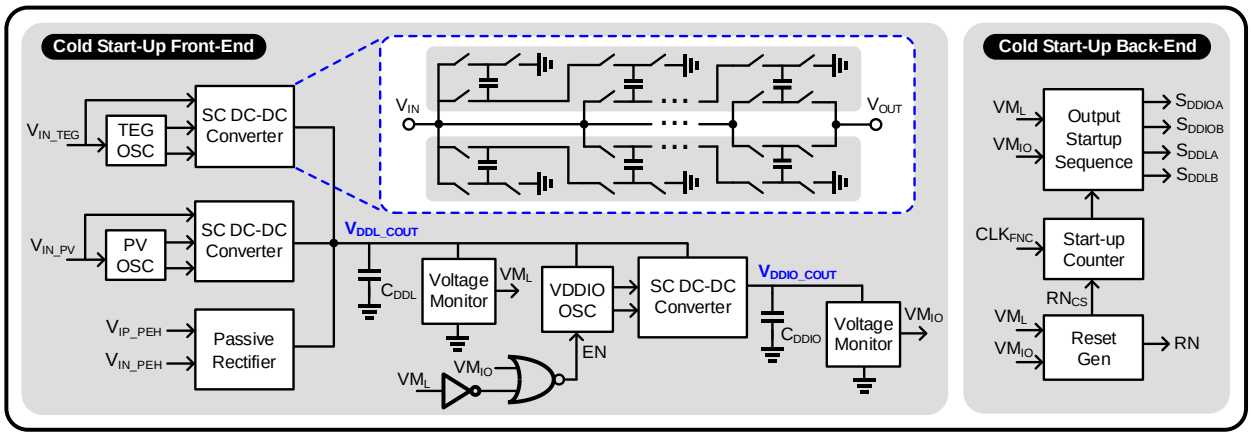


Figure 3-13 Block diagram of the multi-modal cold start-up circuit.

3.4.4 Comparator and Level-Shifter

The control circuits of the system are powered by two voltage supplies, which is shared with V_{DDIO} and V_{DDL}. The V_{DDIO} powers the voltage references, level-shifters and drivers. All other control blocks are powered by the 0.6V V_{DDL}. So, in order to work under low voltage supply with a wide input range, a switched-capacitor comparator has been used in this work. The level-shifter also needs low power consumption and low latency, so it adopts the structure combining thin and thick oxide transistors for voltage protection as shown in Figure 3-14. [41]

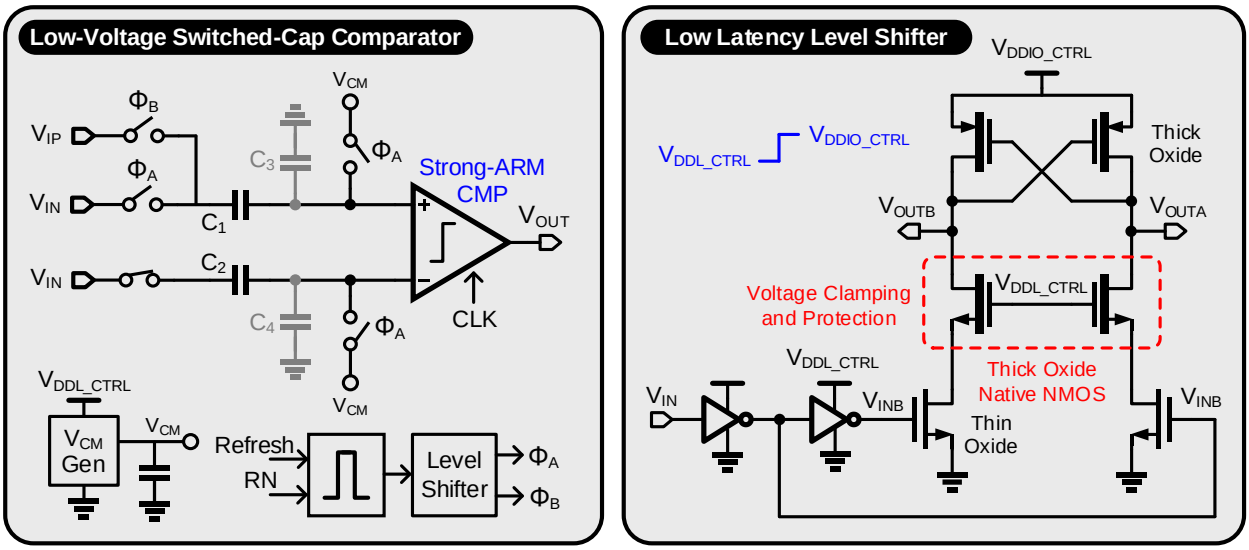


Figure 3-14 Schematic of the switched-capacitor comparator and level-shifter.

3.5 Measurement Results

The MISIMO EHPMU is fabricated in 65nm CMOS technology with an area of 3.11mm^2. Figure 3-15 shows the chip micrograph and the prototype of the EHPMU on the testing board connected with three energy harvesters is shown in Figure 3-16.

The measured cold start-up waveform from TEG when V_{TEG} is 240mV is shown in Figure 3-17. As we can see, V_{TEG} charges the V_{DDL_COUT} first and V_{DDIO_COUT} is charged by V_{DDL_COUT} using a voltage hysteresis between 600mV and 700mV. Once the V_{DDL_COUT} and V_{DDL_COUT} are charged up, which is detected by the voltage monitors, the EHPMU brings the four output voltage supplies. Figure 3-18 and Figure 3-19 show the cold start-up waveforms from PV cell and PEH. During cold start, the start-up circuit generates a power-on-reset (POR) signal until the on-chip voltage references are fully up.

Figure 3-20 shows the measured steady-state waveform at the inputs for three energy harvesters. As we can see, the EHPMU can extract energy from TEG, PV cell and PEH simultaneously. The voltage pulses on the TEG and PV cell waveforms are the open circuit

voltages used to generate the MPPT voltages. Figure 3-21 shows the measured detailed waveform of the proposed MSVR-SECE rectifier, which shows the voltage regulating and the multi-step energy extractions every time the PEH changes the vibration direction.

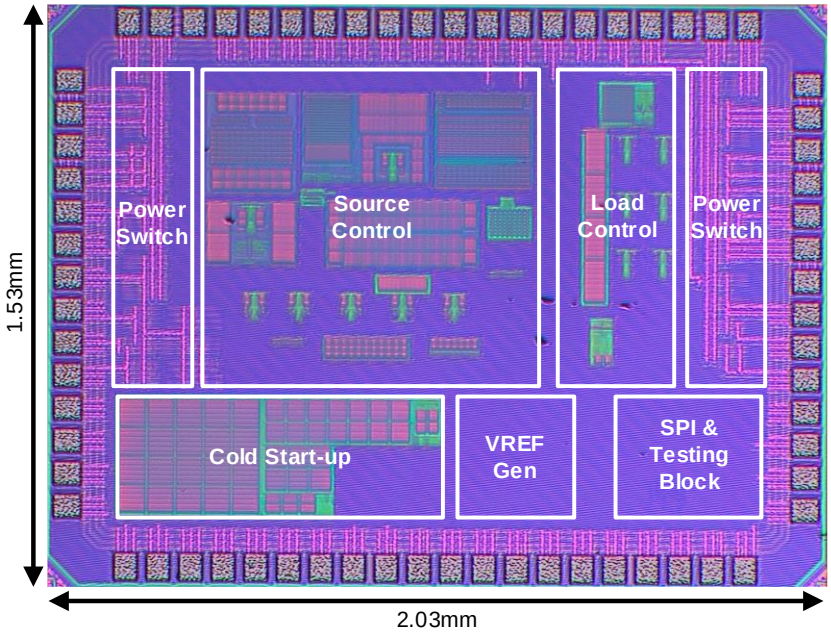


Figure 3-15 Chip micrograph.

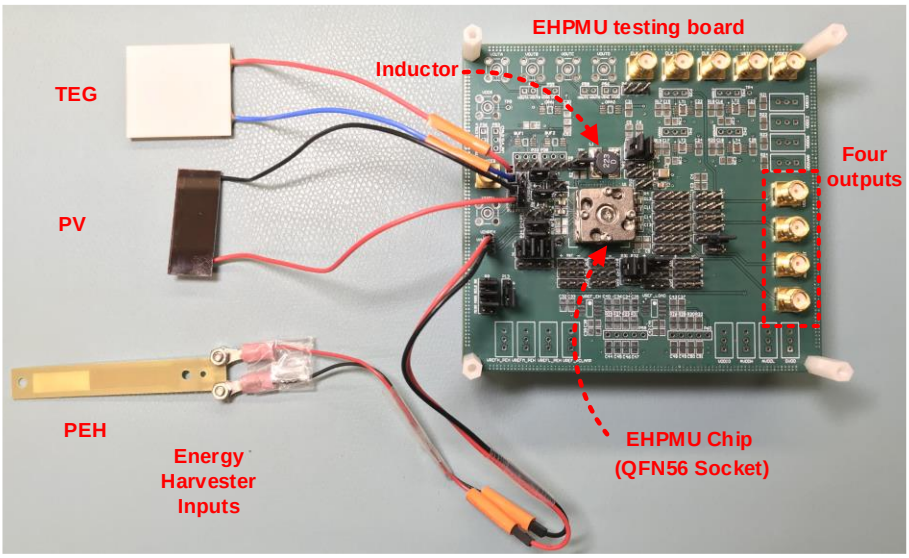


Figure 3-16 Prototype of the MISIMO EHPMU.

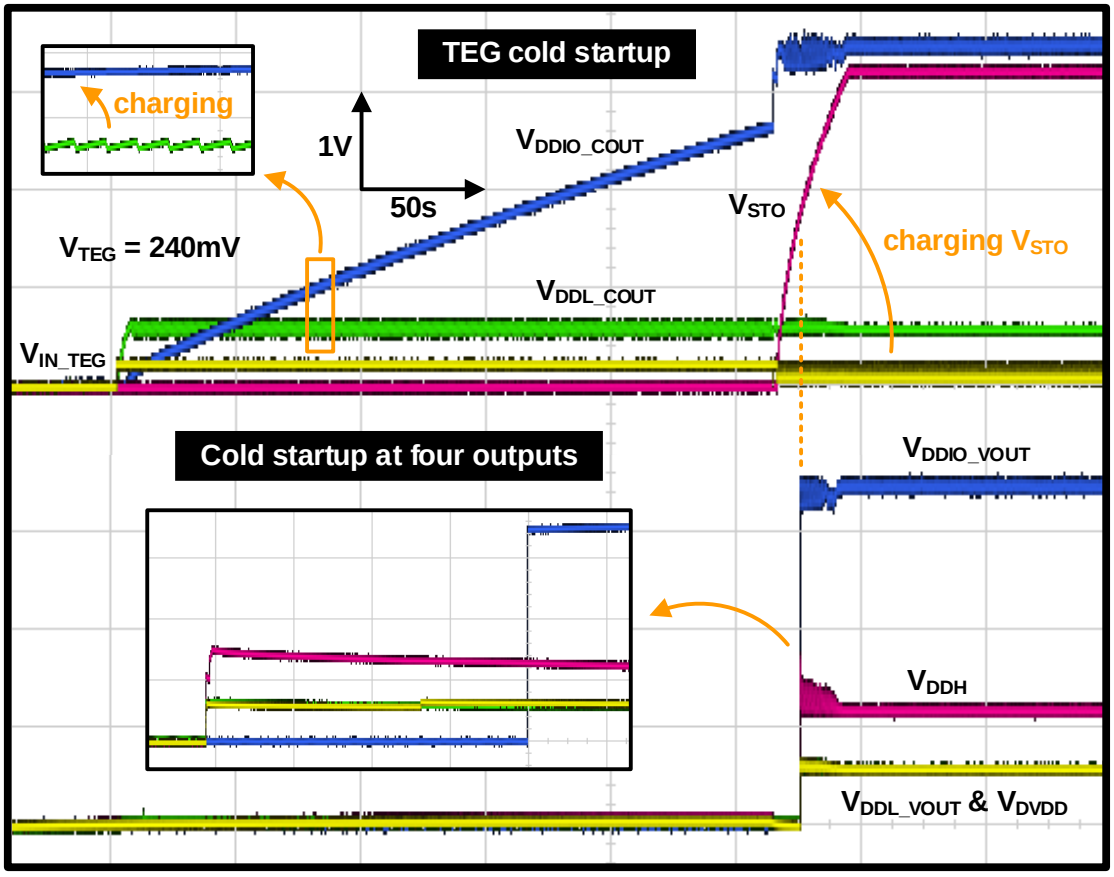


Figure 3-17 Measured TEG cold start-up waveform.

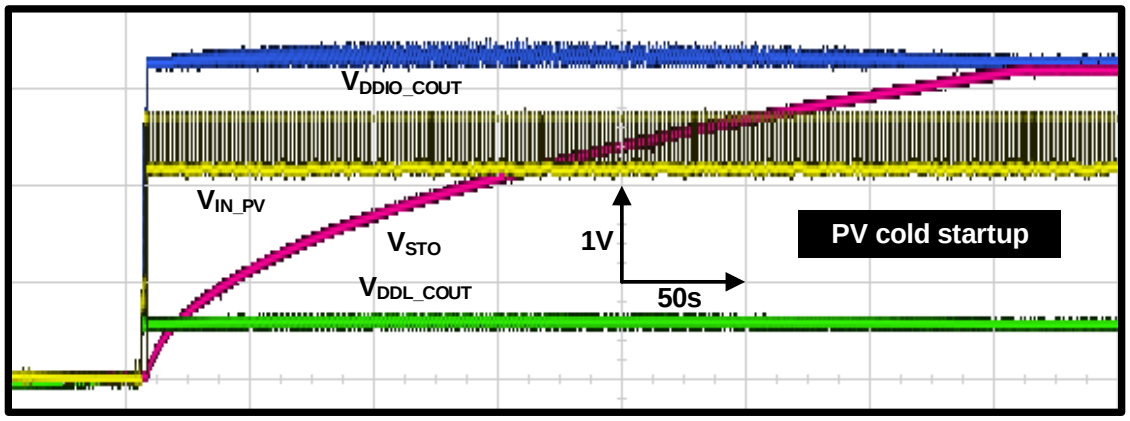


Figure 3-18 Measured cold start-up waveform from PV cell.

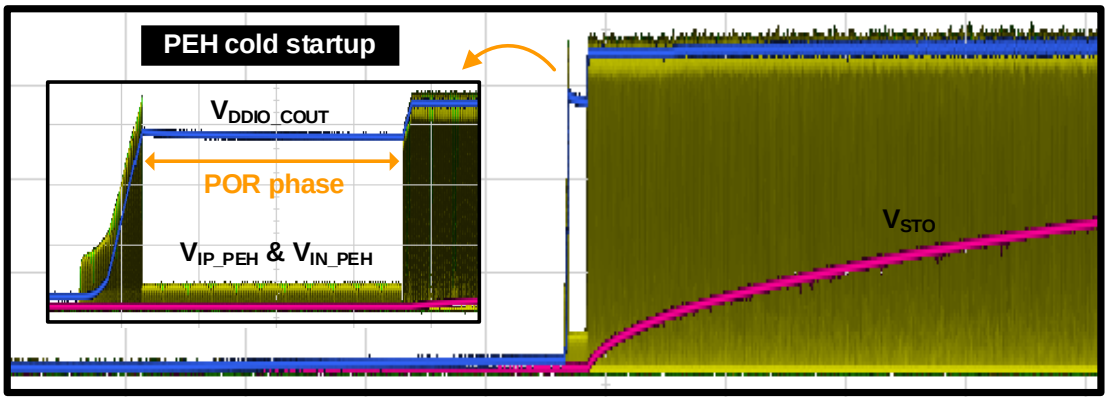


Figure 3-19 Measured cold start-up waveform from PEH.

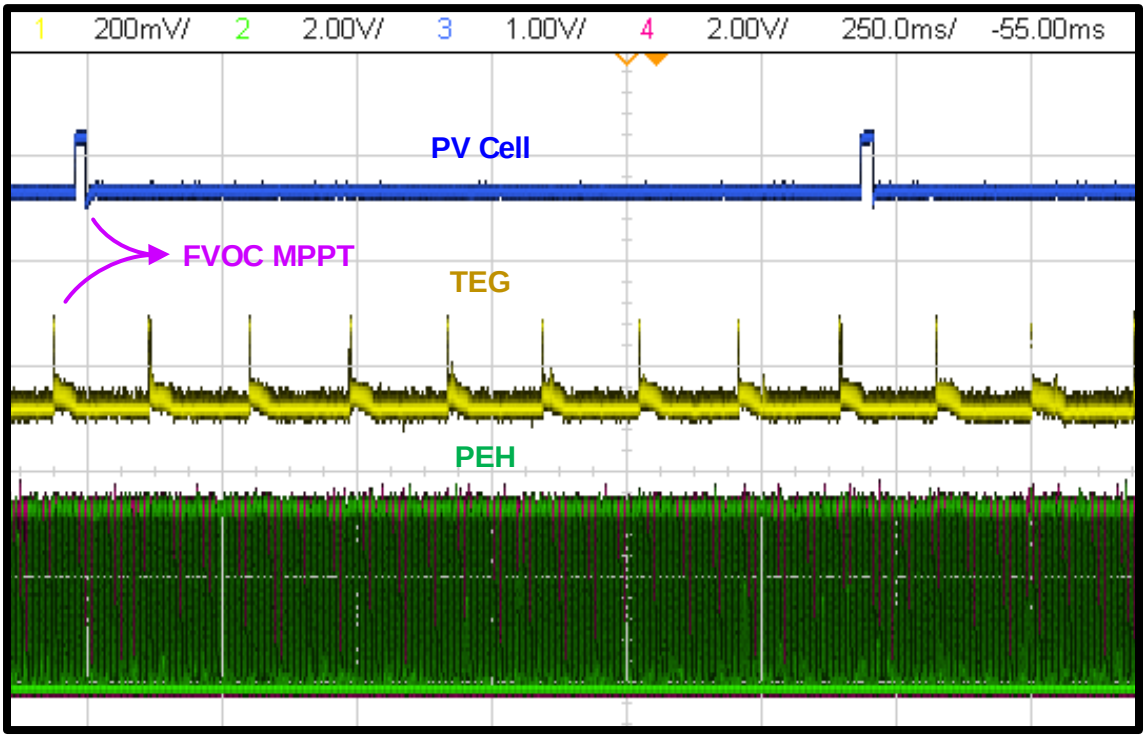


Figure 3-20 Measured steady-state waveform of the EHPMU

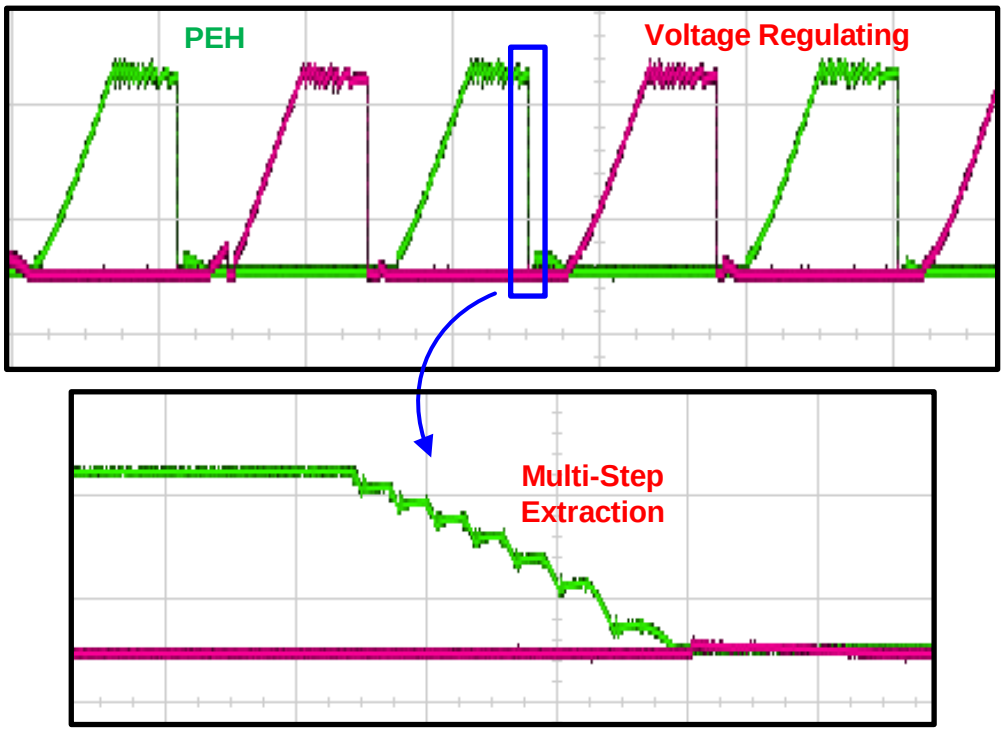


Figure 3-21 Measured transient waveform of the proposed MSVR-SECE rectifier.

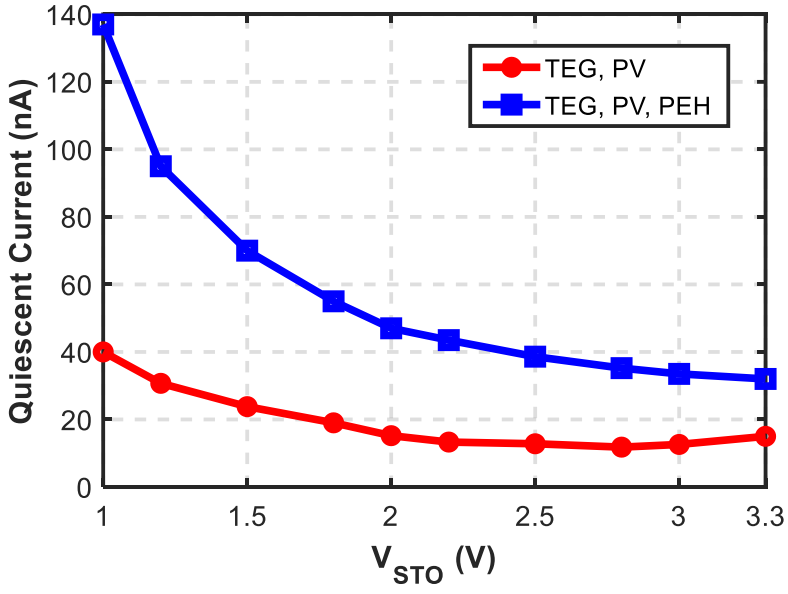


Figure 3-22 Measured quiescent current vs V_{STO}.

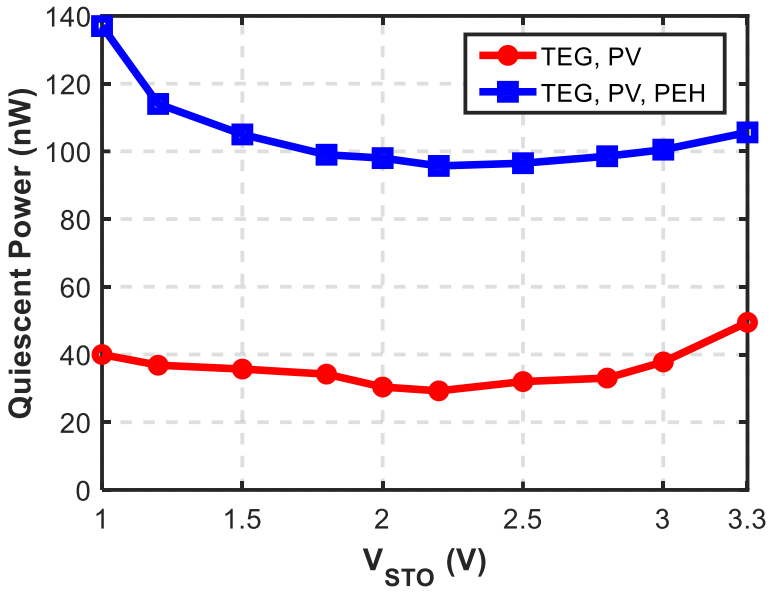


Figure 3-23 Measured quiescent power vs V_{STO}.

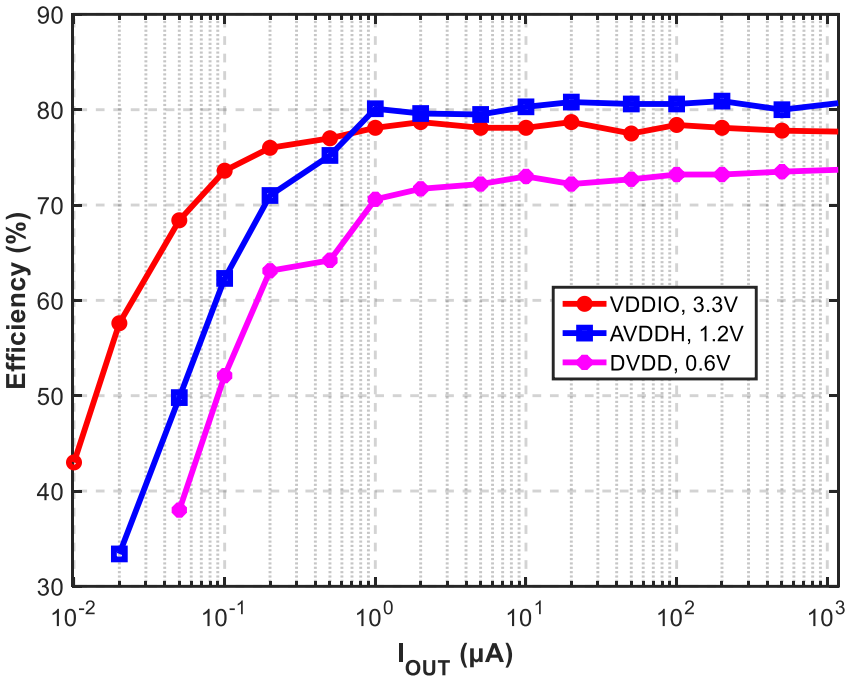


Figure 3-24 Measured power efficiency at the outputs.

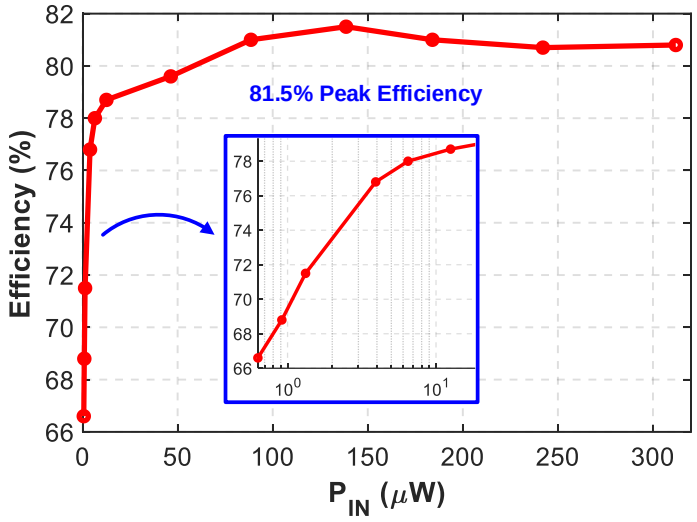


Figure 3-25 Measured conversion efficiency of the PV cell.

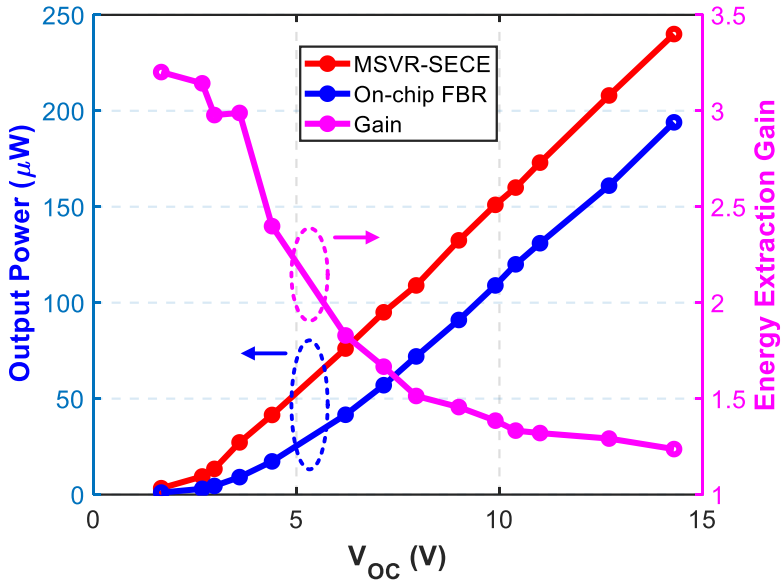


Figure 3-26 Measured MSVR-SECE output power and energy extraction gain.

The measured quiescent current is shown in Figure 3-22 with two configurations. The minimum quiescent current when all three energy harvesters are enabled is 32nA and when only TEG and PV harvesting modalities are enabled, the quiescent current is down to 12nA. Figure 3-23 shows the measured quiescent power consumption across V_{STO}. The minimum quiescent

power is consumed when V_{STO} is around 2.2V. The measured power efficiency for different voltage supplies is shown in Figure 2-24 with a peak efficiency of 81% for the 1.2V voltage rail. Figure 2-25 shows the measured conversion efficiency of the PV cell with peak efficiency of 81.5%. The measured output power of the MSVR-SECE rectifier and its energy extraction gain are shown in Figure 2-26. The proposed MSVR-SECE can extract maximum 3.2× energy compared with on-chip FBR.

Table 3-1 shows the performance comparison with state-of-the-art MISIMO EHPMUs. As we can see, our EHPMU has a quiescent current of only 32nA and when TEG and PV are enabled, it has the lowest 12nA quiescent power. Our EHPMU also achieve the widest dynamic range from 10nA to 1.2mA and can cold start from all three energy harvesters.

Table 3-1 Performance comparison with state-of-the-art MISIMO EHPMUs

	[42] ISSCC2016	[43] JSSC2015	[39] JSSC2019	[44] ISSCC2018	[37] JSSC2016	[25] JSSC2012	This work
Technology	0.35µm	0.18µm	0.18µm	28nm	0.18µm	0.35µm	**65nm**
Area (mm2)	4	4.62	1.23	0.5*	1.1	15	**3.11**
Energy Harvesters	PV (DC)	PV (DC)	TEG/PV (DC)	TEG/PV/BFC (DC)	PV/RF/PEH (DC+AC)	TEG/PV/PEH (DC+AC)	**TEG/PV/PEH (DC+AC)**
No. of Inputs	1 + Battery	1 + Battery	3 + supercap	3 + Battery	3 + supercap	3 + Battery	**3 + supercap**
No. of Outputs	2 + Battery	2 + Battery	1 + supercap	3 + Battery	1 + supercap	1 + Battery	**4 + supercap**
Converter Topology	1-stage 1-ind Buck-boost	1-stage 1-ind Buck-boost	1-stage 1-ind Buck-boost	1-stage 1-ind Buck-boost	2-stage 1-ind Buck-boost	2-stage 1-ind Buck-boost	**1-stage 1-ind Buck-boost**
Load Regulation Control Scheme	Hysteresis	PFM	PFM	Hysteresis + SSM	PFM	PFM	**PFM + PWM**
L & C_L	22µH & 4.7µF	10µH & 10µF	4.7µH & 10µF	10µH & 1µF	47µH & 10µF	22µH & 15µF	**22µH & 4.7µF**
Piezo Energy Extraction Gain	N/A	N/A	N/A	N/A	1 ×	1 ×	**3.2 ×**
Quiescent Power or Current	200nA	400nW	> 500nW†	262nA	18nA	2.7uA	**12nA (TEG/PV) 32nA (TEG/PV/PEH)**
V_{OUT} (V)	3.6†	3/1.8/1	1.2	0.4 - 1.4	1.2 - 1.8	1.8	**3.3/1.2/0.6/0.6**
Output Power	N/R	1~10mW	2.5µW~10mW	1uW - 60mW	12.6nW~31uW	9 - 540uW	**10nW - 1.2mW**
Dynamic Range	N/R	10,000	4,000	60,000	2,460	60	**120,000**
Peak Efficiency	85%	83%	82%	89%	87%	87%	**81.5%**
Efficiency @ 1µA Output Current	N/R	68%	< 50%	76%	77%	N/R	**80%**
Cold Startup	Yes (PV)	No	Yes (PV)	No	Yes (PV/RF)	No	**Yes (PV/TEG/PEH)**

3.6 Conclusions

In this work, we propose a fully autonomous multi-modal EHPMU platform using the MISIMO architecture. The proposed fully autonomous EHPMU platform achieves power extraction from three energy modalities (TEG/PV/PEH) and powers four custom loads based on their specific requirements. Meanwhile the EHPMU also integrates multi-modal cold start-up block, which can cold start from all three energy harvesters. Measurement results show that the EHPMU achieves 3.2× energy-extraction gain for the piezoelectric harvesting interface, 1.2×10^5 dynamic range and 32nA quiescent current, and an 81.5% peak efficiency.

Chapter 4

4. Sub-nA Low Dropout Regulator

4.1 Introduction

Previous two chapters mainly talked about energy harvesting system design using switched-mode power converters. Although switching power converters provide a high conversion efficiency, they usually need large off-chip inductors which increase form factor and cost. Recently, fully integrated switching voltage regulators [45] [46] are actively investigated by researchers, but they need a very high clock frequency up to hundreds of MHz, which makes them not suitable for ULP IoT systems. Also, the inductor-based power converter generates switching noise and ripple making them hard to directly power voltage-sensitive circuits, such as RF transceivers or high-accuracy sensor interfaces.

To meet the requirements of loads, different types of power converters are usually used together on the power delivery path based on their characteristics, as shown in Figure 4-1. Low dropout regulators (LDOs) are generally used at the last stage of the power train, which provide a clean voltage and fast response to the loads. For a SoC which includes different loading components, LDOs are also used to provide multiples voltage domains due to the advantage of low complexity. In this research, we will look into the design of LDOs for ULP IoT systems.

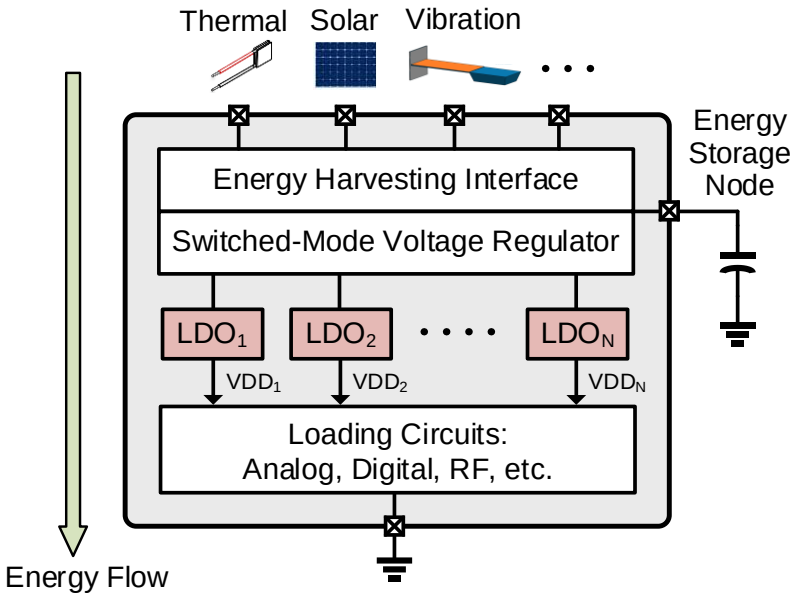


Figure 4-1 Power delivery path in a self-powered IoT SoC.

4.2 Overview of LDO

LDOs can be classified into analog LDOs (ALDOs) and digital LDOs (DLDOs) based on their working principles. An ALDO uses an error amplifier in the feedback loop and has the advantage of fast response time and low output ripple and noise. An DLDO uses digital control in the feedback loop and based on the comparison results of the reference voltage and output voltage, it configures switches to keep a constant output voltage. DLDOs have the advantages of the low voltage operation, good power and performance scalability, and flexible control schemes.

4.2.1 Traditional Analog LDO

A traditional structure of an ALDO [47] is shown in Figure 4-2, which includes an error amplifier, a PMOS power transistor, M_P, and an output decoupling capacitor, C_{OUT}. The loads are represented by a resistor R_L. The LDO output is forced to be the same as the voltage reference, V_{REF}, through the feedback loop. So, the performance of the LDO is determined by the loop

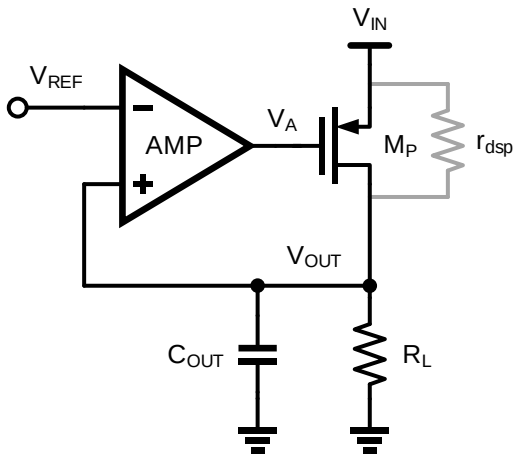


Figure 4-2 Structure of traditional ALDO.

characteristics, including loop gain and bandwidth. The Loop gain, *T(s)*, can be written as

$$T(s) = A_{AMP}(s) \cdot g_{mp} \cdot \left[r_{dsp} \,||\, R_L \,||\, (1/sC_{OUT}) \right] \tag{4.1}$$

where $A_{AMP}(s)$ is the transfer function of error amplifier, r_{dsp} is the resistance due to channel-length modulation of the PMOS transistor, M_P, and g_{mp} is the transconductance of M_P. Loop gain should set to be as high as possible to reduce the residual error. Assuming the error amplifier is a single-pole system in which this pole is at the output node, V_A. So, there are two poles in the feedback loop. To make the loop stable, we usually set the main pole at the output since the output decoupling capacitor, C_{OUT}, normally uses a large off-chip capacitor. ALDO has a simple structure and provides a clean voltage supply and fast load response, however due to the high-performance amplifier, it usually needs a high voltage supply.

4.2.2 Digital LDO Topologies

Recently, digital low dropout regulators (DLDOs) [48]-[50] have brought people's attention. Compared with the analog counterpart, the DLDO has the advantages of low voltage operation, small dropout voltage, flexible control schemes, and synthesizable capability. However, it suffers

from large output ripple and slow transient response. DLDOs can be categorized by the control schemes and classified into synchronous or asynchronous control DLDO. Based on the switching array, it also can be categorized as binary searching and linear searching DLDO.

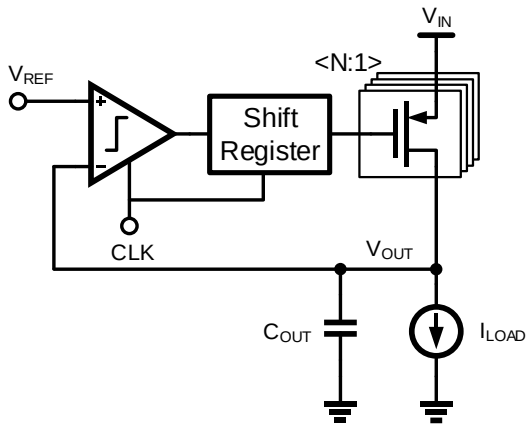
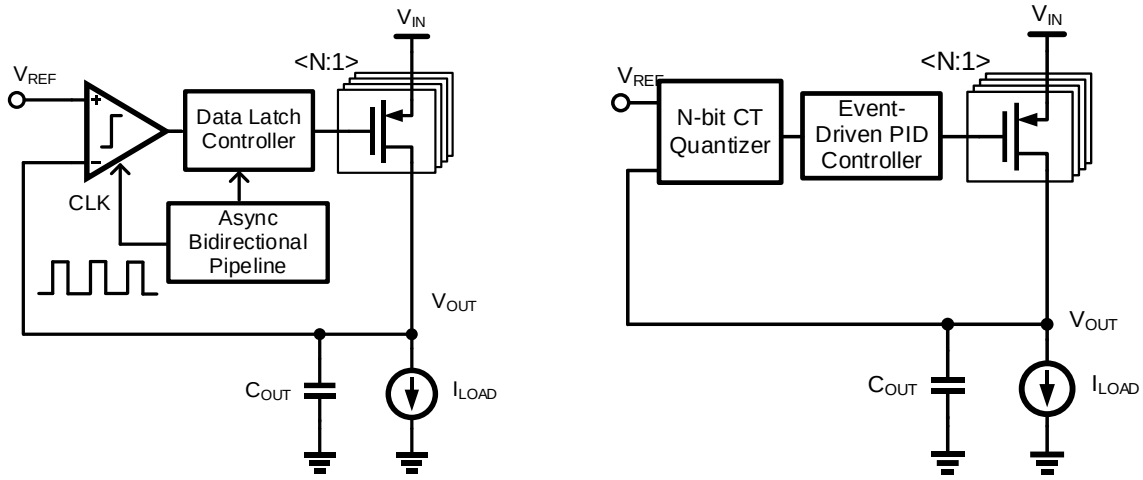


Figure 4-3 Structure of a traditional synchronous DLDO.

A block diagram of a traditional synchronous DLDO is shown in Figure 4-3, which includes a comparator, a shifter register, a PMOS switch array, and an output decoupling capacitor. A synchronous clock-driven comparator is used to compare the output voltage and reference voltage under each clock cycle, and the output of the shift register changes the power switches using a linear searching scheme. This architecture is very simple and has a low design complexity. However, it suffers severe power and performance limitations. The transient performance is directly proportional to the clock frequency, so increasing the clock frequency can enhance the transient response time, but it also directly increases the quiescent power. Moreover, the power switches use linear searching scheme, which also slows the transient speed. The synchronous DLDO changes the switch array at the edge of each of the clock, so the response time is determined by the clock frequency, which at the worst case is one clock period. For a linear searching scheme, the total voltage droop for a synchronous DLDO is

$$\Delta V = I / \left(N \cdot F_{CLK} \cdot C_{OUT} \right) \tag{4.2}$$

where ΔV is the voltage droop, N is the number of clock cycles for V_{OUT} to recover back to the reference voltage, and F_{CLK} is the DLDO clock frequency.



(a) (b)

Figure 4-4 Structures of (a) an asynchronous clock-driven DLDO and (b) an asynchronous event-driven DLDO

To have a fast response time and low power consumption, a better solution is to use an asynchronous control which avoids the slow clock frequency. Figure 4-4 shows the structure of two different types of asynchronous (async) DLDO. The first one is a clock-driven DLDO and the async clock can be generated by the bidirectional pipeline [51], which is triggered by the either an async comparator or control bits from a processor. In such way, it eliminates the constant clock, so it reduces the power consumptions.

The async clock-driven DLDO still needs an async trigger scheme and an oscillator to generate a fast clock after the async trigger. By removing the fast clock, another async scheme which is called event-driven DLDO [52] [53] is shown in Figure 4-4 (b). The latency is reduced from a clock cycle to the delay of the async comparator. However, it needs multiple async comparators for the event-driven detection, which consumes a lot of power.

There are basically four control schemes for digital LDOs, asynchronous and synchronous control, binary searching and linear searching, shown in Figure 4-5. For an ultra-low-power design, synchronous DLDOs that use a high frequency clock for fast response consume too much power, and asynchronous DLDOs can achieve lower current consumption and fast response, but suffer from larger steady-state error. Binary searching can achieve a fast response, but suffers from large ripple and causes large overshoot or undershoot, which may even lead to instability. Linear searching has small ripple, but slow transient response. Recent, more control schemes have been proposed to enhance the LDO performance. Computational LDO [54] [55] has been proposed to increase the settling time by computing the load current changing using either clock cycles or voltage level with ADC. However, it relies on fast clock or complex ADC, which is very power hungry. Hybrid analog and digital LDOs [56] [57] takes the advantages of both ALDO and DLDO, but due to the analog components in Hybrid LDOs, they still need a high voltage supply.

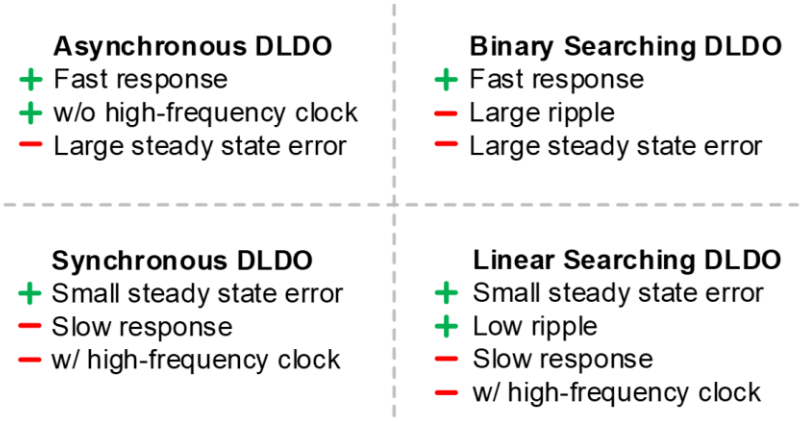


Figure 4-5 Comparison of different control schemes for DLDOs.

The recent power trend of the load circuits shows that there are more and more components working at sub-nW range, which requires the LDO to consume sub-nA quiescent current to power those loads efficiently. Also, previous DLDOs do not target output current in the <10μA range, which is critical to achieve high current efficiency. So, the design challenges for DLDOs include:

- How to achieve sub-nA quiescent current consumption and meanwhile keep a high performance, such as fast transient response, low output voltage ripple, and small steady-state error.
- How to provide a wide output dynamic range from sub-nA up to hundreds of μA with a high current efficiency to cover the load range of nW-to-μW IoT SoCs.

4.3 Sub-nA Digital LDO

If we look at the features of the asynchronous and binary searching, we can find they both have the advantages of fast transient response time, which means if we can combine the two control schemes together, the DLDO can get a better performance during transient step response, such as fast response and low frequency clock to reduce the power consumption. And if we look at the synchronous and linear searching, we can find they both have the advantages during steady state. And if we combine the two control schemes together, the DLDO can get a better performance during steady state, such as small steady state error and low output ripple. So, if all of the four control schemes are combined together, the LDO is supposed to achieve good performance during both transient response and steady state. In this work, we propose an asynchronous binary searching (ABS) and a synchronous linear searching (SLS) scheme to optimize the tradeoff between power consumption and performance.

The proposed DLDO architecture is shown in Figure 4-6. It combines the control schemes of a sync DLDO and an event-driven DLDO, which includes a two async comparator with offsets, which generates a deadzone (DZ) around the voltage reference, V_{REF}. The ABS path includes the async comparators and binary-searching control block. The SLS path includes a clock-driven comparator and the linear-searching control block.

Compared with DLDOs using a single sync or async comparator, this DLDO has several advantages. First, the load step change is monitored by the two async comparators, which avoids

the high frequency clock. Second, compared with the event-driven DLDO, which using N-bit quantizer, the proposed architecture conducts the event-driven comparison with the deadzone, thus only two comparators are needed to keep the quiescent current very low.

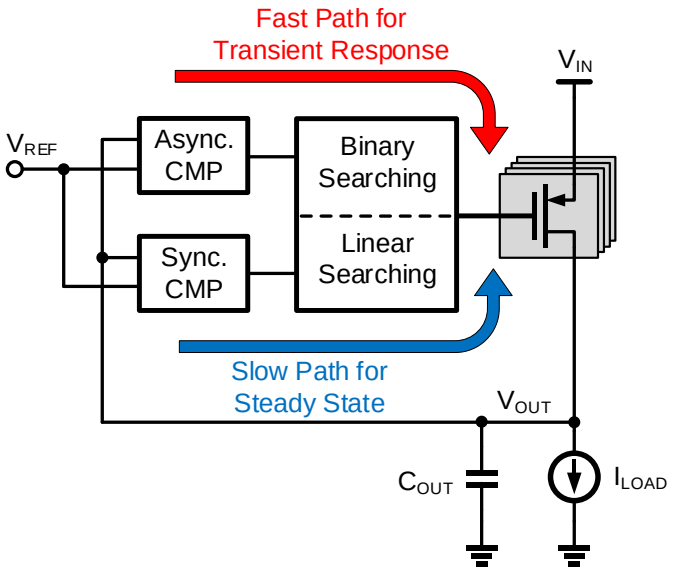


Figure 4-6 Architecture of the hybrid control DLDO.

4.3.1 Proposed Hybrid Control Scheme for DLDO

The operation timing diagram in Figure 4-7 shows how the hybrid LDO works. Whenever there is a current step input, the LDO will go through three phases, ABS, SLS and SRL-bit toggling. If we look at the detailed ABS operation timing diagram, when there is a load step input, V_{OUT} will be pull out of DZ and lower than the low threshold, which makes the output of the asynchronous comparator, *VOL*, become zero. The *VOL* triggers ABS phase immediately and pulls V_{OUT} back to DZ. In such way, it uses the SAR-like binary searching method for the ABS phase. After the ABS, V_{OUT} will go back to DZ but still is not exactly the same as the reference voltage. Next, the LDO triggers the SLS control. During SLS, the LDO linearly adjusts the control bits of the PMOS array using the synchronous comparator to make the V_{OUT} equal to V_{REF}. In order to save power during steady state, after V_{OUT} equals to V_{REF}, the LDO the starts the SRL-bit toggling. In such case, the

DLDO only toggles one transistor instead of driving the whole PMOS array, which reduces the dynamic power dramatically. The ABS-to-SLS transition is triggered by either finishing the full 14b binary search or waiting for a fixed number (3 by default) of clock cycles once V_{OUT} is settled inside the DZ. The flowcharts of the ABS and SLS control algorithms are shown in Figure 4-8.

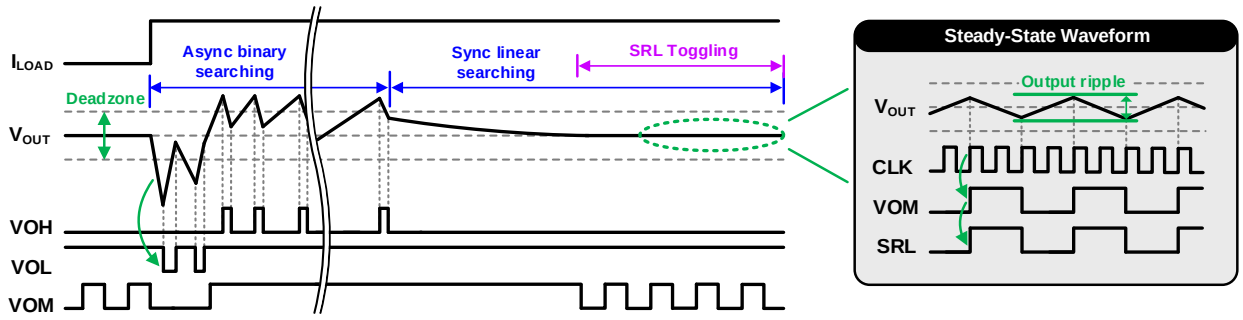


Figure 4-7 Operation timing diagram of the proposed hybrid ABS/SLS control scheme.

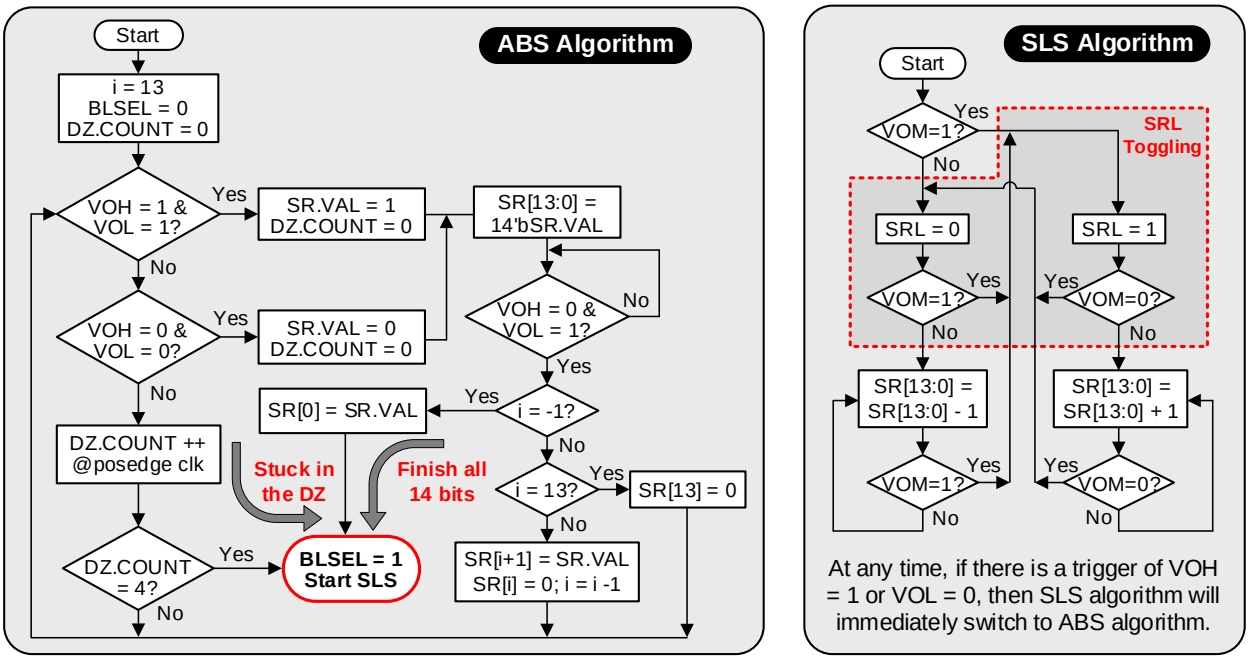


Figure 4-8 Flowcharts of the ABS and SLS control algorithms.

4.3.2 Design Implementations

The schematic of the proposed DLDO is shown is Figure 4-9, which includes two asynchronous comparators, one synchronous comparator, an ABS/SLS digital controller, 14-bit PMOS array, clock generator, VCM generator. The DLDO integrated all the blocks it needs on chip such as the voltage reference or clocks, so it does not need any extra blocks.

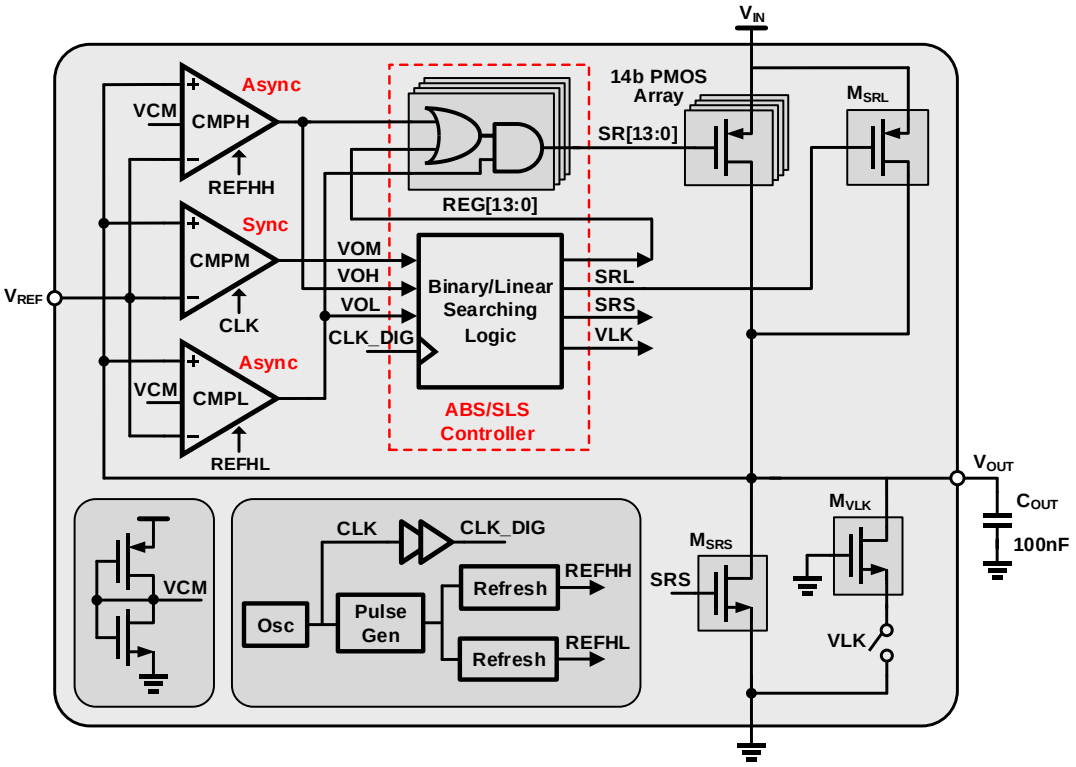


Figure 4-9 Block diagram of the proposed hybrid ABS/SLS DLDO. [58]

The async comparator dominates the transient performance, so it needs to have a good tradeoff between power and latency. The inverter-based structure keeps a high efficiency by utilized both the PMOS and NMOS input transistors. In our design, we adopt an inverter-based and self-biased switched capacitor structure as shown in Figure 4-10, which exactly meets our requirement. First it is very power efficient because of the inverter-based topology, which means given a fixed bias current, this comparator has a higher speed and smaller propagation delay. Second, because of the

isolation function of the switched capacitor, V_{IN} can be very close to the comparator V_{DD}. Third, since the comparator is self-biased, it does not need any extra current bias block. The measured propagation delay of the async comparator is shown in Figure 4-11, which achieves a falling-edge delay of 25.7μs and a rising-edge delay of 15.4μs for 30mV input voltage, while only consuming 111pA bias current.

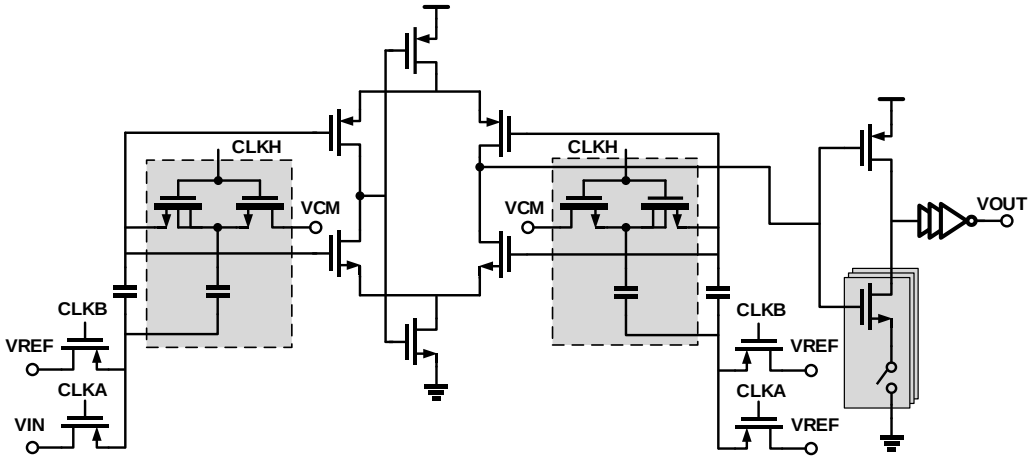


Figure 4-10 Schematic of the inverter-based asynchronous comparator.

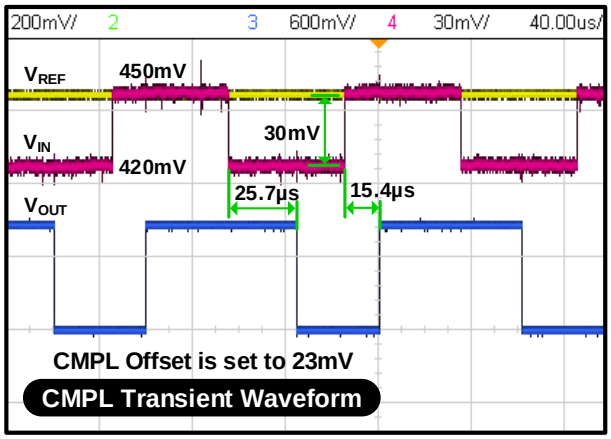


Figure 4-11 Measured propagation delay of the asynchronous comparator.

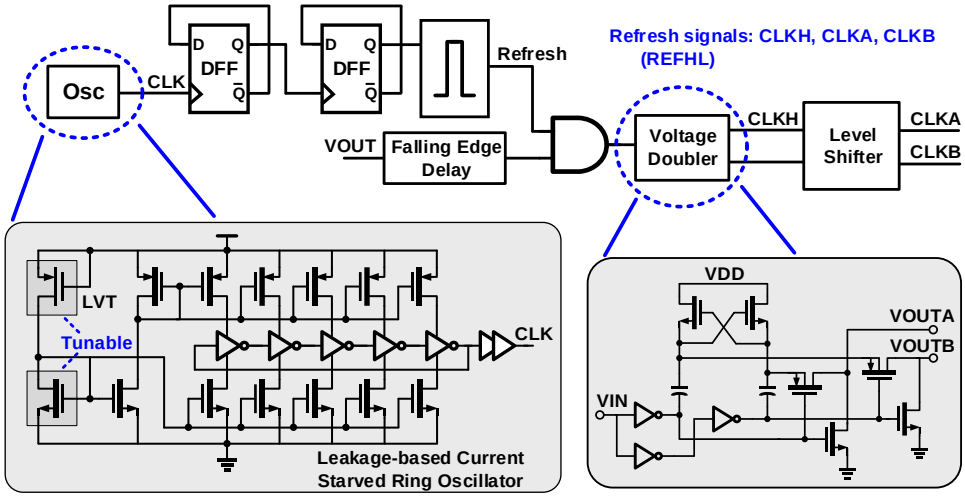


Figure 4-12 Clock generation block.

The clock generation block is used to generate the clock for the digital control logic and the refresh signals for async comparators. The oscillator uses a leakage-based current-starved ring oscillator structure, which is shown in Figure 4-12. The schematic of the digital control logic is shown in Figure 4-13, which includes a binary or linear selection block, a SAR input, a carry input, a binary/linear clock selection block, and 14-bit registers. The inputs of the digital control block are the three comparator outputs and the clock signal, and outputs are *SRS*, *SRL*, *VLK*, and 14 control bits SR[13:0]. The SAR searching path is a fast path, so it is achieved using HVT devices to increase the speed and the linear searching path is a slow path driven by a slow clock, so to reduce the leakage, it adopts the thick oxide devices.

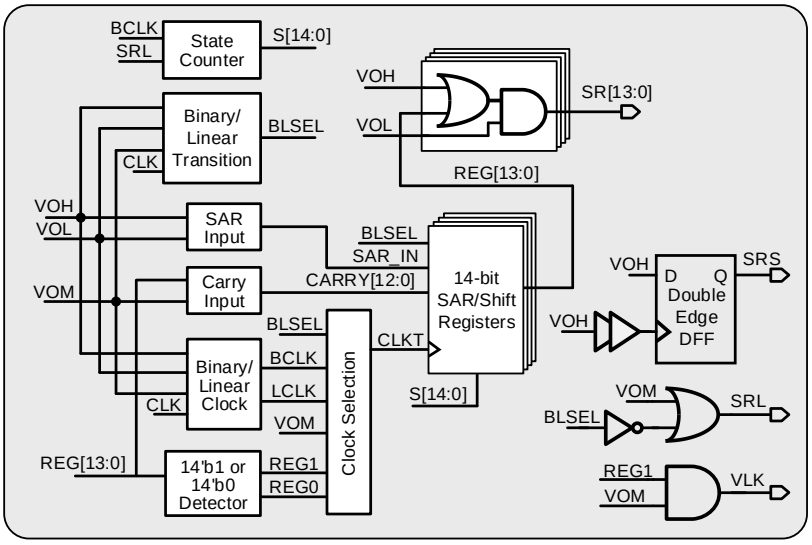


Figure 4-13 Block diagram of the digital control block.

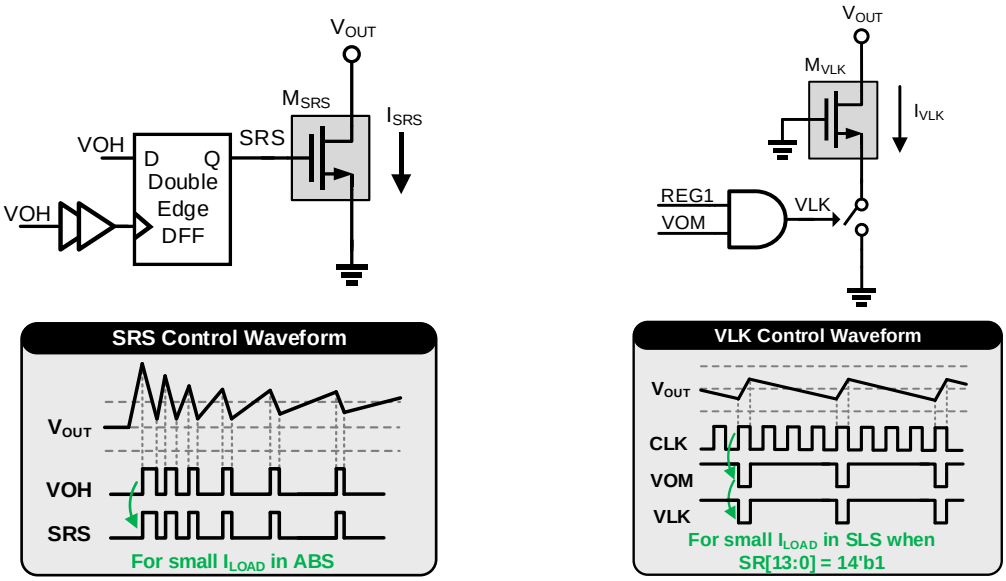


Figure 4-14 Schematic and operating waveform of SRS and VLK control.

During ABS phase, the V_{OUT} settling time is determined by the load current, so if the load current is very small, the settling time is very long. In this design, we add a load transistor, which is controlled by SRS. When V_{OUT} is higher than DZ and *VOH* goes high, the load transistor is turned on to sink the current and speed up the settling time. Other design considerations are needed

when the DLDO output power is extreme low, which is the common case when the load is power gated. There are two issues under this condition. First, the feedback loop will experience instability when the load current is very small. More importantly, due to the leakage current, even when the PMOS array is turned off, the leakage still charges the output decoupling capacitor. Figure 4-14 shows the solution under this circumstance that we add an on-chip load which generates the leakage to compensate the leakage of the PMOS array. This is achieved by adding a leakage-based transistor controlled by a thick oxide switch.

4.3.3 Measurement Results

This DLDO is fabricated in 65nm LP process and the chip micrograph with an area of 0.048mm^2 is shown in Figure 4-15.

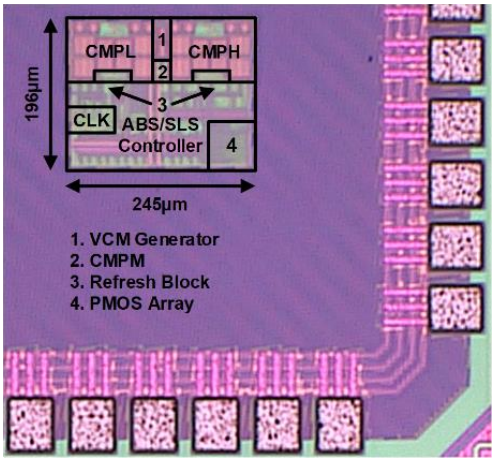


Figure 4-15 Chip micrograph.

Figure 4-16 shows the transient response with a load current step from 710pA to 270µA. We can see that the V_{OUT} go back to the DZ after the first searching for 270µA current step and for the current step changing back to 710pA, the ABS finished all the searching of 14 bits. When working at V_{IN} = 500mV, V_{OUT} = 450mV, F_{CLK} = 464Hz, the DLDO has a total current consumption of 745pA and the current breakdown is shown in Figure 4-17. Due to ultra-low current consumption,

the DLDO still can keep a high current efficiency even under ultra-light load current conditions. The measured peak current efficiency is 99.99% with current efficiency > 90% from 8nA to 0.27mA. The measured voltage droop and load regulation is shown in Figure 4-18. The measured transient waveform in Figure 4-19 clearly shows how the ABS, SLS and SRL-toggling work for a load step change and the measured minimum ripple during steady state is about 2mV.

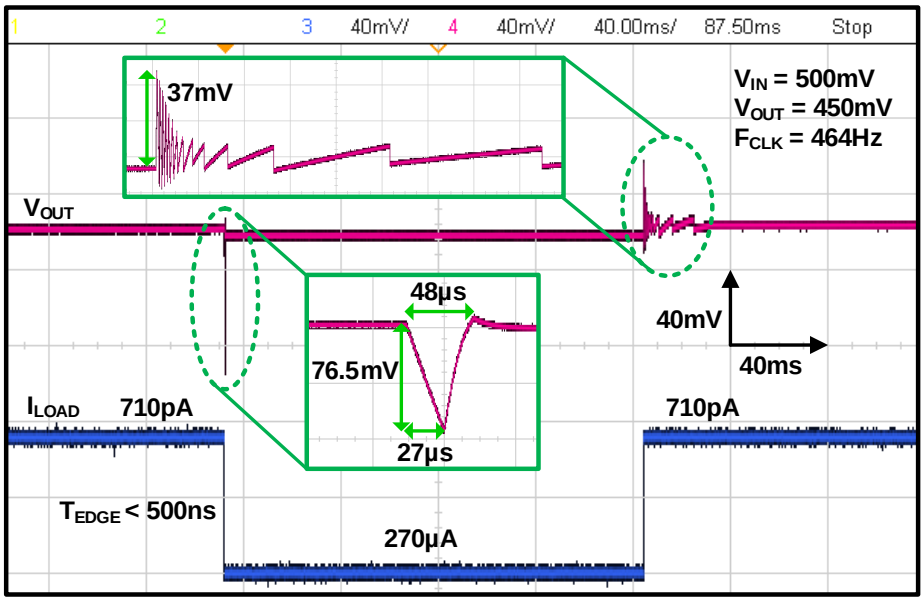


Figure 4-16 Measured transient response of the DLDO

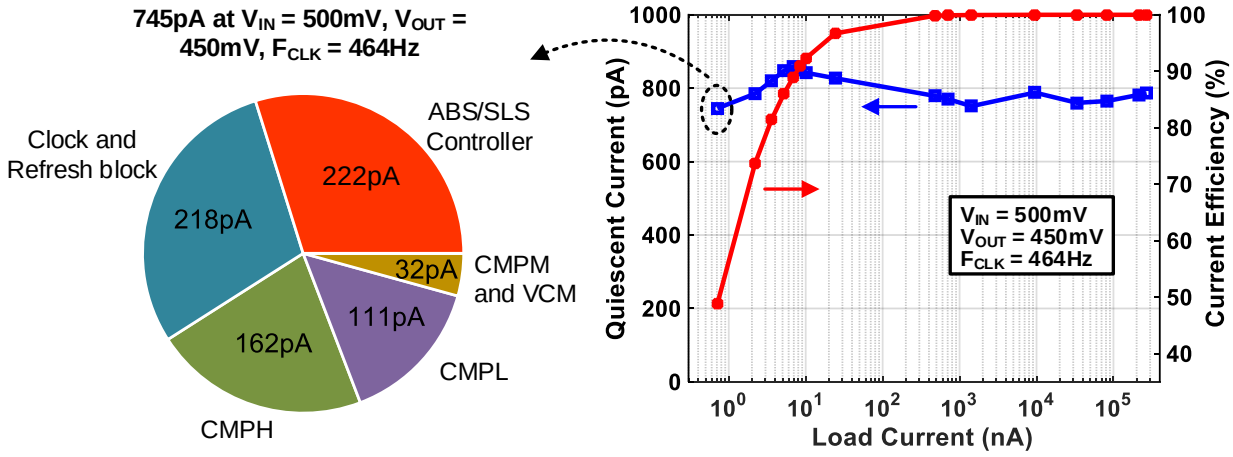


Figure 4-17 Measured quiescent current of the DLDO

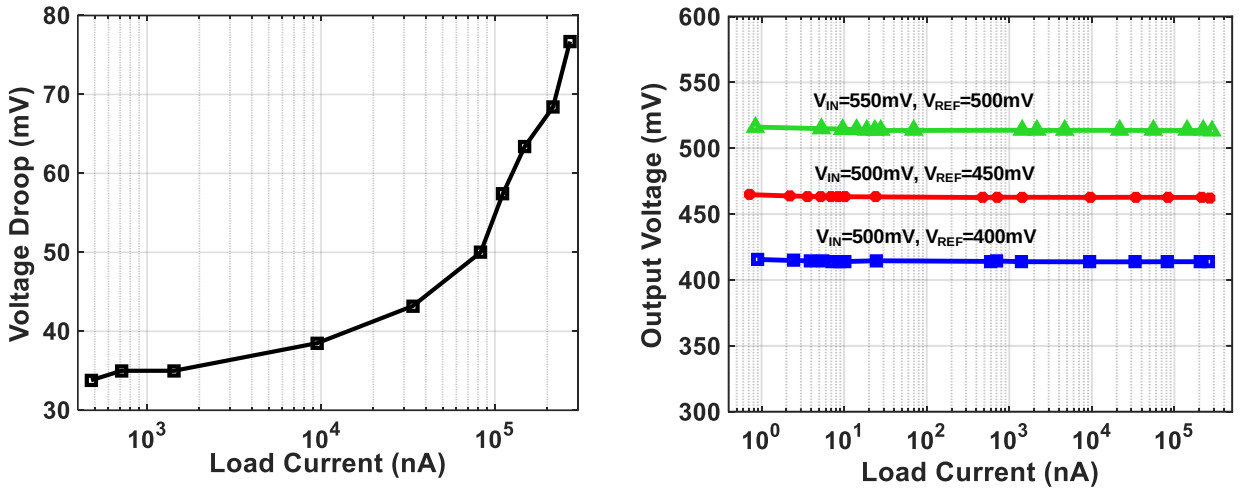


Figure 4-18 Measured voltage droop vs load current and load regulation.

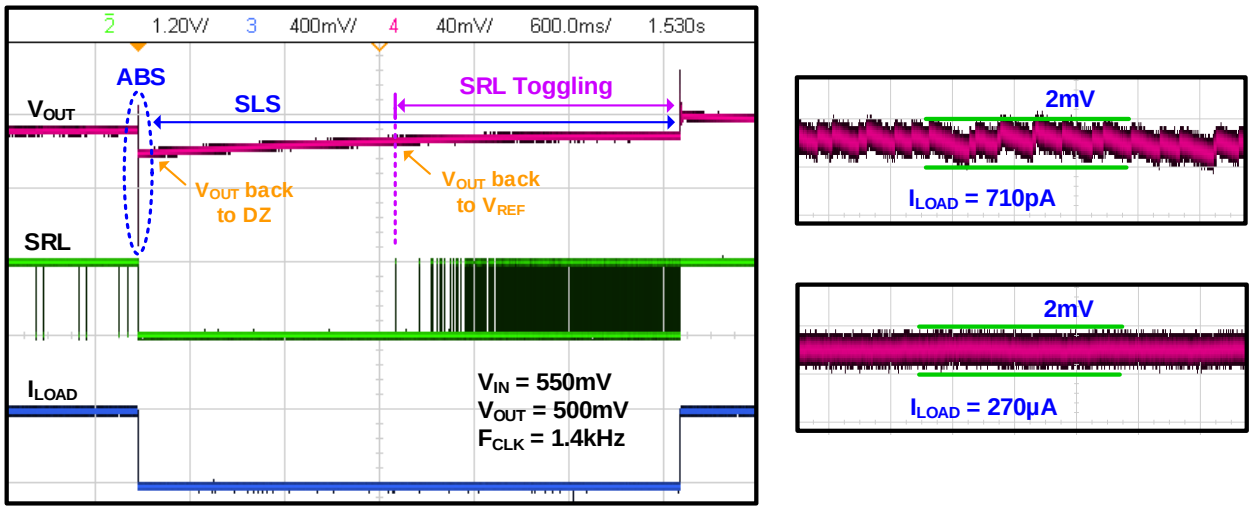


Figure 4-19 Measured ABS-SLS-SRL transient waveform and voltage ripple at the output.

Table 4-1 compares the proposed hybrid ABS/SLS DLDO with other DLDOs, which have not previously approached the pA current consumption range. The hybrid DLDO maintains a high current efficiency (η > 90%) over a load range that is >100× larger than prior-art and consumes >100× less quiescent current, thanks to the proposed hybrid control scheme, highly power-efficient comparators, and 14b PMOS array. Our design achieves the lowest current consumption, the largest dynamic load range, and the lowest load current for DLDOs.

Table 4-1 Comparison of the proposed hybrid control DLDO with state-of-the-art DLDOs.

	[61] ISSCC'17	[53] ISSCC'17	[62] ISSCC'18	[63] ISSCC'18	This work
Process	65nm	65nm	65nm	40nm	**65nm**
Area [mm^2]	0.0023*	0.03*	0.0014*	0.18	**0.048**
Loop control	SAR/PD/PWM	Event-Driven	Hyst. ROSC	NLSC	**Hybrid ABS/SLS**
V_{IN} [V]	0.5 - 1	0.45 - 1	0.5 - 0.9	0.6 - 1.1	**0.5 - 1**
V_{OUT} [V]	0.3 - 0.45	0.4 - 0.95	0.3 - 0.8	0.5 - 1	**0.4 - 0.95**
I_Q [µA]	14	8.1 - 258	48.4	9.2 - 19.6	**0.000745**
Dynamic load range ($I_{LOAD, MAX}/I_{LOAD, MIN}$)	100nA - 2mA (2×10^4)	14µA - 3.36mA (2.4×10^2)	10µA - 3mA (3×10^2)	2µA - 20mA (1×10^4)	**710pA - 0.27mA (3.8×10^5)**
Dynamic load range with η >90%	33.6µA - 2mA (60)	90µA - 3.36mA (37)	10µA - 1.75mA (175)	83µA - 20mA (241)	**8nA - 0.27mA (3.38×10^4)**
Peak current efficiency η [%]	99.8	99.2	99.3	99.95	**99.99**
Output voltage ripple [mV]	20 - 40	N/R	21.7	3 - 6	**2**
Steady-state error [mV]	< 5.2	< 10	< 1.55	N/R	**< 2.7**
ΔV_{OUT}@ ΔI_{LOAD}	40mV @ 1.06mA	34mV @ 1.44mA	20.5mV @ 3.25mA	40mV @ 19mA	**38mV @ 9.5µA 76.5mV @ 0.27mA**
FOM [pF]**	0.47	0.064	0.16	0.19	**0.049**

N/R = Not Reported
* Active area
** FOM = $(I_Q / I_{LOAD}) \cdot (\Delta V_{OUT} / V_{OUT}) \cdot C_{OUT}$

4.4 Sub-nA Fully Integrated Analog LDO

Although DLDOs have the advantage of low voltage operation and their performance can be improved using advanced control algorithms, ALDOs are still popular options to provide a clean voltage supply without any switching ripples. In this work, we design an ALDO with sub-nA quiescent current, which can be fully integrated on chip.

4.4.1 Design Implementation

Figure 4-20 shows the structure of the fully integrated ALDO designed in this work, which adopts a classic analog feedback loop and a NMOS power transistor. To make the ALDO fully integrated on chip and the feedback loop stable, the dominant pole is designed to be at the output

of the error amplifier, V_A, and the NMOS power transistor is used to reduce the output impedance and push the secondary pole far away from the dominant pole. The capacitor bank C_{BW} is used to tune location of the dominant pole, which has a tradeoff between phase margin and loop response speed. The error amplifier, *AMP*, consumes pA current, which also makes the amplifier output impedance very large and helps with the loop stability.

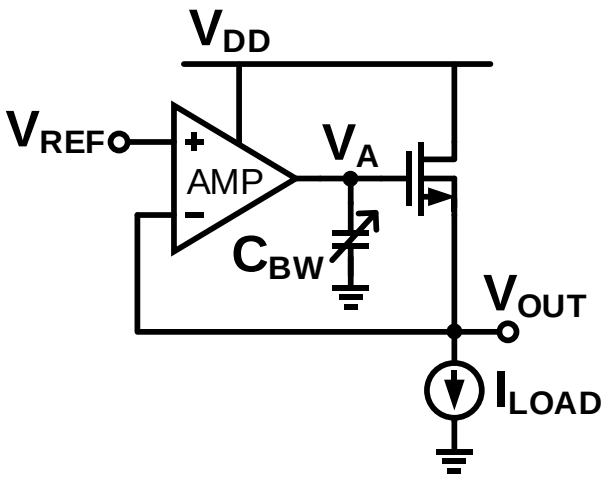


Figure 4-20 Block diagram of the sub-nA fully integrated NMOS ALDO

Figure 4-21 shows the schematic of the error amplifier and its bias circuits. A low-voltage folded cascode structure is adopted for the amplifier, which has the benefit of a wide input voltage range, very high gain and high output impedance. For the bias circuit, the 300pA bias current comes from off-chip during testing and it can be provided by an on-chip current source when integrated in a large system.

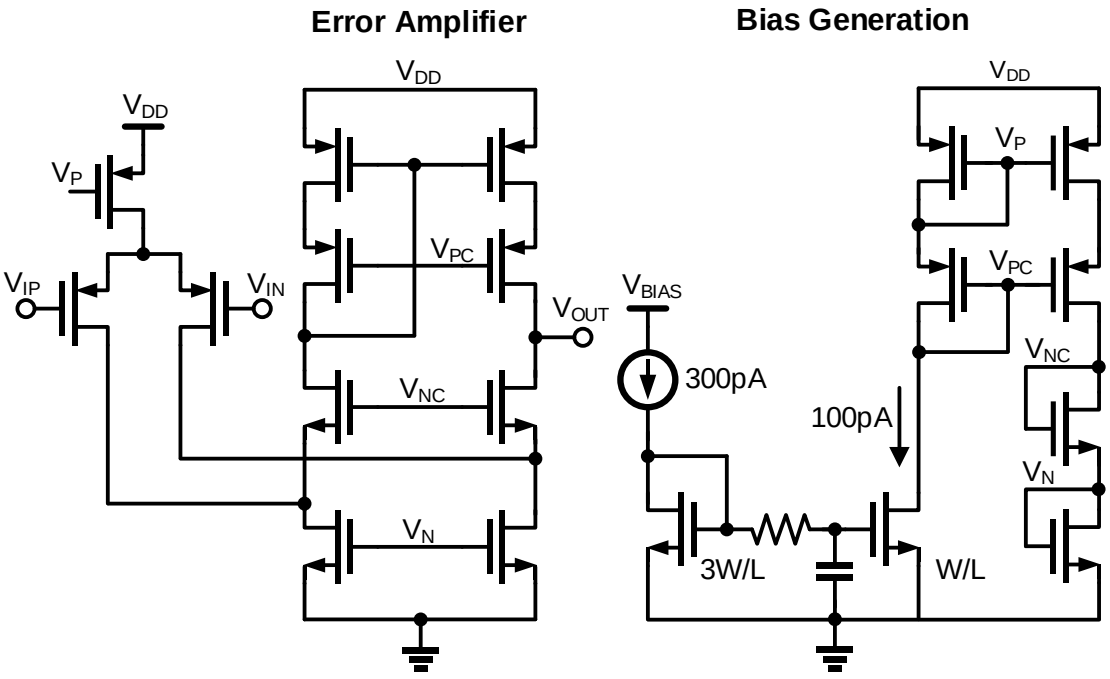


Figure 4-21 Schematic of the error amplifier and its bias circuit.

4.4.2 Measurement Results

The sub-nA ALDO is fabricated in 65nm LP process and the chip has a total area of 0.015mm^2, which is shown in Figure 4-22.

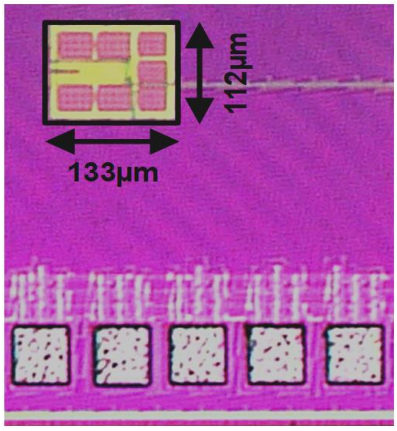


Figure 4-22 ALDO chip micrograph.

Figure 4-23 shows the measured transient step response, which has a droop voltage of 151mV and settling time of 13.6ms for a 10nA to 1µA step input when V_{IN} = 1.5V and V_{OUT} = 0.5V. Figure 4-24 shows the measured load and line regulation. As we can see, load range for the ALDO is from about 4nA up to 500µA. However, the phase margin will decrease for a light load, and the transient droop voltage will increase for a large step input. Figure 4-25 shows the measured quiescent current with a minimum value of 970pA and the voltage droop across load step current.

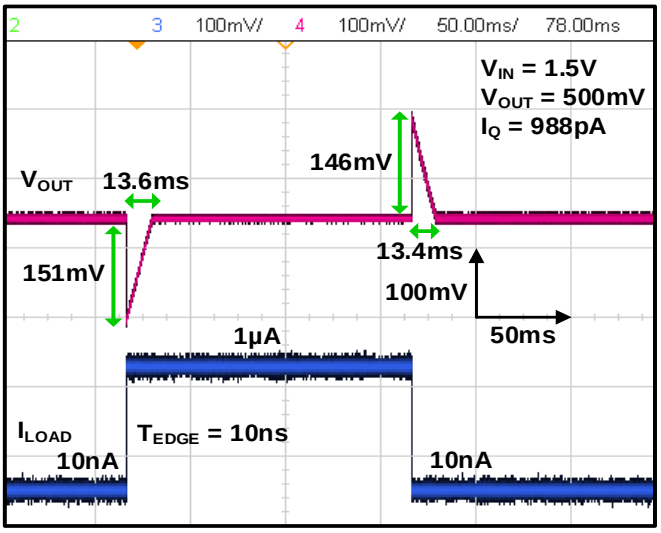


Figure 4-23 Measured load transient response of the ALDO

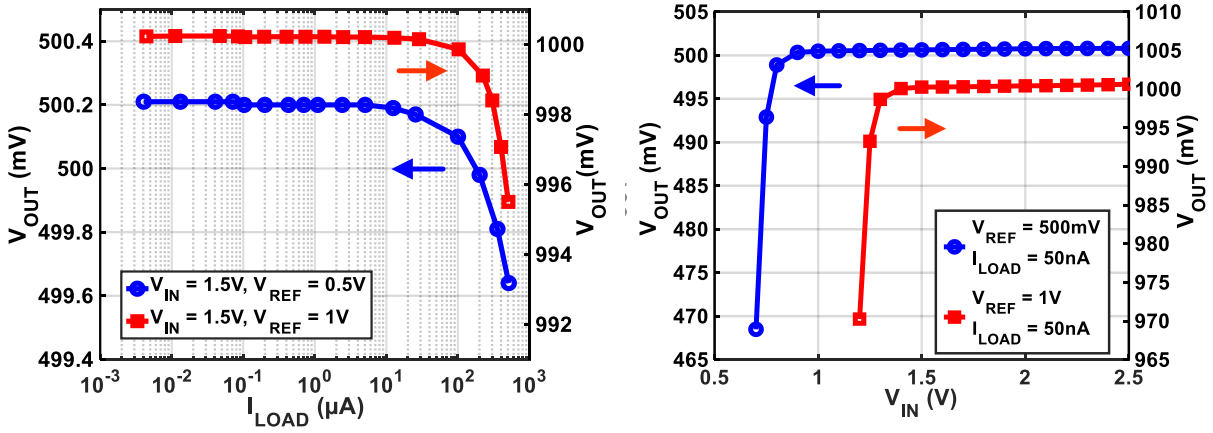


Figure 4-24 Measured load and line regulation of the ALDO.

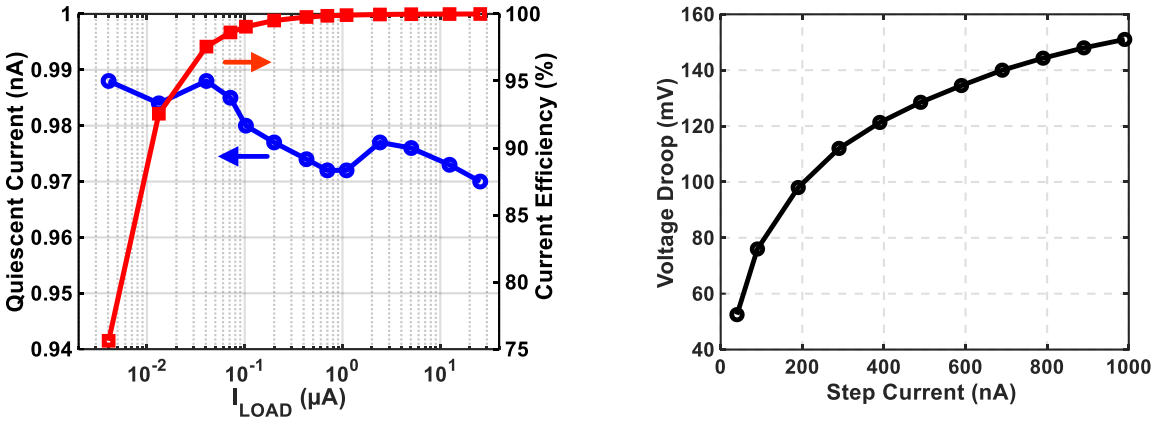


Figure 4-25 Measured quiescent current and voltage droop.

4.4.3 Comparison with Sub-nA DLDO

The performance summary of the ALDO and DLDO is shown in Table 4-2. The two LDOs both consume sub-nA quiescent current. Although the load range of the two LDOs are similar, the DLDO has 2× lower droop voltage for a 270× larger step input, and it also has 283× faster settling time and 6× lower dropout voltage. However, the input voltage of the ALDO can go up to 2.5V due to using 2.5V IO devices. There is no switching ripple for the ALDO, but there is output noise, which is less than 2mV. The output noise can be further reduced if larger decoupling capacitors are used in this work. Also, the ALDO can be fully integrated using on-chip decoupling capacitors.

The performance comparison shows that the DLDO has advantages over ALDO in many aspects, such as faster settling time, low dropout voltage, and lower input voltage, due to the benefits of low-voltage operation of digital circuits, flexible control algorithms and better power and performance scalability. But the ALDO has no switching ripple and output noise can be minimized by using large output capacitors, which makes it suitable for powering noise sensitive circuits such as RF transceivers.

Table 4-2 Performance summary and comparison of the sub-nA ALDO and DLDO

	I_Q	Load Range	ΔV_{OUT} @ ΔI_{LOAD}	Settling Time	V_{IN}	Dropout Voltage	Output Ripple/Noise	C_{OUT}
ALDO	970pA	4nA - 0.5mA	151mV @ 1µA	13.6ms	0.7-2.5V	300mV	< 2mV Noise	510pF
DLDO	745pA	710pA - 0.27mA	76.5mV @ 0.27mA	48µs	0.5-1V	50mV	2mV Ripple	100nF

4.5 Conclusions

This research explores sub-nW low dropout regulator (LDOs) design for nW IoT devices, which includes two designs, a DLDO and an ALDO. The DLDO uses a hybrid control scheme, ABS and SLS to achieve a better tradeoff between power and performance while still keeping an ultra-low quiescent power consumption. Measurement results shows the DLDO achieves the lowest 745pA quiescent current with a widest 3.8×10^5 dynamic load range. It also supports a fast load transient response through the asynchronous path thanks to the asynchronous comparator. As a comparison, a traditional fully integrated sub-nA ALDO using an analog feedback loop and NMOS power transistor is also presented, which also achieves sub-nW power consumption and is well suited for powering analog and RF blocks in fully integrated nW IoT systems. Finally, the comparison of DLDO and ALDO are analyzed.

Chapter 5

5. Sub-nW Bandgap Voltage Reference

5.1 Voltage Reference for Ultra-Low-Power IoT Systems

Voltage reference is a precision circuit that provides accurate voltage value for many basic circuit blocks, such as DC-DC converters, analog font-ends, and RF transceivers. Figure 5-1 shows an application scenario, where the output of a voltage reference is connected with an LDO. The LDO forces its output voltage to be the same as the reference voltage through a feedback loop, which means the quality of the load voltage supply is also determined by the reference voltage, V_{REF}. For analog and RF circuits, their performance is very sensitive to the voltage supply variation, so the first requirement for designing a voltage reference is to be robust against process, voltage, and temperature (PVT) variation to provide stable voltage supplies to the loads.

For today's self-powered or ultra-low-power (ULP) IoT systems, their available power is very low due to constrained size of batteries or energy harvesters under various environmental conditions. As a basic building block, voltage reference design is also limited by its power consumption, which means the power should be down to nW level for many applications. So, the second requirement for designing voltage references in ULP IoT systems is ultra-low power consumption. For energy harvesting systems, to achieve a low cold start-up voltage, voltage references should bring up and settle down first before energy harvesting interfaces and voltage

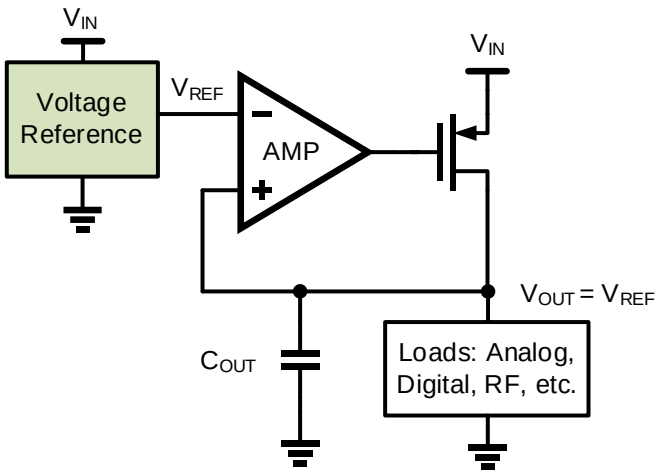


Figure 5-1 Voltage reference connecting with an LDO to generate voltage supply.

regulators start to work. To achieve low system start-up voltage, it requires voltage references to have a very low input operating voltage. However, in a situation where voltage references are powered by an energy storage node, which is either a supercapacitor or rechargeable battery, voltage references should also be able to operate at the highest voltage of the system. So, another challenge for voltage references, which is also the third design requirement, is to have a large input voltage range from around cold start-up voltage up to the system highest supply voltage.

Voltage references can be classified by the quantities used to generate the temperature independent voltage. Generally, a temperature independent voltage is generated by adding two quantities with opposite temperature coefficients (TCs), which associates with either threshold voltage (V_{TH}) in MOS transistors or base-emitter voltage of a bipolar junction transistor (BTJ). So, there are basically two types of voltage references, CMOS-based references [64] [65] or BJT-based references [66] [67], which is also called bandgap reference. In modern CMOS process, V_{TH} value is very small, so the CMOS-based structure can be used under ultra-low voltage supply. Also, due to most of the CMOS-based references working at subthreshold (sub-V_{TH}) region, MOSFETs are biased with ultra-low current, so the CMOS-based structures have the advantages of achieving ultra-low power consumption, which are down to nW or even pW, and ultra-low voltage, which

can be around 0.5V. [68] [69] However, V_{TH} has a large variation with the process, especially for sub-V_{TH} MOSFET, so the CMOS structures does not have a good consistency across multiple chips. BJT has the advantage of providing the most reproducible quantities associated with temperature, so the performance for PVT variation using BJT-based structure has a much better consistency, which makes it widely used for the situations where highly accurate voltage reference are required. However, the BJT diode usually needs a large turn on voltage, so the BJT-based reference usually needs a higher voltage, which is larger than around 0.7V. [70]-[72]

5.1.1 Overview of Bandgap Voltage Reference

Bandgap references (BGRs) uses BJT to generate the reference voltage, which is associated with bandgap voltage of silicon. To achieve a temperature independent voltage in BGR, two quantities with opposite temperature coefficients (TCs), need to be added together, so they can compensate with each other. In an *npn* bipolar transistor, the base-emitter voltage, V_{BE}, exhibits a negative TC, which can be written as [73]

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)V_T - E_g/q}{T} \tag{5.1}$$

where $V_T = kT/q$ is the thermal voltage, k is the Boltzmann's constant, q is electron charge, $m \approx -3/2$ is the temperature exponent of mobility, and $E_g \approx 1.12\ eV$ is the bandgap energy of silicon. With V_{BE} equals to 750mV and $T = 300K$, the negative TC of V_{BE} is around $-1.5\,mV/K$. So, V_{BE} is used as complementary-to-absolute-temperature (CTAT) voltage.

The positive TC can be obtained from the voltage difference of the two base-emitter voltages if two BJTs operates at two different current densities, which generates a proportional-to-absolute-temperature (PTAT) voltage, as shown in Figure 5-2.

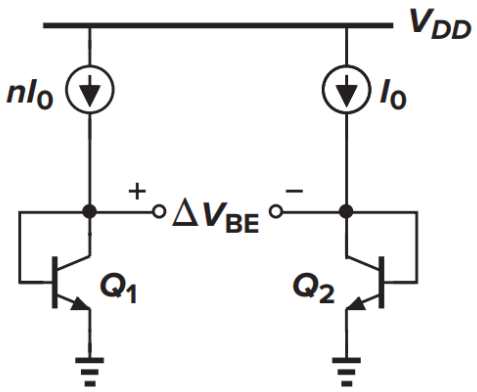


Figure 5-2 Generation of PTAT voltage, ΔV_{BE}. [73]

The calculated ΔV_{BE} and positive TC of ΔV_{BE} is

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = V_T \ln n \tag{5.2}$$

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} \ln n \tag{5.3}$$

where n is the ratio of the bias current for two BJTs, *Q1* and *Q2*. In this example, the two BJTs have the same size, but are biased at different current. Another way to achieve ΔV_{BE} is changing the number of paralleled BJTs while keeping the same bias current. To develop a voltage reference with zero temperature coefficient, we need to add the positive TC and negative TC together. One of the possible implementations of bandgap reference is shown in Figure 5-3 and the voltage at the output of the amplifier A_1 can be set as temperature independent at room temperature if $(1 + R2/R3) \times \ln n$ is equals to about 17.2 [73] and in the case, the reference voltage is equal to

$$V_{OUT} = V_{BE2} + (1 + \frac{R_2}{R_3})(V_T \ln n) \tag{5.4}$$

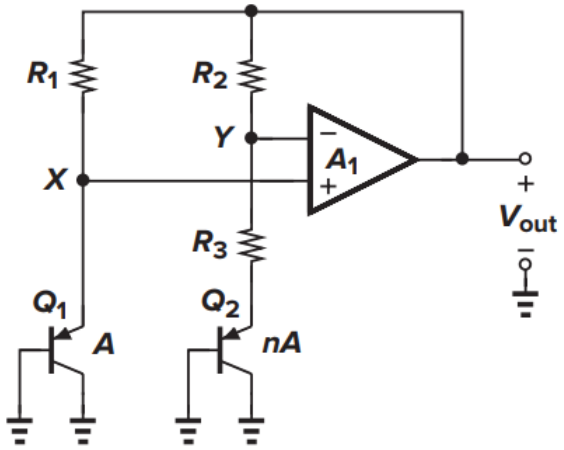


Figure 5-3 A simplified structure of a traditional bandgap voltage reference. [73]

The voltage generated based on (5.4) is called a “bandgap reference” because the voltage has a nominally-zero TC, which only depends on a few parameters including the bandgap voltage of silicon, the temperature exponent of mobility, and the thermal voltage.

5.1.2 Prior Art nW BGR

As we already know, among all the types of voltage references, bandgap topology is regarded as the most reliable choice, which is robust against PVT variations. However, unlike other structures, such as the sub-V_T CMOS topology which can consume only a few pW, the bandgap is normally consume tens of nW or even μW power due to large bias current of bipolar transistors and complex circuit structures. Also, the minimum voltage supply of BGRs is usually limited by the turn-on voltage of the diode, which is around 0.6-0.8V, so traditional BGRs are not able to work under 0.6V voltage supply.

Recently, multiple design techniques have been investigated to reduce the power consumption and supply voltage of BGR. [74]-[76], which include co-designing with switched-capacitor voltage regulators to reduce the input voltage [77]-[79] and using duty-cycled control techniques to reduce

the power consumption [70] [76]. The schematic of a switched-capacitor bandgap reference [77] is shown in Figure 5-4. Two 2× charge pump voltage-doublers are used at the input to reduce the minimum input voltage. An output switched-capacitor (SC) network is used to generate the reference voltage by adding V_{EB1} and ΔV_{EB} together.

$$V_{REF} = V_{EB1} C_1 / (C_1 + C_2) + 3\Delta V_{EB} \tag{5.5}$$

where C_1 and C_2 are the capacitor of the voltage divider in the output switched-capacitor network. This design achieves a minimum 0.5V input voltage supply with minimum 32nW power consumption. However, this structure has many drawbacks. First, 32nW power consumption is too high for many nW or pW systems. Second, due to the usage of 2× charge pump cell, the highest voltage is limited to half of the system voltage supply. Third, the biased current is generated by the input charge pump, so the resistance is related to V_{IN} and clock frequency, which makes V_{REF} very sensitive to V_{IN} and clock frequency variation.

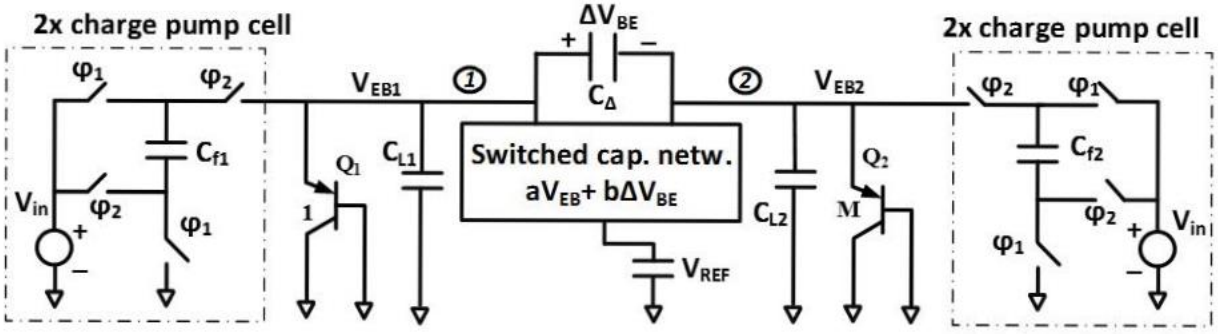


Figure 5-4 Block diagram of a switched-capacitor bandgap reference. [77]

Another nW BGR [76] uses a traditional bandgap structure with duty-cycling control and thus achieves an average power consumption of 2.98nW under 0.003% duty cycle. However, the minimum voltage supply is higher than 1.2V, which is not suitable for many ultra-low-voltage (ULV) systems and due to the low duty cycle, the generated V_{REF} is very sensitive to the transistor

leakage, so extra circuits are needed to reduce the leakage, which increases the design complexity.

5.1.3 Motivations for Sub-nW Bandgap Voltage Reference

One of the important applications for voltage references is to provide accurate values for voltage regulators to generate voltage supplies. For this application, the BGR requirements depend on the load components. Table 5-1 shows the operating voltage and minimum power consumption of pW digital processors in ULP IoT systems. As we can see, the minimum power of those components is all in the sub-nW range and minimum operating voltage is down to 0.3V or even lower. This requires power consumption of voltage references to be sub-nW, which is at the same level compared with those loads, and provide very low reference values to generate the voltage supplies.

Table 5-1 Operating voltage and minimum power of pW digital processors

	Operating Voltage (V)	**Minimum Power (pW)**
[80] SSCL'19	0.3 – 0.9	840 @ 0.3V, 6Hz
[81] ISSCC'18	0.2 – 1.1	595 @ 0.45V, 2Hz
[82] ISSCC'15	0.16 – 1.15	127.1 @ 0.55V, 2Hz

The design challenges and requirements for designing sub-nW BGR include:

- First, the traditional BGR with a high input voltage supply is not compatible for many of the ULV or energy-harvesting IoT systems, which needs a low cold start-up voltage. Therefore, how to achieve a low input voltage supply range, which is down to 0.5V or even lower with a wide input voltage range up to the system voltage supply, is very critical.

- Second, power consumption of traditional bandgap references is at least tens of nW, which is too high for the emerging nW IoT systems. So how to reduce the power consumption of the bandgap reference to sub-nW range is another challenge.
- Finally, as a classic tradeoff between power and performance, how to generate highly accurate and stable voltage references against PVT variation using only sub-nW power is also very challenging.

5.2 Sub-nW Bandgap Reference Design Techniques

To address those challenges and achieve sub-nW power consumption together with a wide input voltage range, several techniques have been used in this work. First, rather than using nA current to bias BJTs, in this work, we bias the BJT with only pA current. Second, a configurable input charge pump is used to increase the input voltage range. Finally, output switched-capacitor network is used to generate the temperature independent voltage around 300mV.

5.2.1 BJT Characterization with pA Bias Current

Bias current, which is used for BJTs to generate V_{EB} and ΔV_{EB}, usually dominates the total power consumption of the BGR. For example, the power of bandgap core in [77] counts for 62% of the total BGR power consumption. Previous work generally biases BJTs with a few to tens of nW. Reducing the bias current could potentially increase the PVT variation and deteriorate the accuracy. Recent hybrid CMOS and BJT voltage references [83] [84] have already explored using pA to bias BJT. However, none of the previous work fully characterizes BJT with pA current and there is no BGR design using such low bias current value. In this research, we directly reduce the bias current of the bipolar transistor down to pA. So, first of all, we are going to explore the design space of pA BJT to see how sensitivity V_{EB} and ΔV_{EB} are under pA current.

In this characterization, we use 65nm LP process for the spice-level simulations and keep the same bias current for the two BJTs, Q_1 and Q_2. Figure 5-5 shows the schematic for BJT characterization and the number of paralleled transistors for Q_2 and Q_1 is 48 and 1, which is used to generate the ΔV_{EB}.

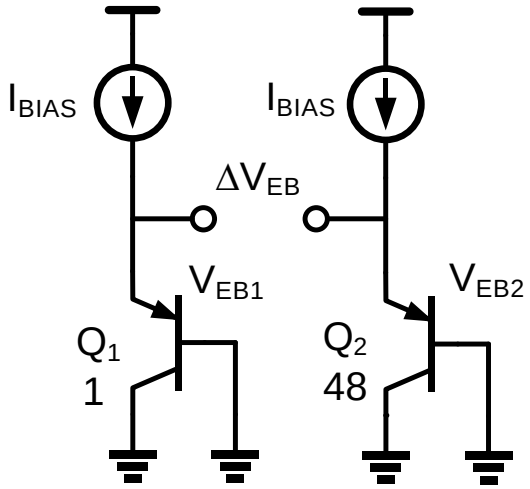


Figure 5-5 Schematic for BJT characterization under pA current.

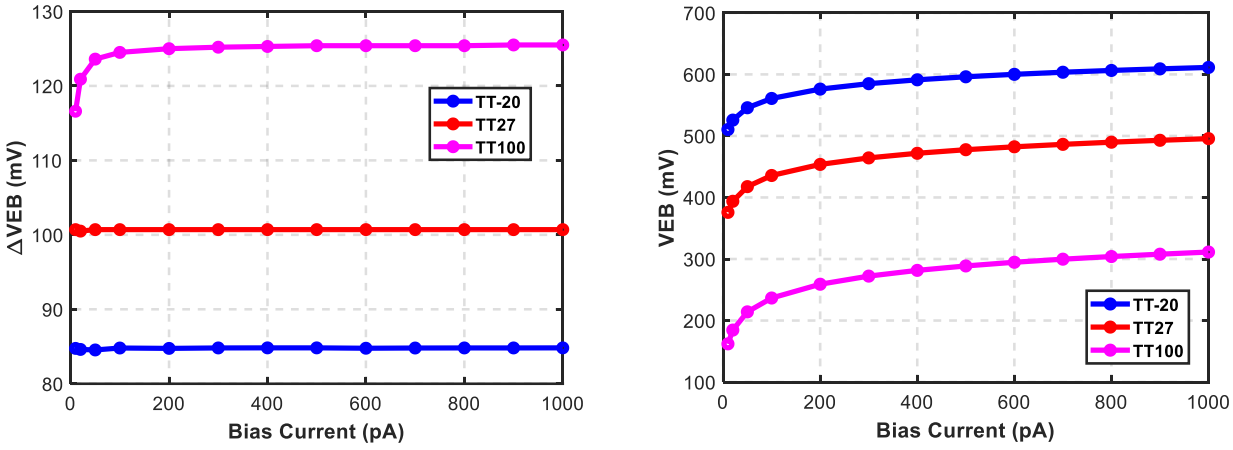


Figure 5-6 Simulated ΔV_{EB} and V_{EB} variation over pA bias current.

Figure 5-6 shows the simulation results of ΔV_{EB} and V_{EB1} across bias current in the pA range. As we can see, ΔV_{EB} keeps almost a constant value for the bias current higher than around 100pA. When the bias current reduces to tens of pA, ΔV_{EB} is very sensitive to the bias current especially at 100°C. The simulated V_{EB1} has the same trend of current sensitivity. When bias current reduces, V_{EB1} reduces exponentially and when bias current reaches to tens of pA, V_{EB1} becomes very sensitive to the bias current.

Figure 5-7 shows 1σ process variation for V_{EB} under pA bias current using a 500-point Monte Carlo simulation for each data point. As bias current reduces, the 1σ variation also increase exponentially and at around 200pA current, the 1σ variation is less than 1.75mV. The simulated V_{EB1} and ΔV_{EB} with a temperature range from -20°C to 100°C is shown in Figure 5-8. In the simulation, the bias current is set to be around 170pA. As we can see, V_{EB1} has a negative TC of -2.65mV/°C and ΔV_{EB} has a positive TC of 345μV/°C. Through the characterization, we can see that BJT is sensitive to the process and bias current variation when bias current reduces to tens of pA, but still keeps a reasonable performance when the bias current is around several hundred pA.

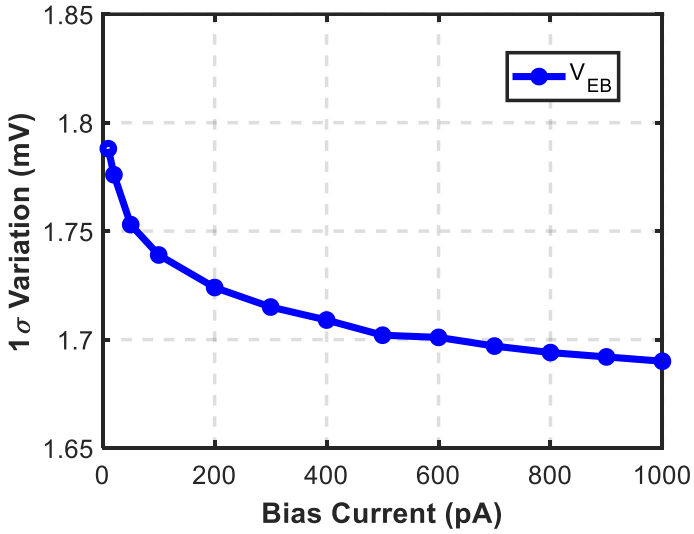


Figure 5-7 Simulated 1σ process variation of V_{EB}.

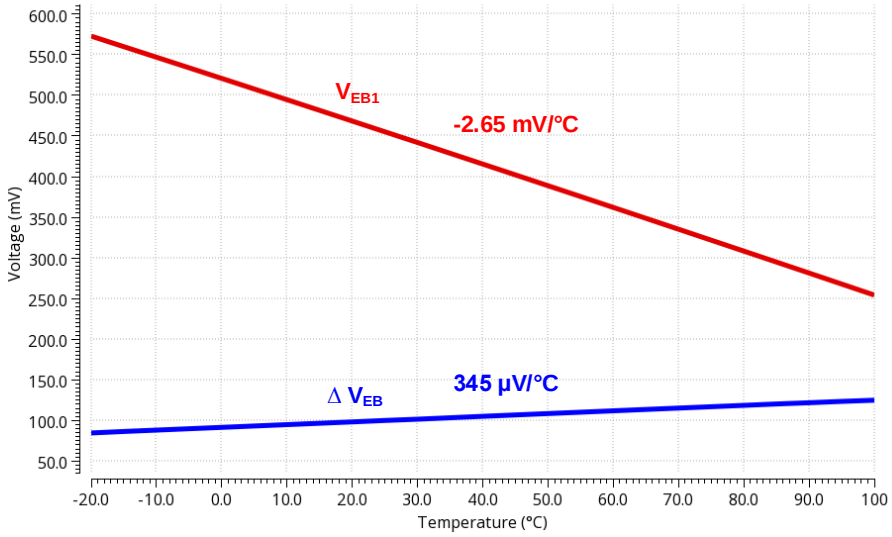


Figure 5-8 Simulated V_{EB1} and ΔV_{EB} versus temperature

5.2.2 Wide Input Voltage Range with Configurable Charge Pump

To reduce the minimum input voltage, a voltage doubler or tripler can be used at the input to boost the voltage up, but it also limits the maximum voltage to half or one third of the system voltage supply (V_{DD}). To address this challenge, an input charge pump with configurable gain is used to expand the voltage range from 0.45V up to 3.3V system V_{DD} in this design. The operation diagram of the charge pump is shown in Figure 5-9, which can be configured with three gain settings, 2×, 1×, and 1/2×. When the input voltage is between 0.45V to 1V, the charge pump is set with a gain of 2, so the output can be boost to higher than 0.8V to power the bandgap core and BJTs. When the input voltage is between 1V and 1.75V, the gain reduces to 1 and finally 1/2 for 1.75V to 3.3V. Another benefit of this configurable charge pump is that the charge pump output, V_{OUT}, achieves a smaller range than V_{IN}, which helps with the reference line sensitivity with a large V_{IN} range.

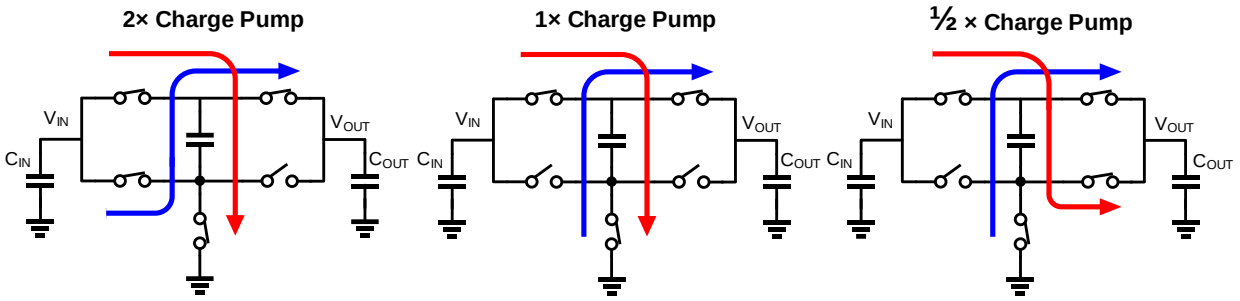


Figure 5-9 Input charge pump with configurable gain.

To achieve a wide input voltage range, the configurable charge pump needs be used together with a voltage monitor and configurable voltage boosters to drive the switches, which is shown in Figure 5-10. The input voltage is detected and quantized by the voltage monitor to three sections represented by a two-bit control signal, *VM*, which controls both of the voltage boosting gain of the booster and the input charge pump configuration.

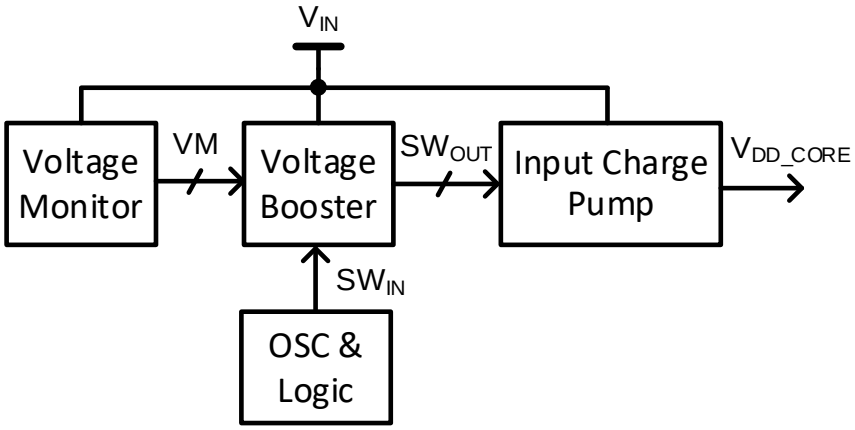


Figure 5-10 Generation of control signals for the input charge pump.

5.3 A Sub-nW Bandgap Reference with Wide Input Voltage Range

Using the design techniques characterized and introduced in Section 5.2, a sub-nW BGR with wide input voltage range for nW IoT systems is proposed in this research. The block diagram of

the sub-nW BGR is shown in Figure 5-11, which includes an input charge pump, a bandgap core, an output switched-capacitor network, a bias generation block, a voltage monitor, a clock generation block, and switch drivers. This proposed BGR is fully self-contained with integrated oscillator and bias generator, so it does not need any off-chip components.

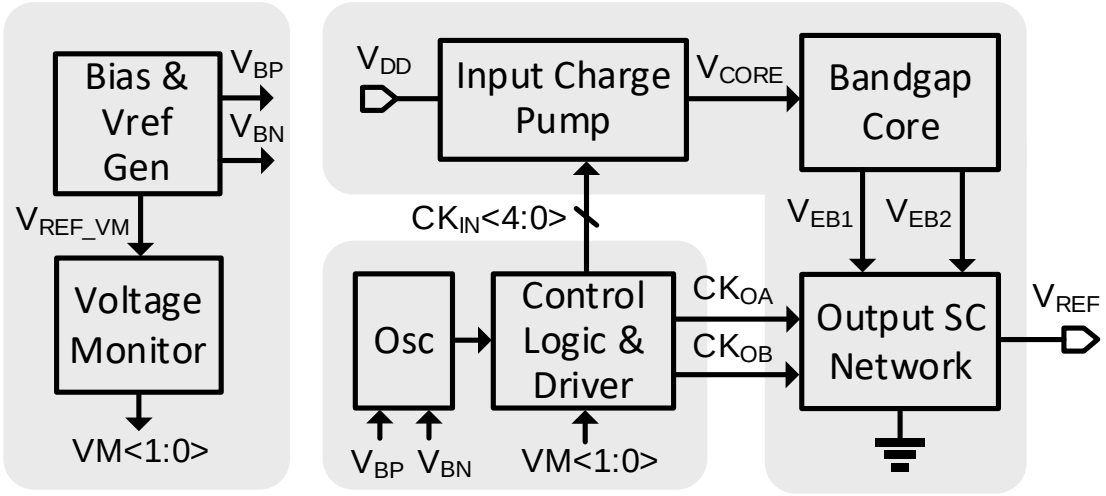


Figure 5-11 Block diagram of the proposed sub-nW BGR.

5.3.1 Design Implementation

The schematic of the bandgap core is shown in Figure 5-12, which includes a bias current generator with its start-up circuit and two V_{EB} generation branches. Several parameters need to be considered during design. First of all, the voltage supply of the bandgap core, V_{CORE}, is provided by the input charge pump, so the minimum V_{CORE} should be smaller than the minimum voltage generated by the input charge pump. In this design, minimum V_{CORE} equals to V_{EB} plus the minimum source-drain voltage of the current mirror, which is about 700mV. Second, the size the current mirrors should be enough large to reduce the mismatch effect on the voltage reference. Finally, the bias current generator uses a constant-G_m structure, so the bias current does not change too much across the voltage supply, which reduces the line sensitivity.

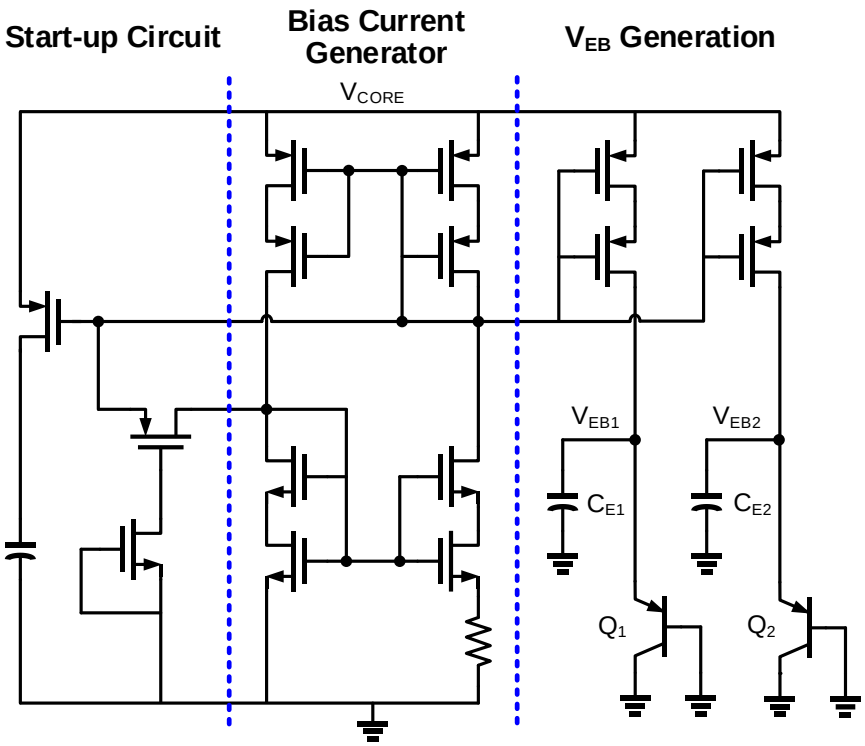


Figure 5-12 Schematic of the bandgap core with bias generation.

Due to the large input voltage range, all the MOS transistors in the design use 3.3V IO devices including the switches in the input and output switched-capacitor block. For low input voltage, the control voltage needs to be boosted to fully turn on those switches and at high input voltage, the voltage boost should be disabled to keep the gate voltage in the safe range. To achieve this function, a voltage booster with configurable gain is designed in this work, as shown in Figure 5-13, which generates boosted control signals for input charge pump and output SC network. This structure is based on the traditional 2× voltage booster [85]. By adding control logics to turn on and off the boosting capacitors and switches from the voltage supply, the configurable voltage booster has a boosting gain of 1×, 2× or 3× based on the control signal VM<1:0>, which comes from the voltage monitor block.

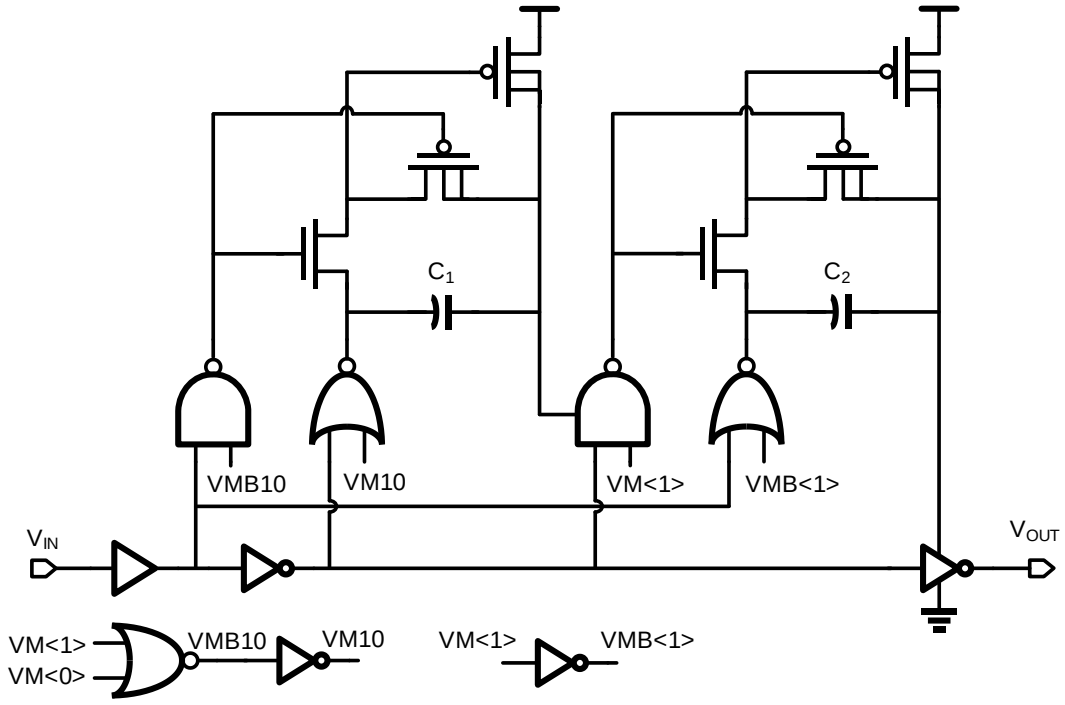


Figure 5-13 Schematic of the voltage booster with configurable gain.

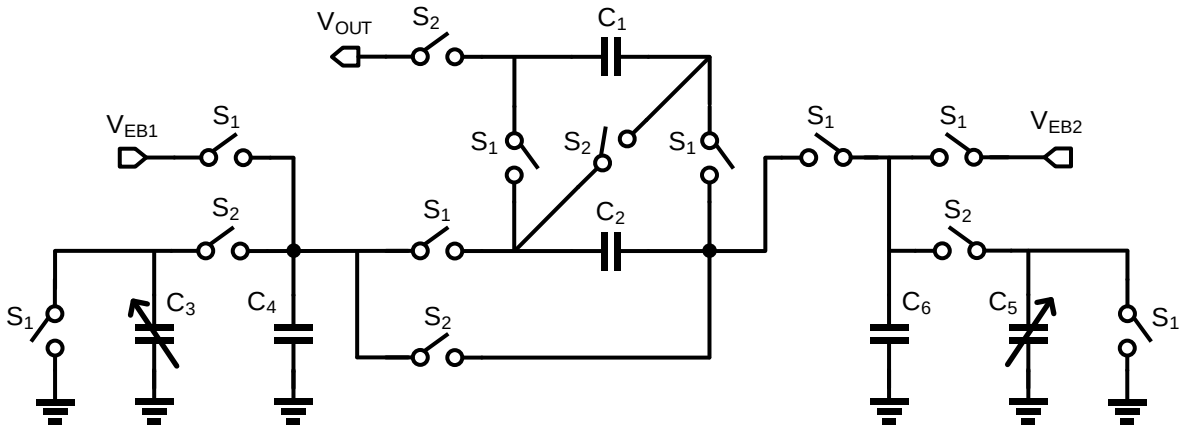


Figure 5-14 Schematic of the output SC network.

The schematic of the output SC network is shown in Figure 5-4. There are several design considerations on this block. First, since the capacitors, especially, C_3 and C_4, act as the load for the BJT V_{EB1}, so the load effect should be optimized as small as possible to reduce the load effect. Second, the bottom parasitic capacitance of those capacitors should also be minimized to increase

the accuracy of the output SC network, so the metal-insulator-metal (MIM) capacitors are used in this design. Third, a dummy load is added to V_{EB2} to compensate the load effect from V_{EB1}. Finally, the switch size is optimized to reduce the charge from MOSFET channel. The output voltage of the SC network, which is the BGR reference voltage is shown below.

$$V_{REF} = V_{EB1}\frac{C_1}{C_2} + 2\Delta V_{EB} \tag{5.6}$$

For the clock generation, a relaxation oscillator has been used in this work instead of ring oscillator to achieve a good stability because the accuracy of the output reference voltage is also related to the clock frequency. A constant-Gm current generator is used to provide the bias current for the relaxation oscillator in this design.

5.3.2 Simulation Results

The sub-nW BGR is designed using 65nm LP process and Cadence Virtuoso and Spectre are used for the spice-level simulations. Figure 5-15 shows the simulated transient start-up waveforms for the BGR across temperature and process corners. The start-up time at TT27 is around 10s due to the slow frequency clock used for the output SC network, which is around 20Hz. The slow clock helps reduce the load effect for BJTs to keep a high accuracy for reference voltage. Figure 5-15 also shows the steady-state waveform, in which the simulated output ripple is about 70μV.

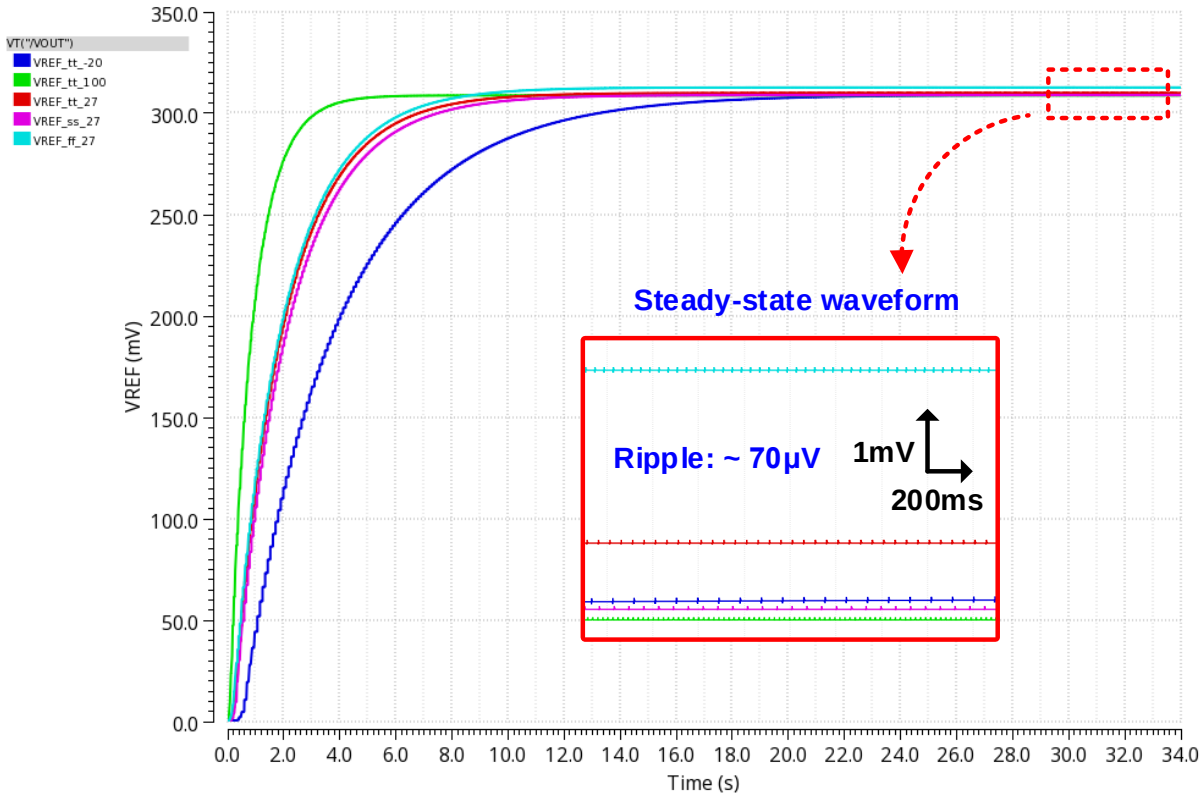


Figure 5-15 Simulated transient start-up waveforms of the BGR.

The simulated V_{REF} across temperature under different input voltages is shown in Figure 5-16. The V_{REF} variation at 0.45V with temperature range from -20°C to 100°C is 1.9mV and the V_{REF} value is 310mV, so the temperature variation of the sub-nW BGR is 51ppm/°C. The temperature variation performance keeps consistent under 1.2V and 3.3V input voltages. Figure 5-17 shows the voltage supply sensitivity. As we can see, the V_{REF} variation is 2mV for the input voltage range from 0.45V to 3.3V, so the line sensitivity is 0.23%/V. The V_{REF} drops at about 1V and 1.75V, which is due to the output control-bit change of the voltage monitor. The voltage monitor output adaptively changes the input charge pump gain and the oscillator frequency, which also helps reduce the voltage supply variation.

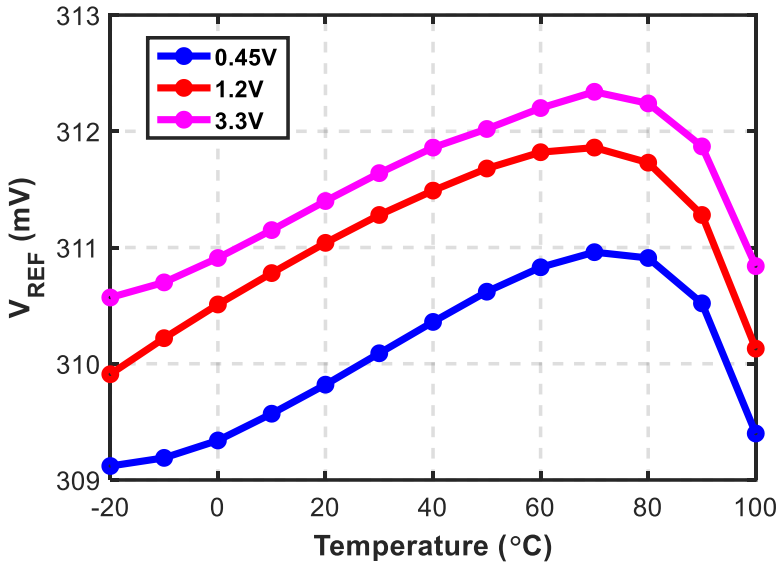


Figure 5-16 Simulated BGR voltage across temperature and V_{IN}.

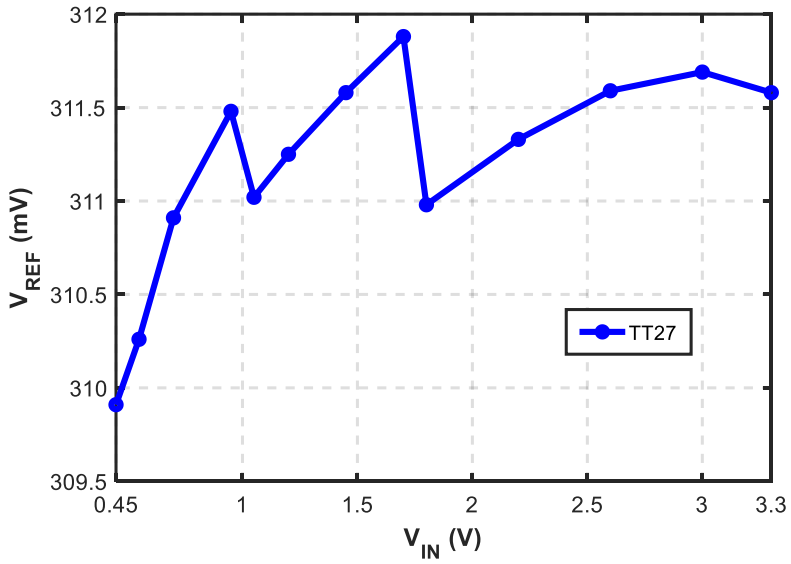


Figure 5-17 Simulated voltage supply sensitivity.

The power consumption over input voltage is shown in Figure 5-18. Under 0.45V, TT27 and 450Hz clock frequency, the BGR has a minimum power consumption of 930pW. This minimum power can be reduced further if the clock frequency is reduced, which increases the settling time

during BGR start-up. The power consumption is 2.7nW at 1.5V, which is 120× lower than the design in [77] and the power is still only 13.3nW even if the voltage supply is up to 3.3V.

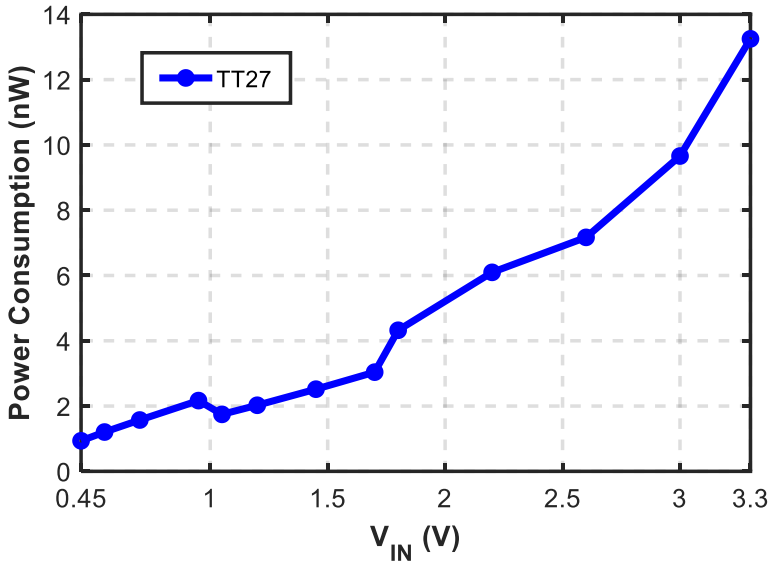


Figure 5-18 Simulated power consumption across V_{IN}.

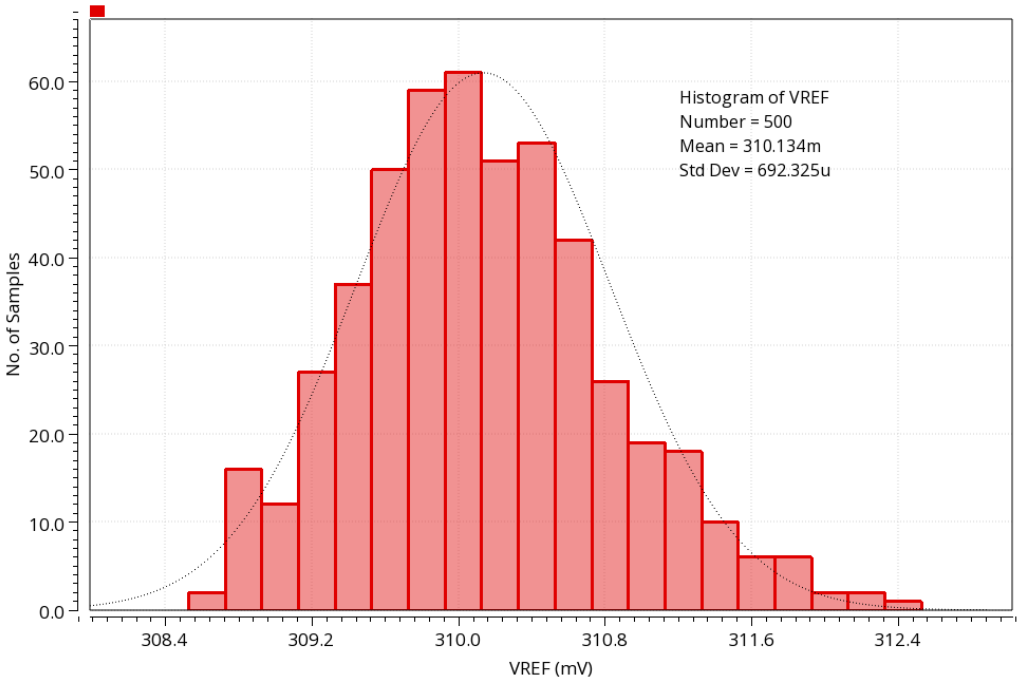


Figure 5-19 Monte Carlo simulation at 0.45V and 27°C for process variation.

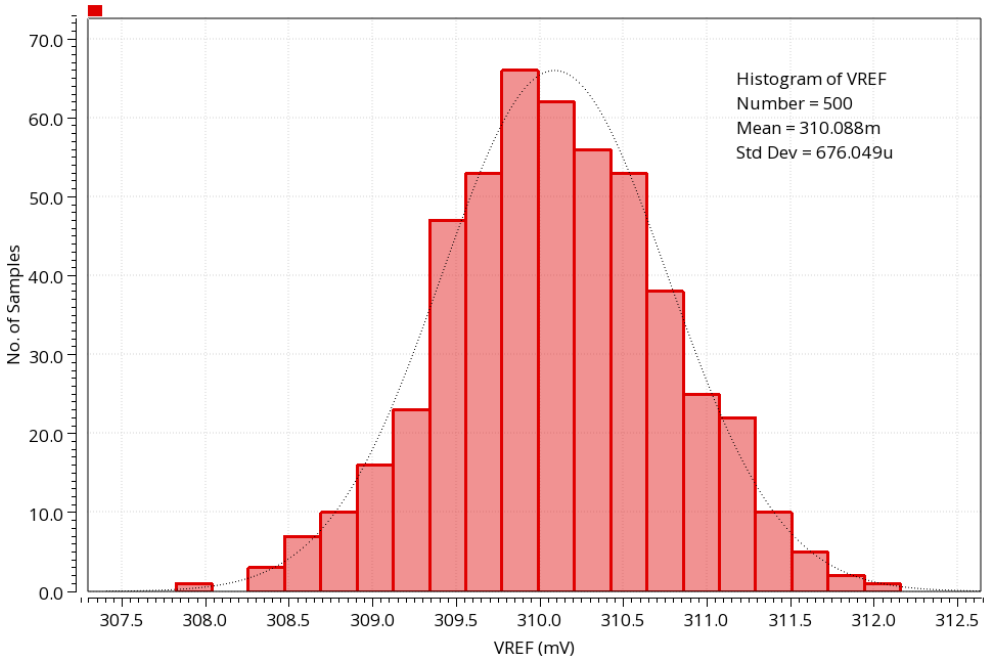


Figure 5-20 Monte Carlo simulation at 0.45V and TT27 for local mismatch.

Table 5-2 Simulated power consumption under different temperatures and process corners

	TT27	TT-20	TT100	SS27	FF27
Power Consumption (nW) @ 0.45V	0.93	0.68	2.3	0.74	1.14

The V_{REF} process variation under 0.45V and 27°C is simulated by 500-point Monte Carlo shown in Figure 5-19. As we can see, the 3σ variation is 2.1mV and the V_{REF} is 310mV, which mean the process variation is only 0.68%. The simulated local mismatch with 500-point Monte Carlo in Figure 5-20 shows that the 3σ variation is 2mV. The transistors in the current mirror dominate the mismatch. Table 5-2 show the power consumption under different temperature and process corners. Table 5-3 shows the performance comparison with state-of-the-art nW BGRs. As we can see, our work achieves the lowest power of 930pW and the largest input voltage range from 0.45V to 3.3V.

Table 5-3 Comparison with state-of-the-art nW BGRs

	This Work	[77] ISSCC'15	[72] JSSC'13	[76] VLSI'12	[70] JSSC'12
Technology (nm)	65	130	180	180	130
V_{REF} (V)	0.31	0.5	0.548	1.2	0.256
Minimum Power Consumption (nW)	0.93	32	52.5	2.98	170
Minimum V_{IN} (V)	0.45	0.5	0.7	> 1.2	0.75
V_{IN} (V)	0.45-3.3	0.5-1.65	0.7-1.8	N/R	0.75-1.6
Temp. variation (ppm/°C)	51	75	114	24.74	40
Temperature Range	-20 - 100	0-80	-40-120	-20-100	-20-85
Line Sensitivity (%/V)	0.23	2	N/R	0.062	N/R
Output Ripple	70μV	50μV	N/A	N/R	20mV

5.4 Conclusions

A sub-nW bandgap reference with a wide input voltage range is designed in this work. By directly biasing BJTs with pA current and using an input charge pump with configurable gain to increase input voltage range, the proposed BGR achieves a 930pW power consumption at 0.45V and an input voltage range from 0.45V up to 3.3V in simulations. The designed sub-nW BGR can be used together with sub-nW voltage regulators to generate voltage supplies with a good stability for process, voltage and temperature variation.

6. Conclusions

As one of the key technologies for the next-generation IoT devices, energy harvesting from ambient energy can potentially enable billions of IoT devices deployed in the near future. To achieve this goal, energy harvesting and power management unit in the self-powered SoC needs to overcome two major challenges, first, how to extract the maximum energy from the environment especially for the applications where energy limits the deployment of the devices, and second, how to keep a high power-efficiency while delivering nW power to the loads. To address those two challenges, four research work has been conducted from both energy harvesting and voltage regulation perspectives and are classified into two categories.

6.1 Highly Efficient Energy Harvesting System

The first category focuses on maximizing the energy extraction ability using advanced energy harvesting interface circuits.

- The first research explores a highly efficient piezoelectric energy harvesting system with maximum power-point tracking. In this work, a high-performance parallel synchronized-switch harvesting-on-inductor (SSHI) rectifier with >400% figure-of-merit (FOM) has been implemented together with a highly efficient MPPT scheme with >95% tracking efficiency.
- The second work in the energy harvesting category is to design a MISIMO EHPMU with nW quiescent power consumption. This MISIMO EHPMU can extract energy from

thermal, solar and vibration energy simultaneously and provide four voltage outputs for loads, which greatly extends the energy extraction and power delivery capability. It also integrates a multi-modal cold start-up block and combines the energy harvesting interfaces and voltage regulators in one power stage to minimize the form factor and eliminate the cascaded power loss.

6.2 Sub-nW Power Management Solution

The second category explores the sub-nW power management solution for powering nW IoT systems, which includes voltage regulators and a bandgap reference.

- The first work explores the design space of sub-nA LDOs, which includes two designs, a DLDO and an ALDO. The DLDO uses a hybrid synchronous and asynchronous control scheme and keeps sub-nW quiescent power. It also supports a fast load transient response through the asynchronous path. As a comparison, a traditional fully integrated sub-nA ALDO using an analog feedback loop is also presented, which also achieves sub-nW power consumption and is well suited for powering analog and RF blocks.
- The final work is to design a sub-nW BGR with a wide input voltage range. By directly biasing the BJTs with pA current and using an input charge pump with configurable gain to increase input voltage range, the proposed BGR achieves a 930pW power consumption with minimum 0.45V input voltage. The designed sub-nW BGR can be used together with sub-nW voltage regulators to generate voltage supplies with a good stability against PVT variation.

7. Publications

[SL1] X. Liu, S. Li and B. H. Calhoun, “An 802pW 93% Peak Efficiency Buck Converter with 5.5×10^6 Dynamic Range Featuring Fast DVFS and Asynchronous Load-Transient Control”, Accepted by 2021 IEEE European Solid-State Circuits Conference (ESSCIRC)

[SL2] D. S. Truesdell, S. Li and B. H. Calhoun, "A 0.5-V 560-kHz 18.8-fJ/Cycle On-Chip Oscillator With 96.1-ppm/°C Steady-State Stability Using a Duty-Cycled Digital Frequency-Locked Loop," in IEEE Journal of Solid-State Circuits, vol. 56, no. 4, pp. 1241-1253, April 2021.

[SL3] D. S. Truesdell, S. Li and B. H. Calhoun, "A 0.5V 560kHz 18.8fJ/Cycle Ultra-Low Energy Oscillator in 65nm CMOS with 96.1ppm/°C Stability using a Duty-Cycled Digital Frequency-Locked Loop," 2020 IEEE Symposium on VLSI Circuits, 2020, pp. 1-2.

[SL4] J. Im, J. Breiholz, S. Li, B. Calhoun and D. D. Wenzloff, "A Fully Integrated 0.2V 802.11ba Wake-Up Receiver with -91.5dBm Sensitivity," 2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), 2020, pp. 339-342.

[SL5] S. Li, J. Breiholz, S. Kamineni, J. Im, D. D. Wentzloff and B. H. Calhoun, "An 85 nW IoT Node-Controlling SoC for MELs Power-Mode Management and Phantom Energy Reduction," 2020 IEEE International Symposium on Circuits and Systems (ISCAS), 2020, pp. 1-5.

[SL6] S. Li and B. H. Calhoun, "Sub-microAmp Energy Harvesting and Power Management Units for Self-Powered IoT SoCs: Analog vs. Digital Implementations," 2020 IEEE Custom Integrated Circuits Conference (CICC) (Invited Paper), Boston, MA, USA, 2020, pp. 1-8.

[SL7] S. Li, A. Roy and B. H. Calhoun, "A Piezoelectric Energy-Harvesting System With Parallel-SSHI Rectifier and Integrated Maximum-Power-Point Tracking," in IEEE Solid-State Circuits Letters (Invited), vol. 2, no. 12, pp. 301-304, Dec. 2019

[SL8] S. Li, A. Roy and B. H. Calhoun, "A Piezoelectric Energy-Harvesting System with Parallel-SSHI Rectifier and Integrated MPPT Achieving 417% Energy-Extraction Improvement and 97% Tracking Efficiency," 2019 Symposium on VLSI Circuits, Kyoto, pp. C324-C325.

[SL9] S. Li and B. H. Calhoun, "A 745pA Hybrid Asynchronous Binary-Searching and Synchronous Linear-Searching Digital LDO with 3.8×105 Dynamic Load Range, 99.99% Current Efficiency, and 2mV Output Voltage Ripple," 2019 IEEE International Solid- State Circuits Conference (ISSCC), San Francisco, CA, USA, 2019, pp. 232-234.

[SL10] C. J. Lukas, F. B. Yahya, J. Breiholz, A. Roy, X. Chen, H. N. Patel, N. Liu, A. Kosari, S. Li, D. A. Kamakshi, O. Ayorinde, D. D. Wentzloff, B. H. Calhoun, "A 1.02 μW Battery-Less, Continuous Sensing and Post-Processing SiP for Wearable Applications," in IEEE Transactions on Biomedical Circuits and Systems, vol. 13, no. 2, pp. 271-281, April 2019.

[SL11] F. B. Yahya, C. J. Lukas, J. Breiholz, A. Roy, X. Chen, H. N. Patel, N. Liu, A. Kosari, S. Li, D. A. Kamakshi, O. Ayorinde, D. D. Wentzloff, B. H. Calhoun., "A battery-less 507nW SoC with integrated platform power manager and SiP interfaces," 2017 Symposium on VLSI Circuits, Kyoto, pp. C338-C339.

[SL12] J. Moody, P. Bassirian, A. Roy, Y. Feng, S. Li, R. Costanzo, N. S. Barker, B. H. Calhoun, S. M. Bowers, "An 8.3 nW −72 dBm event driven IoE wake up receiver RF front end," 12th European Microwave Integrated Circuits Conference (EuMIC), Nuremberg, 2017, pp. 77-80.

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