MIXED SIGNAL PLATFORM CIRCUITS FOR LIFETIME IMPROVEMENT OF ULTRA-LOW POWER SYSTEMS

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ABSTRACT

Ultra-Low Power (ULP) Systems on Chip (SoCs), such as wireless sensor nodes, are being used for an ever-increasing number of applications. They can be used for applications measuring and reporting almost everything, from the flow of crude oil in a remote pipeline, to the degree of corrosion in a steel bridge, to electrocardiogram (EKG), electroencephalogram (EEG), and electromyogram (EMG) signals of a home health patient. Owing to their remote locations and small form factor, these nodes need to consume extremely low power. They should operate from harvested energy, as changing their batteries regularly is not a viable option. Energy autonomy is central to the widespread deployment of these sensor nodes. However, a significant percentage of energy is lost in harvesting, supplying regulated output voltages, and in the "idle mode" of the state-of-the- art sensor nodes. Therefore, energy efficiency is the most important challenge facing the design of these sensor nodes.

The design of the processor, radio, memory, etc. for a sensor node has received much attention. However, a sensor node also needs clock sources and power supplies to be able to operate. These circuits constitute the "infrastructure" around which a digital system can be created. In wireless sensors, these circuits help extract energy from harvesters, provide regulated output voltages and clock sources for the SoC. The design of these infrastructure circuits can impact the energy

efficiency and hence the life time of the SoC significantly. In the state-of-the- art energy harvesting wireless sensor SoC, a significant percentage of energy is lost in harvesting and supplying regulated output voltages for the sensor node due to the poor efficiency of the harvester and voltage regulators. Also, wireless sensor nodes typically have a short burst of activity followed by a long idle time. This is done to save energy. The total power consumption of a sensor is often dictated by the power consumed in the idle mode. A clock source is often the only functional circuit in the idle mode, which is used for time keeping for "wake up" and synchronization needs. For such SoCs, clock power determines the life-time.

This work focuses on the flow of energy in ULP SoCs, such as wireless sensors. The proposed circuits enable highly efficient energy extraction from energy harvesters that can harvest solar and thermo-electric energy, efficient voltage regulators to provide power supplies for the SoC, the proposed work enables low voltage operation, and a ULP Clocking scheme to elongate the life-span in idle mode. These circuits increase the amount of energy harvested from the ambient source, reduce the loss in voltage conversion, enable low voltage operation and decrease the power consumption in idle mode to significantly improve the operational life time of a ULP system

APPROVAL SHEET

The dissertation

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"गुरु प्यारे का दम दम शुकर गुज़ार"

I dedicate my dissertation to my Guru, Param Guru Huzur Dr. Prem Sharan Satsangi Sahab.

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Chapter 1

Introduction

Ultra-Low Power (ULP) Systems on Chip (SoCs), such as Body Sensor Nodes (BSNs) or Wireless Sensor Nodes (WSNs), and more recently internet of things (IoT) promise to change the way we experience life by providing rich information about our activities, health, and the environment. These miniaturized nodes are responsible for sensing data periodically, processing it, and communicating information wirelessly. They can be used for hundreds of sensing applications – measuring and reporting everything from the flow of crude oil in a remote pipeline, to the degree of corrosion in a steel bridge, to EKG, EEG and EMG signals of a home health patient. These devices require small size and must consume extremely low power to be able to operate from harvested energy for their longer life time. Significant progress has been made over the last few years. Sensor nodes, which can operate from harvested energy without batteries, have been demonstrated [1]. However, there is a need to improve the operating lifetime of these systems for their extensive deployment in the environment. This is an ongoing research topic at various levels, from system to software to hardware. This dissertation focuses on improving the lifetime of a ULP SoC at the hardware level. It proposes improved energy harvesting and power management solutions, clock sources, a modeling framework to enable accurate power management, etc. These circuits and the model constitute the basic infrastructure for the efficient use of energy in ULP Systems.

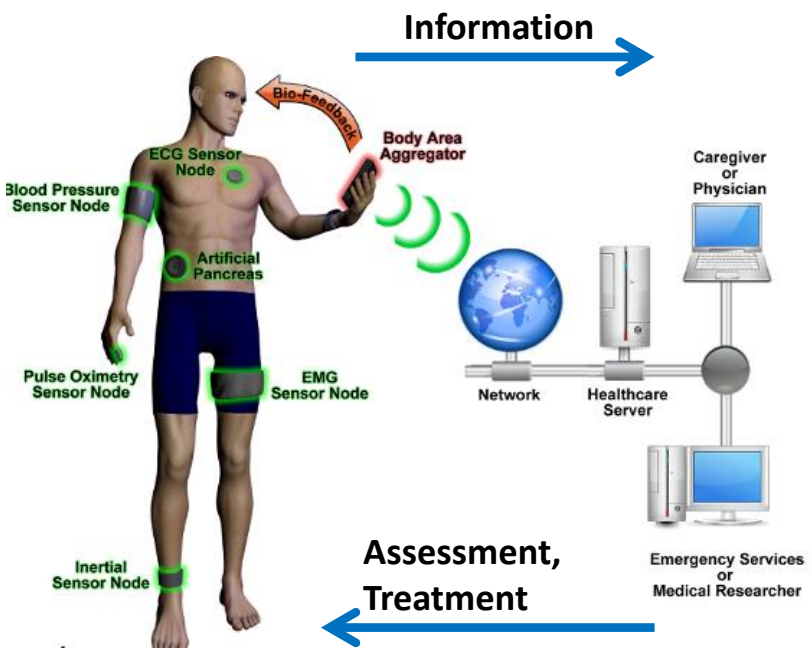


Figure 1-1 Deployment of Body Sensor Nodes [2]

Figure 1-1 shows the deployment of body sensor nodes in a body area sensor network implementation. While the figure here shows a specific application in body area networks, a similar principle exists in interconnected wireless sensor nodes and internet of things. These networks have several sensor nodes deployed at several locations to accomplish a range of sensing functionality. In Figure 1-1, several BSNs are placed on a human subject to monitor his ECG, blood pressure, EMG, etc. The sensor nodes interact wirelessly with the body area aggregator, which acts as a base station in a wireless system. The body area aggregator can be a cell phone or other wireless transceiver system capable of processing. The interconnected system can be used to monitor the health of the human subject, provide information on his bio-metrics and communicate in cases when intervention is required. The sensor nodes are essential systems for the proper operation of these networks, as they provide the raw data. For large scale and pervasive use of

these systems, sensor nodes must be of small factor, consume low power, and have long lifetimes. Since these systems are expected to be ubiquitous and are often remotely located, a batteryless sensor node is desirable, as it requires no intervention and provides energy autonomy. The dissertation focuses on providing power autonomy for sensor nodes by improving the energy harvesting, reducing the power consumption and providing operation from low energy levels.

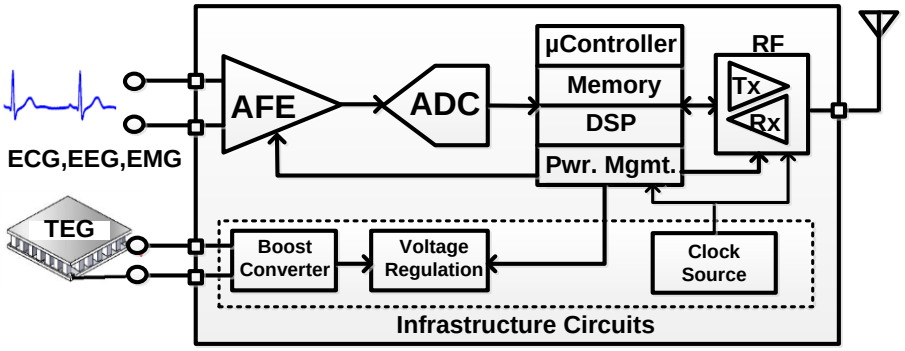


Figure 1-2 A batteryless energy harvesting BSN SoC [1]

Figure 1-2 shows a BSN SoC [1] that is a batteryless system that harvests energy from body heat. It operates using the harvested energy to enable a perpetual energy autonomous system. It has an Analog Front End (AFE) and Analog to Digital Converter (ADC) to perform sensing, which can be ECG, EKG or other environmental sensing. The sensed data is sent for digital processing, which uses a micro-controller, memory etc. The processed data is then transmitted through an RF transceiver to a nearby aggregator (for example, the Body Area Aggregator, as shown in Figure 1-1). The SoC in Figure 1-2 harvests energy from a Thermo-Electric Generator (TEG) utilizing body heat. The circuitry that extracts energy from the harvester consists of a boost converter that collects the energy from the TEG at lower voltage and stores it at a higher voltage on a capacitor. Higher voltage is needed for circuit operation. Finally, a voltage regulation block provides

different power supply rails (V_{DDS}) to run different blocks in the SoC, such as analog, RF, etc. The lifetime of the system is impacted by the amount of energy harvested, the power consumption of the system and minimum energy level at which the system can operate. This dissertation contributes to improve on all these components to improve the life-time of these systems.

1.1 Flow of Energy in a Batteryless System

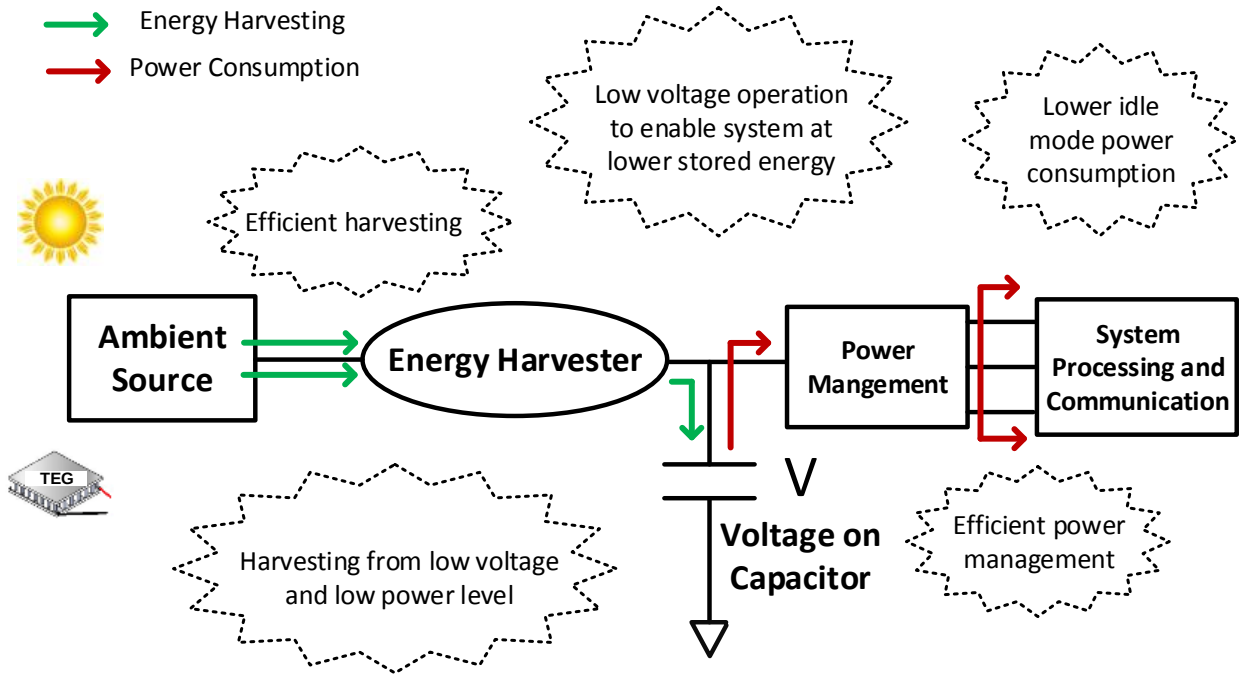


Figure 1-3 Flow of energy in batteryless system highlighting the requirements for increasing the system life-time

Figure 1-3 shows the flow of energy in an energy harvesting battery-less ULP system. First, energy is harvested from an ambient source, such as solar cells, TEG, or other ambient source, using an energy harvester circuit. The harvested energy is stored on a capacitor in the form of voltage V. This stored energy is then taken up by the power management circuit to provide various power

supply voltages (V_{DD}s). These V_{DD}s are used to provide power supply voltages to various communication and processing blocks on the system. While the first part of the system constitutes the process for obtaining energy from the environment, the second part of the system is the use of this energy to accomplish the sensing task. Improvements in low power sub-threshold design [3][4], as well as improvements in the area of low power radios for communication [5][6], are reducing the power consumption of processing and communication which helps in improving the lifetime of the system. However, there is a need for improvement at each step of energy flow in the system to significantly improve its life-time. This can be accomplished through the following design requirements.

- The system should be able to harvest from very low voltage and power levels from the ambient sources to extract every possible bit of energy available there.
- The energy harvester should be efficient and minimize the losses involved in transferring the energy from an ambient source to the storage capacitor.
- The voltage on the storage capacitor is the indicator of the amount of energy available for the system. The system can turn on only if the voltage on the capacitor reaches a set threshold level, which would indicate a minimum energy level for the system to be able to operate. Energy below this level is not useful for the system. The life-time of the system can be improved significantly if the operating voltage on the capacitor is brought down. This would bring down the minimum energy level needed for the system to turn on. In other words, the system can turn on from a lower level of harvested energy. Therefore, the operating voltage of the system should be brought down to improve its lifetime.
- The stored energy on the capacitor is transferred to generate various power supplies needed for the system to operate different blocks in the system at different voltage level (which is

done to reduce the processing and communication power). Therefore, power losses in this step should be minimized and the voltage conversion should be very efficient.

- The ULP systems spend most of their time in idle mode, with short bursts of high activity. The total power consumption of the system is often dictated by the idle mode power consumption. To increase the life-time of the system, the power consumption in idle mode needs to be reduced.

Therefore, the lifetime of the system is increased by increasing the amount of harvested energy, reducing the losses in voltage conversion, reducing the operating voltage, and reducing the standby power consumption. This is the central theme of this dissertation, and the following contributions are made to achieve higher life-time for ULP systems.

- A stable on-chip clock source that can lock to a given clock frequency, a locking scheme to lock the clock source and ultra-low power on-chip clock sources to reduce the idle mode or standby current.
- An ULP crystal oscillator circuit as an alternative clocking solution for lower power consumption and higher stability.
- A low power, high efficiency energy harvester extraction circuit that can harvest from 10mV ambient sources to increase the amount of harvested energy.
- A low power, low voltage bandgap reference for energy harvesting and power management to reduce the idle mode power consumption and enable low voltage operation.
- A single inductor multiple output buck-boost converter that enables high efficiency circuits as well as low voltage operation.

- A single inductor multiple output energy harvesting and power management solution to harvest from low power solar cells, to enable high efficiency, low cost, integrated harvesting and power management system.
- A model that accurately establishes the benefits of power management techniques for ULP SoCs in the presence of voltage regulators to enable design time choices for regulators and power management techniques.
- A single inductor multiple output Voltage regulator with on-chip decoupling capacitors to implement panoptic dynamic voltage scaling technique.
- While not included in this dissertation, the author also made the following contributions for the overall improvement in ultra-low power system design.
    - A clock and data recovery (CDR) circuit for the RF interface of BSN
    - A low power interconnect circuit operational from 0.3V to reduce the interconnect power consumption
    - An ultra-low power analog to digital converter for ECG, EKG applications.
    - Design and system level improvements and options for inter-chip communication between ULP ICs
    - Modeling techniques to assess circuit and system reliability
    - Circuit technique to improve the start-up time of the crystal oscillators by an order of magnitude.

These contributions will help us enable longer life-time, low power systems which will help in making ubiquitous sensing and sensor networks a reality which in turn will help in improving our way of living by improvements in health care, safety, entertainment, activity tracking and various

other aspects of our lives. Next section gives a brief description of the contributions from the system perspective.

1.2 Low Power Clocking

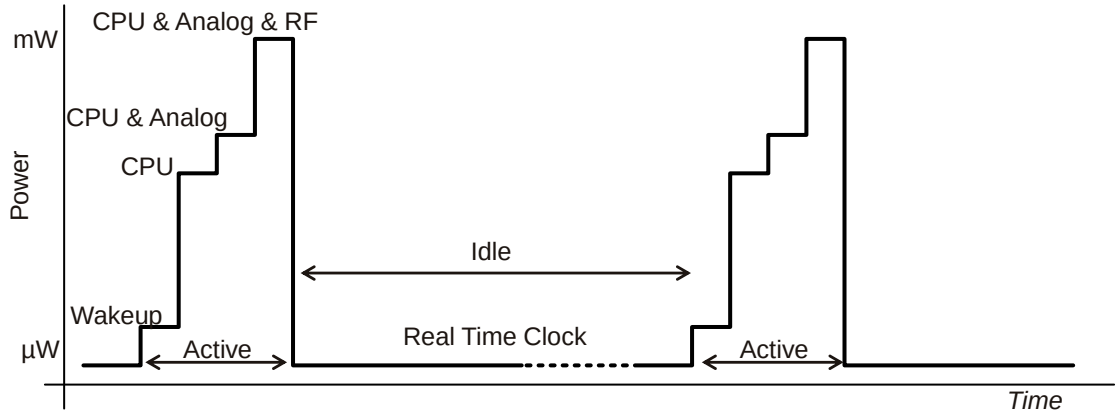


Figure 1-4 Typical Power Consumption Profile of a ULP SoC

A typical operation of a ULP SoC like BSN constitutes a short burst of activity followed by a long idle time. The short burst of activity consumes higher power, whereas in idle mode, the system consumes very little power. Spending larger time in idle mode saves energy relative to the continuous operation. Figure 1-4 shows the power consumption profile of a BSN. The system wakes up first and starts the CPU. Analog blocks are then turned on to perform the sensing application and finally, RF turns on for communication. The power consumption of the system rises in steps as each block turns on. The system goes back into sleep mode after completing the RF communication. These SoCs use a real-time clock (RTC) for keeping time. The RTC maintains precise timing for waking up and synchronizing the chip. Figure 1-4 also shows that the total power consumption of the chip can vary depending on the application. For example, the power can be

dominated by the active mode if the SoC has higher activity, and is dominated by the idle mode (RTC power) if the SoC has lower activity. There is a need to reduce and optimize the power consumption in both regions of activity in order to extend the system life time. In this work the idle mode power is reduced by the proposed low power clocking solution while active mode power consumption is reduced by efficient energy harvesting and power management (EHM) circuits.

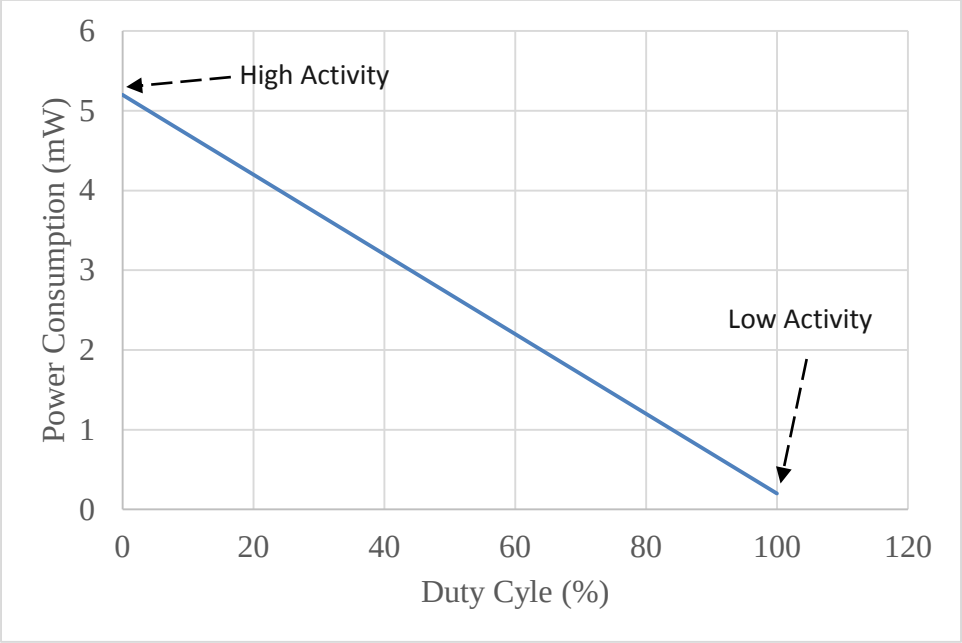


Figure 1-5 Power consumption of the system with duty-cycling

Figure 1-5 shows that the power consumption of a SoC, which stays in the idle mode for the majority of time, is dominated by the RTC. The RTC is typically implemented using an off-chip crystal resonator (XTAL). Their power consumption can be anywhere from a few 100nW to hundreds of µW. This work presents ULP clock sources to reduce the power consumption in the RTC. A solution designed with an on-chip, silicon-based oscillator reduces the power consumption of the clock to 150nW. A locking scheme is proposed to lock the on-chip clock source to a known frequency. The proposed solution has been fabricated and demonstrated in silicon. A second

version of the design brings the power down to 20nW. The proposed on-chip solution has a lower cost when compared to off-chip RTCs utilizing XTAL. Further, we also propose an alternate design of crystal oscillator reducing its power consumption to 1nW. This ULP XTAL can reduce the power consumption in RTC by a few orders of magnitude. It can be used for applications where higher stability is preferred at the expense of cost. Chapter 2 covers the implementation details of the proposed circuit.

1.3 Energy Harvesting and Power Management

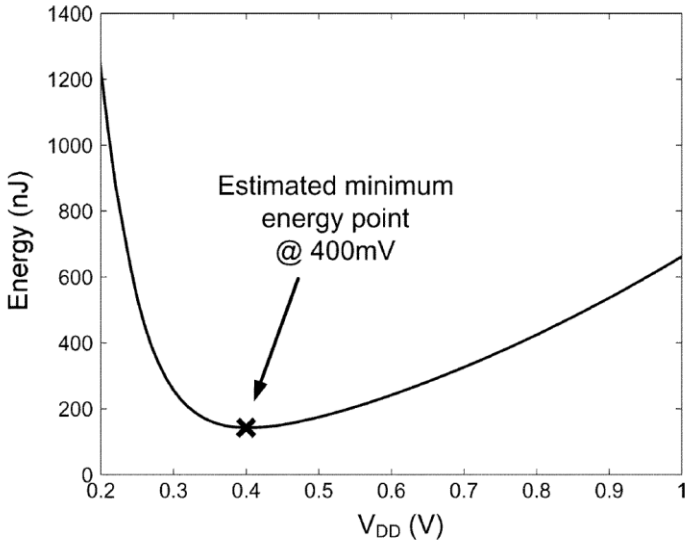


Figure 1-6 Optimal energy point of a block inside a SoC [7]

An optimal energy operating point exists for each block in a SoC [7]. Figure 1-6 shows the variation of energy consumption with VDD. Various blocks of a BSN, such as AFE, RF, or CPU, need their own power supply voltage (VDD) to be able to operate at the optimal energy and performance point. Therefore, a BSN SoC needs multiple supply voltages apart from the energy harvesting interface. Conventional approaches to obtaining and managing energy from ambient

sources either employ more than one inductor, which increases the cost, or use low drop out (LDO) regulators which have lower efficiency. The lower efficiency of LDOs can result in the loss of energy, which is not desirable. There is a need to provide an efficient and low-cost energy harvesting and power management solution for BSNs. This work proposes a highly efficient energy harvesting and power management solution with various design options for BSNs. The proposed solution can harvest energy from TEG and solar cells. It also proposes single inductor power management circuits with on-chip and off-chip decoupling capacitor options.

In addition, the dissertation also presents a model that accurately establishes the benefits of power management techniques for ULP SoCs. The benefits of power management techniques like Dynamic Voltage and Frequency Scaling (DVFS) cannot be established accurately without assessing their impact on voltage regulators like the DC-DC converter. For example, DVFS uses a high voltage to support higher performance and a lower voltage to save power. However, changing the output voltage of a DC-DC converter incorporates significant power overhead, and the efficiency can vary widely across voltage and current loads. These overheads may offset the benefits from DVFS. There is a need to measure the benefits of power management techniques like DVFS, clock gating, etc., in conjunction with their impact on the DC-DC converter. The proposed model enables the study of various power management techniques by taking into account their impact on DC-DC converters of different topologies.

1.4 Dissertation Organization

The dissertation is organized as follows. Chapter 2 presents a clocking solution for ULP SoC. An ultra-low power clock source that can be locked to a desired system clock frequency is presented.

The proposed clock source is very stable and achieves low power by applying duty-cycling techniques. A process calibration scheme and other compensation techniques make it perform well across varying environments. Further, an ULP crystal oscillator circuit that consumes less than a 1nW of power is also presented in Chapter 2. The proposed circuit can operate at 0.3V to enable functionality at very low power levels. The crystal oscillator solution provides a low power and more stable alternative to the on-chip clock source. The contributions in the low power clocking solution help in lowering the idle mode power consumption to increase the system life-time.

Chapter 3 presents the energy harvesting and power management solution for ULP systems. Here we present a low power, high efficiency energy harvester that can harvest from a 10mV ambient source to increase the amount of harvested energy. We also present a low power, low voltage bandgap reference for energy harvesting and power management to reduce the idle mode power consumption and enable low voltage operation. Further, we also present a single inductor, multiple output buck-boost converter that has high efficiency and enables low voltage operation. Finally, we present a single inductor, multiple output, energy harvesting and power management solution to harvest from low power solar cells that enable high efficiency, low cost, integrated harvesting and power management system.

Chapter 4 presents a model which accurately establishes the benefits of power management techniques for ULP SoCs in the presence of voltage regulators to enable design time choices for regulators and power management techniques. It also presents a Single Inductor Multiple output Voltage regulator with on-chip decoupling capacitors to implement panoptic dynamic voltage scaling technique.

Finally, Chapter 5 concludes the dissertation. It quantifies the benefits in life-time improvements of the ULP system based on the contributions made in the dissertation. This chapter also points out areas for future research work and improvements for the design techniques described in this dissertation.

Chapter 2

Ultra-Low Power Clock Sources

In an Integrated Circuit (IC), a clock source is used for various functions, which can include synchronous implementation of an arithmetic and logic unit, inter-chip and intra-chip communication, and time keeping. The clock source constitutes a key component in an IC. It is extremely important for ULP SoCs like a BSN. A typical BSN operation constitutes a short burst of activity followed by a long idle time. The total power consumption of a BSN is often dictated by the power consumed in the idle mode. A clock source is often the only functional circuit in the idle mode. It is used for time keeping, for “wake up”, and for synchronization needs of the BSN. The clock source, therefore, can determine the power consumption of a low duty-cyle BSN.

A clock source can be implemented either using off-chip components, such as a crystal resonator, or using on-chip devices. An on-chip implementation of a clock source is typically lower in cost but poor in stability when compared to the off-chip implementation. In this chapter, we will present a stable on-chip clock source and an ultra-low power crystal oscillator circuit with power consumption in the range of 1nW. The proposed circuits are suited for BSN and show lower power and more stability compared to the state of the art. The proposed solutions provide options in the BSN platform for the implementation of the clock. While an on-chip clock source provides a stable, low power, and cheap solution for clocks, an off-chip crystal oscillator can be used for the cases where more stability and even lower power consumption is desired.

2.1 Prior Art

BSNs typically require a stable clock source for precise data sampling, an RF modulation clock, and keeping time to reduce the cost of re-synchronizing to other radios. The conventional approach of using a crystal oscillator (XTAL) adds 3-4 off-chip passives, has startup times in the ms to second range, and can consume an appreciable fraction of the system power. For example, the energy harvesting BSN SoC in [1] consumes 19µW while measuring ECG, extracting heart rate, and sending RF packets every few seconds, and over 2µW of that total is in the 200kHz XTAL. The alternative clocking scheme, to replace XTAL with low power and low cost on-chip reference oscillators for low power systems, is an ongoing effort [8]-[11].Widely varied approaches exist. In [11], authors present a CMOS relaxation oscillator. High temperature stability is achieved using poly and diffusion resistors together to realize the resistor in an RC relaxation oscillator. These resistors have complementary temperature dependence, and they cancel the effect of temperature variation to achieve a temperature stability of 60ppm/^{o}C. On-chip oscillators, using the gate leakage current, have been proposed in [8]-[10]. Gate leakage current has very small temperature dependence, which makes these oscillators stable. However, these oscillators can operate only at very low frequency (0.1-10 Hz) due to the low magnitude of gate-leakage current. Also, the oscillation frequency is not very well controlled across the process. The most stable oscillator [10] in this category has a temperature stability of 32ppm/^{o}C operating at 0.4Hz.

Parallel to the exploration of on-chip clocks for BSNs, research has been going on for off-chip clock sources using crystal oscillator. Recent work on the design of real-time clocks using crystal oscillator shows power consumption of 5.58nW [13], making it possible to use them for BSN applications. Power consumption of crystal oscillator can be reduced by reducing the amplitude of

oscillation by operating them at lower voltages. Low power electronic watches use this technique to operate crystal oscillator circuits in sub-threshold or weak inversion regions of operation for transistors [14]. The lowest reported power for such circuit is at 27nW [15].

In this chapter we propose two solutions for providing clocks for BSNs. First, we present a new scheme to replace XTALs with a ULP on-chip clock source (no off-chip passives) for the ~100kHz range that is roughly 7X lower power than typical XTALs (operating at 100kHz) and has a temperature stability of 5ppm/^{o}C. Further, for an off-chip solution, we propose a technique of duty cycling the crystal oscillator in conjunction while operating them in a sub-threshold region. We achieve a simulated power consumption of close to 1nW for a real time clock. These solutions provide flexible platform circuits for BSNs clocking schemes, from which a designer can choose, depending on the needs of the application.

2.2 ULP On-Chip Clock Source[1]

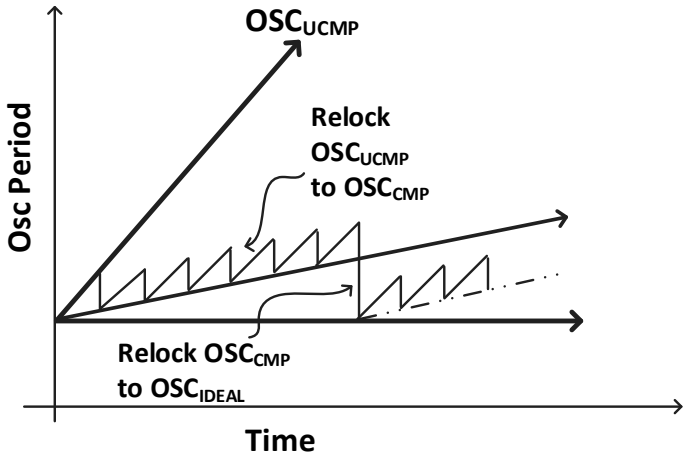


Figure 2-1 Scheme of re-locking low stability oscillator to achieve high effective stability

[1] A lot of content comes from [AS5]

To maintain a stable on-chip clock source, we need a temperature compensated oscillator (Osc_{CMP}). However, these circuits tend to consume power comparable to XTALs, in the few µW range for ~100kHz. We propose a scheme to use an ULP uncompensated oscillator (Osc_{UCMP}), with the Osc_{CMP} to provide both stability and ULP consumption. Figure 2-1 shows the concept. As temperature changes at a given rate, both oscillators will aggregate time error relative to the ideal reference, with Osc_{UCMP} accumulating error much faster, due to its lower stability. If we periodically lock Osc_{UCMP} to Osc_{CMP}, then its effective stability stays within a bounded error relative to Osc_{CMP}, and we can make this error arbitrarily small by changing the duty cycle of re-locking. We can also re-lock to the original reference if it is available (e.g. XTAL or signal over RF). In between lock points, the higher power oscillator(s) can shut down, setting the system power to that of the Osc_{UCMP}. To make this work well, we need a fast locking circuit, low power oscillators with rapid on/off, and digital calibration storage. Figure 2-2 shows the architecture of our clock source. The locking circuit locks clock source B to A. Osc_{CMP} or Osc_{REF} can be selected at A and $Osc_{UCMP,}$ or other clocks to be locked, can be selected at B. The locking circuit digitally calibrates B to provide an output clock with the same period as A.

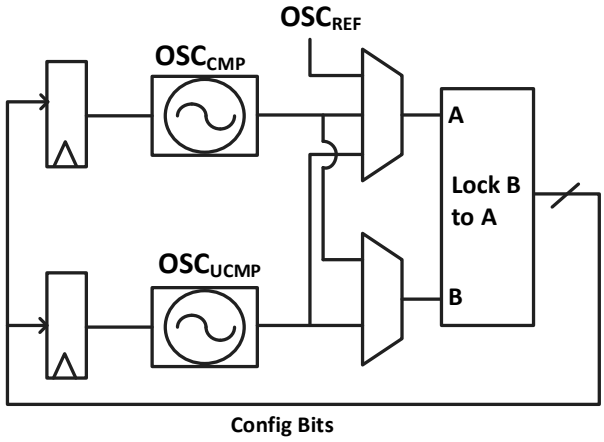


Figure 2-2 Architecture of the clock source

2.2.1 Compensated Oscillator Design

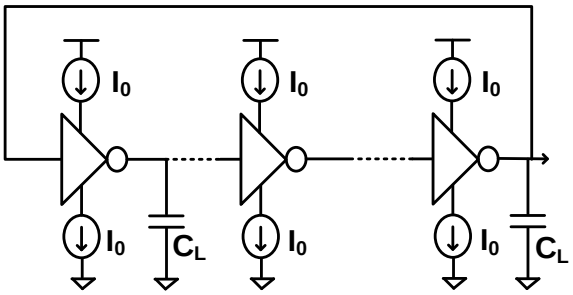
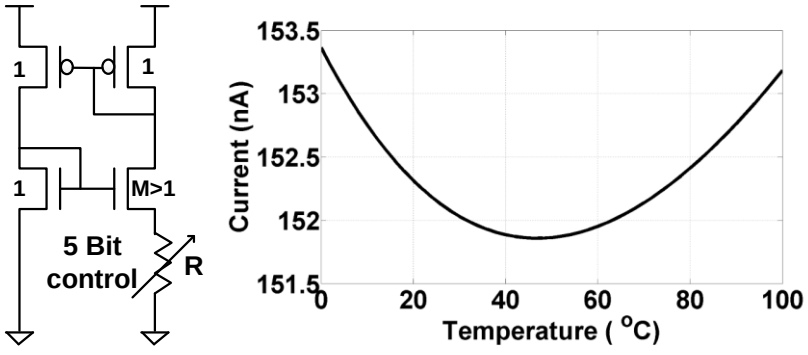


Figure 2-3 Current Controlled ring oscillator

Our Osc_{CMP} uses a current controlled ring oscillator, and Figure 2-3 shows the circuit diagram. It is designed to be stable across temperature, and it uses configuration bits to compensate for process variations. The frequency is set by current Io, capacitance C_L, which are MIM (metal-insulator-metal) capacitors with very small temperature variation, and by the inverter's switching threshold. In this architecture inverter threshold is set to $V_{DD}/2$. To set the constant current Io, we use a PTAT and a CTAT current source. The current of a PTAT current source (Figure 2-4 (a)) increases almost linearly with temperature. We use a long channel MOS transistor operated in the strong inversion region to implement the CTAT, whose current decreases linearly with temperature. We add the current from the PTAT and the CTAT using current mirror to get a current independent of temperature. Figure 2-4 (b) shows that Io varies by 1% over a 100°C range (~100ppm/°C).



a) PTAT b) Simulaton of Constant Current I_0

Figure 2-4 a) PTAT current source b) Simulation result of a Constant current source.

2nd Order Compensation Circuit

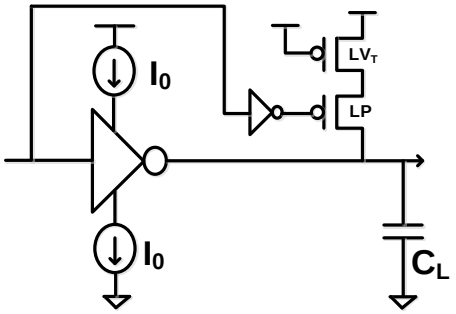


Figure 2-5 2nd order compensation circuit using LV_T transistor to compensate for increase in current with temperature

The oscillator based on the current source of Figure 2-4 (b) will have an oscillation period that will still have a small dependence on temperature in the second order because the current sources are not purely linear . The period of oscillation will reduce as the temperature goes up from 20°C-100°C. We employ 2nd order compensation to further improve stability. This circuit comprises an off, low threshold (LV_T) MOS, a switch, and an inverter. Figure 2-5 shows the circuit diagram of the 2nd order compensation. It essentially forms a leakage pull-up path that adds charge to C_L, slightly increasing the delay. This slight increase in delay increases with temperature.

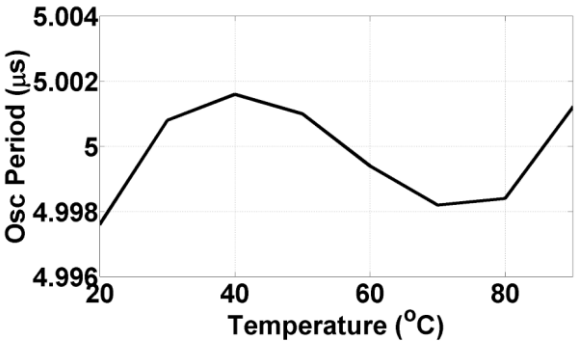
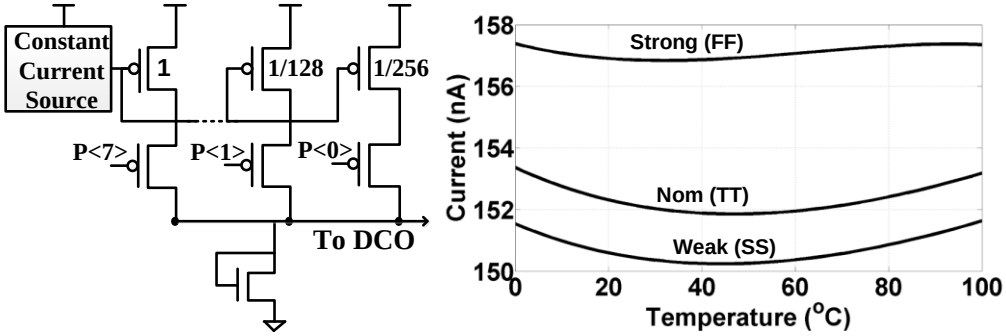


Figure 2-6 Temperature variation of the clock period when employing the 2nd order compensation circuit

Figure 2-6 shows how this nullifies the 2nd order increase in current at high temperature, giving a nearly flat period for a 200kHz reference over the range of 20°C to 90°C.

Process Compensation

We use configuration bits to compensate for the effects of process variation on the constant current source and delay element. In the current source, variation may offset the PTAT and CTAT current, so that one dominates in the target frequency range, making temperature stability impossible. We vary resistance R in the PTAT shown in Figure 2-4 (a) to balance its current with the CTAT against global variation using 5 binary bits. Similarly, we use 6-bit binary weighted off-transistors in the 2nd order compensation to align the leakage current to compensate for the process drift in leakage.



a) Binary Weighted Source b) Process Variation of current

Figure 2-7 a) Binary weighted configuration bits b) Simulation result of current source variation across process points

We use the constant current source as an input to a binary weighted (8-bit) current mirror used in Figure 2-7 (a). This lets us generate the desired current for a given desired frequency across process at 20ns resolution. The PTAT current source addresses the variation of delay of the delay-line with temperature. The simulation results in Figure 2-7 (b) show that the similar stable current can be achieved across process. We include 10-bit coarse and 5-bit fine control for 1ns and 20ps resolution, respectively, which are set by the locking circuit (Section 2.2.3). This results in a Digitally Controlled Oscillator (DCO) that can lock to a desired frequency. Figure 2-8 shows the architecture of the DCO.

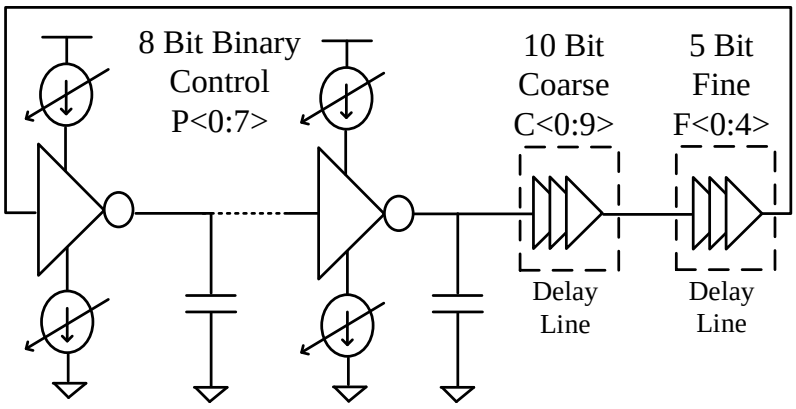


Figure 2-8 OSC_{CMP} DCO Architecture

Power Supply Variation

The Osc_{CMP} is sensitive to variations in the power supply. The PTAT circuit has better power supply tolerance but the CTAT is more sensitive, as it uses V_{DD} directly at its gate. Osc_{CMP} shows a dependence of ~0.1%/mV. This is still better than [4], where power supply dependence is 0.42%/mV, but it could still be a problem for stability if V_{DD} is poorly regulated. Osc_{CMP} will aggregate error over time. This can be addressed either by using a low noise regulator, such as proposed in [6], or by relocking Osc_{CMP} often with the external references.

2.2.2 Uncompensated Oscillator Design

The Osc_{UCMP} uses leakage as the current source to the delay elements, along with the same digital inverter-based coarse and fine delay compensation as the Osc_{CMP}. It uses binary weighted off LV_T transistors for the realization of the current source. Figure 2-9 shows the Osc_{UCMP} architecture. The use of off LV_T transistors gives a lower area DCO at ~100kHz. Long channel transistors are needed to realize it at ~100 kHz frequencies with on transistors. This will increase the area significantly.

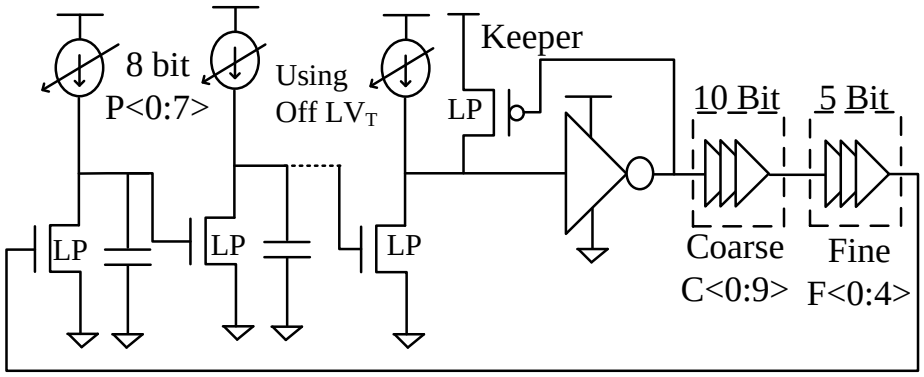


Figure 2-9 OSC_{UCMP} DCO architecture

Since no compensation is needed for $Osc_{UCMP,}$ we chose the lower area solution. Osc_{UCMP} consumes 80nW of power at 100kHz in simulation. It has a poor temperature stability of 1.67%/^{o}C.

2.2.3 Locking Circuit

We use a 5-bit counter as a frequency comparator to compare Osc_{CMP} to a reference or to compare Osc_{UCMP} to Osc_{CMP}. The reference clock (REF_CLK) is divided by 2 and fed to the frequency comparator. The divided clock is called REF. As REF goes high, DCO gets enabled and will start

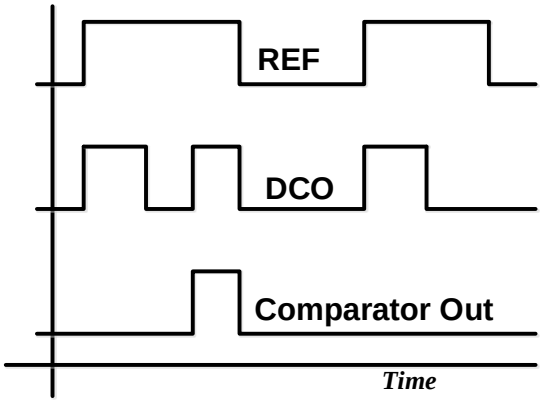


Figure 2-10 Timing diagram of frequency comparator circuit

oscillating. The counter starts counting the rising edges of the DCO when the reference input is high. If it counts more than 1, the output of the frequency comparator goes high; otherwise, it is low. Figure 2-10 shows the timing diagram.

Our locking circuit comprises this comparator, SAR logic, and either DCO in a feedback configuration. Figure 2-11 shows the architecture of the locking circuit. The frequency comparator gives 1 when the DCO's output frequency is higher than the reference and 0 when it is lower. The SAR logic approximates the current and delay inside the DCO, based on the logical output of the comparator and sets the 23 DCO control bits, which are stored in a register. The comparison is performed when REF is high, and the current source is configured when REF is low, to let the current source settle correctly.

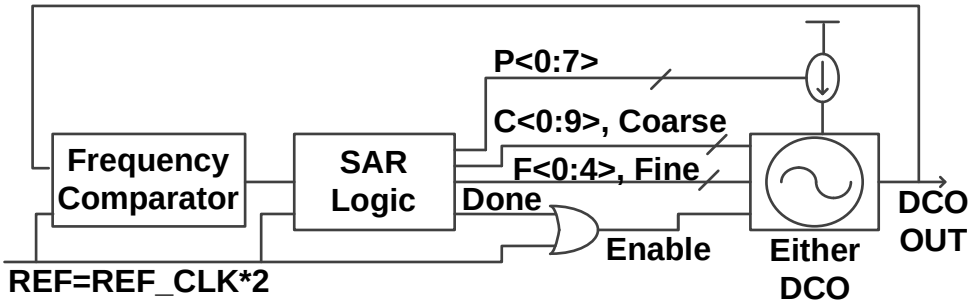


Figure 2-11 Fast locking circuit for DCO using binary search

Figure 2-12 shows the locking transient at 200kHz. The lock takes 46 reference cycles and has a resolution error of ~20ps. Once the calibration is performed, the DCO runs on its own. The temperature compensation scheme controls the drift. In this way, the lower power oscillator is configured to the frequency of the stable clock. We can make the stability of the lower power oscillator similar to the stable clock by performing this lock often.

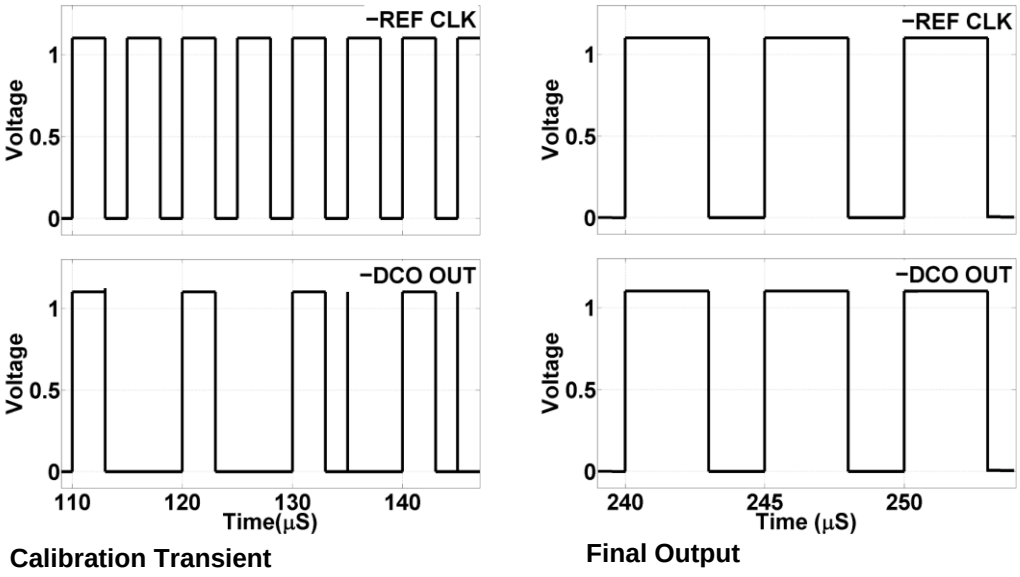


Figure 2-12 Simulation result of the locking transient

2.2.4 Prototype Implementation and Measurement

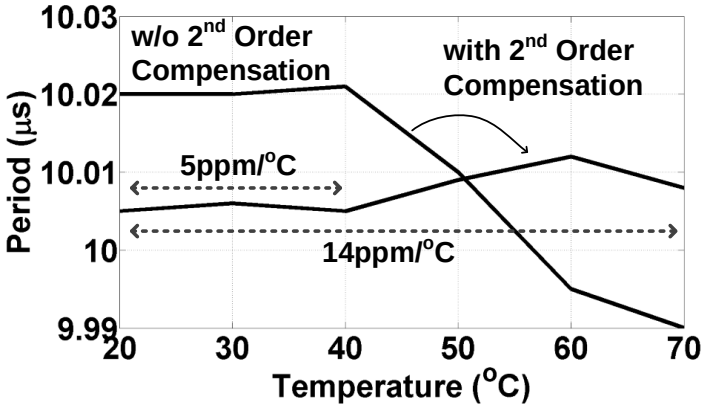


Figure 2-13 Measured Clock Period of OSCCMP showing the improvement in stability by 2nd order compensation circuit

We implemented the clock source (0.5mmx0.5mm) in 130nm CMOS. Osc_{CMP} and Osc_{UCMP} consume 1μW and 100nW at 100kHz, 1.1V VDD, respectively. The process tuning bits give us a full measured locking range from 15kHz to 350kHz. In this range, we can lock successfully to the

reference within the accuracy of jitter on the input clock. Figure 2-13 shows the measured stability of the Osc_{CMP} after calibration as 5ppm/^{o}C in a BSN compatible range of 20-40^{o}C (14ppm/^{o}C from 20^{o}C to 70^{o}C). Without the 2nd order compensation, this stability degrades to 60ppm/^{o}C. Figure 2-14 shows the temperature stability across 10 chips from a temperature range of 20-40^{o}C.

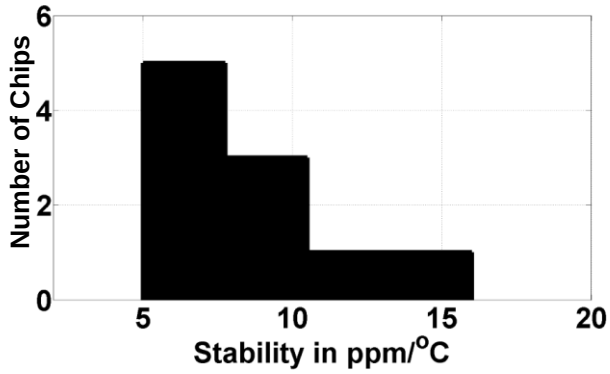


Figure 2-14 Measured Stability of 10-chips from 20 to 40 ^{o}C

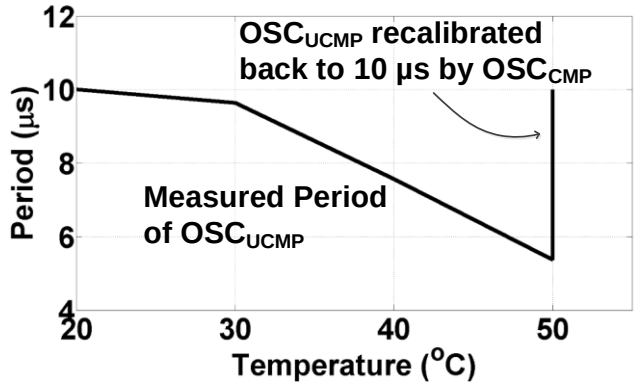


Figure 2-15 Recalibration of OSC_{UCMP} with OSC_{CMP}

We lock Osc_{CMP} to a 100kHz reference, lock Osc_{UCMP} to Osc_{CMP}, then power down Osc_{CMP}. Figure 2-15 shows the measurement result of recalibration of Osc_{UCMP} with Osc_{CMP}. In this test, Osc_{UCMP} and OSC_{CMP} were calibrated to 100kHz by an external reference at 20^{o}C. After that, we shut down Osc_{CMP} and raised the temperature of measurement to 50^{o}C. Then we wake up Osc_{CMP} and recalibrated Osc_{UCMP} with it. Figure 2-15 shows the process, and Figure 2-16 shows the output

waveform after calibration. Using this scheme, we can achieve stability (5ppm/oC) at ultra-low power.

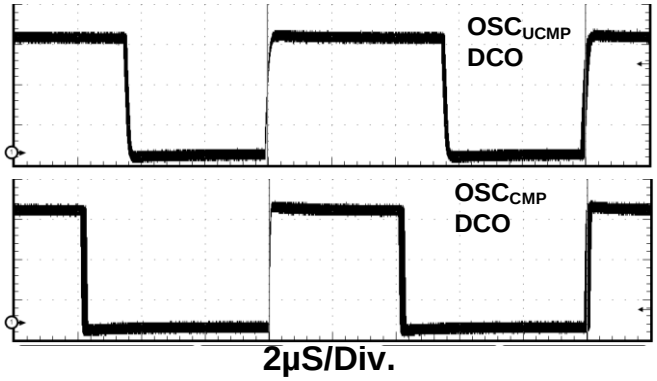


Figure 2-16 Measured waveform of DCO outputs at 100 kHz after recalibration

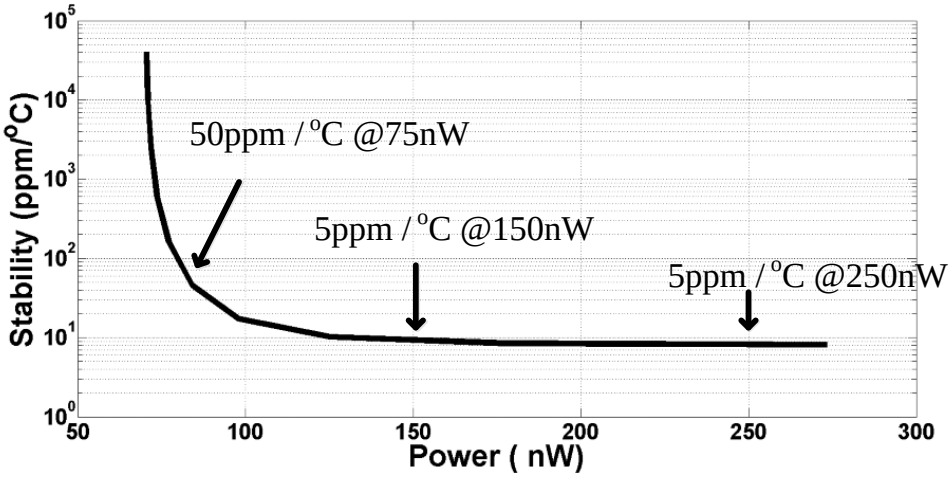


Figure 2-17 Measured power/stability tradeoff with duty cycling for 1oC/s temperature change

Figure 2-17 shows the result of duty cycling for the case when temperature varies by 1°C/s or less. We achieve a stability of 5ppm/°C at 150nW. During locking, we can turn on Osc_{CMP} at the rising edge of Osc_{UCMP} and pass Osc_{CMP} as the clock, to avoid glitching, or clock gate the system clock to prevent problems in downstream circuits. Figure 2-18 shows the die photo with the proposed circuit implementation in 130nm CMOS process.

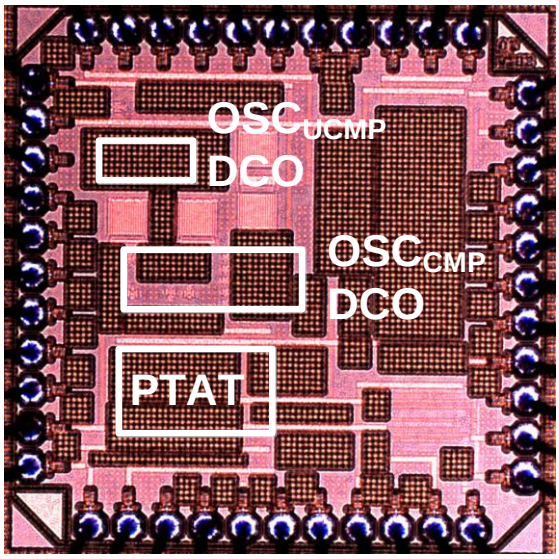


Figure 2-18 Die photo: Implementation of the prototype clock in 130nm CMOS process

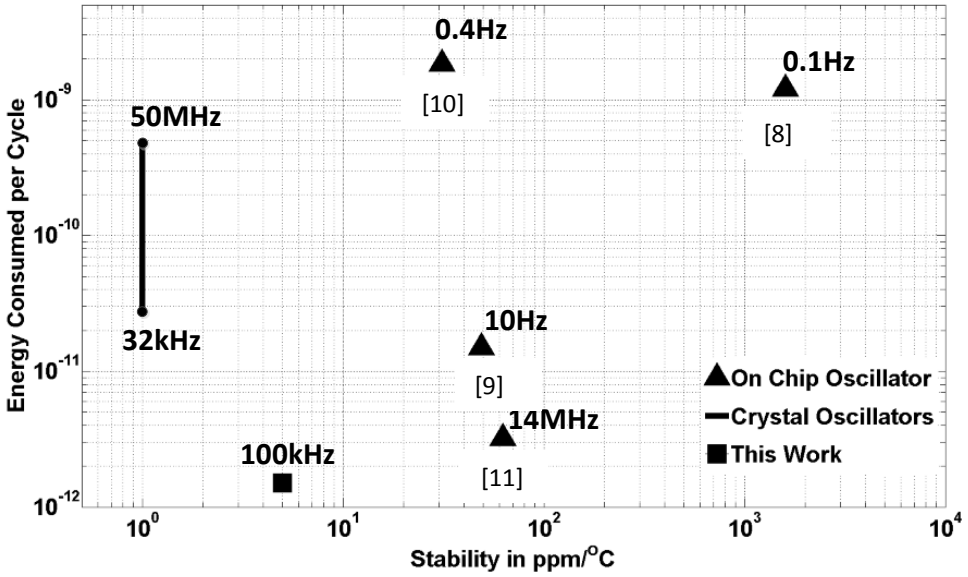


Figure 2-19 Energy per cycle and stability comparison with existing solution

Figure 2-18 shows the die photo. Figure 2-19 shows that our work is 10X more stable and consumes 3X less energy than the prior art. Some ULP timers for BSNs are approaching our stability [3-4], but they are 10^6 slower frequency. We exhibit similar stability to an XTAL with

~7X less power and no off-chip components, providing a low cost ULP solution for wireless sensors and BSNs.

2.3 ULP Crystal Oscillator

In this section, we present an ULP crystal oscillator circuit. A crystal is an electromechanical resonator which resonates at its natural frequency when excited with electrical energy. Figure 2-20 shows a conventional crystal oscillator circuit. The equivalent circuit of a crystal consists of a series RLC circuit, with a parasitic parallel capacitor Cp. The frequency of oscillation is mainly determined by Lm and Cm. The effective series resistor (ESR) is the energy dissipating component of the crystal. The inverting amplifier, Amp, provides the negative resistance that overcomes the loss from ESR and pumps energy into the crystal, making it oscillate at its natural frequency.

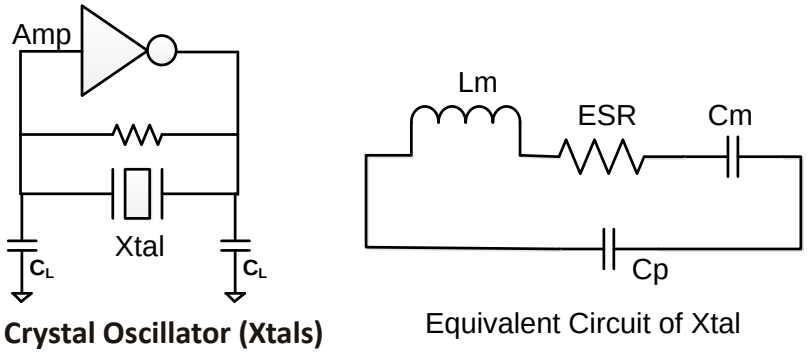


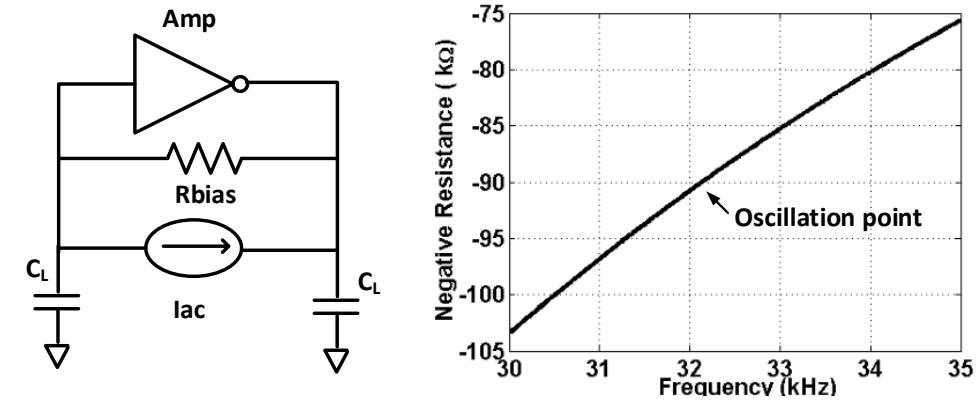
Figure 2-20 Crystal Oscillator Circuit

The output frequency of the crystal oscillator is very precise and its stability is usually specified at parts per million or per billion (ppm/ppb). The extremely precise output frequency of crystal oscillators makes them a natural choice for implementing clocks. A crystal oscillator can be a more convenient solution to implement clocks in BSNs, when compared to the on-chip solution

presented in section 2.2, because it would not need calibration for process and voltage given the application. A crystal oscillator's frequency of oscillation is independent of voltage and process. However, it needs off-chip components and can incur higher costs.

Functioning

Figure 2-20 shows the architecture of the crystal oscillator. It consists of a series RLC circuit, with a parallel parasitic capacitance Cp. The quality factor (Q) of the crystal oscillator is in the 50,000 range, which provides a very precise frequency. The circuit can be made to oscillate in series or parallel mode. Parallel mode is the preferred mode of oscillation. In parallel mode, the crystal is connected with an inverting amplifier with two load capacitors connected in parallel (C_L), as shown in Figure 2-20. In parallel mode, the crystal oscillator appears as an inductor and oscillates with the load capacitors (C_L). In order to oscillate, the circuit needs to meet the Barkhausen criteria of oscillation. The inverting amplifier, Amp in Figure 2-20, is designed to meet the oscillation criteria. Figure 2-21 shows the design method to meet the oscillation criteria.



a) Negative resistance design circuit

b) Negative resistance simulation result

Figure 2-21 Negative Resistance (R_N)design method to meet the oscillation criteria for crystal oscillator, R_N> ESR

In this circuit, crystal is removed from the oscillator and an *ac* current source is connected across the amplifier terminal, as shown in Figure 2-21 (a). The inverting amplifier presents a negative resistance to the applied *ac* current. The value of the negative resistance is a function of frequency. Figure 2-21 (b) shows the negative resistance of the amplifier with frequency. The negative resistance of the amplifier is an active component and is needed to overcome the damping effect in crystal's ESR in the RLC circuit of Figure 2-20. The ESR of the crystal is an energy dissipating component, and the amplifier compensates for this dissipation through the negative resistance by supplying/replenishing the dissipated energy in the crystal. The Barkhausen criteria for oscillation are met when negative resistance of the amplifier is greater than the ESR of the crystal. As a rule of thumb, the negative resistance of the amplifier should be greater than the ESR by at least three times in magnitude. The ESR of the crystal oscillator at 32.768kHz is typically in the range of 30kΩ. Figure 2-21 (b) shows that the designed amplifier shows a negative resistance of -90kΩ. The start-up time of the crystal oscillator is typically very large (~1s range) because of the high Q of the crystal circuit. The negative resistance of the amplifier also controls the start-up time and, the higher the negative resistance, the faster will be the start-up time of the crystal [19].

Power Consumption

The power consumption of the crystal oscillator is determined by the crystal and the design of the amplifier. The energy dissipating component in the crystal oscillator is the crystal's ESR. ESR dissipates energy in the form of heat loss, as Joule's heating, and is given by I^2R, where R is the value of resistance of the crystal's ESR and I is the RMS (Root Mean Square) current flowing into the crystal. This loss is directly proportional to the amplitude of oscillation. To reduce the loss and hence to reduce the power consumption of the crystal oscillator, the amplitude of oscillation

is often reduced. This can be done by operating the amplifier in the sub-threshold region [14][15]. Recent work applies circuit techniques where the amplitude of oscillation can be reduced by using delay locked loop (DLL) [13] or by simply quenching the oscillation amplitude [15]. These techniques have reduced the power consumption of a 32kHz crystal oscillator to 5.58nW [13], making it possible to use the crystal oscillator for BSNs, where a lower power clock is desired.

In this section we propose a 32kHz crystal oscillator circuit that consumes close to 1nW of power. We first operate the crystal oscillator in sub-threshold at 0.3V V_{DD} to reduce the overall power consumption to 2nW. We further reduce the power by applying a duty-cycling technique to turn-off the amplifier often. This technique brings down the over-all power consumption of the crystal oscillator to 1nW, improving the state of the art by almost five times. This proposed solution is more suitable for BSN applications.

2.3.1 Architecture

In this work, we designed the crystal oscillator operating at 0.3V V_{DD}, in the sub-threshold voltage. The transistor sizes of the amplifier determines the negative resistance and power dissipation; increasing the transistor size increases the negative resistance (R_N), but it also increases power. Decreasing the size makes $|R_N| <$ ESR, failing to meet the oscillation criteria. The low voltage operation at 0.3V VDD provides the proper R_N for the oscillator. The amplifier consumes 5-10nA of quiescent current, which sets the power consumption of the crystal oscillator at 2-10nW.

In order for the oscillator to start, $R_N >$ ESR. The start-up time, the time the oscillator takes to reach the full amplitude, is also controlled by R_N. The higher the value of R_N, the faster will be the start-

up [19]. However, a higher value of R_N means higher power consumption. The amplitude of oscillation saturates after start-up. After the oscillation saturates, the R_N of the amplifier decreases because of the non-linearity in the circuit due to saturation, and effectively R_N = ESR at saturation. The saturation of oscillation creates higher harmonics, resulting in unnecessary power dissipation. While higher power is needed during start-up [19], it is not needed when the oscillation saturates. We propose further improvements in design to save this power.

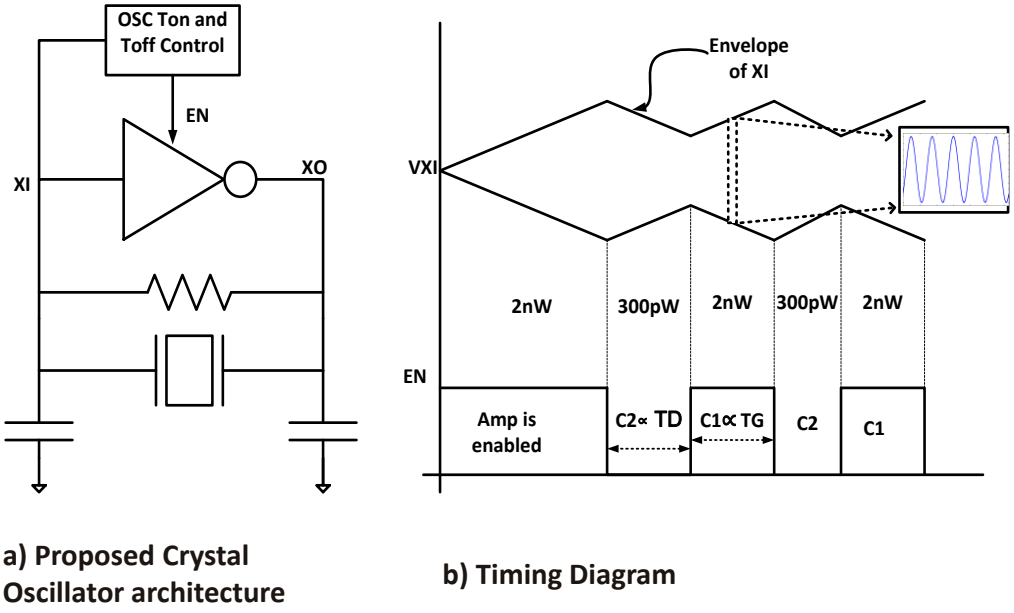


Figure 2-22 Proposed control scheme, where oscillator is turned on and off to save power

The energy of a crystal oscillator is stored in its equivalent inductor and capacitor. After the saturation of oscillation, the stored energy in the crystal's equivalent inductor and capacitor is saturated. After the saturation, if the amplifier is disabled, the oscillation will start decaying, and if we enable it again, it will start growing again. The power consumption becomes negligible when the oscillator is disabled. However, oscillation doesn't die right away and decays slowly, with the

time constant given by ESR and Lm of the crystal. The output of the crystal oscillator is still useful and can be used to provide the clock when it is decaying. Therefore, the power consumption of a crystal oscillator can be further reduced by switching the amplifier. In our design, we switch the amplifier periodically, while keeping the amplitude of oscillation high enough for the receiver circuit to detect the oscillation. Figure 2-22 (a) shows the concept of the control scheme. When the amplifier is disabled, the oscillation at XI will decay with a time constant (TD), which is determined by the ESR and Lm. When the amplifier is enabled, it grows with a time constant (TG), which is determined by R_N –ESR and Lm [19]. For optimal power savings, the amplifier should be disabled for a time proportional to TD, and enabled for a time proportional to TG, as shown in Figure 2-22 (b). A counter running on oscillator output frequency is enabled when the amplitude crosses a set threshold. It counts until C1 and stops when the amplitude crosses a higher threshold. This gives us a digital o/p proportional to TG. Similarly, C2 proportional to TD can be obtained. A clock with the period (C1+C2) is obtained, with C1 as High and C2 as low, as shown in Figure 2-22 (b). The proposed technique enables a calibrated switching of the amplifier of the crystal oscillator and helps in cutting down the power further to 1nW.

2.3.2 Design of Low Power Amplifier

The architecture of the proposed crystal oscillator involved the design of a low power amplifier and control circuit to switch the amplifier periodically. To reduce the power consumption of the crystal oscillator, power at both stages of the design has to be reduced. This section talks about the design of the low power amplifier circuit. Various inverting amplifier architectures can be used to implement the amplifier. A simple push-pull inverter (a digital inverter) with a big bias resistor, as shown in Figure 2-20 (a), is one of the design options and is commonly used because it is single

stage and hence consumes the least power [15]. However, the inverter circuit needs to be designed properly to meet the Barkhausen oscillation criterion. At lower driver strength (smaller sizes for nMOS and pMOS), the negative resistance of the amplifier is lower and cannot meet the oscillation criterion. Increasing the size increases the negative resistance. However, after a certain size, the negative resistance starts decreasing, because of the self-loading in the inverter through the gate-drain capactiance, C_{GD} (miller effect). Also, increasing the size of the inverter increases the power consumption. Therefore, the inverter needs to be sized properly for the power consumption, as well as for negative resistance. Apart from proper sizing, the power consumption can also be reduced by operating the amplifier circuit at lower V_{DD} voltage. At lower V_{DD} voltage, the amplifier can be sized to meet the oscillation criterion. The sizes for lower V_{DD} are typically bigger than the sizes for higer V_{DD}. However, the overall power consumption decreases.

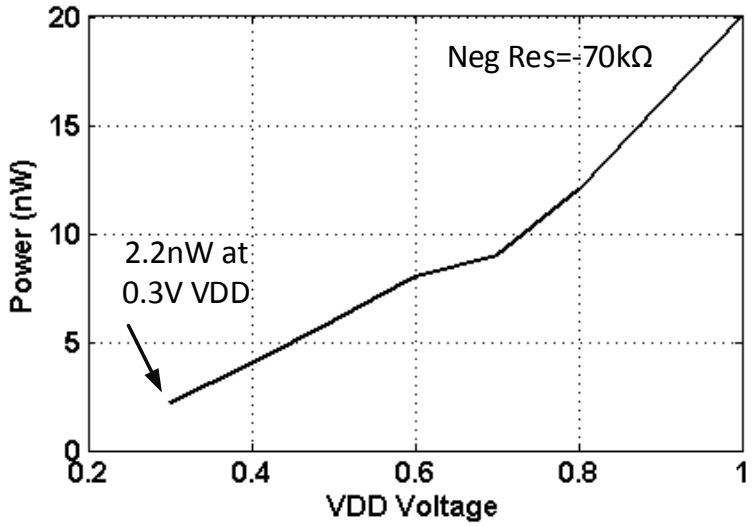


Figure 2-23 Power consumption of the amplifier circuit with V_{DD} voltage for fixed negative resistance of -70k Ω

FFigure 2-23 shows the power consumption of the amplifier circuit designed to provide a fixed negative resistance of -70kΩ at 32kHz for different V_{DD} voltage. The power consumption increases with the voltage almost linearly. This is largely because the bias current of the amplifier almost

remains the same for a given R_N. As a result, power increases because of the increase in the V_{DD}. Therefore, the oscillator needs to be operated at a lower V_{DD} to reduce the power. We designed the inverter to operate at 0.3V V_{DD} and provide -70kΩ negative resistance at 32kHz as shown in Figure 2-23. We used LV_T transistors with longer length to implement the inverter. LV_T transistors give better performance or gain at 0.3V V_{DD}, owing to the lower threshold voltage, while a longer length of the transistor helps in reducing the bias the current.

Process Calibration

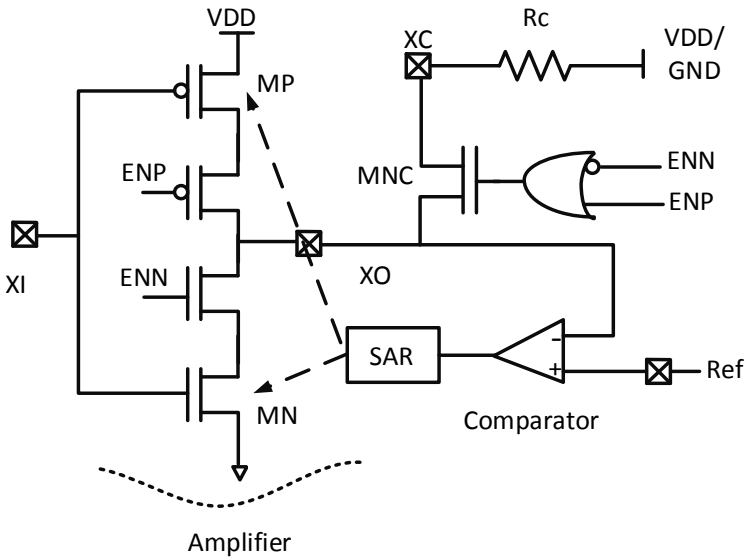


Figure 2-24 Calibration technique for amplifier to address variation effects

The amplifier was designed to operate in the sub-threshold region with a V_{DD} of 0.3V. Owing to the sub-threshold region of operation, the amplifier is sensitive to process variation. As a result, the negative resistance and power consumption of the amplifier can vary a lot. At some process corners, the amplifier can consume higher power and give very high negative resistance, and at other process corners, its negative resistance can be low, and it may fail to meet the Barkhausen

oscillation condition. We propose a calibration method to address this variation. Figure 2-24 shows the calibration circuit. We set the drive strength of the amplifier transistors MP and MN using this circuit. The amplifier is enabled when ENP=0 and ENN=1. For calibration of MN to a given drive strength, ENN and ENP are set to one. This enables the calibration circuit where MN gets connected to an external resistor through the switch MNC. XI is connected to Ref, which is

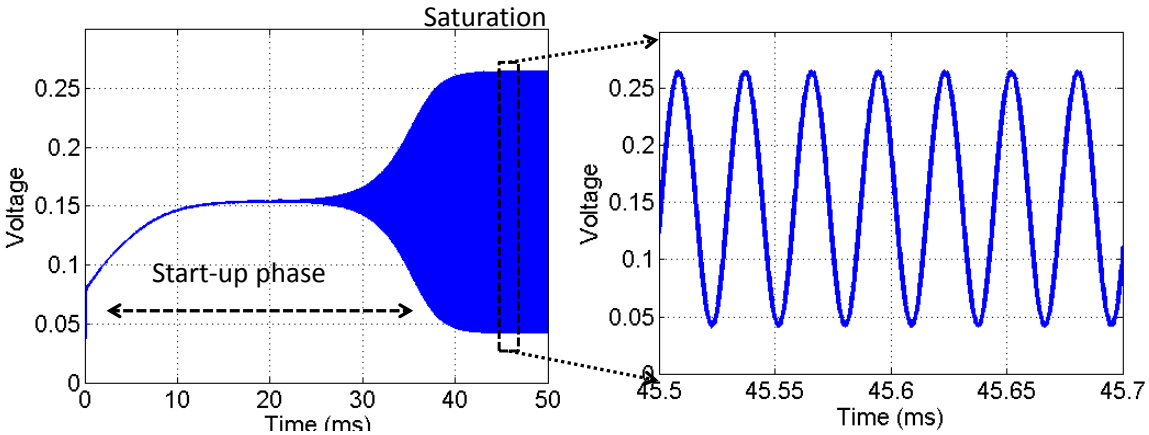


Figure 2-25 Simulation result of the XTAL at 0.3V VDD and consuming 2nW power

selected to be at $V_{DD}/2$. The size of transistor MN is changed using the SAR logic and the comparator in the feedback loop. This happens in the following way. XI and Ref are set to $V_{DD}/2$ and the pull-down path is enabled, while the pull-up path is disabled. The external resistor Rc is connected to V_{DD}. If the size of MN is very big, then it will pull down the XO node below Ref which will cause the comparator output to go low. This low signal tells the SAR logic to reduce the size of the transistor MN. The size of MN is successively approximated, and the method is similar to the one explained in Section 2.2.3 for the on-chip clock source, and it takes 5 clock cycles. This algorithm is like a binary search for the right drive strength of the transistor MN set by the external resistor. This way MN can be sized to the right drive strength. Similarly, MP is sized by setting ENN and ENP to zero and connecting the external resistor to ground. We use a

size of external resistor such that the amplifier can be sized to supply 5-20nA of bias current, which provides enough drive strength to meet the Barkhausen criteria for oscillation. Figure 2-25 shows the simulation result of the oscillator.

2.3.3 Amplifier duty-cycling control implementation

To further reduce the power consumption of the XTAL, the duty cycling technique explained in Section 2.3.1 is implemented. Figure 2-22 shows the control scheme. In this control scheme, the amplifier explained in Section 2.3.2 is periodically turned on and off. When the amplfier is turned-off, the power consumption of the oscillator goes to 0.3nW, and it consumes 2nW when enabled. The oscillation grows when the amplifier is enabled and decays when it is disabled. The amplitude of oscillation during this time is kept high enough for detection. The on time for the amplifier should be proportional to the rate of growth of oscillation (TG). Similarly, the off time of the amplifier should be proportional to the decay of the oscillation (TD). The implementation of the control scheme involves design techniques to obtain the time constants TG and TD.

Obtaining time of growth of oscillation

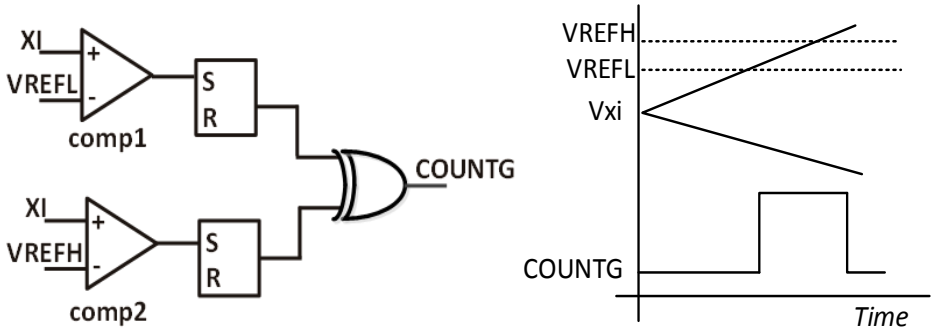


Figure 2-26 Circuit to obtain the time of growth (TG) of oscillation

Figure 2-26 shows the circuit to obtain the TG of the oscillation. It consists of comparators and SR flip-flop. Threshold voltages VREFH=220mV and VREFL=200mV are applied at the negative terminal of the comparator, while XI is applied at the positive terminal. Once oscillation's amplitude goes above VREFL, the output of Comp1 goes high and corresponding SR flip-flop is set. This sets COUNTG to high. A counter is enabled using this signal to count. The amplitude of oscillation keeps on increasing. Once the oscillation crosses VREFH, Comp2 goes high and sets COUNTG to zero. This stops the counter and sets the value of the counter, which is proportional to the growth of oscillation. The value is digital and is stored, while the circuit is disabled to save power. The proposed circuit consumes active power only when the count value is needed.

Obtaining time of decay of oscillation

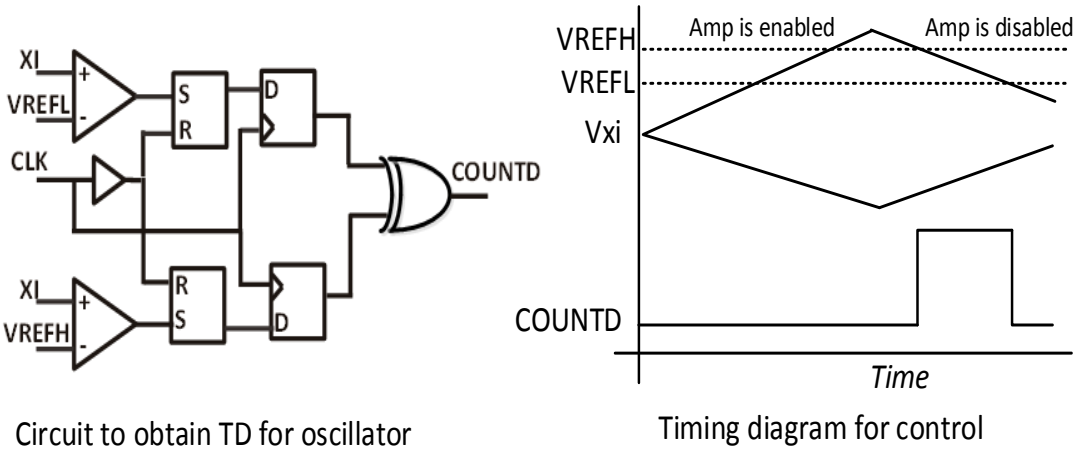


Figure 2-27 Circuit to obtain the time of decay (TD) of oscillation

Figure 2-27 shows the circuit implementation for obtaining TD for the oscillator. The circuit is very similar to the circuit used for obtaining TG. It also enables a counter, which counts when XI is between VREFH and VREFL. While TG is obtained when the amplifier is enabled, TD is obtained when it is disabled. Both TG and TD are stored digitally and their corresponding circuits

are disabled to save power. After obtaining TG and TD, the oscillator control turns on the amplifier for time=TD and turns it off for time=TG. This way, the power consumption is reduced and dutycycled. The total power consumption goes below 1nW. The next section talks about the complete control architecture of the circuit.

2.3.4 Complete circuit implementation

Figure 2-28 shows the complete circuit diagram of the proposed crystal oscillator circuit. First, the calibration of the amplifier is performed, which can be done once after manufacturing. The calibration circuit sets the drive strength of the amplifier and compensates for the process variation.

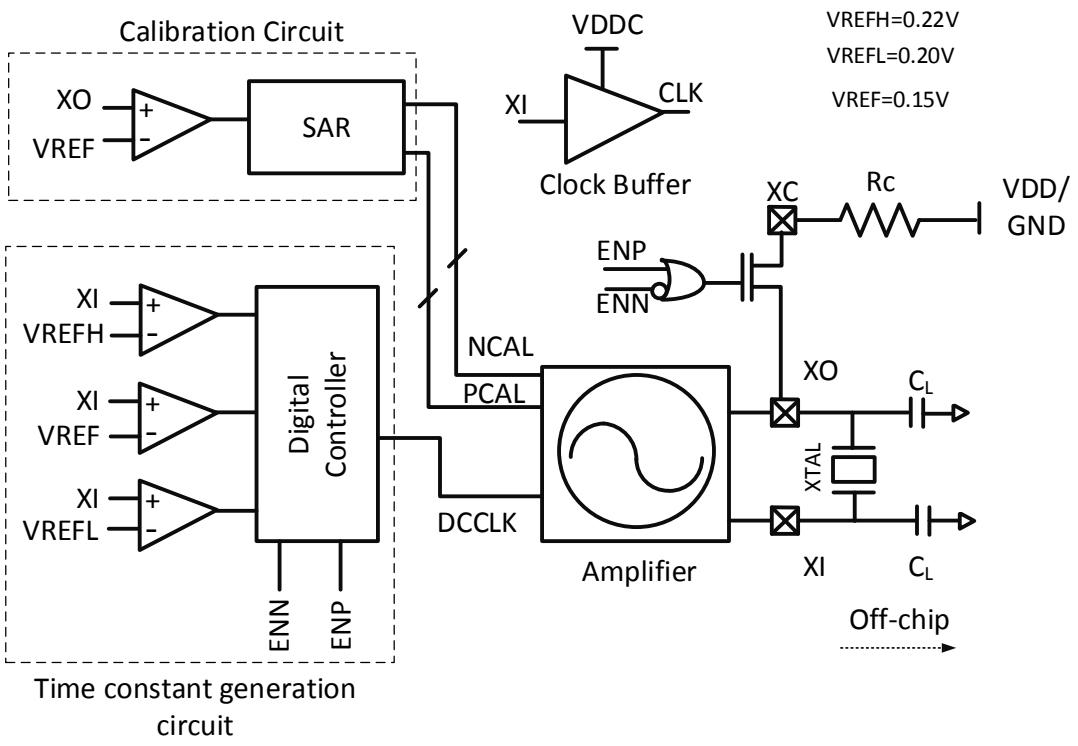


Figure 2-28 Complete circuit diagram of the proposed crystal oscillator circuit

After the calibration, the time constant generation circuit obtains the time of growth (TG) and time of decay (TD) of the oscillator. These time constants are used to configure the clock, (DCCLK) to

switch the amplifier on and off. The duty cycle of DCCLK is determined by TG and TD, with high time=TG and low time=TD. Once the DCCLK is configured, the time constant generation circuit is disabled. Similarly, the calibration circuit is disabled after calibration and all the digital bits are stored. This eliminates the power overhead of the calibration circuit or time constant generation circuit. The power consumption is given by the amplifier with duty cycling. A clock buffer is used to level convert the clock to higher voltage if needed.

2.3.5 Results

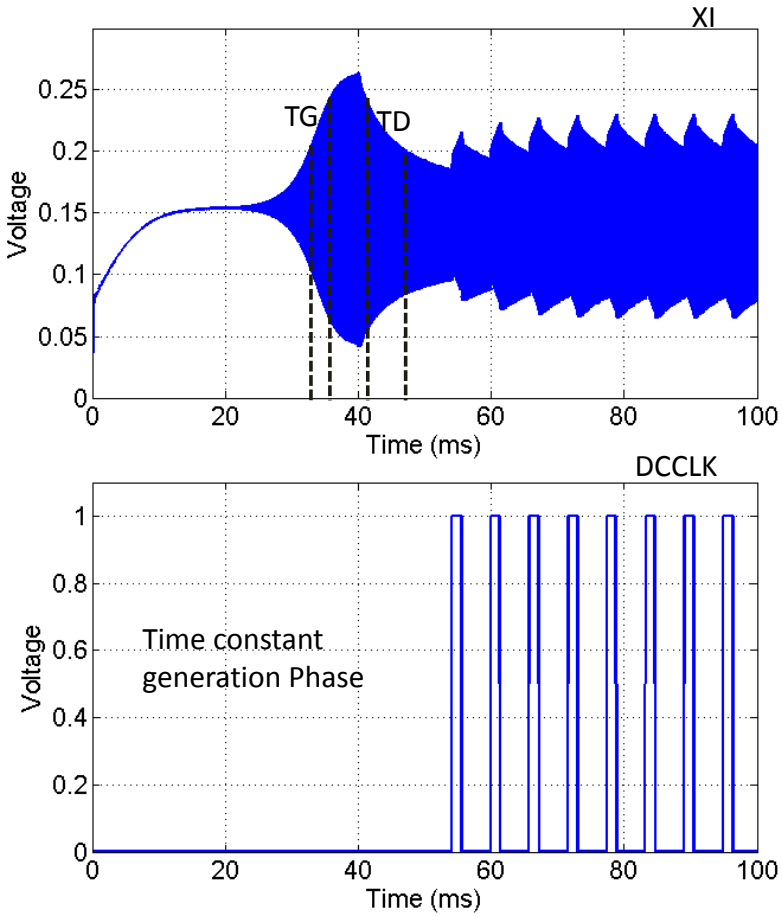


Figure 2-29 Simulation result of oscillator duty-cycling technique

We implemented the crystal oscillator circuit (0.25mmx0.25mm) in 130nm CMOS. Figure 2-29 shows the simulation result of the proposed circuit. Initially, time constants TG and TD are obtained and DCCLK is held low. DCCLK is then configured with a time period of TG+TD with high time of TG and low time of TD. Once DCCLK is configured, oscillation switches on and off and achieves a power consumption of less than 1nW. Figure 2-29 shows that the oscillator's amplitude increases when DCCLK is high and decreases when it is low, achieving the duty-cycling effect in the design.

Table 2-1 Comparison summary of the duty-cycled oscillator with previous low power works

	[13]	[15]	[17]	[18]	This work
Operating Frequency	32kHz	32 kHz	32kHz	2.1MHz	32kHz
Area	0.3mm^2	N/A	25mm^2	0.41mm^2	0.0625mm^2
Power Consumption	5.58nW	22nW	220nW	700nW	1nW
Operating VDD	0.92-1.8V	0.71V	3V	3V	0.3V
Number of Power/Gnd	2/2	1/1	1/1	1/1	1/1
Amplitude of Oscillation	100mV	65mV	N/A	N/A	200mV
Technology	0.18µm	2µm	2µm	2µm	0.13µm

We implemented the crystal oscillator circuit (0.25mmx0.25mm) in 130nm CMOS. Figure 2-29 shows the simulation result of the proposed circuit. Initially, time constants TG and TD are obtained and DCCLK is held low. DCCLK is then configured with a time period of TG+TD with high time of TG and low time of TD. Once DCCLK is configured, oscillation switches on and off and achieves a power consumption of less than 1nW. Figure 2-29 shows that the oscillator's amplitude increases when DCCLK is high and decreases when it is low, achieving the duty-cycling effect in the design.

Table 2-1 shows the comparison summary of the proposed crystal oscillator circuit with previous work. Our crystal oscillator circuit consumes 1nW of power and has an area of 0.0625mm^2 .It has over 5X lower power and 8X lower area compared to [13], which is the lowest reported power crystal oscillator circuit. We also operated the circuit at 0.3V, which is the lowest reported power supply voltage for a crystal oscillator amplifier circuit. The circuit in [13] also uses a DLL based technique and employs two power supplies and two grounds to achieve lower power. Our circuit uses a single power supply. Previously reported work, such as [15] or [16], achieves a power consumption of 22nW and 18nW by reducing the amplitude of oscillation. We reduce the amplitude of oscillation by operating the circuit at 0.3V. The proposed circuit provides a low power, lower area crystal oscillator circuit. It applies lower voltage design in conjunction with a duty-cycling technique to achieve lower power suitable for BSN applications.

2.4 Conclusions

We presented an ultra-low power clock source platform for BSN application. It provides an on-chip and an off-chip oscillator circuit utilizing a crystal oscillator. Proposed circuits utilize low voltage design and duty-cycling technique to achieve lower power. The ULP on-chip clock source uses a 1µW temperature compensated on-chip digitally controlled oscillator (Osc_{CMP}) and a 100nW uncompensated oscillator (Osc_{UCMP}), with respective temperature stabilities of 5ppm/^{o}C and 1.67%/^{o}C. We also presented a fast locking circuit that re-locks Osc_{UCMP} to Osc_{CMP} often enough to achieve high temperature stability. Measurements of a 130nm CMOS chip show that this combination gives a stability of 5ppm/^{o}C from 20^{o}C to 40^{o}C (14ppm/^{o}C from 20^{o}C to 70^{o}C) at 150nW, if temperature changes by 1^{o}C or less every second. The proposed circuit exhibits similar stability to an XTAL with ~7X less power and no off-chip components. We also proposed

a crystal oscillator circuit for a more precise and lower power solution in an off-chip implementation. The crystal oscillator circuit operates at 0.3V, with a power consumption of 2nW without duty-cycling and 1nW with duty-cycling, over 5X lower power and 8X lower area compared to the state-of-the-art. The proposed circuit has the least reported power and power supply for the crystal oscillator operating at 32.768kHz.

Chapter 3

Energy Harvesting and Power Management for ULP Systems

The previous chapter showed the clocking solution for ULP SoCs. The clock source is usually always on and adds to the standby power consumption of the system. The clocking scheme proposed in Chapter 2 provides low power solutions suitable for BSN applications. Another component of standby power consumption in a ULP SoC is the energy harvesting and power management circuit (EHM). While the voltage sources (V_{DD}s) are always needed for the SoC, the energy harvesting circuit also needs to be on to tap into dynamically varying harvesting sources. Further, in order to increase the overall life time of the system, the EHM circuits need to be more efficient and operate at lower output voltage.

ULP SoCs, like BSN, can now operate from harvested energy obtained from ambient sources such as sunlight, ambient light, vibration, RF or the body heat of a human being. These sources provide low energy due to the constrained operating condition. It is vital that the energy be harvested efficiently and managed with minimum loss, in order to enable battery less operation of ULP systems. It is also vital that the energy harvesting and management circuit do not increase the cost or bill of materials (BOM) of the BSN, which can hinder their wide spread deployment. Conventional approaches to obtaining and managing energy from ambient sources either employ

more than one inductor, which increases the cost and bill of material (BOM), or use low drop out (LDO) regulators, which have lower efficiency. The lower efficiency of LDOs can result in the loss of energy, which is not desirable. There is a need to provide an efficient and low cost energy harvesting and power management solution. This chapter proposes a highly efficient energy harvesting and power management solution with various design options. The proposed solution can harvest energy from TEG, and solar cells. It proposes a single inductor power management circuit to provide regulated output voltages for BSN, which helps in reducing the cost of the power-management circuit. It also presents a bandgap reference voltage circuit which operates at lower voltage and consumes lower power than state of the art reference voltage circuits. The lower voltage operation of the bandgap reference circuit enables a lower start-up or power-on voltage for the body sensor node, which helps in increasing the life-time of BSN node.

3.1 Energy Harvesting and Power Management System

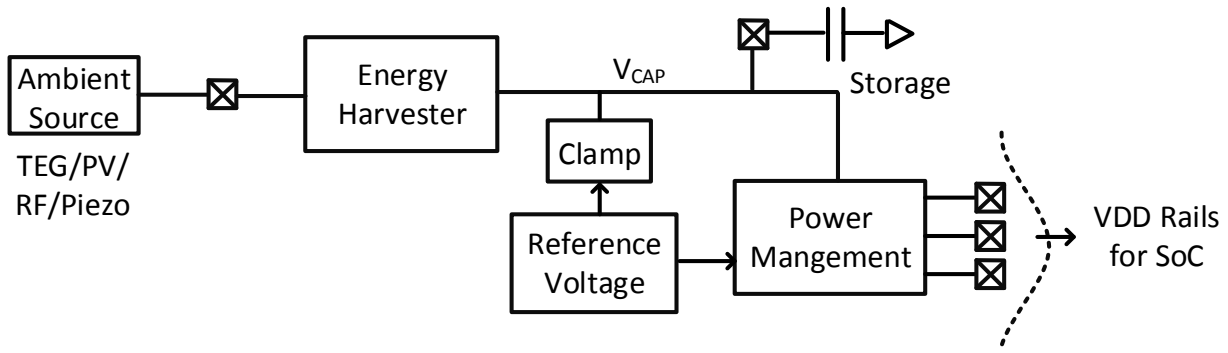
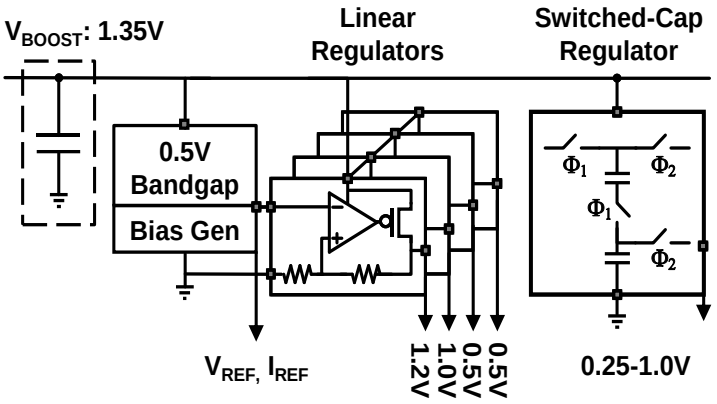


Figure 3-1 Energy harvesting and power management system

Figure 3-1 shows the typical block-level architecture of an energy harvesting and power management (EHM) system for an ultra-low power system such as a BSN. The functioning of such

a system can be broadly divided into two categories; harvesting energy and power management. The system can harvest energy from ambient sources, such as a thermo-electric generator (TEG), solar cell or a photovoltaic cell (PV), RF sources, or vibration, using a piezoelectric harvester. Usually, the harvested energy is stored on a capacitor. The power management circuit then generates multiple meaningful voltages (V_{DD}s) for the SoC. These output voltages are regulated using the reference voltage. The purpose of the reference voltage is to supply a well-controlled absolute reference voltage. The reference voltage is also used to supply the clamp circuit for the energy harvester. The purpose of the clamp circuit is to prevent the output voltage on the storage capacitor from going higher than a set maximum for its reliable operation.

The design and architecture of the EHM system impact the overall operation and lifetime of the BSN. For a longer lifetime of the node, various design and architectural requirements are to be met. For example, the system should be able to harvest energy efficiently at very low levels of output power from the ambient sources. Another requirement is that the system should start-up at lower initial voltage on the storage capacitor. This is limited by the output voltage at which the reference voltage starts-up. A lower start-up voltage on the storage capacitor increases the life time of the node because more energy on the capacitor can be used. The regulated output voltages coming out of the power management circuit should also be efficiently regulated and their loss is to be minimized. The system includes several bias circuitries, including the reference voltage, which consumes quiescent power even in the absence of any load on the SoC. This power is used for the control circuitry in the EHM system. It is very important to reduce the static power consumption for the longer life time. Finally, the cost of implementation of such a system should also be very minimal for its widespread deployment.



Voltage Domain	Blocks Powered
1.2V	Pads, AFE
1.0V	TX LO
0.5V	TX PA
0.5V	DPM, MEM, Accels
SC Reg. (0.25-1.0V)	Accels for DVS

Figure 3-2 Energy harvesting and power management system in a BSN SoC [1]

Figure 3-2 shows the power management block of a state-of-the-art BSN chip [1]. The implementation of each block on the system is not the existing state-of-the-art for that given block. However, the implementation presents all the blocks needed for EHM and is the state of the art solution for the complete implementation of EHM for a BSN SoC. The solution provides an energy harvester, as well as power management, to provide multiple V_{DD} rails for the SoC. It also includes a reference voltage circuit, Bandgap reference for voltage regulation. It uses an inductor based boost-converter circuit to harvest energy from a thermo-electric generator (TEG). The energy harvester can harvest from an input voltage of 20mV or 1-2^{o}C temperature difference on TEG. The Bandgap reference circuit provides a 0.5V reference voltage for power management circuits and for the voltage clamp on the boost converter. It starts at the storage voltage of 0.9V and consumes a power of 200nW. Therefore, the EHM circuit on [1] cannot start before the voltage on the storage capacitor goes to 0.9V. The EHM circuit's standby power consumption is also greater than 200nW. Further, the existing power management solution for the chip includes multiple linear regulators and a switched capacitor regulator to supply different V_{DD} rails. A linear regulator such as an LDO suffers from poor efficiency. The existing power management solution for the

chip includes multiple linear regulators and a switched capacitor regulator to supply different rails. The theoretical maximum efficiency of an LDO cannot be more than V_{DD}/V_{BOOST}. Therefore, more than 63%, 26% and 12% of energy on the V_{DD} rails, 0.5V, 1.0V, and 1.2V gets wasted in obtaining the regulated V_{DD} voltage. There is a need to provide energy efficient solutions for the power management, which can increase the lifetime of the BSN chip. This work proposes a highly efficient energy harvesting and power management solution with various design options for BSNs. It proposes novel circuits for each component of the EHM and improves the state of the art for each one of them.

3.2 Energy Harvesting for Thermo Electric Generator

There are various ambient sources for harvesting energy. However, the following four sources are commonly explored for ULP systems. These are light, vibration, thermal, and RF. Energy harvesting from outdoor sun-light is a well explored research area. Usually, these harvesters are much bigger in size. They are used to harvest large amounts of power (in kWs) at high voltages. These converters achieve high efficiency with very good maximum power point tracking [20]-[22]. Recently, interest in micro-power energy harvesters using solar cells has emerged for their use in ULP systems, such as WSNs or BSNs energy harvesters [23]-[25]. These are used for low power systems. Usually, they are small in size and harvest very low amounts of energy (in μWs), due to the smaller size of the solar cell and low ambient light because of the indoor lighting condition. Another harvester that is commonly suited for BSN application is the piezoelectric harvester, harvesting mechanical energy from vibration. These harvesters can harvest 10-100's of μW of available power [26]. Electrical energy is generated when mechanical stress is applied on a piezoelectric material, which underlines the physics behind energy harvesting. Recently,

piezoelectric harvesters suitable for BSNs have been demonstrated. These harvesters can harvest output powers of a few μW to 100's of μW, at efficiencies above 80% [27]-[29]. Harvesting energy from available RF power is another means of obtaining energy for BSNs. However, RF energy is not true energy harvesting, as RF signals are powered from other sources. Nevertheless, RF can also supply enough energy to power BSNs [30]-[32]. Finally, thermoelectric generators (TEG) can also be used to harvest energy from thermal gradients existing in our surroundings or systems. TEGs have found widespread use in industrial space, where large temperature gradients, such as heat exhausts, are common [33]-[35]. These are usually big in size and harvest energy at the rate of a few 100's of Watt. Smaller TEGs have also been designed to be used for ULP SoCs. One of the application of TEG is harvesting energy for SoCs that are worn by the human body. 1-10^{o}C of temperature difference can exist between a human body and its ambience. We can harvest 100's of μW of available power [36][37]. Recent TEG energy harvesters can harvest energy from very low temperature difference, usually 1-2^{o}C, resulting in an input voltage of less than 50mV [38]-[41]. In this chapter, we present an energy harvester using a TEG that can harvest from 10mV input voltage. We also present a control scheme for improving the efficiency of the harvester. We will first explain the functioning of a thermo-electric generator and then dive into the design details of the extraction circuit.

3.2.1 Functioning of TEG

A thermoelectric generator converts the thermal energy arising from the difference in temperature between two conductors into electrical energy and vice-versa. The physics behind the thermoelectric phenomenon is the Seebeck effect. The Seebeck effect is the production of an electromotive force (emf) and, consequently, voltage or current between two dissimilar conductors,

when their junctions are maintained at different temperatures. The conductors can be metals or semiconductors and they need not be solid. Apart from generation of emf, thermo-electrics are also used for measuring temperature, as well as for heating or cooling. When electricity is passed through the junction of two different conducting materials, heat can either be generated or taken away (cooling). This effect is called the Peltier effect. Similarly, if a temperature difference exists between two metals, the amount of electromotive force generated is proportional to the difference in temperature. By measuring the produced voltage or current, the temperature can be measured.

The thermoelectric materials used for generating electricity need to be good conductors of electricity, as a scattering effect can generate heat on both sides of the barrier. Also, the material needs to be a poor conductor of heat; otherwise, the temperature difference that must be maintained between the hot side and cold side produces large heat backflow. Materials which optimize these electrical and thermal properties fit the bill. The highest performance has been shown by heavily doped semiconductors, like Bismuth-telluride or Silicon-Germanium [42]. The semi-conductor material also needs to form a base on which both n-type and p-type semiconductor can be generated. Segments of p-type– and n-type–doped semiconductor materials, such as suitably doped bismuth telluride, are connected together to form an electric circuit. The shunts are made of an excellent electrical conductor, such as copper. A voltage drives a current through the circuit, passing from one segment to another, through the connecting shunts. For determining efficiency, this configuration is equivalent to the electrons passing directly from one thermoelectric material to the other. Conventional thermoelectric cooling/heating modules are constructed of thermoelectric segments repeated many times, and organized into arrays such as the one shown in Figure 3-3. When current flows within the module, one side is cooled and the other is heated. If the current is

reversed, the hot and cold sides reverse also. The geometry for power generators (Figure 3-3) is conceptually the same. In this case, the top side is connected to a heat source and the bottom to a heat sink. Thermoelectric power generators often are similar in physical form to cooling modules, except that fewer taller and thicker elements are used.

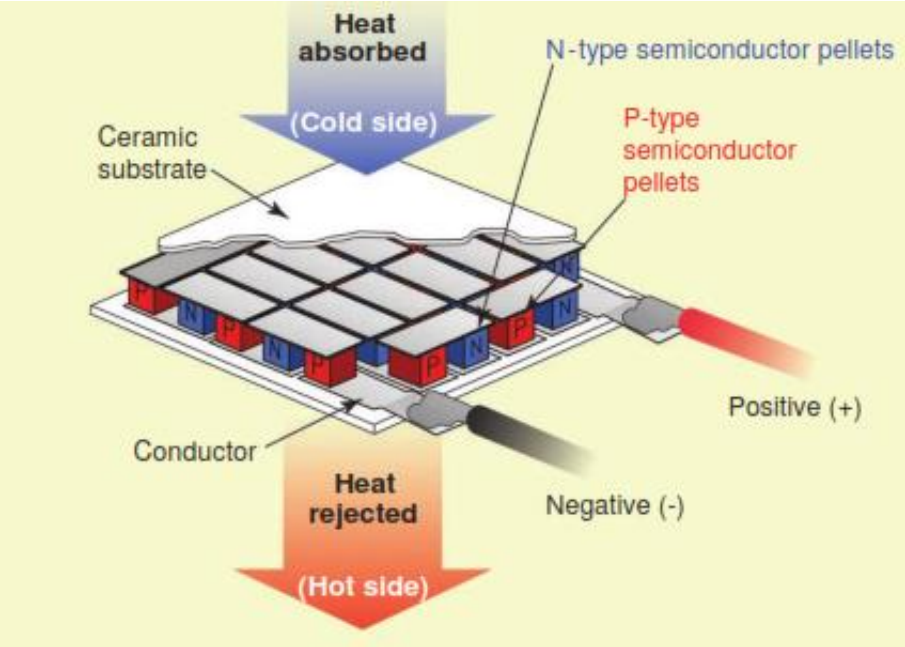


Figure 3-3 Practical Thermoelectric generator connecting large number of *pn* junction to increase the operating voltage [42]

The Seebeck effect in the semiconductor material creates a flow of excess electrons from the hot junction in the n-type material to the cold junction. In the p-type material, holes migrate toward the cold side, creating a net current flow in the same direction as that of the n-type material. The measure of the performance of the material used in TEG is the Seebeck coefficient, defined as the change in voltage per degree of temperature change.

$$\boldsymbol{S = \frac{dV}{dT}} \tag{3.1}$$

Since heat flows from the top to the bottom, all of the thermoelectric legs are thermally connected in parallel. In the power-generation mode, heat flowing from the top to the bottom drives an electric current through an external load. The voltage obtained at the output of the thermal harvester is proportional to the temperature difference across the thermoelectric element. For body-worn devices, the temperature difference is very small and an output voltage of few mV - 50mV is all that can be produced using a $10cm^2$ thermal harvester. The energy harvester should be able to harvest energy from such low input voltages. Several circuit design challenges had to be overcome to be able to harvest from such low voltages. In this chapter, we present a TEG harvester that can harvest from an output voltage of 10mV and above.

Electrical Characteristics of TEG

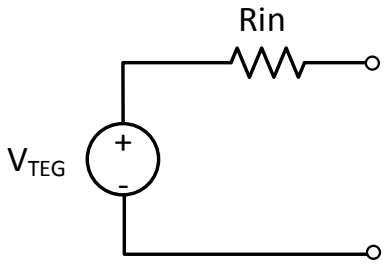


Figure 3-4 Equivalent circuit of a thermoelectric generator

The thermoelectric generator can be modeled as a voltage source in series with an input resistance [43][44]. Figure 3-4 shows the equivalent circuit of the TEG. The open circuit voltage V_{TEG} is directly proportional to the temperature difference between the hot and cold sides, and is given by,

$$\boldsymbol{V_{TEG} = S\Delta T} \tag{3.2}$$

where S is Seebeck coefficient given by equation (3.1), and ΔT is the temperature difference between the hot and cold sides of TEG. Commercial TEGs use semiconductor material bismuth

telluride due to its good electrical conductivity and poor thermal conductivity [42]. The Seebeck coefficient of an n-type bismuth telluride material is -287μV/K at 54°C. The lower voltage coming out of one TEG cell requires that multiple cells be used in series to increase the output voltage, as shown in Figure 3-3. Connecting more cells in series increases the input resistance of the TEG and can reduce the efficiency. Also, a smaller size TEG is needed for body-worn devices. Therefore, the output voltage of the TEG can be very small, at times a few mV only. This chapter presents a design to harvest energy from such low output voltages in TEG material.

Maximum Power Point in TEG

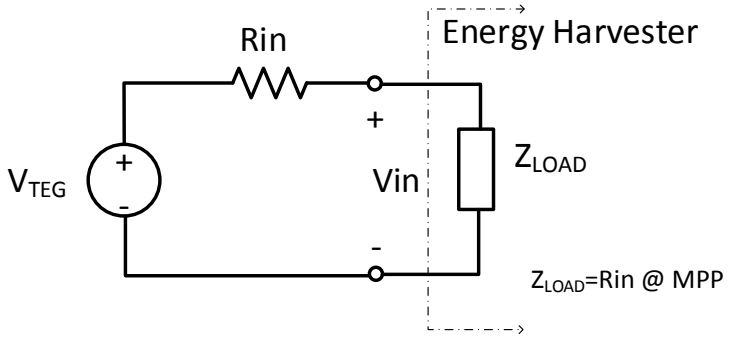


Figure 3-5 Energy harvester harvests maximum energy when impedance of the harvester matches TEG's input resistance

Figure 3-5 shows the condition when a harvester is connected to the TEG. The harvester will present a load with output impedance Z_{LOAD} to the TEG. The power drawn from TEG is dependent on the value of the Z_{LOAD}. When Z_{LOAD} is very high, the current drawn by the harvester will be very small and so the output power will be small. Similarly, if the Z_{LOAD} is low, output voltage will be small and, consequently, the output power will be small. From basic electrical engineering, we know that the maximum power will be delivered to the load when,

$$Z_{LOAD} = Rin \tag{3.3}$$

Figure 3-6 shows the output characteristics of an energy harvester connected to TEG. It shows the output power and output voltage as functions of load current. The output power peaks and a maximum power point exists for the load. The maximum power point happens when the load matches the input resistance Rin by satisfying equation (3.3). At this operating condition, the output voltage Vin in Figure 3-5 is given by,

$$Vin = V_{TEG}/2 \tag{3.4}$$

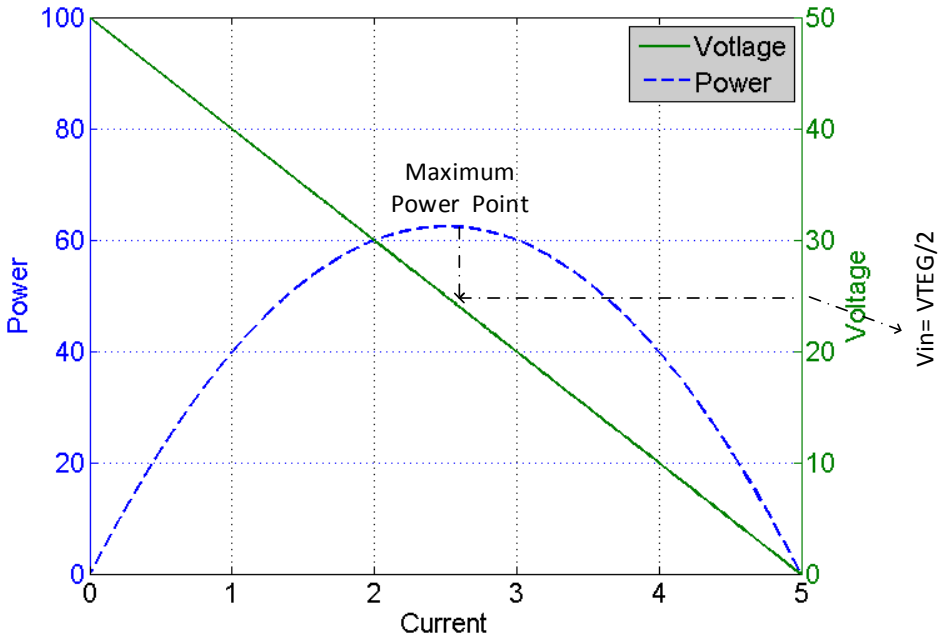


Figure 3-6 Maximum power point characteristics of a TEG energy harvester

The ambient condition in which a thermoelectric generator operates is dynamic. For example, the temperature difference between the hot side and the cold side in a TEG can change. This can lead to a change in the open circuit voltage of the TEG. As a result, the maximum power point (MPP) of a TEG is a dynamic quantity that changes with time. The energy harvester should always track

and operate at the maximum power point to maximize the harvested energy. In the proposed solution, we present a maximum power point circuit that continuously tracks and always operates the energy harvester at the MPP point.

3.2.2 Design of the TEG Energy Harvester

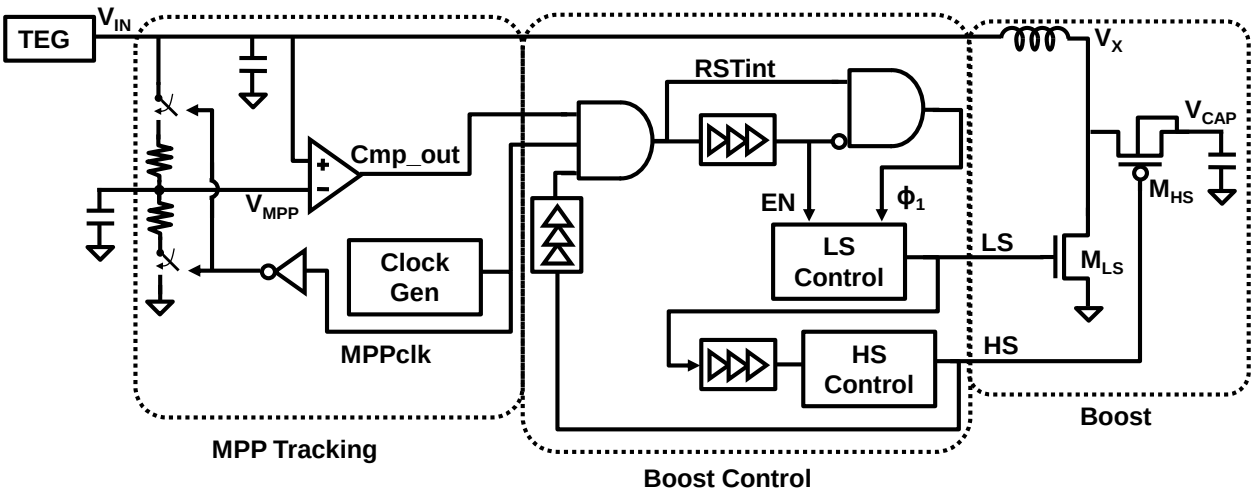


Figure 3-7 proposed design architecture for the TEG harvester using a boost converter.

Figure 3-7 shows the architecture of the proposed energy harvester for TEG. It uses a boost converter to harvest energy. The boost converters are switching mode power converters and they operate on the following basic principle [45]. Referring to Figure 3-7, first, the signal LS goes high and transistor M_{LS} is turned on. This connects the inductor between TEG and ground. As a result, the current in the inductor starts rising and starts storing energy. It obtains its energy from TEG. After a well-defined time, LS is brought down to ground, and M_{HS} is turned on. Now the stored current in the inductor discharges on the capacitor and raises the voltage of V_{CAP}. This switching pattern repeats over and over to charge the output voltage to a higher voltage. The above

description of the operation of the boost converter is very basic, and a more detailed description of the proposed converter in the context of the challenges for low voltage TEGs will follow in succeeding sections. However few important design topics can be introduced here for the reader.

In the ideal case, the energy that is taken from the TEG should be stored on V_{CAP} without loss. However, this is not possible in a practical system, and some energy losses are involved. The efficiency of the converter, defined as the ratio of power delivered to the load to the power obtained from the source, is the measure of the performance. Some of the losses that are involved are explained as follows. The switches M_{LS} and M_{HS} have finite resistance, and they carry current during the switching cycle. As current flows through a resistor, conduction loss takes place in the form of Joule's heating in the switches. Also, the switches M_{LS}, M_{HS} and other circuits in the converter, switch in a periodic fashion to harvest energy. This switching also involves energy loss and is termed simply as switching loss. Finally, various bias current circuits are needed to implement the control of the converter. This results in power loss that is always present and is called static loss. In order to maximize the efficiency of the converter, all these losses are to be minimized. Finally, maximum power can be harvested from the TEG when the efficiency of the boost converter is at its maximum, and the boost converter's operating point is always the maximum power point of the TEG.

The proposed architecture of Figure 3-7 has three components. It consists of an MPP tracking circuit to operate the converter at the maximum power point. The second component of the design is the boost converter. The boost converter is designed to have maximum possible efficiency for the given operating condition, while the MPP tracking circuit tracks the MPP point of the TEG

and operates at that point. The next section talks about the architecture of the MPP tracking scheme. The section after that, talks about the design of the boost converter control circuit.

Maximum Power Point Tracking Circuit

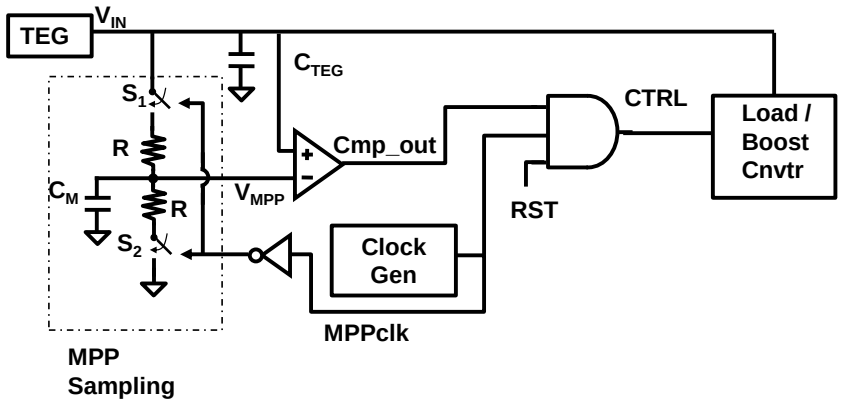


Figure 3-8 Maximum power point tracking circuit for TEG

Figure 3-8 shows the maximum power point tracking circuit for the energy harvester connecting to the boost converter. It consists of an MPP sampling circuit, a comparator and a clock generator. The clock generator generates a clock with periods of 150ms, which is fast enough to track the slow changing ambient condition, as well as the leakage of the V_{MPP} capacitor. This clock is used to generate a pulse that goes low for 10ms shown in Figure 3-9. 10ms is large enough time to charge a 10nF cap using a 100kΩ resistor. When this pulse goes low, the boost converter is disabled and, as a result, the load current goes to zero. Since no load is connected to the output of TEG, the TEG voltage goes to its open circuit voltage V_{TEG}. This pulse is also used to close the switches S_1 and S_2, as shown in Figure 3-8. The two resistors get connected to the TEG voltage and the V_{MPP} node goes to the voltage $V_{TEG}/2$ through the resistor divider. Therefore, the capacitor C_M gets charged to $V_{TEG}/2$. The output voltage of the V_{MPP} node is maintained by the cap C_M. The

MPP sampling circuit samples the half of the TEG's open circuit voltage and stores it on the cap. After the pulse goes high again, the boost converter starts drawing the current from the TEG. As it draws current from the TEG, the voltage level of *Vin* will start decreasing. The boost converter increases the current drawn from the TEG source by increasing the frequency of switching. As long as the output of the comparator is high, the boost converter switches at higher frequency and the current drawn from the TEG source is high.

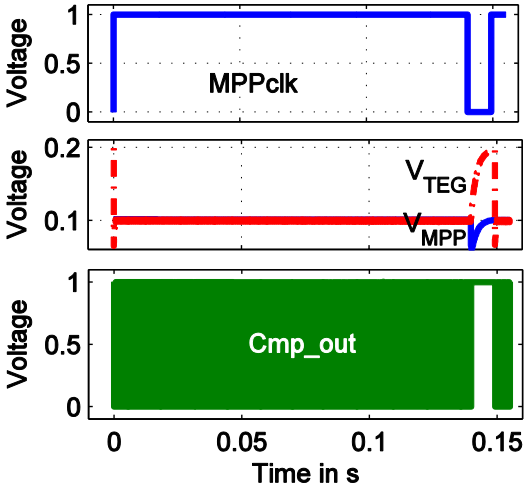


Figure 3-9 Simulation Result of MPP tracking circuit showing

Figure 3-9 shows the simulation result of the MPP tracking circuit. As the current is drawn, the output voltage of TEG goes low, and eventually reaches V_{MPP} value, which is set to $V_{TEG}/2$. As it crosses V_{MPP} value, the comparator output goes low and the boost converter is disabled. As the boost converter is disabled, the *Vin* voltage will start going higher and it will go above V_{MPP}. At this point, comparator output goes higher and the converter is enabled again. This way the output voltage of TEG is maintained at $V_{TEG}/2$, which is the maximum power point of the circuit given by the equation (3.4). The output voltage of the TEG is maintained at its maximum power point by the control circuit with a voltage ripple around it. The amount of ripple is a function of the

capacitor connected at TEG. The ripple can be made negligibly small by connecting a large capacitor. We use 5µF cap at the output. This way the circuit is maintained at its maximum power point. The output voltage is sampled frequently using the clock, which helps keep track of the TEG's open circuit voltage to account for the dynamic changes in the operating condition.

3.2.3 Control Circuit for Boost Converter

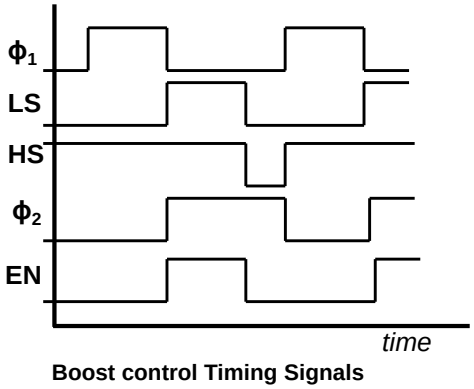


Figure 3-10 Timing diagram of the control signal for the boost converter showing use of two phases ϕ1 and ϕ2, where ϕ1 is used for cancelling mismatch to harvest at low voltage

The boost converter design involves charging of the inductor current and storing it on the capacitor on V_{CAP}. The signals LS and HS, as shown in Figure 3-10, are used to accomplish this switching. The signal LS goes high to turn on M_{LS} transistor in Figure 3-7. This starts charging the inductor current. After a well-defined time, which sets the inductor peak current, the inductor current is discharged on the capacitor, raising V_{CAP}. This is done when HS goes low, as shown in Figure 3-10. Usually, LS and HS signals are controlled to control the performance in a boost converter. However, the proposed boost converter is designed to harvest energy from very low input voltage, such as 10mV. The effect of mismatch or non-idealities in the circuit needs to be addressed if energy is harvested at low voltage levels. The mismatch between the threshold voltage

of two transistors can itself be as high as ~50mV. It is not possible to harvest energy at low voltages if the mismatch between the devices in circuits such as the comparator is not compensated. Therefore, the energy harvesting control scheme is broken down into two phases. In phase one, designated by control signal $\phi 1$, the mismatch throughout the design is compensated for. Phase one is followed by phase two $\phi 2$, which includes control and generation of signals LS and HS. Figure 3-10 shows the timing diagram. We will now explain the circuits needed to control the LS and HS signals.

Low Side (LS) Control Scheme: Peak Inductor Current Control

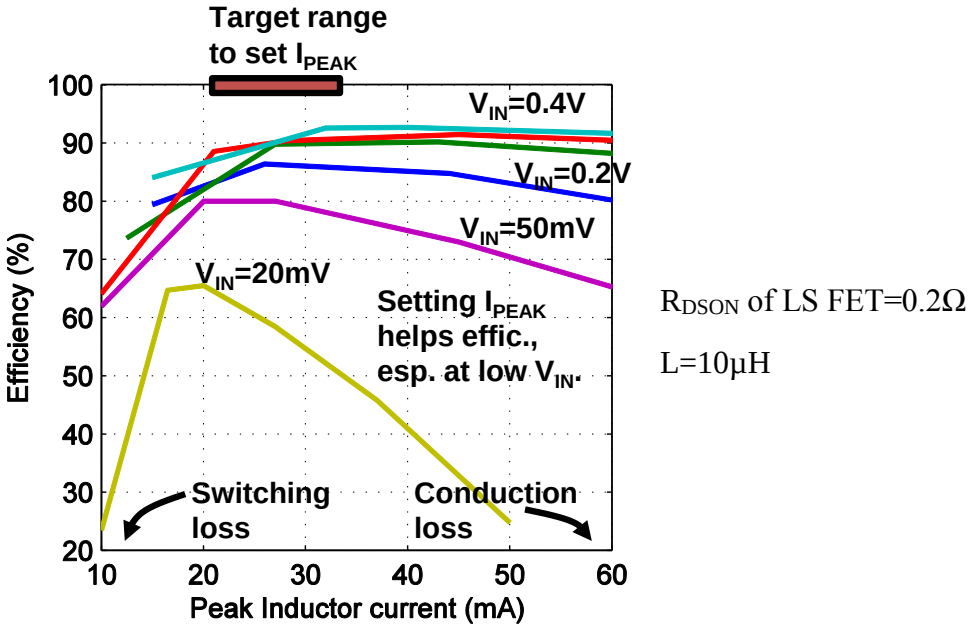


Figure 3-11 Efficiency variation with peak inductor current for various input voltages

The low side control signal (LS) controls the amount of energy harvested from TEG. During the time when LS is on, the inductor current increases and reaches peak value, I_{PEAK}. The value of the peak current depends on the on-time of the LS switch M_{LS}. The longer the on-time, the higher the

peak current would be. For micro-power design, all the inductor current is discharged into the storage capacitor on V_{CAP}. So, the energy transferred from TEG in each cycle is given by,

$$\boldsymbol{E = 0.5 * LI_{PEAK}^2} \tag{3.5}$$

Losses are involved when a transfer of energy happens. These are switching and conduction loss. The conduction loss is dependent on I_{PEAK}. The efficiency of the converter greatly depends on the value of I_{PEAK}. Figure 3-11 shows the variation of the efficiency with I_{PEAK} for different input voltages. At lower value of I_{PEAK}, the switching loss in the converter dominates and lowers the efficiency. This happens because the energy transferred, given by equation (3.5), is small compared to the switching loss. At higher values of I_{PEAK}, the conduction loss increases greatly to reduce the efficiency. There are values of I_{PEAK} where the efficiency can be maximized. Therefore, it needs to be well-controlled (See Appendix B for analytical details).

It is a common practice, in switch mode power supply design, to control the peak inductor current for maximizing efficiency (See Appendix B). In the conventional approach, the resistance of the MOS transistor is used to measure the peak inductor current. The drop across the LS transistor $M_{LS,}$ when the inductor is on, is the representation of peak inductor current. However, this method is sensitive to mismatch and can result in ±20-40% error in the peak inductor current [46]. Also, this method consumes higher power, which can reduce the efficiency by more than 3% [46]. Usually, LS is turned on for a fixed time [38][39] to control the peak inductor current. This method is not expensive in terms of power. However, the efficiency can be reduced because the inductor current is not controlled. Also, the process variation can result in a variation of the peak current further impacting the efficiency of the converter. We propose a low power control scheme to control the peak inductor current. The proposed control scheme is one of the first implementations

of peak inductor control for micro-power harvesters. The proposed scheme has very small dependence (±2.5%) because of the mismatch between the devices. We also propose means to control the process variation or voltage variation.

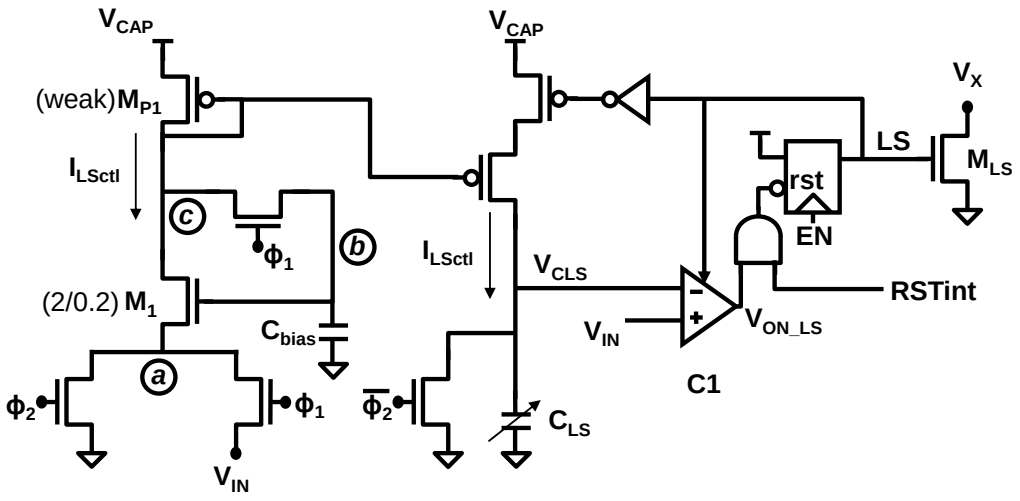


Figure 3-12 LS control circuit to generate the constant peak inductor current

Figure 3-12 shows the circuit that is used for generating constant peak inductor current. The circuit generates the timing for LS signal. The value of the peak inductor current can also be programmed by this circuit. It uses phase 1 and phase 2 of the switching cycle to generate the timing for LS. The functioning of this circuit is explained with the help of the following timing diagram.

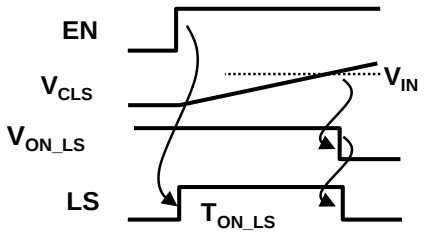


Figure 3-13 Timing diagram for LS control circuit

The circuit operates in the following manner. During phase ϕ1, node *a* is connected to V_{IN}, which the output voltage of TEG, V_{CLS} is held to ground and comparator C1 is disabled. The output of

LS is set to ground. The transistor M_{P1} is made weak, which sets the output voltage of node *b* and is given by $V_{IN}+V_{TM1}$, where V_{TM1} is the threshold voltage of the transistor M_1. Weak M_{P1} drives M_1 very close to its threshold voltage. In phase ϕ2, node *a* is connected to ground, while the connections between *b* and *c* are removed. The transistor M_1 is designed to be in saturation and sets the current I_{LSctl} which is given by,

$$I_{LSctl} = k * (V_{IN} + V_{TM1} - V_{TM1})^2$$

$$\boldsymbol{I_{LSctl} = k * (V_{IN})^2} \tag{3.6}$$

The current generated for LS control is made proportional to the square of the input voltage. It is used for the generation of LS timing. This current is mirrored to charge the capacitor C_{LS}. As ϕ2 goes high, the capacitor starts charging. The timing of LS is given by the charging of the capacitor. Once ϕ2 goes high, LS goes high and the capacitor starts charging. Once the capacitor C_{LS} crosses V_{IN}, output of the comparator C1 goes low, which resets the flip-flop and brings LS to ground. Figure 3-13 shows the timing diagram for the generation of LS. The timing of LS is given by,

$$I_{LSctl} = C_{LS}\frac{dv}{dt}$$

as the capacitor charges from 0 to V_{IN}.

$$T_{ON\_LS} = C_{LS}\frac{V_{IN}}{I_{LSctl}}$$

Using equation (3.6), we get

$$\boldsymbol{T_{ON\_LS} = \frac{C_{LS}}{kV_{IN}}} \tag{3.7}$$

This is the time for which the inductor is kept on. It increases as V_{IN} decreases. Now, let us find out how the peak inductor current is obtained. Assuming negligible drop across M_{LS}, we can write the basic equation for inductor,

$$L\frac{di}{dt} = V_{IN}$$

The inductor current charges from 0 to I_{PEAK} during the time LS is on.

$$So, \qquad I_{PEAK} = \frac{V_{IN}T_{ON\_LS}}{L}$$

Using equation (3.7), we get

$$\boldsymbol{I_{PEAK} = \frac{C_{LS}}{kL}} \tag{3.8}$$

Equation (3.8) gives the formula for peak inductor current. The proposed circuit reduces it into a very compact form. The expression shows that the I_{PEAK} is independent of V_{IN} and V_{CAP} voltages. It depends on the value of the capacitance C_{LS} and the inductor value *L*. By controlling the value of C_{LS}, peak inductor current can be set to a constant value, which gives the maximum efficiency, as shown in Figure 3-11. The constant *k* in the expression is a function of process and temperature. As a result, the peak inductor becomes a function of variation in process. The capacitor C_{LS} and the inductor *L* are the design components. They can be changed to compensate for the process variation. Often, it is not practical to change the value of inductance, either because of the cost involved or because of the size, as it is an off-chip component. However, the capacitor is on-chip and can easily be controlled. Therefore, we propose to address the variation using the capacitor C_{LS}. We use 5 bit binary control on the capacitor to address the process variation. Figure 3-14 shows the simulation result for the peak inductor current at different values of V_{CAP} and V_{IN}. Simulation shows that the circuit shows very small dependence on V_{CAP} or V_{IN}. The peak current value decreases at lower values of input voltage V_{IN}. The capacitor C_{LS} can be trimmed to increase the peak inductor current. The inductor current can also saturate at lower V_{IN} voltages. The switch

resistance has to be small to avoid this. Also, the peak inductor current should be reduced to avoid saturation if it doesn't reduce the efficiency (see Figure 3-11).

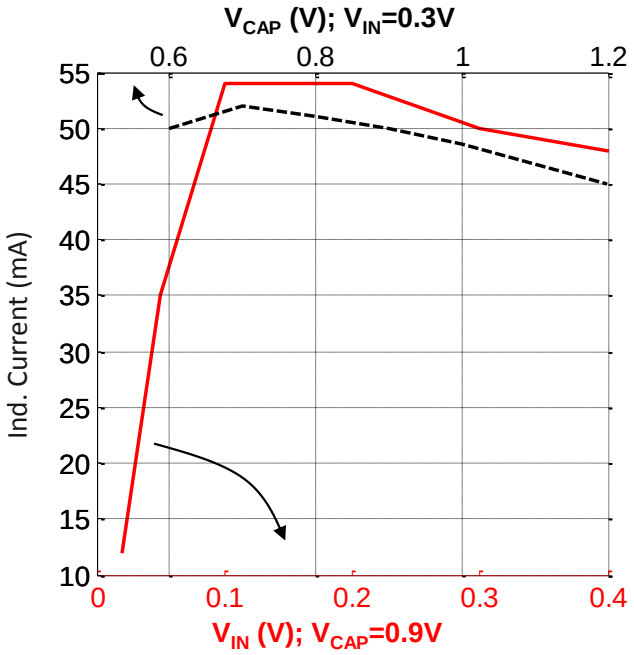
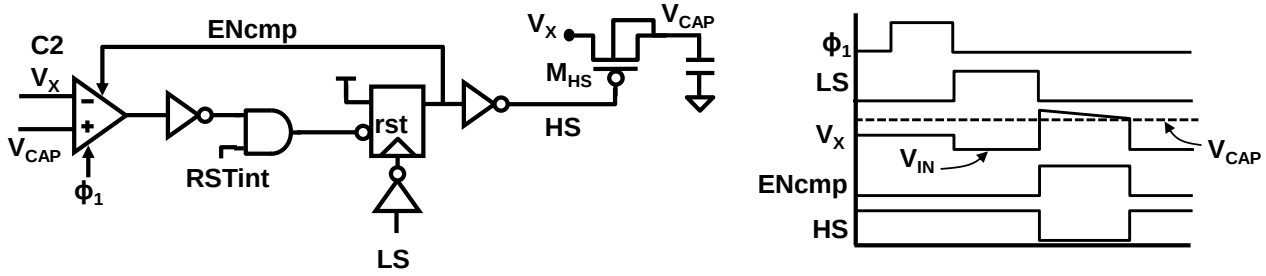


Figure 3-14 Simulation result of peak inductor current with V_{IN} and V_{CAP}

High Side (HS) Control Scheme: Zero Detection

The previous section shows the method to generate a set peak inductor current to maximize the efficiency. Boost conversion also requires the transfer of this energy stored in the inductor to the capacitor on V_{CAP} shown in Figure 3-7. This is achieved by controlling the high side switch of the converter. The HS switch needs to be well-controlled to achieve better efficiency. The HS conduction happens in the following way. Once the inductor has charged to I_{PEAK}, the HS signal goes low and the transistor M_{HS} turns on. The inductor current starts discharging on to the capacitor. At this point, the node V_X goes above V_{CAP} to satisfy the conduction. As the capacitor charges the inductor current reduces and the V_X voltage drops. The inductor current eventually

goes to zero and V_X becomes equal to V_{CAP}. The switch M_{HS} needs to be turned off at this point or the inductor current reverses direction and starts taking charge away from V_{CAP}, which will reduce the efficiency. Similarly, if the switch is turned off before the inductor current goes to zero, the remaining current discharges through a high impedance diode, which also hurts the efficiency. Therefore, an inductor current's zero crossing needs to be detected for accurate timing. This is usually termed as zero detection. Figure 3-15 shows the circuit for generating the HS timing using the zero detection. Comparator C2 is used and it compares the V_X node with V_{CAP}. Once V_X crosses V_{CAP} and goes below it, the comparator output goes low and turns off the switch M_{HS}. The previous works on micro-power converters have considered comparator-based zero detection very high power [38][39]. They do not implement it and instead use a correction technique for zero crossing. In this work, we present the comparator based zero detection scheme as shown in Figure 3-15. There are several challenges involved in designing this for a micro-power converter. We address these challenges by proposing new circuit architectures for the comparator block.



a) Circuit diagram of HS Control

b) Timing diagram for HS Control

Figure 3-15 Circuit to generate the HS timing using zero inductor current crossing

The HS signal is generated using the zero detection comparator C2, by monitoring the node V_X as shown in Figure 3-15. The design of the comparator plays a very important role in zero detection.

Several issues need to be addressed. First, the performance of the comparator needs to be very good. If the delay through the comparator is high, the exact timing of HS control cannot be met. Second, the power consumption of the comparator needs to be small, as it will add to the loss in the boost converter. Finally, the mismatch between the devices inside the comparator can result in high offset which can alter the zero detection. This is particularly critical for harvesting from very low input voltage, as offset itself can be much higher than the input voltage, V_{IN}. Therefore, the offset due to mismatch needs to be cancelled. This work proposes a comparator that addresses all the above issues.

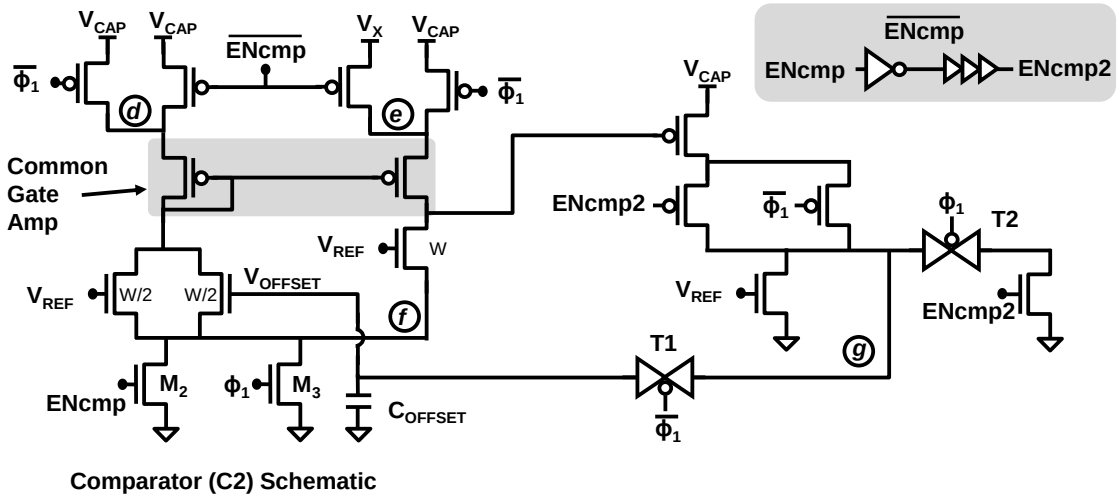


Figure 3-16 Schematic of zero detection comparator with offset cancellation scheme

Figure 3-16 shows the circuit diagram of the zero detection comparator. It uses a common gate amplifier, which is biased at 20µA of quiescent current. The use of a common gate amplifier provides very good performance. However, if this comparator is always on, then the static power of the boost converter will become high and it will result in very low efficiency at low input voltages of V_{IN}. The comparator is duty-cycled to address this. It is turned on only when the switching happens. For example, during MPP tracking the switching happens at low frequency.

Every time a switching cycle is activated through the MPP comparator of Figure 3-7, the zero detection comparator is turned on, and it is turned off after the completion of zero detection. Therefore, the comparator is on only during the switching cycle and its power consumption is the component of the switching loss. The power overhead because of the zero-detect comparator is greatly reduced. It reduces the efficiency of the converter by ~2% at V_{IN} of 10mV and by ~0.3% at V_{IN} of 100mV.

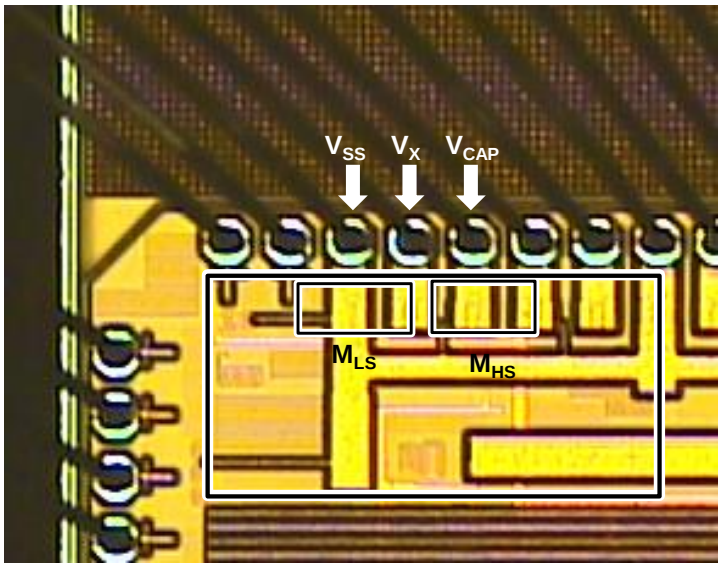
While the performance and power issues are addressed as explained above, the circuit also addresses the offset issues. The offset in the design is cancelled in phase ϕ1 of the switching cycle. It works as follows. In ϕ1, nodes *d* and *e* are set at V_{CAP} while *f* is set at V_{SS}, and switch *T1* is turned on while *T2* is off. The feedback from node *g* sets V_{OFFSET} to remove offset in the comparator. If there is no offset in the design, $V_{OFFSET}=V_{REF}$. The measured comparator offset after compensation was <1mV. The other comparators in the converter use a similar offset compensation circuit. After offset compensation, zero detection is performed. Once LS goes low, the comparator is enabled in phase ϕ2. Node *d* is connected to VCAP while *e* gets connected to V_X and switch *T1* is turned off while *T2* is on. The comparator is configured to normal operation. As inductor current decreases, the node V_X starts going down. Once V_X crosses V_{CAP}, the common gate amplifier changes state and comparator output goes low, which turns off M_{HS}. The higher performance and offset cancellation method ensures correct zero detection. The measured V_X waveform (Figure 3-22 in Section 3.2.3) shows no overshoot or undershoot at t1 indicating ideal zero detection, which confirms that the HS timing is correctly turning off MHS when $I_L=0$.

Start-up in the boost-converter

The boost converter circuit needs a start-up voltage. It is not possible to start charging up from low input voltages such as 10mV from TEG. Several start-up techniques are proposed in literature. One of the ways to start-up is to implement a mechanical switch which initially transfers charge to raise the voltage on storage node high enough to run the circuits reliably [39]. Another method to start-up can be to use a ring oscillator on V_{TEG}. The oscillator can be used to implement switching of the inductor and can charge the V_{CAP} voltage [40]. However, this technique requires a higher voltage at V_{IN}. These circuits start at voltages higher than 330mV [40]. The boost converter can also be started up using transformers [41]. They can start-up at voltages of 40mV. However, transformers are often very big in size. Our start-up circuit consists of the RF kick-start circuit method proposed in [1]. It consists of a 30-stage RF rectifier, The RF rectifier circuit receives the RF signal from outside and starts charging the V_{CAP} voltage. The boost converter circuit starts-up at 500mV.

3.2.4 Prototype Implementation and Measurement

The circuit of the boost converter was implemented in 130nm CMOS process. Figure 3-17 shows the die photo of the circuit. We targeted the resistance of V_{IN} to V_{SS} line to 300mΩ, which included bond-wire, inductor's parasitic DC resistance, board's trace resistance and resistance of the MOS transistor M_{LS}. The inductor used for the design was a 10µH coil-craft inductor. The total area for the implementation was $0.12\mu m^2$. We used three IO pads for V_{SS} and two IO pads for V_{CAP}. Figure 3-18 shows the maximum power point tracking scheme. It shows the pulse period where the boost converter is disabled and switching stops. The maximum power point voltage is sampled at this point and stored on the capacitor, which is used for the implementation of control.



Parameter	Value
Technology	130nm bulk CMOS
Total area	600 µm x 200 µm
Inductor value, L	10 µH
Designed V_{IN}-to-V_{SS} M_{LS} resistance	300 mΩ (Target)
Inductor DCR	70 mΩ
Bondwire	50 mΩ (1mm,1mil,gold)
NMOS Res	120 mΩ
Layout parasitic	60 mΩ

Figure 3-17 Die Photo and design parameter of the boost converter

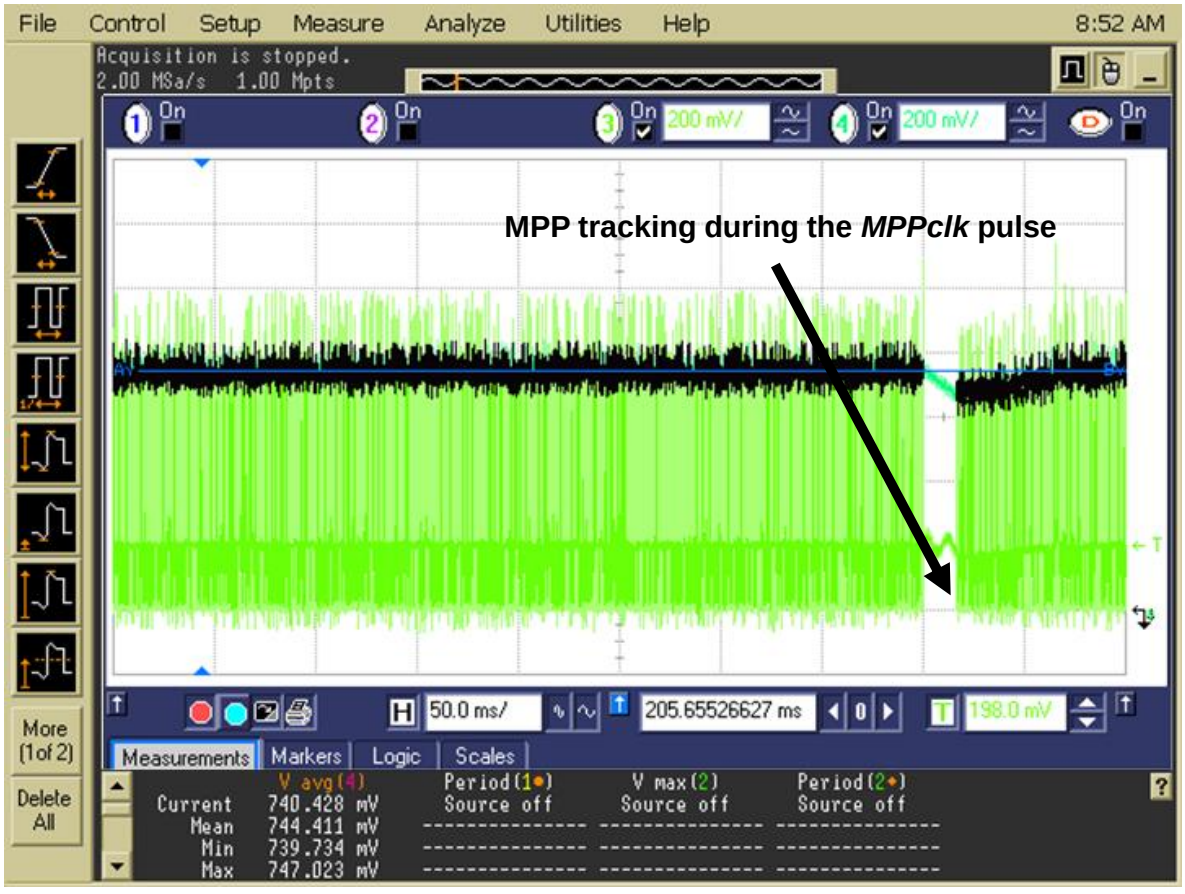


Figure 3-18 Maximum power point tracking pulse for MPP CLK

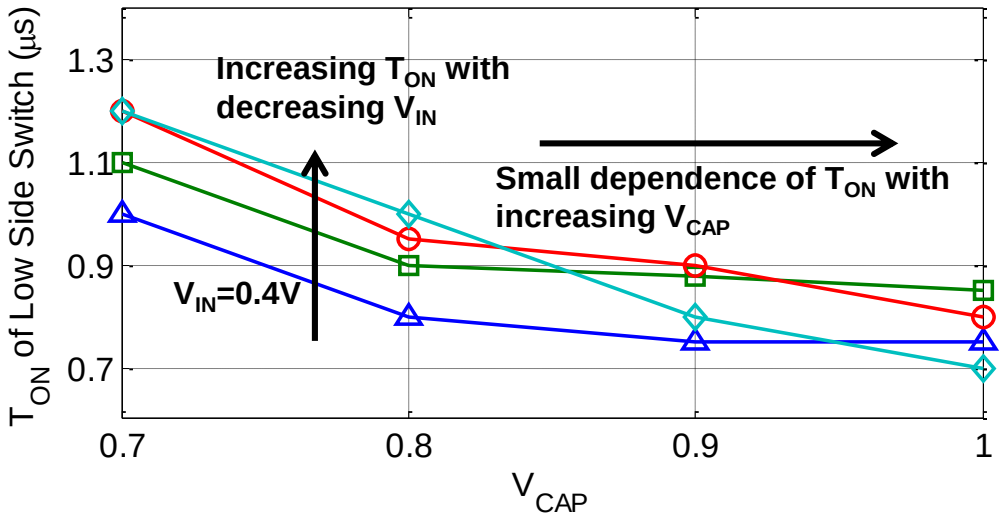


Figure 3-19 Measured TON of low side LS switch w.r.t. V_{CAP} and V_{IN} indicating peak inductor current control scheme

Figure 3-19 shows the measured LS switch pulse width with V_{CAP} and V_{IN}. The LS pulse width is directly proportional to the peak inductor current. The Figure shows small dependence of peak inductor current change with V_{CAP} for a given V_{IN}. With decreasing V_{IN}, the LS time increases. As I_{PEAK} is directly proportional to V_{IN}, decreasing V_{IN} requires that T_{ON} should increase to maintain a constant peak inductor current. Figure 3-19 shows increasing T_{ON} with decreasing V_{IN}.

Figure 3-20 shows the efficiency measurement of the boost converter at various input voltages V_{IN}. The efficiency is measured by changing the time period of the LS switch. It shows that a peak efficiency point exists for each value of V_{IN}. At very low value of $T_{ON,}$ the peak inductor current is low and switching loss dominates, resulting in lower efficiency, with at higher value of T_{ON} peak inductor current is high and it causes higher conduction loss, again reducing the efficiency. The T_{ON} time for the peak efficiency point for each V_{IN} increases with decreasing V_{IN}. These

measurements agree with the requirement to control I_{PEAK} to maximize the efficiency, as shown in Figure 3-11.

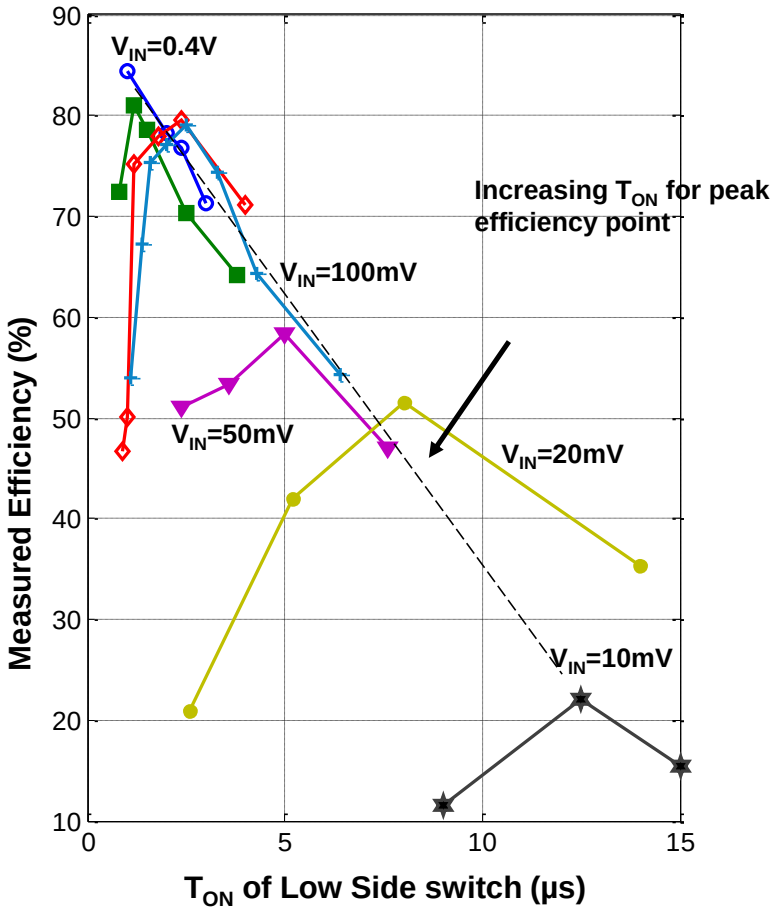


Figure 3-20 Measured efficiency with Low Side T_{ON}, showing increased efficiency at Higher T_{ON} for Low V_{IN}. It achieves 84% efficiency and 0.4V V_{IN} and 22% efficiency at 10mV V_{IN}

Figure 3-20 shows the measurement of efficiency for low input voltage and supports maximum of 10mA load current. The converter achieves a peak efficiency of 84% at an input voltage of 0.4V. It is able to harvest at input voltages as low as 10mV, with an efficiency of 22%. This is the least reported voltage from which energy can be harvested in a boost converter. It also improves over the state-of-the-art boost converter harvesting at 20mV [38]. The efficiency of the converter in [38]

is 48% at 20mV, while our work achieves an efficiency of 53% at 20mV. Figure 3-21 shows the Monte-Carlo simulation result of the peak inductor current. The peak inductor current varies with process. This is compensated by trimming the timing capacitor C_{LS} in the design.

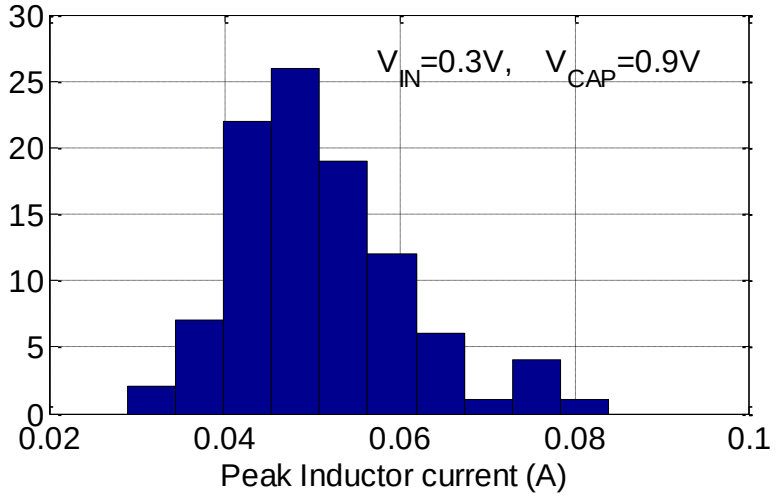
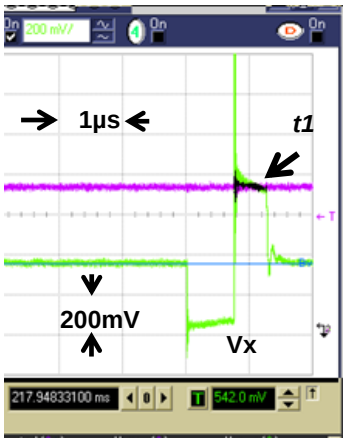


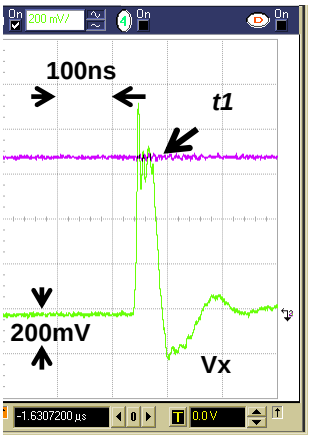
Figure 3-21 Variation of peak inductor current with process using Monte-Carlo simulation

Figure 3-22 shows the result of the zero detection scheme. The optimal zero detection helps in achieving higher frequency. The behavior of the node V_X during switching indicates the performance of zero detection. If the switch M_{HS} is opened before or after inductor current goes to zero, the output at the node V_X will over-shoot or under-shoot. For example, suppose the inductor was still carrying current when M_{HS} was opened. As a result, the low impedance of the switch is replaced by the high impedance of the diode. Therefore, the drop between V_X and V_{CAP} must increase. Therefore, the V_X node overshoots. Similarly, if the switch is turned on for a longer time and the current crosses zero and changes the direction and starts removing charge from the V_{CAP} voltage, then the V_X node will undershoot. Absence of overshoot or undershoot upon opening the switch is the indication of optimal zero detection. Figure 3-22 shows the measured zero detection

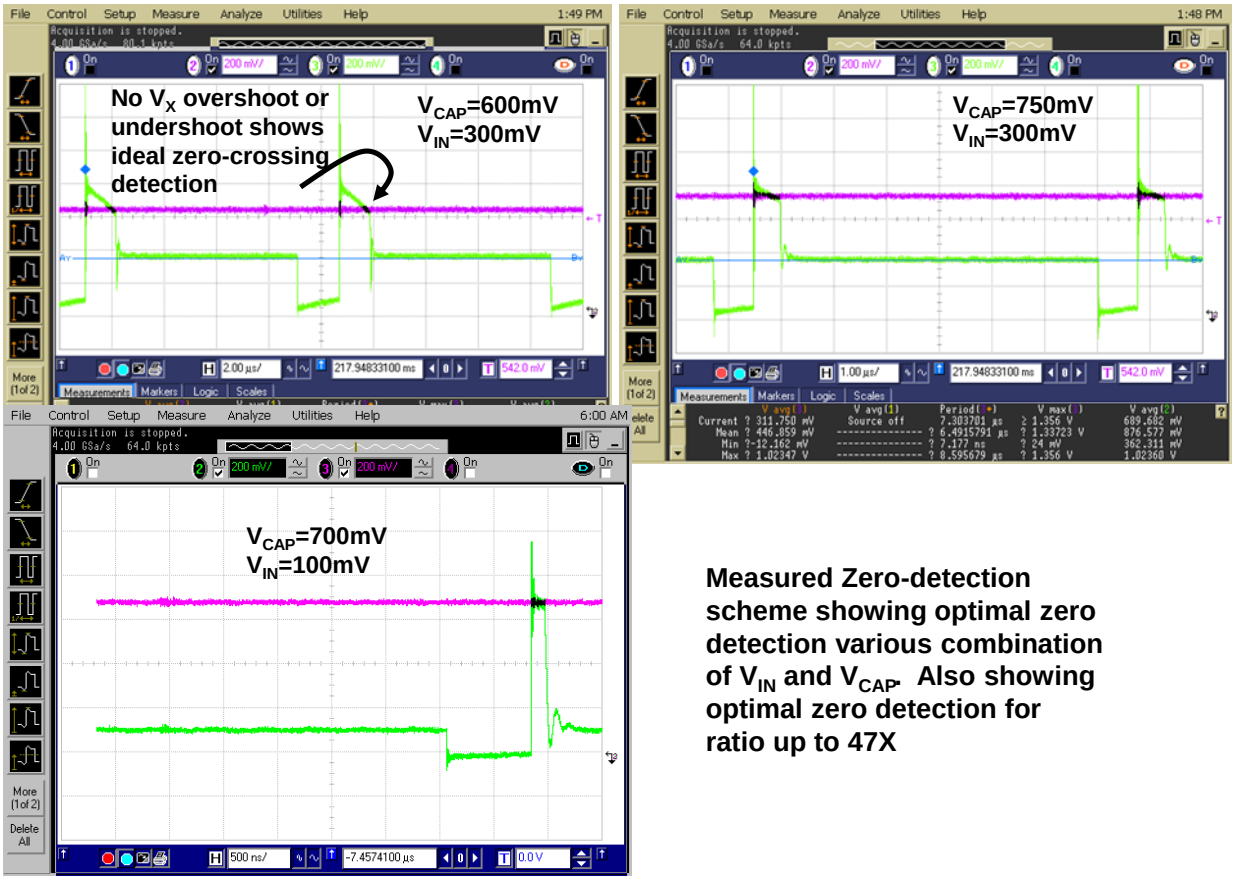
for various combinations of V_{IN} and V_{CAP}. Node V_X in all the waveform does not overshoot or undershoot, indicating ideal zero detection.



V_{IN}=0.3V, V_{CAP}=0.75V



V_{IN}=0.015V, V_{CAP}=0.7V



Measured Zero-detection scheme showing optimal zero detection various combination of V_{IN} and V_{CAP}. Also showing optimal zero detection for ratio up to 47X

Figure 3-22 Measured optimal zero detection

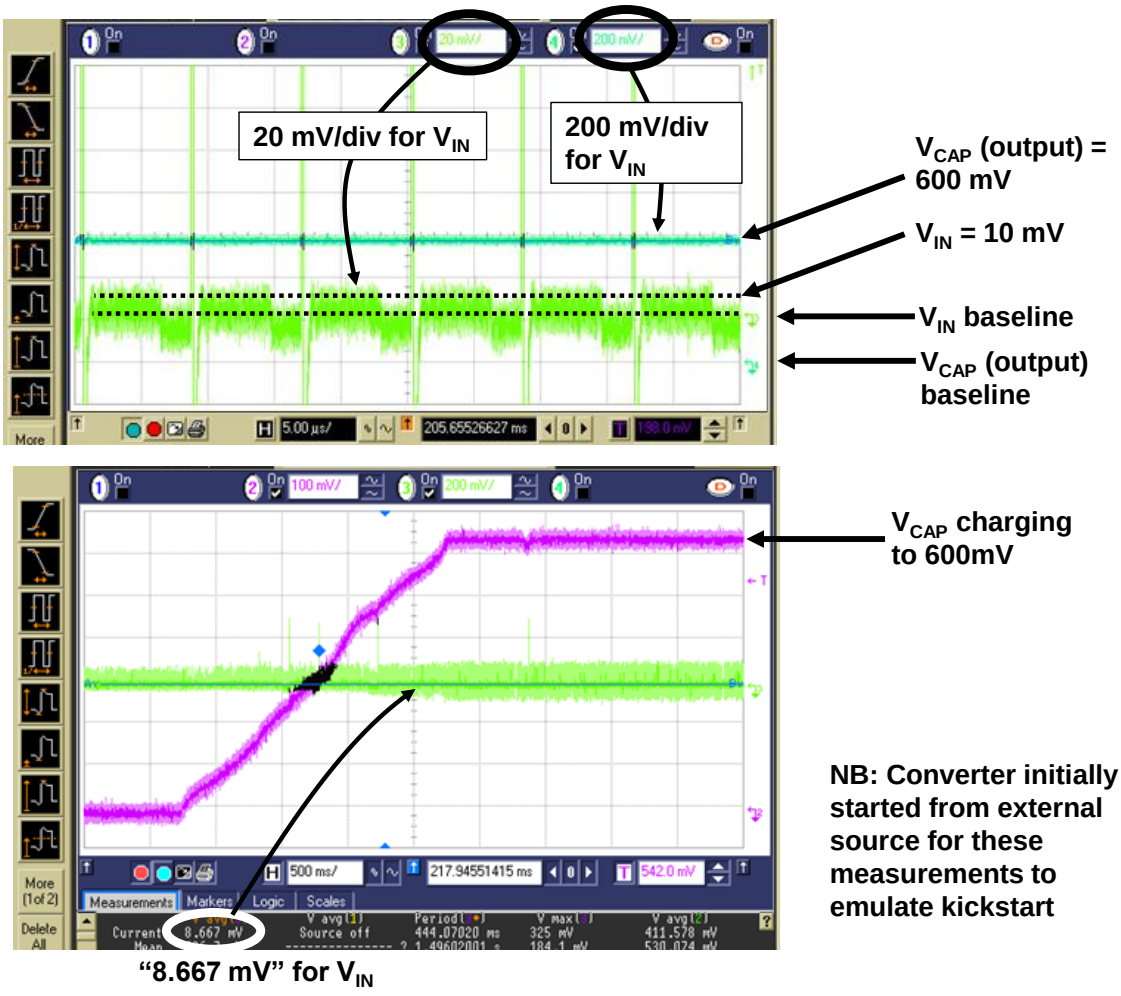


Figure 3-23 Measured operation of the boost converter with VIN=10mV and VIN=8mV.

Figure 3-23 shows the measured boost conversion from an input voltage of 10mV and 8mV. In this set-up, the V_{CAP} was broken into two rails, one supplying the circuit and another as the output of boost converter. The V_{CAP} supplying circuit was initially pre-charged to higher voltage. Figure 3-23 shows that the output can charge from V_{IN} of as low as 10mV. Figure 3-24 shows the waveform for kick-start. In this set-up, VCAP is initially charged to 590mV and then left to charge from boost converter. The boost converter charges the rail from 590mV to 1V.

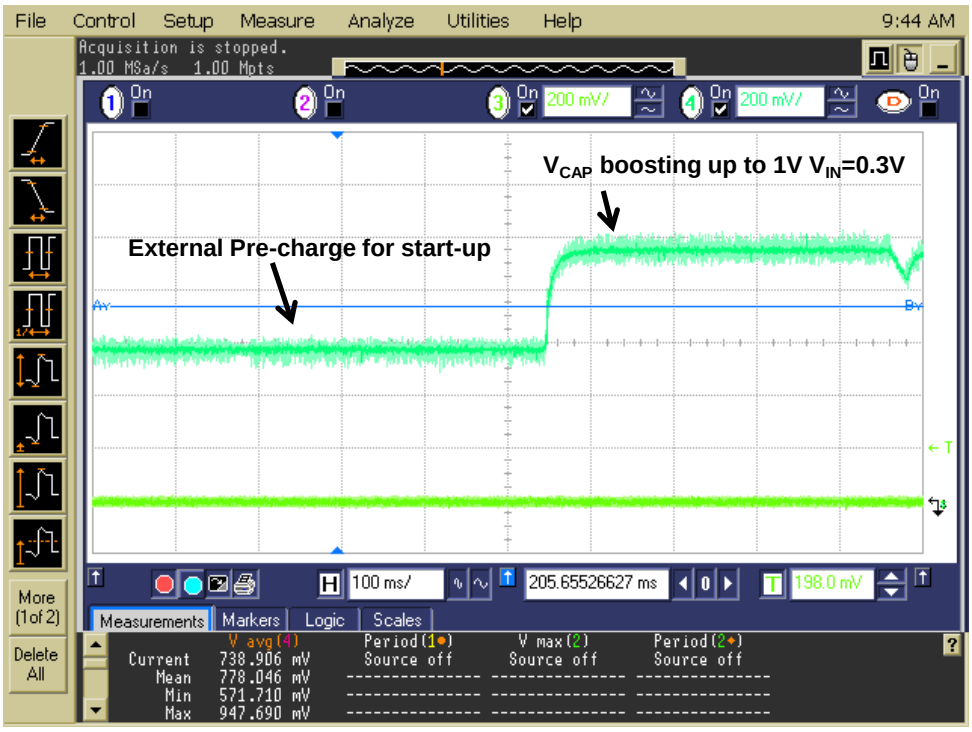


Figure 3-24 Measurements showing kick-start from 590mV charging to 1V

Table 3-1 compares this work with previously reported micro-power boost converters for low input voltages. Our work reports harvesting from least input voltage at 10mV, with an efficiency of 22%. Our static power consumption is 300nW and the circuits are designed in 130nm. The start-up voltage is similar to [38][40] at 500mV. The cold start-up mechanism for our system is RF assisted. Other work starts using mechanical kick-start [39] or transformers [41] to start at low voltages such as 35-40mV. This work proposes a peak inductor current control scheme and offset calibration implementation to improve performance, and to achieve an efficiency of 84% at 0.4V input voltage over 4% better than [40] for higher voltage category. In a low voltage category it improves the efficiency by 6% over [38] for input voltage of 20mV.

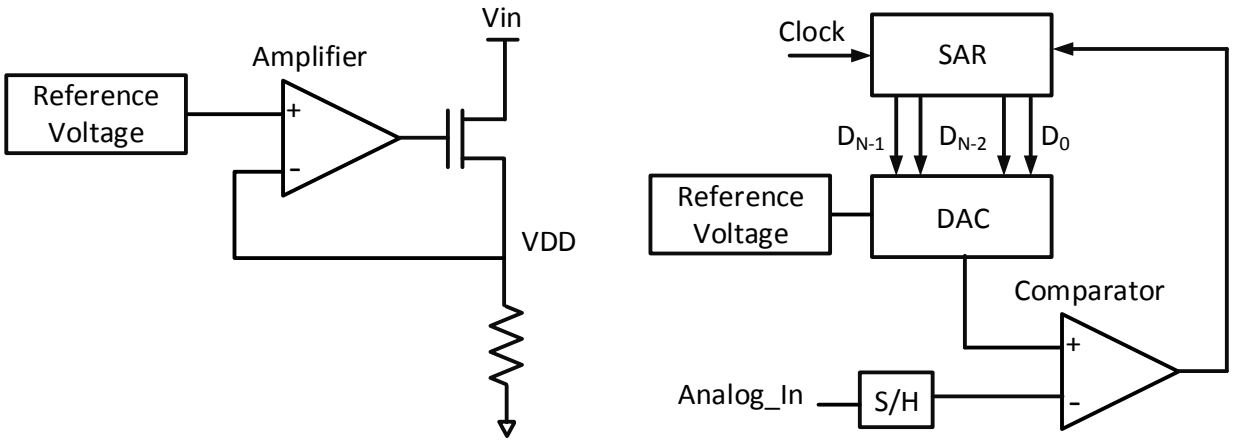
A thermoelectric boost converter combines an I_{PEAK} control scheme with offset compensation and duty cycled comparators, to enable energy harvesting from TEG inputs as low as 5mV to 10mV, 50% to 75% lower than prior work. Maintaining constant I_{PEAK} allows the converter to sustain high efficiency across a broad V_{IN} range, achieving 52% and 84% efficiency at 20mV and 400mV, respectively, which improves on prior designs. These features allow the converter to extend the operating window for thermal harvesting with low thermal gradients, which is ideal for body-worn sensors.

Table 3-1 Comparison summary of the boost converter with previous micro-power converters

	This work	[38]	[39]	[40]	[41]
Harvesting Mode	TEG	TEG	TEG	TEG/PV	TEG
Minimum V_{IN}	10mV	20mV	25mv	-	40mV
Maximum V_{IN}	none	250mV	none	none	-
V_{OUT}	1V	1V	1.8V	-	0.3V
Start-up Voltage	0.5V	0.6V	35mV w/ mech.	330mV	40mV w/ x-former
Quiescent Current	300nW	~1µW	-	330nA	-
Constant I_{PEAK} Control	✓	×	×	×	×
Offset Compensation	✓	×	×	×	×
MPP Tracking	✓	×	✓	✓	✓
Peak Efficiency @ V_{IN} (end to end)	84% @ 0.4V 81% @0.3V 79% @ 0.1V	75% @ 0.1V	58% @0.1V	80% @ 0.5V	61% @ 0.3V
Efficiency at low V_{IN}	52% @ 20mV 22% @10mV	46% @ 20mV	-	-	30% @ 50mV
Technology	130nm	130nm	350nm	-	130nm

3.3 Voltage Reference Circuit for ULP Systems

An ideal voltage reference is independent of variations of power supply or temperature. The term *reference* is used to indicate that the voltage coming out of a voltage reference circuit is more precise than ordinarily found in other sources. Many applications in a system require voltage reference. Figure 3-25 shows the block diagram of a voltage regulator circuit and a successive approximation register (SAR) analog to digital converter (ADC). The voltage reference block forms an essential component in these circuits. In a voltage regulator circuit, output V_{DD} is controlled through the voltage reference. A precise reference voltage gives a precise V_{DD}. In an ADC circuit, the analog voltage from the external world is converted into digital bits. The external signal is compared with the reference voltage for conversion. The accuracy of the conversion depends on the accuracy of the reference. A voltage reference circuit is an essential component in a SoC, and greatly determines the performance of various blocks inside it. In this section, we present a voltage reference circuit suitable for ULP applications.



a) Reference voltage used in voltage regulator circuit for accurate VDD

b) Reference voltage used in analog to digital (ADC) circuit

Figure 3-25 Use of voltage reference circuit in basic building blocks such as voltage regulators and ADC

The voltage reference circuit is needed for our EHM system, for both the energy harvester circuit and the power management circuit, for regulation and control as shown in Figure 3-1. The design of voltage reference is very critical for our EHM system and it needs to meet several design requirements. The voltage reference should have very small variations with process, temperature, and voltage which, in this case, is V_{CAP} of Figure 3-1. These are typical requirements for voltage references in any system. However, for ULP systems running on harvested energy [1], additional requirements have to be met. First, the voltage reference circuit needs to be low power. Second, the area of the circuit should be small to keep the size of the BSN node small. Finally, the voltage reference circuit should become operational at a lower voltage of V_{CAP}. This is very critical for ULP systems, for the following reason: The V_{CAP} value at which voltage reference becomes active is typically the voltage at which the node can turn on. At this voltage, all the V_{DD}s for the system become operational. Therefore, the voltage reference circuit puts a threshold voltage for V_{CAP} at which the BSN node can turn on. If this voltage is low, the BSN will have a longer life-time. The voltage reference circuit used in [1] has a start-up voltage of 0.9-1V, which is typical of circuits used for voltage references in low power areas, and consumes 200nW. In this work, we present a voltage reference circuit which has a start-up voltage of 0.8V and which consumes 80nW power.

3.3.1 Bandgap Voltage Reference

The design of the voltage reference circuit has been a subject of research in the circuit design community since the early days of integrated circuits. This is because of the impact voltage reference has on the overall performance of the system. In the early days of circuit design, temperature compensated zener diodes were used for generating the voltage references. The break down voltage of zeners was close to 6V in those days, they were very noisy, they consumed large

amount of power and they were discrete, off-chip components. The voltage reference using zeners did not meet many requirements of a typical reference. The voltage reference circuit needs to be process and temperature independent. It should support large voltage ranges and be independent of supply variation. The bandgap voltage reference circuit [47] (pp. 153-159) meets the key parameters for all of the above requirements. The concept and first implementation of bandgap reference was proposed by Wildar [48], providing a reference at 5V. A key advantage of this circuit in those days was its ability to scale. Soon after the invention of the first bandgap reference circuit [48], voltage reference ICs producing 10V [49] and 2.5V [50] were demonstrated, using the same concept. The bandgap voltage reference is produced by adding a voltage that is proportional-to-absolute-temperature (PTAT) to another voltage that is complementary-to-absolute-temperature (CTAT), which produces a temperature-compensated voltage.

Over the years of CMOS scaling and evolution in circuits, the bandgap reference has undergone changes in its architecture. However, the concept remains the same since the first bandgap reference was published more than 30 years ago. Various voltage reference circuits have been proposed as alternatives to bandgap reference. Some of the recent publications in this area are listed in the Bibliography [51][52][53]. These circuits use different characteristics of the MOS transistor to obtain a temperature-compensated voltage. However, the bandgap reference circuit outperforms these alternatives in one or more critical parameters for voltage references. As a result, the alternative circuits are used only in limited applications with relaxed specifications. On the other hand, the bandgap voltage reference is widely used. In this section, we present a bandgap voltage reference circuit with a new architecture for our EHM system, shown in Figure 3-1. The proposed circuit is designed to meet the power, area, and voltage requirements of a ULP system.

This section is divided into the following sub-sections. In Section 3.3.2, we present the basic concept of bandgap reference. In Section 3.3.3, we present the current architectures of bandgap reference and their limitations, particularly in the context of ULP systems such as BSNs. In Section 3.3.4, we present the proposed design. In Section 3.3.5, we present the results and limitations of the proposed design.

3.3.2 Background

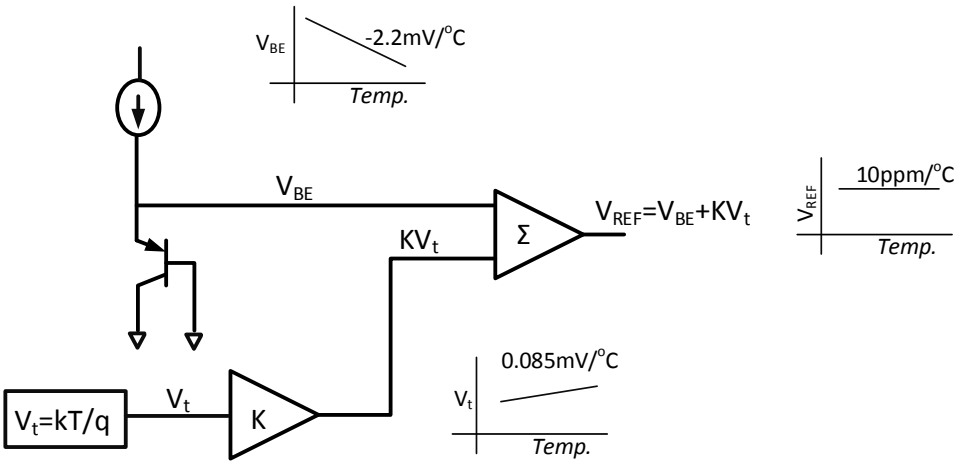


Figure 3-26 Principle of bandgap voltage reference circuit generating a constant voltage reference with temperature

In this section, we present a qualitative background of bandgap voltage reference circuit. A more theoretical background is available in [47] (pp. 153-159). Figure 3-26 shows the principle behind the bandgap reference circuit. The voltage V_{BE} is complementary-to-absolute-temperature (CTAT). It decreases with increasing temperature with a slope given by -2.2mV/^{o}C. The CTAT voltage is added to the voltage V_t, which is proportional-to-absolute-temperature (PTAT), and its slope is given by 0.085mV/^{o}C. The PTAT voltage is multiplied with a constant K and added to the CTAT

voltage to obtain the bandgap reference, V_{REF}. The value of K is chosen such that the temperature dependence of CTAT and PTAT cancel each other, and V_{REF} becomes a temperature independent voltage reference (10ppm/^{o}C).

Generation of Bandgap Voltage

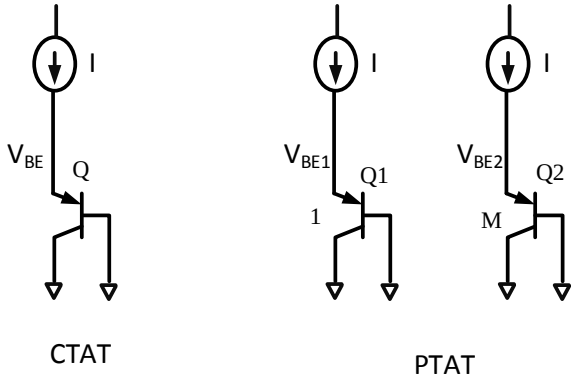


Figure 3-27 PTAT and CTAT voltage generation circuit

Figure 3-27 shows the CTAT and PTAT voltage generation circuit used for bandgap. The bipolar junction transistors (BJT) are used for the generation of PTAT and CTAT voltages. The CTAT voltage is simply generated by connecting the BJT transistor Q into a diode configuration, as shown in Figure 3-27. The CTAT voltage is given by the base-emitter voltage, V_{BE} of the transistor. As temperature increases, the voltage V_{BE} decreases because of the increase in the number of carriers. Since the number of carrier increases, the conductivity of the transistor increases, which decreases the V_{BE} voltage. The expression of V_{BE} with temperature is given by [47] (pp. 155),

$$V_{BE} = V_{G0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\left(\frac{T}{T_0}\right) + \frac{\gamma kT}{q} ln\left(\frac{T}{T_0}\right) + \frac{kT}{q} ln\left(\frac{J_C}{J_{C0}}\right) \quad (3.9)$$

where V_{G0} is the bandgap voltage of silicon, T is the temperature, T_0 is the room temperature, V_{BE0} is the V_{BE} voltage at room temperature, J_C and J_{C0} are the current densities, and γ, k, q and α are various physical constants. The value of V_{BE} decreases with temperature. The PTAT voltage is obtained by using two BJT transistors, Q1 and Q2 as shown in Figure 3-27. The transistor Q2 is bigger than Q1 by multiplicity factor M. If the same current is made to flow through Q1 and Q2, the voltage drop across these transistors, V_{BE1} and V_{BE2}, will be different, because of the different current densities (J_C in equation (3.9)). The difference between V_{BE1} and V_{BE2} is called ΔV_{BE} and can be obtained by using equation (3.9),

$$\boldsymbol{\Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{kT}{q} ln\left(\frac{J_{C1}}{J_{C2}}\right) = V_t ln\left(\frac{J_{C1}}{J_{C2}}\right)} \tag{3.10}$$

The ΔV_{BE} voltage is PTAT and increases with temperature. Thus, equation (3.9) and (3.10) give the expression of CTAT and PTAT voltages from the circuit shown in Figure 3-27. The temperature independent voltage V_{REF} is given by addition of CTAT and PTAT voltages,

$$\boldsymbol{V_{REF} = V_{BE1} + K\Delta V_{BE}} \tag{3.11}$$

where K is the multiplication factor for PTAT to cancel the temperature coefficient in V_{REF}. Solving (3.11) for V_{REF} to obtain zero temperature coefficient, gives K as,

$$\boldsymbol{K = \frac{V_{G0} - V_{BE0} - (\gamma - \alpha)V_t}{V_{t0}}} \tag{3.12}$$

which gives V_{REF} as,

$$\boldsymbol{V_{REF} = V_{G0} + (\gamma - \alpha)V_{t0}} \tag{3.13}$$

The voltage V_{REF} is called the bandgap voltage reference voltage and its value at room temperature is 1.262V. The term bandgap reference is used for V_{REF} because the voltage in equation (3.13) is largely determined by the V_{G0}, which is the silicon bandgap voltage.

We have now obtained both CTAT and PTAT voltages and the constant to obtain a voltage reference independent of temperature. Now we will present a typical circuit implementation of bandgap voltage reference.

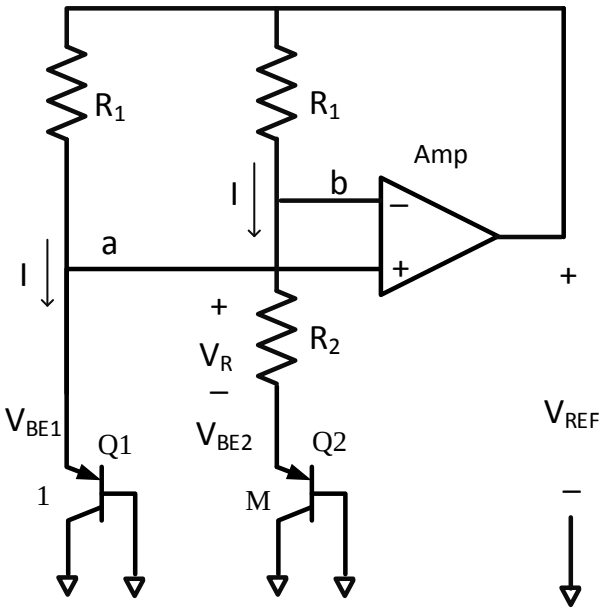


Figure 3-28 A conventional bandgap reference circuit

Figure 3-28 shows the circuit diagram of a conventional bandgap voltage reference circuit. Transistors Q1 and Q2 are used, along with resistors R_1 and R_2 and amplifier Amp. The functioning of the circuit is explained as follows. The amplifier sets the same voltages at its input net *a* and *b,* because of its high gain (assuming zero offset voltage). Therefore, the same current flows into the transistor Q1 and Q2. Q2 is sized M times bigger than Q1. The voltage V_{BE2} is lower than V_{BE1}. The voltage V_{REF} can be written as,

$$\boldsymbol{V_{REF} = V_{BE1} + IR_1} \tag{3.14}$$

I is also given by V_R/R_2, because the same current flows in both Q1 and Q2. Since *b* is at the same voltage as *a*, which is equal to V_{BE1}. Therefore, *I* can be written as,

$$I = \frac{V_{BE1} - V_{BE2}}{R_2} = \frac{\Delta V_{BE}}{R_2} \tag{3.15}$$

so, V_{REF} can be written as,

$$V_{REF} = V_{BE1} + \frac{R_1}{R_2}\Delta V_{BE} \tag{3.16}$$

The equation (3.16) takes the form of bandgap voltage expression given by equation (3.11), where constant *K* is given by the ratio of R_1 and R_2. The values of R_1 and R_2 can be chosen such that the temperature dependence of V_{REF} can be eliminated. Figure 3-29 shows the output of bandgap reference voltage at 1.24V. It shows that that output changes by 2.5mV, for a change of temperature from -20-100ºC (17ppm/ºC). Further, the dependence of V_{REF} on power supply can be investigated by examining the expression of equation (3.16). V_{BE} and ΔV_{BE} are clamp voltages obtained from the diodes of Q1 and Q2. They have very small dependence on power supply. Bandgap reference voltage has small process dependence, which is not significant for various power management applications. However, for high precision applications such as precision ADC, the process variation can be addressed by trimming the resistor R_2 in the design.

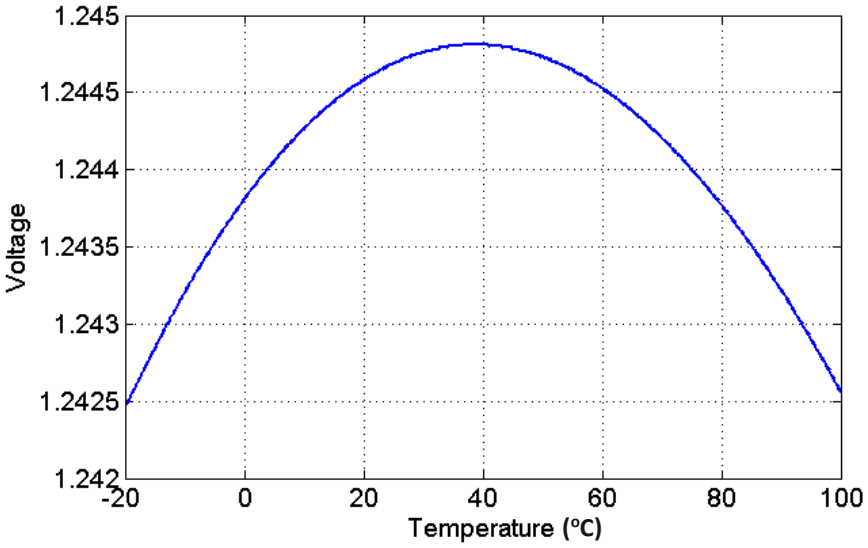


Figure 3-29 Variation of bandgap reference with temperature showing 17ppm/ºC variation

The bandgap reference circuit shown in Figure 3-28 performs very well and provides almost an ideal voltage reference circuit. However, it has two primary limitations which become critical with CMOS scaling. The first limitation is that the output voltage of bandgap comes out at ~1.25V, which is much higher than the V_{DD} of modern processes. The second major limitation of this circuit is that it needs a supply voltage higher than 1.2V, because the reference voltage is produced in step-down fashion. These were critical limiting factors of bandgap architecture of Figure 3-28 and its usage for modern systems. New architectures for bandgap, which overcome these limitations, have been proposed in the literature [54][55][56]. In the next section, we will present the state-of-the-art low voltage bandgap references.

3.3.3 State-of-the-art Bandgap Circuits for Low Power Applications

CMOS process scaling has brought down the operating voltage of the system to sub-1V range. Further, the sub-threshold operation of systems to save power has brought the VDD voltages below 500mV [1]. A voltage reference circuit that can provide reference to support lower voltages was needed. It also needed to be operational at lower supply voltage, as well as consume lower power, particularly for mobile applications such as mobile phones, laptops, etc. The conventional architecture of bandgap could no longer support these voltages. New architectures were proposed to support low voltage operation. In this section, we will discuss a few recently published low voltage bandgap circuits.

Banba Bandgap Reference

The very first bandgap circuit that produced a reference voltage lower than 1V was published by H. Banba [54], and is popularly known as Banba bandgap. Figure 3-30 shows the architecture of

the Banba bandgap reference. It also works as follows. Net *a* and *b* are set at the same voltage by the amplifier. So,

$$V_a = V_b = V_{BE1} \tag{3.17}$$

Therefore, the current *I* is given by looking at node *b*,

$$I = \frac{V_b}{R_1} + \frac{V_b - V_{BE2}}{R_2} \tag{3.18}$$

Using equation (3.17), we get *I* as,

$$I = \frac{V_{BE1}}{R_1} + \frac{V_{BE1} - V_{BE2}}{R_2} = \frac{V_{BE1}}{R_1} + \frac{\Delta V_{BE}}{R_2} \tag{3.19}$$

Now, transistors M1, M2, and M3 form mirrors. Therefore, the same current comes out of all the transistors. Therefore, the Voltage V_{REF} is given by,

$$V_{REF} = IR_3 = \frac{R_3}{R_1}\left(V_{BE1} + \frac{R_1}{R_2}\,\Delta V_{BE}\right) \tag{3.20}$$

The equation (3.20) gives us an expression of bandgap reference similar to the expression of equation (3.16), with a scaling factor given by R_3/R_1.

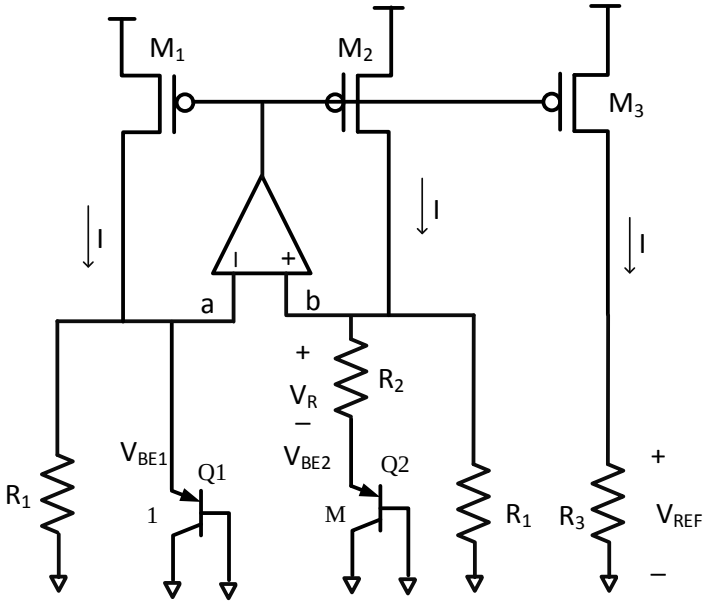


Figure 3-30 Architecture of Banba Bandgap circuit

There are few advantages of Banba bandgap reference, when compared with conventional architecture as shown in Figure 3-28. First, the bandgap reference voltage, which was always fixed at ~1.25V, can now be scaled down by carefully choosing R_1 and R_3. Second, the minimum operating voltage for this circuit also scales down. The minimum operating voltage V_{min} for this circuit is given by,

$$\boldsymbol{V_{min} = V_{BE1} + V_{DS}} \tag{3.21}$$

where V_{DS} is the drain to source voltage of pMOS, M_1. The V_{BE} of BJT is between 700mV-800mV and V_{DS} of transistor M1 can be as low as 100mV. Therefore, the circuit can operate for voltages below 1V, which makes it suitable for modern scaled designs. The BSN SoC reported in [1] uses Banba architecture and starts operating at 0.9V.

The lower V_{min} for bandgap is even more important for ULP systems such as BSNs. The V_{min} of bandgap determines the voltage at which the BSN node can turn on because the reference is made available at that voltage and is used to turn on the power supplies for the system. The lower turn-on voltage will increase the operational life time of the system. Therefore, it is necessary to bring the V_{min} of bandgap voltage down, as low as possible. Recent work [56] brings the V_{min} voltage down to 750mV. It uses switched capacitor circuits for the architecture where, instead of resistors, switching capacitors are used for generating the ratios of V_{BE} and ΔV_{BE}. The V_{min} of this circuit is also limited by equation (3.21) and a lower V_{min} is achieved by proper sizing and design. In the next section, we present a bandgap voltage reference circuit that starts operating at 800mV. Further, the power consumption of the proposed circuit is ~80nW, which is 2X lower than [56] and best in class for non-duty cycled bandgap reference. The proposed circuit is also lower in area. The next section presents the proposed bandgap circuit.

3.3.4 A 80nW, Low Power Bandgap Reference Operational from 0.8V

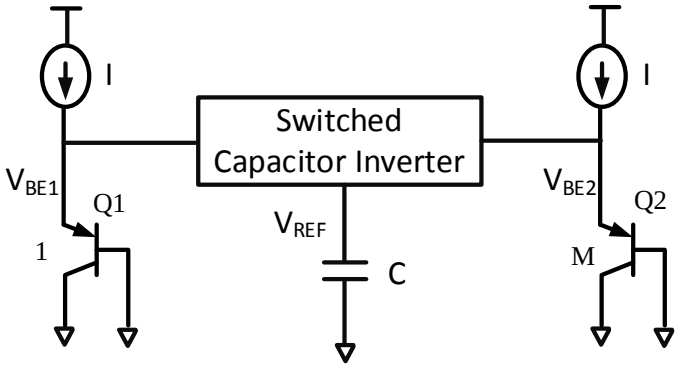


Figure 3-31 Circuit diagram of the proposed bandgap reference

Figure 3-31 shows the circuit diagram of the proposed bandgap reference. It uses switched capacitor techniques to generate the bandgap voltage. The circuit consists of a switched capacitor inverter, BJT transistors Q1 and Q2, current sources, and a sampling capacitor for holding bandgap voltage. The current sources are used to generate voltages V_{BE1} and $V_{BE2,}$ as shown in Figure 3-31. The switched capacitor inverter circuit is used for generating ratios of V_{BE1} and V_{BE2} to obtain the bandgap voltage. The switched capacitor inverter circuits are typically used for generating voltages that are negative of V_{in} [58]. In Figure 3-31, the switched capacitor inverter is connected to Q1 and Q2, which provide the output voltages at V_{BE1} and V_{BE2}. The use of the switched capacitor inverter circuit removes the need for large resistance in Banba architecture and can provide lower area solution. Further, a clock is used for the inverter circuit that can be made to operate at lower frequency to reduce the power. The use of the switched capacitor inverter circuit, and lower clock frequency, provides lower area and lower power consumption compared to the state-of-the-art bandgaps.

The design description of the proposed circuit is divided into descriptions of each sub-block. First, we explain the functioning of the switched capacitor inverter circuit, then the use of the principles of voltage inversion for generating bandgap reference, followed by the complete circuit implementation. Finally, we will present the results.

Switched Capacitor Voltage Inverter Circuit

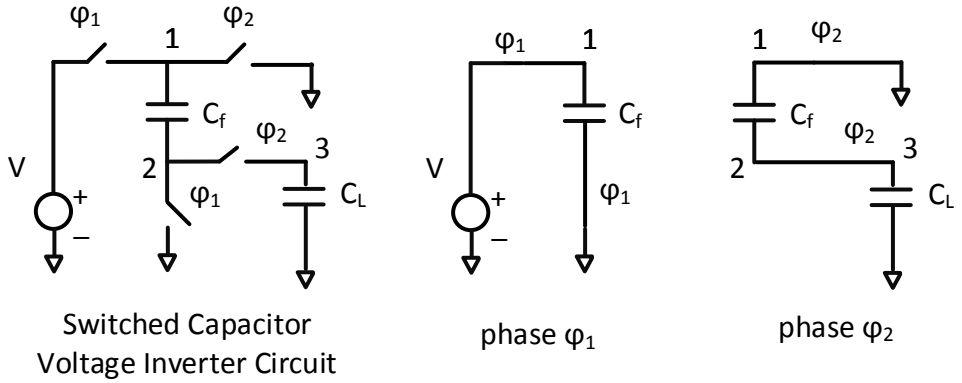


Figure 3-32 Switched capacitor voltage inverter circuit and its operation

Figure 3-32 shows the switched capacitor voltage inverter circuit used in our design. Its functioning is explained as follows. The switched capacitor inverter uses non-overlapping clock phases, ϕ_1 and ϕ_2. In phase ϕ_1, node 1 is connected to V and node 2 is connected to ground, charging the top plate of capacitor C_f to V and the bottom plate to ground, as shown in Figure 3-32. In phase ϕ_2, node 1 is connected to ground and node 2 to the output capacitor C_L. Since the top plate of the capacitor C_f was charged to V in phase ϕ_1, charging the top plate to ground pushes the voltage on the bottom plate to –V, as voltage across capacitors cannot change since the bottom plate is not connected to a voltage source. The capacitor C_L will eventually charge to -V after a given number

of switching cycles. Therefore, the switched capacitor inverter circuit generates a voltage which is negative of the input voltage V.

Proposed Bandgap Circuit : Concept

The equation for bandgap reference voltage is given by equation (3.11),

$$V_{REF} = V_{BE1} + K\Delta V_{BE}$$

which can be rewritten as,

$$V_{REF} = (K+1)V_{BE1} - KV_{BE2}$$

$$V_{REF} = (K+1)\left(V_{BE1} - \frac{K}{K+1}V_{BE2}\right)$$

Therefore, we propose to obtain the reference voltage as,

$$V_{REF} = a(V_{BE1} - bV_{BE2}) \quad (3.22)$$

The negative coefficient for V_{BE2} is obtained through a voltage inverter circuit. In the next section, we will show the working of the proposed bandgap circuit.

Proposed Bandgap Circuit

Figure 3-33 shows the circuit diagram of the proposed bandgap voltage reference circuit. It uses switched capacitor techniques to utilize a switched capacitor voltage inverter circuit for the generation of V_{REF} voltage. The two phases of the clock, ϕ_1 and ϕ_2, are non-overlapping and facilitate the switching capacitor functionality. In phase ϕ_1, the proposed circuit reduces into the circuit shown into Figure 3-33 (b). The capacitors, C_1 and C_2, are connected across the BJTs, Q1 and Q2, and are charged to voltages, V_{BE1} and V_{BE2}. Therefore, the charge stored on capacitor C_1 and C_2 is given by,

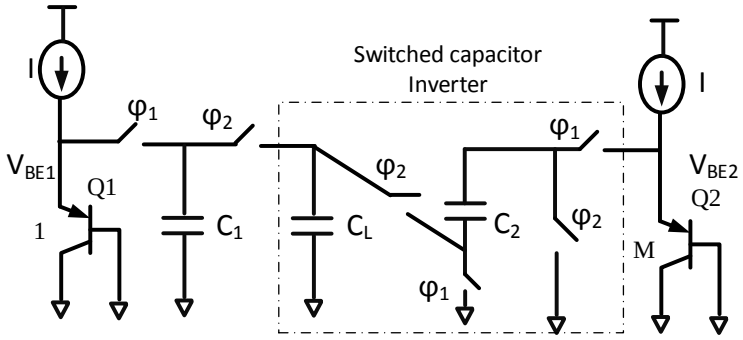
$$\boldsymbol{Q_1 = C_1 V_{BE1}} \ , \ \boldsymbol{Q_2 = C_2 V_{BE2}} \tag{3.23}$$

The switch connections are changed in phase ϕ_2 and the circuit reduces into the circuit shown by Figure 3-33 (c). In phase ϕ_2, the top plate of C_1 gets connected to the bottom plate of C_2 and the top plate of C_2 is connected to ground. Since top plate of C_2 is connected to ground, the output voltage on C_2 will be $-V_{BE2}$. Voltage on C_1 is V_{BE1}. Therefore the connection with C_1 with C_2 results in charge sharing given by,

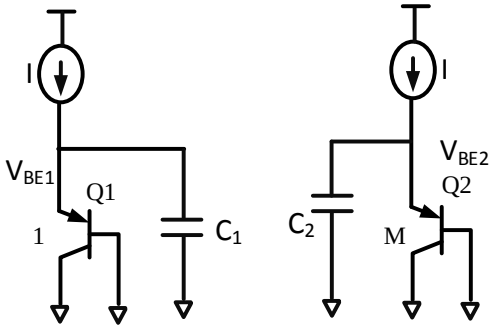
$$\boldsymbol{Q = Q_1 - Q_2 = C_1 V_{BE1} - C_2 V_{BE2}} \tag{3.24}$$

Now, the voltage on the capacitor C_L is given by, (The value of C_L doesn't play a role in charge sharing because it is the load capacitor used for final settling voltage.)

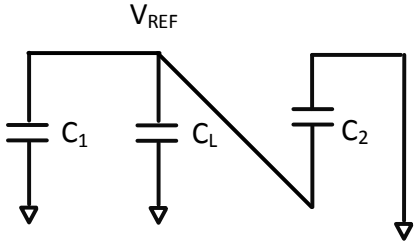
$$\boldsymbol{Q = (C_1 + C_2) * V_{REF}}$$



a) Circuit diagram of the proposed bandgap reference circuit



b) Circuit operation in phase φ_1



b) Circuit operation in phase φ2 to gnerate V_{REF}

Figure 3-33 Proposed bandgap reference circuit using switched capacitor voltage inverter

Therefore, the output voltage can be written as,

$$(C_1 + C_2) * V_{REF} = C_1 V_{BE1} - C_2 V_{BE2}$$

$$\boldsymbol{V_{REF} = \frac{C_1}{C_1 + C_2}\left(V_{BE1} - \frac{C_2}{C_1} V_{BE2}\right)} \quad (3.25)$$

Equation (3.25) reduces in the form of bandgap reference equation given by equation (3.11), where the value of constant *b* can be obtained by selecting the value of capacitance C_1 and C_2. The proposed circuit has noise injection through the charge coupling of switches. There will be an error in the output voltage given by (3.25) because of the charge sharing. Since the charge coupling will change with V_{IN}, therefore output voltage will also change with V_{IN}.

By applying the above circuit technique, we have successfully obtained the bandgap reference voltage. The proposed scheme has the following advantages over classical Banba bandgap reference. First, large resistances are no longer needed for generating bandgap voltages. Therefore, the area of the proposed circuit will be much smaller than the Banba architecture implementation for low power application. Second, the power consumption of the proposed scheme will be lower, because the elimination of resistors eliminates the static power consumption in the resistors, and the switched capacitor converter power can be lowered by lowering the clock frequency. The noise performance of the circuit is traded with capacitor C_L and settling time of the converter. Therefore, the proposed bandgap solution provides a low power, lower area solution for the implementation of voltage reference for our EHM system.

3.3.5 Prototype Implementation and Results

The proposed bandgap circuit was implemented in 130nm CMOS process. It has an area of 0.0264mm^2. The capacitors are implemented using MIM capacitors to reduce the effect of parasitic loading. The total area of the proposed circuit is much smaller than a conventional low power

bandgap circuit because it does not use big resistors. It consumes 80nW power at 0.8V Vin (V_{CAP}), which is 2X lower than the best reported power for non-duty-cycled bandgap reference.

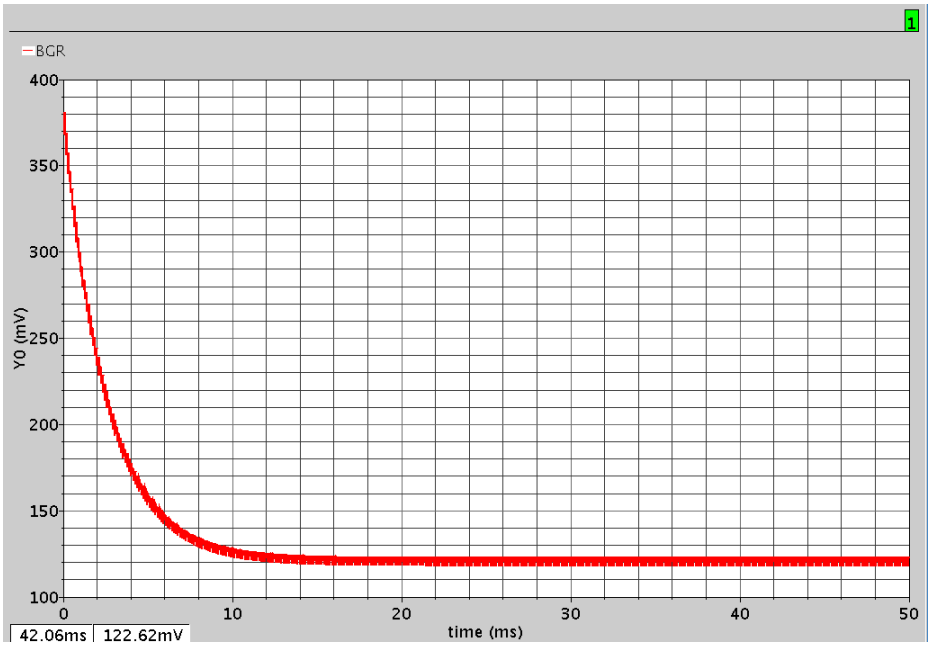


Figure 3-34 Transient behavior of bandgap reference

The circuit is a switching capacitor circuit; therefore, it has settling time. Figure 3-34 shows the transient behavior of the bandgap circuit. It takes 15ms to achieve a settling time at 0.8V V_{in}. The output voltage of bandgap reference is 123mV. The settling time is directly dependent on the clock frequency and power supply. In some applications, the settling time of the bandgap can be large. Therefore, we also propose a fast start-up mode for the circuit. During start-up, the clock frequency can be made several times faster, which reduces the settling time. This is done during power-on reset mode, where the current source of the clock source is increased several times, increasing the frequency. We achieve a settling time of 20µs during start-up if used in fast start-up mode.

The circuit was verified for a temperature range of -20°C to 100°C. While this range is quite large for the intended ULP applications, the performance of the circuit in this range is crucial for it to compare with the state-of-the-art circuits. Figure 3-35 shows the variation of the bandgap output for a temperature change of -20°C to 100°C. The proposed bandgap circuit is designed to provide an output voltage of 122mV, and the output voltage varies by 1.5mV over a temperature variation of 120°C, achieving a performance of 100ppm/°C. The performance of the bandgap circuit with temperature is in line with the reported work. A better performance is usually achieved at higher output voltage.

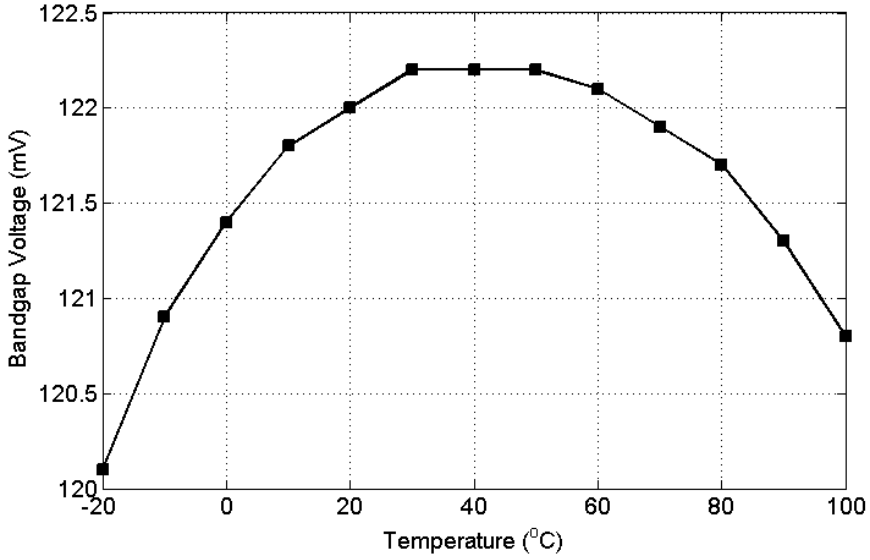


Figure 3-35 Bandgap output variation with temperature

Figure 3-36 and Figure 3-37 show the output of a bandgap circuit with respect to process and mismatch variation, and with input voltage variation. Figure 3-36 shows the untrimmed output of the bandgap and it achieves a 3σ variation of the <2.5%. The variation of the output voltage can be reduced by trimming the bandgap output, using the capacitors used in switched capacitor

circuits to generate the constants for bandgap. Figure 3-37 shows the variation with V_{in}. The output varies by ~1% when an external constant clock is used. The variation with respect to power supply can be reduced by using a dedicated clock source.

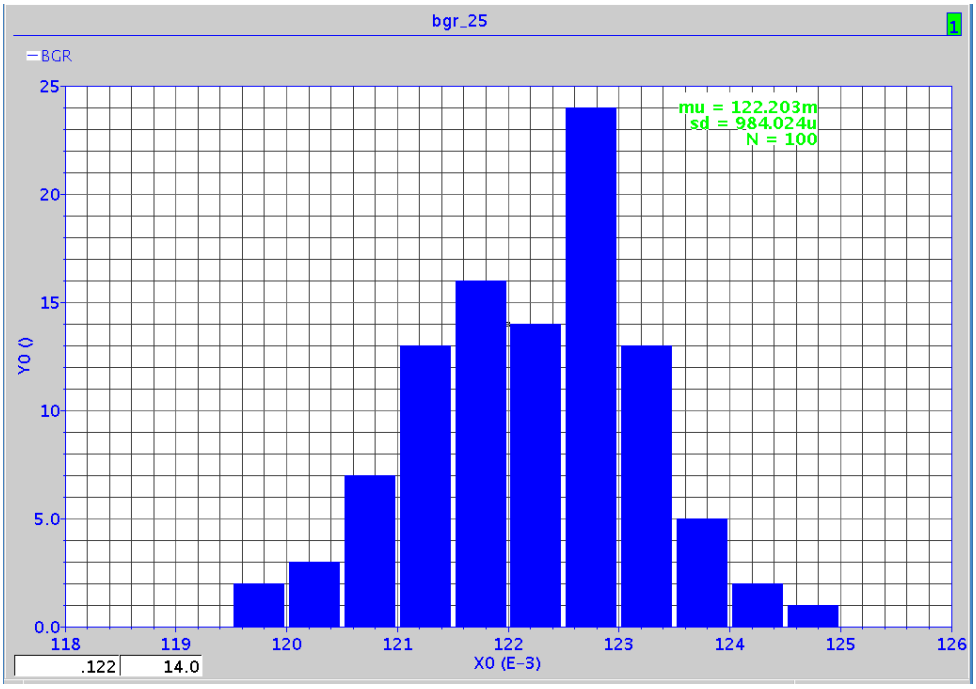


Figure 3-36 Variation with process: Monte-Carlo Simulation

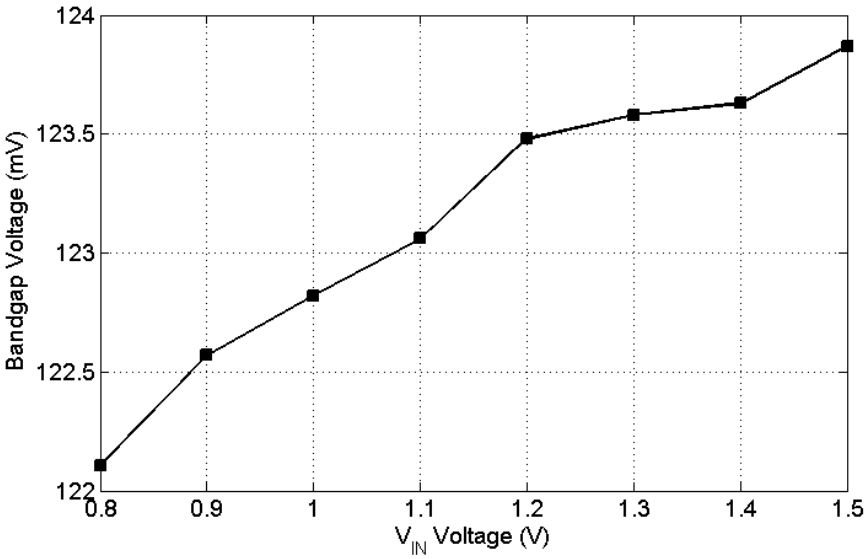


Figure 3-37 Variation with Vin Voltage

Table 3-2 Comparison summary with previous low power bandgaps

	[57]	[53]	[54]	[55]	[56]	This work
Power Consumption	300nW	1.85µW	13.6µW	20µW	170nW[1]	80nW
Technology	300nm	400nm	600nm	600nm BiCMOS	130nm	130nm
Area (mm^2)	0.055	0.1	0.055	0.4	0.07	0.0264
% variation with process	6	5.8	12	1.5	3	2.5
Temp. variation (ppm/^oC)	15	119	37	11	40	100
PSRR (%)	0.002%	0.138%	0.038%	0.0048%	0.005%	2%
Minimum Supply	1.4V	0.84V	1.4V	0.9V	0.75V	0.8V

[1]uses duty-cycling to reduce power

Table 3-2 compares this work with previously reported state-of-the-art low power bandgap circuits. Our work reports operation from minimum input voltage of 0.8V improving, which is similar to the reported least operating voltage circuit in [56]. Our power consumption is 80nW, which is over 2X lower than [56], achieved without duty cycling the reference. The work in [56] achieves a power of 170nW by sampling the reference voltage on a capacitor by periodically turning it on and off. Even lower power can be achieved in our work if duty-cycling is employed. The power supply variation is higher in our circuit because our architecture doesn't use current sources which are used in all of the previous architectures. The lower area of the circuit ($0.0264mm^2$) is achieved because big resistors are not used [55]. A low power, lower input voltage bandgap reference, which improves the power consumption by 2X and minimum operating voltage 0.8V, is presented.

3.4 Power Management Solution for ULP SoCs

In the previous sections, we presented the design of a boost converter energy harvester that can harvest energy from a thermo-electric generator, and a design of a low power bandgap voltage reference. The energy harvester circuit is used to harvest energy from low power ambient sources. It can harvest energy from a source with an ambient source voltage as low as 10mV, which is stored on an energy accumulator such as a battery or a capacitor. On the other hand, the bandgap circuit can be powered-up at a low voltage level of storage capacitor (V_{CAP}) which helps in reducing the start-up voltage of the system. The bandgap voltage itself is used for providing stable reference voltage. The output of these two blocks is used in our EHM system to provide multiple regulated output voltages for the voltage regulator circuits that are used to power different blocks of the system. This section talks about the design of the power management system that produces multiple output voltages to be used by the SoC.

3.4.1 Voltage Regulation for Integrated Circuits

One or more DC power supplies are needed for the functioning of different blocks inside a SoC. The power supply(s) is one of the most important design and system knobs for the SoC, which can determine several key performance metrics. Therefore, power supplies in a system are very well-regulated. There are several reasons to control the power supply. First, the operating voltage for a circuit can determine its operating frequency. Therefore, power supply is critical for the performance of the IC. Second, power supply also determines the power consumption of the circuit. Often, the performance and the power consumption of a circuit have contradictory attributes. A higher performing circuit would need a higher power supply and hence higher power. Therefore,

it is desirable to have a power supply that gives good performance, as well as restricts the power consumption. Figure 3-38 shows the energy-delay characteristics of a digital circuit obtained by changing the power supply, V_{DD}. It shows that energy consumption increases for a lower delay, which is obtained by operating the circuit at higher V_{DD}. Figure 3-38 shows that V_{DD} needs to be controlled to control power consumption or the performance of the circuit. The third main reason to control the power supply is to be able to operate the circuits within a safe operating voltage for better reliability. Fourth, a transient fluctuation in power supply can lead to a system shut down because of an internal set-up time or hold-time violation inside the chip. The other reasons to control power supply are meeting compliance for IO standards for chip-chip communications, maintaining good signal to noise ratio for analog circuits (sometimes for digital circuits as well), to maintain the functionality of memories, such as retention, etc. However, the power and performance needs of a system are the primary motivating reasons to set the level of power supply in most of the systems.

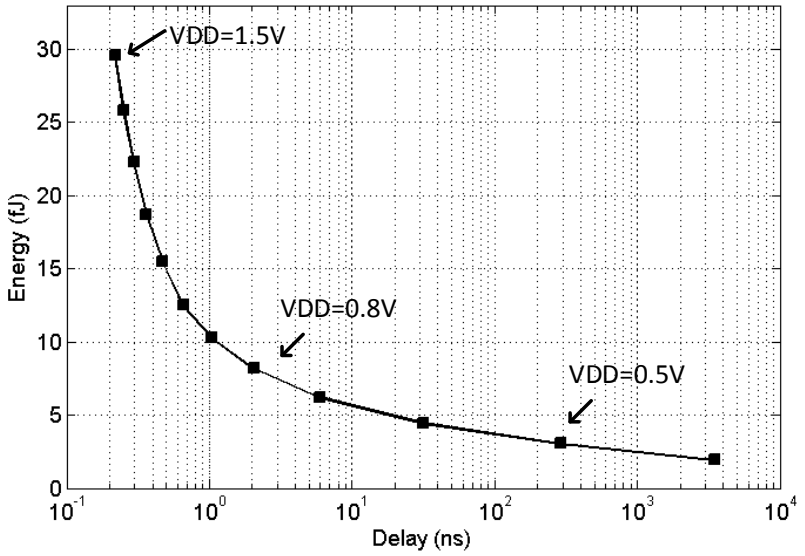


Figure 3-38 Energy-Delay characteristics of a digital circuit

Voltage Regulator Circuit: Linear Regulator

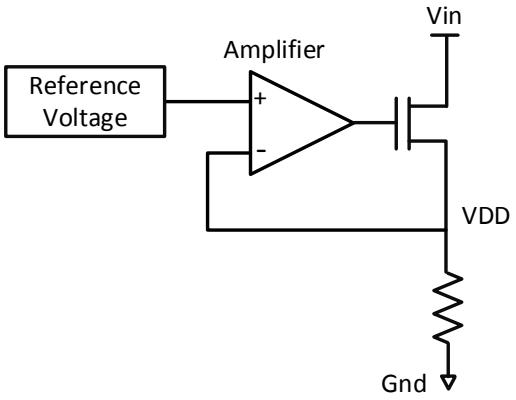


Figure 3-39 A linear regulator circuit to supply V_{DD}

Figure 3-38 shows that V_{DD} needs to be regulated to control the power consumption or performance of a circuit. A circuit that controls V_{DD} is shown in Figure 3-39, which is a linear voltage regulator circuit. A linear regulator circuit, as shown in Figure 3-39, is often sold as 3-pin IC by various semiconductor companies [60][61][62]. The three pins would be V_{in}, Gnd and V_{DD}. The circuit operates in the following way. A reference voltage, usually a bandgap reference, as described in Section 3.3, is used with an amplifier in a negative feedback loop. If V_{DD} goes a little bit below the reference, the feedback from the amplifier increases the gate voltage of the nMOS and supplies more current to raise the V_{DD}. Similarly, if the V_{DD} goes high, the current supply from V_{in} is reduced. The negative feedback keeps the V_{DD} voltage the same as the reference. A linear regulator circuit is small in size and has a very low noise at its output. In modern SoCs, the linear regulator circuit is often integrated. Since modern systems need more than one power supply, multiple linear regulators are integrated on chips to generate these supplies [1]. Further, lower quiescent current and better transient performance linear regulators have been reported for low power systems [63][64]. However, there are two main limitations of a linear regulator circuit when

used for low power applications. The first limitation is the low efficiency for voltage conversion. The efficiency of a linear regulator is given by,

$$\eta < \frac{V_{DD}}{V_{in}} \tag{3.26}$$

If the difference between V_{in} and V_{DD} is large, then efficiency can be very small. For a V_{DD} of 0.5V, with a V_{in} of 1.5V, the efficiency of the converter will be less than 33%. The second main limitation of the circuit is higher operating voltage. V_{in} always needs to be higher than V_{DD}. For an energy harvested system, it means that the voltage on the storage capacitor, V_{CAP}, needs to be higher than V_{DD}, which means that the energy stored on the capacitor cannot be used unless it reaches a threshold voltage that is higher than V_{DD}. For the BSN reported in [1], this voltage was 1.35V, because it needed to generate a 1.2V power supply.

To enable low voltage start-up for the system, we proposed a bandgap reference circuit in Section 3.3 that can provide stable reference at 0.8V of V_{in}. Further, the power supply(s) should become operational at low input voltages. For example, if the power supply is made available at 0.8V of V_{CAP} or V_{in}, then the system can start-up at 0.8V instead of 1.35V, which will increase the life time of the system. Therefore, there is a need to overcome the limitations of linear regulators to improve the life-time of ULP systems. Switching regulators provide better efficiency and can operate at lower V_{in} are proposed and explained in the next section.

Voltage Regulator Circuit: Switching Regulator

Switching regulators are broadly divided into two categories, inductor-based switching regulators and switched-capacitor regulators. The switched-capacitor regulators use the switching of capacitors to generate various ratios or multiples of the output voltages. The voltage inverter circuit,

shown in Figure 3-32, is an example of a switched capacitor regulator where an output is inverse of the input voltage. Recent works show that it is possible to achieve good efficiency for switched capacitor converters for given sets of output voltages [65][66][67].

There are certain advantages and disadvantages of using switched-capacitor techniques rather than inductor-based switching regulators. An obvious key advantage is the elimination of the inductor and the related magnetic design issues. Application circuits are simple, and are usually integrated for low power systems. As there is no need for an inductor, the size of the PCB implementing the system will be small. Switched-capacitor inverters are low cost and compact, and are capable of achieving efficiencies equal to or greater than 90%. The current output is limited by the size of the capacitors and the current carrying capacity of the switches. However, switched-capacitor voltage converters do not maintain high efficiency for a wide range of ratios of input to output voltages. Since the current input to output ratio is scaled according to the basic voltage conversion (i.e., doubled for a doubler, inverted for an inverter), regardless of whether or not regulation is used to reduce the doubled or inverted voltage, any output voltage magnitude less than $2V_{in}$ for a doubler or less than $|V_{in}|$ for an inverter will result in additional power dissipation within the converter, and efficiency will be degraded proportionally.

The inductor-based switching regulators give good efficiency for both varying input and output voltages. They can also start-up at lower input voltages V_{in} and can boost up from very low voltages, as was shown in Section 3.2. The rest of this section will talk about inductor-based switching regulator circuits. We will first present the basic principle behind an inductor-based switching regulator, then explain a multiple output switching regulator to provide multiple voltages

for an SoC. Finally, we will present an EHM (Energy harvesting and power management system), which harvests from solar cells and provides multiple regulated output voltages.

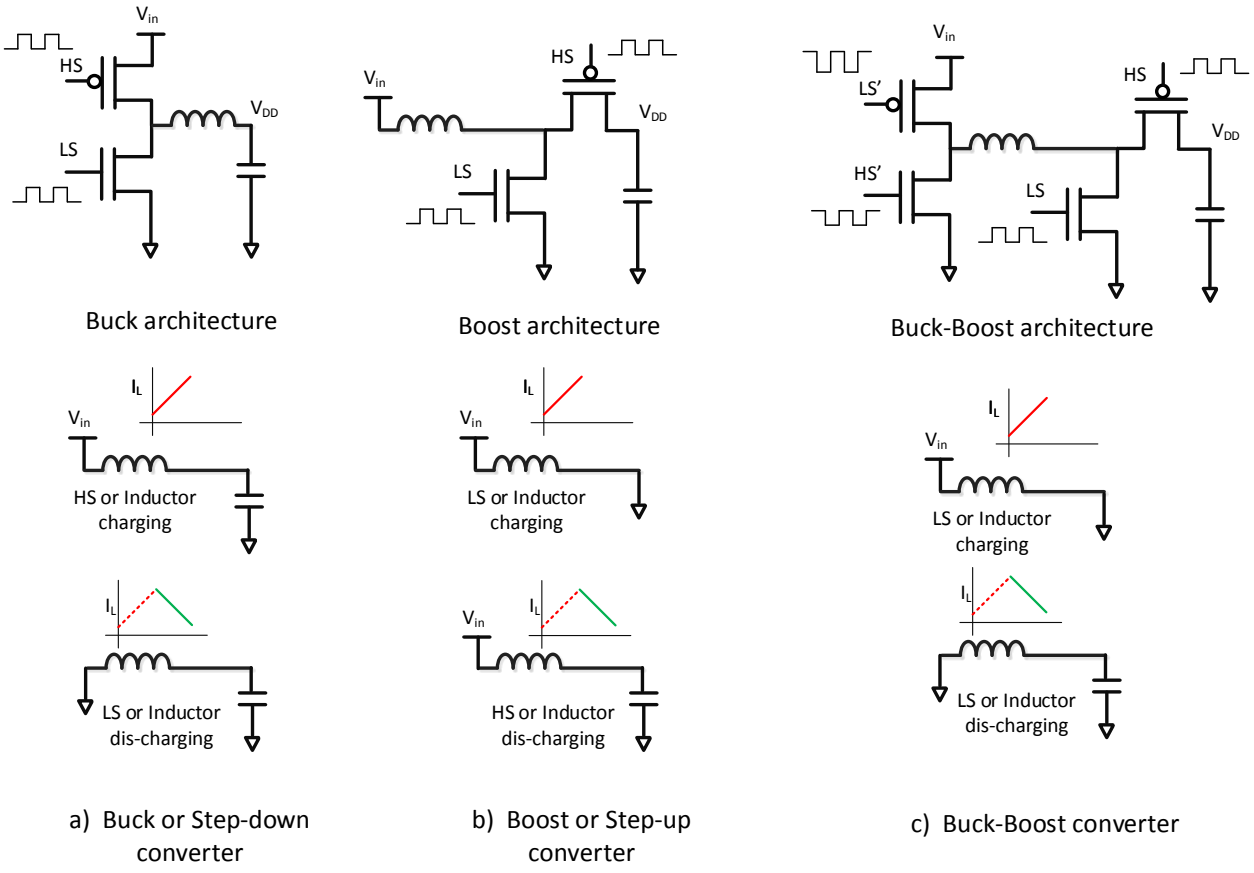


Figure 3-40 DC-DC converter architectures

Figure 3-40 shows the architectures of various DC-DC converters using inductors. The basic principle behind the operation of DC-DC converter involves charging and discharging of inductor current on a capacitor. In the first phase of a switching cycle, the inductor is charged and its current is raised, while in the second switching cycle, the inductor current discharges on the capacitor. The energy transfer takes place in electro-magnetic fashion where first, electrical energy is converted into magnetic energy in the inductor and then transferred back to electrical on the capacitor. The energy loss in this way is smaller and the efficiency of these converters is usually very high (in

~90% range). Figure 3-40 shows the architecture of three different kinds of DC-DC converters. Figure 3-40 (a) shows the architecture of a buck-converter, which is used to generate an output voltage V_{DD} lower than the input voltage V_{in}. In the first switching cycle, the inductor is connected between V_{in} and V_{DD}. Since V_{in} is higher than V_{DD}, inductor current starts increasing. After a set time, the high side switch (HS) is disabled and the low side (LS) switch is enabled, which configures the inductor between ground and V_{DD}. The inductor current discharges, transferring the stored energy onto the output capacitor. Figure 3-40 (b) is a boost converter and is used when $V_{DD}>V_{in}$. We covered the design of the boost converter in Section 3.2. Figure 3-40 (c) shows the architecture of a buck-boost converter when V_{in} can be higher or lower than the output voltages. Additional switches are used in buck-boost converters; therefore, their efficiency is slightly lower than the buck or boost converters.

Better efficiency and the ability to support (almost) any voltage conversion ratio are the main reasons for the wide scale use of the DC-DC converter. The low loss in a DC-DC converter is typically achieved by using low resistance switches (often big in size), lower parasitic loss in inductor and capacitor, and choice of switching control scheme for a particular application. However, implementation of a DC-DC converter requires external off-chip inductors and capacitors, which can increase the cost and area of the system. Also, multiple V_{DD}s are needed in a system, but multiple instances of the DC-DC converter cannot be implemented because of the cost and area. Therefore, linear regulators with lower efficiencies are often used to implement multiple V_{DD}s in a ULP system such as BSN [1]. There is a need to provide a low cost and efficient solution to implement multiple regulated output voltages for ULP systems. In the next section, we present low cost multiple output DC-DC converter design suitable for ULP systems.

3.4.2 Single Inductor Multiple Output DC-DC Converter for ULP Systems

Figure 3-2 shows the power management block of a BSN chip [1]. The BSN chip needs multiple rails for optimal power performance. The existing power management solution for the chip includes multiple linear regulators and a switched capacitor regulator to supply different rails. A linear regulator, such as an LDO, suffers from poor efficiency. The theoretical maximum efficiency of an LDO cannot be more than V_{DD}/V_{in}. Therefore, more than 63%, 26%, and 12% of the energy on the V_{DD} rails, 0.5V, 1.0V, and 1.2V gets wasted in obtaining the regulated V_{DD} voltage. There is a need to provide energy efficient solutions for the power management which can increase the lifespan of the BSN chip. This work proposes a highly efficient, single inductor, multiple output power management solution for BSNs.

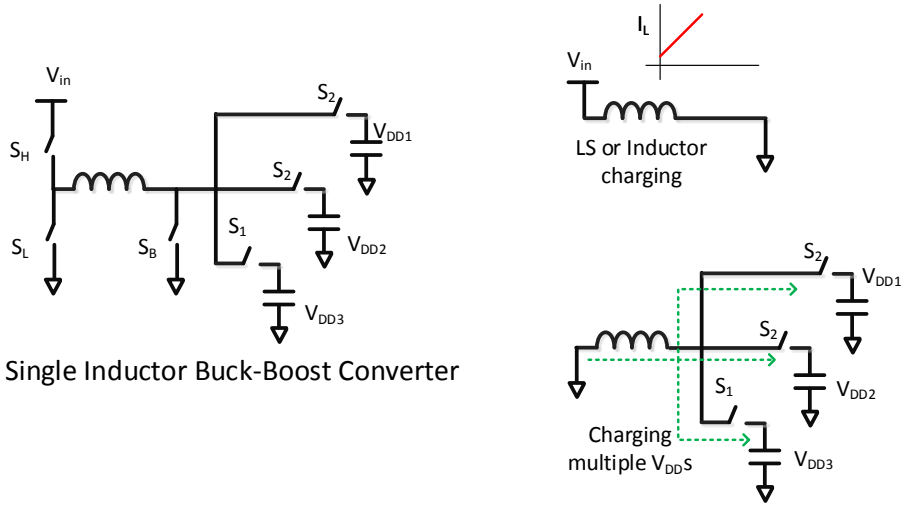


Figure 3-41 Single inductor multiple output buck-boost converter for ULP systems

The power management solution for ULP systems needs to meet the following three main requirements. First, the solution should be highly efficient; second, it should be low cost; and, third,

it should start operating at lower input voltage. Figure 3-41 shows the architecture of the proposed single inductor, multiple output DC-DC buck-boost converter for ULP systems. The use of a DC-DC converter ensures good efficiency for the converter. The use of buck-boost architecture enables operation at lower V_{in} voltage. Finally, a single inductor, multiple output design provides a low cost solution for the system. Single inductor, multiple output (SIMO) DC-DC converters have been proposed as a low cost solution for mobile applications [68][69]. The inductor is used by different V_{DD} rails in time-division, multiplexed (TDM) fashion for regulation. In this work, we propose the use of SIMO for ULP systems. Figure 3-41 shows the architecture of the proposed SIMO converter. When LS control is enabled, switches S_H and S_B are enabled and other switches are open. The inductor is connected between ground and V_{in}, which starts raising current in the inductor. After a set peak, current in the inductor LS control is disabled and switch S_L is closed, along with either S_1, S_2, or S_3. The stored energy in the inductor gets transferred in each of the three rails shown. The input voltage V_{in} can be lower or higher than all the V_{DD}s. This particular architecture enables low voltage, low cost, and efficient implementation of power management for a ULP system. The proposed architecture was implemented in 130nm CMOS process. We achieve a low voltage operation, from 700mV compared to 1.35V in [1].

In this section, we talked briefly about the SIMO buck-boost architecture to enable low voltage, efficient and low cost solution for ULP systems. The complete EHM solution will include an energy harvester to harvest from ambient sources, and a power management solution as shown in Figure 3-1. The EHM system is implemented using a boost converter and we explained the architecture in Section 3.2. Further, to enable low voltage operation for a ULP system, bandgap voltage reference and buck-boost architecture were covered in Section 3.3 and in the previous

section. The implementation of a complete EHM system is shown in Figure 3-42. A boost converter harvests from ambient sources, while the SIMO converter provides a solution for power management. This implementation required two inductors. A further improvement over this architecture is proposed, where a boost converter and power management are integrated. We propose a single inductor EHM system, where the boost converter and power management were merged into one solution. The next section shows the implementation of the proposed improvement using a photo-voltaic or solar cell (PV).

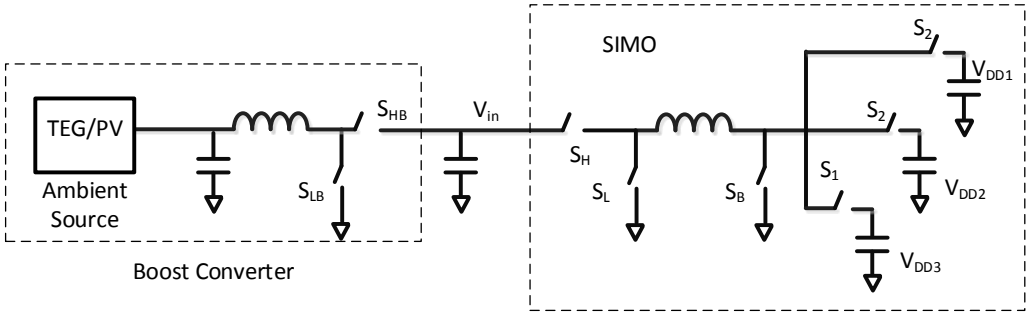


Figure 3-42 Architecture of the proposed EHM system

3.4.3 Single Inductor EHM for ULP Systems[2]

Energy harvesting from ambient sources, such as solar or thermal, is used to enable battery free operation of wireless sensors, body sensor nodes (BSN) [1] or Internet of Things (IoT). The energy harvested from a solar cell depends on illumination level and can vary greatly. The energy harvesting system needs to harvest energy efficiently, in varying conditions, to prolong the operational lifespan of the system. Further, BSNs, like most SoCs, need multiple supply rails to power core circuits, memories, and RF and IO cells. The existing solutions for BSNs use low drop out (LDO) regulators which have poor efficiency [1]. BSNs need an energy harvesting and power

[2] A lot of content of this section comes from [AS3] and [AS10]

management (EHM) system that can efficiently harvest energy from ambient sources, as well as provide the multiple regulated output voltages. The system also must be low cost for its widespread deployment. Single inductor multiple output (SIMO) EHM systems have been recently proposed to provide low cost and efficient solutions for BSNs [70]. In this section, we present a SIMO EHM system that can harvest from a solar cell (0.4V to 3.3V i/p voltage) to a storage capacitor or a battery interface. It also provides multiple output voltages (1.2V, 1.5V and 3.3V) at the same time, using the same inductor. It supports 0-5V output voltage for capacitive storage and 1.7-5V for a battery interface. It has a maximum power point tracking (MPPT) circuit, and an over-voltage and under-voltage protection scheme for battery management. A cold start-up circuit operating at minimum input voltage of 0.38V is also presented.

Architecture

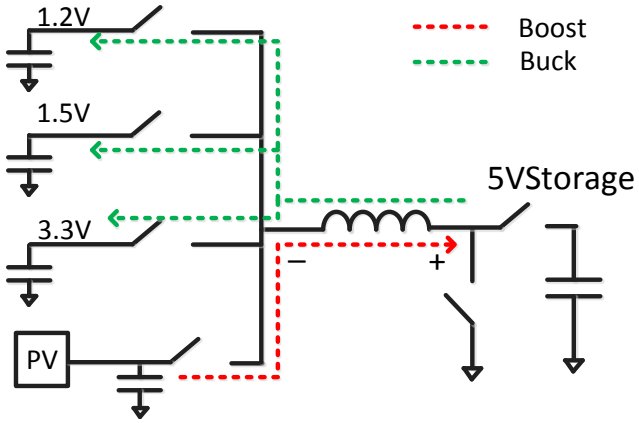


Figure 3-43 Proposed energy and power management solution using single inductor

Since the output power from a solar cell can be much smaller than the peak power needed by the system for applications such as RF communication, it is not possible to supply the V_{DD} rails directly from it. Therefore, the energy from the solar cell is first stored on an energy accumulator (a big capacitor or battery) and used to supply other V_{DD} rails [1]. Figure 3-43 shows the concept

of the switching scheme used in our EHM system. The energy from the solar cell (PV) is harvested and stored on the accumulator, and from there it is used to supply different voltages needed for a system. The arrangement of the switches in this way eliminates the need for additional switches to reconfigure the accumulator to supply in cases of high output load. This reduces the number of switches needed for EHM compared to [70]. The storage or battery is kept on the +ve side of the inductor and the PV module and regulated output voltage are kept on the negative side. The inductor current flows from the –ve of the inductor to the +ve terminal for storage. For supply regulation, the current flows from battery or storage into the loads (i.e from + to -) as shown in Figure 3-44.

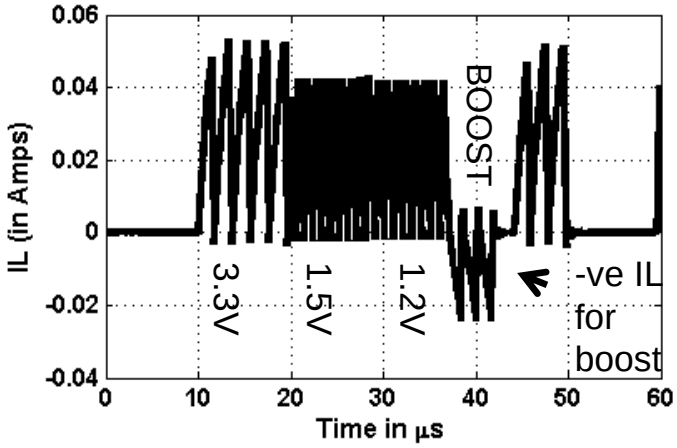


Figure 3-44 Inductor current waveform for the EHM switching scheme showing the change in direction of Inductor Current for boost operation

Figure 3-45 shows the complete architecture of the proposed EHM system. A SIMO control scheme is used with all the converters in the design, and operated in discontinuous conduction mode (DCM), using a pulse frequency modulation scheme (PFM), to achieve higher efficiency at light loads. Each converter generates two output signals, Busy and Ready. The Busy signal indicates that a particular converter is getting the service of the inductor, while the Ready signal

indicates that a particular converter needs to be serviced by the inductor. The switching control is performed by the Digital Controller. Using the Busy and the Ready signal from each converter, it generates an EN signal based on priority to enable a particular converter which, in turn, controls common switches MP and MN through signals HS and LS, as shown in Figure 3-45. The highest priority is assigned to the heavily loaded rail. The least priority is assigned to the energy harvester block.

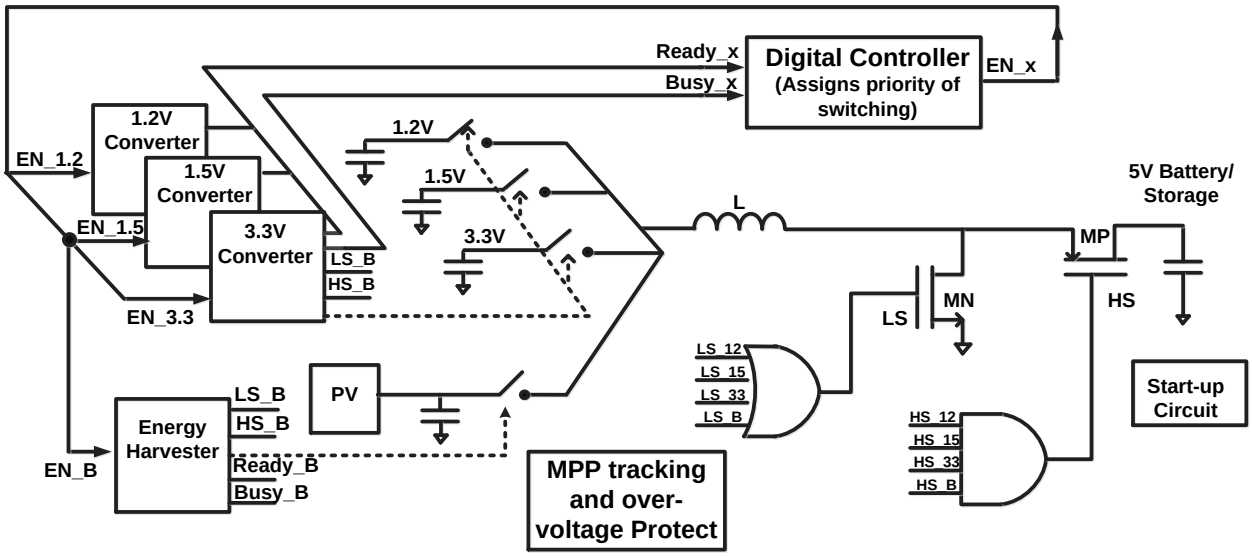


Figure 3-45 Complete architecture of the EHM System

Architecture of the buck-converter

In order to achieve maximum overall system efficiency across a wide range of output conditions, especially for light loads, each converter inside the EHM must also provide maximum efficiency. Figure 3-46 shows the control architecture of the buck converter used in EHM. It implements a PFM control scheme with peak inductor current (I_{PEAK}) control for high side switching and inductor zero current detection (ZD) for low side switching. A 70nA comparator is used for

regulation. If output rail is below Vref, the comparator output goes low which generates the Ready signal as shown in Figure 3-46. The digital controller sends an EN signal based on the priority of the converter to start the switching. The switching continues until the rail is charged above the reference voltage and the Busy signal goes to high. Once the rail is charged, the Busy and Ready signals go low and the inductor is made available for other rails. 70nA quiescent current, I_{PEAK} control, and ZD scheme enable high efficiency for the buck converter from 1µA to 30mA load current. While the ZD and comparator designs are conventional, the I_{PEAK} control scheme is novel and has not been previously implemented for micro-power converters. The conventional scheme to implement I_{PEAK} control uses a method where R_{DS} of a MOS transistor is matched with the switch R_{DS}, which is several orders of magnitude smaller than the representative MOS device. As a result, the method is sensitive to mismatch (+/-20%) and has large power overhead [46]. In this Section, we present an I_{PEAK} control scheme which is low power and less sensitive to mismatch, and similar to the I_{PEAK} scheme proposed for boost converter energy harvester in Section 3.2.

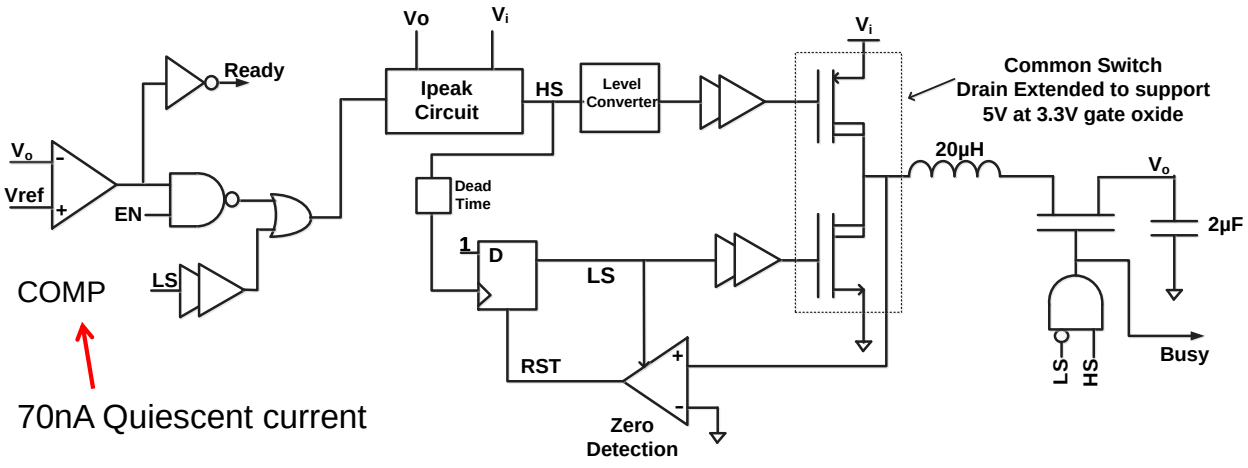


Figure 3-46 Architecture of the buck converter used in EHM

I_{PEAK} control for buck converter

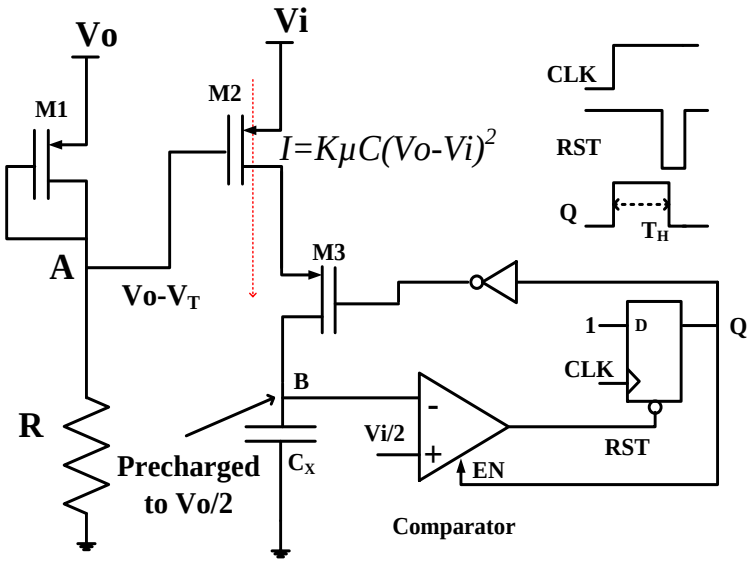


Figure 3-47 Peak inductor current control scheme in buck converter to achieve high efficiency

The need for controlling the peak inductor current for maximizing efficiency was shown in Figure 3-11 in Section 3.3.2 and Appendix C. If I_{PEAK} is high, the conduction loss in the converter dominates, while switching loss dominates when I_{PEAK} is low. Therefore, controlling the peak inductor current is necessary to optimize the efficiency of the converter. Figure 3-47 shows the circuit of the I_{PEAK} control scheme, which is explained as follows. A large resistor R sets the node A close to its threshold voltage of M1. Therefore, voltage at A is given by $Vo-V_T$ which goes to the gate of M2. Using long channel saturation current approximation of MOS transistor, the current in M2 is given by,

$$I= K\mu C(Vo-V_T-Vi+V_T)^2 = K\mu C(Vo-Vi)^2 \quad (3.27)$$

The capacitor is pre-charged to $V_0/2$. Figure 3-47 shows the HS turn on time T_H is given when capacitor C_X charges from Vo/2 to Vi/2. So T_H is given by,

$$T_H = C_X(Vi-Vo)/2I = C_X/2K\mu C(Vo-Vi) \quad (3.28)$$

Now, the peak inductor current is approximately given by,

$$I_P = (Vi-Vo)*T_H/L \quad (3.29)$$

Using equation (3.27),

$$I_P = C_X/2K\mu CL \quad (3.30)$$

The expression in equation (3.30) is independent of input voltage Vi and output voltage Vo, which enables wide input and output voltage range support for the system. It is also independent of the threshold voltage of the transistor. As a result, the peak inductor current is made to be constant. It is fixed by controlling the size of on-chip capacitor C_X at design time.

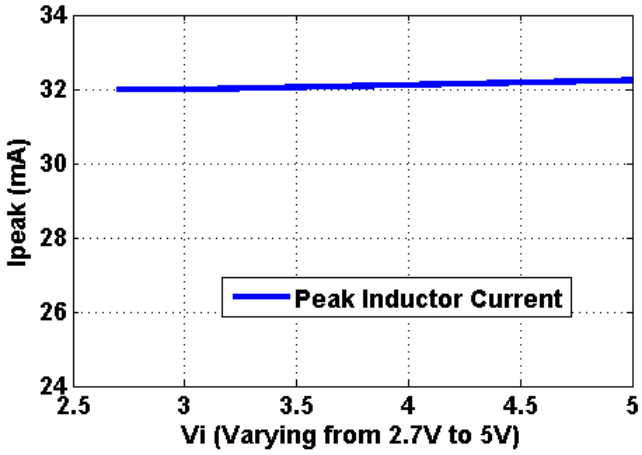


Figure 3-48 Variation of I_{PEAK} Vi showing <1% variation with Input Voltage Vi

The proposed scheme performs well when compared with conventional MOS R_{DS} methods. In this scheme, the timing is generated by the integration of charge on a capacitor from Vi/2 to Vo/2, which makes it less sensitive to mismatch. For example, if Vi is 5V and Vo is 1.5V, then the integration happens over 1.75V. Even a 100mV offset because of all the circuits involved in the

design results only in a mismatch of 6%. On the other hand, in the MOS R_{DS} method, the voltage drop across the switch is compared to a MOS transistor in linear region. Usually, the drop across the switches is very small, in the range of 50mV, which makes it very sensitive to mismatch [46]. Figure 3-48 shows the performance of the I_{PEAK} control scheme with Vi. It achieves less than 1% variation in I_{PEAK} with 2.3V variation in Vi. Figure 3-49 shows the monte-carlo simulation result for I_{PEAK} control and it shows +/-6% variation because of the process and mismatch which can be further controlled by trimming C_X in Figure 3-47.

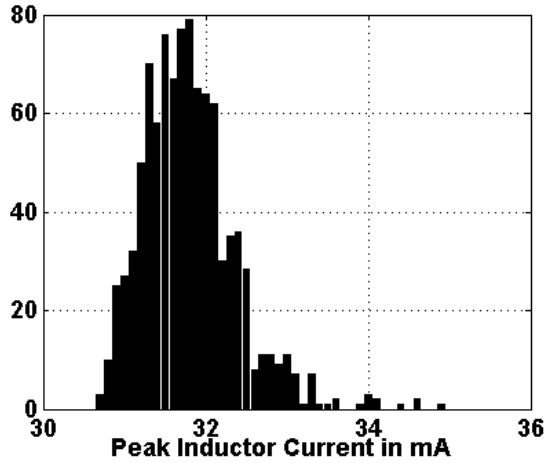


Figure 3-49 Variation of peak inductor current with process and mismatch variation

Architecture of the boost-converter

The circuit is designed using a 130nm 3.3V process with drain extended MOS transistor to support up to 5V operation to handle a wider range of different battery types, such as Lithium based battery chemistries, as well as store higher amounts of energy on the storage device. While the peak inductor current of the boost converter can be configured using a technique similar to the one used in Figure 3-47 , the conventional ZD cannot be used because of the reliability issues involved in

designing with 3.3V transistors. Figure 3-50 shows the control circuits to generate LS and HS timing signals for the boost converter. The LS signal is generated when C_Y charges from Vi/2 to Vo/2 and HS signal is generated when C_Y charges from ground to Vi/2, with their values given in Figure 3-50. The ratio of LS and HS times gives the boost converter ratio assuming the voltage drop across the switches much smaller than Vi or Vo. Therefore, the zero crossing of the inductor current in the boost converter can be accurately predicted by the given circuits. Figure 3-50 also shows the inductor current waveform for different input voltages, with different peak current showing accurate zero crossing, which helps in achieving wide input and output voltage range for the boost converter.

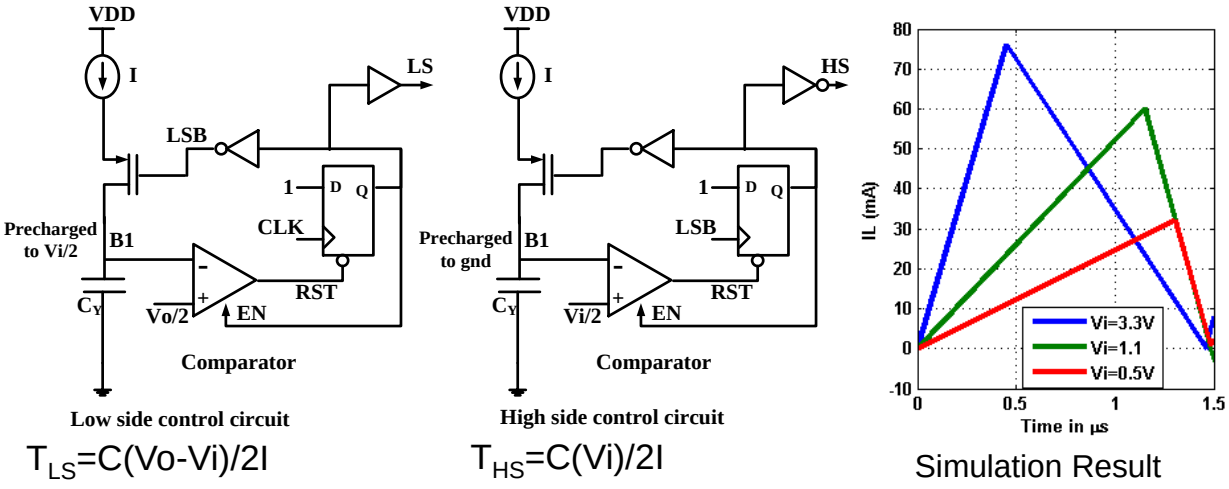


Figure 3-50 High side control scheme for the boost converter to accurately predict the zero crossing of the inductor current enabling reliable operation for 5V battery/storage using 3.3V devices

The boost converter also uses a PFM architecture with a constant voltage maximum power point tracking, which is well suited for a slow changing condition such as low illumination. The maximum power point tracking scheme is implemented to operate the PV cell at its maximum power point. The maximum power point of a PV cell occurs at ~76% of the open circuit voltage

[73]. The implementation of the MPPT control is similar to the MMPT control explained in Section 3.2 for TEG. Figure 3-51 shows the architecture of the boost converter circuit. The node V_{MPP} is set at 76% of open circuit voltage of the PV cell. The boost converter also has a buck-boost mode to harvest when output voltage is lower than the input voltage. A programmable over-voltage protection comparator is used to control the output voltage.

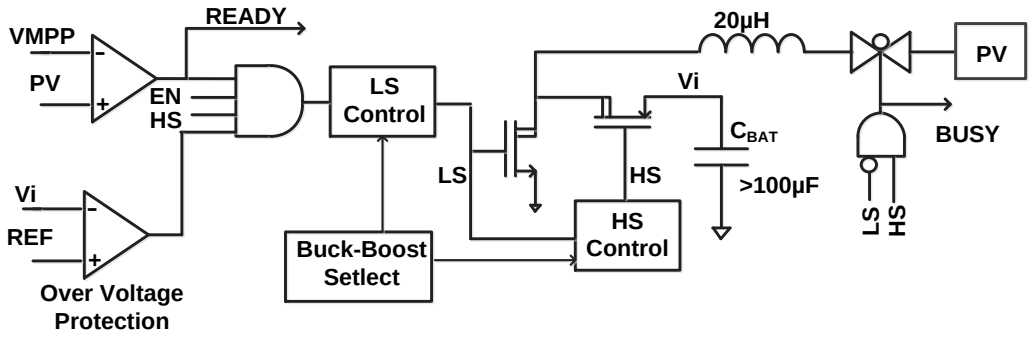


Figure 3-51 Boost converter architecture

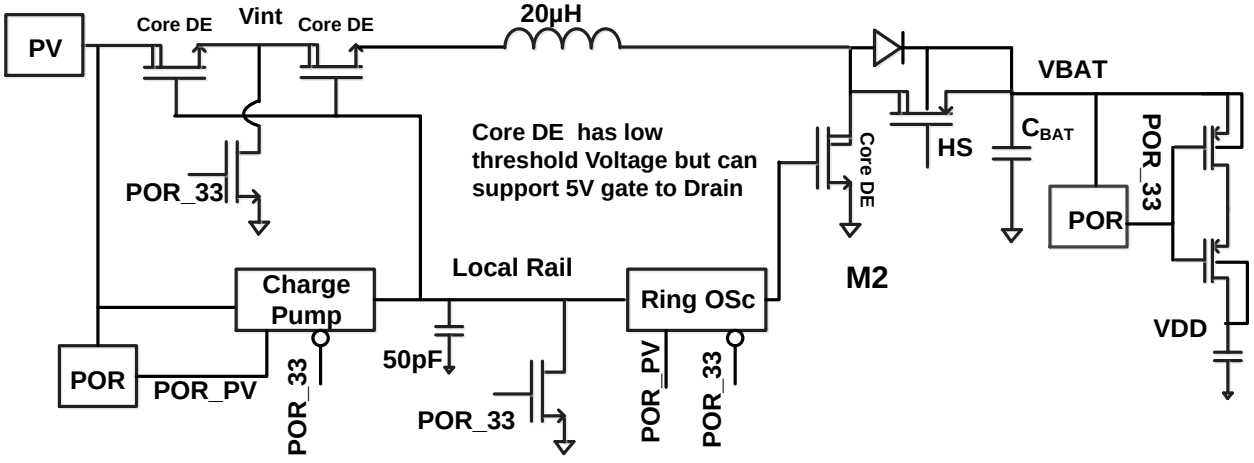


Figure 3-52 Cold start circuit using an internal charge-pump to start operation from 380mV

In this implementation, we also present a cold-start up circuit. Figure 3-52 shows the cold-start circuit. A local rail is produced using a charge pump circuit, which supports a ring oscillator to

control the switching during start-up. The process used doesn't support 5V gate to source operation. Therefore, the accumulator voltage cannot be used for internal circuits inside the converter, and instead the 3.3V rail is used. Since the circuit is powered by 3.3V rail in normal operation, it needs to be charged up during start-up as well. 3.3V rail and Storage node, V_{BAT}, are connected together during the cold start mode, as shown in Figure 3-52. Once V_{BAT} crosses 1.7V, the 3.3V rail can reliably handle switching. Therefore, the connection between 3.3V rail and V_{BAT} is removed and normal switching operation commences. The 3.3V buck converter and boost converter have buck-boost mode to take care of varying PV and V_{BAT} levels.

Prototype Implementation and Results

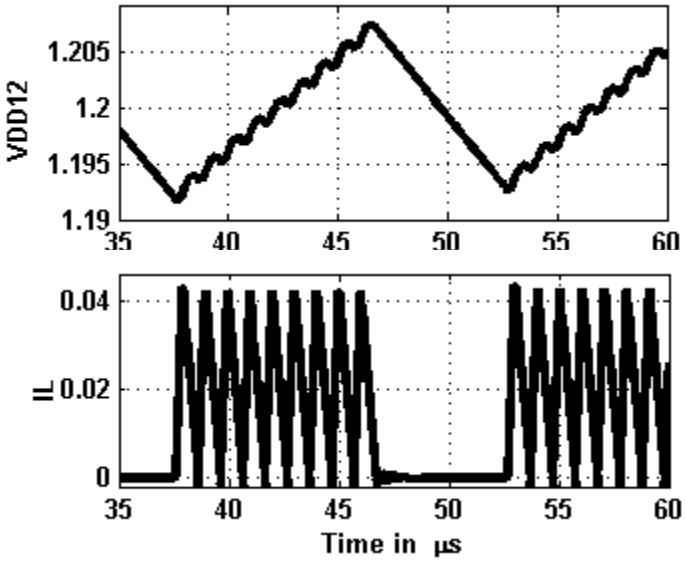


Figure 3-53 Voltage regulation output of 1.2V rail showing <15mV ripple

The proposed EHM system is implemented in 130nm CMOS process with drain extended devices to support 5V operation. Figure 3-53 shows the simulation result of the regulated output voltage at 1.2V, showing less than 15mV ripple at 10mA of load current. Figure 11 shows the

measurement result of the multiple regulated EHM output voltage rails coming out from the EHM system. It supports a peak load of 30mA on one VDD, with other rails lightly loaded, or a peak of 10mA on each VDD (max 30mA total).

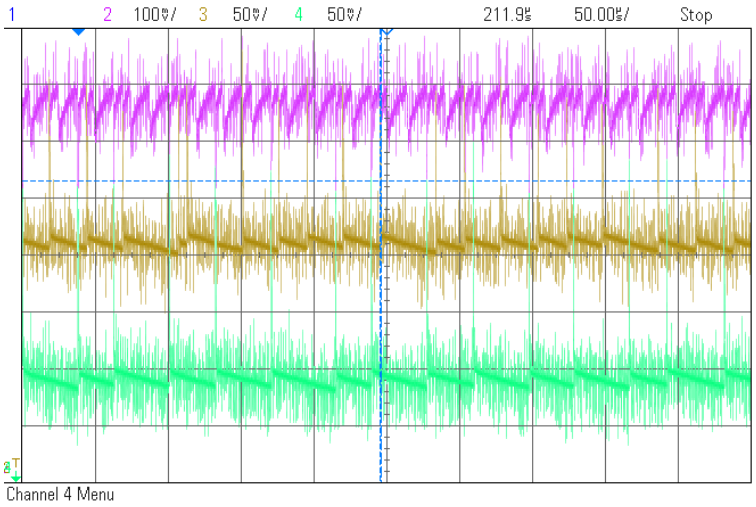


Figure 3-54 Measurement result of multiple output V_{DD}s coming at 1.2V, 3.3V and 1.5V

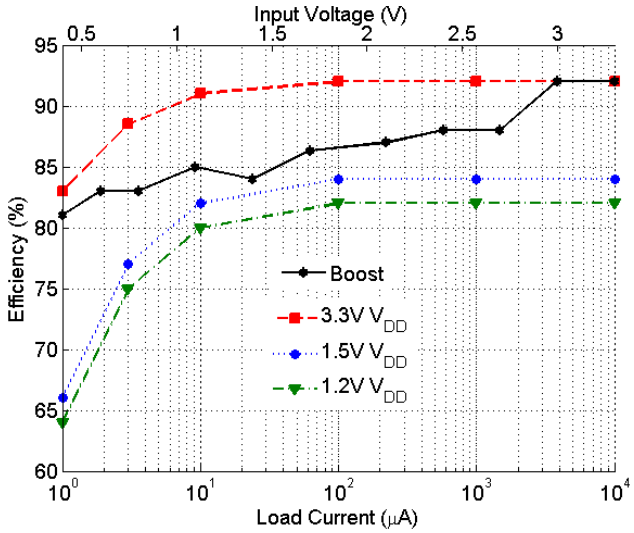


Figure 3-55 Efficiency of buck Converters

Figure 3-55 shows the efficiency measurements for the buck converters used in the SIMO converter. The peak efficiency is 92% on 3.3V rail at high load and 83% at 1µA load. The 1.2V

and 1.5V achieve peak efficiency of 82% and 81%, respectively, at high load condition, while 68% and 70% at 1µA load. The architecture supports a maximum of 30mA of load current which can support ULP systems such as a BSN [1]. Figure 3-56 shows the efficiency result of the boost converter. The boost converter achieves a peak efficiency of 90% at higher input voltages and an efficiency of 81% at 0.4V, Vin supplying 10µA of current. The circuit starts up at 380mV. Figure 3-57 shows the die-photo.

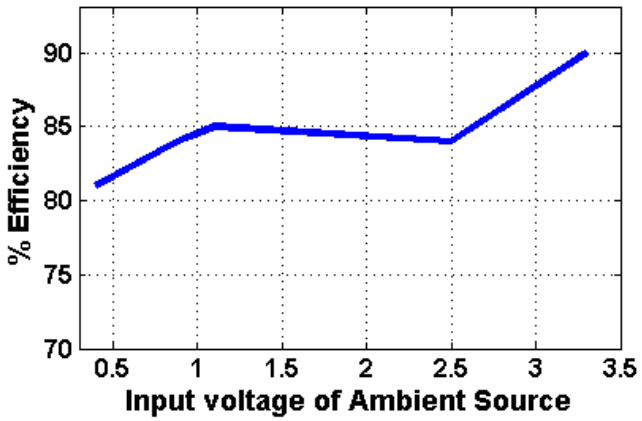


Figure 3-56 Efficiency of the boost converter

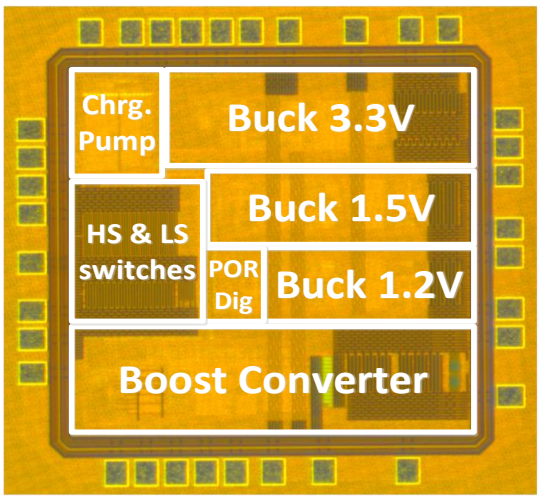


Figure 3-57 Die photo of EHM system

Table 3-3 Comparison with existing state-of-the-art harvesters

	[70]	[71]	[40]	This Work
Process	0.18µm	0.25µm	0.35µm	0.13µm
# of o/p	3	1	1	4
o/p Voltages	1V, 1.8V &3V	5V	0-3.3V	5V, 1.2V,1.5V & 3.3V
Efficiency	83% max @100µW, 67% @ 1µW, 70% @10mW	87%	80% @0.5V 95% @ 3V for boost	81% @ 0.4V, 92% @ 3.3V for boost* 92% @ high load, 83% @1µA for 3.3V buck * *(in SIMO)
Idle Power	0.4µW	2.4µW	1µW	1.2µW
Start-up	-	1V	0.33V	0.38V
Max. o/p V	3V	3V	3.3V	5V
Area (mm^2)	4.625	11.56	-	2.25
Max. Load	10mW	10mW	25mW	100mW
SIMO Reg.	✓	×	×	✓
Bat. Mgmt.	×	×	✓	✓
Cold start	×	×	✓	✓

Table 3-3 shows the comparison of the proposed EHM system with state-of-the-art energy harvesters. Among the reported work, this work is the first complete EHM system with energy harvester, multiple output regulated voltages for the system, a cold start circuit, a wide input voltage range 0.4-3.3V support, and a wide-output voltage to enable 5V operation. The solution in [70] has energy harvester and regulated output voltage, but it doesn't support wide input voltage range, battery management or cold-start. The solution in [40] provides battery management, but doesn't support voltage regulators. The static power consumption of the system is 1.2µW and is higher than [70] because of the implementation of all the control schemes needed for complete system design. The proposed I_{PEAK} control scheme enables efficient operation over a wide input-

output voltage range for the system. These features provide efficient energy harvesting and power management system for BSNs, WSNs or IoT.

3.5 Conclusions

In this chapter, we presented architectures to implement energy harvesting and power management solution for ULP systems. A thermoelectric boost converter combines an I_{PEAK} control scheme with offset compensation and duty-cycled comparators to enable energy harvesting from TEG inputs as low as 5mV to 10mV, 50% to 75% lower than prior work. Maintaining constant I_{PEAK} allows the converter to sustain high efficiency across a broad V_{IN} range, achieving 52% and 84% efficiency at 20mV and 400mV, respectively, which improves on prior designs. These features allow the converter to extend the operating window for thermal harvesting with low thermal gradients, which is ideal for body-worn sensors. We also presented a bandgap reference voltage circuit to enable low operating voltage for ULP systems. Our work reports operating from a minimum input voltage of 0.8V and achieving a lower power consumption of 80nW, which is over 2X lower than previous work achieved without duty cycling the reference. The proposed circuit also has the lowest area for bandgaps because big resistors are not used for lowering the power. Further, a power management solution that combines the boost converters and voltage regulators is presented to provide a completely integrated EHM solution. Among the reported work, this work is the first complete EHM system with energy harvester, multiple output regulated voltages for the system, a cold start circuit, a wide input voltage range 0.38-3.3V support, and a wide-output voltage to enable 5V operation. These features provide efficient energy harvesting and power management system for ULP systems such as BSNs, WSNs or IoT.

Chapter 4

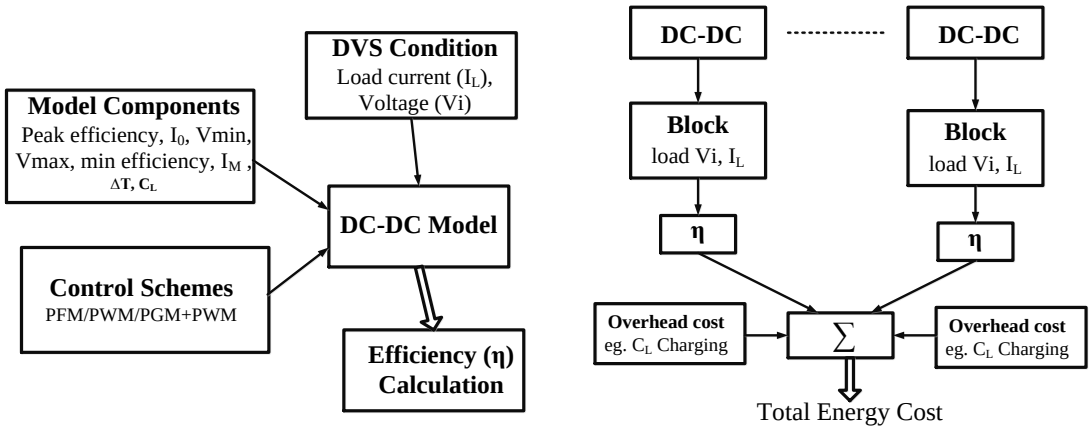
Modeling and Implementation of Power Management techniques for ULP Systems

We presented a low power clocking scheme and efficient, low voltage, low power EHM circuits in Chapter 2 and Chapter 3. These circuits improve the overall lifespan of a ULP system by decreasing the power consumption, increasing the harvested energy, and reducing the operating voltage of the system. Further improvement of ULP system lifespans can be achieved by employing power management techniques, such as dynamic voltage and frequency scaling (DVS). The improvements from DVS are orthogonal to the design improvements presented in Chapter 2 and Chapter 3. The application of DVS is achieved by changing the supply voltages. Design of DC-DC converters and their properties plays a significant role in the actual implementation of DVS. This Chapter presents a model of a DC-DC converter that can be used to study different power management techniques. The model helps us in studying the overhead and impact of various power management techniques reported in literature. Based on the model, we can determine the merit of one power management technique over the other. Further, a design of single inductor multiple output (SIMO) DC-DC converter is presented to implement a block level DVS, and panoptic dynamic voltage scaling (PDVS). The PDVS technique is studied using the proposed model and is identified as a more practical and efficient way to implement DVS.

4.1 Modelling for Power Management[3]

This section presents a model for inductor-based DC-DC converters and their application to quantify the benefits of power management techniques for ultra-low power (ULP) SoCs. Various power management techniques, such as dynamic voltage and frequency scaling (DVFS), clock gating, and power gating are now commonly employed in many SoCs. However, the power benefits of these techniques cannot be quantified accurately without assessing their impact on the DC-DC converter that delivers power. For example, DVFS uses a high voltage to support higher performance and lower voltage to save power. However, changing the output voltage of a DC-DC converter incorporates significant power overhead, and the efficiency can vary widely across voltage and current loads. These overheads may offset the benefits realized from DVFS. There is a need to characterize the benefits of power management techniques like DVFS in conjunction with their impact on the DC-DC converter. This is particularly important for ultra-low energy near- or sub-threshold systems that operate in a very dynamic power environment, and whose power constraints are stringent. This section presents a model that enables the study of power management techniques by taking into account their impact on DC-DC converters of different topologies. The model is based on an analytical treatment of inductor-based DC-DC converters, and it captures their efficiency trends with varying current load and output voltage. Since parameter selection will influence the specific behavior of the modeled converter, the model provides a rapid and effective tool for early design phase exploration of the impact of a converter, by using parameters based on different prior designs or by sweeping parameters to investigate the optimal design requirements for the overall system.

[3] A lot of content of this section comes from [AS9] and [AS4]



a) DC-DC efficiency modeling b) System energy cost model

Figure 4-1 Structure of the proposed model

Figure 4-1 shows the structure of the proposed model, which is broken into two parts. First, a model of inductor based DC-DC converters shown in Figure 4-1 (a) takes the operating condition of a workload as an input, which includes peak efficiency, load at which the peak occurs, minimum efficiency, maximum and minimum output voltages, settling time, and the decoupling capacitance of the DC-DC converter, and generates an efficiency calculation. In order to capture the dynamic load condition of the converter in the context of the operation of a specific power management scheme, the second part of the model shown in Figure 4-1 (b) uses one or more of the DC-DC converter models in a larger system model that includes the input voltage (Vi), output voltage (Vo), load current (I_L), time of operation, parasitic capacitance on the block, switching frequency, and activity factor. These parameters can change dynamically in power management techniques like DVFS. Using these parameters as input, the model calculates the overhead cost and change in the efficiency of each DC-DC converter in the system and provides the total system level energy consumed while executing a power management technique for the given workload profile.

The energy savings for a power management technique are typically reported at the load circuit operating voltage and load level in literature [75]. For example, the authors in [75] report the

energy savings obtained by scaling the voltage and frequency to a lower value. The paper does not calculate the total energy drawn from the original source of the supply voltage, for example a battery, which may not change linearly with load at the final circuit. Changing the operating condition of a voltage regulator causes deviation from its optimal behavior. If the output voltage of a buck converter is reduced, the efficiency of the converter decreases. Also, reducing the output voltage means that the capacitor C_L is discharged to a lower voltage by dissipating its stored energy. The actual benefits can be obtained by taking these losses and overhead into account. Figure 4-2 shows a block diagram of a typical inductor-based DC-DC converter. It includes a bias generator and comparators that cause the static loss. The control scheme that implements the switching pattern of the power switches MP and MN can vary across topologies. The switching loss is a function of the control scheme and the load. The power switches MP and MN, parasitic resistance of inductor (LPAR), and capacitor (CESR) cause the conduction loss, which is determined by the load current and output voltage. These losses are all a function of the operating condition. The proposed model accurately predicts the trends in behavior of DC-DC converters across topologies, implementing both pulse width modulation (PWM) and pulse frequency modulation (PFM) control schemes.

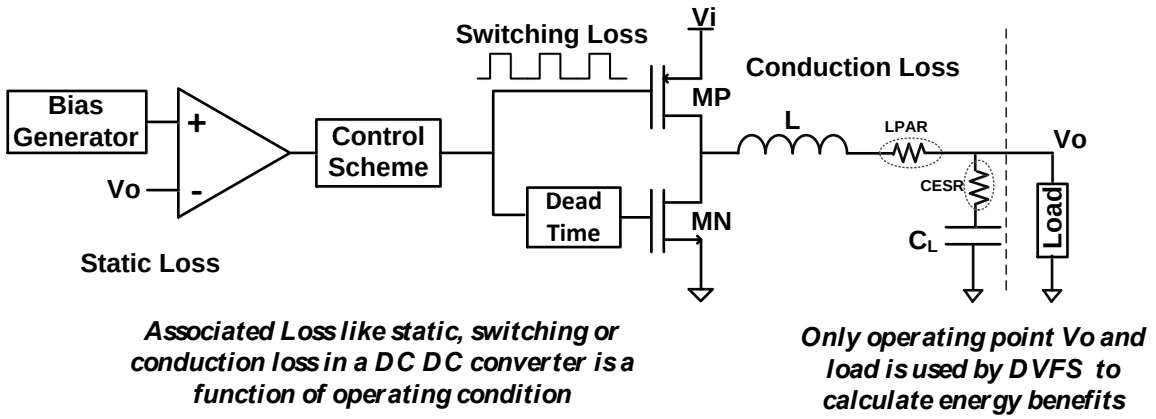


Figure 4-2 Loss mechanisms inside a typical switching DC-DC converter

4.1.1 DC-DC converter model

In order to model DC-DC converter trends and to capture the impact of DC-DC converters on power management strategies, it is essential to account for the converter efficiency, which is the power delivered to the load divided by the total power drawn by the converter. This efficiency of the DC-DC converter is a function of its output load, output voltage (Vo), the switching frequency, the switch resistance, and the parasitic resistance in the inductor and capacitor, as shown in Figure 4-2. In this section, we derive models for the efficiency for both PWM and PFM control schemes. Additionally, it is important to model how the converter will respond to changes in its usage. In a dynamic power environment like DVFS, Vo and load current vary dynamically, which changes the efficiency of the converter and results in energy overhead. Also, the converter can take significant time to settle from one voltage to another, resulting in timing overhead. Additional energy overhead comes in the form of charging and discharging of the decoupling capacitor. To quantify the benefit of a given power management technique like DVFS, we need to account for these overheads, in addition to modeling the efficiency at a fixed load. In this section, we derive and describe the proposed model for an inductor based DC-DC converter that accounts for these overheads and that can be used in a larger system model to study specific power management techniques.

DC-DC Efficiency with Load Current: PWM Control Scheme

Voltage and frequency are varied in DVFS to trade off power consumption with speed. This changes the load current and output voltage of the DC-DC converter, which changes its efficiency. In this section, we define a model that captures the change in efficiency that results from changing

load conditions. One prior work [76] models the power loss in a DC-DC Buck converter using a PWM switching scheme with the following equation:

$$P_{Buck} = a\sqrt{(I_L^2 + \Delta i^2/3)f_s} + b\left\{\frac{I_L^2}{\Delta i f_s} + \frac{\Delta i}{3f_s} + \frac{C_L {V_{DD1}}^2}{R_{L0}\Delta i}\right\} + d f_s \Delta i \quad (4.1)$$

where I_L is the load current, Δi is the current ripple in the converter, fs is the switching frequency, C_L is the decoupling capacitor, R_{LO} is the inductor series resistance, and *a*, *b*, and *d* are constants. Equation (4.1) represents the power loss in terms of various constants that cannot be obtained and that are non-intuitive to approximate prior to the design of the converter, so it is difficult to apply this equation for design space exploration or for general modeling of DC-DC converter trends. Instead, we propose a model that accurately captures the trends in the efficiency of the DC-DC converter in terms of the peak and minimum efficiency values of the converter, which can be either predicted, specified as targets, or pulled from prior work. To derive this simplified model, we begin by following previous work [76][77] in the observation that (4.1) leads to an efficiency in the form.

$$\eta_{I_L} = \eta_2 - (\eta_2 - \eta_1) * (\log(I_L/I_O))^2/4 \quad (4.2)$$

where η_2 is the peak efficiency occurring at load Io, and η_1 is the least efficiency at a given load. For the verification of the model proposed in equation (4.2), let us consider the following cases. For a light load condition in Equation (4.1),

$$I_L \sim \Delta i$$

so the power loss given by equation (4.1) in the buck converter takes the form of

$$P_{Buck} = \alpha I_L + \beta/I_L$$

The efficiency of the converter will be given by power delivered (VI_L) over power drawn:

$$\eta_{I_L} = VI_L/(VI_L + \alpha I_L + \frac{\beta}{I_L}) \quad (4.3)$$

Expanding equation (3) using Taylor's series we get,

$$\eta_{I_L} = V/(V+\alpha)\{1 - \frac{\beta}{(V+\alpha){I_L}^2} + \frac{\beta^2}{(V+\alpha)^2{I_L}^4} + \cdots\} \quad (4.4)$$

It is clear from Equation (4.3) that the efficiency decreases as load current decreases for the cases of light load conditions on the converter. The proposed equation in the model is given by,

$$\eta_{I_L} = \eta_2 - (\eta_2 - \eta_1) * (\log(I_L/I_O))^2/4$$

This expression also decreases for the light load condition, capturing the correct behavior of DC-DC converter efficiency trend. We know from Taylor's series that,

$$\ln(I_L/I_O) = -\{\left(\frac{I_O}{I_L} - 1\right) - 1/2\left(\frac{I_O}{I_L} - 1\right)^2 + \cdots\} \quad (4.5)$$

Since, $I_O \gg I_L$ and converting natural logarithm into logarithm of base 10 we get,

$$\log(I_L/I_O) = -2.303\{\left(\frac{I_O}{I_L}\right) - 1/2\left(\frac{I_O}{I_L}\right)^2 + \cdots\}$$

so the efficiency equation in (4.2) can be rewritten as,

$$\eta_{I_L} = \eta_2 - 2.303(\eta_2 - \eta_1)/4 * \{\left(\frac{I_O}{I_L}\right)^2 - \left(\frac{I_O}{I_L}\right)^3 + \cdots\}$$

$$\ln(I_L/I_O) = -\{\left(\frac{I_O}{I_L} - 1\right) - 1/2\left(\frac{I_O}{I_L} - 1\right)^2 + \cdots\} \quad (4.6)$$

$$Using, x > logx$$

The proposed model in (4.2) for the DC-DC converter reduces to (4.6) under light load, which follows the behavior of the DC-DC converter as reported in literature [76] and compares well with (4.4) with maximum efficiency η_2 in (4.2) can be obtained by equating the constants in (4.4) and (4.2),

$$\eta_2 = V/(V+\alpha) \quad (4.7)$$

Equations (4.2) and (4.6) are not bounded for the cases when I_L becomes very small, but they can predict the behavior for light load condition in a PWM control switching scheme based DC-DC converter with less than 5% error. Figure 4-4 shows this result.

Now consider the case when load is very high compared to the point of peak efficiency. The constant *a* in equation (4.1) represents the resistance of the MOS transistor used for switching [76]. The model of [76] assumes it to be a constant. However, the resistance of the MOS transistor increases with the increase in load current and it is given by,

$$R_D = K * (1 + \frac{I_L}{I_{DSAT}}) \tag{4.8}$$

where I_{DSAT} is the saturation current of the transistor. Clearly, as load current increases, resistance increases. For light load condition, it is correct to assume that resistance doesn't change, as I_{DSAT} is much larger compared to I_L. However, with an increase in load, the MOS resistance increases, causing elevated conduction loss. Also, at higher load the increased current in the inductor causes elevated conduction loss in the inductor's parasitic resistance. Overall, the I^2R loss increases, because of the increase in current and because of the increase in resistance caused by that increase in current. For a high load we know that,

$$I_L \gg \Delta i$$

so the power loss in the buck converter using equation (4.1) of [76] takes the form of,

$$P_{Buck} = \alpha_1 I_L + \beta_1 I_L^2$$

The equation for efficiency can be written as,

$$\eta_{I_L} = VI_L/(VI_L + \alpha_1 I_L + \beta_1 {I_L}^2) \tag{4.9}$$

This expression shows that efficiency decreases as the load current increases. Using Taylor series expansion, this expression can be written as,

$$\eta_{I_L} = V/(V+\alpha_1)\{1 - \frac{\beta_1 I_L}{(V+\alpha_1)} + \left(\frac{\beta_1 I_L}{(V+\alpha_1)}\right)^2 + \cdots\} \quad (4.10)$$

In the proposed equation in this paper, equation (4.2), the efficiency also decreases for the higher load. Expanding (4.2) using Taylor's series,

$$\eta_{I_L} = \eta_2 - (\eta_2 - \eta_1)/4 * \{k1 + k2\frac{I_L}{I_O} + k3\left(\frac{I_L}{I_O}\right)^2 + \cdots\} \quad (4.11)$$

Equation (4.11) and (4.10) follow closely, with constants η_2, η_1, $k1$, etc. in (4.11) can be obtained by equating with respect to the powers of I_L in (4.10). The proposed equation matches the trend of equation reported in literature [76].

While equation (4.1), (4.4) or (4.10) can be more analytical versions of the DC-DC converter efficiency formulation, they are not very useful for early design space exploration or for studying system level power management techniques because of the unknown constants. In contrast, the compact model in (4.2) can be expressed in terms of peak efficiency and minimum efficiency, making it easy to use.

DC-DC Efficiency with Load Current: PFM Control Scheme

In the PFM control scheme with a constant peak inductor current, the switching and conduction loss scale with frequency, and the efficiency remains flat for higher loads. The power loss is given by,

$$P_{Buck} = K * P_{Out} + C \quad (4.12)$$

where K and C are constants. The first term indicates switching and conduction loss that scales with frequency. The second term indicates the static loss that does not scale with frequency. Therefore,

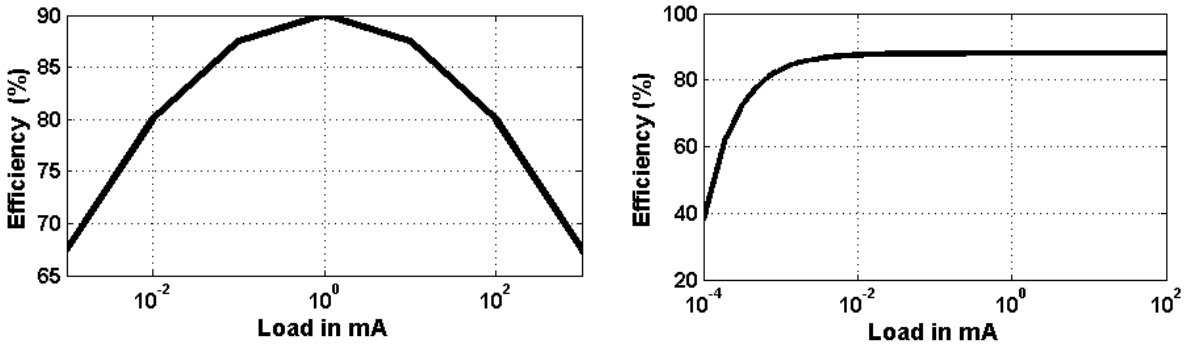
$$\eta_{I_L} = \frac{P_{Out}}{(P_{Out} + K * P_{Out} + C)} \tag{4.13}$$

Using $P_{Out}=VI_L$ and expanding using Taylor series,

$$\eta_{I_L} = \eta_2 - \frac{a}{I_L} \tag{4.14}$$

Equation (4.14) shows that the efficiency increases and becomes constant as load increases. This happens because power loss in PFM schemes scales with the load. At light load condition, the static loss dominates and reduces the efficiency.

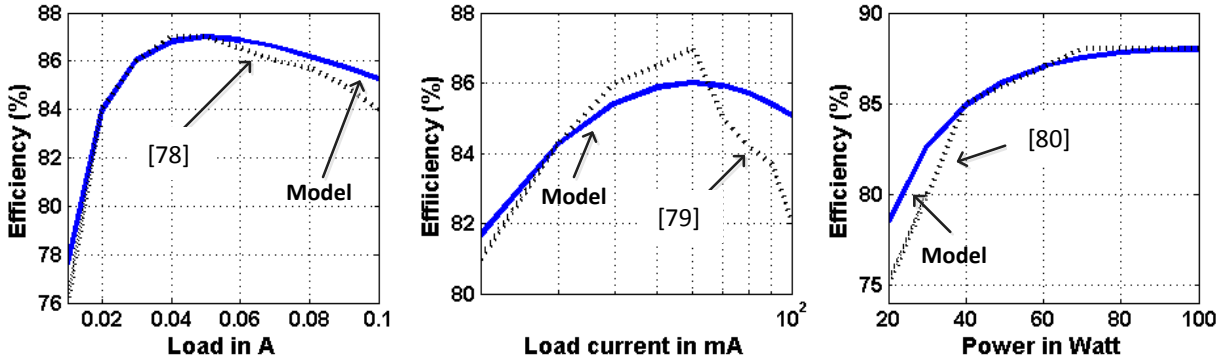
Verification of the model:



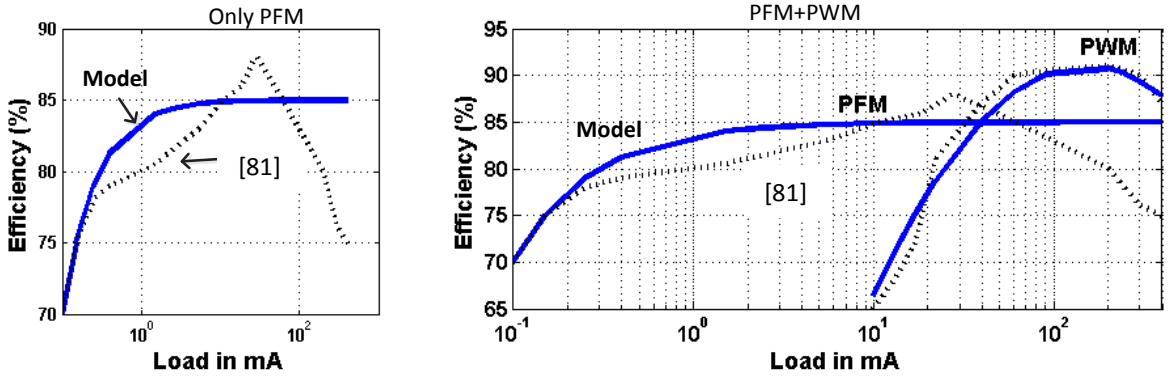
a) Efficiency Variation in PWM b) Efficiency Variation in PFM

Figure 4-3 Efficiency Variation with load current in a) PWM scheme with η_2=0.9, η_1=0.68 and I_L=1mA b) PFM scheme with η2=0.88 and a=5x10-5

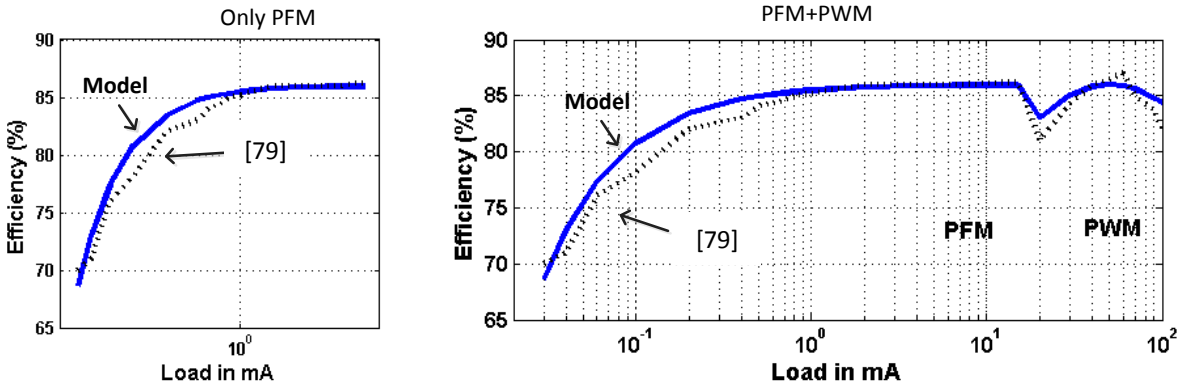
The equations we have provided accurately model the trends for PWM, PFM, and combinations of those control schemes. Figure 4-3 shows the variation of efficiency with respect to load when using dedicated PWM and PFM control schemes. In the PWM scheme, the efficiency degrades at high load and at light load conditions, while in the PFM scheme the efficiency remains flat as load increases and degrades at light load conditions. Figure 4-4 shows the comparison of the model



a) Comparison of model with the measured PWM DC-DC converter reported in literature



b) Comparison of model with [8], implementing both PFM and PWM



c) Comparison of model with [6], schemes implementing both PFM and PWM

Figure 4-4 Comparison of the load equation with measured work in literature

equations for PWM and PFM control schemes, with the measured results reported in literature [78]-[81]. Figure 4-4 (a) shows the results for the PWM scheme. For equation (4.2), we have selected η_2 as the peak efficiency reported in the corresponding paper and I_O as the load for that

peak efficiency. The value of η_1 is obtained experimentally, based on [78]-[81], and we set η_1=10 for all the papers ([78]-[81]) employing the PWM control scheme. The converters [78]-[80] and [81] in part implement PWM. We find that the model predicts the efficiency behavior of the converters very accurately (<5% error for these papers). For [78], [80], and [81], the error is less than 3%.

We also compared the model with reported works that employ the PFM switching scheme. Figure 4-4 (b) and Figure 4-4 (c) show the results. For the PFM scheme, we used η_2 as the peak efficiency reported in the corresponding paper. The constant *a* represents the static loss of the converter and will vary from one converter to another. It causes the degradation in efficiency at light load condition in a PFM control scheme. For this comparison, we set the value of constant *a* in (4.14) to match the least efficiency reported in each paper. The model predicts the behavior of [79] correctly for the PFM scheme, while it deviates at higher load for [81]. This is because we assumed in our model that the PFM scheme is used only for a light load condition, whereas [81] shows results for loads up to 400mA.

To further illustrate the usefulness of the model, we also compared it with the schemes where both PFM and PWM schemes are employed. This is often done to increase the range of load a converter can support. Figure 4-4 (b) and Figure 4-4 (c) show the results of comparison of the model, with efficiencies reported in [79] and [81]. The model accurately predicts the behavior of such converters. There can be other combinations in which the model can be used. For example, it can be used for a segmented switch scheme if two or more curves for (4.2) are used in conjunction, with each curve having a peak efficiency (η_2) corresponding to a different value of I_O.

The proposed model is accurate in predicting the efficiency trend with respect to the load if the control scheme is PWM or PFM. Also, an approximate peak efficiency of a DC-DC converter can be obtained very early in the design cycle, as it is dependent on the technology, size of the inductor, and ripple on rails. Therefore, the model can be employed for analyzing the DC-DC converter overheads early in design, while implementing power management techniques.

Efficiency with Output Voltage

The peak efficiency of an inductor-based DC-DC converter decreases with a decreasing output voltage. For a given load current, the switching loss and conduction loss of the converter remain the same. The decreased output power level at lower voltages results in decreased efficiency. The efficiency as a function of voltage can be modeled as,

$$\eta_V = \eta_1 + m(V - V_{min}) \tag{4.15}$$

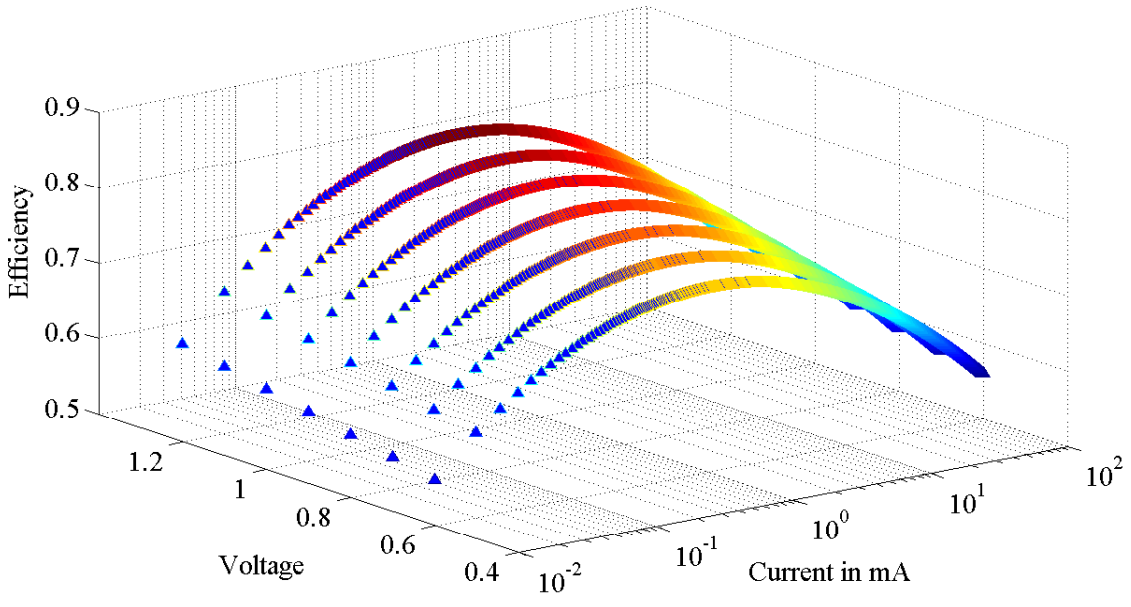


Figure 4-5 Dynamic efficiency variation with current and voltage

where *m* is the slope of the line given by $m = (\eta_2 - \eta_1)/(V_{max} - V_{min})$. This approximate linear behavior is reported in both [76] and [78]. Plugging (4.2) for PWM or (4.14) for PFM and using (4.15), lets us write the combined voltage and load efficiency as:

$$\eta = \eta_V * \eta_{I_L} \tag{4.16}$$

Figure 4-5 shows the output of the proposed model with V_O and with load current assuming a PWM control scheme. A DC-DC converter designed for a specific voltage and load will follow this trend when its load current or output voltage changes.

Settling Time

The settling time of a converter is the time it takes to reach the desired supply voltage. A typical converter has a large inductor and a large filter capacitor that makes the settling time very large (few µs to ms [82]). In a dynamic environment such as DVFS or Ultra DVS (UDVS), the output voltage V_O is expected to change. The settling time of a converter to reach the desired voltage becomes an important overhead for these scenarios. The settling time ΔT in our proposed model is approximated as,

$$\Delta T = \frac{T}{V} * \Delta V \tag{4.17}$$

when output voltage is charged to V from ground, and where T is the settling time of the converter. We assume that the inductor carries the same amount of current for each cycle of charging. Consequently, the rate at which the output reaches a given voltage will be linear with time. T/V is the slope of this curve and is set by assuming that at each switching cycle the inductor carries the same amount of current even for the cases when the output voltage is rising from zero.

Supply Rail Switching Energy

The change in the output voltage of a converter results in a change of the stored energy on the capacitance of the supply voltage rail of the load blocks. Some of this stored energy is dissipated if the new voltage is lower than the previous voltage, whereas energy is consumed from the source supply, Vin, if the new voltage is higher than the previous voltage. The additional energy overhead Ec is given by equation (4.18), where V_1 and V_2 are the new and previous voltages of the converter. If V1 is greater than V2, work is to be done by the supply Vin. When V1 is less than V2, no work is done by Vin; hence, energy overhead will be zero.

$$E_C = V_{in} C_L \max(V_1 - V_2, 0) \tag{4.18}$$

In some cases, the voltage on the capacitor is not immediately discharged to lower voltage. V_{DD} slowly discharges from V2 to V1 while running workloads. In such cases, E_C will be lower than given by equation (4.18). Equation (4.16) helps us to predict the losses at a given load or voltage condition, while (4.17) and (4.18) give the conversion energy and timing overhead. These equations enable a framework where overheads that originate from dynamic changes to the DC-DC converter output can be calculated for techniques like DVFS to accurately measure their energy benefits.

4.1.2 Evaluation of DVS techniques using the proposed model

The DC-DC converter model can be used for assessing a variety of block level power management techniques. Since the model captures both the efficiency of the converter for fixed loads and the cost of making dynamic changes to the converter output voltage and load, we can use it to model system level implementations of varying complexity. In the most basic case, the model can provide additional insight into the system level cost of reducing the voltage delivered to a block or to a

chip. For example, Figure 4-6 shows the measured energy consumption of a microcontroller in a sub-threshold system on chip [86] across voltage. The minimum energy voltage occurs at below

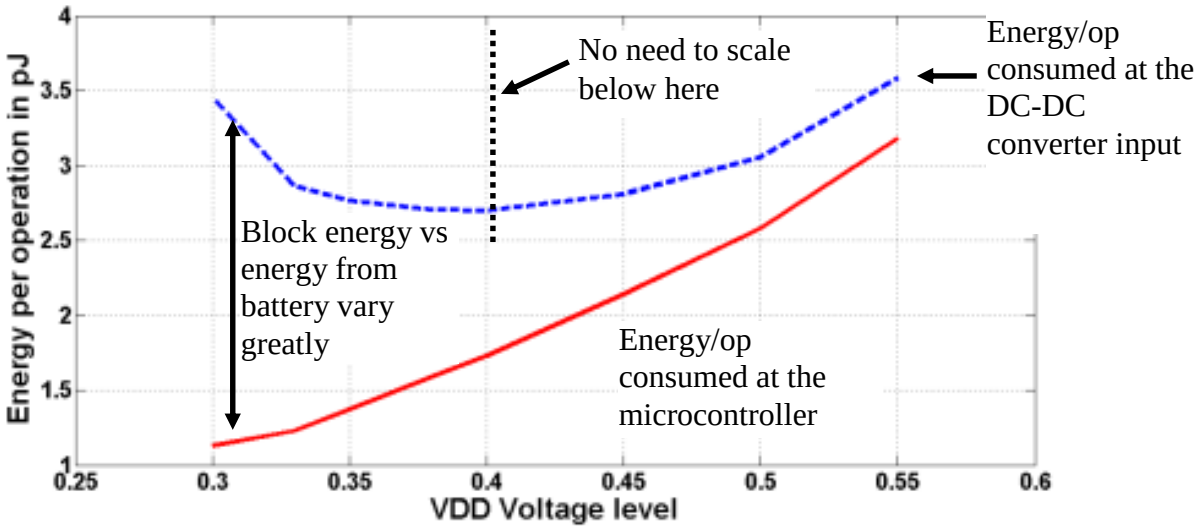


Figure 4-6 Energy consumption for a microcontroller across voltage with and without consideration of the DC-DC converter efficiency.

0.3 V. However, when we consider the amount of energy drawn from the battery or energy storage node, including the overhead of loss in a DC-DC converter, the situation changes significantly. The top line in Figure 4-6 shows the energy consumed from the source (at the input to the DC-DC converter) using our model, which was fitted to low load DC-DC converter measurements from [87] to illustrate an example converter for this system. Since the output voltage and load current both vary for the block as V_{DD} decreases, it is not accurate to assume a constant efficiency loss in the converter, and our model captures the changing efficiency across the space. This result shows that reporting block level consumption only can result in an inaccurate view of the total impact on the battery, and that the actual optimal voltage [92] for minimizing energy consumed at the battery may be higher than anticipated from block measurements alone.

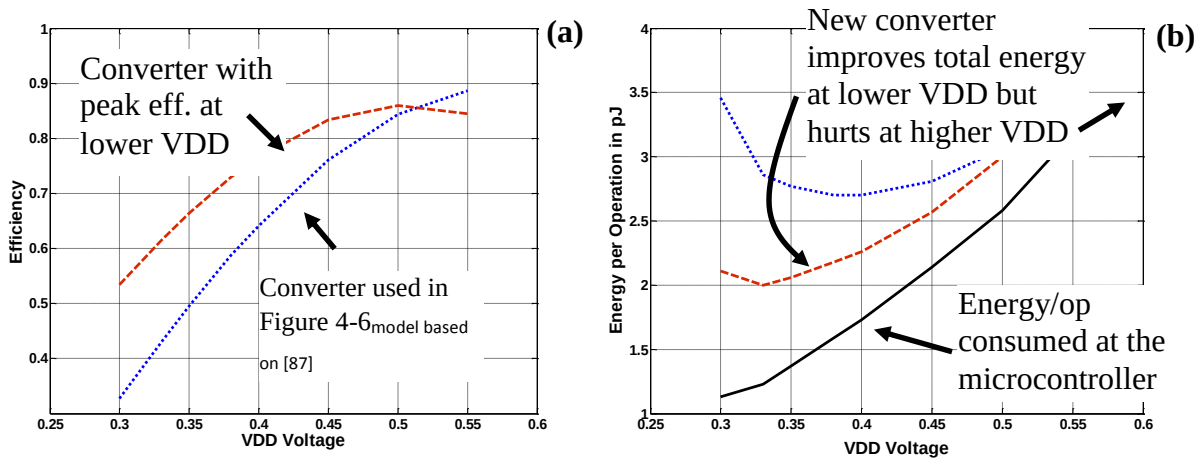


Figure 4-7 Efficiency profiles for two different converters (a) and the impact of a converter change on the overall energy drawn from the battery (b)

Further, the DC-DC model can help designers to choose the optimal specification for a converter to use for a given block or chip. This is especially important for embedded converters serving extremely low power systems like the one in [86], which operates from harvested energy. For example, we revisit the design in Figure 4-6 and consider a different converter design with lower overall peak efficiency, but whose peak efficiency occurs at a lower voltage. Figure 4-7 (a) shows the efficiency versus V_{DD} for two different converters: one is the converter used in Figure 4-6 and modeled on [87], and the other is a hypothetical converter. The new converter has a lower overall peak efficiency than the original design, which might lead to the misconception that it will hurt the overall energy consumption of any chip. However, its peak efficiency comes at a lower voltage, so its efficiency scales better across the lower range of voltage values. The impact of this is that, at lower voltage (and lower current) values, the second converter provides more efficient operation. Figure 4-7 (b) shows the impact of using this converter alongside the curves from Figure 4-6. Not only is the total energy drawn from Vin much lower, the optimal voltage for minimizing energy

occurs at a voltage much nearer to the optimal voltage of the block. The flexibility of our model allows a designer to experiment with different converter specifications while co-designing an embedded converter with its loading system, providing for rapid design space exploration early in the system design process.

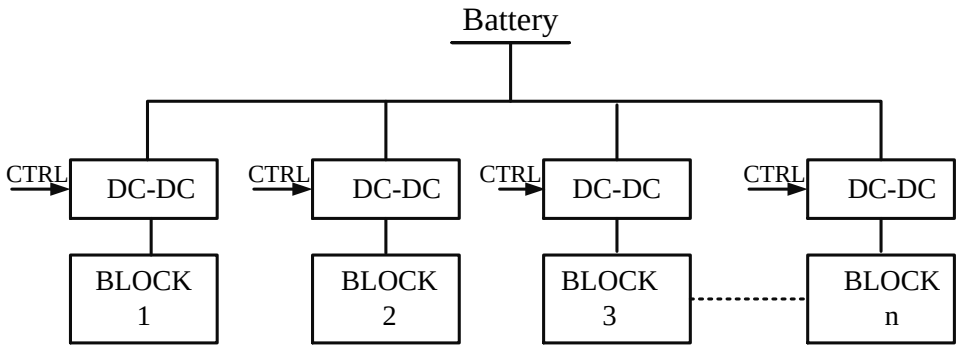


Figure 4-8 Dedicated DC-DC converter per block.

In addition to supporting the co-design of embedded DC-DC converters, our model can enable higher level comparisons of power management techniques that apply to multiple blocks. The next example illustrates the application of our model to two different power management strategies.

DVFS is commonly used to save power in a SoC by changing the supply voltage at the full chip level. Even larger energy savings can be realized by implementing block level DVFS, so that each block can use a voltage that is best matched to its own workload. Figure 4-8 shows the idealized implementation in which each block has a dedicated DC-DC converter. However, it may not be practically possible to implement such a system because of the area and cost of replicating DC-DC converters for each block. We study this scheme using our model to analyze its benefits by taking into account the overheads discussed earlier in the chapter. Later on, we compare this with a more practical implementation of block level power management.

VDD	Load	Time of operation
V1	i1	T1+ΔT1
V2	i2	T2+ΔT1
……	…….	…….

Optimal Condition for a Block

VDD	Load	Time of operation
0.9V	100µA	8µs
1.2V	900µA	8µs
……	…….	…….

Example Table

Figure 4-9 Operating condition for dedicated DC-DC.

Framework for Energy Calculation in DVFS

In this section, we establish the framework for computing the system level energy consumption of a multiple block DVFS system, where individual DC-DC converters are modeled using the equations from Section 4.1.1. Figure 4-9 shows the operating condition of an example block that has a dedicated DC-DC converter. V_{DD} and load will change with time. We have assumed a uniform random distribution for the power supply voltage setting in the range of 0.4V to 1.2V. ΔT is the settling time of the converter, and we use T=20µs and V=1V in equation (4.18) [76]. The load capacitor on each block is assumed to be 200pF.

$$E_{op} = \frac{V_1 i_1 (T_1 + \Delta T_1)}{\eta_1} + \frac{V_2 i_2 (T_2 + \Delta T_2)}{\eta_2} + \cdots \tag{4.19}$$

Eop is the operating energy and η is calculated using equation (4.2).

$$E_C = V_{in} C_L (\max(V_1 - V_2, 0) + \max(V_2 - V_3, 0) + \cdots) \tag{4.20}$$

$$E_{TOTAL} = E_{OP} + E_C$$

Each block is modeled as a chain of inverters with different depths. The delay of the block is calculated as its time of operation. The power supply level changes for 100 iterations. The rate at which the voltage changes to a new value is varied from 10ns to 1ms. The energy dissipation in

each case is compared with a single V_{DD} (always 1.2V) block. Figure 4-10 shows the result of our experiment. We find that at fast rates of voltage scaling (a voltage transition every~10ns), the overheads of a DC-DC converter dominate, and there is an energy loss. Energy benefits can be realized for T_{OP} greater than 1µs with a maximum benefit of more than 150% achievable at slower rates of V_{DD} transitions. This implies that, for these assumptions, the 5 V_{DD} system would save energy relative to the single V_{DD} system, when transitioning V_{DD} to adapt to changes in the workload that are slower than ~1µs.

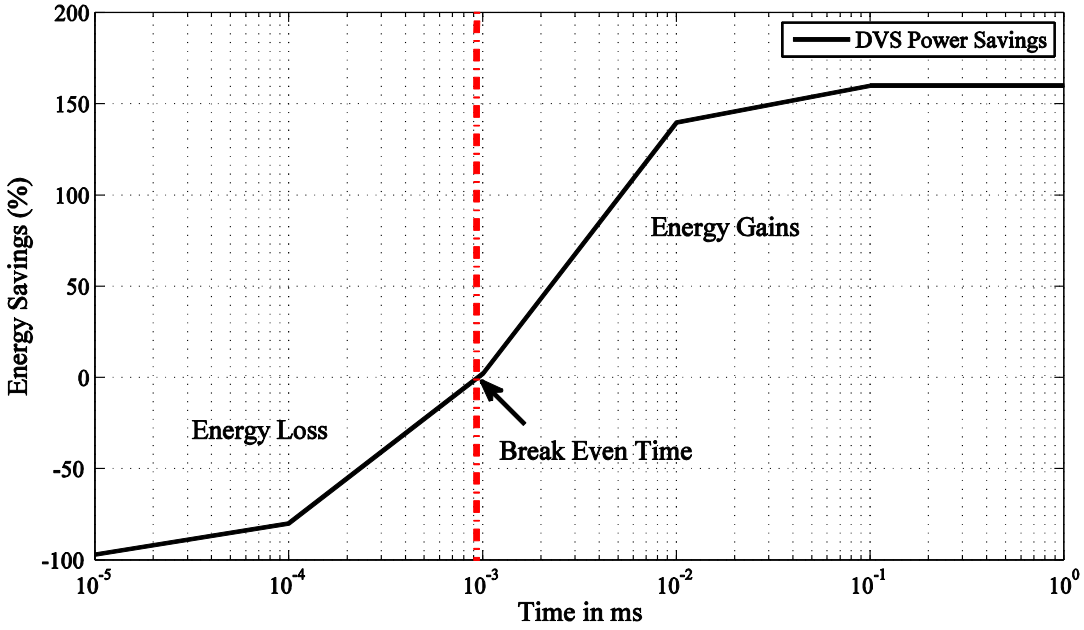


Figure 4-10 Energy Savings with rate of Voltage Scaling

Panoptic Dynamic Voltage Scaling

This section applies the DVFS modeling approach to a different DVS implementation. Figure 4-11 shows the block diagram of a block level voltage scaling technique called panoptic dynamic voltage scaling (PDVS) [88]. In the PDVS technique, a block can switch from one voltage to

another by the use of headers, as shown in Figure 4-11. The advantage of this technique is that it enables a much faster switching. An equivalent DVFS voltage can be realized by dithering between the supplies. This scheme is more practical and has lower cost.

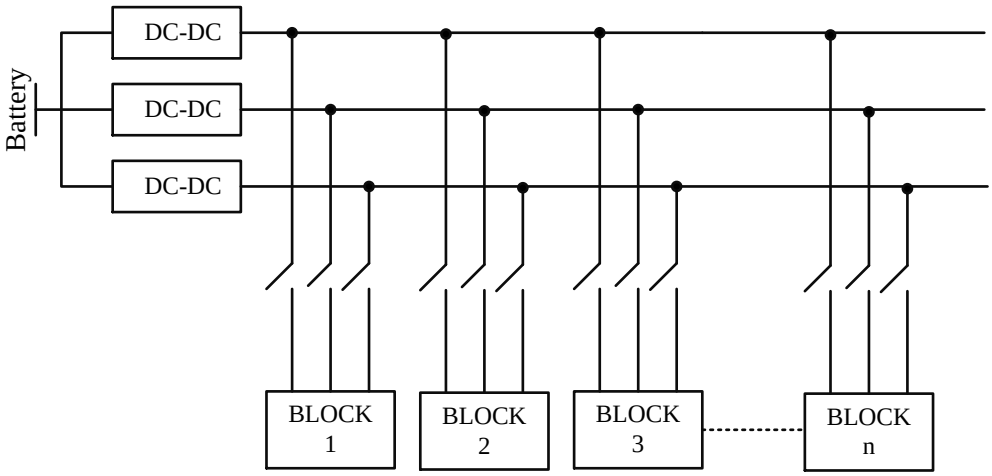


Figure 4-11 PDVS: Block Level Voltage Scaling Technique

Framework for Energy Calculation in PDVS

We reproduce the operating condition of a block from Figure 4-9. This block operates at different voltages for different times to accomplish optimal energy operation. We break down the operating condition of Figure 4-9 into Figure 4-12. If a block has to operate at V1 (0.4V<V1<0.8V) for T1 time, PDVS accomplishes it by connecting the block to 0.4V for T11 and 0.8V for T12, such that T11+T12=T1 of Figure 4-12. This approach is called voltage dithering. T11 and T12 are such that the performance of the block does not change. A final operating condition is given by Figure 4-12 (b). The load on each supply will change, depending on the blocks that are connected to it, and results in a continuous time varying load on each supply. We include time to obtain the energy. Each supply has larger load variation, which will have an impact on the overall efficiency. The total energy is given by,

$$E_{OP} = 0.4\int i_1(t)/\eta_1(i_1)dt + 0.8\int i_2(t)/\eta_2(i_2)dt + 1.2\int i_3(t)/\eta_3(i_3)dt$$

$$E_C = V_{in}C_L(\max(V_1 - V_2, 0) + \max(V_2 - V_3, 0) + \cdots) \quad (4.21)$$

$$E_{TOTAL} = E_{OP} + E_C$$

We keep the same system set-up as was used for the dedicated DC-DC converter case. It should be noted that there will be an insignificant overhead of settling time in this case. We assume a capacitive load of 20pF on each block, since the local block virtual V_{DD} rail switches instead of the total chip-wide V_{DD} rail (with all of its decoupling capacitance).

VDD	Load			T_{OP}
	0.4V	0.8V	1.2V	
v1 V	i11 µA	0	0	T11
v1 V	0	i12 µA	0	T12
v2 V	0	i21 µA	0	T21
v2 V	0	0	i22 µA	T22
…….	…….	……..	…..	…….

a) Operating Condition

Load			dT_{OP}
0.4V	0.8V	1.2V	
$i_1(t)$	$i_2(t)$	$i_3(t)$	1e-9

b) Final load table

Figure 4-12 PDVS Operating Condition Evaluation

4.1.3 Comparison of DVFS and PDVS using the Model

Figure 4-13 compares the PDVS scheme with a dedicated DC-DC converter case using the system level model that incorporates the DC-DC converter equations. The PDVS scheme has a break-

even time of 30ns compared to 1µs in the dedicated supply case. This is because of the very small settling time in PDVS, as the block is charged to the rail almost instantly. It also has lower conversion energy. The total energy benefits from the PDVS scheme are, however, lower than the dedicated DC-DC converter case, because it sees much wider load variation. The PDVS scheme, however, is better- suited for implementing block level DVFS because of its much smaller break-even time, allowing it to adjust to short changes in the workload. PDVS scales much better to larger numbers of blocks, since it requires only one DC-DC converter output per voltage rail rather than per block, as in the dedicated DVFS scheme. These results are, of course, influenced by the values of the parameters in the model, and the model makes it very easy to investigate how the results will vary when the assumptions change.

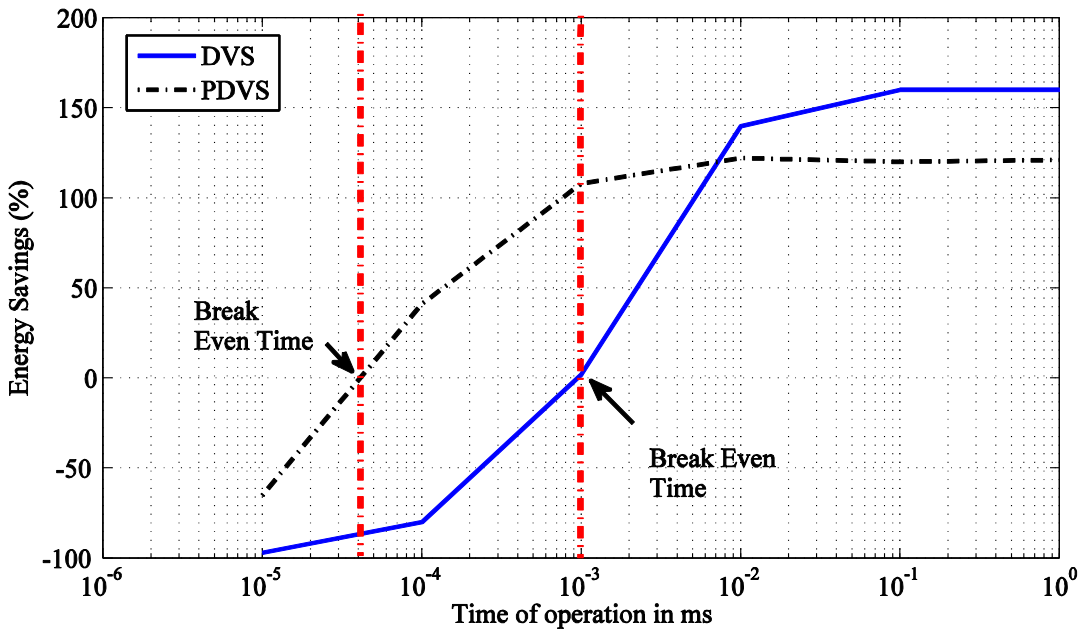


Figure 4-13 Energy Benefits of PDVS and Dedicated DVFS

Figure 4-14 shows how the PDVS savings for the same scenario as before will change as a function of the capacitance of the virtual V_{DD} rail of each PDVS block. As the capacitance of the block

increases, the breakeven time moves to larger times, meaning that the workload needs to remain at a new value for a longer time to make it worthwhile to switch the voltage of that block.

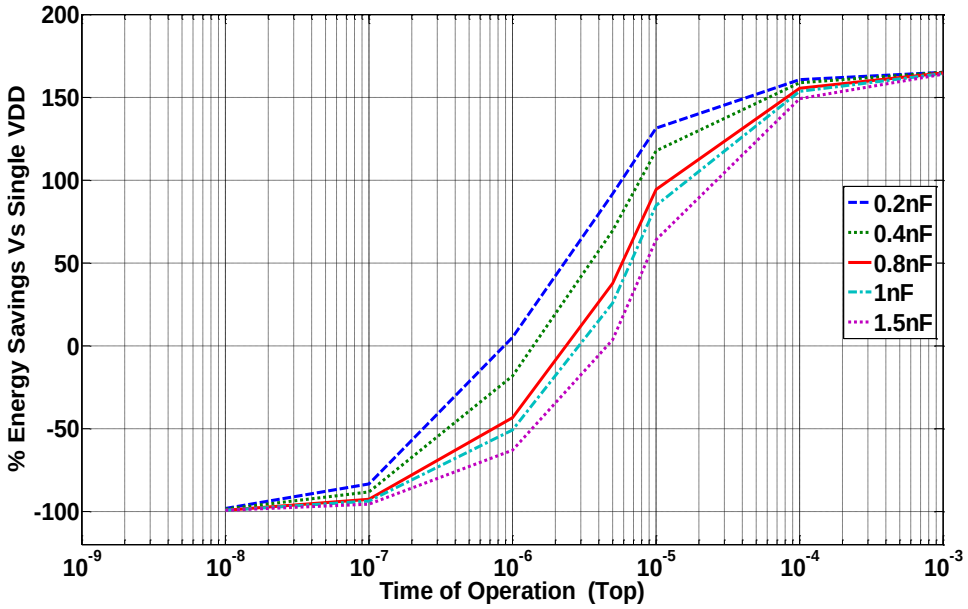


Figure 4-14 Energy Benefits of PDVS for different values of the virtual VDD capacitance of the block

4.2 Implementation of Power Management for PDVS

Minimizing power consumption by employing power management techniques is a common practice today in integrated circuit (IC) design. Several techniques have been researched and applied to this end. Initially, Dynamic Voltage Scaling (DVS) [93], where the power supply of an Integrated Circuit (IC) is modulated according to its performance needs, has been successfully utilized to reduce the power consumption. Usually, voltage is scaled up for the IC to perform at a higher rate or scaled down to trade off performance for lower power consumption. Also, the IC can be divided into multiple voltage domains as multi-V_{DD} systems, where multiple power rails are used to operate non-critical paths at lower voltages to save power. Moreover, it has been

claimed that the lowest energy operating point is achieved when the processing rate matches the rate of the work-load. Such a system needs to operate an individual block at different voltages at different times.

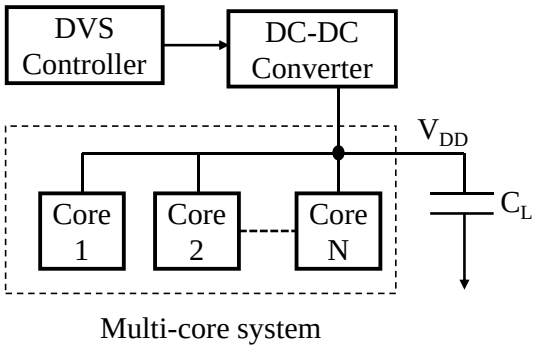


Figure 4-15 Dynamic Voltage Scaling for multi-core system

Practical implementation of power management techniques, such as DVS, involves several overheads. Figure 4-15 shows the implementation of DVS for a single V_{DD}, multi-core system. The V_{DD} is scaled according to the performance or power needs of the IC. This implementation involves several overheads. The output capacitor (C_L) of a DC-DC converter is usually large; therefore, it has a large settling time. The energy stored on the capacitor is also high, so changing the output voltage involves energy overheads. Usually, these overheads limit the rate at which V_{DD} can be scaled [95] and, hence, the amount of energy that can be saved. The flexibility of DVS is also limited, as individual cores do not operate at their optimal voltages. Operating each core with its own V_{DD} can save more power. However, the number of DC-DC converters needed for this purpose increases linearly with core. Low Drop Out (LDO) and switched capacitor converter present on-chip options for implementing DVS for the multi-core system, albeit at lower efficiency, which again limits power savings.

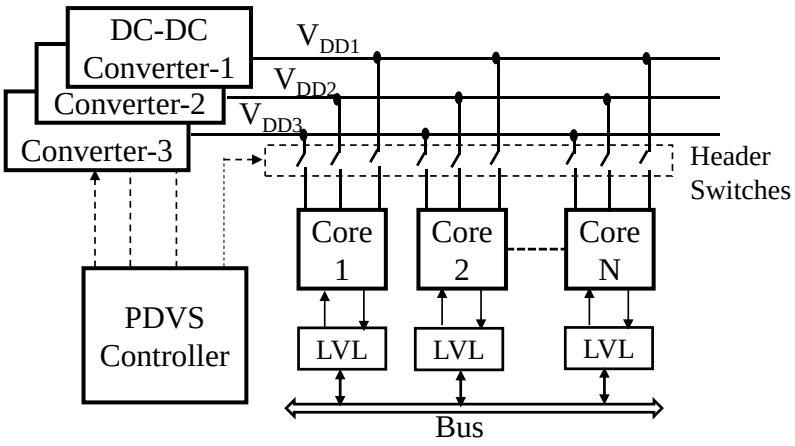


Figure 4-16 PDVS implementation for multi-core system

Panoptic dynamic voltage scaling (PDVS), as explained in the previous Section, has been proposed [97] to overcome these limitations of DVS. Figure 4-16 shows the implementation of a PDVS scheme. Each core inside a multi-core system is connected to three different rails through header-switches. The blocks can be connected to a given V_{DD} rail, depending on power or performance requirements. It allows the cores to switch from one voltage to another. Utilizing three different voltage levels, a block can be made to operate at its optimal voltage by using the voltage dithering technique [98]. Using PDVS techniques, several limitations of classical DVS can be overcome. In PDVS, each block can theoretically be made to operate at its optimal voltage which results in higher overall power savings [97]. The voltage rails in PDVS are fixed and the blocks are connected to these rails depending on their throughput requirement. The fixed voltage level in PDVS eliminates the settling time and energy overhead costs usually present in the classical DVS technique because of the overhead cost of the DC-DC converter [95]. As a result, PDVS can implement a faster rate voltage scaling technique and can save more power [94][95]. However, the implementation of PDVS requires at least three DC-DC converters. The other cost involved is

higher area owing to the routing, switches and level-converter (LVL) needed to implement it. The routing, the switches, and the LVLs area overhead are less than 15% [94] for each block, which doesn't amount to significant cost given the energy benefit. However, the cost of three or more DC-DC converters needed to implement PDVS can amount to significant cost when compared to a system implementing a single V_{DD} DVS. Therefore, a practical PDVS system has not yet been implemented. This section presents a power management solution to implement PDVS.

Several design challenges have to be overcome to implement a low cost power management solution for PDVS. We need more than three DC-DC converters to implement PDVS. A simple implementation will be to have as many dedicated DC-DC converters as needed by the PDVS scheme. However, this will still be costly and not practical. A single inductor multiple output (SIMO) [96] DC-DC converter, where one inductor is used to generate multiple output supplies, is proposed for PDVS. The three output rails for PDVS are generated through SIMO architecture which is a lower cost, higher efficiency solution. To further reduce the cost and system volume, the capacitors are integrated. The integration of capacitors is only possible if smaller capacitances are used. However, use of small sized capacitances will increase the ripple on the power supply. We use small sized on-chip capacitances. The ripple on the power supply is reduced through a proposed hysteretic control scheme. Further, the use of SIMO will also result in higher ripple and cross regulation issues in the design, because of the changes in loads on different V_{DD} rails. This issue is addressed by designing the SIMO converter to be able to configure itself based on the load information which is available in a PDVS system. This section proposes the design of a SIMO DC-DC converter with on-chip capacitors, utilizing the features of PDVS technique. It provides a cost efficient, energy efficient way to implement block level DVS. The proposed circuit is the first

reported practical implementation for PDVS and implements low cost and efficient PDVS. The use of SIMO reduces the cost of multiple DC-DC converter requirements for the implementation. The proposed solution provides three output rails at 0.9V, 0.7V, and 0.4V, at peak efficiency of 86% with integrated capacitance.

The design description of the proposed circuit is divided into the following sections. First, we talk about the overall system architecture and the SIMO control scheme. Second, we will describe the hysteretic control scheme which helps in reducing the size of the capacitors. Third, we will describe the scheme for co-designing SIMO with PDVS load environment which helps in dealing with cross-regulation and higher ripple arising from SIMO architecture. Finally, we will present the measurement results and compare the proposed design with the state-of-the-art.

4.2.1 PDVS SIMO Architecture

Figure 4-17 shows the block diagram implementation of the proposed SIMO DC-DC buck converter to drive an example PDVS system. It consists of hysteretic comparators, a SIMO controller, and buck DC-DC converter, and provides three output rails at V_{OH}=0.9V, V_{OM}=0.7V, and V_{OL}=0.4V. The comparator, SIMO controller and the DC-DC converter implement the control loop to provide the output voltages. The SIMO controller steers the inductor current (I_L) to different rails through switches S1-S3. The hysteretic comparator compares each rail to its reference voltage and provides a digital output. It also controls the switching turn-on time of the comparator, which we will explain later in this section. The hysteretic comparator controls the regulation and switching of each rail. These comparators can be disabled when a particular rail is

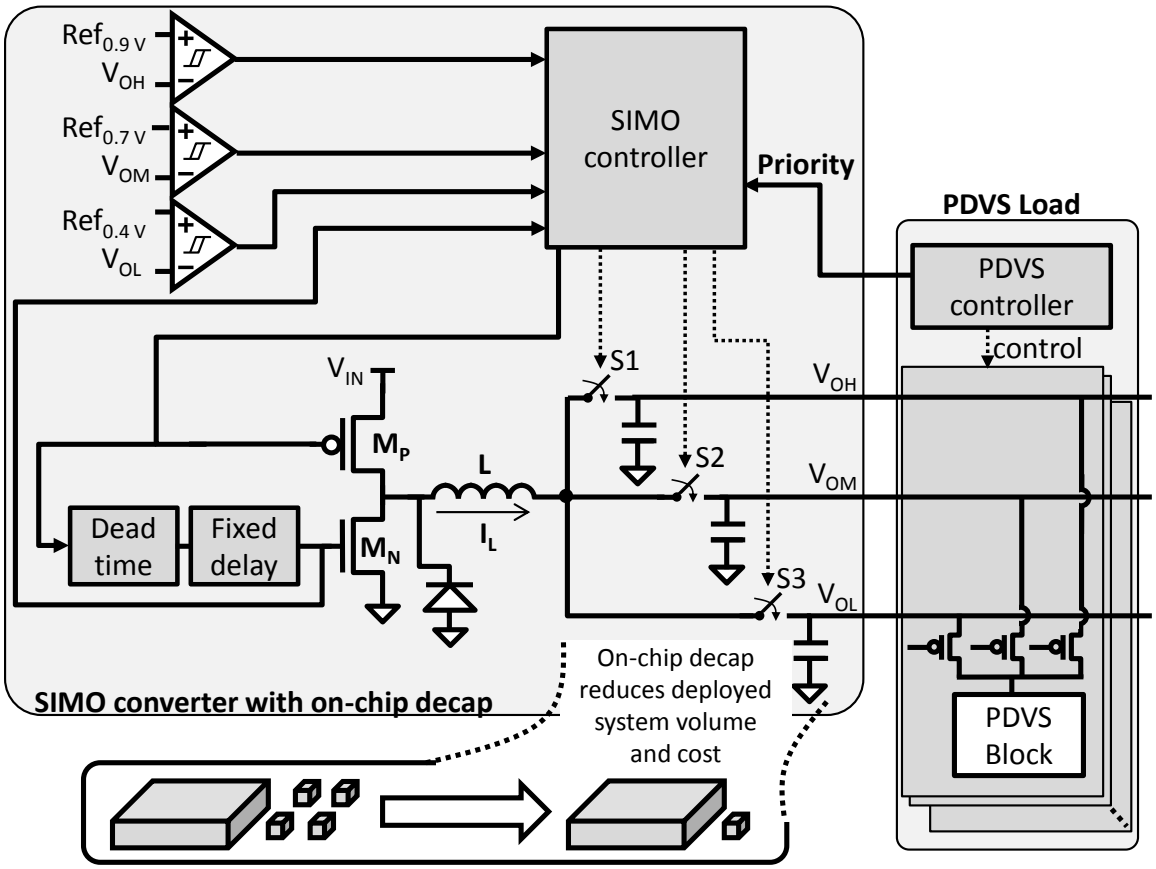


Figure 4-17 SIMO DC-DC buck converter for low voltage DVS-enabled. On-chip decoupling capacitance saves system level volume and cost

not needed in the system. The digital output of the comparator goes into the controller, along with the priority signal from the PDVS controller. These signals are used to generate control for the DC-DC converter, as well as to assign switching sequence for the switches S1-S3. The priority signal from the PDVS controller provides the current loading scenario on each rail. The SIMO controller uses this signal to set the switching priority, and assigns highest and lowest priority to switches S1-S3. For example, if 0.9V rail is heavily loaded, the priority is set on this rail and, in the event that 0.9V comparator output goes low, the SIMO controller starts steering inductor current into 0.9V rail. In a case where all three rails are heavily loaded, this switching configuration can result in higher ripple or cross regulation. However, it is not possible for all of the rails to be

loaded simultaneously in a PDVS system. As a result, higher ripple is typically not seen on other rails.

Control Architecture

The design goals of the control architecture are following. First, the architecture should be able to support lower sized capacitance with small ripple. Second, it should provide high efficiency and, finally, the static power consumption of the circuit should be small. We will first explain the control of an individual controller making the SIMO to operate as a simple buck converter providing a single V_{DD}. This can be achieved in the system by disabling other two converters by disabling their comparator. The design decisions at this level are used to reduce the overall system power and cost. The switching time of the converter is controlled by the comparator, which helps reduce the additional control circuit, which, in turn, reduces static power consumption of the system. We used two approaches to reduce the dimensions of the passives in the converter. First, we used 65nm advanced process nodes compared to [96][68][69][99][100][101]. The smaller CMOS technology will enable faster switching frequency for the converter, which will enable lower sizes for inductor and capacitors. Secondly, we propose a new hysteretic control scheme, which further brings down the size of the capacitor to nF range.

Figure 4-18 shows the conventional control scheme to generate the High Side (HS) switching control for a DC-DC converter. Usually, two approaches are common. In the first approach, a fixed delay is generated and the turn-on time of the HS switch, MP, is controlled by the fixed delay. This delay generates the current in the inductor and HS switching is enabled, followed by Low Side (LS) switching. The HS control determines the amount of energy being transferred in each cycle.

The second approach for HS control uses current sensing of the inductor and is more popular for higher output power switching converters. However, this scheme suffers from inaccuracies and higher energy overhead [46], which makes it unsuitable for low-energy lower voltage systems. Also, fixing the current of the inductor requires a high amount of decoupling capacitor to reduce the ripple. The inductor current gets stored on the capacitor for the cases of light load. This can cause higher ripple if the capacitor is small.

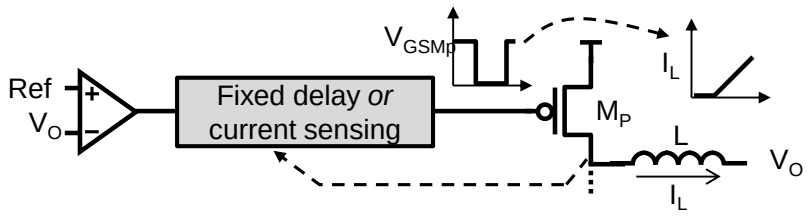


Figure 4-18 Conventional HS control

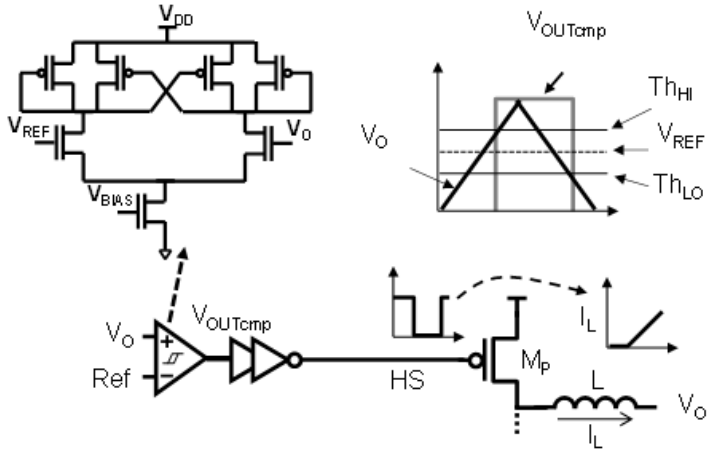


Figure 4-19 Proposed control scheme

Figure 4-19 shows the circuit of a proposed HS control scheme. It uses a hysteretic comparator to control the HS switch. The hysteresis of the comparator and the delay of the comparator set the ripple on the rail. The high side transistor, MP, is turned ON when V_O goes below Th_{LO} of the

hysteretic comparator, where Th_{HI} and Th_{LO} are the higher and lower thresholds of the comparator, respectively, with hysteresis given by, Th_{HI}-Th_{LO}. The inductor starts charging the output rail and its current starts ramping up. Once V_O crosses Th_{HI}, MP is disabled and inductor current starts discharging through to the output capacitor.

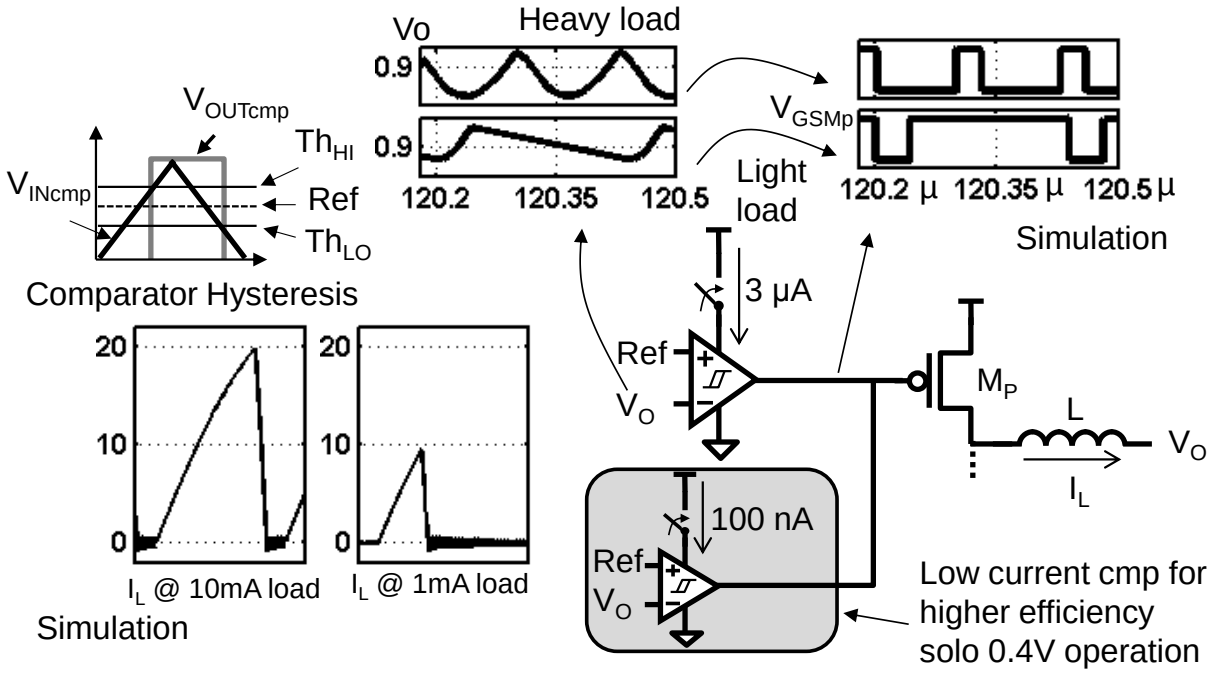


Figure 4-20 Control Architecture to reduce the ripple

Figure 4-20 shows the behavior of the HS control circuit. At the light load condition, the voltage at the output rises quickly, since the current drawn from the output capacitor is low and most of the current is used to charge the capacitor. Therefore, the hysteresis of the comparator sets a lower inductor current and insuring lower ripple. If the load current increases, the rise time of the output voltage increases, and, as a result, MP is on for a longer duration of time (since higher current is drawn out of the output). This increases the peak current in the inductor. The proposed circuit adapts itself with the output load. This scheme makes the ripple on the rail less dependent on the output capacitor. Figure 4-21 shows simulation results of the variation of the output ripple of the

capacitor, with load current at different values of the decoupling capacitor. The ripple voltage varies from 30-60mV for 0.8V V_{DD} and 1.2V Vin. We selected 4.3nF of output capacitor, which gives us ~5% ripple on the rail. This value of capacitance is significantly smaller than the typical decoupling capacitors (µF range) used on output rails in a DC-DC converter. At these values, the capacitance can easily be integrated on-chip. A significant percentage of the capacitance can come from the parasitic capacitance of the cores connected to these rails [105].

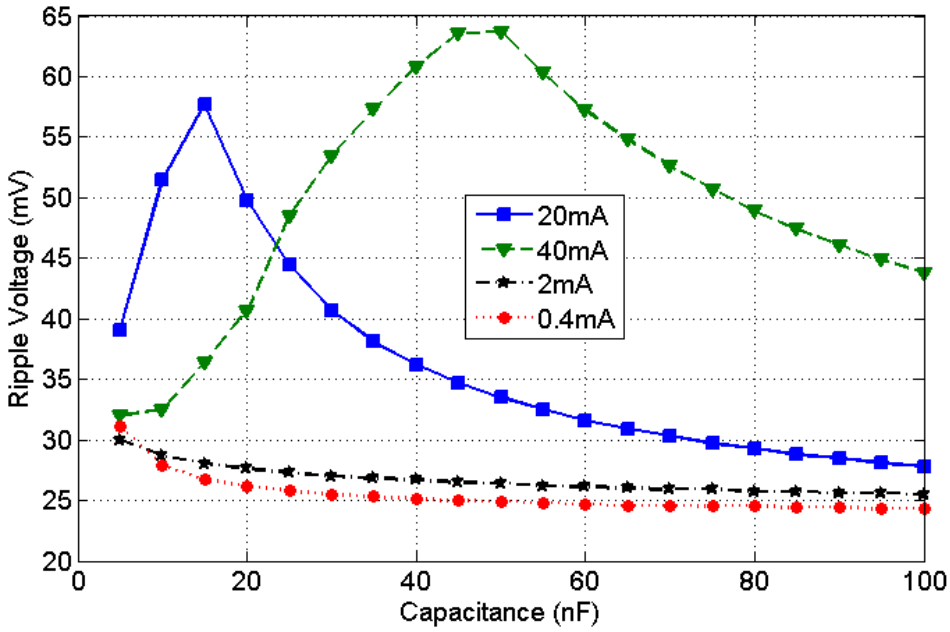
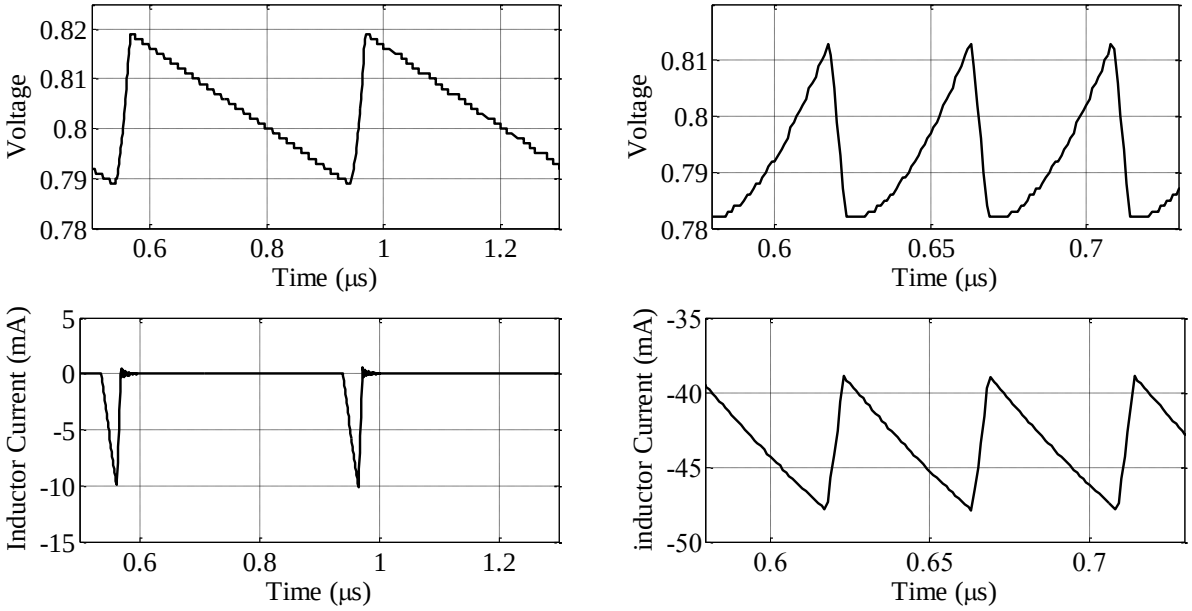


Figure 4-21 ripple Voltage for different values of decoupling capacitor at different loads

The proposed HS control scheme supports a load up to 50mA and can operate the converter in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM). At light load condition, the converter goes into DCM. The HS turn on time is used to charge the inductor. After LS control cycle, the inductor current goes to zero. However, V_O goes below Th_{LO} later than LS cycle, due to the light load condition. The HS control scheme starts again, once V_O goes below Th_{LO}. Operating in DCM at light load helps in achieving good efficiency as well as controlled

ripple. The converter operates in CCM at high load condition. At high load condition, V_O goes below Th_{LO} before the inductor current goes to zero and, hence, conducts continuously. Operating in CCM helps in targeting heavy load condition for the converter. Figure 4-22 shows the simulation results of the output voltage and inductor current at light load and heavy load conditions, respectively. It shows that the converter operates in CCM at high load and in DCM at light load condition.

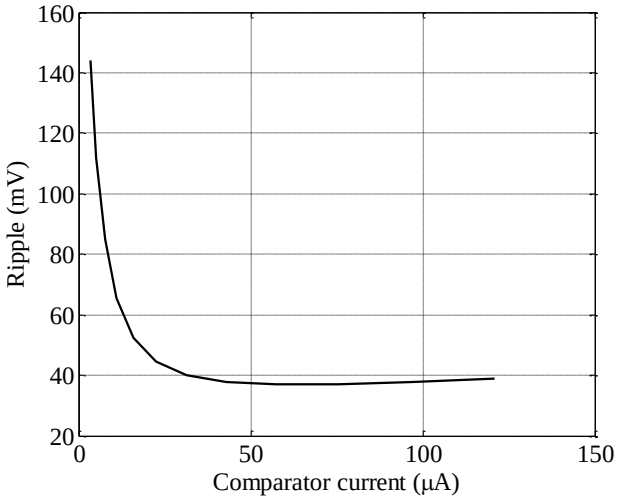


a) Load Current = 0.4mA b) Load Current = 40mA

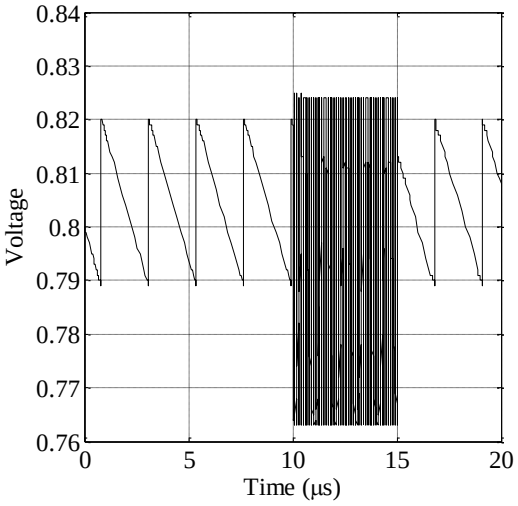
Figure 4-22 Converter Operation in CCM and DCM mode

The static power consumption of the HS circuit is dictated by the power consumption of the comparator. More power can be saved by lowering the comparator quiescent current. However, the performance of the comparator also controls the amount of ripple seen on the rail. For example, if the comparator has higher delay (lower power), then response of the comparator to the changes at the output voltage will be slower, which will result in elevated ripple. Figure 4-23 (a) shows the variation of ripple with the comparator quiescent current. The ripple decreases with increased

quiescent current. The ripple becomes constant after 25µA of comparator current. After this point, the hysteresis of the comparator and output capacitor controls the amount of ripple. We select 25µA quiescent current for the comparator of 0.9V and 0.7V rails and use two comparators for 0.4V rail. One comparator has 3µA, while the other has 100nA quiescent current. This is done to lower the static power consumption of the converter for the low power mode, where all the cores in the PDVS system can be connected to 0.4V. The other two converters can be disabled, while 0.4V rail will supply the V_{DD} with higher ripple.



a) Ripple of the converter with comparator quiescent current



b) Behavior of the converter when load changes from 100µA to 10mA

Figure 4-23 Transient behavior of the converter

Hysteresis of the comparator is also important in determining the peak inductor current, which is important in determining the overall efficiency of the converter, particularly at light load condition. At higher value of inductor current, conduction loss increases, thus decreasing the efficiency, while, at lower value, the switching loss reduces the efficiency. We control the inductor current through the hysteresis in the comparator. At high load condition, the losses are governed by the load current, as the converter operates in continuous conduction mode. The comparator and the output capacitor

are also important for the transient behavior of the converter. Figure 4-23 (b) shows the condition when output load changes from 100µA to 10mA in 10ns. It shows that the converter can continue to regulate even for a fast change in load condition. However, owing to the small size of the output capacitor, a very sharp change in output load to high load, such as 40-50mA, can result in overshoot or undershoot at the output rail. The converter needs a few µs to recover under such conditions. This happens because the converter goes from DCM to CCM in a very short time, which can result in higher inductor current build- up and can cause higher ripple. However, if the load changes slowly, then higher ripple is not seen on the rail.

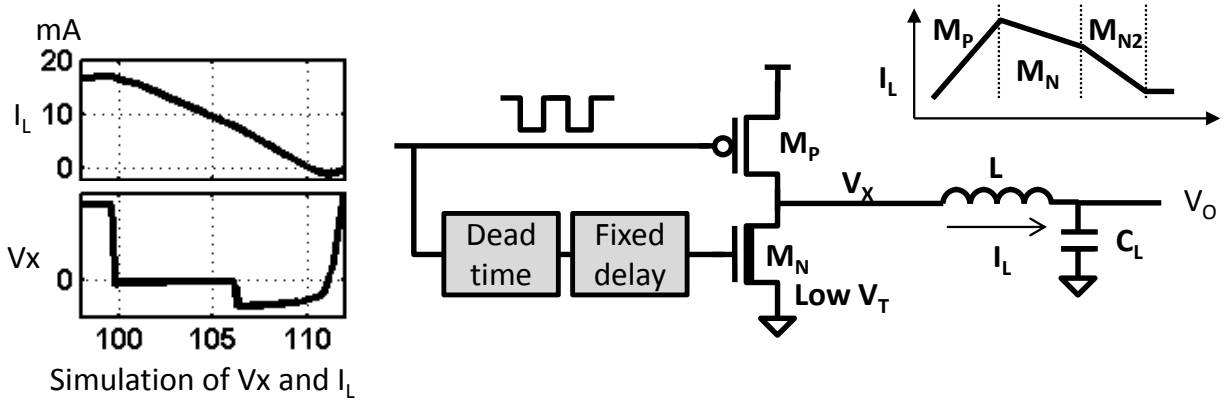


Figure 4-24 Low Side control Scheme

Figure 4-24 shows the low side (LS) control of an individual controller. The low side control is implemented to keep the LS switch on for a fixed time. For the rest of the time, LS conducts as a diode. The LS switch is implemented with an L_{VT} device. As a result, the diode doesn't contribute significant loss. A conventional scheme for LS control implements a zero detection comparator. For light load condition and lower inductor current, as in the current implementation, the performance required for zero detect comparator is very high. For higher performance, static current in the comparator becomes higher, which adds significant overhead on the DC power

consumption of the converter. The scheme to implement fixed delay turn on time for LS eliminates this overhead with a smaller penalty in efficiency.

SIMO Digital Controller

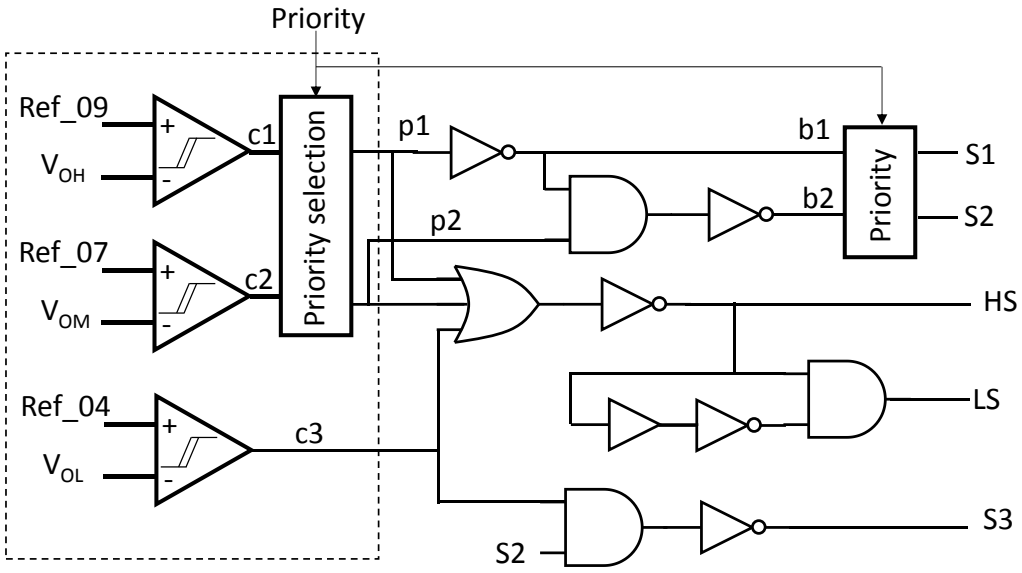


Figure 4-25 Digital control logic of SIMO controller

Figure 4-25 shows the simplified circuit diagram of the SIMO controller. The HS control is enabled when any one of the three comparator outputs goes high. At this time LS is disabled. Once HS is disabled, LS turns on for a given pulse width, as shown in Figure 10. Switches S1-S3 are the SIMO switches for 0.9V, 0.7V, and 0.4V rails redrawn here from Figure 4-17. The priority selection selects between c1 and c2 and correspondingly S1 and S2. For example, if 0.7V rail has higher priority, then c2 gets connected to p1 and c1 to p2. Similarly, b1 gets connected to S2 and b2 gets connected to S1. Only one switch out of S1, S2, and S3 is turned on at a given time. Priority

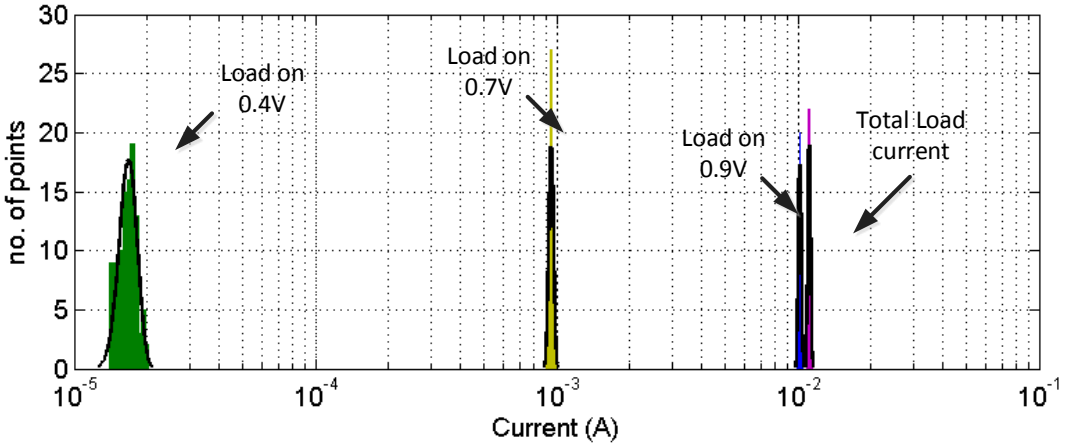
selection plays a role in selecting a particular switch. If more than one rail is below its Th_{LO}, then the switch corresponding to the rail with higher priority is turned on. We assign higher priority to the rail with a higher load. This design is well-suited to the PDVS system. If one rail is heavily loaded, then other rails are going to be lightly loaded in PDVS. Also, since load information is well known in PDVS (through the header switch connection), priority can be assigned correctly.

In this scheme, the rail with higher load gets serviced first, which prevents it from having higher ripple. The rail with lower load discharges slowly and can be serviced in the meantime. The proposed circuit can see higher cross regulation in the case where difference in load becomes too large among rails. This happens in the CCM mode of operation. If one rail is heavily loaded with (40-50mA), while other rail is lightly loaded at (~10-100µA), then the lightly loaded rail can charge up because of the higher current present in the inductor. Several methods have been proposed to overcome this problem. One of the methods is to short both terminals of the inductor, which results in energy loss. We dump the extra current on the 0.4V rail, which has the least priority. In the event that voltage goes higher, a clamp can be used to control the voltage at 0.4V rail.

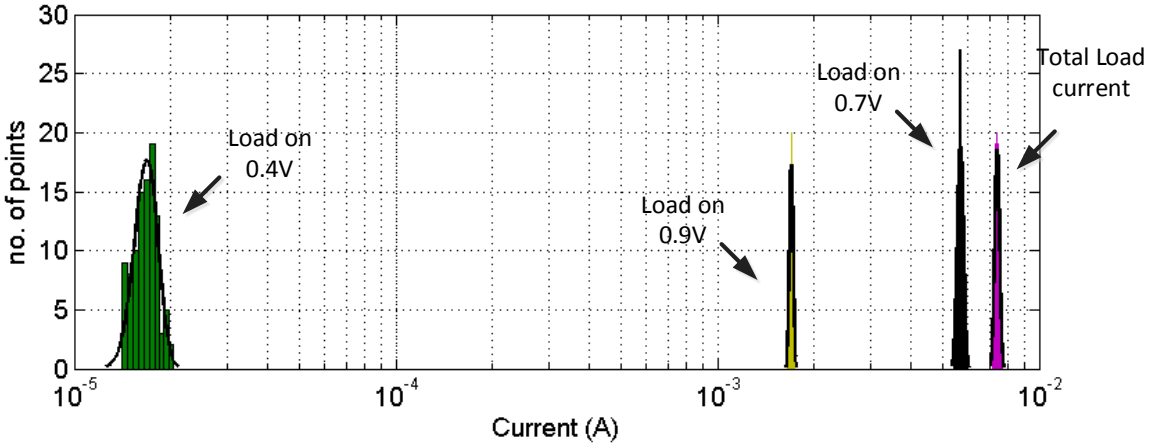
Control of Ripple through PDVS

Figure 4-26 shows the distribution of load current for different scenarios. It shows the cases when most of the cores are connected to 0.9V and 0.7V, respectively. It provides an insight that, if one V_{DD} rail is heavily loaded (case when most of the cores are connected to that V_{DD}), the other V_{DD} rails are lightly loaded. This is a unique characteristic of PDVS which can be used to the advantage

of SIMO converter design. This feature can be used to address the issue of cross-regulation in SIMO converters. Cross-regulation arises in SIMO converters usually operating in



a) current consumption when most of the cores are connected to 0.9V, total load current=15mA



b) current consumption when most of the cores are connected to 0.7V, total load current=8mA

Figure 4-26 PDVS load conditions when most of the cores are connected to one supply

CCM, when the changes in load current of one of the output voltage rails result in the change of output voltage of another rail. This happens largely because of the load transients on voltage rails in a system. Often, SIMO converters are over-designed to address the worst case load transients to

address cross-regulation. The well-defined loading configurations in a system implementing PDVS, the load transients, are well known in advance. It is also well known which of the three rails is going to be heavily loaded and which is lightly loaded at any point in time. This information can be easily obtained by scrutinizing the number of cores (or type of cores) getting connected to a given rail at a given time. Since the information is already known or needed to configure the header switches in PDVS (Figure 4-16). We use this information in our SIMO converter design to set the priority of the switching rails. For example, if a SIMO is designed to provide 0.9V, 0.7V and 0.4V rails, and 0.9V rail is heavily loaded, then the 0.9V rail is set on the priority. This way, the 0.9V rail is regulated first and then the 0.7V and 0.4V. If loading information is not well-known, priority cannot be set correctly and higher cross-regulation can be seen on the rails. In order to maintain the rails within the specified error, often higher values of capacitors are used, with value in µF range. This design proposes new circuit methods, in conjunction with the PDVS, to significantly lower the value of the decoupling capacitor. The capacitor used in the proposed SIMO are 2.1nF for 0.4V, and 4.3nF for 0.7V and 0.9V V_{DD} rails.

4.2.1 Prototype Implementation and Results

In PDVS, the abrupt change of load due to DVS control is deterministic. If most of the cores switch to 0.7V from 0.9V, the PDVS controller will indicate this to the SIMO converter, which will prioritize the 0.7V rail. The feed-forward information can be used to dynamically reassign the priority that controls cross-regulation due to abrupt load transition. This eliminates complex feedback schemes that will also reduce efficiency at light load conditions. Figure 4-27 shows the measured ripple on the 0.7V and 0.9V rails with and without our DVS priority scheme. The ripple on the 0.9V supply, due to our priority scheme, reduces by 30mV in measurements. Figure 4-27

shows the steady state outputs of the SIMO at high and moderate loads. When the SIMO supplies 10mA on 0.9V, 1mA on 0.7V, and 1mA on 0.4V, the efficiency is 86%, with measured ripple of 40mV. The measured gate leakage of the 0.9V and 0.7V decap was 5µA and 1µA at room temperature.

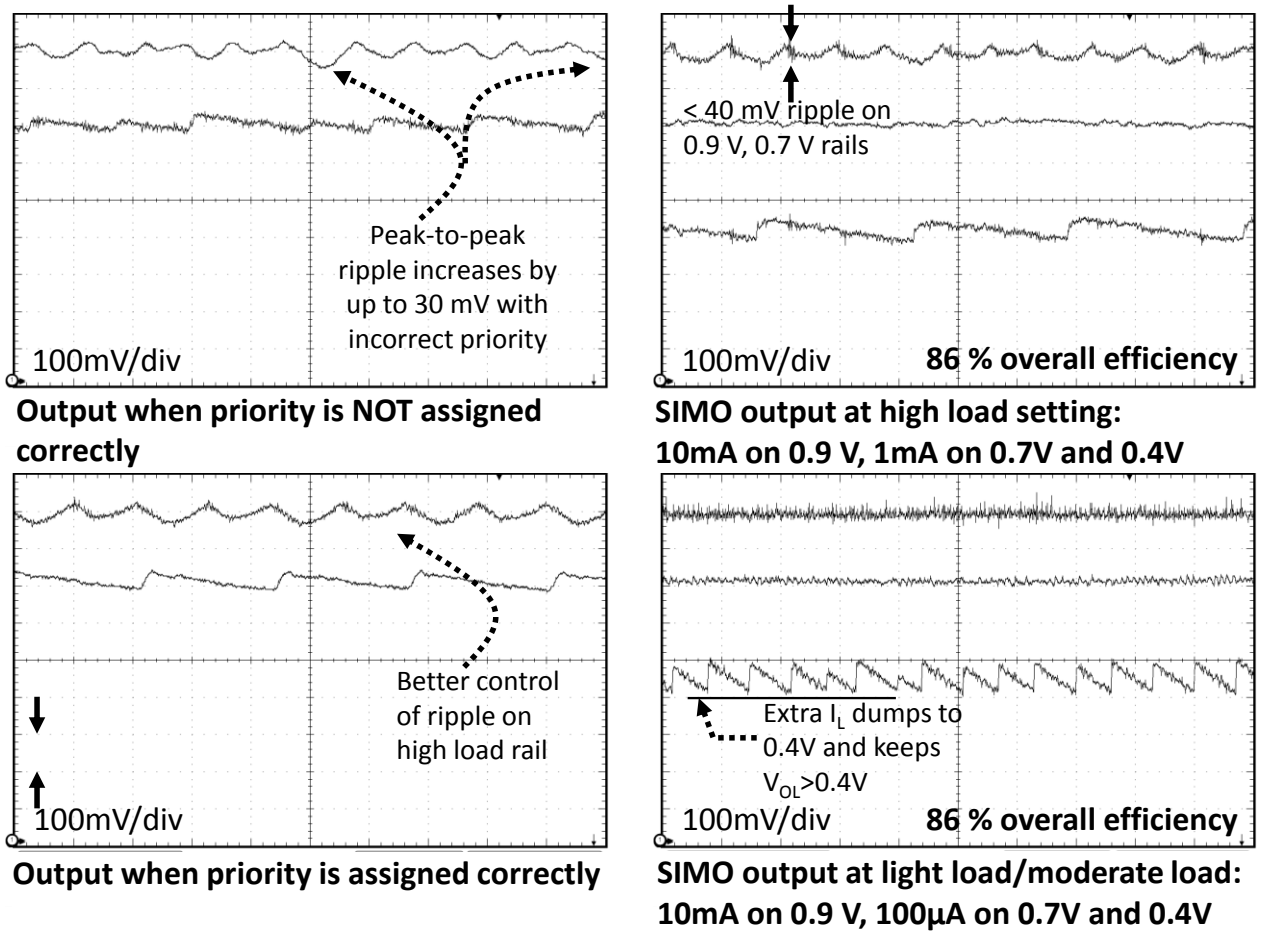


Figure 4-27 Measured outputs of the SIMO. During different load switches at constant total load of 10 mA, compensating PDVS changes with rail priority adjustments reduces ripple by 30 mV. High load efficiency is 86%, and low load efficiency is 62%.

Figure 4-28 shows the measured efficiency of the converter in various configurations. The peak efficiency for the standalone 0.9V converter is 88% at 10 mA, and with the low voltage comparator,

the efficiency of the standalone 0.4V converter was 60% at 100µA and 68% at 1mA (vs. 33% for ideal LDO) over 23% better than the switched capacitor converter reported in [104]

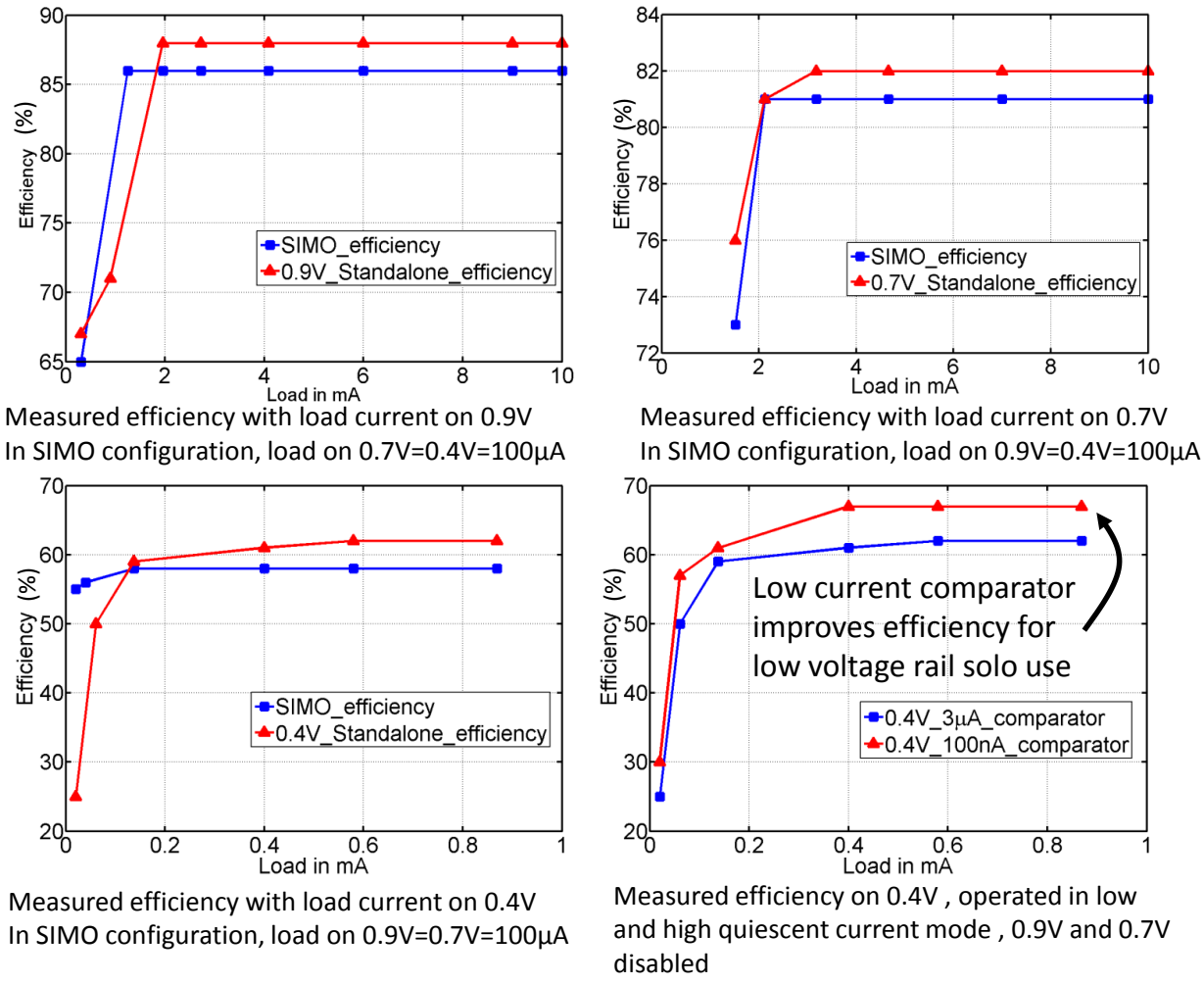


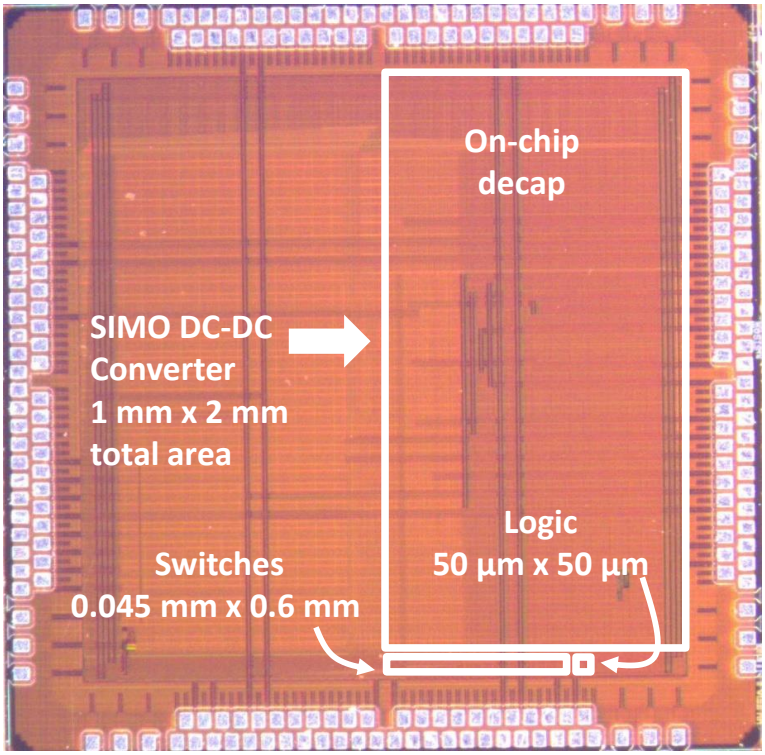
Figure 4-28 Measured efficiency plots for different configurations

Table 4-1 shows the comparison of the proposed work with prior low load SIMO and on-chip converters. The proposed design is a first integrated SIMO design with 1µH external inductor. The measurement result shows that proposed design achieves a peak efficiency of 86% with a maximum ripple of 40mV.

Table 4-1 Comparison with prior art for low load converters. This design supports 3 outputs at lower voltage and load than any prior SIMO with comparable efficiency and ripple but no off-chip capacitors.

	This work	[103]	[101]	[104]
Technology	65nm	65nm	250nm	45nm
Topology	SIMO buck	SIMO buck	SIMO buck/boost	Switched Capacitor
# Outputs	3	5	4	1
V_{IN} (V)	1.0-1.1	3.4-4.3	1.8-2.2	1.8
V_{OUT} (V)	0.9,0.7,0.4	2.8, 2.5, 1.8, 1.5, 1.2	2.25, 2.0, 1.35, 1.25	1.0-0.8
Target I_{LOAD}	0.9V: 10mA-10µA 0.7V: 10mA-10µA 0.4V: 1mA-1µA	<230mA per output	100mA-~20mA	8mA-100µA
Efficiency @ load	86% @ [10mA, 1mA, 1mA]	83.1% @ 75mA/out	90% @ high 80% @ low	69% @ 1V, 5mA 66% @0.9V, 5mA
Max Ripple	40mV	40mV	22mV	50mA
Caps	On Chip	Off-chip	Off-chip	On Chip
Area (mm^2)	2 (0.03 w/o caps)	1.86	1.8 x 2.1	0.16
Inductor	1µH	2.2µH	10µH	NA

Figure 4-29 shows the implementation of the proposed with on-chip decaps. The capacitors for the design are implemented using nMos capacitors. The value of the capacitance is 4.3nF for 0.9V and 0.7V rails and 2.3nF for 0.4V rail. The capacitance contributes to ~1µA of standby current, because of the gate oxide leakage. The total area of the converter is $2mm^2$. The area of the control circuits is $0.03mm^2$.



Process	Output V_{DD}s	Max efficiency			
		Total	0.9 V only	0.7 V only	0.4 V only
65 nm CMOS	0.9, 0.7, 0.4	86 %	88 %	82 %	68 %

Figure 4-29 Die microphotograph of the SIMO chip and performance summary

We proposed a SIMO DC-DC converter design for the PDVS system that can support a peak load of 50mA on the 0.9V and 0.7V rails, and 10mA on the 0.4V supply. To reduce system level volume and cost, we integrate two 4.3nF (0.9, 0.7V) and one 2.1nF (0.4V) poly-Nwell decaps on-chip. The PDVS load circuit uses multiple header switches to select each local core V_{DD} from a discrete set of global V_{DD} rails, depending on the local workload, which allows V_{DD} switching times near 1ns [2]. The PDVS controller shares connection information with the SIMO controller, allowing it to

set the priority of switching for the given rails. In this implementation, the highest priority is given either to 0.7V or 0.9V, since they will see a higher load than the 0.4V sub-threshold rail, unless their loads are power gated. The 0.4V supply can be used for operations during idle mode, in which case it will be lightly loaded, with the other rails potentially off. We have a lower static current mode for 0.4V rail. The proposed topology gives 86% peak efficiency over a wide range while using on-chip decap. It provides a low cost, highly efficient implementation for PDVS.

4.3 Conclusions

A model has been presented that can accurately capture the behavior of inductor based DC-DC converters in a dynamic environment. The converter model has been validated and compared with measured results from a variety of DC-DC converter topologies in existing literature. We used this model to study block level power management techniques for a SoC by incorporating it into a higher level model of the multiple block system. The system model predicts that there is a break-even time before the benefit of voltage scaling becomes positive, and our proposed modeling framework provides a quantitative means for comparing multiple power management techniques in a given use case scenario. Further, we proposed a SIMO DC-DC converter design for the PDVS system that can support a peak load of 50mA on the 0.9V and 0.7V rails, and 10mA on the 0.4V supply. To reduce system level volume and cost, we integrated two 4.3nF (0.9, 0.7V) and one 2.1nF (0.4V) poly-Nwell decaps on-chip. The proposed topology gives 86% peak efficiency over a wide range, while using on-chip decap. It provides a low cost, highly efficient implementation for PDVS.

Chapter 5

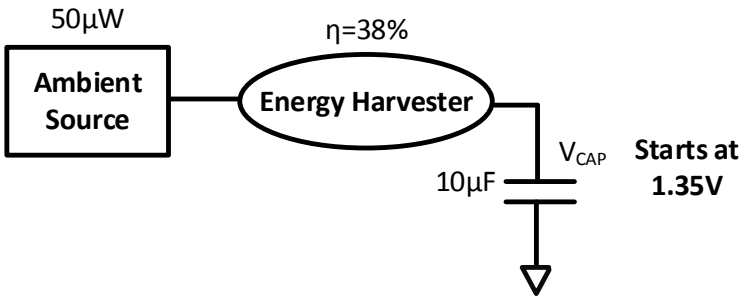
Conclusions

ULP SoCs, such as BSNs, WSNs, or IoTs, are used for sensing activities, our health, and the environment. These miniaturized nodes are responsible for sensing data periodically, processing it, and communicating through RF. The information about our environment, health, home, etc. can significantly improve the way we live. The sensor nodes can be used for many sensing applications – measuring and reporting everything from the flow of crude oil in a remote pipeline, to the degree of corrosion in a steel bridge, to EKG, EEG and EMG signals of a home health patient. These devices require small size and must consume extremely low power to be able to operate from harvested energy for their longer lifespan. Significant progress has been made over the last few years. However, there is a need to improve the operating lifetime of these systems, for their extensive deployment in the environment. This dissertation successfully improves the lifetime of the system by increasing the amount of harvested energy, reducing the losses in voltage conversion, reducing the operating voltage, and reducing the standby power consumption. Further, a modeling framework to enable accurate power management, and integrated on-chip implementation of the PDVS power management technique are also presented.

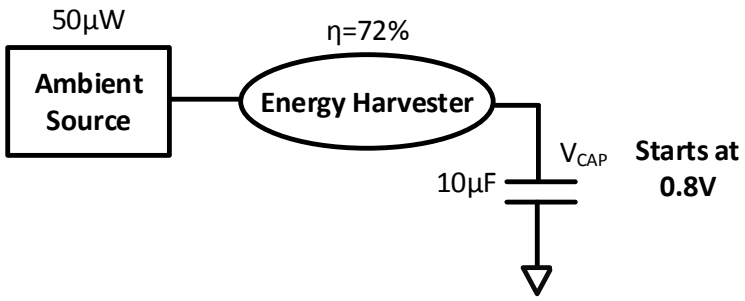
5.1 Impact of contributions on system life-time

This dissertation improves the lifetime of the system by increasing the amount of harvested energy, reducing the losses in voltage conversion, reducing the operating voltage, and reducing the standby

power consumption. Figure 5-1 shows the performance of the harvesting solution and low voltage operation compared with the state-of-the-art system [1]. The proposed solution starts operation at 0.8V compared to 1.35V in [1]. Therefore, the energy needed to start the system for BSN SoC [1] is 9.11µJ and 3.2µJ for the proposed EHM solutions, using a storage capacitor of 10µF. The proposed solution lowers the amount of energy needed to start the system by ~3X.



a) Energy Harvesting and operation of BSN SoC [1]



b) Energy Harvesting and operation with proposed Solution

Figure 5-1 Energy System level performance impact of the proposed EHM Solution

Further, both systems will have to start from zero energy level in a harvesting environment; therefore, system start-up time is another key metric. This is the time the system needs to achieve the operating voltage after ambient sources have available energy. The system start-up happens after cold start-up of 600mV for both systems. However, the BSN SoC [1] needs to achieve a start-

up voltage of 1.35V to start operating, compared to 0.8V in the proposed system. Further, the harvesting efficiency is 72% in the proposed system, compared to 38% in BSN SoC [1]. The system start-up time for BSN SoC comes out to be 384ms, compared to 20ms for the proposed system, thus lowering the system start-up time by ~20X. Therefore, the proposed solution reduces the start-up energy for the system by 3X and start-up time by 20X.

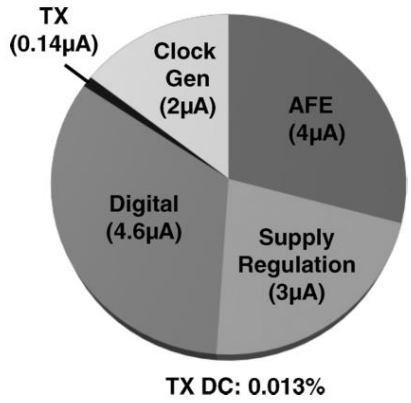


Figure 5-2 Current Consumption break-down of a BSN SoC [86] while performing ECG

Figure 5-2 shows the current consumption of various blocks in a BSN SoC [86]. The proposed solution reduces the power consumption of various blocks in the system. It reduces the power consumption of the clock source from 2.7µW to 1nW. The power consumption of supply regulation is brought down from 4µW to 0.5µW. Further, not included in this dissertation, the author has also proposed an ADC operating at 100nW. These contributions can bring the power consumption of the system to ~8µW. Now supposing the system is powered to 1.5V in both the cases and the harvesting source is cut-off. The time for the system to shut down is 112ms for the BSN SoC in [1], while using the proposed solution the system can be kept on for 1s, increasing the power down time for the system by 9X. The contributions help in reducing the start-up by 20X

and operational time by 9X for a system which is operating all the time. Figure 5-3 summarizes the results.

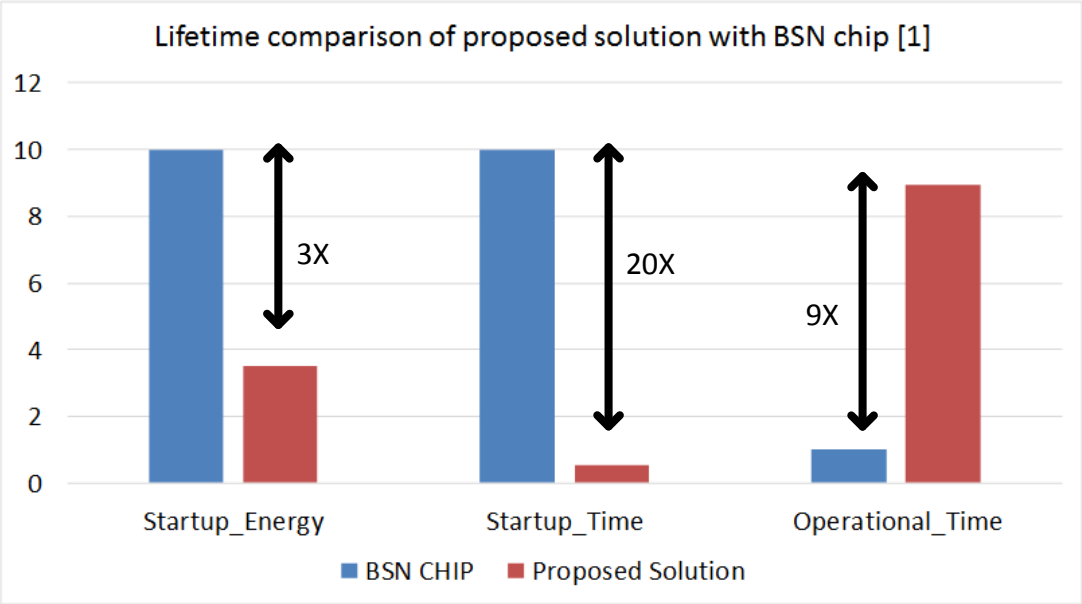
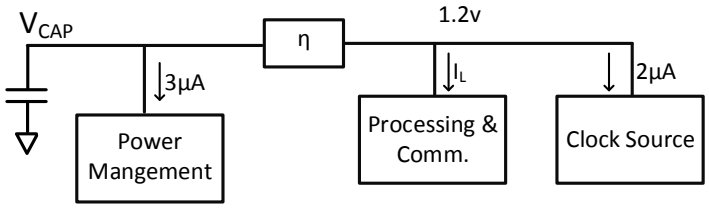
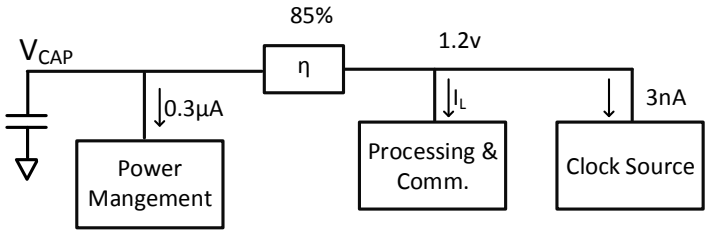


Figure 5-3 Lifetime improvement by proposed solution. The system start-up energy is reduced by 3X, start-up time by 20X and operational time is increased by 9X



a) Power consumption in BSN SoC



b) Power consumption with proposed solutions

Figure 5-4 Performance and power consumption of BSN SoC [1] and the proposed solutions

We showed the benefits from the proposed solution in a particular application. Now, a more general study of the improvement is presented. Figure 5-4 shows a system with power management and clock sources separated from the system. Both the clock source and power management circuit consume standby power, and they are always on. The power is delivered from the V_{CAP} through power management circuits with efficiency given by η. For the BSN chip [1], the power management circuit consumes 3µA current, while the clock source consumes 2µA current. The proposed solution reduces this power consumption to 0.3µA and 2nA respectively. A more general characteristic of the system can be obtained by varying the current for processing and communication blocks. These blocks are usually duty-cycled to save power. Therefore, a wider picture of the benefits from the proposed solution can be obtained by sweeping the average load current I_L, of processing and communication blocks.

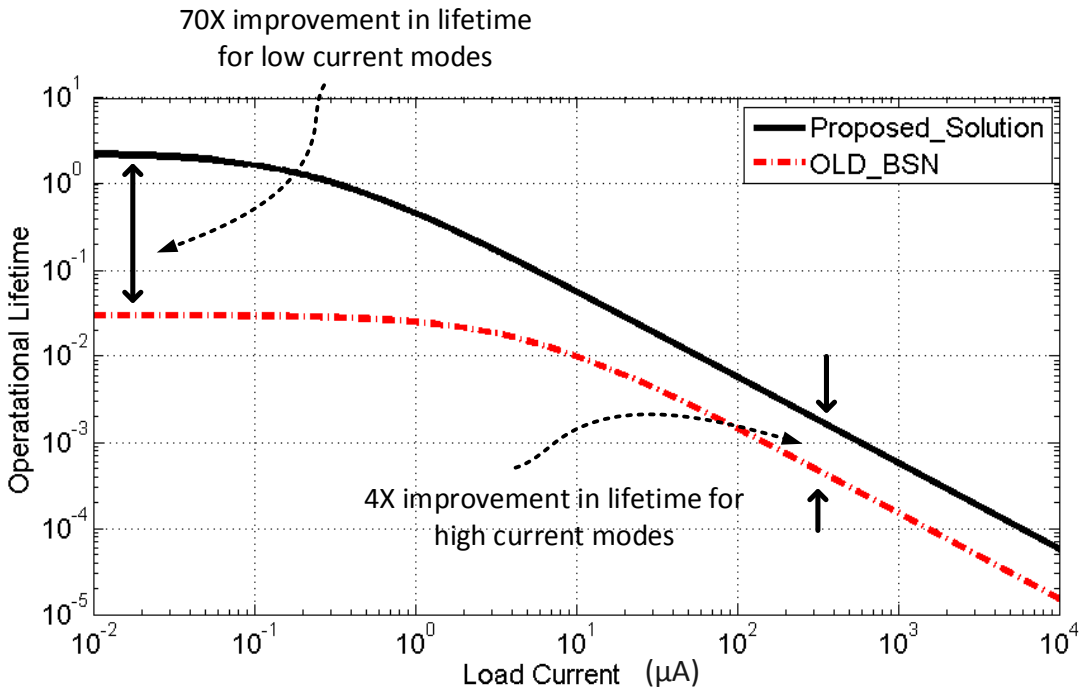


Figure 5-5 Operational lifetime improvement in ULP systems by using proposed contributions

Figure 5-5 shows the improvement in the operational lifespan of a BSN chip using the proposed solution. A 4X improvement in lifespan is achieved, using the proposed solution for cases when the system consumes higher power (mA). The 4X benefit is achieved through more efficient DC-DC converters and by enabling lower voltage operation for the system. The lifespan is increased by over 70X when the system consumes low power. At low power conditions, the lifespan is determined by power consumption of blocks that are always on. These are clock sources, and bandgap reference. The improved designs for clock sources, bandgap references, etc. presented in this dissertation, reduce the power consumption significantly. Further, lower voltage application also provides more energy for sustaining the operation for a longer time. These benefits are shown assuming the same amount of energy is harvested in both systems. However, our energy harvesting solution is more efficient and harvests from very low voltages, as well, which will increase the amount of harvested energy to further improve the lifetime.

5.2 Summary of Contributions

The solutions proposed in the dissertation improves the lifetime of the system by increasing the amount of harvested energy, reducing the losses in voltage conversion, reducing the operating voltage, and reducing the standby power consumption. The following contributions are made to achieve higher life-time for ULP systems.

- A stable on-chip clock source which can lock to a given clock frequency, a locking scheme to lock the clock source and ultra-low power on-chip clock sources to reduce the idle mode or standby.

- A ULP crystal oscillator circuit as an alternative clocking solution, with off-chip component with lower power and higher stability.
- A low power, high efficiency energy harvester that can harvest from 10mV ambient source to increase the amount of harvested energy.
- A low power, low voltage bandgap reference for energy harvesting and power management, to reduce the idle mode power consumption and enable low voltage operation.
- A single inductor, multiple output buck-boost converter, which enables high efficiency circuits as well as low voltage operation.
- A single inductor, multiple output energy harvesting and power management solution to harvest from low power solar cells to enable high efficiency, low cost, integrated harvesting and power management system.
- A model which accurately establishes the benefits of power management techniques for ULP SoCs in the presence of voltage regulators, to enable design time choices for regulators and power management techniques.
- Single Inductor Multiple output Voltage regulators with on-chip decoupling capacitors to implement panoptic dynamic voltage scaling technique.
- While not included in this dissertation, the author also made the following contributions for overall improvement in the ultra-low power system design.
    - A clock and data recovery (CDR) circuit for the RF interface of BSN;
    - A low power interconnect circuit operational from 0.3V to reduce the interconnect power consumption;
    - An ultra-low power analog to digital converter for ECG, EKG applications;

- Design and system level improvements and options for inter-chip communication between ULP ICs;
- Modeling techniques to assess circuit and system reliability;
- Circuit technique to improve the start-up time of a crystal oscillator by an order of magnitude.

5.2 Conclusions and Open Problems

The work that this dissertation describes improves the operational lifespan of ULP systems. The energy harvesting and power management circuits, voltage reference circuits, clock sources, PDVS SIMO DC-DC, overcome several challenges for increasing the lifespan of ULP systems. This section offers the key lessons from each of these areas and discusses opportunities for future work.

The ULP on-chip clock source provides a method for implementing a low power, stable, on-chip clock. However, the solution presents opportunity for improvements. For example, power consumption can be reduced significantly by reducing the power consumption of an uncompensated clock. A design effort is already underway to reduce this power. The proposed locking scheme locks only within the jitter at the input clock. Therefore, there is an opportunity to improve the locking scheme by implementing the lock through a PLL kind of architecture, to eliminate interference from noise. Further, the crystal oscillator power can potentially be reduced further if the swing of the oscillation is reduced to 100mV or lower. Even lower power consumption can further improve the system lifespan.

The energy harvesting solution provides an efficient means to harvest from low power, low voltage sources. However, a key improvement needed in this area is the ability to cold start circuit operational from very low voltages. These systems currently need an external source for wake-up, which comes in the form of RF kick-start or mechanical switch or transformers. There is a need for cold-start circuits that can operate from even lower voltages, as well as be small in shape and sizes. Further, the maximum power point tracking scheme needs external components, and it is based on predicted system behavior. Often, the MPP point can vary from its predicted point and a more robust maximum power tracking solution can further improve the system performance. Cost of the MPP circuit can also be reduced by reducing the external components.

The single inductor, multiple output solutions presented in this dissertation provide a low cost means for achieving higher efficiency. The solution can support current loads of up to 30mA, which caters to low power applications. However, even wider applications can be targeted by increasing the load current consumption to a few 100mA. A nice improvement over proposed designs will be SIMO for ULP systems that can support a few 100mA. The PDVS SIMO can be improved further by improving the transient behavior at fast load transients.

Appendix A: List of Acronyms

ADC	Analog to Digital Converter
AFE	Analog Front End
BOM	Bill of Material
BSN	Body Sensor Node
CCM	Continuous Conduction Mode
CDR	Clock Data Recovery
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CTAT	Complementary to Absolute Temperature
DC	Direct Current
DCCLK	Duty-Cycled Clock
DCM	Discontinuous Conduction Mode
DCO	Digitally Controlled Oscillator
DLL	Delay Locked Loop
DVFS	Dynamic Voltage and Frequency Scaling
DVS	Dynamic Voltage Scaling
ECG	Electrocardiogram
EEG	Electroencephalogram
EHM	Energy Harvesting and Power Management
EKG	Electrocardiogram
emf	electromotive force

EMG Electromyogram

ESR Effective Series Resistance

HS High Side

IC Integrated Circuits

IO Input Output

IoT Internet of Things

LV_T Low Threshold Voltage

LS Low Side

LDO Low Drop Out

MIM Metal Insulator Metal

MPP Maximum Power Point

MPPT Maximum Power Point Tracking

nMOS n-type Metal Oxide Semiconductor

Osc_{CMP} Compensated Oscillator

Osc_{REF} Reference Oscillator

Osc_{UCMP} Uncompensated Oscillator

PDVS Panoptic Dynamic Voltage Scaling

PFM Pulse Frequency Modulation

pMOS p-type Metal Oxide Semiconductor

PTAT Proportional to Absolute Temperature

PV Photo Voltaic (Solar Cell)

PWM Pulse Width Modulation

RF Radio Frequency

RLC Resistor Inductor Capacitor

RMS Root Mean Square

RTC Real Time Clock

SAR Successive Approximation Register

SIMO Single Inductor Multiple Output

SoC System on Chip

TDM Time Division Multiplexing

TEG Thermo Electric Generator

UDVS Ultra Dynamic Voltage Scaling

ULP Ultra Low Power

WSN Wireless Sensor Node

XTAL Crystal

Appendix B: Efficiency Dependence of DC-DC on Peak Inductor Current

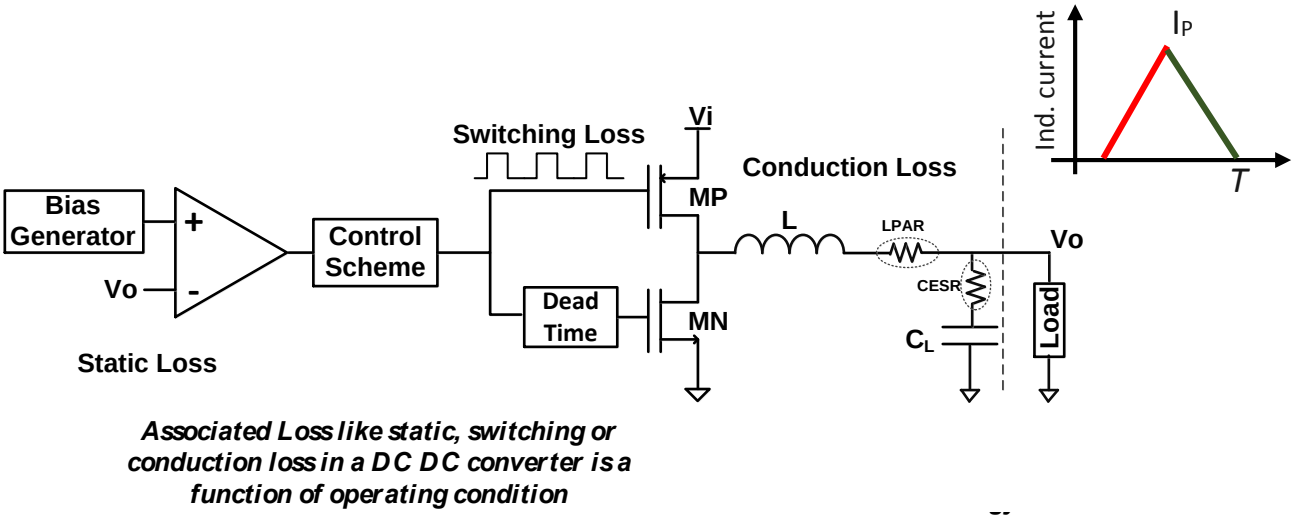


Figure A. 1 Losses in DC-DC converter

We presented methods to control the peak inductor current (I_P) in Chapter 3 for the buck and the boost converter designs. In this section we present the analytical reasons for controlling and maintaining a peak inductor current in DC-DC converter designs. The control of the peak current of the inductor is central to the maximization of the efficiency in a DC-DC converter. To understand the impact of peak inductor current on the efficiency of the DC-DC converter, we have to understand the losses in the DC-DC converter. In a DC-DC converter design, a control circuit is used for voltage regulation and for other control mechanisms. The control circuit usually contains analog circuits which consume static or bias currents for their operation. The energy overhead of the control circuits constitutes the Static losses in a DC-DC converter. This loss will be a constant for a given Vi and Vo combination. We denote the static energy loss as E_{ST}. The

control circuit continuously switches transistors MP and MN of Figure A.1 to charge the inductor. There is an energy overhead in switching the circuits and the transistors. This overhead is called switching loss. This loss is also a constant for a given Vi and Vo combination. We denote the switching loss as E_{SW}. Finally, the third component of losses inside the DC-DC converter is called the conduction loss (E_{CN}) and it occurs in the switches MP and MN and the parasitic resistance of the inductor and capacitor. The switch MP is turned on for a set time which charges the inductor to a peak current (I_P). The conduction loss is a function of the peak current. The total energy transferred in one switching cycle is also a function of I_P. Therefore, value of I_P plays a great role in the overall efficiency. The analytical analysis that follows explains the dependence of efficiency of a DC-DC converter on I_P. The total loss in one switching cycle of a DC-DC converter can be written as the sum of static, switching and conduction loss. Therefore,

$$E_L = E_{ST} + E_{SW} + E_{CN} \tag{A.1}$$

$$E_L = a + E_{CN} \tag{A.2}$$

Where *a* is the constant for the sum of switching and static loss. If the energy transferred in each cycle is given by E_T, then the percentage loss is given by,

$$\eta_L = \frac{E_L}{E_T} = \frac{a + E_{CN}}{E_T} \tag{A.3}$$

A switching cycle in DC-DC converter involves charging the inductor to I_P and then transferring the stored energy in the inductor to the load. Assuming that the losses involved in charging the inductor is very small compared to the energy stored in it, the total energy transferred from source voltage Vi to output load can be approximately given by,

$$E_T = 0.5 L {I_P}^2 \tag{A.4}$$

Now we will try to find out the conduction loss in terms of I_P.

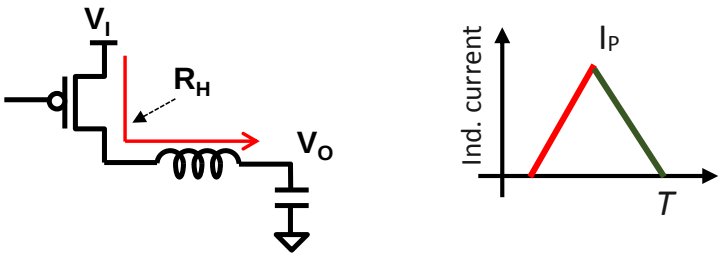


Figure A. 2 High side conduction

The switching cycle involves two conduction cycles, high side (HS) and low side (LS) switching as explained in Chapter 3. Both HS and LS switching involves conduction loss. Let us say that the total resistance shown in the HS conduction is given by R_H. Assuming that the inductor charges from 0 to I_P current in high side turn on time T_{HS}. Therefore, total conduction loss in high side switching can be written as,

$$E_{CN,H} = \int_0^{T_{HS}} i^2 R_H \, dt \tag{A.5}$$

Also, the inductor charging is given by,

$$L\frac{di}{dt} = (Vi - Vo) => dt = \frac{Ldi}{Vi - Vo} \tag{A.6}$$

Putting it in equation (A.5) we get,

$$E_{CN,H} = \int_0^{I_P} \frac{i^2 R_H \, Ldi}{Vi - Vo} \tag{A.7}$$

Therefore,

$$E_{CN,H} = \frac{LR_H {I_P}^3}{3(Vi - Vo)} \tag{A.8}$$

Similarly, the low side conduction loss can also be obtained. Figure A. 3 shows the case when inductor current discharges.

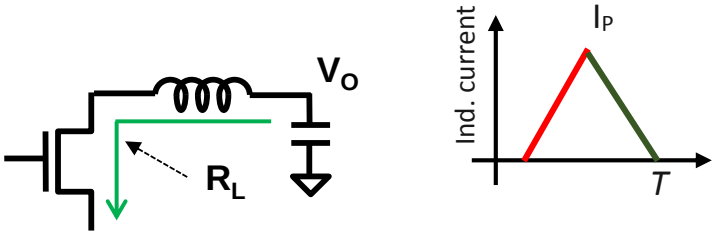


Figure A. 3 Low side loss

Total conduction loss in high side switching can be written as,

$$E_{CN,L} = \int_0^{T_{LS}} i^2 R_L \, dt \tag{A.9}$$

The inductor discharge rate will be given by,

$$L\frac{di}{dt} = -Vo \Rightarrow dt = -\frac{Ldi}{Vo} \tag{A.10}$$

Therefore,

$$E_{CN,L} = -\int_{I_P}^{0} \frac{i^2 R_L \, Ldi}{Vo} \tag{A.11}$$

Therefore,

$$E_{CN,L} = \frac{LR_H {I_P}^3}{3Vo} \tag{A.12}$$

Total conduction loss is given by,

$$E_{CN} = E_{CN,H} + E_{CN,L} = \frac{L}{3}\left(\frac{R_H}{Vi - Vo} + \frac{R_L}{Vo}\right){I_P}^3 = b{I_P}^3 \tag{A.13}$$

Where b is given by $\frac{L}{3}\left(\frac{R_H}{Vi-Vo} + \frac{R_L}{Vo}\right)$. Therefore, total loss using equation (A.2) is given by,

$$E_L = a + b{I_P}^3 \tag{A.14}$$

Therefore total percentage loss is given by,

$$\eta_L = \frac{E_L}{E_T} = \frac{a + bI_P{}^3}{0.5LI_P{}^2} \tag{A.15}$$

Therefore,

$$\eta_L = \frac{a}{0.5LI_P{}^2} + \frac{bI_P}{0.5L} \tag{A.16}$$

The expression in equation (A.16) increases at both high and low values of I_P. The minimum loss is given by,

$$\frac{d\eta_L}{dI_P} = -\frac{4a}{LI_P{}^3} + \frac{2b}{L} \tag{A.17}$$

The I_P value for minimum loss is given by,

$$I_P = \sqrt[3]{\frac{2a}{b}} \tag{A.18}$$

Therefore a minimum loss or the maximum efficiency of the DC-DC converter is given by the peak inductor current I_P given by equation (A.18). The given analytical expression proves the need for maintaining a constant peak inductor current.

Appendix C: List of Publications

[AS1] A. Shrivastava, and B. H. Calhoun, “A 50nW, 100kbps Clock/Data Recovery Circuit in an FSK RF Receiver on a Body Sensor Node” VLSI Design Conference. Jan. 2013.

[AS2] Y. Zhang, F. Zhang, Y. Shakhsheer, J. Silver, M. Nagaraju, A. Klinefelter, J. Pandey, J. Boley, E. Carlson, A. Shrivastava, et al., "A Batteryless 19 uW MICS/ISM-Band Energy Harvesting Body Sensor Node SoC for ExG Applications “, Journal of Solid State Circuit, Jan. 2013.

[AS3] A. Shrivastava, Y. Ramadass, S. Bartling and B. H. Calhoun, “Single Inductor Energy Harvesting and Power Management Circuit for Body Sensor Nodes”, ISSCC SRP 2013.

[AS4] A. Shrivastava, and B. H. Calhoun, “Modeling DC-DC Converter Efficiency and Power Management in Ultra Low Power Systems"” Sub-threshold Conference Oct-2012.

[AS5] A. Shrivastava, and B. H. Calhoun, “A 150nW, 5ppm/o C, 100kHz On-Chip Clock Source for Ultra Low Power SoCs” Custom Integrated Circuits Conference. Sept. 2012.

[AS6] A. Shrivastava, J. Lach, and B. H. Calhoun, “A Charge Pump Based Receiver Circuit for a Voltage Scaled Interconnect” International Symposium on Low Power Electronics and Design, Jul. 2012

[AS7] F. Zhang, Y. Zhang, J. Silver, Y. Shakhsheer, M. Nagaraju, A. Klinefelter, J. Pandey, J. Boley, E. Carlson, A. Shrivastava, et al., "A Batteryless 19uW MICS/ISM-Band Energy Harvesting Body Area Sensor Node SoC", International Solid State Circuits Conference, Feb. 2012.

[AS8] A. Shrivastava, and B. H. Calhoun, “A sub-threshold clock and data recovery circuit for a wireless sensor node”, Sub-threshold Conference. Sept. 2011.

[AS9] A. Shrivastava, and B. H. Calhoun, “A DC-DC Converter Efficiency Model for System Level Analysis in Ultra Low Power Applications”, Journal of Low Power Electronics Application 3-2013

[AS10] A. Shrivastava, Y. K. Ramadass, S. Khanna, S. Bartling, and B. H. Calhoun, “A 1.2µW SIMO Energy Harvesting and Power Management Unit with Constant Peak Inductor Current Control Achieving 83-92% Efficiency Across Wide Input and Output Voltages” , Symposia on VLSI Technology and Circuits, June 2014

Upcoming Publications : Own

[AS11] SIMO for PDVS Implementation, *Submitted*

[AS12] A 10mV TEG boost converter, *Submitted*

[AS13] Ultra-low power crystal oscillator, *Submitted*

[AS14] A low power ADC Circuit, *Submitted*

Upcoming Publications : Group

[AS15] BSN Chip-2

[AS16] Low Power Clocking solution

Patents:

[AS17] A. Shrivastava, and Y. Ramadass, “Apparatus and Method for Controlling Peak Inductor Current in a Switched Mode Power Supply” US Patent application 13768448

[AS18] A. Shrivastava, Y. Ramadass, and S. Bartling, “Single Inductor Energy Harvesting and Management Interface System and Method” US Patent application

[AS19] A. Shrivastava, and B. H Calhoun, “Single Inductor Multiple Output (SIMO) Step-down DC-DC Converter for Ultra Low Power SOCs” US Patent application 61/700979

[AS20] A. Shrivastava, and B. H. Calhoun. US Patent Application 61/698,534. “On-Chip Clock Source for Ultra Low Power SoCs”

[AS21] A. Shrivastava, et al, US Patent 8120439 “A Fast Start-up Crystal Oscillator”

[AS22] A. Shrivastava, and B. H. Calhoun. US Patent Application. “Ultra-Low Power crystal oscillator circuit”

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