Processing and Properties of Si-based Bulk Nanocomposites and Hybrid Devices for Thermoelectric Applications

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Abstract

Thermoelectric (TE) materials can directly convert waste heat into electrical energy. The conversion efficiency is an increasing function of a dimensionless figure of merit, $ZT=S^2\sigma T/\kappa$, where S is the Seebeck coefficient, σ is the electrical conductivity, $S^2\sigma$ is the power factor, κ is the thermal conductivity, and T is the temperature. One of the main challenges in the design of thermoelectric materials with better performance is to minimize the thermal conductivity while preserving the electrical conductivity. This requires mechanisms that scatter heat-carrying phonons without perturbing the electrons. Nanostructuring, combined with electronic structure optimization, can be an effective approach to enhance thermoelectric performance. This strategy can potentially decouple the thermal and electrical properties, as electrons and phonons possess different characteristic lengthscales of wavelength and mean free path.

Both Si-based bulk nanocomposite (work 1) and nano-meshed thin-film (work 2) materials are studied in this dissertation. Both works aim to understand the coupling between processing/fabrication, the resultant nanostructuring, and thermal/electronic transport. In work 1, synthesis and transport properties of the bulk Fe-Si-Ge system is studied. Synergistic approaches including hierarchical structuring, phase percolation, and selective doping are implemented using a novel powder process scheme, successfully improving the thermoelectric performance of eco-friendly β-FeSi2 – SiGe nanocomposites, which are promising for industrial-scale waste heat recovery applications. In work 2, a holey Si thin-film device is fabricated and the in-plane electrical/thermal transport properties are studied. Subsequently, a hybrid F_4TCNQ – Si device utilizing organic – inorganic charge transfer as doping mechanism is investigated. We anticipate that this study will open a door for applying the concept of hybrid holey Si/organics towards efficient thermoelectric materials in device applications.

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List of Terms and Symbols

TE: Thermoelectric

S: Seebeck coefficient

σ: Electrical conductivity

κ: Thermal conductivity

κ_L: Lattice thermal conductivity

κ_e: Lattice thermal conductivity

ZT: Thermoelectric figure of merit

RTG: Radioisotope thermoelectric generators

n: Carrier concentration

μ: Carrier mobility

DOE: Density of states

m^*: Effective mass of electron

MFP: Mean free path

k_B: Boltzmann constant

E_f: Fermi energy

h: Plank's constant

ω: Phonon frequency

$\hbar$: Reduced Planck constant

v: Speed of sound

θ_D: Debye temperature

τ: Relaxation time

L: Lorentz number

2DEG: 2D electron gas

SOI: Silicon on insulator

SPS: Spark plasma sintering

DC: Diamond cubic

R/T SPS: React/transform spark plasma sintering

EBL: Electron beam lithography

RIE: Reactive ion etching

RTP: Rapid thermal annealing
PVD: Physical vapor deposition
XRD:X-Ray diffraction
SEM: Scanning electron microscopy
EDS: Energy-dispersive X-ray spectroscopy
FIB: Focused Ion Beam
TEM: Transmission Electron Microscopy
AFM: Atomic Force Microscopy
V_H: Hall voltage
α: α-FeSi2
BSE: Backscattered Electrons
β: β-FeSi2
ρ: Density
DSC: Differential Scanning Calorimetry
ε: ε-FeSi
v_g: Group Velocity
C_p: Heat Capacity at Constant Pressure
JMA: Johnson-Mehl-Avrami
S2σ: Power Factor
TDTR: Time Domain Thermoreflectance
MODFET: Modulation-doped field-effect transistors
HEMT: High electron mobility transistors
LUMO: Lowest unoccupied state
F_4TCNQ: Tetrafluoro-tetracyanoquinodimethane
RMS: Root mean square

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Chapter 1: Introduction

1.1. Fundamentals of thermoelectrics

Currently more than 65% of energy consumption is dissipated as waste heat, which provides the broad context of use for Thermoelectric (TE) materials in both power generation and waste heat recovery. TE materials can directly convert heat into electrical energy. The conversion efficiency is an increasing function of a dimensionless figure of merit *ZT* expressed as:

$$ZT = \frac{S^2\sigma}{\kappa}T \qquad 1\text{-}1$$

where *S* is the Seebeck coefficient, σ is the electrical conductivity, $S^2\sigma$ is the power factor, κ is the thermal conductivity, and *T* is the temperature. In order to maximize *ZT*, one needs to improve the power factor while suppressing the thermal conductivity according to Eq. 1-1.

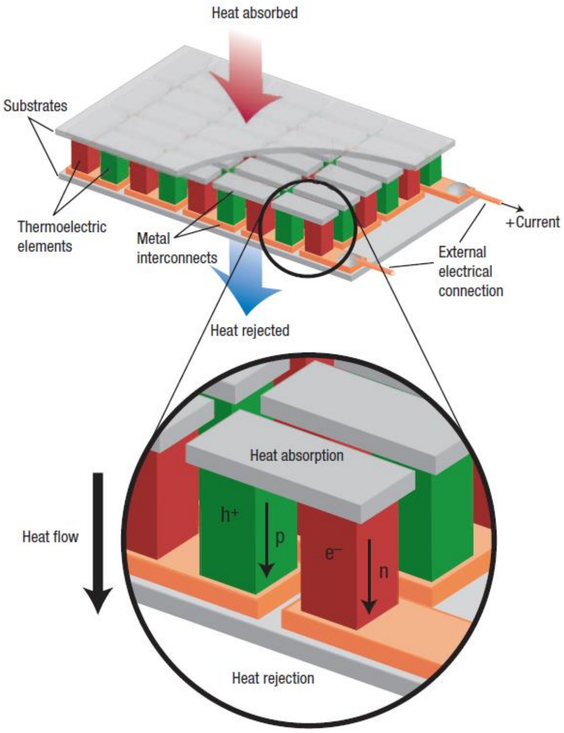

Figure 1-1: Cartoon of a thermoelectric module with a zoom-in view of the TE legs[1]

A TE module is shown in Figure 1-1[1], which is comprised of a series of p–n thermoelectric couples. Each couple consist of a p- and n-type “leg” connected electrically in series and thermally in parallel, sandwiched between a heat source and heat sink. Due to the Seebeck effect, charge carriers diffuse from the hot side to the cold side, generating a voltage, and thereby a current for power generation when the circuit is closed. This module can also be operated in a reversed manner by instead supplying electricity to cool one side of module by extracting heat from the junction via the

Peltier effect. Eq.1-2 shows the maximum efficiency of a TE module as a power generator.

$$\eta_{max} = \frac{T_h - T_c}{T_h} \frac{\sqrt{1+Z\bar{T}}-1}{\sqrt{1+Z\bar{T}}+\frac{T_c}{T_h}} \qquad 1\text{-}2$$

where T_h and T_c are the temperatures of the hot side and cold side respectively. $\bar{T}$ is the average of T_c and T_h. Apparently, η_{max} is always smaller than $\frac{T_h-T_c}{T_h}$ (Carnot efficiency), and is an increasing function of *ZT*. Therefore, maximizing the *ZT* of the material is the overarching goal in developing efficient thermoelectric devices. However, improving ZT towards competitive efficiencies (~20%) is extremely challenging in practice. Figure 1-2 shows the η_{max} vs. T_h when T_c is fixed at 300K. The commercial thermoelectric materials (eg., Pb-Te based systems) nowadays generally possess

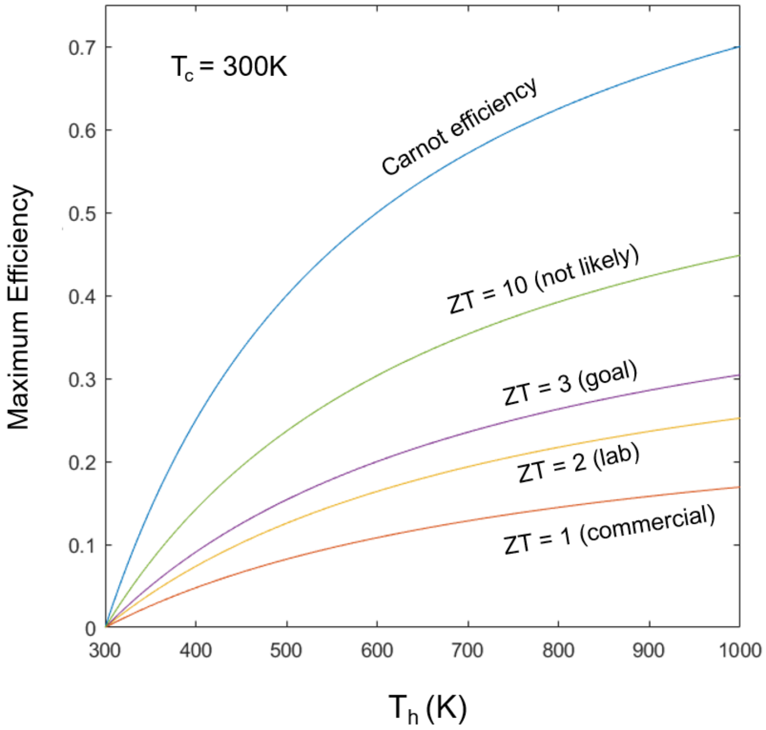

Figure 1-2: Maximum efficiency vs. hot side temperature of TE module (derived from Eq. 1-2)

a ZT of ~ 1, which gives an efficiency around 10% under a reasonable temperature differential. Considering the efficiency of other alternative energy sources, such as 50% ~ 70% for fuel cells, 40% ~ 50% for wind turbines, and 20% ~ 40% for both biomass and tidal turbines, TE materials can hardly compete with them as a routine solution for primary electricity generation. Take the widely applied photovoltaic technology as an example, so far the efficiency of commercial solar cell can reach up to ~ 20%, which would be equivalent to that of TE material with $Z\bar{T}$~2 under temperature differential of ~ 500K. Note that here $Z\bar{T}$ is the average ZT of the working temperature range. And it is also on the premise that both n-type and p-type of the same system are available, and the electrical and thermal resistances of the contacts and electrodes are neglected.

On the other hand, TE materials inherently have no moving parts and extremely long life-times, which made them favorable in space applications such as radioisotope thermoelectric generators (RTG), in which decaying radioactive material produces heat that the thermoelectric module converts to provide continuous electrical energy to the spacecraft without maintenance. Other applications as a power source are limited to niche markets, such as wearable device or sensors using body heat, geothermal TE generators using vast geothermal resources, and solar thermoelectric generators (STGE) using the heat generated by concentrated sunlight, etc.

TE materials for waste heat recovery, one the other hand, can potentially create a greater impact. So far it has been tentatively used in automotive industry to harvest the waste heat (~40% of total energy from combustion) from the exhaust heat exchanger, which is well-suited to hybrid cars. Potential applications recovering the waste heat from power plants and industrial furnaces represent a large-scale application that brings in the challenge of developing low-cost and eco-friendly TE materials with good performance, which motivates our investigation of Fe-Si based thermoelectric materials. A detailed study is present in Chapter 3 & 4 of the dissertation.

Thin film or micro/nanoscale TE devices are promising in biomedical and sensing applications, as a continuous power supply is crucial, yet only a very small energy output is required. On-chip thermal management using Peltier effect is also a hot topic in research nowadays, as increased device integration and downscaling drives the pressing issue of heat dissipation beyond just passive cooling. Thus nanoscale refrigeration cooling or active cooling technologies are needed for high power microelectronics. In this context, we are motivated in studying the thermoelectric transport of holey Si thin film and its hybrid device, which will be discussed in the Chapter 5 of the dissertation.

1.2. Thermoelectric transport parameters

As shown earlier in Eq. 1-1, to improve ZT, one needs to improve electrical transport while suppressing thermal transport. In practice, these two aspects in one material are usually coupled in a complex way. This section will provide more details on each parameter underlying thermoelectric transport, with implications towards ZT optimization strategies, which will be described in Section 1.3.

The ***electrical conductivity***, $\boldsymbol{\sigma}$, depends on the concentration (n/p) and mobility (μ) of charge carriers in the material, expressed as follow:

$$\sigma = n(p)q\mu \qquad \text{1-3}$$

where q is the elementary charge (= 1.6×10^{-19} C). Metals usually possess high electrical conductivity due to high carrier density (>10^{22} cm^{-3}). However, since the Fermi level is deep within the conduction band, and density of states (DOE) differential in vicinity of the Fermi level is too little to generate a large Seebeck voltage. Therefore, TE materials with high performance usually come from heavily doped semiconductors or potentially semimetals. The optimized carrier concentration is generally on the order of 10^{19}~10^{20} cm^{-3}.

The mobility μ also possesses technical significance as a variable in tuning electrical transport. It has the following relationship:

$$\mu = \frac{q\tau}{m^*} \qquad 1\text{-}4$$

where m^* is the effective mass of the charge carrier, and τ is the carrier relaxation time. m^* depends on the morphology of band structure, which can be modified by e.g. alloying. τ can be affected by scattering processes associated with defects or heterophases in the material. Thus a careful control of materials chemistry and microstructure is essential in ensuring a large mean free path (MFP) of charge carrier to improve electrical transport.

The ***Seebeck coefficient***, ***S***, as mentioned, results from the asymmetry in the density of states (DOS) around the Fermi level or chemical potential, and gernerally the dominant charge carrier determines the sign of the Seebeck coefficient, i.e., a negative *S* is expected from the n-type materials with electron transport and a positive *S* is expected from p-type materials with hole transport. One of the challenges in TE materials design is associated with the considerable interplays between with the Seebeck coefficient and the aforementioned parameters regarding the electrical conductivity. *S* can be determined by the Mott formula in Eq. 1-5

$$S = \frac{\pi^2 k_B^2 T}{3q} \left| \frac{\partial[ln\sigma(E)]}{\partial E} \right|_{E=E_f} \qquad 1\text{-}5$$

where k_B is Boltzmann constant, E_f is Fermi energy. To access more insights, Eq. 1-5 can also be expressed as:

$$S = \frac{\pi^2 k_B^2 T}{3q} \left(\frac{g(E)}{n} + \frac{1}{\mu} \frac{\partial \mu}{\partial E} \right)_{E=E_f} \qquad 1\text{-}6$$

where $g(E)$ is the density of states near E_f, suggesting a large S can be obtained when there is local increase in DOS over E_f. It is also indicated that increasing the energy dependence of mobility μ is expected to improve S, for instance by introducing a scattering mechanism that strongly depends on the energy of charger carrier, referred as "energy filtering" effect[2]. In addition, S is inversely related to carrier concentration n and mobility μ. Therefore, the tradeoff between Seebeck coefficient improvement and electrical conductivity reduction must be carefully examined in terms of materials design.

For degenerately-doped semiconductors, assuming a single parabolic band with energy-independent scattering approximation, the Seebeck coefficient is given by [3]:

$$S = \frac{8\pi^2 k_B^2}{3qh^2} m^* T \left(\frac{\pi}{3n}\right)^{2/3} \quad 1\text{-}7$$

where h is Plank's constant, n is carrier concentration, and m^* is the effective mass of charge carrier. According to this equation, larger m^* is favored for improving S. However, increasing m^* would result in lower mobility, as discussed previously in Eq. 1-4. Therefore, an alternative parameter called weighted mobility $(m^*)^{2/3}\mu$ is used in terms of optimization.

The ***thermal conductivity,*** κ, consists of contributions from both the lattice thermal conductivity (κ_L) and the electronic thermal conductivity (κ_e). κ_L is determined by the distribution and mobility of phonons, which are the quantum expression of the crystal vibrational field. Using the Debye model, lattice thermal conductivity can be expressed as:

$$\kappa_L = \frac{{k_B}^4 T^3}{2\pi^2 v \hbar^3} \int_0^{\theta_D/T} \tau \frac{x^4 e^x}{(e^x - 1)^2} dx \quad 1\text{-}8$$

where $x = \hbar\omega/k_BT$, k_B is the Boltzmann constant, ω is the phonon frequency, $\hbar$ is the reduced Planck constant, v is the speed of sound, θ_D is the Debye temperature, and τ is the total phonon scattering relaxation time. The most critical takeaway from the Debye approximation is that κ_L is dependent on the relaxation time of various phonon scattering processes. In other words, unlike electrons, it is necessary to minimize the MFP of the phonons in the material. The total scattering rate (τ^{-1}) can be empirically expressed using Matthiessen's rule, assuming each scattering mechanism is independent. For different material systems, the possible scattering processes can be derived from: point defects (${\tau_{PD}}^{-1}$), including impurities, alloying and vacancies; phonon-phonon scattering (or Umklapp scattering ${\tau_U}^{-1}$), where total crystal momentum is not conserved; and boundary scattering (${\tau_b}^{-1}$), sometimes referred as the "size effect", which is dependent on the crystal dimensions, grain boundaries or heterointerfaces. The total scattering rate can then be expressed by the sum of these scattering contributions (additional scattering mechanisms may be significant in certain cases), as follows:

$$\tau^{-1} = {\tau_{PD}}^{-1} + {\tau_U}^{-1} + {\tau_b}^{-1} \tag{1-9}$$

Therefore, materials chemistry modification, defect engineering and nanostructuring are often considered to reduce the phonon relaxation time, so as to minimize the lattice thermal conductivity.

The electronic component of the thermal conductivity is determined by the charge carriers contributing to the heat conduction via the Wiedemann-Franz Law:

$$\kappa_e = L\sigma T \tag{1-10}$$

where L is Lorentz number, σ is electrical conductivity and T is temperature. In metal or degenerate semiconductors where charge carrier can be considered as free electrons, $L = 2.44 \times 10^{-8}\ W\Omega K^{-2}$. For non-degenerate semiconductors, determining L can be non-trivial and is usually based on some empirical formula[4]. In some intrinsically low lattice thermal conductivity materials, for instance large atomic mass or complex unit cell systems, their κ_e can be comparable or even larger than κ_L, thus careful examination is needed as suppressing κ_e by reducing σ conflicts the purpose of improving the power factor.

1.3. Strategies to improve TE performance

With the discussions on the TE parameters, it can be seen that the major difficulty in the design of thermoelectric materials with better performance is to minimize the thermal transport while preserving the electrical transport. This requires mechanisms that scatter heat-carrying phonons without perturbing the electrons. While each parameter can be tuned in orders of magnitude, the complex coupling and interplay amongst these properties makes it challenging to optimize the ZT beyond values of about 1. In this section, I will discuss a few strategies that aimed to decouple the electrical and thermal transport, including nanostructuring, electronic structuring modification, novel doping schemes and phase percolation. These strategies are directly related to the materials systems in my dissertation work.

1.3.1. Nanostructuring (bulk and thin film)

Embedding nanostructures in bulk materials is an effective strategy to improve thermoelectric performance, mainly by suppressing thermal conductivity, which can either be understood in terms of size-dependent phonon scattering rates, or in terms of high thermal boundary resistance[5–8]. Oftentimes, the reduction of thermal conductivity can prevail the compromise in electrical conductivity as the characteristic length scales of phonons and electrons generally have orders of magnitudes' difference, thus their respective scattering processes are to some extent independent.

Nanostucturing in the context of bulk material synthesis usually refers to nanosized grains or introducing nano-inclusions. The former can be achieved by sintering nanopowders of the material (e.g. by mechanical alloying) or by recrystallization under diffusion kinetics that suppress grain growth. The latter can also be achieved by sintering a nanosized multi-phase mixture. However, this gives a very limited morphological control and tends to introduce considerable impurities and defects that deteriorate the power factor due to high inter-grain or matrix/inclusion interface resistance. Solid-state transformation offers an elegant approach to synthesize nanocomposites in a self-assembled fashion, in which case the electron-trapping defects and exterior impurities can be significantly reduced. More importantly, by accessing specific stoichiometric and kinetic windows, one can have a precise control of the morphology and length scales of the microstructure, as illustrated in Fig. 1-3.

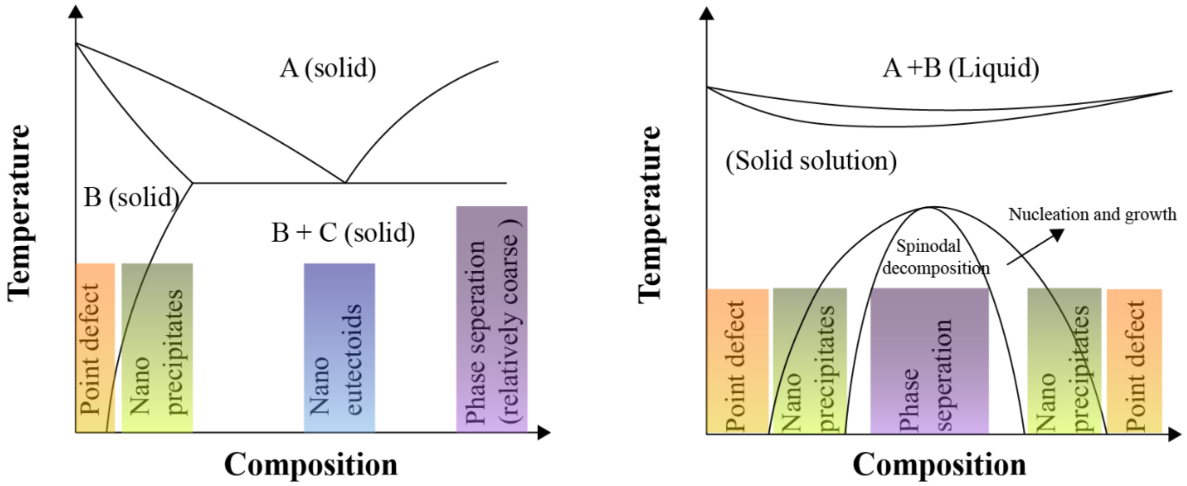

Figure 1-3: illustrative phase diagrams showing a) precipitation and eutectoid decomposition, and b) spinodal decomposition

Figure 1-3 a) shows the phase diagram where either precipitation or eutectoid decomposition may be exploited. When supersaturated (by quenching) solid solution B is annealed at relatively low temperature, it will normally undergo precipitation of C phase nanoparticles homogeneously distributed in the B phase matrix. The precipitates in this case would have a small volume fraction. Nevertheless, the particle size can be on the nanometer scale, resulting in a high interface density and small interparticle spacings, which may effectively scatter phonons. Figure 1-3 a) also shows eutectoid decomposition, where the solid phase A can decompose into another two solid phases B and C. The eutectoid products can also be nanoscale when diffusion kinetics are carefully controlled. Unlike precipitation, the minority eutectoid phase usually possesses higher volume fraction, in which case its impact on electrical transport needs to be examined more carefully. The β-$FeSi_2$ – SiGe nanocomposites in this work follows the eutectoid decomposition route, which will be elaborated in Chapter 3. Similar strategies are possible in in spinodal decomposition systems, under certain composition and process parameters, as shown in Figure 1-3 b). One key difference is that spinodal systems tend to have much more diffuse heterointerfaces.

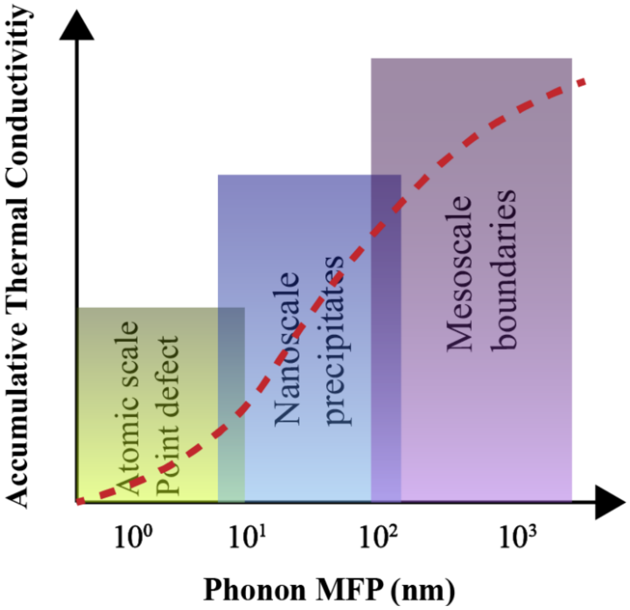

Figure 1-4: Schematic of accumulative thermal conductivity versus phonon MFP contribution, with respect to the structural length scales in TE materials

If one can access multiple thermodynamic or kinetics windows in the synthesis process, two or more length scales of constituent phases can potentially be obtained. This brings in the concept of *hierarchical structuring*. As heat-carrying phonons possess a broad range of wavelengths and mean free paths (MFP), maximal reduction in lattice thermal conductivity via all-scale phonon scattering may be achieved by hierarchical structuring from atomic-scale lattice disorder, to nanoscale inclusions, to mesoscale grain boundaries. This concept of hierarchical structuring has been successfully applied in some lead chalcogenide systems[9,10]. However, for mid – high temperature range TE materials, due to their relatively high sintering temperature, in order to initiate nucleation/growth meanwhile avoiding over-coarsening puts strict constrains on synthesis parameters (e.g. maximum temperature and its corresponding holding time). Alternative process routes to address this issue will be discussed in later sections.

In the context of low dimensional systems, such as thin films (2D), nanowires (1D) and quantum dots (0D), the "size effect" can play a crucial role, as the dimensionality acts as a cutoff limit for phonon MFPs. For practical TE device applications, thin films are still the most feasible and accessible option among the three. However, reduced thickness of a film may not sufficiently reduce thermal conductivity. Therefore, growing alternating superlattice structures to introduce a significant boundary resistance, or fabricating nanopatterned holey films or nano-meshed structures to increase surface scattering by maximizing the surface-volume ratio have been exploited. In both cases, the characteristic structures are ordered, so that the electrical transport can be preserved. This concept is often times referred as the "phonon glass, electron crystal" approach. In Chapter 5, I will discuss the heavily-doped holey Si device based on this consideration.

1.3.2. Control of interface (for charge transport) and electronic modification

Nanocomposites have been shown to be effective in reducing thermal conductivity. However, heterointerfaces are usually associated with excess defects and may also exhibit band discontinuities that restrain electrical carriers. Therefore, *control of interfaces* (in terms of minimizing charge-trapping defects) and *band alignment*[11,12] have been exploited in order to minimize the degradation of electrical transport as result of nanostructuring. On the other hand, considering the power factor ($S^2\sigma$), the electrical conductivity and Seebeck coefficient have inverse relationships with the carrier concentration, assuming a parabolic band structure. The carrier concentration is thereby subject to a tradeoff, which limits the magnitude of the resultant power factor. Significant efforts have been taken to decouple the two electrical parameters. The fundamental mechanism is to manipulate electronic structure by modification of density of states, such as achieving *band convergence* and *resonant states*. In this section, strategies to facilitate charge transport and to modify the electronic structure will be discussed.

Control of interfaces is crucial in multi-phase systems, aimed to decouple the electrical and thermal transport. In the case of *coherent interfaces*, the surrounding atomic order is not disrupted compared with incoherent interfaces, in which interfacial dislocations can act as charge traps that are detrimental to the electrical transport, resulting in limited ZT improvement in spite of increased phonon scattering. Coherent interfaces can be present when the constituent phases are chemically and structurally similar, usually by phase precipitation or separation via metallurgical methods. In general, the embedded phase or precipitates are kept very small (<10 nm) to avoid dislocation formation. Meanwhile, due to the lattice mismatch, there is certain degree of strain associated with the interfaces. These so-called “endotaxial” strained interfaces are expected to facilitate charge transport but strongly block/scatter phonon propagation[13]. Figure 1-5 shows the typical strained endotaxial nanostructuring present in PbTe – SrTe system[14], where 2~4 nm SrTe nanoprecipitates are coherently embedded in the PbTe matrix.

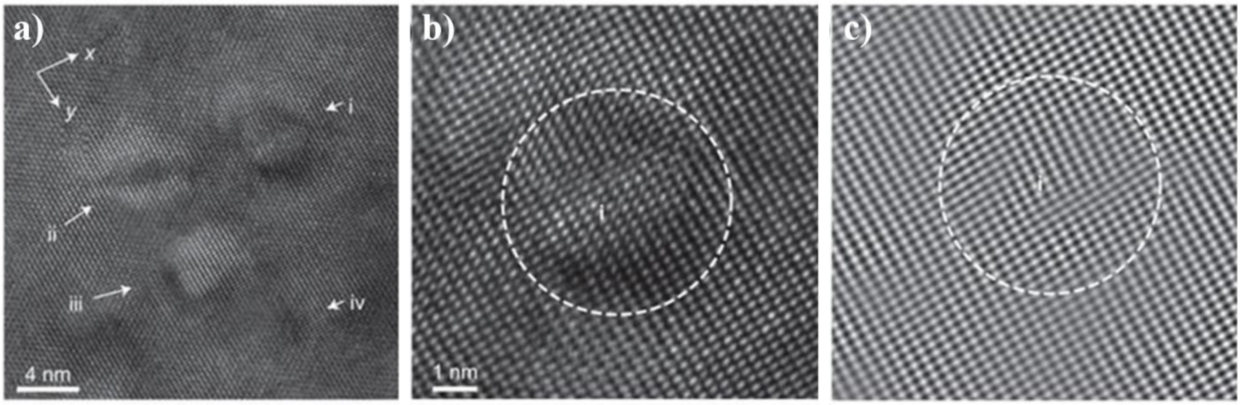

Figure 1-5: a) High-resolution TEM image of SrTe nanoprecipitates (i, ii, iii, and iv) embedded in the PbTe matrix; b) enlarged view of nanoprecipitate i showing coherency at the boundary highlighted by the dotted line; c) Inverse first Fourier transform image of precipitate i, indicating the absence of dislocations at the interface. Reproduced from Ref [14]

Since minimizing grain size is pervasive in nanostructured TE materials, a high density of grain boundaries is also of great concern regarding the electrical transport. The use of solid-state, displacive phase transformations to produce a fine distribution of coherent domain boundaries could provide a new and useful route to electronically benign interfaces[15]. Yu, et al, used a so-called liquid state manipulation (LSM) method followed by melt-spinning, ball mill and spark plasma sintering to synthesize $Bi_{0.5}Sb_{1.5}Te_3$ alloy with large density of homogeneously distributed twin boundaries[16]. It was found that extensive twin boundaries are effective reducing the lattice thermal conductivity while maintaining a good electrical conductivity. Moreover, the Seebeck coefficient is enhanced due to “energy filtering” effect, by which the low-energy charge carriers are preferentially scattered, as previously discussed in Eq. 1-6. Figure 1-6 shows the HAADF-STEM image of the twin boundary in the sample and its ZT comparison with twin-free cast samples.

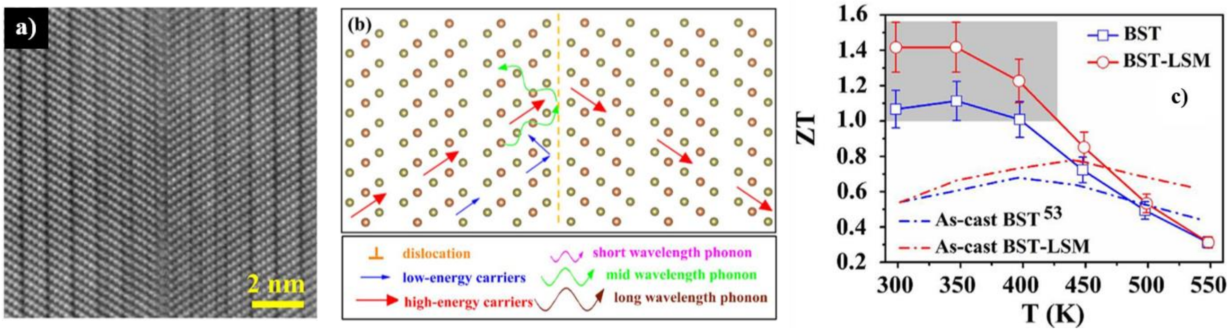

Figure 1-6: a) HAADF-STEM image of a typical twin boundary in $Bi_{0.5}Sb_{1.5}Te_3$ alloy; b) schematic highlighting the phonon blocking and carrier transmitting character of the twin boundary; c) ZT comparison among the twin-free as-cast samples and the samples with extensive twin boundaries. Reproduced from Ref. [16]

The other highlight of utilizing phase transformations for nanocomposite synthesis is that "self-assembled" lamellar/plate structures can be obtained in, for instance, eutectic or eutectoid decomposition. Such ordered structures are not readily obtained by mechanical allying/mixing and sintering, and less impurities and defects are associated with the "in situ" constructed interfaces. More importantly, in most of cases, the lamellar phase may possess specific orientation relationships with the matrix phase. Figure 1-7 shows the Sb_2Te_3 – PbTe pseudo-binary phase diagram, where lamellar growth of Sb_2Te_3 and PbTe can be achieved by eutectic decomposition

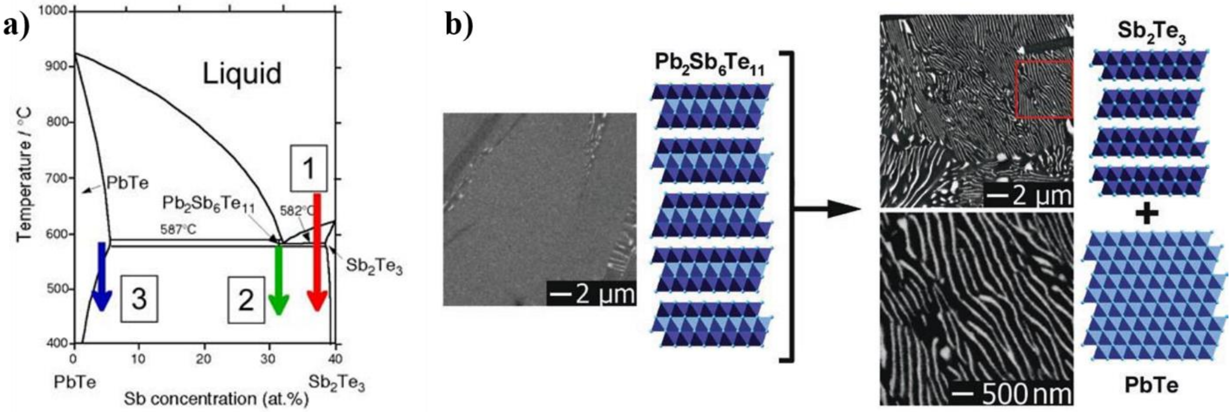

Figure 1-7: a) Sb_2Te_3 – PbTe pseudo-binary phase diagram; b) Back scattering electron images showing lamellar growth of Sb_2Te_3 and PbTe from metastable $Pb_2Sb_6Te_{11}$ by eutectic decomposition, with schematic illustrating the interface orientation relationship. Reproduced from Ref. [1]

from metastable $Pb_2Sb_6Te_{11}$ phase[1]. Orientation relationship is illustrated in Fig. 1-7 b) where low lattice mismatch between the PbTe (111) and Sb_2Te_3 (001) planes leads to coherent interfaces amongst the lamellae.

Rapid solidification can access small length scales in eutectics, again with preferred orientation relationships being possible. Our group produced Ge-rich lamella structures embedded in α-$FeSi_{2+\delta}$ by arc-melting (slow cooling), melt-spinning, as well as laser melting, shown consecutively in Fig. 1-8 a) b) and c). It can be noticed that by increasing solidification rate, the length scales of Ge-rich lamellae are reduced by orders of magnitude - the thickness of the lamellae, and their spacing, goes from sub-millimeter for arc-melting, to microns for melt-spinning, and to tens of nanometers for laser melting. For the melt-spun ribbon sample, it is determined by EBSD that the Ge-rich lamellae grow along the (001) habit plane of tetragonal α-$FeSi_{2+\delta}$[17]. Subsequently, the sample is annealed below Fe-Si eutectoid isotherm (~600 °C), giving rise to a microstructure with ~30nm DC Si laths embedded in β-$FeSi_2$ by eutectoid decomposition. The β-$FeSi_2$ – SiGe nanocomposite synthesis in this dissertation also exploits this eutectoid phase transformation, which will be discussed in chapter 3 & 4.

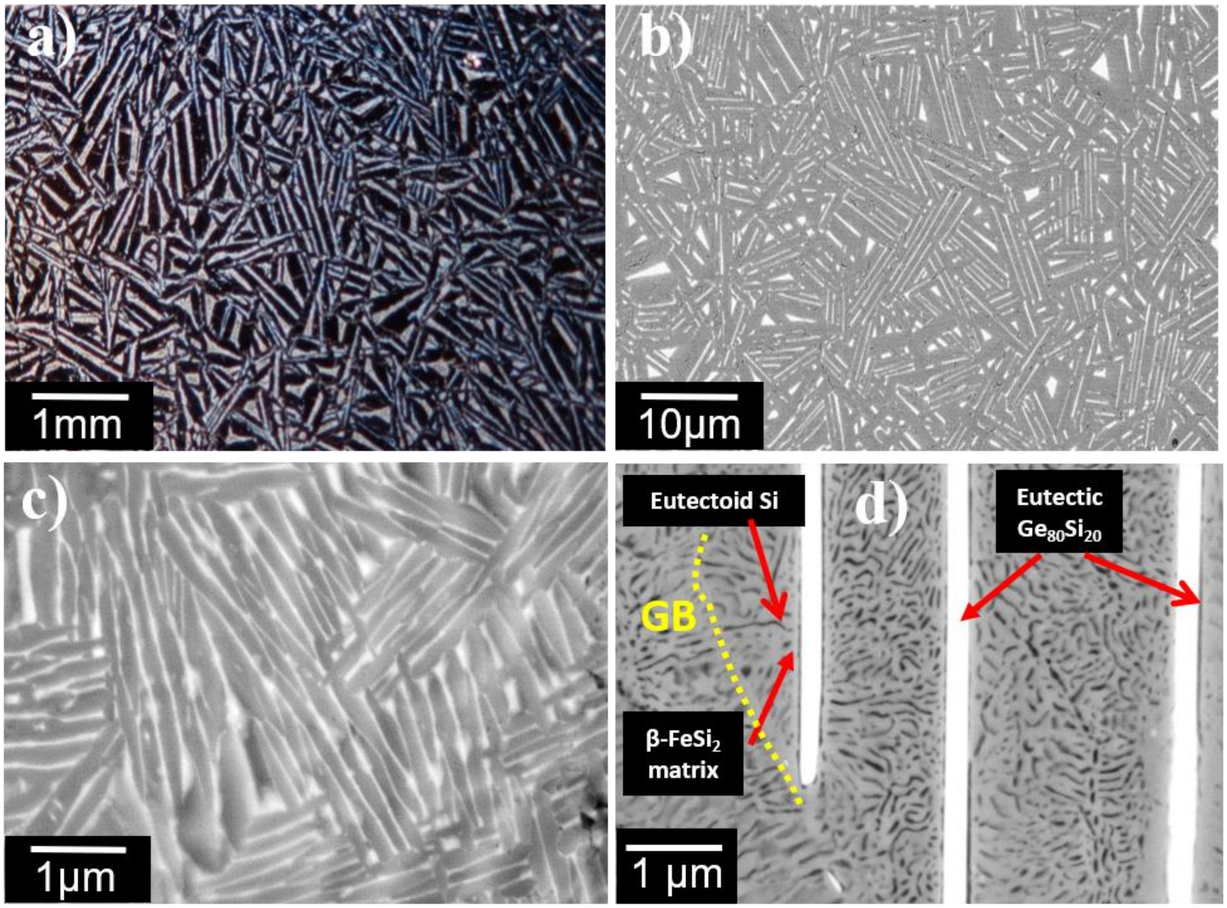

Figure 1-8: a) Optical micrograph of the coarse, slow cooling (arc-melting) eutectic microstructure; b) and c) backscattered electron image showing the rapid cooling (melt-spinning) and ultra-fast cooling (laser melting) eutectic microstructure. Reproduced from Ref. [17]

Besides avoiding excess atomic disruption on interfaces, the conduction (or valance) band edge of the matrix and precipitate phase should also match in energies (minimal band offset or energy barrier) to facilitate electron/hole transport, which is shown schematically in Figure 1-9. This concept has been experimentally demonstrated in the p-type PbTe – SrTe system, where SrTe nanocrystals are embedded in PbTe matrix[14], as well as in the $CdS_{1-x}Se_x$/$ZnS_{1-x}Se$ system[10], where the valence band edge of each phase can be tuned by the alloy composition. In both of the studies, hole mobilities were significantly enhanced due to valence band alignment, result in ZT enhancement. For n-type nanocomposite TE materials, conduction band alignment is scarcely discussed in literature. However, in principle, if the electron affinity, as well as the chemical potential (determined by doping level of each phases) of the two phases are close enough, conduction band alignment is expected to achieve facile electron transport across the heterointerface. Moreover, if the two phases are both degenerately doped, in which case the Fermi level lies within the energy bands, the energy barrier will essentially be zero regardless of the band offset. However, it is challenging to deliberately dope the nano-inclusion phase. Strategies to selective dope the constituent phases will discussed in β-$FeSi_2$ – SiGe synthesis in Chapter 4.

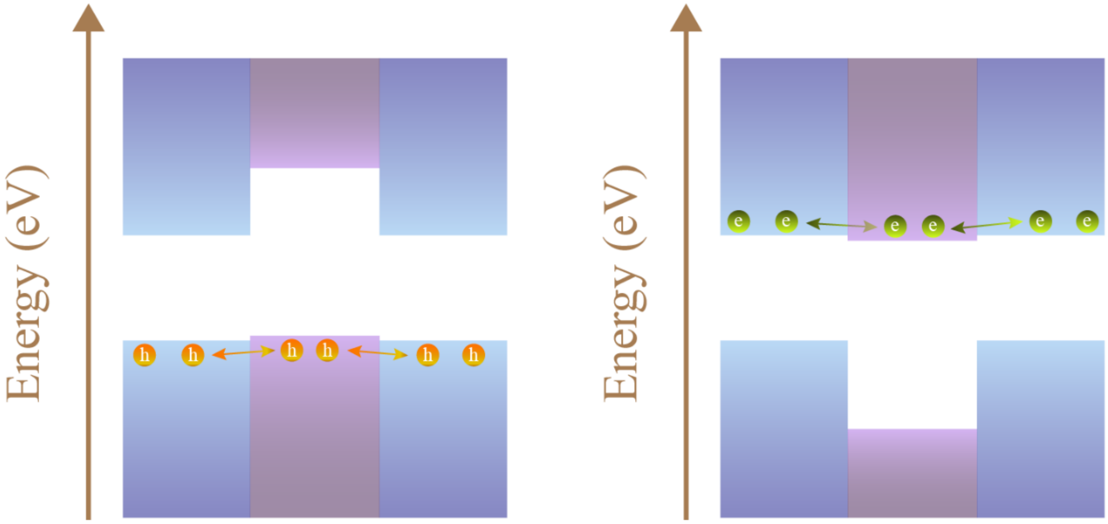

Figure 1-9: schematic for valence band alignment (left) and conduction band alignment (right), which facilitate holes and electrons transport respectively, hence the charge carrier mobility

Electronic structure modification has also been found to effectively improve the Seebeck coefficient. The energy-filtering approach, as introduced previously, is closely related to interface characteristics such as coherent nanoparticles or twin boundaries, which are expected to selectively block the low-energy electrons. In addition, due to the inverse relationship between mobility and effective mass, power factor can be improved only by increasing weighted mobility $(m^*)^{2/3}\mu$. Multiple degenerate valleys (multiple valence or conduction bands in vicinity to Fermi surface) have the effect of producing a large m* without explicitly reducing μ[18]. The Seebeck coefficient can thus be improved without deteriorating the electrical conductivity. In practice, this scheme can be realized by doping or alloying in some materials with high symmetry crystal structure, such as p-type Na doped PbTe(Se) system for valence band convergence[18], and n-type $Mg_2Si_{1-x}Sn_x$ solid solutions for conductioin band covergence[19].

As represented by Eq 1-6, the Seebeck coefficient can also be improved if the density of states (DOS) in vicinity to Fermi level can be enhanced. In practice this can be achieved by introducing impurity levels that provide additional DOS at the Fermi level, to achieve so-called “resonant states”[20]. For low dimensional systems, including thin film, nanowire and quantum dot materials, the density of states is quantized, which provides more possibilities to engineer and exploit the asymmetry of the DOS at Fermi level, to improve the Seebeck effect.

1.3.3. Novel doping schemes

Selective doping

As discussed, minimum energy barrier across the inclusion/matrix heterointerface favors facile charge carrier transport. And if the inclusion and matrix phases are both degenerately doped, the heterointerface will instead act like a metal-metal ohmic contact. Seemingly one can easily achieve such a scenario by mechanically mixing two heavily doped materials and sintering into a composite. In that case however, the excess defects at the interface will severely trap or scatter the charge carriers irrespective of the energy level alignment, resulting lower mobility than expected. Thus, it is more favorable to obtain a self-assembled nanocomposite, with degenerate or close to degenerate doping levels in both phases, using solid-state phase transformations. The challenges associated with this route is to selectively incorporate the impurity ions into constituent phases, especially into the nanoinclusions that are hardly accessible. This becomes even more challenging when the constituent phases have disparate chemistry, in which case different dopant elements are required for each phase. We anticipate selective doping can potentially be achieved by precisely controlling the thermodynamic and kinetic parameters of the doping elements incorporated to their respective parent phase, perhaps assisted by non-equilibrium processing, such current/field assisted sintering techniques (or SPS). Selective doping strategies for bulk thermoelectric materials are scarce within literature, and will be discussed in Chapter 4 for n-type β-$FeSi_2$ – SiGe nanocomposite, doped with Co and P(Sb) respectively.

Modulation/transfer doping

The modulation-doping concept has been applied in high mobility transistors, where a heavily doped wide gap material is in contact with an undoped narrow gap material, e.g. AlGaAs/GaAs. A confined 2D electron gas (2DEG) channel will be formed in vicinity to the heterointerface due to band inversion. Exceptionally high mobility can be obtained due to the fact that the 2DEG channel is spatially separated from the impurity ions so that scattering of electrons is greatly reduced. Similar strategy has also been applied in bulk thermoelectric materials. Zebarjadi, et al. pioneered this approach in nanograined SiGe composite, where the dopants are incorporated only into the minority silicon nanograins. These heavily doped grains are finely dispersed (on the order of a few tens of nanometers) and embedded in the undoped nanograined SiGe host. Due to the band alignment between the grains, the charge carriers spill over from the nanoparticles into the surrounding matrix, while the ionized dopant atoms remain spatially segregated within the nanoparticles. In the demonstrated case, they have observed a 40% enhancement in the power factor compared to uniformly alloyed nanocomposites, shown in Fig 1-10, due to the enhanced mobility. This 3D modulation doping strategy has also been widely investigated in other systems, and we expect the selective doping approach as discussed earlier could be promising in constructing a heavily doped nano-phase embedded in undoped matrix.

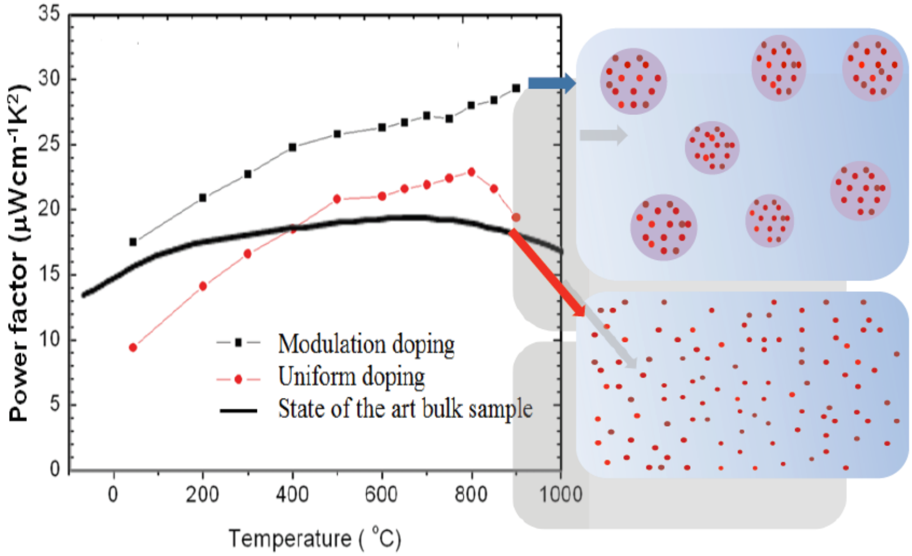

Figure 1-10: Schematic and power factor comparison of bulk SiGe with modulation and uniform doping

Despite the success in applying 3D modulation doping to bulk thermoelectric materials, 2D modulation doping has rarely studied in low-dimensional TE materials for device applications. The strategy has several advantages. Conventional techniques such as ion implantation ubiquitously require solid-state thermal diffusion for activation, which cannot be applied to materials that are heat sensitive. In addition, devices with ultrafine structures would also suffer from non-negligible statistical variation or deactivation of dopants[21]. More importantly, conventional doping approaches all involve incorporating aliovalent impurity ions, which create long range coulomb potentials that scatter conduction electrons and lowers their mobility. Modulation doping or transfer doping schemes, on the other hand, circumvents these issues, due to that fact that the doping mechanism is based on charge transfer or confinement according to band structure on the heterointerface. In this dissertation work, hybrid devices utilizing the organic/inorganic charge transfer is investigated for thermoelectric transport, which will be discussed in Chapter 5.

1.3.4. Percolation

Percolation approaches for thermoelectric nanocomposites has mostly been utilized in disordered organic semiconductors that exhibit hopping conduction[22–24]. In inorganic bulk systems, incorporation of a metallic phase has been studied to promote electrical transport by short-range percolation[25]. The volume fraction of the metallic phases has to be kept small, as a complete percolation of metallic phase would deleteriously enhance thermal transport and degrade the Seebeck coefficient. There are also other studies wherein coated powders were produced and subsequently consolidated into bulk, polycrystalline thermoelectric materials in which the grain boundaries consist of a second phase of nanometer-scale thickness, for instance $Pb_{0.75}Sn_{0.25}Te$ coated with $Pb_{0.75}Sn_{0.25}Se$[26] and $La_{0.067}Sr_{0.9}TiO_3$ with small amount of graphene decorating on the grain boundaries[27]. Only moderate improvement in ZT was observed due to reduction in lattice thermal conductivity by interface scattering. The reason for their limited impact on electrical properties, despite being highly conductive, is mainly due to the limited volume fraction, which is far below the percolation threshold despite the fact that it has favorable morphology as being coating on the grain boundaries.

In my dissertation work, I extend the percolation stratagem to an all-semiconducting system, where the inherently lower conductivities but much higher Seebeck coefficients, relative to metals, permits use of larger volume fractions of the second phase. To facilitate the percolation, liquid phase sintering is the key to the process. Liquid phase sintering involves sintering under conditions where solid grains coexist with a wetting liquid. This technique is more often used in ceramic community, as the “liquid” provides a capillary force that pulls the grains together. At the same time, the high temperature softens the solid, further assisting densification. Large diffusion rates are associated with liquids, giving fast sintering or lower sintering temperatures [28]. For thermoelectric materials processing, a low melting point phase can be introduced as the liquid phase, which is expected to wet the nano-grains of the matrix materials. Alternatively, one can just use a low melting temperature element to facilitate the liquid-phase sintering, and subsequently alloyed or incorporated in the percolated phase. Moreover, one can carefully design the sintering parameters to utilize the liquidus lines in the eutectic systems, in order to have one phase to form a liquid while sintering. Figure 1-11 shows an example of utilizing $Bi_{0.5}Sb_{1.5}Te_3$–Te pseudo-binary eutectic system to form Te coated $Bi_{0.5}Sb_{1.5}Te_3$ platelets for subsequent consolidation [29]. Although this study is focused on the impact of the dislocations generated on the grain boundaries

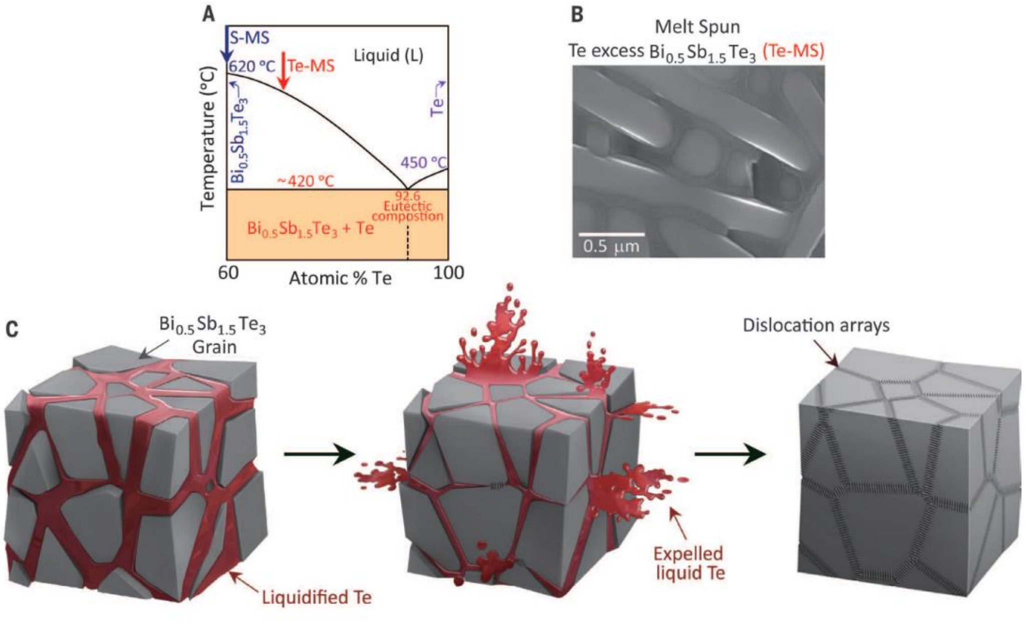

Fig. 1-11: (A) Phase diagram of $Bi_{0.5}Sb_{1.5}Te_3$–Te system showing a eutectic composition at 92.6 at % Te; (B) The SEM image of melt-spun ribbon with $Bi_{0.5}Sb_{1.5}Te_3$ platelets coated by Te; (C) Schematic illustration showing the generation of dislocation arrays during the liquid-phase compaction process [29].

due to expelled liquid Te during sintering, it still provides the feasibility of achieving a percolated composite by liquid phase sintering via eutectic decomposition.

The goal of the percolation approach in this study is to form a composite with a matrix phase exhibiting high Seebeck coefficient, and a secondary phase possessing high carrier mobility and hierarchical length scales. While smaller length scale nanoparticles would contribute to the phonon scattering, the simultaneous presence of larger lengthscales could permit phase percolation that retain good electrical conductivity. The schematic is shown in Fig 1-12. The percolation approach will be especially useful when the constituent phases have drastically different crystal and electronic structures, in which case the aforementioned approaches such as constructing coherent interfaces and band alignment are impossible to implement.

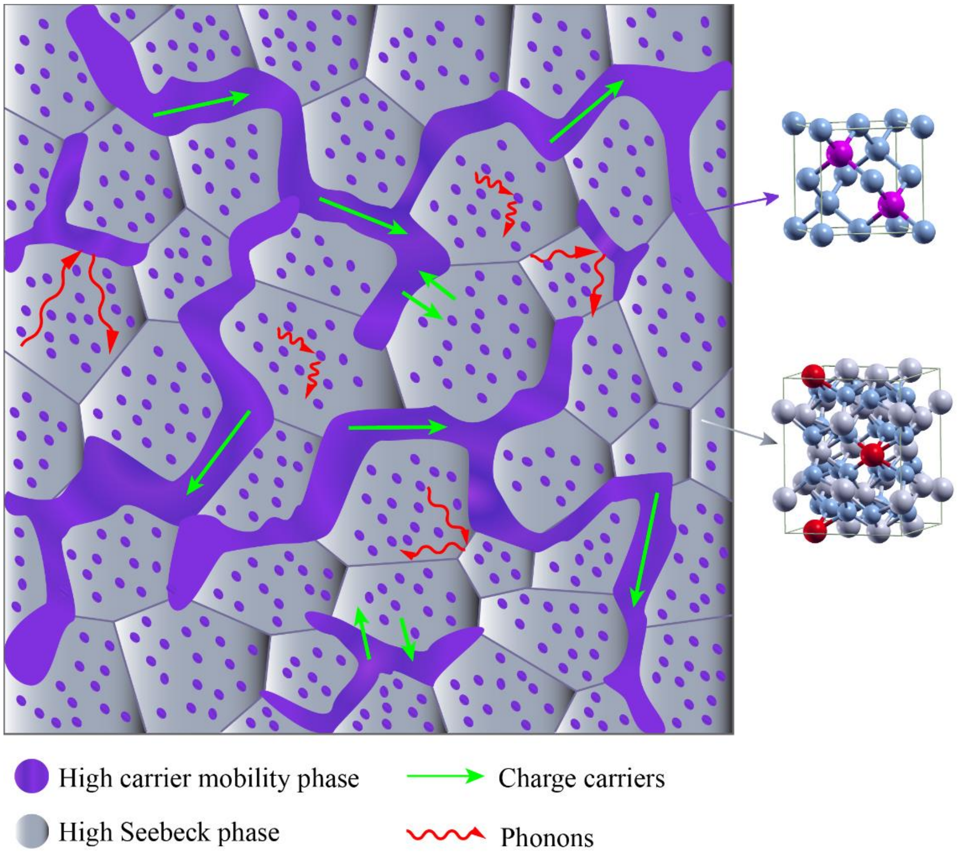

Figure 1-12: Schematic of nanocomposite microstructure with high Seebeck phase as matrix embedded with hierarchical, percolated high mobility phase

1.4. Dissertation outline

The dissertation consists of 7 chapters, with research focused on Si-based thermoelectric materials in both bulk and thin film forms. The objectives are two-fold: the first goal is to develop an n-type bulk β-$FeSi_2$ – SiGe nanocomposite for ZT optimization, and the second is to fabricate a hybrid Si device studying the effect of charge transfer in thermoelectric transport.

The **first chapter**, as already presented, describes the fundamentals of thermoelectrics and the mathematical expressions of the major parameters, followed by the rationales and strategies to improve the TE performance by the manipulation on the microstructure and electronic structure, closely related to the material of interest in this dissertation. The **second chapter** introduces the experimental and characterization methods involved in the studied systems. The **third chapter** discusses the mechanism and phase evolution of the React/Transform spark plasma sintering approach in microstructure optimization of β-$FeSi_2$ – SiGe nanocomposite, and evaluates the thermal conductivity by Ge incorporation both experimentally and analytically. The **fourth chapter** extends the findings in the third chapter and investigates various methodologies for ZT optimization by hierarchical structuring, phase percolation and selective doping. The **fifth chapter** studies the thermoelectric transport of the nanopatterned holey Si thin film on SiO_2 substrate (SOI). The holey Si device is heavily doped by boron ion implantation (p-type). The **sixth chapter** introduces the fabrication of F_4TCNQ/Si hybrid devices, validates the charge transfer mechanism, and investigates its effect on thermoelectric transport. The **seventh chapter** summarizes the key outcomes of my research work as well as give a prospective view for future study.

Chapter 2: Experimental and Characterization Methods

2.1. Synthesis and fabrication

2.1.1. Powder processing for β-$FeSi_2$ – SiGe nanocomposite

The process flow for β-$FeSi_2$ – SiGe nanocomposites can be crudely summarized as follows: Fe(Co)-Si cast by arc-melting → adding Ge and dopants/additives for a light ball milling → spark plasma sintering. Detailed process specifications and phase evolutions will be discussed in Chapter 3. A brief introduction of the major facilities involved in the process is provided as below.

Arc-melting

The Fe-Si as-cast ingots (Co is added as dopant) is obtained by arc-melting the elemental Fe and Si chunks (and Co wire) with certain compositions using the home-built arc-melter facility at UVa (*courtesy of Prof. Shiflet*), shown in Fig.2-1. It consists of a water-cooled stainless-steel bell jar hinged to a fixed baseplate. The electrode stinger is sealed at the top of the bell jar by means of a ball joint and a stainless steel bellow (separated from the main chamber), so that it can be easily operated under a certain pressure. The hearth is thick, water-cooled copper panel. Multiple cavities are on the hearth top surface to hold separate charges for melting. A roughing pump is attached to the chamber, which gives a base pressure of ~10^{-2} torr for the subsequent Ar back-filling. The power input for the arc can be adjusted, giving a temperature up to 3000 °C for melting. The pre-cleaning and initial evacuation of the chamber is critical, not only to avoid contamination, but also to minimize slag formation during the melting. The slag would wrap round the cast, and makes it very hard for the arc to penetrate through the oxidation layer after flipped. Since a pristine Si chunk is a poor electrical conductor, directly striking the arc onto the Si will deflect most of the arc onto the edge of the copper cavity, so it cannot be melted. Therefore, in practice, Fe chucks are put in front, which is melted first and subsequently incorporates Si to form a liquid drop. All charges are melted, flipped over, and re-melted to improve chemical homogeneity.

Spark plasma sintering

Sintering is the process of firing and consolidation of powders below the melting temperature, where diffusional mass transport leads to the formation of a dense body[30]. For conventional pressureless sintering, the sintering mechanism can be briefly summarized as: the surface diffusion (first stage) at elevated temperature results in particle coalescence with a narrow neck bridging them, where subsequently grain boundary diffusion (intermediate stage) takes in filling up the

Figure 2-1: Arc-melter facility at UVa

enclosed pores, along with lattice diffusion (final stage) leading to final densification. Spark plasma sintering (SPS) is a sintering technique utilizing uniaxial force and a pulsed (on-off) direct electrical current (DC) under low atmospheric pressure to perform rapid consolidation of the powder. The configuration of SPS is shown in Figure 2-2. The powder is filled in a graphite die secured with two graphite punches, which are also used as electrodes for conducting the current. The in-situ pressure (10~60 MPa for graphite punch) is provided by a hydraulic system. The graphite die has a pinhole reaching close to the inner sidewall, so temperature of the sample (for feedback control) can be monitored by either a thermocouple (suitable for low temperature), or using a pyrometer (suitable for high temperature). In spark plasma sintering, due to the in-situ pressure and applied current, the first stage surface diffusion can be circumvented, and the local joule heating mechanism also enhances the grain boundary and lattice diffusion, so as to accelerate the consolidation process[31–34]. In this dissertation, A React/Transform SPS approach is developed for β-$FeSi_2$ – SiGe nanocomposite synthesis, *courtesy of Prof. Poon and Prof. Wadley's SPS apparatuses at UVa.*

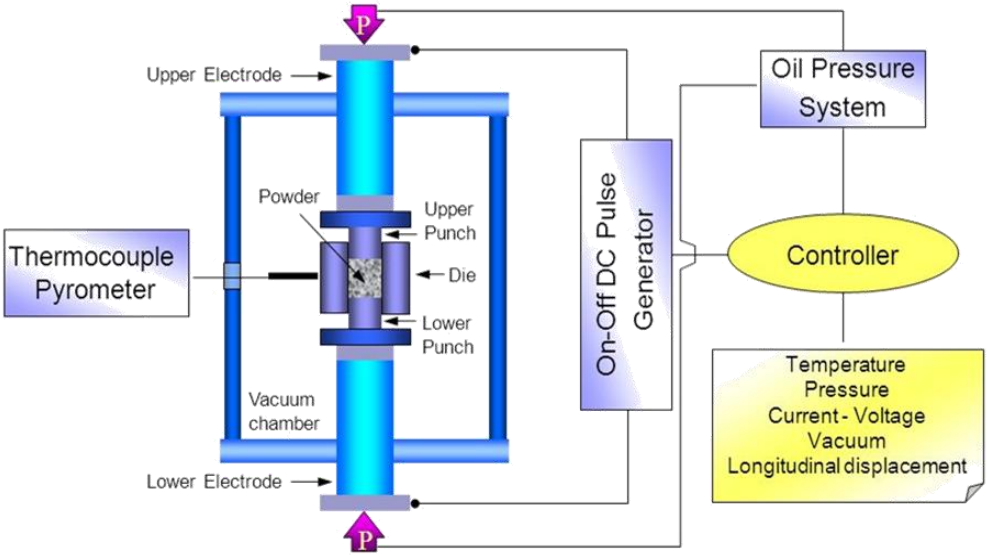

Figure 2-2: Schematic spark plasma sintering system configuration

2.1.2. Fabrication of holey Si and F4TCNQ-Si hybrid device

The holey Si fabrication involves patterning a periodic dot array by electron beam lithography (EBL), followed by reactive ion etching (RIE) to transfer the pattern onto the Si film (the film is a silicon-on-insulator, or SOI, structure) generating hole arrays. Ion implantation is used to yield a certain doping level. Contacts are deposited by electron-beam evaporation, followed by rapid thermal annealing to facilitate ohmic contact formation. For the F_4TCNQ-Si hybrid device, a home-made thermal evaporator is used for F_4TCNQ deposition. Detailed process flows for the two devices will be described in Chapter 5. In this section, a brief introduction of the major fabrication techniques will be provided.

Electron beam lithography (EBL)

EBL can create masks or templates by directly writing with a focused electron beam, which can generate structures finer than typical photolithography. EBL patterning involves three major steps: exposure, development, and pattern transfer. During exposure a highly focused electron beam is writing on the resist material (e.g. PMMA: polymethyl methacrylate) that is spin-coated the

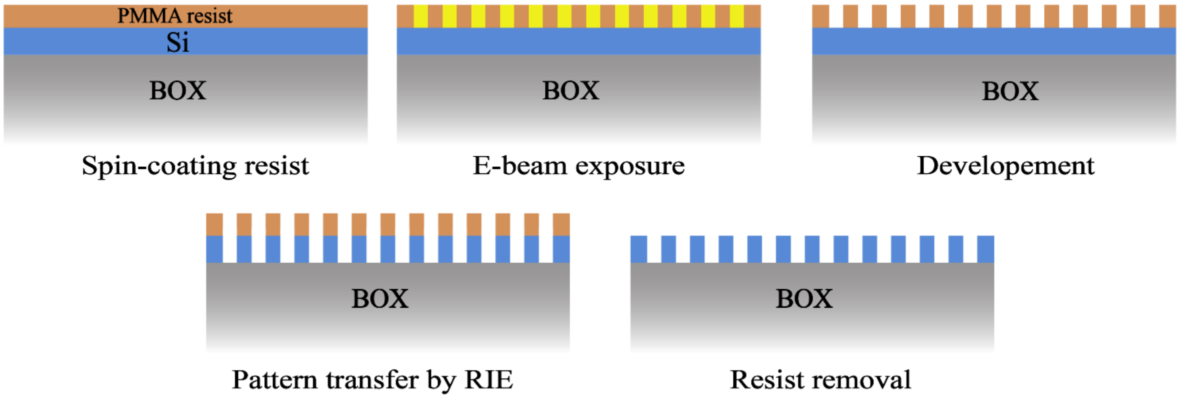

Figure 2-3: Process flow for "holey Si" fabrication involving EBL patterning and reactive ion etching

substrate, according to a pre-designed pattern. In the development step, the e-beam treated areas of the resist material are stripped off by the developer solvent (e,g. MIBK: methyl isobutyl ketone). The pattern can then be transferred to the substrate by reactive ion etching (RIE). A schematic diagram of the patterning process is shown in Figure 2-3.

E-beam evaporation

The majority of device fabrication prior to rapid thermal annealing (RTP) was conducted by our collaborator at UCSB. Nevertheless, the contacts/microheater deposition for certain samples and the subsequent RTP process needed to be done in the cleanroom at UVa. The contact/microheater are deposited with 1 μm Al with 50 nm Au as the capping layer, using CHA six crucible E-beam Evaporator.

E-beam evaporation is one type of physical vapor deposition (PVD) technique in which an electron beam is generated from a filament by thermionic emission and steered via electric and magnetic fields to impinge on the target material (in this case: pellets of Au or Al) and thermally vaporize it under high vacuum. The energy of the vapor atoms for e-beam deposition is very low (~0.1 eV), and the chamber pressure should be below the point where the mean free path is longer than the throw distance. Therefore, the base pressure of the chamber is pumped to less than 10^{-5} torr prior deposition. This can also be important for film cleanliness. A crystal microbalance is placed the chamber to monitor the thickness of the deposited metal film in-situ. The substrate holder is rotating to minimize film thickness inhomogeneity.

Rapid thermal annealing

Since the Si film device for charge transfer study (transfer doping) is only mildly doped (~ 10^{16} cm^{-3}), a certain degree of interdiffusion between the Al contact and Si can help to form an ohmic contact for transport measurements. Therefore, Rapid Thermal Annealing is used for contact interfacial diffusion. In principle, the operation involves rapid heating of the device surface using a IR-lamp from ambient to 500°C within 30 seconds, As soon as the chip reaches this temperature, it is held there for some seconds and then quenched to room temperature. The temperature of the wafer is determined by a thermocouple touching against the sample holder (Si wafer). Pyrometers can be used to monitor higher temperatures. With this rapid thermal treatment, ohmic contacts can potentially be formed without breaking down the device.

Thermal evaporation

For charge transfer studies in the hybrid device, the Si surface needs to be free of native oxide (can be removed using a standard buffered oxide etch). And the organics should be selectively deposited on the Si surface of the device with full coverage, meaning good wetting is favored. Therefore, a home-made miniature thermal evaporator was built for the organic film deposition. Figure 2-4 shows the configuration. In a typical thermal evaporator, a crucible made of refractory metal is heated up by an external power supply, and the temperature can be precisely adjusted using a feedback control. Since the primary goal of this study is to form an organic (F_4TCNQ) film with full coverage on the Si device to ensure the maximum charge transfer, the film surface morphology and thickness are less important. Therefore, the organic source of my thermal evaporator is simply a quartz tube sealed onto a six-way vacuum cross. The organic crystal powders are put in the quartz tube, which is heated by oil bath immersion on a hot plate. A thermocouple is attached to the quartz tube side-wall in the oil bath to monitor the temperature. A glass slide (with a magnet) is placed in the left chamber arm as the shutter, which can be manually moved by another magnet outside the chamber arm. A manual valve is connected to the deposition chamber, and an Edwards T-Station 85 pump (equipped with a roughing pump and a miniature turbo pump) is connected to the manual valve with a stainless-steel bellow, which provides a base pressure of less than 10^{-6} torr.

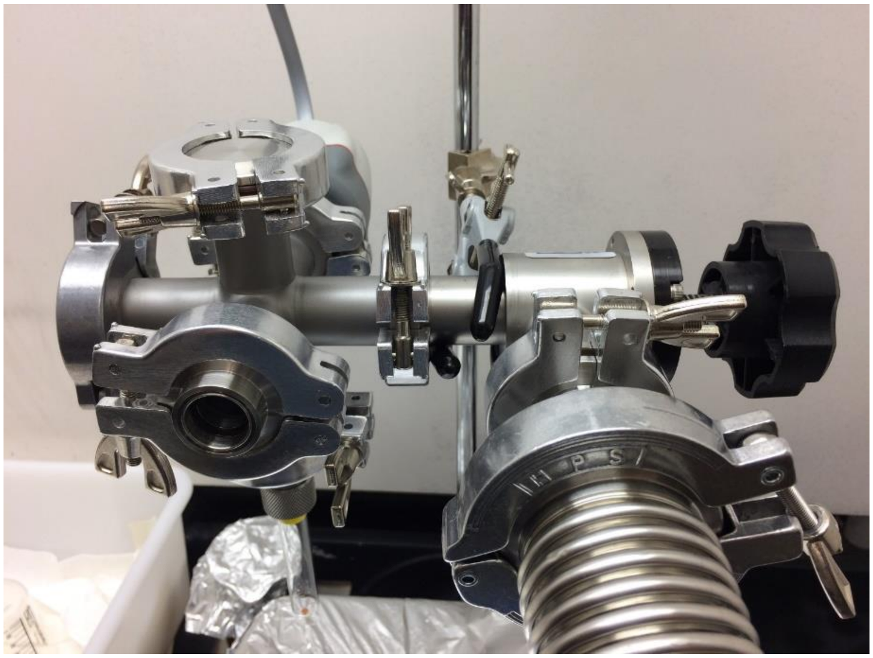

Figure 2- 4: Chamber configuration of the home-made miniature low-temp thermal evaporator for organics deposition

2.2. Materials characterization methods

X-Ray diffraction (XRD) and Rietveld refinement

Powder XRD is used in this study for phase indexing and lattice parameter determination. Crystals with periodic lattice planes scattered monochromatic x-rays that can be in-phase on adjacent planes. This constructive interference gives a characteristic pattern of diffraction peaks, which in turn can be used to index the phase. Lattice spacings can be derived using the Bragg's law:

$$n\lambda=2d\sin\theta \tag{2-1}$$

where n is an integer called the order of reflection, λ is the wavelength of x-rays, d is the characteristic spacing between the crystal planes of a given specimen and θ is the angle between the incident beam and the normal to the reflecting lattice plane.

For powders or polycrystalline bulk samples having randomly oriented crystallites, all possible diffraction peaks can be detected to form a XRD pattern, by varying the 2θ angle along a fixed scattering direction. XRD data is obtained from the PANalytical Empyrean powder diffractometer at UVa for phase identification and Rietveld refinement. For the latter purpose, high-resolution data is obtained by scanning from 15 – 60° 2θ for 2 h to ensure a high signal to noise ratio. Rietveld refinement is strong technique for quantitative analysis of the X-ray diffraction patterns, which is implemented in this study for phase volume fraction and composition determination of the composite material. The working mechanism can be briefly described as follows: based on the theoretical crystal parameters of the targeted material and relevant instrumental parameters, a calculated pattern with precise peak intensity can be obtained. In Rietveld refinement, a least square approach is used to fit the measured high-resolution XRD pattern, by refining the parameters of the aforementioned calculated pattern. These refined parameters contain information for instance phase volume fractions (which affect the peak intensity) and chemical compositions or lattice constants (which affect the peak 2θ angle).

Scanning electron microscopy (SEM)/ Energy-dispersive X-ray spectroscopy (EDS)

SEM uses a focused electron beam rastering on the sample surface to generate a variety of signals, which can then be captured by different detectors above the sample. The two modes have been constantly used in this work are secondary electron imaging and backscattered electron imaging, which reveal the surface topography and chemical composition information of the sample, respectively. The energy of the electron beam can be tuned by adjusting the accelerating voltage (1~30 kV), which determines the electron-sample interaction volume, and the energy range of the X-rays that can be generated for EDS analysis.

EDS is an analytical technique used for the semi-quantitative elemental composition identification. It compiles the characteristic x-rays of different elements into an energy spectrum. For example, most of the EDS peaks are X-rays given off as electrons return to the K shell, giving the K-alpha and K-beta peaks. In general, compositional analysis for elements with large atomic number is more quantitatively accurate, as these elements possess more energy shells, so that the spectrum can be uniquely distinguished (which also requires large accelerating energy of the electron beam). On the contrary, elements with small atomic number have less characteristic X-ray excitation and their spectra suffer from overlapping peaks in the low energy range of the EDS spectrum. Data in this work is obtained from the FEI Quanta 650 SEM equipped with an Oxford EDS system at UVa. Figure 2-5 illustrates the electron beam interaction within the material using SEM. Different sources of signal can be detected for various purposes as discussed above.

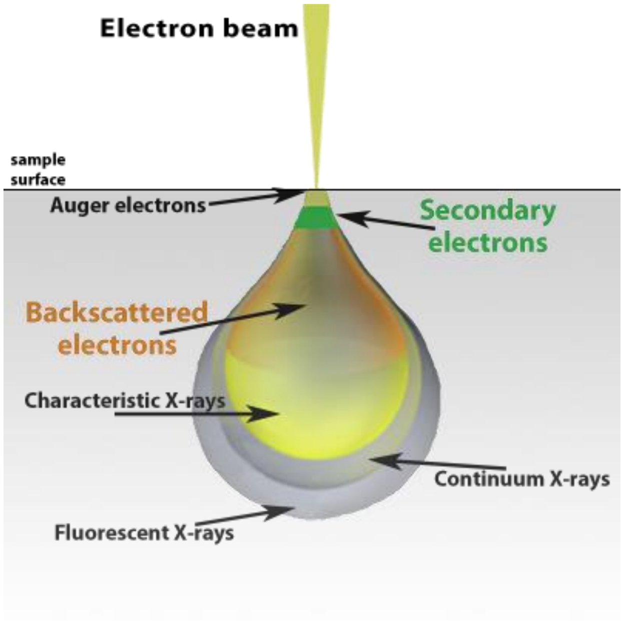

Figure 2-5: Schematic of electron beam interaction within the material, and different sources of signal that can be detected by SEM/EDS

Focused Ion Beam (FIB)

While the SEM uses a focused electron beam to image the sample in the vacuum chamber, a FIB system uses a focused ion beam that can sputter mill select regions. The FEI Helios dual-beam FIB system at UVa is equipped with a high-resolution SEM as well as a Ga+ ion source for both imaging and machining purposes in nanometers' scale. This dual-beam FIB system is used in this study for various purposes. Sample lift-out process is conducted using this system to prepare site specific or cross-section TEM samples. The brief procedure process for the XTEM sample of F_4TCNQ/Si hybrid device is shown in Fig. 2-6. First, the area of interest (on the surface of the film device) is found using SEM mode. Then a certain thickness of C and Pt is deposited using FIB mode (Fig. 2-6 a)). This acts as a protection layer for subsequent Ga^+ ion etching, which is performed around the area of interest making trenches to suspend the lift-out sample (Fig. 2-6 b)). A Pt needle is then welded on the Pt capping layer and transfer the sample onto a Cu grid (Fig. 2-6 c)). Finally, ion polishing is performed on both sides of the lift-out sample for multiple iterations

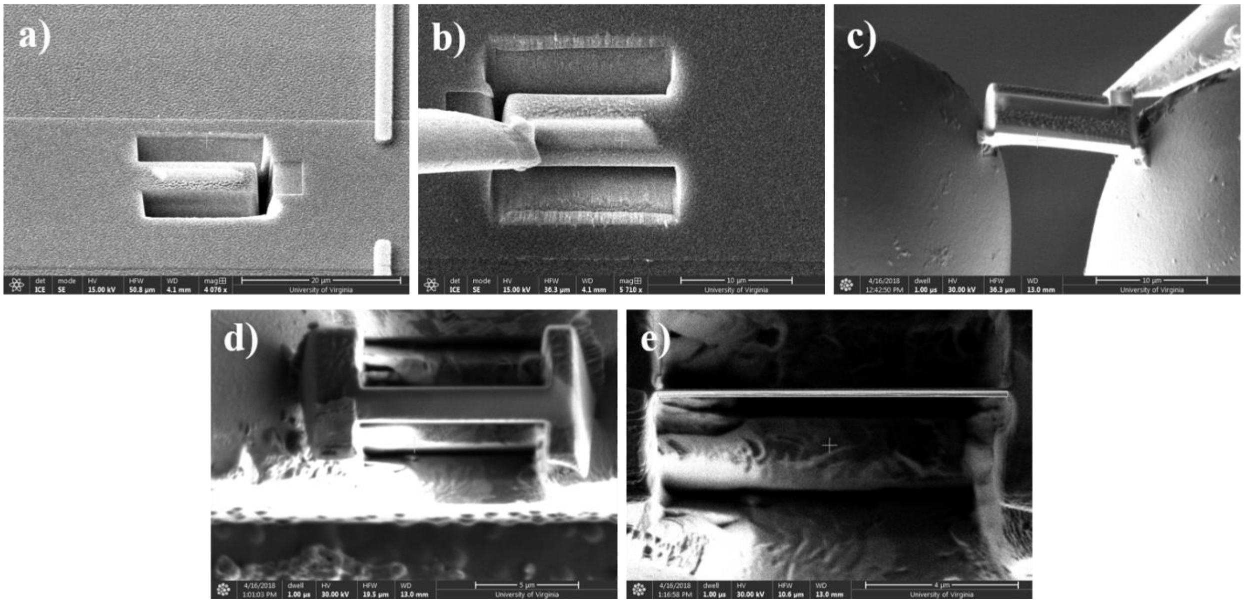

Figure 2-6: Brief process flow of FIB lift-out for a XTEM sample

to ensure the electron transparency for the subsequent TEM analysis (Fig. 2-6 d) and e))

Dual-beam FIB is also used for 3D reconstruction of the nanocomposite to evaluate the phase percolation in β-$FeSi_2$ – SiGe. The process involves serial sectioning in the area of interest by the Ga^+ ion beam, SEM images are then taken every 50 nm in etched thickness. The obtained SEM images can then be used to reconstruct the 3D tomography using Avizo software. Details and results will be described in Chapter 4.

The other application of dual-beam FIB in this study is to edit/repair the metal lines on the device, simply by sputtering off the metal in the unwanted area followed by locally depositing Pt. This can be greatly helpful to restore a microheater that is burnt (usually a slight failure point) during transport measurement, avoiding the time-consuming device fabrication.

Transmission Electron Microscopy (TEM)

Transmission electron microscopy (TEM) was performed on the FEI Titan 80-300 operated at 300 kV. In TEM, a high-energy electron beam is transmitted through a thin specimen (<100 nm), and the transmitted electrons can then provide insight into structural and compositional configuration of the material. A diagram of a TEM in both diffraction and imaging mode is shown in Figure 2-7. TEM is capable of imaging at significantly higher resolution than other microscopy techniques, where even single atomic columns can be resolved along certain zone axes. This is also known as high-resolution transmission electron microscopy (HRTEM). TEM can also be used in Z-contrast imaging mode, using the scanning transmission electron microscopy (STEM) technique. Similar to SEM, it uses a finely focused electron beam rastering on the sample. Interactions between the beam electrons and sample atoms generate a serial signal stream, which is correlated with beam position to build a virtual image in which the signal level at any location in the sample is represented by the gray level at the corresponding location in the image. In this mode, the scattered electrons are collected in an annular detector. EDS can thus be applied under STEM mode for quantitative elemental analysis in local areas. Another elemental analysis technique equipped in the FEI Titan 80-300 TEM at UVa is the electron energy loss spectroscopy (EELS) system. When a material is exposed to a beam of electrons with a known, narrow range of kinetic energies, some of the electrons will undergo inelastic scattering, and the amount of energy loss can be measured via an electron spectrometer. This data can be interpreted in terms of what caused the energy loss. Elemental imaging can thereby be obtained using EELS at a much faster rate, as well as in a less-destructive manner compared with EDS. As previously explained, EDS works better for large atomic mass elements. EELS, on the contrary, is more suitable for low atomic elements, as their electron energy levels are more well-defined, so that the energy loss information can be easily extracted. In this dissertation, bright field TEM, HRTEM, SAD, STEM, EDS elemental mapping and EELS elemental imaging techniques have been used to investigate various structural and compositional information in both material systems.

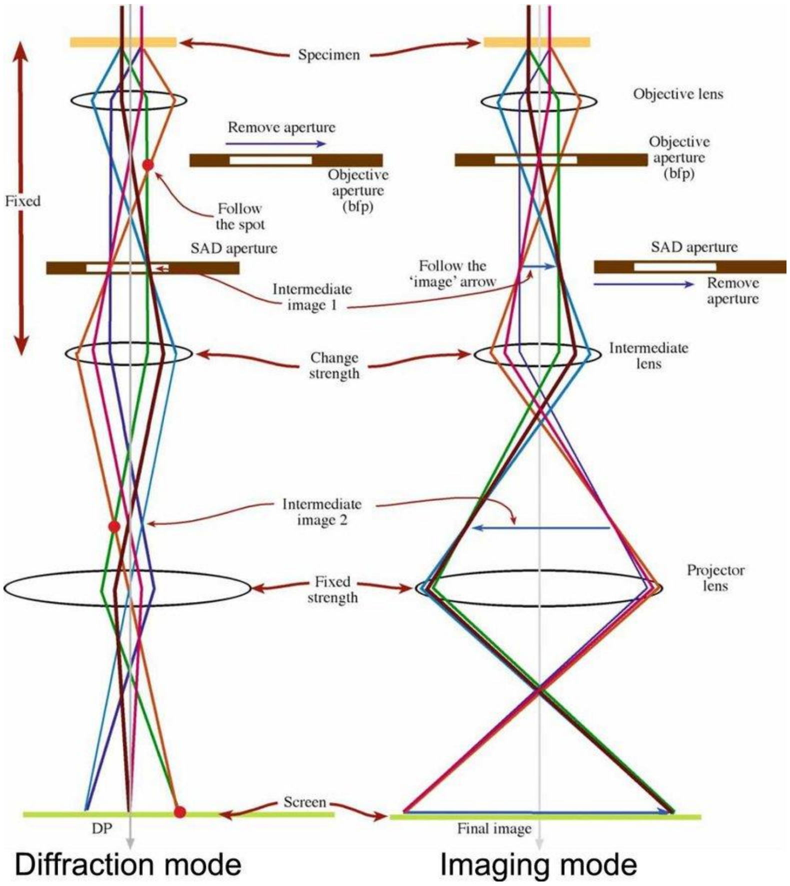

Figure 2-7: The imaging system of a TEM in diffraction and in imaging mode (Williams and Carter, 2009)

Atomic Force Microscopy (AFM)

AFM is a surface analysis technique that can harvest the topographical information of a sample surface. In this study, the surface morphology of the holey Si and F_4TCNQ/Si hybrid devices are characterized by our NT-MDT AFM with Solver Pro software, using NSG01/NSG10 tips with a typical tip curvature radius of 6 nm. Tapping mode (semi-contact mode), which utilizes the inter-atomic attractive force region, is used for all sample measurements. While operating, the cantilever is oscillated at a resonating frequency and the amplitude changes when encountering topographic features on the sample surface. The cantilever position will then change by the piezoelectric scanner according to the feedback loop, in order to maintain the tip-oscillation amplitude. The topographical information, manifested by laser deflection from the cantilever, is then captured by the photodiode, which has 4 segments, as schematically shown in Fig 2-8. In this way, the tip can raster across the area of interest on a sample and the z-height is recorded to form a topographic z(x,y) map.

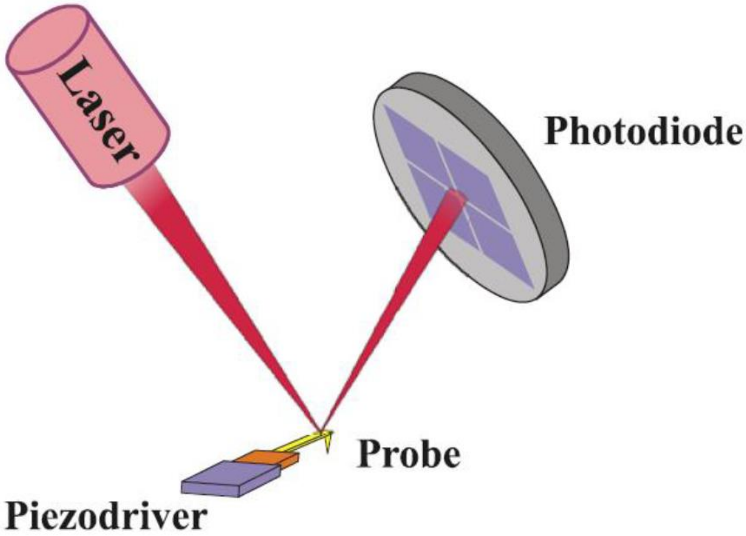

Figure 2-8: Layout of an atomic force microscopy (NTMDT solver pro AFM manual)

2.3. Transport Measurements

Seebeck Coefficient/Electric Resistance Measurement System (ZEM-3)

The Seebeck coefficient and electrical conductivity of the bulk materials in this study are measured by the ZEM-3 system (*courtesy of Prof. Poon*), as schematically shown in Figure 2-9. A SPSed disc is cut into a rectangular prism, and is then vertically set in between the upper and lower blocks in the heating furnace. One of the blocks can be heated by an embedded heater to provide a temperature gradient cross the sample. The Seebeck coefficient is measured by measuring the upper and lower temperatures T_1 and T_2 with the thermocouples pressed against the side of the sample, followed by measurement of thermal electromotive force *dE* between the same wires on one side of the thermocouple. Electric resistance is measured by the DC four-point probe method, when there is no temperature differential cross the sample. A constant current is applied to the two ends of the sample and a voltage between the same wires of the thermocouple can be determined.

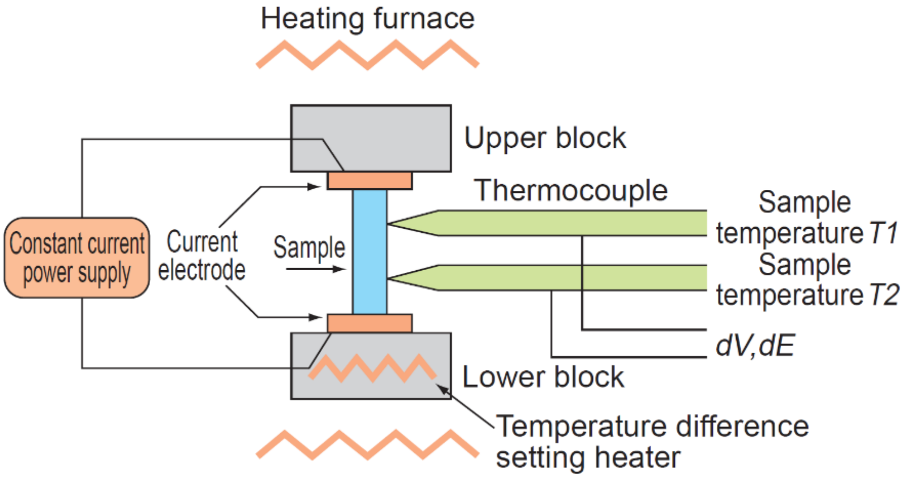

Figure 2-9: Layout of ZEM-3 system

Laser flash thermal diffusivity system

The thermal diffusivities of the bulk samples in this dissertation were measured by a Netzsch LFA 467 Laser Flash instrument. The temperature dependence of specific heat of the composite material is measured by Differential Scanning Calorimetry (DSC). The thermal conductivities are then obtained by the product of the specific heat, thermal diffusivity and density, i.e. $\kappa = C_p \alpha \rho$. In carrying out a thermal diffusivity measurement, the lower surface of a plane parallel sample is first heated by a short energy pulse from a flash lamp. The resulting temperature change on the upper surface of the sample is then measured with an infrared detector, as shown in Fig. 2-10. Thermal diffusivity is then extrapolated from the curve of the IR signal from the upper surface versus time.

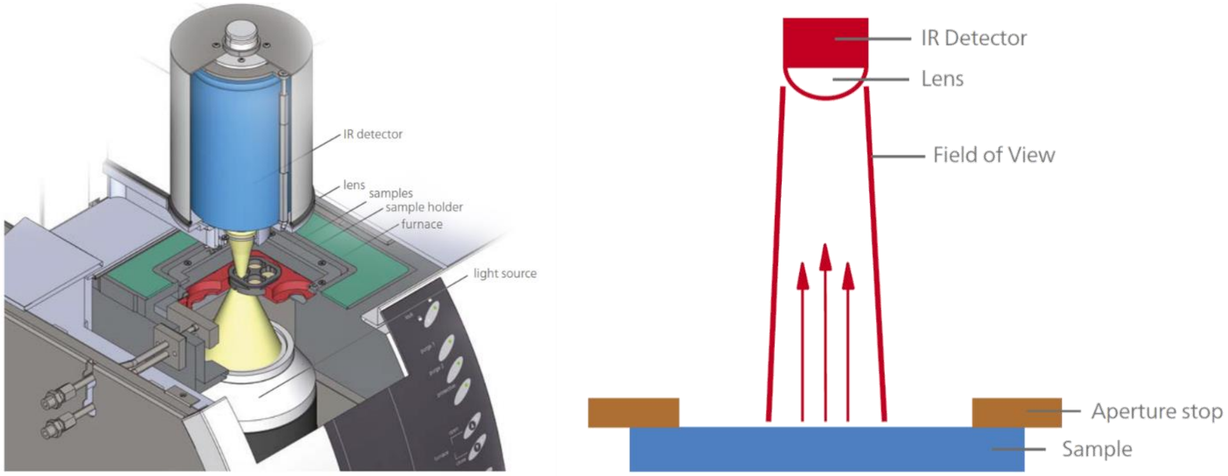

Figure 2-10: The left shows the configuration of the LFA laser flash system, and the right shows its optics configuration (Netzsch LFA 467 manual)

Hall measurements

Hall measurements were performed using a Quantum Design VersaLab to obtain carrier concentration and mobility for the n-type doped β-$FeSi_2$ – SiGe nanocomposite material. The principle of Hall measurements is that when the dominant carriers moves along a direction perpendicular to an applied magnetic field, they experience a magnetic Lorentz force, $-q \cdot \boldsymbol{v} \times \boldsymbol{B}$**,** acting normal to both **v** and **B**. The carriers then accumulate on one side (transverse) of the sample, resulting in an internal electric field being built up, referred to as Hall voltage V_H, which can be expressed by:

$$V_H = \frac{IB}{nqd} \qquad 2\text{-}2$$

where I is the applied current, $\boldsymbol{B}$ is the magnetic field, q is the elementary charge, d is the thickness of the measured sample, and n is carrier concentration to be determined, which can be calculated by measuring V_H, knowing the values for I, $\boldsymbol{B}$ and d. In order to determine mobility, a resistivity measurement is also needed, which follows the equation:

$$\mu = \frac{1}{nqR_s} \qquad 2\text{-}3$$

where n is the carrier concentration calculated from the Hall measurement, and R_s is the sheet resistivity ($\rho = R_s \cdot d$). To measure the sheet resistance, Van der Pauw geometry is used in this study for bulk materials, even though it is usually more suitable for thin film with a small thickness. This is because the samples are heavily doped, meaning a large n value. By decreasing the thickness d, the measured V_H/I slope vs magnetic field B can be more accurately be determined as a result of a higher signal to noise ratio. Therefore, the samples for Hall measurements were cut into $3\times3mm^2$ square, and polished down to 200μm, as shown in Fig.2-11. R_s is then calculated by:

$$R_s = \left(\frac{\pi}{ln2}\right)\left(\frac{R_A + R_B}{2}\right) \qquad 2\text{-}4$$

where $R_A = \frac{V_{A,C}}{V_{B,D}}$, and $R_B = \frac{V_{B,A}}{V_{D,C}}$, as annotated in Fig. 2-11. Since it is a square, and the sample is isotropic, it can be assumed that $R_A = R_B$.

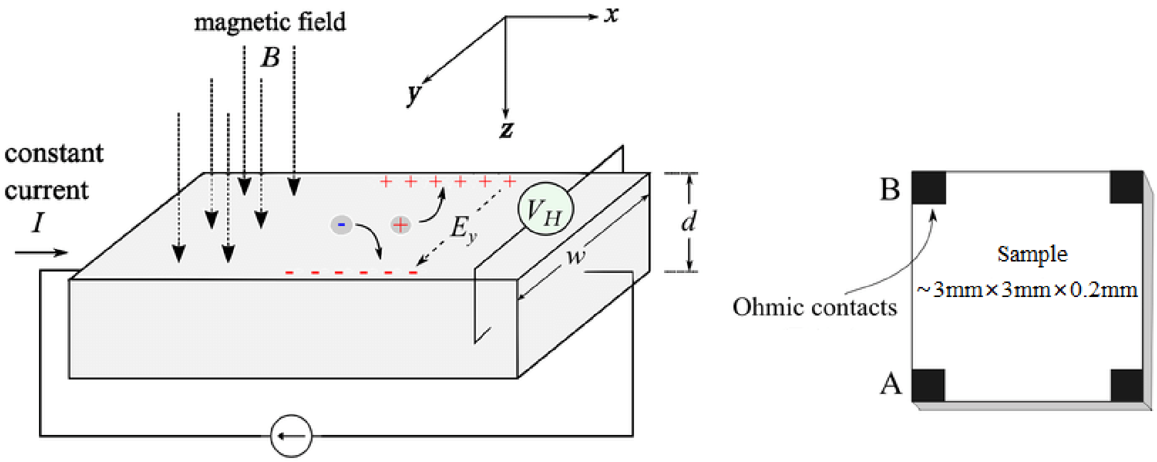

Figure 2- 11: The left shows the schematic of Hall effect mechanism, and the right shows the sample configuration by Van der Pauw method)

Electrical Transport Measurements for Thin Film Materials

The electrical transport measurements for holey Si and the hybrid F_4TCNQ/Si device were conducted in a self-designed cryostat chamber with a temperature range from 50K – 800K, as shown in Fig. 2-12. The vacuum level can reach to 10^{-6} torr using a mini turbo pump. The sample holder, attached to a Cu rod, is cooled to cryogenic temperature by helium compressor. A feedback-controlled temperature system is equipped to heat up the sample holder and monitor the sample temperature. Twelve electrical feedthroughs are embedded, which can connect to the pins on a sample package for various transport measurements. Two lock-in amplifiers are used to measure small resistances by 4-point probe method. Keithley 2000, 2001, and nanovolt meter are also equipped for Seebeck coefficient measurement. The detailed measurement procedures associated with the contact configurations on the device will be discussed in Chapter 5.

Thermoreflectance imaging

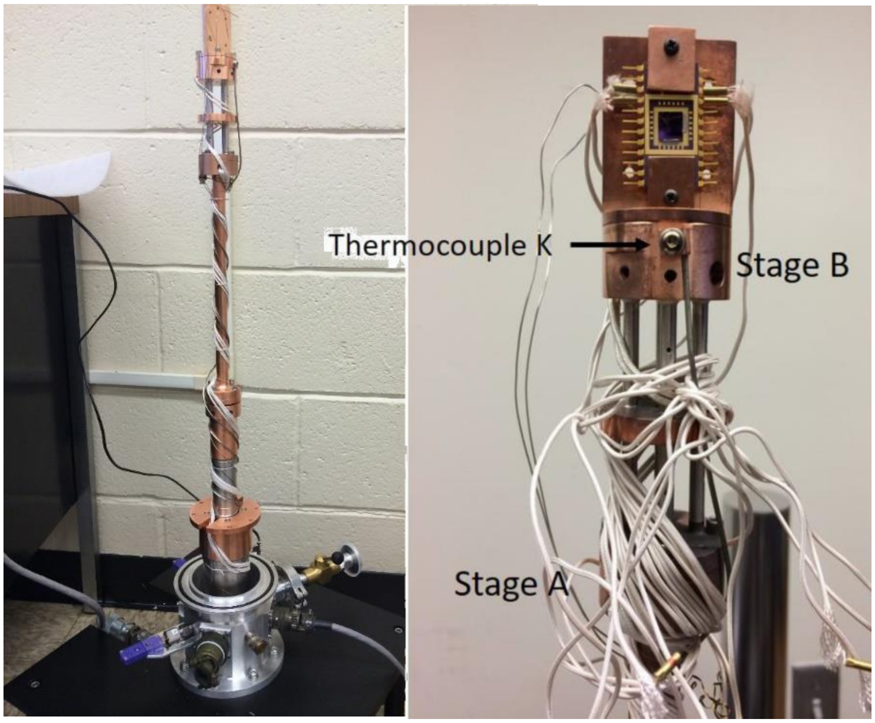

Figure 2- 12: Transport measurement station for thin film materials

Thermoreflectance imaging is a non-invasive technique based on the physics of light reflectance which responds proportionally to the material's temperature change [35], as the refractive index of the sample surface changes with temperature (ΔT), resulting in a change in the reflection intensity ($\Delta R/R$), following the relation expressed as Eq. 2-5 [36]:

$$\frac{\Delta R}{R} = \chi \Delta T \tag{2-5}$$

where χ is the thermoreflectance coefficient, which mainly depends on the studied material and the wavelength of the illuminated light. Except for some well-documented elemental materials such as Au, Pt and Si etc, the thermoreflectance coefficient needs to be calibrated to obtain the absolute temperature values.

The thermoreflectance imaging system (MicroSanj) in our laboratory and its schematic diagram are shown in Fig. 2-13. It has a control unit that generate and synchronizes a LED light source (530 nm green light is used in this study) for illumination, and a pulsed electrical current applied on the measured device. The temperature change due to the applied current modifies the reflection intensity, which can be captured by a charge-coupled device (CCD) camera and sent back to the control unit for analysis. The synchronized diagram for a typical transient thermoreflectance measurement can be found in Ref. [35]. A precise lock-in of the light and electrical signals allow the system to capture the transient temperature mapping under bias. However, since the proportional reflectivity change corresponding to the temperature change is usually very small as being on the order of 10^{-4} [35], signal measured by the CCD camera is averaged over many device thermal excitation cycles to improve the signal to noise ratio.

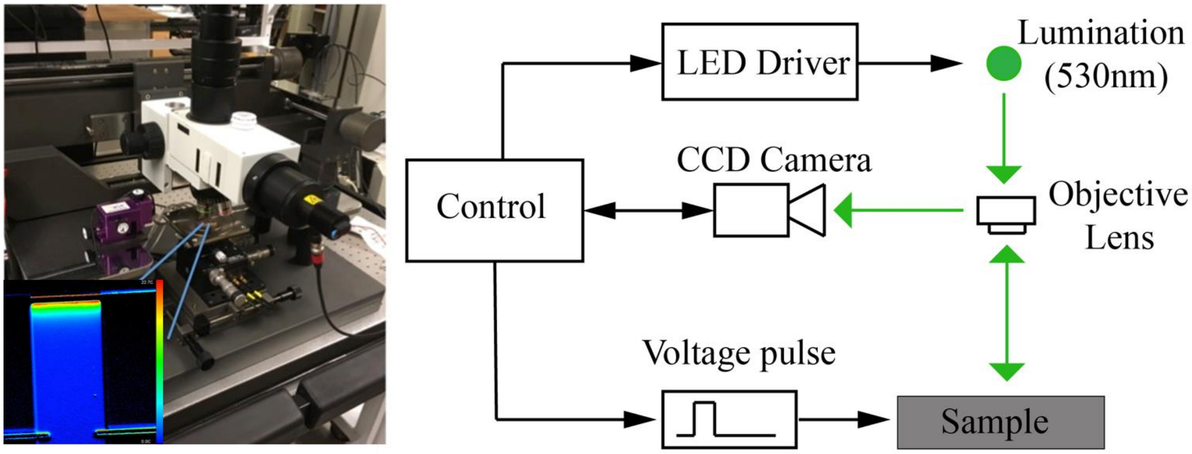

Figure 2- 13: MicroSanj thermoreflectance imaging system in our laboratory and its working schematic diagram

Using this technique, we can measure either transient or steady state temperature profile of the device surface under pulsed voltage bias. Then, by using the classical fin equation [37] to fit the exponential-decay temperature curve, we can extract the in-plane thermal conductivity of thin film materials, which is the holey Si device for this study.

In order to measure the in-plane thermal conductivity as a function of temperature, we have designed and installed a low-vibration cryostat chamber station equipped with the thermoreflectance imaging system, as shown in Fig. In order to maintain a relatively strict alignment of sample surface during the thermoreflectance measurement, the cryostat has a vibration damping system allowing thermal imaging in vacuum and under controlled wide temperature range from 8K to 800K. A high-quality quartz window is used for light transmission (close to 100%).

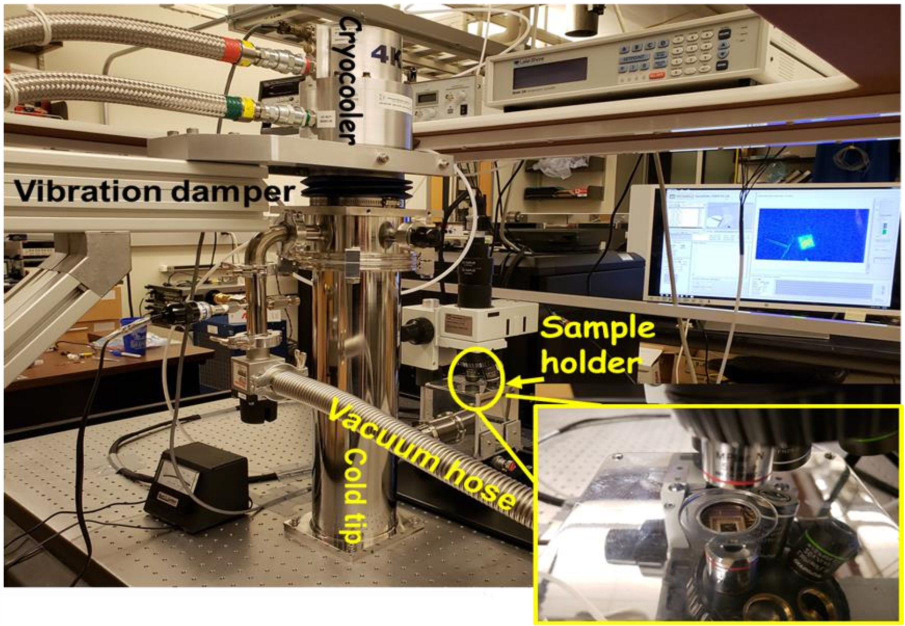

Figure 2- 14: An ultralow vibration cryostat chamber equipped with the thermoreflectance imaging system

Chapter 3: β-$FeSi_2$ – SiGe nanocomposites by React/Transform Spark Plasma Sintering

3.1. Introduction and rationales

According to the Fe-Si binary phase diagram shown in Figure 3-1, there are two phases of iron disilicide: metallic α-phase (α-$FeSi_{2+\delta}$), which has a tetragonal structure and is stable at $T > 1210$ K; and semiconducting β-phase (β-$FeSi_2$), which has an orthorhombic structure and is stable below 1210 K. ε-phase monosilicide (ε-FeSi) is a metallic, cubic phase, which can be generated by the eutectic decomposition at ~66.6 at% Si.

As one of a handful of semiconducting silicides, β-$FeSi_2$ has been studied as a potential candidate for industrial scale thermoelectric materials, due to its inexpensive and non-toxic constituents, excellent oxidation resistance[38] and mechanic robustness. However, despite its high Seebeck coefficient[39], ZT has been limited to values on the order of 0.2[40]. This is mainly due to its relatively high thermal conductivity (>12 W/m K for undoped β-$FeSi_2$ at room temperatures[41]) and poor electrical conductivity resulting from low carrier mobility (~ 1 cm^2/V s at room temperatures[42][43]). In addition, conventional approaches to synthesize β-$FeSi_2$ are inefficient, as the eutectic reaction (L → ε-FeSi + α-$FeSi_{2+\delta}$, as annotated with the blue arrow in the Fe-Si binary phase diagram in Fig. 3-1) makes it impossible to obtain single phase β-$FeSi_2$ directly from the melt. While the phase transformation from the semiconducting to metallic phase is fast, the reverse transition from eutectic α-$FeSi_{2+\delta}$/ε-FeSi and to β-$FeSi_2$ is very slow. This usually requires prolonged annealing at elevated temperature (~850 ºC) for the peritectoid reaction (ε-FeSi + α-$FeSi_{2+\delta}$ → β-$FeSi_2$) to complete, as the product β-$FeSi_2$ forms an intervening layer and suppresses further diffusion between α-$FeSi_{2+\delta}$ and ε-FeSi[44]. In turn, this produces coarsened microstructure with excessive thermal conductivity. Direct formation of β-FeSi$_2$ from elemental powders by mechanical alloying[45][46] requires extensive milling time and inevitably introduces contamination and defects[47] that are deleterious to the electrical transport. Another route that has been explored by us and others is to create a β-FeSi$_2$ + Si nanocomposite by annealing stoichiometric α-FeSi$_{2+\delta}$ below the eutectoid isotherm (α-FeSi$_{2+\delta} \rightarrow \beta$-FeSi$_2$ + Si, as annotated as the red arrow in the Fe-Si binary phase diagram in Fig. 3-1). Aging for > 100 hrs at 600 ºC circumvents ε-FeSi formation and forms finely dispersed, rod-like diamond cubic Si inclusions with diameters < 50 nm in β-FeSi$_2$ matrix[48][49], as shown lower right in Fig. 3-1. Higher aging temperature (~900 ºC) would result in coarsening of the microstructure, as shown upper right in Fig. 3-1. Using this approach, besides the obvious processing inefficiency, poor thermoelectric performance has been shown in the nanocomposite system[50]. The electrical conductivity is too low due to the intrinsically low carrier mobility in β-FeSi$_2$ matrix and the large band offset between

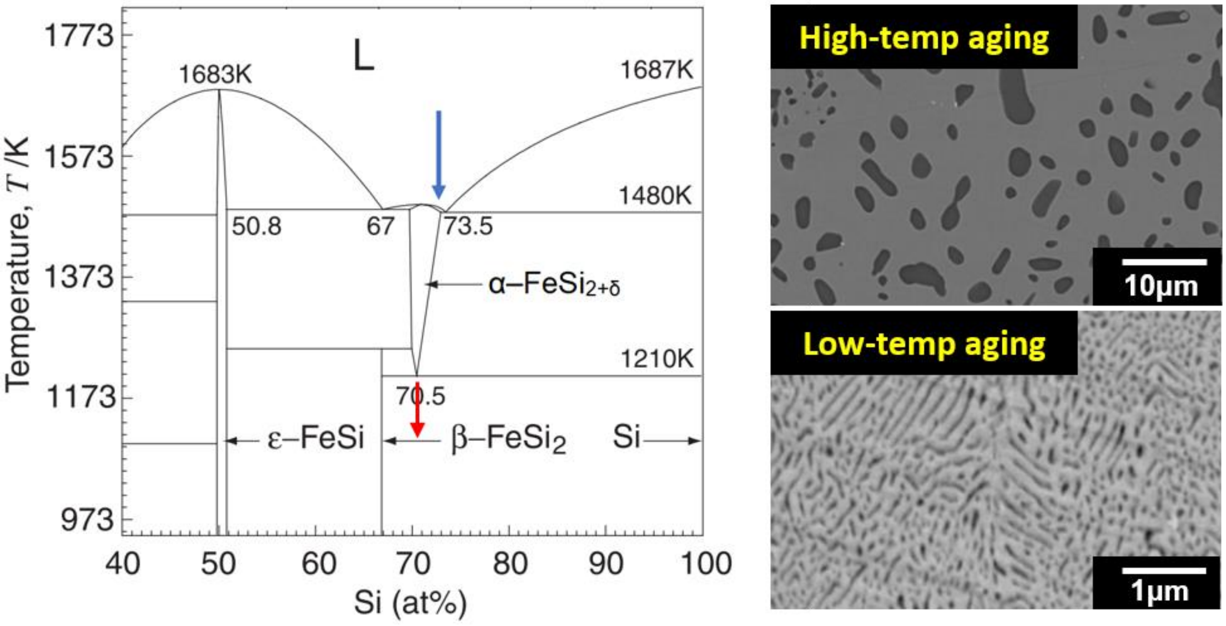

Figure 3-1: The left showing Fe-Si binary phase diagram on Si-rich side; on the right showing the microstructure comparison by aging Fe-Si at eutectoid isotherm at low and high temperatures

β-$FeSi_2$ and Si (~0.3eV for β-$FeSi_2$/Si(n) at 300K[51]). The thermal conductivity is still relatively high despite the nanostructuring, due to the high thermal conductivity of Si and the rather low β/Si thermal boundary resistance[52].

In the pursuit of improving the β-$FeSi_2$–based system as thermoelectric materials that have potential commercial feasibility, we developed a facile synthesis route to incorporate small amounts of Ge into the material, in the form of SiGe nano-inclusions amongst the nano-grained β-$FeSi_2$ matrix, solely by solid state reaction/transformation without prolonged mechanical alloying or post-annealing, using spark plasma sintering (SPS).

Having a combination of interatomic-scale (alloying) and nanoscale features can effectively scatter phonons over a large range from small to long wavelengths[53]. It is shown that nano-structuring can reduce the thermal conductivity of bulk silicon by a factor of 10 and that the addition of only 5% germanium can reduce the thermal conductivity of the nanostructured sample by another factor of 2[54]. Therefore, the boundary scattering from nanoscale matrix grains and inclusions, combined with alloying scattering from the Si-Ge diamond cubic (DC) phase, are expected to hierarchically suppress the thermal conductivity of the β-$FeSi_2$/DC composite system. Furthermore, the bandgap of the DC phase will be reduced by incorporation of Ge, permitting tuning of the Ge composition to improve band alignment across the heterointerface to facilitate carrier transport. Therefore, the benefit of compositing the high mobility DC phase within β-$FeSi_2$ might be realized. Otherwise it is nearly impossible to improve the intrinsically low carrier mobility by modifying β-$FeSi_2$ phase alone due to the unusually strong electron-phonon scattering in the band-edge states of β-$FeSi_2$[55].

In order to obtain these benefits, however, we must selectively incorporate Ge into eutectoid Si while maintaining the nanoscale structure. This is very challenging by conventional metallurgical approaches. Ge has limited solubility in α-$FeSi_{2+\delta}$, so the subsequent alloying of the Ge and eutectoid Si is diffusion limited during eutectoid decomposition. On the other hand, the requirement for use of low annealing temperatures in order to produce fine-scale eutectoid structures restricts diffusional alloying of Ge and Si across the interleaved β-$FeSi_2$ phase.

Mohebali, et al. reported the thermoelectric properties of β-$FeSi_2$ – $Si_{0.8}Ge_{0.2}$ composites and compared with β-$FeSi_2$[56]. The β-$FeSi_2$ – $Si_{0.8}Ge_{0.2}$ composites were formed by mixing powders of Co-doped β-$FeSi_2$ and P-doped SiGe. These powders were themselves formed by mechanical alloying from elemental powders. The electrical conductivity was indeed enhanced significantly after adding SiGe into β-$FeSi_2$, and the peak figure of merit ZT of the composite reached 0.54 at 850K. Nevertheless, the process was still inefficient with prolonged mechanical alloying of each constituent phase (~200 hrs in total) and post-annealing (20 hrs at 850 ºC). Furthermore, no microstructural information whatsoever was reported in Mohebali, et al. Thus we anticipate that the thermoelectric properties can be further improved by optimization of the microstructure and electronic structure. In this study, I have developed a novel React/Transform Spark Plasma Sintering (R/T SPS) approach. Different from the Reactive SPS[32], accelerated *phase transformation* under SPS conditions underlies the nanocomposite synthesis. A two-step sintering process is adopted using a powder mixture of Ge and α-$FeSi_2$ requiring only 1 hr. ball milling. It shows that eutectoid decomposition of α-$FeSi_2$ completes rapidly in the first stage (800 ºC for 5~10 mins). Ge then selectively incorporates into the eutectoid Si during the second stage (880 ºC for 5~10 mins). We thus obtain fully dense β-$FeSi_2$ – SiGe nanocomposite in an efficient manner and at a relatively low temperature.

In next sections, both processing to achieve excellent microstructural control, and the resultant thermal conductivities will be discussed. To understand the key determinants of the thermal transport, the thermal conductivity of this two-phase nanocomposite system is modeled, in which phonon-phonon scattering, alloying scattering (in DC phase) and boundary scattering (size effect) are considered in each phase and finally average over the two phases to obtain the thermal conductivity of the composite. The model reproduces the experimental data closely. It was found that thermal conductivity was considerably suppressed both by nanostructuring and Ge incorporation into DC inclusions. This study provides a foundation for subsequent investigation of electronic structure optimization, and the electronic doping strategy for final ZT enhancement, discussed in Chapter 4. The enhanced phase transformation rates and selective alloying in R/T SPS approach can also be applied in other nanostructured thermoelectric materials synthesis.

3.2. Experimental details

Single-phase α-$FeSi_{2+\delta}$ was first prepared by arc-melting elemental Fe (99.99% purity) and Si (99.999% purity) pieces at stoichiometric ratio of $Fe_{29.4}Si_{70.6}$ in an argon atmosphere. X-Ray Fluorescence (XRF) and Inductively Coupled Plasma - Optical Emission Spectroscopy (ICP-OES) were used to confirm the stoichiometry. The α-$FeSi_{2+\delta}$ ingot was then crushed and combined with elemental Ge (99.999% purity) pieces to respective nominal compositions - $(Fe_{29.4}Si_{70.6})_{1-x}Ge_x$ (x = 0, 0.02, 0.05, 0.07, 0.1). Tungsten carbide grinding balls and the material with a weight ratio of 5:1 were then loaded into a tungsten carbide vial under Argon atmosphere for 1 hr. vibrational ball milling (SPEX 8000). The resultant submicron powder was then loaded in a graphite die of 12.7 mm inner diameter and sintered in Thermal Technologies spark plasma sintering system (model 10–4). A two-step sintering approach was adopted - the temperature was first ramped up to 800 ºC at a rate of 200 ºC/min and held for 10 minutes, and then ramped up to 880 ºC and held for another 10 minutes, at 60 MPa under argon atmosphere. The densities of the compacted pellets were measured by the Archimedes' method, and near-bulk densities were generally obtained. Phase identification was performed using x-ray diffraction on a PANalytical X'Pert Pro MPD, combined with Rietveld refinement analysis (Highscore Plus) for determining the phase compositions and volume fractions. Microstructure images and elemental mapping were obtained using FEI Quanta 650 scanning electron microscope (SEM) and energy-dispersive X-ray spectroscopy (EDS), operated at 5-10kV. Transmission electron microscopy (TEM) was performed on FEI Titan 80–300 operated at 300 kV. Local elemental imaging was obtained under energy-filtered TEM (EFTEM) mode. The thermal diffusivities were measured by a laser flash apparatus (467 HyperFlash, NETZSCH). The specific heat of the composite material was estimated by averaging the C_p of constituent phases[41][57] according to their weight fractions. The thermal conductivities were then obtained by the product of the specific heat, thermal diffusivity and density, i.e. $\kappa = C_p \alpha \rho$.

3.3. React/Transform Spark Plasma Sintering

Our broad strategy in the two-step R/T SPS process follows from the following observations. SPS at 800 ºC promotes rapid eutectoid decomposition $\alpha \rightarrow \beta + Si$ since this temperature is at the nose of the time-temperature-transformation (TTT) diagram[49][58][59], which on the other hand, still requires ~ 3 hours to complete transformation by conventional isothermal anneal. However, at this moderate temperature, Ge from the powder does not have sufficient mobility to alloy, and sintering itself is also incomplete. By raising the temperature in the second step (880 ºC), we achieve $\beta + Si + Ge \rightarrow \beta + SiGe$, at nearly full bulk density. These mechanisms – enhanced eutectoid decomposition and facile, selective Ge-Si alloying by R/T SPS process – are depicted in Fig. 3-2, illustrating the evolution of the phases and microstructure. First, a submicron powder of well-mixed α-$FeSi_2$ and Ge is obtained by a short time ball milling. It is then held at 800 ºC in the SPS, mainly for completion of eutectoid decomposition. Nucleation in the confined submicron α-$FeSi_2$

particles give rise to nanograined β-$FeSi_2$. The Si rejected from the α phase to become eutectoid Si can then easily diffuse onto the β-$FeSi_2$ grain boundaries. This depletes excess Si within the β-$FeSi_2$ nanograins. Meanwhile, the localized joule heating rapidly produces necking, reducing the free surface area, which suppresses surface diffusion that leads to unwanted coarsening of particles. More importantly, the rapid formation of grain boundaries implies that grain boundary diffusion becomes the dominant transport mechanism, which provides fast diffusion paths for Ge to infiltrate the eutectoid grain network, and then alloy with the resultant eutectoid Si. Therefore, facile formation of compositionally homogeneous SiGe nanograins takes place along the β-$FeSi_2$ grain boundaries. Another 5-10 minutes held at 880 ºC then completes the selective alloying and final compaction, leaving a dense nanocomposite with microstructure as shown in Fig. 3-2 c), in which the SiGe nanograins are randomly distributed among the nanograined β-$FeSi_2$ matrix. Microstructure characterization will be discussed in the next session.

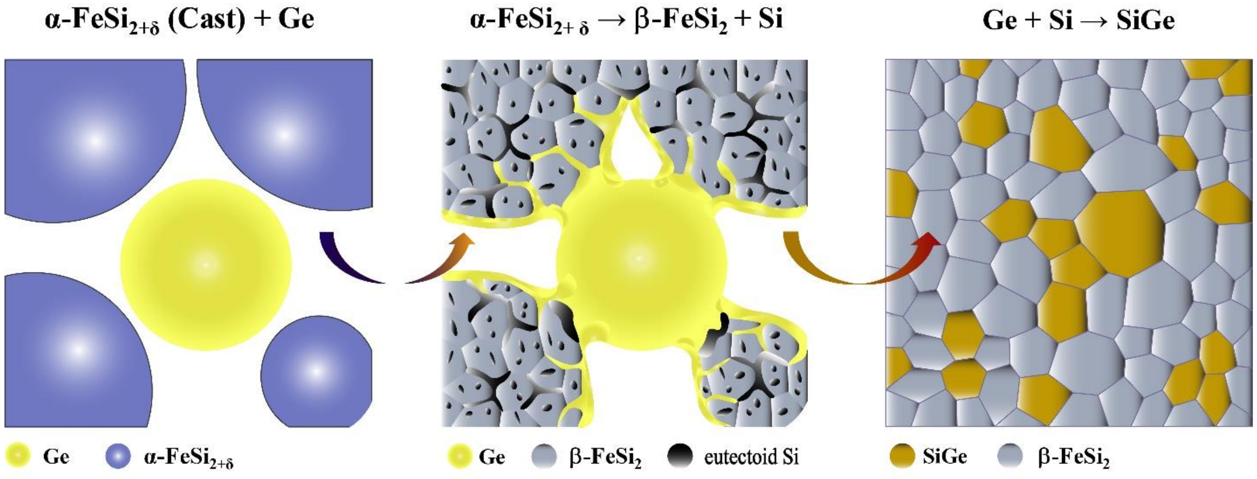

Figure 3-2: Schematic of the two-step R/T SPS process – a) as-milled α-$FeSi_{2+δ}$ + Ge powder; b) microstructure evolution during first stage heating to 800 ºC with completion of eutectoid decomposition and start of Ge selective alloying; c) second stage heating at 880 ºC to sinter to final microstructure of nanograined SiGe distributed amongst nanograined β-$FeSi_2$

3.4. Results and discussion

3.4.1. Phase and microstructure

X-ray diffraction and Rietveld refinement analysis

Figure 3-3 a) shows the XRD pattern of as-milled powder after 1 hr. ball milling. The powder consists of α-$FeSi_{2+\delta}$ and elemental Ge, with no apparent impurity phases or indications of mechanical alloying. Fig. 3-3 b) displays the spectra of the SPS-ed samples with compositions $(Fe_{29.4}Si_{70.6})_{1-x}Ge_x$; x=0, 0.02, 0.05, 0.07, 0.1. Hereafter we refer to this sequence of samples simply as G0, G2, G5, G7, G10. Fig. 3-3 c) shows the enlarged view of b) over the range 2θ = 27.5-29.5º. All SPS-ed samples were processed by two-step sintering, as described above. For G0 and G2, eutectoid decomposition was already nearly complete, with only a small amount of residual α-$FeSi_{2+\delta}$ observed. For G5 and G7, the XRD patterns indicate a composite of β-$FeSi_2$ and SiGe phases, with no residual α-$FeSi_{2+\delta}$. For G10, the metallic ε-FeSi phase emerges, which we believe is an expression of ternary phase equilibrium. Examination of the DC (111) peaks shown in Fig. 3-3 c) indicates that as the Ge content increases, the DC peaks shift towards lower angles. This proves that Ge incorporated substitutionally with a concomitant increase in the lattice parameter. On the other hand, the β-$FeSi_2$ peaks have constant 2θ, meaning little Ge substitution within β-$FeSi_2$. We obtained both the volume fraction and Ge composition of the DC phase by Rietveld refinement of the high resolution XRD patterns, as listed in Table 3-1: both quantities increase as x (overall Ge content) increases. For G10, the three-phase equilibrium indicates that the saturation point of Ge composition is ~ 42.5%, which determines the tuning range of Ge composition in the DC phase. This allows us to map out the Fe-Si-Ge ternary phase diagram in the Si-rich corner (at 880 °C), as shown in Figure 3-4. It indicates that, in order to avoid ε-FeSi formation, Fe-Si-Ge composition needs to be within the β-$FeSi_2$ + DC region.

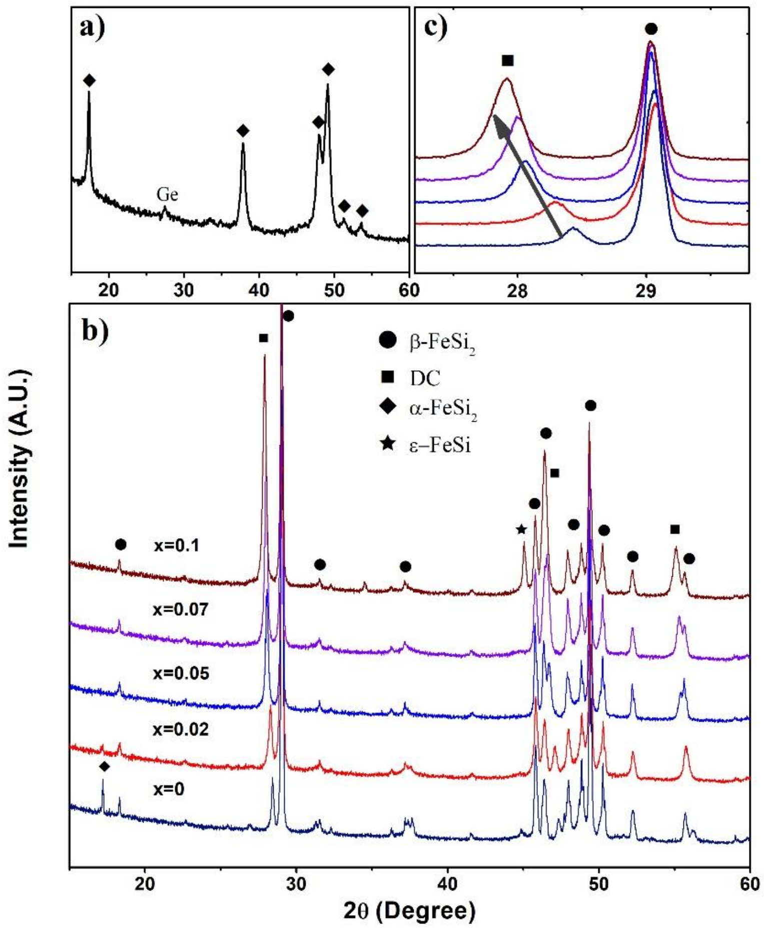

Figure 3- 4: XRD patterns of a) as-milled α-FeSi$_{2+\delta}$ + Ge powder, b) SPS-ed samples of (Fe$_{29.4}$Si$_{70.6}$)$_{1-x}$Ge$_x$ (x=0, 0.02, 0.05, 0.07, 0.1 as nominal compositions), and c) the enlarged view of b) at 2θ = 27.5-29.5°

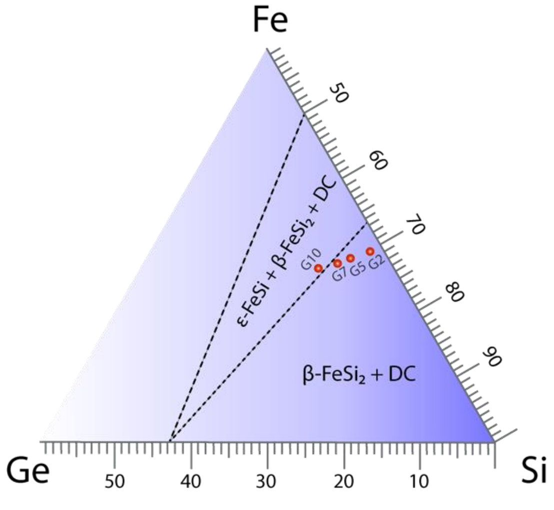

Figure 3-3: estimated Fe-Si-Ge ternary phase diagram (Si-rich corner)

Table 3-1

$(Fe_{29.4}Si_{70.6})_{1-x}Ge_x$	Name	Phases	Volume fraction (% DC)	DC composition (at% Ge)	Relative density
x = 0	G0	β-$FeSi_2$ DC α-$FeSi_2$ (undecomposed)	16.3%	0	93.8%
x = 0.02	G2	β-$FeSi_2$ DC	17.9%	9.3%	99.1%
x = 0.05	G5	β-$FeSi_2$ DC	21.3%	28.5%	99.8%
x = 0.07	G7	β-$FeSi_2$ DC	23.0%	33.5%	98.8%
x = 0.10	G10	β-$FeSi_2$ DC ε-FeSi	N/A	42.5%	~98%
β-FeSi	Reference sample	Comments: undergo conventional synthesis with average grain size of ~500nm			99.5%

Mesoscale microstructure by scanning electron microscopy

Mesoscale microstructures of the precursor powder and sintered material are presented using SEM. Figure 3-5 a) shows a representative SEM micrograph of the as-milled α-$FeSi_{2+\delta}$ /Ge mixed powder, with particle sizes of submicron range. The fracture surface, mostly intergranular, of the sintered pellet shown in Fig. 3-5 b) indicates that the final grain size is 200 nm on average, which is smaller than the initial powder particle size, due to multiple β nucleation events within each α grain. This provides an additional mechanism for controlling the grain size via nucleation or recrystallization, as discussed in Chapter 2. The backscatter electron (BSE) images of G0 – G7 all exhibit two-phase nanocomposite microstructure, with DC grains embedded amongst the β-$FeSi_2$ grains. This is also confirmed by the EDS elemental mapping of sample G5 shown in Fig. 3-5 f). The BSE contrast of the DC phase becomes brighter as Ge content increases. Although there is variable contrast within the DC inclusions, point-by-point EDS measurements obtained from multiple DC inclusions in each sample show that the inclusions all have consistent compositions (within a range of ± 1.5

at%), suggesting that thermodynamic equilibrium in composition is achieved during the short SPS process. The contrast variation arises in part from imaging effects, and also because the DC inclusions are polygranular, as shown below using TEM. For sample G10 shown in Fig. 3-5 h), the metallic ε-FeSi phase is clearly observed, consistent with the XRD data. In these samples, the size of DC inclusions ranges from 100 nm to 500 nm according to the SEM images. The DC inclusions slightly coarsen as x increases. In all BSE micrographs of Fig. 3-5, a very fine (typical diameters < 20 nm) dispersion of dark particulate, with very small volume fraction, can be observed. Based on EDS linescans, these are believed to be SiO_2, an almost inevitable result of the ball milling process. The role of these precipitates on the thermal conductivity in our samples is believed to minor due to the very small volume fractions.

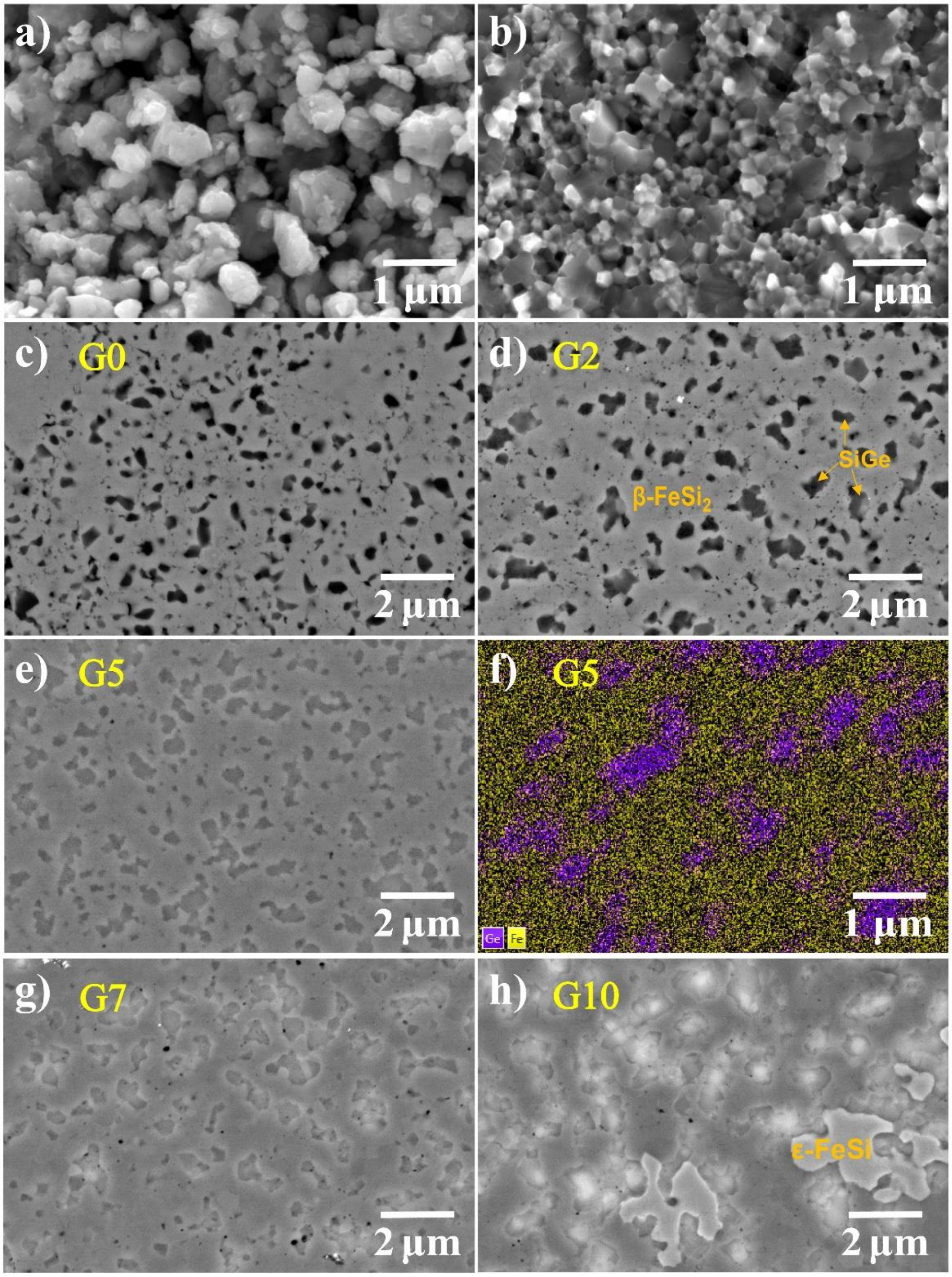

Figure 3-5: a) typical SEM micrograph of as-milled α-$FeSi_{2+\delta}$/Ge mixed powder; b) fracture surface of the SPS-ed sample; c) – h) BSE images of polished G0 – G10 samples; f) EDS map of sample G5, showing Ge and Fe distributions

Nanoscale microstructure by transmission electron microscopy

Figure 3-6 a) displays a typical bright field (BF) TEM image of sample G5. The grain size ranges from 50nm – 300nm. It is noted that the β-$FeSi_2$ grains all exhibit internal lamellar contrast in the BF image. Fig. 3-6 b) shows one particular β-$FeSi_2$ grain along a <012> zone axis, with a high density of planar defects spanning the whole grain, also resulting in diffuse streaks in the selected area electron diffraction (SAED) pattern. Atomic resolution imaging shown in Fig. 3-6 c) reveals the nature of these defects. The oblique orange lines correspond to the continuous lattice shifting

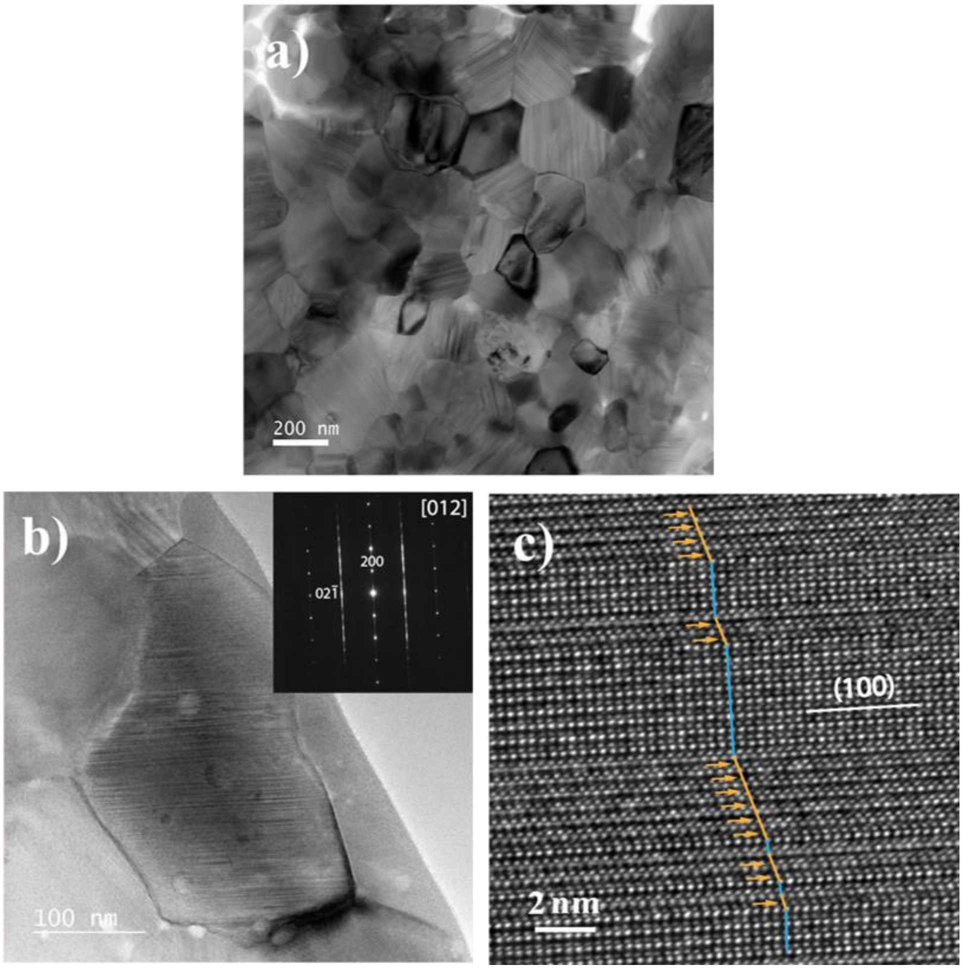

Figure 3-6: a) bright field TEM image of sample G5 and b) one particular β-$FeSi_2$ grain along [012] zone axis, with selected area diffraction pattern shown inset; c) high-resolution TEM image of β-$FeSi_2$ with arrows showing the lattice shifting of the dominant stacking faults along the [012] zone axis

by ½ along [011] in β(100) planes, i.e. β(100)[011]/2 stacking faults. Both the imaging and diffraction results are fully consistent with a detailed TEM analysis by Zheng, et al. on β-$FeSi_2$ thin films grown on Si (111) by solid-phase epitaxy[60].

Elementally-sensitive imaging in Fig. 3-7 b) obtained by EFTEM, with its corresponding BF image in Fig. 3-7 a), shows the distribution of the DC phase (colored in purple) in the β-$FeSi_2$ matrix. This further shows that DC particles are not embedded within individual β-$FeSi_2$ grains. Instead, the DC phase forms standalone or clustered grains with comparable grain size to those of β-$FeSi_2$. The most apparent DC inclusions shown in the previous SEM images are the larger SiGe multi-

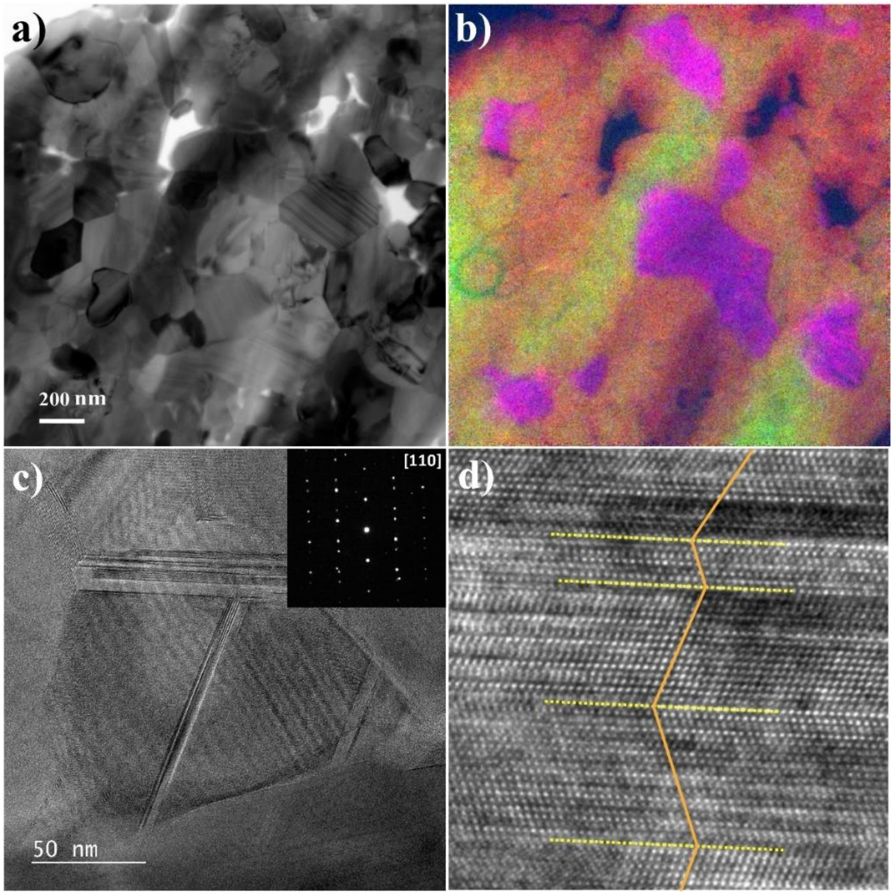

Figure 3-7: a) BF image of sample G5; b) corresponding EFTEM image highlighting disposition of Ge; c) DC grain embedded amongst β-$FeSi_2$ grains with clean grain boundaries; d) high-resolution image of {111} twins from c)

grain clusters, such as the one shown in the center of Fig. 3-7 b). Planar defects are also found in the DC grains. Fig. 3-7 c) shows a typical embedded SiGe grain with clean grain boundaries and {111} twins as indicated by the SAED pattern along [110]. The twin boundaries are marked in the yellow dashed line in Fig. 3-7 d).

Discussion

According to XRD, eutectoid decomposition in sample G0 was close to completion within 10 minutes at 800 ºC, with only trace amounts of undecomposed α-$FeSi_{2+\delta}$ in some of the large particles observed in SEM. By contrast, isothermal annealing of cast eutectoid Fe-Si materials at 800 ºC requires up to 8 hours to complete the eutectoid decomposition according to the TTT diagram. This strongly suggests that phase transformation kinetics can be enhanced when taking place under SPS conditions. Two aspects of the processing may be important. The first is the increased area per volume of interfaces/surfaces in the green body. The second aspect relates to the SPS process itself, wherein relatively large pulsed direct currents can create local joule heating and applied pressure can induce plastic deformation and particle rearrangement[31]. Local joule heating enhances local diffusion, and may create additional mass transport processes associated with large thermal gradients[33]. In addition, electromigration[61], reduced activation energy of defects migration[34], as well as grain boundary diffusion (facile neck formation), all can accelerate the growth kinetics. In order to understand which SPS mechanisms are the dominant factor contributing to the enhanced eutectoid decomposition rate, it would be necessary to perform a more detailed analysis on SPS vs. conventional heat treatment for the Fe-Si binary system.

For the Ge-containing samples G2 – G10, the α-$FeSi_{2+\delta}$ phase completely transformed to β-$FeSi_2$ and DC under the same processing conditions that yielded incomplete transformation in sample G0, which contained no Ge. This implies that the presence of Ge further facilitates the eutectoid decomposition. The reason for it promoting the nucleation of the phase transition is unclear. The shift of the (111) Bragg peak of the DC phase towards lower angles in Fig. 3-3 c) proves that selective Ge incorporation to form $Si_{1-y}Ge_y$ alloys is tunable simply by varying the Ge addition to the powder before SPS. The lack of significant broadening of the DC Bragg peaks indicates that the Ge concentrations in the DC inclusions are relatively consistent, in agreement with EDS. This is important for achieving consistent band edge engineering of the /DC heterointerfaces. For sample G10, the metallic ε-FeSi phase starts to emerge, which is unwanted and expected to deteriorate the power factor. I further annealed the G7 and G10 samples at 880 ºC for 7 days. The resultant XRD patterns (not shown) were identical with the as-SPSed samples, which suggests that thermodynamic equilibrium was achieved by the initial short process in SPS within 10~20 minutes.

The mechanism and phase evolution associated with R/T SPS process discussed in section 3.3 is confirmed by the EFTEM elemental imaging in Fig. 3-7 b), in which the SiGe grains (colored in purple) are adjacent to β-$FeSi_2$ grains instead of being embedded within the β grains. According to the comparison between the bright-field image and EFTEM imaging, some of SiGe inclusions consist of multiple grains. The individual grains and clusters give rise to grading sizes of DC inclusions from 100nm~500nm, as shown in the SEM images. This is favorable for scattering phonons across a range of wavelengths in the Brillouin zone.

TEM identifies the presence of a high density of planar defects in this composite material, which could impact the transport properties. For β-$FeSi_2$, a high density of stacking faults is observed throughout each grain, with spacings from <1 – 10 nm, consistent with a low stacking fault formation energy. According to Zheng's structure model[60], the low stacking fault energy can be attributed to the small Si-Fe-Si bond distortion, with no change in Fe-Si bond distance. This type of defect may be ubiquitous: has been seen in β-$FeSi_2$ formed by solid-phase epitaxy,[62], ion-implantation of Fe into Si[63], and cast bulk samples[44]. The impact of high densities of stacking faults on the thermoelectric properties has rarely been studied[64]. The structure might behave like a coherent superlattice, scattering phonons with shorter wavelength. Combined with phonon scattering from the 50nm ~ 1um grains and inclusions, our hierarchical microstructure may scatter phonons with different mean free paths to suppress the overall lattice thermal conductivity. Furthermore, it may introduce additional electronic carrier scattering to increase the Seebeck coefficient. And the carrier conduction should not be severely compromised, as no broken bonds are present to act as carrier trapping states in β-$FeSi_2$ lattice.

3.4.2. Thermal conductivity

In the two-step R/T-SPS process, Ge can be selectively incorporated into eutectoid Si to form compositionally homogeneous DC nanograins. Here, we evaluate the effect of nanostructuring and germanium incorporation on the thermal conductivity. Figure 3-8 shows the experimental data (diamonds) of the thermal conductivity versus temperature for samples G0 – G7. Adding just a few atomic percent of Ge to the system significantly reduces the overall thermal conductivity, with a 38% reduction in κ (compared with the porous G0 sample) at room temperature when x=0.07 (G7). Since the DC grains and clusters are relatively large in size (~ 400 nm on average) and have a non-negligible volume fraction (~20%), the thermal conductivities of both constituent phases need to be considered when modeling the overall $\kappa_L(T)$. Therefore, we simulate the lattice thermal conductivity of both the β-$FeSi_2$ and DC phase with their respective composition and grain size in each sample.

The total thermal conductivity is the sum of lattice (κ_L) and electronic (κ_e) thermal conductivities. In our case, both constituent phases are undoped, so κ_e can be neglected as it is orders of magnitude lower than κ_L, indicated by the very low measured electrical conductivities. The Debye model of lattice thermal conductivity is given by Eq. 3-1,

$$\kappa_L = \frac{{k_B}^4 T^3}{2\pi^2 v \hbar^3} \int_0^{\theta_D/T} \tau \, \frac{x^4 e^x}{(e^x - 1)^2} dx \qquad 3\text{-}1$$

where $x = \hbar\omega/k_B T$, k_B is Boltzmann constant, ω is phonon frequency, $\hbar$ is reduced Planck constant, v is sound velocity, θ_D is Debye temperature, and τ is the total phonon scattering relaxation time. The total scattering rate (τ^{-1}) is expressed using Matthiessen's rule, as a sum of point defect (${\tau_{PD}}^{-1}$), alloying (${\tau_a}^{-1}$), Umklapp (${\tau_U}^{-1}$), and boundary (${\tau_b}^{-1}$) scattering contributions, as follows:

$$\tau^{-1} = {\tau_{PD}}^{-1} + {\tau_a}^{-1} + {\tau_U}^{-1} + {\tau_b}^{-1} \qquad 3\text{-}2$$

In this study, point defect, Umklapp, and boundary scattering are considered for the β-$FeSi_2$ phase, and alloying, Umklapp, and boundary scattering are considered for DC SiGe phase. To analyze the SiGe phase, I first use the Debye model to fit the experimental data reported for bulk intrinsic Si and Ge in the 300-800K temperature range[65] using a least squares fitting method in Matlab. Since these references are pristine phases, the only important mechanism is Umklapp scattering ${\tau_U}^{-1}$, expressed as

$${\tau_U}^{-1} = BT\omega^2 e^{-\theta_D/3T} \qquad 3\text{-}3$$

where B is used as a fitting parameter to reproduce the experimental data (all parameters used are listed in Table 3-2). For the $Si_{1-y}Ge_y$ alloys, the Umklapp term can then be approximated as a linear interpolation between Si and Ge:

$${\tau_U}^{-1} = (1-y){\tau_{U,Si}}^{-1} + y{\tau_{U,Ge}}^{-1} \qquad 3\text{-}4$$

I then introduce the alloy scattering term ${\tau_a}^{-1}$, expressed as:

$${\tau_a}^{-1} = y(1-y)A_{SiGe}\omega^4 \qquad 3\text{-}5$$

where I use the parameter A_{SiGe} value reported in Ref [66]. I also include a boundary term, which represents the cutoff phonon mean free path due to finite grain size, expressed as:

$$\tau_b{}^{-1} = v_{SiGe}/L, \tag{3-6}$$

where $v_{SiGe}^{-2} = (1-y)v_{Si}^{-2} + yv_{Ge}^{-2}$, and L = 400 nm. We can then simulate $\kappa_L(T)$ of $Si_{1-y}Ge_y$ where y = 0.093, 0.285, 0.335 (i.e., the Ge compositions of DC phase in sample G2, G5, G7 according to Rietveld refinement of XRD), as shown in Fig. 3-9 a).

Next, I develop a similar Debye model for the β-$FeSi_2$ phase. Since it is not feasible to obtain single phase β-$FeSi_2$ by the same process, in order to know the $\kappa_L(T)$ of nanograined β-$FeSi_2$ (200 nm), I spark plasma sintered a ball-milled $FeSi_2$ powder (mixture of α, β and ε-FeSi) at 1000 ºC for 5 minutes, followed by an isothermal annealing at 850 ºC for 48 hours to complete the peritectoid reaction (ε-FeSi + α-$FeSi_{2+\delta}$ → β-$FeSi_2$). The resultant β-$FeSi_2$ possessed a larger average grain size of ~500 nm due to grain growth through the prolonged heat treatment at elevated temperature. I fit the experimental data for $\kappa_L(T)$ in this sample (Fig. 3-9 a)) by considering point defect ($\tau_{PD}{}^{-1} = A_\beta\omega^4$), Umklapp ($\tau_U{}^{-1} = B_\beta T\omega^2 e^{-\theta_D/3T}$), and boundary scattering contributions($\tau_{BD}{}^{-1} = \frac{v_\beta}{500nm}$). The $\kappa_L(T)$ of β-$FeSi_2$ with 200 nm grains (matrix) can then be simulated simply by modifying the boundary scattering term (Fig. 3-9 a)). In order to better ascertain the extent to which nanostructuring suppresses thermal conductivity, I calculated the cumulative thermal conductivities versus mean free path for β-$FeSi_2$ and $Si_{1-y}Ge_y$ at room temperature, shown in Figure 3-9 b). The κ_L of $Si_{1-y}Ge_y$ with grain size of 400 nm have ~70% reduction compared with their single crystal forms, and β-$FeSi_2$ with grain size of 200 nm has a reduction of ~35%.

Table 3-2

Components	Parameter	Value (unit)	Comments
SiGe	v_{Si}	$6400\ (m/s)$	Ref. [66]
	v_{Ge}	$3900\ (m/s)$	Ref. [66]
	$\theta_{D,Si}$	$640\ (K)$	Ref. [57]
	$\theta_{D,Ge}$	$374\ (K)$	Ref. [57]
	B_{Si}	$3.52 \times 10^{-19} (s/K)$	This work
	B_{Ge}	$6.81 \times 10^{-19} (s/K)$	This work
	A_{SiGe}	$3.01 \times 10^{-41} (s^3)$	Ref. [66]
β-$FeSi_2$	v_β	$5663\ (m/s)$	Ref. [67][68]
	$\theta_{D,\beta}$	$630\ (K)$	Ref. [41]
	A_β	$4.21 \times 10^{-43} (s^3)$	This work
	B_β	$1.42 \times 10^{-18} (s/K)$	This work

Finally, to estimate the thermal conductivity of the two-phase nanocomposite, we apply the rule of mixtures (Eq. 3-7) using the modeled $\kappa_L(T)$ of β-$FeSi_2$ and $Si_{1-y}Ge_y$ with their volume fractions from Table 3-1.

$$\frac{1}{\kappa_{AB}} = \frac{f_A}{\kappa_A} + \frac{f_B}{\kappa_B} \tag{3-7}$$

The solid curves shown in Fig. 3-8 match well with the experimental data (G2 – G7), indicating that the reduction of thermal conductivity in these samples are mostly determined by Ge incorporation in DC phase as well as nanostructuring. Note that once the models are built for each phase (that is for SiGe and β-$FeSi_2$ phases), no further fitting parameters were used and the thermal conductivity of the composite material can be predicted by the rule of mixtures. The agreement of the prediction and the experimental data is very good.

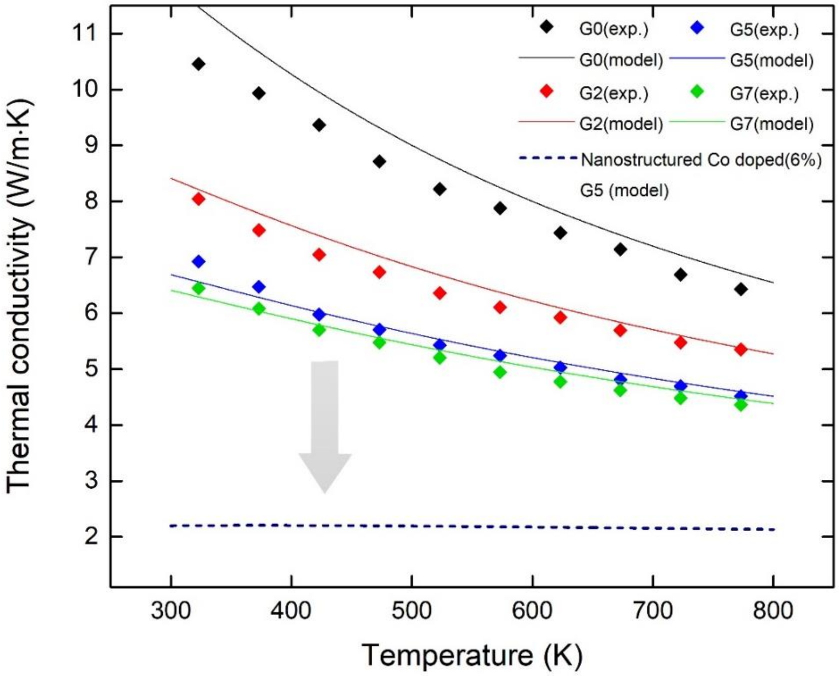

Figure 3-8: Comparison of modeled $\kappa_L(T)$ (solid curves) to measured $\kappa_L(T)$ (diamonds) for samples G0, G2, G5 and G7. Simulated values for nanocomposite of 100 nm β-$(Fe_{0.94}Co_{0.06})Si_2$ and 200 nm $Si_{0.715}Ge_{0.285}$ (G5) are shown with the dashed curve

It is noted that the modeled $\kappa_L(T)$ still slightly overestimates the thermal conductivity (besides the obvious overestimation of the specific G0 sample due to its retained porosity), implying that other sources of scattering may also play a minor role, such as the β/DC interface scattering. One key challenge would be to engineer the DC grain size to be even finer to further boost the interface scattering effect. Meanwhile, substitutional doping (eg. Co) of β-$FeSi_2$ phase was also found to significantly reduce the lattice thermal conductivity[40][69], presumably due to local lattice deformation by strong electron-phonon interactions[70]. We used the same method to predict the $\kappa_L(T)$ of the nanocomposite of β-$Fe_{0.94}Co_{0.06}Si_2$ with grain size of 100nm and $Si_{0.715}Ge_{0.285}$ (G5) with grain size of 200nm, as shown in Fig. 3-8. A very low thermal conductivity approaching 2 W/m K can potentially be realized in this system. These lengthscales, while challenging, should be achievable in R/T SPS process. Efforts to further optimize the microstructure, tune Ge incorporation and electronic doping, with the goal of concurrent optimization of electrical transport, will be discussed in the next chapter, aimed for improving the final ZT performance of the β-FeSi2 based nanocomposite.

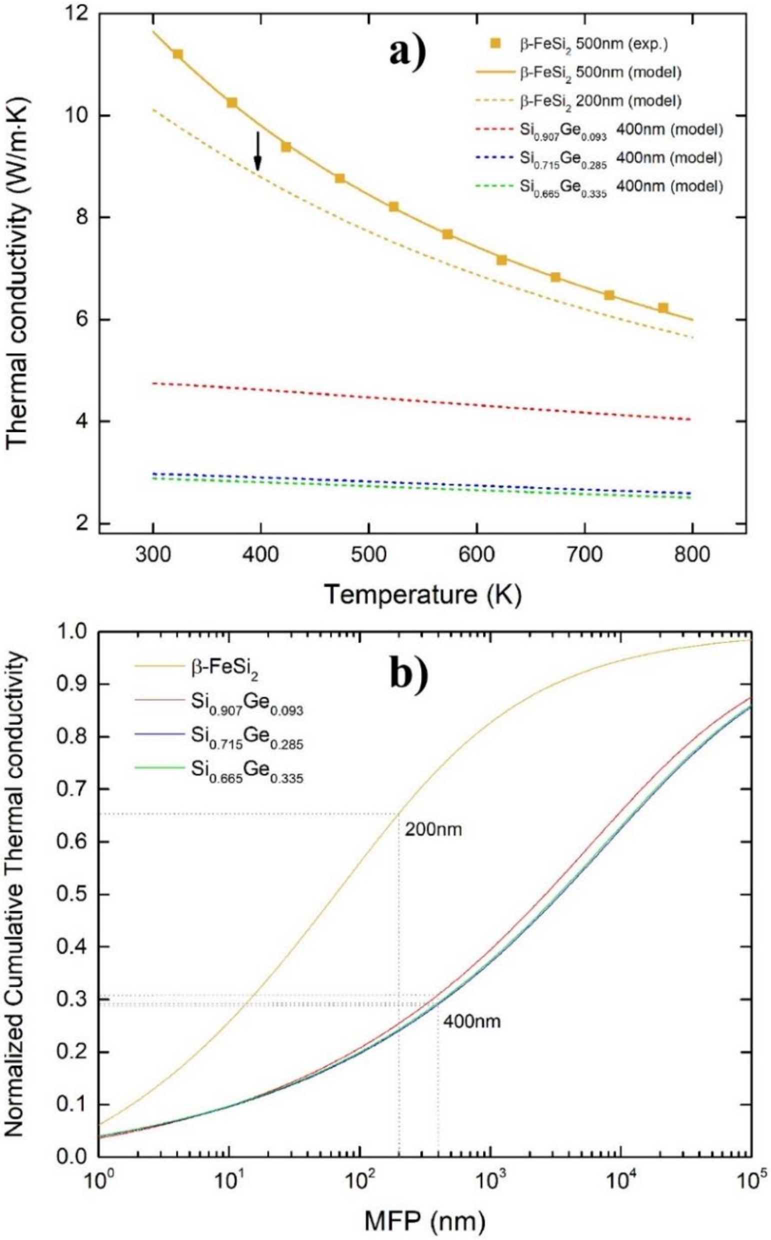

Figure 3-9: a) comparison of theoretical fits to measured $\kappa_L(T)$ for the reference β-FeSi$_2$ (500 nm grain size). Simulated values for 200 nm β-FeSi$_2$ and 400nm Si$_{1-y}$Ge$_y$ are shown with the dashed curves; b) Normalized cumulative thermal conductivity at room temperature versus mean free path calculated from Debye model

3.5. Summary

I developed a novel R/T SPS approach, providing accelerated phase transformation and selective alloying for efficient production of nanocomposites. Bulk, intrinsic β-$FeSi_2$ – $Si_{1-y}Ge_y$ ($(Fe_{29.4}Si_{70.6})_{1-x}Ge_x$) nanocomposites with x=0–0.1 were synthesized solely by solid-state reaction/transformation without mechanical alloying and post-annealing. Fully dense samples were obtained using a two-step sintering method, in which the eutectoid decomposition of α-$FeSi_2$ completes within 10 mins at 800 ºC in the first stage (30 times faster than that of bulk isothermal annealing). It is followed by selective incorporation of Ge into eutectoid Si and final sintering in the second SPS stage, at 880 ºC for 10 mins. This gives a final microstructure of 100–500 nm SiGe grains/clusters embedded amongst 200 nm β-$FeSi_2$ grains.

The Ge composition in DC nanoinclusions is tunable with a broad tuning range of 0 ~ 42.5%, believed to bound the two-phase β+DC equilibrium region in the ternary phase diagram. This provides a foundation for subsequent investigation of band alignment of inclusion/matrix heterointerface for final ZT enhancement. Ge additions of only a few atomic percent suppresses the thermal conductivities significantly, with a 38% reduction when x = 0.07. We successfully modeled the lattice thermal conductivity of the constituent β-$FeSi_2$ and $Si_{1-y}Ge_y$ phases separately by including phonon-phonon scattering, alloying scattering (in DC phase) and boundary scattering (size effect), and then averaging over the two phases to obtain the overall thermal conductivities. The analysis shows that nanostructuring and Ge incorporation, achieved by R/T SPS, were the two dominant contributive mechanisms for reduction of thermal conductivity in this system. Further suppression of the $\kappa_L(T)$ can be realized by transition metal doping the matrix β-$FeSi_2$, which is required anyway to increase the carrier density for use in thermoelectric applications.

In a broader context, the concept of R/T SPS with accelerated phase transformation and selective alloying is a promising alternative route for synthesizing self-assembled nanocomposite materials for thermoelectric applications.

Chapter 4: ZT Optimization of β-$FeSi_2$ – SiGe nanocomposite

4.1. State of art and rationales for improvement

In this chapter, the thermoelectric transport properties will be investigated in n-type doped β-$FeSi_2$ – SiGe nanocomposites. The goal is to understand how the transport properties arise from the tailored microstructure and chemistry, as well as to enhance the ZT performance following the strategies discussed in Chapter 2.

β-$FeSi_2$ has a direct band gap of 0.80–0.95 eV and an indirect band gap of 0.7–0.78 eV [71][72], although there is significant variability in the literature on the gap. Nominally undoped β-$FeSi_2$ is subject to auto-doping and/or non-stoichiometry, which in most reports exhibit p-type conduction and positive Seebeck coefficient. However, β-$FeSi_2$ single crystals obtained from 5N purity starting material showed a n-type conduction instead, with a large negative Seebeck coefficient of -750 μV/K at room temperature[73]. The most effective dopants for n- and p-type β-$FeSi_2$ are Co and Mn (or Al), respectively. Effects of Cu and Pt doping in β-$FeSi_2$ (Fe-site) were studied in Ref. [74] and Ref. [70]. Ge and P doping for Si-site were reported in Ref. [74] and Ref. [75]. In these studies, the final ZT values all show moderate increases after adding these dopants. However, we believe the observed minor improvement should be due to phase precipitation/segregation (e.g. SiGe or SiP phase may be formed in the process) rather than substitutional doping. This argument is also supported by our structural analysis in similar systems discussed in later sections. Isoelectronic substitution of Fe-site provides another possibility to tailor the transport properties. In Ru substituted β-$FeSi_2$, increased power factor is observed for both n- and p-type β-$FeSi_2$[76]. We anticipate that isoelectronic Os substitution could be even more promising, based on the concept of high mismatched alloys (HMA), where the containing isoelectronic elements have large differences in terms of atom size, ionicity, and electronegativity, etc. In HMAs, the hybridization between the extended states of the majority component and the localized states of the minority component results in a strong band restructuring, leading to peaks in the DOS and creation of new sub-bands near the original conduction or valence band edge, which give rise to a higher Seebeck coefficient[77]. In addition, $OsSi_2$ is isostructural to β-$FeSi_2$ (*Cmca*), which is expected to allow of a relatively wide tuning range due to large solubility. Moreover, large mass fluctuation would surely suppress the lattice thermal conductivity. Despite having a great promise, due to the toxicity (of its oxide), extremely high melting temperature (3033 °C) and the rarity of osmium, Os-substituted β-$FeSi_2$ for thermoelectric applications is not found in literature so far.

The highest ZT reported for single phase n-type β-$FeSi_2$ is ~ 0.25 for β-$Fe_{0.94}Co_{0.06}Si_2$ at ~ 900K[78], ~0.20 for β-$Fe_{0.95}Co_{0.05}Si_{1.98}$ at ~850K[79], and ~0.19 for β-$Fe_{0.95}Co_{0.05}Si_2$ at 770K[80]. Compositing with small amounts of secondary phases by mechanical mixing are also widely examined, such as using SiO_2[81], Ta_2O_5[82], TiB_2[83], ZrO_2 and rare-earth oxides (Y_2O_3, Nd_2O_3, Sm_2O_3 and Gd_2O_3)[84]. These inclusion phases are indeed helpful in suppressing thermal conductivity as one can expect. However, without concurrent careful control of the microstructure and electronic structure, these composite systems exhibit very limited improvement on final ZT, due to excess compromise in power factor.

As discussed in Chapter 3, the challenge to improve the power factor of β-$FeSi_2$ can be mainly attributed to its poor electron mobility, especially when Co-doped (~ 0.4 $cm^2/V\ s$ for $Fe_{0.95}Co_{0.05}Si_2$[43,85,86]). To further improve the electrical property of β-$FeSi_2$ – SiGe nanocomposites based on the findings in Chapter 3, a phase percolation approach is proposed here. The rationales are two-fold: 1. it is almost impossible to enhance the mobility of β-$FeSi_2$ phase by chemistry modification alone; 2. *Cmca* β-$FeSi_2$ and $Fd\overline{3}m$ diamond cubic DC phases possess drastically different crystal structures and lattice constants, thus semicoherent or incoherent interfaces may play a dominant role in scattering or trapping electrons, despite the fact that the composite is synthesized in a self-assembled manner by eutectoid decomposition. In this context, phase percolation can potentially be a decoupling strategy by forming a composite with β-$FeSi_2$ as the matrix phase, embedding high mobility DC SiGe phase with *hierarchical length scales*. While smaller length scale nanoparticles would contribute to the phonon scattering, the simultaneous presence of larger lengthscales could permit phase percolation that retain good electrical conductivity. The schematic microstructure is shown previously in Fig. 1-13. Here the thermodynamics and kinetics of SiGe phase formation in β-$FeSi_2$ is manipulated via a carefully designed processing sequence, in order to dictate both the volume fraction and morphology of the DC "inclusions" to have a quasi-percolated microconstituent, and a nanoparticulate microconstituent. The percolated DC network should provide electrically-parallel, high mobility pathways for charge carriers while the nanoscale inclusions concurrently reduces thermal conductivity.

I will show that the DC phase can concurrently form in both an extended, percolating morphology due to segregation of Si and Ge to the grain boundaries, and in a compact, nanoscale morphology occurring by eutectoid decomposition in the interiors of the β-grains. We must simultaneously optimize the morphology and volume fraction of the DC phase, the Ge content within the phase, and the selective doping of both phases β, all the while suppressing overall coarsening of the matrix grains and the DC inclusions. These contradicting requirements can be met using React/Transform Spark Plasma Sintering (R/T SPS) approach, which combines solid-state phase transformation, in-situ alloying and doping, and liquid phase sintering into a single process. As discussed in Chapter 2, the conditions inherent to SPS (eg. pulsed current, grain boundary diffusion, applied pressure) can greatly enhance solid-state diffusion[31,33,34,61]. This may permit incorporation/activation of dopants at a lower temperature and shorter times than by isothermal annealing, conducive to retention of nanostructuring.

This chapter is laid out as follows: in section 4.2, I further discuss the synthetic approach, focusing on the use of Sb as a liquid phase sintering aid to facilitate the percolation, as well as additions of Cu as a nucleation aid for the eutectoid transformation. Phase determination of the resulted nanocomposite materials is described in section 4.3. Microstructure control is then discussed in section 4.4, emphasizing self-assembly of DC morphologies in a hierarchical manner. Section 4.5 shows how the Co and P dopants selectively disperse within the heterogeneous microstructure. The temperature-dependent transport properties as a function of the DC phase content, are summarized in section 4.6. In section 4.7, the transport properties and overall figure of merit, ZT, in controlled microstructures, are discussed. Section 4.8 discusses our key finding, that the electron mobility in our structures can be of order 30x superior to comparable material in the literature. This conductivity enhancement leads to a maximum ZT of 0.67, obtained in an optimal sample at 973K (700 ºC), whose overall composition is $((Fe_{0.95}Co_{0.05})_{0.27}Si_{0.73})_{0.94}Ge_{0.06}$ (with 0.5 wt% Cu, 3 at% P and 1 at% Sb of DC phase).

4.2. Experimental details

α-$FeSi_{2+\delta}$ was first prepared by arc-melting elemental Fe (99.99%) and Si (99.999%) pieces at stoichiometric ratio of $(Fe_{0.95}Co_{0.05})_{0.27}Si_{0.73}$ in an argon atmosphere. The as-melt cast was then crushed and combined with elemental Ge (99.999% purity), P(99.9%), Cu (99.99%), and sometimes Sb(99.99%), using vibrational ball milling for 1.5 hour under argon atmosphere. The resulting submicron powder was then sintered by a Spark Plasma Sintering (SPS) apparatus at 820 °C ~ 860 °C for 10 ~ 20 minutes at 60 MPa under argon atmosphere. Densities were measured by the Archimedes' method. Phase identification was performed using X-ray Diffraction (XRD).

Microstructure images and elemental mapping were obtained by Scanning Electron Microscopy (SEM), Energy-dispersive X-ray Spectroscopy (EDS), and Transmission Electron Microscopy (TEM). Three-dimensional microstructural tomography was performed by a dual beam Focused Ion Beam (FIB). The electrical transport, including temperature dependent electrical conductivity and Seebeck coefficient was measured by a ZEM system. Hall measurements were conducted by the Van der Pauw method (3mm×3mm×0.2mm) to obtain carrier concentrations and mobilities. The thermal diffusivities were measured by a Laser Flash apparatus. The specific heat of the composite material was measured by Differential Scanning Calorimetry (DSC). The thermal conductivities were then obtained by the product of the specific heat, thermal diffusivity and density, i.e. $\kappa = C_p \alpha \rho.$ Moreover, in order to gain insights in the Seebeck behaviors of the system, first principle calculations of β-$FeSi_2$ was performed by my colleague Emad Rezaei. The QUANTUM ESPRESSO package[87] was employed to do density-functional theory (DFT) calculations with a norm-conserving pseudopotential with the Perdew-Burke-Ernzerhof exchange-correlation functional[88]. A 8×8×8 Monkhorst-Pack k-point mesh was selected to cover electronic states in first Brillouin zone and kinetic energy cutoff for wave function and for charge density were 70, and 700 Ry, respectively. Crystal structure was relaxed using BFGS quasi-Newton algorithm[89]. Transport properties were evaluated through semi-classical Boltzmann theory as implemented in BoltzTraP code [90].

The nominal chemical compositions, process conditions, phase volume factions, densities and Hall data are summarized in Table 4-1.

Table 4-1

Sample name	Nominal dopant concentrations (as at% of the DC phase)	Cu content (wt%)	SPS process	Nominal volume fraction of resultant phases	Relative density	n (cm^{-3})	μ (cm^2/V s)
P-1	P: 3%	1%	800°C/10min + 860°C/10min	66% β-$FeSi_2$ 34% $Si_{0.75}Ge_{0.25}$	97.1%	1.64×10^{20}	10.1
P-2	P: 4%				97%	1.91×10^{20}	8.8
P-3	P: 5%				97.5%	2.01×10^{20}	8.7
Sb-1	P: 3% & Sb: 1%	0.5%	820 °C/10min		98.2%	1.71×10^{20}	12.1
Sb-2	P: 3% & Sb: 2%				99.1%	2.21×10^{20}	7.8

4.3. Phase determination

The R/T SPS approach circumvents prolonged mechanical alloying or extended post annealing that is typically used to process β-$FeSi_2$-based materials. Instead, I directly SPS the lightly ball-milled mixture of α-$FeSi_{2+\delta}$ (formed by arc melting) and elemental Ge. In order to optimize the thermoelectric properties, selective n-type doping of the constituent β-$FeSi_2$ and DC phases with Co and P/Sb, respectively, needs to be achieved. Cobalt is incorporated in the α-$FeSi_{2+\delta}$ phase in the initial arc-melting process, and is retained in the β-$FeSi_2$ lattice after eutectoid decomposition, substituting on Fe sites,[91] in the subsequent R/T SPS process. This is due to the large solubility of Co (> 10 at%) in both silicide phases[92]. It will be shown later that phosphorus is primarily incorporated in the DC phase.

The initial Si composition is 73 at%, see the Fe-Si binary phase diagram in Fig. 4-1 a). Thus the as-cast material consists of α-Fe(Co)$Si_{2+\delta}$ and a small amount of eutectic Si, as confirmed by the XRD pattern shown in Fig. 4-1 b). Ge, P (Sb) and Cu are then added followed by 1.5 hour ball milling to break down the coarse as-cast structure and to ensure homogeneous intermixing. Since

Co tends to stabilize α-$FeSi_{2+\delta}$ phase against eutectoid decomposition[78], 0.5~1 wt% Cu is added to accelerate the transformation[44].

Figure 4-1 c) shows the XRD patterns of the sintered samples. They all exhibit a two-phase composite of β-$FeSi_2$ – SiGe, with trace amounts of metallic ε-FeSi only in the Sb-free samples, P-1, P-2 and P-3. The low melting temperature of Sb, combined with its extremely low solubility in Si, is thought to promote local melting that facilitates liquid-phase sintering. In addition to avoiding the presence of the ε-phase, samples Sb-1 and Sb-2 possess higher relative densities than those of Sb-free samples despite a lower sintering temperature (Table 4-1). The compositional homogeneity of Ge and P in the DC phase is also improved when Sb is added. The comparisons of backscattered electron images and EDS line-scans are provided in the next session.

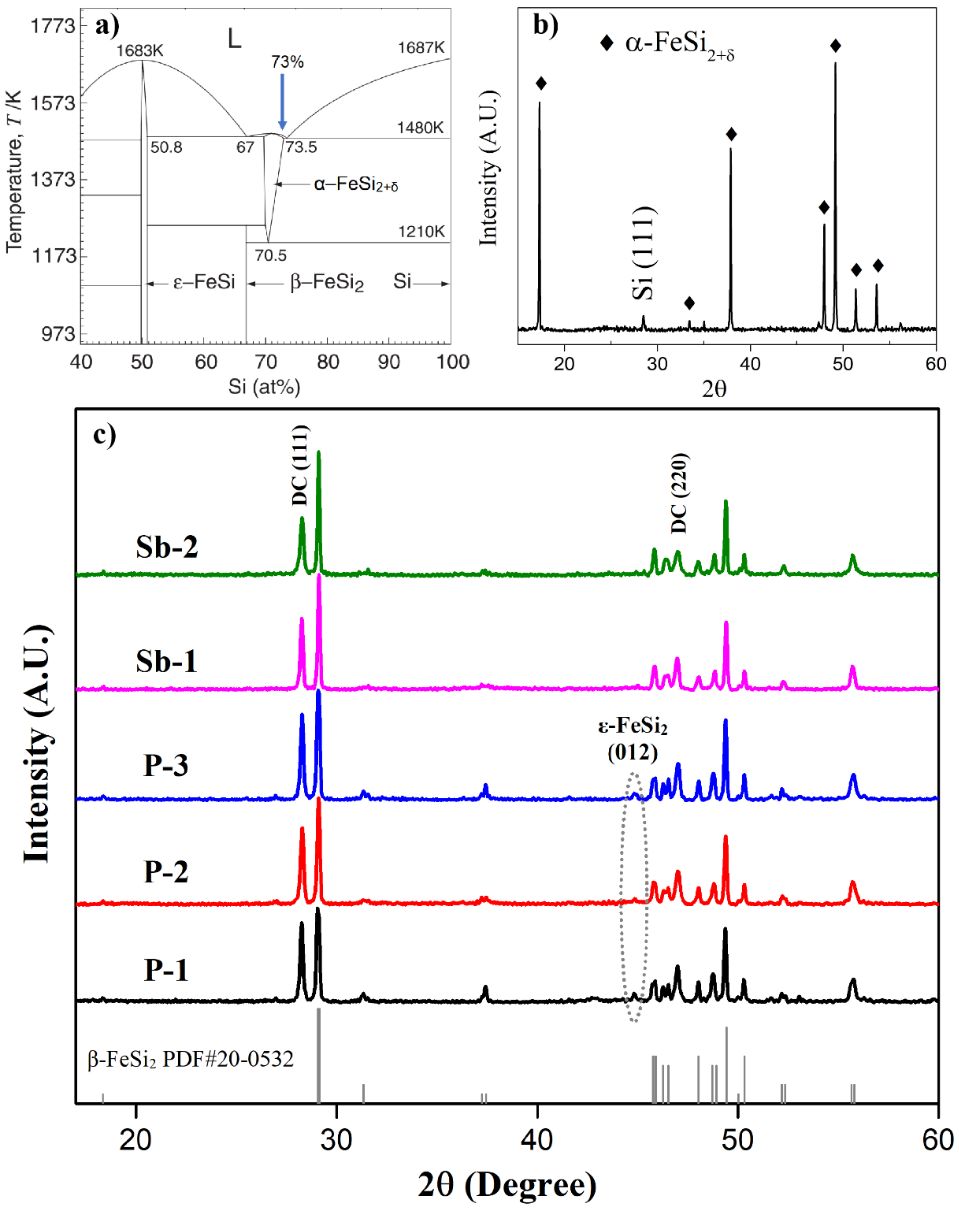

Figure 4-1: a) Fe-Si binary phase diagram; b) XRD pattern of as-melt $(Fe_{0.95}Co_{0.05})_{0.27}Si_{0.73}$ cast; c) XRD patterns of sintered samples

4.4. Microstructure and percolation

The as-cast $(Fe_{0.95}Co_{0.05})_{0.27}Si_{0.73}$ exhibits pro-eutectic α-Fe(Co)$Si_{2+\delta}$ and eutectic α + Si as shown in the SEM image of Fig. 4-2 a), consistent with the Fe-Si phase diagram. After 6 at% Ge and n-type dopant P are introduced as powders with the ball-milled material, held in the SPS at 800°C for 10 minutes and then sintered in at 860 °C for another 10 minutes, about 25 at% Ge is homogeneously distributed in DC phase, according to EDS and backscatter SEM (see Fig. 4-2 c). Ge incorporation is expected to significantly reduce the thermal conductivity by alloy scattering. The embedded DC phase is rather coarse, as the majority of the eutectoid Si rejected during α→ β diffused onto and along the grain boundaries. Reducing the sintering temperature in order to minimize the DC phase coarsening would increase porosity and chemical inhomogeneity, proved by the BSE contrast and the EDS elemental line scan shown in Fig. 4-3, in which sample P-1 sintered at 820 °C suffers from a compositional inhomogeneity despite successfully retaining DC nanoinclusions. However, adding 1 at% Sb (relative to the DC phase composition) aids sintering. Sample Sb-1 is well-sintered at only 820 °C for 10 minutes, with homogeneous Ge incorporation and reduced coarsening that allows formation of eutectoid DC nanoinclusions, see Fig. 4-2 c). The general morphology shown in Fig. 4-2 e) exhibits a hierarchical microstructure with mesoscale DC grains/clusters (1 ~10um) and the nanoscale DC inclusions (10 ~ 100 nm).

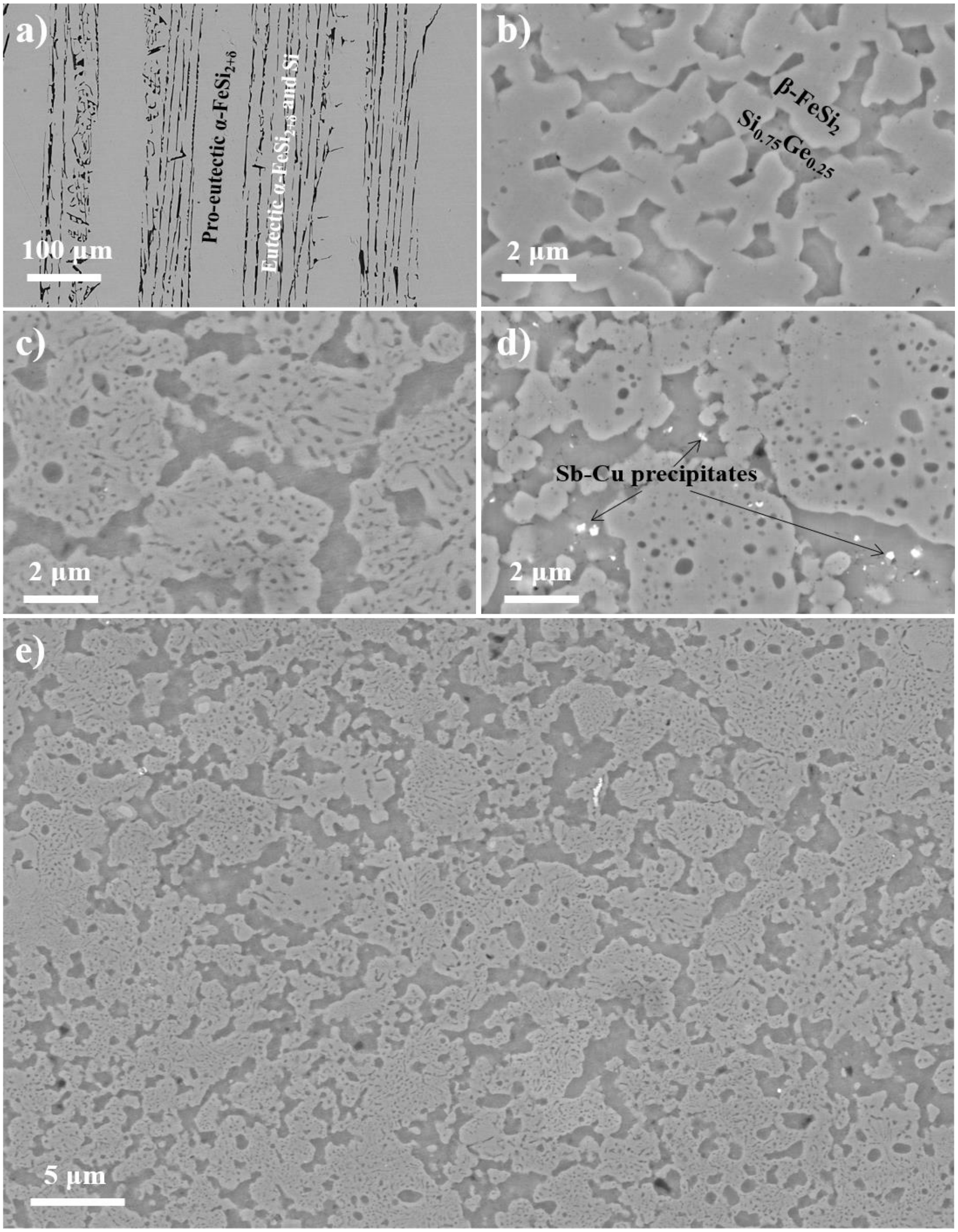

Figure 4-2: Backscatter electron SEM image of a) $(Fe_{0.95}Co_{0.05})_{0.27}Si_{0.73}$ as-c, b) sample P-1, c) sample Sb-1, d) sample Sb-2, and e) lower magnification view of c)

The mesoscale DC phase after SPS likely derives from the eutectic Si present in the initial melt. Ge was then incorporated into this microconstituent during SPS, facilitated by enhanced grain boundary diffusion due to inter-grain joule heating, and liquid phase sintering promoted by low melting point Sb. As a result, the mesoscale DC microconstituent tends to manifest a relatively large aspect ratio instead of being equiaxed. Such morphology is expected to lower the percolation threshold compared with that of random space-filling of spheres. The nanoscale DC inclusions are contributed from the Si nanostructures that result from eutectoid decomposition. Given that Co doped β-FeSi$_2$ – Si nanocomposites still possess rather high thermal conductivity (~7 W m^{-1} K^{-1} at

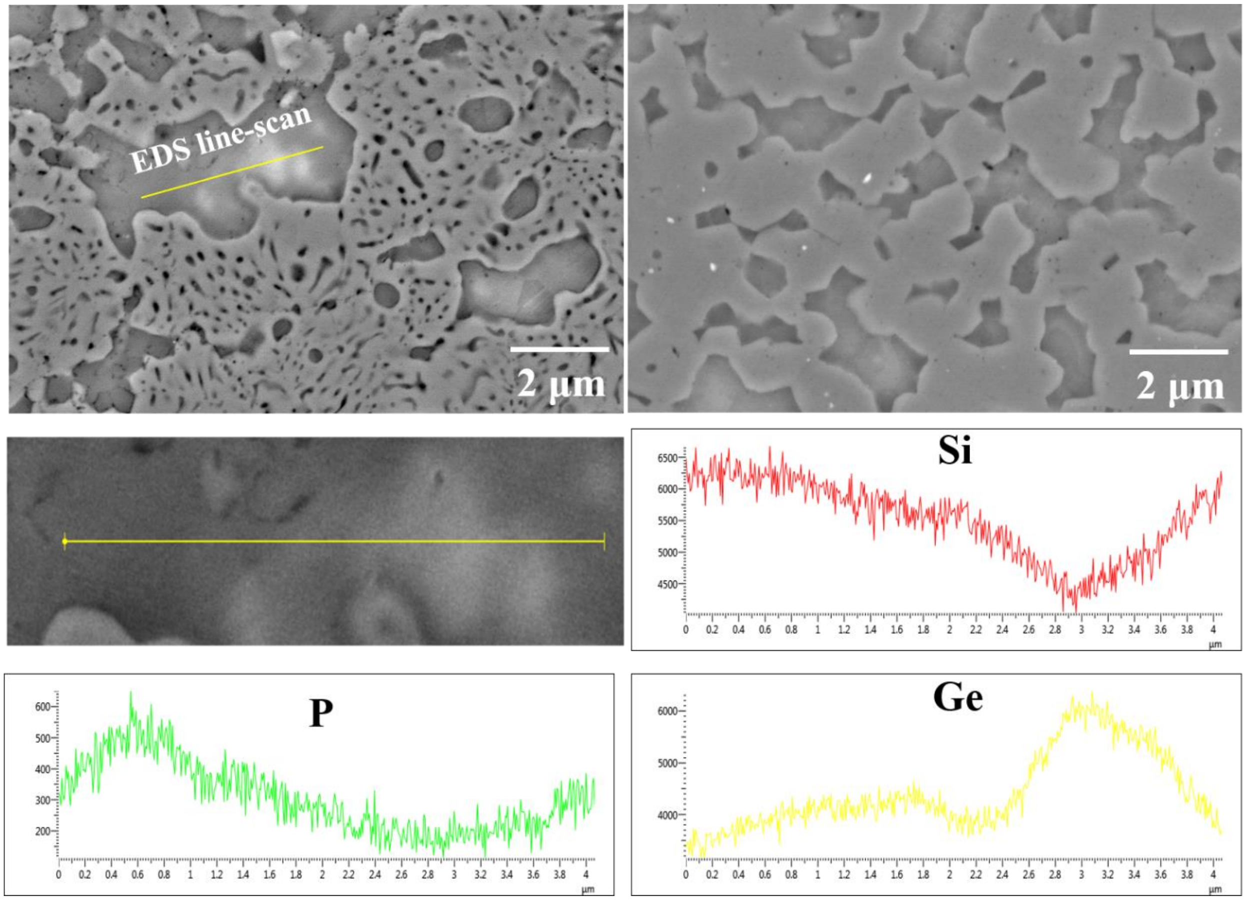

Figure 4-3: Backscatter electron SEM image of sample P-1 sintered at 820 °C (upper left), compared with that sintered at 860 °C (upper right), as well as EDS line scan of the selected area within the SiGe phase showing compositional inhomogeneity

R.T.) despite a large interface density[52,93], while β-$FeSi_2$/SiGe heterointerfaces exhibit much large boundary resistance than that of β-$FeSi_2$/Si[17], it is thus critical to ensure effective Ge incorporation into those DC nanoinclusions. The local elemental mapping will be discussed in the next session. Excess Sb addition (2 at%) results in extensive coarsening in DC phase, as well as metallic Cu-Sb compound formation, shown in Fig. 4-2 d), both of which are expected to deteriorate the power factor. Since Sb tends to further accelerate the eutectoid decomposition thereby less Cu (0.5 wt%) was used in samples containing Sb.

In order to investigate the extent to which the DC phase percolates, dual beam FIB/SEM serial-sectioning was used for 3D tomographic reconstruction. Secondary electron micrographs were taken every 50 nm in sputtered thickness. Figure 4-4 shows that the DC phase is close to the percolation threshold in the β-$FeSi_2$ matrix here, at least within the interrogated volume of

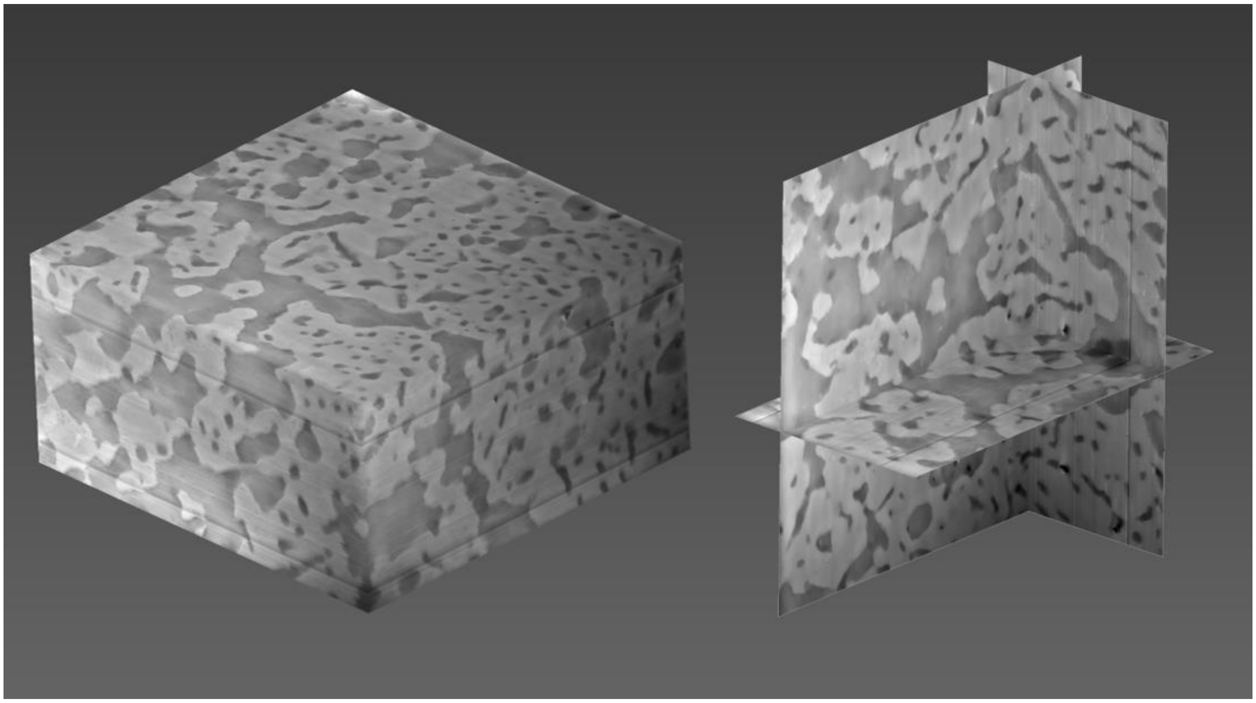

Figure 4-4: 3D tomographic reconstruction (12µm×12µm×5µm) of sample Sb-1 with percolated DC phase in β-$FeSi_2$ phase. The two views are from the same volume, but the right-hand view is rotated to better display key features

12μm×12μm×5μm. A 3D tomography movie was also made, which explicitly shows that the SiGe phase propagating across the whole analyzed volume, further proving the SiGe phase percolation.

Figure 4-5 a) and b) show bright field TEM micrographs of the samples P-1 and Sb-1. The DC inclusions are clearly much finer and better dispersed in the β grain for sample Sb-1. Both samples possess frequent β(100)[011]/2 stacking faults, likely associated with the phase transition from α. Their impact on transport properties should be minor, as these planar defects are subject to only small Si-Fe-Si bond distortion with no change in Fe-Si bond distance[62]. The stacking faults and a typical DC nanoinclusion of sample Sb-1 can be seen in the high-resolution micrograph in Fig. 4-5 d). The HAADF-STEM image (Fig. 4-5 c)) also shows the distribution of the nanoscale DC inclusions. It is observed that Sb and Cu tend to accumulate on β-$FeSi_2$/DC interfaces, consistent with the dominant grain boundary diffusion mechanism for the process discussed earlier. Figure 4-5 e) shows that the β-$FeSi_2$ grains have a relatively small size of 1~ 2 of microns, while Figure 4-5 f) shows the inter-grain SiGe microconstituent, which effectively bonds multiple β-$FeSi_2$ grains due to liquid phase sintering assisted by Sb. This may improve the overall carrier mobility due to better inter-grain bonding and/or phase percolation. Transport properties will be discussed shortly.

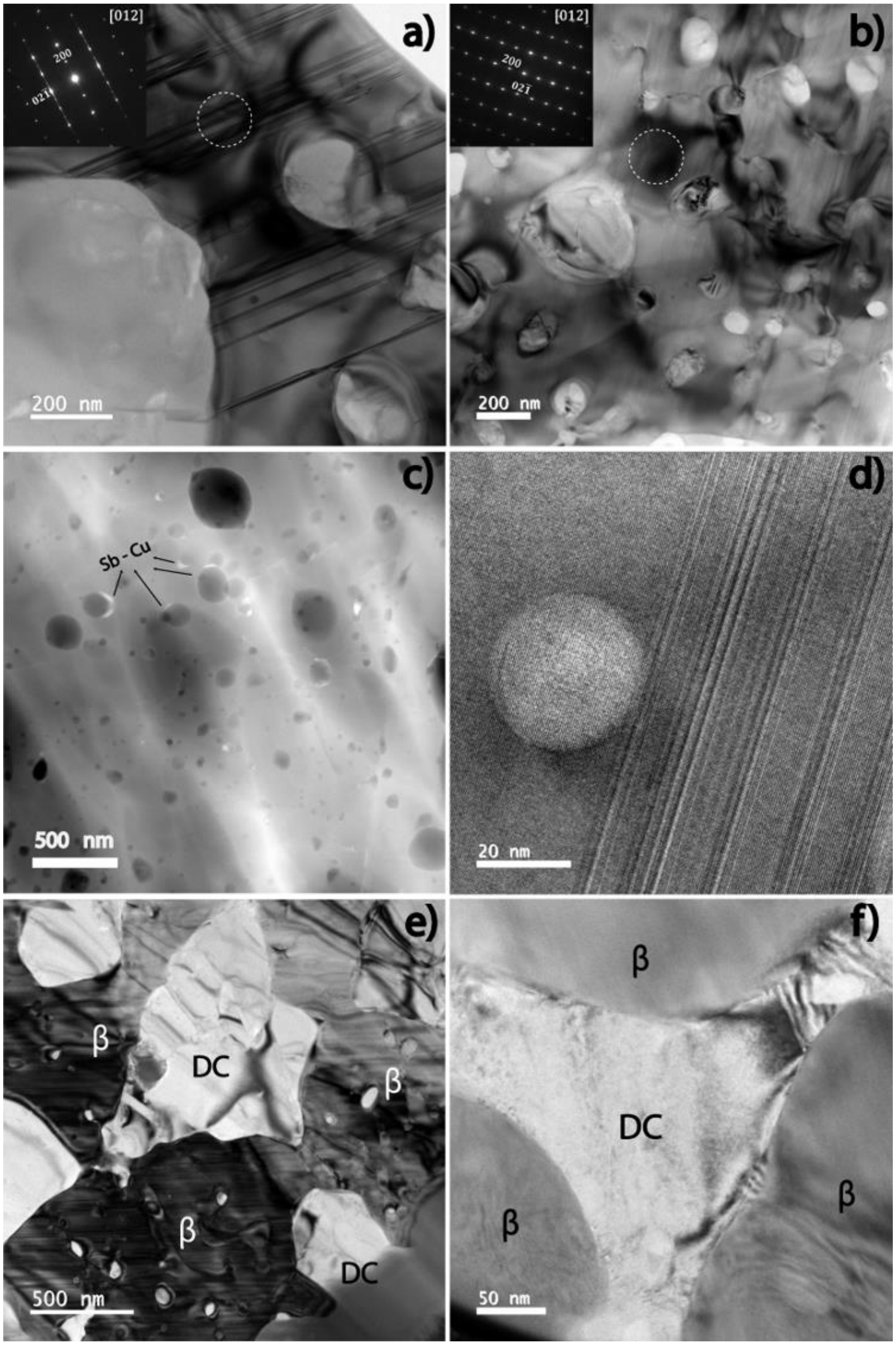

Figure 4- 5: Bright field TEM images of a) sample P-1 and b) sample Sb-1 with selected area diffraction patterns inset; c) HAADF-STEM image and d) high-res image of sample Sb-1. In c) the dark gray particles are DC, and Sb-Cu can often be observed at the β/DC interface. In d), the spheroid is a DC nanoinclusion. e) Bright field TEM showing typical grain sizes in sample Sb-1; f) inter-grain (β-$FeSi_2$) DC phase due to liquid phase sintering.

4.5. Spatial disposition of dopants and hall measurements

Phosphorus incorporation in the DC phase is critical for electrical transport. Since both the matrix and inclusions are semiconducting phases, electron transport across the heterointerface is important and would be enhanced if both phases are heavily doped to better align the conduction band edges. Ideally, a large density of DC nanoinclusions would simultaneously disrupt thermal transport without degrading electron transport. Figure 4-6 shows the HAADF-STEM image of a β-$FeSi_2$ grain embedded with DC nanoinclusions. The corresponding EDS elemental maps show that Ge and P were successfully incorporated into the inclusions. While fortuitous, this is not a trivial result to understand. The diffusion kinetics of Si in β-$FeSi_2$ are apparently are slow enough to prevent the DC inclusions from coarsening, and yet Ge and P diffusion in β-$FeSi_2$ on the same lengthscales is sufficiently rapid for alloying and doping of the DC inclusions to occur. There are several possible reasons for this that our data will not be able to distinguish between, including: intermixing has a larger driving force (entropy of mixing) than coarsening (capillarity); Ge and P

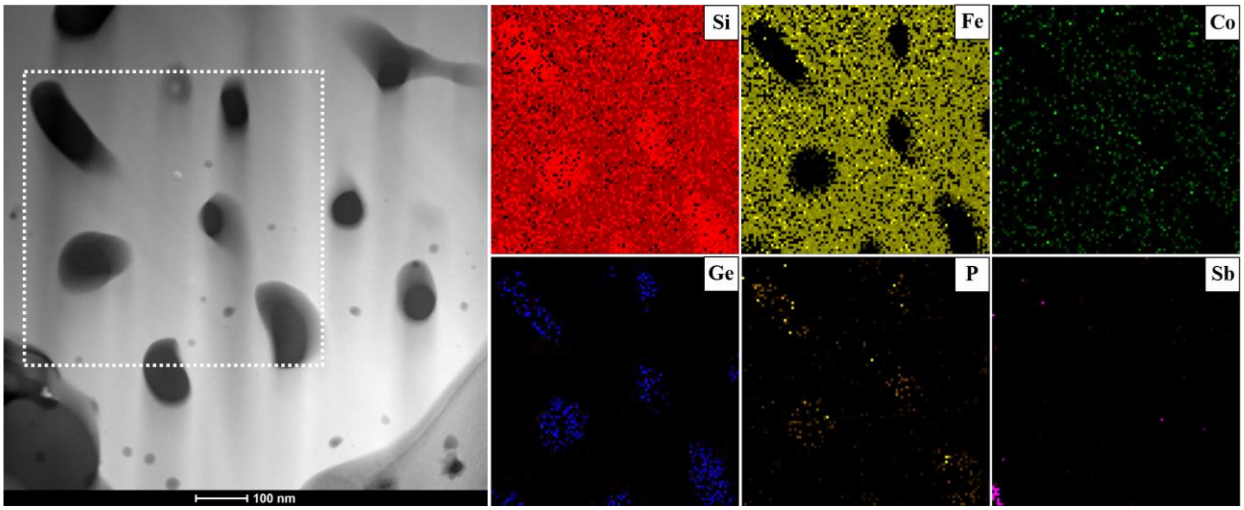

Figure 4-6: HAADF-STEM image of a typical β-$FeSi_2$ grain with DC nanoinclusions, and its (dashed square) corresponding EDS elemental mapping. It is clear that Co preferentially dopes the $FeSi_2$ matrix, while P dopes the diamond cubic inclusions.

may simply have smaller activation energies for diffusion in β than Si; or, coarsening may be detachment limited rather than diffusion limited. In any event, the relatively small grain size of β-$FeSi_2$ is important to facilitating the alloying and doping of the DC nanoinclusions.

The phosphorus disposition indicates that P thermodynamically favors incorporation in the DC phase instead of substituting the Si-site of β-$FeSi_2$. Conversely, Co prefers to substitute Fe sites in β-$FeSi_2$ via eutectoid transformation. Therefore, Co and P are selectively and homogeneously incorporated in β-$FeSi_2$ and SiGe, respectively, as n-type dopants under a single SPS process. Antimony tends to accumulate at the heterophase boundaries (β-$FeSi_2$/DC), as indicated by the Sb-rich region shown at the bottom left corner of the EDS mapping, and in the TEM micrograph of Fig. 4-5 c). Despite being an ineffective electron donor due to its limited solubility in DC, it nonetheless plays a crucial role as a sintering aid promoting inter-grain metallurgical junctions that improve electron mobility by suppressing void formation.

Hall measurements were performed using Van der Pauw method to obtain the overall carrier concentrations of all samples. Figure 4-7 shows the Hall resistivity ρ_{xy} vs. applied magnetic field B. The slope of each linearly fitted line represents the Hall coefficient, by which the overall carrier concentration can then be calculated. It can be observed that in sample Sb-1, P-2 and Sb-2, the slopes increase gradually, meaning increased electron densities. Mobility can then be derived by measuring the resistivity (sheet resistance). The Hall data of all samples studied is provided in Table 4-1.

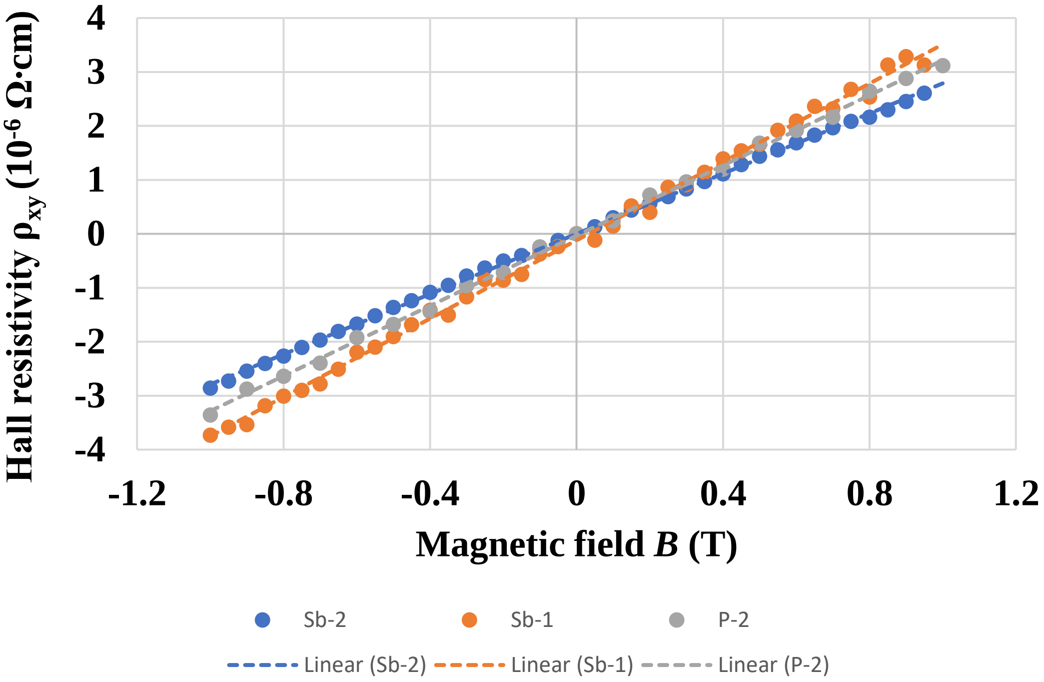

Figure 4-7: Hall resistivity ρ_{xy} versus magnetic field *B* of sample Sb-1, P-2 and Sb-2. Hall coefficient is expressed by the slope of the linear fit.

4.6. Effect of DC phase fraction on Electrical Transport

In order to investigate potential percolation effects on the electronic transport, different DC volume fractions were obtained by varying the Si composition in the initial $(Fe_{0.95}Co_{0.05})_{1-x}Si_x$ melt (x = 70.6%, 71.5%, 72.5%, 73% for this study). According to the phase diagram in Fig. 4-1 a), when x increases, increased volume fractions of eutectoid Si (for $x \leq 71.5\%$), or eutectic Si (for $x > 71.5\%$), will be obtained. Subsequently, Ge and P dopants were added by ball milling. The P amount was adjusted to keep a consistent nominal doping level in the DC phase. After the full process, we obtained DC volume fractions of 24%, 28%, 31% and 34%. The specifications of these samples are listed in Table 4-2. Figure 4-8 a) shows there is a consistent enhancement of σ across the entire temperature range with increasing volume fraction of DC. We attribute this to the increasing extent of percolation of DC phase, which gradually improves the composite's overall mobility. In addition, electrons can transport across β-$FeSi_2$ and DC phases fairly easily due to heavy n-type doping of both phases, minimizing the energy barrier across the heterointerface. I defer further justification until later, when the optimized samples

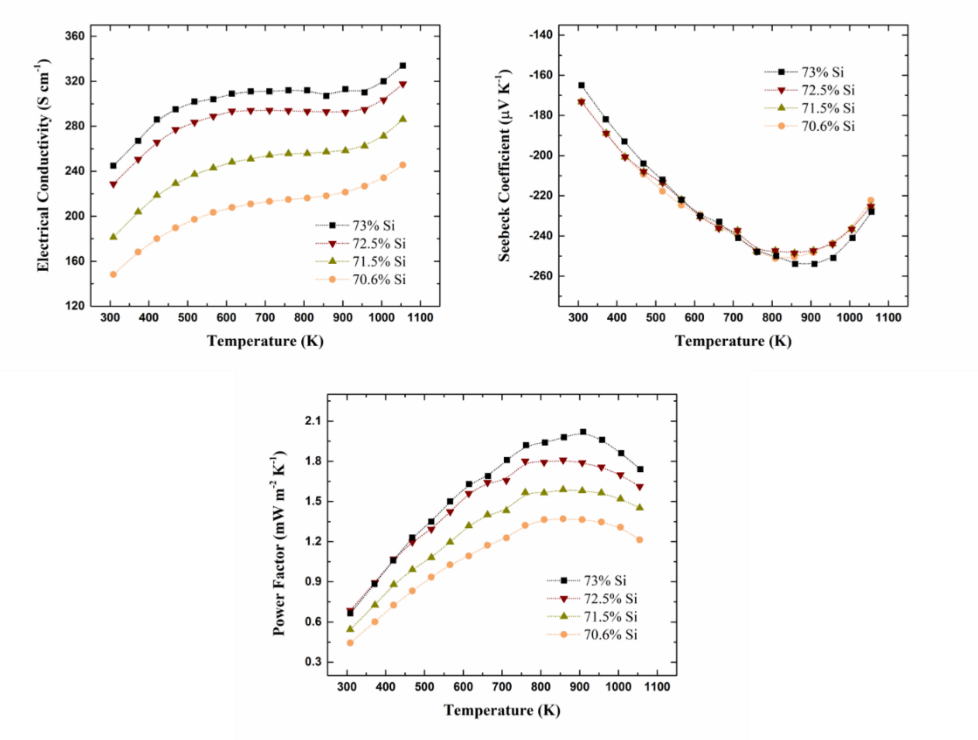

Figure 4-8: Temperature dependence of the electrical conductivity, Seebeck coefficient and power factor of the samples where DC volume fractions were varied.

Table 4-1

Nominal Composition $[(Fe_{0.95}Co_{0.05})_{1-x}Si_x]_{1-y}Ge_y$	P addition (at% of DC phase)	Cu additive (wt%)	SPS process	Nominal volume fraction of resultant phases & SiGe compositions	Relative density
x= 0.706; y=0.05	3%	1%	800°C/10mins + 860°C/10mins	76% β-$FeSi_2$ + 24% $Si_{0.7}Ge_{0.3}$	98%
x= 0.715; y=0.05				72% β-$FeSi_2$ + 28% $Si_{0.74}Ge_{0.26}$	97.4%
x= 0.725; y=0.05				69% β-$FeSi_2$ + 31% $Si_{0.77}Ge_{0.23}$	97.%
x= 0.73; y=0.06				66% β-$FeSi_2$ + 34% $Si_{0.75}Ge_{0.25}$	97.1%

Interestingly, despite the enhancement of σ with the DC volume fraction, the Seebeck coefficients of these samples vary very little with DC volume fraction, as shown in Fig. 4-8 b). This could imply similar Seebeck behaviors associated with the β-$FeSi_2$ and DC phases. A $Si_{80}Ge_{20}$ reference[94] which possess a composition and doping level close to that of the DC phase in our composite does show a similar temperature dependence of Seebeck coefficient. The generic behavior of *S(T)*, increasing in magnitude to around 900 K, followed by a decrease at higher temperatures, has been seen before in Co-doped β-$FeSi_2$ but is not well understood[95]. On the other hand, Birkholtz and Schelm found a very different temperature dependence of *S(T)* for this system. To explore these behaviors, we performed first principles calculations of β-$FeSi_2$ to evaluate *S(T)*. The crystal structure was relaxed using the BFGS quasi-Newton algorithm[89], and comparison of lattice constants is provided in Table 4-3. Figure 4-9 a) shows the band structure of β-$FeSi_2$ along high-symmetry k-points. An indirect bandgap of 0.76 eV is found, which agrees with experimental measurements using photothermal deflection spectroscopy[96]. The corresponding DOS of electrons is also shown. In order to calculate *S(T)*, we assumed dopants are ionized according to $n = n_o \exp(\frac{E_a}{2k_BT})$, where E_a is the activation energy, estimated to be 30 meV from to the slope of the $log\sigma$ vs. $1/T$ plot at lower temperature range (300K-500K). *S(T)* is then calculated using Boltztrap code[90] by a constant relaxation time approximation (CRTA), shown in Fig. 4-9 b), with its corresponding carrier concentration curve. As temperature increases, despite an increase in the carrier concentration, the corresponding chemical potential shifts toward the middle of the gap, resulting in the increase of Seebeck coefficient with respect to temperature. When temperature is > 900K, in addition to the shift of chemical potential, the Fermi window becomes large enough that the holes in the valance band start to contribute to the transport, hence lowing the Seebeck coefficient.

The DFT-predicted *S(T)* of β-$FeSi_2$ is compared with the experimental *S(T)* of sample P-1 and $Si_{80}Ge_{20}$ reference[94] in Fig. 4-9 b), which both show very similar temperature dependence. Therefore, we suggest that the relative insensitivity of *S* to the volume fraction of the DC phase is fortuitous, but sensible. Close agreement is obtained between calculation and our experimental data, although it requires a 2× larger carrier concentration to produce this agreement. In addition, the calculated maximum Seebeck coefficient shifts towards higher temperature by ~100K compared with the experimental data. This can be attributed to the fact that a constant relaxation time versus energy was used in the calculation, and the Co impurity levels are not taken into account, which in reality bring in additional states and narrows the bandgap.

Table 4-2

	Our calculation	Experimental values [97]	DFT calculation
a (^{0}A)	9.846	9.863	9.83
b (^{0}A)	7.778	7.791	7.81
c (^{0}A)	7.810	7.833	7.85

Finally, we note that further increasing Si composition (>73%) in the initial melt does not improve thermoelectric performance, as additional coarse Si eutectic microconstituent will effectively replace nanoscale eutectoid Si due to lower volume fraction of the α phase obtained upon solidification. This would tend to deleteriously increase the thermal conductivity. Therefore, we fixed our composition at $(Fe_{0.95}Co_{0.05})_{0.23}Si_{0.73}$ for the initial cast material for subsequent optimization of ZT. This is the base composition used for all the samples in Table 1, whose thermoelectric properties are discussed next.

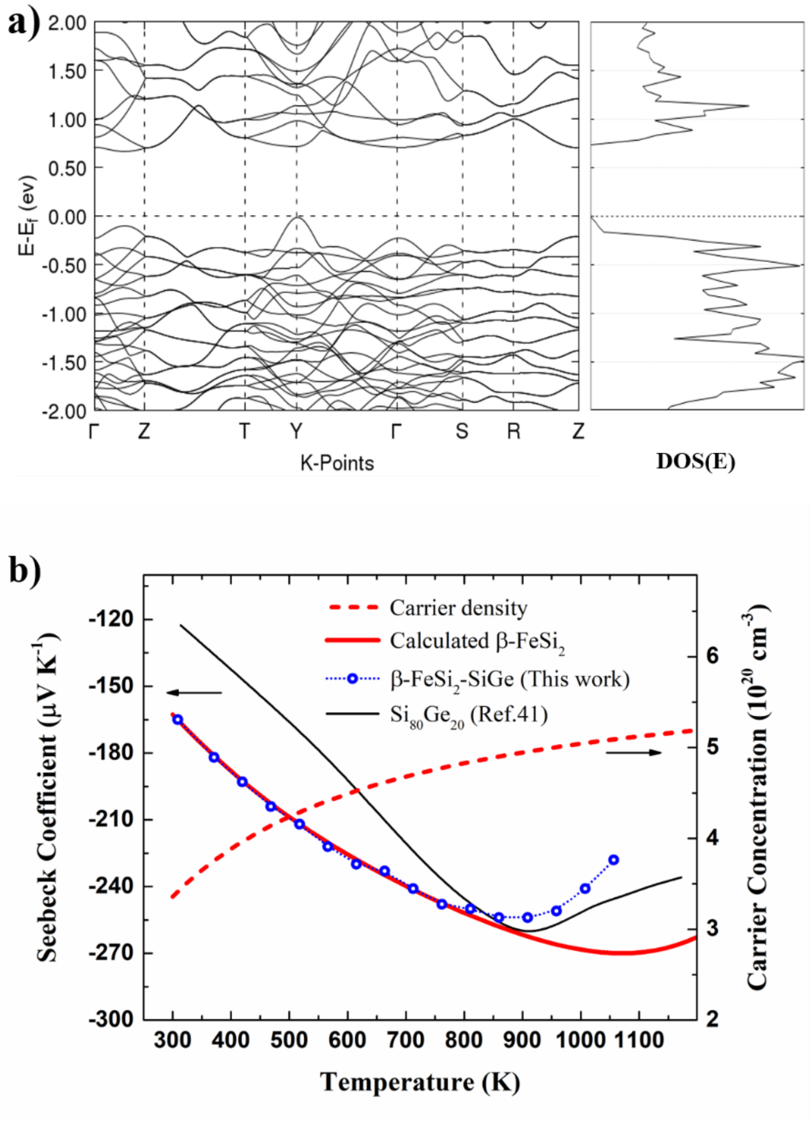

Figure 4-9: a) The calculated band structure and DOS of β-FeSi$_2$; b) comparison of calculated Seebeck coefficient of β-FeSi$_2$ with a Si$_{80}$Ge$_{20}$ reference and the data for the β-FeSi$_2$ – SiGe nanocomposite sample P-1. The carrier density used in the calculation is also shown

4.7. Optimization of thermoelectric properties

Figure 4-10 a) shows the temperature-dependent specific heat C_p of sample Sb-1. Since all samples listed in Table 1 have identical volume fractions of the β-$FeSi_2$ and $Si_{0.75}Ge_{0.25}$ phases, it is reasonable to use this C_p curve to calculate the thermal conductivities of the other samples; the results are shown in Fig. 4-10 b). Several trends are apparent. First, the thermal conductivities of sample P-1 ~ P-3 increase with P content, ostensibly due to coarsening of the DC phase with excess phosphorus, along with a small electronic effect from the higher carrier concentration. Sample Sb-1 has significantly reduced thermal conductivity, due to the presence of numerous nanoscale DC inclusions, cf. Fig. 4-2. However, sample Sb-2 has higher κ than Sb-1 as additional Sb increases the DC length scales. In order to elucidate the effect of nanostructuring on the lattice thermal conductivity (κ_{lat}), the electronic component of thermal conductivity (κ_{ele}) is estimated by the Wiedemann-Franz law, $\kappa_{ele} = L\sigma T$. L is the Lorenz number calculated by an empirical formula $L = 1.5\_exp(-\frac{|S|}{116})$, where L is in 10^{-8} WΩ/K^2 and S is in μV/K[4]. The thermal conductivity by the lattice and bipolar contributions determined by subtracting out the estimated electronic contributions, is shown in Fig. 4-10 d). All samples present similar trend of temperature dependence. The increase of κ_{lat} from 300 K ~ 473 K reflects the rapid increase in C_p near room temperature. Then κ_{lat} gradually decreases in the intermediate temperature range, in which κ_{lat} also shows a linear relationship versus 1/T, indicating a dominant 3-phonon process. In the intermediate temperature range, the electronic contribution to the thermal conductivity is about 10% of the total. The increase of the thermal conductivities at ~900K is attributed to bipolar effects due to thermally-generated carriers, consistent with the observed increase in σ and corresponding drop in S in the same temperature range, as shown in Fig. 4-11. The thermal conductivity of sample Sb-1 is greatly reduced due to phonon scattering, established by the microstructure, which has been optimized in terms of the length scales, phase morphologies/volume fractions, and Ge content.

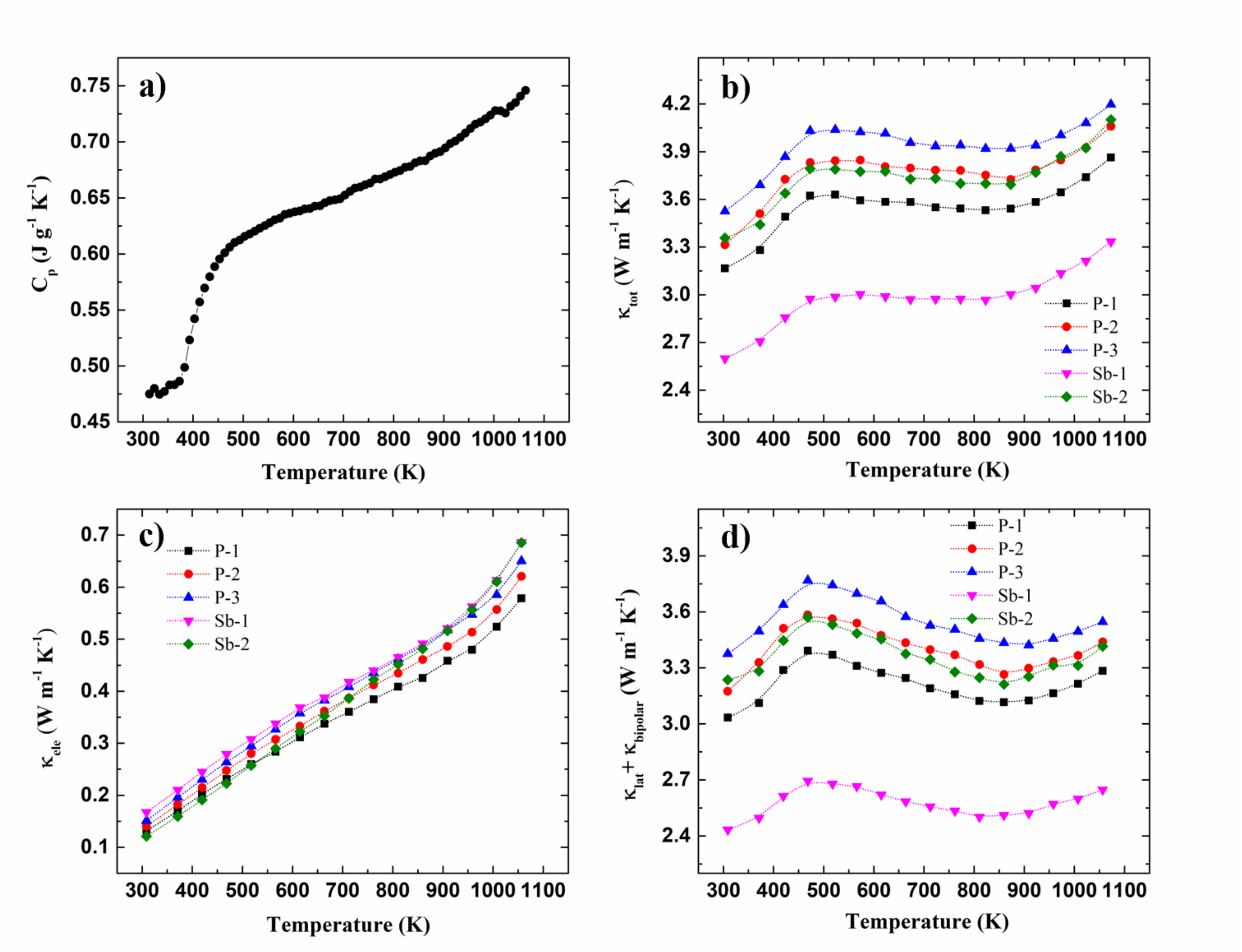

Figure 4-10: a) The experimental C_p vs. temperature of sample Sb-1; b) the measured thermal conductivities, c) the estimated electronic thermal conductivities, and d) the lattice + bipolar contributions to the thermal conductivities.

Figure 4-11 a) shows the temperature dependence of the electrical conductivity. Interestingly, despite having a high density of SiGe nanoinclusions that effectively reduce κ, sample Sb-1 also possesses higher electrical conductivity than other samples. Figure 4-11 b) shows the Seebeck coefficients, and the power factor is shown in Fig. 4-11 c). Finally, the thermoelectric figure of merit, ZT, is shown in Fig. 4-11 d). While most of the samples from Table 1 have a maximum in ZT of about 0.45 – 0.5 at 700 ºC, optimized sample Sb-1 stands out with ZT_{max} = 0.67 at 700 ºC.

This is primarily the result of the Sb-1 simultaneously having the lowest thermal conductivity and highest power factor amongst the comparison group.

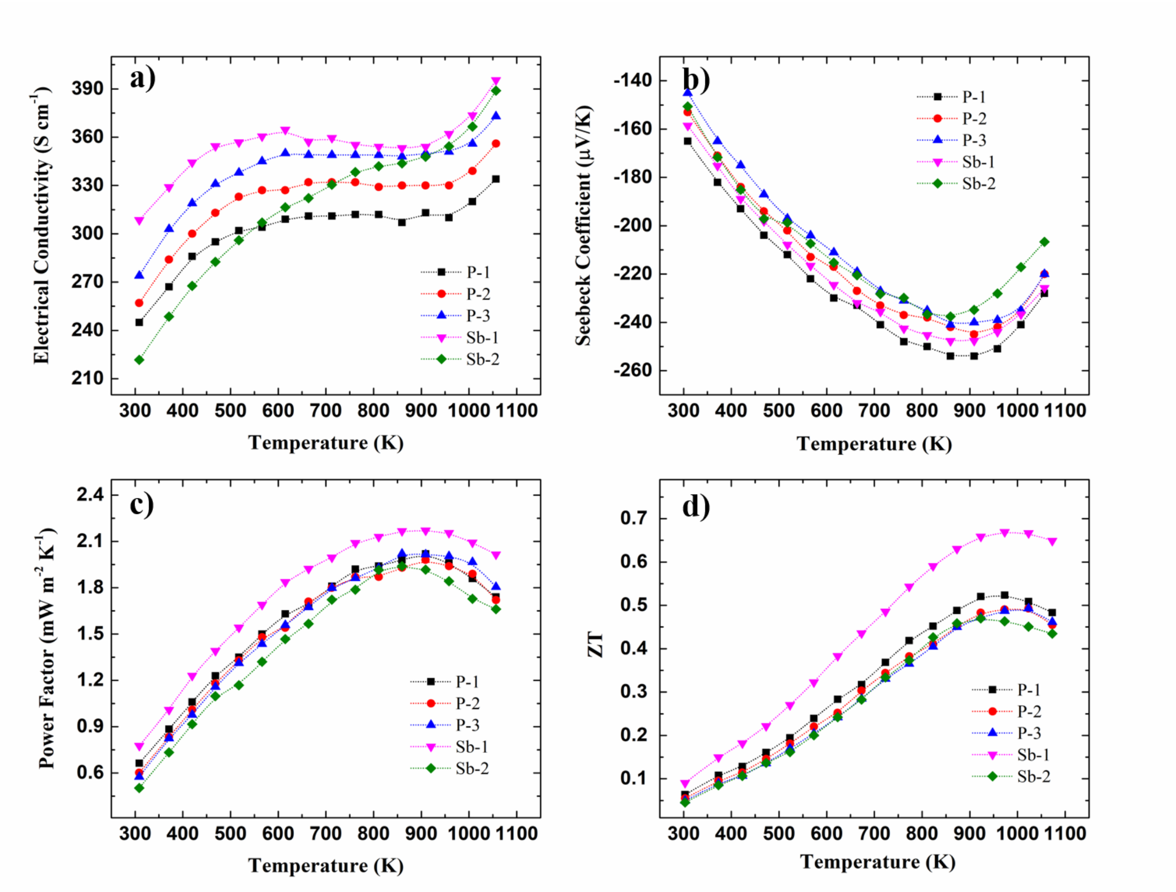

Figure 4- 11: a) Thermoelectric transport properties of sample P-1, P-2, P-3, Sb-1, Sb-2

Similar performance was achieved by Mohebali, et al., who obtained ZT$_{max}$ = 0.54 at 650 ºC in material listed as $(FeSi_2)_{0.75}(Si_{0.8}Ge_{0.2})_{0.25}$, also with Co and P doping as used here. Comparing their transport data against ours indicates that the somewhat larger ZT obtained herein results from sample Sb-1 having reduced thermal conductivity and improved electrical conductivity, compensating a lower Seebeck coefficient. Since little microstructural data was reported by Mohebali, et al., it is difficult to assess the detailed origins of these differences. However, the increased Ge content in the DC phase and the larger volume fraction of DC, leading to phase percolation, likely play a significant role in enhancing electrical conductivity, while the retained nanoscale inclusions decreasing thermal conductivity. From a processing standpoint, the R/T SPS process used herein reduces the sintering temperature by nearly 300 ºC, and the overall process time by at least 50 times.

4.8. Origins of enhanced electron mobility

According to Table 4-1, all the samples have room temperature electron Hall mobilities in the range 8~12 $cm^2/V \cdot s$, with sample Sb-1 having the highest value in this range. It is useful to place this range in perspective. For β-$FeSi_2$ epitaxial thin films with low autodoping, electron mobility can approach 1000 $cm^2/V \cdot s$[98]. On the other hand, in bulk β-$FeSi_2$ crystals that are Co-doped with carrier concentrations of order 1×10^{19} cm^{-3}, μ_e only ranges up to about 6 $cm^2/V \cdot s$[99]. Finally, for powder-processed β-$FeSi_2$ with similar Co doping levels to ours, typical mobilities are even lower, about 0.4 $cm^2/V \cdot s$, both in a eutectoid-based material[50], and in a single phase material[86]. Hence, we obtained electron mobilities in a heterogeneous nanocomposite of β-$Fe(Co)Si_2$ + SiGe that surpass those of Co-doped monocrystals of β, even though our carrier concentrations are 20× larger than in Brehme, et al[99].

We nominally attribute this result to percolation of the diamond cubic phase, and assert that percolation tends to favor parallel conduction paths in the phases. For a *compact* second phase in a matrix, the phase resistances are in series, and the effective conductivity is dominated by the lowest conductivity phase, $\sigma_{eff} \sim \sigma_\beta$. If we assume both phases have similar carrier concentrations, then $\mu_{eff} \sim \mu_\beta$, where $\mu_\beta \sim 0.5$ $cm^2/V \cdot s$ and $\mu_{SiGe} \sim 50$ $cm^2/V \cdot s$[100]. On the other hand, if conduction is primarily in parallel, then following similar logic, $\mu_{eff} \sim 0.34\mu_{SiGe} = 17$ cm^2/V-s, where 0.34 is the volume fraction of the DC phase. This is comparable to the mobility values observed in Table 4-1.

The assertion that percolation promotes parallel conduction is non-trivial. The percolated DC phase is clearly tortuous. As mentioned earlier, the conduction band edge of β-$FeSi_2$ is expected to be around 200 meV *lower* than that of $Si_{0.75}Ge_{0.25}$. While energy barrier will be reduced by heavy doping in each phase, there is still likely a retained offset favoring electron transfer out of the SiGe. Nonetheless, we can anticipate that charge transfer is not excessive. Parallel conduction will be more likely if the mean free path for electrons in the percolated DC is significantly smaller than the small dimension of the DC "filaments", which are of order 200-500 nm according to Figs. 3 and 4. This avoids facile ballistic transit of electrons across regions of the percolation network that are misaligned with respect to the applied electric field.

Any alternative explanation to percolation and parallel conduction would require that the β-$FeSi_2$ matrix itself have mobilities in the range of 10 $cm^2/V{\cdot}s$. This is larger even than single crystal samples with 10× lower carrier concentration[99]. For Co doping levels and carrier concentrations in the range used here, the temperature dependence of the electron conduction is usually attributed to small polaron conduction associated with local lattice deformation around the dopants, such that $\mu_e < 1$ $cm^2/V{\cdot}s$[101,102]. Values well in excess of this have been attributed to band conduction rather than thermally active hopping, occurring primarily at lower carrier and dopant concentrations[98,99]. In order for the β-matrix in our samples to have mobilities in this range would suggest that we have essentially reduced the activation energy to near zero. The incorporation of Ge and P in the β-$FeSi_2$ might locally reduce lattice distortions due to Co dopants that could fortuitously produce such a result. However, our XRD and EDS data suggest that such incorporation is at levels well below that of Co, so it seems an unlikely mechanism. Hence we favor the percolation concept as the primary means for the observed mobility enhancement in our composite material.

4.9. Summary

An eco-friendly β-$FeSi_2$ – SiGe nanocomposite was synthesized via React/Transform Spark Plasma Sintering, introduced in Chapter 3, with significantly reduced process time and thermal budget compared to typical powder process routes. This work combines the nature of SPS processing to control and exploit phase transformations (eutectic/eutectoid decomposition) in order to tailor the microstructure and thermoelectric transport. We obtained a hierarchical structure with a mesoscale, percolated DC phase coexisting with nanoscale DC inclusions in the β-$FeSi_2$ matrix, along with selective doping of both constituent phases, that to a great extent decouples the thermal and electrical transport. An overall electron mobility at room temperature as high as 12 $cm^2/V\cdot s$, which is much higher than usually observed in this system for thermoelectric materials produced by powder routes, is suggested to be the result of parallel conduction paths in the percolated DC phase. An improved ZT of ~0.67 at 973K, with an average ZT of ~0.65 at a broad temperature range from 823K to 1073K was achieved in the β-$FeSi_2$ – SiGe nanocomposite. Both the material system and the methodology show promise in developing economic thermoelectric materials for potential industrial scale application.

Chapter 5: Holey Si Hybrid Device for Thermoelectric Applications

Si-based thin film thermoelectric materials, compatible with the well-stablished semiconductor process technology, give promise of a broad device applications, such as thermoelectric sensors integrated in Micro-Electro-Mechanical Systems (MEMS)[103], human energy harvesting (wearable thermoelectrics)[104], power generation compatible with CMOS fabrication[105], etc. If a favorable efficiency (ZT performance) can be achieved, Si based devices can be used for emerging but pressing application scenarios, such as on-chip thermal management[106], and power generation for wearable electronics and IoT (Internet of Things) nodes[107].

In section 5.1, I will demonstrate a doped (by boron implantation) holey Si device with a nanopatterned square lattice of holes, and study its thermoelectric transport properties. In section 5.2, I will investigate the charge transfer mechanism of the F_4TCNQ – Si interface, and validate the transfer doping effect by studying the thermoelectric transport properties of the hybrid device. The set of control experiments will demonstrate the feasibility of fabricating organic-holey Si hybrid device for thermoelectric applications, in which the thermal and electrical transport can be optimized by nanostructuring and transfer doping.

5.1. Holey Si Device and the Thermoelectric Transport Properties

5.1.1. Rationales and State of Art

Pristine bulk Si has relatively large power factor. The power factor times temperature in silicon is about 0.6 W/mK at room temperatures and 4.54 W/mK at 920K[108]. Despite its large power factor, silicon is not a good thermoelectric materials due to its high thermal conductivity (~150 W/m K at 300 ºC) resulting in a very low ZT of 0.01 at room temperature[109]. In the context of low-dimensional Si for device applications, the overarching goal is to reduce thermal conductivity while preserve electrical transport, which is referred as “phonon glass, electron crystal”. According to the solution of the phonon Boltzmann transport equation (BTE):

$$\kappa(T) = \sum_{\lambda} \int C_{v,\omega}(T) v_{\omega}^{2} \tau_{\omega}(T) d\omega = \sum_{\lambda} \int \hbar\omega \frac{dn}{dT} v^{2} \tau_{\omega}(T) d\omega \qquad 5\text{-}1$$

where λ is the band index (mode index), ω is the phonon frequency, $C_{v,\omega}$ is the mode specific heat, υ is the group velocity component in the direction of propagation, and τ_{ω} is the phonon relaxation time. Thermal conductivity suppression can be realized by: 1. introducing various scattering processes to reduce the relaxation time (or MFP) of phonons; and/or 2. modifying phonon dispersion relations, which impacts the DOS of phonon, group velocities, and anharmonic scattering processes.

Silicon is known to possess a relatively long phonon MFPs. According to both theoretical[110] and experimental studies[111], ~90% of its thermal conductivity is contributed by phonon MFPs > 50nm, and ~40% by phonon MFPs > 1μm. Meanwhile, the MFPs of electron are typically sub-nanometer in heavily doped silicon. Therefore, if the average size of the scattering centers, such as nanostructured features, lies in between their respective characteristic length scales, κ can be effectively suppressed while σ is to a large extent preserved, resulting an improved ZT. Nanoparticle scattering is effective in suppression of the thermal conductivity of large MFP phonons which are usually low energy. Alloy scattering (mass-mismatch) has been proven effective in lowering the thermal conductivity significantly by scattering small wavelength (high frequency, high energy) phonons. Combining alloy scattering and nanoparticle scattering is an effective method to suppress the thermal conductivity of semiconducting materials.

As Ge forms complete solid solution with Si, it can be easily co-deposited with Si to grow a SiGe alloy film, in which the thermal conductivity is greatly suppressed due to alloying scattering. It is shown that only 5% addition of Ge, is enough to lower the thermal conductivity of nanostructured silicon to 5W/mK. A ZT value of 0.95 at high temperatures is reported for Si95Ge5 nanostructured sample which is due to effective lowering of thermal conductivity.[108]

In addition, carefully manipulating the thermodynamic and kinetic parameters for the growth may lead to ordered SiGe phase, resulting in a larger unit cell and a reduced Brillouin zone, and thereby increased umklamp scattering. Meanwhile, electrical transport is expected to improve due to ordered atomic potentials[112][113]. On the other hand, Si/(Si)Ge superstructures can also be obtained by epitaxial growth, and the periodicity of the superstructures would modify the phonon band structures. While boundary scattering of phonons suppresses the thermal conductivity, electron transport can largely be maintained due to structural periodicity and coherent interface. Examples are Si/(Si)Ge superlattice [114][115][116][117] and Si/(Si)Ge quantum dot (QD) crystals[118][119]. In both cases, the length scales of the superstructures, such as the superlattice spacing or QD spacing, can be tuned by deposition or patterning parameters.

For single-phase Si materials, the thermal conductivity can be suppressed by introducing boundary/surface scattering according to Casimir limit, that is, the dimensions (diameter or thickness) act as a cutoff limit for phonon MFPs in Si. Near 100-fold suppression in lattice thermal conductivity was found in Si nanowires (SiNWs), resulting in a great enhancement in ZT up to 0.4 - 0.6 at room temperature [120][121]. Meanwhile, quantized electronic density of states in 1D SiNW possesses a large asymmetry, which is expected to enhance Seebeck coefficient if the chemical potential is carefully manipulated. However, synthesis of uniform, high density arrays of SiNWs is extremely non-trivial and is not currently feasible for scalable production of TE modules. The other alternative is to morphologically modify Si thin films to obtain nanopatterned holey Si [122][123] or sometimes referred as Si nanomesh [124]. The structure is more robust compared to n SiNWs and can be fabricated by scalable processes using a top-down lithography patterning + etching methods. These films are patterned with periodic holes with spacing that is comparable to, or shorter than, the average phonon MFP of silicon. Yu, *et al* [124], found that the thermal conductivity of the Si nanomesh is even smaller than that of the Si nanowires array with the same periodicity (pitch distance), despite the fact that Si nanomesh has a lower surface-to-volume ratio. This indicates a phononic modification is involved based on the superstructure, where the phonon group velocity decreases due to flattening of phonon bands. Meanwhile, the electrical properties for the monolithic Si thin film were only slightly reduced in the Si nanomesh with a doping level on the order of 10^{19} $cm^2/V \cdot s$ [124]. Tang, *et al* [122] performed a complete thermoelectric characterization on a similar holey Si membrane device fabricated via nanosphere lithography and block copolymer lithography, shown in Fig. 5-1. The thermal conductivity was dramatically reduced down to 1.73 – 2.03 W/m K in the holey Si device with the neck/pitch size of adjacent holes = 23/55 nm and a membrane thickness of 100 nm. Meanwhile, the power factor reduced only by a factor of ~1.5 compared with non-holey reference sample, resulting in a final ZT of 0.4 at room temperature. However, a more recent work from the same group reported a much lower ZT ~ 0.04 in similar samples due to degradation in electrical conductivity as well as a slightly higher measured thermal conductivity[123]. It can be seen that the transport mechanisms in holey silicon are quite complex, and the properties are rather sensitive to the fine-grained sample specifications, such as surface roughness, morphology, and impurities, which are all subject to the fabrication processes. It is also noted that thermoelectric measurement of small structures such as silicon nanowires and holely silicon could have very large error bars.

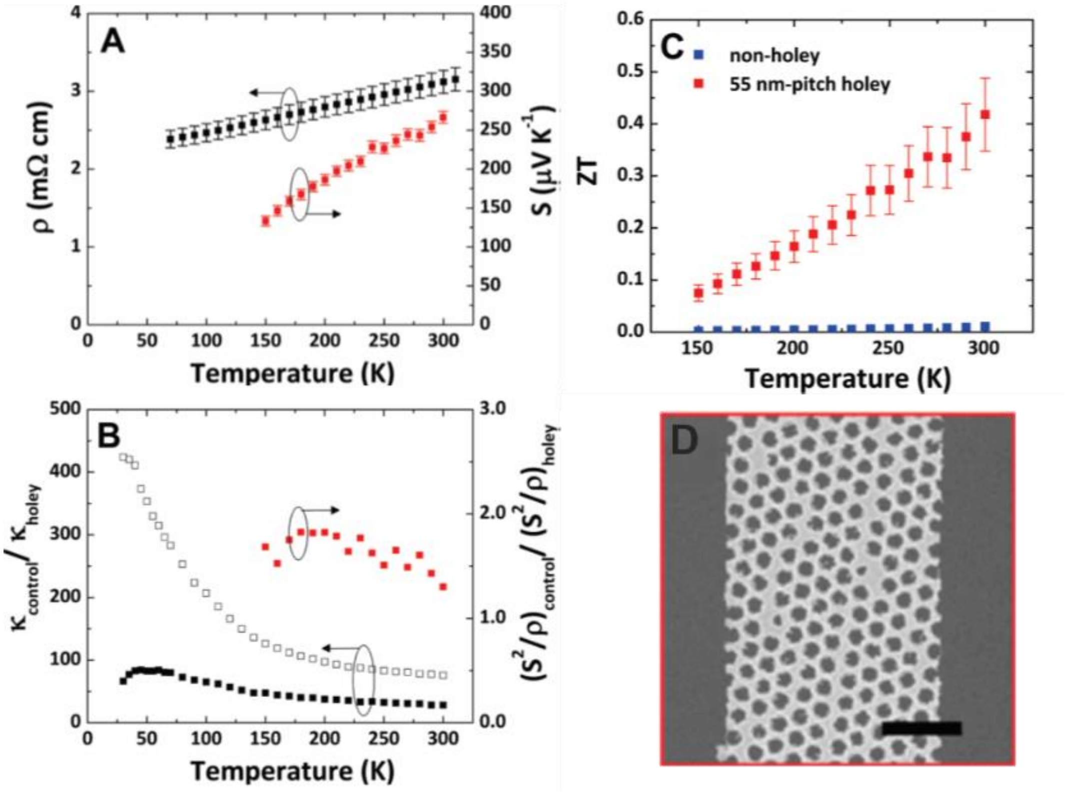

Figure 5-1: Thermoelectric properties and ZT calculation for 55 nm pitch HS ribbon. (A) Temperature-dependent ρ and S of a boron doped 55 nm pitch HS ribbon (B) κ comparison of doped 55 nm pitch HS ribbon with doped nonholey silicon ribbon (black squares), or bulk silicon (open squares, 1.7× 10^{19} cm^{-3}, As-doped); Seebeck comparison (red squares) of doped 55 nm pitch HS ribbon with nonholey silicon ribbon. (C) ZT of 55nmpitch HS ribbon (red squares) compared with nonholey ribbon (blue squares). (D) the morphology of 55nm-pitch HS ribbon. Reproduced from ref. [122]

M. Nomura, *et al* [125] had a comprehensive summary of effective thermal conductivity as a function of the critical size (neck size) for holey Si samples reported in the literature, show in Fig. 5-2. The observed trend is easily conceivable as the increased surface to volume ratio is associated with the reduced neck size, which in turn suppresses the thermal conductivity. As a rule of thumb, the neck size should be <50nm in order to reduce the thermal conductivity of Si film below 10 W/m K, according to Fig. 5-2. However, holey Si with the neck size on the order of ~50nm can hardly modify the phonon dispersion, and yet the the thermal conductivity reduction deviates from the classic Eucken model taking account of the porosity φ:

$$\frac{\kappa_{porous}}{\kappa_{solid}} = (1 - \varphi)/(1 + \varphi/2) \qquad 5\text{-}2$$

For instance, our holey Si device is 100nm in thickness, and has a square lattice of holes with a pitch size of 100 nm and a neck size of 45 nm. The porosity can thus be calculated as 0.24. According to equation 5-2, κ_{holey_Si} should be 34 W/ m·K (here $\kappa_{solid} = 50$ W/m K for 100 nm non-holey Si thin film[122]), which is much larger than the values of the close counterparts shown in Fig. 5-2. The dramatic discrepancy can be attributed to the "necking effect", which was found to trap the phonons with MFPs longer than the neck size, so that hole surfaces would scatter the ballistic phonons and cause a negative temperature gradient locally behind holes, resulting a significantly reduced thermal conductivity[124][126].

The works referred above are all *suspended* holey Si films and the thermoelectric transport are characterized at low temperature to room temperature range. In this work, we fabricate boron doped holey Si device directly using a SOI wafer, and conducted in-plane thermoelectric transport measurements at an elevated temperature range.

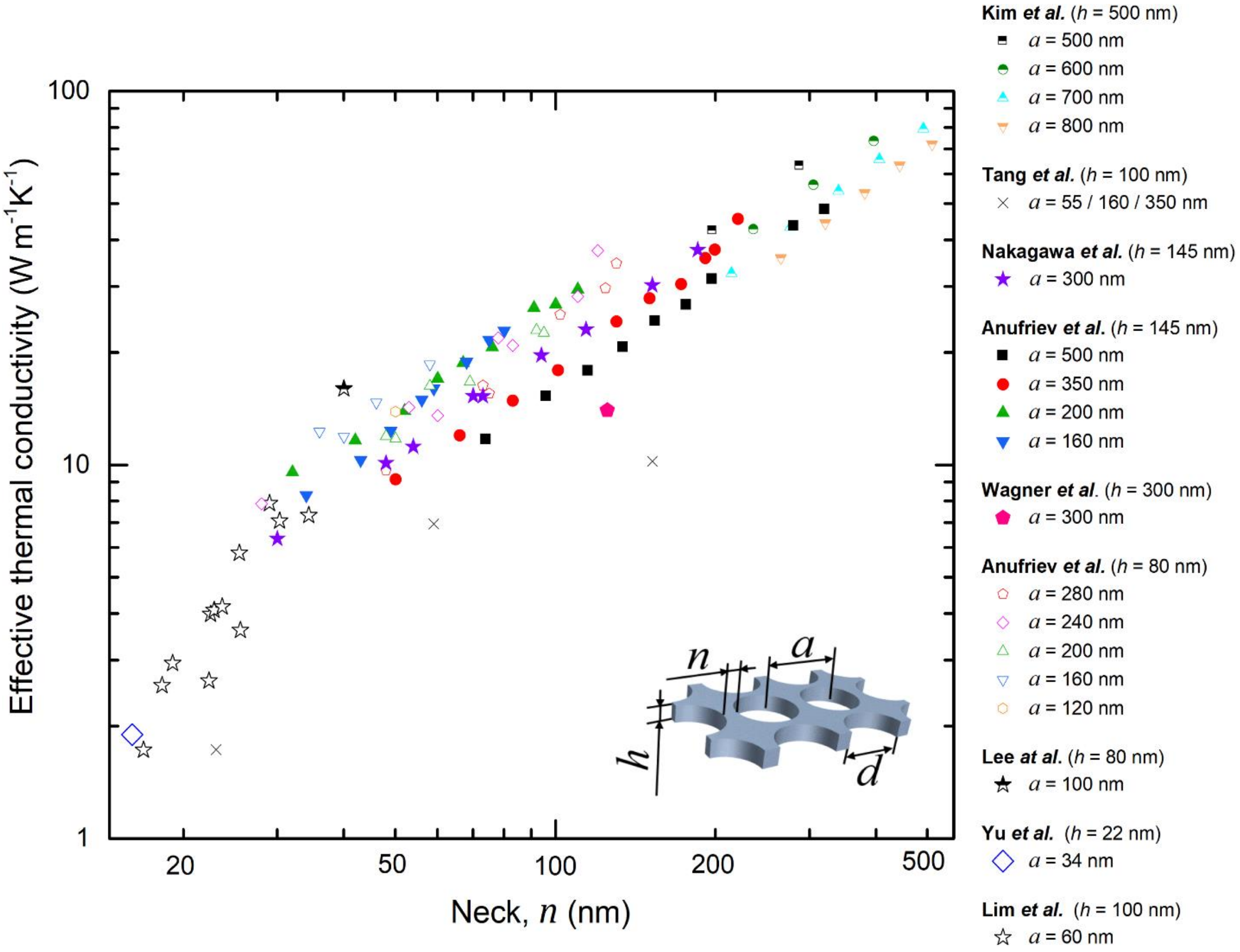

Figure 5-2: Experimental values of effective thermal conductivity at room temperature as a function of neck size. Reproduced from ref. [125]

5.1.2. Fabrication and device configuration

The holey Si device fabrication, prior to final metal deposition, is mainly conducted by our collaborator at UCSB. The brief process steps are described as follows:

A 4" SOI wafer (a 100 nm active Si layer on a 1 µm buried oxide) was first sent to Leonard Kroko Inc. for the blanket boron implantation, which would eventually yield a $3\times10^{19} \sim 1\times10^{20}$ cm^{-3} p-type doping level (boron 5 keV, 3×10^{14} atoms/cm^2 followed by boron, 25 keV, 3×10^{14} atoms/cm^2

with 7 degree off-axis tilt). Rapid thermal annealing was then conducted at 1100 °C for 30 seconds to repair the implant damage and activate the boron dopants. Electron beam lithography (EBL) was used to write dot array to a size of 30 µm × 200 µm for each device, with a dot (hole) pitch spacing of 100 nm. Resist development was conducted to transfer the pattern onto the Si surface, and reactive ion etching (RIE) was then used to etch the exposed areas to generate array of holes, with a dimeter of ~55 nm (neck size ~45 nm). Subsequently, the active device areas were covered with resist, and the rest of Si layer was etched down to BOX to form arrays of 30 µm × 200 µm Si mesas for the following metallization. 1µm Al with 50nm Au capping layer (Al can form Ohmic contact with p-type Si, and the Au cap helps to prevent Al from oxidation) was deposited as contacts for the subsequent transport measurements. The holey Si device and the contact configuration are shown in Fig. 5-3 and Fig. 5-4, where the contacts, heater, thermometers are annotated.

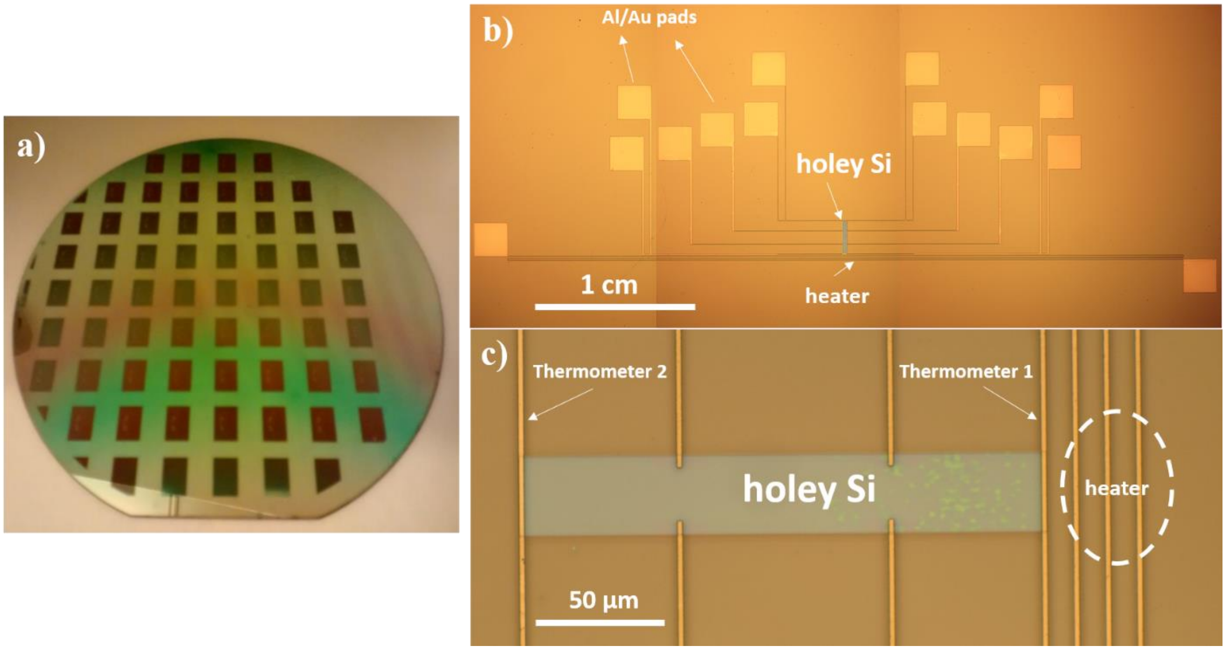

Figure 5-3: a) SOI wafer with completion of device fabrication. b) Device configuration for transport measurements. c) 90° zoom-in view of b) with Si device layer, heater and thermometers annotated

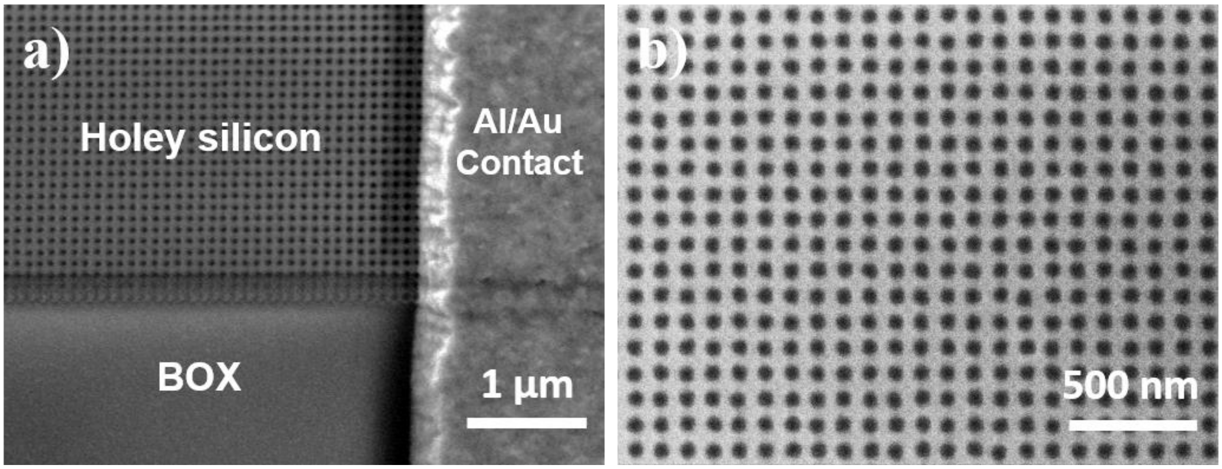

Figure 5-4: a) SEM image showing holey Si film on buried oxide layer, as well as Al/Au metal contact. b) enlarged view of the holey Si device

5.1.3. Electrical transport measurements

The wafer was diced into 9 mm × 9 mm chips for the subsequent packaging and wire bonding. The final package was mounted on our thin-film electrical transport measurements station, which is JANIS cryostat vacuum chamber, equipped with a helium compressor and a temperature controller (10K – 800K), a nanovolts meter for Seebeck voltage measurement, and two lock-in amplifiers for resistance measurements, as well as several digital multimeters and power supplies for applying current or bias voltage, etc.

The Seebeck coefficient was measured using a micro-heater and two calibrated thermometers, as annotated in Fig. 5-3. When applying a current to the heater, a temperature difference is built up across the two ends of the holey Si mesa as a result of joule heating of the heater. Therefore, an electrical potential is produced due to Seebeck effect. Since the thermometers are in direct contact with Si surface, the Seebeck voltage could thereby be measured. Figure 5-5 a) exhibits the Seebeck voltage response of the holey Si device by applying 30 mA to the micro heater at 350K. As shown, the absolute voltage instantly changes and quickly saturates at ~ 225 μV when the heater was on, indicating a steady state of the temperature differential built up across the two ends of the sample. In order to extrapolate the actual Seebeck coefficient (S = $-\frac{V_S}{\Delta T}$), the corresponding temperature differential must also be measured. The respective temperature of the device's ends can be measured by the thermometers on top of those. Thus, temperature calibrations need to be implemented for both thermometers. To do that, the same current (30 mA) was applied to the heater, and the resistance-versus-time curves of the two thermometers were simultaneously measured using separate lock-in amplifiers. Since the resistance of the metal lines are relatively small and subject to considerable noise in DC measurement, resulting in excess uncertainty in the temperature calibration, lock-in method is adopted rather than using a DC multimeter. After that, the temperature dependence of resistance of the thermometer was measured by raising the ambient temperature up by ~ 10K (heater OFF). Thus, the device temperature (heater ON) can be easily calibrated according to the linear temperature – resistance relationship of the thermometers, as shown in Fig. 5-5 c) and e). Figure 5-5 b) and d) show the resistance change with time in the two thermometers when heater is ON/OFF, corresponding to the Seebeck voltage response shown above in Fig. 5-5 a). ΔT was then calibrated as 0.981 ± 0.06 K, giving a Seebeck coefficient of 239.5 ± 5.1 μV/K, at 350K. The positive sign of Seebeck coefficient also confirms the p-type conduction mechanism in the boron doped holey Si device. Using the same method, temperature dependence of Seebeck coefficient was obtained, as shown in Fig. 5-6 b).

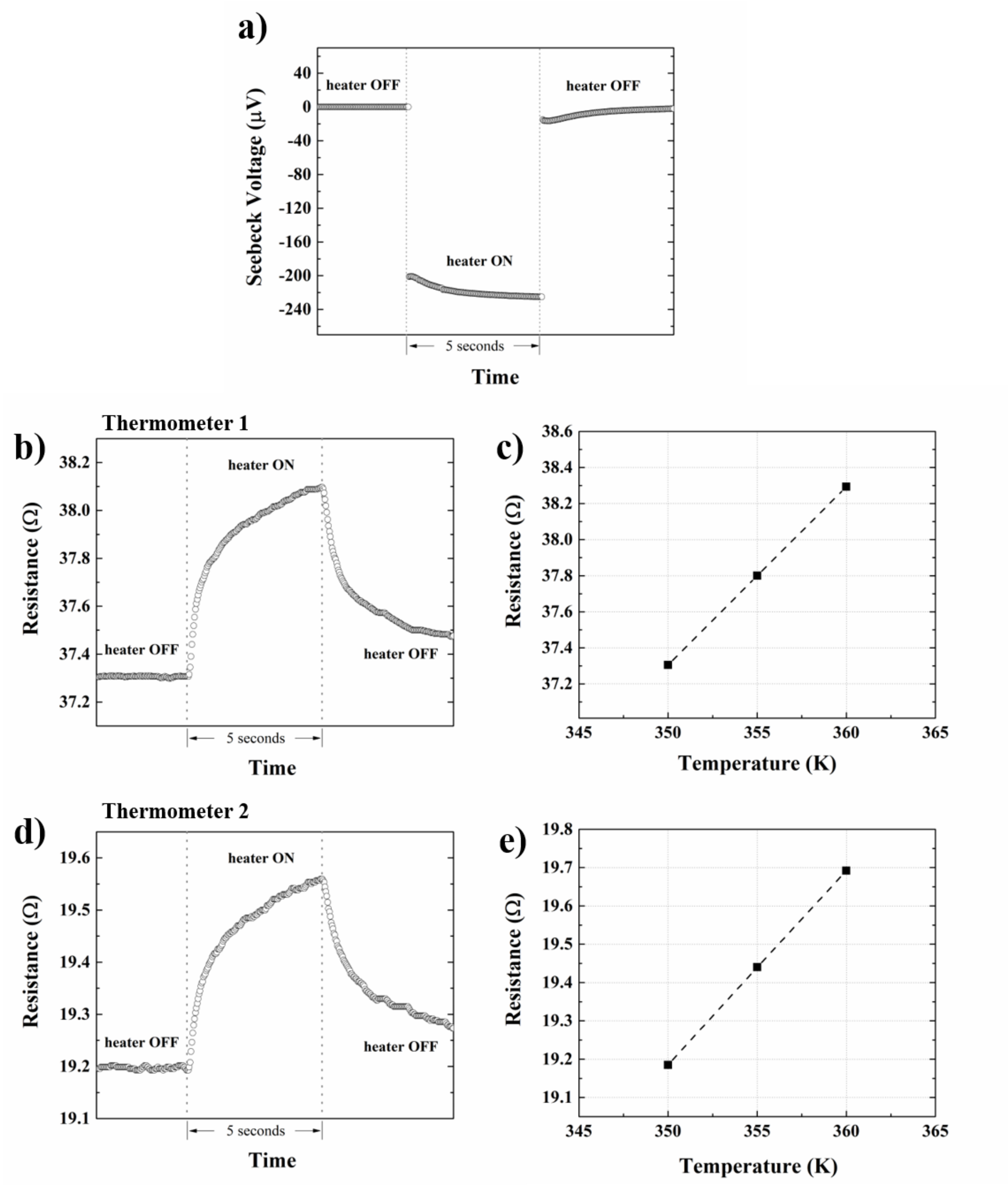

Figure 5-5: a) Seebeck voltage response of the doped holey Si device when the heater is ON/OFF; and the corresponding resistance change of b) thermometer_1 and d) thermometer_2, as a function of time, at 350K. c) and e) temperature calibration for b) and d) respectively

The electrical conductivity was measured using four-point probe method, by applying a current across the two thermometers and measuring the voltage drop on the two metal probes in between, as shown in Fig. 5-3 b). Since a small current of 0.1 µA was used for the measurement a lock-in method was also used for improving signal to noise ratio. The measured temperature dependence of electrical conductivity is shown in Fig. 5-6 b), which exhibits a metallic behavior due to the heavy doping. The corresponding power factor times temperature curve is shown in Fig. 5-6 c), in which 0.52±0.04 W/m K is obtained at room temperature and 1.10±0.09 W/m K at ~ 650K.

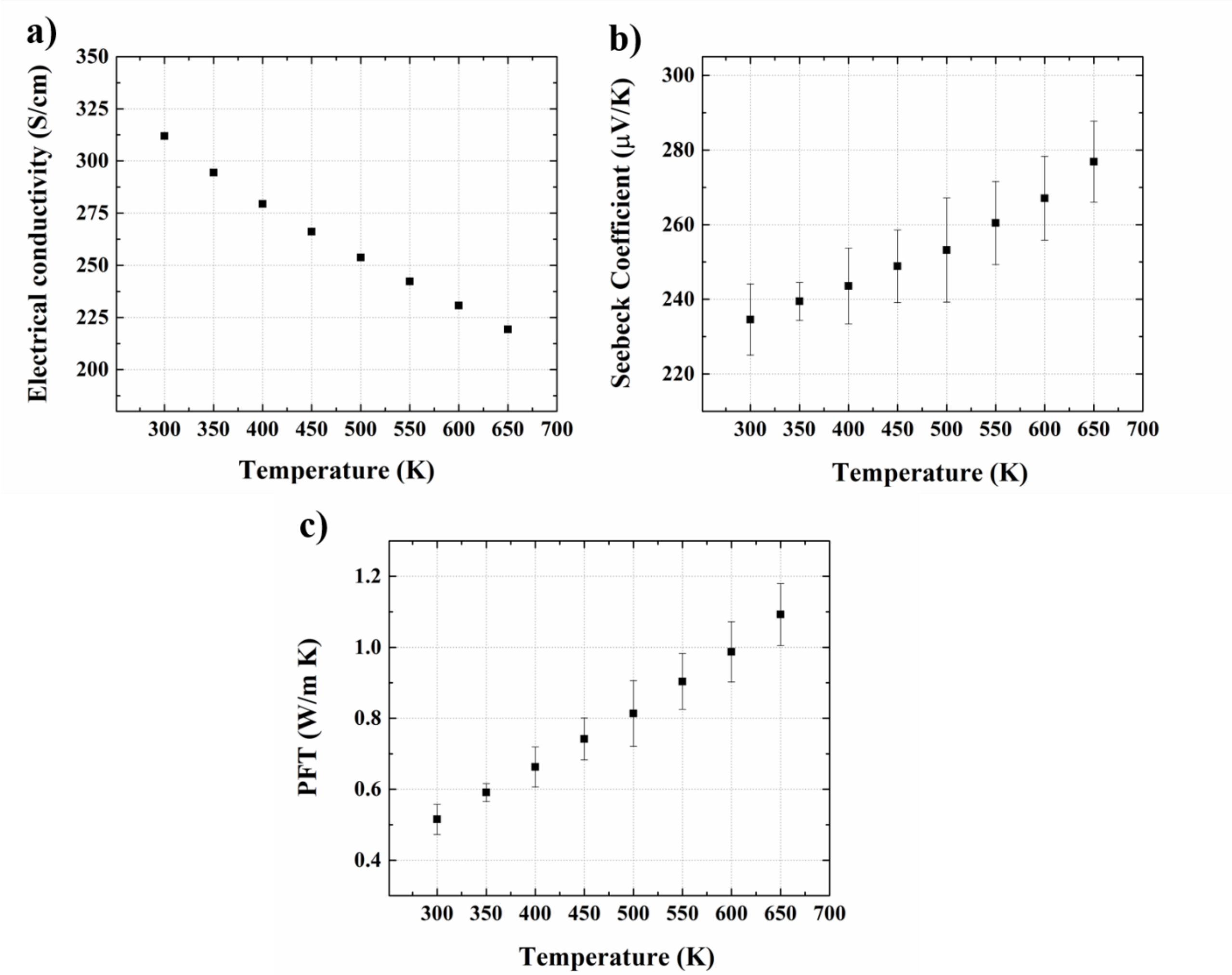

Figure 5-6: Temperature dependence of a) electrical conductivity, b) Seebeck coefficient and c) power factor times temperature of the doped holey Si device

5.1.4. Thermal transport measurements

In-plane thermal conductivity measurement for thin film materials still remains very challenging in practice. For thin films on a substrate, there are only few methods available. The two main ones are namely variable-linewidth 3ω method [127] and heat spreader method [128], both are difficult to implement. Cross-plane thermal conductivity is usually measured instead using 3ω method [129], or TDTR [130][131] assuming material is isotropic.

Thermal transport in holey Si is obviously anisotropic due to its morphology, and therefore, the previous work on holey Si all used suspended films for in-plane thermal conductivity measurement. In our lab, we have a thermal imaging system, which can directly capture the transient temperature profile of the sample surface under bias. The detailed working mechanism of thermal imaging system is provided in Chapter 2. Based on this temperature or thermal profile, we can then use a model similar to heat spreader method[128] to extract the in-plane thermal conductivity of the holey Si device.

As shown in Figure 5-7, the film of interest (holey Si) is on a thin insulation layer (buried oxide) and metal heater line is deposited on the film. When applying a current, Joule heating of the heater would spread along the film building up a temperature decay profile. The heat leaking vertically through the buried oxide layer will be taken into account in the model. The temperature profile on the film obeys the classical fin equation, decaying exponentially in lateral direction[37]. The temperature profile follows the relation

$$T(x) - T(\infty) \propto e^{-\beta x} \qquad 5\text{-}3$$

$$\beta = \sqrt{\frac{h_i}{k_x d}} \qquad 5\text{-}4$$

where k_x is the in-plane thermal conductivity of the film, d is the thickness of the film. $h_i = k_{i,z}/d_i$ accounts for the cross-plane conduction into the underneath insulation layer, where $k_{i,z}$ and d_i are the cross-plane thermal conductivity and the thickness of the insulation layer, respectively. The thickness of the holey silicon film for our sample is 100 nm and that of the insulating SiO_2 layer is 2 µm. The thermal conductivity of the thermally grown SiO_2 is ~1.35 W/m K [132]. Thus, $h_i = 6.75 \times 10^5$ W/(m^2K). The air convection to the surroundings is in parallel to h_i and is about 10 W/(m^2K), and therefore it is negligible. The thermal contact resistance between the holely silicon layer and the SiO_2 layer is in series to h_i and is much larger (about 2 G W/(m^2K) and therefore is also negligible. . Therefore, $k_x = \frac{h_i}{d\beta^2} = \frac{6.75\times10^{12}}{\beta^2}$ W/m K. Then fitting the

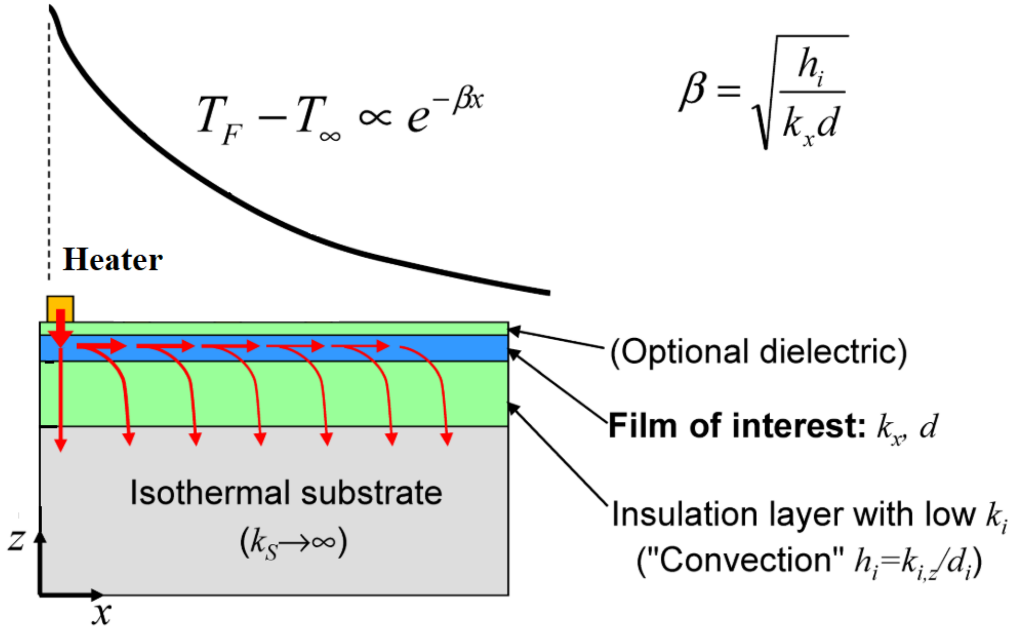

Figure 5-7: Schematic of heat spreader method for in-plane thermal conductivity measurement. Joule heating from the heater line is spread laterally on the device film, while at the same time leaking vertically through the buried oxide layer. The temperature profile on the film obeys the classical fin equation, decaying exponentially in lateral direction

temperature profile obtained by thermal imaging would give β value, for finally calculating the thermal conductivity.

A pulsed voltage of 4V with 10 ms pulse width and 30% duty cycle is applied on the heaters of both holey Si and non-holey Si films. Figure 5-8 show the transient temperature gradient maps of the two devices at the end of each duty cycle (averaged over many thermal cycles). It can be clearly observed that the heat conduction gradient shown on non-holey Si is much more extended than that of the holey Si device, due to a much larger thermal conductivity. Arbitrary unit is used for the isothermal scale instead of calibrating the actual temperature, as β is the exponential factor of the temperature profile curve, which is irrelevant to the absolute temperature.

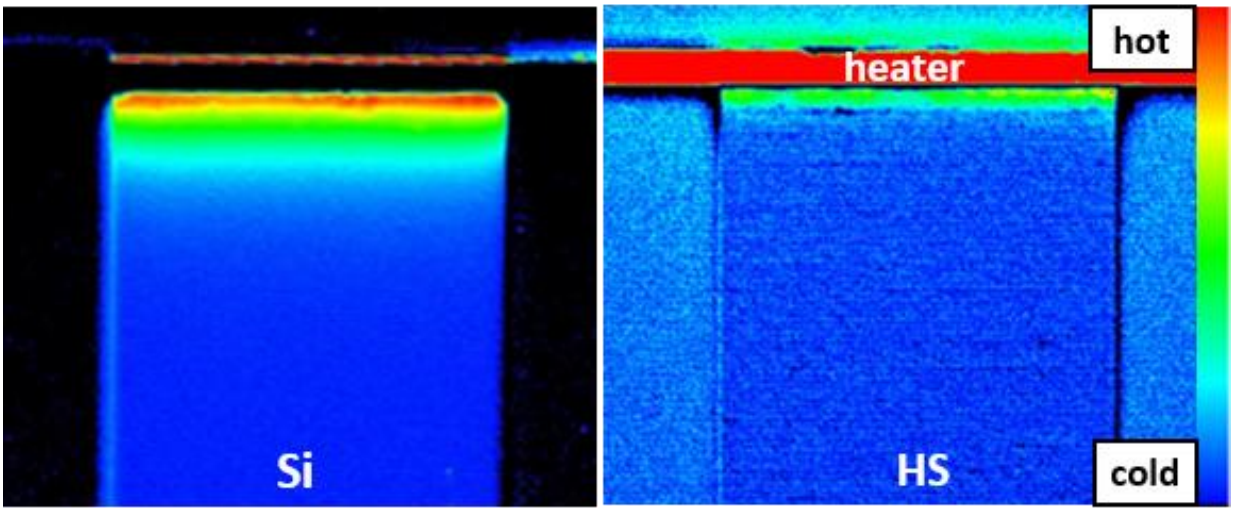

Figure 5-8: Temperature maps of a) non-holey Si and b) holey Si sample produced by the thermal imaging system with 4V applied to the heater at one end of the sample, and 530nm-wavelength illumination. Note that the heater in a) is shown in dark color due to opposite sign of thermo-reflectance coefficient

Temperature line-profiles taken at different areas, and also on different devices are obtained. The representative temperature profiles of both devices as shown in Fig.5-9. the parameter β can then be extracted by fitting the temperature profile curve, and finally estimate the in-plane thermal conductivity. The average k_x for the Si sample is ~ 73.21 ± 4.66 W/mK, while for holey Si is ~ 6.3 ± 1.3 W/m K.

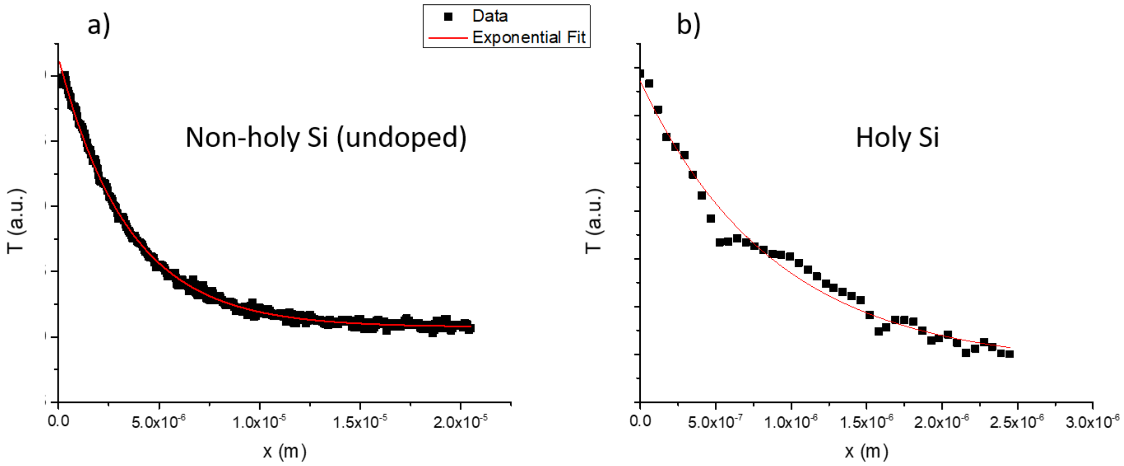

Figure 5-9: Representative temperature line profiles of a) non-holey and b) holey Si device

5.1.5. Summary

This work extends the transport study of holey Si devices to elevated temperature range, which to our best knowledge has not been reported. A novel method to measure in-plane thermal conductivity of thin film materials using thermal reflectance imaging is successfully conducted. We measured ZT at room temperature to be 0.08 which is consistent with previously reported ZT values. We have also designed and installed a cryostat coupled with thermal imaging system to extend the thermal conductivity measurements to high temperatures, so that obtaining ZT at high temperatures would be possible. More importantly, the doped holey Si by ion implantation serves as a control sample for my following investigation on the organics – holey Si hybrid device, which utilizes a non-destructive doping mechanism by charge transfer at the heterointerface. To achieve this goal, in the next chapter, F_4TCNQ – non-holey Si hybrid device will be studied first to validate the charge transfer mechanism.

5.2. F_4TCNQ-Si Hybrid Device

5.2.1. Unconventional doping schemes towards thermoelectric applications

As discussed previously, in order to optimize power factor ($S^2\sigma$), good thermoelectric materials are usually heavily doped semiconductors. The conventional doping strategies for semiconductors all involve introduction of aliovalent ion impurity or defect engineering (i.e. vacancies). The activation process ubiquitously requires solid-state thermal diffusion, which cannot be applied to materials that are heat sensitive. Devices with ultrafine structures, such as nanowires, ultra-thin film or self-assembled nano-features, etc., would also suffer from non-negligible statistical variation or deactivation of dopants[21]. The other main drawback of conventional doping methods is that they all involve incorporating impurity ions or defects, which create long range Coulomb potentials that scatter conduction electrons and lowers their mobility. *Modulation doping* has been proposed for 2D structures to overcome these shortcomings and has been implemented in transistor technology[133], that is, modulation-doped field-effect transistors (MODFETs) or high electron mobility transistors (HEMTs), which has been studied extensively for applications where high frequencies, high gain and low noise are required. In essence, it uses a heterojunction to form a quantum well in the conduction band confining electrons in the undoped region, which creates 2D electron gas (2DEG) with exceptionally high mobility under a gate voltage. This heterojunction is usually obtained by an epitaxially grown heavily-doped large-bandgap material on an undoped narrow-bandgap material. The modulation doping effect, was first demonstrated in GaAs/AlGaAs superlattice system, in which only the AlGaAs layer was selectively doped. This resulted in electrons confinement in the undoped GaAs region in vicinity to the interface due to band inversion, while the ionized donors remained in AlGaAs. Dramatic electron mobility improvement was observed compared with that of a uniformly doped GaAs counterpart, especially at low temperature range (~ 10^4 $cm^2/V{\cdot}s$ below 50K)[133], at which the impurities or defects play as the dominate scattering mechanism. In the next two decades, the 4 orders of magnitude in mobility enhancement have been reported in GaAs[134] using modulation doping scheme.

As another unconventional doping approach, polarization-induced doping has also been investigated in wide-bandgap semiconductors for applications such as in laser, light-emitting diode (LED), and high-power electronic devices, etc. One of the technical challenges is to achieve a substantial doping level due to the large thermal activation energy. It is found that the built-in electronic polarization can be utilized as the source of doping carriers. For III-VI nitride compounds *e.g.* Ga(Al)N, the bonds are partly ionic due to different electronegativities of Ga(Al) and N, along with intrinsic asymmetry of the bonding in wurtzite crystal structure, giving rise to a large spontaneous polarization. Tensile strain from hetero-epitaxy can also result in piezoelectric polarization that is parallel and adding up to the spontaneous polarization[135]. For *sharp heterojunctions* of AlN/GaN, 2DEG with a high sheet density ~ 5.5×10^{13} cm^{-2} (at 77K) was formed simply due to the polarization charge induced electrical field and band bending, similar to the modulation doping scheme, but without deliberately introducing impurity dopants as in GaAs/AlGaAs systems. On the other hand, a very different doping mechanism can be achieved in epitaxially grown *compositionally graded* $Al_xGa_{1-x}N$/GaN crystals, where the net polarization-induced unbalanced charges are formed in the graded $Al_xGa_{1-x}N$ unit cells, which essentially form

3D electron slabs[136]. This is because $Al_xGa_{1-x}N$ has higher polarization than that of GaN, and the strength of charge dipoles in each unit cell keeps increasing when x increases. The space charge after compensation in each unit cell would then result in net polarization charges in the bulk, which effectively dope the material. Polarization direction can be inversed by changing compositional grading orientation to achieve either p- or n-type doping. The carrier concentration of the 3DEG is insensitive to temperature as it is "field-ionized" and is not subject to thermal freeze-out effect. More importantly, the mobility enhances due to the fact that the ion impurity scattering is absent[136].

Compared with III-VI compounds, the mobility of 2DEG in silicon is couple of orders of magnitude lower. For Si metal-oxide-semiconductor field-effect transistors (MOSFETs), the mobility is limited to $\sim 10^4$ $cm^2/V\cdot s$ due to impurity scattering and Si/SiO_2 interface roughness[131]. Si/SiGe superlattice with strain-induced hetero-band-structure modification can generate 2DEG residing in the Si quantum well by modulation doping[137]. A good-quality epitaxy with minimized misfit dislocations and roughness can improve the electron mobility to the order of $\sim 4\times10^5$ $cm^2/V\cdot s$[138]. Nevertheless, the ionized impurity scattering from the supply layer due to the long-range Coulomb potentials would still suppress the mobility from further improvement. Thus, in principle, an undoped Si 2DEG formed by top gating would possess higher mobility than the modulation-doped heterostructures. Mobilities on the order of $\sim 10^6$ $cm^2/V\cdot s$ have been reported[139][140], which again suggest that electron transport can be greatly enhanced if impurity scattering can be circumvented.

The unconventional doping mechanisms discussed above all involve minimizing ionic impurity scattering for mobility improvement, which is also critical for power factor optimization in thermoelectric materials. "3D modulation doping" scheme has been applied in bulk thermoelectric materials. The pioneering work by Zebarjadi, *et al* [141] studied thermoelectric properties of the selectively doped Si-SiGe nanocomposite, where heavily doped Si nanoparticles are embedded in undoped nanograined SiGe. Due to band alignment, the charge carriers diffuse from the nanoparticles into the surrounding matrix, while the ionized dopant atoms remain spatially segregated within the nanoparticles. The key in 3D modulation doping is to obtain close proximity amongst interfaces, with an average distance of ~20 nm. Given a screening length of 5–10 nm, carriers can then flow through the whole host matrix, rather than being confined near the interfaces. Enhancement in power factor were observed in both n- and p-type SiGe nanocomposite, compared to uniformly doped control samples due to the enhanced mobility, shown in Fig 1-11 in Chapter 1.

While this 3D modulation doping strategy has been widely investigated in other bulk systems, studies on 2D modulation doping for thermoelectric device applications are still scarce within literature. Nevertheless, field-induced 2DEG by gating has shown the promise for thermoelectric power factor improvement. Ohta *et al*[142], fabricated a Al_2O_3/AlGaN/GaN MOS-HEMT, and studied its thermoelectric transport by tuning the gate voltage to modulate the S and σ of the 2DEG. It exhibits a high thermoelectric power factor PF of ≈ 9 $mW{\cdot}m^{-1}$ K^{-2} at room temperature, which is an order magnitude greater than that of doped GaN bulk, mainly due to mobility enhancement. Seebeck coefficient enhancement was also observed for 2DEG formed in ion-gated transistor with ZnO as the channel material[143]. As previously described, the quantized DOS of 2DEG can result in large Seebeck coefficient if the chemical potential is tuned properly. Under a large gate voltage (~3.5V), a sharp band bending at the ZnO surface result in formation of a high-density 2DEG up to $\sim 7 \times 10^{13}$ cm^{-2}. Along with the Seebeck coefficient enhancement, the power factor was reported one order of magnitude larger than that of the 3D-band ZnO materials by impurity doping[143].

In order to make such an interface effect practical for power generation, strategies in increasing effective thickness of 2DEG, or even extending 2DEG into bulk 3DEG need to be investigated. 2DEG induced by field effect (gating) consumes electrical power, which is more proper for thermal management applications rather than power generation. In addition, to extend 3D doping with gating seems to be an insurmountable challenge. As for modulation doping or polarization doping schemes, besides the strict epitaxial growth of heterojunctions to minimize the misfit dislocations and roughness, ionized impurity scattering from the remote supply layer would still suppress the mobility, while increasing the spacer thickness would in turn result in lowering the carrier density in the channel material. In this chapter, we are investigating another doping mechanism utilizing charge transfer between organic–inorganic (F_4TCNQ – Si) interface for thermoelectric applications. Physisorption of certain organic molecules on Si can easily be achieved by solution based or physical vapor deposition, to initiate charge transfer. And ultimately, it is also feasible to extend this 2D transfer doping to 3D bulk doping by maximizing the surface to volume ratio of the inorganic part (*e.g.* holey Si), so that a 3D network of transferred change carriers can extend through the bulk.

5.2.2. Charge transfer on F_4TCNQ – Si interface

We select tetrafluoro-tetracyanoquinodimethane (F_4TCNQ) as the organic part of the hybrid device, to investigate the charge transfer and its implication on the thermoelectric transport, rationales and previous relevant studies will be discussed as follows, in this section.

F_4TCNQ is a fluorinated TCNQ derivative, and has an exceptionally high electron affinity of $E_a = 5.24$eV[144]. It's well known as a strong electron acceptor, to dope molecules p-type by forming charge transfer organic complex, as well as to enhance hole injection by energy level alignment at organic – metal interfaces[145][146]. Therefore, F_4TCNQ has been widely applied in organic light emitting diodes (OLEDs)[147][148], photovoltaics,[149],[150] organic field-effect transistors

(OFETs)[151], etc. P-type surface doping was also achieved at inorganic semiconductor surfaces, such as diamond[152], graphene[153], and VO_2[154], and investigated by photoemission spectroscopy (PES) techniques. However, as the most pervasive semiconductor material for electronic devices, Si, has only sparsely been examined experimentally as the active layer for transfer doping by F_4TCNQ. The limited prior reports mainly focus on electronic structure study of the interface using PES [155,156] or transmission infrared spectroscopy[157] techniques, where the charge transfer has been experimentally verified by essentially comparing spectra of the first layers of F_4TCNQ with those of multilayers (neutral bulk F_4TCNQ) on Si. We seek to further investigate the electrical transport properties of the F4TCNQ – Si interface, towards thermoelectric device applications.

To understand the charge transfer mechanism, as shown in Fig. 5-10 a), the lowest unoccupied state (LUMO) of F_4TCNQ lies below the silicon valence band maximum (VBM), hence the electron affinity of F_4TCNQ is larger than the ionization energy of Si. This favors electron-transfer from silicon to F_4TCNQ molecules, and Si is thus p-type doped near the interface. The holes are confined in the direction normal to the interface due to the established electrostatic potential but free to move in the parallel direction. XPS study shows that the shift of Si 2p binding energy peak saturates when the in-situ deposited F_4TCNQ thickness is 2 nm[158], meaning the F_4TCNQ molecules farther to the interface do not contribute to the charge transfer, as illustrated in Fig. 5-10 b).

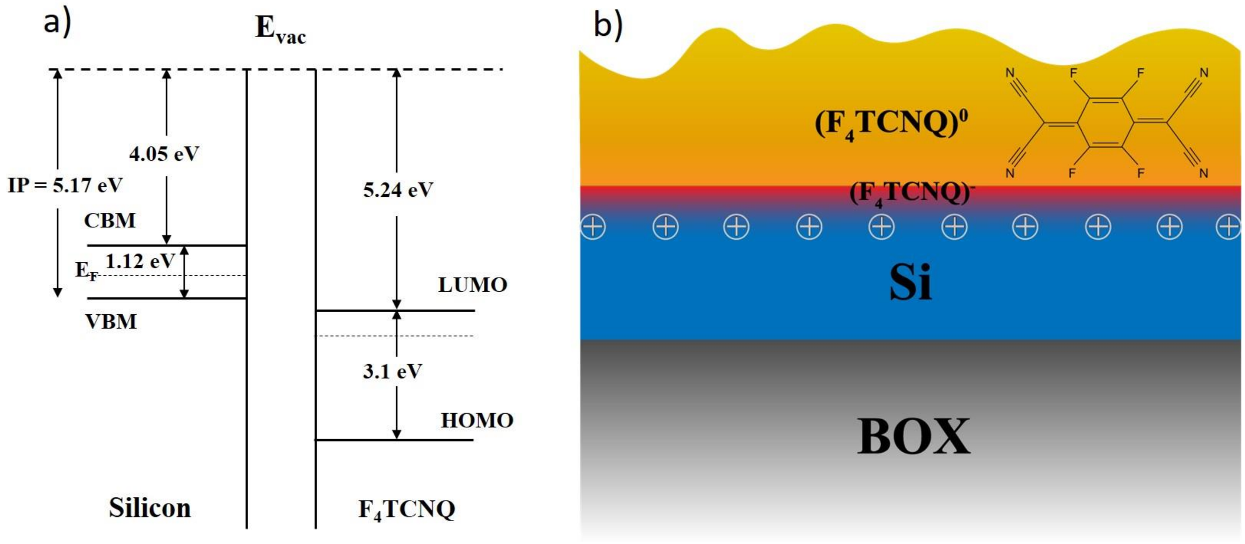

Figure 5-10: a) the band structure of silicon and F_4TCNQ before contact; b) the device configuration studied in this work: buried oxide/Si/F_4TCNQ. And The charge transfer is only effective in proximity of the interface

Our previous DFT calculation by X. Wang[159] indicates that physisorbed F_4TCNQ self-assembled monolayers can efficiently dope silicon, achieving hole concentrations as high as 10^{13} cm^{-2}. Figure 5-11 shows the calculated local density of states of hydrogen terminated Si(100) – TCNQ interface, as well as the charge transfer efficiency using different TCNQ derivatives, including F_4TCNQ.

With an effective charge transfer providing a large carrier concentration, the conductivity is expected to be greatly improved due to mobility enhancement, as impurity scattering is absent. In addition, since the transferred charge layer resides in Si, the relatively large Seebeck coefficient of Si can be harvested leading to a large power factor. In further step, a combination of enhanced mobility by transfer doping and low thermal conductivity of F_4TCNQ could be utilized to design a high performance F_4TCNQ – nanostructured Si (e.g. nanopatterned holey Si or nanowires) hybrid thermoelectric materials. However, this concept relies on a fundamental understanding of charge transfer and thermoelectric transport at the interface of F_4TCNQ – silicon, which is thereby the main focus of this work.

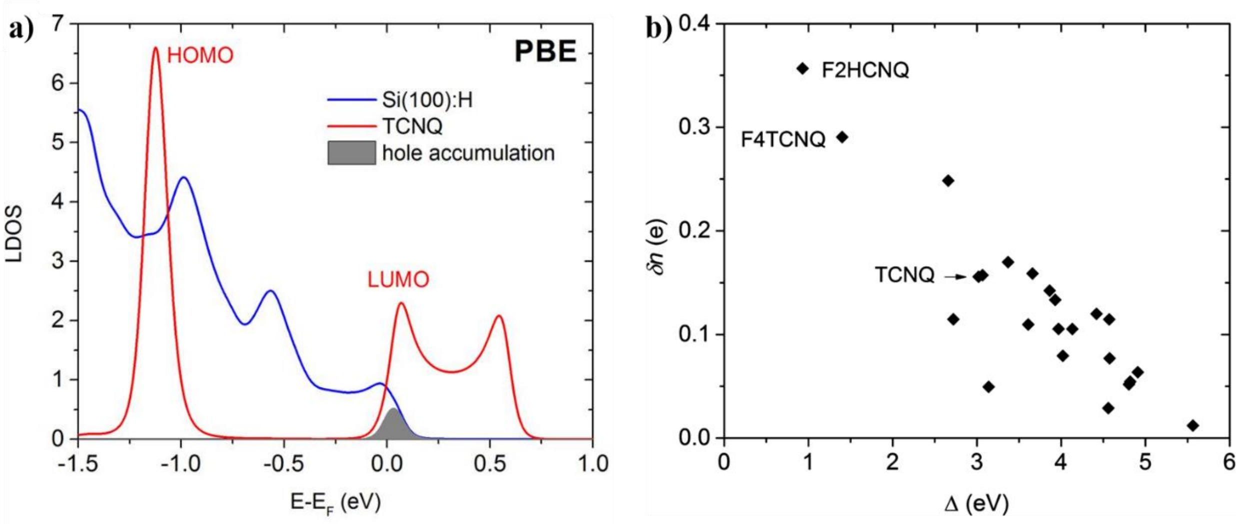

Figure 5-11: a) Local density of states (LDOS) of Si(100):H −TCNQ by DFT (PBE: Perdew−Burke− Ernzerhofb) calculation. b) Net charge transfer δn between the Si(100):H slab calculated by the chemical hardness method. Δ is the charge transfer energy

5.2.3 F_4TCNQ – Si hybrid device

To fabricate the F_4TCNQ – Si hybrid device, F_4TCNQ molecules were deposited on the Si surface (directly on the metalized Si device) by thermal evaporation. The Si device has the same configuration with the holey Si device described in section 5.1.2, and the fabrication is similar. Since it is non-holey Si there were no patterning and etching steps involved in the fabrication process. For the purpose of validating the charge transfer mechanism, Si mesas were only mildly doped by a blanket boron implantation yielding a $1\times10^{16} \sim 3\times10^{16}$ cm^{-3} p-type doping level (boron 5 keV, 9×10^{11} atoms/cm^2 followed by boron, 25 keV, 9×10^{11} atoms/cm^2 with 7 degree off-axis tilt). Moreover, in order to achieve Ohmic contact, additional rapid thermal annealing was conducted at 500 °C for 30s.

Next, F_4TCNQ molecules was deposited on the non-holey Si device using a homemade miniature thermal evaporator. The thermometers and the electrodes are then in between the Silicon and F_4TCNQ allowing us to characterize the interface. Despite withdrawing electrons from Si upon contact, the electrical conduction of the F_4TCNQ film is negligible compared to the Si layer. Therefore, it was feasible to directly deposit F_4TCNQ onto the metallized device, without shorting the metal lines. Prior to the deposition, the device was dipped in BOE for 25 seconds to create a passive H-terminated Si surface, in order to prevent charge confinement by the surface states. The metal pads were then covered by a shadow mask for the ease of wire bonding after deposition. The F_4TCNQ crystal powder (Sigma-Aldrich, 99.9%) and the device were loaded into a homebuilt miniature thermal evaporation chamber with a base pressure of $<10^{-6}$ torr. F_4TCNQ was degassed below 100°C and then sublimated at 140°C for deposition. It was found that the F_4TCNQ has a relatively low sticking probability on H-Si(100), which is commonly observed for molecules physical adsorbed on inorganic substrate[160]. Furthermore, due to the limited wettability, F_4TCNQ adsorbates tend to coalesce into densely-packed islands on Si. In order to achieve full coverage and maximize the charge transfer, a relatively high vapor flux is required to create a high nucleation rate. Therefore, we used a higher F4TCNQ temperature of ~ 140°C compared to other PES studies[155–157]. The net deposition rate was calibrated as ~ 1.5Å/s. Surface morphology was then characterized by atomic force microscopy (AFM). Figure 5-12 shows the surface morphology of F_4TCNQ with root mean square (RMS) roughness of ~17 nm under this deposition condition.

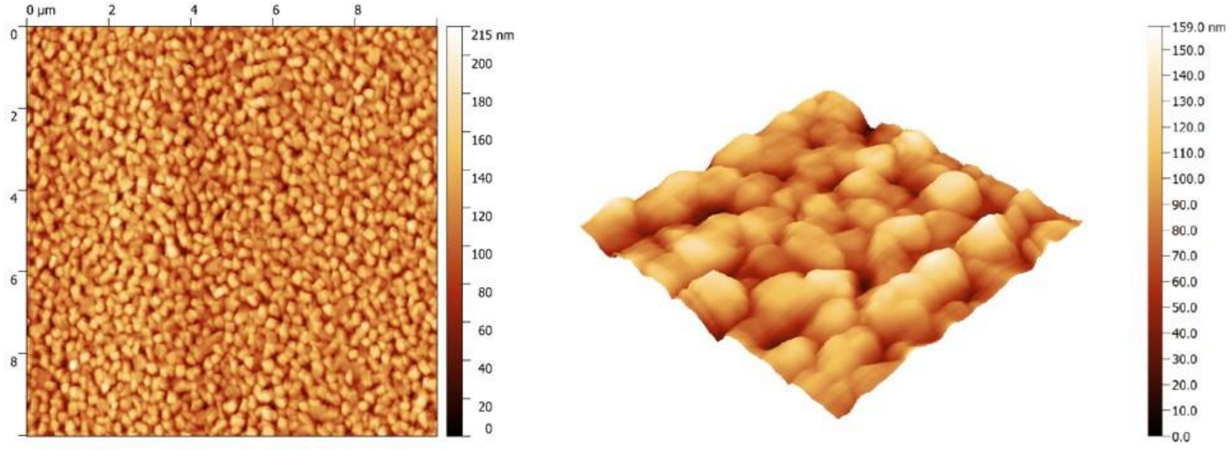

Figure 5- 12: Surface morphology of F_4TCNQ with a) 10 µm × 10 µm and b) 2 µm × 2 µm by AFM

The XTEM sample with F_4TCNQ/Si interface was prepared by a focused ion beam (FIB) lift-out process, and the interface morphology was then characterized by transmission electron microscopy (TEM) along Si [110], as shown in Fig. 5-13. The active Si layer is ~100nm in thickness, on a 2µm buried oxide layer, so that the subsequent transport measurements are minimally affected by the substrate. As shown in Fig. 5-13 a), continuous coverage of F_4TCNQ on Si was achieved, with an average thickness of ~150nm. In essence, only the first few layers of molecule would contribute to the charge transfer, leaving the majority as neutral F_4TCNQ bulk. Figure 5-13 b) is the high-resolution image along Si [110] axis. It exhibits a smooth interface without observable voids or interlayers. Therefore, an effective charge transfer can be expected across the interface. Nevertheless, the orientation of molecules on Si surface is still unclear, which could affect the transfer doping efficiency[159]. Future work using STM[161] or IR spectroscopy[157] techniques may shed light on orientation of the molecules

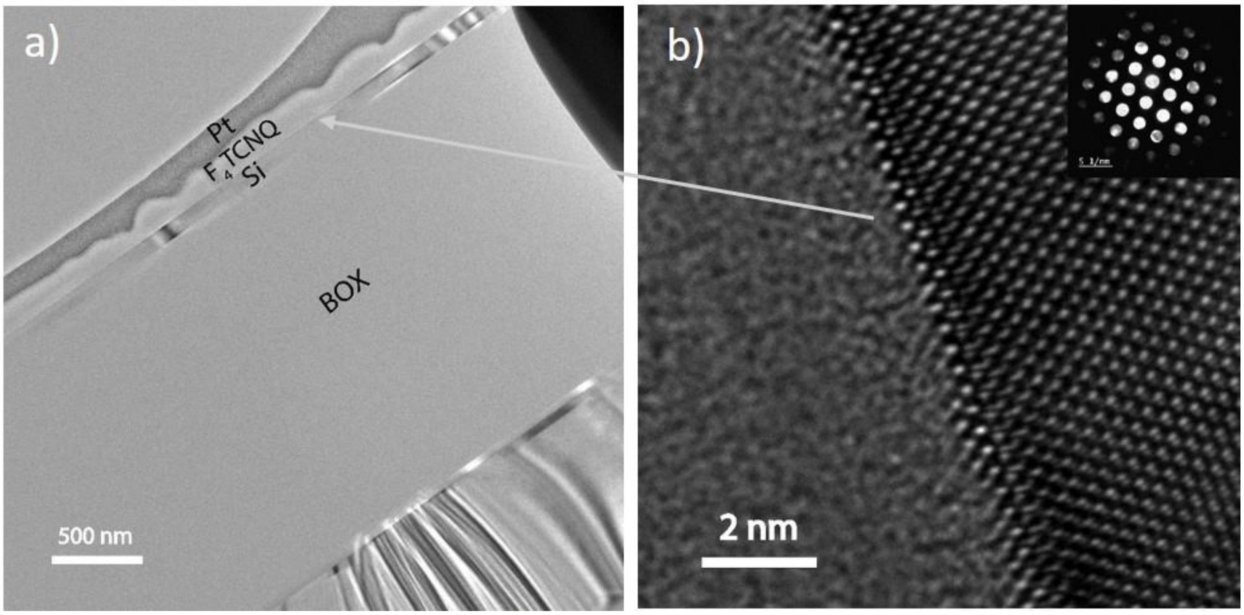

Figure 5-13: a) XTEM of the device by FIB lift-out, with each layer annotated; b) high-resolution TEM image of F_4TCNQ – Si interface along Si [110]. The inset shows the convergent-beam electron diffraction (CBED) pattern

5.2.3. Electric transport properties

In order to evaluate the charge transfer, and its effect on power factor, electrical transport measurements were performed. I-V measurements by the 4-probe method were conducted first on the mildly p-doped, uncoated Si device, and then on the same device deposited with F_4TCNQ. As shown in Fig. 5-14, Ohmic IV curves were achieved in both cases. The measured resistance of F_4TCNQ – Si (401kΩ) is 10 times lower compared to the resistance of plain Si device (4.36 MΩ). The result provides a direct evidence that charge transfer at the interface occurred and that silicon is surface doped by the physically adsorbed F_4TCNQ.

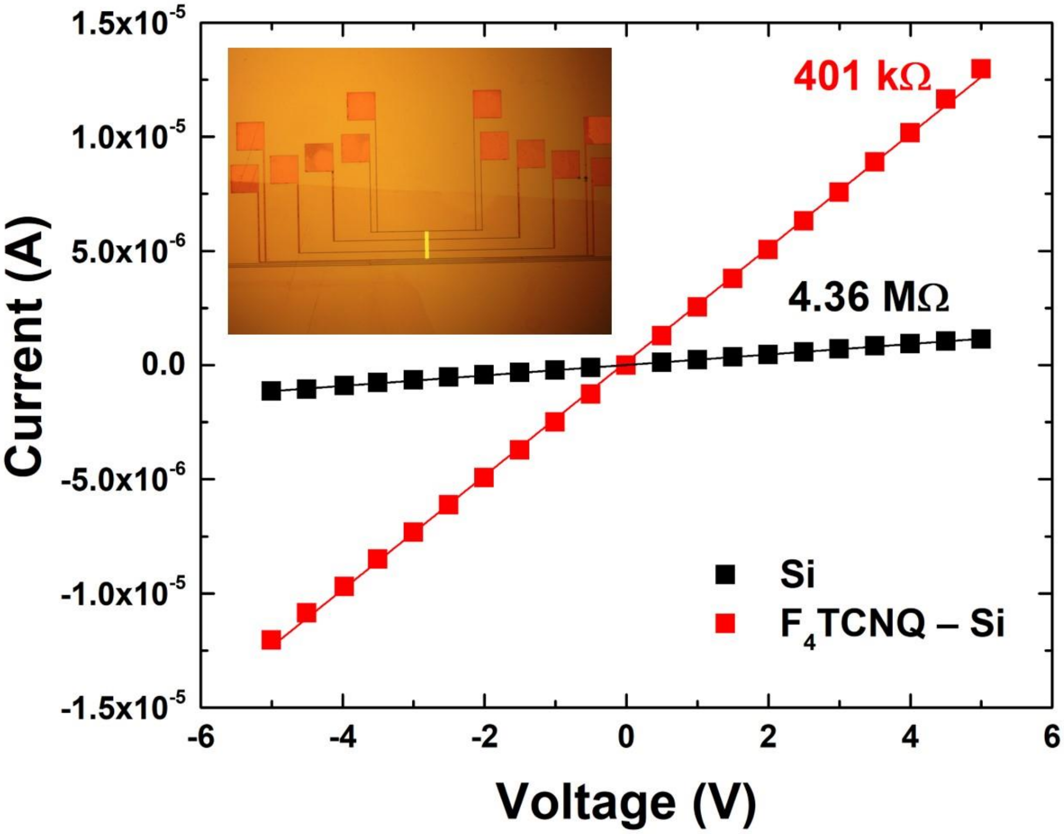

Figure 5-14: Comparison of IV curves for Si and F4TCNQ – Si device. The embedded figure is the optical image of the device partially deposited with F4TCNQ using a shadow mask

The Seebeck coefficient was then measured using a micro heater and two calibrated thermometers, as described in section 5.1.3. A large drop in the Seebeck voltage was observed from -208.9 ± 12.3 μV for mildly doped, uncoated Si to -73.9 ± 3.7 μV after deposition of F$_4$TCNQ (see the steady state voltage shown in Fig. 5-15 a). A minor increase of thermometer resistance after depositing F$_4$TCNQ was noted due to the presence of the molecules on the gold lines and therefore their resistances were recalibrated afterwards.

During the Seebeck measurement, when the heater turns on, the resistance (by 4-point method) of the thermometers ramps up as shown in Fig. 5-15 b) – e). Using the calibration curves, we could then extrapolate the ΔT ($TC_1 - TC_2$), which reached to a steady state after ~ 20 seconds, corresponding to the Seebeck voltage plateau. The Seebeck coefficients determined by this approach for the uncoated Si device is 594.6 ± 38.0 μV/K, and for F_4TCNQ – Si device is 243 ± 12.3 μV/K. The sign of Seebeck coefficients confirms that both devices are p-type doped. It was found that the power factor (S^2/R) of silicon had a 75% enhancement after depositing F_4TCNQ.

Since the screening length of surface-doped holes is estimated to be less than 10 nm, the majority of the coated device is not contributing to the conductance. Given that the resistance had 10 times' reduction, and carrier mobility should be unchanged in F_4TCNQ – Si, a ~100 times enhancement in hole concentration can be estimated in the modulation doped region in proximity to the interface. The obtained Seebeck value of 243 ± 12.3 μV/K for F_4TCNQ – Si sample, could be interpreted as the Seebeck coefficient of the 2D hole gas since the transferred charge accumulated near the surface is the dominant contributor to the Seebeck voltage. The thermal conductivity is not affected and we estimated a similar thermal resistance with and without F_4TCNQ since in this case, measurements are done for the interface and lattice thermal conductance of silicon is the dominant heat transfer mechanism.

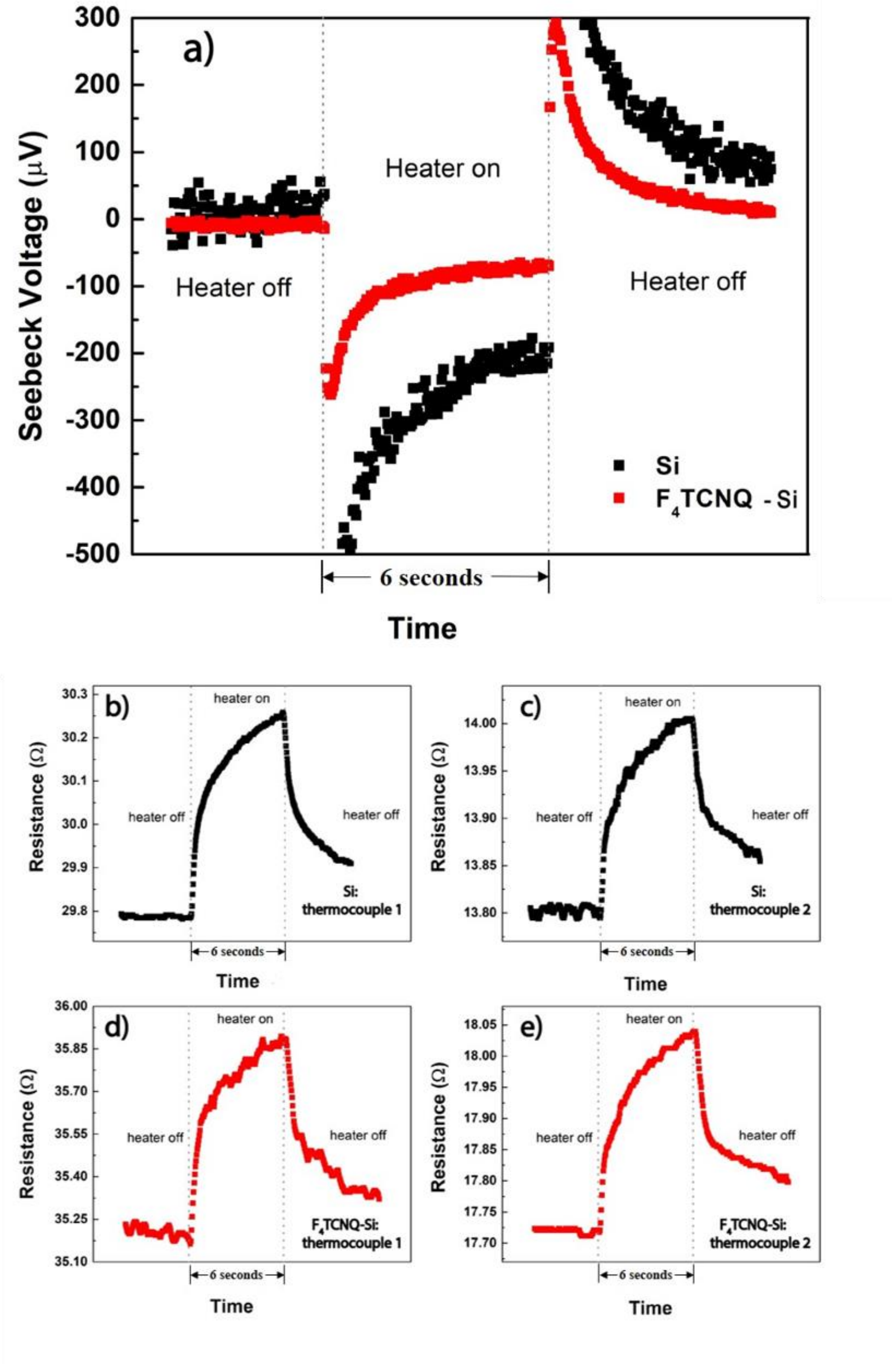

Figure 5-15: a) Comparison of Seebeck voltage for Si and F_4TCNQ – Si devices; b) – e) resistance curves of each thermometer when heater is on/off

5.3 Summary and perspective

The results in section 5.2 serve as a proof of concept of the potential of organic – Si interfaces with large charge transfer for power factor optimization for thermoelectric device applications. The issue of limited conductance enhancement due to the short screening length brings in the necessity of having holey Si with high surface-to-volume ratio, in which case the transfer doping can be maximized, and the necking size is comparable to the screening length of transferred charges so as to freely transport throughout the material. To achieve this goal, F_4TCNQ or other organic materials with large electron affinity need to be disposed in the nanosized holes, covering all the surface. To obtain a full step coverage on the such fine structures can be challenging in deposition, but should not be insurmountable. Manipulating the molecule orientation, and surface treatment to minimize surface states as charge trap is also expected to further enhance the power factor. Furthermore, thermal conductivity suppression by holey Si structure studied in section 5.1, along with the intrinsic low thermal conductivity (typically <1 W/m K) in organic materials make the hybrid nanostructured Si device very promising in thermoelectric device applications.

Chapter 6: Summary

Si-based bulk nanocomposite as well as nano-meshed thin-film materials for thermoelectric applications are studied in this dissertation, which includes the synthesis and structure/properties relationship of n-type β-$FeSi_2$ – SiGe nanocomposites; fabrication and thermoelectric transport of holey Si thin-film device; as well as transport properties of the F_4TCNQ – Si hybrid device utilizing organic – inorganic charge transfer as the doping mechanism. The goal of this dissertation is to understand the coupling between processing/fabrication, the resultant nanostructuring, and thermal/electronic transport.

First, I developed a novel React/Transform SPS approach, providing accelerated phase transformation (α-$FeSi_{2+\delta}$ → β-$FeSi_2$ + Si) and selective alloying (Si + Ge → SiGe) for efficient production of nanocomposites. Bulk, intrinsic β-$FeSi_2$ – $Si_{1-y}Ge_y$ ($(Fe_{29.4}Si_{70.6})_{1-x}Ge_x$) nanocomposites with x=0–0.1 were synthesized solely by solid-state reaction/transformation without mechanical alloying and post-annealing, with a final microstructure of 100–500 nm SiGe grains/clusters embedded amongst 200 nm β-$FeSi_2$ grains. The Ge composition in DC nanoinclusions is tunable with a broad tuning range of 0 ~ 42.5%, bound to the two-phase + DC equilibrium region in the ternary phase diagram. Ge additions of only a few atomic percent suppresses the thermal conductivities significantly, with a 38% reduction when $x = 0.07$. I successfully modeled the lattice thermal conductivity of the constituent β-$FeSi_2$ and $Si_{1-y}Ge_y$ phases separately by including phonon-phonon scattering, alloying scattering (in DC phase) and boundary scattering (size effect), and then averaging over the two phases to obtain the overall thermal conductivities. The concept of R/T SPS can be a promising alternative route for synthesizing self-assembled nanocomposite materials for thermoelectric applications.

Then, based on the R/T SPS synthesis approach, Co and P was introduced as n-type dopants selectively incorporated in β-$FeSi_2$ and DC phases. Sb was added to facilitate liquid-phase sintering, which essentially formed a wetting liquid (DC phase) along the β-$FeSi_2$ grain boundaries during sintering. As a result, a hierarchical structure is obtained with a mesoscale, percolated DC phase coexisting with nanoscale DC inclusions in the β-$FeSi_2$ matrix, along with selective doping of both constituent phases, that to a great extent decouples the thermal and electrical transport. An overall electron mobility at room temperature as high as 12 $cm^2/V\cdot s$, which is much higher than usually observed in this system for thermoelectric materials produced by powder routes, is suggested to be the result of parallel conduction paths in the percolated DC phase. An improved ZT of ~0.67 at 973K, with an average ZT of ~0.65 at a broad temperature range from 823K to 1073K was achieved in the β-$FeSi_2$ – SiGe nanocomposite. Both the material system and the methodology show promise in developing economic thermoelectric materials for potential industrial scale application.

In the second part of the dissertation, I demonstrated the fabrication, transport measurement methods, and thermoelectric properties of the p-type holey Si device by boron implantation. I extended the transport study of holey Si devices to elevated temperature range, which to our best knowledge has not been reported. A novel method to measure in-plane thermal conductivity of thin film materials using thermal reflectance imaging was successfully conducted. A ZT of ~0.08 at room temperature was obtained. We also designed and installed a cryostat coupled with thermal imaging system to extend the thermal conductivity measurements to high temperatures, so as to obtain ZT values at high temperatures. This holey Si sample serves as a control sample for the following investigation on the organics – holey Si hybrid device, which utilizes a non-destructive doping mechanism by charge transfer at the heterointerface. By fabricating a F_4TCNQ – *non-holey* Si device and studying its electrical transport, I successfully demonstrated the large charge transfer at the hybrid interface, which effectively p-type doped the Si surface. The power factor (S^2/R) of silicon had a 75% enhancement after depositing F_4TCNQ, and a ~100 times enhancement in hole concentration was estimated in the modulation doped region in proximity to the interface. To give a perspective for future study, undoped holey Si with high surface-to-volume ratio coated with F_4TCNQ is expected to maximize the transfer doping, and the necking size should be comparable to the screening length of transferred charges so as to freely transport throughout the material. To achieve this goal, F_4TCNQ or other organic materials with large electron affinity need to be disposed in the nanosized holes, covering all the surface. To obtain a full step coverage on the such fine structures can be challenging in deposition, but should not be insurmountable.

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