Techniques for Design of Temperature- and Interference-Robust Sub-100 nW Wakeup Receivers at Sub-GHz and Multi-GHz RF Frequencies

A

Dissertation

Presented to

the faculty of the School of Engineering and Applied Science

University of Virginia

in partial fulfillment

of the requirements for the degree

Doctor of Philosophy

by

Pouyan Bassirian

August 2020

APPROVAL SHEET

This

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Keywords: sensor networks, low-power RFIC design, wakeup receivers, temperature variation, interference suppression, impedance matching, microelectromechanical systems (MEMS).

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(ABSTRACT)

To achieve the exponential growth needed for a 1-trillion-node Internet of Things (IoT) in the next decades, innovative solutions are required to eliminate recurring battery replacement costs, enable reliable operation in environments with uncontrolled temperatures and interferers, leverage the massive communication infrastructure at sub-GHz and multi-GHz frequency bands, and reduce the overall system size. Ultra-low-power (ULP) chip-scale sensor nodes can enable decade-long lifetimes for low-cost cyber-physical systems. In event-driven cyber-physical systems with low activity factors, a sensor node's dormant-mode energy consumption can dominate its active-mode energy consumption over its operational lifetime. ULP wakeup receivers (WuRx) and wakeup sensors aim to overcome the lifetime limitations of ubiquitous IoT systems by minimizing their dormant-mode power consumption.

A WuRx is a critical block that keeps a sensor node connected while its main power-intensive transceiver is turned off to save energy for useful processing of information until an RF wakeup is received. Sub-100 nW ULP WuRx's promise energy-efficient operation for event-driven applications. However, the building blocks of these receivers are based on sub-threshold circuits that are susceptible to temperature variations. Until now, ULP WuRx's have favored sub-GHz frequencies due to the low quality-factor of passives at higher frequencies, which limit the receiver sensitivity. Also, sub-GHz ULP WuRx's rely on bulky discrete air-core inductors that are susceptible to electromagnetic interference.

This dissertation presents design techniques that demonstrate the feasibility of implementing temperature- and interference-robust sub-100 nW WuRx's at sub-GHz and multi-GHz RF frequencies using the envelope-detector-first architecture. The dissertation also demonstrates that microelectromechanical system (MEMS) resonators can provide substantial improvements over discrete-element matching networks for sub-100 nW WuRx's in terms of reduced size, robustness to interference, higher quality-factor matching, and immunity to electromagnetic interference.

The proposed techniques are implemented on several proof-of-concept CMOS chips that promise significant lifetime extension for power-constrained IoT systems, energy-efficient calibration methods for robustness to temperature and interference, high-sensitivity operation at sub-GHz and multi-GHz RF frequencies, and a reduction in system components size via co-designed MEMS and CMOS technologies.

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In college, I obtained my first hands-on experience with RF measurement equipment in the Microwave Lab at the University of Tehran under the supervision of Dr. Rashed. Dr. Rashed allowed me to work with graduate students in the lab even though I had no prior experience in the field. My work in the lab produced a publication that was helpful in my graduate school applications. Another influential professor was Dr. Shahabadi, whose intuitive teaching of Antenna Engineering brought together all the topics that I had learned until that point and solidified my electrical engineering knowledge. He also allowed me to audit two of his graduate-level classes and made himself available, sometimes late in the evenings, to answer my questions.

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Chapter 1

Introduction

1.1 Problem Statement

The Internet of Things (IoT) vision invokes a world in which connected computers are interwoven into all types of everyday items [1]. IoT systems can sense the physical world—from human bodies and household items to factories and cars—and send the collected data over a computer network to create a cyber-physical system (CPS). A CPS can process the collected information, learn from the data, interpret what it means, and communicate the desired control signals back to the environmental actuators. However, the idea of embedding computers into "things" is not a new invention. The computerized spacecraft that enabled the moon landing in 1969, the flight management system used in aircrafts since the mid-1970s, and the engine control unit (ECU) used in commercial vehicles since the 2000s are well-known examples of computerized objects. What makes the IoT special is that it aims to make sensing, computation, communication, and actuation ubiquitous throughout the physical world. The following analogy with electricity is helpful for understanding the purpose of the IoT. Electricity has granted a wide range of consumers access to a critical demand—energy. What electricity has done for energy is analogous to what IoT aims to do for information [2]. IoT systems can be used in a variety of applications (Figure 1.1(a)), including industrial monitoring [3], wearable electronics [4, 5], aerial monitoring [6], agriculture [7], smart homes and cities [8], and supply chain analytics [9].

The advent of low-cost and ubiquitous IoT systems is a result of a convergence in sensing technologies, machine learning, and computer networks [10]. The magic of semiconductor technology is that it can provide complex computation and communication chips for IoT systems at remarkably low cost. The first generation of digital computers made with vacuum tubes in the 1940s were so expensive that they could only be operated by governments and large corporations. The invention of the transistor in 1950, followed by the invention of the integrated circuit (IC) in 1958, revolutionized the computing industry by miniaturizing computers and making them economically feasible to fabricate and purchase. In 1965, Gordon Moore, one of the founders of Intel, predicted that the number of transistors on an integrated circuit chip would double every 24 months [11]. Moore's prediction turned into a driving force for the progress in the IC industry, and, by the early 2000s, the price of each transistor on an IC was one-millionth of what it was in the 1970s. Today, the cost of computation, measured in microprocessor cost per transistor cycle, is less than a ten-billionth of what it was four decades ago (Figure 1.1(b), (c)) [12, 13]. Thanks to the IC revolution, the computational capabilities of today's smart phones are greater than those of the super computers of the 1970s. A future with the IoT promises that the spread of computers into every facet of our lives is just getting started. The economic opportunities that will open up in the semiconductor industry due to the IoT market have the potential to exceed all the opportunities offered by prior classes of computers [14].

Another factor that motivates the ambitions of IoT is the growing value of data and information. Networks on which millions of humans share personal data, such as Facebook and Twitter, are worth billions of dollars. Similarly, a large network of objects that could collect and communicate useful information could also be extremely valuable. The trend in Moore's law suggests that access to more complex semiconductor products will become cheaper over time, and Metcalfe's law states that the value of a network of connected objects grows in a manner proportional to the square of the number of its nodes [15]. These two laws are the foundational incentives for economic investment in the IoT market.

While semiconductor technologies promise low-cost hardware for the backbones of ubiquitous IoT systems, the operating costs of such a large and distributed network threaten to be unsustainable. To achieve the ambition of the IoT, connected objects need to be deployed at tera-scale volumes [16]. However, accomplishing this goal in the next decades faces fundamental energy and economic challenges. To put this challenge in perspective, assume that the systems use 1.5 V 357/303H coin cell batteries [17]. If one trillion of these batteries were to be laid out edge-to-edge in a line, the line would be 30 times longer than the distance between the Earth and the Moon. Most importantly, the overhead cost of replacing the batteries can dwarf all other costs, including the cost of the semiconductor chips. Even if we assume that each battery replacement would take only one minute, doing a full round of one trillion replacements could provide full-time annual employment for about eight million people [18]. Therefore, such a massive deployment of IoT devices requires that nodes with decade-long lifetimes—or theoretically indefinite lifetimes—be designed that use a combination of energy harvesting and energy-efficient operation.

Fortunately, plenty of applications that are targeted by the IoT are event-driven, meaning that an individual sensor node spends the majority of its lifetime in a dormant mode, waiting to detect the ambient signature of an event or to perform a specific task after receiving an RF wakeup. For instance, the node might need to detect a chemical, infrared, or vibrational stimulus, or might respond to an RF wakeup with a temperature or humidity reading (Figure 1.2).

Ultra-low-power (ULP) wakeup receivers (WuRx) are critical in enabling a variety of emerging IoT applications, especially in terms of the development of distributed sensor networks. Advancements in wakeup receiver technology will enable the realization of large-scale, event-driven sensor networks with limited available energy resources and constrained operational agility that can last

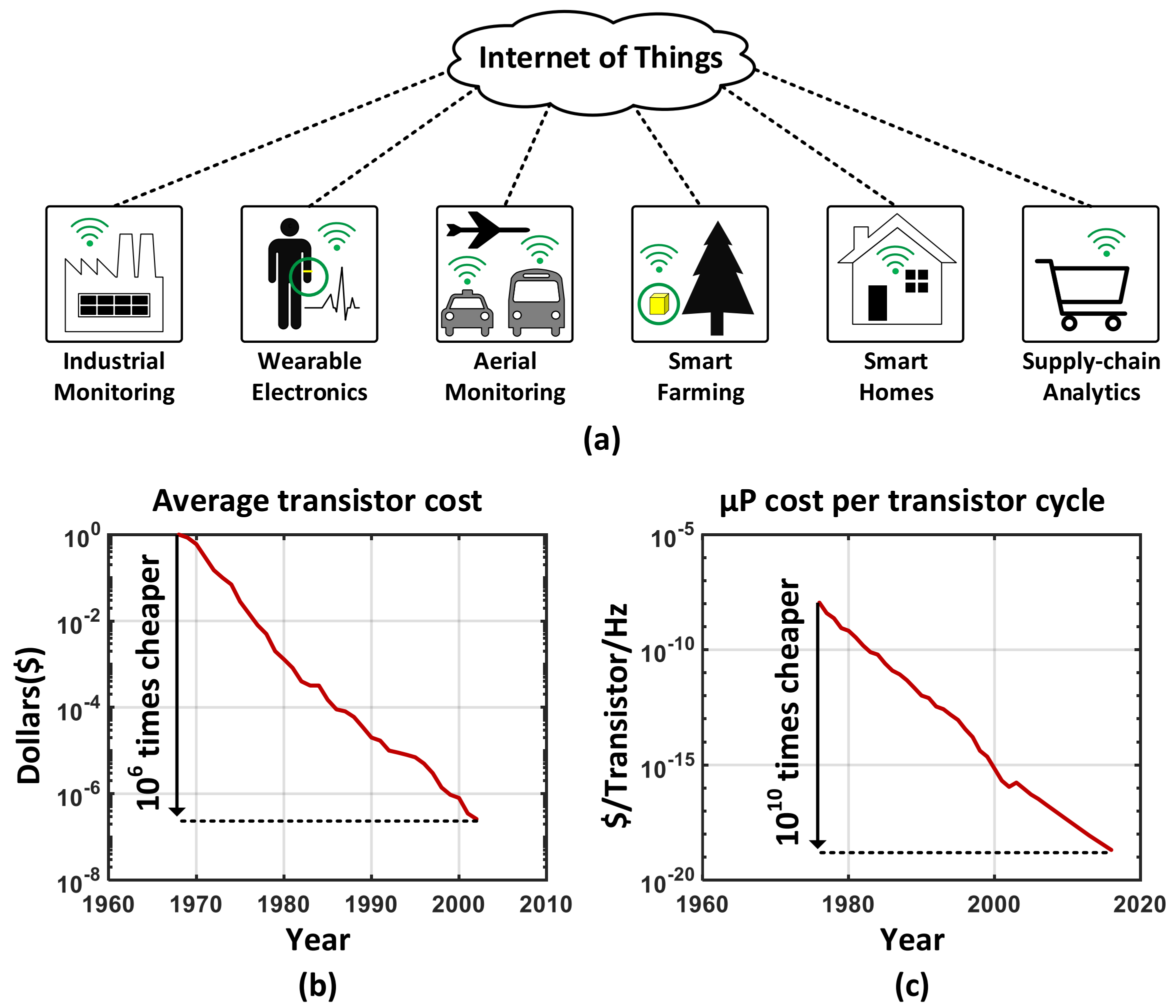


Figure 1.1: (a) Application space for the Internet of Things. (b) The trend in the average cost of a transistor over the past decades. (c) The trend in microprocessor cost per transistor cycle over the past decades.

several years without maintenance, and operate indefinitely on energy harvested from the environment [19]. The WuRx—or the wakeup sensor—in each node, as indicated in Figure 1.2, listens for infrequent ambient stimuli or RF wakeups to power up the rest of the node, either for taking additional sensing measurements or to communicate with other nodes in the network. Until such a signal is issued, the rest of the node remains dormant; hence, the wakeup receiver is the dominant power consumer in the node. Therefore, it is imperative that it consumes as little power as possible [20].

To achieve sensor node lifetimes of several years without battery changes, one solution is to increase the battery capacity. However, increasing the battery capacity results in increases in the

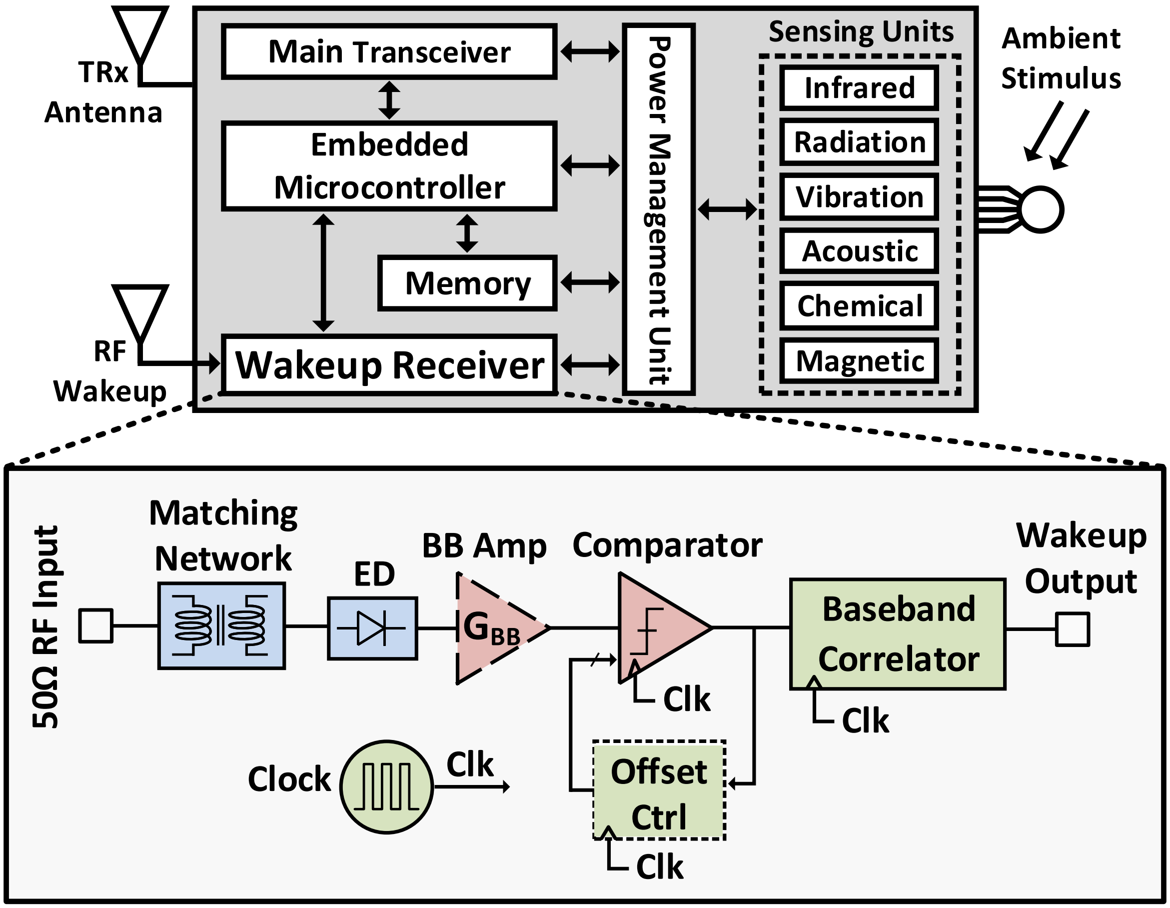


Figure 1.2: Conceptual system block diagram of a smart IoT sensor node and the system-level architecture of state-of-the-art sub-100 nW wakeup receivers. The sensor node consists of a variety of sensing modes, a power management unit, embedded digital processing, a main transceiver, and a wakeup receiver.

battery and system sizes. Alternatively, for a given battery size, the battery lifetime can be increased via a more energy-efficient system design. Therefore, this work focuses on reducing the power consumption of a system's dormant mode to the order of the battery self-leakage rate, which can be as low as tens of nanowatts [21]. Any improvement below this limit has extraordinarily diminishing returns in terms of lifetime extension for battery-powered systems.

This research presents fundamental analyses and design techniques for reducing the size and power consumption of the ULP WuRx's and improving their robustness to temperature variations and interference in a wide range of the RF frequency spectrum. In particular, it presents: 1) design-oriented analysis, modeling, and fundamental detection limits for Dickson envelope detectors, 2) the analysis and design of fault-tolerant wakeup codes, 3) techniques for achieving sub-100 nW

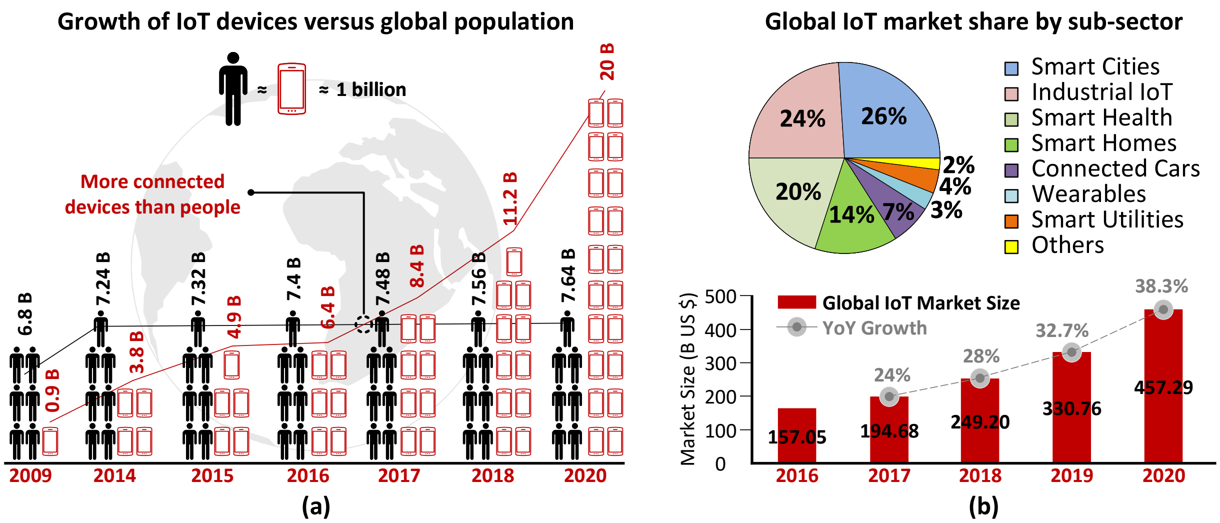


Figure 1.3: (a) The growth in the number of IoT devices versus the global population over the past decade. (b) Share of sub-sectors in the global IoT market, and its year-over-year (YoY) economic growth rate. [Source: Gartner / World Bank]

WuRx's for sub-GHz to multi-GHz frequencies, 4) energy-efficient calibration techniques that enable robust functionality across temperatures and in the presence of blockers, 5) co-design techniques for envelope detectors with MEMS-based matching networks enabling significant size reductions at sub-GHz frequencies and the optimization of the WuRx signal-to-noise ratio (SNR), and 6) co-design techniques for envelope detectors with matching networks that are based on discrete air-core inductors to optimize the WuRx SNR.

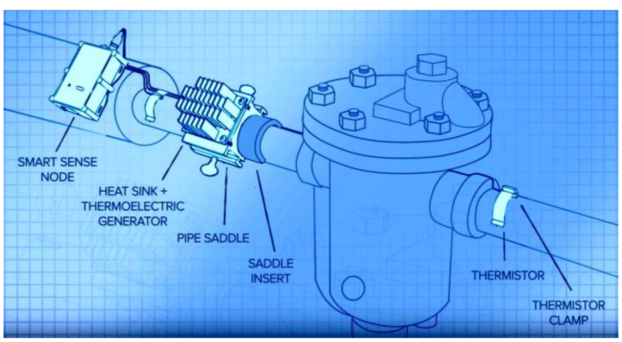
1.2 Significance of the Research

Recent trends in the growth of the IoT devices indicate that connected devices already number in the billions (Figure 1.3) and currently outnumber people by a factor of two to three. Retreating from the original prediction of 50 billion devices by 2020 [22], current projections suggest that there will be around 20 billion IoT devices by 2020 [23] and 125 billion devices by 2030 [24]. The economic trends in the IoT market over the past decade indicate that the IoT market has been growing by about 20% to 30% a year [25]. Smart cities and industrial IoT each account for about one quarter of the market, followed by smart health, which accounts for one fifth of the market. This section presents some promising IoT applications that can benefit from ULP WuRx technology and also focuses on the rationale and motivation behind the system-level design objectives put forth in this dissertation.

1.2.1 Applications of Ultra-Low-Power Wakeup Receivers

Industrial Internet of Things

The goal of industrial IoT (iIoT)—also known as industrial monitoring and machine monitoring—is to replace preventative maintenance (PM) with predictive maintenance through the continuous, data-driven monitoring of industrial equipment. The iIoT could have a significant impact on the efficiency and safety of manufacturing environments by providing insights into the condition of various equipment. Manual inspection of industrial equipment is labor-intensive and can be prone to observation errors. Alternatively, continuous, data-driven monitoring is highly scalable, cost-effective, and can maximize the lifetime and production uptime of critical equipment by collecting the performance and utilization data from complex machinery, such as steam traps and motors (Figure 1.4). Industrial settings are enriched with dissipated energy in the form of light, heat, and vibration that can be harvested using photo-voltaic (PV) cells, thermoelectric generators (TEG), and vibrational energy harvesters. This harvested energy can then be used to sustain ULP chips.



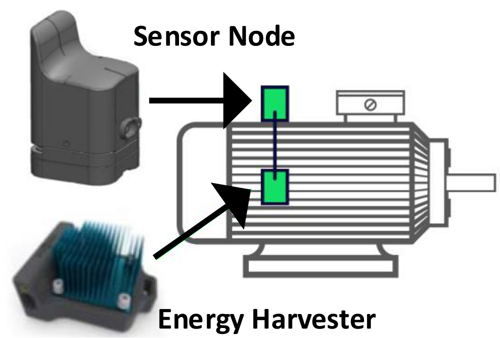


Figure 1.4: Examples of wireless iIoT sensor nodes for monitoring (a) steam traps [26] and (b) motors [3].

In the manufacturing sector, one application that has gained significant momentum is monitoring motors via ULP sensor networks. An estimated 300 million motors are installed globally that account for 70% of manufacturing electricity usage [3]. Some common motor failures include: 1) damaged mounting piece or bearings, which can both cause undesired vibrations and increase safety risks; 2) loose windings or shorted windings due to the corrosion of insulation, which can create unexpected vibrations and heat loss; 3) excessive exposure to high temperatures or humidity in uncontrolled environments, which can reduce the lifetime of the motor; and 4) under-lubrication, which results in excessive heat, friction, and safety hazards and reduce the motor's lifetime [27]. The System-on-Chip (SoC) reported in [3] is an example of a motor monitoring system that can support near-real-time motor parameter readings with regards to temperature, relative humidity, magnetic field, vibration, and so forth. The SoC also has limited edge processing to reduce the amount of data communicated, and consequently its power consumption, because data transmission is a power-intensive task for ULP nodes. For example, the vibrational or acoustic data generated by a motor can be processed by a Fast Fourier Transform (FFT) processor to detect anomalies in its performance [28–30]. The cloud-based platform uses an event-driven WuRx instead of a duty-cycled synchronized data transceiver to reduce the dormant power consumption of the SoC substantially. Unlike cellular applications, in which cellphones receive precise timing information from the base station, synchronized low-power MAC protocols require each dormant node to keep track of time with an accurate internal real-time clock. Since the internal clock drifts over time, the nodes need to wait through a guard time period before transmitting their data. This guard time is directly proportional to the duty-cycle ratio and results in a power-latency trade-off [31]. In iIoT applications, data transmission can be on the order once every tens of minutes, which is not suitable for synchronous protocols. Alternatively, the proposed event-driven protocol in [3] can be scaled to thousands of devices.

Wearable and Implantable Electronics for Healthcare

Using wearable IoT devices to diagnose, monitor, and treat health conditions [32] is an emerging application that envisions providing gap-free, quality care for individuals in any location, reducing unnecessary visit costs, and eliminating variability in care. Wearables can replace point-of-care devices to monitor physical, electrical, or chemical attributes of the human body [33] during athletic activities, daily activities, and sleep (Figure 1.5). Since wearable devices need to be integrated seamlessly with everyday items, they must be designed in compact form factors—that can be enabled by MEMS integration at sub-GHz and small antennas at multi-GHz frequencies for WuRx's. Due to the high attenuation of human tissue at higher frequencies, sub-GHz frequencies are more suitable for biomedical applications. One of the major challenges in designing wearables is that unlike in controlled medical environments, the measurements taken by these devices suffer from motion artifacts, environmental interference, and low-quality sensor interfaces.

Non-invasive wearables can measure human physiology and medically important parameters including: 1) physical attributes such as motion [36], temperature [37], respiration rate [38], and social interactions [39]; 2) electro-physiological attributes such as heart rate (ECG) [40], brain activity (EEG) [41], and muscle activity (EMG) [42]; and 3) physiochemical attributes such as glucose [43], lactate [44], blood oxygenation [45], and blood alcohol concentration (BAC) [46]. The most well-known examples of non-invasive wearables are the commercialized wrist wearables such as smart watches and fitness bands. Wrist wearables are mainly used to measure physical parameters, such as motion, while wearable patches can provide further insight into electro-physiological and physiochemical parameters such as ECG and body fluids. Wearables can also be used as home-based patient compliance monitors. The research in [35] presents a strain sensor that monitors the swallowing activity of patients with neck and head cancers after radiation therapy to prevent the atrophy and fibrosis of the swallowing muscles caused by disuse. Current research is focused on making non-invasive wearables less visible to the users by integrating them into everyday items, such as antennas that are shaped like buttons [47] or medical patches that look like tattoos [46].

Implantable devices (IMD) promise more accurate insight into parameters that cannot be measured

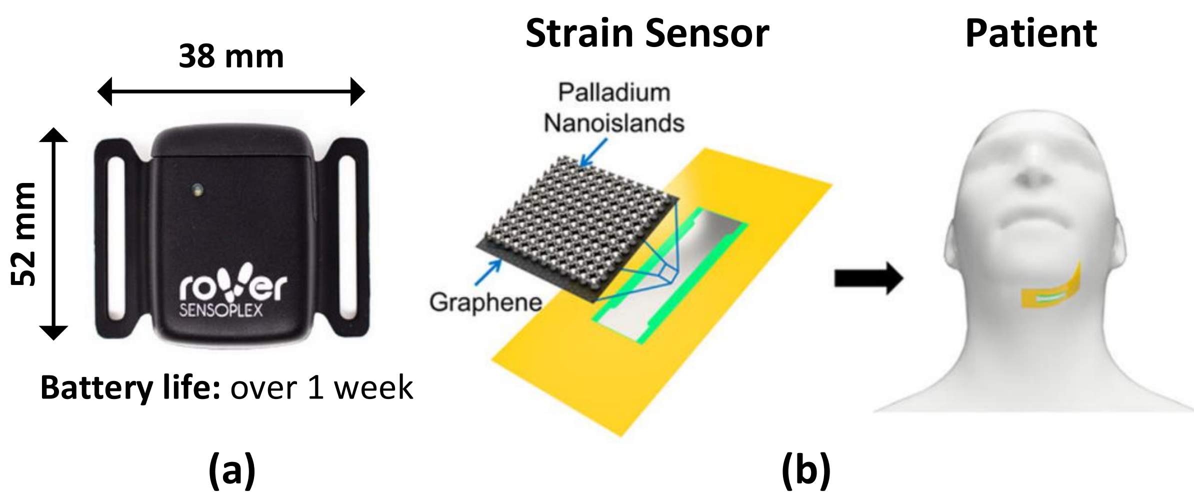


Figure 1.5: (a) Wearable fall risk monitoring device [34]. (b) Patch to monitor the swallowing activities of patients with neck and head cancers after radiation therapy [35]. Researchers aim to make wearables less visible to the users and extend their lifetimes.

effectively by non-invasive methods. Designing IMDs faces two major challenges. First, an IMD needs to be small enough to make it compatible with human anatomy and avoid damage to human tissue. Second, the power consumption of an IMD needs to be low to comply with safety regulations and avoid increasing the temperature of local body tissue [48]. Since low-power consumption has the potential to enable wireless power delivery and the elimination of the battery in some applications, these challenges are entangled to some degree. IMDs can be used in a variety of medical applications, including: 1) injectable IMDs for heart condition [49] and pressure [50] monitoring; 2) encapsulated endoscopes [51, 52] for the diagnosis of digestive and gastrointestinal diseases; 3) wireless drug-delivery implants [53], which can control the therapy parameters and release of a specific drug to increase its efficacy—implants that can navigate through the bloodstream and release their payload at a specific location [54] promise improvements in medical treatments by focusing the drugs on the problematic areas and minimizing disturbance to the rest of the body; and 4) early seizure detection and neural stimulation for the treatment of neurological disorders such as Parkinson's Disease, dystonia and epilepsy [55].

Environmental and Aerial Monitoring

Environmental monitoring involves collecting ambient information, such as acoustic, gaseous chemical, light, temperature, and motion readings, from nodes that can be placed on the ground, humans, and vehicles. The information acquired from the nodes can be used for security, surveillance, and infrastructure monitoring to increase situational awareness. For example, the sensor data can be used to enhance fire safety in critical infrastructure, detect intruders in high-security zones, and detect hazardous gas in industrial or military settings. An early generation of sensor networks with similar missions were used in the Cold War era. For instance, during this time,

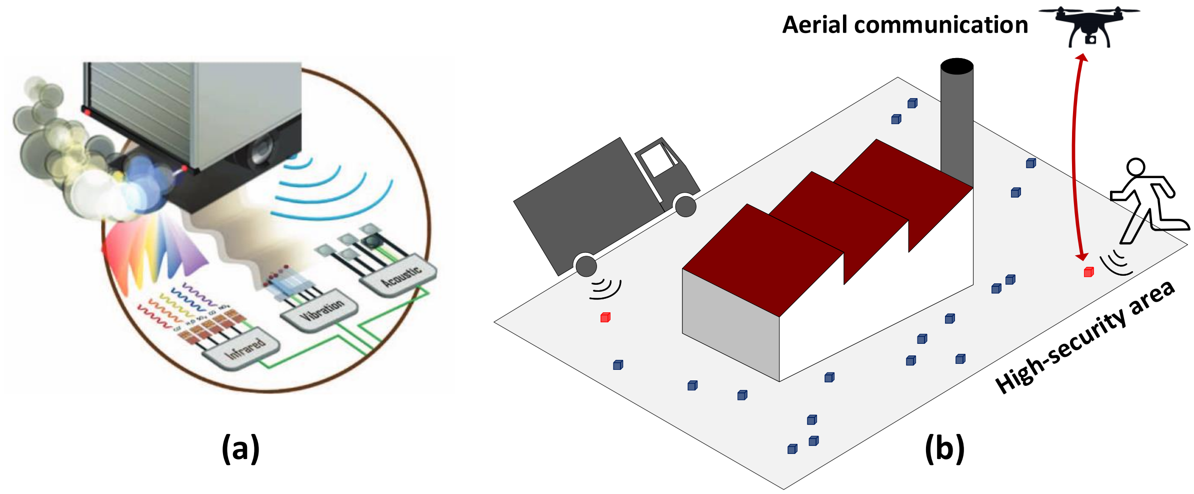


Figure 1.6: (a) Sensor fusion enables more robust decisions by combining the information acquired from different sensors [20]. (b) Example of a sensor network used for environmental monitoring around a high-security area.

the US government deployed an under-water network of acoustic sensors (hydrophones), named the Sound Surveillance System (SOSUS), to help detect the presence of Soviet submarines [56]. Today, SOSUS is used by the National Oceanographic and Atmospheric Administration (NOAA) for studying seismic activity and the habitats of marine mammals [57]. These early networks were expensive to maintain; therefore, they were operated mainly by governments.

The research program Near Zero Power RF and Sensor Operations (N-ZERO) proposed by the Defense Advanced Research Projects Agency (DARPA) in 2015 sought to expand the use cases of sensor networks by developing ULP sensors and RF technologies [20]. During this program, several research groups focused on developing wakeup sensors and WuRx's with sub-100 nW power consumption levels. The wakeup sensors developed include acoustic sensors, infrared photo-detectors, accelerometers, vapor sensors, temperature sensors, and a vibration, acoustic, magnetic, and rotation sensor [58–65]. MEMS and CMOS are the two key technologies used in the implementation of these systems.

As illustrated in Figure 1.2, an N-ZERO node consists of a variety of sensing modalities and a WuRx. The responsibility of the WuRx is to keep the node connected to the network so that the base station can send a request for a specific measurement, make a change in the node setting, or simply ping the node to see if it is still functional when the node is dormant. Meanwhile, the sensors are responsible for waiting for the desired environmental stimulus. For example, assume that a sensor network is deployed for monitoring a high-security area, as illustrated in Figure 1.6, to report the presence of intruders such humans, cars, or trucks. Therefore, the sensors would be interested in the infrared signature of a truck engine, the vibrations caused by movement, or the acoustic signatures of humans and vehicles. The node can use sensor fusion, which means that it makes a more robust decision by combining the information acquired from different sensors. Once the node has gathered its data, the data can be transmitted to a central control unit for further assessment through an airborne or a ground-based link.

Agricultural Internet of Things

There is a tremendous opportunity for sensor networks to transform current agricultural practices through the enhancement of productivity, work efficiency, and profitability while mitigating negative environmental impacts [66]. These networks require sensors that monitor environmental conditions, such as soil temperature [67], moisture [68], and salinity, [69] and communicate this data for management decisions such as irrigation planning, targeted pesticide delivery, and crop disease risk evaluation [66].

Recent advances in agriculture have addressed the global increase in the demand for food production with pesticides, fertilizers, and genetically modified organisms (GMOs) [70]. However, modern agricultural practices face serious challenges [71] such as climate change [72–76]; water shortages [77–79]; labor shortages due to an aging, urbanized population; soil erosion; and increasing societal concern regarding food safety and environmental impacts [80]. Increased carbon dioxide levels have been shown to alter the micro-nutrient contents of grains [72], and increases in average temperatures can affect production yields [81]. Furthermore, more efficient water management systems and strategies are required to sustain food production, as current practices have already exhausted surface and ground water resources [77, 78, 82].

Agricultural IoT (AIoT) refers to the deployment of technology for collecting critical information that increases situational awareness of the states of pastures, animals, and farms. These technologies can contribute to soil analysis, fertilizing, field sensing, cattle breeding and production management, and environmental controls for greenhouse horticulture [86]. Fujitsu [87] has been a pioneer in promoting smart farming and has over 40 years of experience in the field. Their efforts have focused on the utilization of information communication technology to engage young producers and prevent the loss of cultivation knowledge. They have made improvements in terms of management, production, and sales. Their data analysis platform “Akisai” collects real-time environmental data such as temperature, humidity, sunlight, and rainfall. This information is then processed to generate management decisions. Used by more than 400 agricultural corporations, the platform has resulted in promising outcomes such as a 14% increase in work efficiency at a rice farm, three-fold increase in an orange farm’s harvest, 30% increase in the crop harvest at a cabbage farm, and 30% increase in the annual harvest of a greenhouse strawberry farm [84].

Another example in this field is the SoC developed by Intel [88], which consists of a WuRx, processor, neural network, cryptography engine, memory, transceiver, power management unit, and camera. This SoC is designed for the controlled release of pesticide targeted at a specific species of moth. To achieve this goal, the system’s camera faces a glue trap sheet and takes images of the sheet during the day. Each node then processes these images with its convolutional neural network (CNN) to determine the number of the trapped targeted moths. Once a day, this information is collected by drone from all the nodes and used to estimate the moth population and create a schedule for the release of pesticides. The power-intensive transceiver of each node is on

Figure 1.7: Commercially available sensing nodes: (a) the Fujistsu temperature and humidity monitoring station [83], (b) Kinki University's ubiquitous environmental control system [84], (c) Stevens Water soil monitoring station [85]. The installation and maintenance costs of these bulky stations make them unaffordable for small and medium-sized farms.

for only about 10 seconds each day when communicating with the drone. Therefore, the SoC can produce economic benefits by reducing the amounts of required chemicals and labor required and can diminish the negative environmental impacts of modern agriculture.

Despite their promising outcomes, the main limitation of these existing solutions, shown in Figure 1.7, is that they are too expensive to use on small or medium-sized farm, and too large to be deployed at higher densities. The sensors cost on the order of several hundred dollars [84], they are bulky [83], and need to be carefully installed and maintained. Therefore, despite their positive financial and environmental impacts, the ultimate profit margin is too narrow for small farms to make these sensors economically sustainable. In order to improve cooperation among farmers, these systems need to become more compact, more easily deployable, and cheaper in terms of cost per node. ULP cyber-physical sensor networks can enable affordable smart farming for all farmers by reducing or eliminating installation fees and reducing the hardware costs of these systems.

1.2.2 Motivations and Design Objectives

So far, the previous sections have explained the application-level needs for WuRx's in various fields. This section describes the motivations for the design objectives, including sub-GHz and

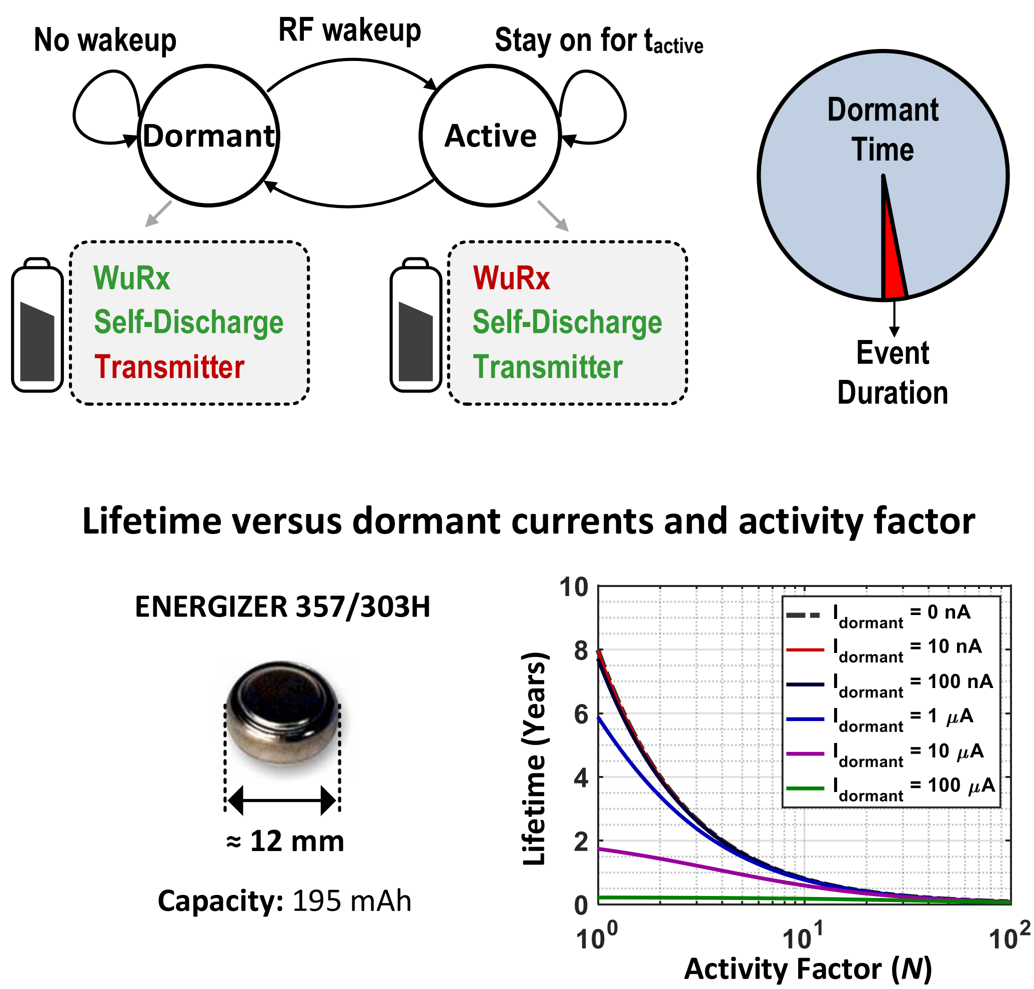


Figure 1.8: Reducing the dormant-mode power consumption to battery self-leakage rates in an infrequent event-driven scenario can increase the node lifetime to several years.

multi-GHz operation, chip-scale system size, and robustness to temperature and interference, in more detail. The section also highlights the rationale for achieving all the objectives listed above with less than 100 nW of power. The goal of the following analysis is to find the lower limit of WuRx power consumption that remains practically useful in most applications. Two cases are studied; the first case is a battery-powered system, and the second case is an energy-harvesting system. In mission-critical applications where the node redundancy for obtaining information is insufficient, the energy harvesting source is unreliable, or the continuous operation of every single node needs to be guaranteed, battery-powered systems are preferred to those that rely solely on energy harvesting. A system can also be designed to use both of these sources of energy to enhance reliability.

To illustrate the advantage of sub-100 nW power consumption in event-driven, battery-powered scenarios, consider a hypothetical case in which a 357/303H coincell battery [17] with a total capacity of $Q_{bat} = 195\ mAh$ and an internal leakage current of $I_{leakage} = 10\ nA$ is used [89]. Assume that the node consumes the current $I_{dormant}$ from the battery during its dormant mode, and, after receiving a wakeup signal, the node switches to the active mode for $t_{active} = 10\ s$ and draws $I_{active} = 1\ mA$ from the battery during this period. Assuming that N is the activity factor of the node, which is defined to be the number of wakeup events that occur in an hour, the lifetime of the node (T_{bat}) can be written as

$$T_{bat} = \frac{Q_{bat}}{N t_{active} I_{active} + (1 - N t_{active}) I_{dormant} + I_{leakage}}. \tag{1.1}$$

Figure 1.8 plots the node's lifetime versus activity factor and dormant mode power consumption. These plots indicate the significance of dormant-mode power consumption in an event-driven scenario, as the lifetime can be on the order of several years if the dormant power use approaches the sub-100 nA range. For the values smaller than $I_{leakage}$, the battery leakage itself becomes the dominant factor in determining the lifetime. Therefore, designing sub-100 nW event-driven systems provides tremendous opportunities for lifetime-constrained IoT devices.

The second case study is illustrated in Figure 1.9. Suppose that the system relies solely on the harvested energy from an indoor solar source and that the system state machine is similar to the one with active and dormant modes used in the previous example. The required PV cell area for continuous operation of the system can be calculated with

$$PV\ Area = \frac{N T_{on} I_{on} + (1 - N T_{on}) T_{dormant} + I_{leakage}}{I_{harvest}}. \tag{1.2}$$

The required solar area for continuous operation versus the activity factor is plotted for different dormant power usages in Figure 1.9. The results indicate that when its dormant power consumption is on the order of hundreds of nanowatts, a mm-sized solar harvester can support continuous operation of the node. Meanwhile, the available energy from other harvesting sources, such as industrial heat, outdoor light, or industrial motion, can be several orders of magnitude greater than that available from indoor solar [90, 91]. Therefore, in applications with higher available harvesting energy, even higher levels of WuRx dormant power may be suitable. Overall, in both cases, a dormant power consumption on the order of tens of nanowatts is the lowest justifiable number that has practical value. Note that in addition to the WuRx, this power budget counts towards the power consumption of all wakeup sensors as well.

While some emerging or future applications could call for a further reduction in dormant power consumption, there are additional challenges that circuit designers need to consider. The first challenge pertains to the reliability of the electronic hardware. The average lifetime of transistors in modern CMOS technology is around a decade when they operate on the nominal voltage supply level. Therefore, power consumption is not the only bottleneck for extending the lifetime of such systems beyond a decade. The second challenge involves the protective circuitry necessary for

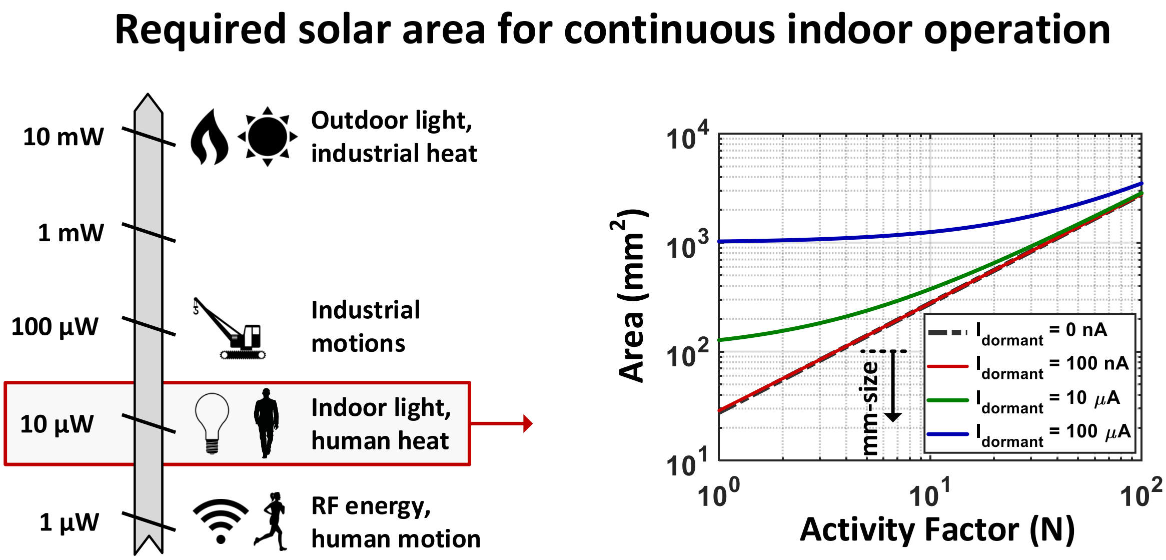


Figure 1.9: In a node that uses energy harvesting as the primary source of power, reducing the dormant power to hundreds of nanowatts is sufficient for continuous operation with a mm-sized solar harvester that uses indoor light.

the WuRx to ensure the robustness of its electronics to electrostatic discharge (ESD). An ESD protection circuit usually includes at least one large device in the supply clamp to provide a low-impedance current path for the ESD current [92]. This device in the supply clamp can leak several nanowatts of power under normal operation. Therefore, these two challenges also need to be addressed to reduce the power consumption further.

Additionally, reducing the size of the wakeup receivers can enable sensing in locations in which smart devices have not been present before. In particular, applications that involve attaching sensors to humans, such as wearables and biomedical implants, can benefit significantly from receiver compactness. The Friis equation suggests that the power received by an antenna is directly proportional to its aperture size $A_{eff,R}$, as follows

$$P_R \propto \frac{P_T G_T}{4\pi d^2} \times A_{eff,R}. \tag{1.3}$$

In the above equation, P_R is the received power; P_T and G_T are the transmitter antenna power and gain, respectively; and d is the distance between the receiver and transmitter. Since A_{eff} is proportional to the wavelength, it is easier to achieve greater A_{eff} at higher frequencies for a given area [93]. Moreover, the MEMS resonators that are widely used as RF filters [94] offer a promising solution to be used as matching networks [95]. MEMS resonators have a small form factor and allow for tight packaging with CMOS integrated circuits. Furthermore, compared to discrete element matching networks, they can achieve considerably higher Q matches (several hundred versus $<$50).

Finally, ensuring robust operation during temperature swings and in the presence of interference is another critical aspect that a receiver design needs to address for real-world applications. In general, most IoT systems are exposed to environments with variable temperatures, such as factories, outdoor environments, or the exterior of the human body. A possible exception to this general rule is an IMD implanted inside a human body, where the temperature does not vary a lot. There is no general solution for ensuring temperature robustness, especially at such low power levels. The sensitivity of sub-threshold circuits to temperature variations is a prominent effect due to the exponential dependence of the transistor currents on the threshold voltage, which is a function of temperature [96]. Also, it is critical for a WuRx to maintain its basic functionality in cluttered RF environments; otherwise, the entire sensor node will be effectively disconnected from the network. Interference can degrade the sensitivity of a ULP WuRx significantly and must be diminished through power-efficient methods.

1.3 Background

The number of connected nodes in the IoT is rapidly increasing, resulting in a plethora of new applications and technological developments, and ULP chip-scale sensor nodes are essential components for accomplishing the IoT vision. This communication paradigm requires ubiquitous and unobtrusive sensors with digital identities that can sense the environment, interact with each other, and respond to a central cloud, all without the need for battery replacements. Sensor nodes with sub-100 nW power consumption can bring about the decade-long lifetimes that are required in event-driven cyber-physical systems. In event-driven scenarios, a sensor's sleep-mode energy consumption can dominate its active-mode energy consumption over its operational lifetime. Therefore, it is desirable to reduce the sleep-mode power consumption to the battery self-leakage rate level, which can be on the order of tens of nanowatts, in order to extend the lifetime of a sensor node from weeks to several years.

To operate within such a stringent power budget, low-power wakeup receivers have favored simple modulation schemes, such as on-off-keying (OOK), that do not encode any information in the signal phase. Wakeup receiver architectures are mostly inspired by classic data receiver architectures, such as the super-heterodyne topology, as shown in Figure 1.10. These architectures include the duty-cycled heterodyne, the mixer-first or uncertain-IF, the LNA-first, and the ED-first topologies. In this section, we explore the performances and limitations of these topologies.

The required sensitivity for a wakeup receiver depends on the type of network that it is being used in. For a wakeup signal at 1 GHz that is issued from an airborne station with a transmitted power of 1 W, -60 dBm of sensitivity corresponds to a station-to-node range of 1 km. In the same network, a sensitivity of -80 dBm to -100 dBm corresponds to a station-to-node range of 10 km to 100 km. Alternatively, in a ground-based sensor network with a node transmitted power of 10 mW and $1/d^4$ multi path loss, -60 dBm, -80 dBm, and -100 dBm sensitivities correspond to 10 m, 30 m, and 100 m node-to-node ranges, respectively [97].

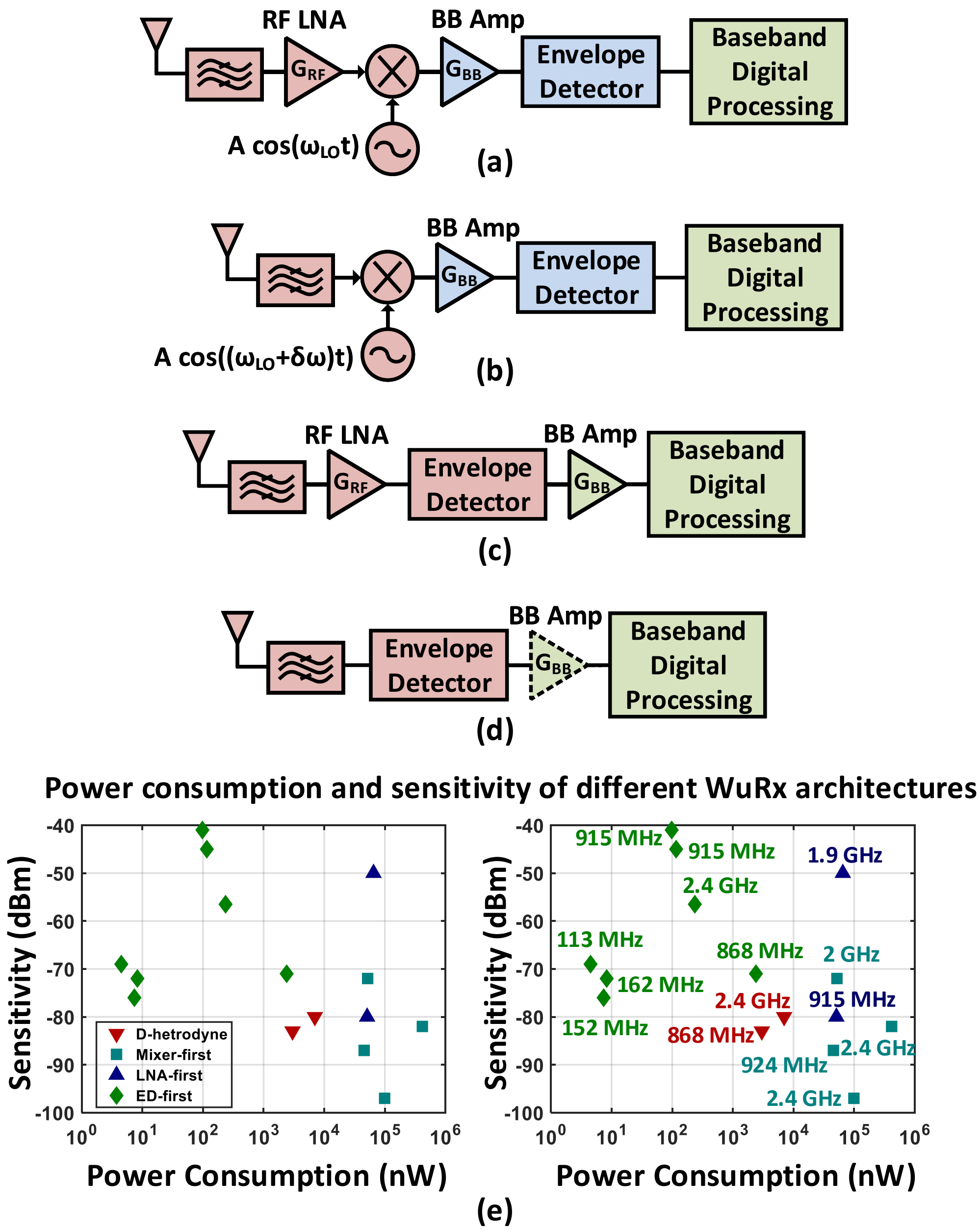


Figure 1.10: Block diagrams of various topologies used in the wakeup receivers: (a) duty-cycled super-heterodyne, (b) mixer-first (uncertain IF), (c) LNA-first (tuned RF), and (d) ED-first with or without baseband amplification stage topologies. (e) Scatter plots of the performances of the low-power wakeup receivers, as categorized by their architecture.

Figure 1.10(a) shows the heavily duty-cycled super-heterodyne receiver topology. The blocks used in this architecture need to be designed for fast start-up and settling times since they need to be powered up and down periodically. Implementing this system provides flexibility with regards to the operation frequency and enables the designer to take advantage of all the options offered by this topology. Duty-cycled systems usually suffer from an energy-latency trade-off [98] but are advantageous in applications where high sensitivities (e.g. <-100 dBm) are required and the WuRx's power consumption does not significantly reduce the system's lifetime. The reported power consumptions for this architecture are on the order of a few microwatts [99, 100].

Figure 1.10(b) shows the mixer-first or uncertain-IF topology. The main limitation of this architecture in terms of achieving an integrated low-power system is the need for a high-frequency local oscillator (LO) with LO drivers. Due to the high power consumption needs of RF oscillators, the LO is not designed for accuracy and therefore suffers from high jitter at low power. Consequently, the inaccuracy-induced uncertainty in the down-converted signal does not allow for the sharp filtering of the baseband signal, resulting in a high noise floor in the spectrum of the down-converted baseband signal. Thermal noise and flicker noise are the main limiting factors of the overall system SNR. The mixer in this topology can be designed in CMOS and allow for high data rates, which is desirable for applications where low network latency is required. The reported power consumption range for this architecture is on the order of tens of microwatts [101–104].

Figure 1.10(c) shows the LNA-first or tuned-RF topology. In this approach, the mixer, and therefore the LO, are eliminated from the RF chain, and the received RF signal is amplified and fed directly into an envelope detector. This approach can achieve high sensitivities (<-100 dBm) but suffers from high power consumption at higher frequencies due to the front-end RF amplifier [105, 106].

Figure 1.10(d) shows the architecture of state-of-the-art ULP WuRx's. This architecture utilizes a high-impedance passive ED at the RF front-end input. One of the key features of this architecture is the passive voltage boost provided by the matching network at the input port, which is designed to increase the SNR at the output of the ED. The most common matching network topologies rely on discrete air-core inductors, which have been able to achieve 25-30 dB in passive voltage gain [107–113]. During the past few years, several research groups have developed ULP WuRx's using this architecture. The wakeup receivers that are demonstrated in silicon (including this work) [107–109, 114, 115] have achieved sensitivities down to -80 dBm with <10 nW in power consumption, and they have also included interference-rejection calibration loops in their stringent power budgets.

Recent designs have focused on pushing the boundaries of WuRx power and sensitivity and have approached the technology limits in some architectures, creating a gap in the literature with respect to the effect of environmental factors, such as thermal drift, on the aforementioned topologies. These effects are especially discernible in sub-threshold circuits due to the quadratic and exponential dependence of the transistor current on thermal and threshold voltages, respectively, and therefore on temperature. For example, sub-threshold comparators that are designed to detect sub-mV voltages can move away from their calibrated settings with a few degrees of temperature change, without a continuous calibration loop. Baseband amplifiers that operate in the same regime can move away from their designed dc operating point due to thermal drift as well. Therefore, in order to achieve a reliable system, compensation loops must be added to the designs for autonomous self-calibration.

Prior to this work, no existing solution offered sub-100 nW power wakeup receivers, meaning that once several wakeup sensors, all with the same order of magnitude of power consumption, are integrated with the wakeup receiver in a system, several years of the battery's lifetime have been compromised. The existing solutions rely on discrete-element matching networks that limit the volumes of the system components to several centimeters cubed, which should be reduced to a millimeter cubed for wearable electronics and implantable devices. The operational frequencies of the existing solutions do not exceed a few gigahertz, making them incompatible with a variety of communication infrastructures, avionics, and future 5G links. Furthermore, there have been no reports on the temperature stability of such low-power receivers, a necessary step in applications exposed to variable temperatures.

1.4 Dissertation Contributions and Organization

Research Questions

This dissertation tackles the following research questions.

Research Question 1. What is the fundamental detection limit of the ED-first topology in terms of WuRx sensitivity at sub-GHz and multi-GHz frequencies?

Research Question 2. What is the co-design methodology for integrating MEMS resonators with the ED-first topology necessary for leveraging the benefits of MEMS technology in ULP WuRx's?

Research Question 3. How should the wakeup code be designed to optimize the WuRx's sensitivity to a given false positive rate?

Research Question 4. What are the functionality-critical variations in the ED-first topology with respect to temperature and interference and how can these effects be compensated for in a power-efficient manner?

Thesis Statement

This dissertation presents design techniques that demonstrate the feasibility of implementing temperature- and interference-robust sub-100 nW WuRx's at sub-GHz and multi-GHz RF frequencies using the envelope-detector-first architecture. The dissertation also demonstrates that MEMS resonators can provide substantial improvements over discrete element matching networks for sub-100 nW WuRx's in terms of reduced size, robustness to interference, higher quality-factor matching, and immunity to electromagnetic interference.

The proposed techniques are implemented on several proof-of-concept CMOS chips that promise significant lifetime extensions for power-constrained IoT systems, energy-efficient calibration methods for robustness to temperature and interference, high-sensitivity operation at sub-GHz and multi-GHz RF frequencies, and reductions in the system component sizes through co-designed MEMS and CMOS technologies.

Research Contributions

This research presents fundamental analyses and design techniques for reducing the size and power consumption of the ULP WuRx's and improving their robustness to temperature variations and interference in a wide range of the RF frequency spectrum. The highlights of the dissertation's contributions are as follows.

1) Design-oriented analysis, modeling, and establishment of the fundamental detection limits of Dickson envelope detectors.
2) Analysis and design of fault-tolerant wakeup codes.
3) Techniques for achieving sub-100 nW WuRx's from sub-GHz to multi-GHz frequencies.
4) Energy-efficient calibration techniques enabling robust functionality across temperature ranges and in the presence of interference.
5) Co-design techniques for envelope detectors with MEMS-based matching networks, enabling significant size reductions at sub-GHz frequencies and optimizing WuRx's SNR.
6) Co-design techniques for envelope detectors with matching networks based on discrete air-core inductors for optimizing the WuRx's SNR.

In comparison with prior state-of-the-art, this dissertation achieves the following high-level impacts.

1) Demonstration of robustness to temperature in 0-to-70°C commercial range for sub-100 nW ULP WuRx's for the first time in the literature.
2) Demonstration of MEMS-based matching networks that decrease the system's size by more than two orders of magnitude and reduce the input RF bandwidth by up to one order of magnitude, compared to discrete element matching networks.
3) Achieving more than an order of magnitude improvement in terms of figure of merit (FoM) compared to prior state-of-the-art in sub-μW WuRx's.
4) Demonstration of operation at 4× higher RF frequency compared to previous sub-μW multi-GHz WuRx's with similar FoMs.

For low-throughput, event-driven applications, the following FoMs are used [116]

$$FoM_1(dB) = -P_{Sensitivity} + 5\log R_b - 10\log\frac{P_{dc}}{1\ mW} \tag{1.4}$$

$$FoM_2(dB) = -P_{Sensitivity} + 10\log R_b - 10\log\frac{P_{dc}}{1\ mW}, \tag{1.5}$$

where $P_{Sensitivity}$ is the WuRx sensitivity, R_b is the baseband bit rate, and P_{dc} is the WuRx power consumption. Equation (1.4) is used for ED-first architecture, and Equation (1.5) is used for LNA- and mixer-first architectures. Figure 1.11(a) shows a comparison of the WuRx's used in this re-

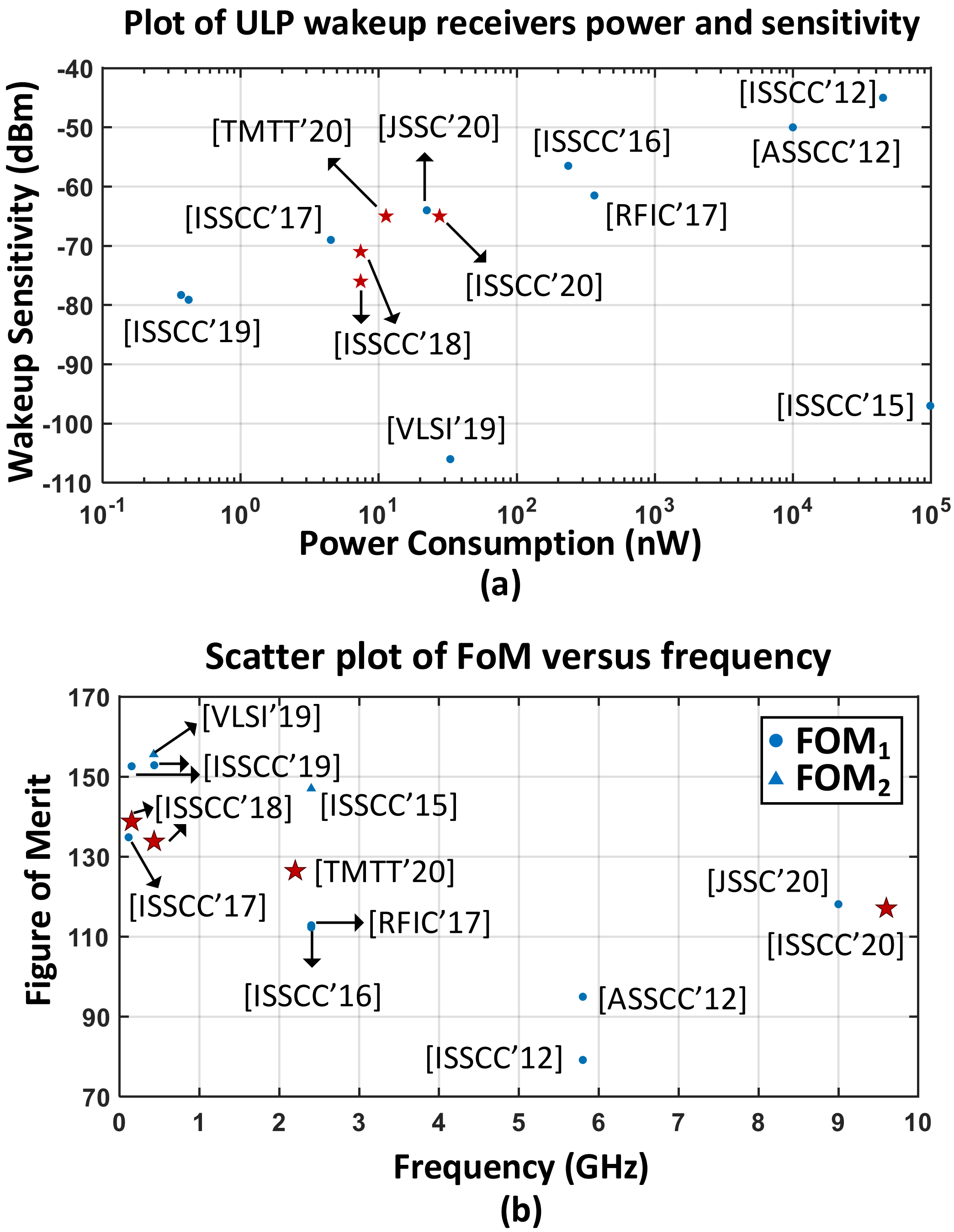


Figure 1.11: Comparison of the dissertation results with prior state-of-the-art in terms of (a) power and sensitivity, and (b) FoM versus frequency. The star markers indicate this dissertation's results.

search with prior implementations, indicating more than an order of magnitude improvement compared to pre-2016 results. Figure 1.11(b) compares the sub-GHz and multi-GHz demonstrations from this research with previous implementations, indicating more than an order of magnitude improvement in FoM among sub-μW WuRx's and a four-fold higher RF frequency compared to previous sub-μW multi-GHz WuRx's with similar FoMs.

Dissertation Organization

The remainder of this dissertation is organized as follows.
Chapter 2 presents a qualitative and quantitative design-oriented analysis and modeling of Dickson EDs. This chapter studies the fundamental detection limits of the Dickson EDs across temperature and their behavior at sub-GHz and multi-GHz frequencies. The chapter also examines the statistics associated with wakeup code detection to understand the design issues and trade-offs associated with fault-tolerant wakeup codes. Measurements of a proof-of-concept ED test structure chip are presented to illustrate the design space of the EDs in a 130 nm RF CMOS process.
Chapter 3 presents techniques for the design of temperature- and interference- robust ULP WuRx's as well as a proof-of-concept CMOS chip that operates at X band RF frequency and is robust to temperature variation in the 0-to-70°C commercial range. The chapter also presents a proof-of-concept CMOS chip at S band frequency.
Chapter 4 investigates the co-design of the MEMS-based matching networks with passive CMOS EDs and presents two proof-of-concept WuRx front-ends.
Chapter 5 studies the co-design of CMOS EDs with discrete matching networks that use air-core inductors and presents a proof-of-concept WuRx operating at MURS band.
Chapter 6 concludes the dissertation and includes a discussion of the future work needed to complement the ULP WuRx technology developed in this thesis.

1.5 List of Publications

[PB1] P. Bassirian, et al., "Design of an S-Band Nanowatt-Level Wakeup Receiver with Envelope Detector-First Architecture," *in IEEE Transactions on Microwave Theory and Techniques*, 2020.

[PB2] P. Bassirian, et al., "A Temperature-Robust 27.6nW -65dBm Wakeup Receiver at 9.6GHz X Band," *2020 IEEE International Solid–State Circuits Conference–(ISSCC)*, San Francisco, CA, 2020.

[PB3] J. Moody et al., "Interference Robust Detector-First Near-Zero Power Wake-Up Receiver," *in IEEE Journal of Solid-State Circuits*, 2019.

[PB4] P. Bassirian et al., "Nanowatt-Level Wakeup Receiver Front Ends Using MEMS Resonators for Impedance Transformation," *in IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 4, pp. 1615-1627, April 2019.

[PB5] S. M. Bowers et al., “Nanowatt Level Wake-up Receivers Using Co-designed CMOS-MEMS Technologies,” *in Proceedings of GOMACTech*, Mar. 2018, pp. 1–4.

[PB6] J. Moody et al., “A -76dBm 7.4nW Wakeup Radio with Automatic Offset Compensation,” *2018 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, 2018, pp. 452-454.

[PB7] P. Bassirian et al., “A Passive 461 MHz AlN-CMOS RF Front-end for Event-driven Wakeup Receivers,” *2017 IEEE SENSORS*, Glasgow, 2017, pp. 1-3.

[PB8] J. Moody et al., “An 8.3 nW -72 dBm Event Driven IoE Wake up Receiver RF Front End,” *2017 12th European Microwave Integrated Circuits Conference (EuMIC)*, Nuremberg, 2017, pp. 77-80.

[PB9] P. Bassirian, J. Moody and S. M. Bowers, “Event-driven Wakeup Receivers: Applications and Design Challenges,” *2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Boston, MA, 2017, pp. 1324-1327.

[PB10] P. Bassirian, J. Moody and S. M. Bowers, “Analysis of Quadratic Dickson Based Envelope Detectors for IoE Sensor Node Applications,” *2017 IEEE MTT-S International Microwave Symposium (IMS)*, Honololu, HI, 2017, pp. 215-218.

[PB11] P. Bassirian, et al., “A 27.6 nW Temperature- and Interference-Robust Wakeup Receiver at 9.6 GHz X Band,” *to be submitted to IEEE Journal of Solid-State Circuits*, 2020.

Chapter 2

Techniques for the Design of Dickson Envelope Detectors and Wakeup Codes

2.1 Analysis and Modeling of Dickson Envelope Detectors

The following two sections present a study of passive Dickson EDs operating in the quadratic small signal regime, used in the RF front end of the ULP WuRx's. Critical parameters, such as open-circuit voltage sensitivity (OCVS), charge time, input impedance, and output noise, are studied, and linear circuit models are proposed for predicting the behavior of the ED, thus providing design intuitions. There is a strong agreement between the model predictions, simulation results, and measurements of 15 representative test structures that were fabricated in a 130 nm RF CMOS process.

Conventional radio architectures, such as full heterodyne receivers, often require high-power amplifiers and stable LOs that require high dc power levels to operate in the microwave band. Alternatively, ED-first radio receiver architectures that use envelope detection as the first block in the receiver chain—after filtering and input matching—can significantly reduce the power consumption from μW to nW levels and achieve practical sensitivities [117]. A simplified block diagram for this receiver architecture is illustrated in Figure 2.1.

The most promising ED topology used in state-of-the-art ULP WuRx's is the passive Dickson ED, shown in Figure 2.1. The main advantage of a passive Dickson ED over active EDs is that the Dickson ED can support a high input impedance without suffering from flicker noise [117, 118]. The co-design of the Dickson ED varies considerably based on the application and type of matching network. For example, in wireless power transfer applications, large RF signals drive the devices into deeply nonlinear regimes, where the analyses require large signal considerations for the devices [119]. Alternatively, RF diode detectors at power levels below -30 dBm can be analyzed by approximating the device nonlinearity with a quadratic expression, which is the focus of this work.

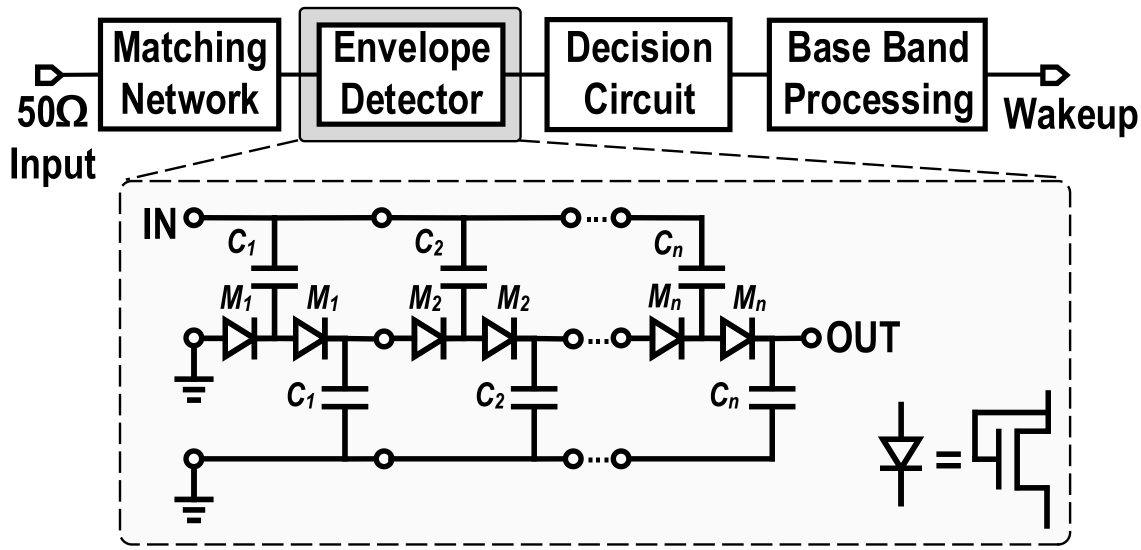


Figure 2.1: Block diagram of an ED-first wakeup receiver architecture using a Dickson envelope detector. This architecture can significantly reduce the receiver's power consumption from μW to nW levels and achieve practical sensitivities.

2.1.1 Key Metrics of the Envelope Detectors

Figure 2.2 shows the block diagram of the Dickson ED and its models at RF and baseband frequencies as well as the output noise model. For weak RF excitations, the functionality of the detector can be approximated with a quadratic expression [120]. The Dickson topology [121] consists of a diode detector with N stages of similar structures. In each stage, two diodes are configured in parallel with respect to the input RF signal and in series at the baseband frequency. The functionality of this detector can be explained by two separate models for the RF and baseband frequencies, as shown in Figure 2.2(b) and Figure 2.2(c), respectively. At sufficiently high RF frequencies, where the capacitance of each diode (C_{Di}) dominates its impedance behavior, the voltage swing across each diode is determined by the capacitive voltage division between the coupling capacitors (C_is) and the diode capacitances. Therefore, the coupling capacitors are designed to be large compared to the diode capacitances so that they function as short circuits at the RF frequency. As the architecture suggests, the input impedance of the detector at the RF frequency is equal to the parallel combination of diode impedances. Therefore, if all the stages are identical, the input impedance is equal to $((1/2N) \times R_D)||(2N \times C_D)$, where R_D and C_D are the equivalent shunt resistance and capacitance of the diodes, respectively. The C_{p1} and C_{p2} are due to the capacitance of the traces and coupling capacitors with the chip substrate. These on-chip parasitics, in addition to the off-chip package parasitics, can significantly affect the performance of the ED, particularly at multi-GHz frequencies.

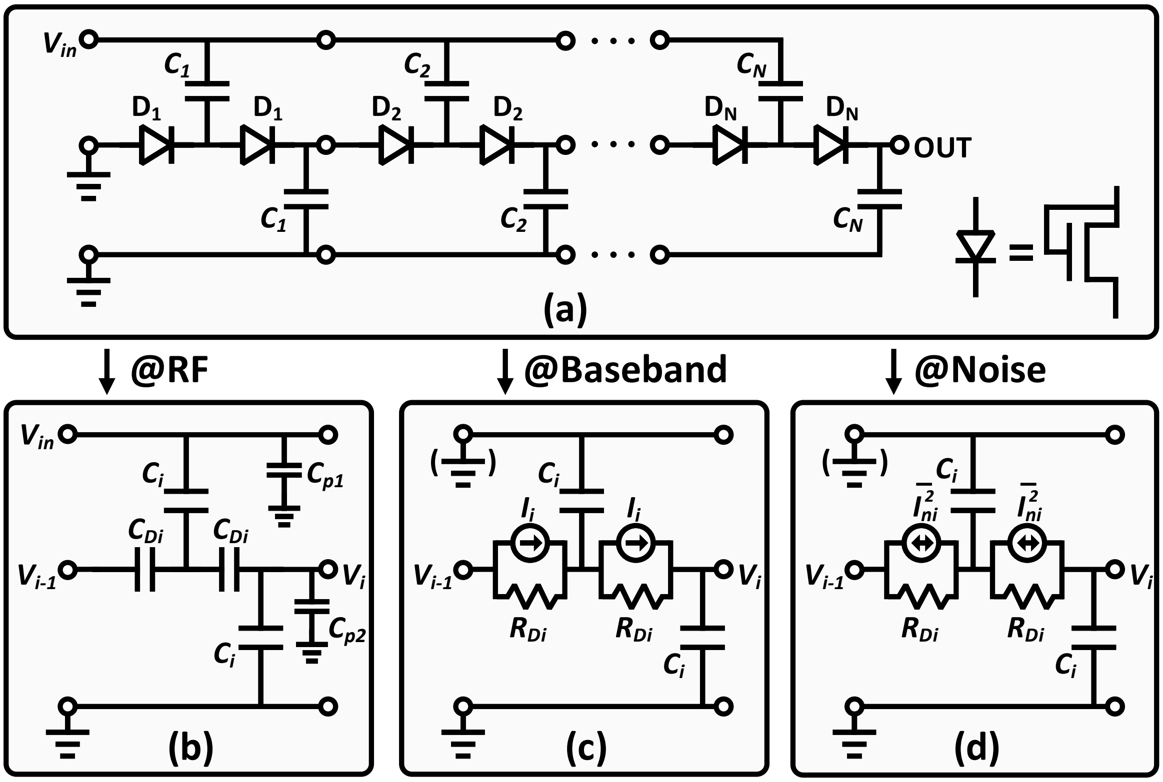


Figure 2.2: (a) Schematic of a Dickson ED and its equivalent circuit models for the (b) RF frequency, (c) baseband frequency, and (d) output noise.

At the baseband frequency, the second-order nonlinearity of the device creates a dc component that can be modeled as a step current source that turns on with RF excitation. The current sources charge up the coupling capacitors until the reverse leakage current across each diode is equal to the current flowing in the forward direction (Figure 2.2(c)). The sub-threshold current of a MOSFET can be expressed as [122]

$$I_D = \mu C_d V_T^2 \frac{W}{L}(\exp\frac{V_{GS}-V_{th}}{\zeta V_T})(1-\exp\frac{-V_{DS}}{V_T}), \tag{2.1}$$

where C_d is the capacitance of the gate depletion region, $V_T = \frac{kT}{q}$ is the thermal voltage, and $\zeta = 1 + \frac{C_d}{C_{ox}}$ is the sub-threshold slope. For a zero-biased diode-connected transistor ($V_{DS} = V_{GS}$) that is excited by the RF voltage $V_{in}\cos\omega t$, the device impedance R_D and output baseband voltage V_{BB} are equal to

$$R_D = \left(\frac{\partial I_D}{\partial V_{DS}}\Big|_{V_{DS}=0}\right)^{-1} = \frac{V_T \exp\frac{V_{th}}{\zeta V_T}}{(\mu C_d V_T^2)\frac{W}{L}}, \quad V_{BB} = 2N \times \frac{1}{2V_T}\left(\frac{1}{\zeta} - \frac{1}{2}\right)V_{in}^2 = 2N \times \mu_D {V_{in}}^2 \quad (2.2)$$

Therefore, the steady-state output baseband voltage of the ED can be written as $V_{BB} = 2N \times \mu_D {V_{in}}^2$, where μ_D and $2N \times \mu_D$ are the open-circuit voltage sensitivities (OCVS) of each diode and the entire ED, respectively. This baseband model can also be used to predict the transient behavior of the detector. An important metric for the transient behavior of the ED is its charge time (t_r), which limits the maximum WuRx data rate and is defined here as the amount of time that it takes the ED output to rise from 10% to 90% of its steady-state voltage. Empirical results show that the ED charge time is directly proportional to the diode resistance, coupling capacitors, and the square of the number of stages.

The equivalent baseband circuit can be slightly modified to model the output thermal noise of the detector, which is the dominant noise source at weak excitations [123]. By replacing the dc current sources with white-noise current sources, the output noise model can be achieved. Through co-design of the ED with the matching network that is presented in the next chapters, the minimum detectable signal (MDS) of the front-end can be optimized.

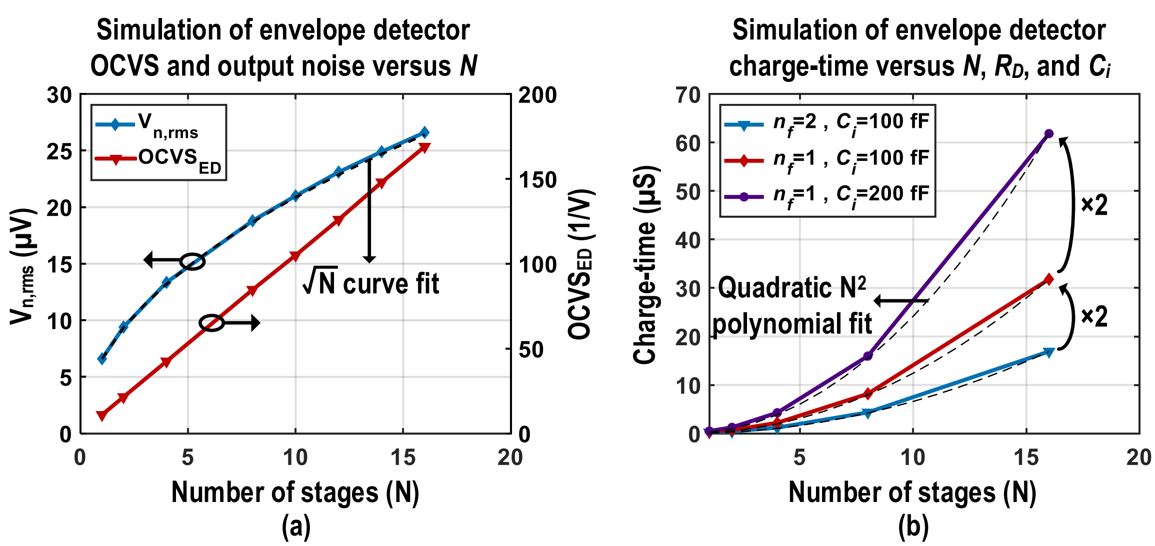


Figure 2.3: (a) Simulated output thermal noise and OCVS show that the output voltage noise of the ED is proportional to $\sqrt{N}$ and OCVS is linearly proportional to N. (b) Charge time simulations show that this quantity is proportional to N^2 and linearly proportional to the device resistance (changes with n_f, the number of fingers) and capacitance of coupling capacitors.

Figure 2.2 shows the simulation results for EDs that utilize minimum-sized zero-voltage threshold thick gate oxide (ZVTDG) devices to examine the OCVS, output noise, and charge time of Dickson

EDs. The OCVS simulation illustrated in Figure 2.2(a) uses a 100-MHz input RF signal and the output noise simulation is integrated over a 1 kHz bandwidth, which is a realistic value for bandwidth in the context of nanowatt-level WuRx's. This simulation indicates that the OCVS of the ED is linearly proportional to N and its output voltage noise is proportional to $\sqrt{N}$. Figure 2.2(b) examines the charge time for the ED versus the device resistance, coupling capacitors, and the number of stages. These simulations indicate that charge time is linearly proportional to the values of coupling capacitors and device resistance, which is varied by changing the number of fingers n_f . In addition, they show that the ED charge time is proportional to the square of the number of stages (N^2).

2.1.2 Charge Time Estimation and Optimization

An estimation of the ED charge time can be achieved by using the zero-value time constants method [124]. This method states that in a low-pass system with the transfer function

$$H(s) = \frac{a_0 + a_1 s + ... + a_p s^p}{1 + b_1 s + ... + b_q s^q}, \tag{2.3}$$

the high pole of the system can be estimated from

$$\omega_h \approx \frac{1}{b_1}, \tag{2.4}$$

where b_1 is the first-order coefficient of the denominator. Equation (2.4) underestimates the system bandwidth and therefore overestimates the charge time. Assume that the ith ED stage has two coupling capacitors, both equal to C_i. The first-order coefficient b_1 is equal to the sum of zero-value time constants of the RC ladder equivalent circuit

$$\begin{aligned} b_1 = \sum_{i=1}^{N} \tau_i^0 = \sum_{i=1}^{N} C_i R_{Di}^0 & \quad (2.5) \\ = [C_1(R_D) + C_1(2R_D)] + ... + [C_n(2N-1)R_D + C_n(2NR_D)] & \quad (2.6) \\ = (4N-1)R_D C_N + (4N-5)R_D C_{N-1} + ... + 3R_D C_1, & \quad (2.7) \end{aligned}$$

which, under the assumption of identical ED stages, can be simplified to

$$b_1 = (2N^2 + N)R_D C_i = \binom{2N+1}{2} R_D C_i \tag{2.8}$$

$$\Rightarrow t_r \approx 2.2\binom{2N+1}{2} R_D C_i. \tag{2.9}$$

Equation (2.5) provides several design intuitions regarding the contribution of the coupling capacitors to the charge time of the ED. First, it indicates that the time constant associated with the ith stage coupling capacitor is proportional to the stage number. Therefore, the capacitors of the last stages slow down the detector more than the capacitors of the first stages of the ED. Second, the detector charge time is proportional to the square of the number of stages, meaning that in applications that require fast charge times, there is going to be a trade-off between the charge time and OCVS of the ED.

Equation (2.5) can also be used to find the maximum drivable capacitive load of the ED. The ED usually drives the capacitive load of the subsequent receiver stage, such as a comparator or baseband amplifier. The maximum drivable capacitive load C_{L-max} is defined as the capacitance that increases the charge time by 10%. After adding C_L, the ED charge time increases to

$$t_r \approx 2.2R_D((2N^2 + N)C_i + 2NC_L). \tag{2.10}$$

For less than a 10% increase in the charge time, the C_L needs to satisfy the following condition

$$C_{L-max} = \frac{NC_i}{10}. \tag{2.11}$$

Equation (2.5) also indicates that for a given OCVS, the charge time of the ED can be optimized by choosing stepped coupling capacitor values. Optimizing the charge time can be useful in applications with critical latency requirements. Since the last-stage capacitors contribute the most to the charge time, the coupling capacitors for those stages can be made smaller. The marginal loss in sensitivity can be compensated for by choosing a larger capacitor for the first stages. To find the proper capacitor profile, the parameter $b_1(C_1, ..., C_N)$ needs to be optimized conditional on a constant OCVS constraint. To formalize the constant OCVS, the parameter average capacitive voltage division ratio parameter $0 < \alpha_v < 1$, of the ED is defined as

$$\alpha_v = \frac{1}{N}\sum_{i=1}^{N} \frac{C_i}{C_i + 2C_D}, \tag{2.12}$$

where C_D is the parasitic capacitance of the diodes at the RF frequency, and α_v is the sum of the voltage division ratios that determine the RF voltage swing across each diode in the ED. The Lagrange multiplier method can be used to minimize the function $f(.)$ subject to the constraint $g(.) = 0$, where f and g are defined as

$$f(C_1, ..., C_N) = (4N-1)C_N + (4N-5)C_{N-1} + ... + 3C_1 \tag{2.13}$$

$$g(C_1, ..., C_N) = \sum_{i=1}^{N} \frac{C_i}{C_i + 2C_D} - N\alpha_0. \tag{2.14}$$

The Lagrangian function can be written as

$$\mathcal{L}(C_1, ..., C_N, \lambda) = f - \lambda g. \tag{2.15}$$

The vector $\langle C_1, ..., C_N \rangle$ that minimizes the function f can be found by solving the equation $\nabla\mathcal{L} = 0$.

$$\Rightarrow \nabla\mathcal{L} = \langle 4N - 1 - \frac{2\lambda C_D}{(C_N + 2C_D)^2}, 4N - 5 - \frac{2\lambda C_D}{(C_{N-1} + 2C_D)^2}, ..., 3 - \frac{2\lambda C_D}{(C_1 + 2C_D)^2}, \tag{2.16}$$

$$N\alpha_0 - \sum_{i=1}^{N} \frac{C_i}{C_i + 2C_D} \rangle = 0. \tag{2.17}$$

The first N equations result in $(1 \leq i \leq N)$

$$C_i = \sqrt{\frac{2\lambda C_D}{4i-1}} - 2C_D. \tag{2.18}$$

To calculate λ, the expression for C_i in Equation (2.18) can be substituted into Equation (2.17), which results in

$$\lambda = (\frac{\sqrt{2C_D}(\sum_{i=1}^{N} \sqrt{4i-1})}{N(1-\alpha_0)})^2. \tag{2.19}$$

A comparison between the simulated charge time in the model prediction and the estimation resulting from Equation (2.9) is presented in Figure 2.4(a). The simulation uses an ED made of ZVTDG devices with $W/L = 3\ \mu m/560\ nm$ and 100 fF coupling capacitors. The plot indicates that the model follows the simulation closely, with less than a 1% discrepancy. The estimation also follows the general trend of the simulation, with about a 20% to 30% discrepancy. The estimation always overestimates the charge time value, and its overestimation increases for a higher number of stages due to more terms in the transfer function being ignored. The simulation in Figure 2.4(b) presents a comparison between the charge times of stepped and non-stepped 20-stage EDs that use similar ZVTDG devices. In these simulations, the parameter α_v changes from 0.4 to 0.9 and for each set of solutions, the charge times are compared with an ED with equal coupling capacitors that achieves the same OCVS. Overall, the stepped profile for the coupling capacitors provides on the order of a 20% improvement in the charge time.

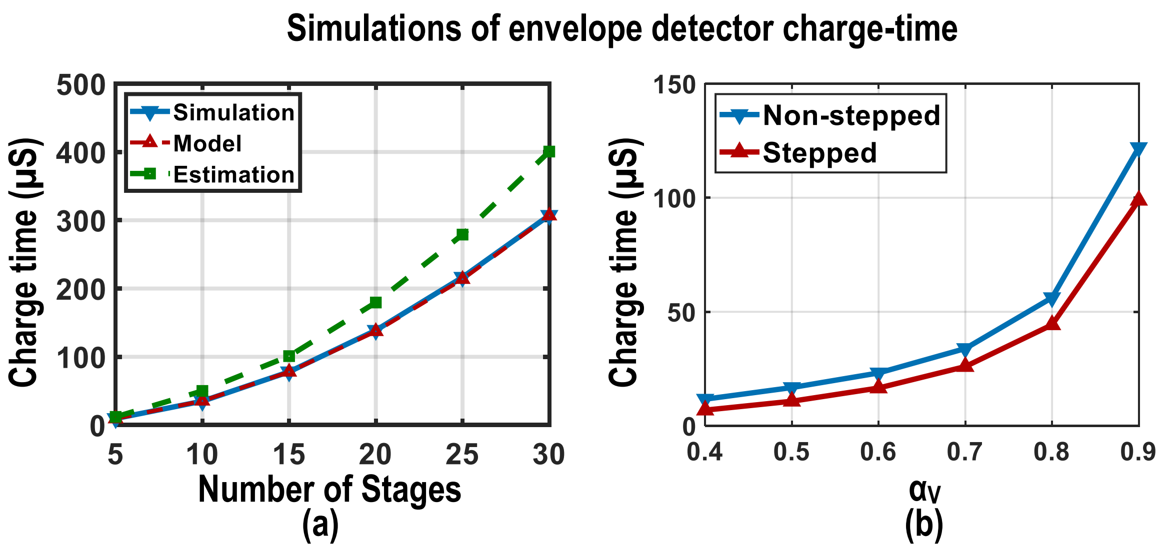


Figure 2.4: (a) Simulated charge times of an ED versus the number of stages using ZVTDG devices with $W/L = 3\mu m/560nm$ and 100 fF coupling capacitors. (b) A comparison between the charge times of stepped and non-stepped EDs shows that faster ED charge times can be achieved by using smaller capacitors in the last stages, which have larger time constants.

2.1.3 Measurements of the ED Test Structure Chip

This section presents the measurement results for a test structure chip implemented in a 130 nm RF CMOS process to identify the design space for the EDs in a modern CMOS technology process. The chip includes ED test structure for four minimum-sized devices with different threshold voltages from the design kit: 1) low threshold voltage RF (LVTRF) diode connected transistors and low threshold voltage PFET (LVTPFET) diode connected transistors, 2) near-zero threshold voltage (ZVT) diode connected transistors with normal oxide thickness, and 3) near-zero threshold voltage thick (dual) gate oxide (ZVTDG) diode connected transistors, where the thick oxide results in a higher nominal V_{th} than the regular ZVT devices. In the LVTRF devices, the channel length is swept from the nominal 130 nm to 300 nm to take advantage of the reverse short channel effect to reduce their threshold voltage. Two EDs with stepped and non-stepped capacitor profiles are implemented to study the effect of stepping the coupling capacitors on the charge time of the EDs. The number of stages is swept from 16 to 32 and 64 to study the effect of the number of stages on the charge time and OCVS.

Additionally, a PFET-based ED is implemented to study the effect of body biasing on the input impedance, charge time, and OCVS of the EDs. The benefit of body biasing is that it can compensate for the threshold-voltage-dependent characteristics of the EDs that change across process and temperature. The schematic of the measurement setup, a photo of the measurement setup, and a die photo are shown in Figure 2.5. To prevent the oscilloscope from loading the output of the devices, a FET-based Op-Amp is used to measure the transient responses of the circuits, although the loading effects of the PCB traces and the buffer are still present.

Figure 2.6 and Table 2.1 present the measurement results for the test structures. Devices with lower channel impedances, such as ZVTs, achieve faster charge times and lower input impedances, while devices with higher impedances, such as LVTRFs, have higher impedances and slower charge times. ZVTDG devices offer a good trade-off between impedance and charge time and can achieve several kilo-ohms of impedance with high sensitivities. The PFET-based test structure shows the increase in charge time resulting from the body voltage; this effect can be used for tuning the matching network to achieve the optimal SNR. The effect of the body voltage on OCVS is less than 20% on this specific test structure.

Several measurement artifacts cause further discrepancies between the simulations and measurements. First, due to the loading effects of the PCB and buffer on the ED and the loading effect of the oscilloscope on the buffer, in some cases, the measurements show a slower transient response. Also, the sensitivity of the charge time to the channel impedance and threshold voltage creates further uncertainty. Second, input impedances on the order of tens of kilo-ohms cannot be measured reliably with a network analyzer. Overall, the charge time measurements are within 50% of the simulations, while OCVS and the input impedance are within 15% and 30% of the simulations, respectively.

2.2 Pseudo-Differential ED Topology and Multi-GHz Operation

The Dickson topology can be modified as illustrated in Figure 2.7 to provide a differential baseband output [117]. The operation of the pseudo-differential ED is similar to that of the single-ended Dickson topology, which was explained thoroughly in the previous section. The main difference between the two architectures is that a second reverse parallel branch generates a negative baseband

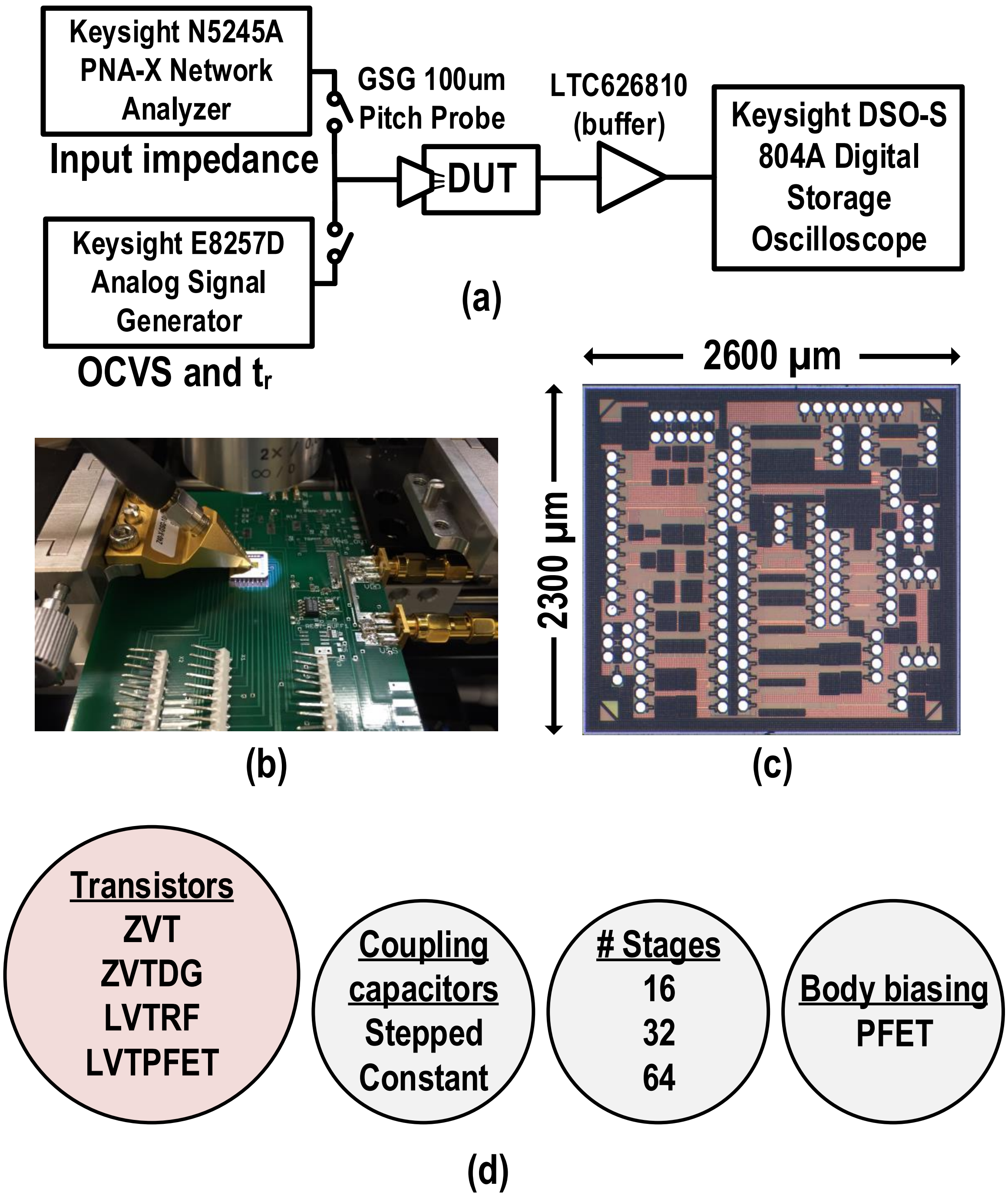


Figure 2.5: (a) Schematic of the measurement setup for the charge time, OCVS, and input impedance. (b) Measurement setup photo. (c) ED test structure chip die photo. (d) Types of devices, coupling capacitor type, number of stages, and body biasing on the chip.

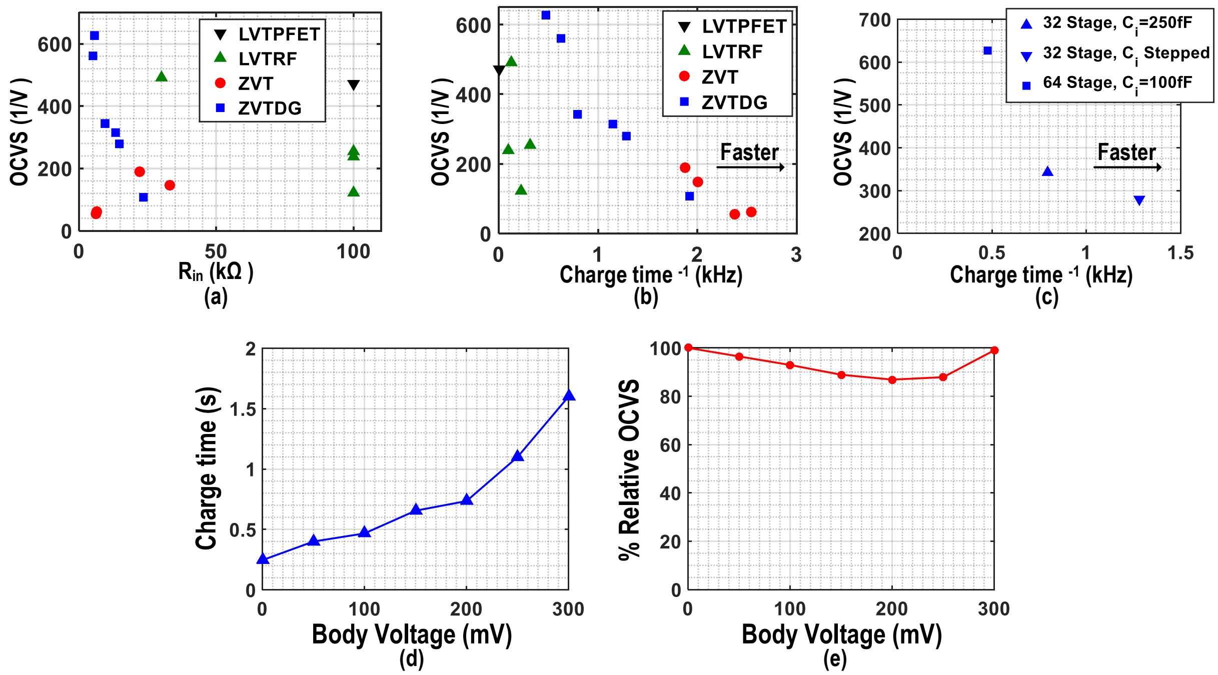


Figure 2.6: (a), (b) Measured input impedances of EDs versus their charge times and OCVSs. (c) Measurement results comparing the OCVSs and charge times for three different detectors with differing numbers of stages and stepped versus non-stepped coupling capacitors. (d), (e) Measurements of OCVS and charge time for an LVTPFET-based ED indicating that body-biasing technique can be used to trade-off charge time and input impedance with minimal change in OCVS.

Table 2.1: Comparison of measured and simulated results for six representative EDs.

DUT			OCVS (1/V)		Charge time (µs)		Input impedance (kΩ || pF)	
Devices Type	# Stages	Coupling capcitors (fF)	Measured	Simulated	Measured	Simulated	Measured	Simulated
ZVT	10	100	55	97	421	20	6.1 || 0.7	10.8 || 0.5
ZVT	16	250	189	180	533	260	22 || 1.54	38.2 || 1.13
ZVTDG	16	100	314	353	869	664	13.2 || 1.45	19.8 || 1.93
ZVTDG	16	Stepped	280	310	780	400	14.8 || 1.82	22.8 || 1.41
LVTRF	32	Stepped	254	237	3200	730	100 || 1.3	109 || 0.97
LVTRF	32	Stepped	491	462	8100	2100	30 || 2.1	54.6 || 1.76

output voltage in the pseudo-differential ED. The advantage of this topology is that its differential output allows for the differential design of the analog baseband in the WuRx front-end without having to use external RF baluns, thus providing robustness to common mode noise and, most importantly, comparator kickback noise, which will be discussed further in the next chapter. In addition, for a given power sensitivity (k_{ED}), defined as ED output voltage to the available input power (referenced to 50 Ω), the pseudo-differential ED achieves a faster charge time, because the forward and reverse branches have fewer stages in series [118].

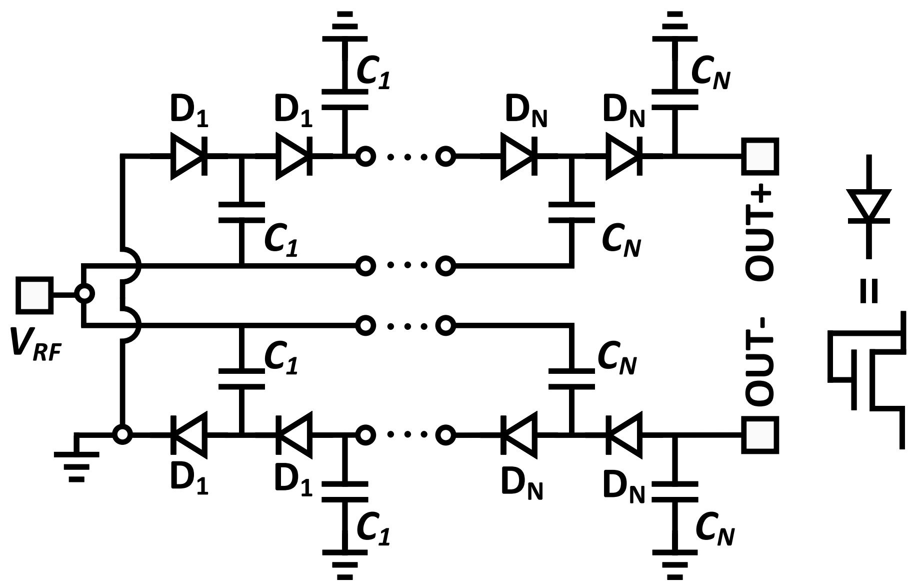


Figure 2.7: Pseudo-differential Dickson envelope detector topology enables a differential receiver architecture for RF and baseband circuits, adding robustness to kickback and common mode sources of noise.

An ED-first architecture does not use active RF gain in the front-end and relies on the impedance transformation from the 50 Ω RF input to the high impedance of the sub-threshold input diodes. At multi-GHz frequencies, the loss due to the parasitic RF layout capacitance that originates from the p-doped chip substrate can become comparable to the impedance presented by the diodes. This additional loss reduces the minimum detectable signal of the ED by several decibels. The key to maintaining a high ED input impedance at multi-GHz frequencies is proper layout design. Despite the small value of the parasitic capacitance of the on-chip RF trace (tens of femtofarads), its quality-factor (Q) can be relatively low in a high-impedance environment. The equivalent shunt resistance of the RF trace due to substrate loss can be on the same order as the ED input impedance, which means that it can load the input port significantly and reduce the maximum achievable passive voltage gain. Figure 2.8 shows the simulation results of the RF traces in the Golden Gate Momentum, which compares the parasitic input impedance with and without a substrate shield. This layout belongs to the S-band WuRx ED that is presented in the next chapter. These simulations

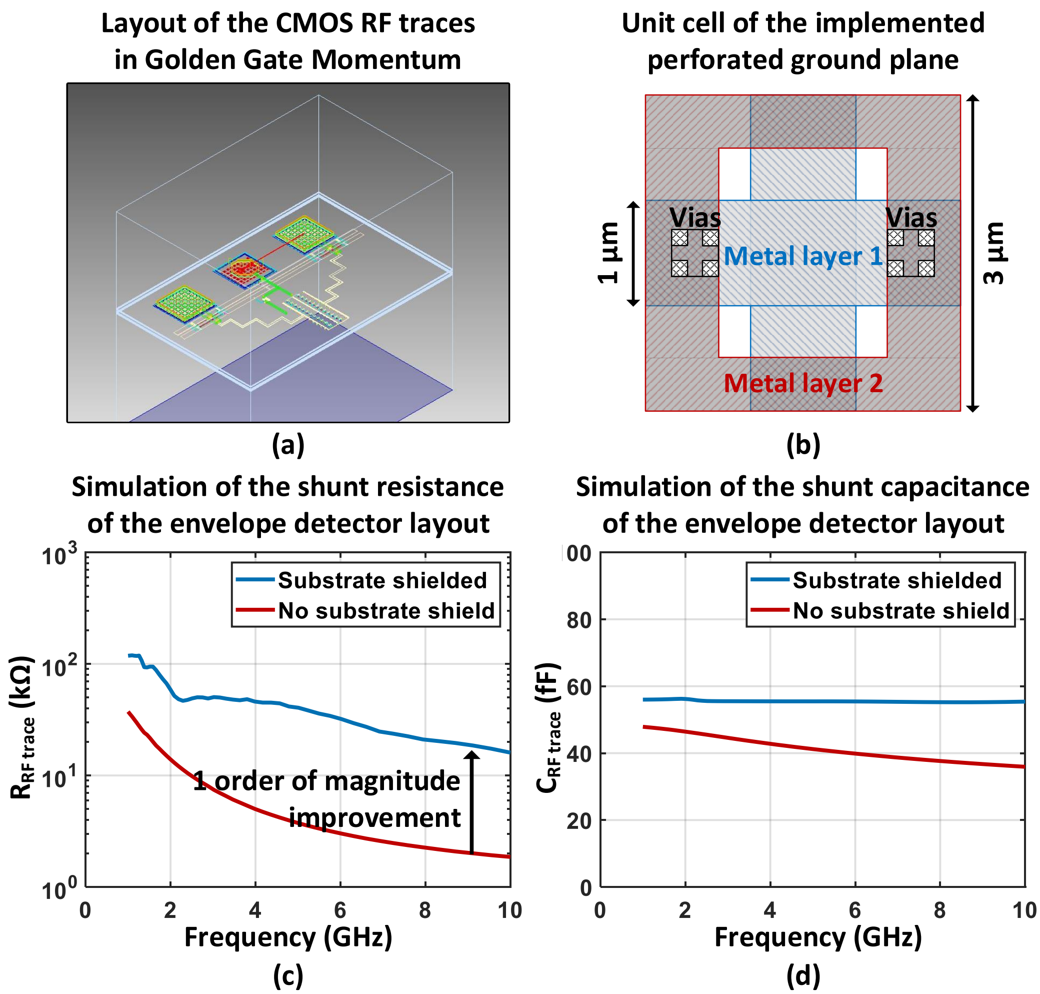


Figure 2.8: (a) Layout of the on-chip RF traces in the Golden Gate Momentum. (b) The unit cell of the perforated ground plane, comprised of the first and second metal layers. Momentum simulation comparing the on-chip RF trace (c) shunt resistance and (d) shunt capacitance, with and without a substrate shield.

include just the RF traces and do not include any of the ED diodes. The simulation utilizes a solid ground plane at the metal 1 layer and simplifies the via stacks. The simulation results in Figure 2.8(c), (d) indicate that the substrate shield can increase the shunt resistance of the traces by one order of magnitude at multi-GHz frequencies, at the cost of a slightly higher shunt capacitance. The actual on-chip ground plane is perforated due to the maximum metal density design rules and consists of the first and second metal layers, as shown in Figure 2.8(b).

In addition, the pad size on the high impedance node is reduced to 45 μm. Compared to a standard 75 μm pad, this reduction in size decreases the pad capacitance from about 200 fF to 40 fF.

Including the ESD protection diodes, the total simulated pad capacitance is 56 fF. A tight layout that reduces the per stage capacitance permits the use of a higher matching inductance at a given frequency and leads to a higher residual shunt resistance and smaller loading effect from the matching network. Also, the surrounding areas near the ED do not include any dummy metal fillings. A dummy metal filling introduces additional loss and can reduce the effective distance of the top metal line from the substrate, which translates into a higher capacitance with lower Q.

A test structure chip presented in Figure 2.9(a) is used to measure the impact of the layout design on the input impedance of the ED. The three EDs have different layouts at the high-impedance RF input and are otherwise identical. The first ED uses a perforated substrate shield that consists of the first and second metal layers and does not have any dummy metal filling around the RF input. This ED is used in the X-band WuRx that is presented in the next chapter. The second ED uses a substrate shield with dummy metal filling. The third ED does not use a substrate shield but uses dummy metal filling. Figure 2.9(b), (c) present the measured shunt input resistances and capacitances of the test structures, respectively. The measurements indicate that the substrate shield and removal of the dummy metal fillings increase the shunt input resistance by a factor of $\times 2.2$, which results in a 3.4 dB improvement in the MDS of the ED via maintaining the high-impedance interface.

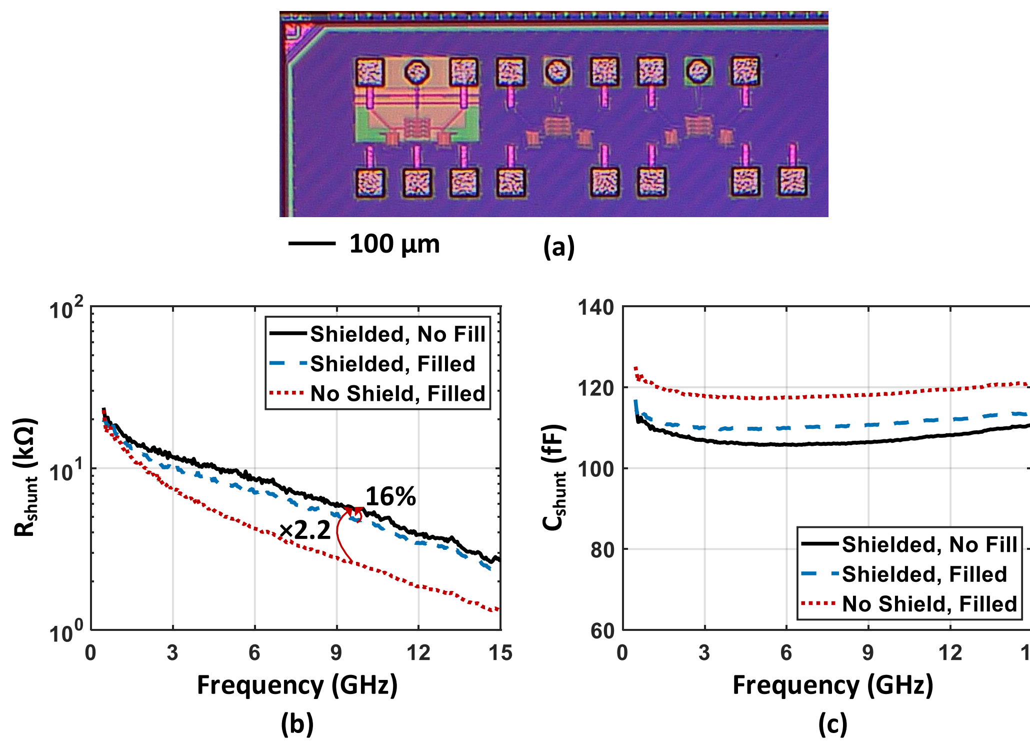


Figure 2.9: (a) Die photo of the test structure chip used for measuring the effect of the EM field confinement on the ED input impedance. (b) Measured shunt resistances and (c) shunt capacitances of the ED test structures.

2.3 Detection Statistics and Wakeup Code Design

The stringent sub-100 nW power budget for the ULP WuRx's prohibits the use of clock and data recovery (CDR) circuits. Therefore, these receivers use oversampling with incoherent detection to ensure high-SNR detection at the proper sampling time. The oversampling occurs at the decision circuit (Figure 2.1) by a factor of $2\times$ or $4\times$. To provide robustness to interference and the ability to discriminate between different nodes, the sampled outputs of the comparator are processed by a digital baseband circuit. The digital baseband uses a serial-to-parallel converter to distribute the comparator output bit stream to a four-phase correlator. Each phase of the correlator consists of a shift register that compares the wakeup code with the incoming bit stream. If the number of errors in a phase is fewer than a programmable threshold, the correlator issues a wakeup flag.

ULP event-driven WuRx's are meant to be used as the initial step in establishing communication with sensor nodes. Further authentication using more sophisticated and encrypted codes might be required before establishing a communication link and waking up higher-power modules in the node. Therefore, depending on the application, a certain FP rate must be achieved. The FP rate determines the expected rate of the wakeup events that occur due to the existence of noise in the system. The wakeup receiver sensitivity is then defined as the minimum signal power that can result in a wakeup with a probability greater than the TP ratio (e.g., 95%) for the given FP rate (e.g., 1/hour). The TP ratio determines the statistical proportion of actual wakeup events that are detected successfully by the WuRx. This observation indicates that wakeup detection is a form of asymmetric binary detection, as shown graphically in Fig. 2.10(a). Therefore, unlike a data receiver, the probabilities of a bit flip from zero to one and from one to zero are not necessarily identical.

Figure 2.10(b) shows the spectrums of a single-bit noisy zero and a noisy one. Since the main source of noise before the comparator is the filtered Gaussian thermal noise of the analog front-end, the probabilities of bit flips can be written as the tail probabilities

$$p_1 = P(1 \mid 0) = Q(\frac{\lambda}{v_n}) \tag{2.20}$$

$$p_2 = P(0 \mid 1) = 1 - Q(\frac{\lambda - V_{sig}}{v_n}), \tag{2.21}$$

where $Q(x) = (1/\sqrt{2\pi}) \int_x^\infty \exp(\frac{-u^2}{2})\, du$ is the Q-function, λ is the comparator decision threshold, V_{sig} is the baseband signal peak amplitude, and v_n is the RMS amplitude of the noise signal.

Using a fault-tolerant correlator allows a soft decision to be made based on the confidence level for the correctness of a received code. Designing the wakeup code with an optimized error tolerance can have a significant effect on minimizing the required SNR for satisfying a desired TP rate, while complying with a given FP rate. Assuming that the wakeup code is n bits long (code length), with b ones (code weight) and error tolerance of e, the probabilities of wakeup TP and FP are equal to

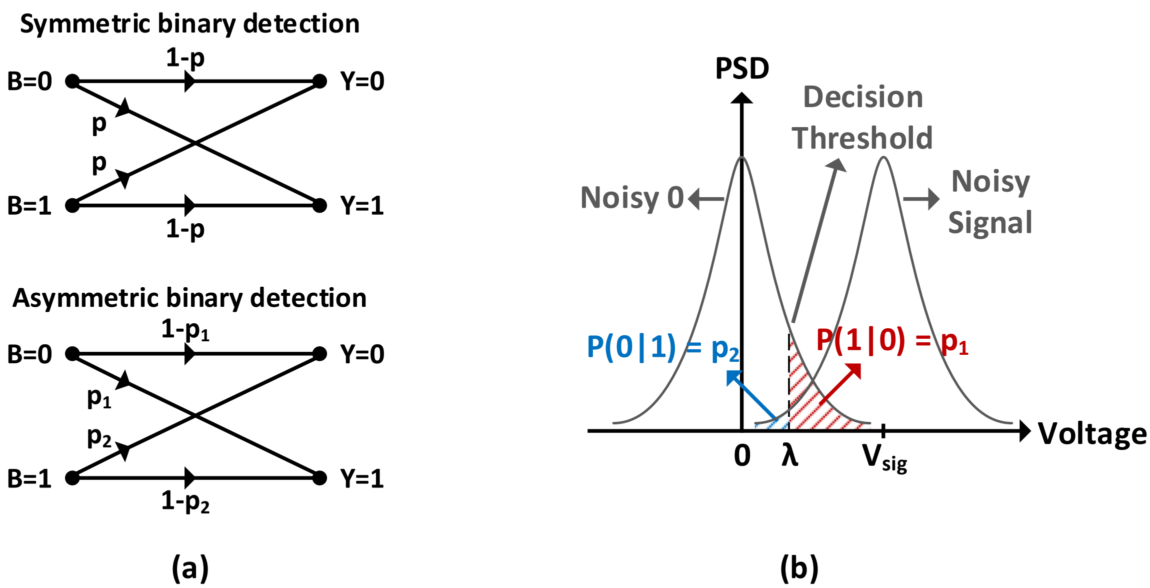


Figure 2.10: (a) Graphical representations of symmetric and asymmetric binary detection. (b) Power spectral densities of noise and a noisy signal, and the probabilities of a false positive and false negative in a single-bit binary detection.

$$P_{FP} = \sum_{i=0}^{e}\sum_{j=0}^{i}\binom{b}{b-j}p_1^{b-j}(1-p_1)^j \times \binom{n-b}{i-j}p_1^{i-j}(1-p_1)^{(n-b)-(i-j)} \tag{2.22}$$

$$P_{TP} = \sum_{i=0}^{e}\sum_{j=0}^{i}\binom{b}{j}p_2^{j}(1-p_2)^{b-j} \times \binom{n-b}{i-j}p_1^{i-j}(1-p_1)^{(n-b)-(i-j)}. \tag{2.23}$$

Figure 2.11 shows the simulation results for an 8-bit correlator with $b = 3$ and a 63-bit correlator with $b = 18$, assuming that the comparator decision threshold can be adjusted perfectly. Figure 2.11(a) indicates that if $e = 0$, with a longer code length, the minimum required SNR is higher, because, in that case, the longer code length needs to assure that more single bits are detected correctly. However, when e is set to 12, the longer correlator can theoretically improve the required SNR by about 6 dB. This is possible because the comparator can reduce its decision threshold and allow more FPs at its output without violating the FP limit. A further increase in e requires the comparator threshold to increase as well to keep the FP rate below the desired limit at the cost of RF sensitivity. Figure 2.11(b) plots the optimum error tolerance for different values of n and for two different code weights. Empirically, it appears that the fractional weight e/n eventually converges for large values of n. Note that it is not trivial to improve the sensitivity of a ULP WuRx via making the wakeup code length longer. Detecting longer codes requires a clock with higher accuracy and lower jitter, which is challenging to achieve with nanowattts of power.

Figure 2.11(c), (d) use the simulated minimum required SNR values from Figure 2.11(a) to plot the simulated Receiver Operating Characteristic (ROC) curves for different values of e. The ROC curves show the statistical relationship between TP and FP as the comparator decision threshold is swept from low to high. The points on the bottom left sides of the ROC curves correspond to higher decision thresholds. For lower decision thresholds, the points moving towards the right side of the plots represent higher FP rates. For the values below the optimal e, there is a wide range of λ values that can satisfy the FP rate. However, the ROC curves cannot go above the 95% TP line before violating the 1 FP/hour limit due to the tight error tolerance requirement. The FPs may eventually become detrimental for the detection of TPs, and the ROC curves might eventually roll back down as λ decreases. Alternatively, for the values above the optimal e, satisfying the FP rate becomes more difficult because the error tolerance criterion is too relaxed. Therefore, selecting the optimal error tolerance and the proper decision threshold, which can be enabled by the comparator's granular fine offset control, can improve the wakeup sensitivity by several decibels.

In applications where simultaneous wakeup of the nodes is needed, the wakeup code that enables the highest sensitivity can be used. In applications where a larger set of wakeup codes are needed for discriminating between various nodes, a set of codes with smaller error tolerance and lower sensitivity need to be used. Note that an eight-fold slower 8-bit code can improve WuRx sensitivity and achieve the same latency as the 63-bit code. However, the main advantage of using a 63-bit code is its ability to discriminate between a greater number of nodes.

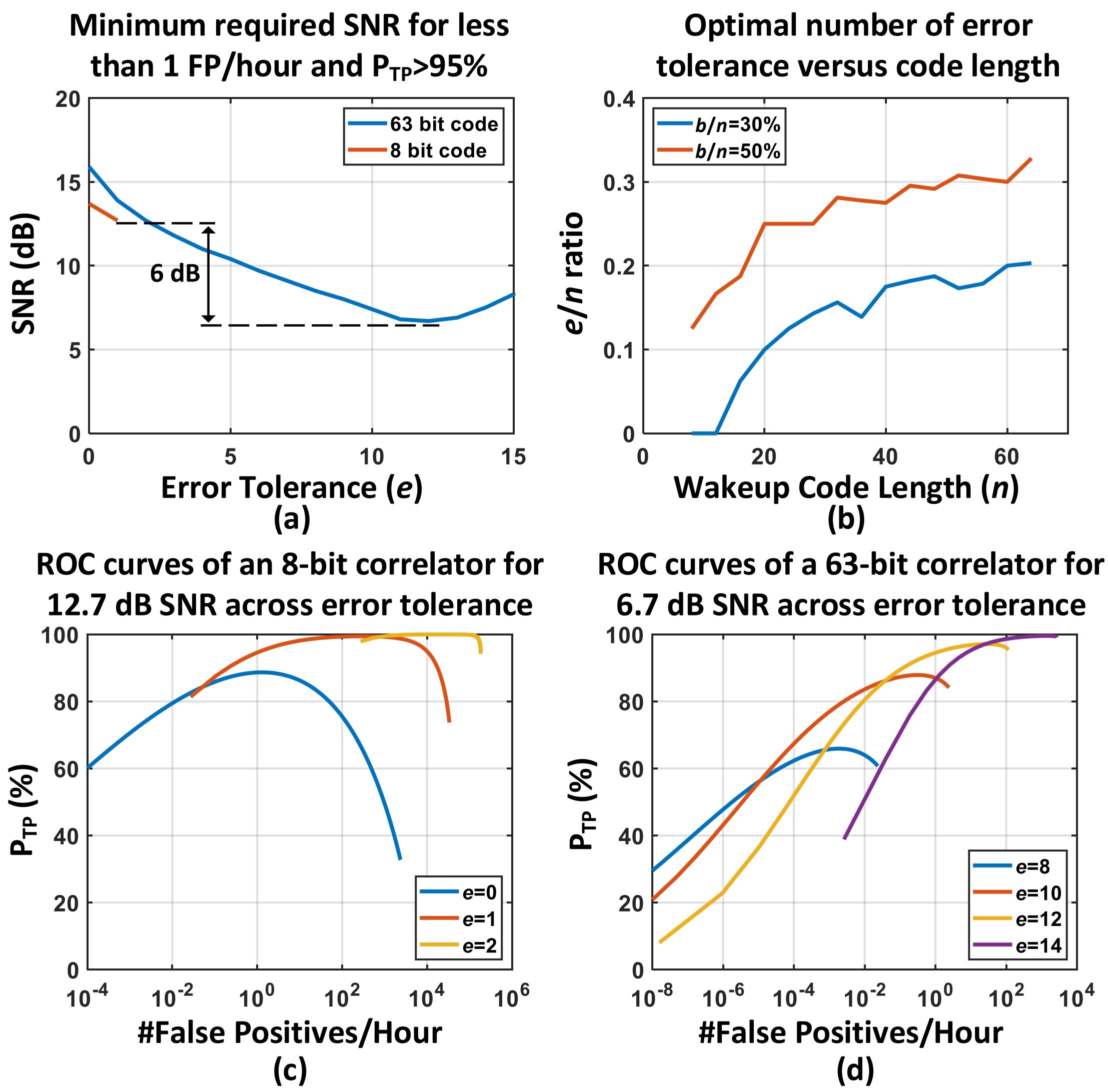


Figure 2.11: Simulation of (a) the minimum required SNR for achieving less than 1 FP per hour and a greater than 95% TP rate, (b) optimal error tolerance across code lengths for different code weights, (c) ROC curves of an 8-bit correlator with b=3 and 12.7 dB of SNR across different error tolerance values, (d) ROC curves of a 63-bit correlator with b=18 and 6.8 dB of SNR across different error tolerance values.

2.4 Fundamental Detection Limit of the ED-First Architecture

The goal of this section is to find the lowest power of the RF wakeup signal that can be reliably detected if the ED is used in an optimal receiver. This section also studies how that limit changes with respect to temperature. The ED metrics used in this section belong to the X-band chip ED that is presented in the next chapter. The schematic of the optimal detector is exhibited in Fig-

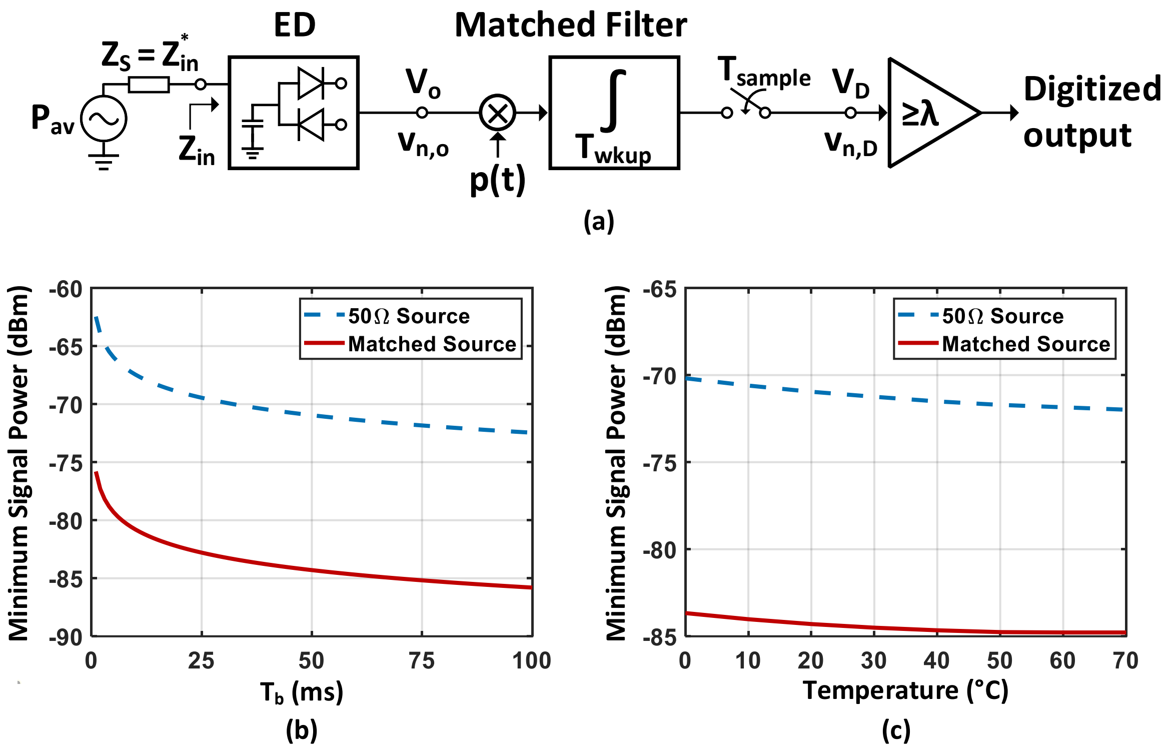


Figure 2.12: (a) Schematic of the optimal receiver conditioned upon using the ED. (b) Simulated minimum wakeup signal power versus bit length. (c) Simulated minimum wakeup signal power versus temperature for $T_b = 50$ ms.

ure 2.12(a), which has a matched source impedance at the ED input ($Z_s = {Z_{in}}^*$) with a noiseless matched filter at the ED output to process the baseband wakeup signal. The wakeup code used in the measurements of the X-band chip is $n = 63$ bits long (code length), with $w = 14$ ones (code weight), an error tolerance of $e = 9$, and a bit length of $T_b = 50$ ms. The measurements are taken while following the criteria that the WuRx achieves a wakeup FP rate of less than one per hour and has a wakeup missed detection ratio (MDR) of $< 10^{-3}$ [125, 126]. Since the ED charge time is much faster than the bit length ($t_r << T_b$), it is reasonable to assume that the baseband wakeup signal consists of a train of non-overlapping rectangular pulses. In this case, the matched filter can be implemented with a correlation detector that uses an integrate-and-dump block [127]. The pulse train $p(t)$ is the binary baseband wakeup signal that is multiplied by the ED output signal V_o. Assume that the digitizer threshold λ can be tuned perfectly to any level and that the digitizer knows the perfect sampling instant T_{sample}.

The detection signal-to-noise ratio of the optimal receiver $SNR_D = (\frac{V_D}{\sigma_{v_{n,D}^2}})^2\Big|_{t=T_{sample}}$ can be calculated from

$$V_D\Big|_{t=T_{sample}} = V_{D,max} = \bar{k}_{ED} P_{av} \times w \cdot T_b \tag{2.24}$$

$$\sigma^2_{v^2_{n,D}} = \frac{N_0}{2} \times w \cdot T_b, \tag{2.25}$$

where $\bar{k}_{ED}$ is the ED sensitivity with a matched source, P_{av} is the available power of the matched source, and N_0 is the double-sided noise spectral density at the output of the ED. Since the ED thermal noise, input impedance, and sensitivity vary with temperature, both $\bar{k}_{ED}$ and N_0 are functions of temperature. The probabilities of FPs and MDs determine the required SNR as in [125]

$$P_{FP} = Q(\frac{\lambda}{\sigma_{v^2_{n,D}}}) \tag{2.26}$$

$$P_{MD} = 1 - Q(\frac{\lambda - V_{D,max}}{\sigma_{v^2_{n,D}}}) \tag{2.27}$$

$$\Rightarrow \sqrt{SNR_D} = Q^{-1}(P_{FP}) - Q^{-1}(1 - P_{MD}). \tag{2.28}$$

Substituting Equations (2.24) and (2.25) into Equation (2.28) results in

$$P_{av} = \frac{Q^{-1}(P_{FP}) - Q^{-1}(1 - P_{MD})}{\bar{k}_{ED}} \times \sqrt{\frac{N_0}{2w \cdot T_b}}. \tag{2.29}$$

Equation (2.29) provides the lowest power required to satisfy the P_{FP} and P_{MD} conditions in the optimal receiver. Figure 2.12(b) plots P_{av} versus T_b, and Figure 2.12(c) plots P_{av} versus temperature. These simulations indicate that the measured sensitivity of -65 dBm in this work is about 20 dB higher than the fundamental detection limit. The fundamental limit improves by about 2 dB at higher end of the temperature range, mainly due to the reduction in the ED thermal noise.

Several nonideal effects in hardware implementation limit the ability of WuRx's to reach this fundamental limit of detection. The first challenge pertains to the proper packaging and design of the input matching network at high frequencies with high impedance interfaces. For example, the system presented in the next chapter of this dissertation uses the inductance of a single bond wire to transform the impedance at the input, which results in about 10 dB more loss compared to an ideal match. Proper packaging, such as flip chip bonding on a high-resistivity substrate, can significantly improve this loss in future work. The second challenge pertains to the implementation of a noiseless matched filter at the baseband. Most implementations of WuRx's oversample and digitize the output of a baseband amplifier, thus providing significantly lower SNR compared to a noiseless matched filter. The third challenge pertains to the resolution of the comparator decision threshold. This issue will be discussed and addressed in further detail in the next chapter.

2.5 Summary and Conclusions

The highlights of this chapter are as follows.

1) A qualitative and quantitative design-oriented analysis and modeling of Dickson EDs. An analytical estimation of charge time that is useful for sub-GHz designs when the transient simulation of the optimal detector with tens of stages is computationally heavy.

2) Measurements of a proof-of-concept ED test structure chip that illustrate the design space of the EDs in a 130 nm RF CMOS process.

3) Introduced the pseudo-differential ED topology that is an advantage to the single-ended architecture due to enabling a differential baseband design without using lossy RF baluns.

4) Studied the impact of the confinement of the electromagnetic field and careful layout design for the operation of the ED at multi-GHz frequencies.

5) A study of the detection statistics and trade-offs associated with the design of fault-tolerant wakeup codes.

6) The fundamental detection limits of the ED-first architecture.

2.6 List of Relevant Publications

[PB1] P. Bassirian, et al., “Design of an S-Band Nanowatt-Level Wakeup Receiver with Envelope Detector-First Architecture,” *in IEEE Transactions on Microwave Theory and Techniques*, 2020.

[PB2] P. Bassirian, et al., “A Temperature-Robust 27.6nW -65dBm Wakeup Receiver at 9.6GHz X Band,” *2020 IEEE International Solid–State Circuits Conference–(ISSCC)*, San Francisco, CA, 2020.

[PB4] P. Bassirian et al., “Nanowatt-Level Wakeup Receiver Front Ends Using MEMS Resonators for Impedance Transformation,” *in IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 4, pp. 1615-1627, April 2019.

[PB9] P. Bassirian, J. Moody and S. M. Bowers, “Event-driven Wakeup Receivers: Applications and Design Challenges,” *2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Boston, MA, 2017, pp. 1324-1327.

[PB10] P. Bassirian, J. Moody and S. M. Bowers, “Analysis of Quadratic Dickson Based Envelope Detectors for IoE Sensor Node Applications,” *2017 IEEE MTT-S International Microwave Symposium (IMS)*, Honolulu, HI, 2017, pp. 215-218.

[PB11] P. Bassirian, et al., “A 27.6 nW Temperature- and Interference-Robust Wakeup Receiver at 9.6 GHz X Band,” *to be submitted to IEEE Journal of Solid-State Circuits*, 2020.

Chapter 3

Techniques for Multi-GHz WuRx Design and Robustness to Temperature and Interference

3.1 Introduction

Thus far, it has been established that state-of-the-art ULP WuRx's can operate at sub-GHz frequencies and have mostly utilized the ED-first architecture to meet their stringent power budget requirements. This architecture faces several challenges when used at frequencies above a few gigahertz. First, due to the limited quality-factor of the on-chip passive elements, maintaining a high input impedance at the input port of the ED is challenging. A critical part of achieving high sensitivities in this architecture is the passive voltage boost delivered by the input matching network. Therefore, this issue can significantly limit the MDS of the WuRx. Second, the amplitude of the on-chip baseband signals of interest prior to the comparator can be on the order of a few millivolts due to the lack of active RF gain. Therefore, enabling noise-limited detection of such small signals requires comparator designs that are able to tune their decision threshold down to sub-mV levels. Comparator circuits that utilize binary-weighted offset control bits [111] can suffer from trip voltage non-monotonicity and range shifting due to process variation, which becomes a more prominent issue for granular offset control requirements.

Additionally, many parameters in a CMOS process, including the threshold voltage, sub-threshold slope, intrinsic carrier density, bandgap energy, and mobility, change with temperature [122]. Some of these dependencies are quadratic or exponential in the sub-threshold regime. In general, at a constant bias voltage, the drain current of a sub-threshold MOS transistor increases with increasing temperature. Equation (2.1) expresses the sub-threshold drain current of a MOS transistor. Assuming that $V_{DS} > 4V_T$, the drain current becomes independent of V_{DS} and is given by

$$I_D = \mu C_d V_T^2 \frac{W}{L}(\exp\frac{V_{GS}-V_{th}}{\zeta V_T}). \tag{3.1}$$

The threshold voltage of a MOSFET V_{th} exhibits a negative temperature coefficient of about -1 mV/K and can be expressed as $V_{th} = V_{th0} - \kappa T$, where V_{th0} is the threshold voltage at 0 K. Mobility also follows a trend, which is empirically expressed as $\mu = \mu_0(300/T)^{3/2}$, where μ_0 is the carrier mobility at room temperature $T_0 = 300\ K$ [128]. Note that the drain current is also proportional to the square of the thermal voltage, which is a linear function of temperature. In the sub-threshold regime, the variations in threshold and thermal voltages dominate the temperature-dependent behavior of the drain current, whereas, in strong inversion, the degradation in mobility dominates the temperature-dependent behavior of the drain current. The approach this dissertation has chosen to take is to compensate for the variations that are critical for functionality, as opposed to compensating for all of the temperature dependencies that exist in different blocks. The effects that are studied and compensated for are the variations in the comparator trip voltage and system clock frequency across temperature.

This chapter introduces the following design techniques to overcome the challenges discussed above, thus ensuring reliability in uncontrolled IoT environments while leveraging the communication infrastructure at multi-GHz frequency bands: 1) Confining the electromagnetic field at the RF input to the top dielectric layers by adding a perforated ground plane that shields the p-doped chip substrate, thus reducing the substrate loss. 2) Using an autonomous nW-power proportional-integral-derivative (PID) controller for adjusting the decision threshold of the comparator across temperature. The PID controller can also compensate for blockers by raising the comparator decision threshold above the interference level. 3) Using an area-efficient gate-leakage-based current DAC for implementing a tunable relaxation oscillator (RXO) calibrated with a gate-leakage-based digital temperature sensor. 4) Using a sub-nW comparator based on the StrongArm Latch topology with a thermometer-coded DAC enabling granular sub-mV control of the comparator decision threshold as well as monotonicity across its tuning bits, which is required for the proper functionality of the PID controller.

3.2 Sub-nW Comparator Design for mV-Level Signal Detection

The comparator design objective is to enable granular sub-mV trip voltage control for noise-limited detection of the mV-level output signal of the baseband amplifier. The comparator should also provide a monotonic trip voltage control for proper functionality of the PID controller, which is discussed in the next section. Non-monotonicity can cause the PID controller to move in the wrong direction due to the existence of the derivative term.

The schematic of the comparator and its component parameters is presented in Fig. 3.1. The comparator uses a capacitively-balanced StrongArm Latch topology [129] with a thermometer-

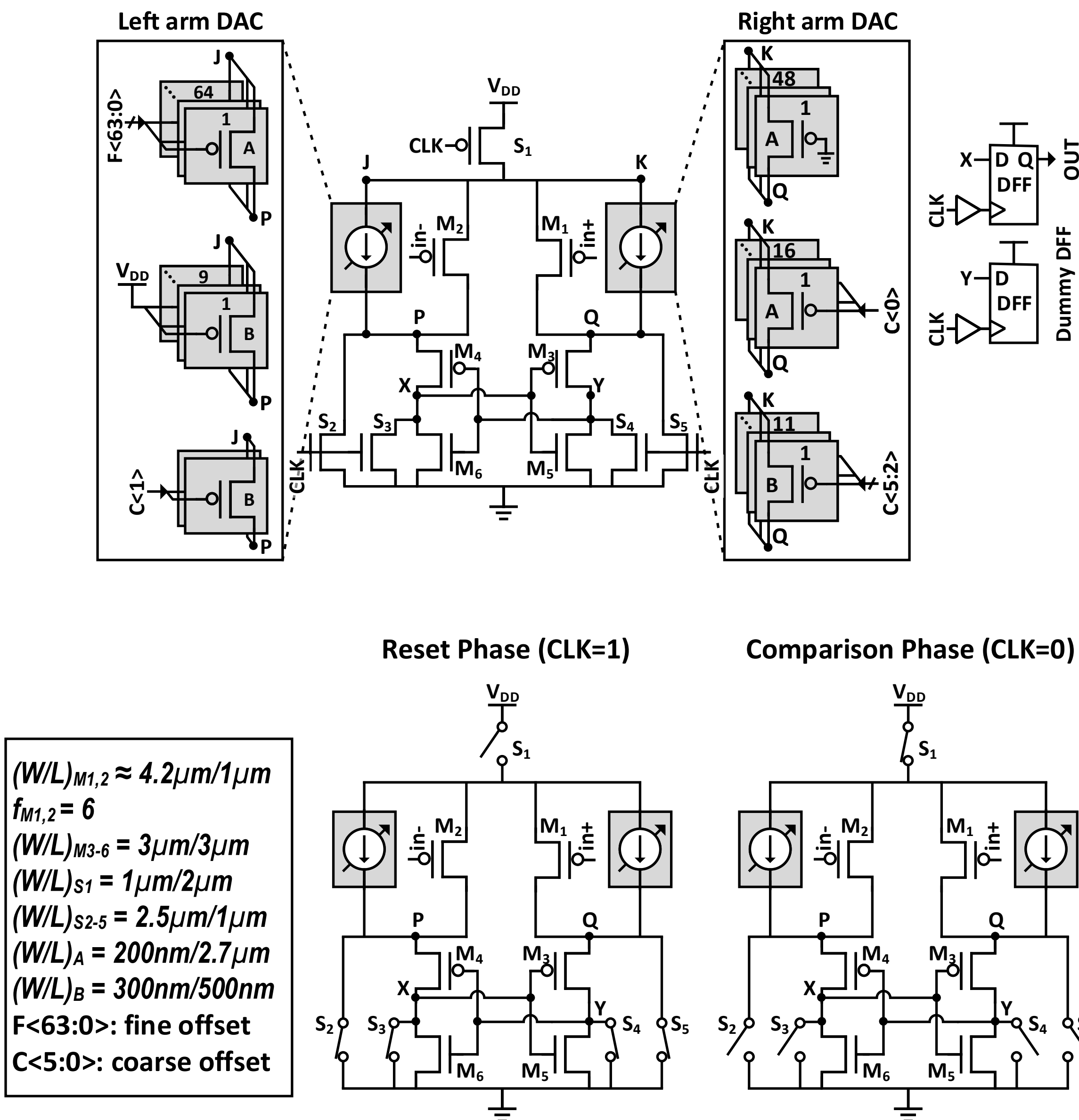


Figure 3.1: Schematic of the capacitively-balanced StrongArm Latch comparator with a thermometer-coded fine offset control current DAC. The comparator architecture can enable granular sub-mV trip voltage control for noise-limited detection of the mV- level output signal of the baseband amplifier.

coded offset control DAC to achieve the goals mentioned above. It consists of reset switches $S_1 - S_5$ that are controlled by the clock signal, pre-amplifier transistors $M_1 - M_2$ on the top connected to the output of the analog baseband, fine and coarse offset control current DAC transistors F[63:0] and C[4:0], and latch transistors $M_3 - M_6$ on the bottom. When CLK=1, the comparator is in its reset phase and all the bottom node voltages are shorted to the ground. In the comparison phase when CLK=0, M_1 and M_2 charge the internal capacitances on the P and Q nodes until the latch transistors turn on. Based on the relative strengths of the left and right arms, which depend on ΔV_{in} and the setting of the offset bits, the voltage on one of the P and Q nodes increases at a faster rate and determines the way the latch trips.

Binary weighted DACs are not an appropriate design choice for achieving sub-mV granularity in fine offset bits to control the trip voltage because they exhibit a significant post-fabrication variations [111, 130]. This effect becomes more prominent for smaller step sizes, as they require more accurate size matching. Alternatively, thermometer-coded DACs have better differential non-linearity (DNL) behavior and do not suffer from mid-code glitches when some devices turn on and some turn off. In addition, thermometer-coded DACs are inherently monotonic, which makes them a good design choice for auto-calibration algorithms [126]. In deployed environments where the temperature varies and interfering signals exist, control loops that adjust the trip voltage of the comparator by changing the offset bits can enable robust functionality for the WuRx [118].

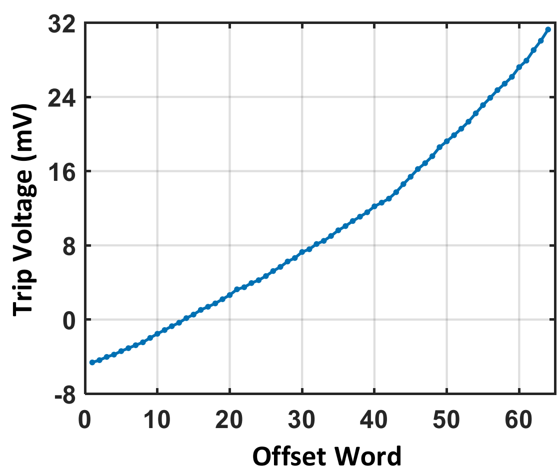


Figure 3.2: Measured comparator trip voltage across its offset words demonstrates a monotonic trend with an average sub-mV step size of 570 μV from -4.6 mV to 31.2 mV.

Another factor that can cause significant variation after fabrication is the mismatch between the capacitive loadings on the P and Q nodes. In order to keep the capacitive loading equal in both arms of the comparator, the fine and coarse offset transistors are identical on both sides but grouped differently. The fine offset transistors on the left arm are duplicated on the right, but 48 of them are connected to the ground, and the other 16 are C[0]. The other coarse offset bits consist of seven identical transistors that create C[1:4], with some of them grounded on the left arm. There is also a dummy D flip-flop at the latch output to keep the capacitances of the output nodes balanced as well.

The other effect that can shift the range of the comparator trip voltage after fabrication is kickback noise. At every edge of the clock, the parasitic capacitance of the M_1 and M_2 transistors can send a spike back into the baseband amplifier output. Since the output impedance at the amplifier stage is relatively high, the peak of this spike can go up to tens of millivolts, which is significant compared to the levels of the signals of interest. A differential topology for the front-end can mitigate this issue by creating an identical kickback on both arms of the comparator.

The comparator remains functional across different supply voltages from 0.5 V to 1 V. In general, increasing the supply voltage reduces the trip voltage step size and therefore the comparison range across the offset words. Simulation results indicate that reducing the supply voltage of the comparator from 1 V to 0.5 V reduces the amplitude of the kickback noise by about one order of magnitude, from 10 mV to 1 mV. This reduction in kickback noise is observed in the measurements as well. Figure 3.2 presents the measured trip voltage of the comparator across its offset words at $V_{DD} = 0.5\,V$, demonstrating a monotonic trend with an average sub-mV step size of 570 μV from -4.6 mV to 31.2 mV.

3.3 Nanowatt-Power PID Controller Design for Comparator Calibration

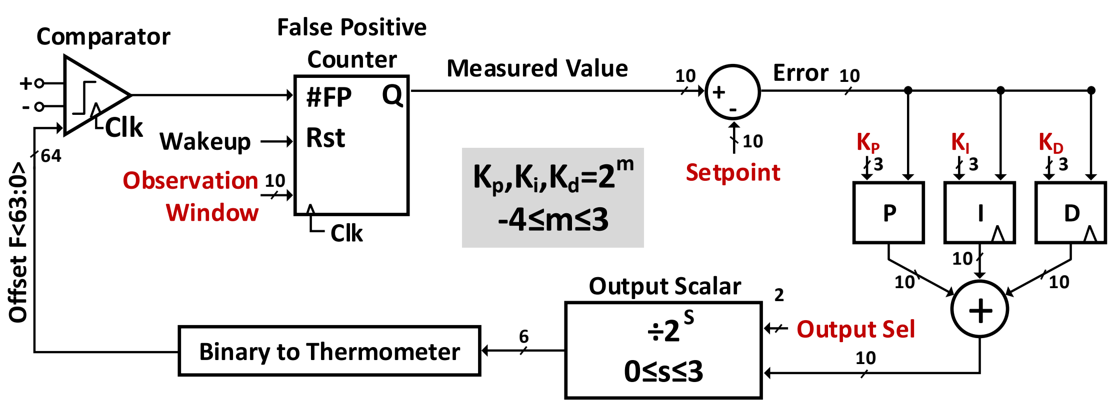


Figure 3.3: Block diagram of the PID controller used for calibrating the number of false positives at the output of the comparator across temperature and in the presence of interference.

Continuous calibration of the comparator is critical for keeping the WuRx in the most sensitive functional state. Because the comparator needs to be sensitive enough to detect mV-level signals, its decision threshold changes significantly with temperature (relative to the levels of the signals

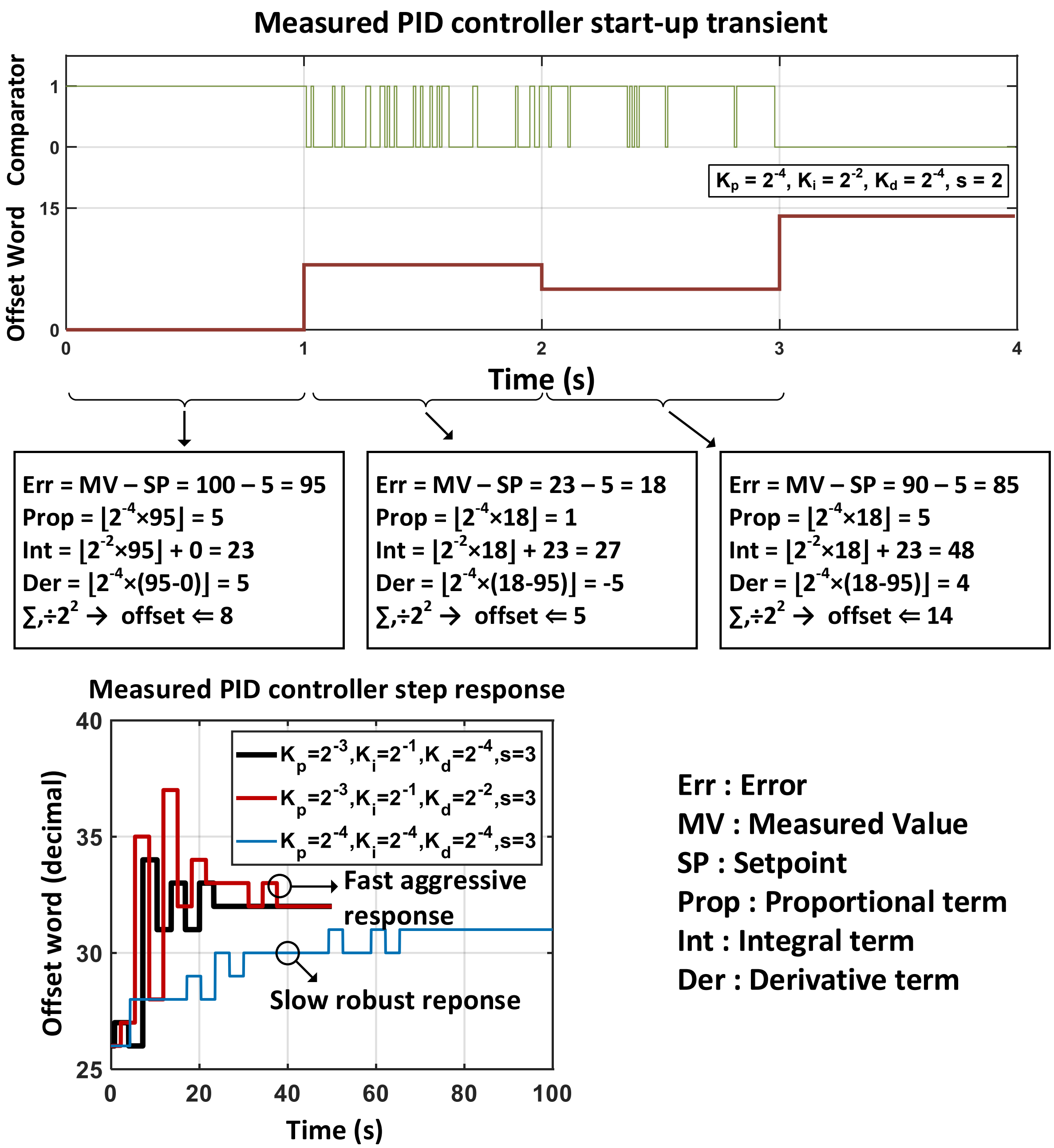


Figure 3.4: Measured start-up transient of the PID controller and the control loop step response to an OOK interferer for different settings of the PID parameters.

of interest). Temperature swings can change the relative strength of the comparator's tuning DACs as well as the output noise of the RF front-end. The PID controller aims to set the statistics of the comparator output false positive rate to a desired percentage by adjusting its decision threshold. This percentage ultimately determines the wakeup false positive rate of the WuRx [125]. In event-driven applications, there are no wakeup signals in the channel for the majority of the time. Therefore, the WuRx listens to background interference plus noise while waiting to detect a wakeup signal. The controller keeps the decision threshold above the background interference and noise levels, while providing enough delay for the wakeup signal to be detected without raising the decision threshold.

The schematic of the PID controller is presented in Figure 3.3. The controller measures the comparator output continuously for the window determined by the observation window. At the end of each measurement cycle, the counter updates the measured number of false positives. This number is subtracted from the programmable set point to determine the number of errors in the current measurement cycle. Using the number of errors in the current cycle, the number of errors in the previous cycle, and the integral from the previous cycle, the P, I, and D blocks update the controller output. All of the multiplications and divisions to be carried out, including those for k_p, k_i, and k_d, and the output scalar s, are simplified to multipliers of two, which can be implemented in a power-efficient manner using level shifters. Ultimately, the controller reaches a state where the comparator false positive rate is close to the ratio of the set point to the observation window. If a wakeup signal is detected in the current observation window, the controller does not consider the wakeup pulses to be false positives and instead uses the parameters of the previous measurement window for the next cycle.

A transient measurement of the PID controller startup is exhibited in Figure 3.4. In this measurement, the observation window is set to 100, which is 1 s long, and the set point is programmed to 5. Therefore, the controller aims to calibrate the comparator FP rate to 5% in this measurement. The values of different registers in the first three measurement cycles are shown on the bottom of the figure. Figure 3.4 also shows a measurement of the controller output step response when an OOK -58 dBm interferer in the 5.8 GHz ISM band is applied to the X-band WuRx using three different PID parameters. This measurement demonstrates that the controller can trade-off a slower response time for less aggressive transient behavior, which makes the control loop adaptable to various quiet and cluttered environments.

3.4 Crystal-Less nW-power Active Temperature Compensation of Clock and Temperature Sensor Design

Since the WuRx does not use a clock recovery mechanism, the accuracy and consistency of its timing is critical for proper functionality. To remain within one oversampled bit after 63 data bits, the WuRx clock needs to be less than 0.3 Hz off from the ideal 80 Hz clock frequency. Relaxation oscillators are good candidates for on-chip clocks at such low power levels. The required accuracy of the clock translates into designing a very fine-grain, tunable DAC for controlling the oscillator charge pump current as well as a temperature sensor.

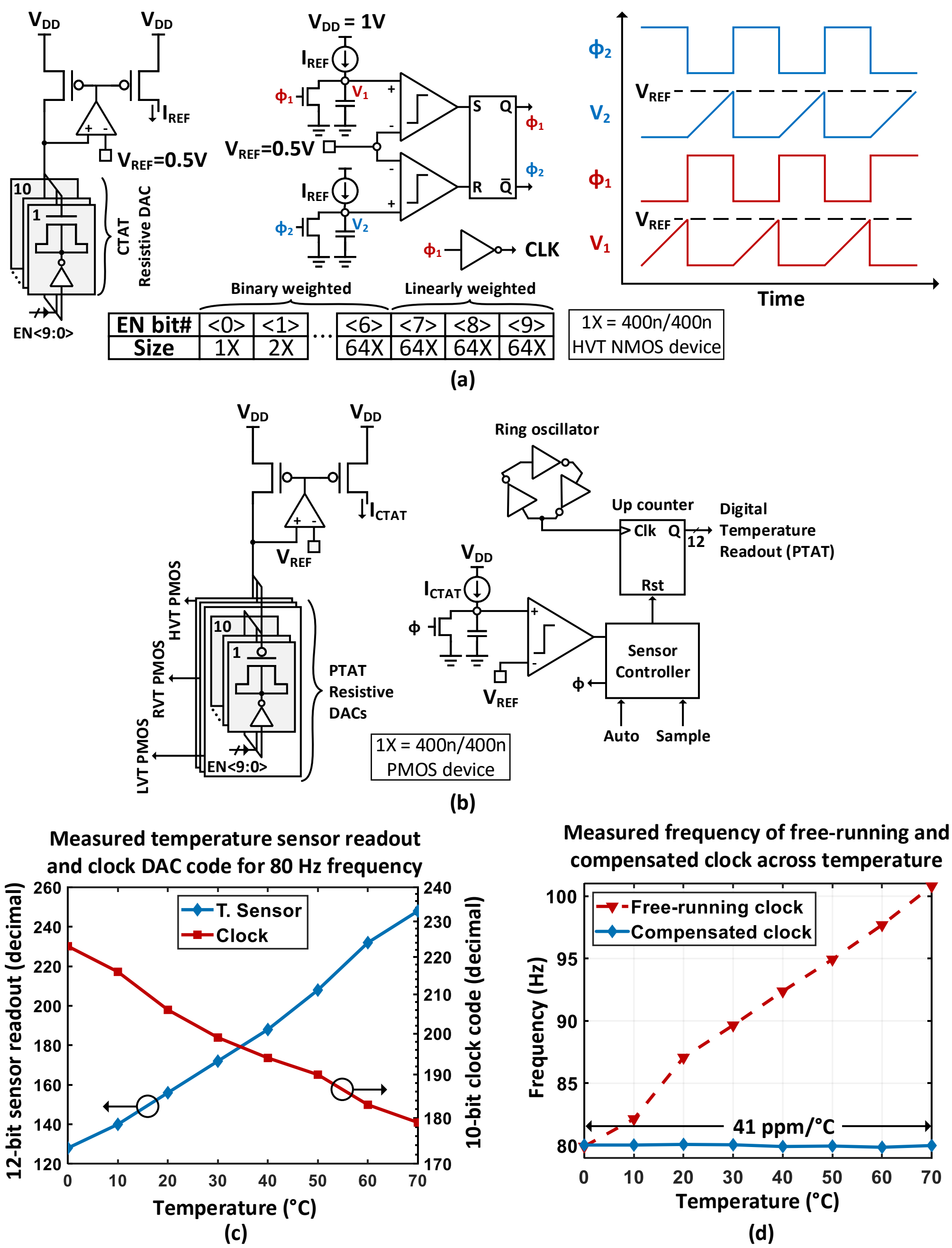


Figure 3.5: (a) Schematic and transient waveforms of the area-efficient, gate-leakage-based, dual-phase relaxation oscillator. (b) Schematic of the area-efficient, gate-leakage-based temperature sensor. (c) The measured temperature sensor readout and clock DAC code used to maintain an 80 Hz clock frequency across temperature. (d) Measured frequencies of the compensated and free-running clocks across the commercial temperature range.

The schematic of the proposed clock is exhibited in Figure 3.5(a). To generate a reference current with a fA-level LSB resolution, the clock uses the gate leakage of high-voltage-threshold (HVT) NMOS devices from the design kit. The HVT NMOS devices have resistive behaviors comparable to a complimentary-to-absolute-temperature (CTAT) resistance. The proportional-to-absolute-temperature (PTAT) current generated by this DAC is used in the charge pumps of the dual-phase RXO. In every cycle, one charge pump sets the SR latch, and, in the next cycle, the other charge pump resets the SR latch. The latch output is buffered and used for the system clock. For a fixed setting on the DAC, the clock frequency exhibits a PTAT behavior, which requires compensation across temperature.

Fig. 3.5(b) illustrates the schematic of the temperature sensor. The sensor consists of an RXO that determines the window during which it counts the number of zero crossings of a ring oscillator (RO). The RXO uses a CTAT gate-leakage-based reference current that is generated by PMOS devices in the design kit with PTAT resistive behavior. Therefore, the temperature sensor generates a PTAT digital temperature readout. This readout is used as the address of an off-chip look-up table to determine the required clock DAC word for maintaining an 80 Hz clock frequency. Figure 3.5(c) presents the measured values for the clock DAC word and temperature sensor readout across temperature. The measurement in Figure 3.5(d) compares the frequency drift of the calibrated clock to the free-running clock that is tuned to 80 Hz at 0°C. The calibrated clock drifts less than 41 ppm/°C across the commercial temperature range from 0 to 70°C, while the uncalibrated clock frequency drifts at an average rate of 0.3 Hz/°C across the temperature range.

The clock calibration loop introduced in this section uses an off-chip look-up table for testing flexibility. However, this approach can be implemented on-chip using nW-powered synthesized logic. The most accurate calibration method consists of using the sensor readouts on each die as the LUT addresses that determine the corresponding clock tuning bits. Alternatively, a more efficient approach is to collect a large set of temperature sensor data points across temperature and fit a second-order polynomial to the readouts. Once the polynomial's coefficients are determined, each sensor can be calibrated at one or two intermediate temperatures.

3.5 Proof-of-Concept Temperature- and Interference-Robust X-Band WuRx

This section presents a temperature- and interference-robust proof-of-concept WuRx in the 0 to 70°C commercial range that operates at the 9.6 GHz X-band RF frequency. Using a 63-bit wakeup code at a data rate of 20 b/s, the WuRx achieves a sensitivity of −65 dBm with $<$2 dB degradation across the temperature range. It consumes an average power of 27.6 nW at 20°C, which increases at a rate of 1.4 nW/°C. The measured results demonstrate that the WuRx can tolerate up to 9 dBc of in-band CW blockers and up to 16.9 dBc of out-of-band 10 MBaud PRBS7 16-QAM modulated blockers. The CMOS chip is fabricated in a low-power mixed-signal RF 65 nm process and occupies a total area of 3 mm^2.

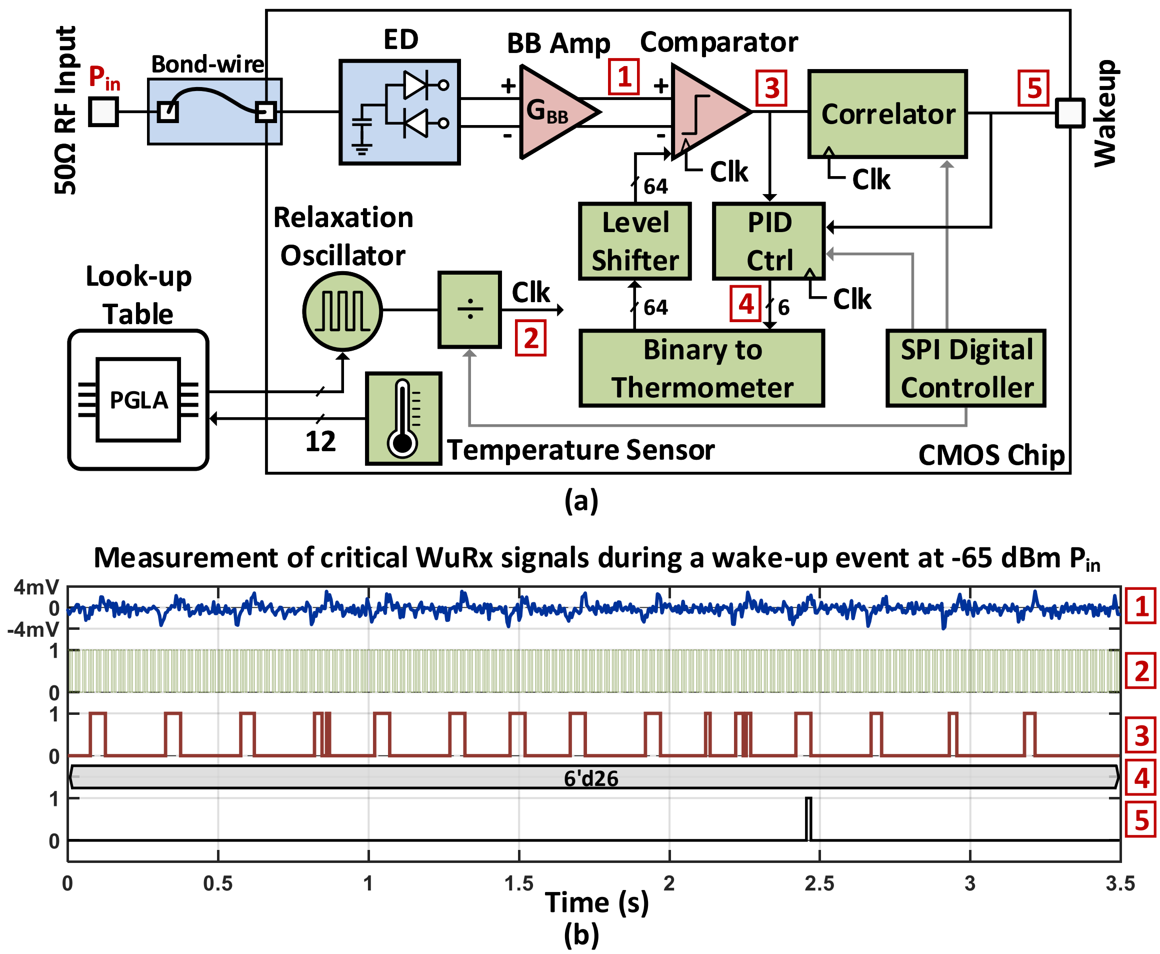


Figure 3.6: (a) Wakeup receiver block diagram, and (b) the combined measurement of its internal signals during the successful reception of an RF wakeup.

The block diagram of the WuRx is presented in Figure 3.6(a), and the combined measurement of the critical internal signals when an RF wakeup is successfully detected is exhibited in Figure 3.6(b). The WuRx front-end consists of a pseudo-differential, passive, diode-based ED, whose input impedance is transformed to a 50 Ω RF input using the inductance of a bond wire. The μV-level output baseband signal of the ED is amplified with the baseband amplifier to a mV-level signal prior to digitization. The comparator digitizes the differential output of the amplifier at a 4$\times$ oversampling rate of 80 Hz, and its decision threshold is adjusted with a nW-power PID controller. The PID controller calibrates the number of false positives out of the comparator continuously, while providing a sufficient time delay for the wakeup signal to be detected without increasing the comparator's decision threshold.

The output bit stream of the comparator is processed using a 63-bit four-phase correlator with a programmable error tolerance that issues a wakeup flag when at least one of the phases finds a match for the reference wakeup code. The WuRx clock is a sub-nA dual-phase relaxation oscillator (RXO) that uses an area-efficient, gate-leakage-based current DAC providing fA-level tunability. To achieve a stable sampling frequency across temperature, the clock DAC is controlled using the digital readout of the temperature sensor. An SPI digital controller stores the values for the wakeup code, PID coefficients, and the DACs of the clock and temperature sensor.

3.5.1 RF and Analog Front-End Design

The schematic of the eight-stage pseudo-differential [117], Dickson-based ED is depicted in Figure 3.7(a). The ED topology allows for a differential design of the WuRx without using lossy RF baluns, resulting in robustness to common-mode and kickback noise. One main design consideration is the dc coupling of the outputs of the ED to the subsequent baseband amplifier stage. The reason for this choice is that placing a capacitor at the output of the ED will create a low-frequency pole that can distort the baseband wakeup signal by high-pass filtering it [131]. Ideally, this pole should be 10^{-3} times lower than the wakeup signal rate [132]. However, due to the smaller number of ED stages compared to prior implementations [125], which is required for high-frequency operation, reducing this pole to sub-mHz frequencies is very challenging and requires a prohibitively large coupling capacitor. As a result, instead of connecting the node X to the ground, the capacitor $C_0 = 100\ fF$ provides an ac short at this node, while allowing the diodes to accept a dc bias from the baseband amplifier.

The transient response of the ED is measured with a -30 dBm input RF signal at 9.6 GHz and is presented in Figure 3.7(b). The measured charge time value of $t_r = 130\ \mu s$ is significantly greater than the simulated value of $t_r = 1.36\ \mu s$ because the observability buffers drive a large capacitance due to the loading of the PCB, cable, and oscilloscope. The ED power sensitivity k_{ED} is measured using a 50 Ω probe and a power source calibrated for the cable and probe losses, and demonstrates functionality up to the X band (Figure 3.7(c)). Here, k_{ED} relates the output voltage of the ED (V_{out}) to the available input power of the 50 Ω source via $V_{out} = k_{ED} \times P_{in}$ in the quadratic regime.

The inductance of a bond wire and the capacitive portion of the ED input impedance are used to transform the high input impedance of the ED to the 50 Ω input port. The test structure exhibited in Figure 3.8(a) is used to measure the quality-factor of the 1 mil-diameter Aluminum bond wire used in the LC impedance transformer. This measurement uses a custom-made, on-chip SOLT calibration standard (Figure3.8(b)) to place the VNA reference plane at the tip of the bond wire contacts. The measurement result is plotted in Figure 3.8(c), which suggests that the quality-factor of a ≈ 1 nH bond wire at the X band is around nine.

Figure 3.8(d) presents a photo of the packaged chip-on-board system. The 50 Ω input GCPW transmission line resides on the top layer of the mixed material PCB, which consists of a 15 mil Duroid RT5880 substrate with FR4 layers on the bottom to provide mechanical rigidity. Figure 3.8(e) presents the measured and simulated S_{11} of the matched ED. The simulation uses bond wire parameters acquired from the measurement made in Figure 3.8(c). The discrepancy between the measured and simulated S_{11} is likely due to the different shapes of the bond wires and the mutual inductance between the ground and RF signal bonds. The simulated value of the transducer voltage gain G_T of the impedance transformer, using the measured bond wire parameters, is around 11 dB at 9.6 GHz (Figure 3.8(f)). More advanced packaging techniques such as flip-chip bonding on a low-loss substrate can improve the loss of the matching network further and take advantage of the high-impedance input interface.

The baseband amplifier design objective is to convert the μV-level output signal of the ED to a

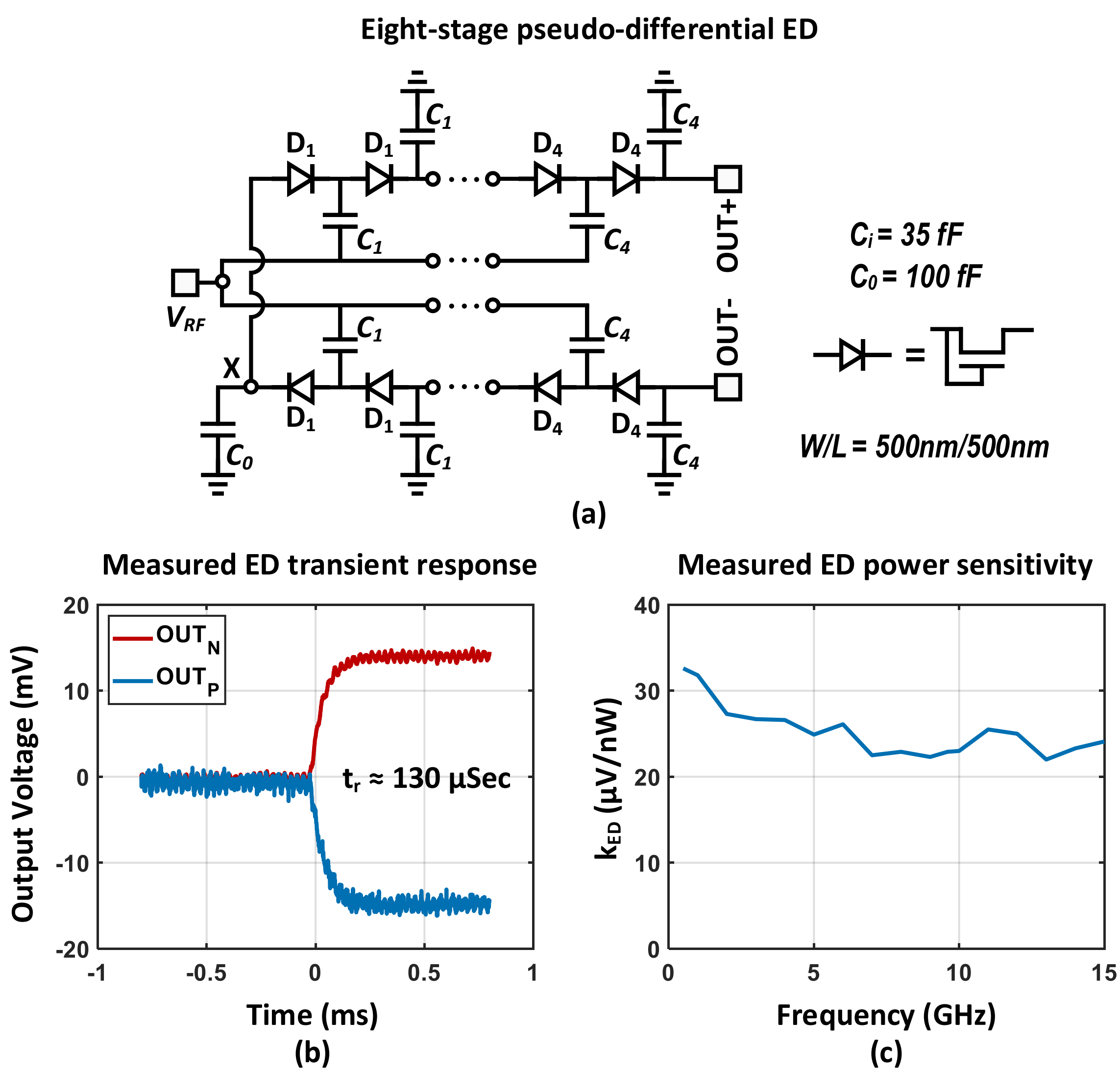


Figure 3.7: (a) Schematic of the eight-stage pseudo differential envelope detector and its (b) measured transient response and (c) measured power sensitivity.

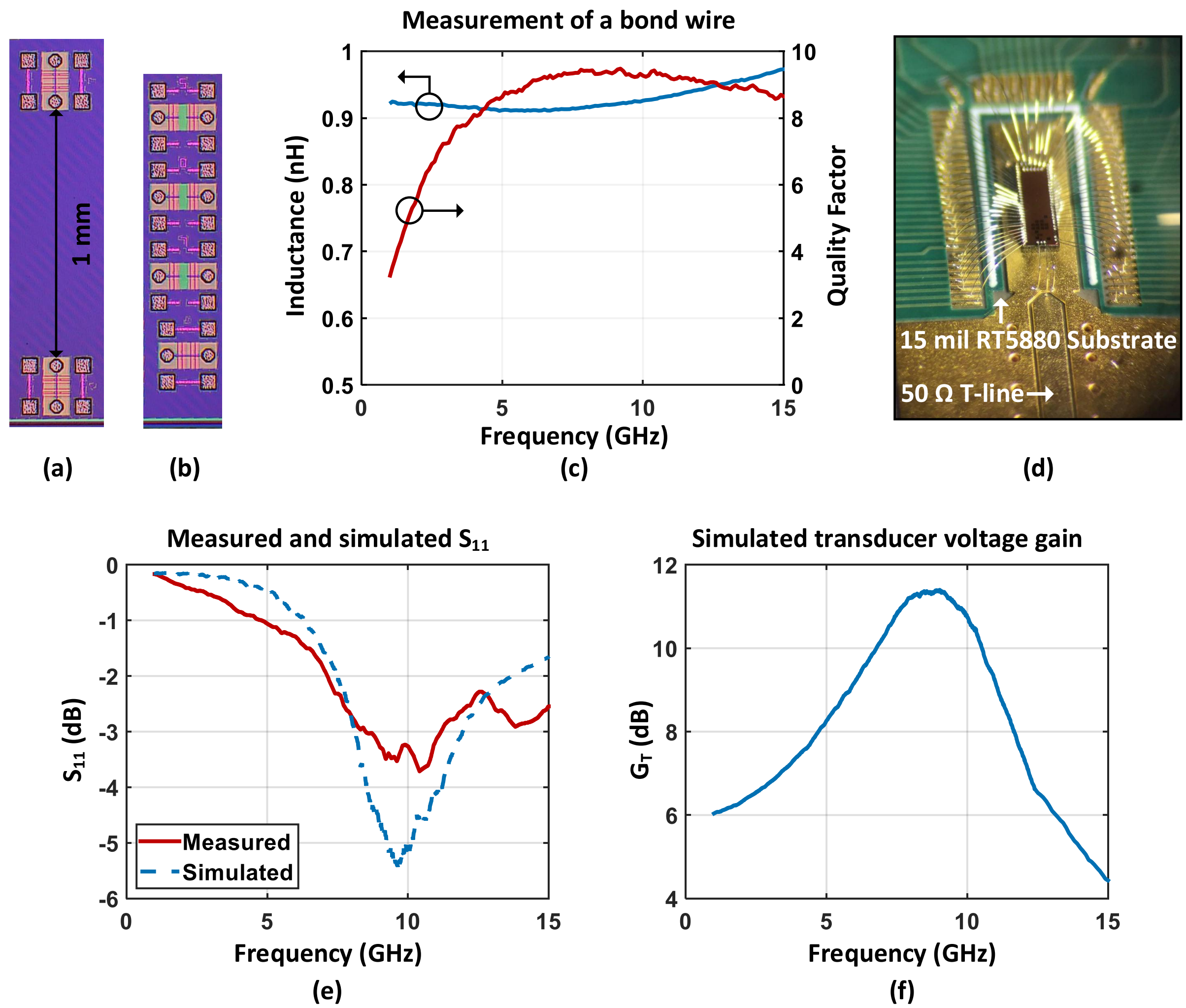


Figure 3.8: (a) Test structure for measuring a bond wire. (b) On-chip calibration standards. (c) Measured inductance and quality-factor of a 1 mm-long Aluminum bond wire with a 1 mil diameter. (d) Photo of the input transmission line and chip-on-board bond wire packaging. (e) Measured and simulated S_{11}. (f) Simulated transducer voltage gain of the impedance transformer.

mV-level signal that is detectable by the comparator. This conversion should ideally keep the output thermal noise of the ED as the dominant source of the pre-digitization noise. The schematic of the two-stage baseband amplifier and the component parameters are presented in Figure 3.9. The first stage of the amplifier is based on the current-reuse, self-biased topology, which can be properly biased with a single current source. The second gain stage is dc coupled to the first stage, and its transistors are sized similarly to the first-stage transistors. Therefore, the second stage is biased by first-stage dc point and a matched current source. The amplifier is designed for a 40 Hz bandwidth from 0.2 to 40 Hz. The first stage uses the Miller effect across the C_f capacitor to

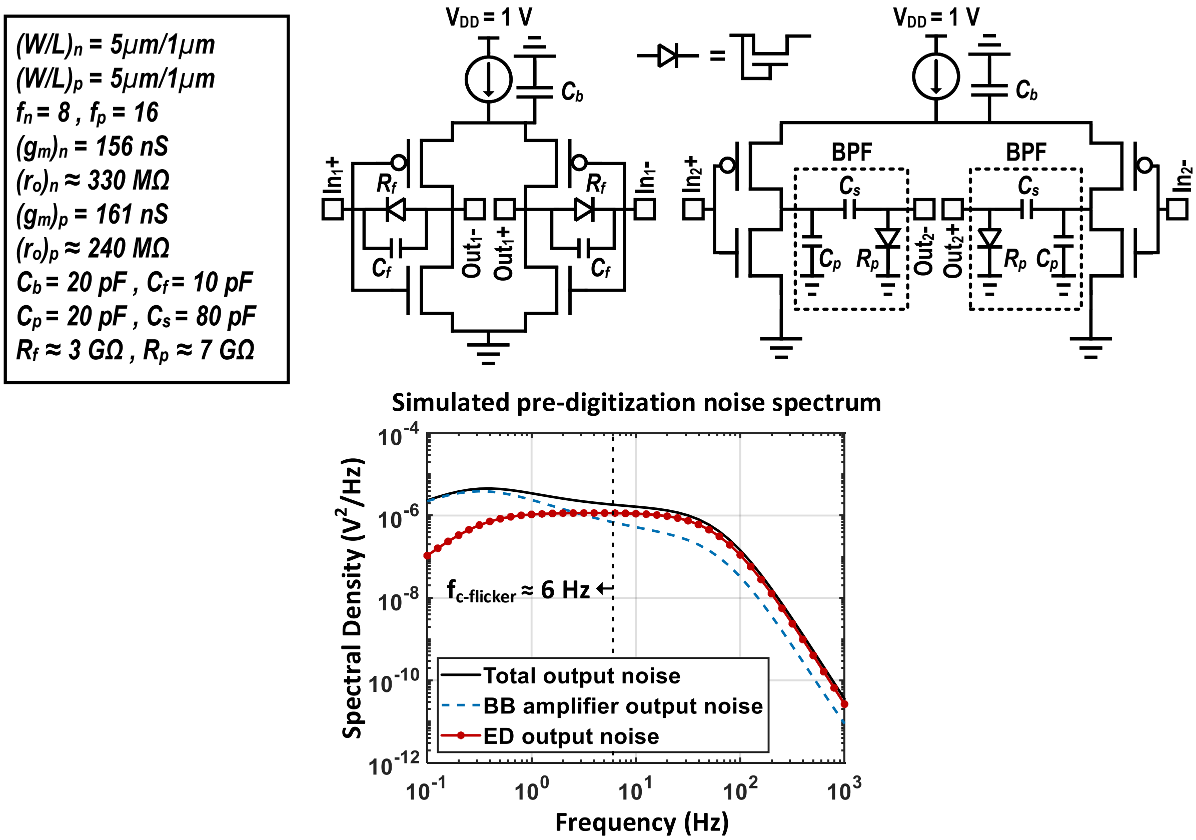


Figure 3.9: Schematic of the two-stage, self-biased, current-reuse baseband amplifier and the simulated pre-digitization noise at the output of the amplifier.

limit the bandwidth, and the output bandpass filter reduces the level of the out-of-band noise. The feedback resistor R_f and high-pass filter resistor R_p are implemented with a diode-connected MOS transistor. Since $R_f >> r_o$, the mid-band voltage gain of each stage is

$$|A_v| = (g_{mn} + g_{mp}) \times (r_{on}||r_{op}) \approx 32\ dB, \tag{3.2}$$

and the amplifier input impedance is $R_f/|A_v| \approx 70\ M\Omega$.

The simulated pre-digitization noise of the front-end is exhibited in Figure 3.9. The amplifier's flicker noise corner is reduced to 6 Hz by increasing the size of the devices and contributes to 12% of the detection noise. The thermal noise of the amplifier is predominantly a function of its bias current, which is limited by the system's power budget. At 10 nA of current for each stage, the amplifier thermal noise contributes to 18% of the detection noise. The ED thermal noise is the dominant source of noise and contributes to 70% of the pre-digitization noise.

3.5.2 System-Level Measurements

To issue a robust wakeup signal and have the ability to discriminate between various nodes, the WuRx uses a fault-tolerant digital correlator with programmable error tolerance. The correlator relaxes the FP and true positive requirements at the output of the comparator and enables a more robust detection in the presence of blockers. The 63-bit, four-phase correlator processes the 4× oversampled output bit stream of the comparator, and, at each phase, determines the distance of the received code from the wakeup code. If either of the phases detects a match with fewer errors than the programmed value, the correlator issues the wakeup flag.

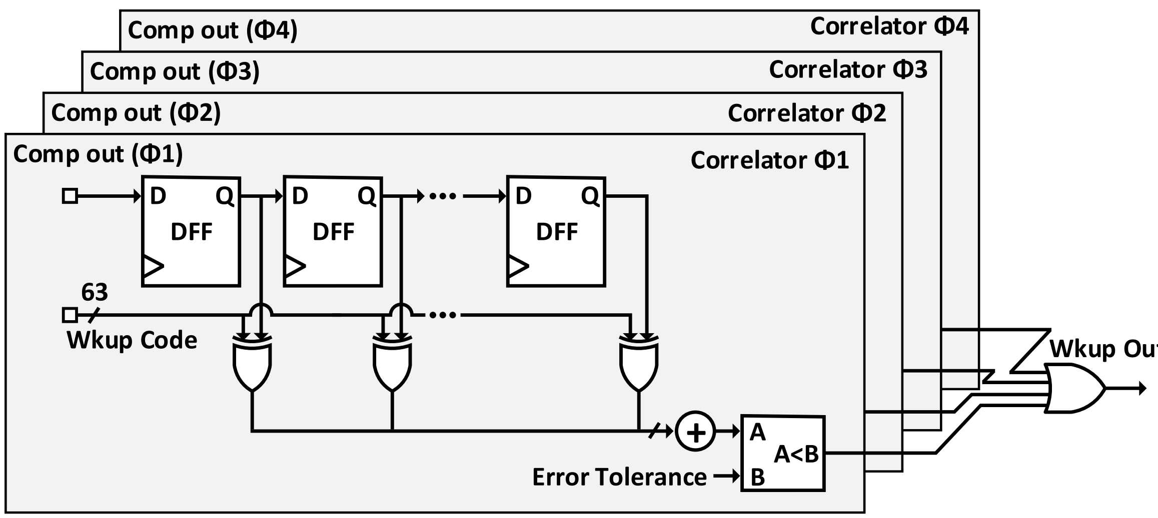


Figure 3.10: Schematic of the 4× oversampled correlator with programmable error tolerance.

The CMOS chip is fabricated in a low-power mixed-signal RF 65 nm process and occupies a total area of 3 mm^2. A photo of the CMOS chip and the measurement setup as well as the equipment used in the wakeup and interference tests are presented in Fig. 3.11.

The WuRx sensitivity measurements are made under the criteria of less than 1 FP per hour and better than 10^{-3} MDR. The FP rate measurements at each temperature are averaged over 12 hours in a quiet RF environment. The MDR measurements use 10^4 wakeups that are sent every five seconds (14-hour-long measurement at each temperature) without any synchronization between the transmitting signal generator and the on-chip clock. The output power for the wakeup signal and interference are calibrated to account for cable and connector losses. The measurement in Figure 3.12(a) illustrates that the correlator relaxes the FP ratio at the output of the comparator by about two orders of magnitude, allowing for a lower decision threshold and higher sensitivity. The measured WuRx waterfall curve at 20°C is presented in Figure 3.12(b). The WuRx achieves a sensitivity of -65 dBm and 18 dB of dynamic range. RF wakeup powers greater than -47 dBm saturate the baseband amplifier and cannot be detected by the receiver. The measured WuRx sensitivity

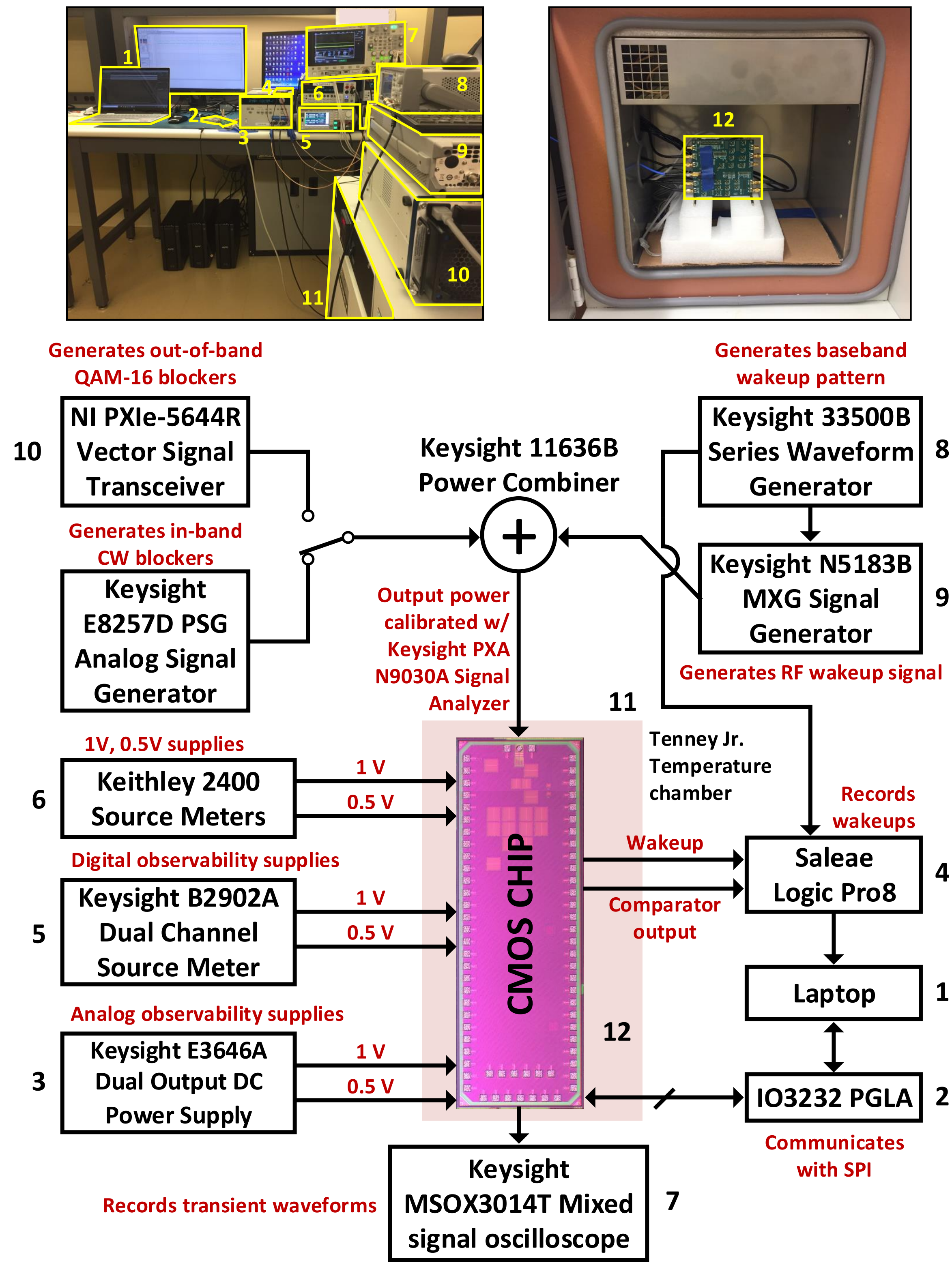


Figure 3.11: Photos of the measurement setup, schematic of the measurement equipment used in the wakeup and interference tests, and a photo of the chip.

and MDR versus temperature plotted in Figure 3.12(c), (d) illustrate that the WuRx sensitivity of -65 dBm degrades by less than 2 dB across the temperature range. An X-band airborne station with 1 W isotropic transmitter power can trigger a ground-level node with -65 dBm of sensitivity from a distance of about 180 m. If the transmitter and WuRx use antennas with 10 dBi of gain, the communication range increases to $\approx$1.5 km.

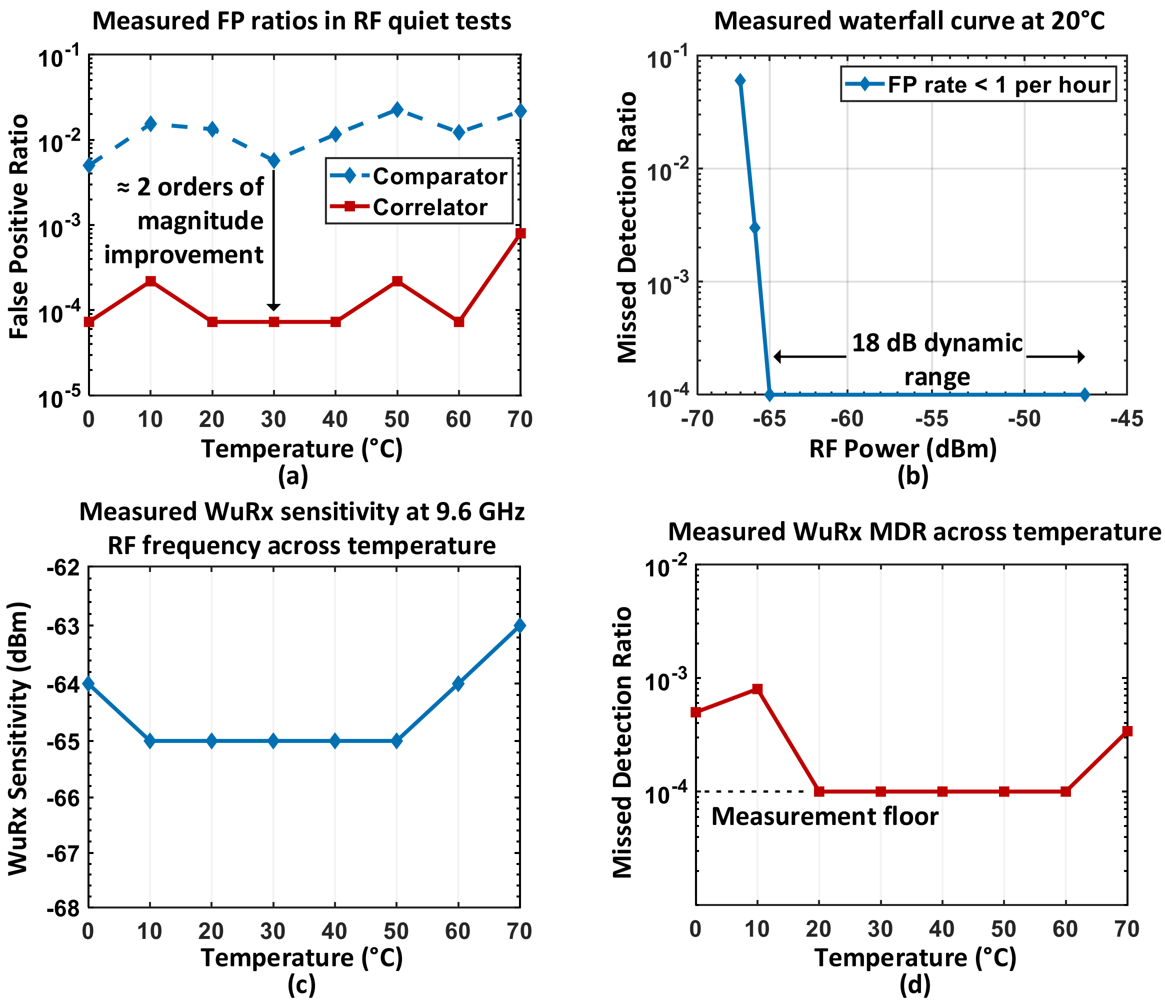


Figure 3.12: Measurement plots of (a) the FP ratio versus temperature, (b) the WuRx waterfall curve at 20°C, (c) WuRx sensitivity versus temperature, and (d) MDR versus temperature.

A transient measurement of the WuRx detecting a -60 dBm RF wakeup in the presence of a -58 dBm 20 b/s OOK blocker at 5.8 GHz is presented in Figure 3.13(a). The WuRx's robustness to interfering signals is measured using various types of in-band and out-of-band interferers. In the interference measurements, the RF wakeup power is set 3 dB higher than the WuRx sensitivity, and the interferer power is increased until the MDR returns to 10^{-3}. The in-band tests use continuous-wave (CW) signals at 3 MHz and 12 MHz offsets, and the out-of-band tests use 10 MBaud PRBS7

QAM-16 modulated signals. The measurement results presented in Figure 3.13(b) demonstrate that the WuRx is robust to 9 dBc in-band interferers and 15 dBc, 16 dBc, and 16.9 dBc out-of-band interferers in the 5.8 GHz ISM, 2.4 GHz ISM, and 750 MHz 4G-LTE bands, respectively.

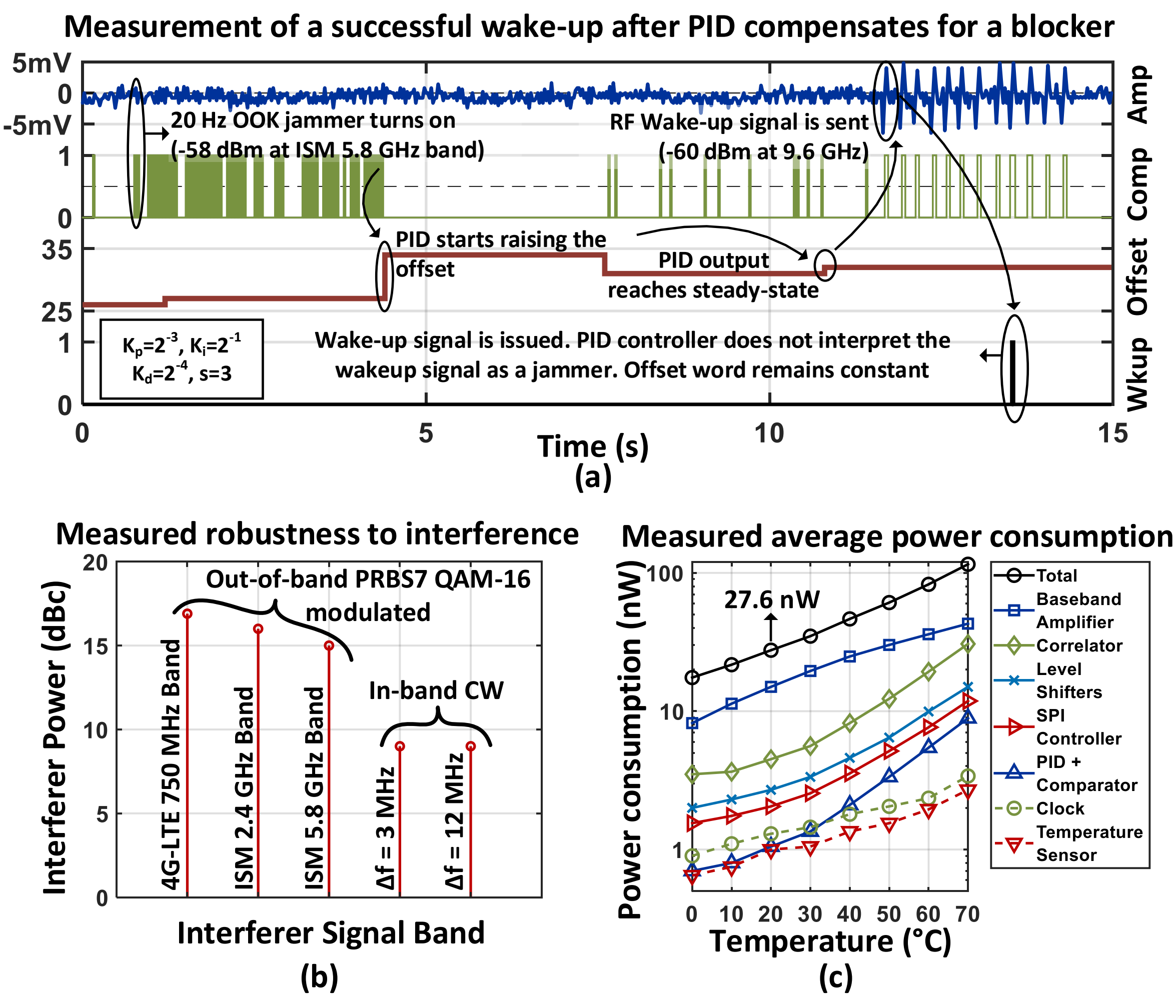


Figure 3.13: (a) Measurement of the WuRx detecting an RF wakeup in the presence of a blocker. (b) Measured WuRx robustness to in-band and out-of-band interference. (c) Measured WuRx power consumption breakdown versus temperature.

Figure 3.13(c) presents the measurement of the WuRx power consumption breakdown across the temperature range. The WuRx consumes an average power of 27.6 nW at 20°C, with the lowest power consumption of 17.5 nW at 0°C and the highest power consumption of 115.4 nW at 70 °C. The power consumption of the WuRx increases at a rate of 1.4 nW/°C across the temperature range. The performance summary and a more detailed comparison with prior state-of-the-art are provided in Table 3.1 [102, 104, 112, 133, 134].

Table 3.1: Performance summary and comparison table for the proof-of-concept X-band WuRx.

	This Work	TMTT'20		JSSC'20	VLSI'19	ISSCC'19		ISSCC'18		RFIC'17	ISSCC'15
CMOS Technology	65 nm LP	65 nm LP		65, 180 nm	65 nm LP	65 nm LP		130 nm		65 nm	65 nm
Carrier Frequency	9.6 GHz	2.2 GHz		9 GHz	428.3 MHz	434.4 MHz	151.25 MHz	151.8 MHz	433 MHz	2.4 GHz	2.4 GHz
Temperature Range	0-70 °C	N/A	N/A	-10-40 °C	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Power Consumption	27.6 nW	11.3 nW	28.2 nW	22.3 nW	33 nW	0.42 nW	0.37 nW	7.4 nw	7.4 nw	365 nW	99 μW
Bit Rate (R_b)	20 bps	250 bps	250 bps	33.3 bps	3 bps	100 bps	100 bps	200 bps	200 bps	2.5 kbps	10 kbps
Interferer Rejection Method	Bond wire-based match, PID Controller	Off-chip stub matching		High-Q FE	High-Q FE, AGOC	High-Q FE, DLL for CW interferers		High-Q FE, Offset controller		High-Q FE Co-Design	N-path filter
Sensitivity	-65 dBm @ 20°C (<-63 dBm)	-65 dBm	-68 dBm	-64 dBm	-106 dBm	-79.1 dBm	-78.3 dBm	-76 dBm	-71 dBm	-61.5 dBm	-97 dBm
Sensitivity in the presence of interfering signals	-62 dBm w/ interferers: 9dBc CW @ 3MHz offset, 9dBc CW @ 12MHz offset, 15dBc QAM16 @ 5.8GHz, 16dBc QAM16 @ 2.4GHz, 16.9dBc QAM16 @ 750 MHz[1]	-65 dBm w/ 20dBc CW interferer @ 3MHz offset	-68 dBm w/ 20dBc CW interferer @ 3MHz offset	Using antenna -68.5 dBm w/ ~ 2 dBc PRBS @ 0.3 GHz offset	-103 dBm w/ 16dBc CW @ 3MHz offset[2]	-77 dBm w/ 14dBc CW, -5.8dBc OOK interferer @ 3MHz offset[1]	-77 dBm w/ 23.3dBc CW, 3.6dBc OOK interferer @ 3MHz offset[1]	-76 dBm w/ 30dBc CW interferer @ 3MHz offset[1]	N/A	-58.5 dBm w/ 19.1dBc CW, 19dBc FM, 10dBc AWGN interferer @ 3MHz offset[3]	-94 dBm w/ 31dBc, 27dBc CW interferer @ ±5MHz offset[3]
Figure of Merit	117.1 dB	126.5 dB	125.5 dB	118.1 dB	155.6 dB	152.9 dB	152.6 dB	138.8 dB	133.8 dB	112.9 dB	147 dB
Die Area	3 mm^2	3.9 mm^2		14.mm^2	3.95 mm^2	0.093 mm^2 *		1.95 mm^2		1.1 mm^2 *	0.0576 mm^2 *

[1] Measured for 10^{-3} MDR [2] Measured for 10^{-2} MDR [3] Measured for 10^{-3} BER * Active area

3.6 Proof-of-Concept S-band WuRx

This section presents a proof-of-concept sub-100 nW CMOS WuRx with ED-first architecture that operates at the 2.2 GHz S band RF frequency. The WuRx can operate in two modes, allowing a trade-off between power consumption and RF sensitivity. In the low-power mode, the WuRx consumes 11.3 nW and achieves an RF sensitivity of -65 dBm. In the high-sensitivity mode, the WuRx consumes 28.2 nW of power and achieves a sensitivity of -68 dBm. Measurement results indicate that the WuRx architecture is robust to continuous-wave, in-band interferers with as large as -20 dB carrier-to-intereferer ratio. A system-level block diagram of the ED-first architecture wakeup receiver is shown in Figure 3.14. The voltage gain of the stub-based matching network (G_{MN}), minimum detectable signal of the envelope detector (MDS), and the bandwidth (BW) of the baseband amplifier are the important design metrics for enhancing the SNR at the input of the comparator (SNR_i).

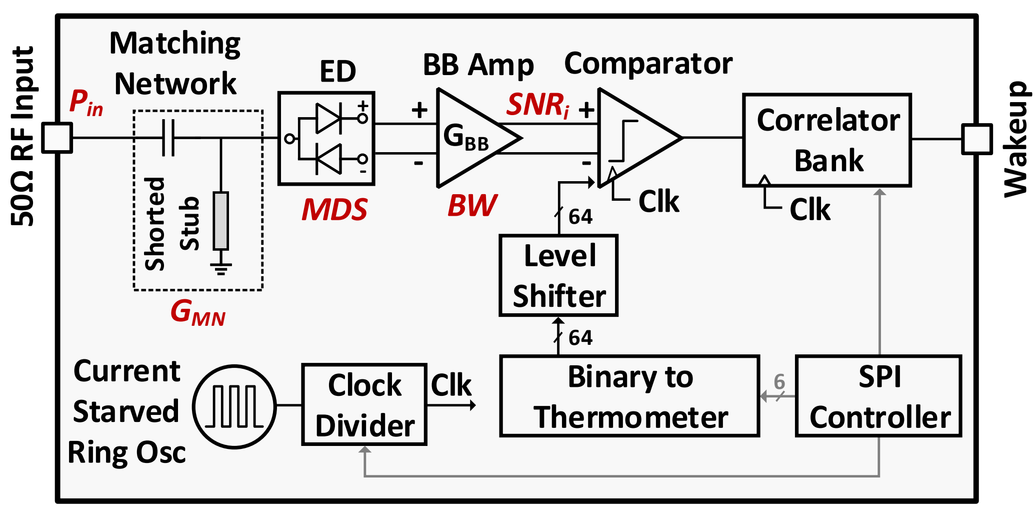


Figure 3.14: System-level block diagram of the ED-first S-band wakeup receiver.

3.6.1 RF and Analog Front-End Design

The ED uses a 24-stage pseudo-differential architecture based on the Dickson detector (Figure 3.15(a)). It uses diode-connected native transistors with $W/L = 500\ nm/500\ nm$, with simulated device shunt resistances of $R_D = 480\ k\Omega$, and parasitic shunt capacitance of $C_D = 0.8\ fF$. The coupling capacitors are minimum-sized, metal-insulator-metal capacitors with $C_C = 35\ fF$. Figure 3.15(b) shows the transient response of the ED outputs measured by an on-chip buffer, showing a charge time of around 383 μS. The measured power sensitivity of the ED is shown in Figure 3.15(c), demonstrating functionality up to the X band.

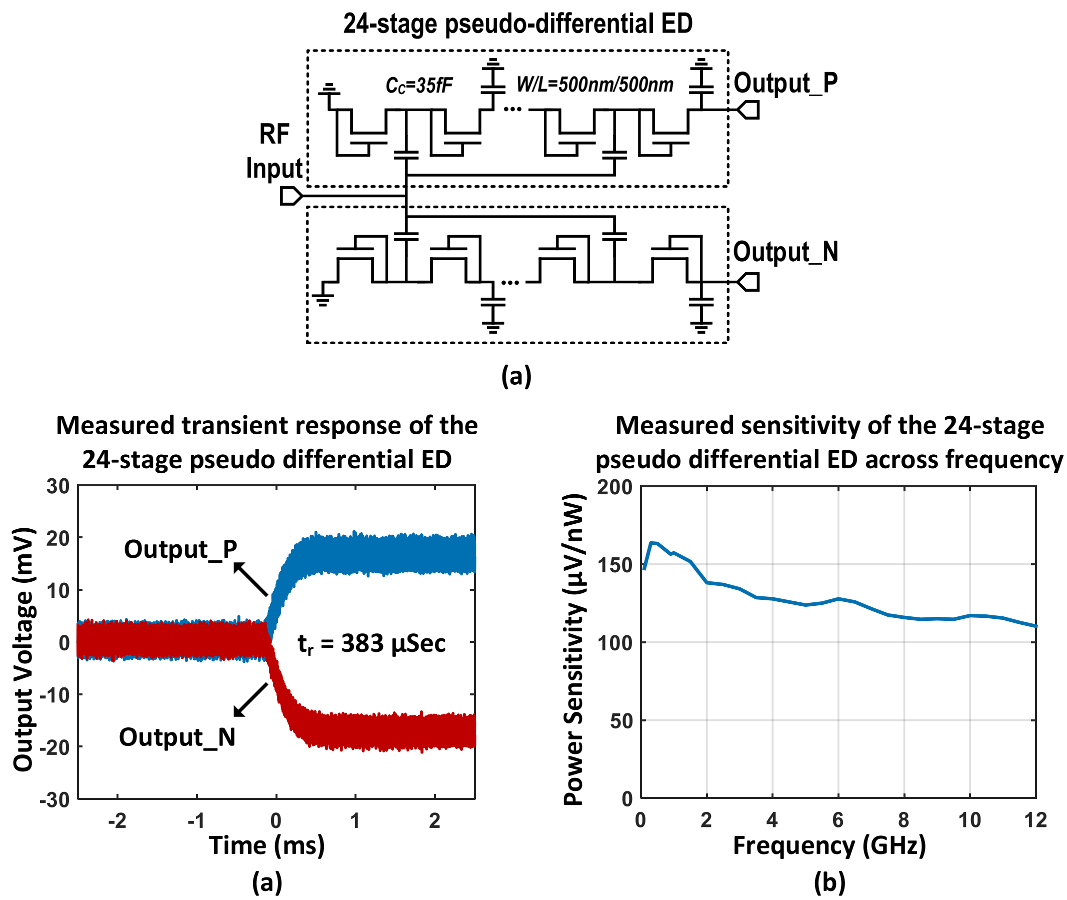


Figure 3.15: (a) Pseudo-differential Dickson envelope detector topology. (b) Measurement of the ED charge time. (c) Measurement of the ED power sensitivity, demonstrating functionality up to the X band.

One other layout consideration is regarding the vias extending up from the ED transistors on the first metal layer to connect them to the coupling capacitors on the top metal layer. In general, routing at a higher metal layer provides the benefit of lower shunt capacitance to the substrate and lower series resistance. However, closely stacked vias can introduce additional shunt capacitance across the diodes. Reducing the shunt routing capacitance of the diodes results in a greater voltage drop across them because the coupling capacitors act as better shorts at RF frequencies. In order to reduce the vertical capacitance between the vias, the vias are configured like a staircase on either side of the diodes, as opposed to being vertically stacked on top of each other. Momentum simulations show that mitigating the via-to-via crosstalk with this technique increases the ED power sensitivity by about 5% at the S band.

Fig. 3.16 compares the measurement results for the ground-backed ED input impedance to the simulation results. The perforated ground plane in the layout is replaced with a solid metal 1 layer to reduce simulation complexity. The simulated layout in Momentum provides the S-parameter

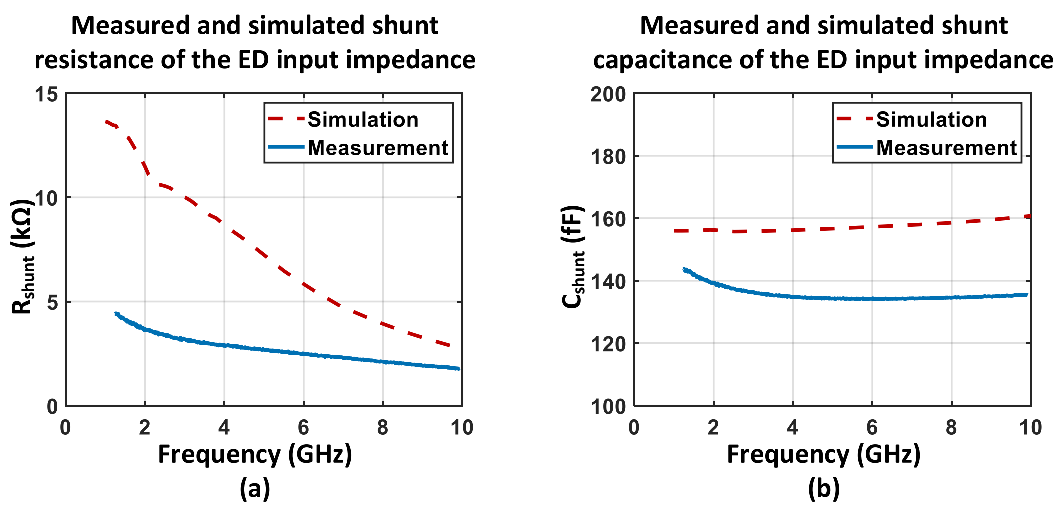


Figure 3.16: Comparison of the ED measured shunt resistance and capacitance with the simulation results.

of the passive layout network. This network is then connected to the coupling capacitors and the transistors in a schematic simulation. The measurement uses a Keysight PNA-X N5245A Network Analyzer and a 67A-GSG-150P Picoprobe, calibrated with a CS-5 calibration substrate. Overall, the simulated impedance values suggest that the substrate shield can increase the MDS of the ED by about 2 dB at the S band and by 6 dB at X band.

The schematic of the stub-based matching network is shown in Figure 3.17. Designing the ED for low MDS is a trade-off between three main effects. Increasing the number of ED stages will increase the amplitude of its output baseband voltage proportional to the number of stages, N. However, at the same time, it increases the output noise proportional to $\sqrt{N}$, which at weak excitations, is dominated by the thermal noise of the diode-connected devices [123]. Alternatively, adding more stages reduces the shunt input resistance of the ED $R_{in} \approx R_D/2N$, which, in turn, reduces the maximum achievable voltage gain of the matching network, as shown in Figure 3.17(b). It also increases the shunt input capacitance of the ED, as $C_{in} = 2N \times \widetilde{C}_D$, where $\widetilde{C}_D = C_D + C_{routing}$ is the per-stage capacitance, including the device and routing capacitances. This increase means that a smaller-sized inductor L_P needs to be used at a given frequency, resulting in a smaller residual shunt resistance R_P for a given Q.

Figure 3.17(c), (d) present the ADS Momentum simulation results for the shorted stub with $W = 30\ mil$ and $L = 550\ mil$ on a 62 mil Rogers 4003C board. The on-chip capacitor $C_m = 60\ fF$ is implemented to create an L-match impedance transformer with the inductive shorted stub. Figure 3.17(e),(f) depicts the measurement results for the S_{11} and transducer voltage gain (G_T) of the matched ED, showing a match at 2.2 GHz with 12.6 dB of transducer voltage gain. To measure the G_T, a 50 Ω probe drives the ED input, and the output voltage of the ED without the matching network is measured. Then, after connecting the matching network, the ED output voltage is measured, and the G_T is de-embedded from these two measurements.

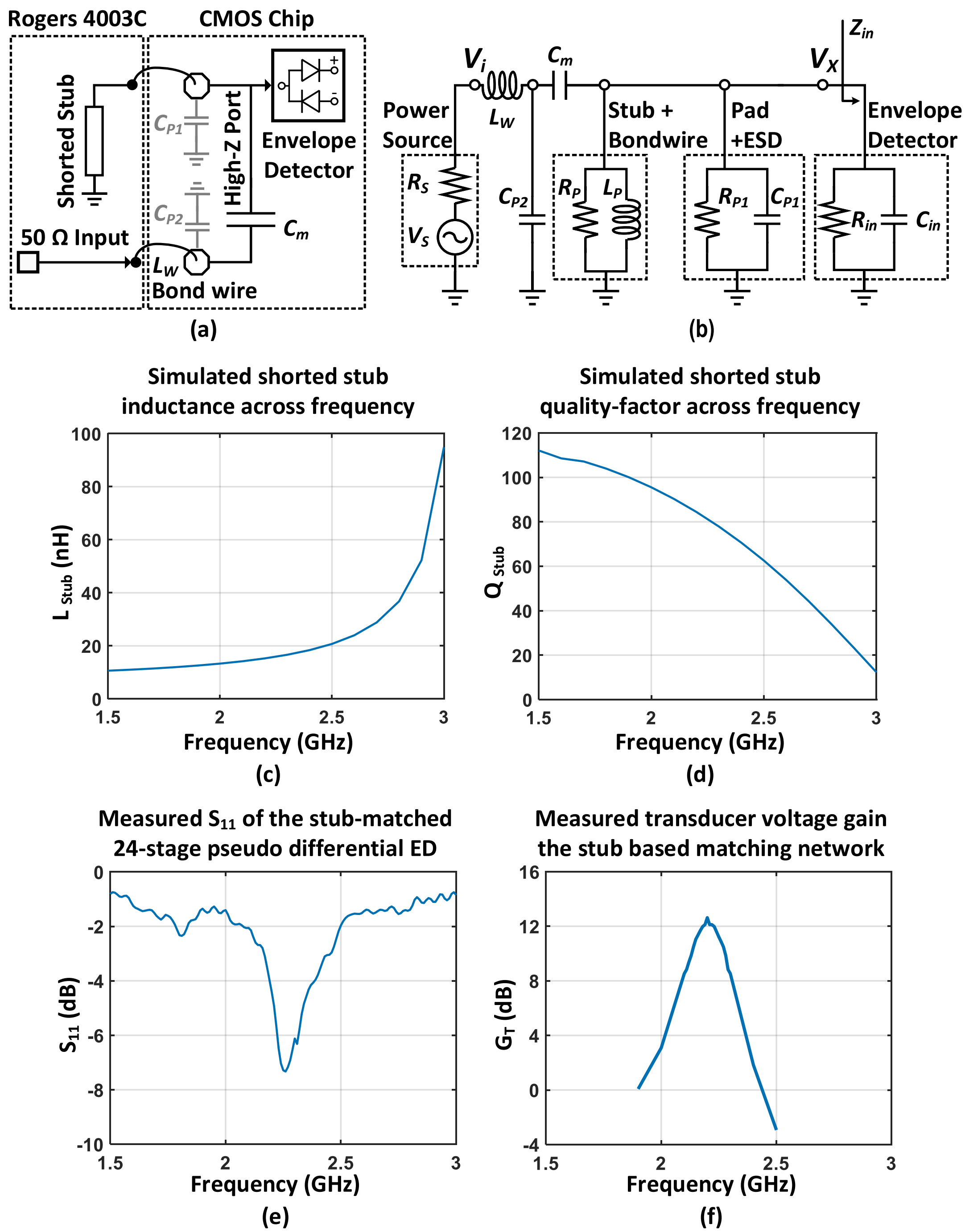


Figure 3.17: (a) Schematic and (b) circuit model of the stub-based matching network with the parasitic bond wire inductances and pad and ESD capacitances. Simulated (c) inductance and (d) quality-factor of the shorted stub with $W = 30\ mil$ and $L = 550\ mil$ on a 62 mil Rogers 4003C board. Measurements of the (e) S_{11} and (f) transducer voltage gain of the stub-based matching network, with 12.6 dB of voltage gain at 2.2 GHz.

Figure 3.18(a), (b) shows the architecture of the ULP baseband amplifier gain stage and its subsequent buffer stage, which provides additional noise filtering before the comparator. The differential outputs of the ED drive the differential inputs of the baseband amplifier. The bandwidth of the baseband amplifier is about 1 kHz. Both stages can be biased using current sources, without need for any bias voltages. The input ac coupling capacitors $C_{ED} = 60\ fF$ have a significant role in enhancing the robustness of the WuRx to continuous wave (CW) intereferers. A CW interference can create dc offsets at the output of the ED and change the bias point of the amplifier, which is sensitive to voltage fluctuations in the sub-threshold regime. The capacitor $C_f = 250\ fF$ takes advantage of the Miller effect across the gain stage to limit the input bandwidth to 1 kHz. The current sources located between the amplifier and the supply as well as the bypass capacitor $C_b = 80\ pF$ provide isolation from supply noise. The bandpass filter at the output of the buffer stage provides a second-order 40 dB per decade roll-off for the transfer function to filter the out-of-band noise. The lower pole of the bandpass filter (BPF) at the output buffer stage is set at 10 Hz, and the higher pole is set at 1 kHz.

The most important consideration regarding the design of the baseband amplifier stage is limiting its noise contribution to the FE chain so that its input-referred noise does not dominate the ED output thermal noise. The two main sources of noise in the baseband amplifier are the flicker noise and thermal noise of the gain stage transistors. The flicker noise corner frequency is set at 200 Hz by increasing the gain stage transistor dimensions to $W/L = 6\ \mu m/240\ nm$.

Simulations in Figure 3.18(c) show that for the biasing condition in the LP mode, the ED thermal noise contributes to 65% of the analog FE noise. The thermal noise of each of the four transistors of the baseband amplifier gain stage contribute about 7%, and their flicker noise contributes about 1.5% for each transistor. For the bias conditions of the HP mode, the baseband amplifier transistors are pushed further into strong inversion and the aforementioned numbers change to 87%, 2%, and 1.25%, respectively.

The measured voltage gains of the baseband amplifier across different bias currents are plotted in Figure 3.18(d). For these measurements, the buffer stage current is fixed at 2 nA, and the voltage gain of the amplifying stage is controlled by its bias current. As the gain curves suggest, increasing the bias current pushes the transistors into strong inversion, and a few nanowatts of power can enhance the gain initially by 10 dB. However, the trade-off of gain versus bias current has diminishing returns, and, after some point (about 20 nW), the gain improves incrementally.

Fig. 3.18(e) shows the transient response of the baseband amplifier to a 4 ms rectangular pulse, a full raised-cosine pulse, and a hybrid pulse with a first-half rectangular and second-half raised-cosine roll-off (Figure 3.18(f)). This time domain ringing is an undesired consequence of having a narrow baseband bandwidth that has the potential to cause inter-symbol interference (ISI). This effect limits the available wakeup code space since sending two "one" bits in a row causes the second pulse to fail to reach the same peak point. A hybrid pulse with a smooth roll-off can mitigate this effect. Measurements show that the hybrid pulse maintains the peak value of the rectangular pulse in the first half of the response, but reduces the undershoot in the second half by about 25%.

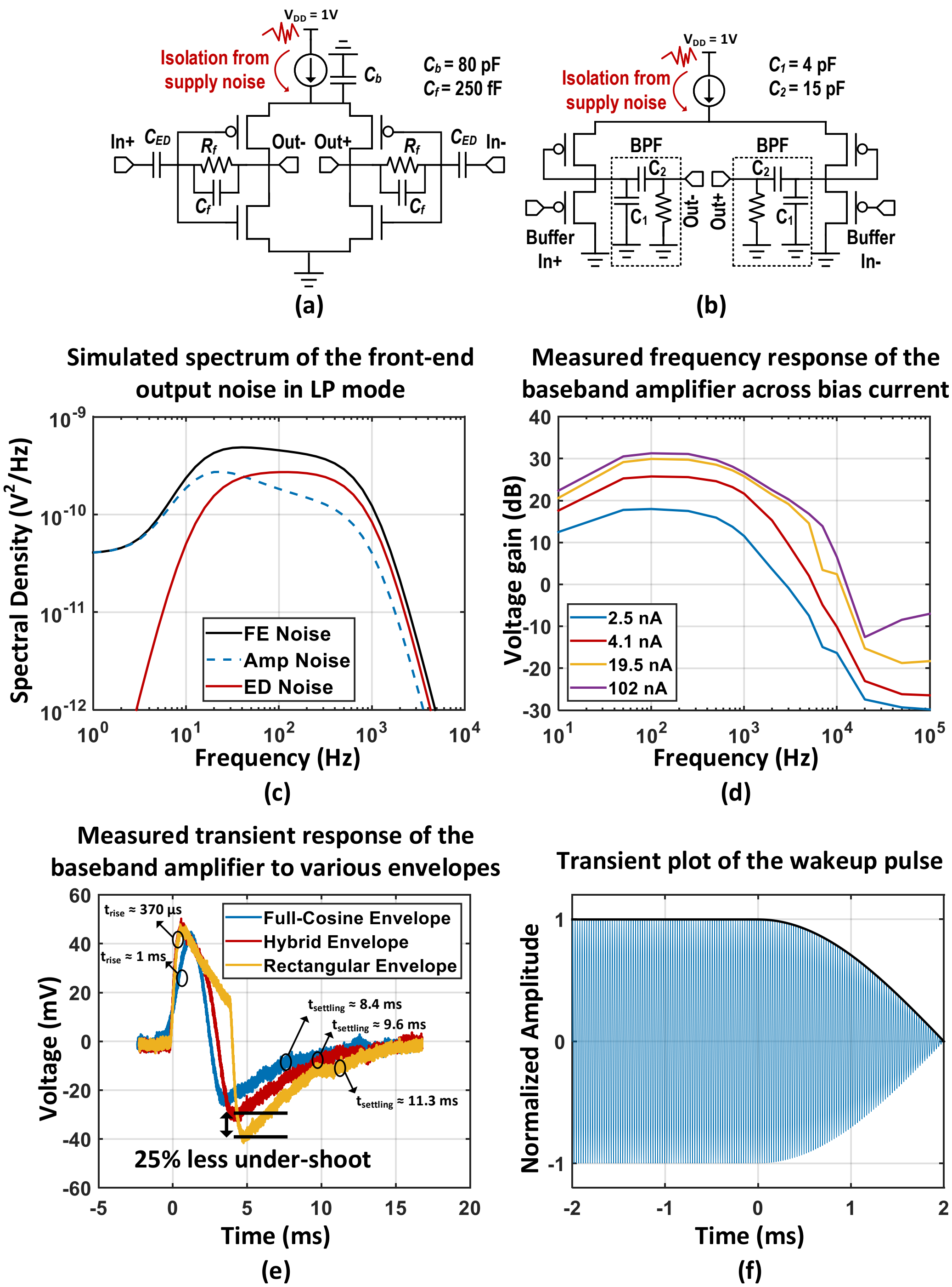


Figure 3.18: (a) Architecture of the self-biased, current-reuse baseband amplifier gain stage and (b) the subsequent buffer stage for additional filtering with a bandpass filter (BPF) load. (c) Simulated WuRx front-end output noise spectrum referred to the baseband amplifier output in LP mode. (d) Measured transient response of the baseband amplifier output voltage shows that a pulse with a smooth tail can reduce the ISI without compromising sensitivity. (e) Measured transient response of the baseband amplifier output voltage shows that a pulse with a smooth tail can reduce the ISI without compromising sensitivity. (f) Transient plot of the hybrid wakeup pulse for “one” symbols.

The clock source, shown in Figure 3.19(a), uses a five-stage differential ring oscillator consisting of leakage-powered delay cells based on [135]. During the steady state, each delay cell holds its differential output within the cross-coupled inverters M_5-M_8, while M_1-M_4 current-starve the inactive devices in each inverter to reduce leakage. When the inputs transition, the M_1-M_4 transistors reverse their configurations and cut off the active devices in the cross-coupled inverters and enable leakage through the inactive devices, thus allowing the leakage current to eventually flip the state of the cross-coupled inverters and transition the differential output. The effectiveness of the supply voltage tuning on the oscillator frequency in this case is limited by Drain-Induced Barrier Lowering (DIBL), because the delay cell transition is limited by the leakage current. Transistors M_9 and M_{10} improve this characteristic by providing additional current during the transition phases of the cross-coupled inverters. The output frequency of the clock can be controlled by the programmable clock divider and its supply voltage. Figure 3.19(b) shows the simulated frequency and power consumption that are achieved by tuning the oscillator supply voltage V_{DD} from 0.3 V to 0.8 V. A 6-bit digital divider is used to tune the oscillator frequency down to the final system clock frequency.

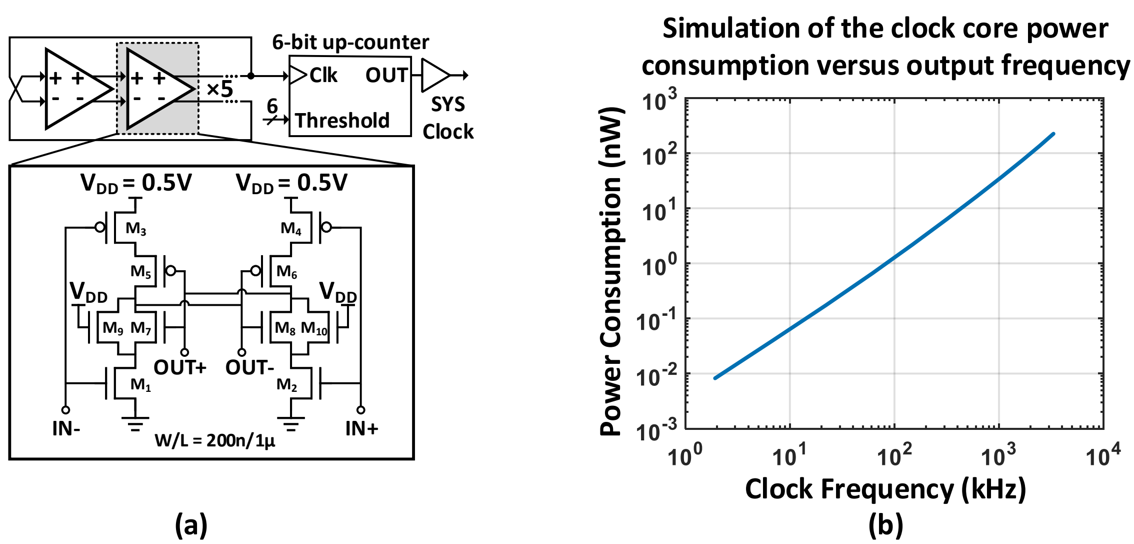


Figure 3.19: (a) Schematic of the ring oscillator clock and the divider following it. (b) Simulation of the clock's power consumption versus its output frequency.

3.6.2 System-Level Measurements

Due to the incoherent nature of WuRx's at such low powers, the comparator output, running at a 1 kHz clock rate, is 4× oversampled, while the analog FE data rate is 250 Hz. The sampled outputs are then distributed by a serial-to-parallel converter to a four-phase correlator. Each phase of the correlator consists of a shift register that compares the wakeup code with the incoming bit stream.

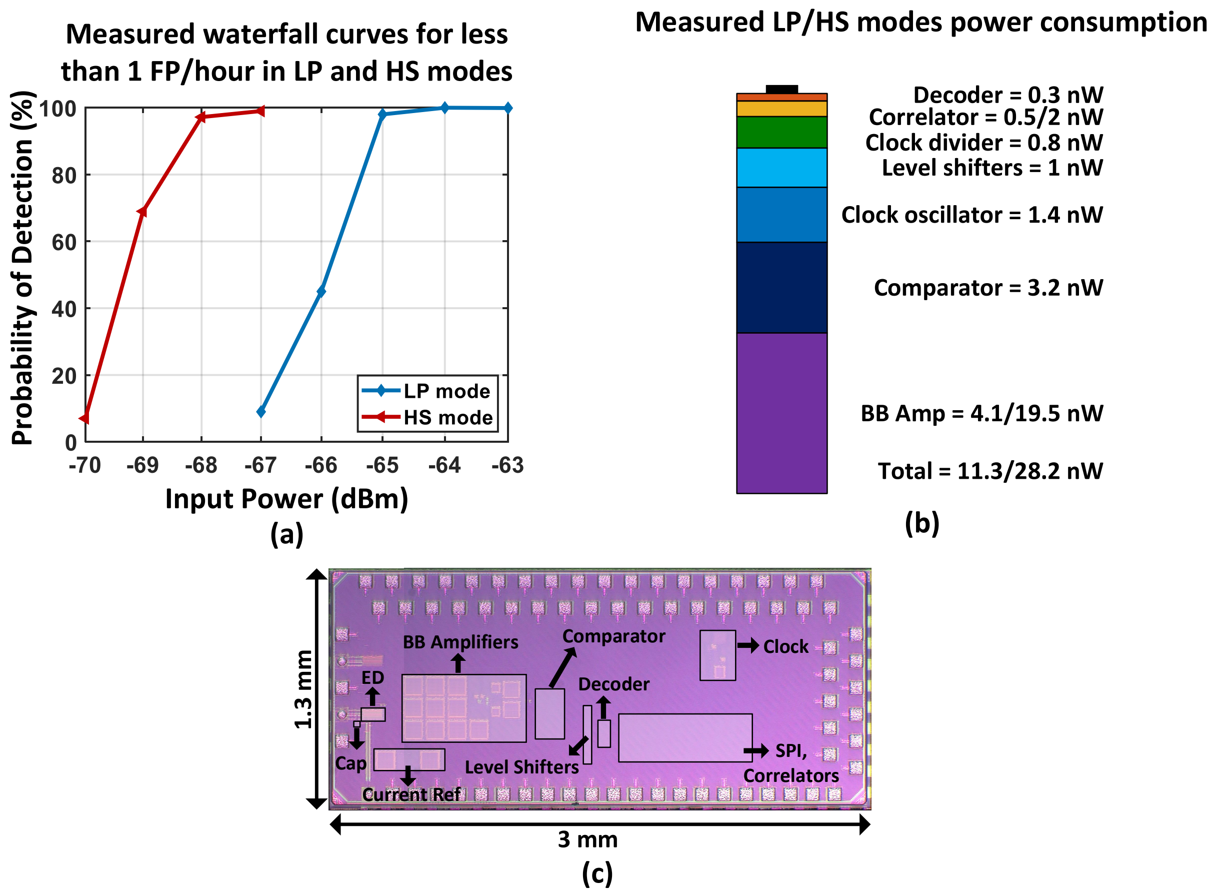


Figure 3.20: (a) Measured waterfall curves in LP and HS mode and (b) their corresponding power consumptions. (c) CMOS die photo.

If the number of errors in either one of the phases is fewer than a programmable threshold, the correlator issues a wakeup.

The chip is fabricated in a 65 nm, low-power CMOS process. Figure 3.20(a) shows the measured sensitivity curves across different input signal powers in the LP and HS modes. In the LP mode, the 8-bit wakeup code is set to 8'h89 with $e = 1$, and, in the HS mode, the wakeup code is set to 63'h4891222248448891 with $e = 13$. The WRX achieves a >98% wakeup detection rate at the decision threshold settings with less than 1 FP/hour with RF power levels of -65 dBm and -68 dBm in the LP and HS modes, while consuming 11.3 nW and 28.2 nW, respectively. The power consumption breakdown is presented in Figure 3.20(b).

Measurements with in-band CW interferers at 3 MHz offsets show that the WuRx architecture is robust to these interference signals and can maintain the sensitivities in both modes in the presence of interference with a -20 dB carrier-to-interference ratio. The die photo is presented in Figure 3.20(c), and Table 3.2 presents the performance summary and a comparison with prior

Table 3.2: Performance summary and comparison table of the proof-of-concept S-band WuRx.

	This Work		Wang SSCL'18	Moody ISSCC'18		Jiang ISSCC'17	Sadagopan RFIC'17	Roberts ISSCC'16	Salazar ISSCC'15	Pletcher ISSCC'08
CMOS Technology	65 nm		180 nm	130 nm		180 nm	65 nm	65 nm	65 nm	90 nm
Carrier Frequency	2.2 GHz		109 MHz	151.8MHz	433 MHz	113.5 MHz	2.4 GHz	2.4 GHz	2.4 GHz	2 GHz
Power Consumption	11.3 nW	28.2 nW	6.1 nW	7.4 nw	7.4 nw	4.5 nW	365 nW	236 nW	99 µW	52 µW
Data Rate	250 bps	250 bps	33.3 bps	200 bps	200 bps	300 bps	2.5 kbps	8.192 kbps	10 kbps	100 kbps
Dissipated Energy per bit	45 pJ	112 pJ	183 pJ	37 pJ	37 pJ	15 pJ	146 pJ	28.8 pJ	9900 pJ	520 pJ
Out-of-band Interferer Rejection Method	Stub matching	Stub matching	High-Q FE Transformer	High-Q FE Transofrmer		High-Q FE Transformer	High-Q FE Co-Design	None	N-path filter	BAW Filter
Front-End Passive Gain	12.6 dB	12.6 dB	30.6 dB	27 dB	23 dB	25 dB	N/A	N/A	9.4 dB	0 dB
Sensitivity	-65 dBm	-68 dBm	-80.5 dBm	-76 dBm	-71 dBm	-69 dBm	-61.5 dBm	-56.5 dBm	-97 dBm	-72 dBm
Sensitivity with interference	-65 dBm	-68 dBm	N/A	-75 dBm	N/A	N/A	-58.5 dBm [1]	N/A	-94 dBm	N/A
Figure of Merit	114 dB	113 dB	132 dB	127 dB	122 dB	122 dB	95 dB	92 dB	107 dB	84 dB
Die Area	3.9 mm^2	3.9 mm^2	6 mm^2	1.95 mm^2		6 mm^2	1.1 mm^2 *	2.25 mm^2 *	0.0576 mm^2 *	0.1 mm^2 *

state-of-the-art.

3.7 Summary and Conclusion

This chapter introduced design techniques to overcome the challenges of robustness to temperature and interference as well as multi-GHz operation in ULP WuRx's. Overcoming these challenges enables reliability in uncontrolled IoT environments and the leveraging of the communication infrastructure at multi-GHz frequency bands. The chapter demonstrated that despite using sub-threshold circuits that are sensitive to variation, the ED-first architecture is a feasible candidate for designing robust sub-100 nW WuRx's at multi-GHz frequencies. The highlights of the chapter is are follows.

1) Introduced a sub-nW comparator based on the StrongArm Latch topology with a thermometer-coded DAC that enables granular sub-mV control of the comparator decision threshold as well as monotonicity across its tuning bits, which is required for the proper functionality of the PID controller and detection of mV-level signals.

2) Introduced an autonomous nW-power PID controller for adjusting the decision threshold of the comparator across temperature. The PID controller can also compensate for blockers by raising the comparator decision threshold above the interference level.

3) Introduced an area-efficient, gate-leakage-based current DAC for implementing a tunable crystal-less relaxation oscillator (RXO) that is calibrated with a gate-leakage-based digital temperature sensor.

4) Introduced on-chip electromagnetic field confinement at the RF input to prevent losses in the p-doped chip substrate while operating in the high-impedance RF environment of ED to increase the MDS of the WuRx by several decibels.

5) Presented a proof-of-concept sub-100 nW ED-first CMOS WuRx chip that operates at the 9.6 GHz X band and is robust to temperature variation in the 0 to 70°C commercial range. The WuRx consumes 27.6 nW of power at 20°C and achieves a sensitivity of -65 dBm with $<$2 dB degradation across the temperature range.

6) Presented a proof-of-concept sub-100 nW ED-first CMOS WuRx at 2.2 GHz S band RF frequency. In the low-power mode, the WuRx consumes 11.3 nW of power and achieves an RF sensitivity of -65 dBm. In the high-sensitivity mode, the WuRx consumes 28.2 nW of power and achieves a sensitivity of -68 dBm. The WuRx architecture is robust to continuous-wave, in-band interferers, with up to -20 dB carrier-to-intereferer ratio.

3.8 List of Relevant Publications

[PB1] P. Bassirian, et al., “Design of an S-Band Nanowatt-Level Wakeup Receiver with Envelope Detector-First Architecture,” *in IEEE Transactions on Microwave Theory and Techniques*, 2020.

[PB2] P. Bassirian, et al., “A Temperature-Robust 27.6nW -65dBm Wakeup Receiver at 9.6GHz X Band,” *2020 IEEE International Solid–State Circuits Conference–(ISSCC)*, San Francisco, CA, 2020.

[PB11] P. Bassirian, et al., “A 27.6 nW Temperature- and Interference-Robust Wakeup Receiver at 9.6 GHz X Band,” *to be submitted to IEEE Journal of Solid-State Circuits*, 2020.

Chapter 4

Techniques for Sub-GHz WuRx Design Using Co-Designed MEMS and CMOS Technologies

4.1 Introduction

Designing a WuRx front-end for achieving low MDS, or equivalently, high SNR is highly dependent on the proper co-design of the matching network and ED. The loading effect of the ED impedance on the matching network depends on the frequency response of the matching network. This dependence necessitates different co-design methods for discrete-element matching networks and MEMS-based matching networks. This chapter presents the co-design of MEMS-based front-ends that can be used in ULP WuRx's.

The most common matching network topologies are shown in Figure 4.1(a)–(c). The matching networks show their best performance at sub-GHz frequencies because they rely on the high quality-factor of the discrete air-core inductors. Despite the high voltage gain of around 30 dB that can be achieved through these matching networks, they may not be desirable design choices under certain circumstances.

The reliance on the high Q values of the discrete air-core inductors leads to several limitations for ULP WuRx's. First, the physical sizes of these inductors do not allow for the chip-scale packaging of different components; therefore, they limit the minimum achievable physical size of any system they are placed in. Second, ULP WuRx's are susceptible to out-of-band interference, and it is challenging to implement interference rejection hardware after the interference passes through the input port due to the stringent power budget [107]. Therefore, achieving narrow input RF bandwidths or, equivalently, high-Q matching is extremely valuable. In addition, discrete inductors are susceptible to EMI and can pick up stray EMI from various sources, such as nearby radio, Wi-Fi, or cellular transmitters [136]. This issue can complicate the packaging of the entire system, as

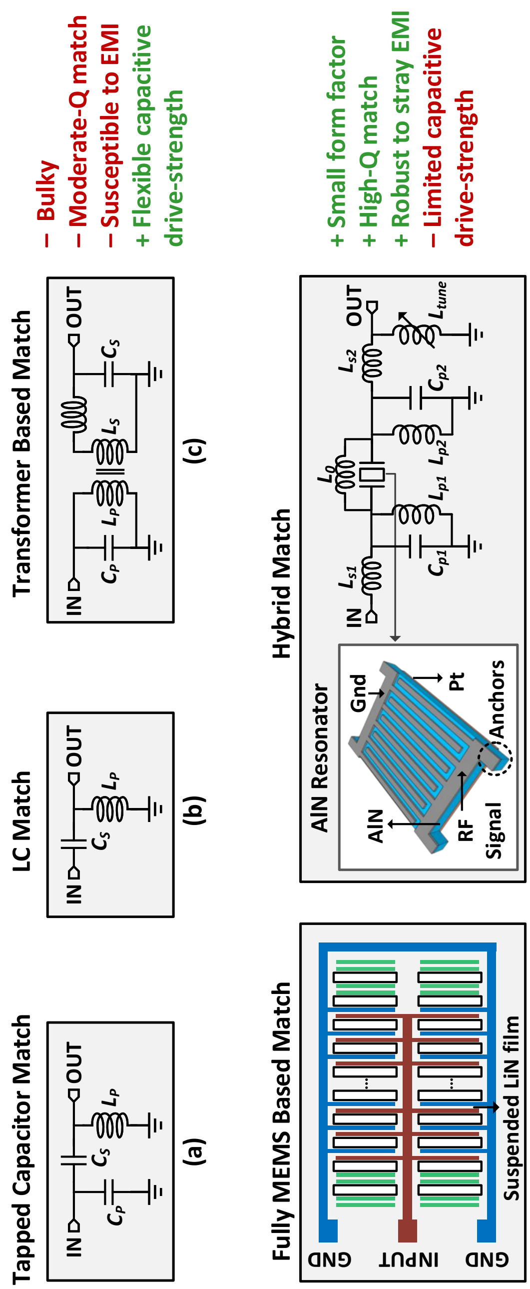


Figure 4.1: Most commonly used MN architectures in sub-GHz nanowatt-level WuRx's for transforming a low 50-Ω source impedance to the high input impedance of EDs (usually on the order of tens of kilohms) (top). MEMS resonators (bottom) can be tightly integrated with a CMOS chip on a planar chip-scale package. They can also improve the robustness of WuRx's to out-of-band interference and stray EMI. (a) Tapped capacitor match. (b) LC match. (c) Transformer-based match. (d) Fully MEMS-based match. (e) Hybrid match.

it necessitates further RF shielding. Alternatively, MEMS resonators, which are widely used as RF filters [94], offer a promising solution to be used as matching networks [95]. MEMS resonators have a small form factor and can be tightly packaged with CMOS integrated circuits. Furthermore, compared to discrete-element matching networks, they can achieve considerably higher Q matches (several hundred versus <50).

This chapter presents a design-oriented theory and analysis for MEMS-based matching networks and co-design techniques for achieving the lowest minimum detectable signal at the MEMS-based WuRx front-ends. It also presents two proof-of-concept CMOS chips fabricated in a 130-nm RF-CMOS process and co-designed with their corresponding matching networks. The first system uses a fully MEMS-based matching network operating at 88.8 MHz FM band that consists of a large 56-element array of parallel lithium niobate (LiN) resonators (Figure 4.1(d)). This system occupies more than two orders of magnitude smaller physical volume and can achieve up to one order of magnitude narrower RF bandwidths than the discrete-element matching networks. The second system is a hybrid matching network that consists of an aluminum nitride (AlN) laterally-vibrating resonator and eight peripheral discrete capacitors and inductors surrounding the MEMS device (Figure 4.1(e)). The system operates at 457 MHz, and its goal is to take advantage of the high-Q MEMS resonance, which results in a narrow bandwidth and therefore a high out-of-band interference rejection.

4.2 Basic Concepts of MEMS Resonators

This section presents an overview of the structure and basic concepts of the MEMS resonators used in this research. More detailed explanations, characterizations, and measurements of the MEMS resonators can be found in [137] and [138]. Figures 4.1(d), (e) show the structures of AlN and LiN resonators. The AlN resonator consists of a suspended AlN thin film sandwiched between the top interdigitated transducer electrodes (IDTs) and a bottom electrode. The IDTs are designed with a thickness of 150 nm, a pitch width (distance between the centers of two adjacent IDTs) of 10 μm, a line width of 5 μm, and an overlapping length of 190 μm. The electrical connections of the IDTs alternate between the ground and RF signal. The bottom electrode is a rectangular metal film with a thickness of 100 nm, which is floating electrically. The AlN thin film is 1 μm in thickness and has the same size as the bottom electrode. The resonant frequency f_s of the resonator is primarily determined by the pitch of IDTs and can be written as [139]

$$f_s = \frac{v}{\lambda} = \frac{v}{2W_p}, \tag{4.1}$$

where v is the phase velocity of the acoustic wave in AlN, λ is the wavelength, and W_p is the pitch of the IDTs.

The fabrication chart of the AlN resonator is illustrated in Figure 4.2. The fabrication process involves the following steps: 1) deposition of Platinum with a thickness of 100 nm for the bottom

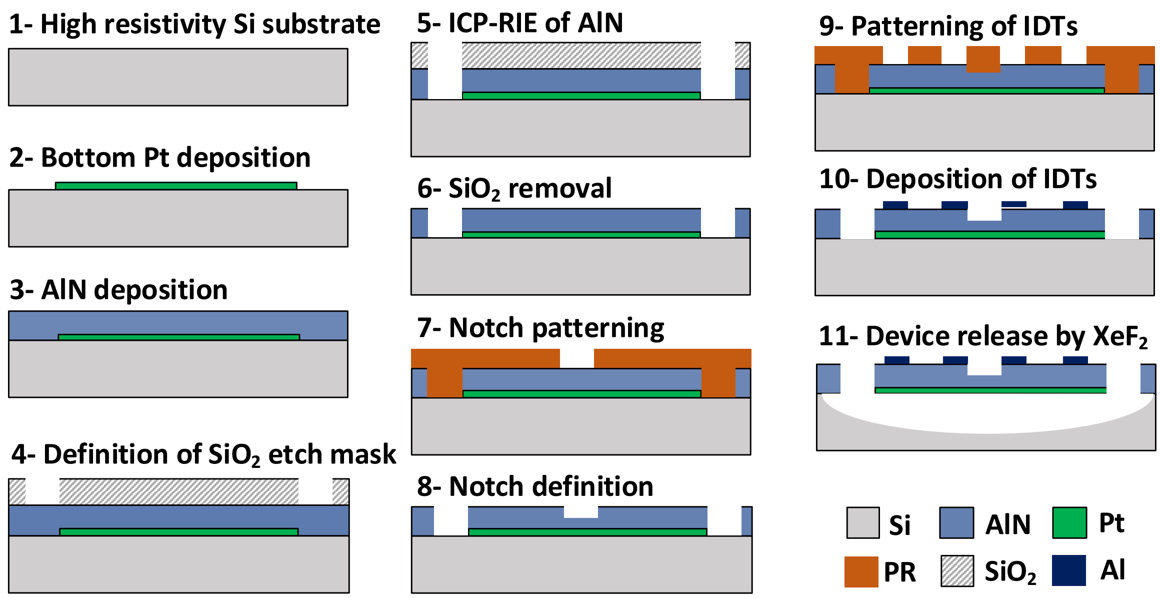


Figure 4.2: Fabrication chart showing the micro-machining steps used in the fabrication of the Aluminum Nitride (AlN) device. The device consists of an AlN thin film layer sandwiched between seven pairs of 150-nm interdigitated Aluminum electrodes and a 100-nm Platinum electrode [137].

electrode on a high-resistivity Silicon wafer; 2) reactive sputtering of AlN with a thickness of 1 μm at a temperature below 350 °C; 3) patterning of the hard etch SiO_2 mask with CHF_3-based reactive ion etching (RIE); 4) etching of the AlN via a Cl_2-based RIE with inductively coupled plasma (ICP); 5) removal of the SiO_2 via a CHF_3-based RIE process; 6) placing a notch in the center of the resonator via a SPR220 photoresist mask and a Cl_2-based RIE-ICP. This notch suppresses the spurious modes of the resonator; 7) sputtering of the top interdigitated Al electrodes with a thickness of 150 nm; 8) release of the resonator with XeF_2.

In the electrical domain, MEMS resonators can be modeled as a one-port device, as shown in Figure 4.3(a). This model consists of a motional branch in parallel with a shunt physical capacitor. In the motional branch, the parameters R_m, C_m, and L_m represent the mechanical resonance in the electrical domain and correspond to the damping, stiffness, and mass of the resonator, respectively. The capacitance C_0 corresponds to the physical capacitance between the electrodes. This lumped-element equivalent circuit model is known as the Butterworth-Van Dyke (BVD) model, which is applicable to many types of piezoelectric MEMS resonators [140]. The values of the elements in the motional branch are not independent of each other, and they are functions of the electromechanical coupling k_t^2, quality-factor Q_m, and mechanical resonant frequency of the device f_s as shown below

$$R_m = \frac{\pi^2}{8} \cdot \frac{1}{2\pi f_s C_0} \cdot \frac{1}{k_t^2 Q_m} \tag{4.2}$$

$$L_m = \frac{\pi^2}{8} \cdot \frac{1}{(2\pi f_s)^2 C_0} \cdot \frac{1}{k_t^2} \tag{4.3}$$

$$C_m = \frac{8}{\pi^2} \cdot C_0 k_t^2. \tag{4.4}$$

The parameter $k_t^2 \times Q_m$ is known as the figure of merit (FoM) of the resonator. The corresponding values of the BVD model parameters for the AlN and LiN resonators used in this proposal are given in Table 4.1.

Table 4.1: Butterworth Van Dyke (BVD) model parameters for the MEMS resonators.

Device Type	**Aluminum Nitride**	**Lithium Niobate**
$R_m(\Omega)$	38.8	18
$C_m(fF)$	8.24	112
$L_m(\mu H)$	14.7	30.99
$C_0(fF)$	532	807

Figure 4.3(b) shows the behavior of the impedance of the AlN device (Z_m) across frequency. This plot shows that Z_m has one series (f_s) and one parallel (f_p) resonance. These resonances occur at

$$f_s = \frac{1}{2\pi\sqrt{L_m C_m}} \tag{4.5}$$

$$f_p = \frac{1}{2\pi\sqrt{L_m(\frac{1}{C_m} + \frac{1}{C_0})^{-1}}} \approx f_s(1 + \frac{C_m}{2C_0}). \tag{4.6}$$

In the narrow range between f_s and f_p, C_m does not completely resonate out L_m in the motional branch; therefore, the MEMS resonator effectively behaves like an inductor. Unlike a wire-wound inductor, its inductance and Q_{eff} are strong functions of frequency. The maximum Q_{eff} of this inductor is an important factor for the match and is directly proportional to the resonator FoM, as seen below.

$$Q_{eff-max} = \frac{2}{\pi^2} \cdot FoM = \frac{2}{\pi^2} \cdot k_t^2 Q_m. \tag{4.7}$$

The disadvantage of the standalone AlN resonator is that it has limited capacitive drive strength and requires additional lumped elements to achieve an acceptable performance. To increase the resonator's capacitive drive strength for the loads with picofarads of capacitance, an array of 56

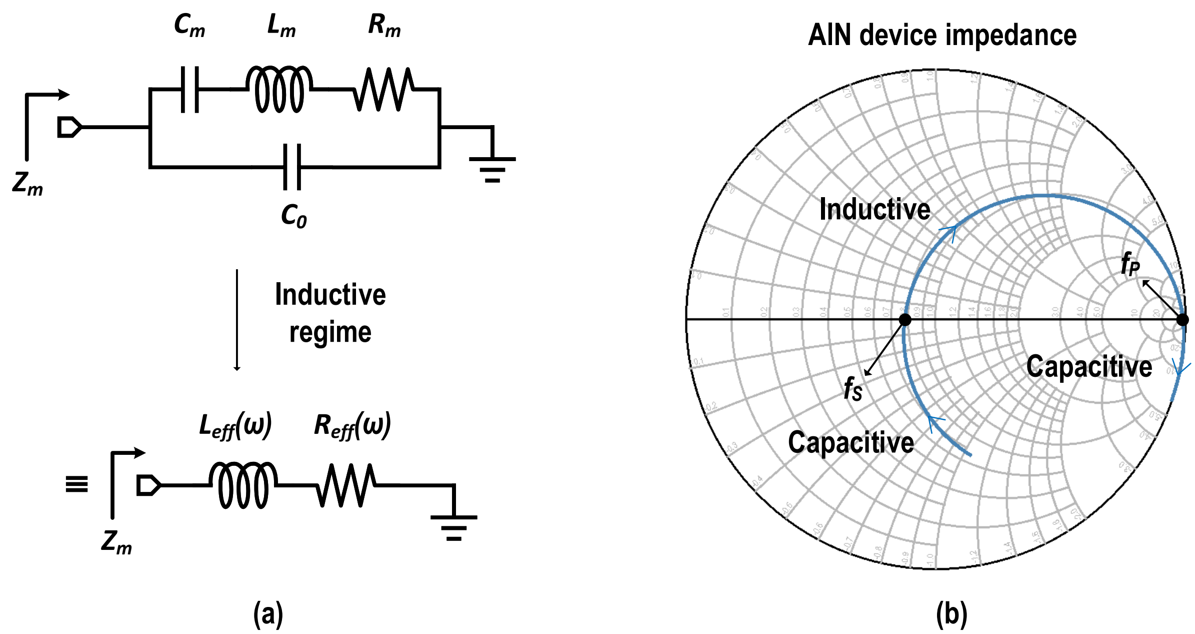


Figure 4.3: (a) BVD model of a MEMS resonator, and its equivalent circuit model in its inductive regime. (b) Simulated behavior of the AlN resonator impedance across frequency using the corresponding BVD model values from Table 4.1. This plot shows that over a short frequency range between f_s and f_p, the inductance of the MEMS device covers a wide range of values, which can be used to implement an LC MN with a capacitive load.

identical LiN resonators is used that has the fabrication chart, layout, simulated performance, and structural dimensions shown in Fig. 4.4 and Table 4.2. The designed resonator array is fabricated with the two-mask process introduced in [141]. Each resonator has two 80 nm patterned interdigitated gold electrodes located on top of a 700 nm LiN thin film. The fundamental shear horizontal (SH0) mode at -10° to the +Y axis, and an X-cut LiN is chosen for its high k_t^2 and Q_m [142].

4.3 Envelope Detector Co-Design with MEMS Resonators

This section explains the co-design and integration of MEMS resonators with the Dickson EDs in WuRx front-ends. A MEMS-based match operates primarily based on the passive voltage boost that can be achieved across the reactive elements in a series LC resonant tank. Figure 4.5(a) shows the schematic of a series LC tank with a finite-Q capacitor and inductor. At the resonant frequency, the current flowing through the branch is at its maximum, and the voltages across the reactive elements can be greater than V_i. Therefore, this circuit can achieve a voltage gain from the input node V_i to the internal node V_X. This gain can be quantified in terms of the quality-factors of the

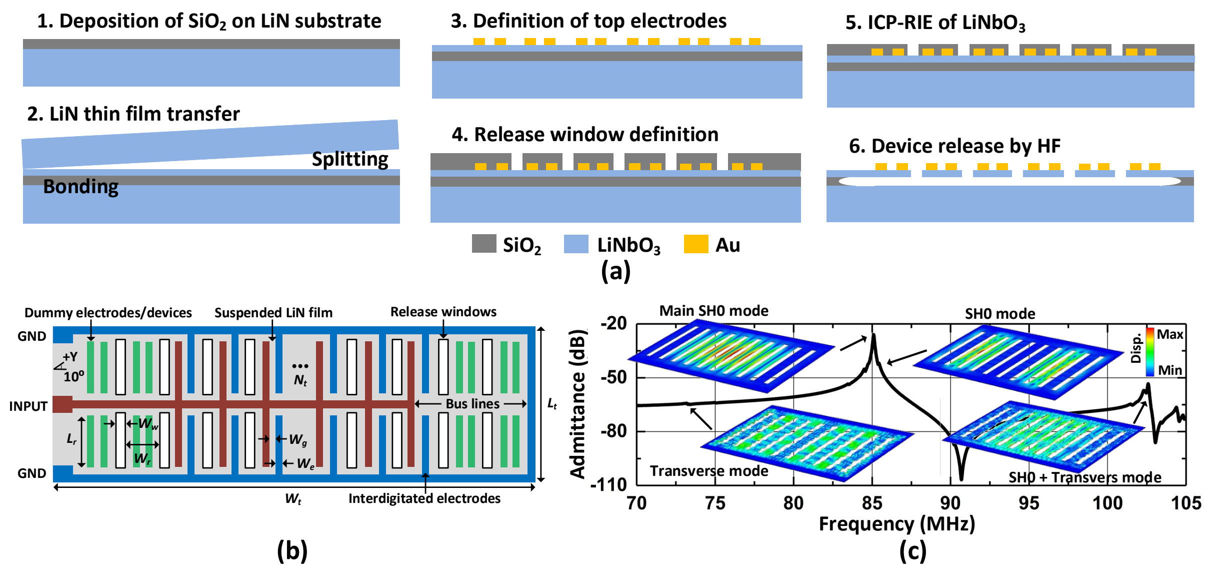


Figure 4.4: (a) Fabrication chart of the LiN resonator consisting of 56 pairs of 80-nm interdigitated gold electrodes on a 700-nm LiN thin film. (b) Physical structure of the Lithium Niobate (LiN) resonator array having the key dimensions shown in Table 4.2. (c) Simulated admittance response of the resonator array. The displacement mode shape of the main SH0 mode on the resonator is presented along with the spurious modes [138].

two reactive elements as follows. At $\omega_0 = \frac{1}{\sqrt{LC}}$

$$\frac{V_X}{V_i} = \frac{Q_L}{Q_L + Q_C} - j\frac{Q_L Q_C}{Q_L + Q_C}, \tag{4.8}$$

where $Q_L = \frac{\omega_0 L}{R_L}$ and $Q_C = \frac{1}{\omega_0 C R_C}$ are the quality-factors of the inductor and the capacitor, respectively. Therefore

$$|\frac{V_X}{V_i}| = Q_L \times \frac{\sqrt{1 + \frac{1}{Q_C^2}}}{1 + \frac{Q_L}{Q_C}}. \tag{4.9}$$

Equation (4.9) indicates that for a given value of Q_L, the asymptotic value of the voltage gain as $Q_C \to \infty$ is equal to $|\frac{V_X}{V_i}|_{max} = Q_L$. This value is the limit on the maximum achievable voltage boost in this circuit. Figure 4.5(b) shows the schematic of this circuit being driven by a power source. The transducer voltage gain G_T in this circuit can be written as

Table 4.2: Dimensions of the Lithium Niobate resonator's physical structure.

Parameter	**Symbol**	**Value**
Resonator Length	L_r	130 μm
Resonator Width	W_r	19 μm
Electrode Width	W_e	5 μm
Gap Width	W_g	5 μm
Window Width	W_w	10 μm
Number of Devices	N_t	56
Number of Dummy Devices	N_d	8
Total Resonator Length	L_t	0.5 mm
Total Resonator Width	W_t	1.1 mm

$$G_T = 2|\frac{V_X}{V_i}| \times |\frac{Z_m + Z_{in}}{R_s + Z_m + Z_{in}}|. \tag{4.10}$$

Assuming that the second term in (4.10) is approximately equal to 1, the maximum value of G_T is about 2 times or 6 dB greater than $|V_X/V_i|$.

Figure 4.5 shows the plots for the effective inductance of the LiN device. Figure 4.5(c) shows that the Q_{eff} of this inductor reaches its maximum value of 31 around 88.3 MHz. According to Equation (4.9), the maximum theoretical voltage boost for this device is equal to $31 \times 2 = 35.8\ dB$. The value of inductance at this frequency is approximately equal to 3.9 μH. Therefore, the highest voltage boost is available for the capacitive loads that can resonate out this inductance at the specified frequency, defining the capacitive drive strength of the resonator. The resonator drive strength corresponds to the range of load capacitances that can resonate with the inductance values in the vicinity of the maximum Q_{eff} frequency and highlights the advantage of arrayed resonators. In a spurious free array with identical elements, placing the resonators in parallel decreases the inductance corresponding to the maximum Q point without affecting the device's FoM. Therefore, larger capacitive loads can resonate out the smaller inductance at the maximum Q point, which means that the capacitive drive strength of the device can be increased.

The contour plots in Figure 4.6 provide the design intuition for the LiN match [143] from the schematic shown in Fig. 4.5(b). Within these contours, different characteristics of the match are found in the Z_{in} load plane. Note that the capacitive load Z_{in} in these plots consists of a parallel combination of an R_{in} resistor and a C_{in} capacitor, which resembles the input impedance behavior of an ED. A wide range of loads achieve their maximum voltage boosts in the frequency range between 87 MHz to 89 MHz in this simulation because the effective inductance of the LiN device achieves its highest Q in the middle of that frequency range.

The constant gain contours are shown in Figure 4.6(a). As predicted by Equation (4.9), the loads located in the low-Q regions, for example, towards the bottom left of the plot (Figure 4.6(b)), do

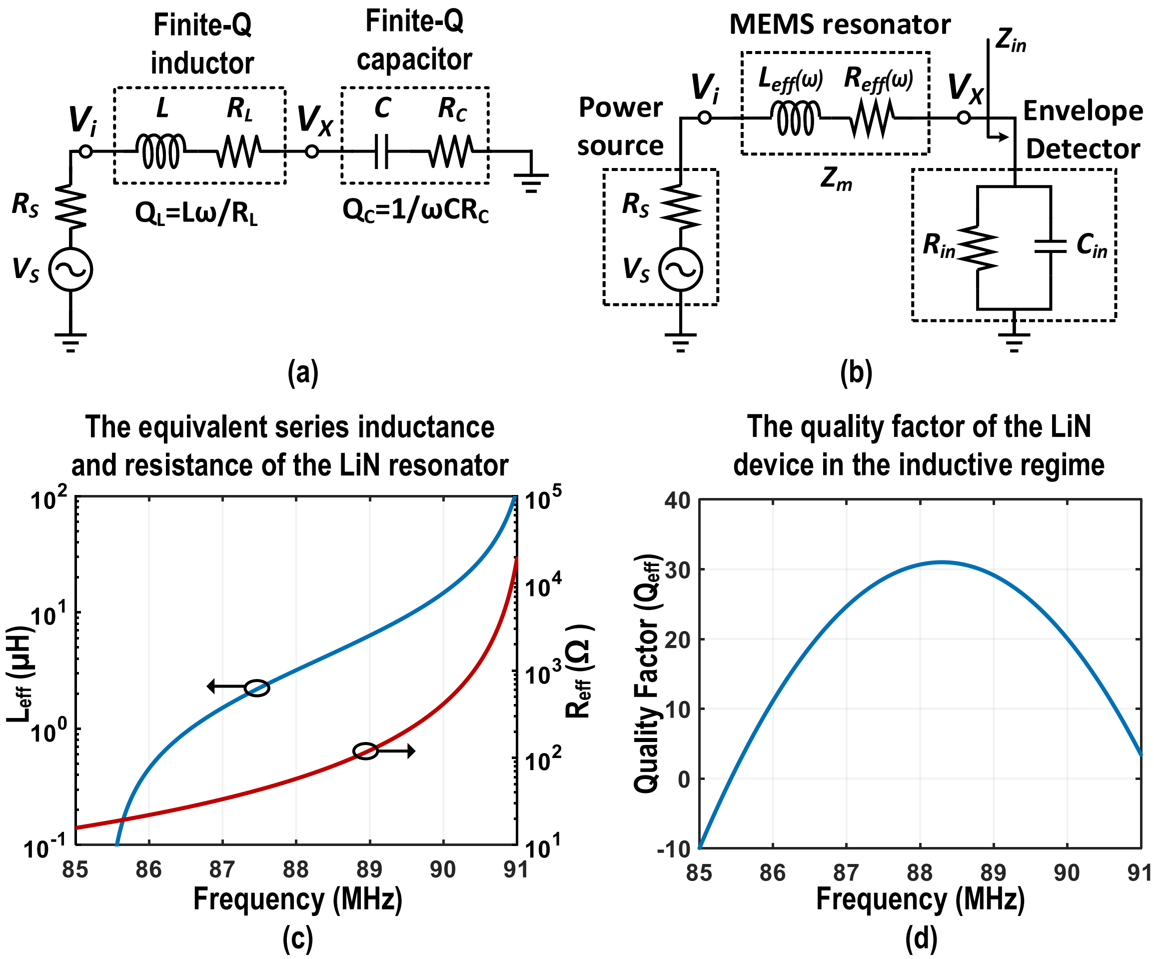


Figure 4.5: (a) A series LC resonant tank that can provide voltage gain from its input V_i to V_X. (b) The circuit schematic of a MEMS resonator in its inductive regime that can provide voltage gain at the input port of the capacitive ED. (c) Simulated effective series inductance, resistance, and (d) quality-factor of the LiN device in the frequency range between its series and parallel resonances. The peak of the quality-factor curve corresponds to the inductance and therefore the capacitive load that can achieve the highest passive voltage boost.

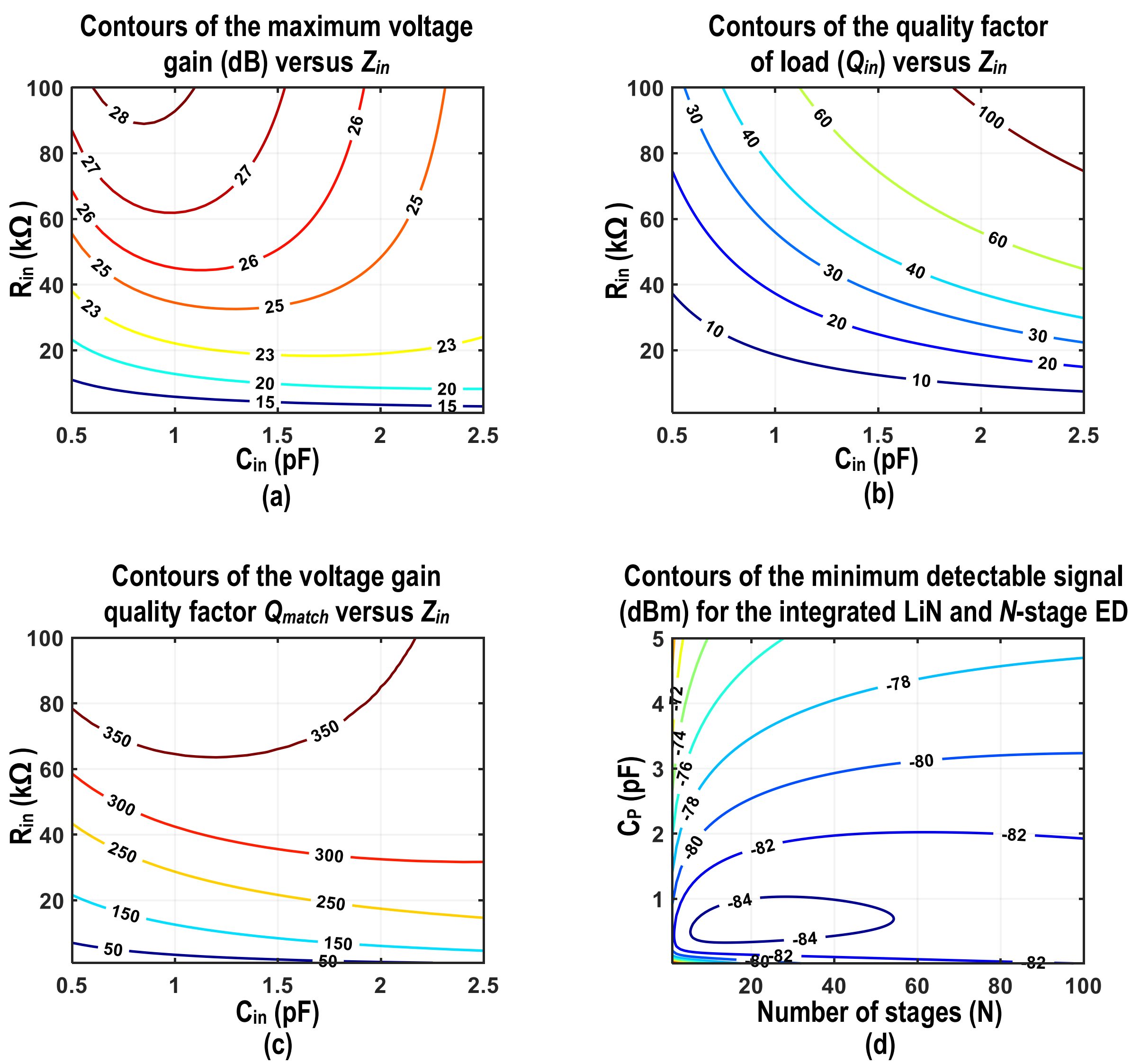


Figure 4.6: Simulated contour plots of various characteristics of the LiN resonator-based match in the load plane (Z_{in}). The x- and y-axes represent the parallel resistive (R_{in}) and capacitive (C_{in}) portions of the load impedance that are connected to the resonator for the impedance transformation. The contour plots can provide design intuitions about the characteristics of the match, including the (a) maximum transducer voltage gain, (b) quality-factor of the load (Q_{in}), (c) quality-factor of the loaded match that corresponds to the sharpness of the match, and (d) minimum detectable signal for the integrated LiN resonator and an N-stage ED using low-voltage-threshold RF (LVTRF) devices with a noise equivalent bandwidth of 1 kHz.

not achieve high voltage gains. Moreover, on a constant C_{in} line, loads with higher R_{in} have higher Q's and can achieve higher voltage gains. However, on a constant R_{in} line, a higher Q does not necessarily result in a higher voltage gain. For example, the loads located in the top-right corner of the plot have higher Q's (Figure 4.6(b)), but, due to the limited capacitive drive-strength of the MEMS device, they do not achieve higher voltage gains compared to the lower-Q loads in the top-left corner.

Figure 4.6(c) plots the quality-factor contours of the loaded MMN in the Z_{in} plane. This plot highlights one of the main advantages of the MEMS-based match. The 3 dB bandwidth of G_T in a MMN can be on the order of a few hundred kilohertz, which is an order of magnitude smaller than what can be obtained in discrete-element MNs. The main reason for this narrow bandwidth is the frequency dependence of the inductance presented by the MEMS devices, which is shown in Figure 4.5(c).

The LiN device is integrated with the CMOS chip, which includes a co-designed ED, to minimize MDS at the input of the ED. This ED utilizes low voltage-threshold RF (LVTRF) devices, which have higher impedances compared to ZVTDG devices and can present larger shunt resistances at the cost of slower charge time. Fig. 4.6(d) shows the MDS contours of the integrated LiN resonator and ED. The x-axis on this plot represents the number of stages (N) of the ED that constitute the variable contribution to the input impedance. On the other hand, the y-axis represents the constant shunt parasitic capacitance (C_P), which is mainly due to the input pad and electrostatic discharge (ESD) protection diodes at the input. These contours show the combined trade-off between Z_{in} and G_T, ED OCVS and N, and ED output noise and N. In order to achieve these contours, the noise equivalent bandwidth (NEB) of the FE is set to 1 kHz, which is primarily determined by the subsequent baseband amplifier stage. For each point on the N-C_P plane, the impedance of the LVTRF diodes and NEB are used to calculate the output noise voltage. Next, the overall input impedance, including the C_P, and the gain versus Z_{in} plots in Fig. 4.6(a) are used to find the corresponding voltage gain. This information is then combined with the OCVS of the ED to calculate the FE MDS, which is the input power level that results in 0 dB of SNR at the output of the ED.

4.4 Proof-of-Concept MEMS-Based FM WuRx Front-End

This section presents the design of a proof-of-concept front-end that uses the LiN MEMS resonator for the impedance transformation to the input of a Dickson ED. The front-end uses a fully MEMS-based matching network that operates at 88.8 MHz FM band. Measurements of the integrated WuRx front-end indicate that its loaded voltage gain achieves a bandwidth of 0.78 MHz with a quality-factor of 114. Compared to discrete-element matching networks, this front-end decreases the system size by more than two orders of magnitude and reduces the input RF bandwidth by up to one order of magnitude.

The post parasitic-extraction (PEX) simulation suggests that the combination of the input pad and

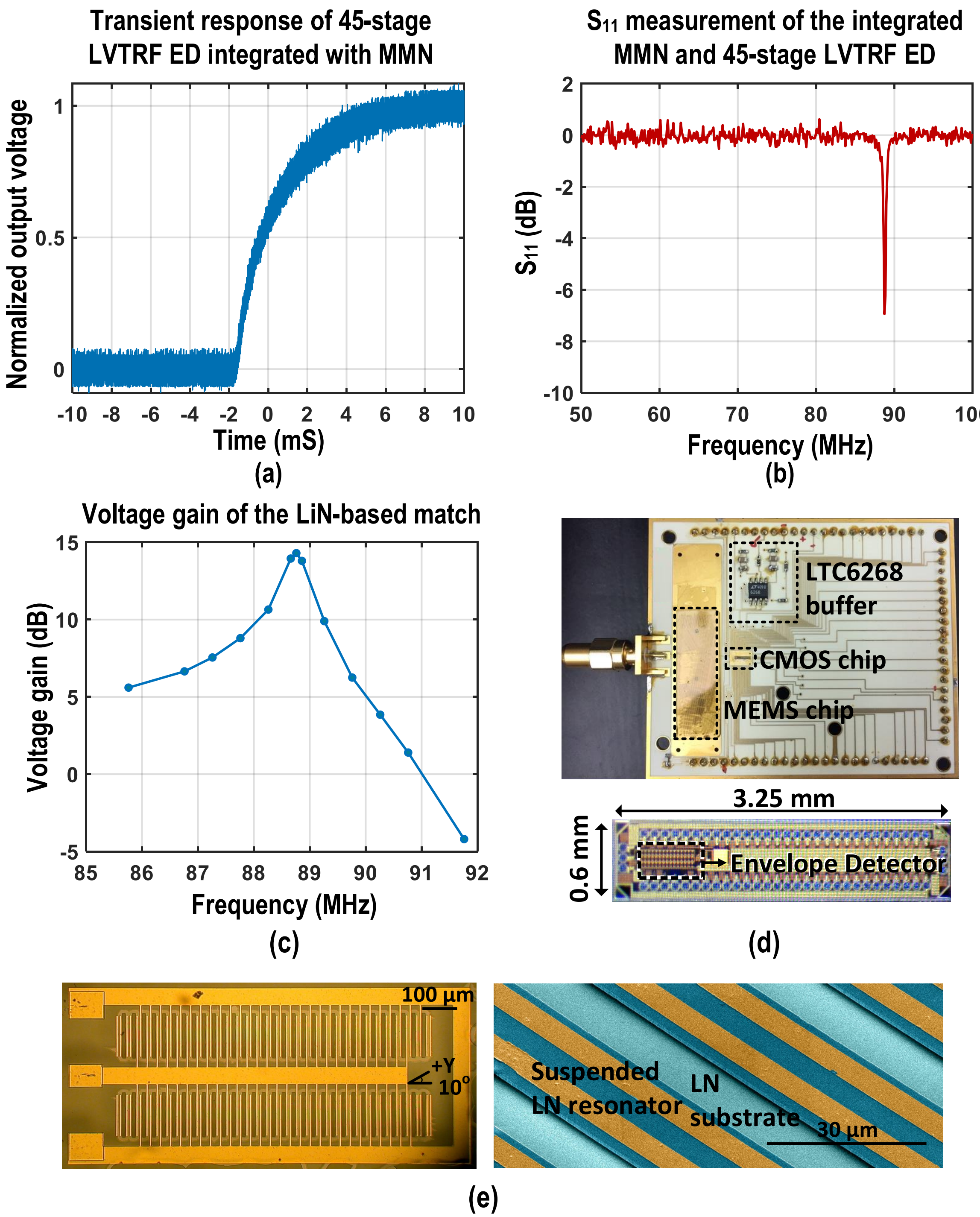


Figure 4.7: (a) Measured transient response of the 45-stage LVTRF ED integrated with the LiN resonator achieving a charge time of 5 ms. (b) Measured S_{11} of the integrated LiN-based front-end. (c) Measured voltage gain of the integrated LiN resonator, with a gain of 14.3 dB at 88.8 MHz and a 3-dB bandwidth of 0.78 MHz. (d) PCB and CMOS die photos. (e) Optical image of the LiN resonator, and its SEM image.

ESD diodes contribute to about 0.4 pF of C_P. To minimize the MDS and increase the output signal level while maintaining the charge time below 5 ms, the number of stages is set to 45 with 60 fF coupling capacitors. The total input impedance of the second ED is equal to 50 kΩ||0.6 pF at 88 MHz. The combined transient response of the integrated LiN resonator and 45-stage LVTRF ED is shown in Figure 4.7(a). This measurement represents the normalized output voltage of the ED when an RF signal is turned on at the input to the matching network. The measured results show that this front-end achieves a charge time of 5 ms.

Figure 4.7(b) presents measured S_{11} response of this front-end, which shows a narrow-band match at 88.8 MHz. The measured voltage gain of the integrated LiN array with the first CMOS chip is shown in Figure 4.7(c). In the setup, the output of the LiN device and the input of the ED are both connected to a PCB trace with a bond wire. The output voltage of the ED is then measured through an LTC6268 buffer op-amp. This front-end can achieve a voltage gain of 14.3 dB at 88.8 MHz with a 3-dB bandwidth of 0.78 MHz, which corresponds to a loaded Q of 114. The reasons for the discrepancy between the expected voltage gain from this integration and the simulated values are as follows. First, the extra capacitance of the PCB trace can shift the voltage gain significantly from its expected value. Second, the integrated LiN device has additional spurious modes that reduce its FoM and degrade its inductive behavior. The PCB and die photo are shown in Figure 4.7(d), and the optical and scanning electron microscope (SEM) images of the LiN resonator are shown in Figure 4.7(e).

4.5 Proof-of-Concept MEMS-Based UHF WuRx Front-End

This section presents the co-design of the AlN MEMS resonator front-end with the CMOS ED. The front-end uses a hybrid matching network that operates in the 457 MHz UHF band. It consists of the AlN laterally-vibrating resonator as well as eight discrete inductors and capacitors surrounding the MEMS device. Measurements of the integrated WuRx front-end with the hybrid matching network indicate that it achieves a sensitivity of -54 dBm and an average power consumption of 7 nW without a digital correlator.

4.5.1 Design of the Baseband Circuits

The schematics of the comparator and clock are shown in Figure 4.8. The ULP comparator [111] (Figure 4.8(a)) consists of a clocked, ground-referenced preamplifier stage, which is connected to a latch on the bottom that provides regenerative feedback, as well as precharge switches that are connected to the CLK signal [129]. The currents through the differential pair and the latch can be controlled through separate binary-weighted DACs. The width of the transistor on the right arm of the preamplifier stage is tunable to control the input offset introduced by the preamplifier and latch stages. During the reset phase when CLK=1, the transistors M_1 and M_2 pre-charge the nodes V_X and V_Y, respectively, to 0. During the comparison phase when CLK=0, the latch transistors are

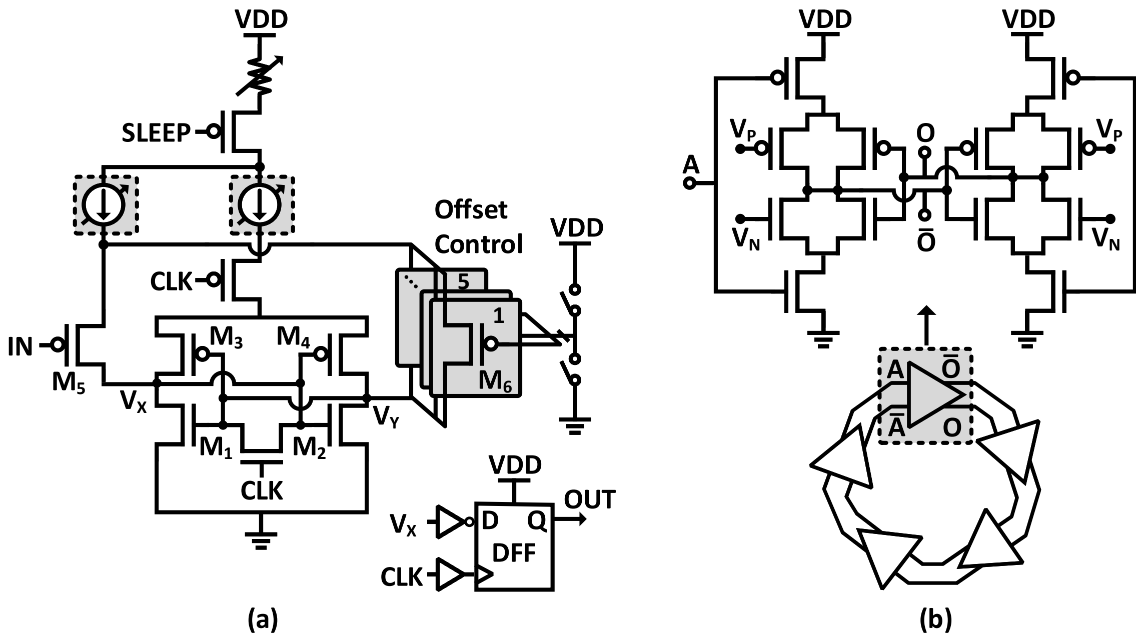


Figure 4.8: Schematic of (a) the digitally-tunable, ultra-low-power comparator consisting of a ground-referenced preamplifier stage on top and a latch on the bottom, followed by a D flip-flop and (b) the 5-stage, leakage-based constant energy-per-cycle ring oscillator (CERO).

initially off, and M_5 and M_6 start charging up the capacitors at the V_X and V_Y nodes, respectively. This process continues until the gate-source voltages of the latch transistors exceed their threshold voltages and they turn on. At this point, the positive feedback loop of the cross-coupled NMOS and PMOS pairs pulls the node with the higher voltage up to 1 and pulls the other node down to 0. The V_X node is then given to an inverter buffer and is latched by a D flip-flop at the positive edge of the CLK signal. The power consumption of the comparator consists of a constant leakage power and a dynamic switching power. In each clock cycle, when the regenerative latch of the comparator trips, there is a short spike in the comparator supply current. Simulation results indicate that the peak value of current at the comparator power supply (without a bypass capacitor) is around 2.2 μA for duration of 6 μs.

The ULP clock is a five-stage leakage-based constant-energy-per-cycle ring oscillator (CERO) [144], which is shown in Figure 4.8(b). The power consumption and frequency of the clock can be set by controlling two voltages, namely V_P and V_N, and it covers a wide range. These voltages can be generated by using a gigaohm resistive divider that consumes less than 1 nW of dc power. In a conventional current-starved ring oscillator, the dynamic power consumption consists of switching loss of delay cells due to charging and discharging of the parasitics capacitors as well as the conduction loss due to the short-circuit current in the output buffer when both the NMOS and PMOS switches momentarily turn on at once. At low switching speeds on the order of several kilohertz, the conduction loss of the output buffer limits the minimum achievable power consumption of the clock. On the other hand, in a CERO, the additional back-to-back inverter pair inside the delay cell can reduce the short-circuit current by accelerating the clock's transition rate between its high and low states, thus enabling greater power scalability across frequency, especially at lower frequencies. The clock frequency can range from 250 Hz to 110 kHz, corresponding to a power consumption ranging from 0.1 nW to 100 nW, which linearly scales with frequency.

4.5.2 Integrated Front-End Measurements

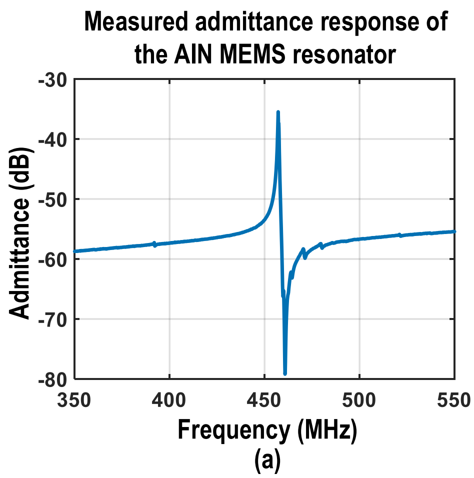
Figure 4.9(a), (b) show the admittance amplitude response of the AlN resonator and the extracted parameters of its BVD model, respectively. Figure 4.9(c), (d) show the Q_{eff} plot of the effective inductance and the maximum gain contours of the AlN resonator, respectively. These plots indicate that due to the low FoM and capacitive drive-strength of this device, the voltage gain for picofarad-level loads is insufficient. Therefore, this device is utilized in a hybrid match that combines it with discrete elements in order to increase its capacitive drive strength and take advantage of its potential to implement a high-Q match.

To increase the capacitive drive strength of the AlN resonator, this device is used in a three-stage match, as shown in Figure 4.9(e). The hybrid match uses three series stages to transform a low impedance of 50 Ω to the input impedance of the ED on the CMOS chip, which is equal to 5.2 kΩ||1.67 pF at the center frequency of 457 MHz. This CMOS chip includes a 16-stage ED that uses ZVTDG devices, which have relatively low impedance and can provide fast charge times. The first stage of the match uses three lumped elements to convert the 50 Ω port impedance to an intermediate impedance of 1.7 kΩ. The second stage consists of an AlN resonator and a parallel inductor L_0. The AlN resonator sets the center frequency and the bandwidth of the match, and the L_0 is used to decouple the anti-resonance of the resonator and generate two symmetric transmission zeros for the transformer. The last stage uses a three-lumped-element network that converts the intermediate impedance to the impedance at the input of the ED. The L_t is a tunable inductor that is used to tune out the input capacitance of the ED that loads the output of the transformer. The values for these discrete lumped elements are given in Table 4.3.

Table 4.3: Values of the peripheral discrete elements of the AlN resonator's three-stage hybrid matching network

$C_{p1}(pF)$	3	$C_{p2}(pF)$	3
$L_{s1}(nH)$	49.2	$L_{s2}(nH)$	49.2
$L_{p1}(nH)$	37.2	$L_{p2}(nH)$	14.5
$L_0(nH)$	214	$L_t(nH)$	≈90

The transient response of the integrated AlN resonator and 16-stage ZVTDG ED is shown in Figure 4.10(a). This measurement represents the normalized output voltage of the ED when an RF signal is turned on at the input of the HMN. The measured results show that this FE achieves a



Extracted BVD parameters of the AlN resonator

R_m	C_m	L_m
38.8 Ω	8.24 fF	14.7 μH
C_0	f_s	f_p
532 fF	457.1 MHz	460.5 MHz
Q	FOM	k_t^2
1150	21	1.8%

(b)

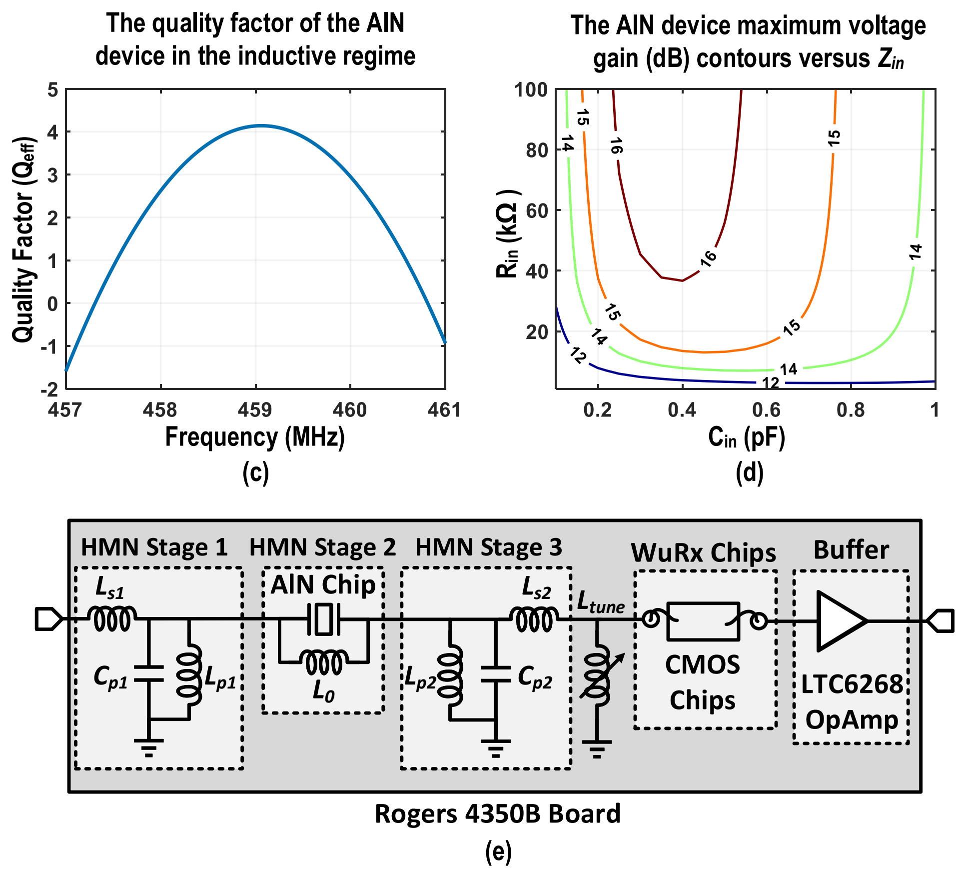


Figure 4.9: (a) Measured admittance amplitude response of the fabricated AlN resonator. (b) Extracted BVD parameters of the AIN resonator are shown in the inset table. (c) Simulated quality-factor plot of the AlN device in the frequency range between its series and parallel resonance. (d) Simulated constant gain contours of the AlN device in the load plane (Z_{in}). (e) Schematic of the hybrid WuRx front-end integrated with the AlN resonator chip.

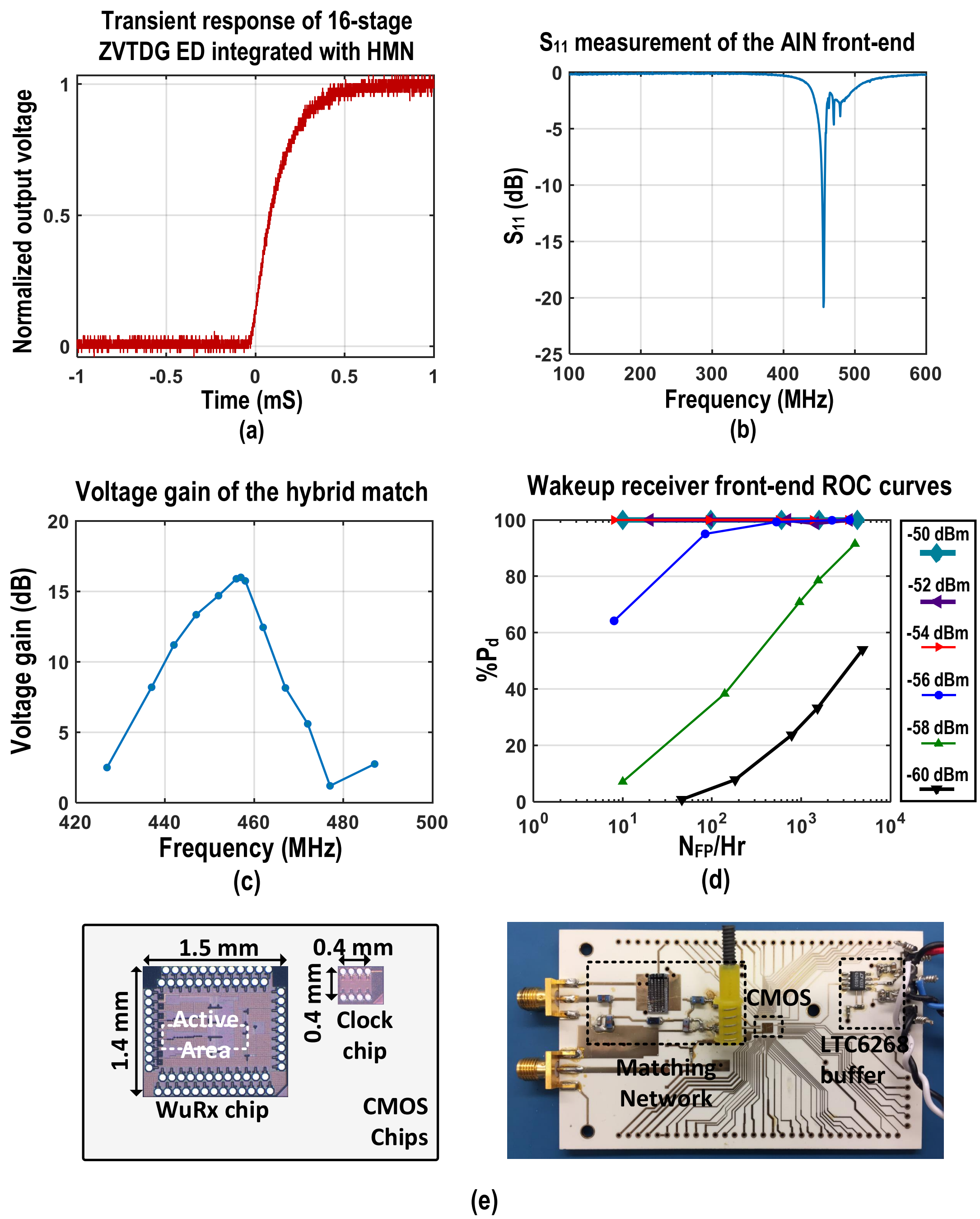


Figure 4.10: (a) Measured transient response of the 16-stage ZVTDG ED integrated with HMN achieving a charge time of 311 μs. (b) Measured S_{11} of the integrated AlN-based front-end with a 16-stage ZVTDG showing a match at 457 MHz. (c) Measured voltage gain of the integrated AlN resonator. (d) ROC curves of the AlN front-end, including the match. (e) PCB and die photographs of the 7-nW WuRx front-end, integrated with the AlN resonator chip.

charge time of 311 μs, which is a faster than that provided by the 45-stage LVTRF ED, mainly due to its fewer stages and the lower impedance of the ZVTDG devices. Figure 4.10(b) shows the measured S_{11} response of the AlN-based front-end, which shows a match at 457 MHz. The measurement results for the match voltage gain are shown in Figure 4.10(c). The voltage gain at 457 MHz is 16 dB with a 3-dB bandwidth of 15 MHz. Therefore, the overall Q of the match is around 30.5. The front-end is also measured with an integrated comparator, and the receiver operating characteristic (ROC) curves are shown in Figure 4.10(d). The ROC curves show the statistical relationship between the number of true positives (P_d) and number of false positives (N_{FP}), across different values of the receiver decision threshold. In a receiver with perfect sensitivity, ROC curves would pass through the top left corner of the plot, which corresponds to a decision threshold with a 100% detection rate and no false positives. In order to create these curves, for each setting of the offset on the comparator, different input power levels ranging from -50 to -60 dBm are given to the receiver. The false positive rates are averaged across different input power levels ranging from -50 to -60 dBm over 20 hours, and the true positive rates are averaged over 10^4 wakeups covering the span of one hour. The data rate of the WuRx is set to 1 kHz with an OOK modulation. The receiver is able to achieve a 100% detection rate with less than a single false positive per hour at an input power of -54 dBm, which can be improved by adding a digital correlator. The total power consumption of the front-end is 7 nW, with 0.7 nW for the system core clock, 0.5 nW for the clock bias generation resistive dividers, and 5.8 nW for the comparator. Note that the decision threshold of the comparator cannot provide noise-limited detection due to the lack of finer control bits over the input-referred offset voltage in the design. The setup and die photographs are shown in Figure 4.10(e).

A performance summary and comparison table of the front-ends is presented in Table 4.4.

4.6 Discussion

In the demonstrated hybrid matching network, the middle AlN-based stage enhances the overall Q and frequency selectivity of the front-end, which increases the robustness of the WuRx to interference-induced false wakeups. The main limitation to achieving higher gains at the current design frequency is the low Q of the tunable inductor L_t. This low Q results in a residual shunt resistance that is smaller than the input resistance of the ED. Since the AlN resonators are demonstrated at multi-GHz frequencies with Qs on the order of thousands [145], the current MEMS topology can be scaled to achieve a match at higher frequencies by reducing the pitch width of the IDTs. However, doing so also necessitates a smaller L_t that results in a smaller residual resistance. Therefore, as the match frequency increases, it is expected that the voltage gain will decrease. To achieve comparable performance at higher frequencies, the alternative solutions need to be able to either harness the high Q of the AlN resonator without the assistance of discrete elements or replace the L_t with higher Q inductive structures.

The main advantage of LiN-based MEMS resonators is their high electromechanical coupling and

Table 4.4: Performance summary and comparison table.

	This Work		Wang SSCL'18	Moody ISSCC'18		Jiang ISSCC'17	Wang ESSCIRC'17	Roberts ISSCC'16	Salazar ISSCC'15	Pletcher ISSCC'08
CMOS Technology	130 nm		180 nm	130 nm		180 nm	180 nm	65 nm	65 nm	90 nm
Carrier Frequency	88.8 MHz	457 MHz	109 MHz	151.8MHz	433 MHz	113.5 MHz	405 MHz	2.4 GHz	2.4 GHz	2 GHz
Power Consumption	N/A	7 nw	6.1 nW	7.4 nw	7.4 nw	4.5 nW	4.5 nW	236 nW	99 µW	52 µW
Data Rate	N/A	1 kbps	33.3 bps	200 bps	200 bps	300 bps	30 bps	8.192 kbps	10 kbps	100 kbps
Out-of-band Interferer Rejection Method	MMN	HMN	High-Q FE Transformer	High-Q FE Transofrmer		High-Q FE Transformer	High-Q FE Transformer	None	N-path filter	BAW Filter
Front-End Bandwidth	780 kHz	15 MHz	N/A	3 MHz	11 MHz	N/A	N/A	N/A	96 MHz	N/A
Front-End Passive Gain	14.3 dB	16 dB	30.6 dB	27 dB	23 dB	25 dB	18.5 dB	N/A	9.4 dB	0 dB
Bulky Element in Matching Network	None	Tunable Inductor	Two Air-core Inductors	Air-core Inductor	Air-core Inductor	Two Air-core Inductors	Air-core and SMD Inductors	Matching Network	SMD Inductors	None
Physical Volume of components	0.76 mm^3	1101.4 mm^3 **	N/A	~359 mm^3	~359 mm^3	N/A	N/A	N/A	N/A	N/A (Two Chip-scale dies)
Sensitivity	N/A	-54 dBm	-80.5 dBm	-76 dBm	-71 dBm	-69 dBm	-87 dBm	-56.5 dBm	-97 dBm	-72 dBm
Die Area	0.12 mm^2 *	0.15 mm^2 *	6 mm^2	1.95 mm^2		6 mm^2	1.27 mm^2 *	2.25 mm^2 *	0.0576 mm^2 *	0.1 mm^2 *

** Tunable inductor can be replaced by regular air-core inductors.
* Active area

FoMs; therefore, they have the potential to be used as standalone inductors with high quality-factors. Alternatively, the main advantages of the AlN technology are its monolithic integration compatibility with CMOS [146], a more mature fabrication process, and its ability to operate at higher frequencies. The proof-of-concept front-ends presented in this work demonstrate the applicability of MEMS resonators in implementing matching networks for nanowatt-level CMOS WuRx's. The overall minimum detectable signal of the front-ends can be optimized through the careful co-design of the MEMS resonators and the CMOS ED.

4.7 Summary and Conclusion

This chapter presented a design-oriented theory and analysis for MEMS-based matching networks and co-design techniques for optimizing the minimum detectable signal of MEMS-based WuRx front-ends. The chapter presented two proof-of-concept CMOS chips that are fabricated in a 130-nm RF-CMOS process and co-designed with their corresponding matching networks. The measured results demonstrate the feasibility of using MEMS resonators in sub-100 nW WuRx front-ends to provide substantial improvements over discrete-element matching networks in terms of reduced size, robustness to interference, and higher quality-factor matching. The highlights of the chapter are as follows.

1) Design-oriented study and analysis of MEMS resonators as frequency-dependent inductors in the electrical domain.

2) Introduced a graphical design method to determine the optimal load for the integration of a MEMS-based matching network with the ED-first architecture.

3) Demonstration of a proof-of-concept front-end that uses a LiN MEMS resonator for impedance transformation to a Dickson ED. The front-end operates in the 88.8 MHz FM band with a measured bandwidth of 0.78 MHz and quality-factor of 114. Compared to discrete-element matching networks, this front-end decreases the system size by more than two orders of magnitude and reduces the input RF bandwidth by up to one order of magnitude.

4) Demonstration of a proof-of-concept AlN MEMS resonator-based WuRx front-end. The front-end uses a hybrid matching network that operates at 457 MHz UHF band with a 3 dB bandwidth of 15 MHz. The measured results indicate that the front-end achieves a sensitivity of -54 dBm with an average power consumption of 7 nW without a digital correlator.

4.8 List of Relevant Publications

[PB4] P. Bassirian et al., "Nanowatt-Level Wakeup Receiver Front Ends Using MEMS Resonators for Impedance Transformation," *in IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 4, pp. 1615-1627, April 2019.

[PB5] S. M. Bowers et al., "Nanowatt Level Wake-up Receivers Using Co-designed CMOS-MEMS Technologies," *in Proceedings of GOMACTech*, Mar. 2018, pp. 1–4.

[PB7] P. Bassirian et al., "A Passive 461 MHz AlN-CMOS RF Front-end for Event-driven Wakeup Receivers," *2017 IEEE SENSORS*, Glasgow, 2017, pp. 1-3.

Chapter 5

Techniques for Sub-GHz WuRx Design Using Co-Designed Discrete Matching Networks

In sub-GHz WuRx applications where the size of the system is not a primary driver of the design, air-core inductors are suitable candidates for implementing an off-chip matching network. Similar to the case for other types of matching networks, the co-design of a discrete match with the ED is required for optimizing detection SNR. This chapter presents a co-design technique for discrete matching networks that use off-chip inductors and for which the Q of the match is limited by the Q of the inductor. The chapter presents a proof-of-concept ED-first 7.4 nW WuRx that operates in the 151.8 MHz Multi-Use Radio Service (MURS) band and uses a discrete tapped-capacitor matching network for the impedance transformation from the 50 Ω port to the ED input. The matching network achieves a Q of about 32 with a bandwidth of approximately 4.7 MHz, and the WuRx achieves a sensitivity of -76 dBm.

5.1 Envelope Detector Co-Design with Discrete Matching Networks

As discussed in the previous chapters, the input impedance of the ED is a capacitive load. To provide a matching network between a source impedance (e.g., 50 Ω) and the ED input impedance, a tapped-capacitor matching network as shown in Figure 5.1(a) can be used. At the resonant frequency, all reactive elements resonate out and the source impedance is up-converted by the ratio of the trimmer capacitors to match the real part of the ED impedance in parallel with R_P, the shunt resistance of the matching inductor. For minimizing the loading effect of R_P, air-core inductors are appropriate design choices. The optimal number of ED stages N_{opt} is determined by a trade-off between three factors, that is, the loading effect of the ED input impedance on the matching

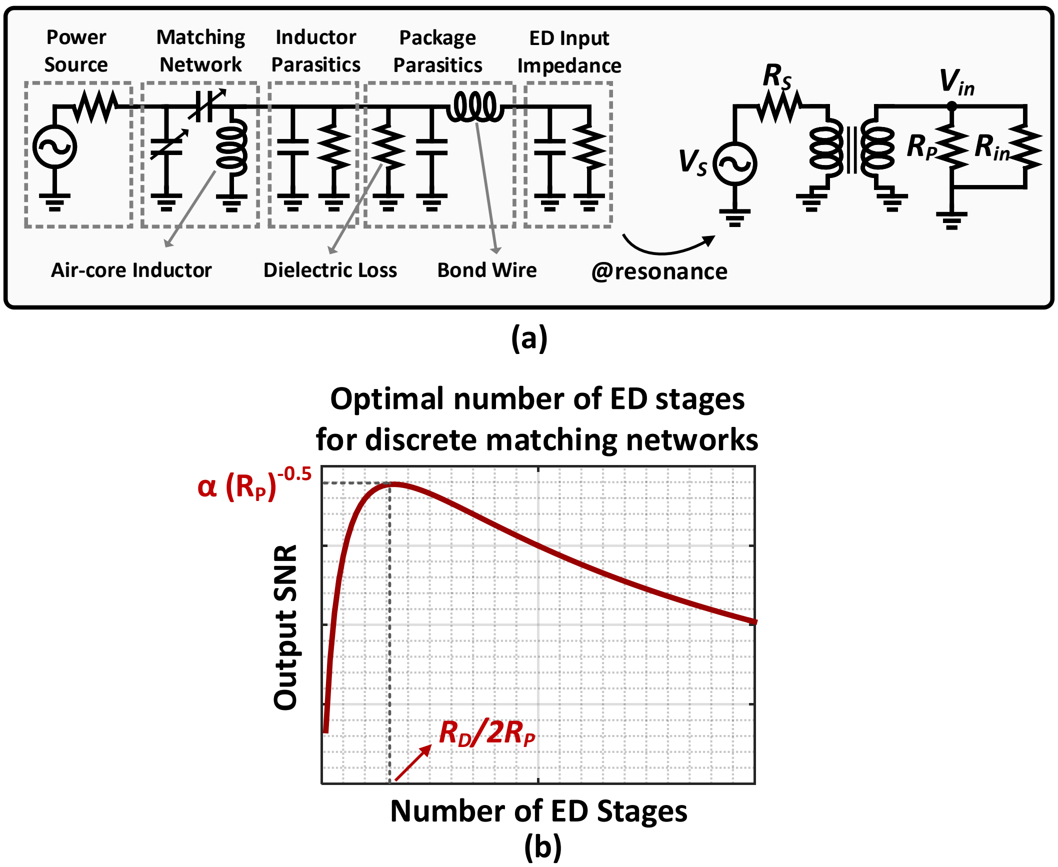


Figure 5.1: (a) Schematic of the tapped-capacitor matching network with packaging parasitics. (b) ED output SNR versus the number of ED stages for a given high-Q air-core inductor.

network, the amplitude of the output baseband signal, and the output noise. Using the conservation of energy, it can be written

$$\frac{V_S^2}{8R_S} = \frac{V_{in}^2}{R_P||R_{in}} = \frac{(R_D + 2NR_P)}{R_D R_P} V_{in}^2 \Rightarrow V_{in}^2 = \frac{V_S^2}{8R_S} \times \frac{R_D R_P}{(R_D + 2NR_P)}. \tag{5.1}$$

Equation 2.2 suggests that the output baseband voltage of the ED can be expressed as

$$V_{BB}(N) = 2N \times \mu_D V_{in}^2 = (\frac{\mu_D V_S^2}{8R_S} R_D R_P) \times \frac{2N}{R_D + 2NR_P}. \tag{5.2}$$

Assuming that the RF excitation is weak, the output noise generated by the ED comes purely from the channel thermal noise and is equal to

$$V_{n,rms} = \sqrt{2N \times 4kT\gamma R_D \times \Delta f}. \tag{5.3}$$

Therefore, the output SNR, defined here as the ratio of the signal and noise voltages, can be written as a function of the number of stages N

$$SNR_{out}(N) = \frac{V_{BB}}{V_{n,rms}} = (\frac{\mu_D V_S^2}{8R_S} \times \frac{R_P\sqrt{R_D}}{\sqrt{4kT\gamma\Delta f}}) \times \frac{\sqrt{2N}}{R_D + 2NR_P} \tag{5.4}$$

The maximum of the output SNR can be found at N_{opt} by setting the derivative equal to zero

$$\frac{d(SNR_{out})}{dN} = 0 \Rightarrow N_{opt} = \frac{R_D}{2R_P}. \tag{5.5}$$

Therefore, the output SNR with the optimal number of stages is equal to

$$SNR_{opt} = \frac{\mu_D V_S^2}{16R_S} \times \sqrt{\frac{R_P}{4kT\gamma\Delta f}} \tag{5.6}$$

which is independent of the diode resistance R_D. For a given sub-threshold slope, a higher R_D (in high-V_{th} devices) results in higher noise and a higher signal at the N_{opt} point. Designing the ED with high-V_{th} devices means that the noise and power requirements can be relaxed for the subsequent baseband amplification block since the ED noise can become the dominate source of noise in the chain. However, this relaxation comes at the cost of a slower charge time, which, in turn, affects the wakeup latency of the WuRx.

5.2 Proof-of-Concept MURS-Band WuRx

The WuRx system's schematic and waveforms at the input and output of each block are depicted in Figure 5.2. The RF input signal first passes through a passive tapped-capacitor matching network with a transducer voltage gain of 27 dB. The match is followed by an ED with an OCVS of 306 1/V, which converts the RF signal to baseband. This baseband signal is further amplified by a baseband amplifier with a gain of 25 dB, which subsequently drives a ULP sub-mV triggered voltage comparator. The digital output of the comparator is latched by an 8-bit correlator that compares the received code with a programmable reference code. The correlator generates a wakeup signal if the correct reference code is received, which can wake up the rest of the sensor node.

The ED is implemented with low-voltage-threshold RF (LVTRF) devices. These devices have a slightly higher R_D compared to zero-voltage-threshold (ZVT) devices and provide good trade-offs between the charge time and the output signal's amplitude. The coupling capacitors are implemented using 60 fF metal-insulator-metal capacitors (MIMCAP) that are located between the

M7-M8 metal layers and have lower parasitic capacitances to the chip substrate compared to metal-oxide-metal capacitors (MOMCAP). To keep the charge time below 5 ms, the number of stages is set to 45. The total simulated input impedance of the ED is $50\ k\Omega||0.6\ pF$, including the input pad and ESD diodes.

The measured S_{11} response of the matched ED is shown in Figure 5.2(b). There is a match at 151.8 MHz with a Q of about 32 and a bandwidth of approximately 4.7 MHz. The normalized transient response of the ED is shown in Figure 5.2(c), indicating a charge time of 5 ms. The front-end is integrated with the WuRx system, as shown in Figure 5.2(d), and achieves a sensitivity of -76 dBm with 7.4 nW of power consumption. The WuRx performance summary and table of comparison with prior state-of-the-art are presented in Table 5.1.

5.3 Summary and Conclusion

This chapter presented a co-design technique for optimizing the detection SNR of discrete matching networks that use off-chip inductors. The optimal number of ED stages is determined by the quality-factor of the off-chip inductor and topology of the matching network. The highlights of the chapter are as follows.

1) Introduced an analytical design method for optimizing the SNR of a tapped-capacitor-based WuRx front-end.

2) Presented a proof-of-concept ED-first 7.4 nW WuRx that operates in the 151.8 MHz MURS band and uses a discrete tapped-capacitor matching network for the impedance transformation from the 50 Ω port to the ED input. The matching network achieves a Q of about 32 with a bandwidth of approximately 4.7 MHz, and the WuRx achieves a sensitivity of -76 dBm.

5.4 List of Relevant Publications

[PB3] J. Moody et al., "Interference Robust Detector-First Near-Zero Power Wake-Up Receiver," *in IEEE Journal of Solid-State Circuits*, 2019.

[PB6] J. Moody et al., "A -76dBm 7.4nW Wakeup Radio with Automatic Offset Compensation," *2018 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, 2018, pp. 452-454.

Table 5.1: Summary of the WuRx performance and comparison with prior state-of-the-art.

	This Work		Sadagopan RFIC'17	Jiang ISSCC'17	Roberts ISSCC'16	Salazar ISSCC'15	Abe VLSI'14	Pletcher ISSCC'08
Technology	130 nm		65 nm	180 nm	65 nm	65 nm	65 nm	90 nm
Carrier Frequency	151.8MHz	433MHz	2.4GHz	113.5MHz	2.4GHz	2.4GHz	925.4MHz	2 GHz
Power Consumption	7.4 nw	7.4 nw	365 nW	4.5 nW	236 nW	99 µW	45.5 µW	52 µW
Data Rate	200 bps	200 bps	2.5 kbps	300 bps	8.192 kbps	10 kbps	50 kbps	100 kbps
Dissipated Energy per bit	37 pJ	37 pJ	146 pJ	15 pJ	28.8 pJ	9900 pJ	910 pJ	520 pJ
In-band Interferer Rejection Method	Auto offset control loop		Off-chip control loop	N/A	Auto threshold control	N/A	2-Step Wakeup	N/A
Out-of-band Interferer Rejection Method	High-Q FE Transofrmer		High-Q FE Co-Design	High-Q FE Transformer	N/A	N-path filter	N/A	MEMS Filter
Sensitivity	-76 dBm	-71 dBm	-61.5 dBm	-69 dBm	-56.5 dBm	-97 dBm	-87 dBm	-72 dBm
Sensitivity with interference	-75 dBm [1]	N/A	-58.5 dBm [1]	N/A	N/A	-94 dBm [2]	-84 dBm [3]	N/A
Die Area	1.95 mm^2		1.1 mm^2 *	6 mm^2	2.25 mm^2 *	0.0576 mm^2 *	1.27 mm^2 *	0.1 mm^2 *

[1] Carrier-to-interference ratio (CIR) of -20dB at -3MHz offset with 10^{-3} BER
[2] CIR of -31dB/-27dB at +/-5MHz offset with 10^{-3} BER
[3] CIR of -40dB at -3 MHz offset with 1% packet error ratio (PER)
* Active area

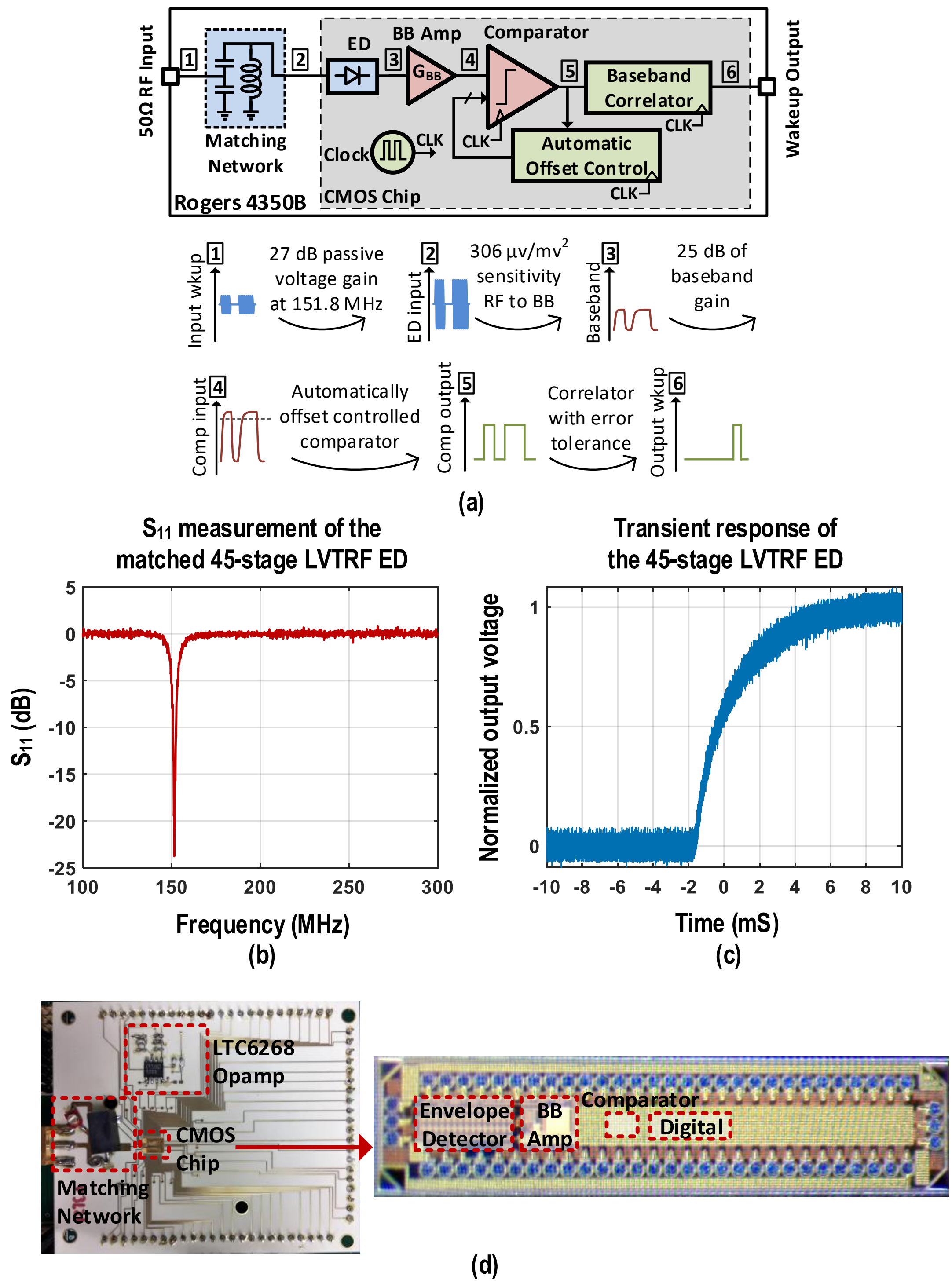


Figure 5.2: (a) Schematic of the MURS band wakeup receiver with analog and digital waveforms at various nodes throughout the chain. (b) Measured S_{11} of the integrated wakeup receiver front-end. (c) Transient response of the ED. (d) Photos of the system PCB and the CMOS die.

Chapter 6

Conclusions and Future Directions

6.1 Dissertation Conclusions

This dissertation presented techniques for the design of sub-100 nW WuRx's to enable low-cost and ubiquitous sensor networks. The dissertation studied the fundamental detection limits of the ED-first architecture and provided implementation techniques for approaching that limit. The experimental results of this dissertation, as demonstrated on several proof-of-concept CMOS chips, indicate that it is feasible to use the ED-first architecture to achieve WuRx's with sub-100 nW power consumption and < -60 dBm sensitivities, that are robust to temperature and interference. The results also indicate that the integration of ED-first RF front-ends with MEMS resonators can enable significant size reductions compared to discrete matching networks at sub-GHz frequencies as well as higher Q matching and robustness to out-of-band interference. The high-level summary of the design techniques proposed in this dissertation are as follows.

1) At the RF front-end of the WuRx, the ED needs to be co-designed with the matching network to optimize the detection SNR. The optimal number of ED stages depends on the quality-factor of the passive elements and the architecture of the matching network. An example of a co-design with a discrete matching network is presented in Section 5.1.

2) MEMS resonators can be used as matching networks in ED-first WuRx's, but they have a limited capacitive drive strength. Therefore, the ED needs to be co-designed with the MEMS resonator to reach the specific capacitive loading needed to optimize the WuRx detection SNR. The graphical design method presented in Section 4.3 can be used to determine the optimal load.

3) On-chip field confinement in the high-impedance RF environment of the ED input is essential for mitigating the substrate loss at multi-GHz frequencies and increases the WuRx MDS by several decibels. Further details and experimental proof of this technique are presented in Section 2.2.

4) To ensure noise-limited digitization of the RF wakeup signal, the sub-nW capacitively-balanced thermometer-coded StrongArm Latch topology can be used to enable sub-mV resolution for the

comparator decision threshold. The details of this techniques are presented in Section 3.2.

5) Calibrating only the WuRx baseband clock frequency and comparator decision threshold can provide temperature robustness in the commercial temperature range of 0°C to 70°C.

6) A nW-power PID controller can be used to calibrate the decision threshold of the comparator continuously across temperature and in the presence of interference signals. An example of this technique, along with further details, is presented in Section 3.3.

7) The design of the WuRx with an optimal fault-tolerant wakeup code can maximize the receiver sensitivity, while enabling discrimination between various nodes and mitigating interference-induced false wakeups. An example of the wakeup code design is presented in Section 2.3.

6.2 Methodology for Sub-100 nW WuRx Design

This dissertation recommends the following methodology for the design of sub-100 nW WuRx's.

I. Perform a system-level power consumption analysis based on the functionality and activity factor of the nodes to determine the WuRx power budget. An example of the power consumption analysis is presented in Section 1.2.2.

II. Determine the operation frequency of the WuRx and the type of matching network to be used.

III. For the particular application, determine the number of required wakeup codes and the wakeup latency. Determine the required network range and perform a link budget calculation to determine the required WuRx sensitivity.

IV. Calculate the fundamental detection limit of the RF front-end with the integrated matching network and ED to verify that the WuRx design objectives do not exceed this limit. If the objectives cannot be satisfied, a trade-off needs to be made with regards to the parameters determined in Steps (I)-(III). An example of the fundamental detection limit calculation is presented in Section 2.4.

V. Synthesize the digital circuits, including the correlator and the PID controller, to determine the power budget for the analog and mixed-signal baseband circuits.

VI. Design the baseband amplifier subject to its power budget. Determine the detection SNR at the output of the amplifier and verify that the WuRx metrics can still be met.

VII. From the amplitude of the pre-digitization baseband signal, design the comparator to provide more than an order of magnitude finer resolution for the decision threshold.

VIII. Tune the parameters of the PID controller based on the types of interference that are present in the environment. An example of this process is presented in Section 3.3.

6.3 Future Directions

The low-power WuRx design space provides an opportunity to re-evaluate the traditional design practices for the receivers and network protocols and to place more emphasis on energy efficiency instead of pushing for higher data-rates and spectrum efficiency. While the research results in this field indicate a promising future for low-power receivers, significant challenges still need to be addressed to enable reliable communication between trillions of low-power devices. These challenges are similar to those faced in traditional receivers but require more power-efficient solutions. Some of the areas that present significant opportunities for the future of the ULP WuRx field are presented in this section.

6.3.1 Compatibility with Batteries and Energy Harvesters

Since the ULP IoT devices are powered by batteries or energy harvesters, they need power management units (PMU) that make them compatible with these sources of energy. Traditional PMU designs need to be tailored towards the needs of low-power IoT systems to create an integrated solution that does not violate the acceptable power consumption range. Designing just the WuRx under a stringent power budget does not accomplish the desired lifetime extension. Also, energy harvesting solutions need take into account the stochastic nature of harvested energy. Therefore, the necessary blocks of a ULP PMU, such as the voltage regulators, voltage references, and current references, need to be designed with greater emphasis on low-power consumption. The new solutions may compromise accuracy and precision in comparison to their higher-power counterparts [147], but they are “accurate enough” for their specific applications.

6.3.2 Robustness to Interference and Frequency Diversification

The massive deployment that is envisioned for the IoT increases the challenge regarding resilience to interference. Meanwhile, a large number of reports on low-power WuRx’s in the literature do not even report on their performance in the presence of interfering signals [148]. At sub-100 nW power levels, filtering out-of-band interference is very significant due to the lack of down conversion mixers and filtering. Therefore, there is a tremendous opportunity for MEMS-based matching networks to provide this enhanced suppression of unwanted signals. Additionally, less cluttered higher-frequency bands, such as the 24 GHz ISM and 60 GHz ISM bands, offer a great opportunity for the diversification of the operation frequencies of ULP systems. Enabling these higher frequency bands requires innovative solutions at the device level to the packaging level.

6.3.3 Enhancing the Dynamic Range of ULP WuRx's

As the measurement in Section 3.5.2 indicate, when a receiver is at its maximum sensitivity setting, the ability to detect desired signals with greater amplitudes diminishes as large signals push the baseband circuits into saturation. In higher power data receivers, this issue can be handled by an initial handshake between the transmitter and the receiver to determine the Received Signal Strength Indication (RSSI). However, a WuRx is not aware of the presence of any signal in the environment and is the means of establishing handshake with the main receiver. This issue motivates the need for power efficient spectrum analysis to reconfigure the WuRx based on its distance to the transmitter and the existing background interference.

6.3.4 Low-Cost and Reliable Clock Calibration

The calibration of the clock frequency to maintain precise timing during the reception of a wakeup is a critical need for temperature robustness in WuRx's. However, if low-power devices are being deployed at tera-scale volumes, the cost of their pre-deployment testing and calibration can be prohibitively large and become a detriment to an IoT deployment scale. The crystal-less clock calibration schemes usually need at least one or two trims before deployment and are prone to deviations due to aging. Therefore, the opportunity for crystal-based clocks and innovative crystal-less solutions remains open in the future of this field.

6.3.5 ESD Robustness and Long-Term Reliability

To enable decade-long lifetimes in ubiquitous sensing systems, low-power circuit design techniques must be accompanied by other long-term reliability enhancements. For example, a device that operates in an uncontrolled environment for a decade is more likely to experience rare and strong ESD stresses and therefore needs ESD-robust input/output interface circuits. This support circuitry needs to be subjected to stringent power budgets; because otherwise, the integrated solution will not achieve its lifetime extension goal. The long-term reliability challenge also applies to the mean time-to-failure (MTTF) of the devices used in a design kit. For example, if an application requires an interface with a high-voltage source of energy, the lifetimes of the devices connected to the high-voltage source can become the bottlenecks to long-term reliability. This challenge calls for innovations at the device and circuit levels to ensure that the final integrated solution can achieve the desired decade-long lifetime.

6.3.6 Ultra-Low-Power Network Protocols

Compliance with universal communication standards is a must for trillions of devices that need to exchange data with one another. So far, low-power communication protocols, such as Bluetooth Low Energy (BLE), have targeted power consumption ranges of hundreds of microwatts to milliwatts. Meanwhile, to comply with pre-existing standards, sub-μW receivers have used back-channel communication methods with standard-compliant transmitters to emulate signals of interest. Future network protocols must take the limitations of ULP receivers into account in order to accommodate more relaxed requirements for these receivers.

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