Heterogeneously Integrated Photodiodes on Silicon

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This dissertation is dedicated to my parents and girlfriend for their love and support.

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Abstract

High speed, high efficiency and high power photodiodes are key components in digital and analog photonic systems [1] [2]. To fully exploit the benefits of optical systems, high performance photodiodes are needed. Silicon photonics, as a promising enabler for low-cost and high performance passive photonic devices with potential deployment in next generation data center and many other applications, has attracted vast research and funding during the past decade. However, due to the fact that silicon is transparent at telecommunication wavelengths and its indirect bandgap, it is challenging to achieve active devices, such as lasers and photodiodes, out of silicon. One solution is to heterogeneously integrate group III-V materials onto a SOI/silicon platform.

The objective of this dissertation is to study and demonstrate high performance photodiodes heterogeneously integrated onto a silicon photonics platform. Chapter 1, 2 and 3 review photodiode fundamentals, heterogeneous integration approaches, optical coupling schemes, and fabrication and characterization techniques. Chapters 4, 5 and 6 focus on device design, fabrication and characterization of molecular bonded waveguide photodiodes. Chapters 7 and 8 describe an alternative bonding process and a waveguide photodiode design using SU8 as adhesive.

In my dissertation I demonstrate modified uni-traveling carrier (MUTC) photodiodes with top p-contact heterogeneously integrated on silicon-on-insulator (SOI) nano-waveguides. Single photodiodes have very low dark current of 1 nA and a high bandwidth of up to 65 GHz. At 70 GHz, a record-high RF output power of -2 dBm at 20 mA was measured. Balanced photodiodes of this type reached 20 GHz bandwidth and a CMRR of 20 dB. In Chapter 7, InGaAsP/InP high-power photodiode structure was bonded onto a silicon die using SU8 and surface normal photodiodes were fabricated. These photodiodes have very low dark currents and are similar to photodiodes on native InP substrate [3]. The responsivity was found to be 0.4 A/W, which is close to the calculated value. Based on my findings in

Chapter 7, I developed a design of an adhesively integrated high efficiency waveguide photodiode on SOI that promises a bandwidth of up to 160 GHz.

Table of Content

List of Figures

List of Tables

Chapter 1 Introduction

Nowadays, fiber optic links are widely used in high-capacity digital data transmission. In addition, they are being considered for emerging analog applications including radio frequency (RF) signal generation, processing, and distribution. The absorption of a typical silica fiber at 1310 nm and 1550 nm is lower than 0.6 dB/km. At 1550 nm wavelength, absorption is below 0.2 dB/km, which is even lower than in free space. Given the high (optical) carrier frequency optical fiber can transmit, it has the potential to accommodate extremely large modulation bandwidths. Other than the advantages of low loss and broadband, fiber optic links also have the advantages of low dispersion, immunity to electromagnetic interference, high security, light weight, and compact size. To fully exploit the benefits of optical fibers, high performance optoelectronic components are needed. On the receive side, this implies photodiodes with the requisite quantum efficiency and bandwidth.

Although most fiber optic systems transmit digital data, analog optic links have found an increasing number of applications [1]. By employing analog optic links in the cable TV signal distribution process, lossy electrical cables and expensive broadband electrical amplifiers have been eliminated. In phased array antennas, bulky and high-cost microwave cables can be replaced by light weight fiber. For antenna

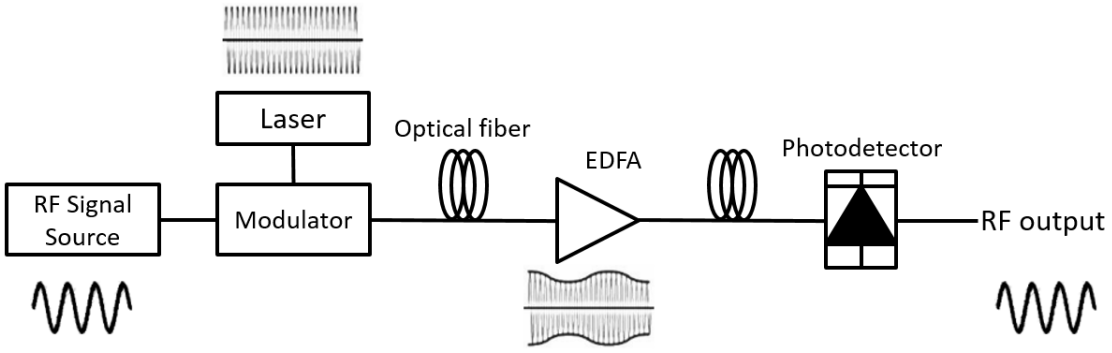


Figure 1.1 Analog optic link

remoting, the low-loss optical fiber is used to deliver the RF-modulated light to a remote antenna from a base-station, where expensive signal processing equipment is kept.

A simple analog optical link includes the following components [4]: laser, RF signal source, modulator, optical fiber, erbium doped fiber amplifier (EDFA) and photodetector, as shown in Figure 1.1. The RF signal is modulated onto the optical carrier by the modulator, and then the modulated light signal is transmitted through the channel – the optical fiber, and amplified by the EDFA. At the receiving end, the modulated laser signal is converted back into an RF electrical signal by the photodetector. In order to exploit the low loss from the fiber and the benefits of the EDFA, the signal wavelength is typically chosen to be 1550 nm. The applications mentioned above continue to push the performance of RF analog optical links to higher performance. Two of the essential figures of merit are link gain and noise figure [1]. A low noise figure is preferable for all RF analog application scenarios described above. The most straightforward method of achieving a low noise figure and high gain is to operate the photodiode at high output photocurrent while maintaining a good linearity [5]. In addition, high link bandwidth requires a high-speed photodiode. Therefore, a high-speed, high-power and high-responsivity photodiode is desired.

Chapter 2 Photodiode Fundamentals

2.1 Fundamentals

A photodiode is a solid-state device that converts incident photons into electron-hole pairs for external circuit extraction (O/E conversion). During the conversion, two main processes are involved: photon absorption and carrier transport. Only when the energy of the incident photon is larger than the bandgap of the absorber material, the photon can excite an electron from the valence band into the conduction band. The equation linking the longest wavelength being absorbed λ_g and the absorber bandgap E_g is given by:

$$\lambda_g[\mu m] = \frac{1.24}{E_g[eV]} \qquad \textit{Equation 2-1}$$

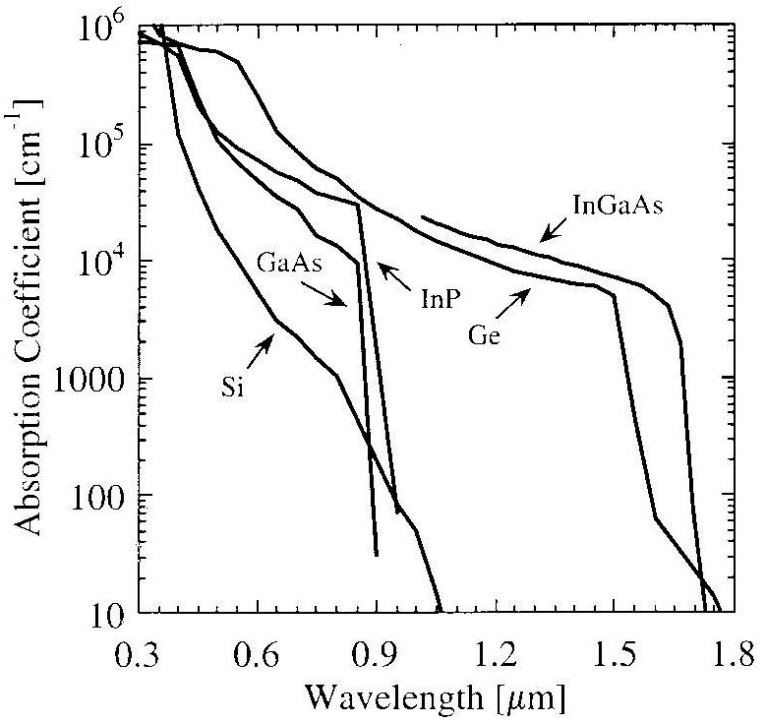


Figure 2.1 Absorption spectrum of some semiconductor materials [7]

After a free electron-hole pair is generated, both drift and diffusion can transport carriers from the absorber to the contact layers.

For telecommunication applications, the wavelength of choice is between 1300 nm and 1600 nm. From the perspective of material systems, photodiodes require high crystal quality, tunable bandgap and high absorption. To this end the quaternary material system, InGaAsP, is an ideal choice. It can be grown lattice-matched onto InP substrates. Typically, the absorber is $In_{0.53}Ga_{0.47}As$, which has an absorption constant α of 7000/cm at 1550 nm wavelength [6]. Figure 2.1 shows the absorption spectrum of some semiconductor materials. Both, $In_{0.53}Ga_{0.47}AS$ and Ge are commonly used as the absorber of the photodetector [7].

A simple but classical photodiode structure is the PIN photodiode grown on InP. The InGaAs absorber is sandwiched by two highly doped contact layers which are bandgap-engineered to be transparent to the operating wavelength. Figure 2.2 shows a schematic band diagram of a PIN photodiode. In response to the built-in electrical field in the space charge region photo-generated electrons and holes drift to the cathode and anode, respectively. Usually, in order to increase the photodiode's response speed, a reverse bias voltage is applied to fully deplete the absorber and support carrier drift.

Dark current is the current that flows through the device under reverse bias voltage when there is no light injected. A low dark current is a desired characteristic of photodiodes as it indicates high material quality, low surface leakage, and improves the signal-to-noise ratio.

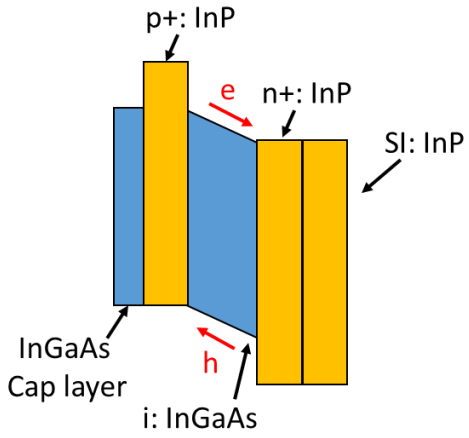


Figure 2.2 Band structure of heterojunction PIN photodiode adopted from ref. [10]

Quantum efficiency is the figure of merit that characterizes how efficient a photodiode converts incident photons into free carrier pairs. If coupling loss from the optical source to the photodiode is calibrated out, the quantum efficiency is called the internal quantum efficiency (IQE); instead, if coupling loss is included in the measurement, the quantum efficiency is called external quantum efficiency (EQE). Quantum efficiency, η, is defined as the number of free carrier pairs generated by the number of incident photons:

$$\eta = \frac{I_{pd}}{q} * \frac{h\nu}{P_{Optical}} \qquad \textit{Equation 2-2}$$

where I_{pd} is the photocurrent, v is the optical frequency of the incident light, and $P_{Optical}$ is the optical input power. If quantum efficiency, η, is viewed as 'micro-level' measure of efficiency, then responsivity, R, can be recognized as 'macro-level' efficiency figure of merit, which is defined as the ratio of photocurrent to the input optical power

$$R = \frac{I_{pd}}{P_{Optical}} = \frac{\eta\lambda[\mu m]}{1.24} A/W. \qquad \textit{Equation 2-3}$$

From the equation, we see that the theoretical upper limit of responsivity at 1550 nm wavelength is 1.25 A/W, assuming a quantum efficiency of η=100%. If η is the value of internal quantum efficiency,

then the corresponding responsivity is called internal responsivity. Likewise, if η is the value of external quantum efficiency, then the calculated responsivity is defined as external responsivity. Internal quantum efficiency describes the optical-electrical conversion efficiency of the absorber alone, while external quantum efficiency includes all the optical loss mechanisms. Polarization dependent loss (PDL) is defined to be [8]

$$PDL = 10lg\left(\frac{R_{max}}{R_{min}}\right) \qquad \textit{Equation 2-4}$$

Here, R_{max} and R_{min} are the maximum and minimum responsivity for all states of polarization.

When incident light is normal to the interface of two materials with refractive index of n_1 and n_2, the percentage of reflected optical power is described by

$$R = \left|\frac{n_1 - n_2}{n_1 + n_2}\right|^2 \qquad \textit{Equation 2-5}$$

The 3-dB bandwidth is another important figure of merit as it quantifies how fast a photodiode can respond to an incident modulated light signal. There are two main factors limiting the bandwidth of a photodiode: the carrier transit time and the resistance-capacitance (RC) time constant. Considering only the RC effect, the 3-dB electrical frequency is [9]

$$f_{RC} = \frac{1}{2\pi C_{pd}(R_L + R_S)} \qquad \textit{Equation 2-6}$$

where R_L is the load resistance, typically 50 Ω; R_S is the photodiode's series resistance originating from metal/semiconductor contacts. A typical value is ~5 Ω; C_{pd} is the photodiode's junction capacitance, which can be estimated by the parallel plate capacitor equation

$$C_{pd} = \frac{\varepsilon A}{d} \qquad \textit{Equation 2-7}$$

where ε is the absolute permittivity of the dielectric material (III-V semiconductor), A is the active area of the photodiode and d is the depletion width. For balanced photodiodes, the area in equation 2-7 needs to be doubled, because of the two individual diodes in parallel.

For the transit time limit, the 3-dB bandwidth can be found to be [9]

$$f_{tr} = \frac{3.5\bar{v}}{2\pi D} \qquad \textit{Equation 2-8}$$

where $\frac{1}{\bar{v}^4} = \frac{1}{2}\left(\frac{1}{{v_e}^4} + \frac{1}{{v_h}^4}\right)$, v_e is the electron drift velocity, v_h is the hole drift velocity and D is the carrier drift distance. In practice, for the MUTC photodiode, the majority carriers that drift most of the distance are electrons; therefore, $\bar{v} \approx v_e$ can be used as an approximation.

Assuming these two limiting factors are independent and have Gaussian response, the overall 3-dB bandwidth is given by [9]

$$f_{3dB} = \frac{1}{\sqrt{\frac{1}{{f_{RC}}^2} + \frac{1}{{f_{tr}}^2}}} \qquad \textit{Equation 2-9}$$

For surface-normal-illuminated pin photodiodes (Figure 2.3a), there is a trade-off between responsivity and bandwidth, regarding the thickness of the absorber. A thick absorber gives rise to a higher responsivity; however, it also increases the carrier transit time, which leads to a reduction in bandwidth. For waveguide photodiodes (Figure 2.3b), this inherent trade-off is solved by decoupling responsivity and bandwidth. In waveguide photodiodes, the responsivity is no longer a strong function of absorber thickness; instead, it is a function of photodiode length. In this way, we can achieve high performance of both, responsivity and bandwidth.

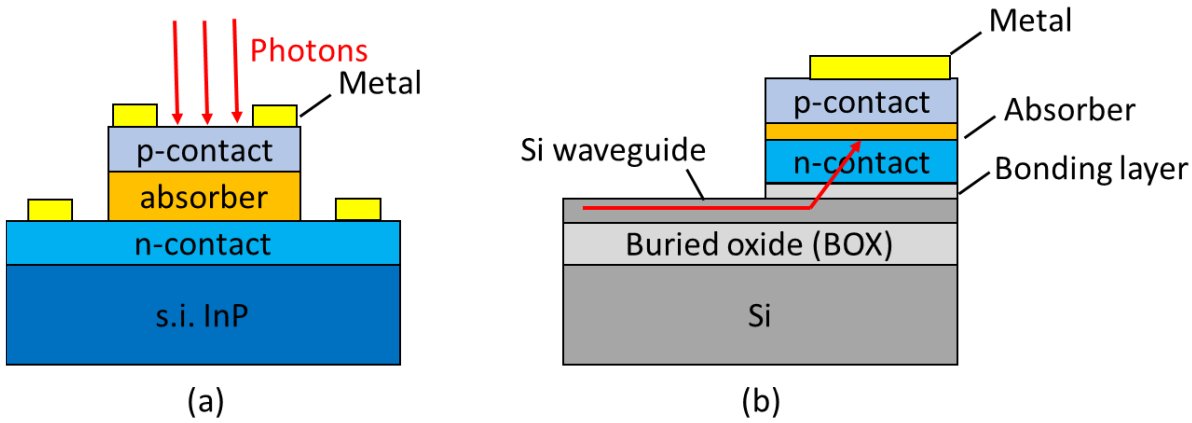


Figure 2.3 Surface normal illuminated pin photodiode (a) and waveguide photodiode (b)

2.2 Types of High Power Photodiodes

In this section, simple PIN photodiodes, partially depleted absorber (PDA) photodiodes, uni-traveling-carrier (UTC) photodiodes and modified uni-traveling-carrier (MUTC) photodiodes, are discussed and compared [10].

2.2.1 PIN Photodiodes

Although PIN photodiodes have relatively high responsivity and simple structures, they cannot endure high photocurrent. The power handling capability of PINs is mainly limited by two factors: thermal failure and the space-charge effect from the slow holes [11].

In order to fully deplete the not-intentionally-doped (n.i.d.) InGaAs absorber and ensure that the electrons and holes drift at their saturation velocity, the electric field needs to be high enough. However, the electric field in the InGaAs absorber is the culprit of most of the heat generation in PINs. This leads to an inherent trade-off between electric field strength and thermal failure.

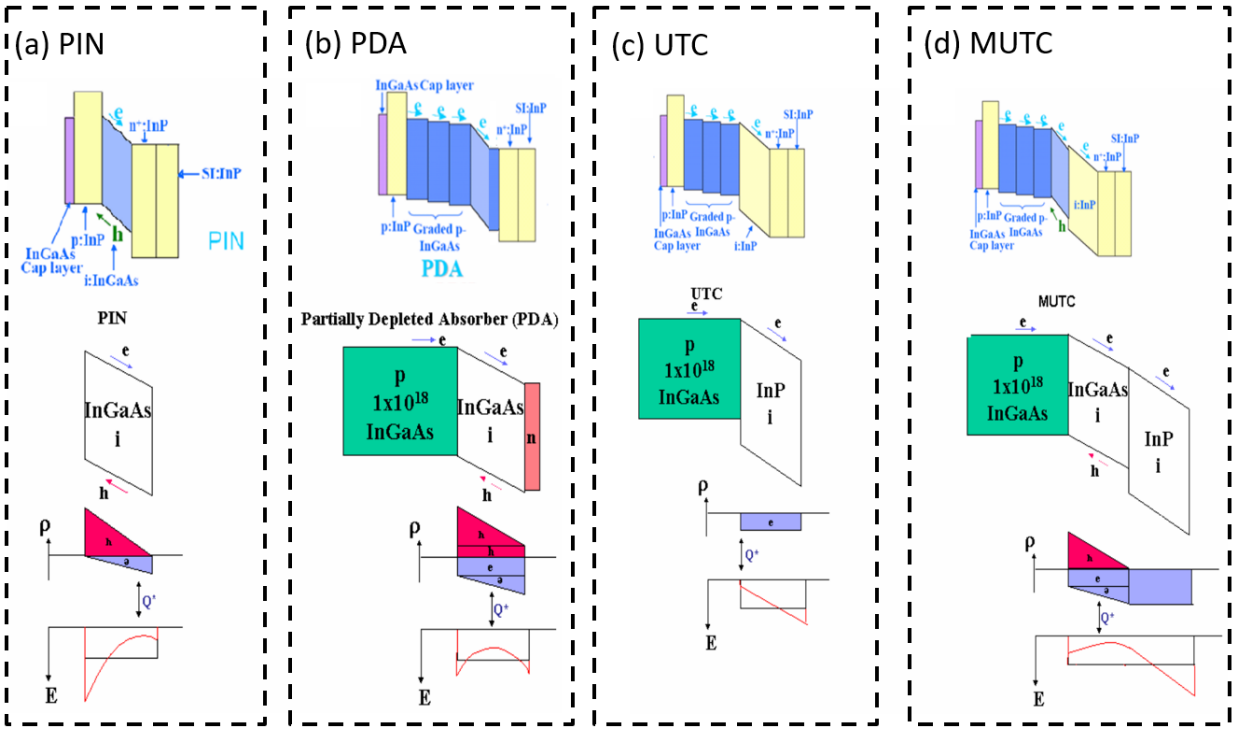


Figure 2.4 Band diagram, carrier distribution and electric field distribution of (a) PIN photodiode, (b) PDA photodiode, (c) UTC photodiode and (d) MUTC photodiode

In most III-V materials, electrons drift faster than holes. This fact leads to an imbalance in the spatial distribution of the photon-generated carriers in such a way that more holes accumulate in the depleted intrinsic absorber, as shown in Figure 2.4a. As the optical power increases and photon-generated carriers accumulate, the electric field in the depleted region is screened by the charge of the photogenerated carriers. Due to this space charge, the electric field collapses near the n side. When the electric field drops below a certain level, carriers cannot drift at their saturation velocity. Therefore, the

bandwidth decreases and the RF output power saturates. Simple PIN photodiodes are of limited use in high-power applications.

2.2.2 Partially Depleted Absorber (PDA) Photodiodes

The photon-generated carriers in the depleted drift region can be balanced by adding sections of undepleted absorber on both sides of the depleted absorber. Such a structure is called partially depleted absorber (PDA) photodiodes [12] (Figure 2.4b). By tuning the doping profile and layer thicknesses, the position where the electric field collapses can be shifted to the center of the depleted absorber. In addition to charge balancing, because of a thinner depleted absorber, the space charge effect is also mitigated. However, since part of the narrow-bandgap InGaAs is depleted, PDA photodiodes still suffer from thermal failure and space-charge effect. PDA photodiodes have achieved higher saturation currents and output power levels than PINs [11].

2.2.3 Uni-Traveling-Carrier (UTC) Photodiodes

The uni-traveling-carrier (UTC) photodiode has an undepleted p-type InGaAs absorber and a transparent, depleted InP drift layer [13], [14], as shown in Figure 2.4c. This type of photodiode can be operated at high output power while maintaining high bandwidth. The outstanding performance of the UTC PD comes from three aspects: first, the electrons are the only carriers that travel in the drift region, which significantly suppresses the space charge effect and increases the bandwidth; second, electrons have higher saturation velocity in InP than in InGaAs; third, the wide bandgap InP introduces less dark current and is less susceptible to thermal failure under high electrical fields. However, there is a tradeoff in the thickness of the undepleted absorber: in order to achieve high responsivity, the layer needs to be thick; which, eventually, limits the bandwidth due to the long electron diffusion time.

2.2.4 Modified Uni-Traveling-Carrier (MUTC) Photodiodes

Charge-compensated modified uni-traveling-carrier (MUTC) photodiodes are developed by combining the structure of the PDA and the UTC photodiodes [15]. The absorber of the MUTC PD consists of undepleted p-type and depleted InGaAs layers. A wide bandgap depleted InP layer serves as the drift region, as shown in Figure 2.4d. Due to the fact that the intrinsic InGaAs layer is thin, the space charge effect is greatly mitigated. The depleted drift InP region can reduce the capacitance and help electrons travel at saturation velocity. The thickness of the undepleted absorber, depleted absorber and drift layer can be separately engineered, which offers multiple degrees of freedom for device optimization.

2.3 Silicon Photonics

Silicon photonics, as a promising enabler for low-cost and high-performance photonic devices with potential deployment in next generation data centers and many other applications, including analog optical links, has attracted vast research and funding during the past decade. Concomitant with the rapid progress in silicon photonics research, silicon-based heterogeneous photonic components, such as lasers [16], electro-absorption modulators [17], optical amplifiers [18] and photodiodes are developed and brought to a high-performance level recently.

The motivation for silicon photonics mainly comes from three aspects [19]: first, silicon photonics can exploit well established silicon IC fabrication facilities, which can bring the unit manufacturing cost greatly down through the economy of scale and allow for photonic-electronic integration. Second, the availability of high-quality and low-cost silicon-on-insulator (SOI) wafers that are an ideal platform to formulate optical circuits at telecommunication wavelength (1550 nm), due to their transparency over a large wavelength range and high contrast of refractive index between silicon (n=3.5) and SiO2 (n=1.5).

The high index contrast enables a compact circuit footprint by supporting well confined optical modes in SOI waveguides. Third, other than transparency, silicon possesses desirable properties, such as high thermal conductivity, high optical damage threshold and high third-order optical nonlinearities, which enable nonlinear optics functionalities.

However, due to the fact that silicon is transparent at telecommunication wavelengths (Figure 2.1) and its indirect bandgap, it is challenging to achieve active devices, such as lasers and photodiodes. Also, unlike group III-V materials there are no lattice-matched compounds available. To enable long-wavelength photodiodes on silicon, several methods have been developed to overcome this inherent drawback, including ion-implanted silicon [20], III-V material direct growth on Si [21] [22], polycrystalline Ge films [23] [24], Si-Ge hetero-epitaxy growth [25] [26], and III-V material on SOI wafer bonding [27] [28]. Si-Ge hetero-epitaxy growth has the advantages of compatibility with standard CMOS processing and cost-efficiency. This approach has led to high-speed photodiodes with 70 GHz bandwidth and 1 A/W responsivity at -1 V [29]. However, their drawbacks are significant: relatively high dark currents due to lattice mismatch between Ge and Si, and low responsivity beyond 1550 nm [26]. In addition, Ge PDs lack the degree of freedom of complex bandgap engineering that is available in group III-V materials. Also, the output power level of Ge PD is significantly lower than heterogeneously integrated III-V on SOI PD as shown in this dissertation. In [30], the bandwidth of a Ge PD is doubled from 30 GHz to 60 GHz using inductive peaking technique. In [31], 200 mm wafer scale selective growth butt-coupling Ge PD with over 50 GHz bandwidth and 0.78 A/W responsivity is demonstrated.

2.4 Integration Techniques

Heterogeneous integration means joining two (or multiple) different materials on a wafer/die scale. Hybrid integration means integrating two (or multiple) fabricated devices onto a platform at the device level. Heterogeneous silicon photonics holds a lot of promise for analog and digital applications that

require high-performance photonic components. In the following, I give a brief overview of hybrid and heterogeneous integration technologies of photonic devices that have been reported in the literature.

2.4.1 Hybrid Integration Using Metal-Metal Bonds

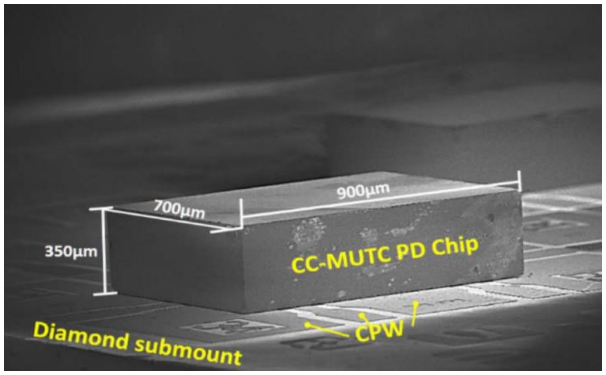


Figure 2.5 InP-based photodiode die chip flip-chip bonded onto a diamond substrate

Hybrid integration by flip-chip bonding has been around for quite a long time. It is a widely used technique in electronics and photonics. In the CMOS industry, finished semiconductor chips are picked and placed to the desired position on the circuit board [32]. Heat and force can be applied to the metal-metal (e.g. gold) bonding interface. Under the bonding condition, solder bumps will join the chip and bonding pad on the board together. Metal-metal bonds provide good mechanical support, heat sink and electrical connection. In photonics, flip-chip bonding can be used to create mechanical support and electrical contacts [33], similar to its application in CMOS.

In our group, we have developed back-illuminated InP-based photodiodes flip-chip bonded onto a coplanar waveguide (CPW) on diamond substrate (Figure 2.5) [33] for mechanical support, heat sinking and RF connection. These devices achieved record-high power dissipation, and saturation current as well as high bandwidth [33] [34]. A balanced waveguide photodiode chip mounted to a silicon-on-insulator (SOI) waveguide platform has been demonstrated in ref. [35] (Figure 2.6). In the latter, an accurate

alignment and low loss optical coupling between the SOI waveguide and the native InP waveguide on the photodiode chip were achieved [35].

Flip-chip bonding offers multiple advantages, such as mature process apparatus, high performance electrical connection and excellent heat sink. Also, cost can be reduced by only bonding tested functional devices. However, several challenges exist. First, flip-chip bonding requires precise alignment, which makes the integration process time- and labor-consuming. In photonics, this problem is exacerbated, especially when single-mode waveguides or fibers are involved. As the alignment tolerances can be as tight as a few hundred nanometers, even small misalignment can deteriorate the optical coupling efficiency significantly. Second, integration density can be limited by the minimum pitch separation imposed by the flip-chip bonder.

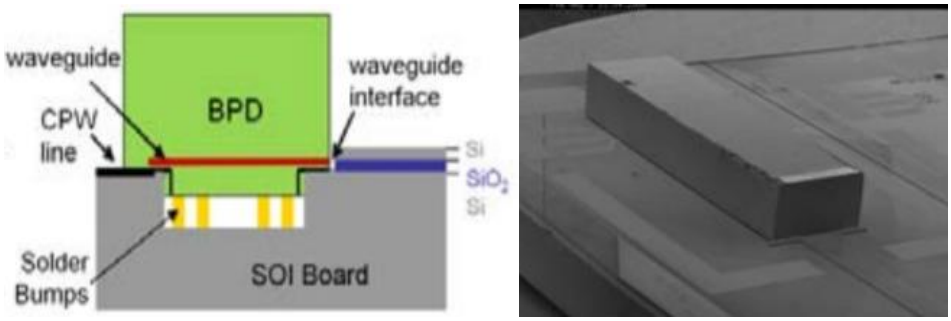


Figure 2.6 InP-based photodiode die chip flip-chip bonded onto a SOI waveguide [35]

2.4.2 Direct Epitaxial Growth of III-V Material on Si

For direct epitaxial growth, due to the crystal defects introduced by the large lattice mismatch between most group III-V materials and silicon, the crystal quality of the III-V semiconductor is usually unacceptable [36] for high performance photonic devices. One solution to mitigate the poor crystal quality is to deposit a thick buffer layer [22] onto the silicon substrate first, and then grow the III-V device layers on top of the buffer layer. However, the thick buffer layer may deteriorate the optical

coupling between the underlying SOI waveguide and the III-V active device on top. Thus, the coupling efficiency and responsivity performance are degraded. One straightforward way to solve the efficiency degradation for photodiodes is to grow the III-V material into recess regions on the wafer and butt-couple to the optical waveguide [37]. Direct epitaxial III-V on Si is the most cost-efficient solution; however, other than material quality issue, thermal expansion mismatch between III-V and Si also imposes a limitation on its high power performance [38].

2.4.3 Molecular Bonding

For evanescently coupled waveguide photodiodes [39], the coupling efficiency is greatly improved by employing ultra-thin bonding layers to integrate III-V semiconductors onto the SOI platform. In addition, the lattice mismatch can be compensated without any buffer layers. In molecular bonding, before the two wafers are brought into contact and go through low-temperature (<400 ˚C) annealing, both surfaces of the III-V and SOI are first thoroughly cleaned, and then, an O_2 plasma is applied as surface activation. High performance photonic devices, such as lasers [40], modulators [41] and photodiodes [42], have been demonstrated to be integrated onto silicon photonics platform using the molecular bonding approach. Recently, it was shown that heterogeneously integrated III-V photonic devices on silicon can outperform their counterparts on native substrate [43]. In ref. [44], it was reported that InP-based modified uni-traveling carrier (MUTC) photodiodes (PDs) on silicon-on-insulator (SOI) waveguides achieved record-high RF output power levels of 12 dBm at 40 GHz. Recently, InP-based III-V pin photodiodes heterogeneously integrated on SOI were demonstrated to operate at 70 GHz with -8 dBm RF output power [45].

2.4.4 Adhesive Bonding

In adhesive bonding, a thin layer of polymer (<1 μm) is used as the bonding intermediate to join the two wafers together. Due to the presence of the polymer bonding intermedia, surface cleanliness and smoothness requirements are eased. Dust particles no taller than the thickness of the bonding polymer can be tolerated. High performance photonic devices have been developed by adhesive bonding ranging from lasers, modulators to photodetectors [46] [47] [48]. Table 2.1 shows a comparison between the two bonding techniques [40]. The common weaknesses of molecular bonding and adhesive bonding include high thermal impedance of the SOI substrate and high manufacturing cost [38].

Bonding characteristic	Molecule bonding	Adhesive bonding
Bonding strength (<400 °C)	High	High
Process complexity	Medium	Low
Tolerance to surface defects, roughness and contamination	Low	High–medium
Bonding-induced strain	Low	Low
Integration proximity	High	High–medium
Intrinsic outgassing problem	High	Low
Uniformity	High	High–medium
Stability	High	High
Scalability	High	High

Table 2.1 Comparison of molecular bonding and adhesive bonding adopted from ref. [40]

2.5 Optical Coupling Mechanisms in Heterogeneously Integrated Photodiodes on SOI

Coupling signal light from the SOI optical waveguide into the III-V absorber is one of the critical problems that researchers have to resolve. As shown in Figure 2.7 [49], five coupling mechanisms have been demonstrated recently: a) evanescent coupling; b) adiabatic coupling; c) grating-assisted vertical coupling; d) 45˚ mirror; e) butt coupling.

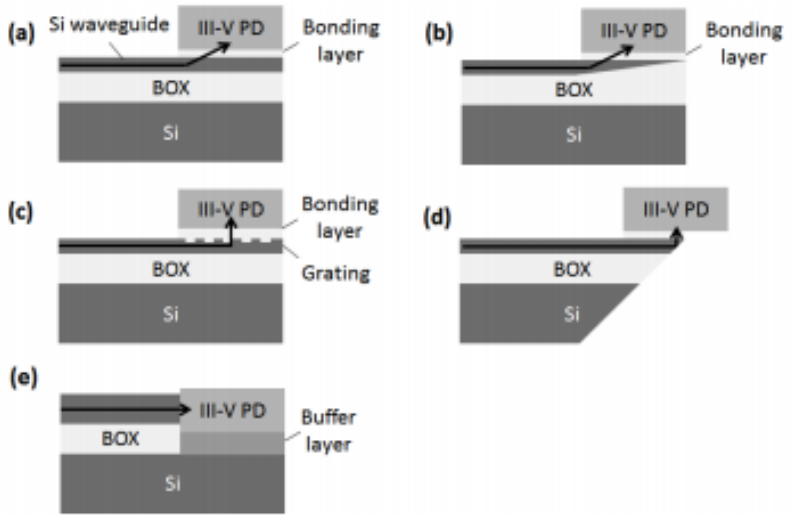


Figure 2.7 Coupling schemes (a) evanescent coupling; (b) adiabatic coupling; (c) grating-assisted vertical coupling; (d) 45˚ mirror coupling; (e) butt coupling (figures adopted from ref. [49])

2.5.1 Evanescent Coupling

Evanescent coupling exploits the proximity between the optical waveguide and the photodiode absorber. As the beam propagates in the optical waveguide, a portion of the evanescent field extends into and overlaps with the absorber. As a result, optical power gets absorbed by the absorber. In [44], an evanescently-coupled photodiode with low dark current of 10 nA at 5 V and responsivity of 0.64 A/W at 1.55 µm was demonstrated. The III-V epitaxy layer was first grown on InP substrate, and then transferred onto patterned SOI waveguide platform by a low temperature oxygen plasma assisted

molecular bonding technology. Further, in [50], it was demonstrated that two different III-V epitaxy layers can be wafer bonded onto a single SOI waveguide platform; an AlInGaAs MQW laser and an InGaAs photodiode were realized on a single SOI chip. In [29], an evanescently coupled germanium pin photodiode was demonstrated to reach 70 GHz with 0.84 A/W responsivity at -1 V. The germanium absorber was selectively deposited within a recess hole to facilitate coupling to the optical waveguide.

2.5.2 Adiabatic Coupling

In this approach a lateral adiabatic waveguide taper acts as an optical mode converter, which converts the optical mode in the waveguide to the mode in the III-V absorber as the beam propagates beneath the photodiode active region. It was shown in [51] that a photodiode with an active area of 4 x 30 μm^2 can achieve a responsivity and bandwidth of 0.36 A/W and 30 GHz, respectively. The III-V epitaxy layers were transferred onto a Si_3N_4 waveguide platform using plasmas-assisted molecular wafer bonding technology similar to the bonding technology in [42].

2.5.3 Grating-Assisted Vertical Coupling

In [52], it was demonstrated that by using a grating coupler, which was patterned at the end of the SOI optical waveguide, light can be diffracted into the III-V absorber. The InP-based epitaxy structure was bonded onto the patterned SOI waveguide platform by an adhesion bonding technology [53]. In the adhesion bonding process, benzocyclobutene (BCB) was used as the bonding media. Due to the nature of the thick bonding layer (~ 3 μm), the requirements for surface smoothness and cleanliness (potential dust particles between the two bonded wafers) were greatly relaxed, compared to those of intimate direct bonding. In [54], a photodiode with a dark current at -1 V and responsivity at 2.2 μm of 4 μA and 0.4 A/W was reported.

2.5.4 45˚ Mirror

By placing the photodiode chip on the edge of an SOI waveguide with a polished 45˚ mirror, light can be redirected from the horizontal optical waveguide into the III-V die which lies above the mirror. This concept was demonstrated in [55]; the photodiode achieved a bandwidth of 28 GHz.

2.5.5 Butt Coupling

In [56], Geng et al. employed selective-area metal organic chemical vapor deposition (MOCVD) to deposit III-V layers into a recess at the end of an optical waveguide. The III-V epitaxy device layers were directly grown on a 2.6 μm-thick InP/GaAs buffer on top of the Si substrate. The dark current was 130 nA at -1 V and the bandwidth was 15 GHz at -5 V. It has been demonstrated that a UTC waveguide photodiode on its native (InP) membrane waveguide platform can reach a high bandwidth up to 67 GHz with high responsivity of 0.7 A/W at 1550 nm [57]. In [57], the UTC photodiode was butt-coupled to an InP membrane waveguide. Both the InP membrane waveguide and the UTC photodiode were integrated onto Si on top of a 2-μm-thick benzocyclobutene (BCB) bonding layer.

In comparing the different optical coupling schemes, it is found that the presence of a grating coupler unavoidably introduces manufacturing complexity in the fabrication of the sub-wavelength gratings. In addition, the limited grating coupler efficiency and the low photodiode responsivity are also disadvantages for grating coupler scheme. Integration of a 45˚ mirror coupling requires extra processing steps for mirror polishing and device die pick-and-place. For butt coupling with direct epitaxy III-V growth, an excellent material quality is needed to avoid defects originating from lattice mismatch and that lead to device performance degradation and excess loss [38]. To avoid the drawbacks from those coupling schemes, I chose adiabatic-taper-assisted evanescent coupling in this work. A die-to-wafer-scale molecular-bonding approach is used to bond the III-V material onto the SOI waveguide platform.

Chapter 3 Photodiode Fabrication Process, Characterization Techniques and Simulation Software

In this chapter, I describe the fabrication process of heterogeneously integrated photodiodes using molecular bonding techniques, the characterization techniques used in measuring device performance and simulation software. In addition, SU8-bonded surface-normal photodiodes were fabricated and characterized using the same techniques described here.

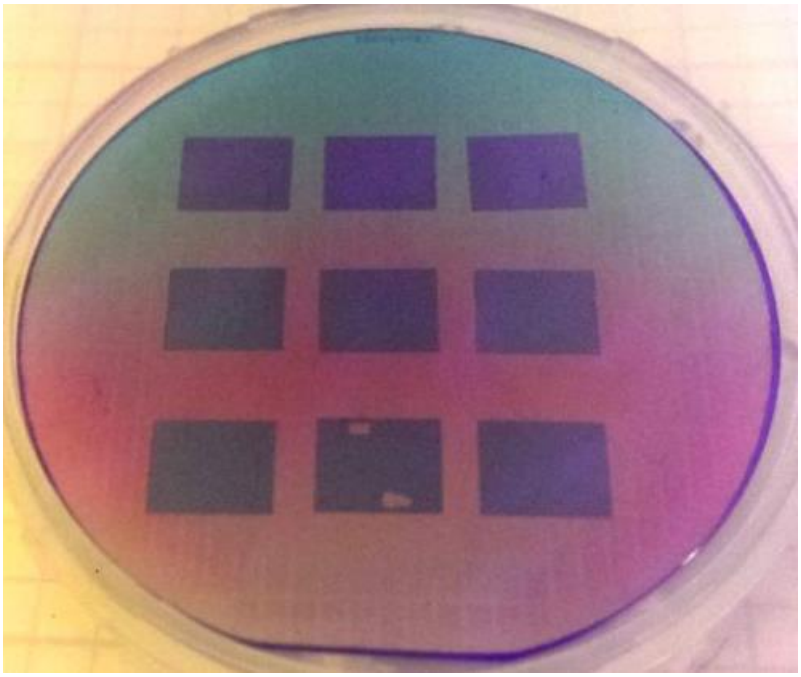


Figure 3.1 SOI wafer with nine III-V epi dies after bonding

3.1 Fabrication Process

The fabrication process starts with forming the optical waveguides on the SOI wafer through dry etching. Then, nine 12 mm x 10 mm III-V epitaxial dies (MUTC8, Figure A.II.2, see Appendix II) were bonded onto a 3'' SOI wafer (Figure 3.1). This bonding process consists of initial die clean, oxygen

activation, silicon dioxide deposition and thermal compression bonding. The wafer etching, bonding processes and substrate removal were conducted in collaboration with Aurrion. Further details of the wafer bonding process can be found in [39].

After the bonding process, I first separated the bonded dies using a dicing saw and then fabricated photodiodes using the microfabrication facility at the University of Virginia. A fabrication recipe is attached in Appendix I.

3.1.1 Fabrication Process Flow

In summary, the fabrication process flow consists of the following steps:

1) Waveguide etch
2) Wafer bonding
3) Substrate removal
4) P-metal deposition
5) Formation of P-mesa (Figure 3.2a)
6) Formation of N-mesa
7) N-metal deposition
8) P-contact open
9) SU8 insulation pad forming
10) Seed metal layer deposition (Figure 3.2b)
11) Gold electro-plating and lift-off (Figure 3.2c)
12) Dicing
13) Edge polishing

Except for steps 1, 2, 3 and 13, I carried out all fabrication steps in the UVA cleanroom facility.

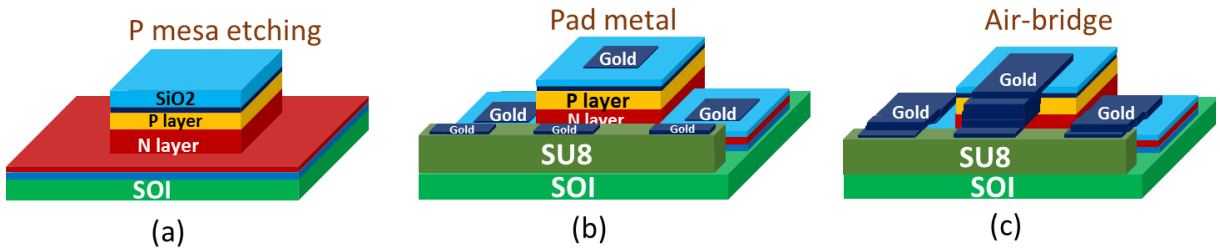


Figure 3.2 Fabrication process schematic

3.1.2 Metal Deposition and Lift-Off

Metal is deposited for the purpose of either contact metallization or the seed layer for gold electro-plating. For the p-contact metallization, the stack of metals consists of 200 Å Ti, 300 Å Pt, 500 Å Au and 100 Å Ti. Similarly, the n-contact metal is a stack of: 200 Å Ti, 300 Å AuGe, 800 Å Au and 300 Å Ni. The metal stacks are designed to achieve low ohmic contact resistance between the semiconductor layers and metal, while maintaining good adhesion. For the seed layer, two layers of metal, 150 Å Ti and 500 Å Au, are used to metallize the entire die surface for subsequent electro-plating.

Before the metal deposition, the sample needs to go through an oxygen plasma cleaning process for thorough photoresist removal. Otherwise, metal may be deposited onto residual photoresist, causing high and random contact resistance. I used electron beam (e-beam) evaporation for metal deposition. Since the e-beam evaporator deposits metal non-selectively, the metal pattern is defined by photolithography in a previous step.

For the following lift-off process, both acetone and N-Methyl-2-pyrrolidone (NMP) can be used to soak the sample for photoresist dissolution. With the help of an ultra-sonic bath, the unwanted metal on top of photoresist can be removed as the underlying photoresist gets dissolved. The power of the ultra-

sonic vibration should be kept as low as possible (normally < 60 units) to prevent damage to the structures on the sample.

3.1.3 SiO_2 Deposition and Removal

SiO_2 is deposited as the hard mask and for mesa side wall passivation. Other than these two functions, the SiO_2 thin film can also function as an anti-reflecting (AR) coating. In the microfabrication facility at UVA, I used a plasma enhanced chemical vapor deposition (PECVD) apparatus to deposit SiO_2 onto my samples. The process requires 400 sccm SiH_4 and 105 sccm NO gas reaction under low pressure and 285 ˚C heating condition. I used a small piece of a Si wafer to monitor the deposited SiO_2 thickness. This Si dummy was placed next to the sample die in the reaction chamber. By measuring the thickness of the SiO_2 on the Si dummy and assuming that the deposition rate is uniform in the chamber, I determined the SiO_2 thickness deposited on the sample. I used a Filmetrics spectral reflectance setup to measure the SiO_2 thickness. The deposition rate was found to be ~ 10 nm/min.

Both wet chemical etching and inductively coupled plasma (ICP) dry etching can be used to remove SiO_2. For wet chemical etching, buffered oxide etchant (BOE, HF) is typically used. Similar to wet chemical mesa etching, BOE SiO_2 etching also results in lateral undercut that may cause problems when the pattern feature is small. A typical etching rate is ~ 120 nm/min for 10:1 BOE. ICP dry etching can be used to remove SiO_2 as well. The dry etching recipe is CHF_3 (25 sccm) with 150 W RF power at 20 ˚C. A typical etch rate is ~20 nm/min.

3.1.4 Mesa Etching

Both P-mesa and N-mesa are patterned by etching. During the P-mesa etching, the active photodiode mesa is formed. During N-mesa etching, the highly doped n-contact layer is mostly removed. As a result, the photodiodes on the wafer are isolated. Prior to the mesa etching, a layer of SiO_2 is

deposited as an etching hard mask and mesa-side-wall surface passivation during the second SiO_2 hard masking process. Photolithography is then used to define the patterns of the P-mesa and N-mesa into the SiO_2 hard mask by Oxford RIE-ICP dry etching. Then, these patterns are transferred into the semiconductor through the mesa etching step.

I used two types of etching techniques in my work: wet chemical etching and inductively coupled plasma (ICP) etching (dry etching). The etch depth was measured by an Alpha profilometer.

I used an Oxford brand RIE-ICP system for dry etching. The dry etch recipe is Cl_2 (8 sccm): N_2 (20 sccm) with 300 W RF power at 50 ˚C. I determined the rate in InGaAs and InP to be ~ 150 nm/min. Since during the dry etching the hard mask will be attacked as well, a sufficiently thick SiO_2 hard mask is necessary. The etching selectivity of SiO_2 and the III-V material is observed to be ~1:3.

Wet chemical etching can create smooth side walls and low dark current, but due to its isotropic nature, the lateral undercut of the mesa can be significant when the diameter of the mesa is small. In contrast, dry etching is highly directional and anisotropic. However, the mesa side walls can be rough and damaged, which may result in a relatively high leakage current. Ideally, a combination of dry and wet etch is preferred.

Details of the wet chemical etching solutions that I used, such as selectivity and rates, can be found in [58]. The acid solution H_3PO_3: HCL (in volume 3:1) can etch InP at ~1000nm/min, and it has good selectivity, i.e. does not etch, InGaAs and InGaAsP. This property is critical because I used a very thin layer (50 nm) of InGaAsP as a P-mesa stop. During P-mesa etching, the first 1560 nm out of 1974 nm total depth was removed by the dry etch, the remaining etching portion was etched by H_3PO_4: HCL (3:1).

3.1.5 Gold Electro-Plating

I use gold electro-plating to form the coplanar waveguide (CPW) and air bridges. First, the sample die is patterned by the seed layer photolithography step. Only areas where the metal should be physically contacted and supported by underneath materials are exposed, everything else is covered by photoresist. It is worthwhile to point out that a long (> 10 mins) post-exposure bake at 110 ˚C is essential. This post-exposure bake can vaporize and dry out moisture in the photoresist which otherwise may cause bubbling issues in the following lithography process. After the seed layer lithography, the seed layer metal (150 Å Ti and 500 Å Au) is deposited. A second photolithography step patterns the sample die with the plating layer. The idea is to sandwich the unwanted seed metal with photoresist for lift-off, while the open patterns will be electro-plated. Before the e-beam metal deposition, a short (300 seconds) oxygen plasma cleaning (150 W RF power) is needed to fully remove photoresist on exposed regions.

The sample die is then electro-plated in a bath of gold plating solution (Technic Inc.) at 50 ˚C. The electro-plating rate depends on many factors, such as sample die area, contact resistance between plating needle and sample die. Generally, the plating current should not exceed 1 mA, otherwise the plating rate may be too fast and cause roughness issues and gold overflow. The plating voltage should be ~ 0.5 V. It is highly advised to check plated gold thickness frequently (every 5 mins).

After plating, the unwanted seed metal is removed by lift-off. Both acetone and NMP solution can be used to dissolve the photoresist, but NMP is preferred, as it results in a better lift-off rate. I used an ultrasonic bath to facilitate the lift-off process. I kept the ultrasonic power below 60 W (units) to avoid damaging the suspended metal air-bridge.

3.1.6 Additional Processing

After gold electro-plating and lift-off, the sample needs to be diced. Before dicing, a thin layer of photoresist is spun onto the sample for protection during the dicing process. Then the sample is mounted onto the dicing carrier using melted white wax. Dicing was carried out with a semi-auto Disco dicing saw, DAD 3220.

In order to reduce the optical coupling loss from rough facet scattering, the diced chips were sent out to Brand Laser & Optics Inc. for edge facet polishing.

3.2 Characterization Techniques

3.2.1 Current-Voltage (I-V) and Capacitance –Voltage (C-V)

The DC current-voltage (I-V) measurement is conducted with a DC probe needle station and an HP4145B semiconductor parameter analyzer. The dark current of heterogeneously integrated SOI MUTC8 waveguide photodiodes is normally in the range of 1 nA to 10 nA at 3 V reverse bias. For SU8-bonded MUTC4 photodiodes on silicon, typical values of the dark current are from 8 nA to 1 μA, depending on device area. A high current level (1 mA) under low forward bias voltage (0.5 V) is an indicator of low series resistance, which is typically in the range of 1 to 5 Ω.

The same DC probe station and an HP 4275A LCR meter are used to measure the photodiode capacitance at different bias conditions (C-V). The pn junction capacitance scales with device size. In order to reach a high 3-dB bandwidth, a low junction capacitance and low parasitic capacitance are desired. Typical values of measured device capacitance are on the order of femtofarad (fF).

3.2.2 Responsivity and Quantum Efficiency

As described in chapter 2, the quantum efficiency and responsivity are two important figures of merit that quantify how efficiently a photodiode converts photons into electron-hole pairs. To determine the quantum efficiency and responsivity I measured the photocurrent for a given optical input power and used the following equations:

$$\eta = R\frac{1.24}{\lambda[\mu m]} \qquad \textit{Equation 3-1}$$

and

$$R = \frac{I_{pd}}{P_{Optical}}. \qquad \textit{Equation 3-2}$$

More specifically, to predict responsivity from a top-illuminated photodiode with exponential absorption the following equation can be used:

$$R = \eta_{ext} * R_{ideal} = R_{ideal} * \left(1 - R_{surface}\right) * \left(1 - e^{-\alpha d_{abs}}\right) \qquad \textit{Equation 3-3}$$

where α is the absorption constant, d_{abs} is the absorber thickness, $R_{surface}$ is the surface reflectance and R_{ideal} is the responsivity when all injected photons are absorbed and all carrier are extracted.

Similarly, to estimate the external responsivity of a waveguide evanescently-coupled photodiode, the following equation can be used [8]:

$$R = R_{ideal}\left(1 - R_{reflection}\right)\eta_c\left[1 - exp\left(-\alpha\int_0^{l_{abs}}\Gamma_{xy}(z,l)dz\right)\right] \qquad \textit{Equation 3-4}$$

where α is the absorption constant, η_c is the input coupling efficiency, $R_{reflection}$ is the reflectance at the optical input facet, l_{abs} is the length of the absorber and Γ_{xy} is optical confinement factor in the absorber describing what fraction of the optical input power is confined within the absorber. Due to the finite absorption length, surface reflection and input coupling loss (η_c), the measured responsivity (R) is always lower than the ideal responsivity.

3.2.3 RF Response Measurement

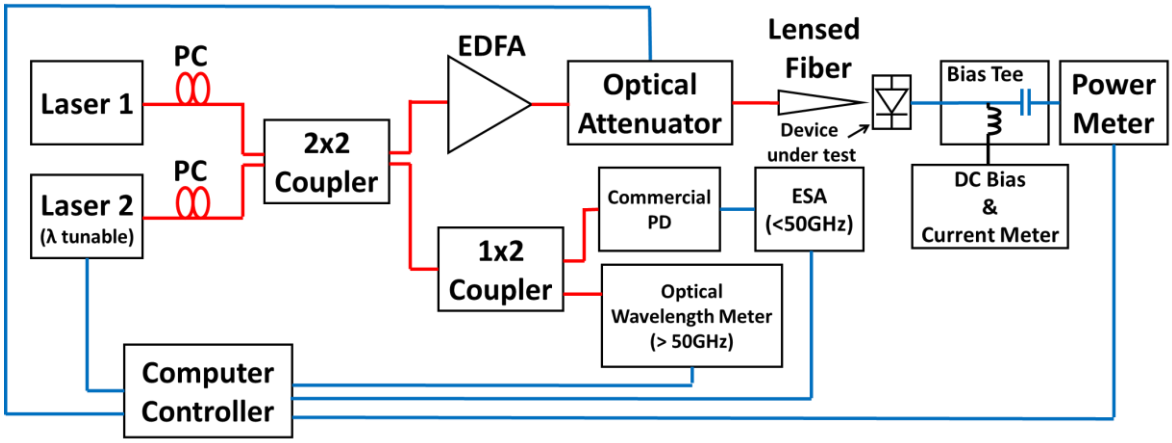


Figure 3.3 Optical heterodyne setup. PC: polarization control, ESA: electrical spectrum analyzer

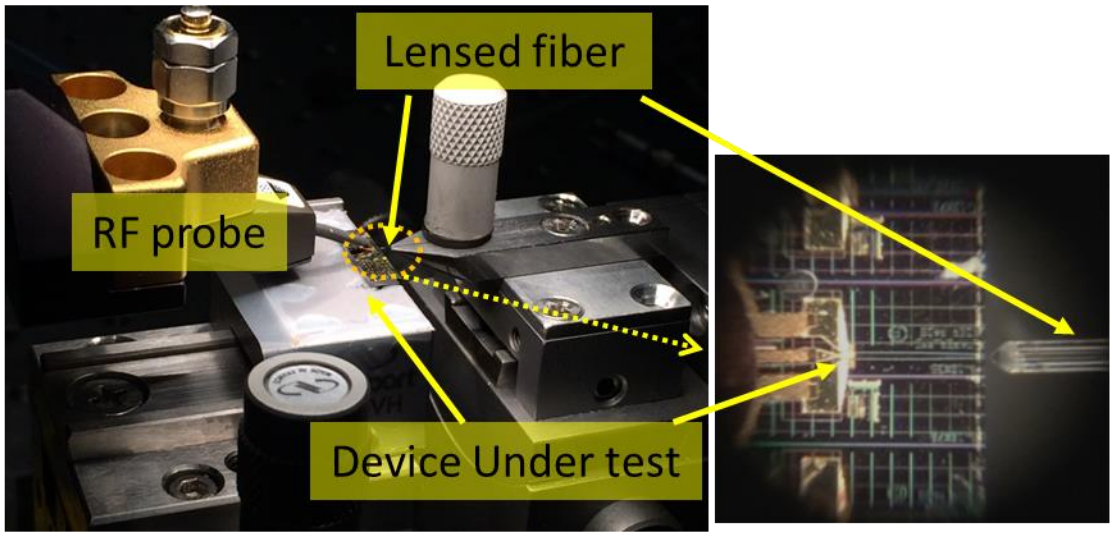


Figure 3.4 Waveguide photodiode measurement setup

Figure 3.3 shows a block diagram of the optical heterodyne setup that I used to characterize the frequency response of the photodiodes. Two distributed-feedback (DFB) lasers with slightly different wavelengths were used to generate a tunable RF signal through optical beating. The output signals of the two DFB lasers are centered near 1544 nm wavelength. The RF beat signal is generated by combining the two lasers using a fiber directional coupler. The frequency of the RF beat signal can be

swept by thermally tuning the wavelength of one DFB laser. In order to achieve 100% modulation depth, the output optical powers and the polarization of the two DFB lasers need to be matched. For an RF frequency range less than 50 GHz, a commercial photodiode and a RF spectrum analyzer are used to measure the RF frequency. For frequencies beyond 50 GHz, an optical wavelength meter is used instead, to provide the frequency information to the Labview program. The second output of a fiber directional coupler is amplified by an EDFA and attenuated by a programmable optical attenuator. Then, the light is fed into the photodiode waveguide through a lensed fiber. The device is electrically connected by a ground-signal-ground (GSG) CPW on-wafer probe (made by GGB Inc.), bias-tee and RF cable to the RF power meter. The RF probe allows the photodiode to be reverse biased during the measurement. An RF power meter was used to monitor the output power level of the photodiode. The measurements were corrected for the losses originating from the cable and bias tee. Figure 3.4 shows the configuration for on-wafer measurement of waveguide photodiodes.

In order to determine the frequency responses of balanced photodetectors in common mode and differential mode operation, I used a dual-output modulator with π (RF-) phase difference between each of its outputs. The experimental setup is shown in Figure 3.5. A laser with 1550 nm wavelength was used as the optical source. 1% of optical power in the upper branch of the modulator output was tapped out for a DC bias control circuit that maintained the modulator at its quadrature biasing point. A tunable RF generator was used to drive the modulator. The RF responses of the modulator, together with all other RF cables, were calibrated out, in order to acquire the RF response of the device under test. Switching between common mode and differential mode operation was achieved by tuning two free space delay lines. To illuminate both photodiodes in the balanced photodetector simultaneously, I used a 2-channel lensed fiber with 250-μm pitch for optical input coupling. An electrical spectrum analyzer (ESA) was used to determine the RF output power. Photocurrents on both photodiodes were balanced through the alignment between lensed fiber array and SOI waveguides.

3.2.4 Output RF Power

The power delivered from the photodiode to a 50 Ω load resistor is defined as the output RF power. The RF power delivered to the load can be calculated to be

$$P_L[dBm] = 10 \cdot log(\frac{1}{2} {I_{DC}}^2 m R_L / 1mW) \qquad \textit{Equation 3-5}$$

where I_{pd} is the average DC photocurrent, m is the modulation depth, and R_L is the load resistor. The output power at a specific frequency can be measured by an electrical spectrum analyzer or a RF power meter.

3.2.5 Saturation Current

Within the photodiode's unsaturated region, the output RF power increases linearly with input optical power or photocurrent (on a log scale). However, as the input optical power keeps increasing, the RF output power deviates from its linear predicted trajectory, owing to saturation effects. The compression is defined as the deviation of the measured output RF power from its linear behavior measured in dB. The saturation current is defined as the average photocurrent at which the compression drops by 1 dB from its peak value (Figure 3.6). To measure compression and saturation

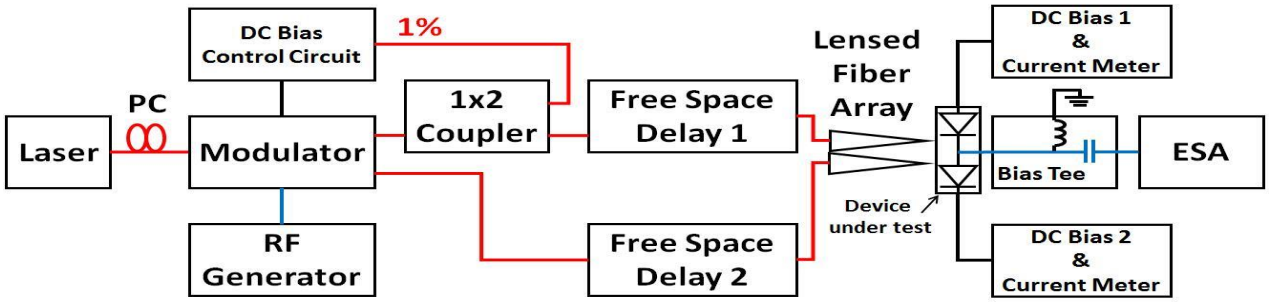


Figure 3.5 Experimental setup for measurements in differential and common mode

current I used the setup in Figure 3.3.

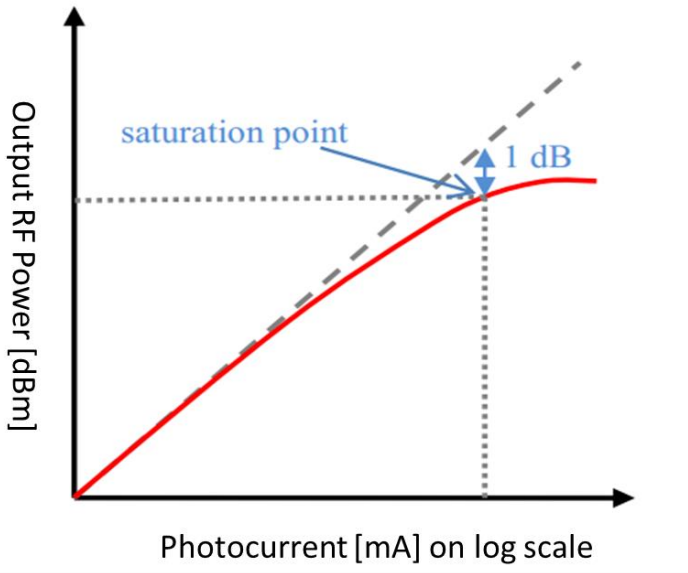


Figure 3.6 Power transfer plot of a photodiode with compression

3.3 Simulation Software

The simulation of the coupling efficiency and photodiode responsivity are carried out using two commercially available software; based on either the beam propagation method or the Eigenmode expansion method. It will be shown in Chapter 8 that the two softwares reach reasonably well matching results.

3.3.1 Beam Propagation Method (BPM)

The beam propagation method is a numerical technique for solving the propagation of a light wave in arbitrary waveguide geometries. The commercial software used in this work is BeamPROP by Rsoft Inc.

[59]. In BeamPROP, the finite difference method computational technique is used to solve the paraxial approximation of the Helmholtz equation:

$$(\nabla^2 + k_0^2 n^2)\psi = 0 \qquad \textit{Equation 3-6}$$

where the electric field is written as,

$$E(x, y, z, t) = \psi(x, y) exp(-j\omega t), \qquad \textit{Equation 3-7}$$

with $k_0 = {}^{2\pi}/_{\lambda}$ being the free space wavenumber, n being the refractive index.

As can be seen from the Helmholtz equation above, the physical propagation problem needs two inputs to be solved:

1. The refractive index spatial distribution
2. The input electric field

After specifying the input parameters, the software, solves the Helmholtz equation and presents the simulation results. Using a paraxial approximation, BPM inherently includes both guided mode and radiating modes, as well as modes coupling and conversion.

To estimate the internal responsivity (R_{int}) the calculation starts with the internal quantum efficiency (η_{z_k}) at slicez_k:

$$d\eta_{z_k} = \alpha_{eff} \Gamma_{z_k} dz_k \qquad \textit{Equation 3-8}$$

where α_{eff} is the effective absorption constant; Γ_{z_k} is the confinement factor at slice z_k, which can be extracted from BeamPROP output files; dz_k is the simulation step distance in the propagation direction.

Then the internal responsivity (R_{int}) is calculated using equation:

$$R_{int} = R_{ideal} * \int_0^{L_{pd}} d\eta_{z_k} \approx R_{ideal} * \sum_{z_k=0}^{L_{pd}} d\eta_{z_k} \qquad \textit{Equation 3-9}$$

3.3.2 Eigenmode Expansion (EME)

Any solution of Maxwell's equations within a given simulation region and boundary condition can be expressed by an expansion of eigenmodes (Figure 3.7):

$$\Psi(x,y,z) = \sum_{i=1}^{N}\left(C_i^f \Psi_i(x,y)e^{i\beta_i z} + C_i^b \Psi_i(x,y)e^{-i\beta_i z}\right) \qquad \textit{Equation 3-10}$$

where $\{C_i^f, C_i^b\}$ are the forward and backward field coefficient.

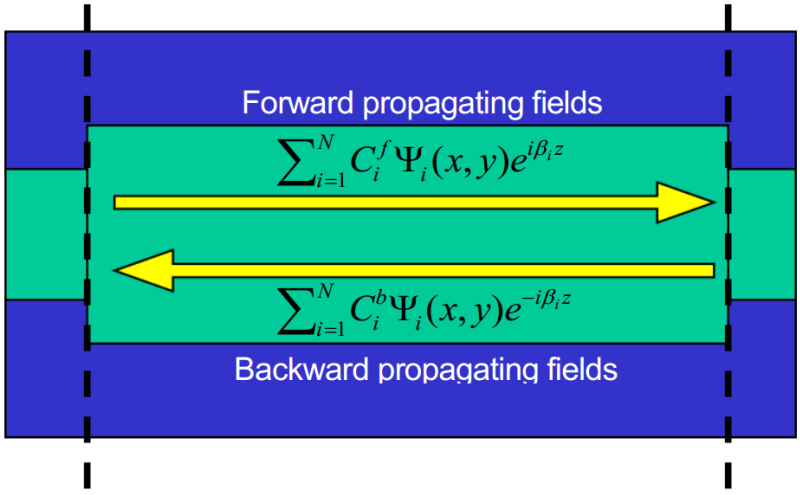


Figure 3.7 Field in a waveguide expressed by eigenmode expansion [83]

The software used in this work, FIMMWAVE, is based on this principle. When multiple waveguides of different cross sections are joined together as an optical device, FIMMWAVE calculates the solution of Maxwell's equation within each section and expresses them in the format of an expansion of eigenmodes. Then, the joint scattering matrix is calculated by integrating the overlap between the eigenmodes of neighboring sections. By cascading the scattering matrix of each section and joint, a complete scattering matrix of the device can be acquired. Compared to BPM, there is no computational error accumulation within each section, regardless of its length. The only source of accumulative error

comes from the joint scattering matrix, due to numerical eigenmode sets overlap integral. In addition, the number of eigenmodes, N, should be selected properly. If N is too small, some eigenmodes carrying significant energy may not be included in the computation, and leading to errors in the simulation. On the other hand, if N is too large, the simulation efficiency suffers.

Chapter 4 Heterogeneously Integrated Single Photodiode

4.1 Introduction

In this chapter, I present high-speed high-power single MUTC PDs that are heterogeneously integrated onto SOI nano-waveguides using wafer bonding. Single photodiodes reach -2 dBm RF output power at 70 GHz which is the highest RF output power that has been reported for waveguide photodiodes on SOI waveguide above 50 GHz. One of my goals was to demonstrate a structure that is fully compatible with the heterogeneous integration process that was presented in [60]. To this end, and unlike our earlier work in [44], an inverted PD layer structure is used that results in the p-contact being on top after wafer bonding. It should be mentioned that this structure has the potential to further enhance the high-power performance since heat dissipation from the depletion layer into the silicon is

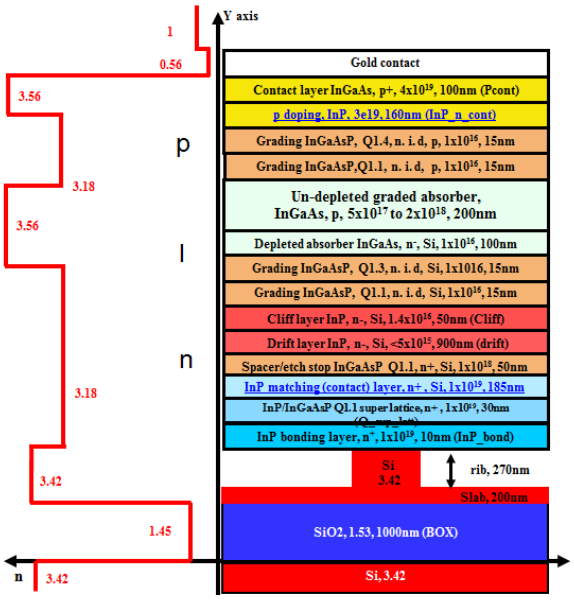


Figure 4.1 Cross section view of refractive index of the waveguide photodiode

not hindered by the low-thermal conductivity InGaAs. As a result, higher bias voltage can be applied to increase saturation current and reduce nonlinear effects, e.g. carrier pile-up at heterojunction interfaces, or electric field collapse in drift layer. The sheet resistance in the lower contact can be minimized by high doping levels (>1e19/cm^3) that are possible in InP, which leads to reduced transient voltage drop and current crowding, as well as improved bandwidth and saturation current. Figure 4.1 shows a cross sectional view of the refractive indices of the waveguide photodiode with top p-contact. It can be seen that the transparent low-index InP drift layer (3.18) is between the high index InGaAs absorber (3.56) and the high index Si waveguide (3.42). As a result, conventional evanescent coupling from the waveguide into the absorber is not efficient because the evanescent field does not penetrate far enough into the low index material. The solution is to use a tapered nano-waveguide underneath the photodiode. I designed the width of the silicon waveguide underneath the photodiode to be 300 nm in order to enhance optical coupling from the waveguide into the absorber. This was made possible by the heterogeneous process that allows us to optimize the widths of the underlying silicon waveguide and photodiode mesa independently [42].

4.2 Device Design and Fabrication

Figure 4.2a shows the layer structure of the MUTC PD on SOI [42]. The light couples evanescently into the InGaAs absorber from the underlying waveguide, which consists of a 1 μm-thick buried oxide layer and a 470 nm-thick silicon waveguide. One of the keys to heterogeneous integration processing is to match the topography of different components on the same die, thus an extra 500 nm-thick p-type InP layer was added beneath the p-contact layer to match overall epitaxy thickness with other III-V components, such as modulators or lasers, to enable future integration. The absorption layer is composed of 100 nm lightly n-doped depleted and 200 nm un-depleted material. Bandgap-graded quaternary layers are designed to reduce the bandgap discontinuity at the heterojunction interface

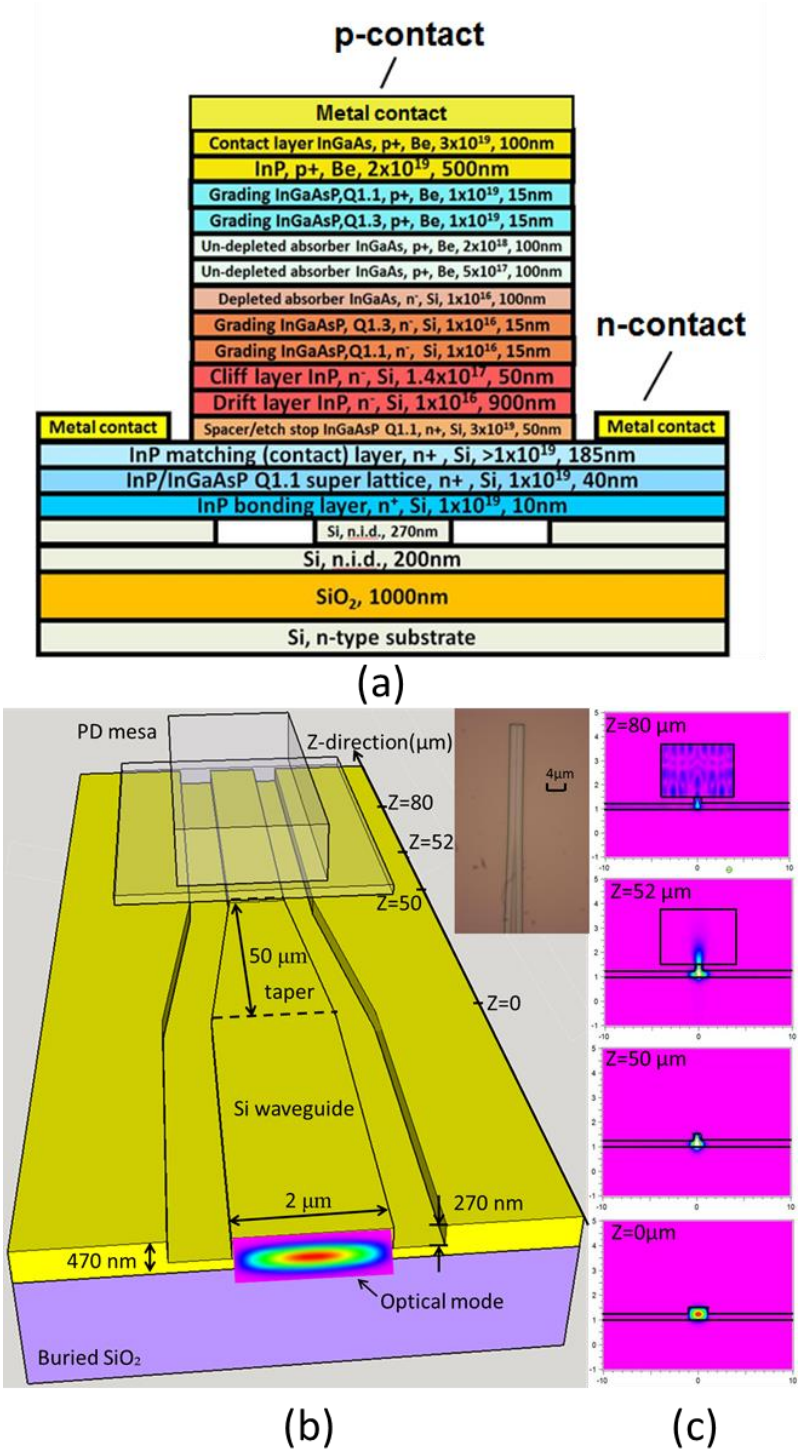


Figure 4.2 (a) Layer structure of heterogeneous MUTC PD with top p-contact. The doping concentrations are given in cm^{-3}. (b) Schematic view of the photodiode. Inset: Picture of nano-waveguide before wafer bonding. (c) Optical intensity at different z-position in the direction of light propagation simulated with commercial beam propagation software

between the InP and InGaAs layers. To achieve high saturation current the layer structure includes a 50

nm-thick n-type InP layer to ensure a sufficiently high electric field between the InP drift layer and the InGaAsP grading layer [61]. To reduce the junction capacitance and thus increase the RC-bandwidth limitation I designed a 900 nm-thick lightly n-doped InP electron drift layer. A 40 nm-thick InP/InGaAsP super-lattice and a 10 nm-thick InP bonding layer are used to reduce the propagation of crystal defects into the active region and act as the bonding interface, respectively. The structure was grown on s.i. InP substrate by molecular beam epitaxy (InPact) and by metal-organic chemical vapor deposition (Landmark).

To achieve efficient coupling from the waveguide through the 900 nm-thick low-index InP layer into the absorber I designed the width of the silicon rib waveguide underneath the absorber to be 300 nm. Hence, the optical mode in the silicon waveguide becomes less confined and is pushed upward into the photodiode [42]. Figure 4.2b shows a schematic of the waveguide photodiode. On the input side the width of the Si waveguide is 2 µm and tapers down to 300 nm before entering the photodiode mesa. The inset of Figure 4.2b shows the nano-waveguide before wafer bonding. Figure 4.2c shows the simulated optical intensity distribution at different positions in the direction of light propagation. Figure 4.3 shows a picture of the designed photodiode mask file.

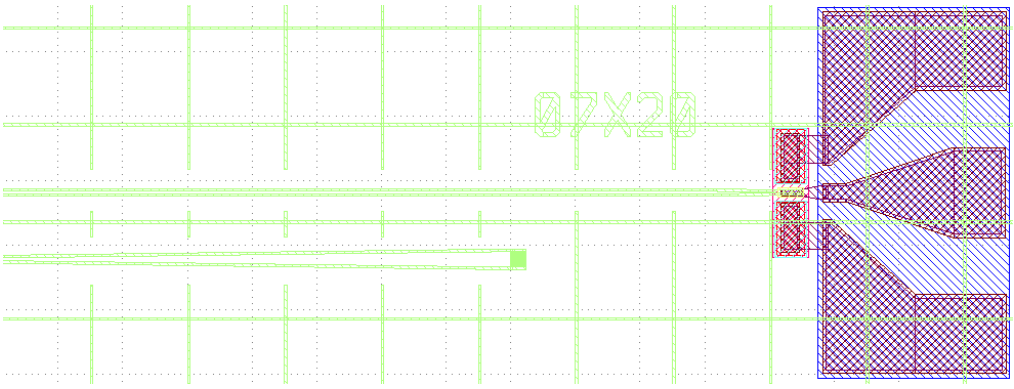


Figure 4.3 Picture of the designed photodiode mask file

As introduced in chapter 3, the fabrication process starts with III-V material transfer to the pre-patterned SOI wafer through a low-temperature wafer bonding process [60] [39]. Next, the bonding intermedia, SiO_2, is deposited on both, the III-V die and the Si. The bonding process was done at Aurrion.

After the InP substrate was removed at Aurrion using wet-etch, I deposited p-contact metal followed by self-aligned p-mesa etching. Next, the n-mesa was etched and n-contact metal was deposited. To passivate the photodiode side walls I deposited a 200 nm-thick layer of SiO_2. The coplanar waveguide (CPW) probe pads were formed by Au electro-plating on a 2 µm-thick layer of SU-8. Finally, I diced the chips and polished the waveguide facets. The inset of Figure 4.4 shows a fabricated photodiode.

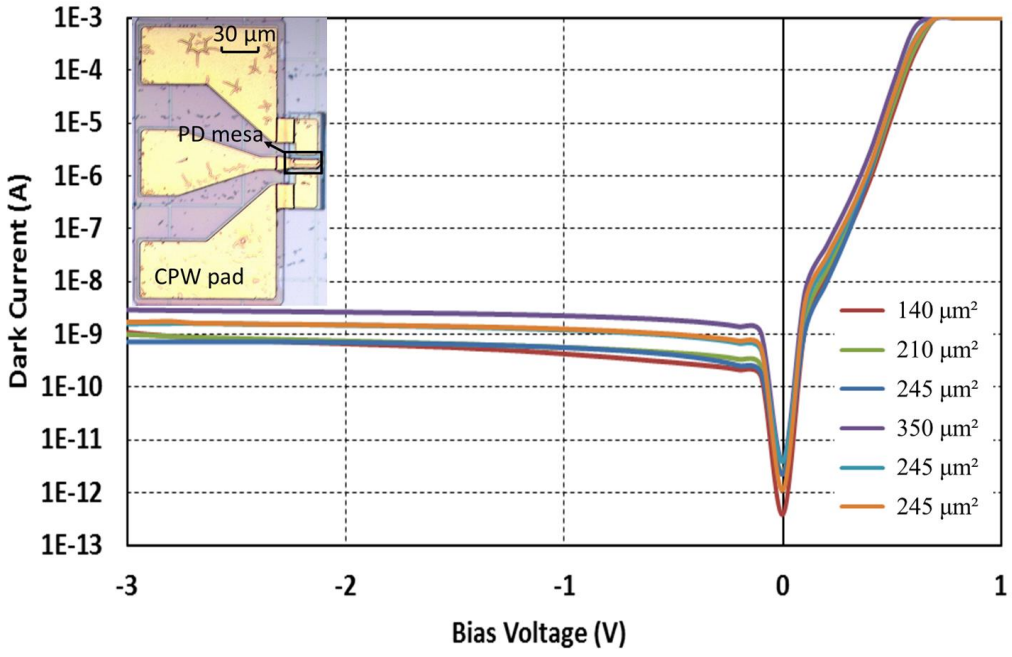


Figure 4.4 Measured dark currents of photodiodes with 140 µm², 210 µm², 245 µm² and 350 µm² active area. Inset: Fabricated photodiode

4.3 Measurement Results and Discussion

Figure 4.4 shows the measured I-V curves indicating very low dark currents of 1 nA at 3 V reverse voltage. I used a lensed fiber with a spot size diameter of 3.8 µm to couple light from a laser source at 1.55 µm wavelength into the silicon waveguide. The measured external responsivity of a photodiode with 50 µm length was 0.13 A/W at 1.55 µm wavelength. By accounting for the fiber-chip coupling (mode mismatch loss) and reflection losses of 6.5 dB (acquired from simulation) and 1.5 dB (the air-Si normal incident reflectance) respectively, I determined the internal responsivity to be as high as 0.84 A/W. Figure 4.5 shows the external responsivity of photodiodes with different lengths, widths, and nano-waveguide widths. Figure 4.6 shows the simulation result of residual power in the waveguide as a function of taper tip width, given the length of taper and PD length are both 50 µm. From the simulation it can be seen that a 300 nm taper tip leads to highest absorption, which agrees with the measured

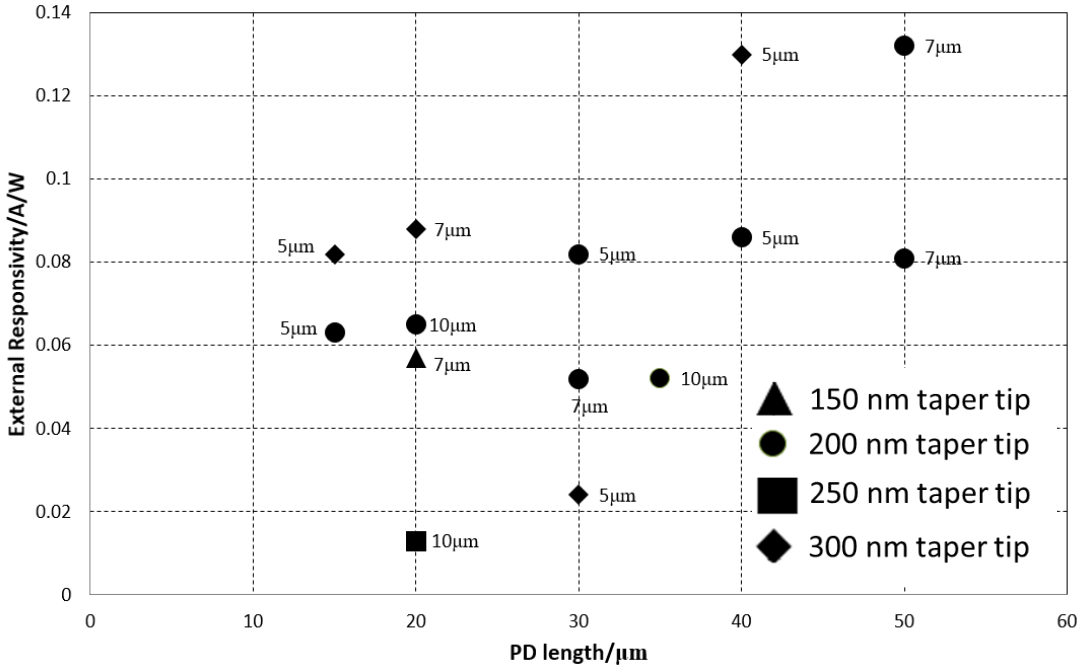


Figure 4.5 External responsivity as a function of PD length and width

trend shown in Figure 4.5.

The waveguide loss is measured to be 5.9 dB/cm by comparing the input and output optical power of a straight passive waveguide. By accounting for the length of the waveguide of the photodiodes (540 µm long), the actual waveguide loss is less than 0.32 dB. The photodiodes exhibit a low polarization dependent loss (PDL) of 0.8 dB, as calculated with equation 2-4. The photodiode capacitance was measured for waveguide photodiodes and large mesa diodes from the same wafer (inset of Figure 4.8) at 1 MHz using an LCR meter. Figure 4.8 demonstrates linear relationships between the capacitance at -7 V and the active area for both device types. Using the data from the mesa diode, I calculated the depletion width to be 1100 nm which is close to the design value of 1080 nm. I found that the slope for the waveguide photodiodes is larger than that for simple mesa diodes which indicates the presence of an additional parasitic capacitance that may originate from the proximity of the n-metal to the p-metal which was only 2 µm for the waveguide photodiode but 10 µm for the mesa diode. The point at which the linear regression crosses the Y-axis estimates the pad capacitance present in each PD and was

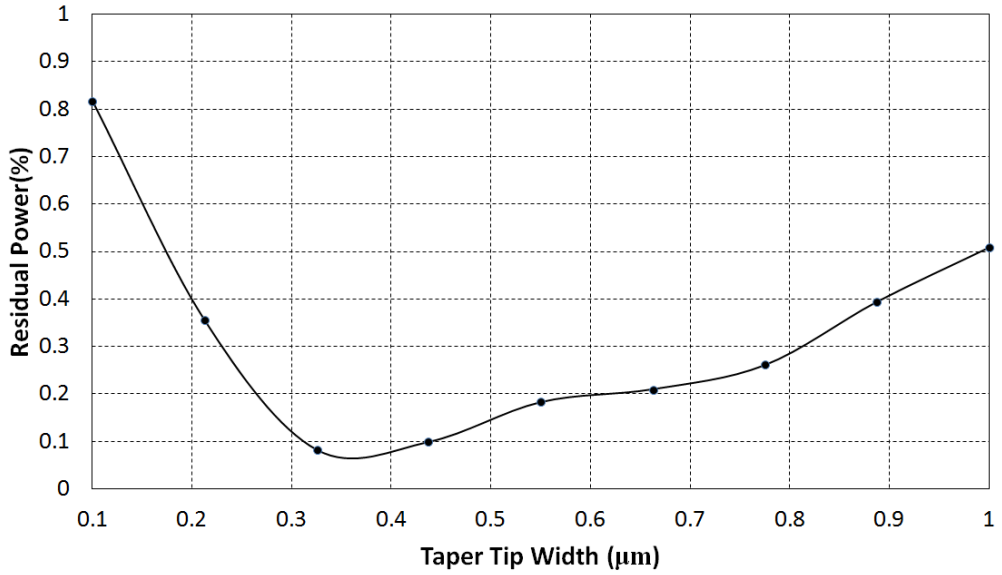


Figure 4.6 Simulation of residual power as a function of taper tip width. Taper length=50 µm, PD length= 50 µm

determined to be 13 fF.

Figure 4.7 shows the measured frequency responses of the heterogeneously integrated MUTC PDs with areas of 30 μm^2, 54 μm^2, 210 μm^2 and 700 μm^2. The 3-dB bandwidths reached 65 GHz, 50 GHz, 43 GHz and 25 GHz, respectively. Figure 4.9 summarizes the results together with the calculated bandwidths. The bandwidths derived from the RC-time constant of each PD (using equation 2-6) accurately match the measured results from photodiodes with photoabsorption layer areas greater than 300 μm^2. However, the calculated values based on RC overestimate significantly the measured data at areas below 200 μm^2. By accounting for the transit time-limited bandwidth (using equation 2-8 and 2-9 and parameters in Table 4.1), the estimates more closely match measured data across all device areas.

I used the heterodyne experimental setup (Figure 3.3) but at a fixed optical difference frequency to

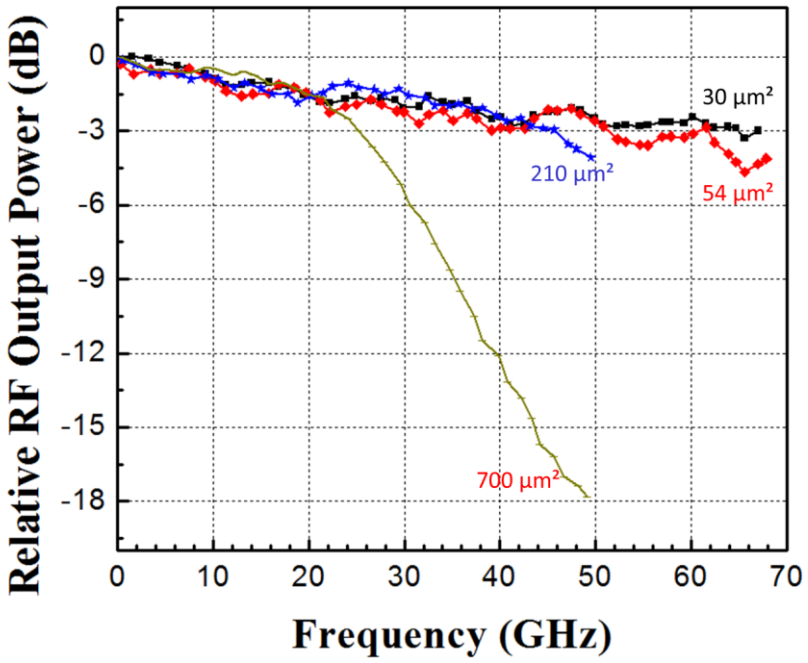


Figure 4.7 Measured frequency responses of heterogeneous MUTC PDs with different active areas at 3 V reverse bias

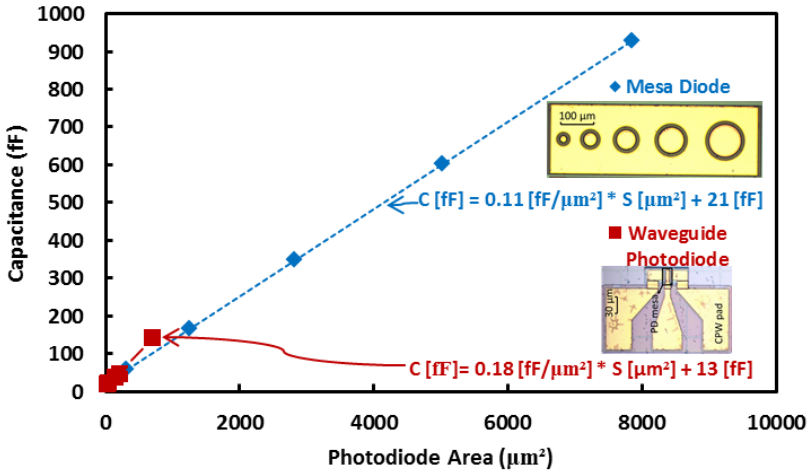


Figure 4.8 Measured capacitance versus photodiode area and linear fit

measure the high-power characteristics. Figure 4.10 shows the results from a PD with 3 x 42 µm^2 active area at 29 GHz and a 5 x 15 µm^2 PD at 50, 65 and 70 GHz. The highest RF output power level and photocurrent for the 3 x 42 µm^2 single photodiode were 8 dBm and 25 mA at 29 GHz, respectively. The 1-dB compression current can be observed at 22 mA. The highest RF output power level and photocurrent for the 5 x 15 µm^2 photodiode were -2 dBm and 20 mA at 70 GHz, respectively. A comparison of my work with works from other groups is shown in Figure 4.11. I demonstrated a record-high output power level at 70 GHz for waveguide photodiodes on SOI waveguides.

Parameter	Value	Reference
V_e (electron drift velocity in InP)	1.5e5 m/s	[84]
D (electron drift distance)	1.08 µm	
ε_r (relative permittivity of InP)	12.5	[85]

Table 4.1 Parameters used in bandwidth estimation

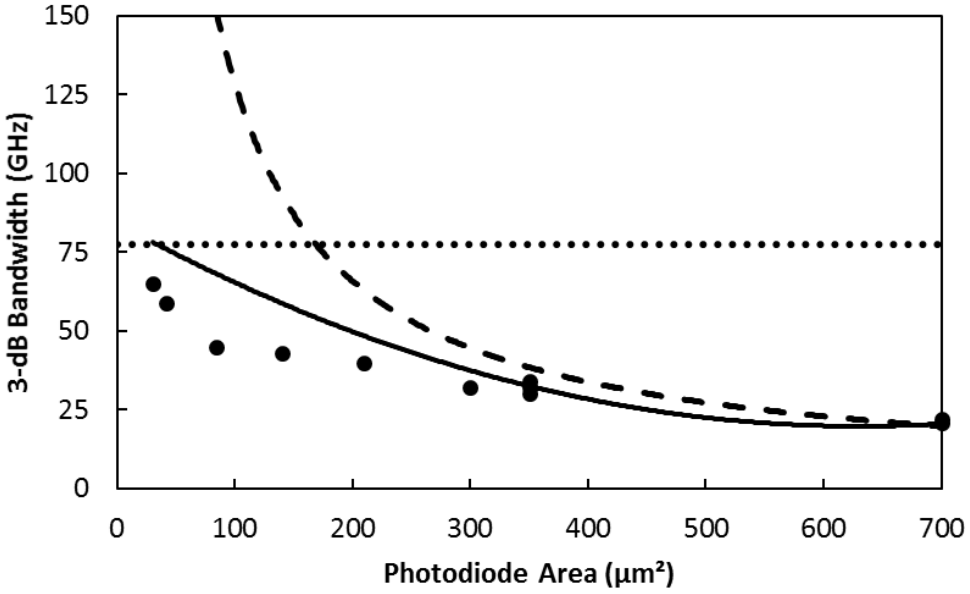
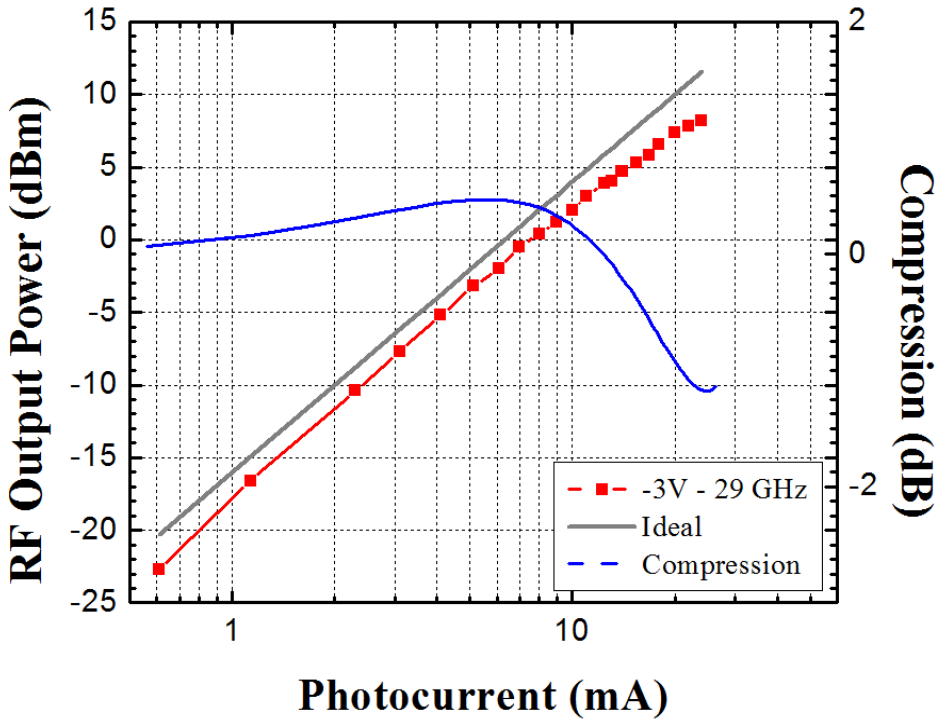
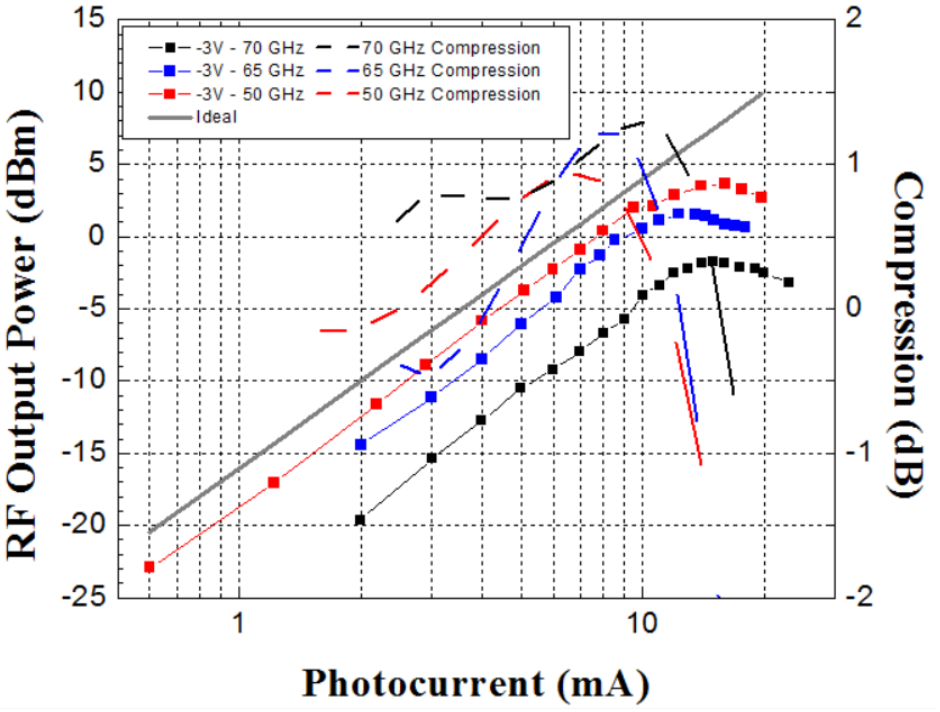


Figure 4.9 3-dB bandwidth versus photodiode area. Circles are measured data, the dotted and dashed lines represent calculated results for the transit time and RC-limited bandwidth, respectively. The solid line includes both effects



(a)



(b)

Figure 4.10 RF output power and compression of (a) 3 x 42 μm² and (b) 5 x 15 μm² single photodiode at -3 V bias voltage

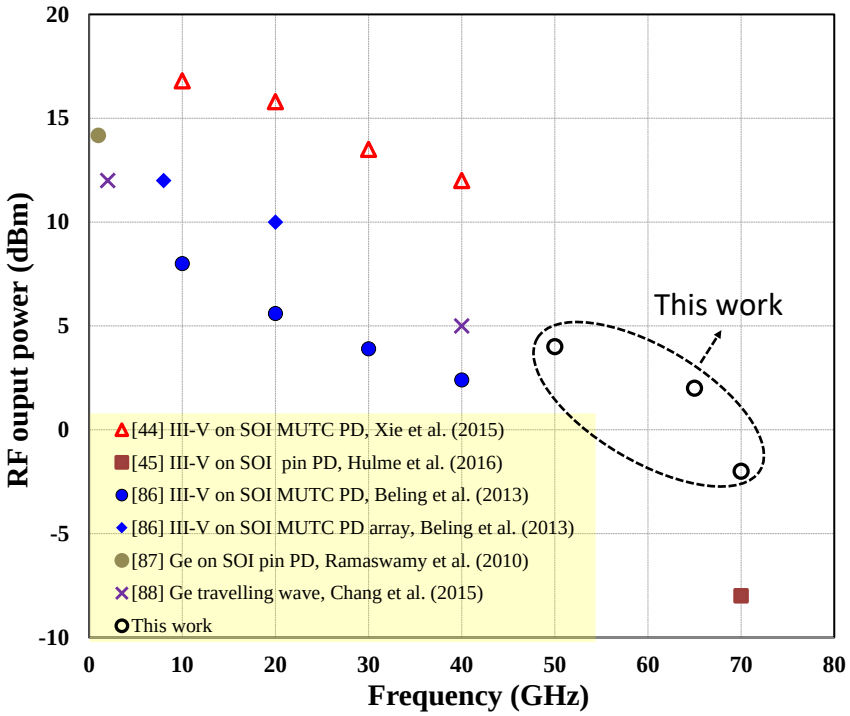


Figure 4.11 RF output power level at 50 Ω load of waveguide photodiodes on SOI versus signal frequency at 1.55 μm wavelength

Chapter 5 Heterogeneously Integrated Balanced Photodiode

5.1 Introduction

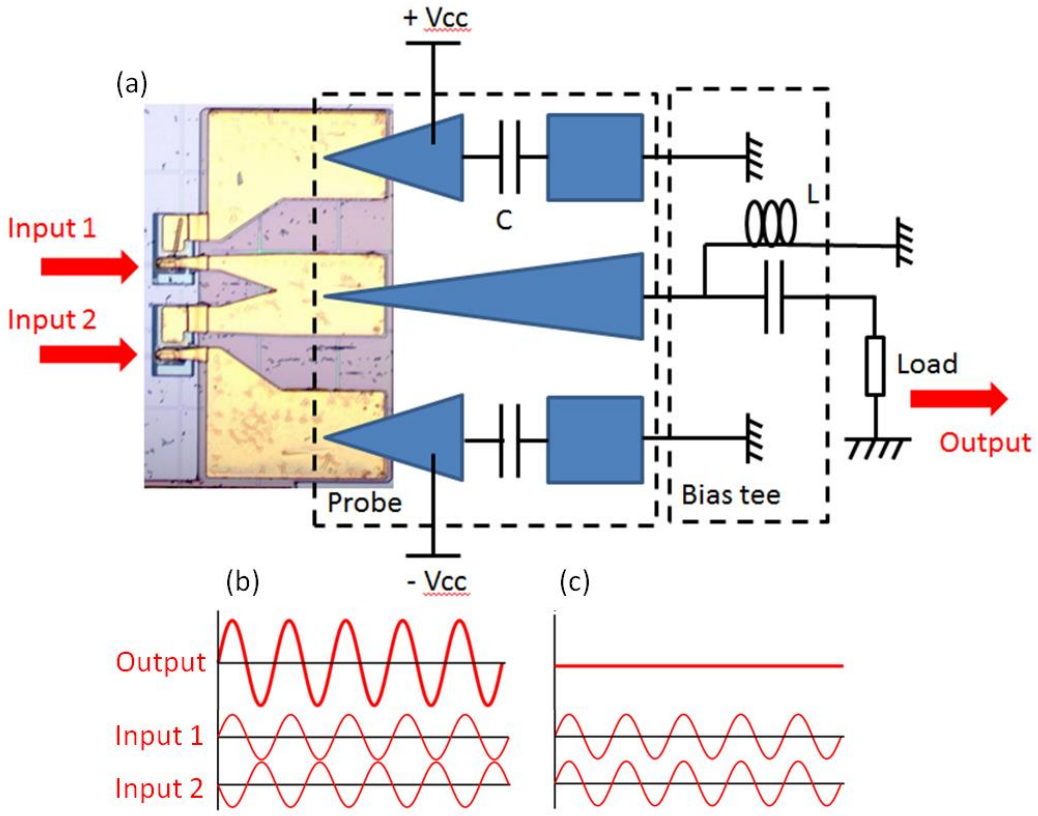


Figure 5.1 Balanced photodiode detection scheme (a), RF-modulated optical carrier input signals (envelopes) and output RF current signal from balanced photodiode under differential mode (b) and common mode (c)

Balanced photodiodes are configured in a way such that common mode (in-phase) input signals can be canceled, while differential mode (quadrature) input signals can be delivered to the external load. This detection scheme has several advantages, for example, by canceling common mode relative intensity noise (RIN) and amplified spontaneous emission (ASE) noise with balanced photodiodes, the SNR of an optic link can be greatly improved [62], especially at high power levels.

5.2 Balanced Detection Scheme and Device Structure

Figure 5.1a shows the balanced photodiode configuration. The p-contact of photodiode PD1 is connected to the n-contact of PD2. For measurements the balanced detector is connected to the load resistor through a customized on-wafer probe and a bias tee. The RF grounds of the probe are decoupled by two large capacitors, so that positive and negative DC bias can be applied individually onto the two photodiodes.

When the input signals are in differential mode, as shown in Figure 5.1b, the RF responses add and power is delivered to the load resistor. However, when the input signals are in common mode (in-phase), as shown in Figure 5.1c, the RF responses cancel and the total output is zero. When, for example, used

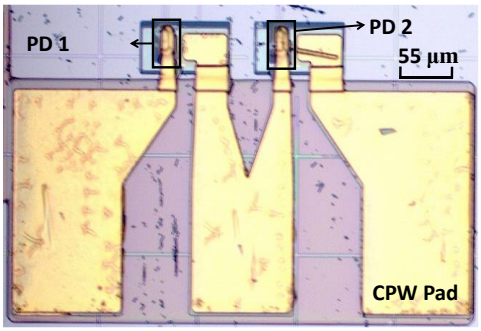


Figure 5.3 Fabricated balanced photodetector

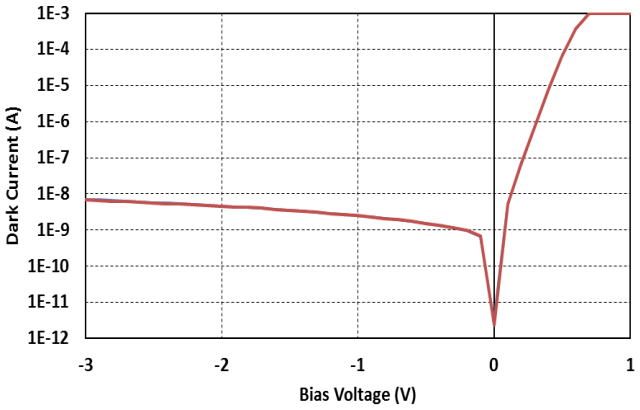


Figure 5.2 Measured dark currents of photodiodes PD1 and PD2 in the balanced photodetector with an active area of 7 x 20 µm². The two I-V curves overlay on top of each other

in a coherent receiver, the signal is differential while RIN and ASE noise are in-phase in both arms, so they can be canceled by the balanced photodiode. However, due to the imperfect symmetry of the balanced photodiode, the in-phase noise cannot be fully eliminated. The output ratio of the differential mode input to the common mode input is defined as the common mode rejection ratio ($CMRR =$

$10log\left(\frac{P_{out-diff\ mode\ input}\ [mW]}{P_{out-comm\ mode\ input}\ [mW]}\right)$), as a measure of the common mode suppression capability of a balanced photodiode.

5.3 Measurement Results and Discussion

Balanced photodiodes were fabricated on the same wafer together with the single photodiodes described in chapter 4. Figure 5.2 shows typical I-V curves of the two photodiodes in the balanced photodetector. Figure 5.3 shows a top-view of a fabricated balanced photodetector. Similar to Figure 4.4, the dark currents are as low as 7 nA at 3 V reverse bias.

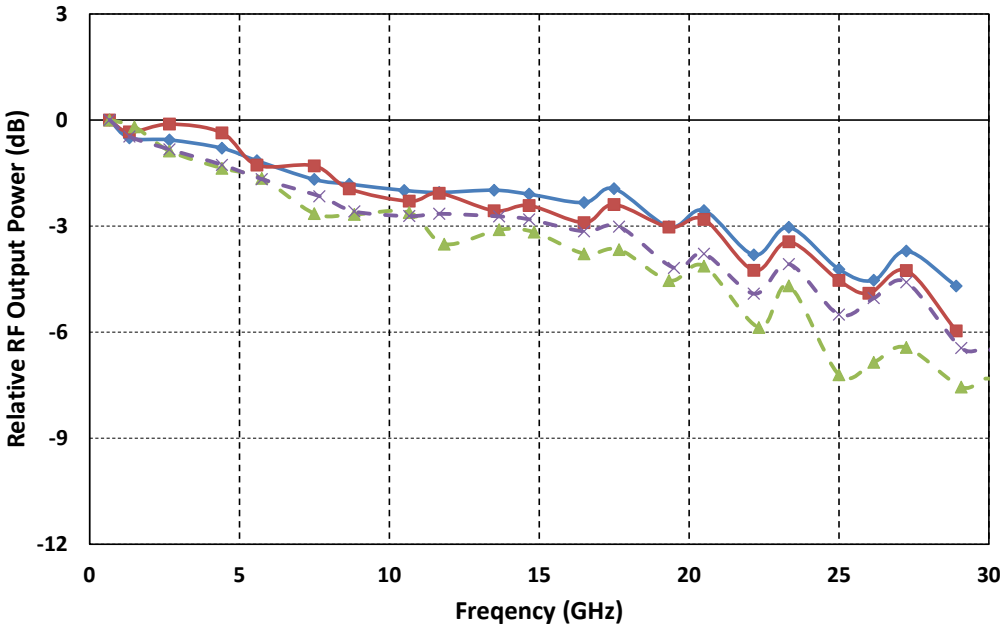


Figure 5.4 Normalized frequency responses of individual photodiodes of balanced MUTC PDs with 7 x 20 μm² (solid) and 7 x 35 μm² (dashed) active areas at 3 V reverse bias and 1.5 mA average photocurrent

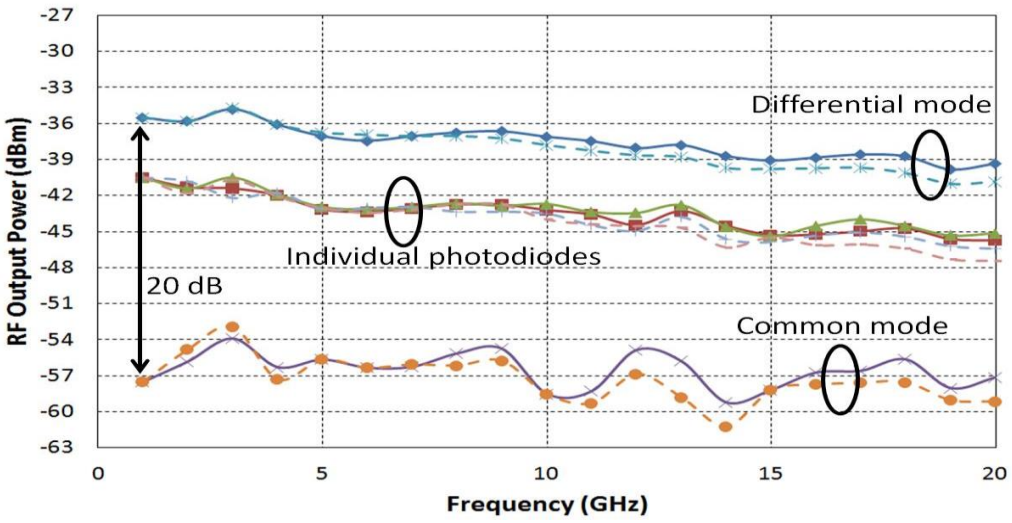


Figure 5.5 Frequency responses of a 7 x 35 μm² balanced photodetector at 2 V (dashed) and 5 V (solid) reverse bias, 0.16 mA photocurrent

Using the setup shown in Figure 3.3, the bandwidth responses of individual photodiodes of two balanced photodetectors were measured. Figure 5.4 shows the measured results. For the photodiodes with 7 x 20 μm² active area, the bandwidth reaches 20 GHz, and for 7 x 35 μm² devices, the bandwidth is 15 GHz. It should be noted that the frequency response curves of the two photodiodes in the balanced detector agree within 1 dB up to their 3 dB bandwidth.

Using the setup shown in Figure 3.5, the performance of the balanced photodetector under differential mode and common mode is characterized. Figure 5.5 shows the measured frequency responses in common mode, differential mode, and from individual photodiodes (illuminating one PD at a time) in the balanced photodetector at 2 V and 5 V reverse bias. The bandwidth in differential mode reaches 20 GHz at 5 V. By subtracting the power in common mode from the power in differential mode I obtain the common mode rejection ratio. I find that the CMRR is larger than 20 dB over a wide range of frequencies. As expected, the RF output power from the balanced photodiode under differential mode operation is 6 dB higher than the power level from a single diode at the same frequency and photocurrent. 3-dB bandwidth and CMRR are not changed much by increasing reverse bias voltage from

2 V to 5 V. The differential mode bandwidth is the highest that has been reported for any heterogeneously integrated balanced photodetectors on a SOI waveguide platform.

Chapter 6 Heterogeneously Integrated Dual-Input Photodiode

6.1 Introduction

It was shown in chapter 4 that the optical coupling efficiency can be significantly increased by optimizing the tapered Si waveguide. However, while this leads to high responsivity, it may also result in local saturation effects and impaired high-power handling capability. Since the waveguide taper is only 300 nm wide the more concentrated optical energy will be more likely to cause localized overheating and saturation within the first few µms of the photodiode absorption region.

6.2 Device Design

In order to make the optical absorption profile more uniform and mitigate localized saturation, I proposed a dual-input waveguide photodiode. Theoretically, the onset of localized saturation effects can be postponed, and as a result, higher saturation current and higher maximum output RF power can be achieved. In this design a 95 µm x 10 µm 1x2 multimode interference (MMI) coupler (Figure 6.1) is used to split the input light equally into two feeding optical waveguides that both terminate at the same photodiode. Figure 6.2 shows a schematic view of proposed dual-input waveguide photodiode. The

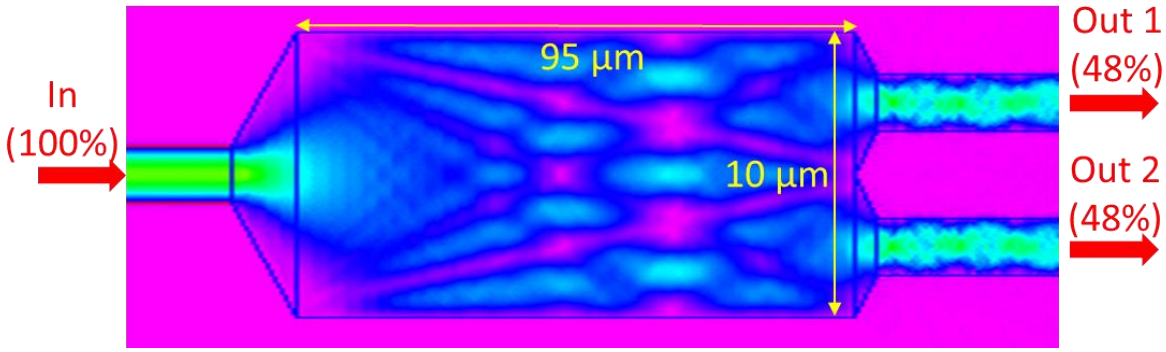


Figure 6.1 Optical intensity in a 1x2 MMI coupler splitting input optical power into two output waveguides, each with 48% of the input optical power

epitaxial structure for the dual-input waveguide photodiode is identical to that shown in Figure 4.2a. The layout of the photodiode mesas and CPW pads are also identical to the previously described single-input device.

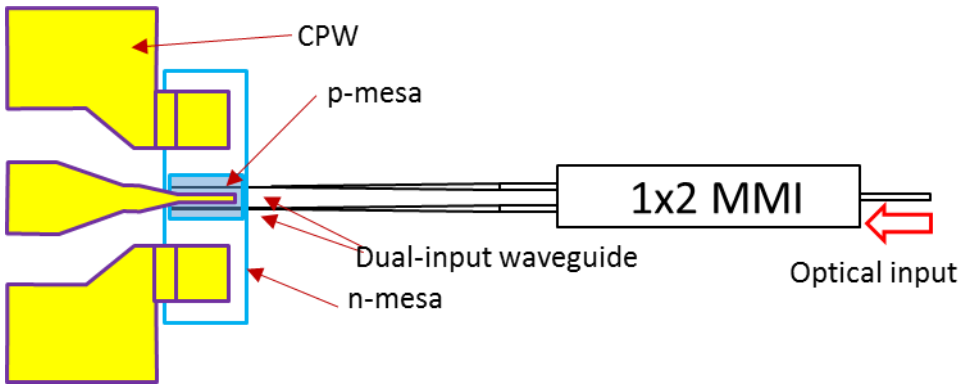


Figure 6.2 Proposed dual-input waveguide photodiode

6.3 Measurement Results and Discussion

Figure 6.3 shows typical I-V curves of dual-input photodiodes with active areas of 350 μm² and 700 μm². The dark currents at -3 V reverse bias are as low as 5 nA. A typical value of the external responsivity for a 35 μm-long dual-input PD was measured to be 0.09 A/W, which is consistent with a single-input waveguide PD. It follows that the optical insertion loss from the MMI is negligible under low intensity optical illumination (photocurrent < 10 mA). The same 350 μm² dual-input PD was measured using the optical heterodyne setup. The RF bandwidth was found to be 33 GHz, which is comparable to its single-input counterpart (Figure 6.4).

The RF output power at different bias voltages and frequencies from dual-input waveguide PDs is shown in Figure 6.5. For comparison, the output power from a single-input waveguide PD is included. It can be observed that the maximum RF output power of the dual-input photodiode is always lower than that of single-input device, even though they follow the same trace when the photocurrent is below 10 mA. For photocurrents above 10 mA, the photocurrent and RF output power drop abruptly to nearly zero. Similar behavior can be observed for the DC photocurrent - CW light optical power relation (Figure 6.6). As the photocurrent increases to ~ 10 mA, the output from the dual-input PD drops dramatically, while the single-input PD's photocurrent keeps increasing linearly. However, this phenomenon is reversible. Turning off the laser, leaving the dual-input PD unbiased for at least 30 minutes, and re-starting the measurement from low photocurrent (<10 mA), the same RF output power curve and

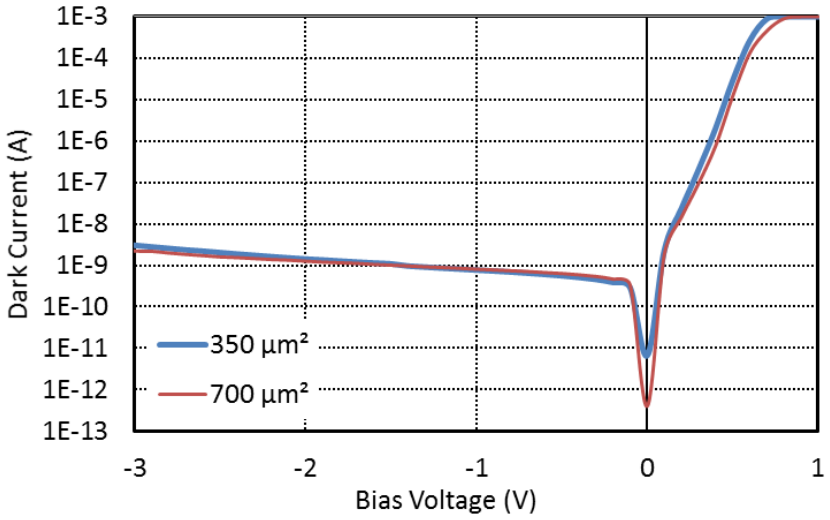


Figure 6.3 Typical I-V curves of dual-input PDs with areas of 350 µm² and 700 µm²

photocurrent level can be reproduced. It is also observed that this phenomenon is wavelength dependent. When the dual-input PD is illuminated by a 1558 nm wavelength laser, the photocurrent can be pushed beyond 10 mA, while under 1541 nm illumination, the photocurrent experiences a sharp drop at ~ 10 mA (Figure 6.7). At 1541 nm illumination, and, instead of starting from low optical power, if a

high (30.7 dBm) optical power is first applied to the dual-input PD, the output can reach a high photocurrent (9.9 mA). However, after less than 10 seconds, the photocurrent drops abruptly to 2.8 mA.

It should be mentioned that the abrupt drop in photocurrent and output power was observed independently of PD bias voltage. Based on the relatively slow transition time the dual-input PD experienced, I suspect the mechanism behind such phenomenon is related to thermo-optical effects. Details on verifying this hypothesis and a further investigation plan will be discussed in the future work section.

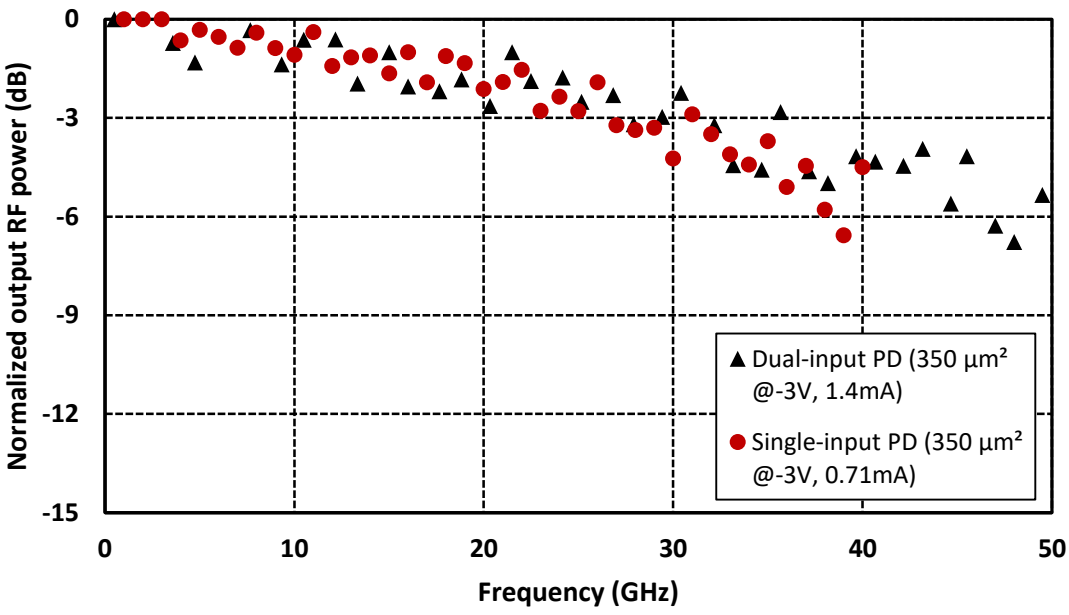


Figure 6.4 Measured frequency response of dual-input and single-input PD with 350 µm² area

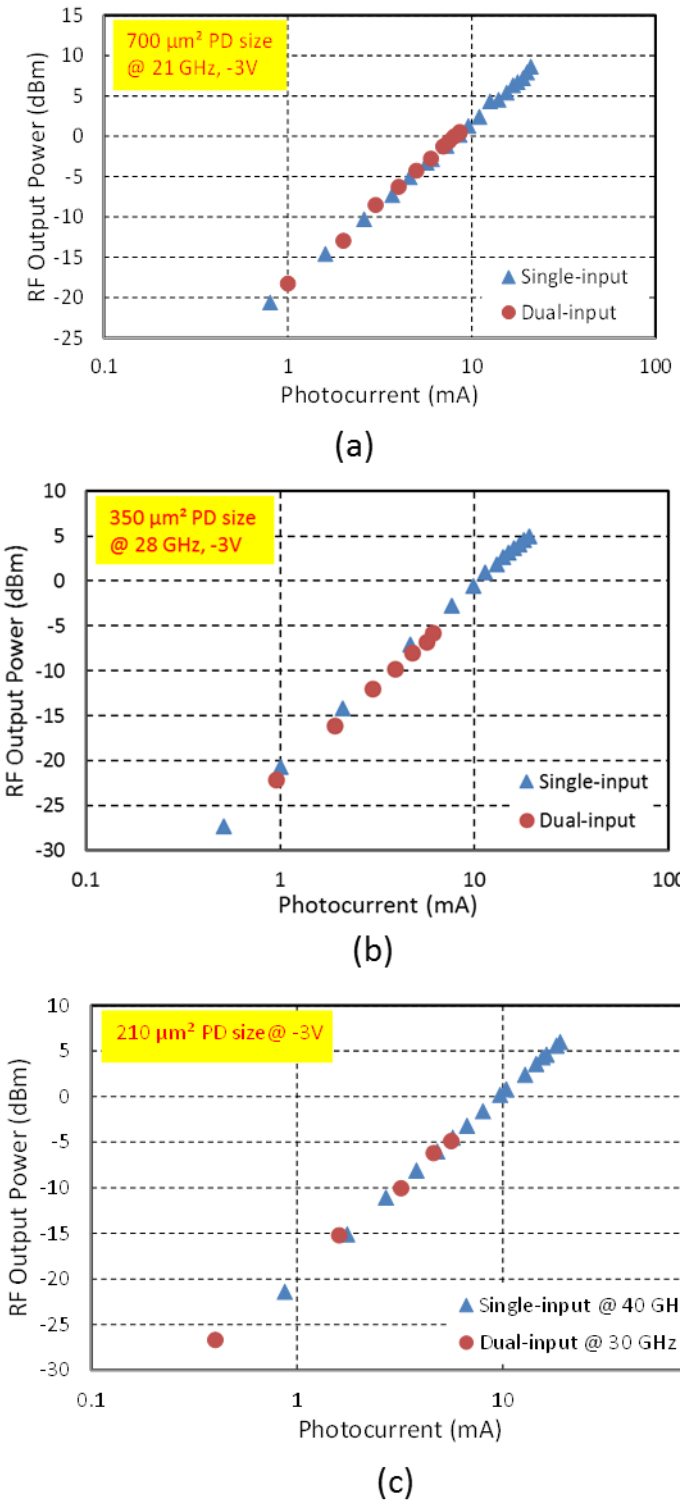


Figure 6.5 RF output power of (a) 700 µm², (b) 350 µm² and (c) 210 µm² photodiodes

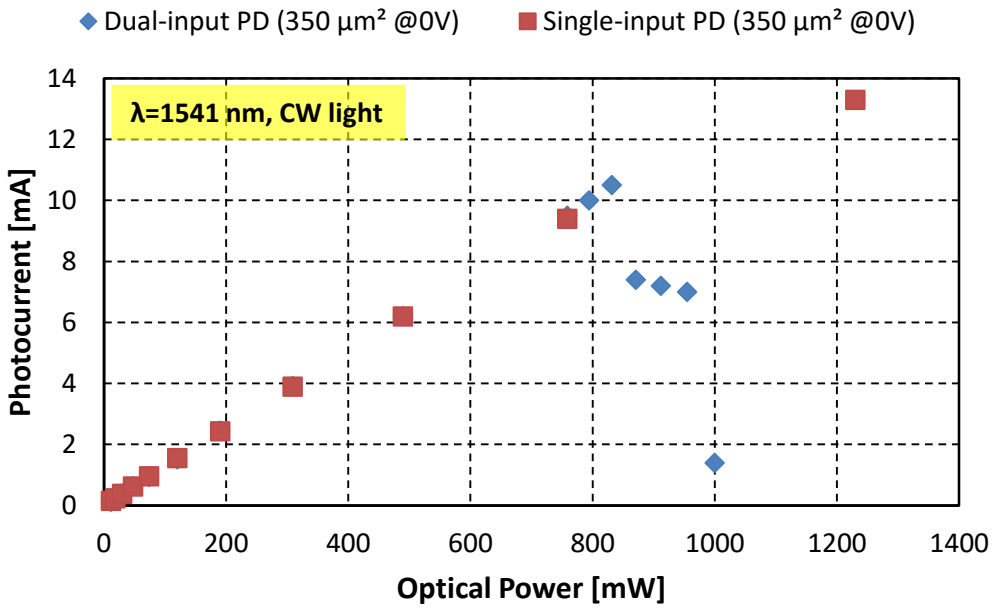


Figure 6.6 Photocurrent as a function of optical power

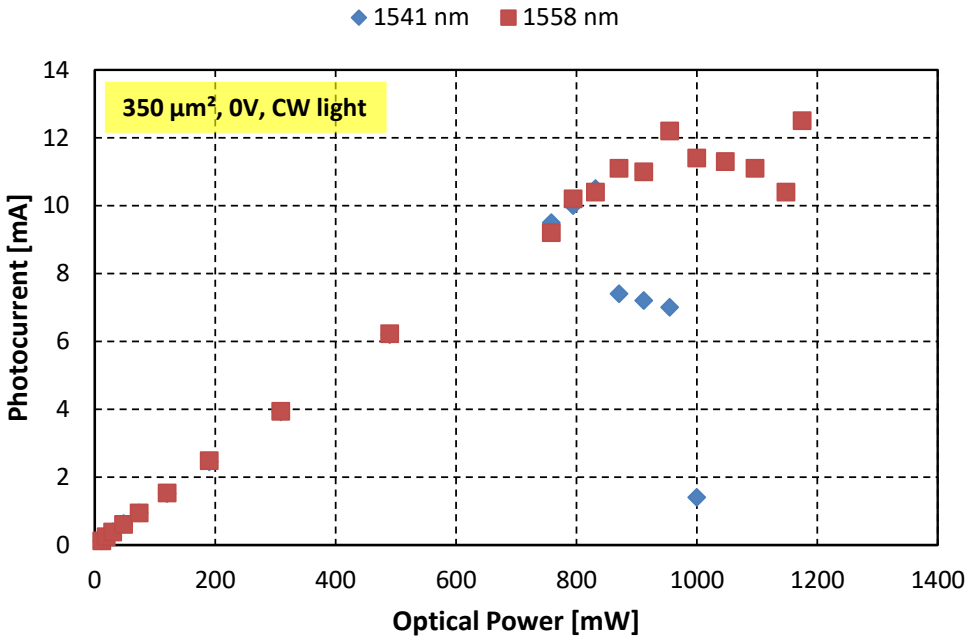


Figure 6.7 Photocurrent of dual-input PD under different illumination wavelength

Chapter 7 Adhesive Bonding Integration

As stated in the previous chapters, heterogeneous integration is an enabling technique for photonic integrated circuits (PICs) on Si. It provides the potential to bring together dissimilar devices and materials onto a single chip [63]. As described in the previous chapters, waveguide photodiodes based on molecular bonding achieved record-high speed and RF output power. An alternative to molecular bonding is adhesive bonding that is available at UVa. Compared to molecular bonding, adhesive bonding has the following advantages: higher tolerance to wafer surface cleanliness, higher tolerance to wafer flatness [40], and the potential for integration with electronic THz devices [64]. To this end, I collaborated with Prof. Weikle's THz group and studied adhesive bonding of photodiodes using SU8.

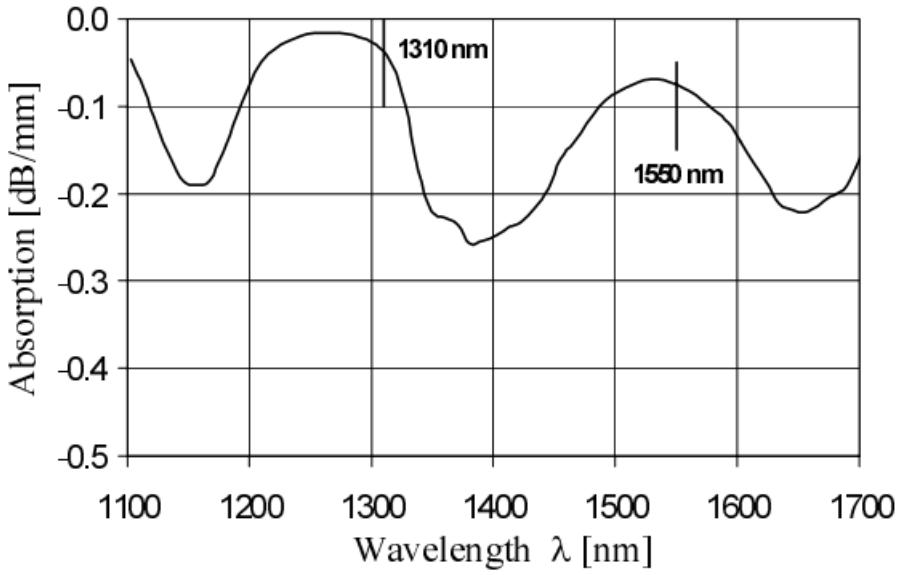


Figure 7.1 Absorption spectrum of cross-linked SU8 [80]

7.1 Heterogeneous Integration Using SU8

7.1.1 Optical Properties of SU8

SU-8 is a commonly used epoxy-based negative photoresist. The optical properties of SU8 are critical whenever it is used in the optical path. Due to its low optical absorption at telecom wavelengths and relatively high refractive index (1.57), SU8 has been fabricated into waveguides [65] and gratings [66].

SU8 exhibits good transparency over a broad wavelength range, covering telecommunication wavelength (1310 nm and 1550 nm) [67]. Beyond 400 nm, transmittance is around 95%. Figure 7.1 shows a transmission spectrum of cross-linked SU8. The refractive index around 1550 nm is 1.51 (Figure 7.2).

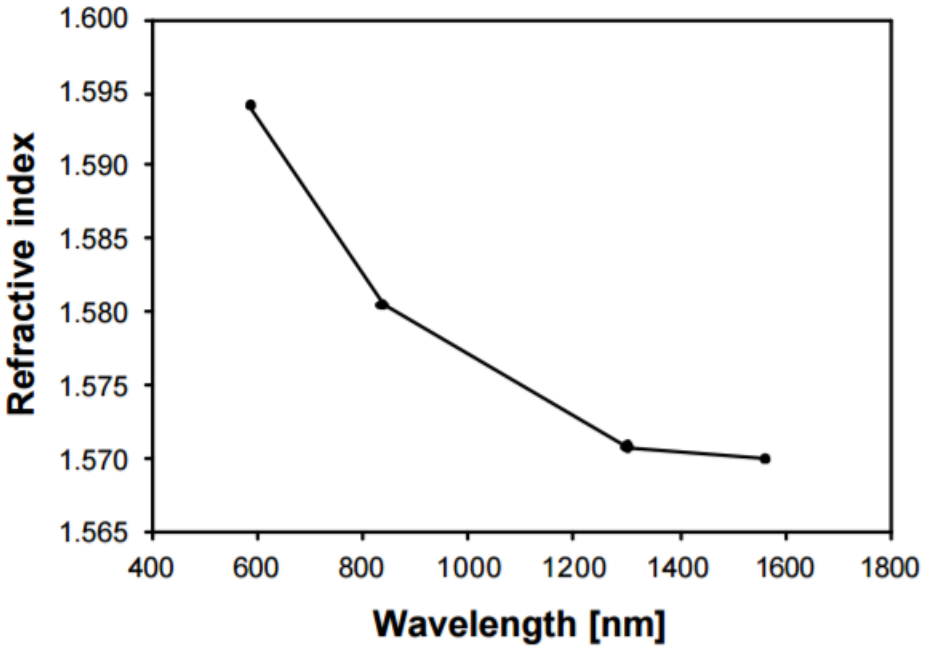


Figure 7.2 Refractive index of cross-linked SU8 as a function of wavelength [81]

7.1.2 Bonding Process Development

Previously, my collaborators, Souheil Nadri and Linli Xie from Prof. Weikle's group, developed an SU8 bonding technique for their THz Schottky diode quadrupler applications [64] [68]. With their support, I developed a similar bonding technique for InGaAsP/InP photodiodes on silicon. I conducted a series of bonding tests and successfully fabricated photodiodes heterogeneously integrated on Si by SU8 bonding, which show comparable performance as their counterparts on native InP substrate.

The heated and pressured bonding process under vacuum is carried out with an in-house designed and manufactured die-to-die bonder, shown in Figure 7.3. Typical dimensions of the III-V die and Si die used for bonding is 1 x 1 cm^2 and 3 x 3 cm^2, respectively.

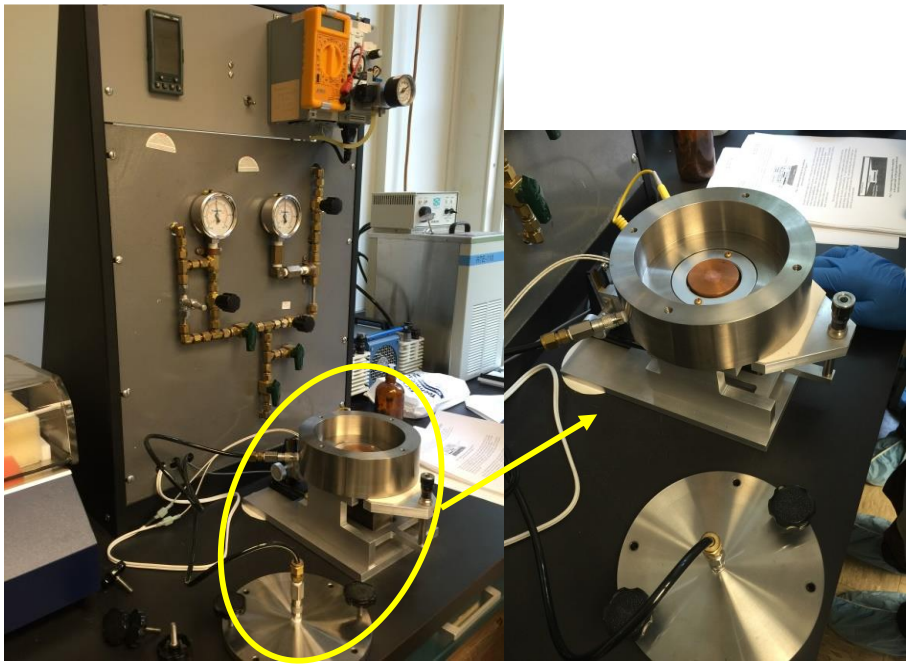


Figure 7.3 In-house designed wafer bonder (left) and zoom-in view of bonding chamber (right)

Surface Cleaning

Although the requirements for surface cleanliness are greatly relaxed in adhesive bonding when compared to intimate molecular bonding, a clean surface is still essential to a successful bonding. Any contamination particles taller than the thickness of the bonding intermedia, SU8, can cause de-bonding issues (Figure 7.4). In order to prepare the surface of both, the III-V and the Si dies to the desired cleanliness, a standard cleaning process was developed.

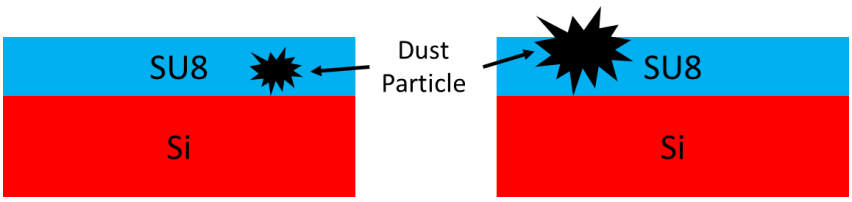


Figure 7.4 SU8 compensating dust particle

Both surfaces to be bonded are first swabbed by a Q-tip soaked with AZ-300K to remove large particles, owing to the sticky nature of AZ-300K. Then, TCE, and reagent alcohol are used during a spin clean. If after multiple iterations some particles still remain, a mechanical treatment is applied. The equipment for inspection and mechanical treatment includes a long-focus microscope with large working distance. Any particles are manually scratched off with a toothpick. After that, AZ-300K swab clean and spin clean is repeatedly iterated until die surface is fully cleaned. The cleaning process is finished when any type of contamination (solvent residual, particles, etc.) is fully removed under 20x microscope magnification.

SU8 Application and Pre-Cure

SU8 is spin-coated on the surface of the Si die using a standard photoresist spinner. The SU8 thickness can be effectively controlled by the spin speed and the SU8 concentration. Spinning at 6k rpm for 30s results in an SU8 (2002.5) thickness of 1.4 µm. After spin-coating, the SU8 is first thermally pre-

cured on a hotplate at 65° C for 60s followed by 95° C for 120s. Next, the SU8 is pre-cured under i-line (365 nm) UV exposure for 90s using the MJB-3 aligner. After pre-curing, the samples are ready to be loaded into the bonder for die-to-die bonding.

Bonding Process

After loading both, the III-V and the Si dies into the bonder chamber, the chamber is pumped down to -24 psi and the dies should remain in the vacuum for at least 30 mins for complete SU8 out-gassing. This is critical in order to achieve a void-free bond.

After out-gassing, the bonding process is conducted at 130° C and 10 psi bonding pressure for 40 mins. During the bonding process, the SU8 is fully cured and a permanent bond between the III-V and the Si die is formed.

InP Substrate Removal

Figure 7.5 shows a schematic of the bonding process, including InP substrate removal. In order to have access to the device layers, the 350 μm thick InP substrate has to be removed. A commonly used method of InP substrate removal is HCL wet etch. The chemical reaction between InP and HCL is given by

$$InP + 3HCL \rightarrow InP_3 + PH_3 \uparrow$$

It should be noted that the gaseous reaction byproduct, PH_3, is highly flammable. Arcs from static discharge in plastic gadgets can easily ignite PH_3. For safety reasons, and to avoid PH_3 accumulation, the reactor beaker should not be covered.

Etching speed and uniformity are largely determined by the HCL solution concentration. 3HCL:1H_2O is a preferred combination to balance the tradeoff etching speed and uniformity [69]. To verify etch

rates I carried out a series of etching tests (Figure 7.6). The etching rate of InP in 3HCL:1H_2O solution is 6 µm/min at room temperature (20° C). Hence, for our 350 µm-thick InP substrate, it takes 60 mins to fully remove the substrate, which was verified experimentally.

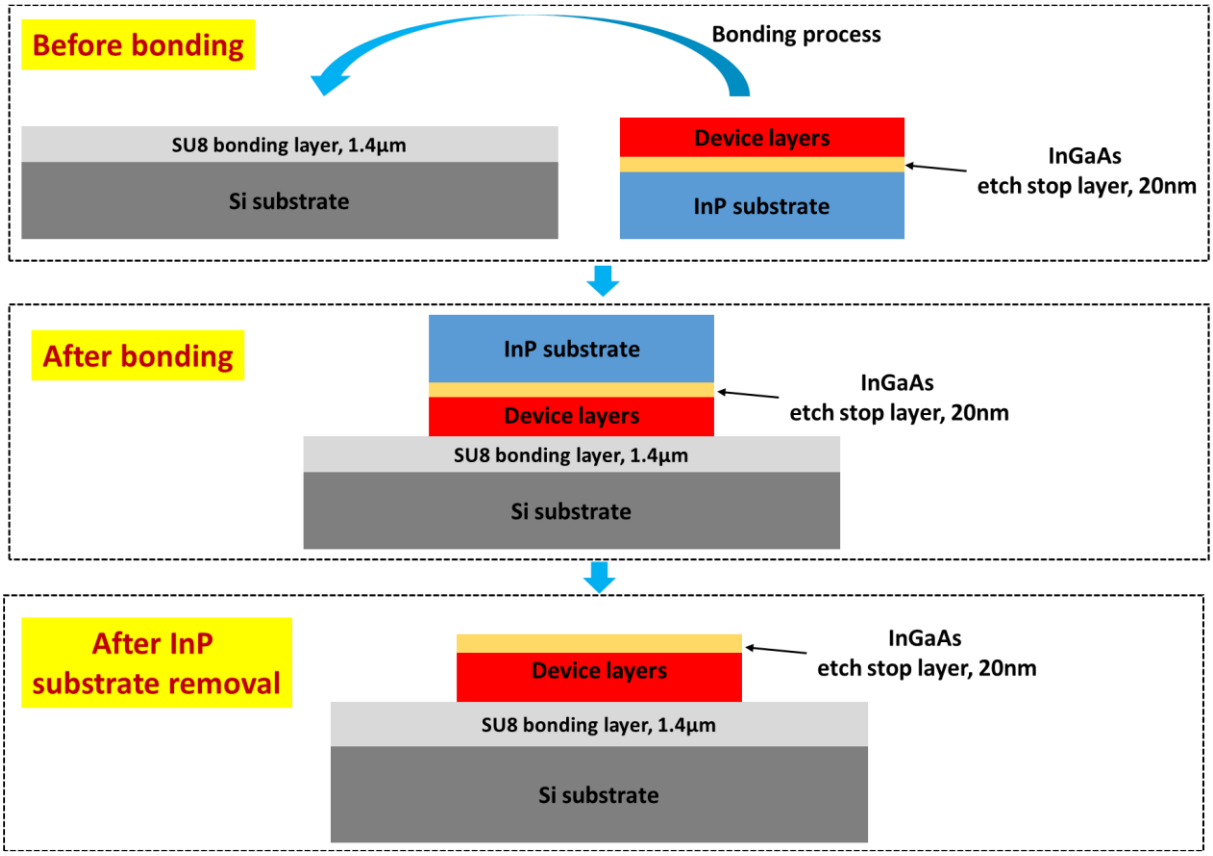


Figure 7.5 Bonding process flow

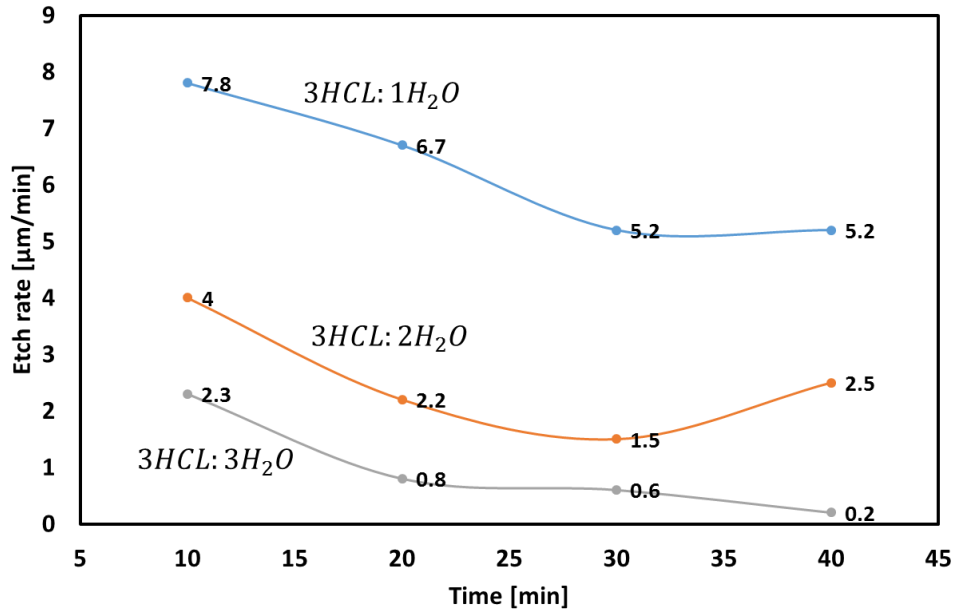


Figure 7.6 InP etch rate at different HCL concentrations at 20 ˚C

One key point for successful substrate removal is the presence of a 20-nm thick InGaAs/InGaAsP etch stop layer beneath the InP substrate (Figure 7.5). Since HCL does not etch InGaAs, the process completely stops at the InGaAs/InGaAsP layer [70]. A table of etchant selectivity is shown in Table 7.1 [58].

	Material Selectivity		
Etchant	InP	InGaAs	InGaAsP
$HCl: H_3PO_4$	Etch	Stop	Stop
$H_3PO_4: H_2O_2: H_2O$	Stop	Etch	Stop
$H_2SO_4: H_2O_2: H_2O$	Stop	Etch	Etch
$HCl: H_2O$	Etch	Stop	No data

Table 7.1 Wet chemical etch selectivity table [82]

HCL wet etch is an ideal approach for InP substrate removal owing to its moderate etching speed and excellent selectivity. However, its anisotropic nature (Figure 7.7), (HCL does not etch into the (0 1 -1) InP crystal plane) on (1 0 0) InP wafers usually leads to considerable ramps on two opposite edges of the InP die [69] [71]. A SEM picture showing such a ramp after substrate removal is shown in Figure 7.9. The angle of the ramp is measured to be 36.6°, which is close to the theoretically calculated 35° in [72].

From the SEM picture, the height of the ramp is determined to be 200 μm. Such a surface condition makes contact lithography impossible. Therefore, in order to proceed, the InP ramp has to be removed. The width of the ramp (<500 μm) is small compared to the die (1 mm x 1 mm), so it can be removed from the die without impairing the usable die area.

The ramps can be removed mechanically by cleaving or dicing. Since the cleaving interface is high quality, no chipping occurs. However, it is important that the crystal orientation of the Si die is known and strictly maintained during the process. The crystal orientation of the III-V can be arbitrary, because the thickness of III-V epitaxial layers is small (~ a few μms) and can be easily pulled apart. Figure 7.8 shows a bonded sample before and after cleaving. After cleaving, the center Si die is covered with 1 x 1 cm^2 ramp-free III-V device epitaxial layers, which is ideal for the following processes. The two ramps are successfully cleaved off.

A dicing saw can also be used to remove the InP ramps. Figure 7.11 shows SEM pictures of the diced interfaces using a Disco chip saw. In the side-view picture, the edges of both, the III-V and Si are chipped off. However, this is not an issue, because the bonded III-V epitaxial layers do not peel off during the dicing process and the chipped area only extends into the center by less than 3 µm, as measured in the top-view picture. Figure 7.10 compares the quality of the cleaved vs. sawed chip edges. It is clear that cleaving produces a smoother interface than dicing, however, dicing provides a better capability of fine alignment and cutting line control.

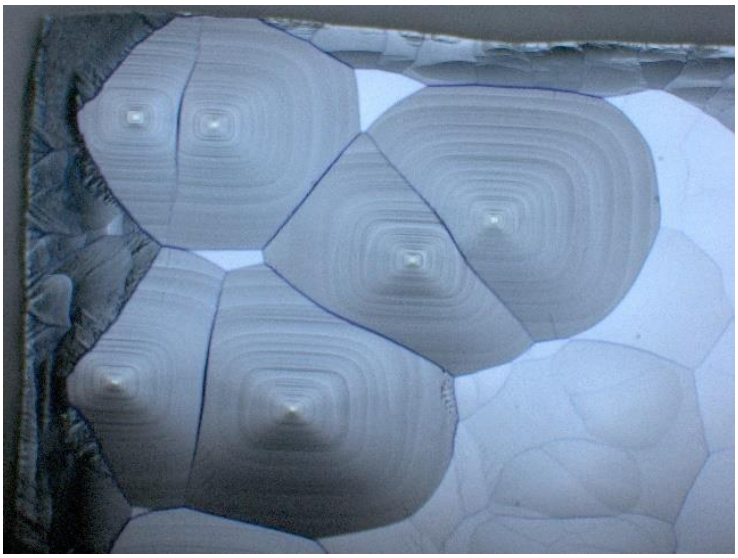


Figure 7.7 InP die surface etched by HCL at room temperature for 20 mins

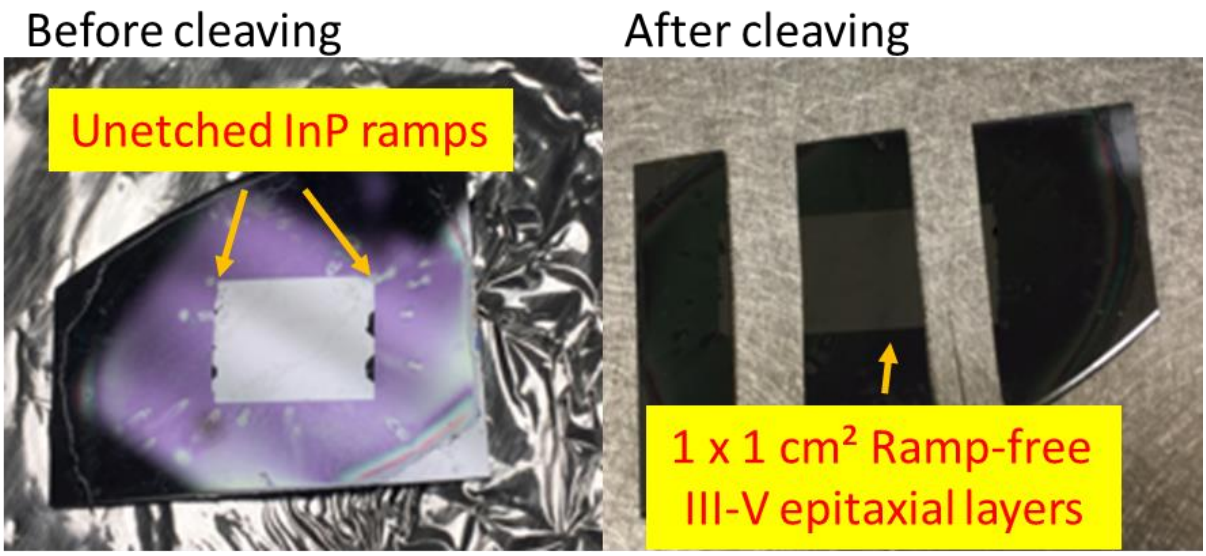


Figure 7.8 Bonded sample before and after cleaving

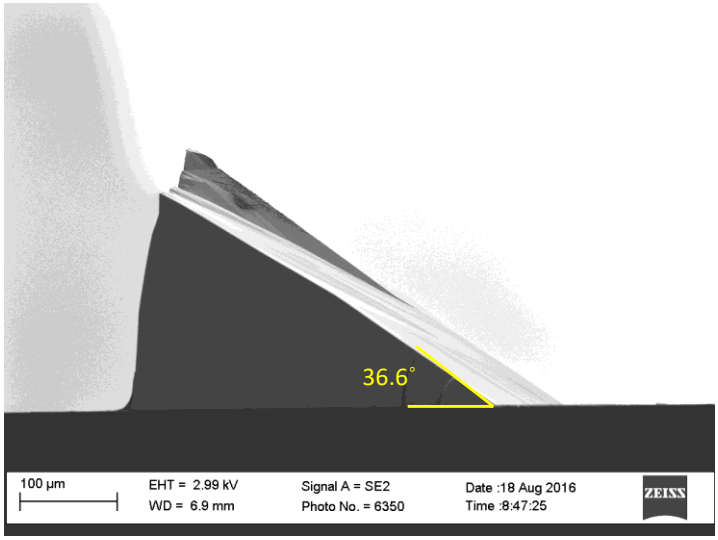


Figure 7.9 InP ramp generated during HCL substrate removal

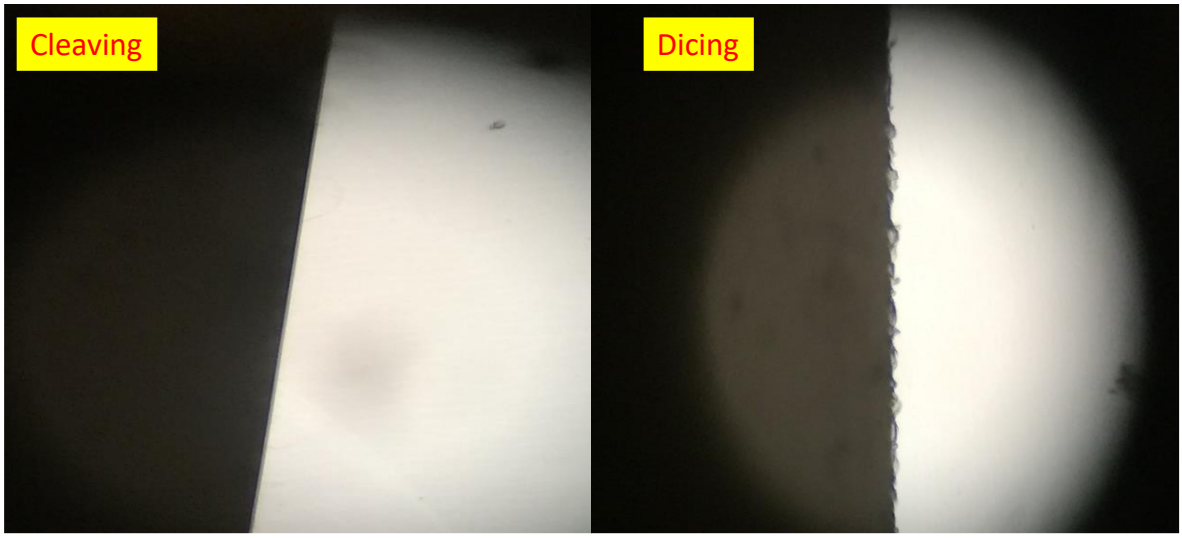


Figure 7.10 Comparison of cleaved and sawed chip edge

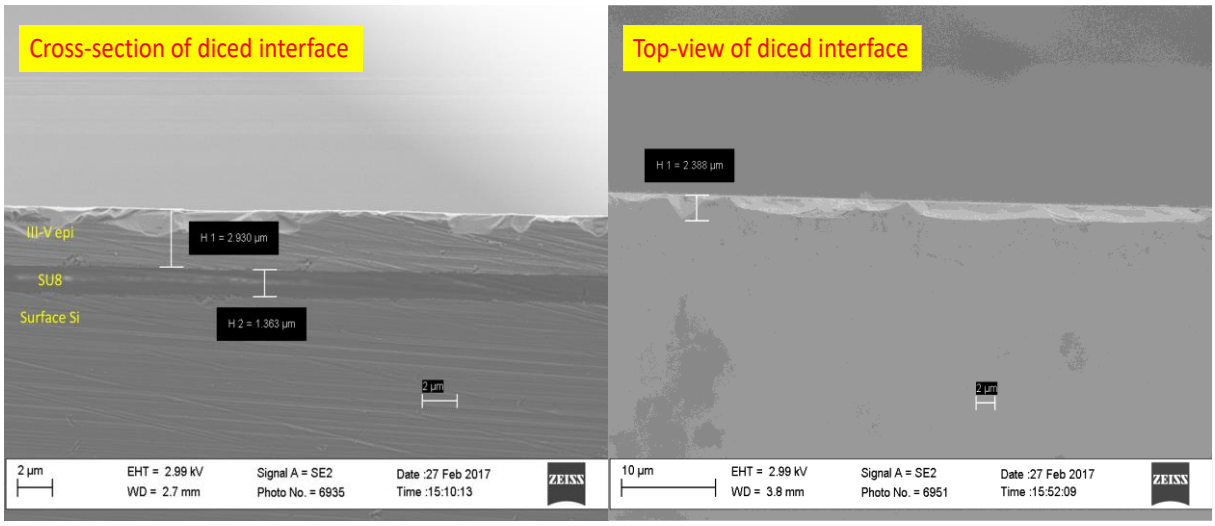


Figure 7.11 SEM examination of diced interface

Bonding Results

Figure 7.12 shows an SEM cross-sectional view of the bonding interface of the InGaAsP/InP epitaxial layers on an un-patterned Si die. A high quality and void-free SU8 bond is achieved. The high quality bond demonstrates the potential of SU8 for silicon photonics heterogeneous integration.

After these initial trials I conducted a series of bonding tests using photodiode epi-layers that have been previously developed in our group. The results are summarized in Table 7.3. The epitaxial structures of MUTC4, MUTC8 and MUTC11 are included in Appendix II. After multiple bonding trials, I

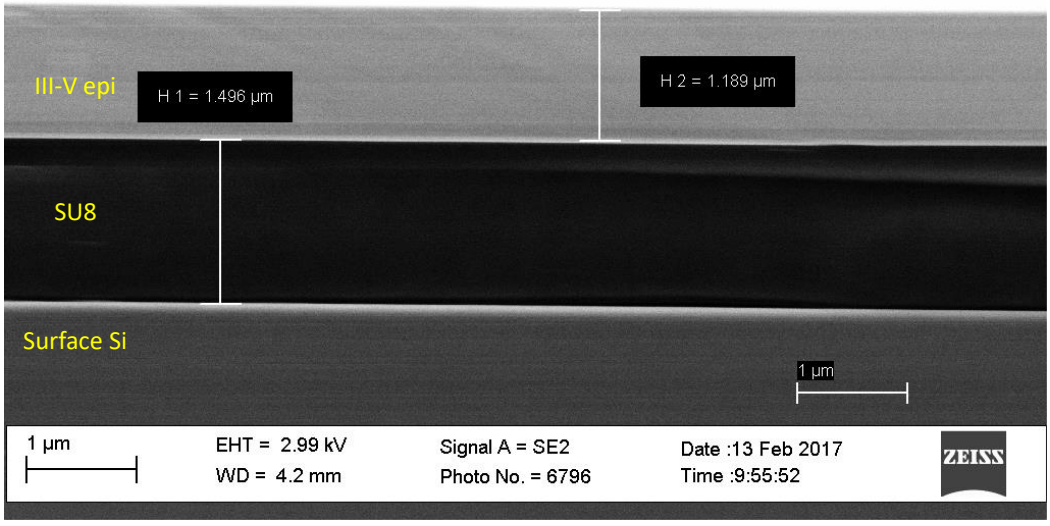


Figure 7.12 SEM cross-section view of bonding interface

found that P+InGaAs on 1.4 µm-thick SU8 delivers the most reliable results.

During my studies I found that the SU8 model (defined by the manufacture) and the type of doping at the bonding interface of the III-V die have significant influence on the substrate removal yield using HCL solution. So far, only bonded dies with SU8-2002 and p-type InGaAs bonding interface survived the HCL-based substrate removal process. Under these conditions the yield can be close to 100%, with reliable and repeatable bonding results. Dies with combination [SU8-2002 + N-type InGaAs] and [SU8-6000.5 + N-type InGaAs] all de-bonded during the substrate etching process, regardless of the type of bonding promoter that was applied. The combination [SU8-6000.5 + P-type InGaAs] has not been tested yet. The results are summarized in Table 7.2. Some hypotheses can be made based on my and other research group's experimental observations: SU8-6000.5 has a dense crosslink network, which makes it more vulnerable to strong acids (such as HCL). As a result, though SU8-6000.5 is not physically etched away by HCL, chemical bonds between the SU8 and the die surface are broken, thus causing de-bonding problems. The crosslink network density of SU8-2002 is not as high as SU8-6000.5, so it is more likely to survive the HCL substrate etching process. Also, it has been confirmed by the observations from other research groups that P-type InP-based III-V materials work better as bonding interface than N-type materials.

SU8 model / III-V interface	SU8-2002 (>1 µm)	SU8-6000.5 (< 300 nm)
P+ InGaAs	Bond	?
N+ InGaAs	Debond	Debond

Table 7.2 Effect of SU8 model type and III-V die bonding interface doping type on substrate removal yield

Label		1st	2nd	3rd	4th	5th	6 & 6.1th	7th	8th	Linli & Souheil's experiment
Time		2016/8	2016/10	2017/1	2017/2	2017/2	2017/2	2017/3	2017/3	
SU8	Model	2002.5	TF6000.5	TF6000.5	TF6000.5	2002.5	2002.5	2002.5	2002.5	TF6000.5
	Thickness/µm	1.4	0.5	0.25	0.25	1.4	1.4	1.4	1.4	0.25
III-V die	Type	MUTC11	MUTC8	MUTC8	MUTC8	MUTC11	MUTC4	MUTC4	MUTC11	InGaAs on GaAs handle
	Substrate thickness /µm	350	650	650	650	350	350	650	350	
	Bonding interface	P+ InGaAs	N+ InGaAs	N+ InGaAs	N+ InGaAs	P+ InGaAs	P+ InGaAs	P+ InGaAs	P+ InGaAs	N++ InGaAs
Promoter		/	Omnicoat	Omnicoat	Ti	/	/	/	50nm Ti	Ti or Omnicoat
Substrate removal	Acids	3HCL: 1H2O	HNO3:H2O+ 3HCL:1H20	HNO3:H2O+ 3HCL:1H20	3HCL: 1H2O	3HCL: 1H2O	3HCL: 1H2O	3HCL: 1H2O	3HCL: 1H2O	HNO3, Citric acid, HF
	Result	Worked	Debonded	Debonded	Debonded	Worked	Worked	Worked	Worked	Worked
Comments						Repeat 1st bonding	Repeat 1st bonding		For metal mirror test, not for fabrication	Work very reliably

Table 7.3 Table of bonding trials

7.2 Surface Normal Photodiode Fabrication and Characterization

To verify the applicability of the process described in the previous section it is necessary to prove that the µm-thin III-V epitaxial layers can withstand the entire device fabrication process. To this end I

developed a fabrication process that is compatible with the bonding intermedia, SU8, and fabricated and characterized top-illuminated photodiodes.

I selected the MUTC4 [61] epitaxial structure (Appendix II, figure A.II.1) for the bonding and fabrication test. This structure includes a 20 nm –thick n-type InGaAs layer between the n-contact layer and the InP substrate, which serves as the etch stop during substrate removal. I used the 1.4 µm-thick SU8-2002.5 bonding process to bond a 1 x 2 cm^2 MUTC4 epi die onto a larger, un-patterned Si die (bonding trial label #6). The InP substrate was removed by 3HCL:1H_2O solution wet etch at room temperature (20° C). Figure 7.13 shows pictures of the bonded sample before and after substrate removal. The two un-etched InP ramps were cleaved off.

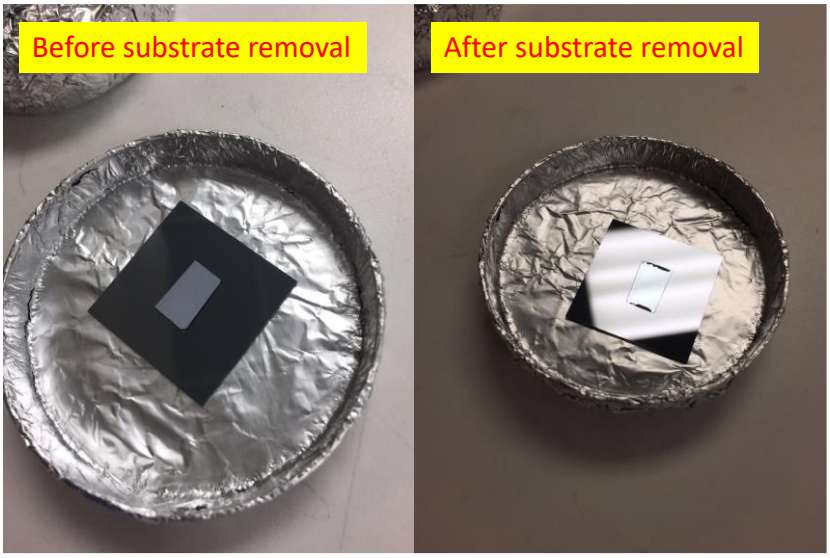


Figure 7.13 Bonded MUTC4 sample before and after substrate removal

Figure 7.14 shows the cross-section of the bonding interface under the SEM. After confirming the bonding quality and successful substrate removal, I fabricated the sample into top-illuminated double-mesa photodiodes.

The fabrication process starts with surface cleaning. Acetone, methanol and deionized water are used to rinse the sample to remove particles. Next, the sample is placed into O_2 plasma at 190 W RF power, 80 sccm O_2 for 600s to remove any organic carbon-based contamination. After thorough cleaning, I used contact photolithography to pattern the p-mesa, followed by another 200s O_2 plasma treatment (190 W RF power, 80 sccm O_2) for residual photoresist removal. The photodiode mesas were formed by a series of chemical wet etches. First, 20 nm InGaAs is selectively etched by a $1H_3PO_4: 1H_2O_2: 10H_2O$ mixture at an etch rate of 10 nm/s [58]. Then, 2 μm InP is selectively etched by an $3HCL: 1H_2O$ mixture at an etch rate of 6 μm/min [58]. Finally, 700 nm InGaAs/InGaAsP are selectively etched by a $1H_2SO_4: 1H_2O_2: 10H_2O$ mixture at an etch rate of 20 nm/s [58]. After mesa etching, all photoresist is removed by acetone rinse and O_2 plasma treatment. Standard contact photolithography is used to define the contact metal regions. Layers of 40 nm Ti and 100 nm Au are deposited onto the sample serving as both, p and n contact metals. Finally, lift-off is carried out to remove redundant metal. No passivation or anti-reflection coating was applied. Figure 7.15 shows the fabricated photodiodes under an optical microscope and SEM. The shapes of the photodiode mesas deviate from circular to irregular during the mesa wet etch process, due to the anisotropic etching nature of the InP/InGaAsP in the etchant acid [73]. Figure 7.16 shows the layer structure of the fabricated photodiode.

I measured the photodiode capacitance vs. reverse bias voltage (C-V) at 100 kHz for multiple photodiodes with different sizes. Figure 7.17 shows the measured C-V curves up to 10 V. Figure 7.18 shows the capacitance as a function of photodiode area at different bias voltages. As the bias voltage increases, the measured capacitance approaches the calculated value using the parallel plate capacitance (equation 2-7) in chapter 2, which indicates a linear relationship between capacitance and PD area, as expected.

Typical current- voltage (I-V) curves are shown in Figure 7.19. Multiple photodiodes with different areas were measured up to -3 V. For small PD areas the dark current can be as low as 4.2 nA, which is comparable to the dark current level of similar photodiodes on native InP substrate [3]. At 1 V forward bias, the dark current of all photodiodes reaches 1 mA, indicating a low series resistance (<5 Ω). It

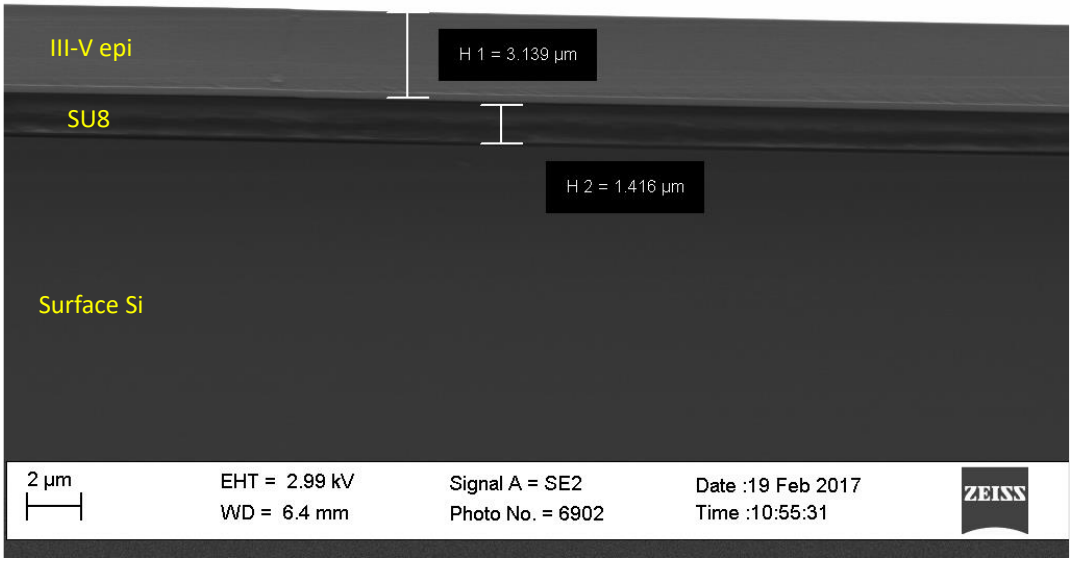


Figure 7.14 SEM cross-section view of bonding interface

should be mentioned that the dark current is not in a linear relation with either PD area or PD radius. Since there is no surface passivation on the sidewall of the diode mesa, it can be concluded that the dark current originates from both, bulk and surface leakage. The responsivity was measured on a PD with 45216 µm² area and was found to be 0.4 A/W at -3 V and 1550 nm, which is close to the calculated value using equation 3-3 from chapter 2 for the responsivity.

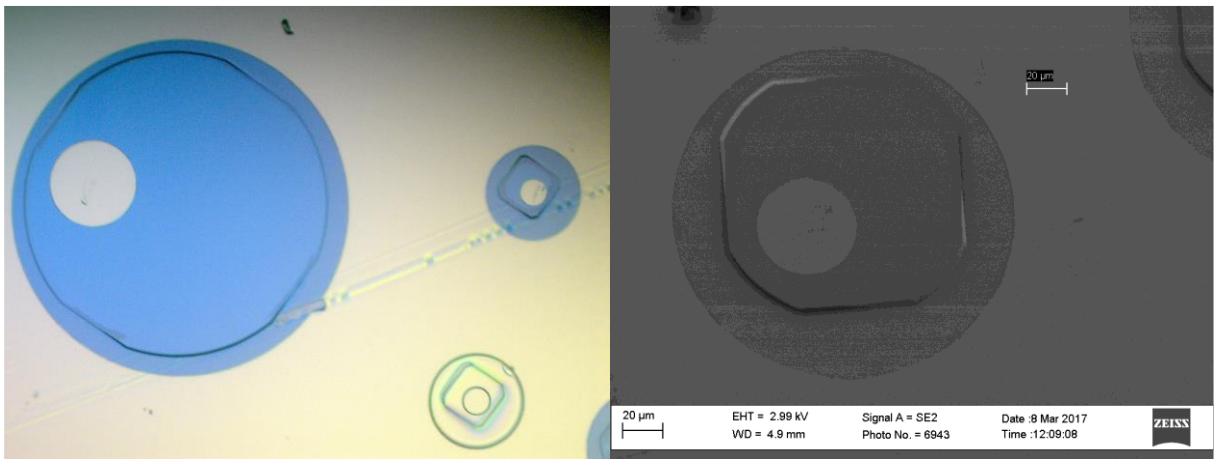


Figure 7.15 Fabricated photodiode heterogeneously integrated on Si by SU8 bonding

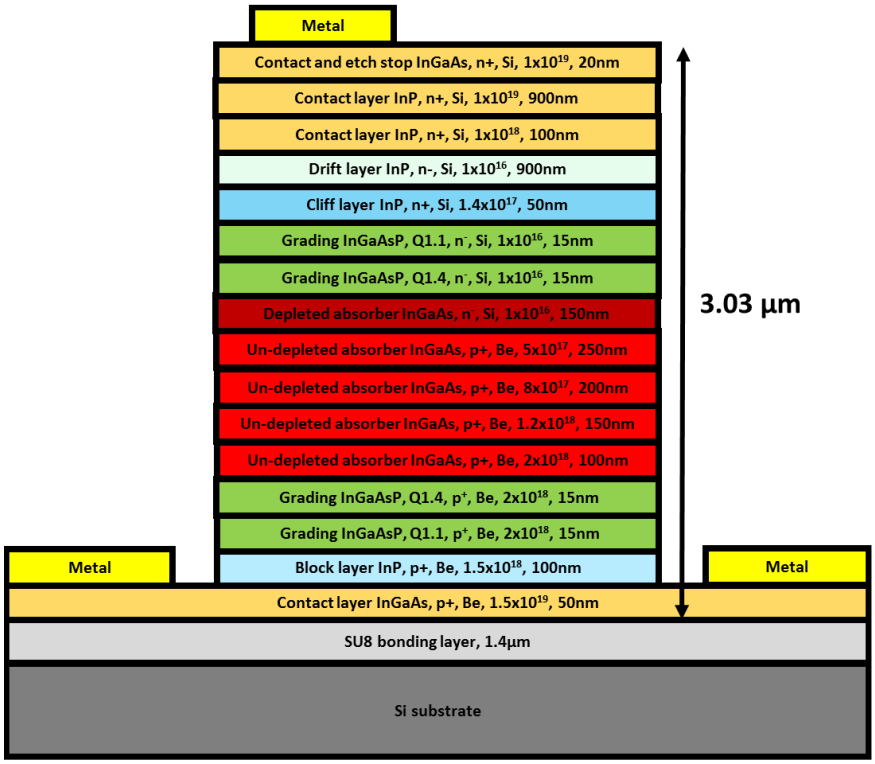


Figure 7.16 Epitaxial layer structure of fabricated photodiode

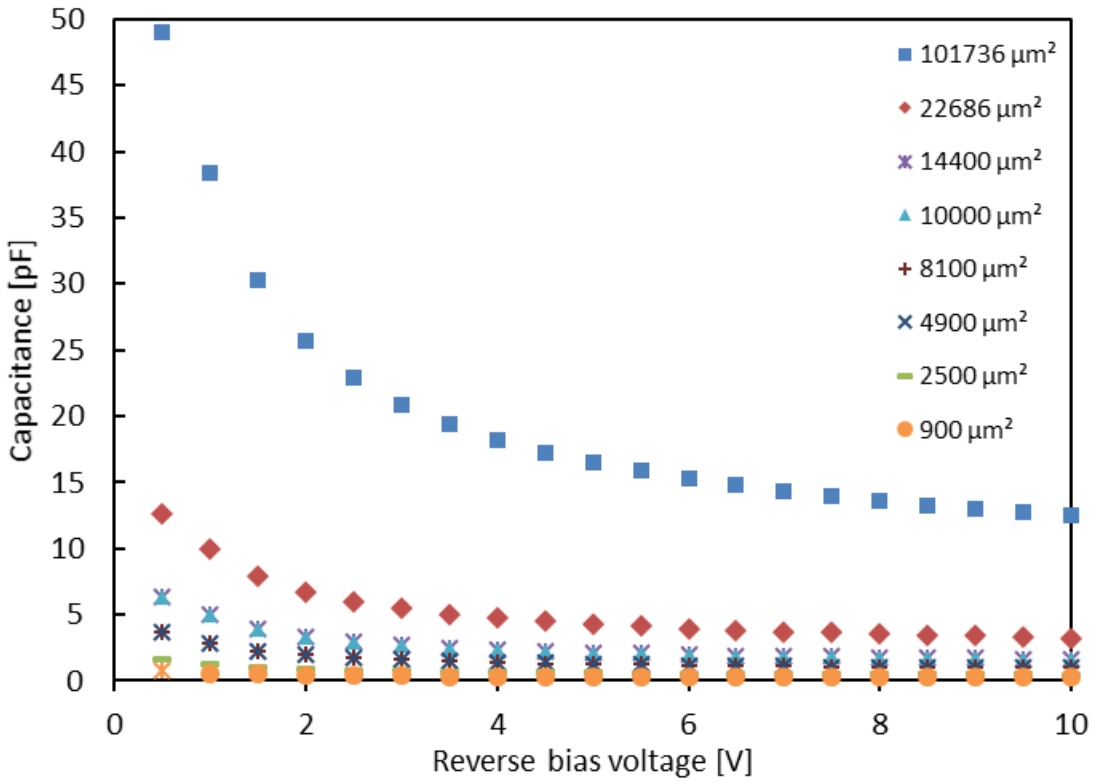


Figure 7.17 C-V curves of different photodiode areas measured at 100 kHz

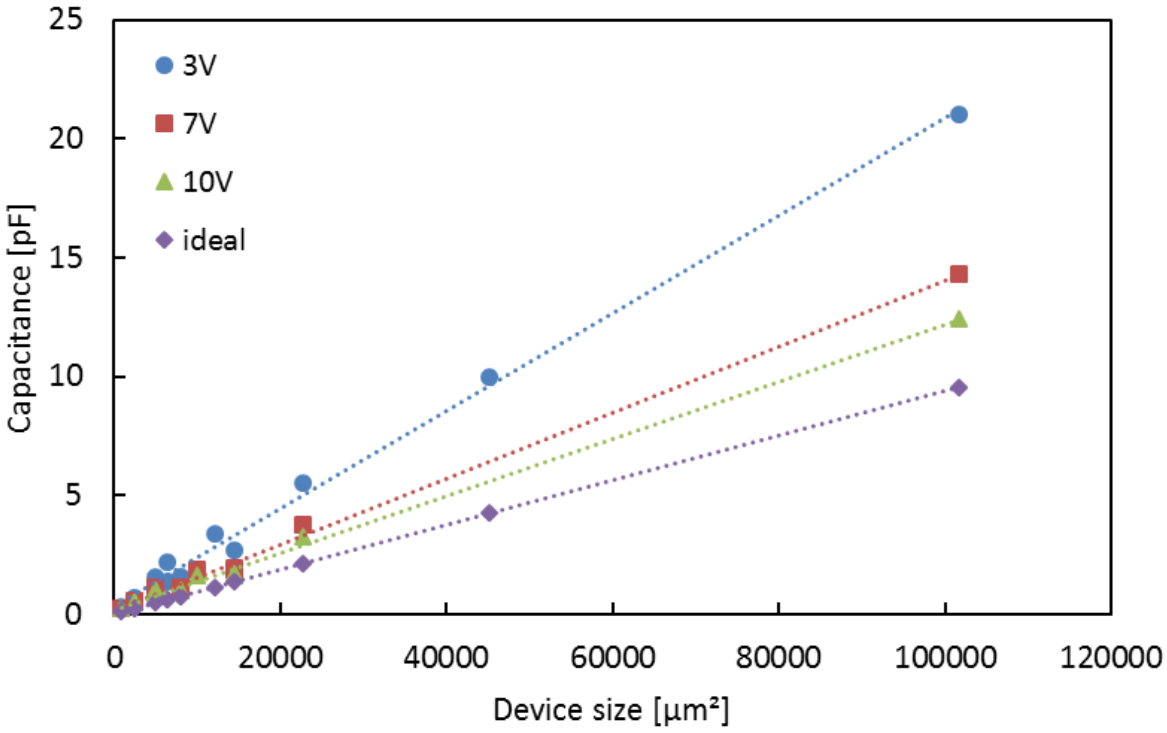


Figure 7.18 Measured capacitance vs. photodiode area at different bias voltages

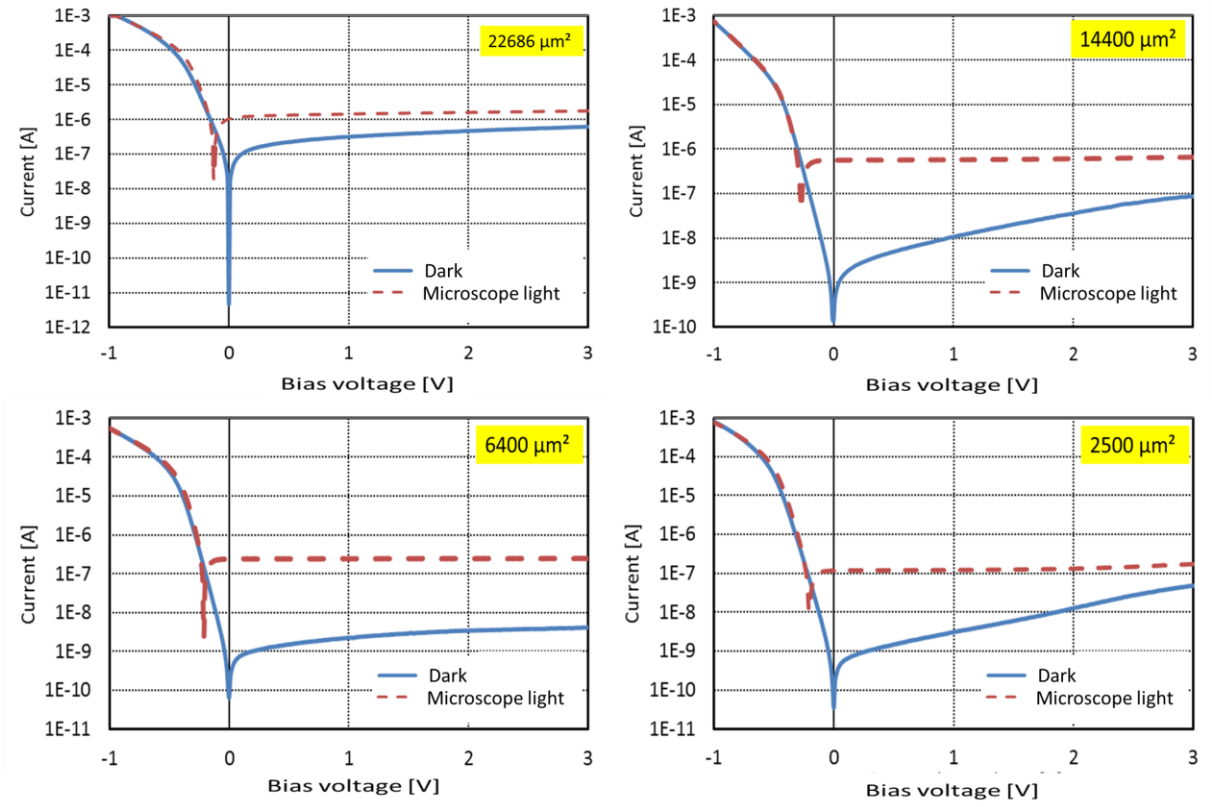


Figure 7.19 Measured I-V curves

Chapter 8 Waveguide Photodiode Design for Adhesive Bonding

8.1 Optical Coupling Design

To make the previously described technology available for photonic-THz electronic integration, the ultimate goal is to develop high-efficiency and high-speed photodiodes that are heterogeneously integrated onto the SOI waveguide platform using SU8 as the bonding intermedia. As the first step, it is important to design an optical coupler that can efficiently transfer optical power from the SOI waveguide to the III-V waveguide or the absorber of photodiode. The coupling scheme used in chapters 4 and 5 is inefficient for SU8 bonded photodiodes, due to the fact that the absorber and the underlying optical waveguide are separated by a relatively thick low-index SU8 bonding layer. In order to couple light from the input waveguide into the photodiode, two types of optical coupling schemes, directional coupler and adiabatic taper coupler, are studied in this section. Both BPM and EME are used to investigate the coupling efficiency and robustness of the two designs. It turns out that due to better fabrication tolerances and design robustness, the taper coupler was selected in the waveguide

Material	Refractive index @ 1550 nm	Reference
Si	3.48	[89]
SiO_2	1.45	[90]
SU8	1.57	[81]
InP	3.17	[91]
$In_{0.53}Ga_{0.47}As$	3.56-i0.086	[6]
InGaAsP, Q1.1	3.26	[92]
InGaAsP, Q1.4	3.49	[92]
Gold	0.56-i9.8	[8]

Table 8.1 Refractive indices of materials used in the simulation

photodiode design. The refractive indices of the materials used in the simulations are summarized in Table 8.1.

8.1.1 Directional Coupler

Based on the coupled mode theory [74], when two waveguides are placed close to each other, the optical mode profile in one waveguide can penetrate through the separating dielectric and has a considerable amount of overlap with the adjacent waveguide. Under such condition, and if phase match in both waveguides is satisfied, light can be coupled from one waveguide into the other. By changing the coupling length, the coupling efficiency can be effectively tuned. A vertical Si to III-V directional coupler

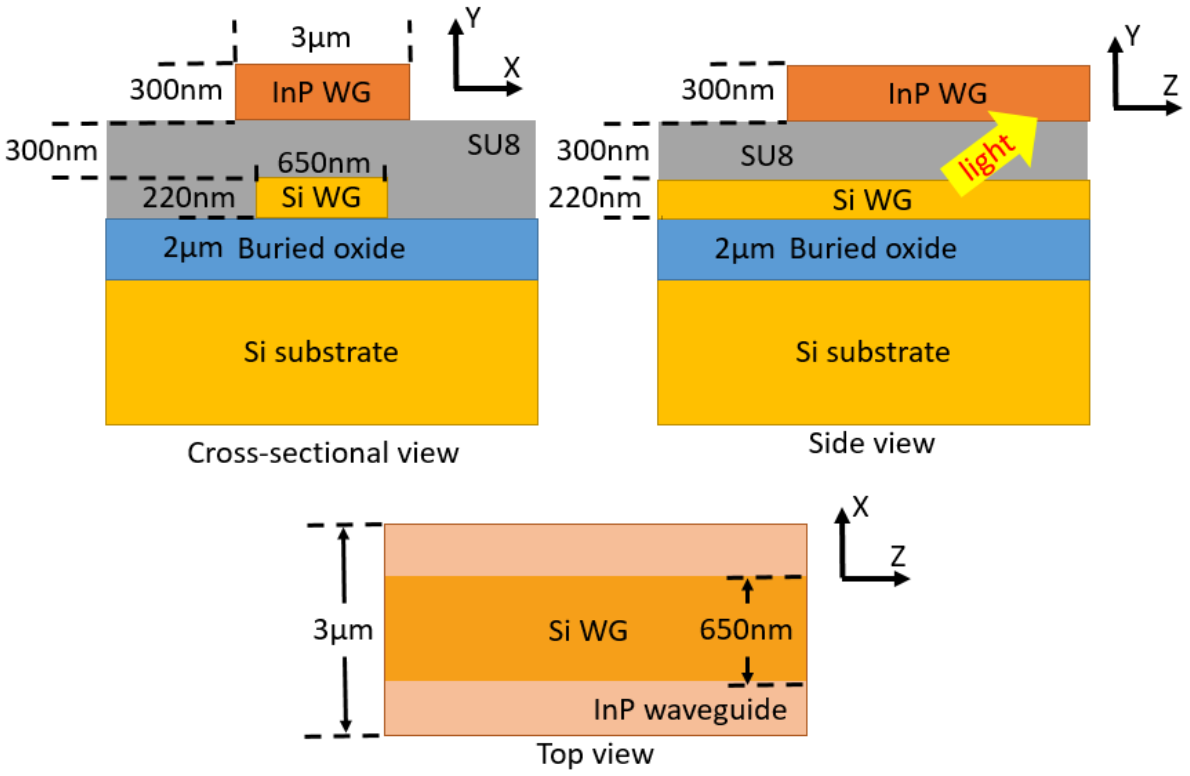


Figure 8.1 Directional coupler

similar to the one in [69] is used as my design starting point (Figure 8.1).

Simulation by BPM

In order to determine the optical coupling efficiency from the Si waveguide into the InP waveguide with the dimensions given in Figure 8.1 a BPM simulation was conducted. Figure 8.2 shows the normalized optical power along the propagation direction in the directional coupler (no photodiode). From Figure 8.2 we find that 75% of the optical power couples into the InP waveguide from the underlying Si waveguide within a coupling length of 25 µm. As a check of the robustness of the design against growth variations, the same simulation was carried out with an InP waveguide layer which is 5%

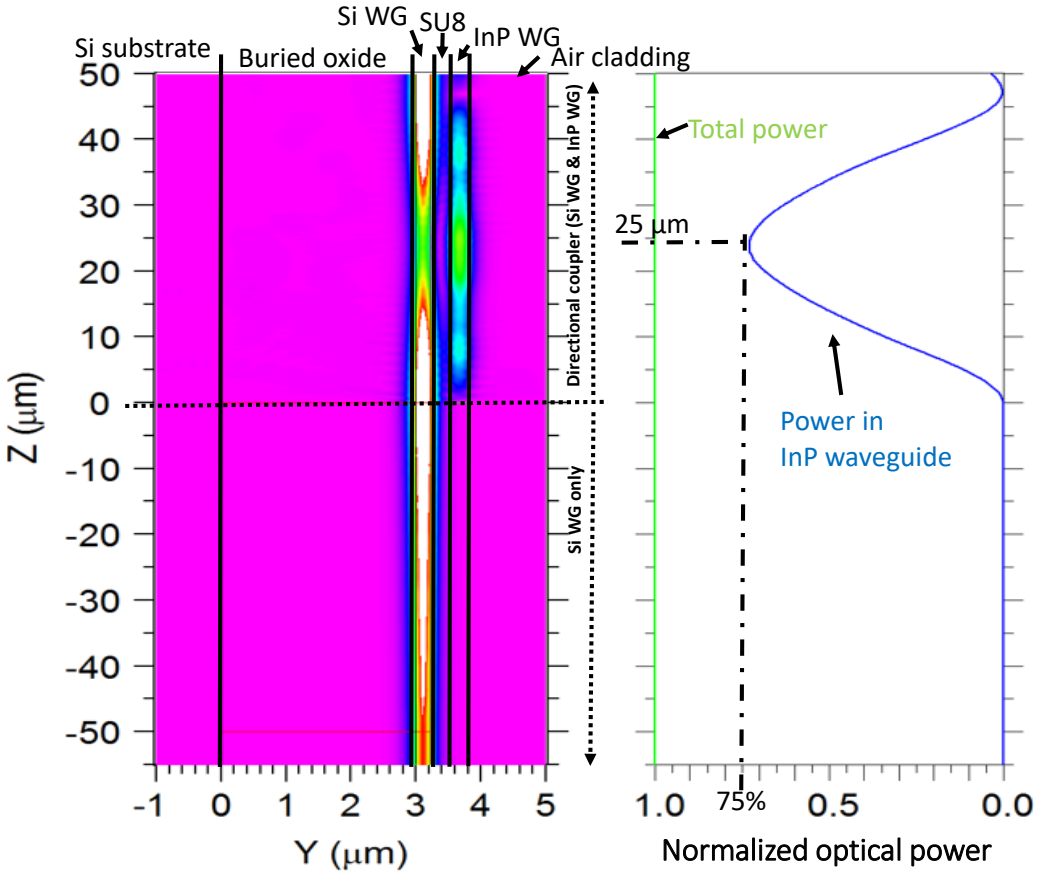
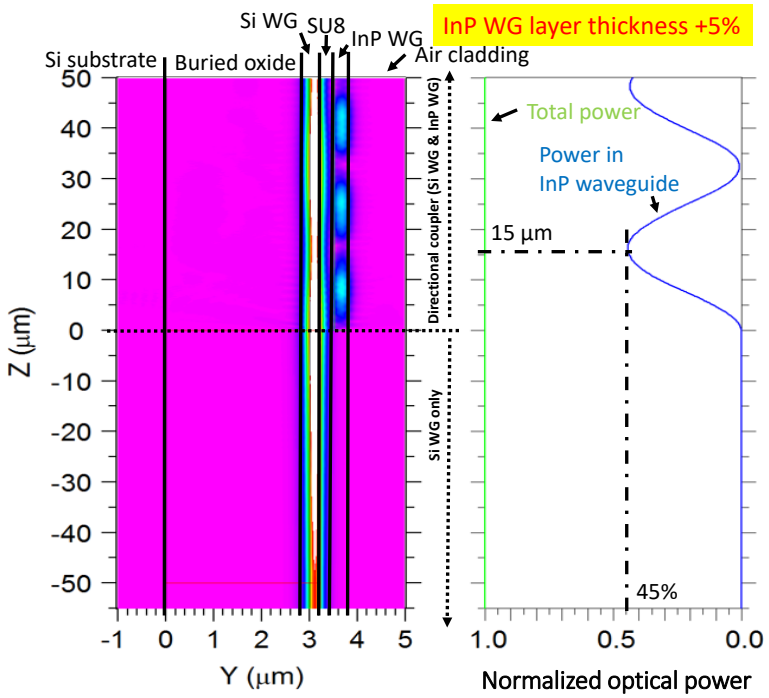
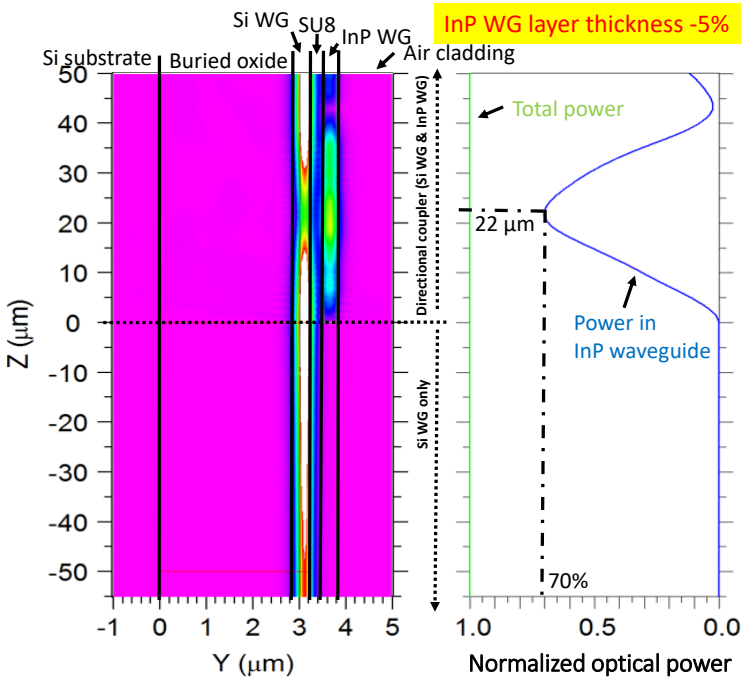


Figure 8.2 Optical power coupling simulation of directional coupler in BPM (TE)

thicker (Figure 8.3a) and 5% thinner (Figure 8.3b). With the InP waveguide layer being 5% thicker, the coupling efficiency drops dramatically to 45%, and the optimal coupling length shifted to 15 μm. While the change for the thinner InP waveguide layer not as severe as the thicker case, the coupling efficiency still drops to 70%. It should be pointed out that ±5% deviation in layer thickness is unavoidable for any epitaxial wafer grower. As a result, the directional coupler design appears to be too sensitive to be practical. This conclusion will be confirmed by EME simulation technique in the next section as well. The design robustness check for the vertical geometry tends to be more critical than the one for the horizontal geometry, due to the fact that errors in the horizontal dimension can be easily compensated by vernierring the layout of the large amount of devices fabricated during each batch.



(a)



(b)

Figure 8.3 Robustness of InP waveguide layer thickness

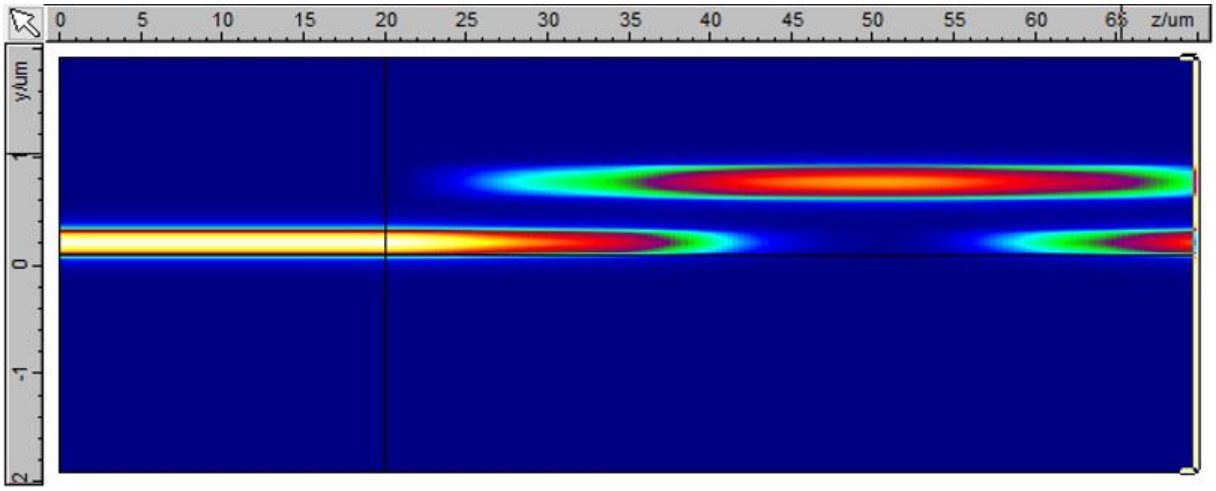
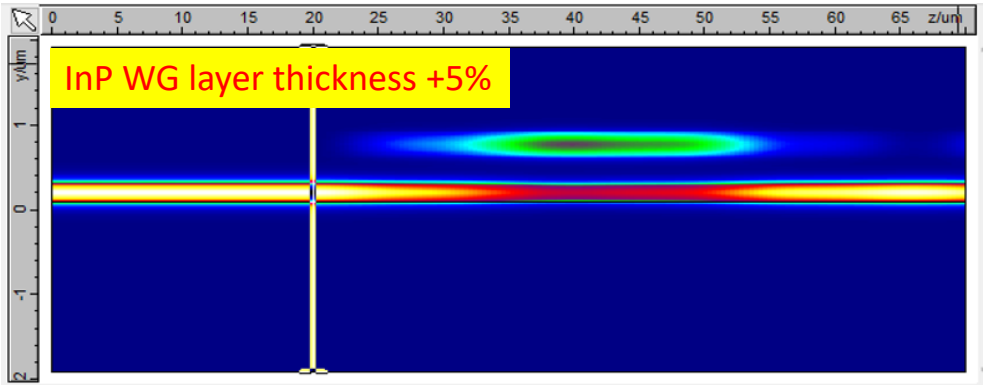
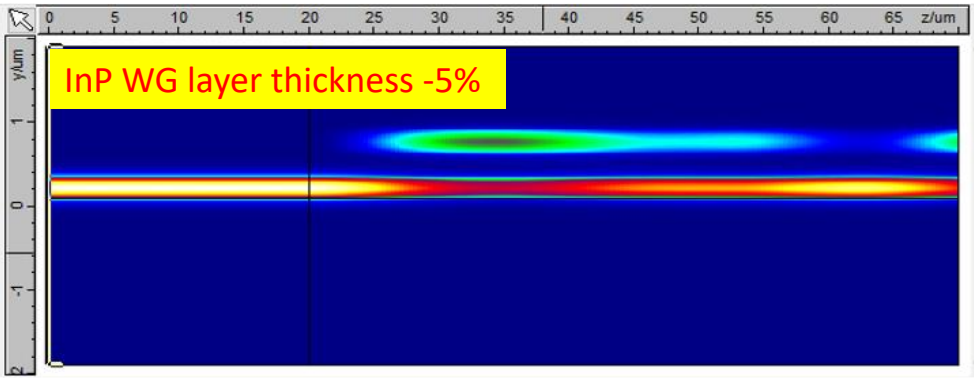


Figure 8.4 Power coupling simulation of directional coupler in EME



(a)



(b)

Figure 8.5 Robustness of InP waveguide layer thickness

Simulation by EME

Figure 8.4 shows optical coupling simulation in directional coupler by EME. The coupling efficiency is almost 100% within 25 µm coupling length. When the InP waveguide layer thickness is deviates from its target value by +5% (Figure 8.5a), the coupling efficiency drops to 15%. For -5% (Figure 8.5b), the coupling efficiency becomes 16%. Although these numbers do not quite match their BPM counterparts, the trend is similar, i.e. small variations in the waveguide layer thickness lead to drastic changes of the directional coupler behavior.

8.1.2 Adiabatic Taper Coupler

One method to ease the narrow tolerances of the directional coupler design is to adopt a tapered Si

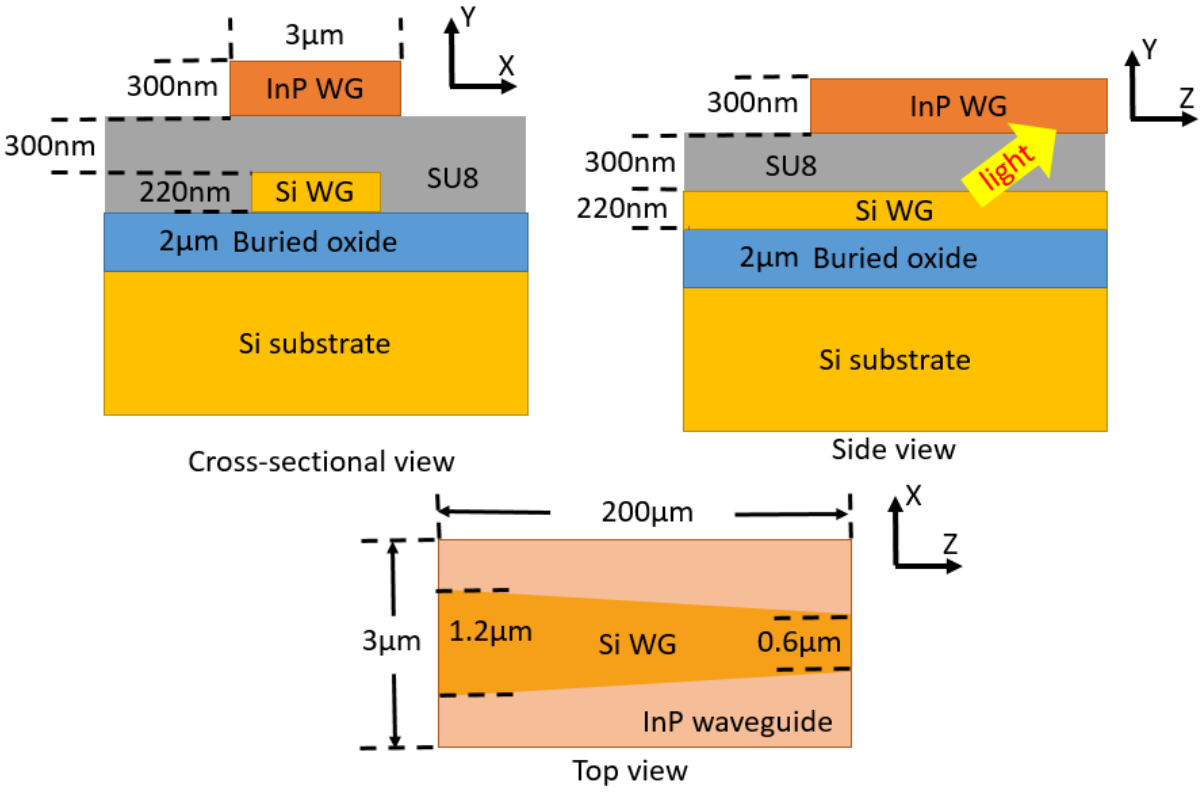


Figure 8.6 Taper coupler [69]

waveguide (Figure 8.6). The linear Si waveguide taper is an adiabatic taper, which means the waveguide width tapers down sufficiently slowly so that no power coupling occurs between modes in the waveguide taper. Supermodes with intensity peaks in both, the Si waveguide and the III-V waveguide, are used to analyze the coupling phenomenon, and separated local modes in the Si waveguide or III-V waveguide are no longer accounted for. A taper coupler was previously studied in [69].

Simulation by BPM

Figure 8.7 shows the normalized optical power propagating along a 150 µm-long taper coupler (no photodiode). From the figure, it can be inferred that the taper coupler structure is lossless, as the total

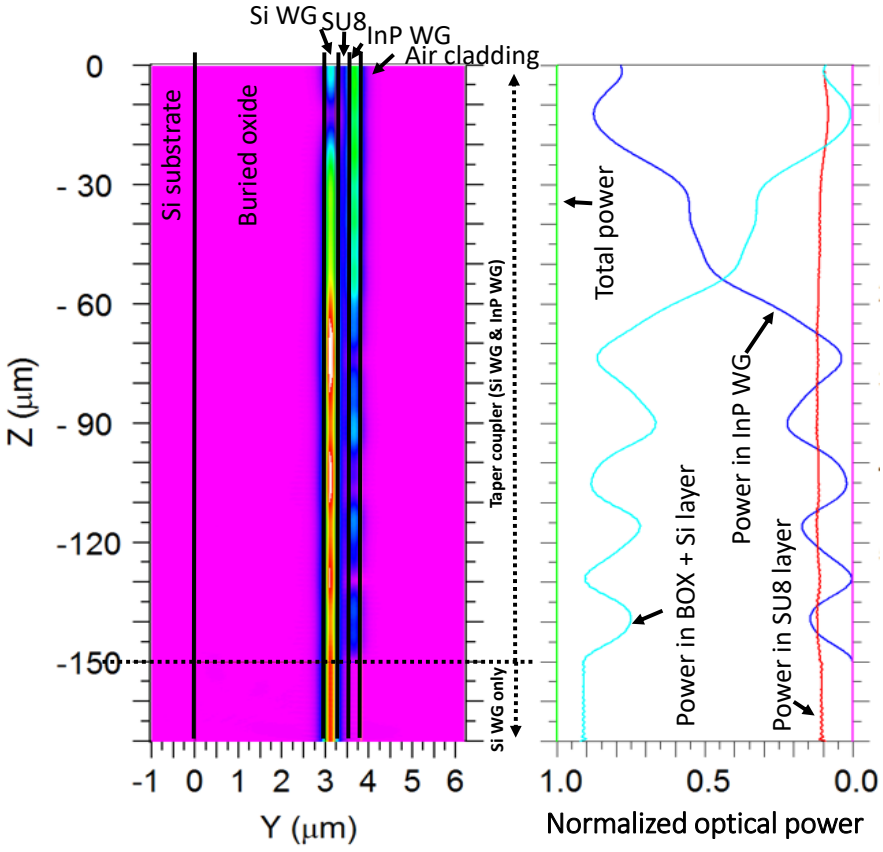


Figure 8.7 Power coupling simulation of taper coupler in BPM

power is 100% throughout the structure. In addition, coupling efficiency is up to 80% at the end of the taper coupler (80% power couples from Si waveguide into III-V waveguide).

Figure 8.8 shows the simulated coupling efficiency as a function of taper length under different InP waveguide layer thickness and SU8 thickness combinations. Both, the InP waveguide and the SU8 layer have a nominal thickness of 300 nm, and the deviation percentage is set to be ±10%. Thickness deviations in both layers can be effectively compensated by elongating the taper length. Also, the thickness of the InP layer has larger impact on the coupling efficiency than the SU8 layer has. A thinner (-10%, 270 nm) InP layer can drop the coupling efficiency to 55%, which is still tolerable, at the end of a 200 µm-long taper coupler. For any other deviation combinations without thin InP, coupling efficiency can be as high as 85%, which suggests that the tapered coupler design can ease the strictness of the InP and SU8 layer thickness requirements during epitaxial growth and etching processes.

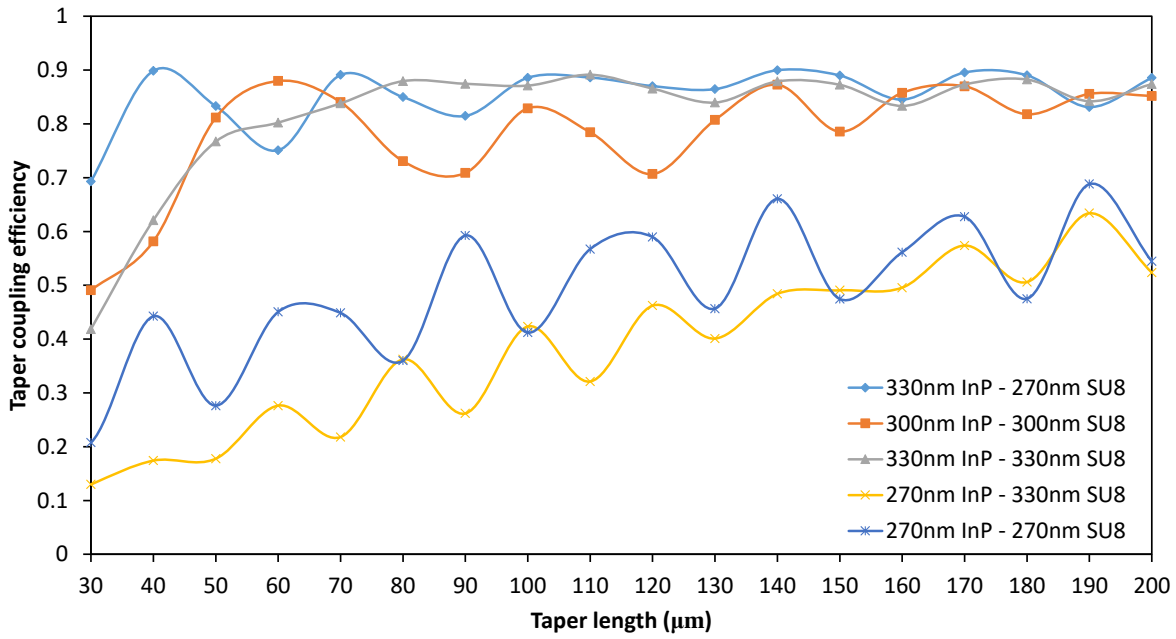


Figure 8.8 Robustness of InP waveguide layer and SU8 layer thickness

Simulation by EME

Figure 8.9 shows optical coupling simulation in taper coupler by EME. The coupling efficiency is ~92% within 150 µm coupling length. Similar to Figure 8.8, Figure 8.10 shows the optical coupling efficiency as a function of taper length for different InP waveguide layer thickness and SU8 bonding layer thickness combinations. Again, both, the InP waveguide and the SU8 layer have a target thickness of 300 nm; the deviation percentage is set to be ±10%. In agreement with BPM simulations I found that the taper design can significantly ease the stringent requirements of the InP and SU8 thickness. Figure 8.11 further reveals how the taper coupler works by illustrating the optical intensity profile evolution at different positions of the taper coupler. At Z=0 position, most of the input optical power is confined within Si waveguide. As beam propagates, more and more optical power is coupled up into the InP waveguide (Z=100 µm, Z=200 µm).

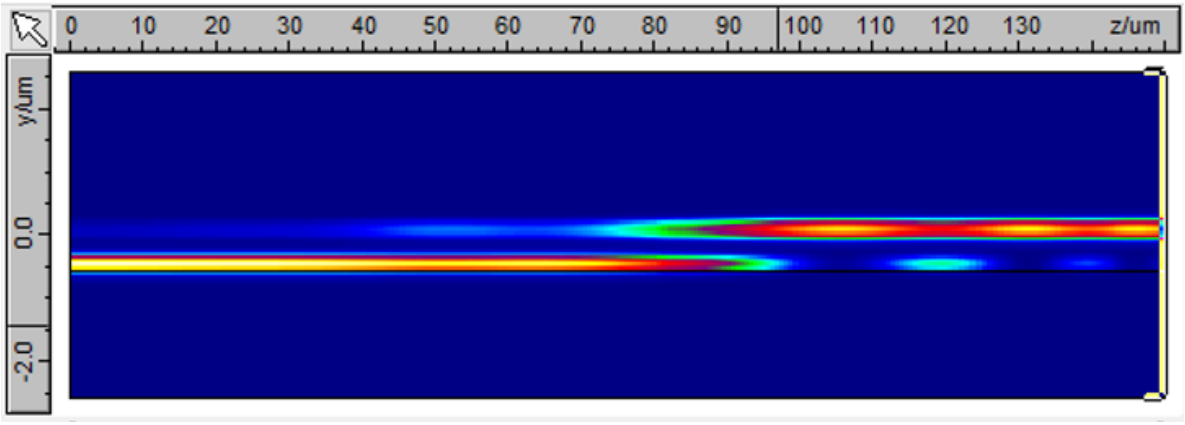


Figure 8.9 Power coupling simulation of taper coupler in EME

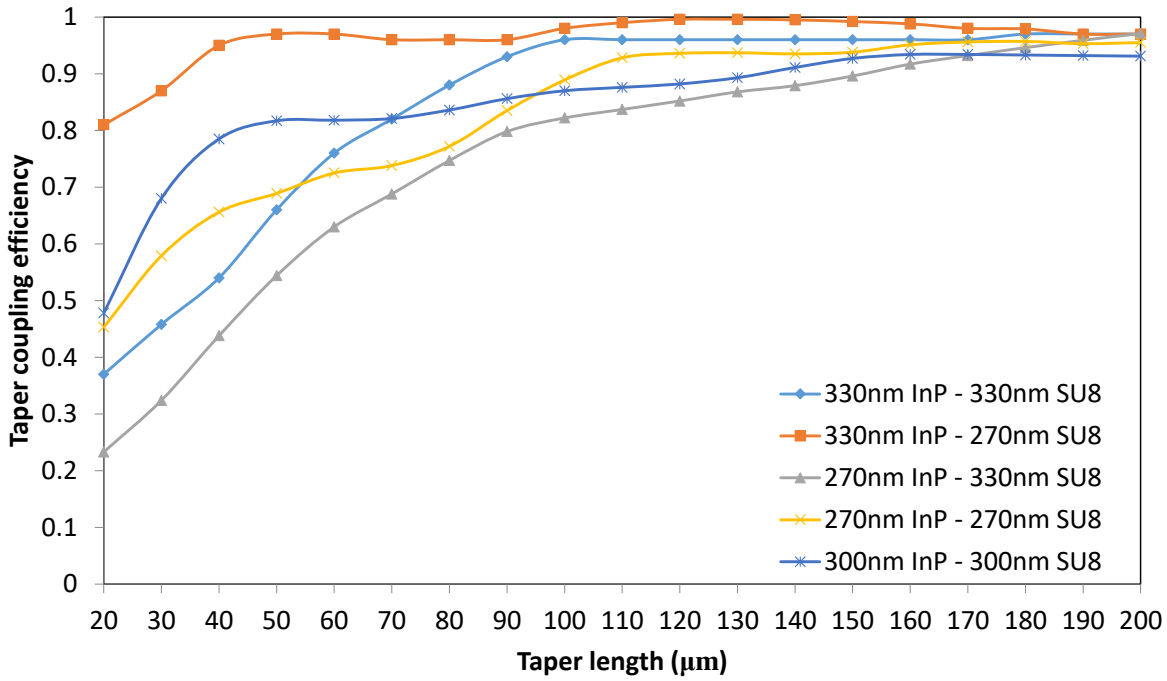


Figure 8.10 Robustness of InP waveguide layer and SU8 layer thickness

Comparison between two simulation techniques

Figure 8.12, Figure 8.13 and Figure 8.14 show a direct comparison between BPM and EME for different InP and SU8 thickness deviations and combinations. In Figure 8.12a,b and Figure 8.14e, the simulation results on coupling efficiency from BPM and EME match well with each other, suggesting a high coupling efficiency up to 95% for a length >150 μm of the taper coupler. In Figure 8.13c and d, the simulated coupling efficiencies from the two simulation techniques differ by 30% when the taper is longer than 150 μm. Although the simulation discrepancy is noticeable, both predict at least 65% coupling efficiency. One potential reason for the discrepancy could be that high-order radiation modes were not included in the EME simulation.

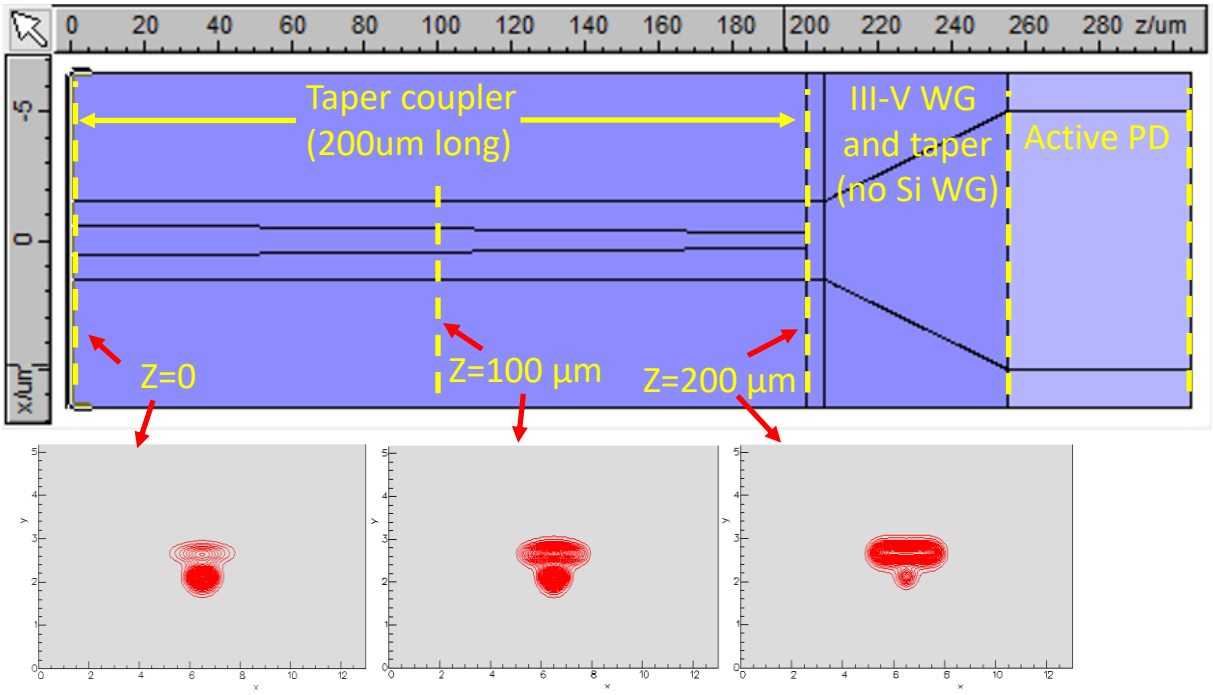
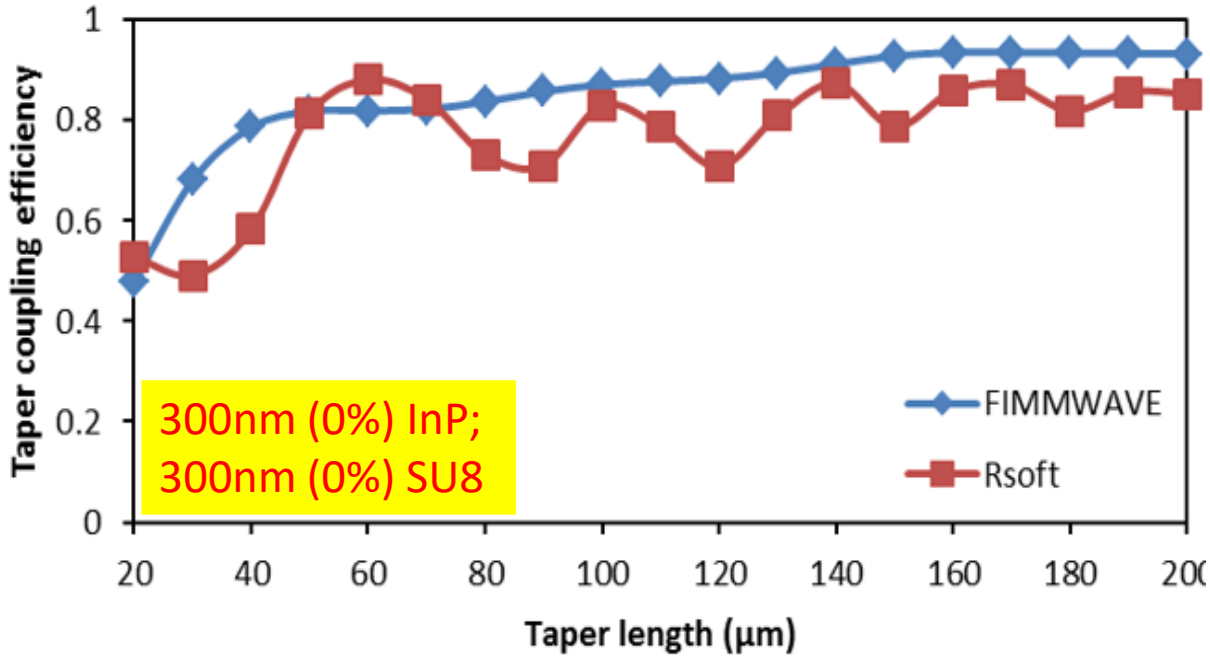
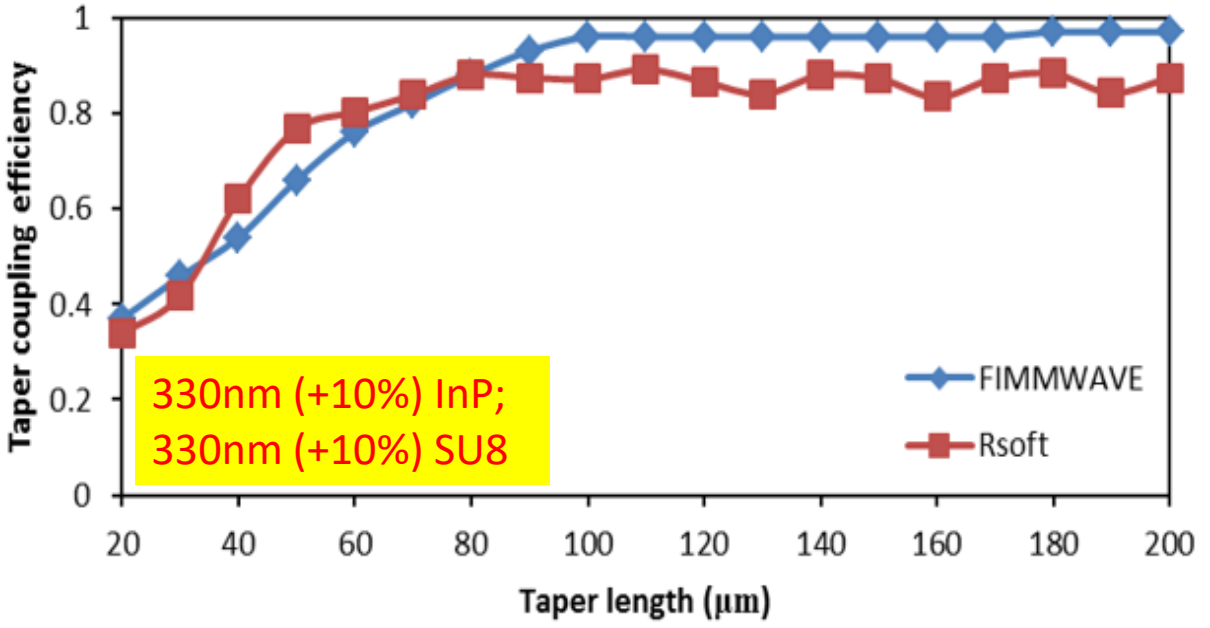


Figure 8.11 Cross-sectional view of optical intensity profile in taper coupler

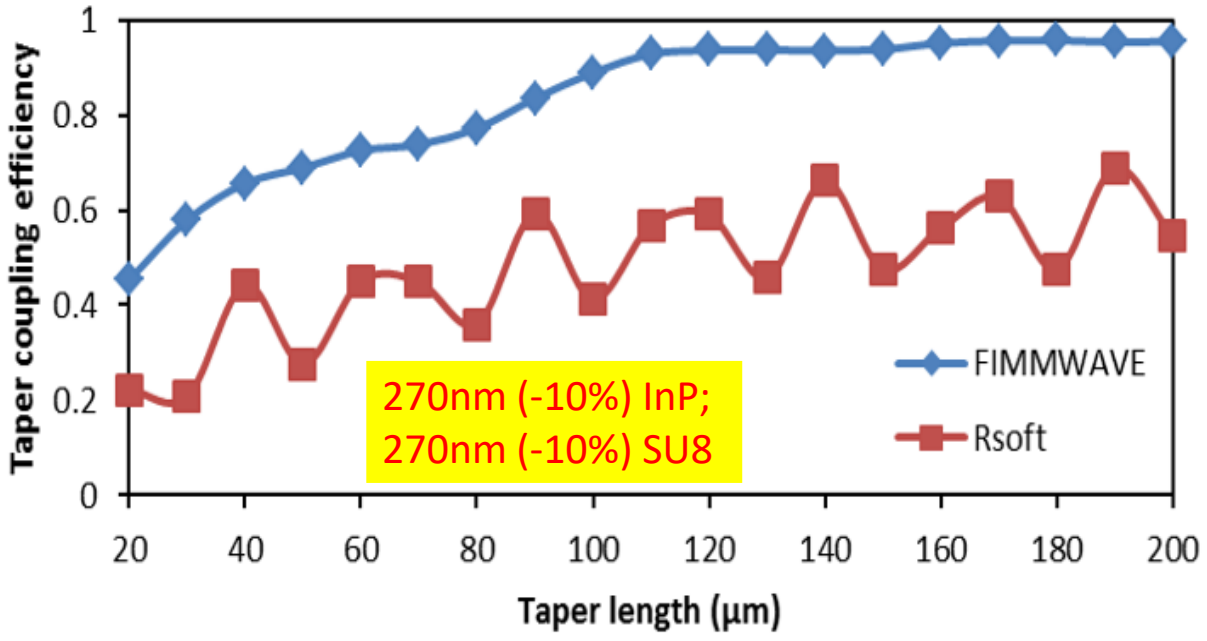


(a)

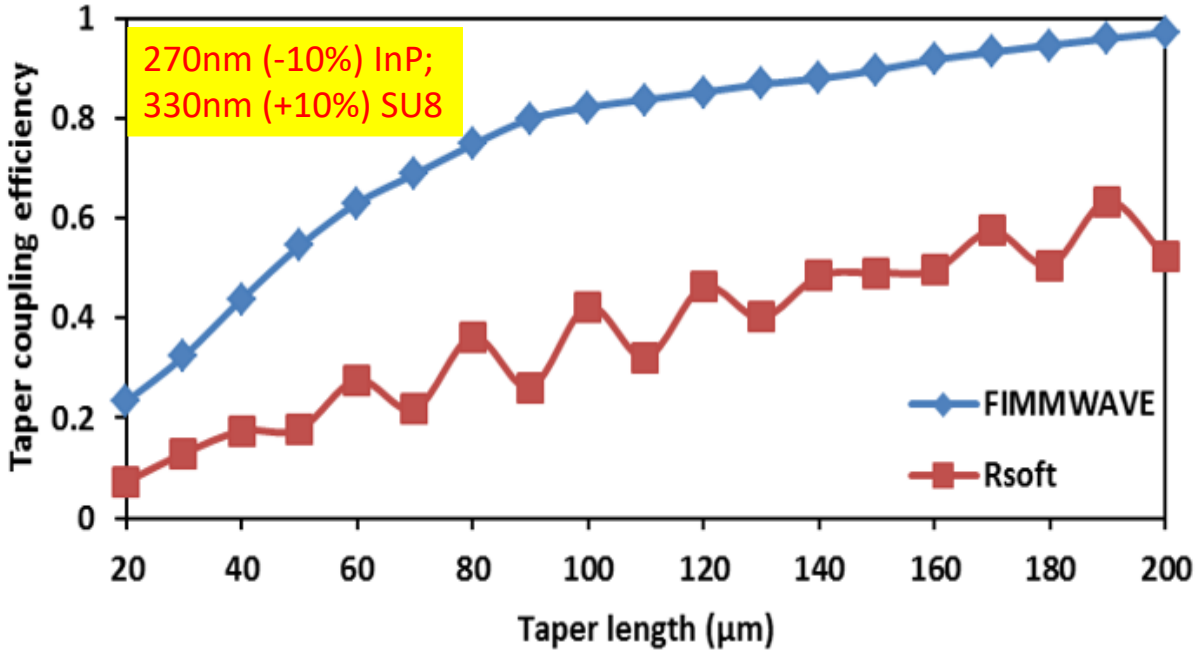


(b)

Figure 8.12 Robustness of InP waveguide layer and SU8 layer thickness



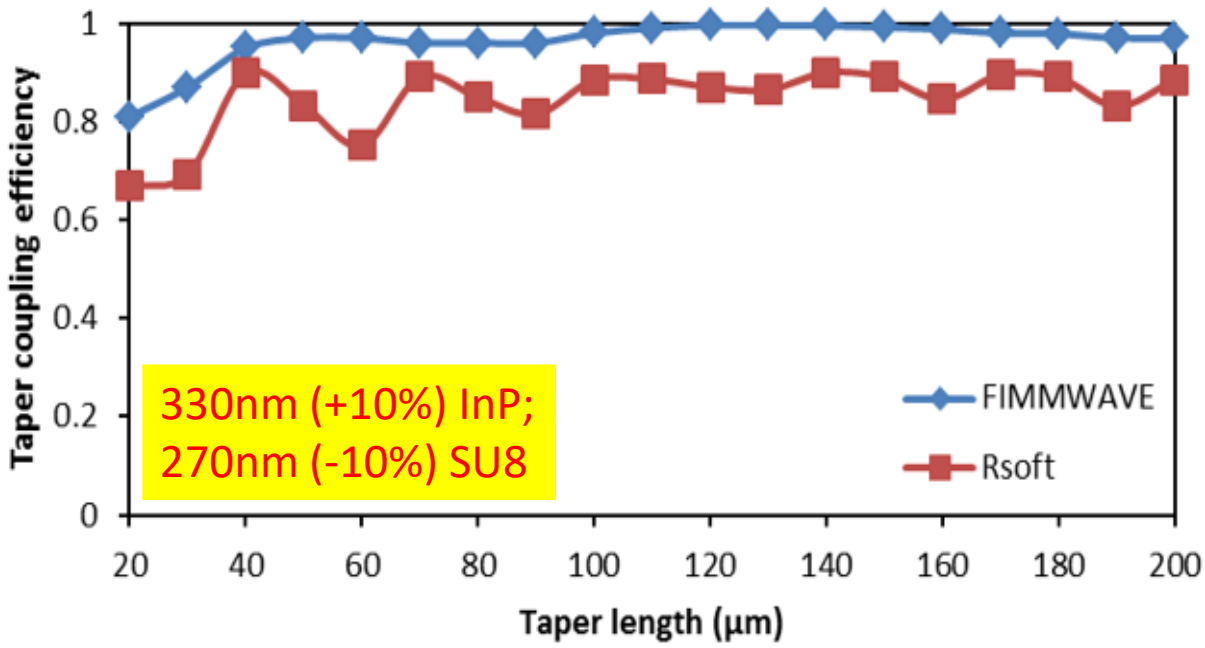
(c)



(d)

Figure 8.13 Robustness of InP waveguide layer and SU8 layer thickness (continued)

8.2.3 Conclusion



(e)

Figure 8.14 Robustness of InP waveguide layer and SU8 layer thickness (continued)

In order to couple light from a Si waveguide into an InP waveguide the directional coupler scheme revealed only small fabrication tolerances of less than 5 %. This is in contrast to the tapered coupler scheme, which shows reasonable tolerances on both, the InP waveguide layer and SU8 bonding layer thicknesses. The analysis showed that longer tapers make the design sufficiently robust against variations as large as 10%. Hence, I adopted the taper coupler design to proceed.

8.2 Epitaxial Structure Layout

The epitaxial structure that I used in my work is based on a previously developed structure (MUTC 12) that was reported in [44] by our group. Such type of structure with p-contact down is preferred for two reasons: first, I found that p-type doped InGaAs/InP is the most compatible and reliable bonding interface for the bonding process. No adhesion promoter is needed, yet the bonding quality is very good. Second, the InGaAs absorber is placed directly above the InP waveguide layer. As a result the

relatively thick (250 nm) and low index (n=3.18 @ 1550 nm) InP drift layer does not impede optical coupling. Compared to MUTC12, I reduced the drift layer thickness to 250 nm for high speed performance up to 164 GHz, and changed the bonding layer to 30 nm InGaAs to avoid de-bonding during substrate removal. (Figure 8.15). In addition, the thickness of the InP p-contact is reduced from 350 nm to 300 nm.

InP Substrate	
N doping, InGaAs, 3e19, 100nm	Contact layer
N doping, InP, 3e19, 100nm	Block layer
N doping, InP, 1e16, 250nm	Drift layer
N doping, InP, 1e17, 10nm	Cliff layer
N doping, InGaAsP, Q1.1, 1e16, 20nm	Smooth layer
N doping, InGaAsP, Q1.3, 1e16, 20nm	
N doping, InGaAs, 1e16, 60nm	Depleted, undepleted absorber
Graded P doping, InGaAs, from 5e18 to 8e19, 200nm	
P doping, InGaAsP, Q1.3, 1e19, 20nm	Smooth layer
P doping, InGaAsP, Q1.1, 1e19, 20nm	
P doping, InP, 1e19 (as high as possible, >1e18), 300nm	WG layer
P doping, InGaAs, 1e16, 30nm	Bonding/Cap layer

Figure 8.15 Epitaxial structure of MUTC15

8.3 Performance Simulation

To simulate the photodiode responsivity, I included a 100 µm-long MUTC 15 structure after the taper coupler (Figure 8.16). Simulations were carried out using both software programs, FIMMWAVE and BeamPROP. It should be mentioned that the simulated structures differed in two minor aspects: first, in FIMMWAVE, there is an additional 50 µm-long III-V waveguide taper connecting the taper coupler and the active PD; second, in FIMMWAVE, the taper coupler is 200 µm long, while in BeamPROP the taper coupler is 150 µm. I included the waveguide taper in Fimmwave to achieve more reliable simulation results by avoiding the abrupt transition. This change should not impact the coupling

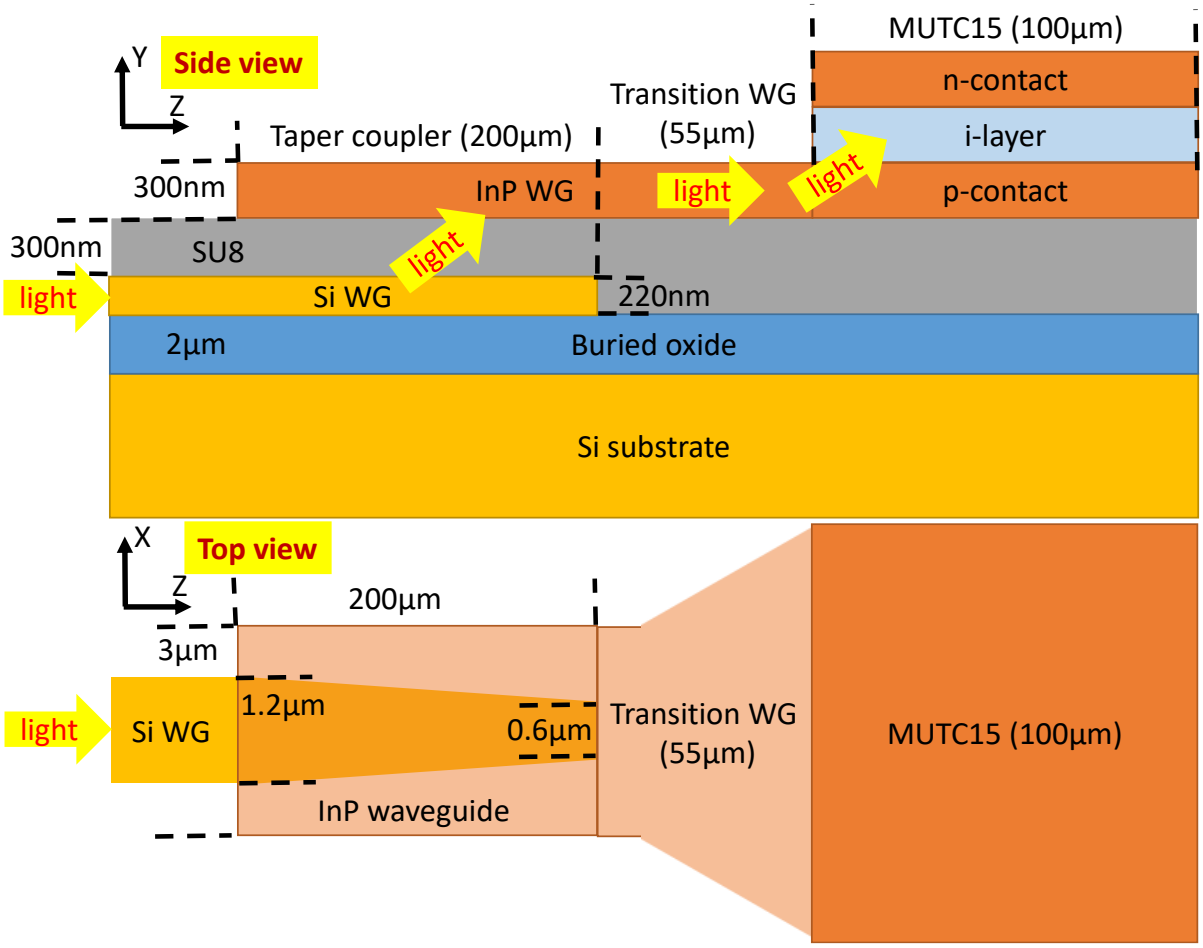


Figure 8.16 Side view and top view of taper coupler and MUTC15 active photodiode

efficiency as it was shown in the previous section, that the coupling efficiency between 150 µm-long taper coupler and 200 µm-long taper coupler is almost the same.

Figure 8.17 shows the mode coupling coefficients at the joint of the III-V transition waveguide and the active PD, and the mode loss α (mode energy decaying rate) due to absorption. The fundamental mode in the III-V transition waveguide is coupled into four modes (they add up to 100%) in the active PD, each mode has high absorption rate (compared to maximum theoretical mode loss of 6968/cm), which indicates high quantum efficiency.

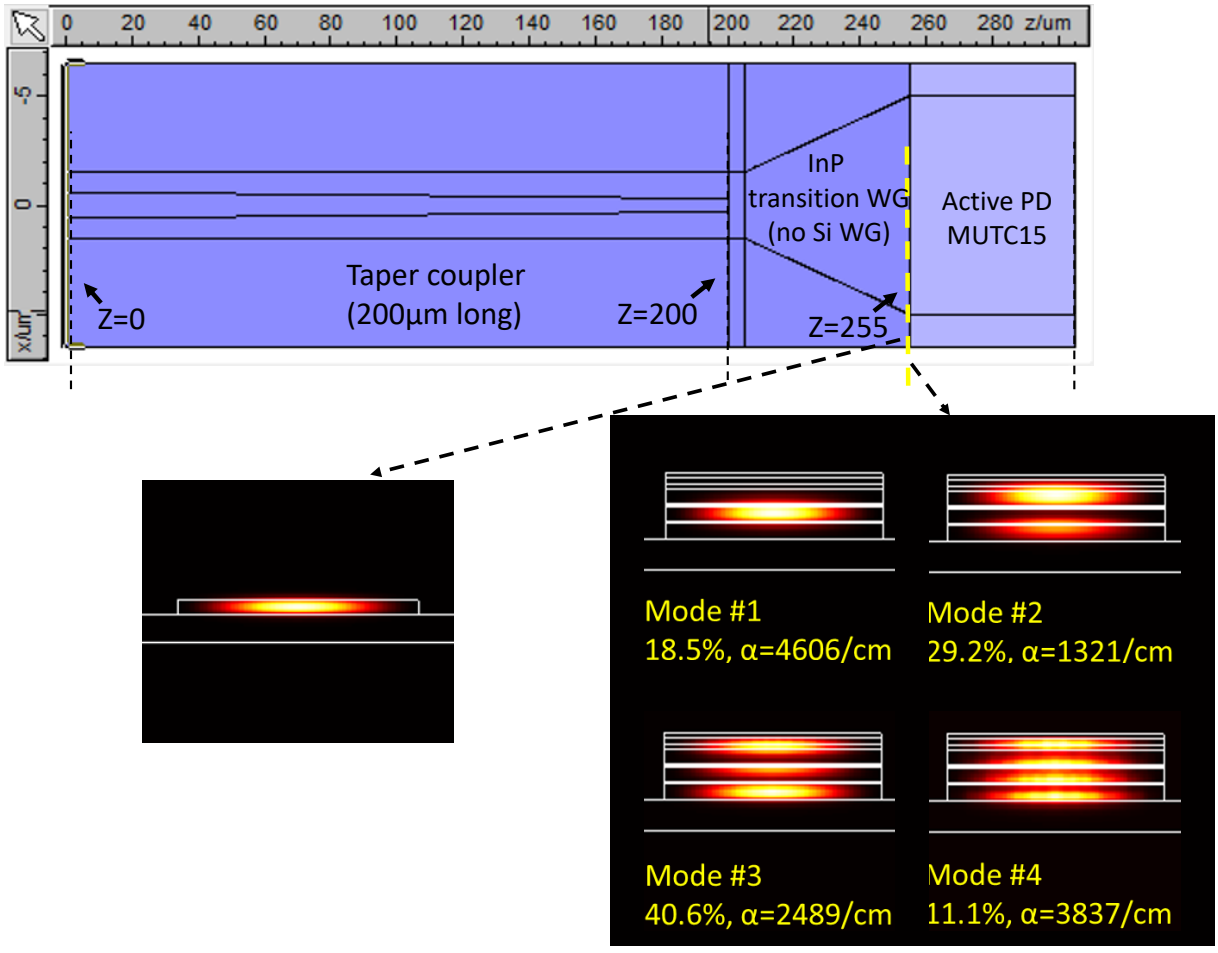


Figure 8.17 Mode coupling between III-V transition WG and active PD

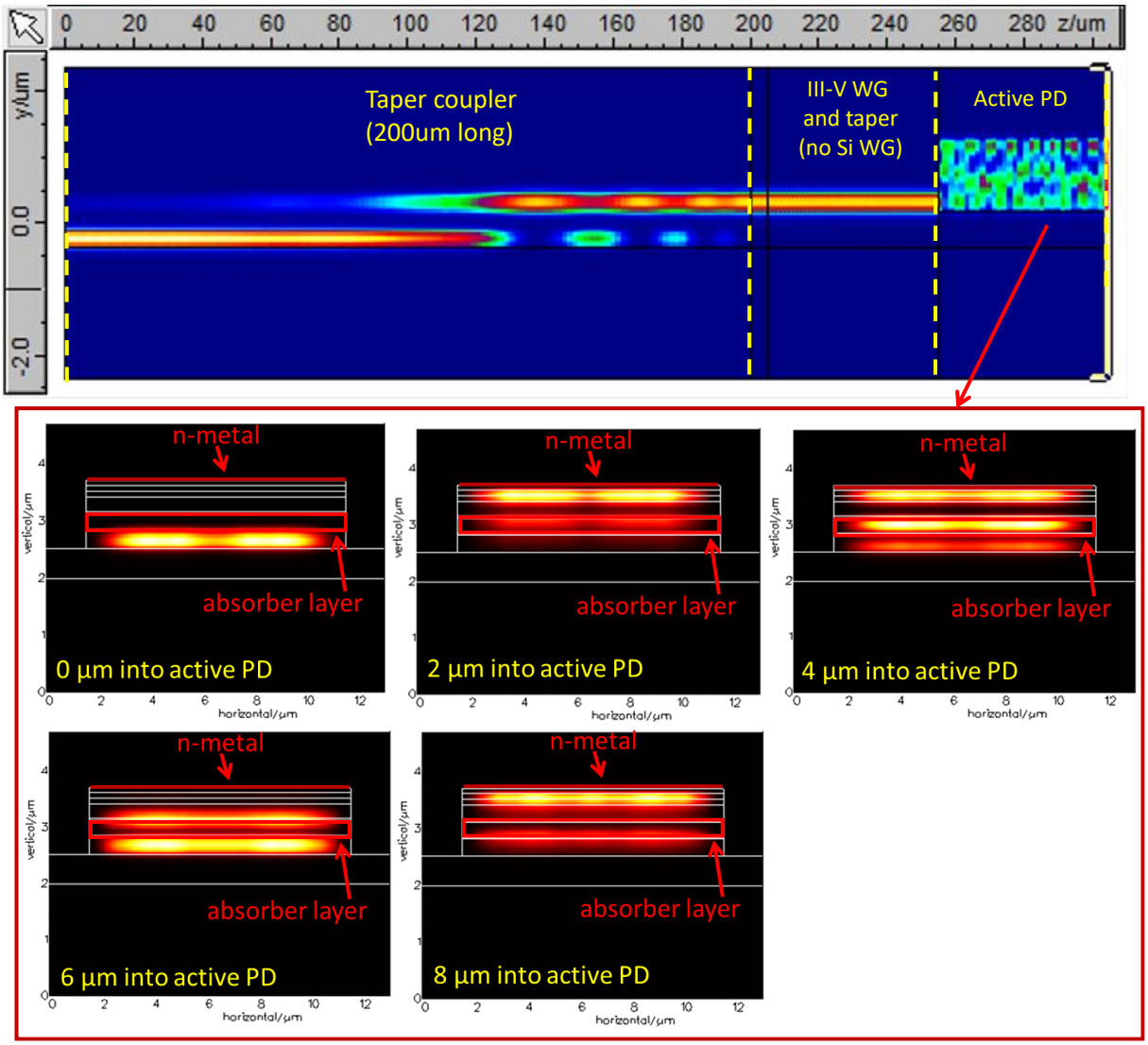


Figure 8.18 Mode beating in active PD (TE), no absorption

When the absorption in the active PD is turned off (no InGaAs and metal absorption), strong mode beating effects can be observed in the active PD region (Figure 8.18). The optical intensity profile at each position is also shown in Fig 8.18. The beat length can be estimated to be ~6 µm. Figure 8.19 shows the optical intensity when the absorption is turned on; the optical power vanishes within the first 7 µm inside the active PD.

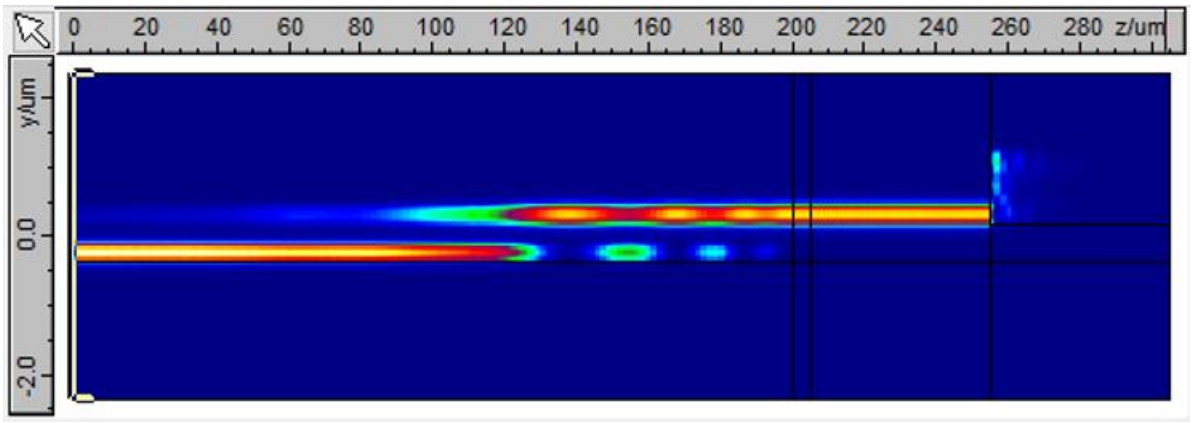


Figure 8.19 Optical intensity distribution with absorption

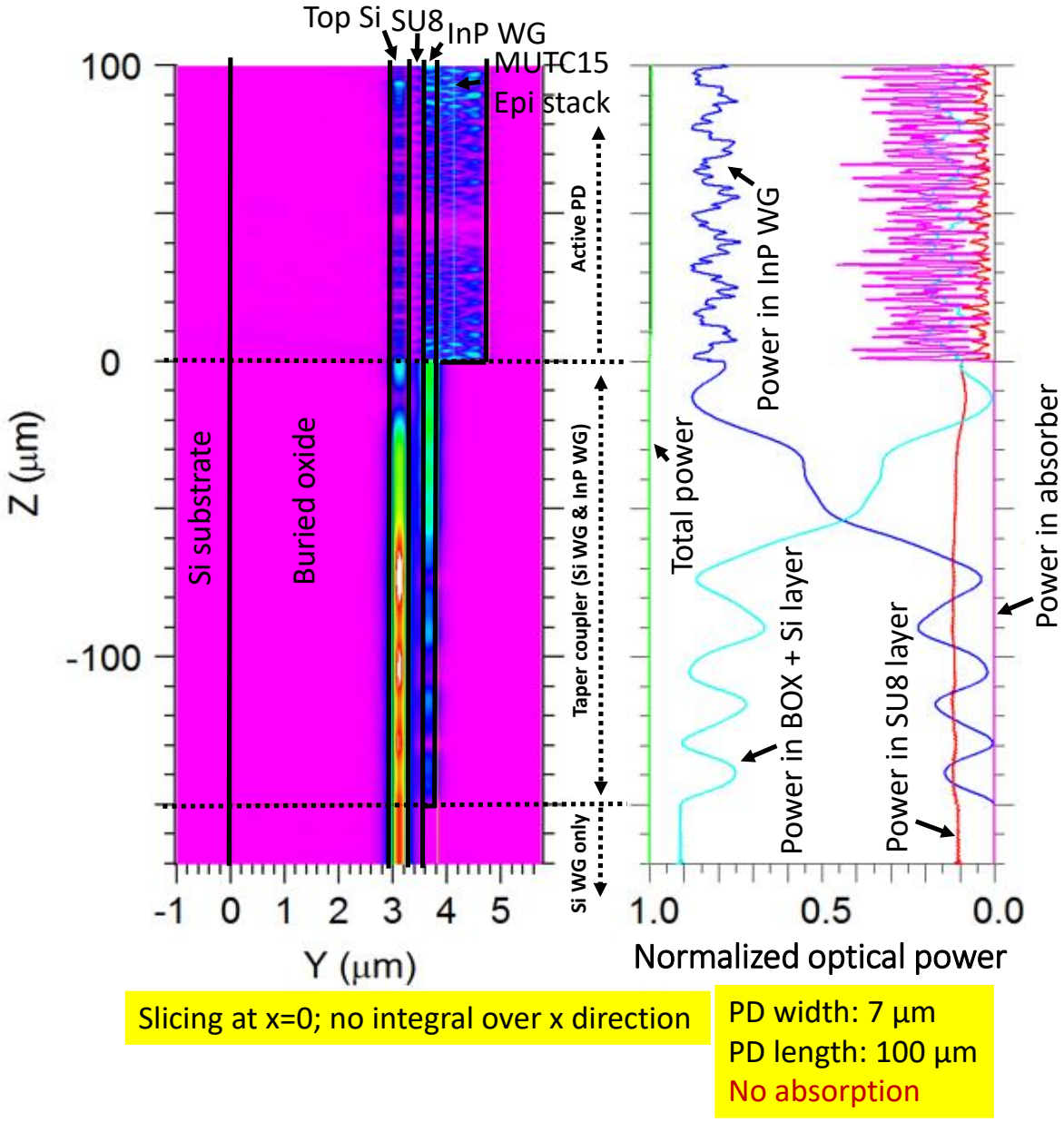


Figure 8.20 Normalized optical power along propagation (z-) direction without absorption in PD

A similar simulation was carried out in BeamPROP. First, the InGaAs and metal absorption is turned off to observe the mode beating effect and to verify that the structure is otherwise lossless. In Figure 8.20, the total power is 100% throughout the entire structure, which indicates the device is

lossless. In addition, 80% of the optical power is coupled from the Si waveguide to the III-V waveguide and active PD. Mode beating effects can be clearly seen.

After turning on the InGaAs and metal absorption, the total power drops dramatically to 15% within the first 7 μm in the active PD. In order to confirm that the power drop is a result of InGaAs absorption (and thus contributes to the photocurrent, and not loss in the metal) two more simulations were conducted: InGaAs absorption only (Figure 8.21); and metal absorption only (Figure 8.22). It can be seen that the total power curve in Figure 8.21 (InGaAs absorption only) matches its counterpart curve in Figure 8.23 (InGaAs and metal absorption). In addition, at 7 μm position in the active PD, metal absorption can be seem to be only 10% from Figure 8.22. These results show strong evidence to support the conclusion that <10% of power is absorbed by the metal.

The calculated internal responsivity as a function of photodiode length, L_{pd} , is shown in Figure 8.24. Even for short PDs (7 μm), the responsivity can reach 0.45 A/W. Assuming a 7x7 μm² (50 μm²) photodiode, the RC limited 3-dB bandwidth (BW) is calculated to be 232 GHz, while the transit time limited bandwidth is 232 GHz. The overall bandwidth is estimated to be 164 GHz using equation 2-9 in [75]. A summary table comparing performances of this work, previous work from our group [11], results from chapter 4, Ghent's [57] and UCSB's [76] work is presented in Table 8.2. Our adhesively bonded waveguide photodiode predicts high efficiency, and ultra-high speed.

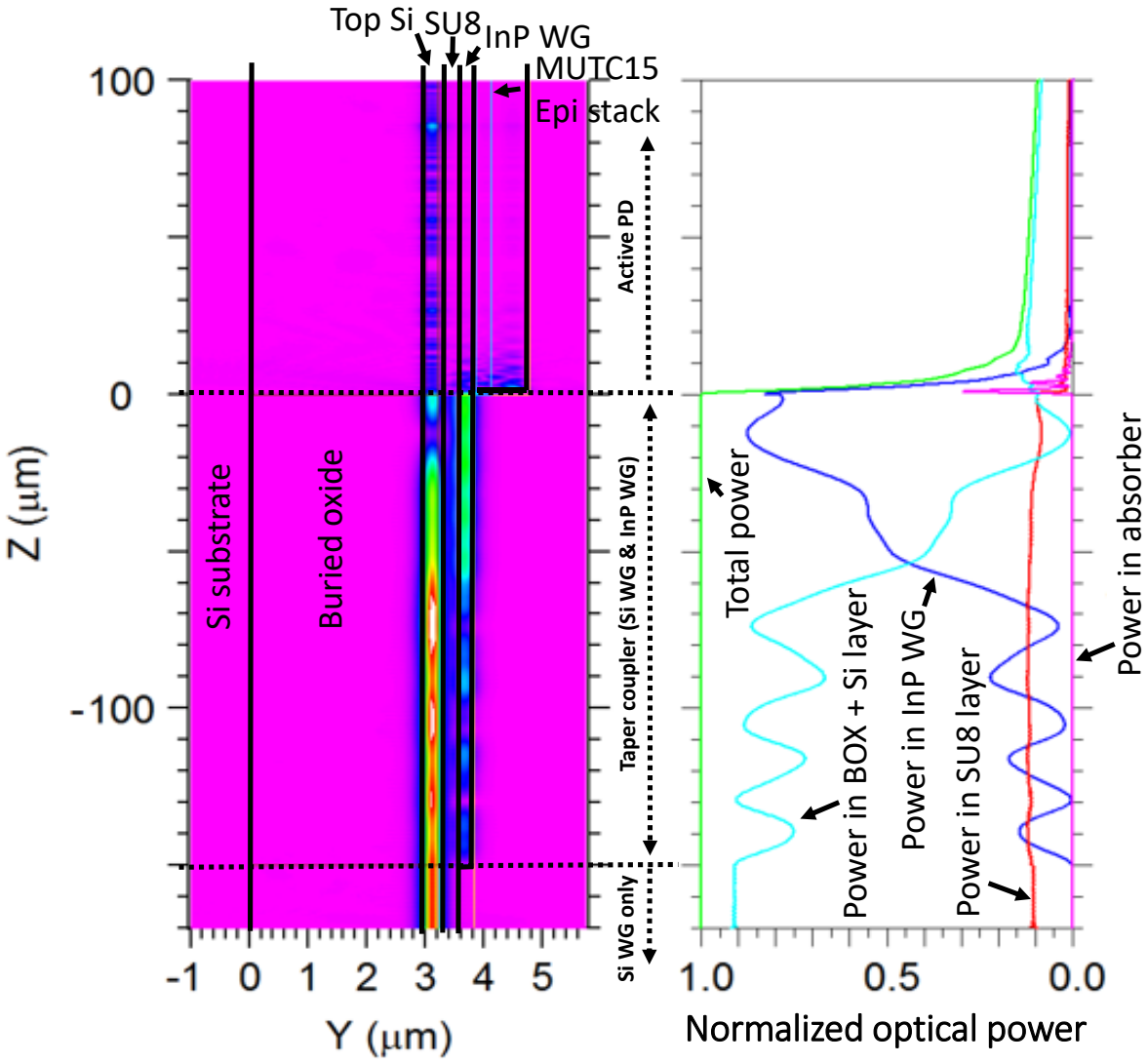


Figure 8.21 Normalized optical power along propagation (z-) direction with InGaAs absorption in PD

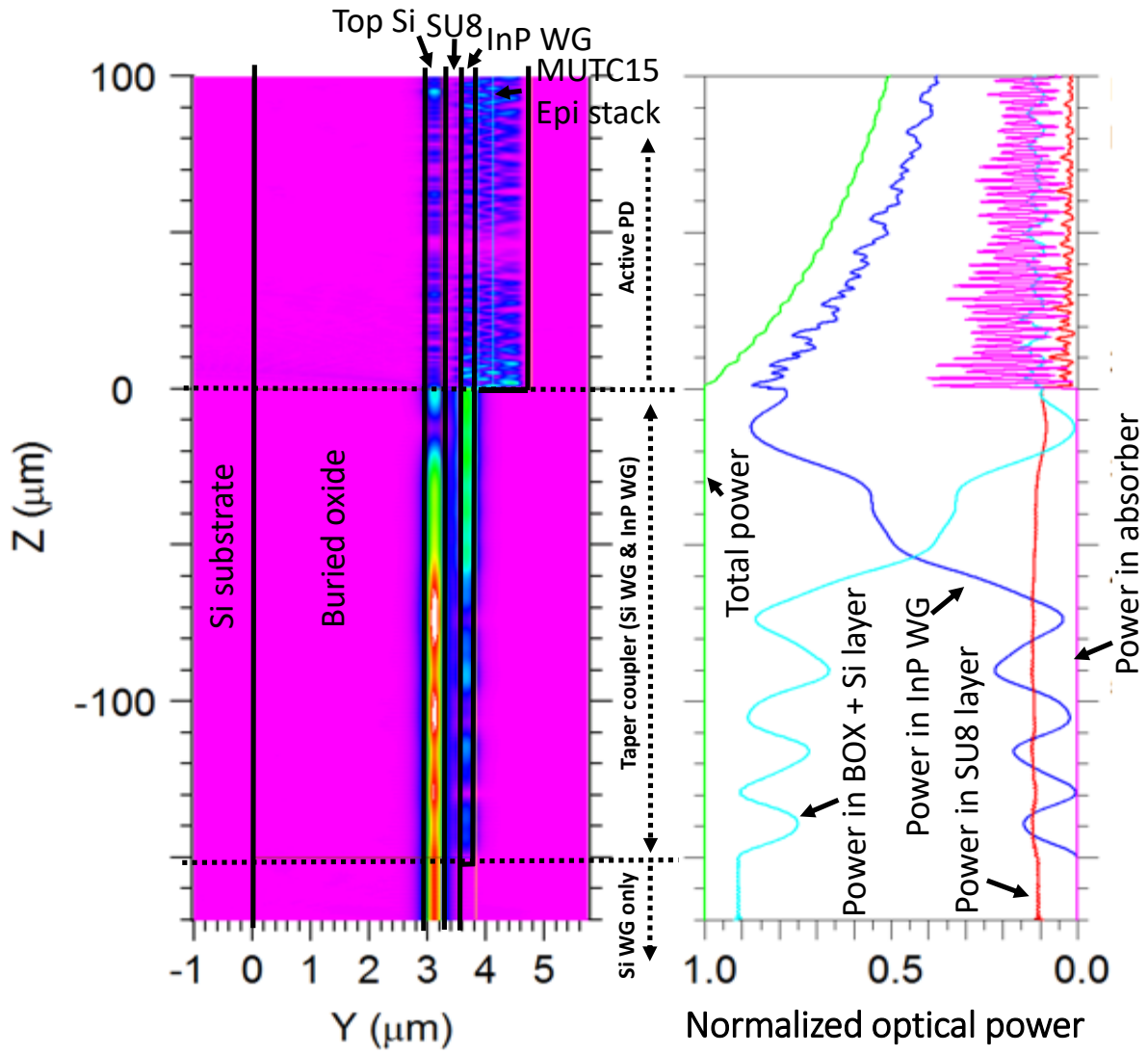


Figure 8.22 Normalized optical power along propagation (z-) direction with metal absorption in PD

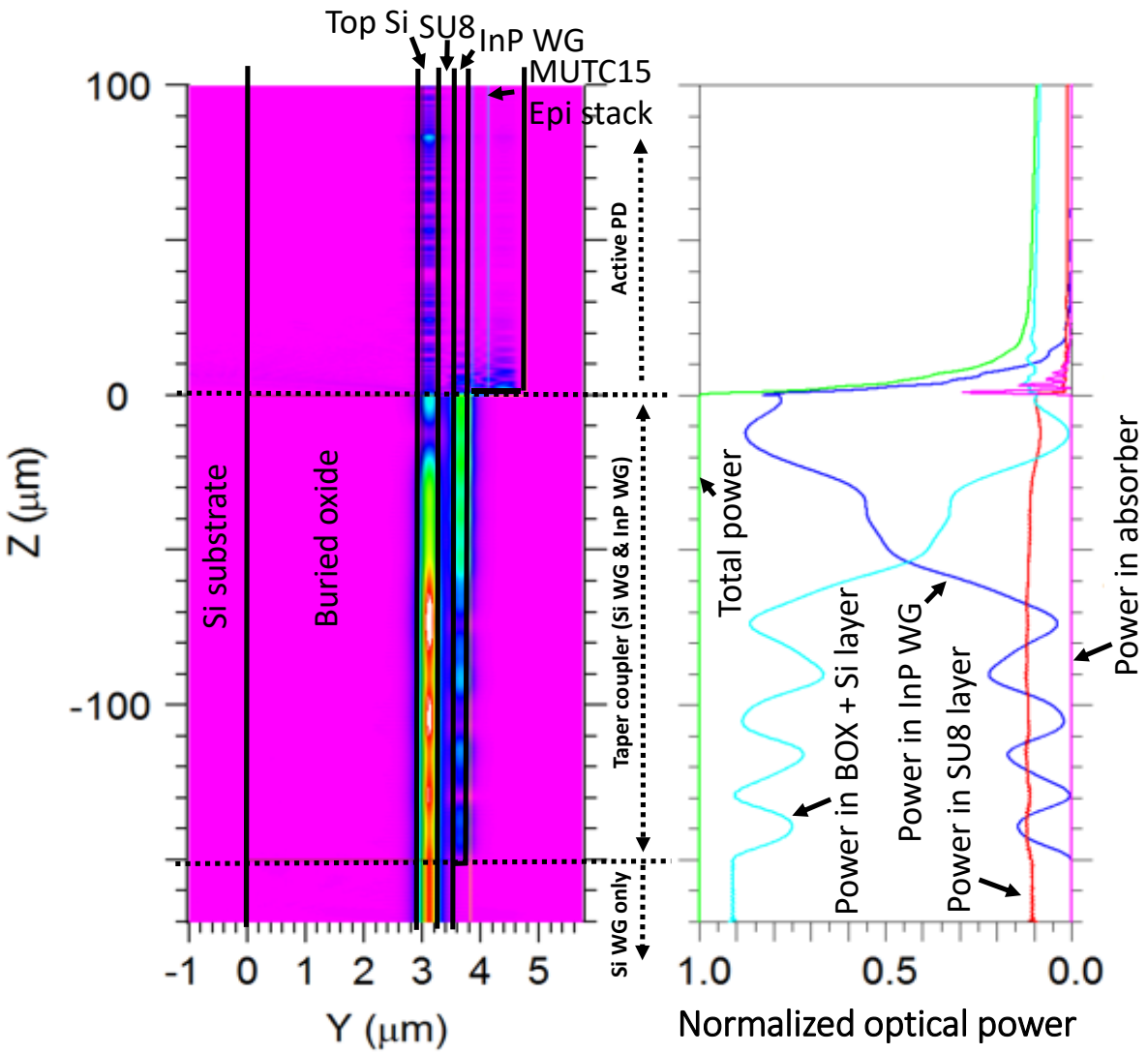


Figure 8.23 Normalized optical power along propagation (z-) direction with InGaAs & metal absorption in PD

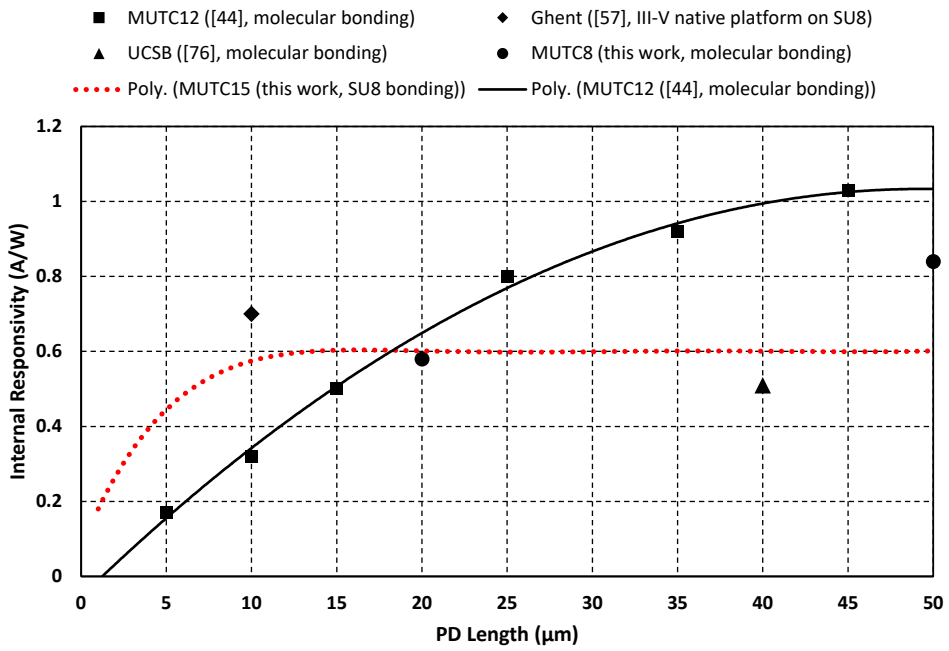


Figure 8.24 Responsivity vs. PD length (black solid line/ markers are experimental data, red dot line is simulated prediction)

	MUTC 15 (this work)	MUTC 12 [44]	MUTC 8 (this work)	Ghent [57]	UCSB [76]
R [A/W]	0.45	0.95	0.58	0.7	0.5
BW [GHz]	164	31	38.5	67	67
BW*efficiency [GHz]	59	23.5	17.8	37.5	25.6
Size [µm²]	7*7	10*35	10*20	3*10	3*40

Table 8.2 Performance comparison table

Chapter 9 Conclusion and Future Work

9.1 Conclusion

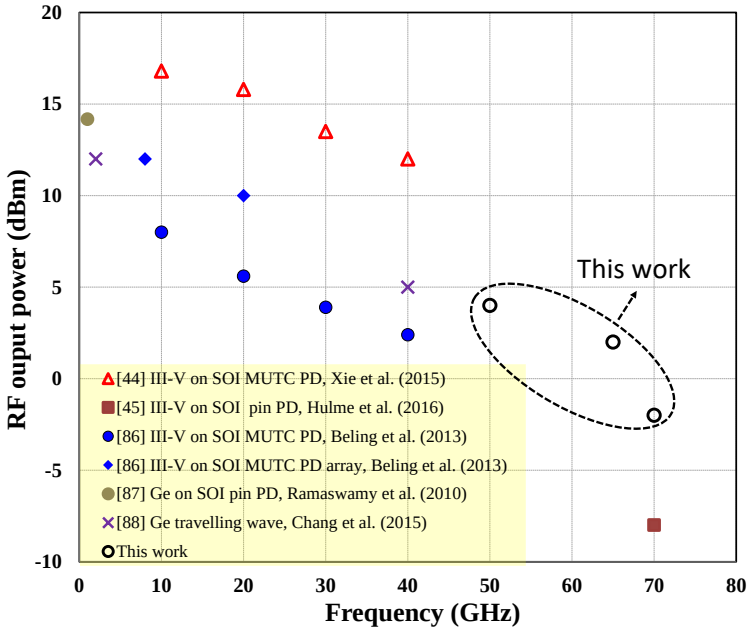


Figure 9.1 RF output power level at 50 Ω load of waveguide photodiodes on SOI versus signal frequency at 1.55 μm wavelength

I demonstrated modified uni-traveling carrier photodiodes with top p-contact heterogeneously integrated on silicon-on-insulator nano-waveguides. Unlike our earlier work, an inverted PD layer structure is used that results in the p-contact being on top after wafer bonding. This structure has the potential to further enhance the high-power performance since heat dissipation from the depletion layer into the silicon is not hindered by the low-thermal conductivity InGaAs. In addition, the photodiode becomes compatible with the heterogeneous integration process that was presented in [77]. I designed the width of the silicon waveguide underneath the photodiode to be 300 nm in order to enhance optical coupling from the waveguide into the absorber. Single photodiodes have very low dark current of 1 nA and a high bandwidth of up to 65 GHz. At 70 GHz, a record-high RF output power of -2 dBm at 20 mA and 3 V reverse bias for a 5 x 15 μm^2 single photodiode was measured. A comparison of the

demonstrated output RF power levels in this work with numbers reported in the literature is shown in Figure 9.1. Balanced photodiodes of this type reached 20 GHz bandwidth and a CMRR of 20 dB.

In chapter 7-8, I describe the process development of InP-based photodiodes that were adhesively bonded onto silicon wafer using SU8 as bonding intermedia. Using this process, I fabricated and demonstrated top-illuminated MUTC photodiodes on Si for the first time. Photodiodes have dark currents as low as 4 nA, which are comparable to dark current levels of photodiodes on native InP substrate. The measured external responsivity was 0.4 A/W at -3 V in agreement with the theoretical prediction. Together with capacitance measurements these results reveal fully functional MUTC photodiodes heterogeneously integrated on Si by SU8 bonding.

9.2 Future Work

9.2.1 Dual-Input Waveguide PD Performance Limitation Study

As described in Chapter 6, the maximum output power of the dual-input waveguide photodiode was lower than its single-input counterpart. Also, the dual-input PD is 'turned-off' at a relatively high photocurrent level (10 mA). In order to verify my hypothesis that the mechanism behind this phenomenon is related to a thermo-optic effect [78], it will be important to fabricate passive waveguides and MMI splitters only as test structures for a direct measurement. Also, images taken by an infrared camera can be helpful to monitor any light leakage or scattering from the waveguide. A section of straight waveguide identical to a waveguide in this work can be used to benchmark the waveguide loss (Figure 9.2a). The MMI test structure can be used to monitor the power splitting ratio and the MMI loss under different wavelengths and optical intensities (Figure 9.2b). The MMI splitter and the narrowed waveguides can help to reveal if there is any optical interference between closely spaced waveguides (Figure 9.2c). In addition, instead of splitting the input light by the MMI, two individual waveguides can be used to direct the light into the photodiode (Figure 9.2d). This can be helpful for

studying the effects of dual-input waveguides on the performance of the photodiode itself, and exclude potential influences from the MMI.

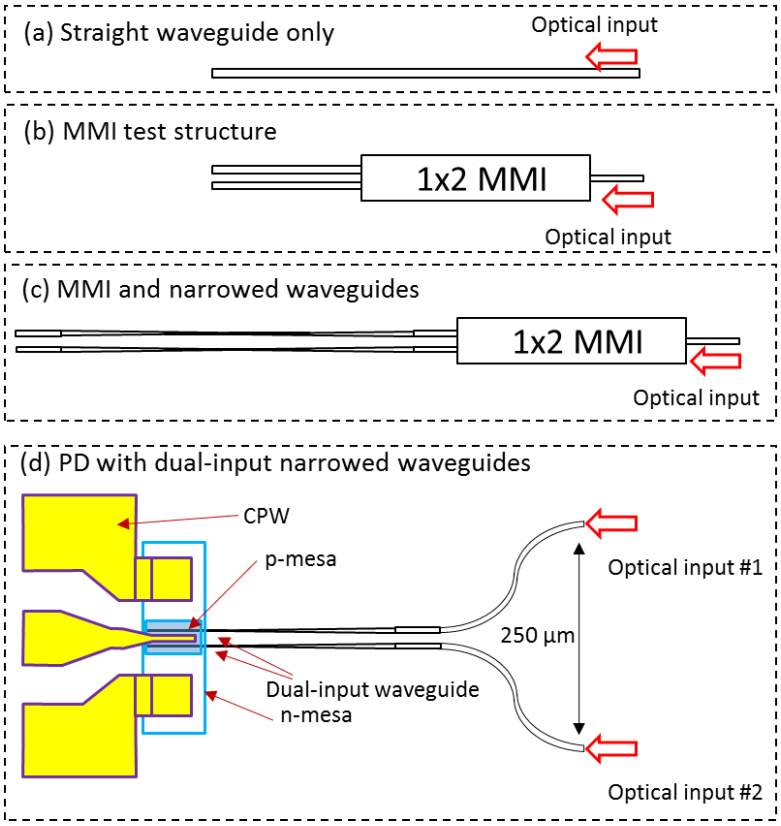


Figure 9.2 Test structures for debugging dual-input waveguide PDs

9.2.2 Fabrication of Adhesively Bonded Waveguide Photodiode

The goal is to achieve high bandwidth, high efficiency MUTC waveguide photodiodes heterogeneously integrated on SOI waveguide platform by SU8 bonding. As designed in chapter 8, adhesively integrated MUTC 15 waveguide photodiode predicts promising results on both bandwidth and efficiency. A device with 50 µm² footprint can reach 164 GHz bandwidth with 0.45 A/W internal responsivity.

300 nm SU8 Bonding Technique for High Bandwidth-Efficiency Waveguide PDs

In order to achieve high coupling efficiency between the silicon waveguide and the photodiode, the separation cannot be too large, as indicated in chapter 8. The desired SU8 thickness is 300 nm in this work. Although SU8-2002 works well in bonding and fabrication, due to the limit of its crosslink network density, its thickness cannot go below 1 µm, which inhibits optical coupling. On the other hand, SU8-6000.5 can easily be thinned to less than 300 nm and bonded with the existing high-yield recipe, but when teamed with an N-type InGaAs bonding interface, it is not compatible with the HCL-based substrate removal approach. It is clear that a bonding test on combination [SU8-6000.5 + N-type InGaAs] should first be carried out. Depending on the outcome, further experiments and modifications may be needed. If 300 nm SU8-6000.5 de-bonds during the HCL substrate removal, photoresist can be applied around the III-V die as a sealing to keep HCL away from SU8, which may avoid the de-bonding issue. In addition, in case bonding metal must be used as bonding promoter for SU8-6000.5, it is worthwhile to look into utilizing the same bonding metals as plasmonic waveguides to enable optical coupling, The idea would be to first couple light from the silicon waveguide into the plasmonic waveguide (as an intermediate step), and then couple the optical power into the absorber of the photodiode.

Optimization of Fabrication Process

Here the goal is to find an SU8-compatible dry etch recipe to pattern the SU8-bonded die. In chapter 7, I fabricated heterogeneously integrated top-illuminated photodiodes. A series of wet chemical etching steps were applied to form the photodiode mesa. Due to the anisotropic etching nature, the shape of the PD mesa deformed significantly. Figure 9.3 and Figure 9.4 show a PD mesa under SEM examination. In order to fabricate much smaller high-speed photodiodes in the future, the wet etch process has to be replaced by an isotropic dry etch process. One boundary condition is that the temperature of the etching process should be lower than the curing point of the SU8 i.e., 130° C. To this end the available RIE-ICP dry etch recipe used in ref. [42] should be modified accordingly. In addition,

the SiO_2 hard mask deposition by PECVD has to be avoided, since the process temperature is 285° C. Instead, low-temperature turbo sputter can be used.

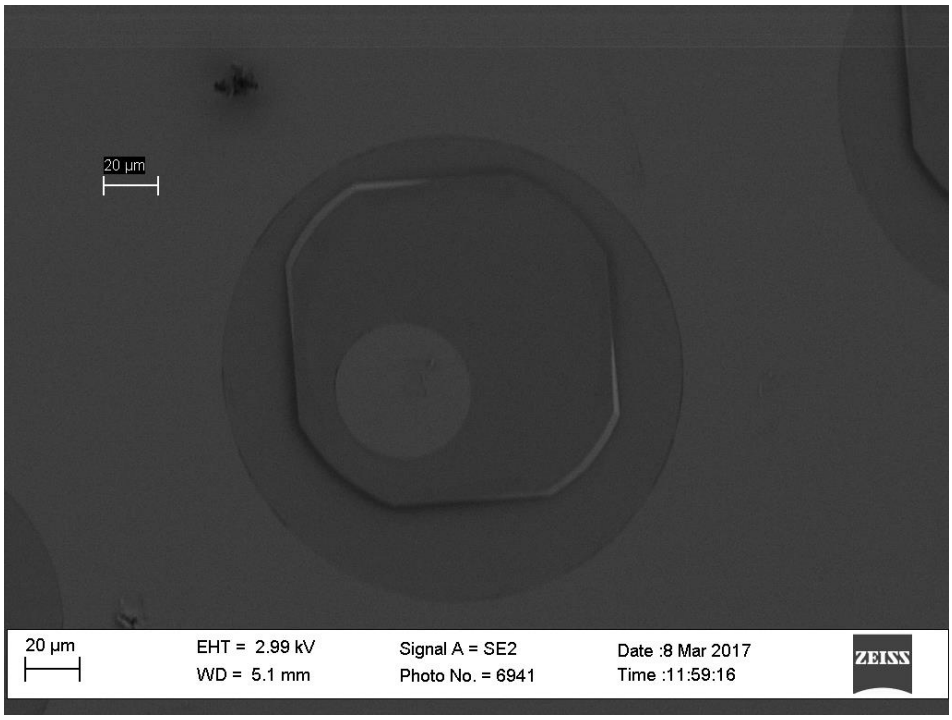


Figure 9.3 SEM picture of a top-illuminated photodiode formed by wet chemical etch

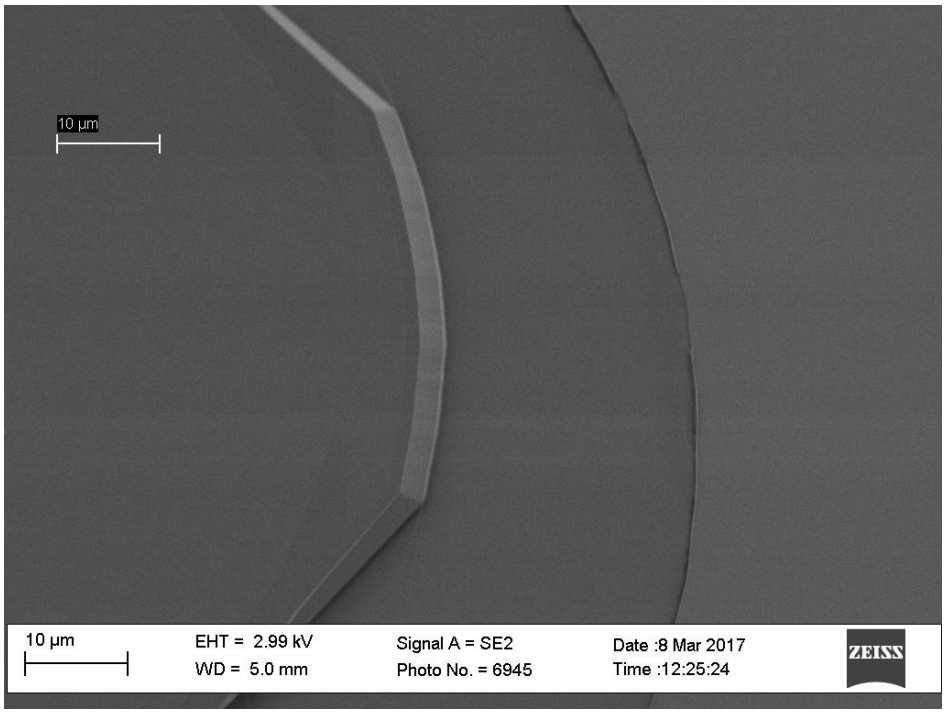


Figure 9.4 Sidewall of chemically wet etched photodiode

9.2.3 Heterogeneous Integration with Submillimeter-Wave Schottky Diodes

The SU8 bonding recipe described in chapter 7 originates from the bonding process used in [64]. Therefore, the integration approach for photodiodes studied in this dissertation is fully compatible with the submillimeter-wave Schottky diodes in [64]. As a potential application, a THz signal generator can be achieved by heterogeneously integrating photodiodes with a Schottky diode. Through optical heterodyning, a relatively low frequency RF signal (<100 GHz) can be generated by the photodiode and frequency up-converted by a Schottky frequency quadrupler diode to submillimeter wavelength.

Appendix I (Fabrication recipe for MUTC8 SOI waveguide PD)

Ye_MUTC 8 SOI WG PD_20160121

MUTC8 dies: #3 (InPact), #6 (Landmark) and #9 (Landmark)

1. P-Mesa (Mesa)

1.1 p-metal

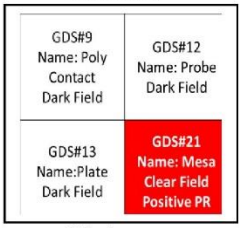
- Clean wafer — Rinse in Acetone, IPA, DI ✓
  Slow bake-out 5min 90C, 5min 110C (stop when bubble) ✓
- O2 plasma — Power: 200, Gas: 80, 600sec ✓
- Metal deposition — Deposit p metal (rates: 1-2 Å/s)
  200Å Ti ✓
  300Å Pt ✓
  500Å Au ✓
  100Å Ti ✓

  Gold target locker PW: 1170

Metal thick=887 - 930 A (by stepper measurement)

1.2 Hard mask SiO2

- Clean wafer — Rinse in Acetone, IPA, DI ✓
  slow bake-out 5min 90C, 5min 110C (stop when bubble) ✓
- O2 plasma — power: 200, gas: 80, 300 sec ✓
- Filmetrics — **Film thickness on Si dummy before deposition**: 0 nm
- PECVD — Clean process and then conditional run 80 mins (~1000 nm) [SiO2 depot rate: 250 nm/20 mins]
  Process "SIO2P35T" (TBD): ✓ [Oxford dry etch selectivity: III-V : SiO2 ~= 1 : 2.5]
  + A large Si dummy
- Filmetrics — **Film thickness on Si dummy after deposition:** 911 nm
- Clean wafer — Rinse in Acetone, IPA, DI ✓
  slow bake 5min 90C, 5min 110C ✓
- O2 plasma — Power: 200, gas: 80, 600sec ✓
- Lithography — Spin HMDS, spin resist AZ5214, and **soft bake 100C 2 min** ✓
  (40sec, 3000rpm → 1.4~1.6 um) TBD



  Exposure "**Plate3 GDS21 "Mesa"**": Align & Expose, soft contact, 376W, 55sec ✓
  Develop **AZ300MIF 30 sec** (agitate) ✓
  Post bake 110C, 50 sec ✓
  Alphastep PR thickness (TBD): 1.70-1.75 um
- O2 plasma — power: 150, gas: 80, 200sec ✓

  ~~Alphastep PR thickness (TBD)~~: _____
- SiO2 dry etch — Oxford/Trion, Process "Chong_SiO2", and Press: 50, ICP power: 25, RIE power: 70, He press: 3
  Rate: 350 nm/600 sec, selectivity SiO2: PR = 1:2.2, time (TBD) ✓
  (Use three dummies to monitor the thickness of the SiO_2)
  OPT------xxj
  Alphastep PR+SiO2 thickness (TBD): T=0 min: SiO2 on Si dummy=915 nm; Stepper on sample=1.75 um
  Alphastep PR+SiO2 thickness (TBD): T=10 min: SiO2 on Si dummy=700 nm [etch rate:200nm/10mins]; Stepper on sample=1.8 um
  Alphastep PR+SiO2 thickness (TBD): T=50 min: SiO2 on Si dummy=330 nm; Stepper on sample=2.4 um
  Alphastep PR+SiO2 thickness (TBD): T=70 min: SiO2 on Si dummy=100 nm (believed to be measurement error); Stepper on sample=2.5 um

[- BOE wet etch (If PR thin)]

- Clean wafer — Remove PR: Acetone, IPA, DI ✓
  slow bake-out 5min 90C, 5min 110C ✓
- Alphastep — SiO2 thickness (TBD): _____ on Dummy (TBD) _____
- O2 plasma — power: 200, gas: 80, ~~300 sec~~ ✓ overnight @ power 200 + 2 hrs @ power 250 [PR after Oxford dry etch gets dry and hard to remove]

1.3 P Mesa dry etch

- Conditional run — Oxford ICP RIE, Process "OPT-InP Etch (Cl2/N2)" 3 min at 50C
  with 4 in Si/SiO2 carrier wafer ✓ Dry etch process target: 1500 nm; then use wet etch (HCL:H3PO4=1:3) @25C to final target 1974nm
- ICP RIE dry etch — Process "OPT-InP Etch (Cl2/N2)-EP", wafer on Grease, see laser monitor

Recipe 'OPT-InP Etch (Cl2/N2) -with Ep_dxj'
ICP=300, RF=115

Time 0 min	wafer 1.05 um	dummy	1050 nm
Time 2 mins	wafer 1.18 um [etched 216nm]	dummy	964 nm
Time 5 mins	wafer 1.55 um [etched 690 nm]	dummy	860 nm
Time 8 mins	wafer 2.0 um [etched 1230 nm]	dummy	770 nm
Time 10 mins	wafer 2.22 um [etched 1495 nm] ✓	dummy	725 nm

Use 4 in Si wafer for cleaning after finish.

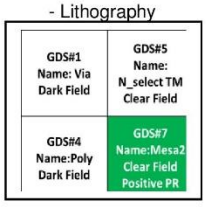
- Alphastep — SiO2+metal+n-mesa thickness (~ µm): ✓ 1955 nm

wet etch:
T=0s: stepper=2.22um [1495 nm etched in total]
~~T=30s: stepper=2.52um [1795~~ nm etched in total]
T=60s: stepper=2.68um [1955 nm etched in total] ✓
T=70s: stepper=2.65um [1955 nm etched in total]
confirmed!

2. N-Mesa (Mesa 2)

2.1 Hard Mask SiO2

- Clean wafer — Rinse in Acetone, IPA, DI ✓
  slow bake-out 5 min 90C, 5 min 110C ✓
- O2 plasma — power: 200, gas: 80, 300 sec ✓
- Filmetrics — Film thickness on dummy Si before deposition: 10 nm
- PECVD — Clean process and then conditional run
  Process "SIO2P35T" (TBD): 13 mins (112 nm) [similar calculation in 1.2]
  +previous Si dummy and new dummy
- Filmetrics — Film thickness on dummy Si after deposition (TBD): new dummy=136 nm; old dummy=900 nm
- Clean wafer — Acetone, IPA, DI, slow bake 5 min 90C, 5 min 110C ✓
- Lithography



  Spin HMDS, spin resist AZ5214:soft bake 100C 2 min: ✓
  (40sec, 3000rpm → 1.4~1.6 um) TBD
  Exposure "plate 1 gds 07 "Mesa 2": Align & Expose, soft contact, 376 W, time: 55sec ✓
  Develop AZ300MIF 30 sec (agitate) ✓
  Post bake 110C, 50 sec: ✓
  Alphastep PR thickness (TBD): 1.8 um
- O2 plasma — power: 150, gas: 80, 200sec ✓
  Alphastep PR thickness (TBD): assume to be the same

- SiO2 dry etch — Oxford/Trion, Process "Chong_SiO2", Press: 50, ICP power: 25, RIE power: 70, He press: 3
  Rate: 350 nm/600 sec, selectivity SiO2: PR = 1: 2.2, T=0: SiO2 (new dummy)=136 nm; stepper (sample)=1.8um
  T=8min: SiO2 (new dummy)=1nm; stepper (sample)=1.95um ✓
  Alphastep PR+SiO2 thickness: ✓
  Remove PR: Acetone, IPA, DI, ✓ + 1 hr O2 plasma @ power 250
  Alphastep SiO2 thickness: 170 nm

2.2 ICP RIE Dry etch

- Conditional run — Oxford ICP RIE, Process "OPT-InP Etch (Cl2/N2)" 3 min at 50C
  with 4 in Si/SiO2 carrier wafer ✓

- ICP RIE dry etch — Process "OPT-InP Etch (Cl2/N2)-EP", wafer die on grease, see laser monitor

Time 0 min	wafer 170 nm	dummy 900 nm (old); 136 (new)	
Time 1 min	wafer 267 nm [132 nm etched]	dummy 865 nm (old); 102 nm (new)	
Time 2 min	wafer 363 nm [223 nm etched]	dummy 836 nm (old); 73 nm (new)	✓
Time	wafer	dummy	
Time	wafer	dummy	

  Use 4 in Si wafer for cleaning after finish.

-Alphastep — SiO2+metal+n-mesa thickness (~ µm): ✓ 363 nm

although didn't hit 273 nm etching target, from microscope,
all air bubbles (bonding error) gone, can see waveguides clearly,
so stopped, done!

3. N-Metal (Metal)

3.1 Open N-contact layer --- the ONLY step that can use LOR (lift-off-resist)

- Clean wafer — Acetone, IPA, DI, slow bake out 5 min 90C, 5 min 110C ✓

- O2 plasma — power: 200, gas: 80, 300 sec ✓

- Lithography — Spin HMDS, spin resist AZ5214, soft bake 100C 2 min ✓
  (40sec, 3000rpm → 1.4~1.6 um) TBD

GDS#8 Name: Contact5um Dark Field	GDS#18 Name: Contact3um Dark Field
GDS#10 Name:SU8 Dark Field	GDS#11 Name:SU8PR Clear Field

  Exposure "plate 2 gds 08 "Contact 5um": Align & Expose, soft contact, 376 W, time: 55sec
  plate 2 gds 18 "Contact 3um
  Develop AZ300MIF 30 sec (agitate) ✓ Post bake 120C, 50 sec ✓
  Alphastep PR thickness (1.5µm thick): 1.49 um

- SiO2 dry etch — ~~Oxford/Trion, Process "Chong_SiO2", Press: 50, ICP power: 25, RIE power: 70, He press: 3~~
  ~~Rate: 350 nm/600 sec, selectivity SiO2: PR = 1: 2.2~~, BOE: 90s, 73 nm SiO2 etched
  Alphastep PR+SiO2 thickness: skipped

- O2 plasma — power: 200, gas: 80, 300 sec ✓

3.2 Deposit metal

- Metal deposition — Deposit 200Å Ti (1Å/s), 300Å AuGe (1 Å/s), 800Å Au (1Å/s), 300A Ni (1Å/s) ✓
- Lift-Off — ~~Acetone soak + Ultrasonic (small Ultrasonic 20-50 units)~~

NMP: Propylene Glycol = 1:1 @120C (40 mins)
O2 plasma @ power 250 (10 mins)

4. Via (open P-contact)

- Clean wafer — Acetone, IPA, DI, slow bake out 5 min 90C, 5 min 110C ✓
- O2 plasma — power: 200, gas: 80, 300 sec ✓
- Lithography — Spin HMDS, spin resist AZ5214: 40sec, 3000rpm, soft bake 100C 2 min: ✓
(40sec, 4000rpm → 1.2~1.4 um) TBD

GDS#9 Name: Poly Contact Dark Field	GDS#12 Name: Probe Dark Field
GDS#13 Name:Plate Dark Field	GDS#21 Name:Mesa Clear Field

Exposure **"plate 3 gds 09 "ploy contact"**: Align & Expose, soft contact, 376 W, 50 sec ✓

Develop AZ300MIF 30 sec (agitate) ✓

Post bake 110C, 50 sec: ✓

Alphastep PR thickness: 470 - 550 nm

- O2 plasma — power: 200, gas: 80, 600 sec ✓
- SiO2 dry etch — Oxford/Trion, Process "Chong_SiO2", Press: 50, ICP power: 25, RIE power: 70, He press: 3 rate: 350nm/600sec, selectivity SiO2: PR = 1: 2.2, **(TBD)** _____sec Oxford: 40 mins, 100 nm SiO2 left; followed by BOE: 5mins +30s

Alphastep PR+SiO2 thickness: ✓

- I-V Test — Measure I-V characteristics on larger-area PD: ✓
I=1mA @ _____V Idark = _____@ _____V
I=1mA@ _____V Idark = _____@ _____V
I=1mA @ _____V Idark = _____@ _____V

mounted dies on 157C hotplate ACCIDENTALLY, PR whitened, cannot be removed by acetone.
O2 plasma @power 250 for 90 mins, all PR gone!

5. SU8

- Clean wafer — Acetone, IPA, DI, slow bake out 5 min 90C, 5 min 110C ✓
- O2 plasma — power: 200, gas: 80, 300 sec ✓
- Lithography — Spin HMDS, bake 15min 90C ✓

GDS#8 Name: Contact5um Dark Field	GDS#18 Name: Contact3um Dark Field
GDS#10 Name:SU8 Dark Field	GDS#11 Name:SU8PR Clear Field

Dispense SU8-2002, spin 5sec 0-500rpm, 30sec 3000rpm ✓

Edge-bead removal with razor blade ✓ soft bake 2min 90C ✓

Exposure **"plate 2 gds 10 "SU8"** (shapes open): Align & Expose, soft contact, 376 W,

time: 35 sec ✓

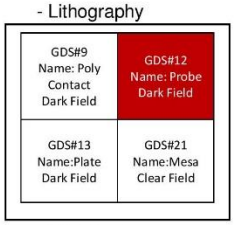
Post-exposure back (PEB) 2min 90C ✓ SU8 Developer 1min, rinse in IPA ✓

Alphastep SU8 thickness (2.5µm thick): 1.645 um

How to control thickness of SU8?

6. Pad Metal and Plating

- Clean wafer — Acetone, IPA, DI, blow nitrogen, slow bake out 5 min 90C, 5 min 110C ✓
- O2 plasma — power: 200, gas: 80, 600 sec ✓
- Lithography — Spin HMDS, spin resist AZ5214: 40sec, 3000rpm, soft bake 100C 2 min: ✓



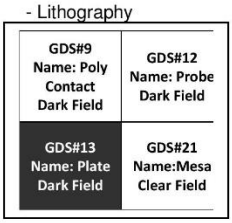
(40sec, 4000rpm → 1.2~1.4 um) TBD

Exposure "**plate 3 gds 12 "probe"**": Align & Expose, soft contact, 376 W, time: 55 sec ✓

Develop AZ300MIF 30 sec (agitate) ✓ Post bake 110C, **10min (tbd)** ✓

Alphastep PR thickness (1.6µm thick): 1.715 um

- O2 plasma — power: 200, gas: 80, 300 sec ✓
- Metal deposition — Deposit 150Å Ti (1Å/s), 500Å Au (1Å/s), ✓
- O2 plasma — power: 200, gas: 80, 300 sec ✓
- Lithography — Spin HMDS, spin resist AZ5214: 40sec, 3000rpm ✓



Soft bake 90C 60sec **STOP when BUBBLES!** 0 min 7 - 13s

Exposure "**plate 3 gds 13 "plate"**", Align & Expose, soft contact, 376 W, time: 55 ✓

Develop AZ300MIF 30 sec (agitate) ✓

Alphastep PR thickness (3.2µm thick): 3.425 um

- O2 plasma — power: 200, gas: 80, 300 secs ✓
- Plating — 25E Technics (ready-to-use), 50C,

Set current: 1mA, V: 0.04V ~ 0.05V, (~0.7µm/10min)

lift-off method:
1. acetone+ultrosonic
2. NMP+PG
3. O2 plasma->Au etch ->O2 plasma (layer by layer)

Total plating time~40min for 2.8µm thick plated gold
Time= 10 mins I= 0.9 mA V= 0.7->0.5 V Step= 3.0 um [420 nm plated]
Time= 20 mins I= 0.8 mA V= 0.7->0.6 V Step= 1.32 um [2.1 um plated]
Time= 30 mins I= 0.8 mA V= 0.7->0.6 V Step= 1.425 um [2 um plated]
Time= 40 mins I= 0.8 mA V=0.68->0.62V Step= 1.1 um [2.3 um plated]

[- O2 plasma — remove top PR layer, power: 150, gas: 80, ~4 hours 40 min

Alphastep PR thickness

- Seed layer etch Gold etch HG400 to remove Au seed layer]

- Lift-Off ~~Acetone soak + Ultrasonic (large Ultrasonic 45 units) 10min~~ NMP+PG @ 120C

after plating, lift-off not complete, devices short-circuit
-> Au etch in HG-800, 1min.
NO short devices anymore!

7. Dicing

- Mount	Mount wafer on Si dicing carrier wafer with black wax on hot plate ✓
	Spin resist AZ5214 ✓
	Dicing saw, use Silicon Blade ZH05-SD2000-N1-50 FF HEFF2016S ✓
	Carrier Height (~530µm): ✓
	Total height HySi (~1350µm): ✓
	Work thickness (HySi + 50µm =~1400µm): ✓
	Blade Height (<= substrate= ~400µm) = ✓
- Dice	Hairline Thickness (~60µm) = ✓
- Clean wafer	TCE, ACE, IPA, DI ✓
- O2 plasma	power: 200, gas: 80, 300 sec ✓

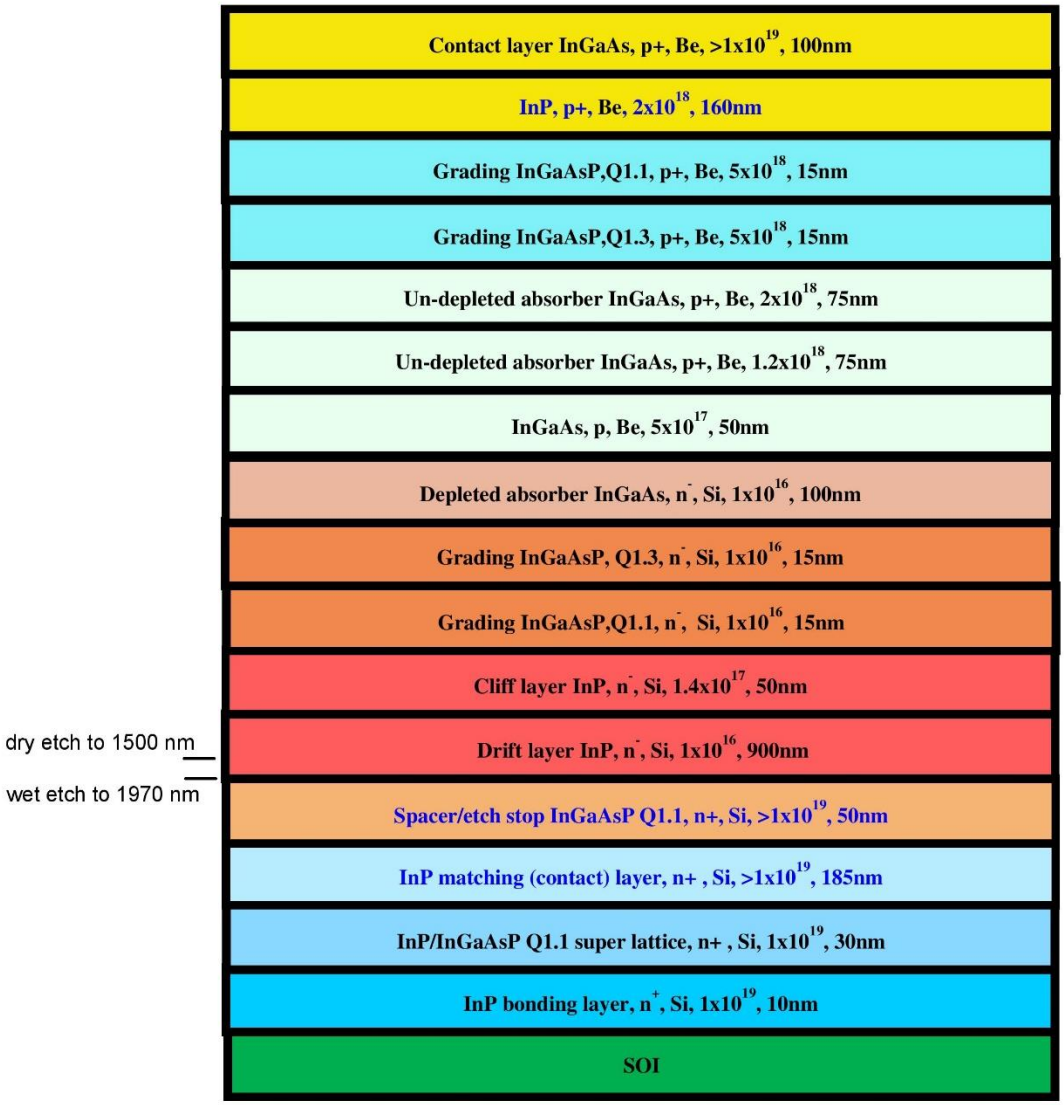
8. Facet Polishing --- sent out for polishing

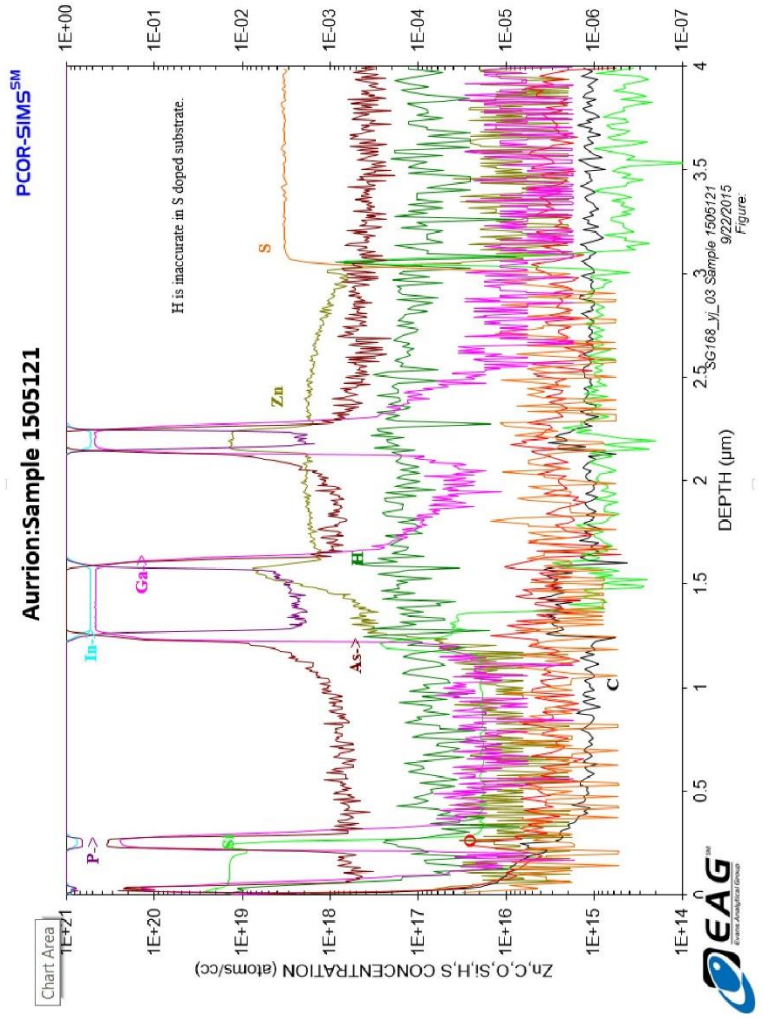
[Spin resist AZ5214]

- Mount	Mount wafer piece on glass fixture using white wax on hot plate
- Polish	Use Tedpella Solution 0.06µ Prod. 815-110 Collodial Silica Suspension
	Polish speed <= 55 rpm, arm 75%, abrasive off, force: ~<1000g

Ye_MUTC 8 SOI WG PD_20160121

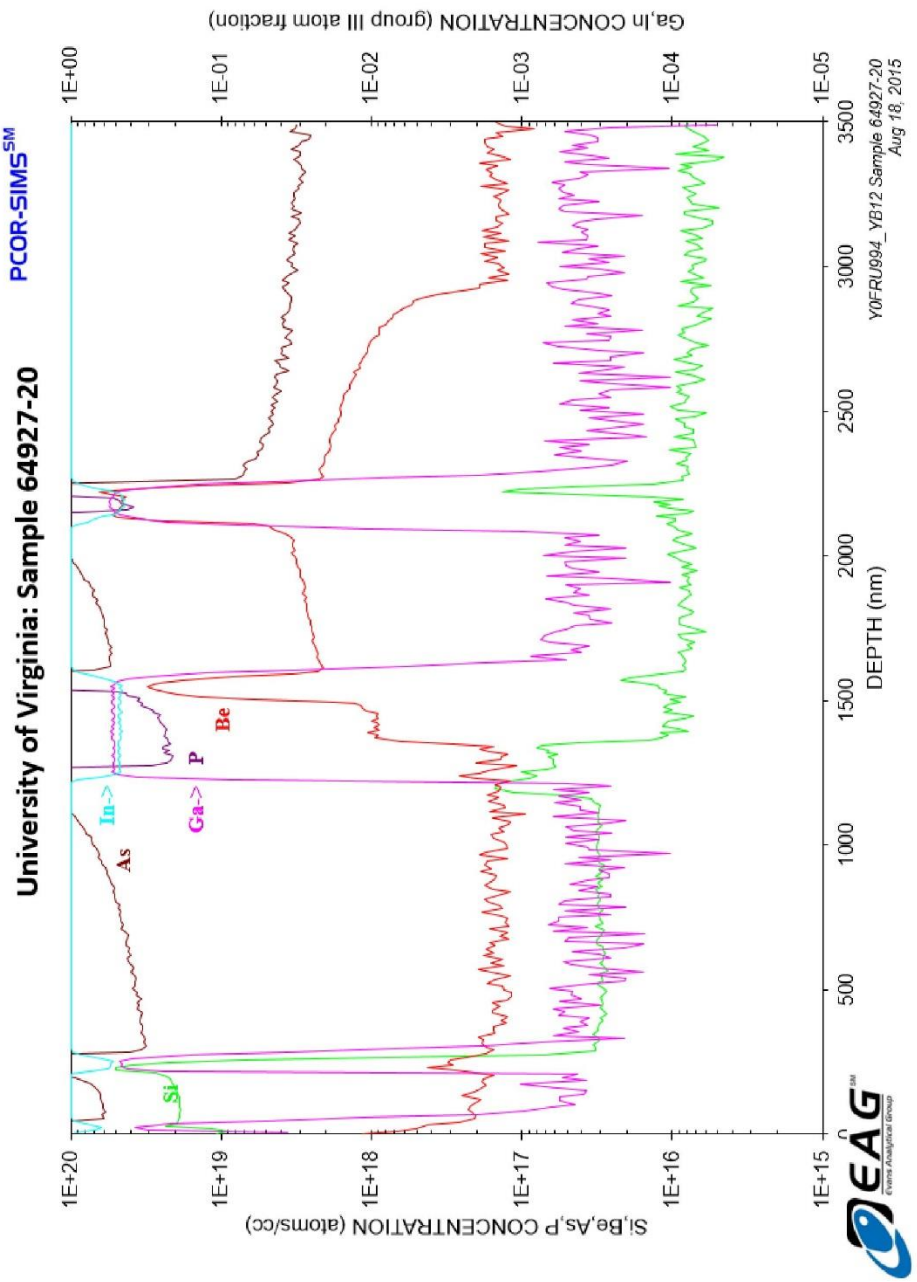
Original design:



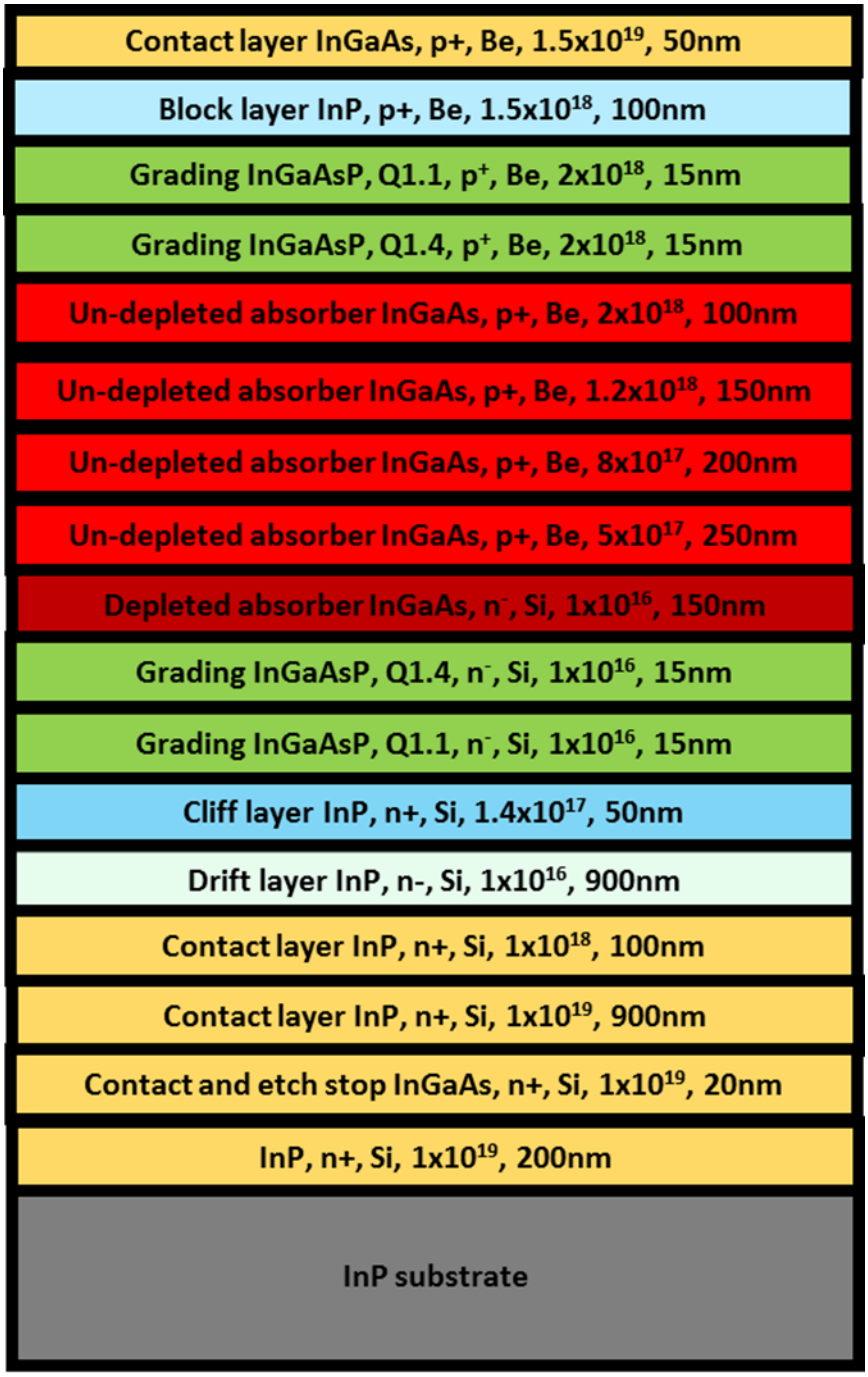


Why Zn has two peaks?

InPact

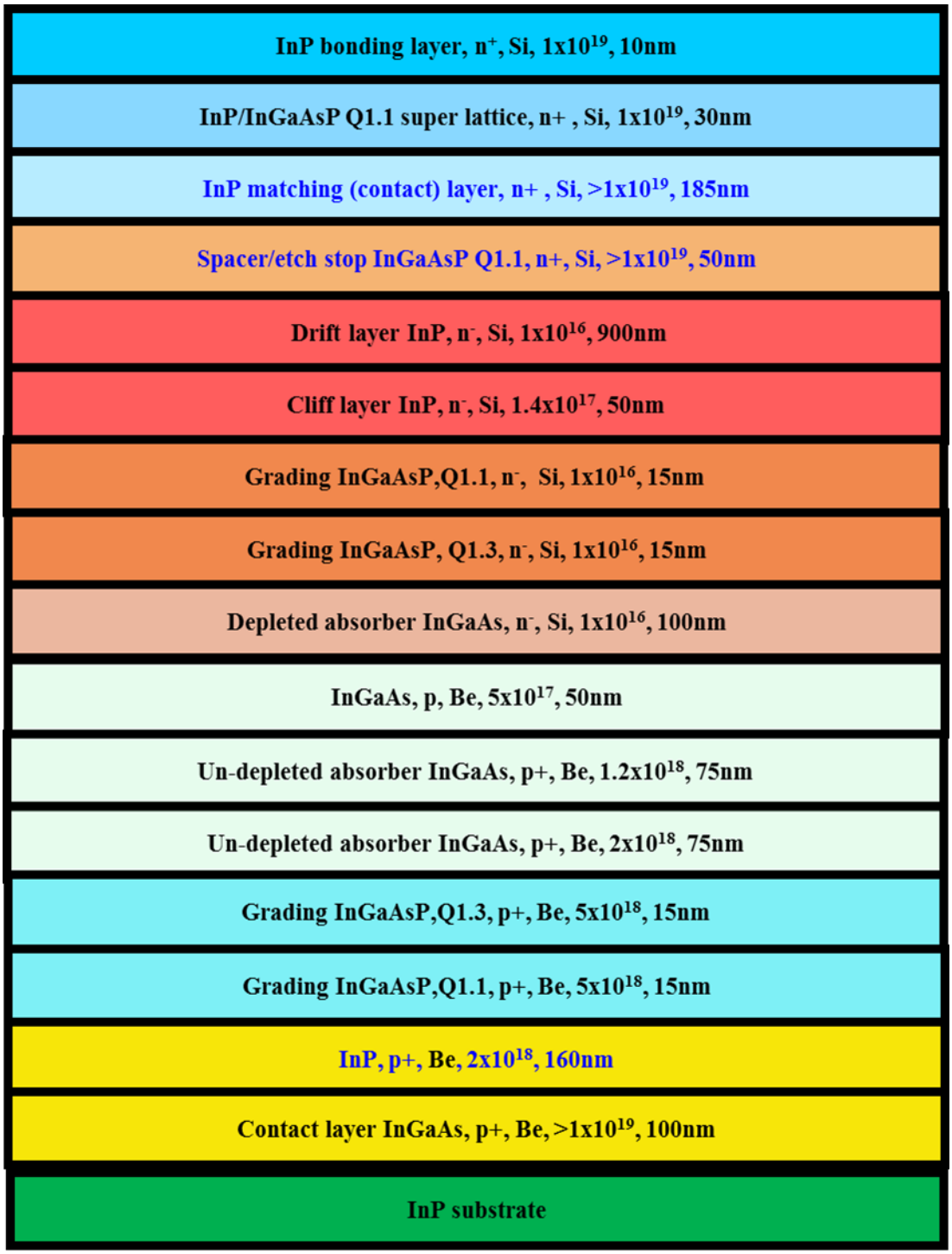

University of Virginia: Sample 64927-20
PCOR-SIMS℠
Si,Be,As,P CONCENTRATION (atoms/cc)
Ga,In CONCENTRATION (group III atom fraction)
DEPTH (nm)
Y0FRU994_YB12 Sample 64927-20
Aug 18, 2015
In->
Ga->
As
P
Be
Si
1E+20
1E+19
1E+18
1E+17
1E+16
1E+15
1E+00
1E-01
1E-02
1E-03
1E-04
1E-05
500
1000
1500
2000
2500
3000
3500
EAG

Appendix II (Epitaxy wafers used in SU8 bonding test)



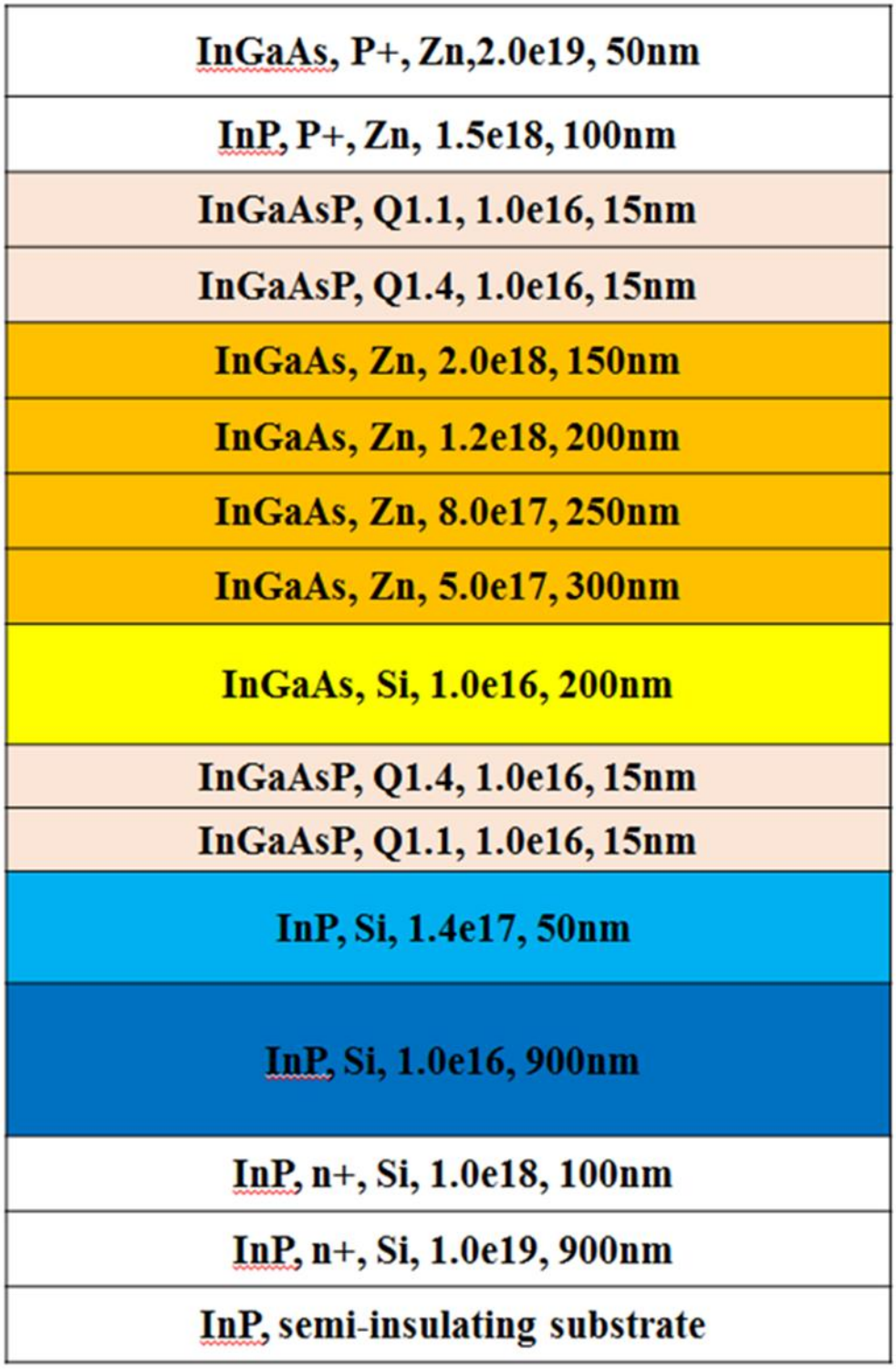
MUTC4

Figure A.II.1



MUTC8

Figure A.II.2



MUTC11

Figure A.II.3

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