Terahertz Detachable Chip-to-Chip Interconnectors

Han-Yu Tsao

Dissertation

Presented to the Faculty of the Graduate School of

The University of Virginia

Department of Electrical and Computer Engineering

Committee Members:

Dr. Weikle, II, Robert M (Chair)

Dr. N. Scott Barker (Advisor)

Dr. Lichtenberger, Arthur W

Dr. Gavin Garner

Dr. Andreas Beling

Dr. Michael Cyberey

Acknowledgments

I am deeply grateful to my advisor, Professor N. Scott Barker, whose mentorship has been instrumental in making this work possible. I would also like to express my gratitude to Professor Weikle II, Robert, and Professor Arthur Lichtenberger, who have been supportive of my academic pursuits and have provided me with the necessary resources and time to achieve my goals.

My Ph.D. journey would not have been complete without the support and guidance of the members of my Dissertation Committee. I would like to thank each of them for their personal and professional advice, which has been invaluable in shaping my research. I would like to express my sincere gratitude to Professor N. Scott Barker, who has served as my advisor and mentor throughout my academic journey. His invaluable guidance and support have been instrumental in shaping my academic career, and I am deeply grateful for his contributions.

I owe a debt of gratitude to my family, who have been an unwavering source of love and support throughout my academic journey. I would like to thank my parents for being my ultimate role models and for instilling in me the values of hard work and perseverance. Lastly, I would like to thank my loving and supportive wife, Yenyu, and my four adorable cats, Lychee, Liamboo, Liaya, and Meowly, for their unwavering emotional support, which has been critical in helping me achieve my academic goals.

Dedication

I am grateful for the unwavering support and encouragement of my wife, family, friends, and beloved pets throughout my academic and professional journey. Their unconditional love has been instrumental in my achievements and has helped me overcome various challenges. I dedicate my success to them, and I am forever indebted to their unyielding support.

Contents

Abstract

This study provides a thorough examination of a chip-to-chip interconnect operating in the frequency range of 140 to 220 GHz, commonly referred to as the WR5.1 band. The research indicates that this interconnect has the potential to serve as a prototype for a compact detachable interconnect that can be scaled to frequencies beyond 1 THz. Both the electrical and mechanical characteristics of the interconnect were evaluated in this study.

The proposed design is based on a 15-μm thick silicon substrate and incorporates a self-holding interference taper, which enables a self-aligned mechanical contact with sufficient force to ensure a low contact resistance. In this regard, the assembly force of the interconnect has been measured to range from 70 to 90mN, while the resulting contact resistance ranges from 2.8 to 3.5 Ω. Furthermore, the disassembly force was found to range from 60 to 85 mN. Notably, the interconnect has demonstrated a high degree of durability, with the ability to sustain up to 100 cycles of assembly and disassembly.

The electrical measured results show good return loss across the WR5.1 band and better than 10 dB from 165 to 220 GHz. The measured insertion loss of the prototype chip (including 28 mm of WR5.1 waveguide and 4 mm of rectangular coax) is better than 2 dB across the band.

1. Introduction

1.1 Terahertz technologies and applications

Terahertz technology refers to systems and components operating in the frequency from 300 GHz to 3 THz. The wavelength in this frequency band is from 1 mm to 100 μm. Countless engineers focus on terahertz technology exploration, and lots of outstanding research has been published. Most applications focus on the development of aerospace technology, high-resolution imaging systems, and terahertz communication systems. However, the atmospheric attenuation of electromagnetic waves generally increases along with the frequency. For example, the achievable range for terahertz communications in air is relatively short (a few meters) compared with space-based communications [1] [2]. Therefore, many terahertz devices and ICs are applied to space-based technology.

Plenty of terahertz sensors, transmitters, and receivers are used by the Earth-observing system microwave limb sounder (EOS-MLS) and other aerospace observatories [3]. The MLS helps scientists monitor the chlorofluorocarbon threat to the ozone layer and it also discovered the Antarctic ozone hole. The EOS-MLS instrument is equipped with five different heterodyne radiometers operating at five different frequency bands. The radiometer one (R1) can cover the 118 GHz band which provides O_2 detection, temperature, and pressure data. The second radiometer (R2) can measure the 183 GHz H_2O and HNO_3 lines. The third radiometer (R3) can measure the 240 GHz O_3 lines and CO line. The fourth radiometer (R4) can measure the 640 GHz HCl line and ClO, BrO, HO_2, N_2O. The fifth radiometer (R5) can measure the 2.5 THz OH line. Each of these measurements provides essential information. For example, the R1 radiometer provides information on cloud ice and geopotential height. More recently, with the progress of terahertz technology and other fields [4] [5], in 2019, for the first time ever, we had a better view of the most mysterious thing in the universe: a black hole.

Another terahertz application is the terahertz detection system, which was first proposed by Dr. Grischkowsky et al [6]. After several decades' effort, the terahertz detection system has been applied to nondestructive testing and other medical imaging systems [7]. The terahertz imaging system has become

a promising tool for next generation imaging systems. A variety of technologies have been applied to terahertz imaging systems, for example: terahertz time-domain spectroscopy imaging [7] [8], Schottky diode terahertz image system [9], Golay Cell terahertz image [10], quantum well terahertz image system [11].

The terahertz detection system is composed of terahertz detectors, readout modules, and processors, as shown in Figure 1.1. The system is composed by a tunable terahertz quantum cascade laser (QCL). The tunable QCL can switch from 2.5 THz to 4.3 THz. The multi-spectral THz sensor is using a detector array to realize multi-band detection. The key to multi-band detection is the integration of various single-band detection cells.

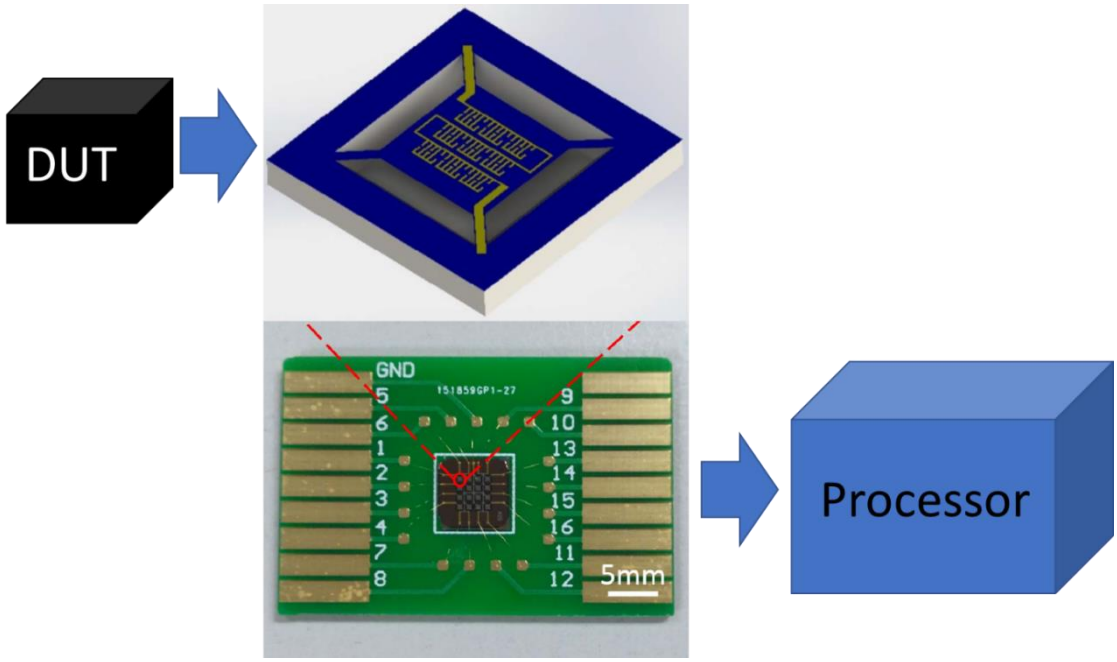


Figure 1.1:Terahertz detector array and detection system [12].

Engineers have also applied terahertz sensors to imaging of biomedical samples. Recent research has demonstrated that terahertz sensors can capture images of bio-tissues such as pork and leaves [12] [13] [14]. The work presented in [12] shows a fully integrated 860 GHz CMOS sensor. The sensor successfully integrated the terahertz sensor and readout circuit into one IC chip. The work presented in [13] is also a

terahertz bio-imaging system that uses a terahertz antenna array and millimeter wave IQ mixer to realize high-resolution detection.

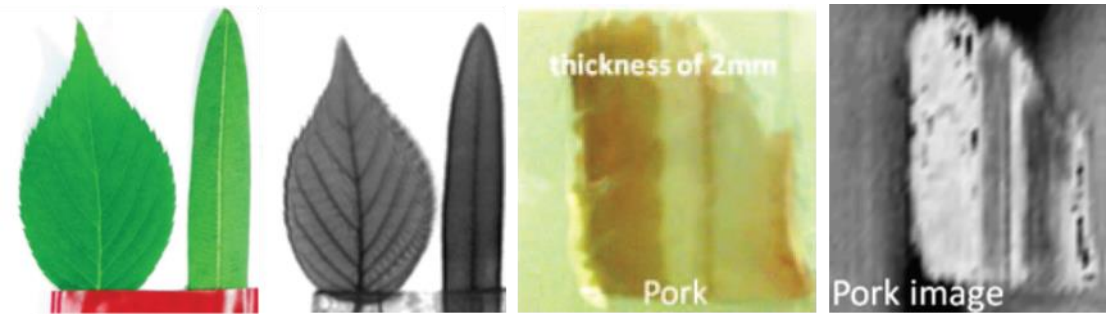


Figure 1.2:Bio-tissues image under terahertz detection [13] [14].

Engineers have also applied terahertz technology to the development of secure communication systems (SCS) [15]. The secure communication system's antenna beams must have high directivity to avoid being received by other systems. The wavelength is inversely proportional to the frequency, which means the wavelength at the terahertz band is shorter than the lower frequency band. Therefore, the antennas' size in the terahertz band is smaller, enabling larger antenna arrays to be made within the same physical space. The compact antenna size enables the terahertz antenna arrays to produce a highly directional beam. Recently, many projects about how to construct a physically secure terahertz communication system have been presented [15] [16] [17].

Terahertz communication is another field which has great potential for the application of terahertz technology. Compared with the 5G network, terahertz communication has a more available spectrum, enabling data transmission rates greater than 100 Gigabits per second [18]. However, pushing the working frequency up to the terahertz range requires the use of III-V semiconductor technology development and fabrication. This technology is required to manufacture terahertz diodes and amplifiers, which rely on solid-state technologies such as GaN or GaAs, that exhibit a cut-off frequency higher than 700 GHz [19].

The InP terahertz integrated circuit has shown the high-power handling ability, making the InP heterojunction bipolar transistors (HBTs) suitable for terahertz power amplifier [19] and other higher

frequency circuits. Also, many InP components for terahertz receivers like LNA, VCO, Mixer, PLL, etc., have been published [20].

Another suitable material for terahertz ICs and devices is GaN. GaN has a higher bandgap energy and saturation velocity compared to GaAs. Therefore, GaN-based components can provide higher output power and operation frequency. GaN has been applied to THz imaging systems [21], detectors [22] [23], and oscillators [24]. On the other hand, the III-V semiconductor substrate will increase the cost rapidly and make terahertz communication difficult to be commercially used.

Compared with terahertz ICs or sensors, the size of terahertz communication systems is still large. Figure 1.3 shows an example of a metal waveguide-based sub-millimeter wave communication system that integrates each device based on metal waveguide blocks. As Figure 1.3 shows, the waveguide integration makes the terahertz system bulky and difficult to be used commercially. Therefore, many researchers are working on the CMOS IC integration technology to assemble the terahertz communication system into a chip. In 2014, a research team lead by Prof. Peyman Nazari successfully integrated a transceiver working at 210 GHz using 32 nm SOI CMOS technology [25]. The CMOS IC integrated the dipole antenna, VCO, LNA, and PA into a single chip.

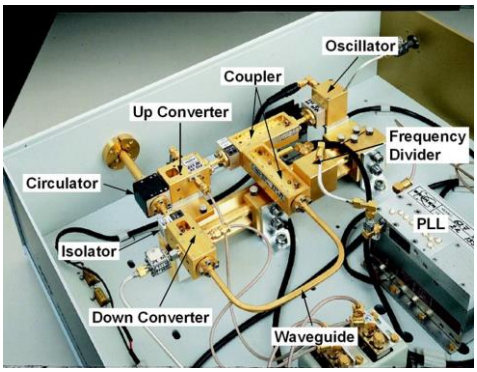


Figure 1.3:Photo of sub-millimeter wave system [25].

Although there are many great terahertz applications, the terahertz components and devices are relatively rarer than millimeter wave technologies. The main reason is that terahertz devices are harder to fabricate and operate. Although recent fabrication technology of semiconductors has pushed the transistor

gate-length to several nanometer scales, for CMOS ICs, the silicon transistor's cut-off frequency is still several hundred gigahertz below the terahertz band [26]. Therefore, GaAs and InP are commonly used in terahertz high-speed ICs. Unfortunately, these III-V semiconductors are much more expensive than silicon. This expense is a significant barrier to the development of terahertz systems for commercial applications. Therefore, efficient integration of terahertz ICs with other terahertz components (e.g., couplers, power dividers, filters, antennas) will be critical. How to integrate the terahertz system with a compact, physically reliable and low-loss solution is the topic for this work.

The most common commercially available integration solutions are flip-chip bonding, wire-bonding, and wireless communication between chips. These integration solutions have their pros and cons, and we will summarize them in the following section. In the subsequent part of this study, we introduce a new integration solution for terahertz chip-to-chip connections: a detachable, dependable, space-saving, and low-loss silicon chip-to-chip interconnect, which provides the capability of reconfiguring and detaching the terahertz system.

1.2 Terahertz chip-to-chip integration solution

Chip-to-chip interconnections are critical to enabling multi-chip integration of hybrid technologies for realizing high-performance terahertz systems. While CMOS ICs dominate most communication system back-ends, there are multiple options for integrating the terahertz system's front-ends and back ends. Interconnections between different terahertz components and devices becomes more challenging at higher frequencies because of the increased parasitic effects, radiation losses, and the decrease of system dimensions. Chip-to-chip interconnection techniques that are commonly used in the microwave and terahertz bands are listed below.

1.2.1 Wire bond interconnection review

Wire bonding is the typical method used to connect microwave and millimeter-wave ICs and devices or CMOS ICs and substrates. Since wire bonding technology was invented in the late 1960s [27], it has been widely applied to microwave and millimeter-wave circuit design and integration. The many advantages of wire bond interconnects are detailed below.

1. Low-temperature processes: the bonding process can be operated under 150 °C [28], which is compatible with most of the CMOS processes.
2. Design flexibility: the wire bond interconnection has large design flexibility that can accommodate different height and distance connections. Also, there are bond wire applications beyond interconnects; for example, bond wires can also function as inductors [29] or antennas [30].
3. Mass production: nowadays, the bond wire interconnection can be realized by auto-machining. For mass production, it is a reliable and low-cost solution.

However, although these advantages are valid, as the working frequency rises above 100 GHz, the radiation loss and parasitic inductances caused by the bond wire start to limit the wire bond interconnect performance. In the research work of Dr. Lee [31], in low frequency domain with the operation frequency below 0.1 GHz, the ohmic loss dominated; in high frequency domain with the operation frequency above 1 GHz, the radiation loss dominated. The most effective way to reduce the radiation is to lower the height from the

bonding pad to the bond wire which adds additional limits to the design. Moreover, the distance between the bonding pads is limiting the design flexibility. According to [32], there are limits of distance between bonding pad and substrate edge, distance between bonding wire and package, etc.

Figure 1.4 below is an illustration of a typical bond wire interconnection. There are two different types of bonding: ball bonding and wedge bonding. The ball-bonding wire is more frequently used because the bonding speed is faster and can typically bond ten wires per second. On the other hand, wedge bonding can apply aluminum bond wire and bond the wire at room temperature – usually used on certain processes with temperature limitations.

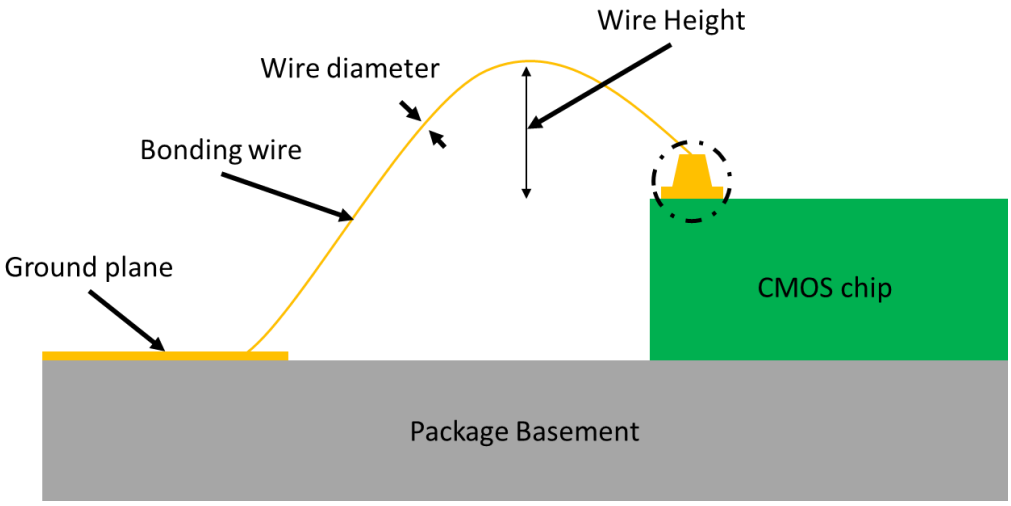


Figure 1.4:Typical bond wire connection.

1.2.2 Flip-chip interconnection review

Flip chip interconnects were developed by IBM in the 1960s and have been widely used for RF system integration. The flip-chip interconnection method uses metallic bumps to connect the substrate and the MMIC, which will be flipped on top of the substrate as shown in Figure 1.5 [33]. The substrate with mounted MMIC can connect to other subsystems through the transmission line on the substrate. Compared with wire bond interconnects, the flip-chip interconnect can provide shorter transition paths. The flip-chip bond is also able to support massive numbers of I/O ports. However, there are still some drawbacks that need to be overcome.

1. The flip chip interconnect cannot be used on a brittle substrate, which might break during the bonding process.
2. During compression, the electrical bumps deform making the radius hard to control. This deformation results in uncertainty in the transition due to uncontrolled parasitics.

When flip-chip interconnection was first introduced by IBM, they made the transistor connected to a substrate, which only had three I/O pads. The bonding technology is known as Controlled Collapse Chip Connection (C4), and the distance between pads needs to be over 130 µm and the pad size is approximately 100 µm. The gap between the chip and substrate is majorly dependent on the solder volume.

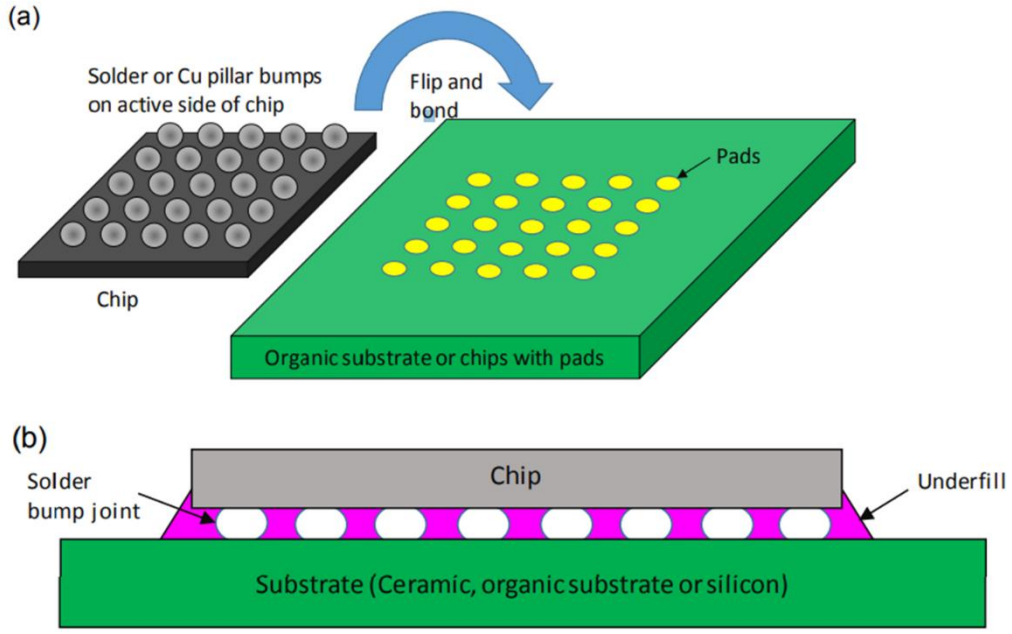


Figure 1.5:Demonstration of C4 bonding and cross section illustration of bonding stacks [33].

As the technology advanced, the number of I/O ports increased and the bump size and pad size of the C4 package needed to be denser. Therefore, the copper pillar with solder became a solution for the bumps; the Micro Copper Pillar Bumps (C2) become a new and denser flip-chip bonding solution. Due to these adjustments, the current copper bump pitch size range is from 40 µm to 130 µm. The current widely used technology is called embedded trace substrate (ETS). The total package height can reach 0.8 mm or even lower. The significant difference between C4 flip-chip bond and C2 bond is the alignment. For the C4 bond,

the bumps can self-align because of surface tension. Yet, for the C2 bond, it needs a warpage structure to help control the bump while compressing.

One significant challenge to the flip-chip bond is the metal bump deformation under high stress and temperature bonding process. For terahertz applications, this metal bump deformation will cause impedance mismatch and decrease the electrical performance. One solution to this problem is the liquid metal transition in which epoxy underfills between the chip and substrate. The epoxy like SU-8 can help make the metal bumps fine and restrict their shape. In Dr. Chen's work [34], he realized and measured the flip-chip bond with SU-8 underfill. After hundreds cycles of thermal compression, the insertion loss of the flip-chip bond is approximately 0.1 dB lower than the loss before thermal compression.

In May 2012, [34], our research group, led by Dr. Chen, conducted a comprehensive review of flip chip integration of two CPW lines. In Dr. Chen's dissertation, two face-to-face CPW lines are connected by flip chip integration and metal bumps. He analyzed the impact of spaces between metal bumps; bump height and bump radius to the reflection coefficient (S_{11}) of the CPW lines flip chip integration.

According to Dr. Chen, [34] larger space between ground bumps and signal bumps can provide better return loss. The measured results shows the return loss of different ground space from 100 μm to 500 μm; the 500 μm ground space measurement is approximately 10 dB higher than 100 μm measurement. Unfortunately, the space increasing will also increase the parasitic coupling to ground which will cause unwanted resonating. Increasing the height of the bumps can also improve the isolation between two substrates, but it does not significantly improve the return loss. However, increasing the bump heights will simultaneously increase the fabrication difficulty. The bump radius can also vary the return loss of the flip-chip bond. A shorter bump radius provides better return loss. The measured result show the 35 μm radius bumps have a return loss higher than 25 dB, yet the 65 μm radius bumps have a return loss less than 10 dB.

One critical reason flip-chip bond is widely applied is that flip-chip bonding does not require additional impedance matching. Furthermore, the chip layout is more flexible because the signal input and output are no longer restricted to the chip's edge.

1.2.3 Quilt package integration review

The Quilt Packaging (QP) is a novel idea proposed by the Bernstein group at the University of Notre Dame [35]. This innovative chip-to-chip interconnect method uses metal bridges to connect different system blocks. As Figure 1.6 below shows, through the help of small metal contact nodules on the edge of the chip, different chipsets can be connected through metal bridges. The nodules are the metal spot at the edge of the chips and provide metal contact for the metal bridges and chips. Compared to the current integration method used by industry, like wire bonding and flip-chip bonding, QP also provides a shorter connection distance between two chipsets. By shortening the connection distance, QP can provide less delay and wider bandwidth.

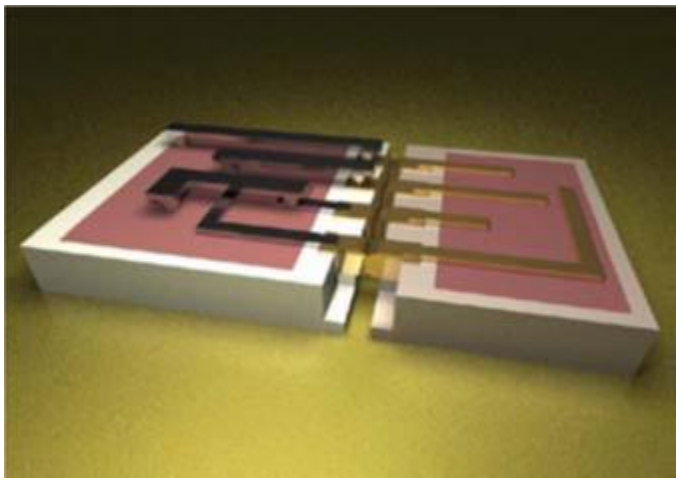


Figure 1.6:Demonstration of two chips connected by quick packaging [39].

The Notre Dame research group also measured the S-parameters of their QP process to improve performance. To measure the interconnection performance, they connected two CPW lines by the Quilt packaging. The test block is shown in Figure 1.7.

For QP package technology, the taper structures are added to the contact nodules and ground plane to reduce parasitic capacitance and interference discontinuity. They also discovered that switching the silicon

substrate from a low resistivity (10 Ω·cm) substrate to a high resistivity (8000 Ω·cm) substrate can help improve the insertion loss and return loss. The reflection coefficient and transmission coefficient significantly improved, as shown in Figure 1.8 below.

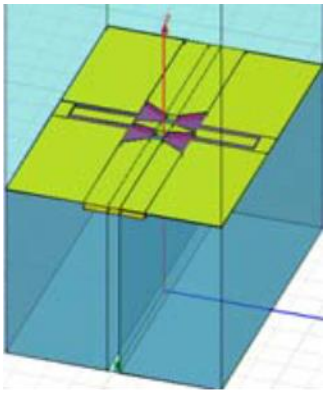
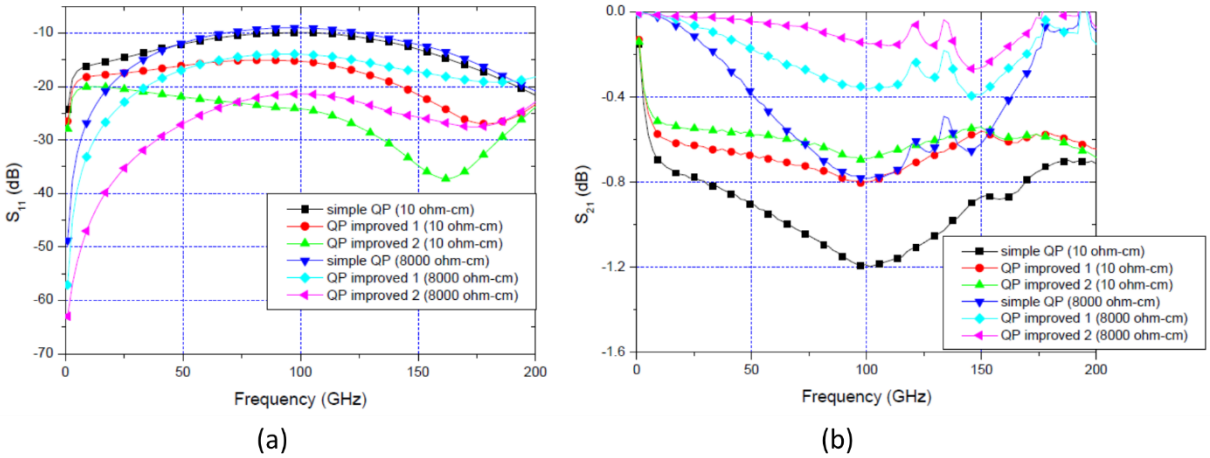


Figure 1.7: Simulation demonstration of CPW test [39].



(a) (b)

Figure 1.8:Measured result of (a) S11 and (b) S21 of different QP design [39].

1.3 Summarization of interconnection solutions

This section reviewed the pros and cons of several different types of high frequency interconnection solutions. The wire bond interconnection can provide more flexibility to different height chip-to-chip interconnection; however, the radiation and parasitic inductance increase with the operating frequency. While the flip-chip bond can provide a short connection path and is also suitable for mass production, the chips must withstand the required pressure and temperature during the flip-chip bonding process.

In the following chapter a different approach to chip-to-chip interconnection is proposed. For most chip-to-chip interconnections working at terahertz frequencies, the interconnections are not detachable. The

detachable terahertz chip-to-chip interconnect provides a novel integration solution for the terahertz systems. In this work, we propose a novel concept of terahertz chip-to-chip interconnects that can turn the terahertz subsystem integration into a detachable functional block like LEGO bricks. Moreover, the detachable interconnection can significantly decrease the system size. Figure 1.9 shows the concept in which the CMOS IC mounted on a silicon substrate can connect with another subsystem through the proposed chip-to-chip interconnect. The chip-to-chip interconnect not only makes the terahertz communication system reconfigurable but also shortens the interconnect distance, making the system more compact.

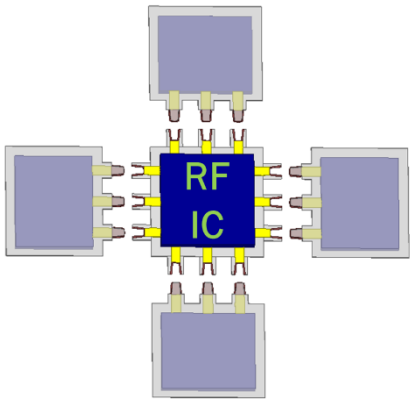


Figure 1.9:Terahertz chip-to-chip interconnect function block demonstration.

One special application of the chip-to-chip interconnect is to improve the terahertz micro-machined probe. The terahertz on-wafer probe is an important invention that helps engineers test terahertz devices and systems. With the help of the terahertz probe, designers can easily and rapidly collect the s-parameter performance of devices and subsystems. The terahertz on-wafer probe measurement system is shown in Figure 1.10. The terahertz probe is composed of the silicon probe-chip and the metal housing [36]. The key component of the terahertz probe is the silicon chip fabricated on a 15 μm silicon on insulator wafer. Different probe chips have various applications.

Our group has integrated many different elements into the probe chip—for example, the baluns integrated on a differential probe [37], the Schottky diodes for on-wafer temperature sensing [38], and strain sensors on the probe to monitor the probe tip's contact force [39]- [40]—so that these micro-machined probes can

be used for different measurements. The probe tip's front side contacts the device under test and must press on the device's contact pads with sufficient contact force that a low contact-resistance is realized. Therefore, the front-end probe tip is a consumable part that will be worn down with use. However, the back-end of the probe chip may include valuable parts like baluns or Schottky diodes, etc. These integrated components add cost to the process and therefore the overall chip. Hence, our research attempts to develop detachable interconnector components so that when front-end probe tips wear down with use, they can easily be replaced without needing to replace the additional integrated components. The chip-to-chip interconnect will be settled in the middle of the probe quasi-coaxial channel, as Figure 1.10 shows.

In an effort to maintain the integrity of the probe components without having the probe tip wear with the use or worse, break, we propose to replace the middle part of probe tip chips with a detachable interconnection device, as shown in Figure 1.10. This proposed design change will allow the complicated and valuable components of the probe to be undisturbed when the probe tip is being replaced.

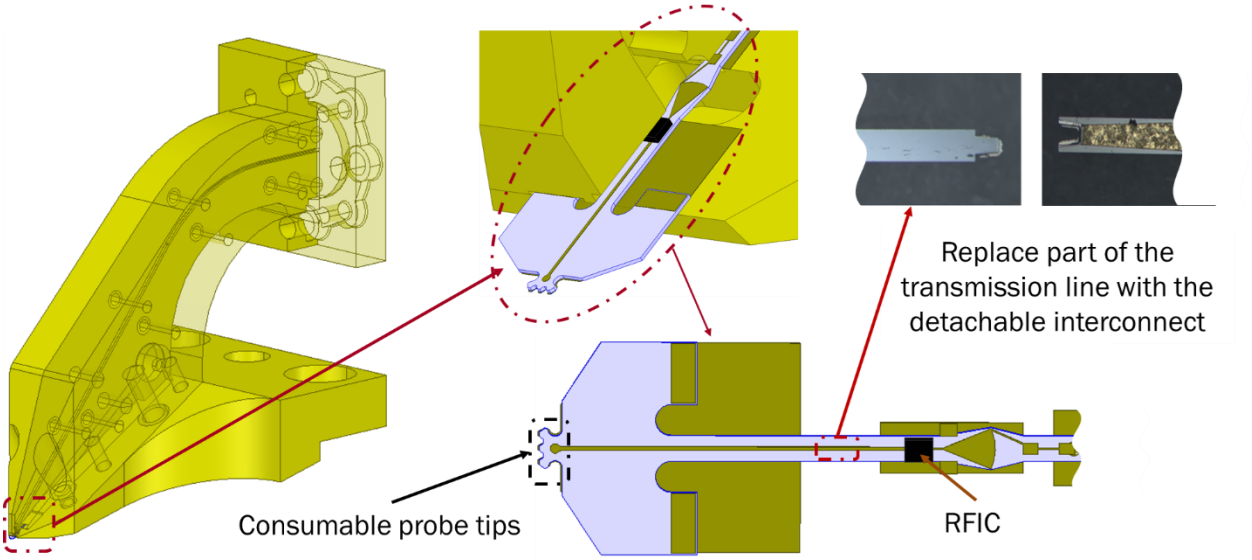


Figure 1.10: Micro-machined on-wafer probe station, probe chips and chip-to-chip interconnects.

The following chapter will showcase the mechanical and electrical design of the detachable chip-to-chip interconnect. The mechanical design chapter will comprise stress analysis, simulation, and contact force estimation, with the assembly force measurement and simulation also being demonstrated in Chapter 2. In

Chapter 2, the interconnect's assembly force and contact resistance study will be presented, along with the measurement and analysis of the interconnect's lifetime.

Chapter 3 will present the electrical simulation and measurement, showcasing the design process of the chip-to-chip interconnect and how to measure its RF performance. Finally, a comparison between the chip-to-chip interconnect and beam lead interconnection will be made.

Chapter 4 will identify potential future applications and possible methods to enhance the prototype chip-to-chip interconnect based on our experiences.

2 Mechanical Design and Measurement of Detachable Interconnect

2.1 Force Analysis

To design an effective interconnect operating at Terahertz frequencies, designers must consider and adhere to the principles of mechanics of materials. This field of study examines the effects of external forces on a deformed body, as well as the internal forces generated within it. By analyzing the applied loads and forces, one can anticipate and predict the resulting deformation and reaction of the body. The concepts and formulas presented here are based on the content of the book "Mechanics of Materials" [41].

The first step of the mechanical analysis of a body is to analyze the forces applied to the body and the internal forces generated inside the body. The external forces can be categorized into two groups: Body forces and Surface forces.

Body Force: A force applied on a body without directly contact, for example, earth's gravitation or electromagnetic force.

Surface Force: A force directly contacting the body on its surface. In all cases, the surface forces are distributed over the area of contact.

After the forces are applied to the body, the body will tend to maintain an equilibrium status. The equilibrium of the body requires both *balances of forces* and *balances of moments*. The balance of forces prevents the body from moving. The balance of moments prevents the body from rotating. The equilibrium status is also one of the conditions we use while the interconnects are joined together. The example of the balance of forces and balance of moments are shown in Figure 2.1.

$$\text{Balance of force: } \sum F = 0$$

$$\text{Balance of moment: } \sum M = 0$$

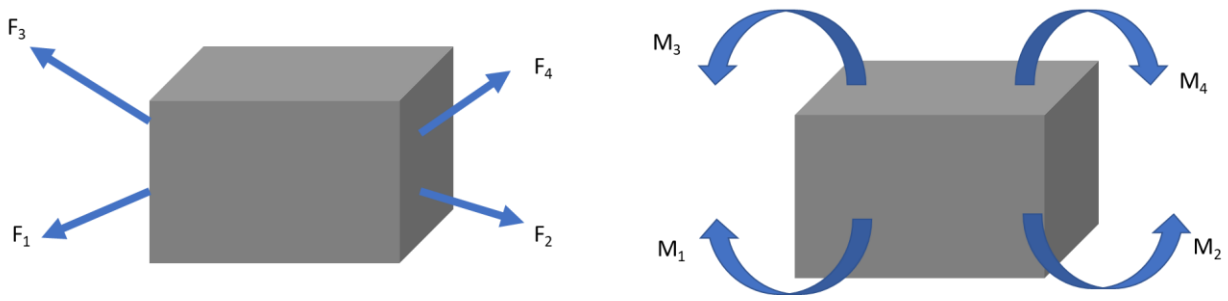


Figure 2.1: Force Equilibrium and moment equilibrium.

Another critical aspect of the mechanic of material analysis is the resultant force and moment acting inside the body. The resulting force and moment are important to hold the body together without breaking. In the following diagram, it shows a body under specific external force and in an equilibrium state, and the resultant force and bending moment.

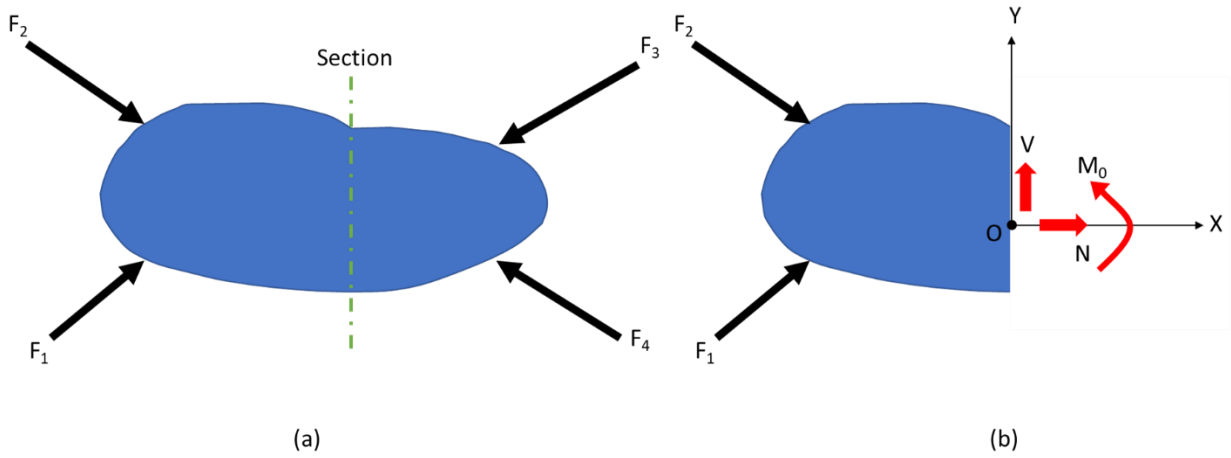


Figure 2.2:Body under external forces (a) and the internal resultant force and bending moment analysis (b).

Normal Force (N): The force acted perpendicular to the cross-section area. It causes push or pull on segments of the body.

Shear Force(V): The shear force lies parallel with the cross section. It causes the segments of the body to slide.

Bending moment(M_0): The bending moment is caused by external force and tends to bend the body.

$$F_x = -N \; ; \; F_y = -V$$

$$\sum M_0 = 0$$

2.2 Stress Analysis

To better understand how the body reacts while the external forces are applied to the body, it is necessary to introduce the concept of stress.

To analyze the stress, the cross-sectional area is divided into several small cubes as Figure 2.3 shows. The forces applied to the cube can be classified into two types of stress: **normal stress** and **shear stress**.

Normal Stress (σ): The force per unit area perpendicular to the area and cause the pull or push force to the area.

Shear Stress (τ): The force per unit area acts parallel to the unit area and cause bending to the area.

To simplify the analysis, two assumptions are made about the body: firstly, that it is continuous, meaning that no unit is void, and secondly, that it is cohesive, meaning that all units are connected without any breaks.

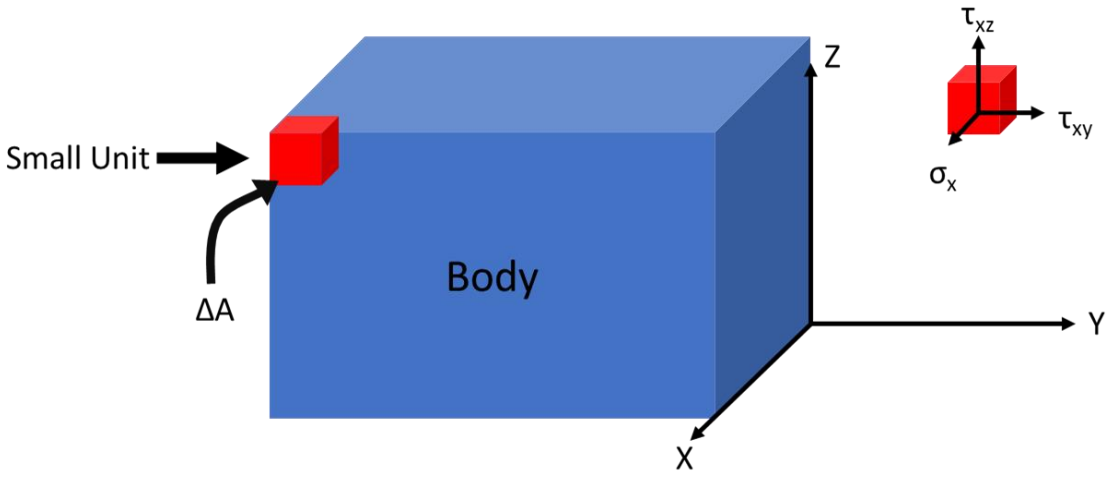


Figure 2.3:Concept of normal stress and shear stress.

$$\sigma_x = \lim_{\Delta A \to 0} \frac{\Delta F_x}{\Delta A}$$

$$\tau_{xy} = \lim_{\Delta A \to 0} \frac{\Delta F_y}{\Delta A}$$

$$\tau_{xz} = \lim_{\Delta A \to 0} \frac{\Delta F_z}{\Delta A}$$

2.3 Bending Analysis

The forthcoming section will explicate the internal shear and moment of the beam to comprehend the loading and bending applied to it. Moreover, comprehension of the maximum stress point on the beam will assist in the design of the chip-to-chip interconnects.

To ascertain the stress along the beam, it is crucial to examine how the internal shear and moment V(x) and M(x) respectively vary along the beam, as illustrated in Figure 2.4. By analyzing the maximum shear and moment, the location of the maximum stress can be determined. Once the maximum stress value and location are known, the cantilever beam can be designed without surpassing the allowable stress limit.

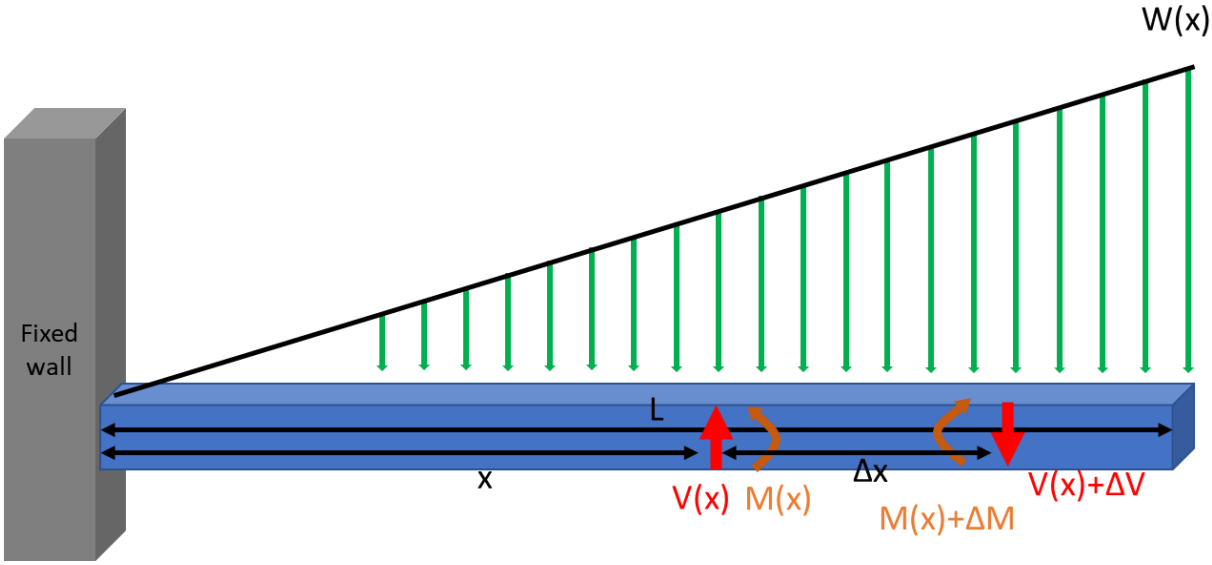
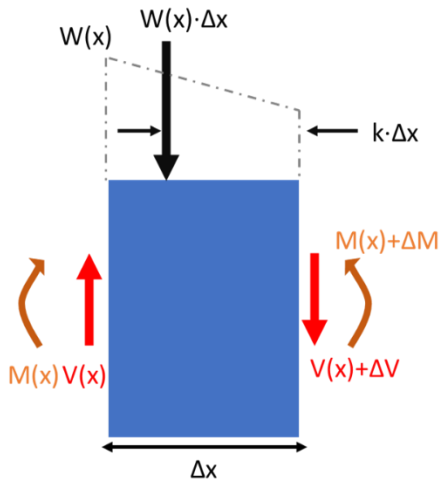


Figure 2.4:Fix cantilever beam diagram.

In order to provide a more comprehensive explanation, it is worth noting that in Figure 2.5, a small segment of the beam, represented by Δx, is subjected to analysis. It is important to recognize that the beam remains in a state of equilibrium, resulting in the derivation of the following equations.



$$\sum F = 0 \rightarrow \quad V - w(x)\Delta x - (V + \Delta V) = 0$$
$$\Delta V = -w(x)\Delta x$$
$$\sum M = 0 \rightarrow \quad -\Delta V - M + w(x)\Delta x[k(\Delta x)] + (M + \Delta M) = 0$$
$$\Delta M = V\Delta x - w(x)k(\Delta x)^2$$

Figure 2.5: Small segment of beam.

If the segments of the beam (Δx) are infinitesimally small (i.e., Δx→0), the equations reduce to the following equation.

$$\frac{dV}{dx} = -w(x)$$

$$\frac{dM}{dx} = V$$

The forthcoming section will explicate the bending behavior of a beam and its surface. As illustrated in Figure 2.6, when a bending moment is exerted on a beam, it induces deformation in the beam.

Figure 2.6:Fixed beam before deformation and after deformation.

Under the action of a bending moment, the top part of a beam experiences tension while the bottom part experiences compression. The neutral axis is the location axis within the beam where there is no change in length, and hence, no stress or strain is developed. This surface is neither in tension nor in compression and is located at the midpoint of the beam height under uniform bending moment, as shown in Figure 2.7.

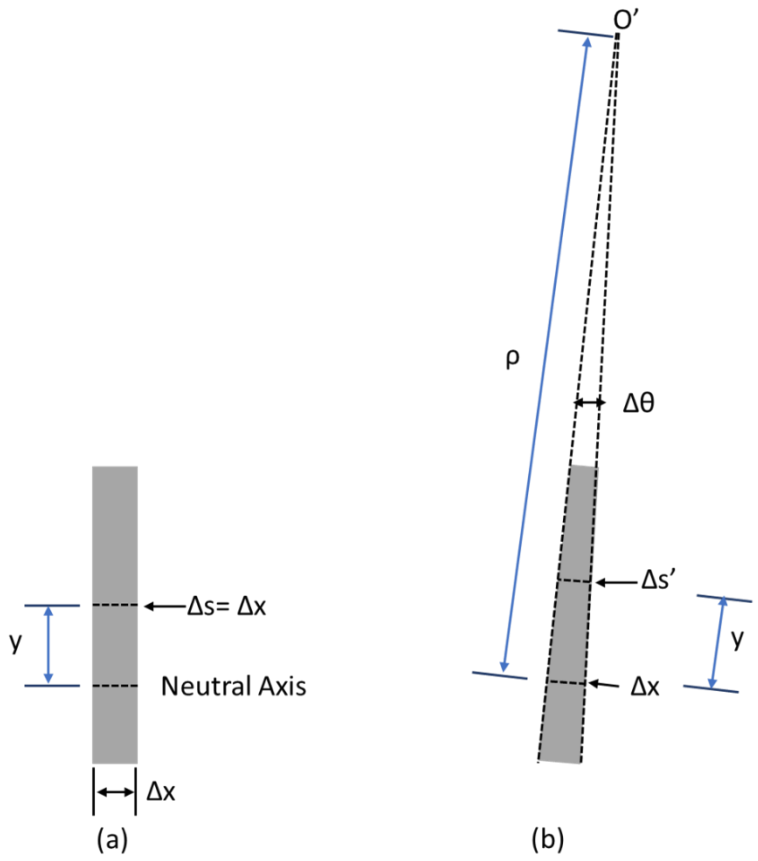


Figure 2.7:Small segments of beam before (a) and after deformed (b).

The deformation behavior of a small segment of a beam at the neutral axis can be observed in Figure 2.7. It is worth noting that the length of the line segment (Δx) at the neutral axis remains unchanged after deformation. The strain along the segment Δs can be expressed using the definition of strain as shown in the following equation.

$$\epsilon = \lim_{\Delta s \to 0} \frac{\Delta s' - \Delta s}{\Delta s} = \lim_{\Delta \theta \to 0} \frac{(\rho - y)\Delta\theta - \rho\Delta\theta}{\rho\Delta\theta} = -\frac{y}{\rho}$$

The strain derivation results in an essential conclusion that is dependent on the distance from the neutral axis to the observed plane (y). As a result, the highest strain occurs at the top plane of the beam, as indicated by the following equation.

$$\epsilon_{max} = \frac{c}{\rho}$$

Hence, the longitudinal normal strain varies linearly with the distance from the neutral plane (y). If the body behaves in the linear elastic region, the relationship between strain and stress will comply with Hooke's law, as depicted by the following equation.

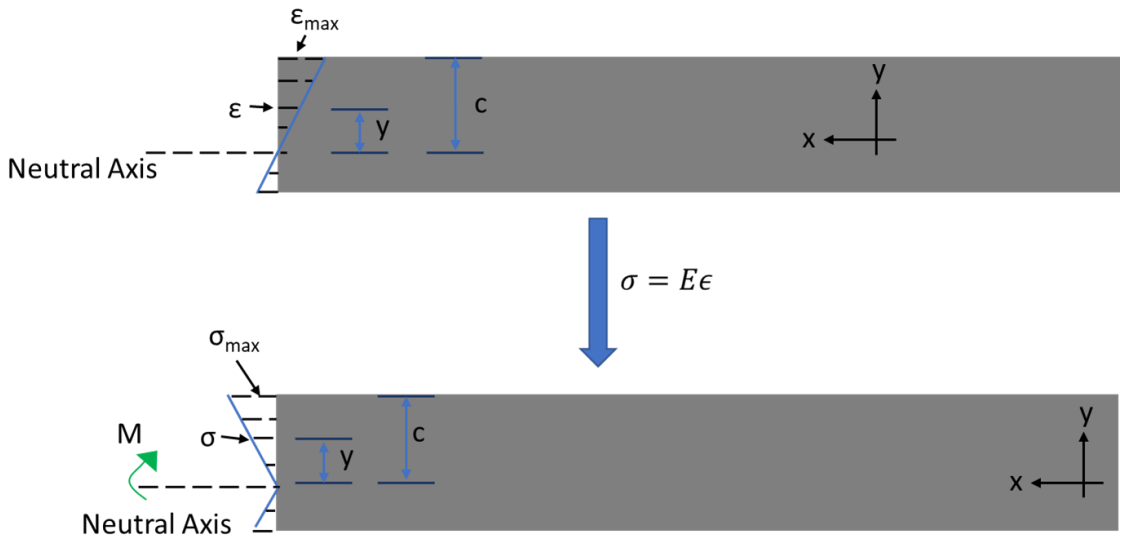


Figure 2.8: Strain and stress beam diagram.

$$\sigma = E\epsilon$$

The symbol "E" denotes the Young's modulus or modulus of elasticity, which is a fundamental material property that quantifies the linear relationship between stress and strain during elastic deformation. Specifically, the Young's modulus represents the proportionality constant that relates the applied stress to the resulting strain within the material's elastic regime.

The stress distribution over the cross-section of the beam is represented by the following equation.

$$\sigma = -\left(\frac{y}{c}\right)\sigma_{max}$$

At the neutral axis, the resultant force must be equal to the stress distribution over the cross-section, which must be equal to zero. The stress on the small segment of the cross-section (dA) can be represented by the following equation.

$$dF = \sigma dA = 0$$

$$\int dF = \int \sigma dA = \int -\left(\frac{y}{c}\right)\sigma_{max} dA = -\left(\frac{\sigma_{max}}{c}\right)\int ydA = 0$$

Since the maximum stress (σ_{max}) is not zero, $\int ydA$ must be zero.

$$\int ydA = 0$$

Therefore, the resultant moment is equal to the moment generated by the stress on the cross section lies on the neutral axis. The relationship can be represented by following equation.

$$dM = ydF = y \cdot (\sigma dA) = y \cdot \left(\frac{y}{c}\sigma_{max}\right) dA$$

$$M = \frac{\sigma_{max}}{c}\int y^2 dA$$

The moment of inertia of the cross-section surface is defined by the following equation.

$$I = \int y^2 dA$$

Thus, the relationship between the moment and stress can be simplified as the following equation.

$$\sigma_{max} = \frac{Mc}{I}$$

$$\sigma = -\frac{My}{I}$$

In the following chapter, these formulas will be useful in analyzing the mechanical design of detachable chip-to-chip interconnects.

2.4 Silicon Properties Discussion

In this section, we aim to explore the correlation between the Young's modulus (E) of silicon and its crystal orientation. Based on the findings of Dr. Matthew A. Hopcroft's research team [42], the Young's modulus of silicon is dependent on its crystal orientation. Within the scope of our interconnect design, our focus lies on analyzing the orientation of the silicon surface specifically in the X-Y plane to facilitate a simplified analysis.

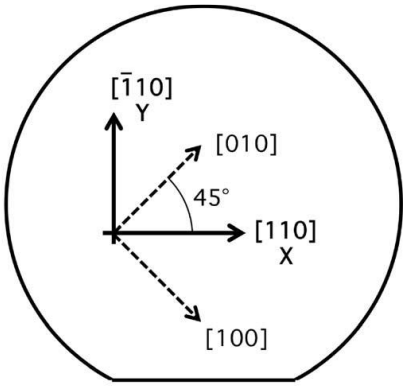


Figure 2.9:Direction of axes in [110] wafer [42].

Figure 2.9 displays the crystal orientation range of the wafer, spanning from (110) to (100). As observed in Figure 2.10, the Young's modulus of the (110) wafer changes from the Y-axis to the X-axis, in accordance with the crystal orientation displayed in Figure 2.9.

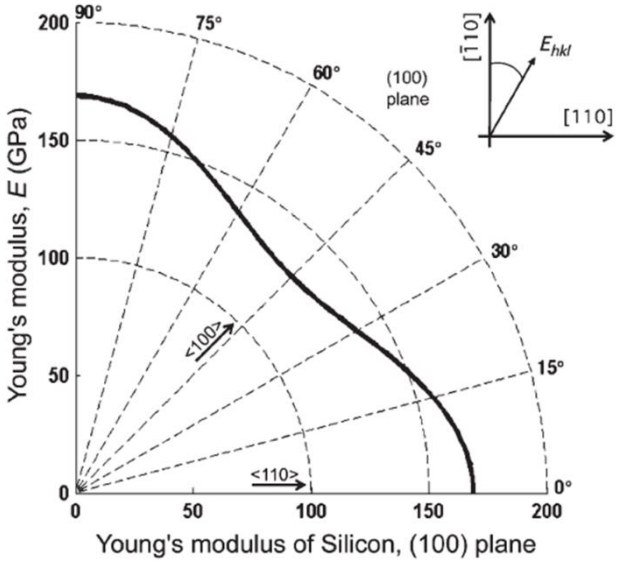


Figure 2.10:Values of Young's Modulus versus orientation in silicon [110] plane [42].

In our earlier work on the probe chip [43], the silicon orientation was aligned with the (110) plane, and the applied Young's modulus for the probe chip design was measured at 185 GPa, consistent with the findings presented in [42]. In the subsequent section, we endeavor to examine the stress and deformation of the prototype interconnect. Given that the prototype interconnect's orientation is aligned with the (110) axis, we have employed a Young's modulus of 185 GPa for our analysis.

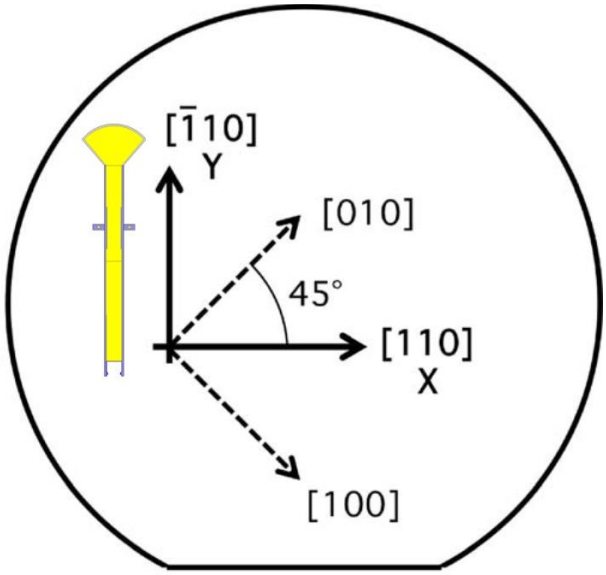


Figure 2.11:Prototype interconnect placement versus orientation [42].

For the chip-to-chip interconnect, we utilized a single crystal silicon wafer with a device layer thickness of 15 µm. Notably, the Young's modulus of silicon ranges between 185 GPa to 130 GPa, depending on the crystal orientation.

2.5 Detachable Chip-to-chip interconnect prototype mechanics analysis

The design of chip-to-chip interconnects involves two significant aspects: the mechanical aspect and the electrical aspect. In terms of mechanical design, the primary requirement is to reliably connect two different

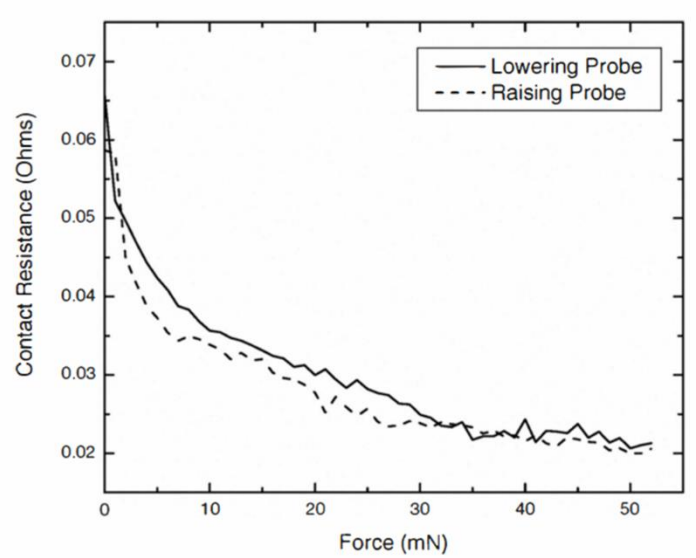


Figure 2.12:Gold to gold contact force vs. contact resistance [43].

devices or subsystems. To achieve this goal, the stress on the interconnector parts is increased to increase the contact force. Moreover, increasing the contact force will also decrease the contact resistance. The relationship between contact force and contact resistance for a gold-to-gold contact is shown in Figure 2.12, where the contact resistance decreases to 0.02 Ohm with a contact force higher than 50 mN.

To try out the possibility of our detachable interconnect, the detachable chip-to-chip interconnect prototypes were designed, as shown in Figure 2.13 below. The chip-to-chip interconnect prototype consists of a plug chip and a socket chip. The socket interconnects are equipped with tap structures that slide into the notch structures on the plug component, thereby preventing the interconnect from unintended separation during operation.

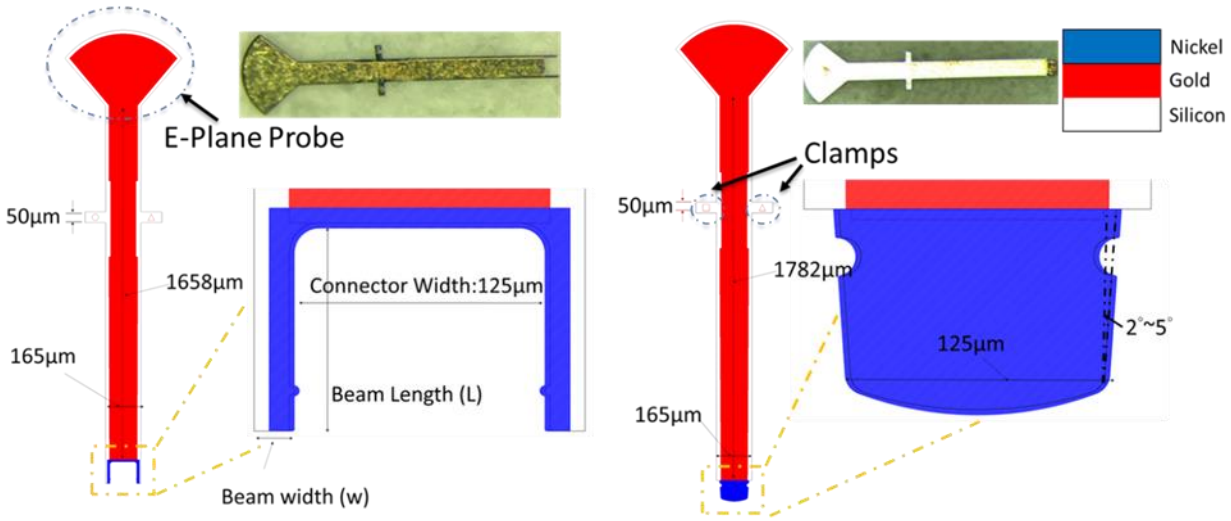


Figure 2.14:Chip-to-chip detachable socket and plug chips prototype.

In the following section, the socket chip interconnects part will be analyzed. In the socket chip's arm shown in Figure 2.14. There are three kinds of socket beams length (L) design: 163.5 µm, 143.5 µm and 103.5 µm. The beam width (w) is 17.5 µm and the beam thickness (t) is 15 µm.

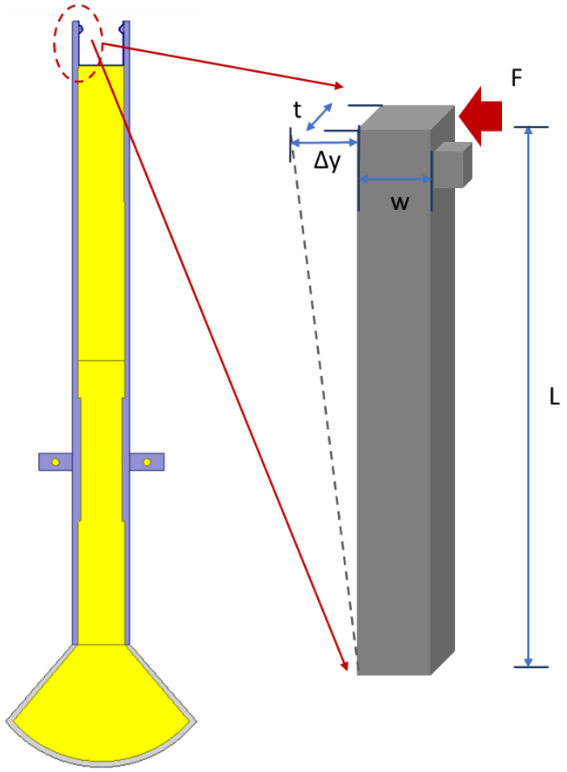


Figure 2.13:Chip-to-chip detachable socket chip and interconnect arm structure.

Based on the design of the prototype tip structure, the contact force is concentrated on the top of the beam. The derivation of the maximum stress is shown below.

$$M = F \cdot \frac{1}{2}t$$

$$\sigma = \frac{M \cdot L}{I} = \frac{F \cdot \frac{1}{2}t \cdot L}{I}$$

$$F = \frac{2I}{L \cdot t}\sigma$$

According to [41], the deflection of beam represent as below.

$$\Delta y = \frac{FL^3}{3EI} = \frac{2L^2}{3Et}\sigma$$

$$\sigma = \Delta y \cdot \frac{3Et}{2L^2}$$

Based on the analysis of the experimental data, it can be deduced that the deflection on the tip of the 163.5 μm beam length socket chip amounts to 16 μm, while the maximum stress reaches an estimated value of 3.4 GPa. It should be noted that the prototype interconnect design employs a silicon substrate, with an elastic constant (E) of 185 GPa, and a thickness of 15 μm. These findings are presented in tabular form below, and were derived using the appropriate stress formula for the aforementioned calculations.

Table2. 1:Prototype chip-to-chip interconnect stress calculation.

	σ	F
L=103.5um; Δy=5um	3.79 GPa	36.3 mN
L=143.5um; Δy=11um	3.53 Gpa	22 mN
L=163.5um; Δy=16um	3.45 GPa	17.6 mN

To further investigate the stress on the interconnects, the Ansys mechanics simulation tool was employed. The results obtained through this simulation method were found to be consistent with the previously

calculated values. Figure 2.15 illustrates the mechanical simulation layout used in Ansys mechanics, where the force applied to the tips of the arms was simulated to determine the bending distance (Δy) and the stress levels along the socket chip interconnect arms. Table 2.2 provides an overview of the worst-case scenarios for three distinct interconnect arm lengths, as determined by the simulation method.

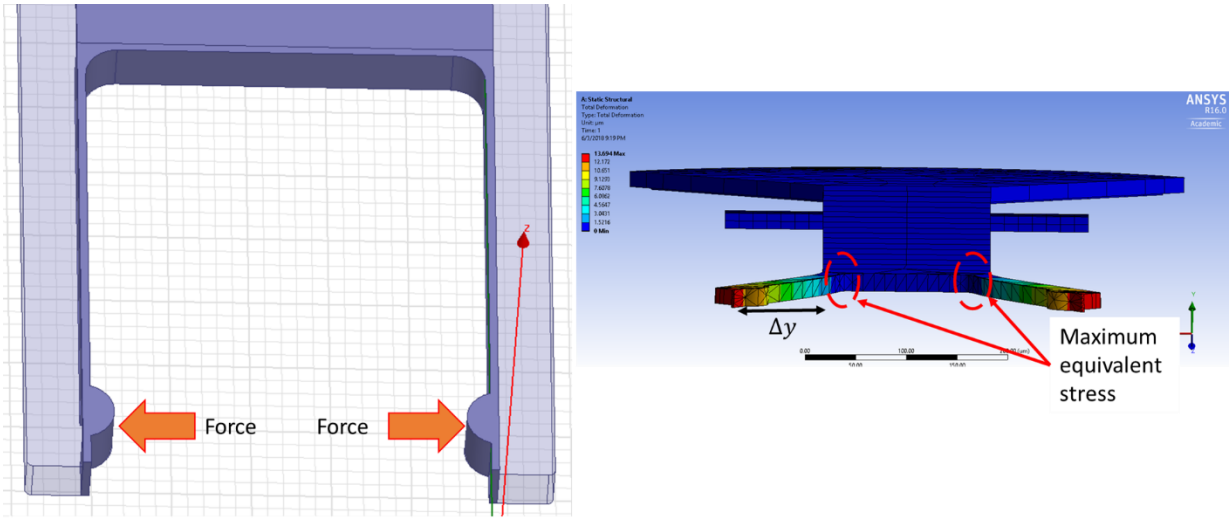


Figure 2.15:Ansys Mechanics simulation layout (a) and results (b)

The summary of all three prototype simulation results shows in Table 2.2.

Table 2.2:Ansys simulation result summary.:

L(μm)	Δy (μm)	$F_{Applied}$	σ_{MAX}
103.5	5	45mN	3920MPa
138.5	11	30mN	3637MPa
163.5	16	27mN	3497MPa

The simulation results agree with the earlier calculations. Notably, the 103.5 μm beam necessitates the highest level of force to generate the desired deflection on the beam. Conversely, the 163.5 μm beam requires the lowest force to achieve the necessary level of deflection for assembly purposes. It should be noted, however, that the stress levels observed in all three scenarios are quite similar, thus rendering a precise comparison between them somewhat challenging.

2.6 Detachable Chip-to-chip interconnects prototype assembly experiment

In order to accurately measure the interconnect chips, a series of channels were etched onto a low resistivity wafer to facilitate the assembly process. The alignment wafer containing these channels is depicted in Figure 2.16 (a). The plug and socket chips were then carefully maneuvered into the channel, and a transparent quiz wafer was placed over the channel to prevent the interconnect chips from tilting during the joining process. Using a micromanipulator with a needle, the plug chip was pushed from the right side in order to bring the plug interconnect chip closer to the socket interconnect chip. The resulting assembly process is shown in the right-hand side of Figure 2.16 (b). Following the successful joining of the chips, they were gently moved from the alignment wafer into the RF channel on the waveguide.

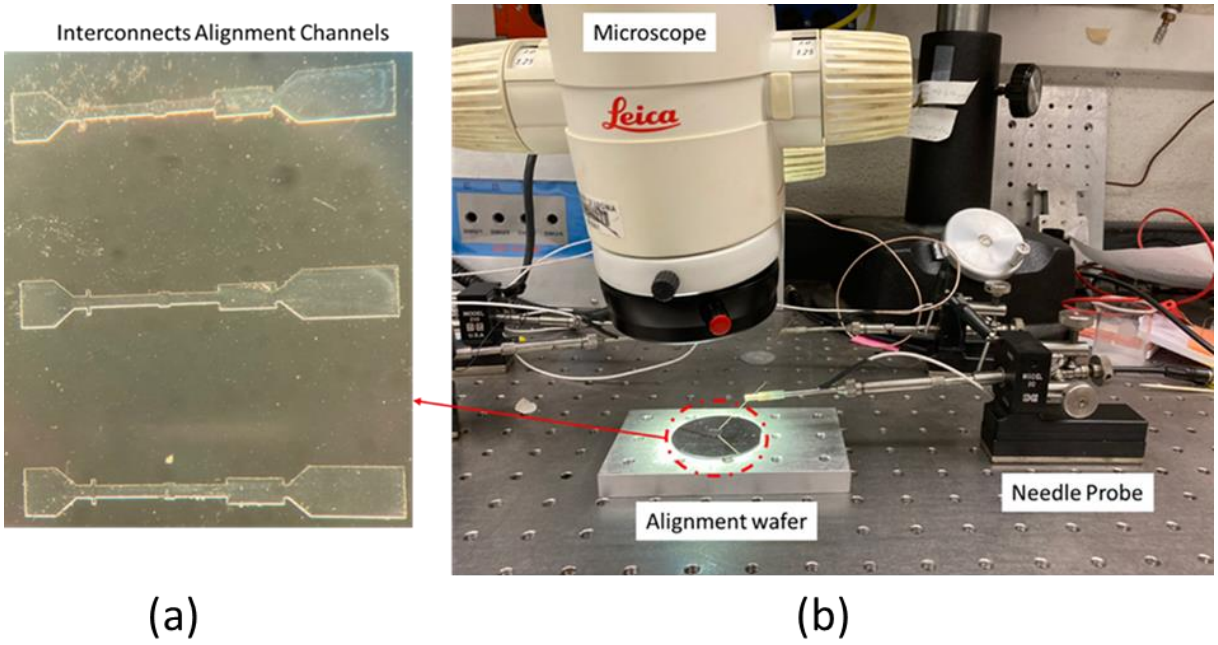


Figure 2.16:Chip-to-chip interconnect prototype alignment wafer (a) and assembly setup (b).

However, the chip-to-chip interconnect prototype assembly process faced several difficulties. On the mechanical design, the prototype socket chip interconnect part breaks very often during the assembly process. Over forty socket interconnect chips broke during the assembly process, and the most fragile part of the socket interconnect is the arms, as Figure 2.17 shows.

One possible explanation for the high rate of interconnect chip breakage during assembly is misalignment between the plug chip and socket chip within the channel. This misalignment resulted in the application of direct pushing force onto the beam, generating a normal force and subsequent normal stress on the silicon substrate.

The misalignment of interconnect chips during the assembly process represents a significant factor contributing to the high rate of failure during assembly. As demonstrated in Figures 2.17 (a) and (b), the arms of the interconnect chips were found to be particularly susceptible to breaking or cracking as a result of this misalignment. Of more than fifty chips measured, only two were found to be successfully connected, although RF measurements revealed that even these two connections ultimately failed. While the failure of the prototype interconnect design can be attributed to a number of factors, this section specifically focuses on the mechanical aspects of the design.

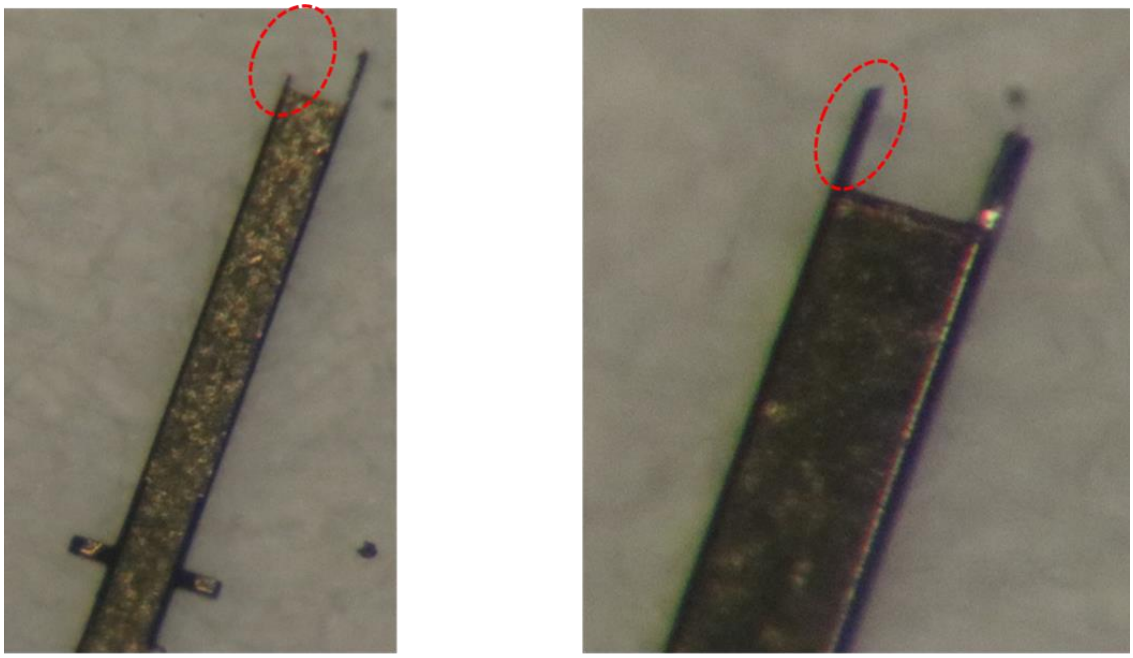


Figure 2.17: Detachable chip-to-chip interconnect prototype socket chips fail examples (a) broken arms (b) cracked arms

2.7 Detachable chip-to-chip tapered interconnects review and modification.

The tapered interconnect assembly experience highlighted two key mechanical design issues that require improvement. The first concerns the thickness of the socket chips' arms, which at 17.5 μm, are significantly thinner than the thickness of the silicon substrate (15 μm). This structural weakness makes the arms particularly vulnerable to breaking or cracking during the assembly process. Secondly, the issue of misalignment between the plug and socket chips during assembly represents a major obstacle to the successful connection of the interconnect chips. Improving these mechanical design aspects will be critical to the successful development and implementation of a reliable interconnect solution.

In order to address the two key mechanical design challenges outlined above, the concept of the morse taper, also referred to as a self-aligned taper, was utilized as a reference point for design. The shape of the morse taper is depicted in Figure 2.18.

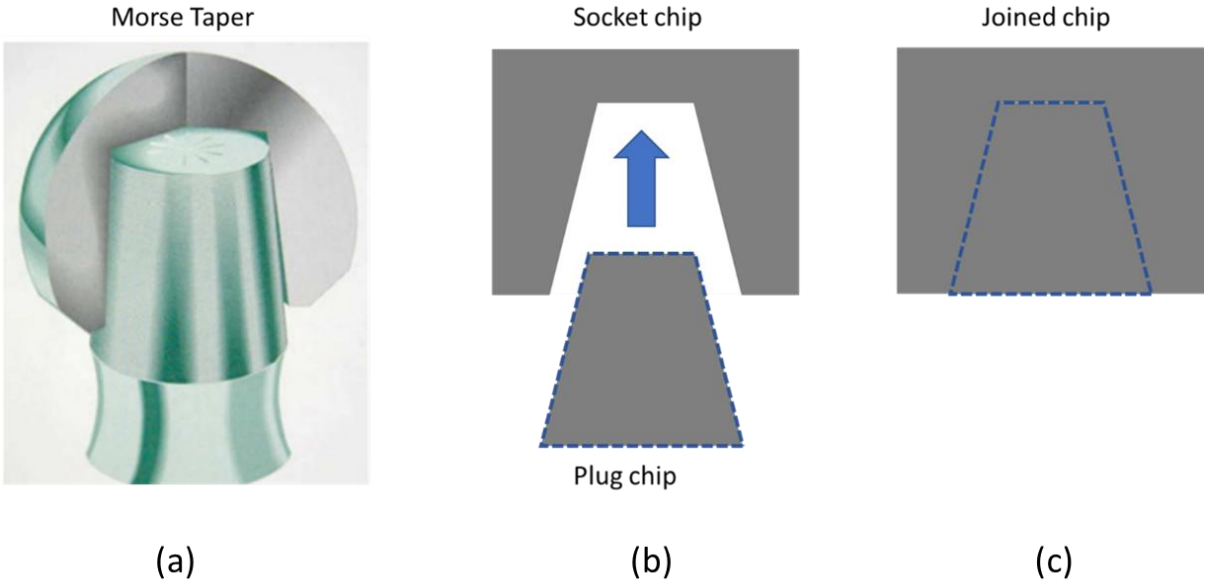


Figure 2.18:(a) Morse taper original application [52](b) Morse taper concept on chip-to-chip interconnect before assembly (c) Morse taper concept on chip-to-chip interconnect after assembly.

The concept of the morse taper design is demonstrated in Figure 2.18, where (a) shows its implementation in the medical field, and (b) and (c) exhibit its application in flat chip-to-chip interconnects.

The updated mechanical design for the chip-to-chip interconnect has been influenced by the self-holding tapers seen in machine tools, such as Morse and Jacobs tapers. These tapers function by inserting a conical plug into a conical socket with a matching taper angle, typically less than 7° [44]. For the chip-to-chip interconnects, we use an interference fit where the plug, featuring an 11° taper, is slightly larger than the socket. The tapered design is depicted in Figure 2.19, with plug bases ranging from 96 µm to 100 µm in width and a 100 µm socket opening. Additionally, a 2 µm thick layer of Nickel is coated on both the plug and socket interconnects. This design induces a lateral force on the socket when the two parts are pressed together and produces self-alignment between the two parts during assembly, significantly simplifying the process.

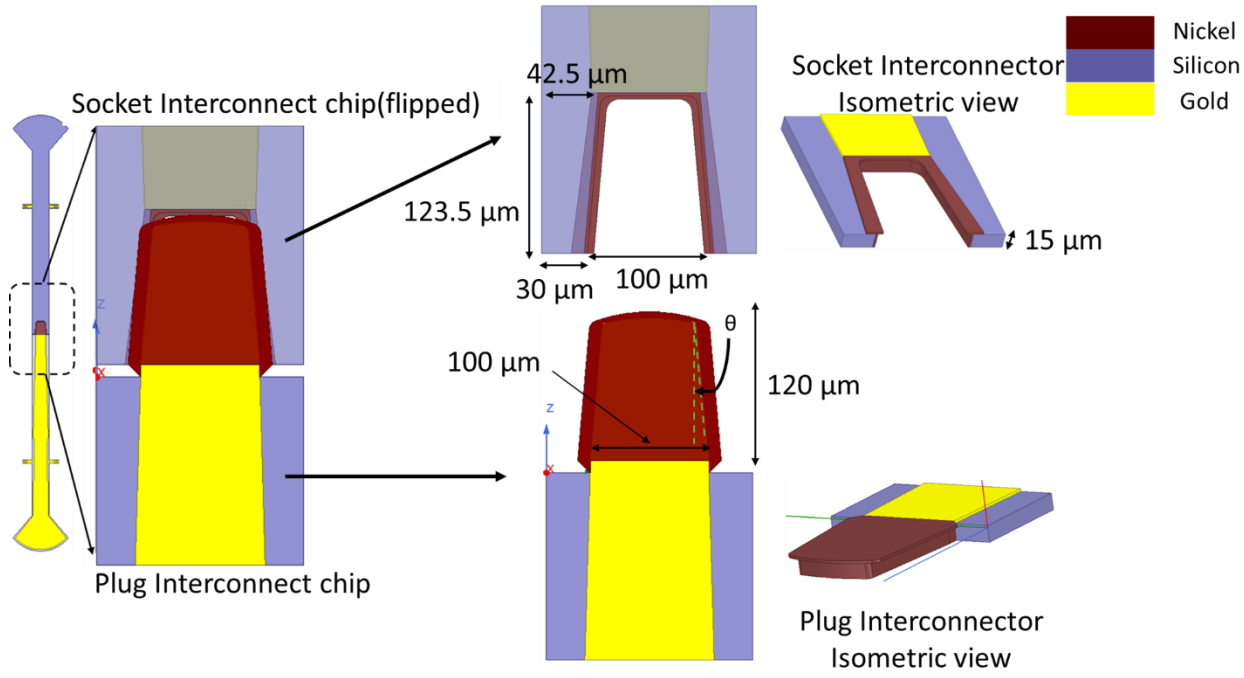


Figure 2.19:Modified chip-to-chip interconnect demonstration.

Figure 2.19 illustrates the modified chip-to-chip interconnect, wherein the blue section represents the high resistivity silicon substrate with a height of 15 μm. The yellow section corresponds to a gold layer of approximately 2 μm, while the red section corresponds to a nickel layer of approximately 2 μm.

The width difference between the plug and socket interconnectors affects the stress and contact force exerted on the socket beams. Specifically, a wider extension (Δy) of the plug interconnector results in higher stress (σ) and contact force (F) on the socket interconnector beams. To regulate these forces and ensure the socket interconnector sidewall is not subjected to excessive stress, the width (Δy) of the plug interconnector was varied between 96 μm and 100 μm to produce different contact forces on the female interconnector beams. The width of the socket interconnector was kept constant at 100 μm, and the thickness of the Nickel coating on the sidewall was approximately 2 μm.

2.8 Detachable tapered chip-to-chip interconnect mechanic analysis

2.8.1 Non-Prismatic Beam Analysis and Simulation

To conduct a comprehensive mechanics analysis of the modified chip-to-chip interconnect, it is crucial to consider the non-prismatic beam shape of the socket interconnector arms. By analyzing the non-prismatic beam, designers can obtain a better understanding of the interconnect's behavior and control the stress and deformation of the socket interconnect, leading to a more optimized design.

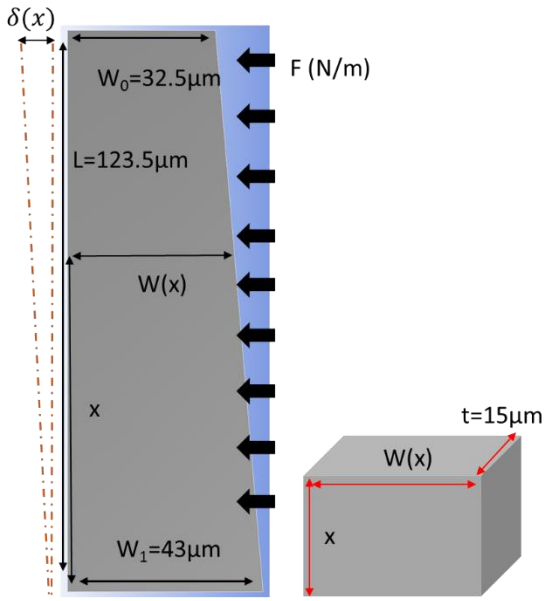


Figure 2.20:Non-prismatic beam applied with uniform load.

To conduct the analysis, the initial step is to analyze the fixed end non-prismatic beam presented in Figure 2.20. The beam's top width (w_0) is 32.5 µm, and the bottom width (w_1) is 43 µm. The length of the beam (L) is 123.5 µm, and the thickness is 15 µm. According to the Young's modulus (E) analysis in [42], the non-prismatic beam on [110] silicon is approximately 160 GPa. The symbol "F" in the context of bending moment refers to the applied force on the non-prismatic beam.

According to Mechanics of Materials [41], the bending stress shows as following formula.

$$\text{Loading Force: } -w(x) = EI\frac{d^4\delta(x)}{dx^4}$$

$$\text{Bending Stress: } \sigma(x) = \frac{M(x)\cdot {}^{w}/_{2}}{I}$$

Bending Moment: $\mathrm{M(x)} = \mathrm{FLx} - \frac{1}{2}FL^2 - \frac{1}{2}Fx^2$

Bending Inertia: $\mathrm{I} = \frac{1}{12}tw^3$

The deformation of the beam can be obtained by solving the following equation. Since one end of the beam is fixed, the deformation rate $(\partial\delta(\mathrm{x}))/\partial\mathrm{x}$ and the deformation $\delta(\mathrm{x})$ are both zero at x=0.

$$\delta(\mathrm{x}) = \iint \frac{M(x)}{EI} dx^2$$

Boundary conditions: $\frac{\partial\delta(x)}{\partial x} = 0$; $\delta(\mathrm{x})=0$ at x=0

In the case of a non-prismatic beam, the width varies linearly along the beam's length. Consequently, the width of the beam can be characterized using the following equations:

$$\mathrm{w} = w_1 - \frac{w_1 - w_0}{L}x$$

Furthermore, the moment of inertia of the non-prismatic beam also varies along its length and can be mathematically represented as follows:

$$\mathrm{I(x)} = \frac{1}{12}t(w_1 - \frac{w_1 - w_0}{L}x)^3$$

According to the relation of bending deformation ($\delta(\mathrm{x})$) and bending moment ($\mathrm{M(x)}$), the bending stress and deformation can be derived as following procedure.

Non-prismatic beam deformation: $\frac{d^2\delta(x)}{dx^2} = \frac{M(x)}{EI} = \frac{FLx - \frac{1}{2}FL^2 - \frac{1}{2}Fx^2}{\frac{1}{12}Et(W_1 - \frac{W_1 - W_0}{L}x)^3}$

Non-prismatic beam stress: $\sigma(\mathrm{x}) = \frac{6 \cdot M(x)}{t \cdot w^2}$

Boundary conditions: $\frac{\partial\delta(x)}{\partial x} = 0$ & $\delta(\mathrm{x})=0$ while x=0.

To streamline the analysis and validate the accuracy of the calculation procedure, a uniformly distributed load of 1000 N/m was applied along the fixed-end non-prismatic beam. The stress and deformation results were computed using Matlab, and subsequently simulated using Ansys Mechanical under the same load conditions. Figure 2.21 illustrates a comparison of the results obtained from the calculation and simulation methods.

Figure 2.21 highlights the notable agreement observed between the calculation and simulation results for both stress and deformation. The simulation outcomes confirm the precision of the formula applied to the non-prismatic beam under uniformly distributed loads. Subsequently, the following step involves estimating the load and stress experienced by the modified chip-to-chip interconnect

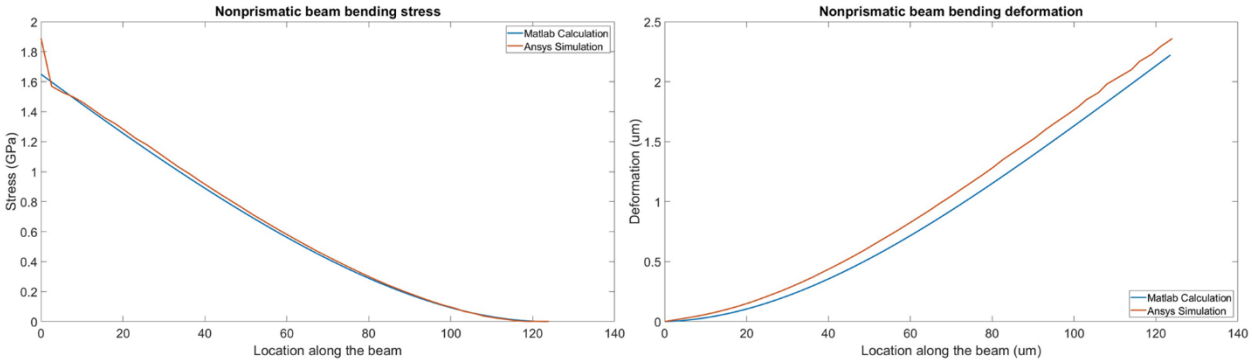


Figure 2.21:Non-prismatic beam stress and deformation comparison.

2.8.2 Mathematical Analysis of Tapered Chip-to-chip Interconnect

To ensure precise estimation of deformation and stress on the modified chip-to-chip interconnect, it is imperative to ascertain the load borne by the socket interconnect's beam. The magnitude of this load will dictate the degree of stress experienced by the beam. With regard to interconnect design, the deformation is chiefly influenced by the male connectors. Various load models were evaluated, and after careful scrutiny, the force model illustrated in Figure 2.22 was deemed to closely align with the simulation results obtained from Ansys.

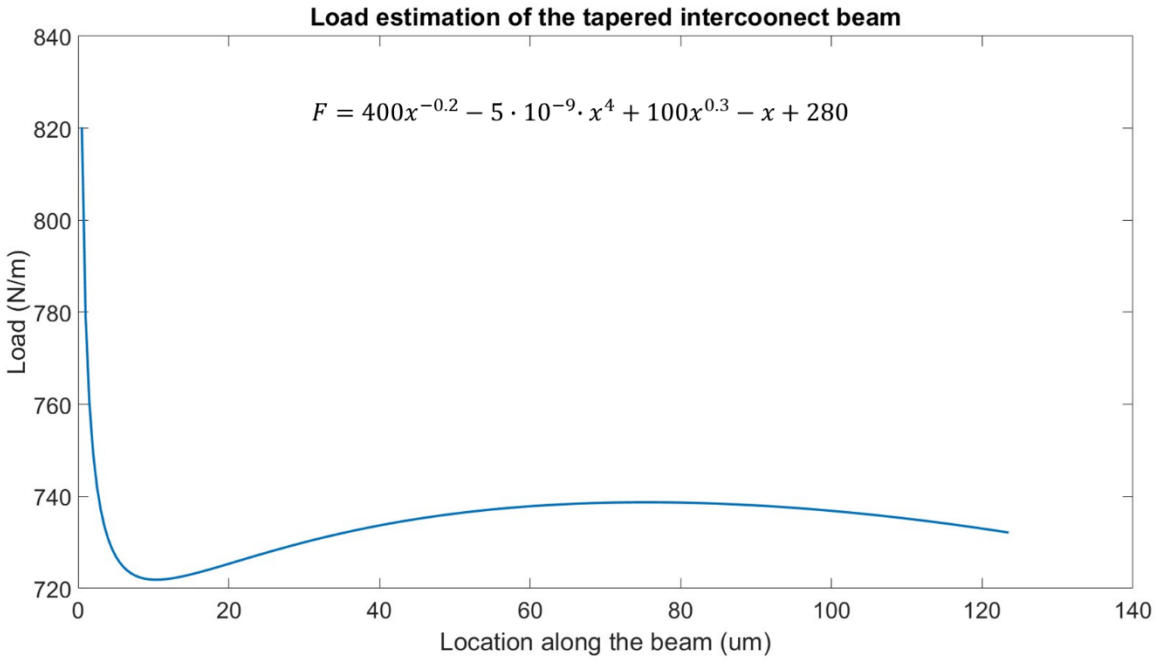


Figure 2.22:Modified Chip-to-chip interconnects load estimation.

According to this model, the contact force initially starts at 820 N/m and exponentially decays to 720 N/m. This distribution of forces is consistent with the expected behavior of the interconnect, with the highest contact force occurring at the bottom of the beams. As depicted in Figure 2.23, the Ansys model consisted of a fixed back for the socket chip interconnector, while the plug chip was pushed towards the socket chip. The dimensions of the interconnector are indicated in the Figure 2.23.

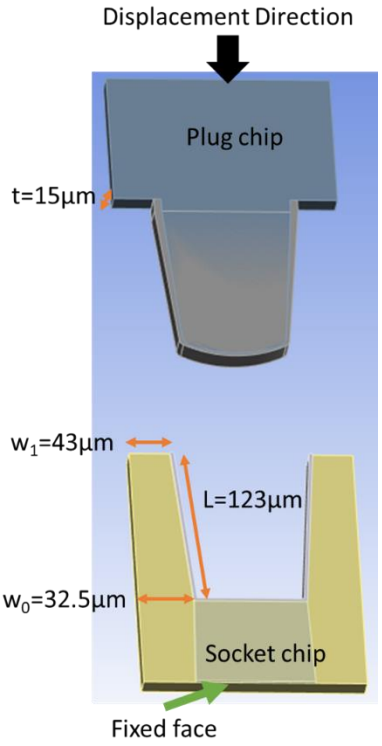


Figure 2.24: Ansys simulation of tapered interconnect assembly.

The stress and deformation results for the interconnect were calculated using this load model and compared to the simulation results, as shown in Figure 2.24.

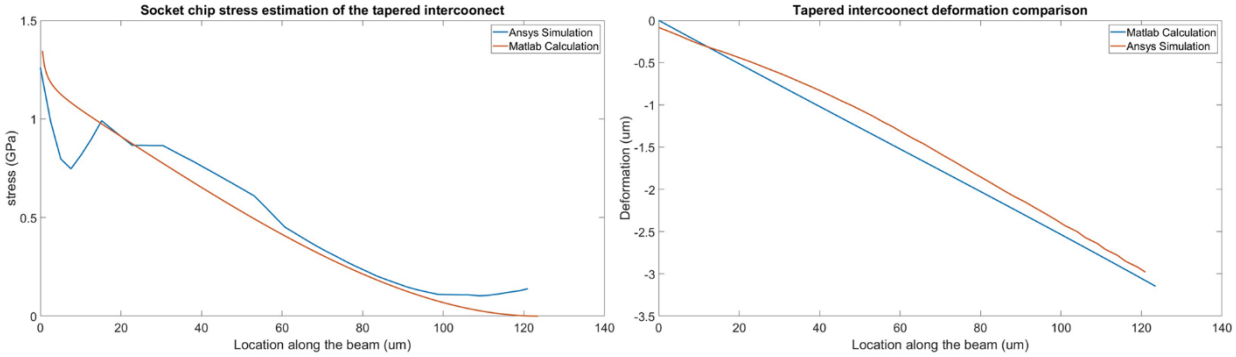


Figure 2.23:Tapered Chip-to-chip interconnects stress and deformation comparison.

Figure 2.22 illustrates that the load applied on the socket interconnect beam follows a non-linear distribution. Specifically, the load magnitude at the bottom of the beam is observed to be 820 N/m, which exponentially decays to 720 N/m. Additionally, Figure 2.24 (a) provides a comparison between the results obtained from the Ansys Mechanical simulation and Matlab calculations. The Ansys Mechanical model assumes that the plug interconnect chip is 3 µm wider than the socket interconnect chip, allowing for an approximate

deformation of 3 μm at the top of the socket chip beam. During the simulation, the plug interconnect chip is positioned at the same plane as the socket chip and is subsequently pushed into the interconnector part of the socket chip.

The simulation results obtained were in good agreement with the calculation results, indicating a consistent outcome. The appearance of a small dimple at a position approximately 10 μm away from the origin of the simulation results was attributed to the round corner design. Figure 2.24 (b) illustrates a comparison of the deformation obtained from the simulation and calculation results, further corroborating the agreement between the two methodologies. Consequently, the simulation and calculation results demonstrated that the highest stress and load were concentrated at the bottom of the socket interconnector beam, with a decrease in magnitude observed as the beam extended. By manipulating the plug chip interconnector head width, one could control the deformation, $\delta(x)$, and stress, $\sigma(x)$, experienced by the socket chip beam. Additionally, adjusting the socket chip's bottom round corner radius could alleviate the stress concentration at the bottom of the socket interconnect chip.

2.8.3 Disassembly Force Analysis

Based on our load model assumptions, we are able to estimate the magnitude of force required for separating the interconnect. As reported in the Journal of Biomechanics [45], the disassembly force for the morse taper interconnect is dependent upon the surface static friction coefficient, μ, and the perpendicular force applied on the plug interconnector. The findings of our disassembly force analysis are illustrated in Figure 2.25.

$$Disaseembly\ Force = -N(\sin\theta - \mu cos\theta)$$

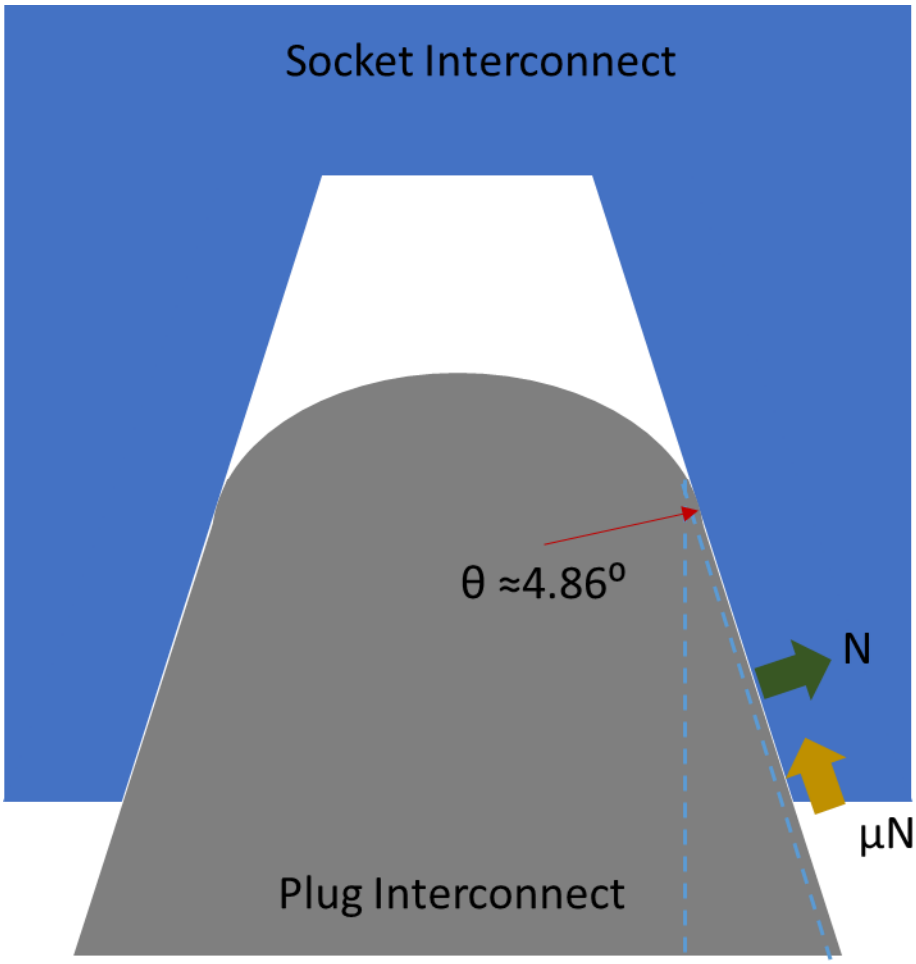


Figure 2.25:Disassembly force analysis

Based on the applied load assumption, the normal force range is estimated to be between 720 and 740 mN per meter. It is important to note that in the current design, the head of the plug interconnector does not come into contact with the socket interconnector. Therefore, the force considered in the analysis is limited to the range between 10 and 123.5 μm on the socket interconnect beam.

Based on the assembly measurement, it was observed that the effective contact area is not spread throughout the entire beam. Hence, for the disassembly force analysis, it was assumed that only 100 μm of the beam constituted the effective contact area. Additionally, according to the Machinery's Handbook [46], the static friction coefficient (μ) was determined to be 0.7.

The disassembly force of 44 mN reported for one beam. If we take consider the force on both beams, the disassembly force is 88 mN. This was calculated using the following formula:

$$Disassembly\ force = 730 \cdot 100 \cdot 10^{-6} \cdot \left(\sin(4.86°) - 0.7 \cdot cos(4.86°)\right) = 44\ mN$$

An Ansys Mechanics simulation was conducted to determine the assembly force. The results showed that a force of 65 mN was necessary for disassembly. However, it should be noted that the calculated disassembly force is strongly influenced by the static friction coefficient, μ. This coefficient is in turn influenced by the quality of the nickel coating. In the event that the static friction coefficient of the nickel coating might vary from 0.5 to 1.1, the disassembly force will correspondingly change from 60.4 mN to 147.6 mN.

2.8.4 Circular corners at the socket interconnector

A technique employed to reduce the stress in interconnects involved the inclusion of circular corners at the base of the socket interconnector. An analysis using Ansys Mechanical was conducted to examine the highest level of stress under varying fillet corner radii while maintaining the same deformation of the socket interconnector. Specifically, the simulation entailed the deformation of a 5 μm socket interconnect while varying the bottom corner radius from 8 μm to 12 μm, as illustrated in Table 2.3.

According to the simulation findings, increasing the corner radius can lead to a slight reduction in stress on the beams of the socket interconnect. However, when the corner radius surpasses 12 μm, the reduction in stress is not significant. The optimal corner radius for the socket interconnect, as indicated by the Ansys Mechanical simulation results, is 12 μm.

The extent of deformation and stress on the beams of the socket interconnector is dependent on the width extension (Δy) of the plug chip's interconnector. A greater width extension translates to increased contact force and stress on the interconnector beam of the socket chip. In accordance with the non-prismatic beam formula, under constant width (W) and length (L) of the female interconnector beam, greater deformation (δ(x)) will lead to heightened stress and contact force on the beams of the socket interconnector.

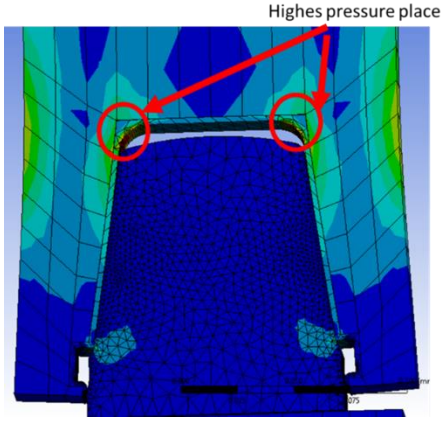
Table2. 3: Ansys corner radius simulation results.

	Bottom Corner Radius (μm)	Maximum Stress (MPa)	Deformation [Δy] (μm)
Case 1	8	4974	5
Case 2	10	4925	5
Case 3	12	4717	5
Case 4	14	4705	5

Our decision to compare the corner radius at 5 μm deformation was driven by the aim to observe a significant decline in stress levels and to comprehensively scrutinize the influence of corner radius on the maximum stress borne by the socket interconnector.

2.8.5 Comprehensive tapered interconnect simulation

In the context of mechanical simulation, the plug interconnects' extension width, denoted as Δy, has been observed to vary within the range of 2 µm to 5 µm, while the socket chip's bottom interconnector corner radius, denoted as R, has been observed to fluctuate within the range of 8 µm to 12 µm. It has been noted that increasing the corner radius, R, tends to alleviate stress concentration at the corner of the interconnect. Specifically, the maximum stress experienced by the female interconnects decreases from 4.9 GPa to 4.7 GPa when the corner radius is increased from 8 µm to 12 µm. However, it has been observed that further increasing the corner radius to 15 µm only results in a negligible decrease in stress of 12 Pa. Therefore, the socket interconnect bottom corner radius is 12 µm.



	Bottom Corner Radius (µm)	Maximum Stress (MPa)	Deformation [Δy] (µm)
Case 1	12	4080	5
Case 2	12	3300	4
Case 3	12	3028	3.5
Case 4	12	2687	3
Case 5	12	2480	2.5
Case 6	12	2128.43	2

Figure 2.26:(a) Ansys Mechanical layout (b)Ansys Mechanical stress simulation summarizes.

Alterations to the deformation (Δy) may significantly reduce the amount of stress placed on the socket interconnector. The outcomes of the estimations were used to simulate three distinct extensions of the plug chip interconnect width, denoted as Δy. The simulation results are presented in Figure 2.26 above. The results illustrate that, when the round corner (R=12 µm) is held constant, the deformation (Δy) diminishes from 5 µm to 2 µm, which, as demonstrated in Figure 2.25 (b), leads to a reduction in stress from 4.1 GPa to 2.1 GPa. The highest concentration of stress is detected at the base of the socket chip interconnectors, indicated by the red circled regions in Figure 2.26 (a). The stress reduction from 4.1 GPa to 2.1 GPa is demonstrated in the table on the right-hand side of Figure 2.26 when the deformation decreases from 5 µm to 2 µm. To balance the trade-off between contact resistance and stress on the socket interconnect, the deformation was tested at 3 µm, 2 µm, and 1 µm.

2.9 Mechanical Assembly Force Measurement

The current section aims to analyze the contact force and contact resistance of the interconnect between plug and socket chips. More specifically, for chip-to-chip interconnects, a robust contact force between the socket and plug chips is crucial in achieving a low contact resistance at the interface surface. Furthermore, this robust contact force is instrumental in establishing a strong and reliable connection between the plug and socket interconnects.

In order to enable the measurement of the contact force and contact resistance, modifications need to be made to both the plug chip and socket chip. The modified chips serve multiple purposes, including (1) supplying an assembly force, (2) producing a disassembly force, (3) measuring the contact resistance, and (4) ensuring the reproducibility of the measurements.

2.9.1 Modified Chips

To accomplish the goals mentioned earlier, changes are necessary in the socket and plug chips. Figure 2.27 illustrates the updated interconnect chips designed for DC measurement purposes, which eliminate the E-Plane probe and RF clamps parts. In RF design, the E-Plane probe couples the signal from the waveguide housing to the interconnect chip, while the clamps structures keep the interconnect chip in place within the RC channel of the waveguide housing. However, since DC chips do not require placement within the waveguide housing, these two features are unnecessary for DC measurement. As a result, the DC chips can be enlarged for easier operation.

In Figure 2.27, it can be observed that the dimensions of the DC chips are larger than those of the RF interconnect chips. Specifically, the DC chips are 4mm in length and 1mm in width, which is approximately twice as long and five times wider than the RF chips. The modifications made to the DC chips include the removal of clamp structures and E-plane probe structures. Instead, two circular gold contact pads have been incorporated into the chips to facilitate contact resistance measurements. Furthermore, a via hole has been added to the DC chips to enable needle probe landing and pushing of the chips.

The contact force and resistance of the RF interconnect chips can be analyzed by measuring the corresponding parameters in the DC interconnect chips, as the two share the same interconnector part design.

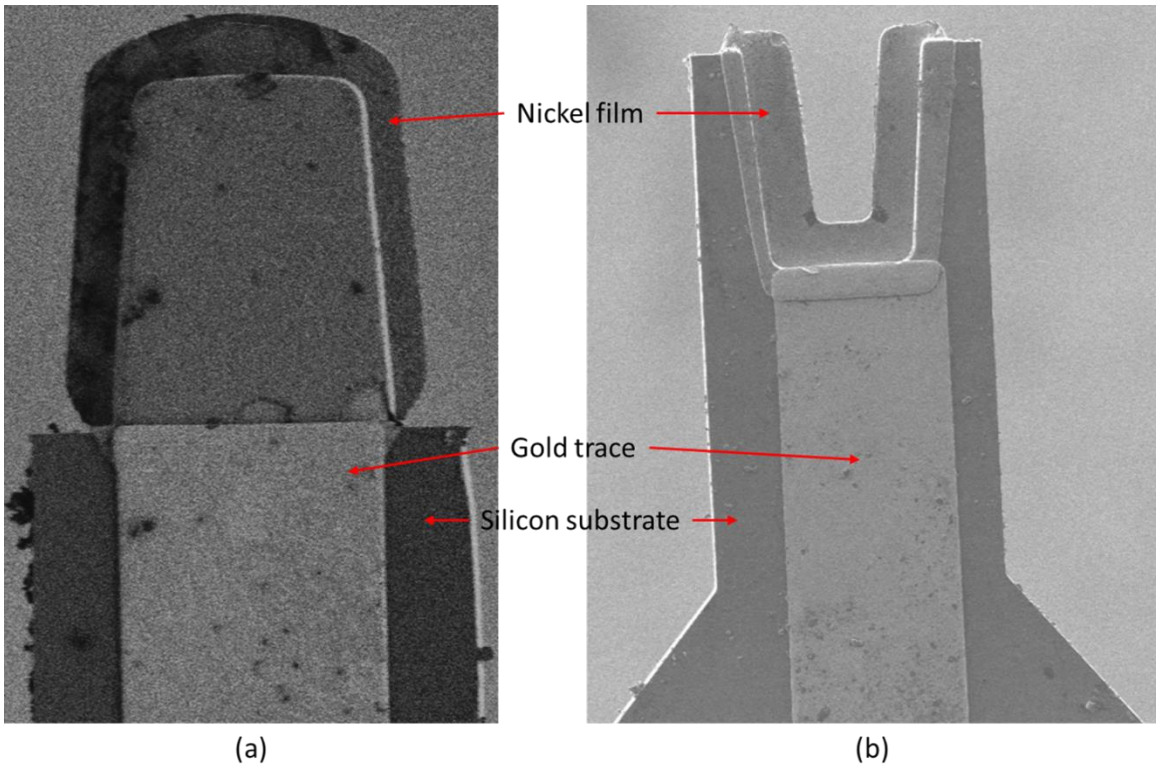


Figure 2.27: SEM images of (a) Plug chip (b) Socket chip

Three sets of interconnect chips were prepared for the DC measurement, each set with a different offset value of 1 μm, 2 μm, and 3 μm. The simulated and calculated results indicate that the interconnect chips with a 3 μm offset generate a stress of approximately 3.1 GPa at the bottom of the socket chip, while the chips with a 2 μm offset generate a stress of approximately 2.4 GPa, and the chips with a 1 μm offset generate a stress of approximately 1.6 GPa at the bottom of the socket chip. Figure 2.27 shows the Scanning electron microscope (SEM) image of the socket chip and plug chip. As Figure 2.27 shows, both chips have nickel thin film remain at the bottom of the interconnector part.

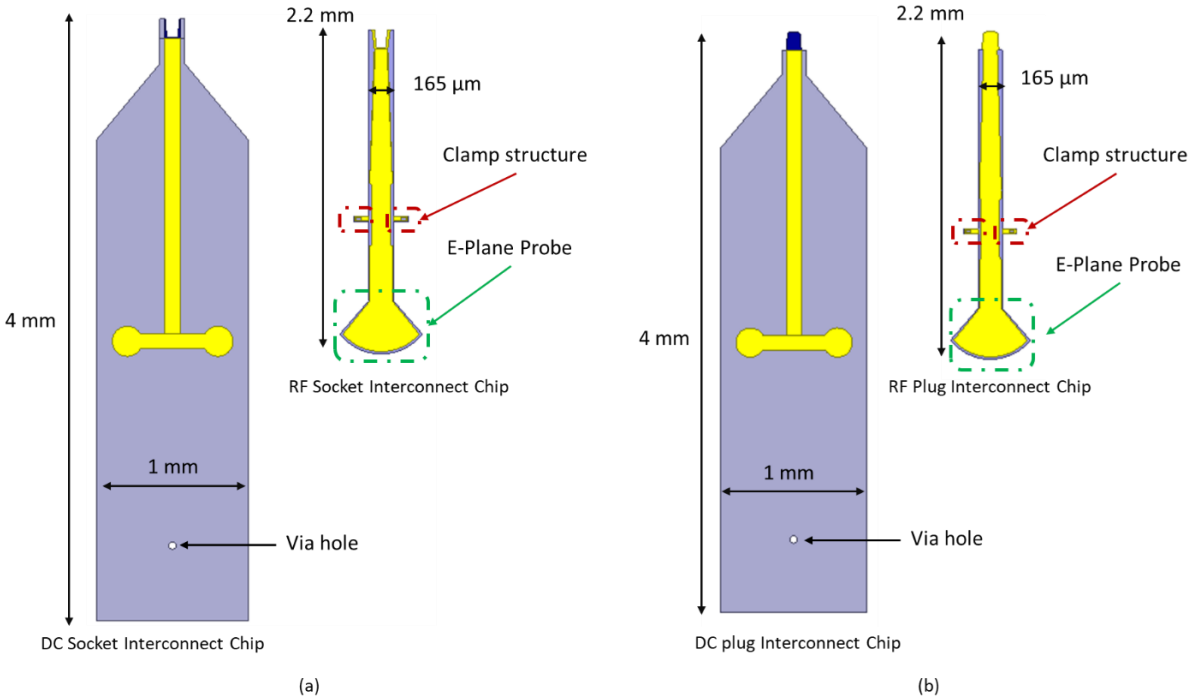


Figure 2.28:Size comparison of DC interconnect chip and RF interconnect chip (a) Socket chip (b) Plug chip

2.9.2 Assembly Force

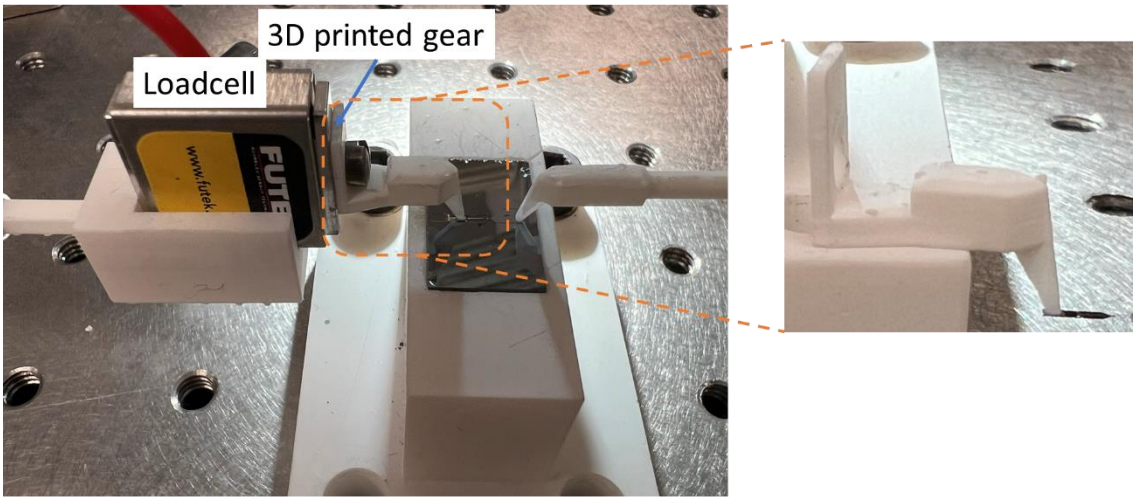


Figure 2.29: (a)Assembly force measurement setup and (b) 3D printed tool for socket chip.

To ensure accurate measurement of the assembly force, a secure connection between the socket chip and the load cell is essential. To achieve this, a 3D-printed tool is utilized to affix the socket chip to the load cell, as depicted in Figure 2.29. A detailed illustration of the 3D-printed tool designed specifically for the socket chip can be found in Figure 2.30.

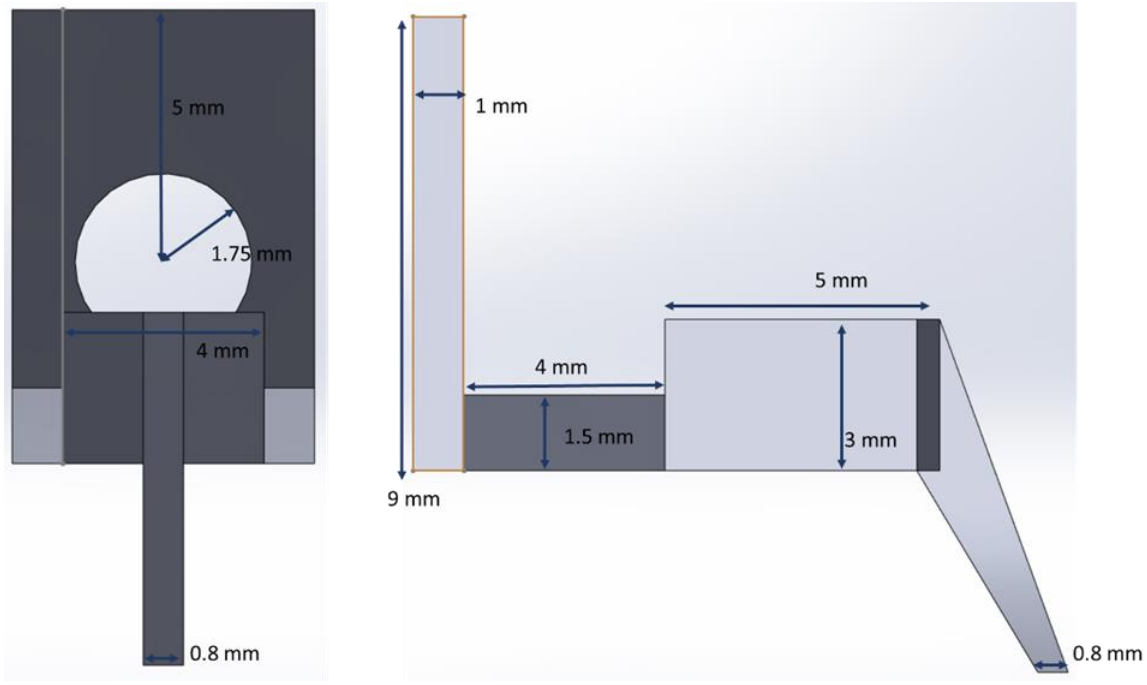


Figure 2.30:3D-printed tool for socket chip.

The 3D-printing machine utilized in the project, specifically the Formlab 3+, employs Rigid 10k as the chosen material. It is worth noting that the Young's modulus of Rigid 10k material, after UV curing, amounts to 10 GPa. As such, the deformation of the 3D-printed tool during the measurement process of the assembly force is regarded as negligible.

The movement of the plug chip was regulated using a micromanipulator, as depicted in Figure 2.31 (a). In this setup, the load cell was held on the left side by the micromanipulator, while the socket chip was linked to the load cell. Another micromanipulator was also linked to the 3D-printed tool and the plug chip on the right side, as shown in Figure 2.31 (b). The plug chip was maneuvered by the micromanipulator using the 3D-printed tool. Further information about the 3D-printed tool used for the plug chip is available in Figure 2.32.

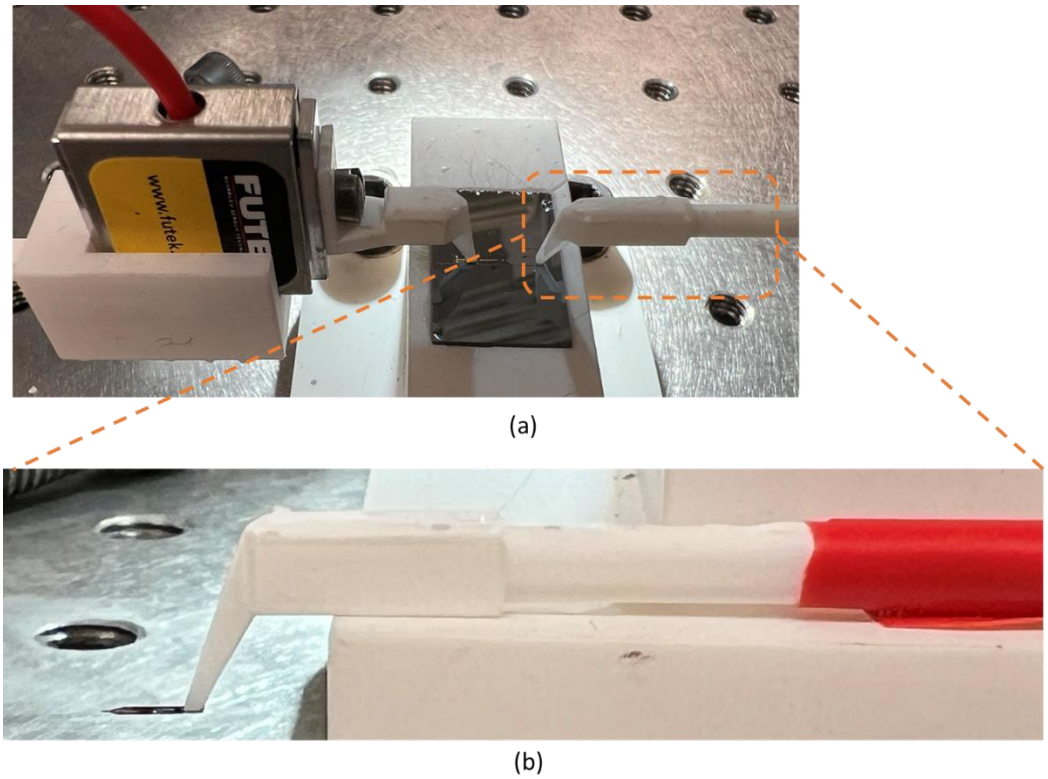


Figure 2.31:(a)Assembly force measurement setup and (b) 3D printed tool for plug chip.

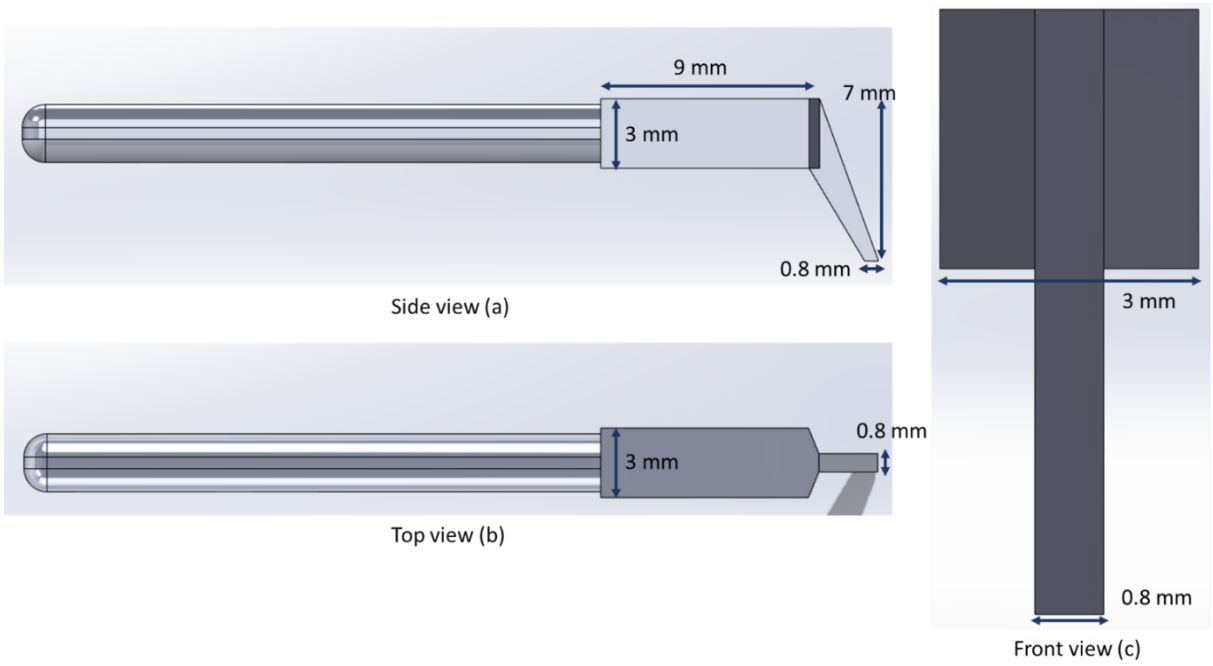


Figure 2.32: 3D-printed tool for plug chip.

The socket chip and plug chip are situated within an alignment wafer that has been specifically etched for DC chips alignment, as illustrated in Figure 2.33. In order to prevent the chips from tilting during the assembly process, a minute section of a transparent quartz wafer is utilized to cover the interconnect part.

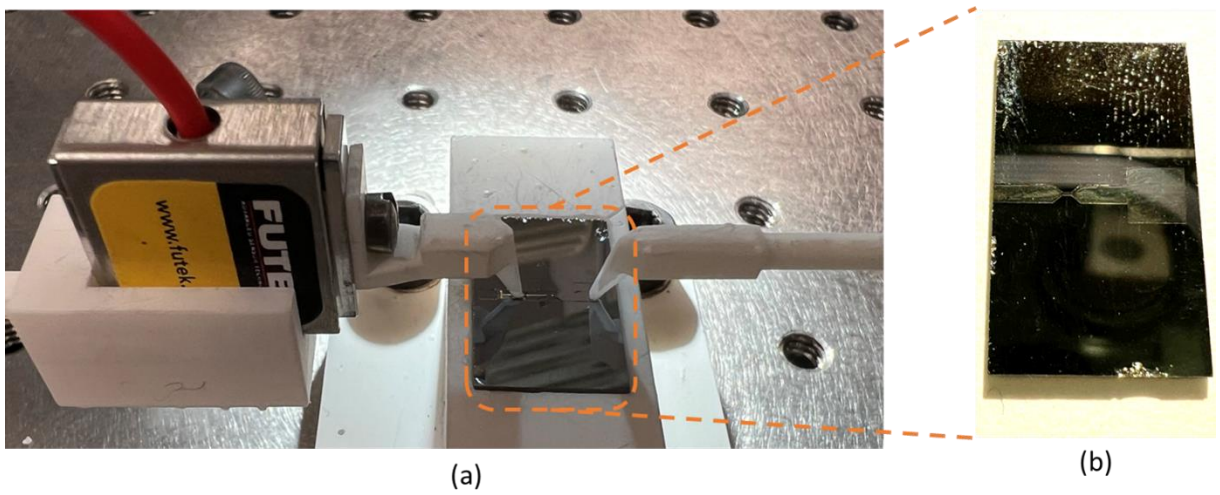


Figure 2.33:(a)Assembly force measurement setup and (b) alignment wafer.

Subsequently, a precise amount of optical adhesive NOA 83H was applied to both 3D-printed tools for the plug chip and socket chip using a sharp needle. It is crucial to carefully control the amount of optical

adhesive applied to the printed tool, as an excessive amount can cause the glue to leak into the alignment channel and negatively affect the measurement results. Conversely, insufficient adhesive may not be able to securely hold the chip during measurement. The last step is to expose the chips under UV light to cure the optical adhesive on the chips.

During the measurement, the plug chip is carefully positioned from the right-hand side towards the socket chip, and the resulting interconnect is observed through a microscope. The alignment wafer, depicted in Figure 2.33 (b), displays the 20 µm deep etched channel used in the measurement process.

2.9.3 Three Micrometer Offset Chip Assembly Force Measurement

In the design of tapered interconnect chips, we introduced three variations in deformation to establish the optimal stress threshold for the interconnect. The deformation of the interconnect is quantified by the Δy metric outlined in Section 2.8.4. The three interconnect designs under consideration are as follows: 3 µm offset chip, 2 µm offset chip, and 1 µm offset chip.

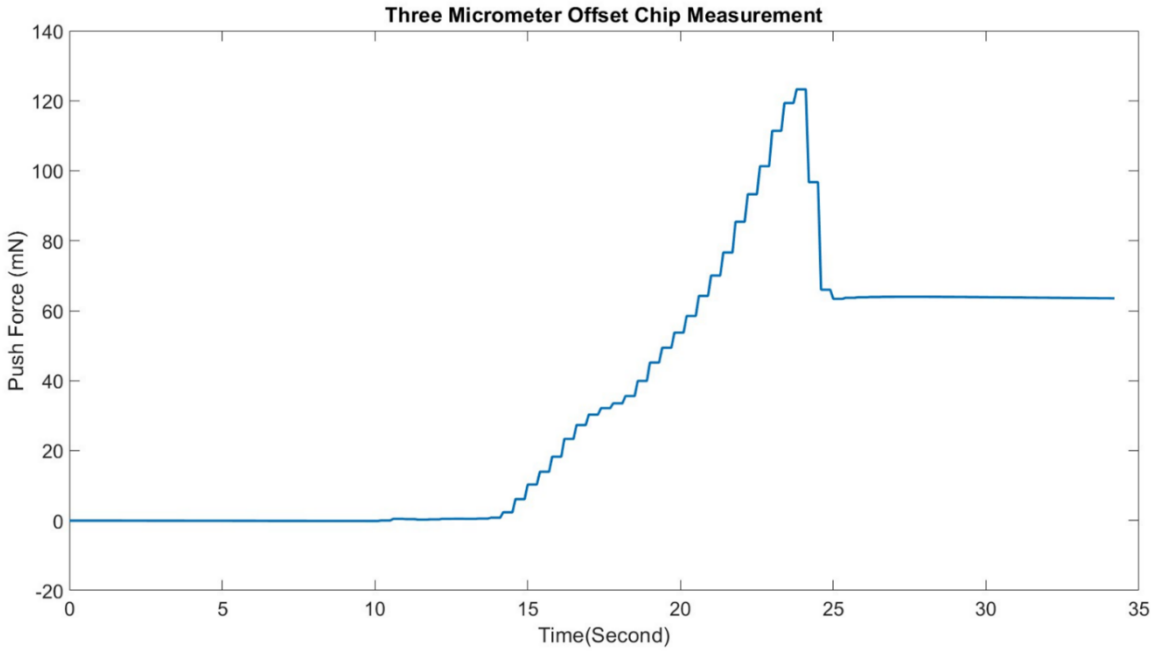


Figure 2.34:3 µm offset chip assembly force measurement.

For the 3 µm offset chip, we repeatly tested for many time but the assembly force is higher than 100 mN. The assembly went up to 120 mN then broke the socket chip arms. The contact force plot show in Figure 2.34. We repeatly tried several times but all the 3 µm offset chips broke the socket chip arms.

2.9.4 Two Micrometer Offset Chip Assembly Force Measurement

To evaluate the assembly force of a 2 μm offset chip, we conducted ten repeated measurements. The first contact force was approximately 90 mN, which we attribute to the nickel thin film that resulted from the silicon on insulator (SOI) wafer fabrication process. The SEM image of the nickel thin film is depicted in Figure 2.27. During the first assembly of the two chips, there was a high probability of the nickel thin film impeding the interconnector component. As Figure 2.35 shows, the highest recorded assembly force was approximately 90 mN, while the lowest was approximately 77 mN. The majority of measurements fell within the range of 75 mN to 85 mN. The average ten times assembly force is 83.44 mN and the standard deviation is 4.02 mN.

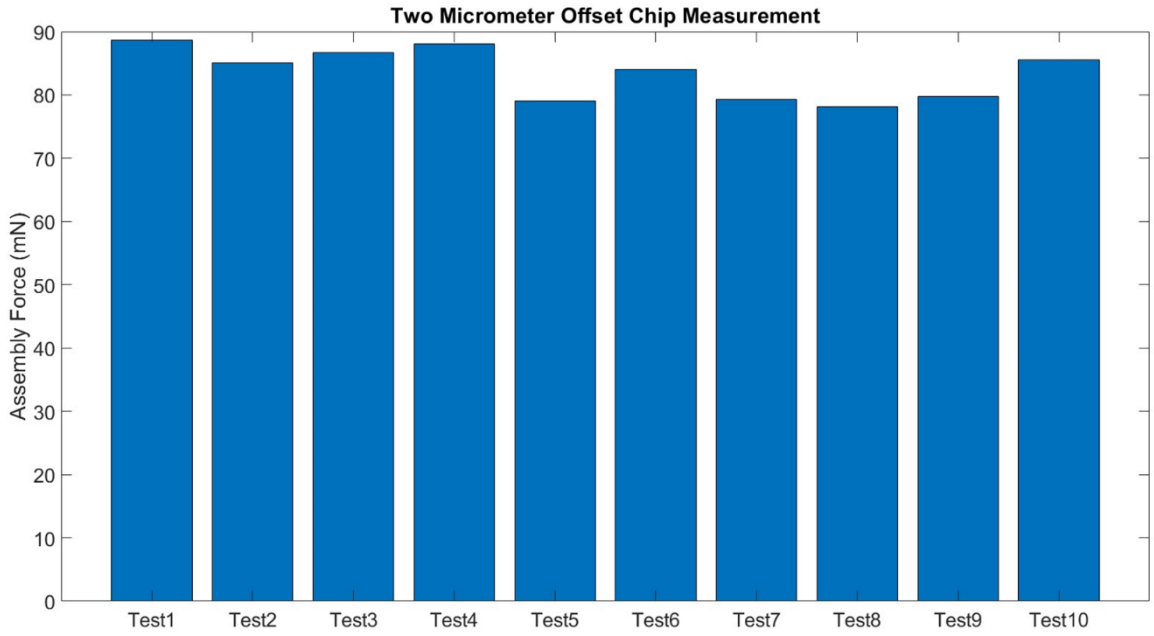


Figure 2.35:2 um offset chip assembly force measure results.

2.9.5 One Micrometer Offset chip Aseembly Force Measurement

In addition to the disassembly force measurements, we conducted ten repeated measurements of the assembly force for a 1 μm offset chip. The first contact force was found to be approximately 80 mN, which is lower than that observed for the nickel thin film caused by the SOI wafer fabrication process.As Figure 2.36 shows, the highest recorded assembly force was approximately 80 mN, while the lowest was

approximately 60 mN. The majority of measurements fell between the range of 60 mN and 70 mN. The average assembly force for ten times assembly is 70.8 mN and the standard deviation is 4.88 mN.

2.9.6 Contact Resistance and Disassembly Force

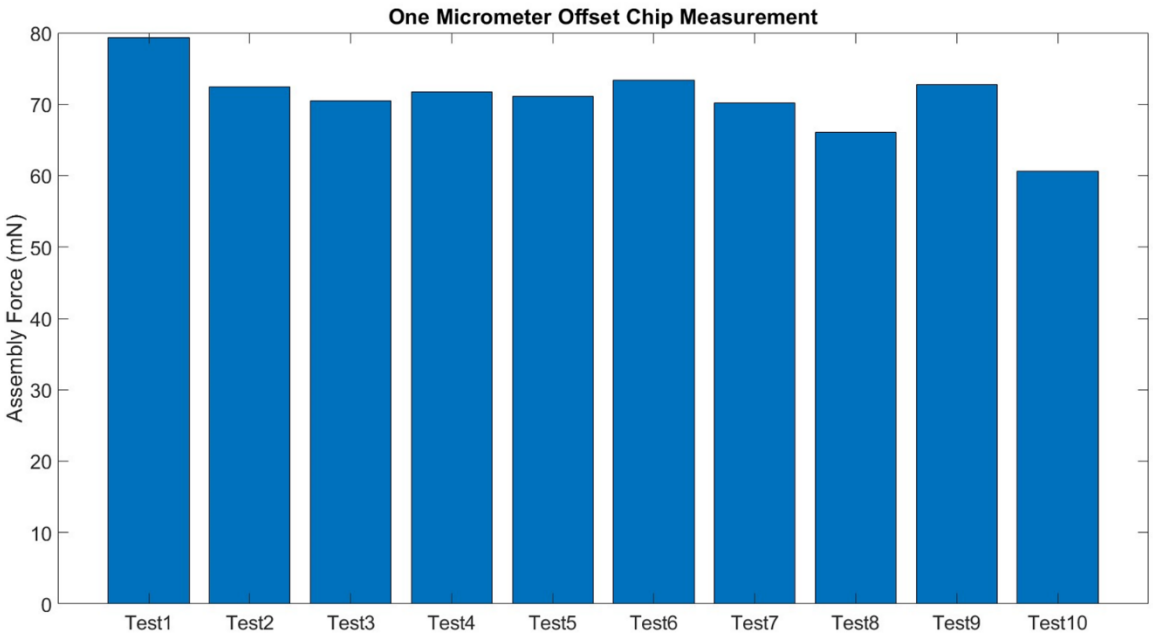


Figure 2.36:1um offset chip assembly force measure results.

The measurement of disassembly force is distinguished from that of assembly force, due in part to a notable factor: the removal of push force on the plug chip after its assembly with the socket chip. If push force persists on the plug chip, the spring within the load cell cannot revert to its original position, which in turn adversely affects the disassembly force measurement. To address this, a 3D-printed tool with needle adhesive was used for the plug chip in the disassembly force measurement. The needle must land with precision and gentleness within the via hole on the plug chip, as Figure 2.37 shows. The measurement setup is presented in Figure 2.37. The socket chip firmly glued to a 3D-printed tool and screwed onto the loadcell. A significant finding during the measurement process was that the needle landing on the plug chip must be brief to prevent bending of the needle.

To measure the contact resistance, we apply four point measurements to eliminate the resistance error from the needle probe. The four point measurements setup also shows in Figure 2.38.

The experimental procedure involved landing the needle inside the via hole followed by pushing the plug chip toward the socket chip. After the assembly of the plug and socket chips, the needle was lifted from the via hole to release the push force on the plug chip. Simultaneously, the spring within the load cell was freed, and returned to its original position. Subsequently, four Direct current (DC) needle probes were applied, and with gentle force, landed on the gold pads section, as illustrated in Figure 2.38. The contact resistance of the interconnects was then measured.

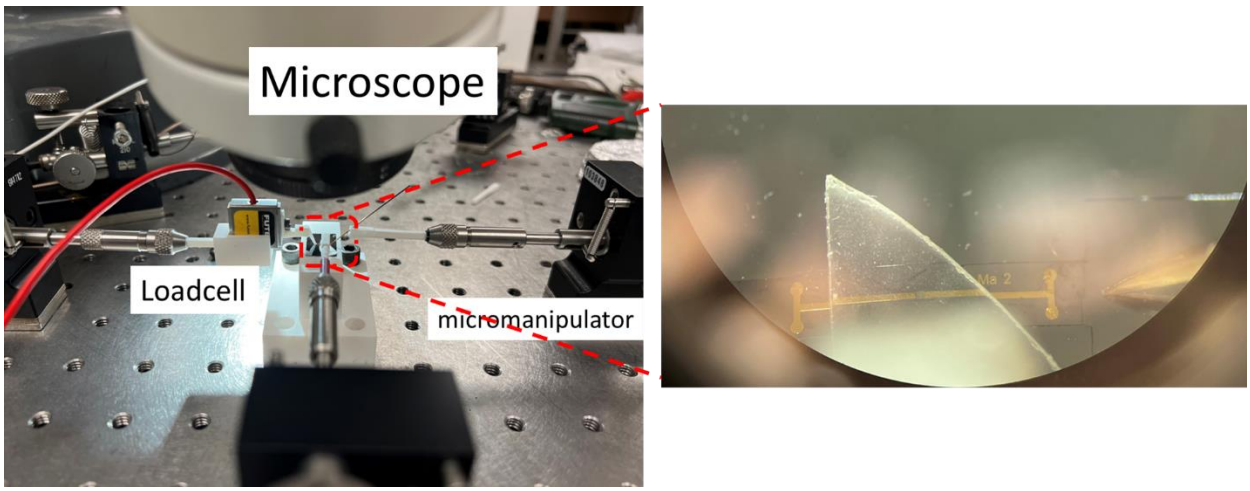


Figure 2.37:Disassembly full measurement.

It is essential to exercise caution when landing the DC needles on the chips to prevent any mishaps. Landing the needle too deep can potentially push the plug or socket chips forward and increase the likelihood of their breakage. Conversely, inadequate placement of the needle on the chips can lead to no contact between the needle and the pad.

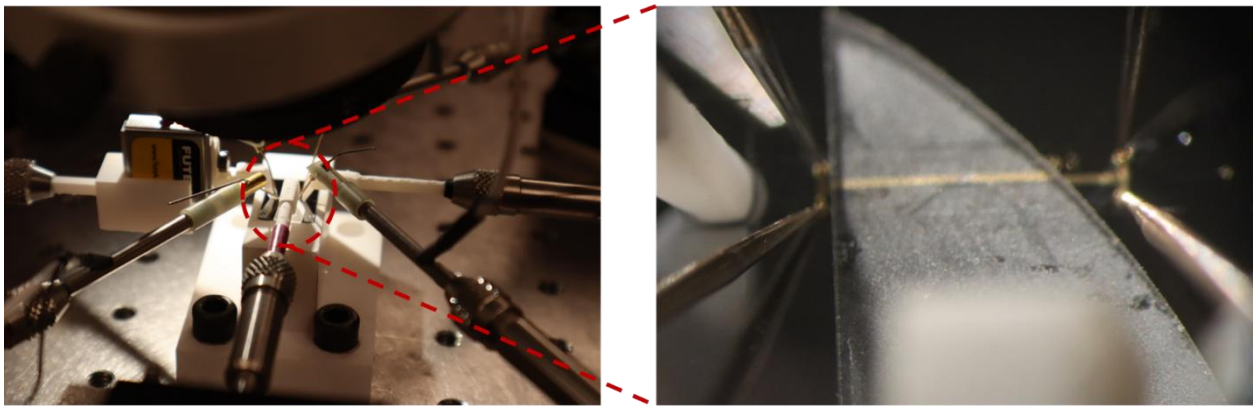


Figure 2.38:Contact resistance and pull test setup.

In our experimentation of contact resistance and disassembly force measurement, we employed the two-micrometer offset design. The resulting assembly and disassembly force were observed to be in the range of 70 mN to 80 mN and 65 mN to 75 mN, respectively. The average assembly force is 76.63 mN and the standard deviation is 6.43 mN. The average disassembly force is 74.32 mN and the standard deviation is 3.17 mN.

During the process, we noted that upon lifting the needle, a slight pulling of the plug chip occurred. This phenomenon can be attributed to the needle's adherence to the metallic material surrounding the via hole. Prior to conducting the disassembly force measurement, a four-point measurement was carried out as depicted in Figure 2.37. At this point, the plug chip and socket chip were assembled without any additional push force applied to the plug chip. The rationale for measuring the contact resistance without any push force was to obtain the most precise measurement, as the addition of push force could potentially result in a decrease in the contact resistance measurement.

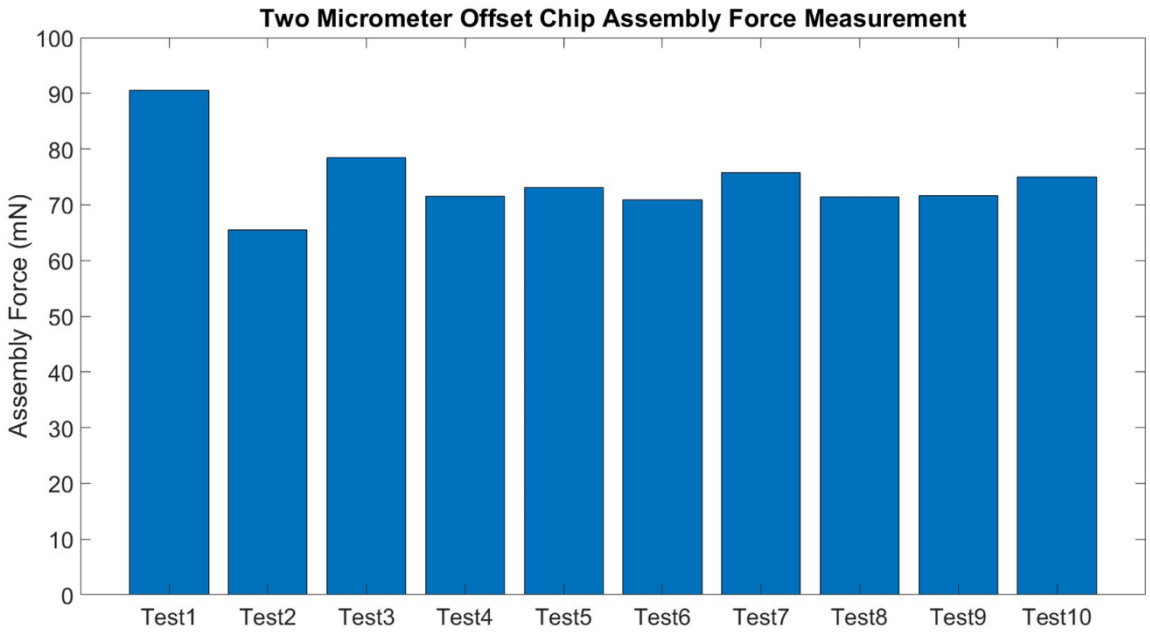


Figure 2.39:Aseembly Force measurement for 2 µm offset.

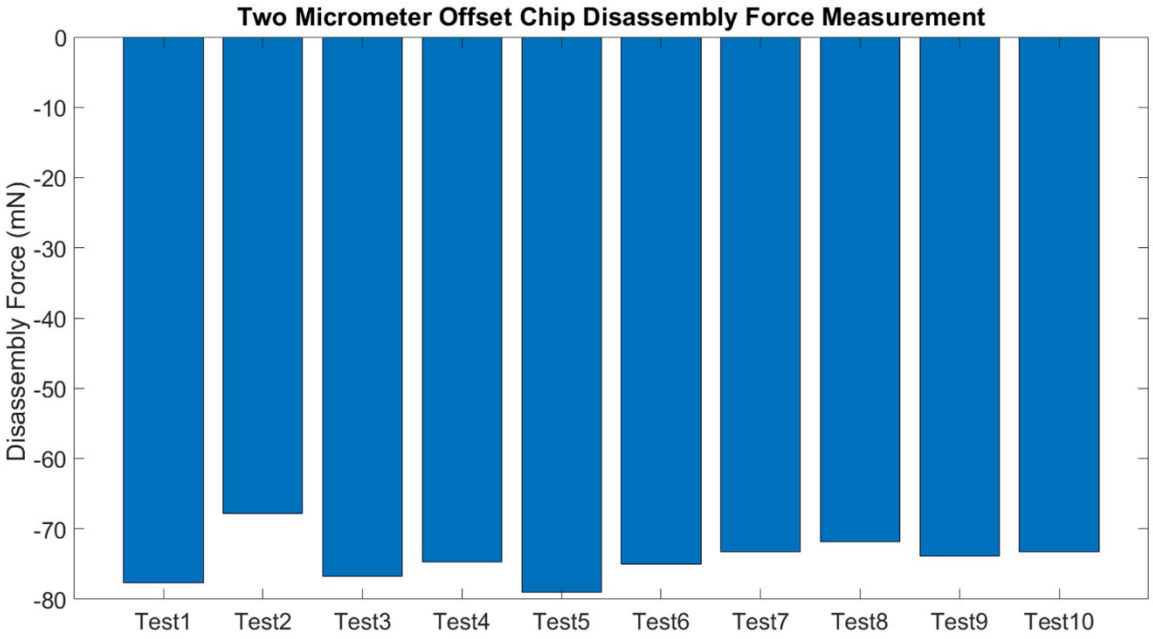
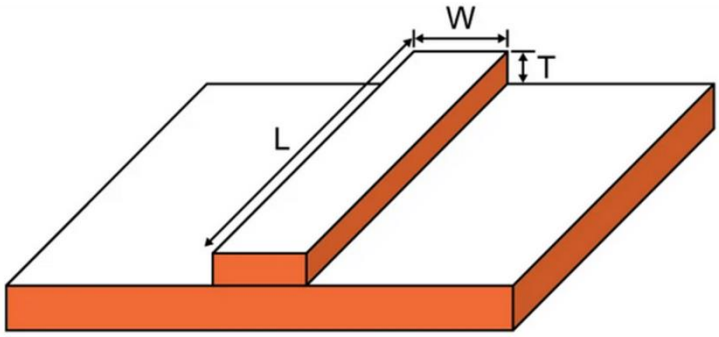


Figure 2.40: Disassembly Force measurement for 2 µm offset.

We conducted measurements of the contact resistance during the first, fifth, and tenth assembly of the plug and socket chips. The recorded contact resistances were 2.8 Ω, 2.9 Ω, and 2.9 Ω, respectively. In recent measurements, the contact resistance remained within the range of 2.8 to 3.2 Ω. However, in cases where the socket chip breaks, the contact resistance measurement increases to 5 Ω or higher.

The static friction coefficient of the nickel coating surface was estimated using the assembly and disassembly forces measured in our study. Based on the formula described in section 2.8.3, the calculated static friction coefficient was determined to be 1.05. Using this coefficient, the disassembly force was estimated to be 140 mN. Therefore, based on our measured results of disassembly force, it is likely that the effective contact area along the socket chip beam is between 60 to 80 µm in length. In this case, the disassembly force is between 70 to 98 mN.

To eliminate the conducting resistance of the gold transmission line, we also measure resistance of the gold through line as Figure 2.42 show. The gold transmission line under same length have 2.2 Ω resistance which fit with our estimation. The formula we apply to calculate the trace resistance shows in Figure 2.41.



ρ_{gold}	$1 \cdot 10^{-7}(\Omega \cdot m)$
L	4 (mm)
T	2 (μm)
W	100 (μm)
$R = \rho_{gold}\frac{L}{T \cdot W}$=2	

Figure 2.42:Gold trace resistance calculation.

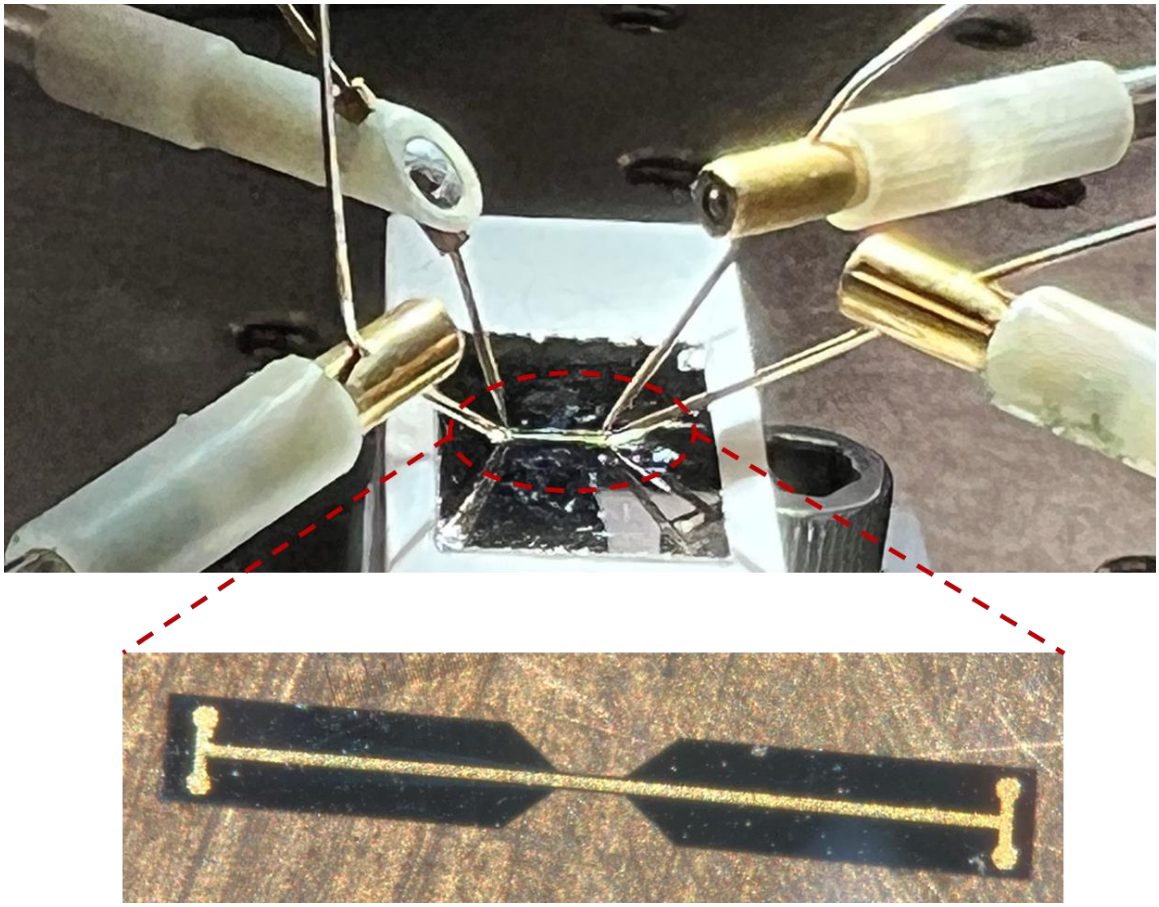


Figure 2.41:Four point measurement of gold trace resistance.

The calculation results match well with the measured result. The gold resistance, trace thickness, width and length shows in Figure 2.41.

Based on the formula provided, the additional resistance ranging from 0.8 to 1.2 Ω caused by the nickel interface has been found to result in an approximate increase of 0.1 dB in insertion loss. These findings are consistent with the measured insertion loss results obtained from both the interconnect chip and the through chip.

$$\Gamma = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} = \frac{R_{Nickel}}{R_{Nickel} + 2Z_0}$$

$$\tau = 1 + \Gamma$$

$$V_1 = \tau V_0$$

$$V_2 = V_1 \frac{Z_0}{Z_0 + R_{Nickel}} = V_0 \tau \frac{Z_0}{Z_0 + R_{Nickel}}$$

A calculation based on the measured nickel resistance of approximately 1 Ω, with a Z0 of 50 Ω, reveals an estimated insertion loss of approximately 0.1 dB.

2.9.7 Repeatibility

To determine the interconnect lifetime, a series of tests were conducted on the prototype interconnects. During the assembly force and disassembly force measurement, we exerted pressure on the plug chip until the tip of the plug interconnector made contact with the bottom of the socket interconnector. While conducting these tests, we observed that many socket chips broke after fewer than ten tests. Thus, we attempted to strike a balance between the assembly force and contact resistance and determine the optimal assembly force for the interconnects. In other words, we aimed to avoid pushing the interconnects to their limits to increase their lifespan.

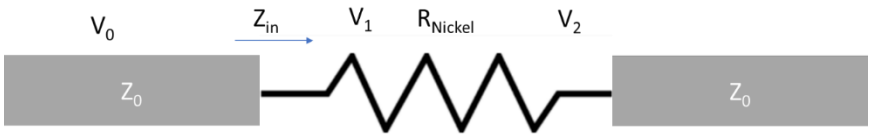


Figure 2.43:Nicke interface resistance and insertion loss model.

The study conducted an initial measurement of the lifetime of the 2 μm offset chip, the results of which are presented in Figure 2.44 and 2.45. The plug chip was fully assembled to the socket chip, with the plug chip head edge in contact with the bottom of the socket chip under the microscope, while the assembly force ranged from 70 mN to 110 mN. The majority of the measured assembly force remained between 80 mN and 90 mN throughout the lifetime measurement. Nevertheless, after 42 cycles of measurement, the first lifetime measurement socket chip failed, as depicted in Figure 2.45. Specifically, both arms of the socket chip were broken. A possible explanation for this failure is that the assembly force increased to 110 mN during the 42nd cycle, thereby causing the socket chip's beams to break. The average assembly force for 42 times is 85.9 mN and the standard deviation is 10.81 mN.

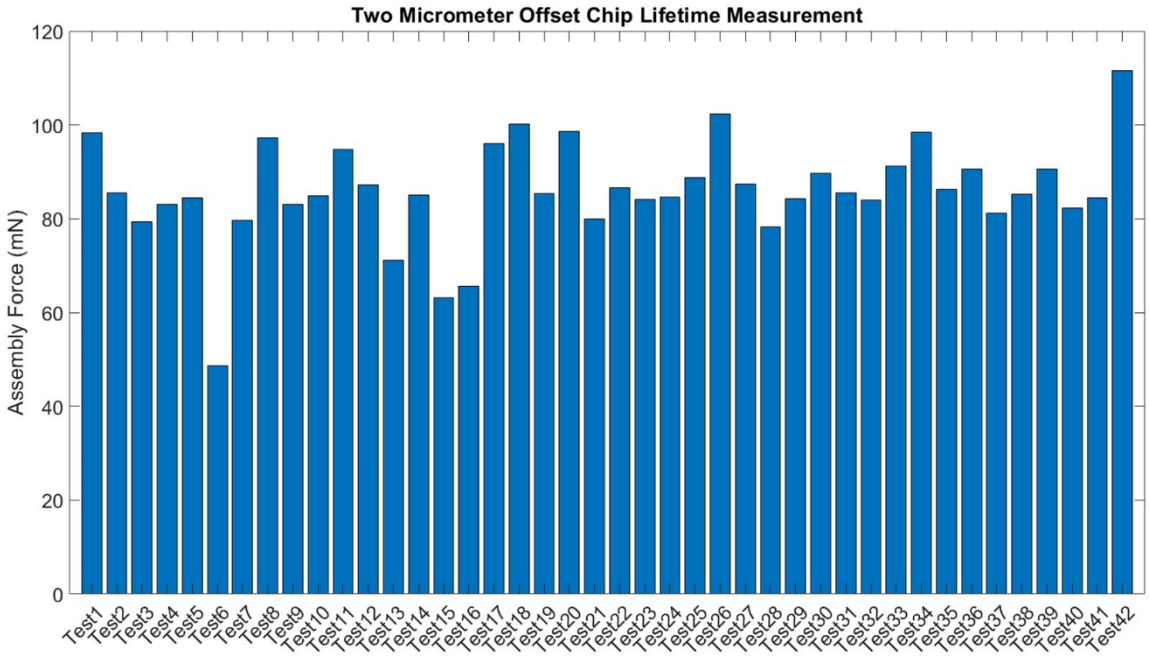


Figure 2.44:2 μm offset chip lifetime measurement 1.

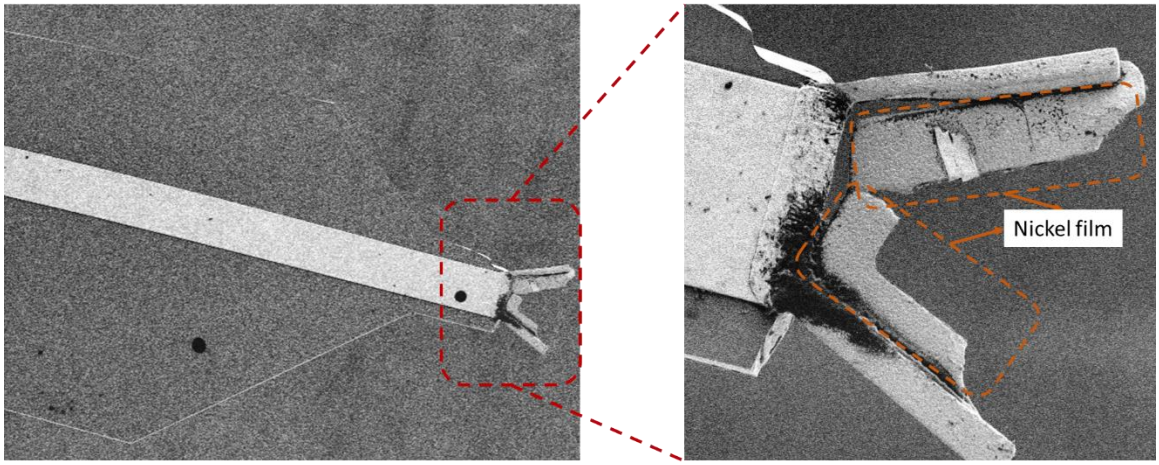


Figure 2.46:SEM pictures of broken socket chips (Test1).

The second lifetime test of 2 μm offset chip measurement shows in Figure 2.46 and 2.47. The second lifetime assembly force ranged from 70 to 100 mN and it broken at 38 times. Figure 2.47 shows the image of the broken socket chip after 38 times of assembly. The average assembly force is 83.03 mN and the standard deviation is 7.11 mN.

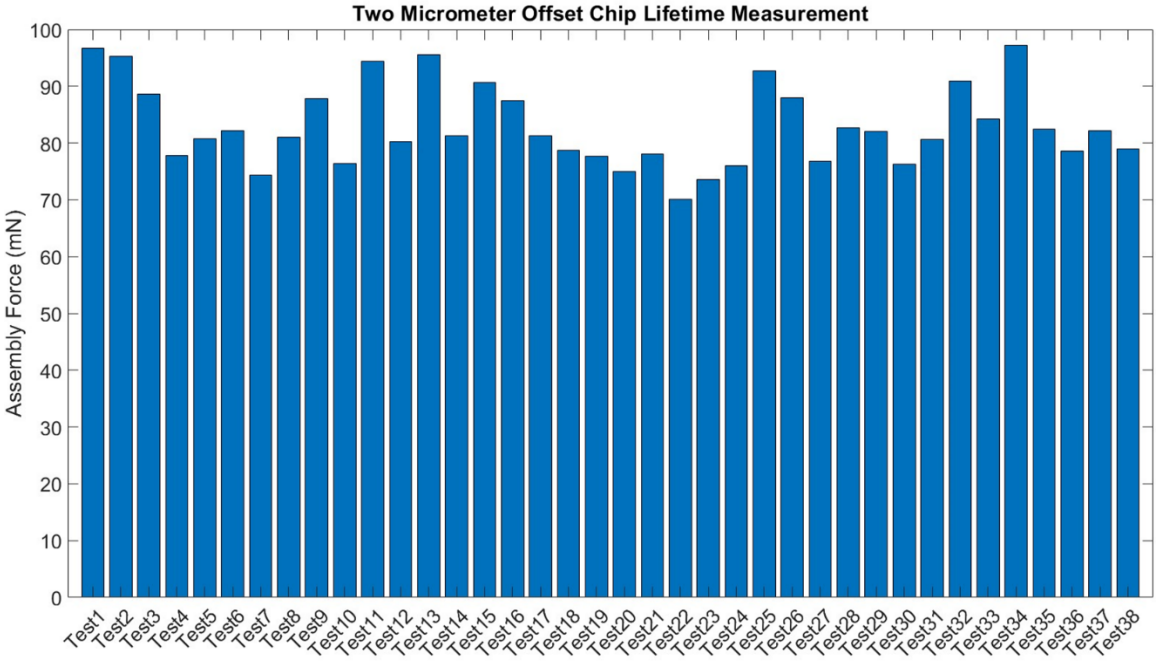


Figure 2.45:Second lifetime test of 2 μm offset chip measurement.

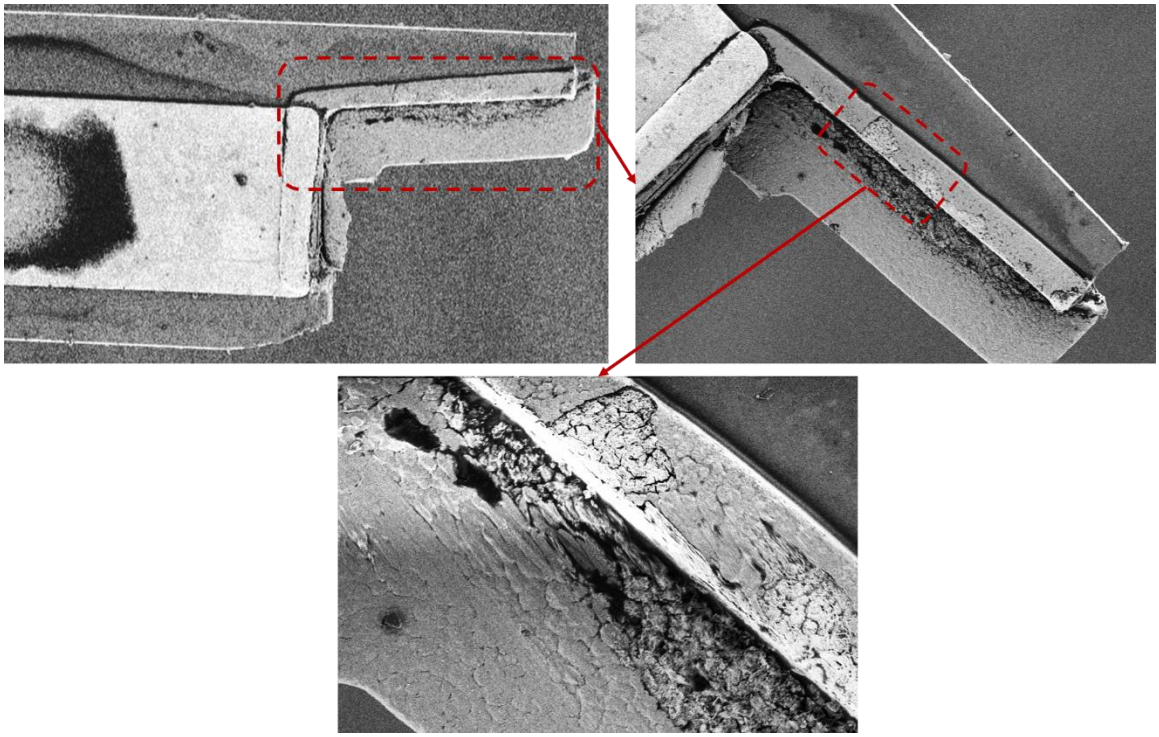


Figure 2.47:SEM pictures of broken socket chips (Test2).

We measured the two micrometer offset under 90, 80, 70, 60, 50 and 40 mN. The contact resistance under different resistance shows in Figure 2.48. As we can see, the 2 um chip under 50 mN is merely touched which means the measured contact resistance isn't accurate. Also, the 1 um chip under 40 mN shows resistance higher than 10 Ω.

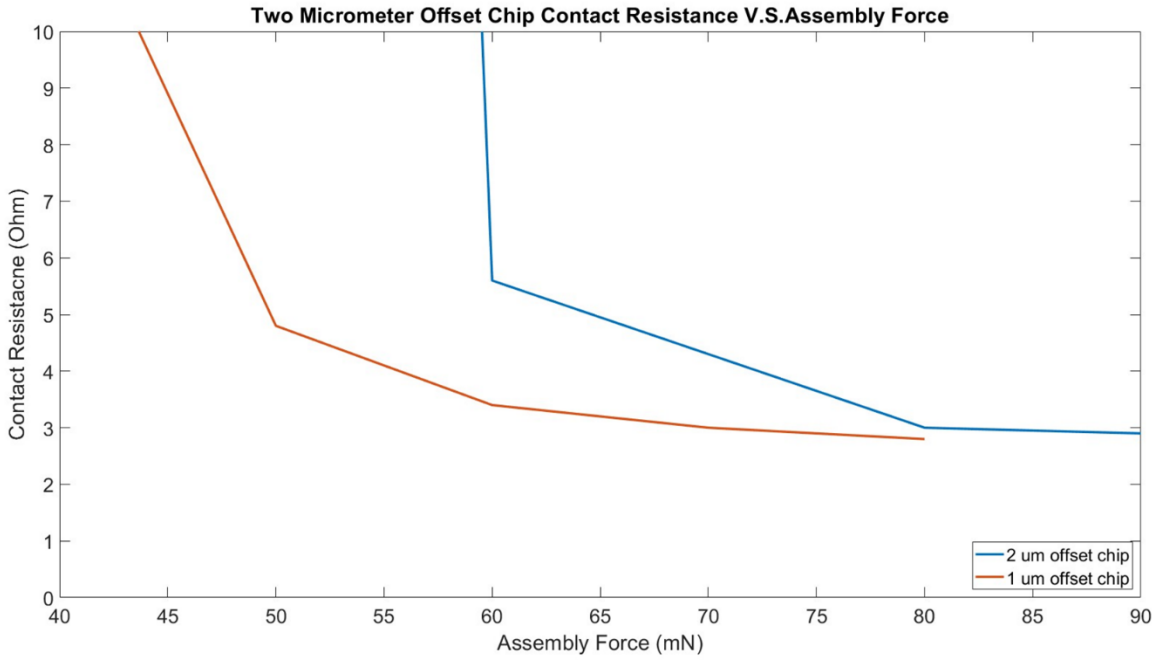


Figure 2.48:contact resistance versus assembly force.

The findings from Figure 2.48 reveal that elevating the contact resistance beyond 70 mN could lead to a decline in contact resistance, resulting in a value as low as 3 Ω for a 2 μm offset chip. Consequently, it is not imperative to apply assembly forces as high as 90 mN when assessing the lifetime of the 2 μm offset chip. Rather, a tradeoff exists between the potential for socket chip breakage and contact resistance in this measurement. As such, during the lifetime measurement of the 2 μm offset chip, the assembly force was regulated to below 80 mN. The lifetime data for the 2 μm offset chip is depicted in Figures 2.50 and 2.51.

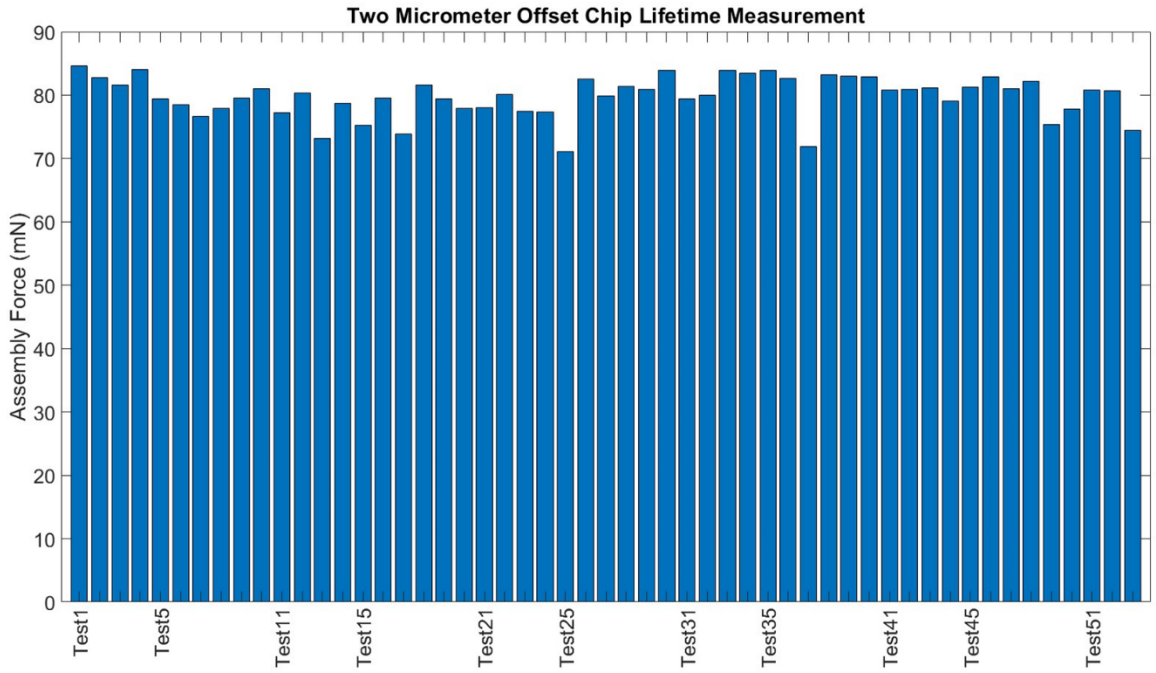


Figure 2.49:Third lifetime test of 2 µm offset chip measurement.

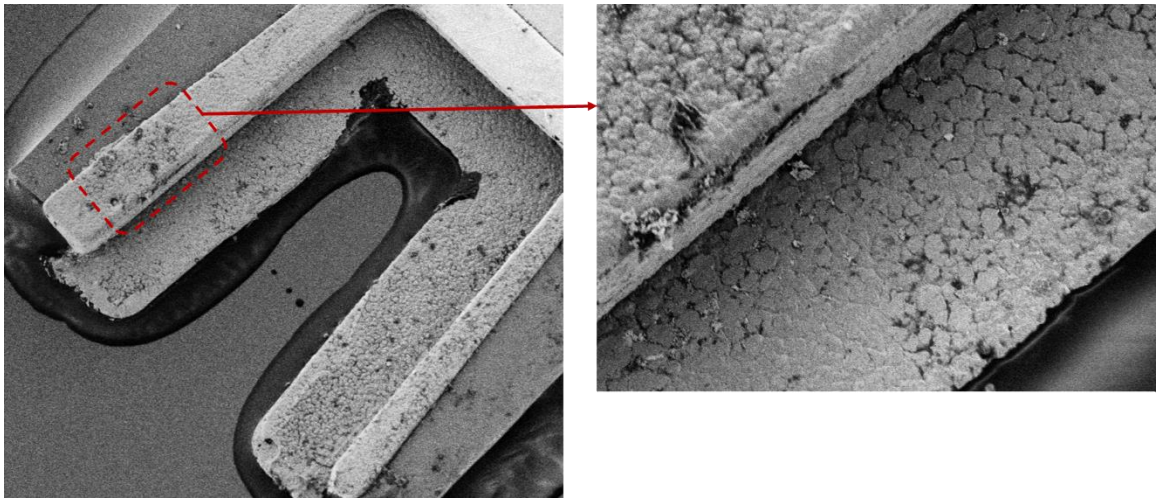


Figure 2.50:SEM pictures of broken socket chips (Test3).

The experiment involved the precise control of assembly force, limited to 80 mN, resulting in a lifespan of the 2 µm offset chip exceeding 50 cycles. To capture SEM images of the socket chip, the test was paused at the 53rd cycle. The dark area in Figure 2.50 near the nickel film being attributed to the L-grease utilized to secure the chip onto the wafer. This method was applied to ensure that the SEM images were taken with high quality, free from electron-related distortions.

For 1 μm offset chip, we control the assembly force under 70 mN. The life time for the 1 μm offset chip shows in Figure 2.51 and Figure 2.52.

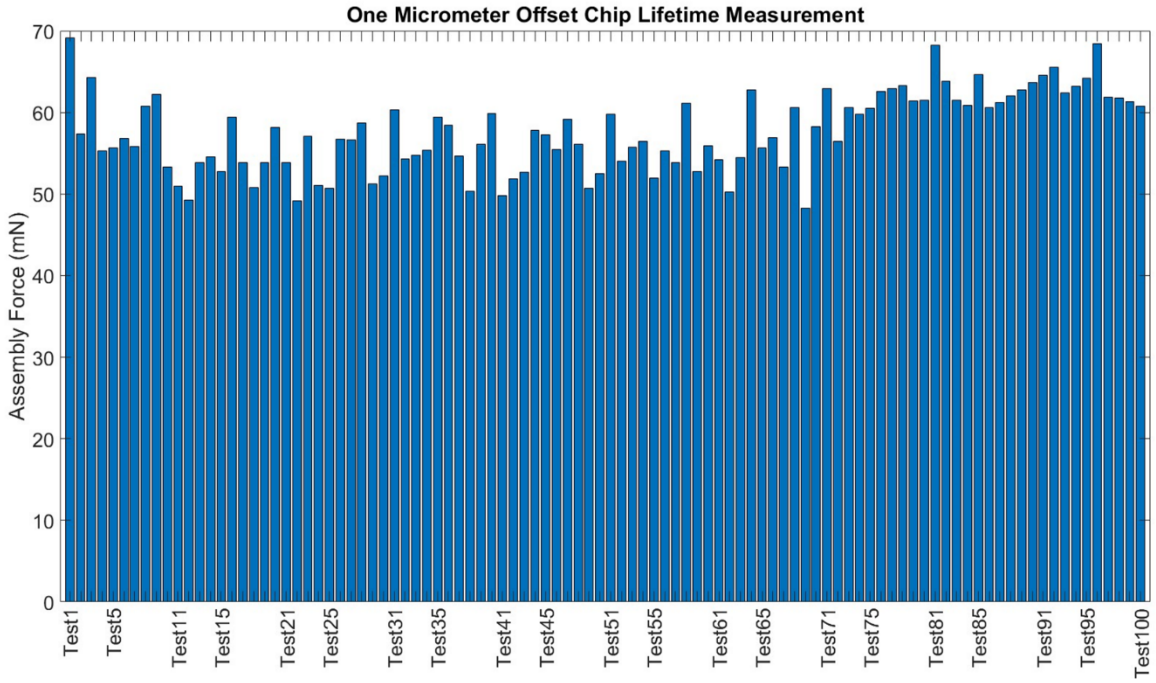


Figure 2.51:Lifetime test of 1 μm offset chip measurement

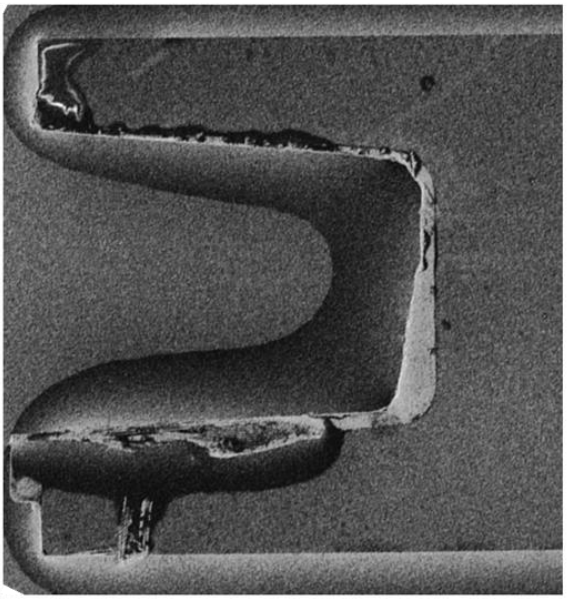


Figure 2.52:SEM pictures of 1 μm offset socket chips after 100 times of lifetime measurement.

To achieve a higher accuracy in the measurement of the 1 μm offset chip, we took steps to eliminate the effect of the nickel film on the socket chip connector, as depicted in Figure 2.50. Specifically, we employed a needle to carefully compress the nickel film and make it as thin as possible, as shown in Figure 2.52.

The average assembly force for 2 μm offset chip over 53 times is 79.79 mN and the standard deviation is 3.2 mN. The average assembly force for 1 μm offset chip over 100 times is 57.59 mN and the standard deviation is 4.77 mN.

The 1 μm offset chip was subjected to assembly forces ranging from 60 to 70 mN, and the resulting socket chip after 100 cycles of assembly is illustrated in Figure 2.51. As evident from Figures 2.51 and 2.52, the 1 μm offset chip demonstrated a remarkable ability to withstand repeated assembly and disassembly, exceeding 100 cycles.

2.10 Mechanical Design and Measurement Summary

In the preceding section, we conducted a comprehensive analysis of the stress and deformation of the socket chip beam. Our initial mechanical design featured a uniform beam and small contact area, aimed at maximizing the contact force. This design resulted in stress on the socket chip beam exceeding 3 GPa.

However, based on our experiences with prototype interconnects and assembly failures, we opted to modify the design by changing the interconnector shape to a non-prismatic beam. This alteration resulted in significantly lower stress levels, with the highest stress on the non-prismatic beam structures remaining below 3.1 GPa.

We measured the assembly force required for the 2 μm offset interconnect assembly to range from 80 to 90 mN, while for the 1 μm offset interconnect, it ranged from 70 mN to 80 mN. The contact resistance of the interconnects chips ranged from 2.8 to 3.3 Ω. Additionally, the 2 μm offset interconnect exhibited a lifetime exceeding 50 times, while the 1 μm offset interconnect's lifetime exceeded 100 times.

3 Electrical Design of Detachable Chip-to-chip Interconnect

3.1 Quasi-Coaxial Transmission Line Design

Transmission line is critical to transmit energy from rectangular waveguide to silicon interconnect chips. In many different type of transmission line, the Mircrostrip line is one of the most popular and widely used. Figure 3.1 below show the geometry of a Microstrip line.

According to textbook: Microwave Engineering [47], the effective dielectric (ε_e) constant can be represented by following equation.

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12d/w}}$$

And the phase velocity v_p and propagation constant is as following equations shows. And the c is speed of light.

$$v_p = \frac{c}{\sqrt{\varepsilon_e}}$$

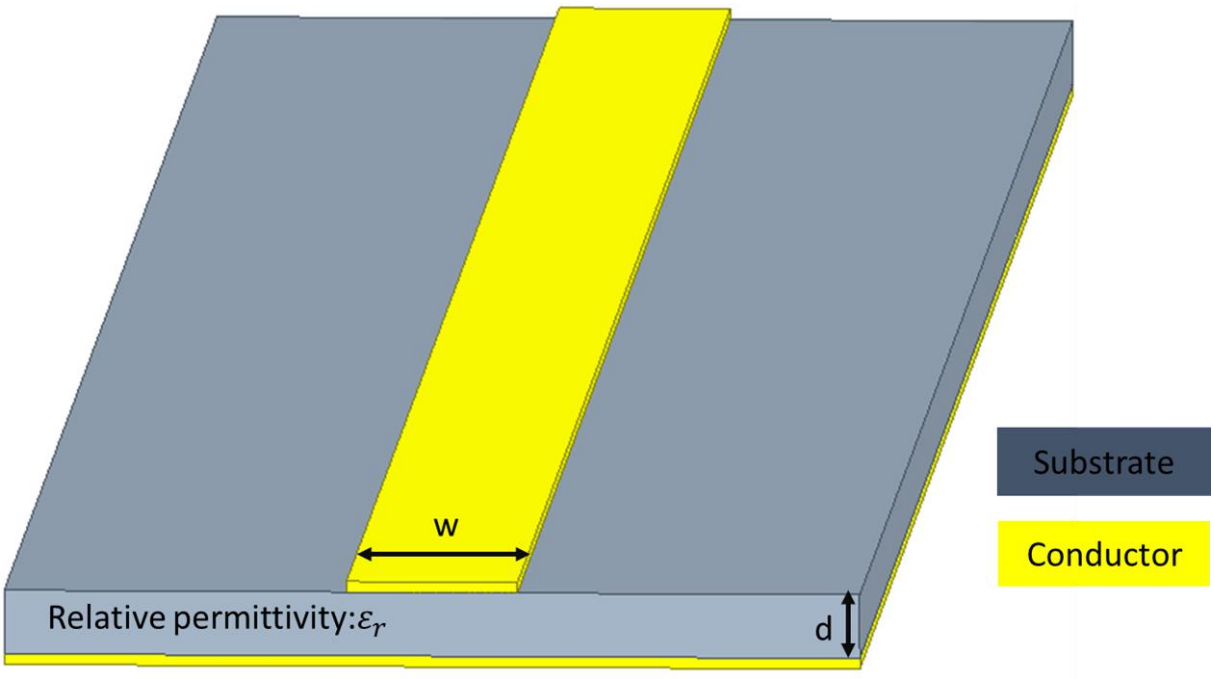


Figure 3.1: Geometry of a Microstrip line

$$\beta = k_0\sqrt{\varepsilon_e}$$

As stated by reference [47], the surface resistivity of the conductor (R_s), characteristic impedance (Z_0), and conductor loss of the Microstrip line (α_c) can be computed at a specific frequency. In our present design, gold is utilized as the conductor material for the transmission line.

$$R_s = \sqrt{\frac{\omega\mu_0}{2\sigma}}$$

$$Z_0 = \frac{120\pi}{\sqrt{\varepsilon_e}\left[{}^{w}/_{d} + 1.393 + 0.667\ln({}^{w}/_{d} + 1.444)\right]}$$

$$\alpha_c = \frac{R_s}{Z_0 W}$$

$$\alpha_d = \frac{k_0\varepsilon_r(\varepsilon_e - 1)tan\delta}{2\sqrt{\varepsilon_e}(\varepsilon_r - 1)}$$

Within our design, the width of the conductor (w) is 135 μm, while the thickness of the silicon substrate (d) amounts to 15 μm. The relative permittivity of silicon (ε_r) stands at 11.9, and the conductivity of the gold conductor (σ) registers as 1×10^7 S/m. Application of the above formulas yields the ensuing outcomes at a frequency of 180 GHz [48]. The loss tanget of the silicon is 1.2×10^{-5} at 300 GHz [49].

Table 3.1:Calculation results of microstrip line without waveguide housing

Quantity	Calculated Results
ε_e	10.02
v_p	9.478×10^7 m/s
β	1.193×10^4 rad/m
$tan\delta$	1.2×10^{-5}
R_s	0.2666 Ω
Z_0	9.961 Ω
α_d	0.165 dB/mm
α_c	0.2 dB/mm

However, in our design, the Microstrip line is placed inside the metal RF channel which the conductive loss is much lower than the Microstrip line without the waveguide cover. The losses of coaxial line inside the rectangular housing can be lower down to 0.04 dB/mm [50].

In the rectangular waveguide, the mode supported is TE_{10} mode. Therefore, the design rule for design the quasi-coaxial line in waveguide is to eliminate all the higher order mode in the operation frequency band

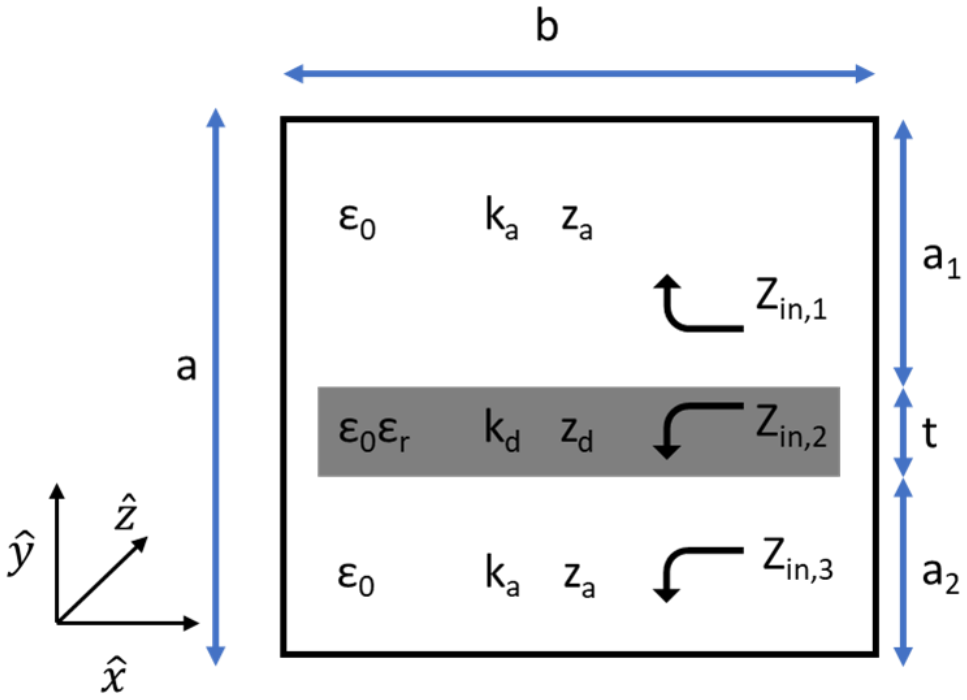


Figure 3.2:Cross section view and transmission line model of coaxial line channel.

which is from 140 GHz to 220 GHz. In this work, we applied transverse resonance method to determine the cutoff frequency.

According to the transverse resonance method, the field in the rectangular waveguide will be standing wave at cutoff frequency. The cross section view of the waveguide channel shows in Figure 3.2. According to the transverse resonance method, the input impedance is equal to zero, which we can derive following equation.

$$Z_{in1} + Z_{in2} = 0$$

In this work, we must make sure that TE_{01}^{y} is the lowest mode. According to the boundary conditions, the propagation constant of the TE_{0n}^{y} must have impedance match along the Z-X plane.

$$\beta = \beta_a = \beta_d$$

$$\beta_a = \sqrt{k_0^2 - k_{y,a}^2}$$

$$\beta_d = \sqrt{k_d^2 - k_{y,d}^2}$$

$$k_0 = \omega\sqrt{\varepsilon_0\mu_0}\ ;\ k_d = k_0\sqrt{\varepsilon_r}$$

At cutoff frequency, the propagation constant is zero.

$$\beta = k_0^2 - k_{y,a}^2 = k_d^2 - k_{y,d}^2 = \varepsilon_r k_0^2 - k_{y,d}^2 = 0$$

$$\rightarrow k_{y,a} = k_0;\ k_{y,d} = k_0\sqrt{\varepsilon_r}$$

Based on above derivation, we can calculate the impedance of dielectric and air part.

$$Z_a = \frac{k_0\mu_0}{k_{y,a}}\ ;\ Z_d = \frac{k_0\mu_0}{k_{y,d}}$$

$$Z_{in,3} = jz_a tan[k_0(a_2)]$$

$$Z_{in,2} = Z_d \frac{Z_{in,3} + jZ_d \tan\,(k_{y,d}t)}{Z_d + jZ_{in,3} \tan\,(k_{y,d}t)}$$

$$Z_{in,1} = jz_a tan[k_0(a_1)]$$

Because $Z_{in1} + Z_{in2} = 0$

$$\rightarrow jz_a tan[k_0(a_1)] + Z_d \frac{Z_{in,3} + jZ_d \tan\left(k_{y,d}t\right)}{Z_d + jZ_{in,3} \tan\left(k_{y,d}t\right)} = 0$$

According to the calculation results, the operation frequency for TE_{10} modal is 502 GHz, which is twice as large than the operation frequency we desired. The dimension of the quasi-coaxial in Figure 3.2 shows in Table 3.2.

Table 3.2:Coefficient of suspended strip line in waveguide.

Quantity	Calculated Results
a	183 μm
b	198 μm
a_1	118 μm
a_2	50 μm
t	15 μm
ε_r	11.9

3.2 Through Chip

The objective of the detachable chip-to-chip interconnect prototype is to facilitate the replacement of the terahertz probe chip, which is illustrated in Figure 1.10 of Chapter 1. Consequently, the prototype interconnect is devised to operate within the metal waveguide housing. Our design of impedance matching was aided by the HFSS simulation tool. During the simulation process, we made the assumption that the contact between the male and female interconnects was perfect. The analysis of contact force and contact resistance can be found in Chapter 2.

The prototype interconnects consist of two chips: plug chip and socket chip, as Figure 3.3 shows.

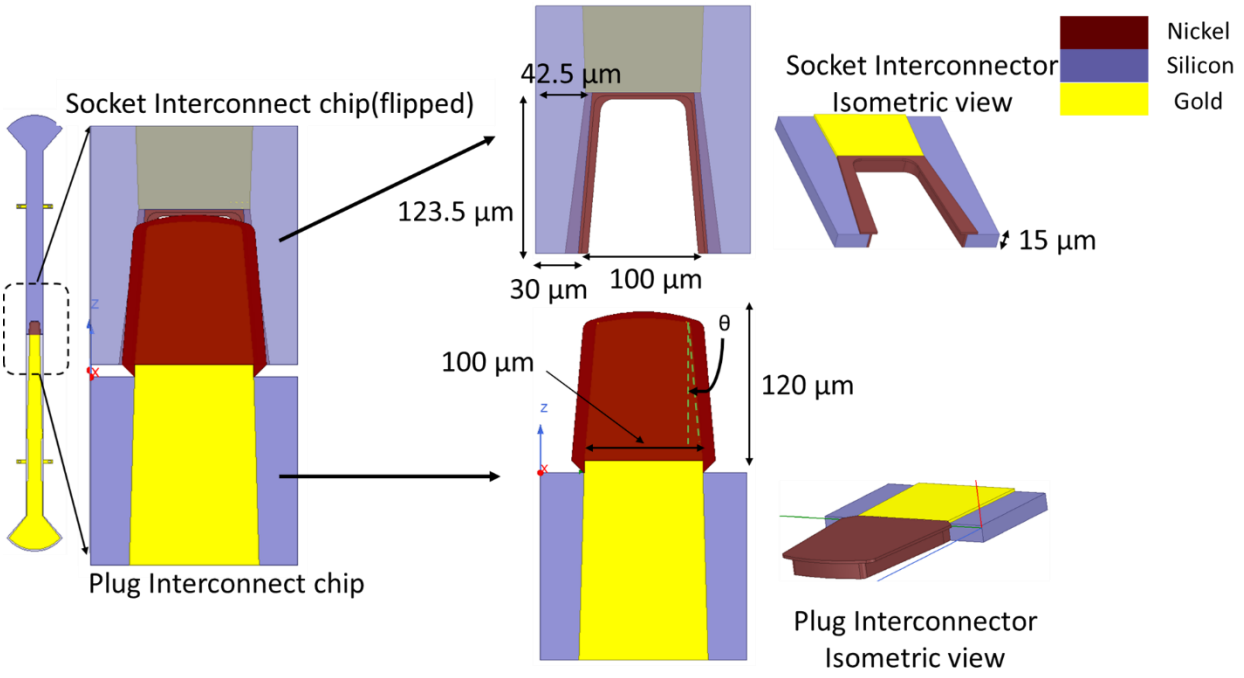


Figure 3.3: Detachable chip-to-chip interconnect demonstration.

The probe chip consists of three parts: the E-plane probe, clamp structures, and the interconnector. The E-plane probe helps to couple the signal from the WR-5.1 waveguide to interconnect chip. The E-Plane probe is suspended inside the waveguide housing, as Figure 3.2 shows. The distance between the E-plane probe and the bottom of the waveguide housing determines the performance of the E-plane probe. The gap between the E-plane probe and waveguide wall is to reduce energy reflected from the waveguide wall, in our design, is 428 µm. Also, the distance from the E-plane probe to the bottom of the waveguide affects the performance of the E-plane probe; in our design the value is 546 µm.

The Ansys HFSS software was utilized to perform simulations on the design using the following default material properties: thin-film gold conductivity of $3 \cdot 10^7$ S/m, nickel conductivity of $1.4 \cdot 10^7$ S/m, and an aluminum block with a 1 μm rms surface roughness and a conductivity of $3.7 \cdot 10^7$ S/m. The relative permittivity of silicon which is 11.9, and the conductivity of silicon which is 0 S/cm. The substrate used in our project is made of high-resistivity silicon, with a resistance greater than 10000 Ω·cm. The simulation's output of 0 conductivity indicates that the dielectric loss is negligible and can be disregarded.

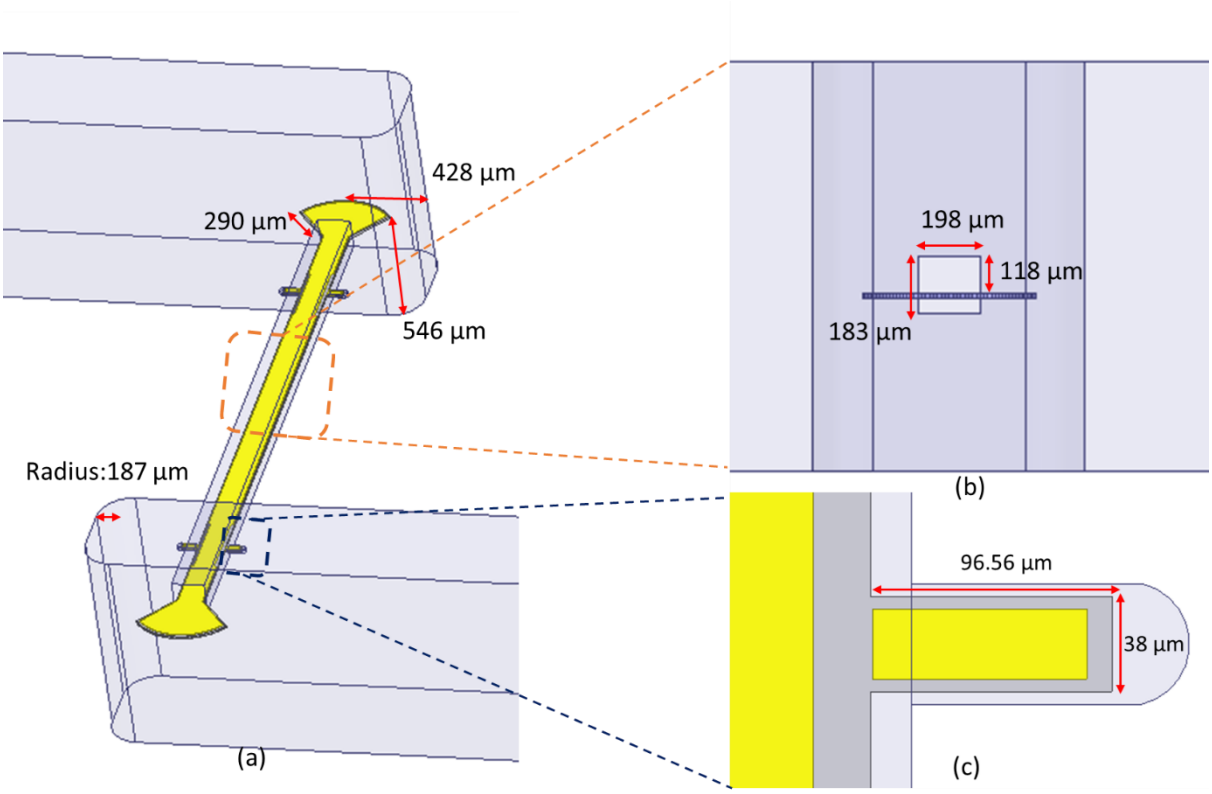


Figure 3.4: (a)Interconnects inside waveguide housing (b)Interconencts inside the RF Channel (c) clamp structure.

The objective of the through chip design is to validate the efficacy of the waveguide housing, E-plane probe, and clamp structure design. As illustrated in Figure 3.2 (b), the through chip is located within the RF channel. In the RF channel, the interconnect operates in quasi-coax mode, with the metal waveguide housing serving as the ground plane. The current on the interconnect chip is concentrated at the edge of the chip. Hence, the interface between the two interconnectors should be positioned near the edge of the interconnect chips to reduce the current discontinuity. The current distribution on the coaxial transmission line shows in Figure 3.5. As simulation shows in Figure 3.5, the current focus on the edge of the center conductor line.

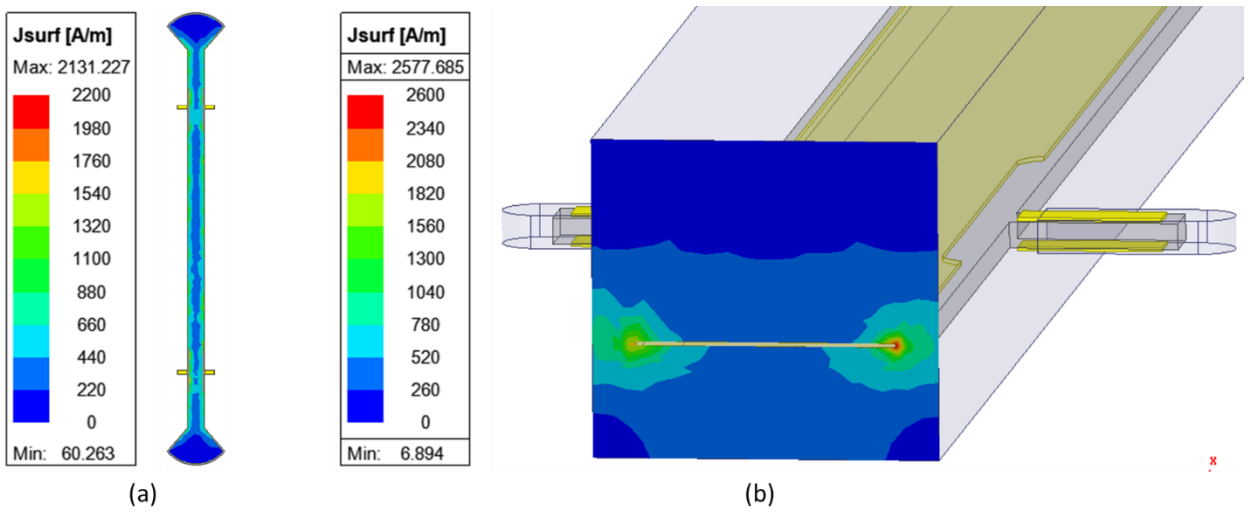


Figure 3.5:(a) Through chip current distribution (b) cross section simulation of through chip current distribution.

In order to secure the chips within the RF channel, two clamps have been devised, as illustrated in Figure 3.4 (c). These clamps are sized at 38 µm by 96.56 µm. Nevertheless, the presence of clamp structures generates a discontinuity in the signal flow, resulting in a current disruption. To mitigate the effects of this current discontinuity stemming from the clamp structures, the gold transmission line on the interconnect chip is severed, as depicted in Figure 3.6. By means of the severed portion of the transmission line near the clamp structure, the simulation reveals an approximate improvement of 10 dB in the return loss of the interconnect, ranging from 140 to 220 GHz.

Figure 3.7 illustrates the simulation results for the through chip with and without the cut structure. In the through chip with the cut structure, the return loss exceeds 20 dB. In contrast, the through chip without the cut structure exhibits a return loss of only over 10 dB, ranging from 140 to 220 GHz.

The simulation reveals that the cut structure plays a pivotal role in determining the return loss of the through chip. Moreover, the loss factor of the through chip reflects the loss arising from impedance mismatch. The loss factor may be calculated utilizing the following equation.

$$Loss\ Factor = 1 - |S_{11}|^2 - |S_{21}|^2$$

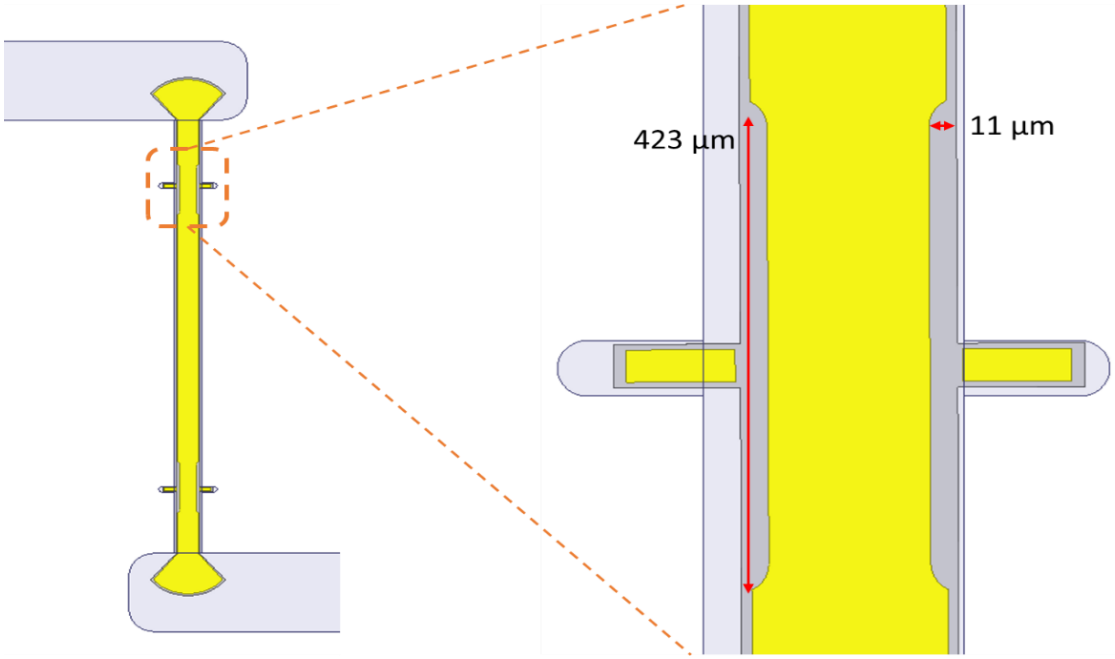


Figure 3.7: Interconnects inside waveguide housing and the clamp compensation structure.

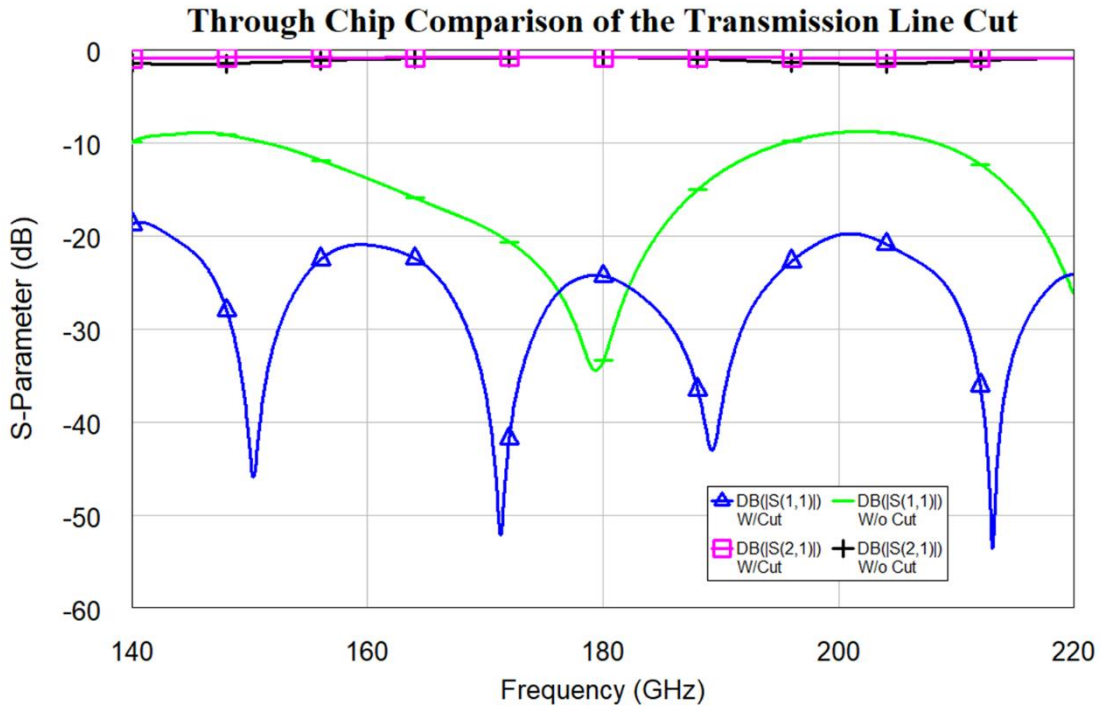


Figure 3.6: Simulation of through chip with and without cut structure.

The following Figure 3.8 shows the loss factor of the through chip with and without cut simulation.

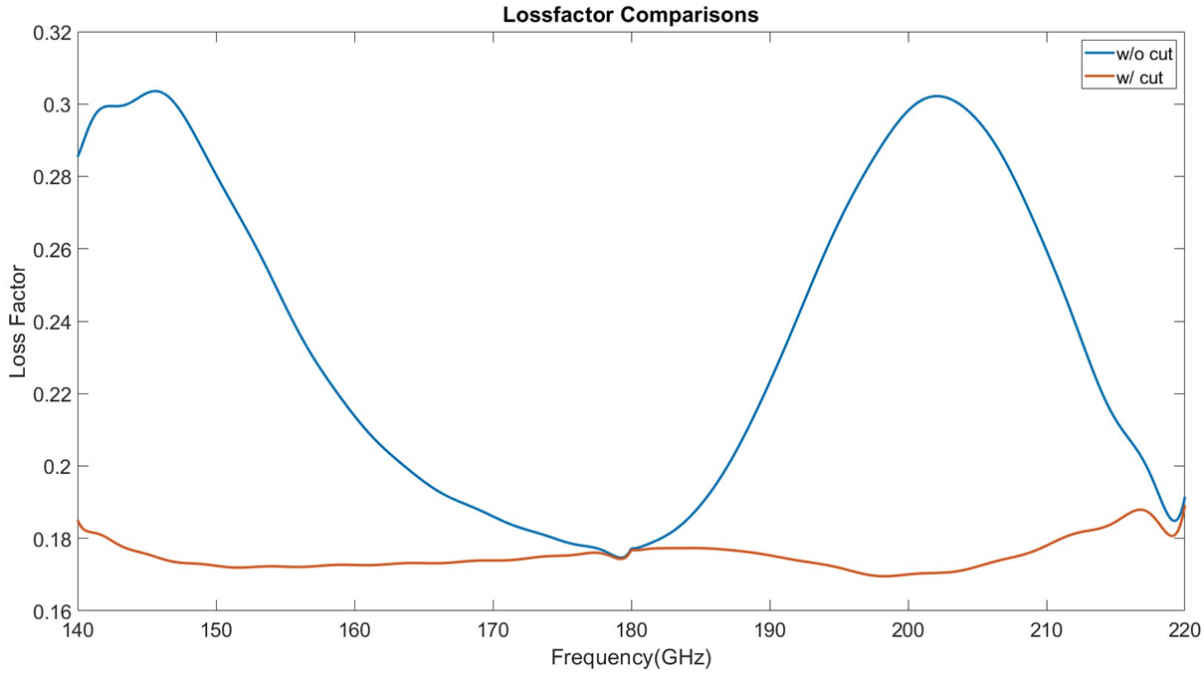


Figure 3.8:Through chip loss factor simulation comparison.

The through chip structure without the cut structure exhibits a significant impedance mismatch, resulting in a higher loss factor of approximately 0.1 compared to the through chip structure with the cut structure between 140 to 160 GHz and 190 to 210 GHz.

3.3 Interconnect chip simulation

Building upon the through chip design and simulation, plug chip and socket chip structures have been incorporated into the through chip design. This design has been bifurcated into two chips, with one being connected to the plug interconnector and the other to the socket interconnector. The simulation layout of the plug chip and socket chip is illustrated in Figure 3.9 and 3.10. It is imperative that the interconnector design takes into account the mechanical structure and contact force, as highlighted in Chapter 2.

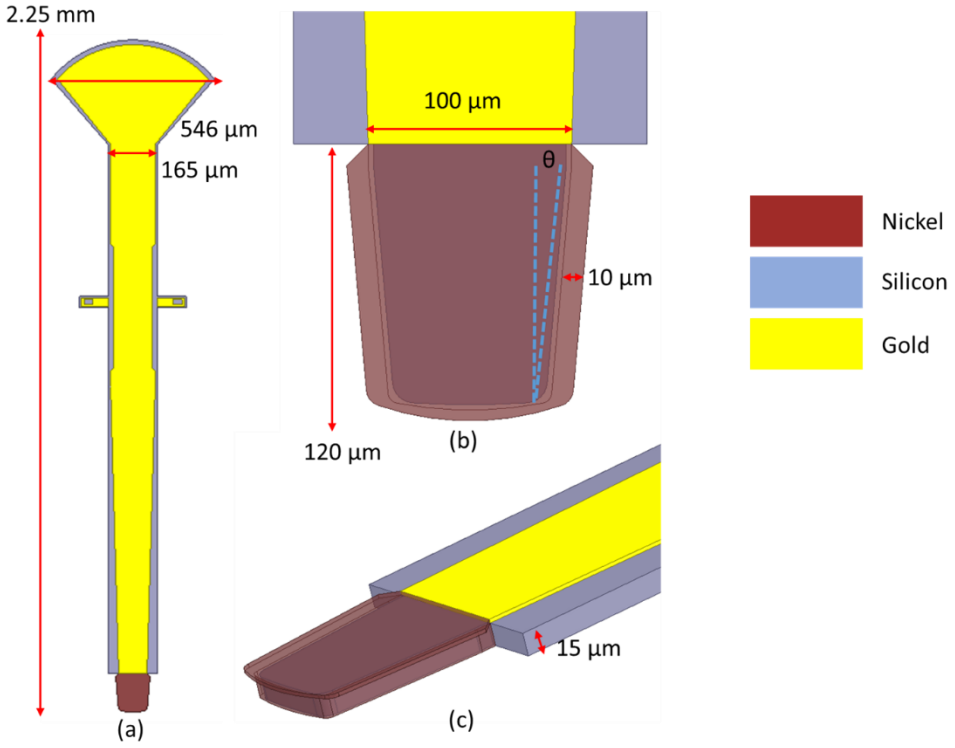


Figure 3.9:(a) Plug chip layout (b) Interconnector part (c) Isometric view of interconnector.

The plug chip has dimensions of 2.25 mm in length and 165 µm in width. The contact part of the interconnector on the plug chip is coated with nickel instead of gold due to a significant reason. Gold has a tendency to adhere together when subjected to contact force, leading to a decrease in the lifetime of interconnects if the gold-covered interconnector head is utilized. Additionally, the gold film may be peeled off under stress.

Figure 3.9 (c) provides an isometric view of the plug interconnector, with the dark red film depicting the thin nickel film. This nickel film has a width of approximately 10 µm and a thickness of 2 µm, which is

attributed to limitations in silicon on insulator fabrication. As can be seen in Figure 3.9 (c), the nickel coating is applied to the side wall of the interconnector, which is the primary contact part between two interconnectors. The design must take into account the fabrication margin required for electroplating nickel on the side wall. Our experience has shown that a margin of 10 µm is an acceptable number for nickel electroplating on the interconnector.

Figure 3.10 provides the HFSS layout of the socket chip, with a focus on the interconnector part, as well as an isometric view of the interconnector. The socket chip has dimensions of 2.14 mm in length and 165 µm in width. The side wall of the socket chip beams has a 2 µm-thick nickel coating. Additionally, due to fabrication limitations, the overlapped area on the beam is 10 µm on top of the silicon beam and 10 µm at the bottom of the silicon beam, as illustrated in Figure 3.10 (b).

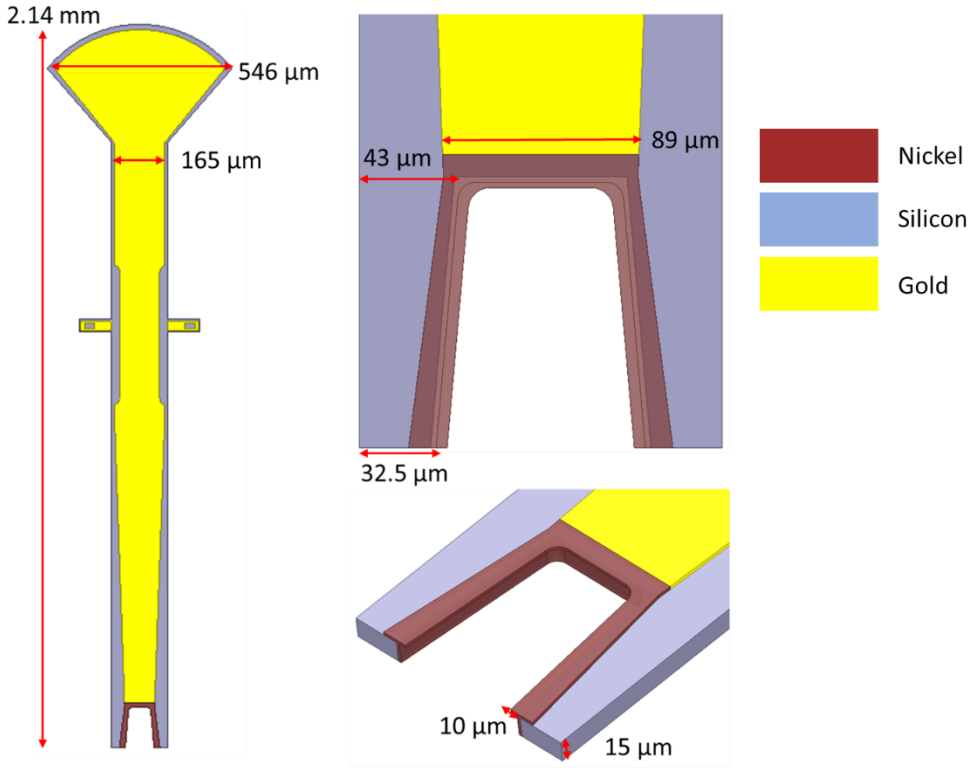


Figure 3.10:(a) Socket chip layout (b) Interconnector part (c) Isometric view of interconnector

The current distribution on the coaxial transmission line within the waveguide housing is depicted in Figure 3.5, wherein it can be observed that the current on the chip flows along the edge of the gold transmission line.

In the RF channel of the waveguide housing, the current on the chip flows at the edge of the gold transmission of the chip. If the socket and plug chips are assembled with their topsides facing upwards, the bottom of the nickel coating will generate extra parasitic capacitance between nickel coating and RF waveguide, as Figure 3.11 shows.

Furthermore, the presences of a nickel thin film resulting from the SOI fabrication process poses challenges in the assembly process. As depicted in Figure 3.11, the overlapping nickel thin films are likely to collide, resulting in increased deformation of the arms of the socket chip during assembly.

Therefore, one of the chips must be flipped and then assembled with another interconnect, as Figure 3.12 shows. The current flows from one chip along the nickel coating on the side wall and transmits to another chip. The flipped chip assembly can significantly decrease the parasitic capacitance at the assembly interface.

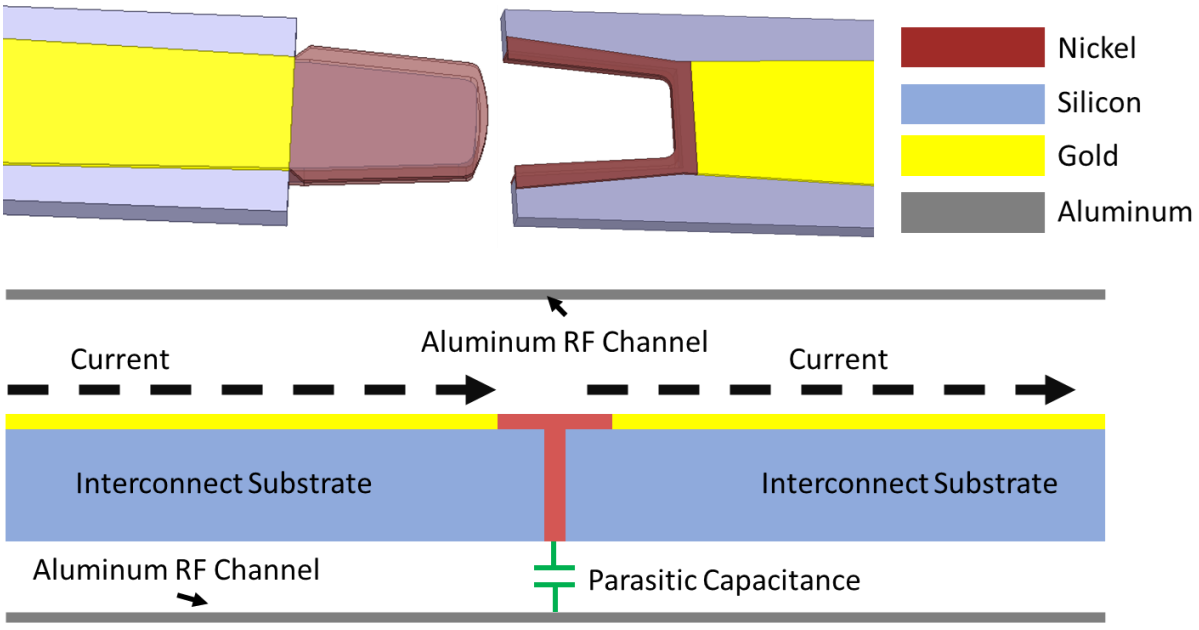


Figure 3.11:Chip to chip interconnect non-flipped assembly and current flow.

The simulation comparison of the assembled interconnect chips with and without flipped. The simulation result shows in Figure 3.13.

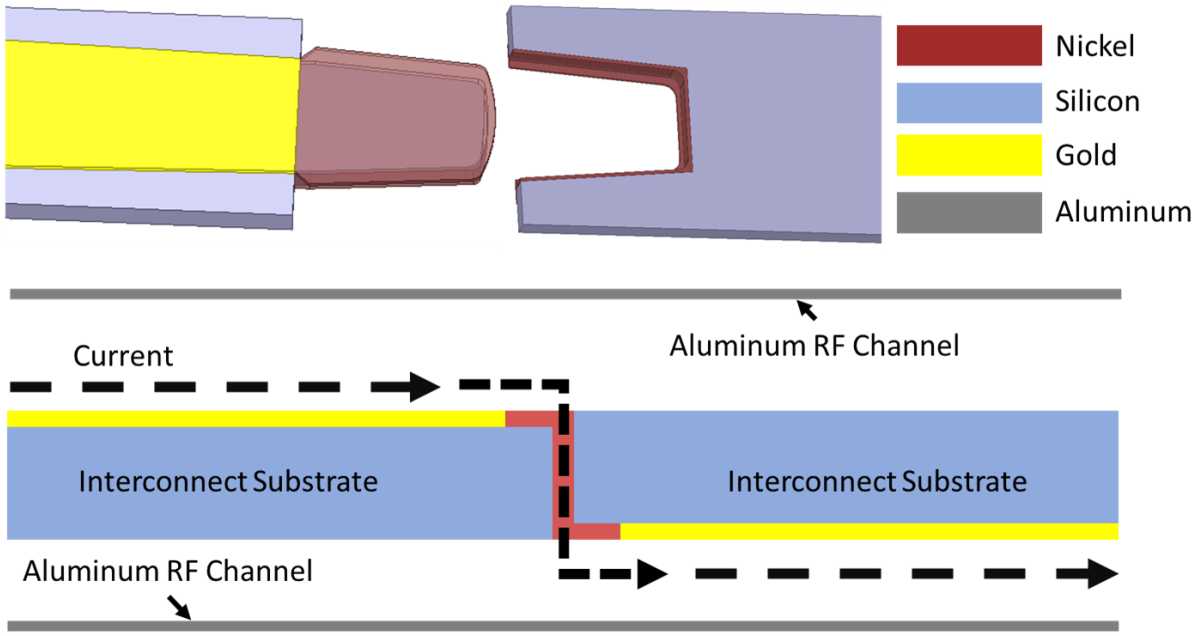


Figure 3.13:Chip to chip interconnect flipped assembly and current flow

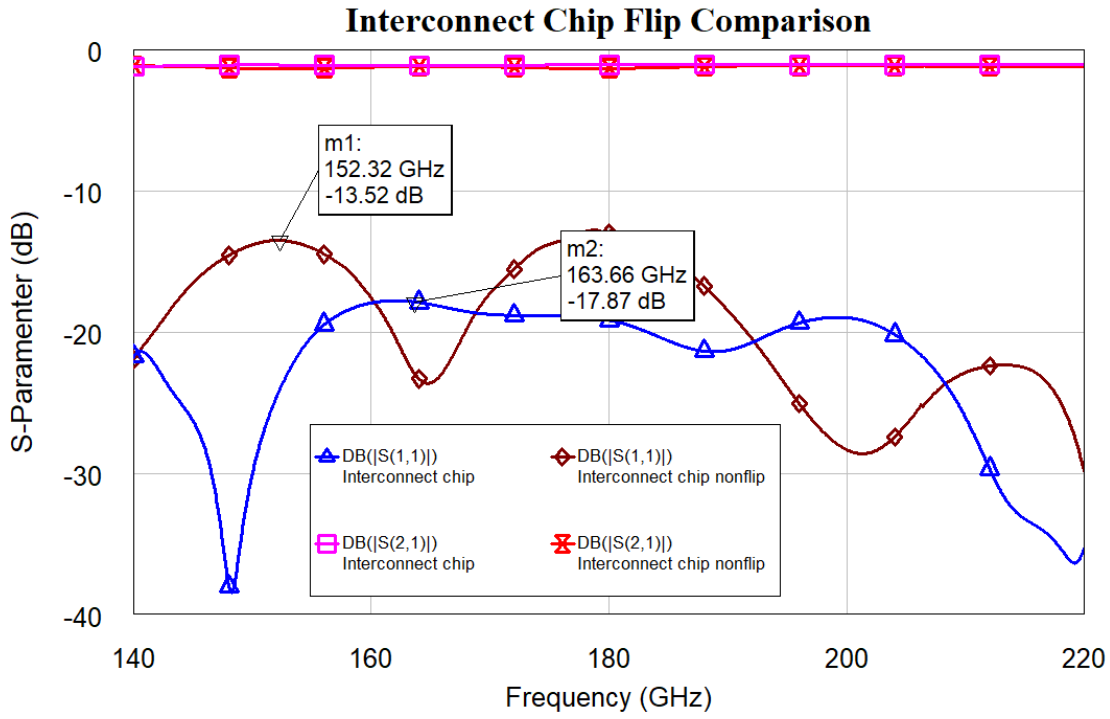


Figure 3.12: Interconnect chip simulation with and without flipped.

As Figure 3.13 shows, the return loss of the interconnect chip without flipped decrease approximately 4 to 4.5 dB. The lowest return loss decrease from 18 dB to 13.5 dB.

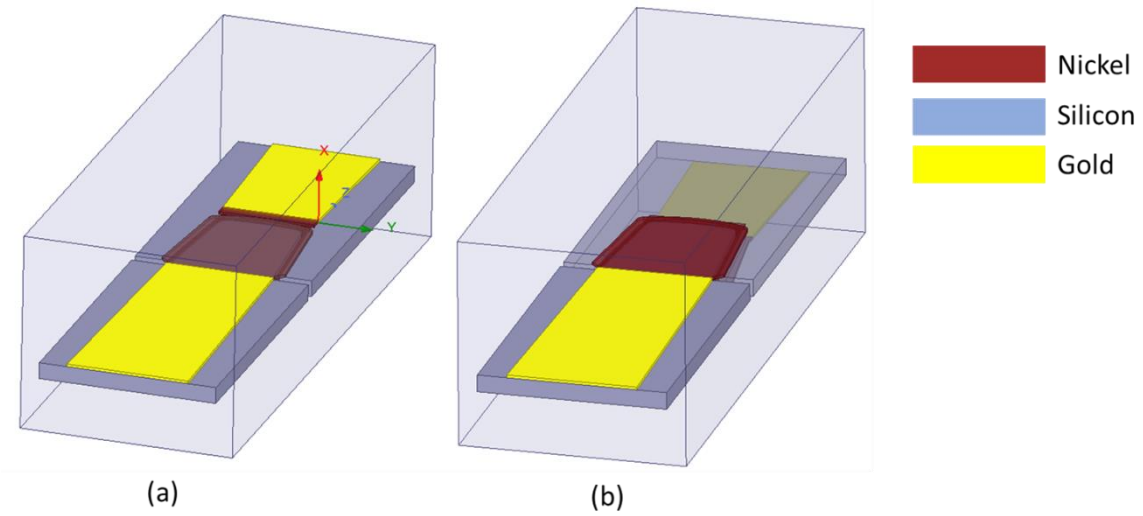


Figure 3.14:(a) Simplified non-flipped interconect simulation (b Simplified non-flipped interconect simulation.

In order to mitigate the impedance resulting from the E-plane probes and clamp structures, we simplified our simulation approach to focus solely on the interconnector components. Figure 3.14 illustrates the suspended interconnector simulation within the RF channel, and compares the S-parameters and loss factors of both the flipped and non-flipped assembled interconnects. The simulation results are presented in Figure 3.15 and 3.16.

The simplified simulation of the interconnector specifically targets the interconnector and reveals that the flipped interconnector exhibits superior performance compared to the non-flipped interconnector, with a 1 dB higher return loss and 0.07 dB lower insertion loss between 140 to 220 GHz. Furthermore, the flipped interconnector demonstrates a lower loss factor by 0.015 compared to the non-flipped interconnector.

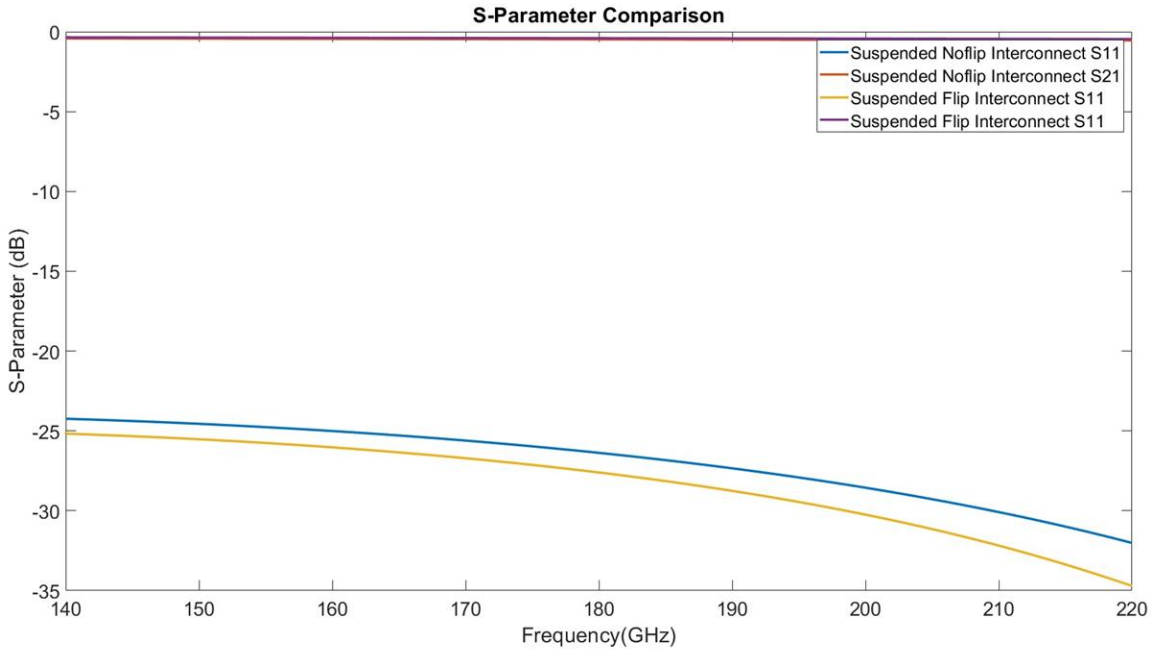


Figure 3.16:Simulation results of simplified flipped and non-flipped interconnector.

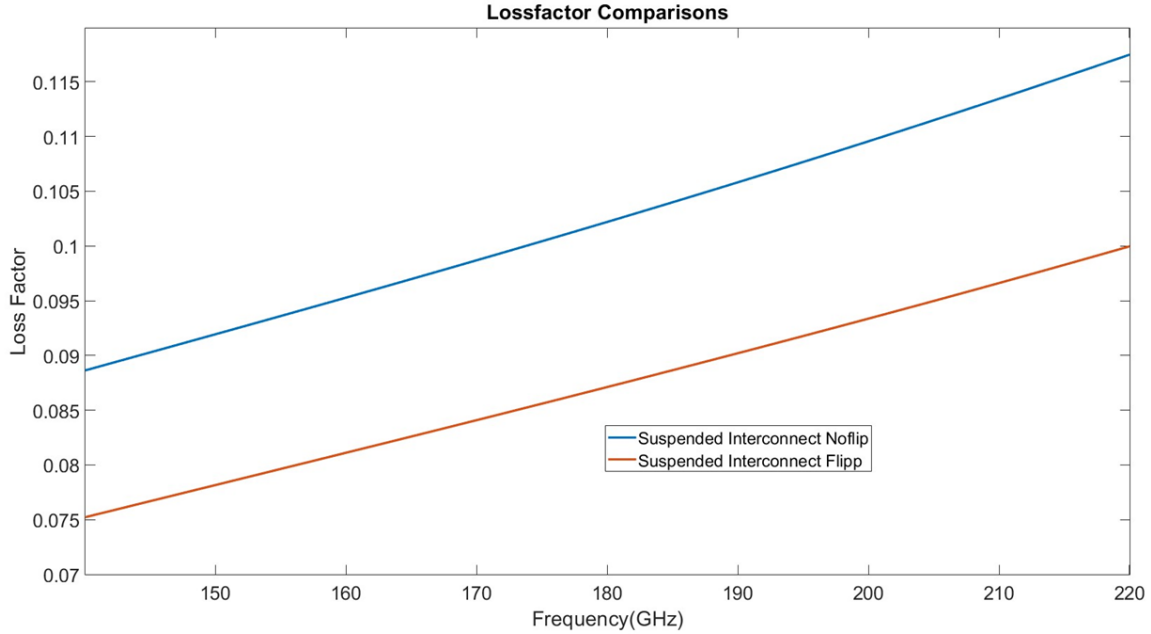


Figure 3.15:Lossfactor Simulation of simplified flipped and non-flipped interconnectors.

3.3.1 Comprehensive Detachable Chip-to-chip Interconnect Simulation

The comprehensive chip-to-chip interconnect simulation is shown in Figure 3.17. The socket chip flipped inside the rf waveguide channel and assembled with the plug chip.

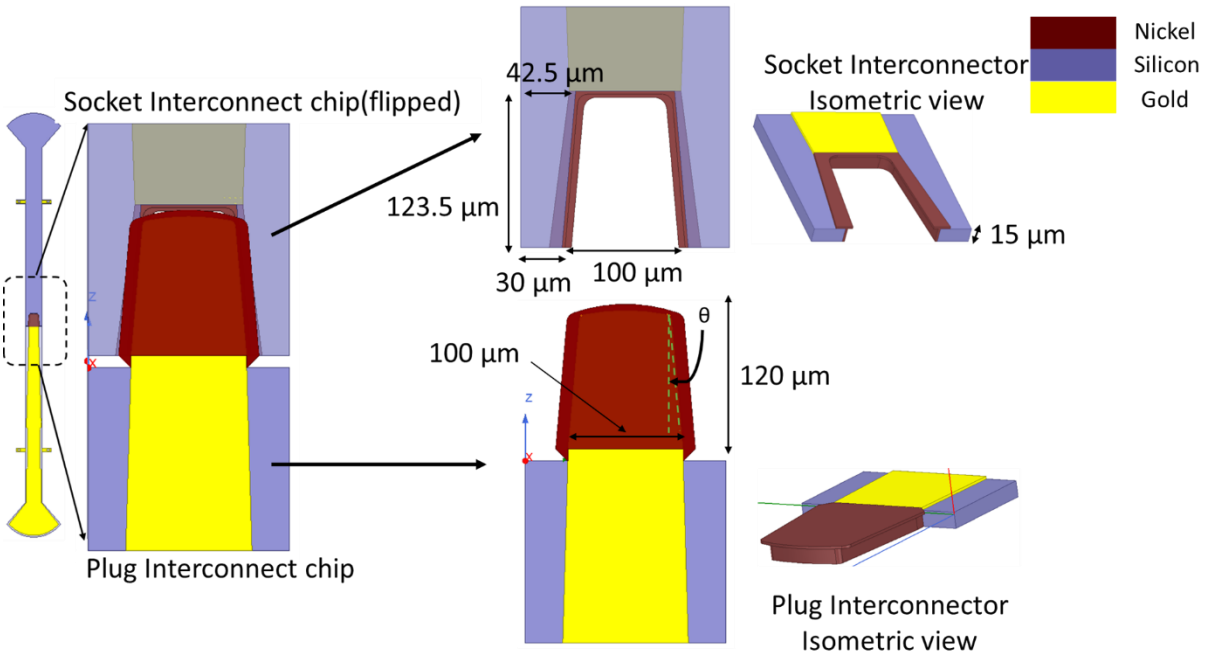


Figure 3.17:Comprehensive simulation of chip-to-chip interconnect.

The simulation results of the chip-to-chip interconnect are shown in Figure 3.18. Also, the comparison of the interconnect chip and through chip is shown in Figure 3.18.

According to the simulation results, the return loss of quasi-coaxial and through chip are above 20 dB from 140 GHz to 220 GHz; the return loss of the chip-to-chip interconnects above 18 dB from 140 to 220 GHz. The forward loss factor comparison shows in Figure 3.19.

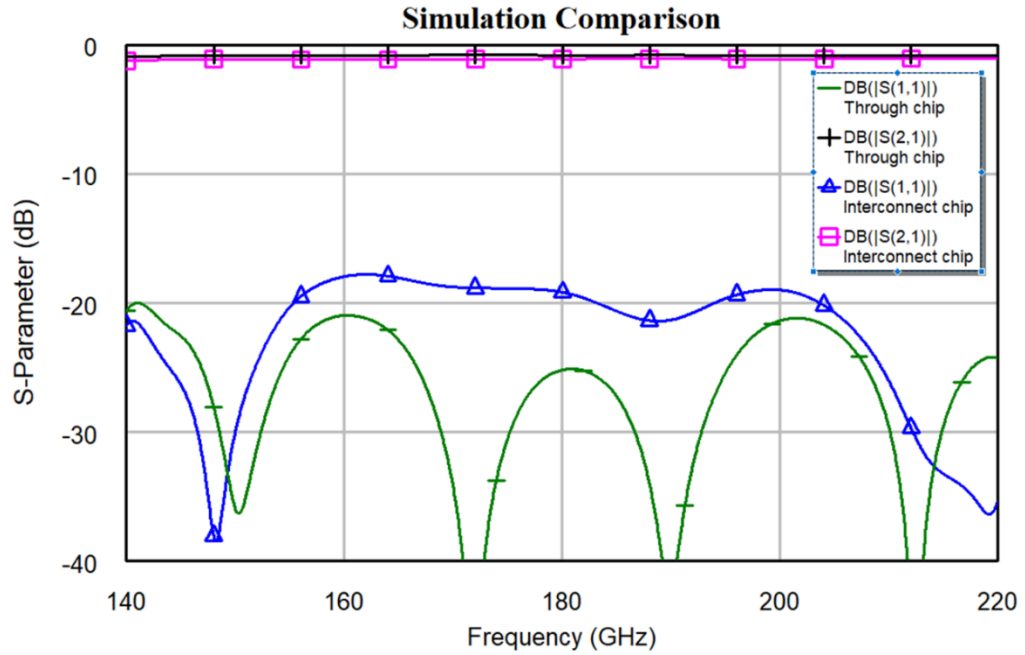


Figure 3.19:Simulation results of through chip and interconnect chip.

The observed trend of the chip-to-chip interconnect is similar to that of the through chip, but the loss factor is higher by approximately 0.06. This increase in loss is attributed to the additional loss contribution of the nickel coating conductor.

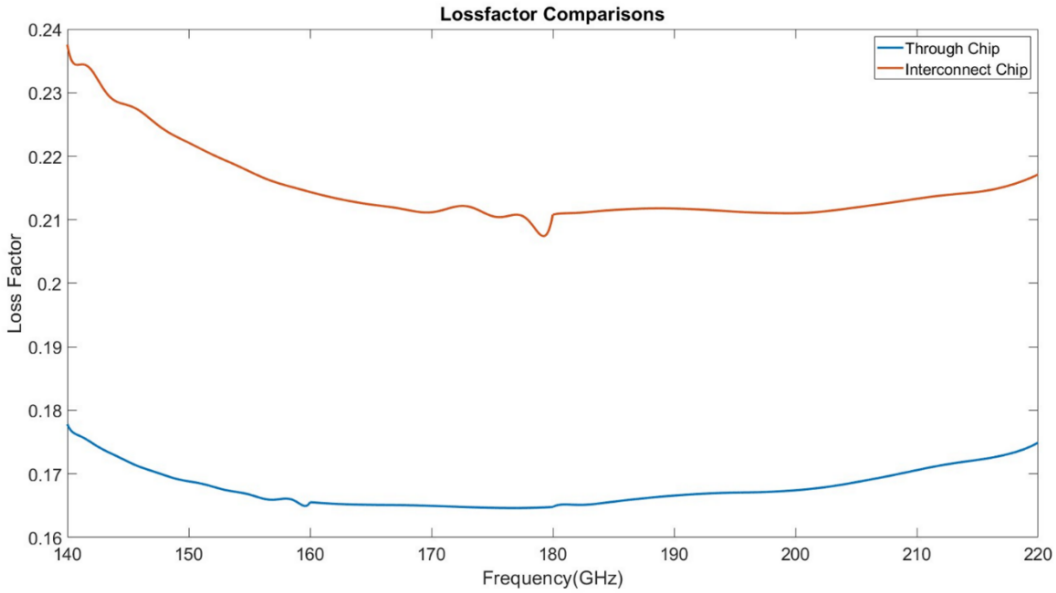


Figure 3.18:Loss factor comparison between through chip and interconnect chip.

In order to validate the additional loss factor sources in the interconnect chip simulation, we conducted simulations of the suspended stripline and suspended interconnector structures within the RF channel, as illustrated in Figure 3.20.

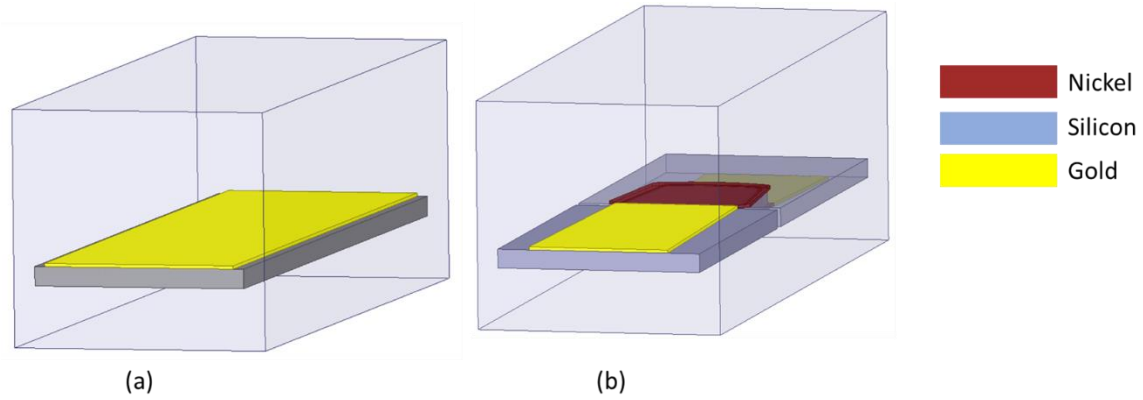


Figure 3.20:(a) Suspended stripline inside RF channel (b) Suspended interconnect inside RF channel.

Figure 3.21 displays the S-parameter simulations of the suspended stripline and interconnect structures within the RF channel. The suspended stripline exhibits an insertion loss ranging from 0.057 to 0.073 dB between 140 to 220 GHz, and a return loss ranging from 52.5 to 50.5 dB between 140 to 220 GHz.

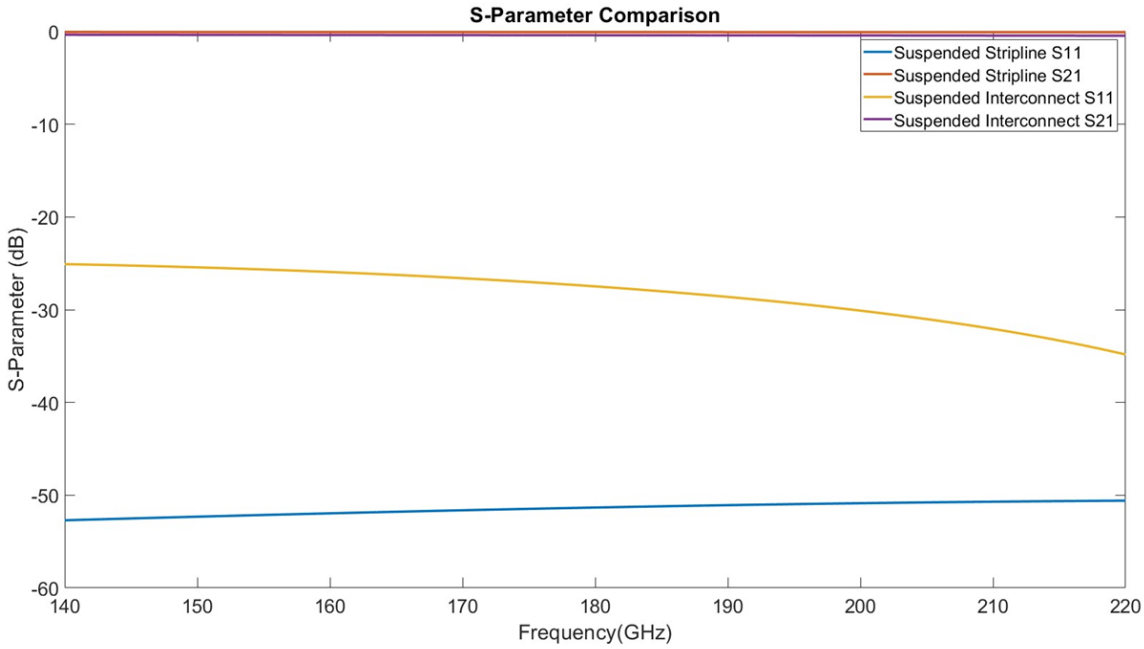


Figure 3.21:S-parameter comparison of suspended stripline and interconnect.

In contrast, the suspended interconnect demonstrates a higher insertion loss, ranging from 0.37 to 0.45 dB between 140 to 220 GHz, and a lower return loss, ranging from 25 to 35 dB between 140 to 220 GHz.

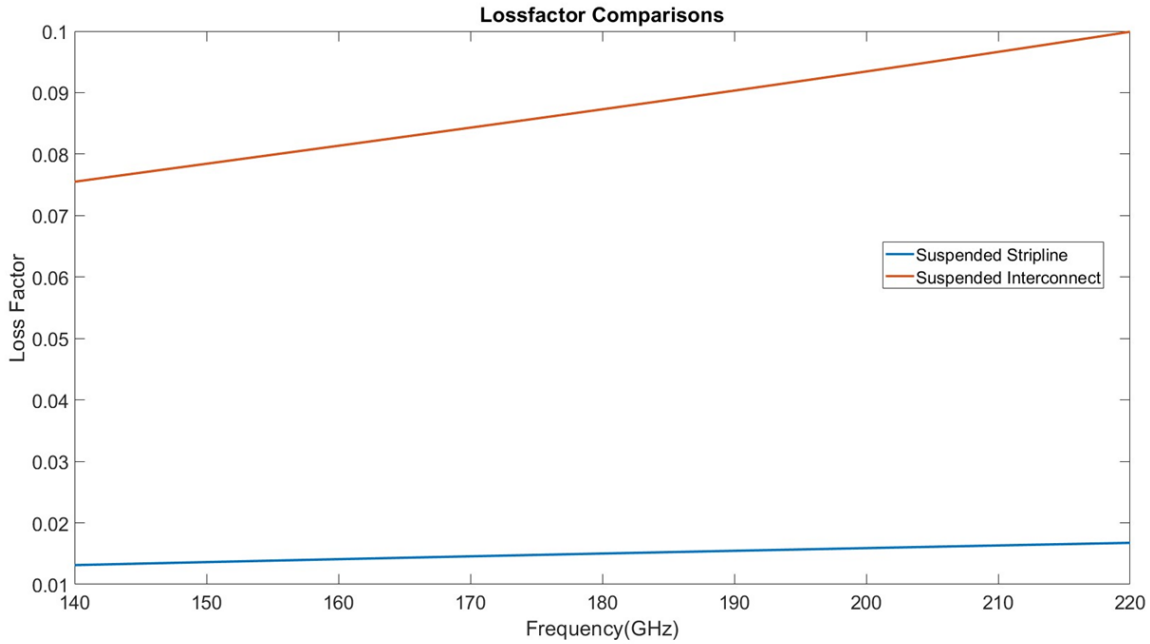


Figure 3.22: Lossfactor simulation comparison of suspended stripline and interconnect.

The results of the loss factor simulation, as presented in Figure 3.22, indicate that the suspended interconnector exhibits an additional loss factor of approximately 0.07 compared to the suspended stripline. These findings are consistent with the comparison of loss factor simulations between the through chip and interconnect chip, and suggest that the primary source of the additional loss factor in the interconnect is likely due to the nickel contact part.

3.4 Chip-to-chip interconnect measurements

The chip-to-chip interconnects and through-chip designs were fabricated using a micromachining process described in the work by Zhang et al. [13]. Further details of the fabrication process can be found in Appendix A. The dimensions of the fabricated interconnect chips are 2.2 mm in length, 0.5 mm in width, and 15 μm in thickness.

To ensure reliable assembly of the chips, a custom jig is created by etching a 25-μm deep outline into a silicon wafer. The plug and socket chips are then positioned within the jig, and a flat quartz wafer is placed on top to hold the chips in place. Figure 3.23 displays the assembly gears and alignment wafer used in this process. To assemble the interconnect chips, one chip is placed on the left side of the channel while the other is carefully pushed using a micromanipulator from the right side of the chip.

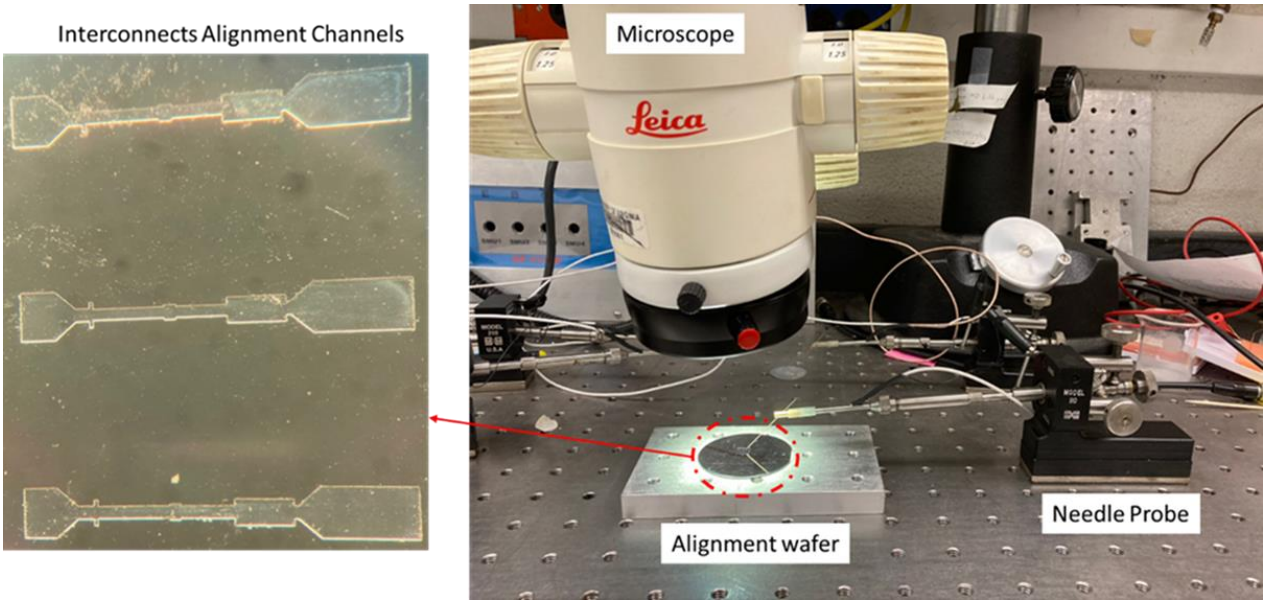


Figure 3.23:Chip-to-chip interconnect assembly gears.

The chips that have been assembled are subsequently inserted into the waveguide block, as illustrated in Figure 3.24, and their characteristics are assessed using a Rohde & Schwarz ZVA-67 vector network analyzer and VDI WR 5.1 waveguide extenders. During these measurements, the reference plane is defined at the waveguide flange interface of the aluminum block shown in Figure 3.24. The measurement outcomes encompass both 28 mm of WR5.1 waveguide and 4 mm of rectangular coax.

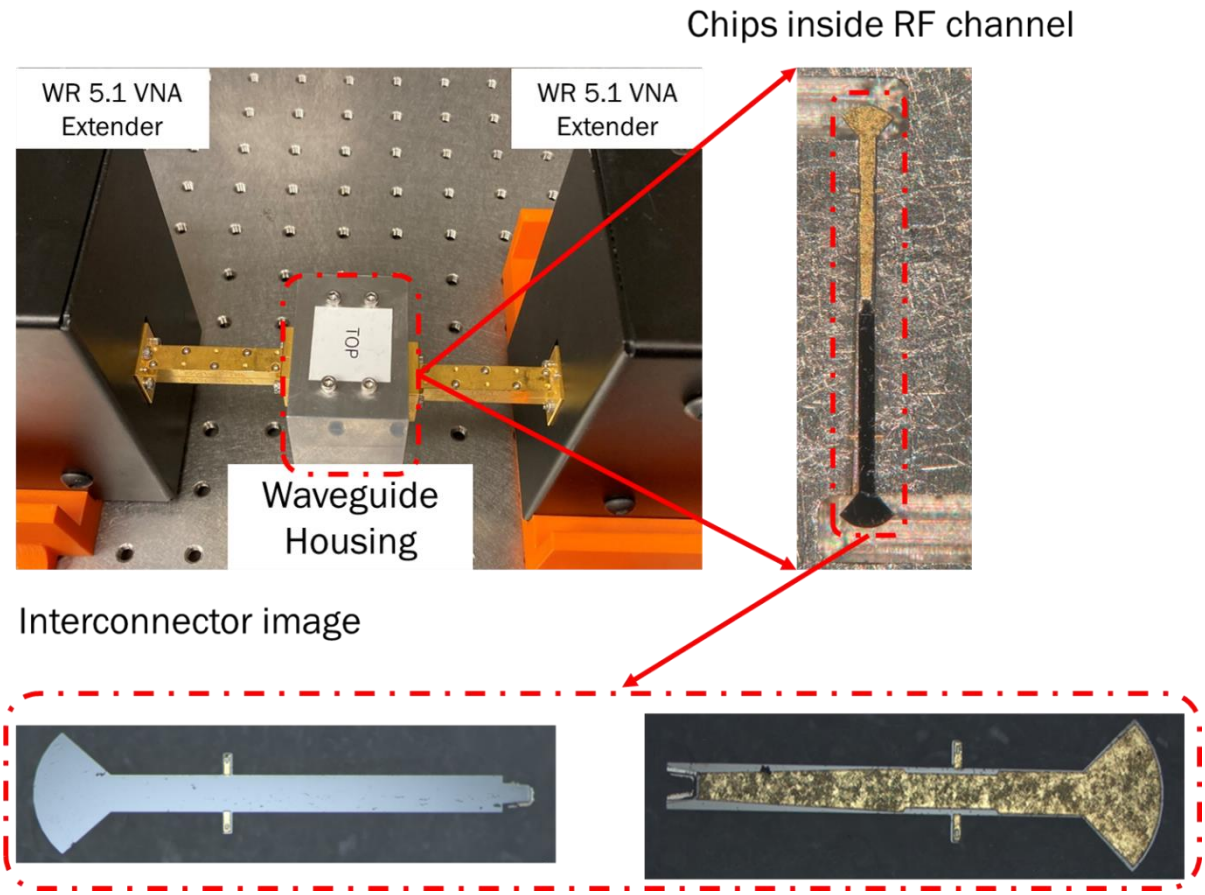


Figure 3.24:Chip-to-chip interconnect waveguide housing and interconnect chips.

The calibratoin method we applied is short, quarter-wavelength short, load and direct through. For the following measurements, the reference plan is set at the waveguide flange interface of the aluminum block seen in Figure 3.24. The following measured includes 28 mm of WR5.1 waveguide and 4 mm of rectangular coax.

We verified the performance of the aluminum block using the through chip design as depicted in Figure 3.4. The results obtained from the measurements presented in Figure 3.25 reveal that the return loss is greater than 14 dB, and the insertion loss is less than 1.5 dB throughout the frequency band. Despite the results being lower than expected, the authors attribute this discrepancy to a variety of factors, such as misalignment during the fabrication process, misalignment of the chip within the coaxial channel, and chip bending caused by the surface tension of plated gold.

According to the results shown in Figure 3.25, the measured performance of the chip-to-chip interconnect exhibits a return loss of 8 to 10 dB below 165 GHz, and it improves to better than 10 dB from 165 to 220 GHz. However, this return loss is lower than the expected value, which can be attributed to the misalignment of the chip-to-chip interconnect assembly as observed in Figure 3.24. On the other hand, the insertion loss of the chip-to-chip interconnect is slightly higher than that of the measured through chip (1.5 to 2 dB across the band), indicating the interconnect interface's excellent performance.

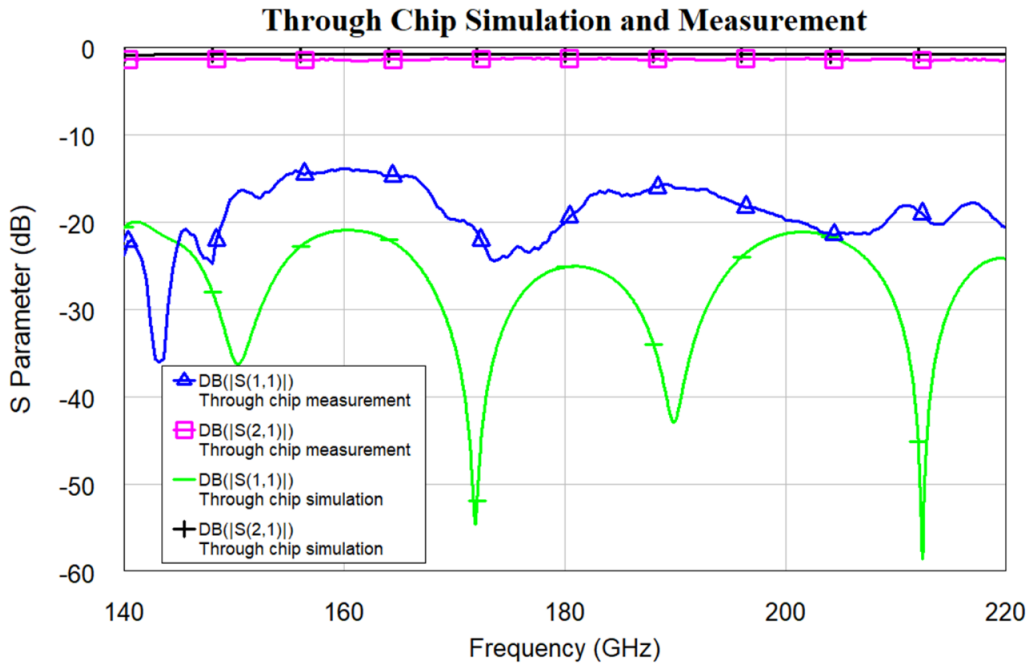


Figure 3.25:Simulation and measurement comparison of through chip.

According to the results shown in Figure 3.25, the measured performance of the chip-to-chip interconnect exhibits a return loss of 8 to 10 dB below 165 GHz, and it improves to better than 10 dB from 165 to 220 GHz. However, this return loss is lower than the expected value, which can be attributed to the misalignment of the chip-to-chip interconnect assembly as observed in Figure 3.26. On the other hand, the insertion loss of the chip-to-chip interconnect is slightly higher than that of the measured through chip (1.5 to 2 dB across the band), indicating the interconnect interface's excellent performance.

To quantify the extent of bending in the through chip, a small piece of glass was employed as a reference surface, as illustrated in Figure 3.26 (a) and (b). The results of this measurement revealed that one side of the through chip exhibits a bending of approximately 175 μm, while the other side lies flat against the glass surface.

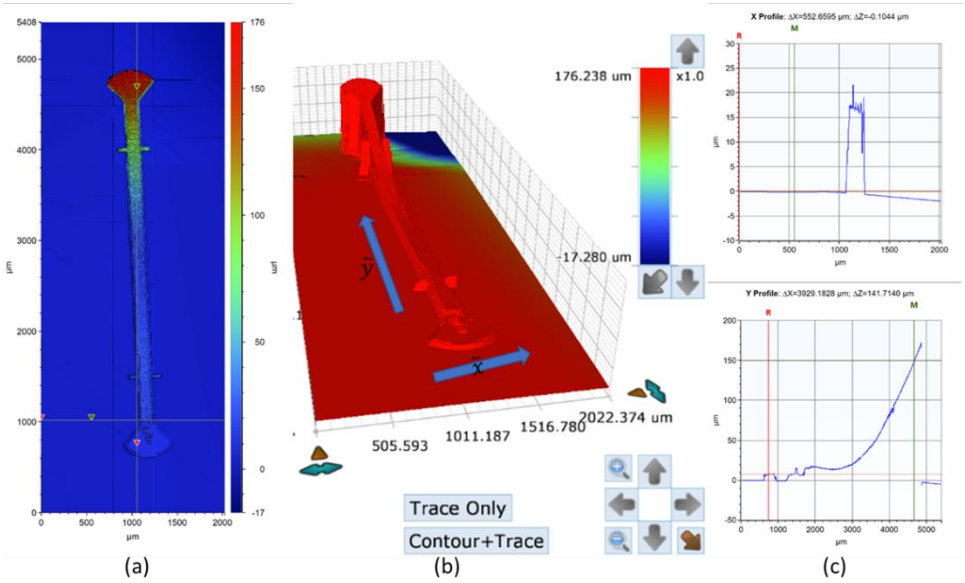


Figure 3.26:White light thermometer height measured results.

We adjust the simulation in the HFSS with both side 75 μm tilt bending inside the RF channel. The simulation results fit better with the measured results as Figure 3.27 shows.

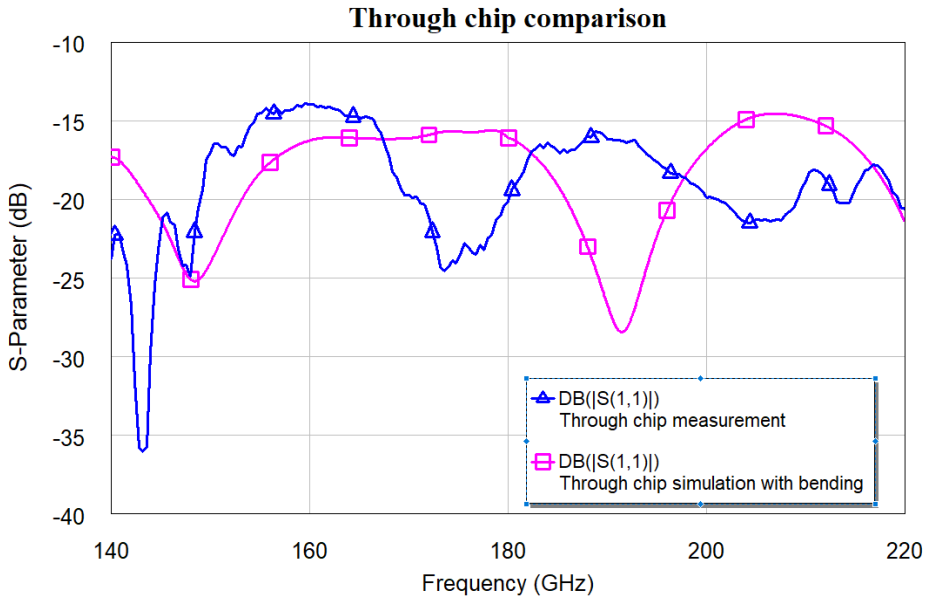


Figure 3.27:Modified Simulation and measured result comparison.

Figure 3.27 shows the measurement results of the loss factor for both the interconnect chips and through chip. The interconnect chip has a higher loss factor than the through chip, ranging from 0.25 to 0.33, while the through chip has a loss factor ranging from 0.25 to 0.28.

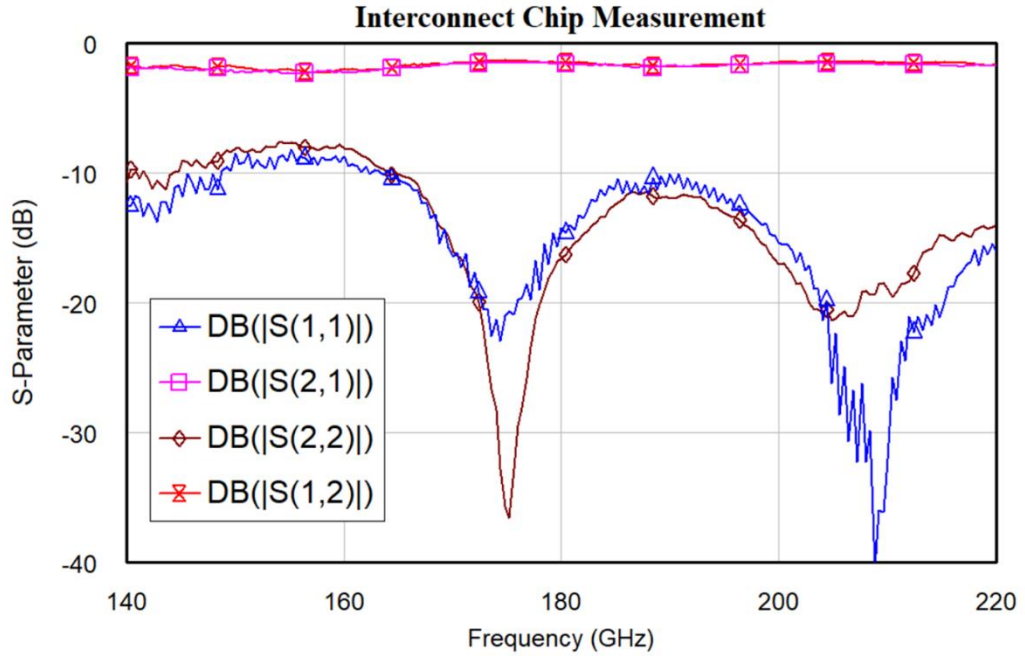


Figure 3.28: chip-to-chip interconnect measured results.

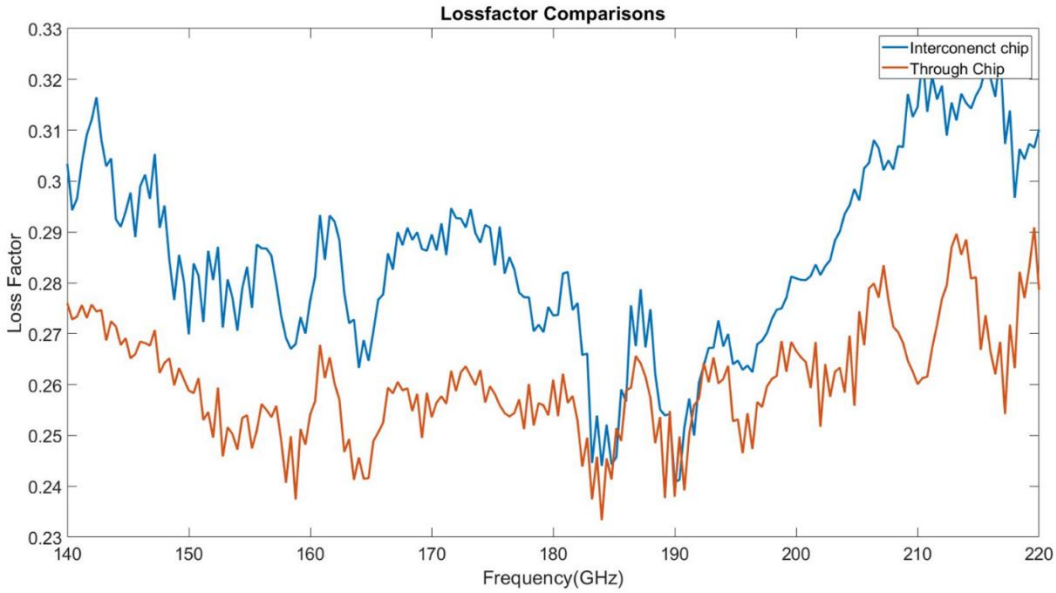


Figure 3.29:Loss factor comparison of through chip and interconnect chip.

The previous chapter on contact resistance measurement indicates that the contact resistance of the nickel interface is between approximately 0.8 Ω to 1 Ω, and varies depending on the amount of contact force applied. If the contact resistance increases, it will result in an additional insertion loss increase ranging from 0.1 dB. Based on the results of the measured contact resistance, we hypothesize that the difference in loss factor between the interconnect chip and through chip is due to the contact resistance between nickel contacts.

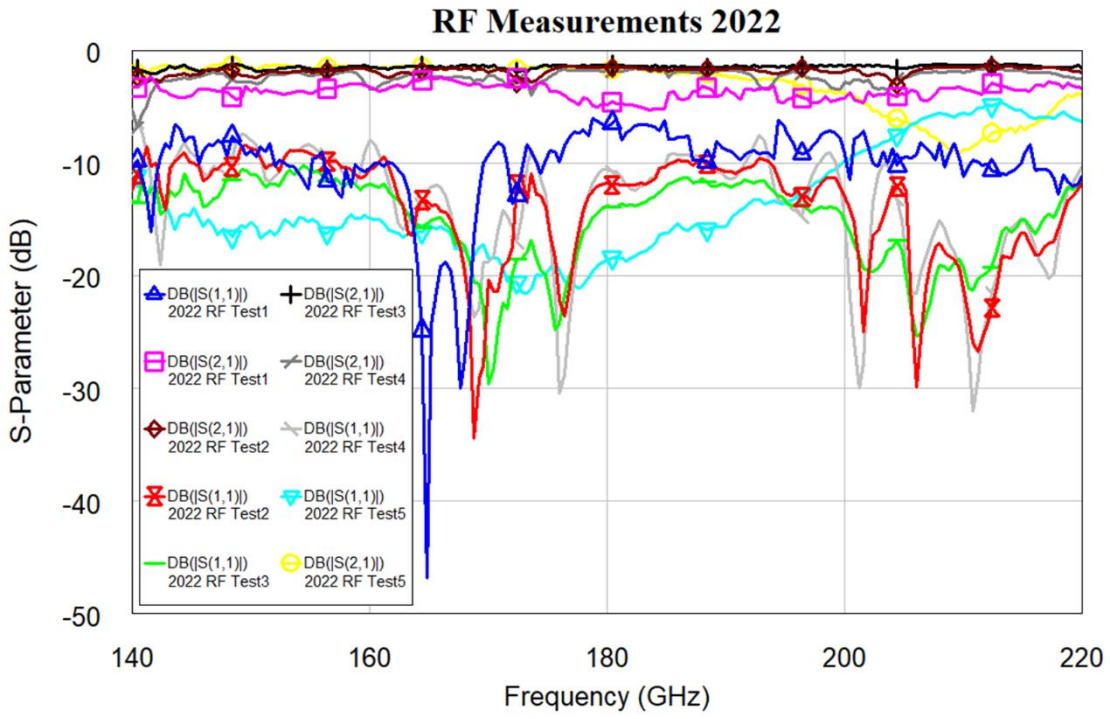


Figure 3.30: RF Measurements in 2022.

We conducted an additional five measurements of the chip-to-chip interconnect, resulting in insertion loss variations ranging from 1.4 dB to 2.6 dB and return loss measurements ranging from 6 dB to 15 dB. The test results also indicated a return loss of up to 4 dB for frequencies above 200 GHz. One potential cause for the measurement variations may be misalignment of the interconnect within the RF channel, as shown in Figure 3.31, where the interconnect chip appears to be rotated approximately 1 degree counterclockwise. While the RF measurements were not consistently perfect, we have identified several potential solutions to improve the interconnect design, which will be discussed in Chapter 4.

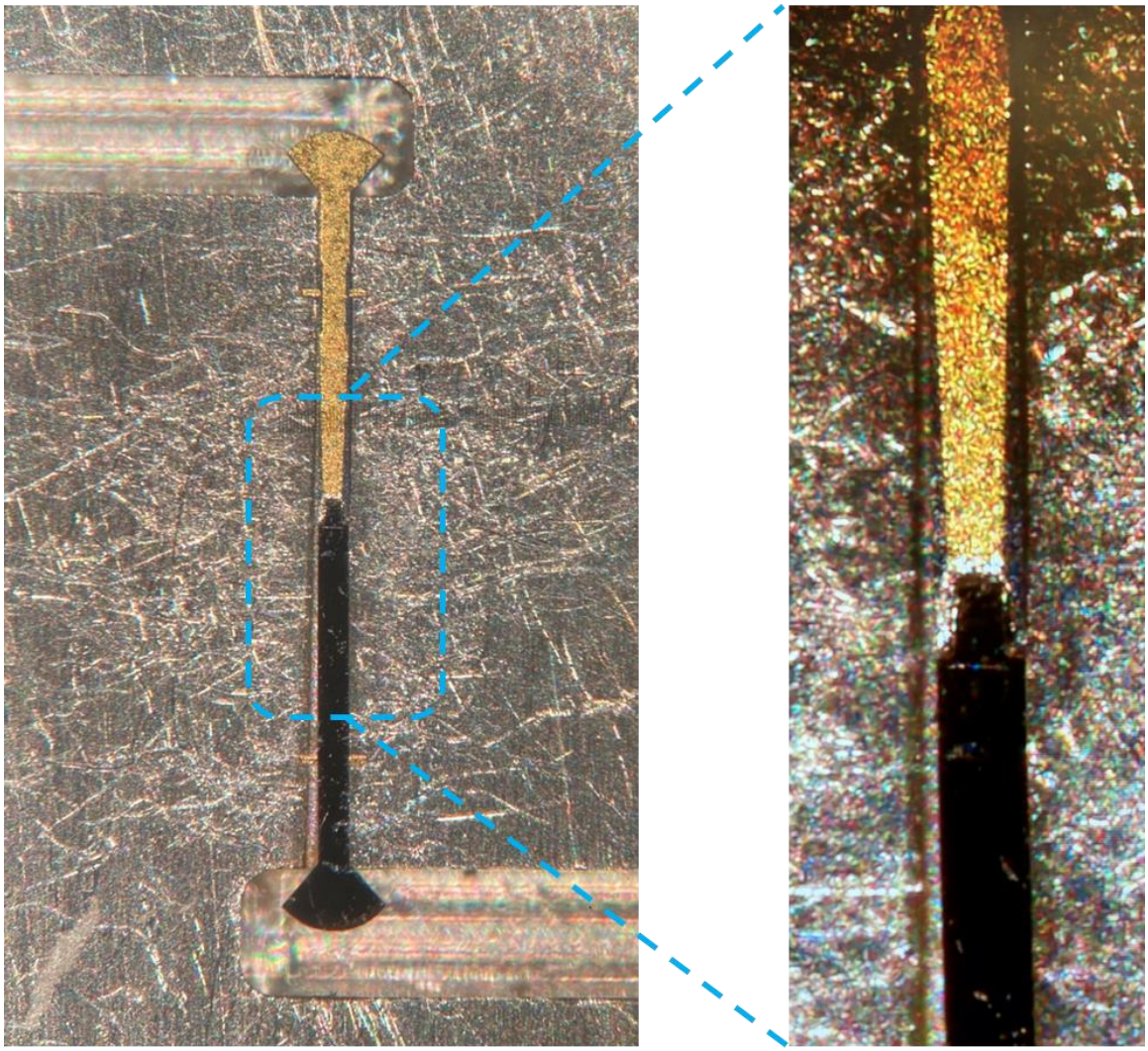


Figure 3.31: Interconnect chip image of Test3.

3.5 Beam lead chip

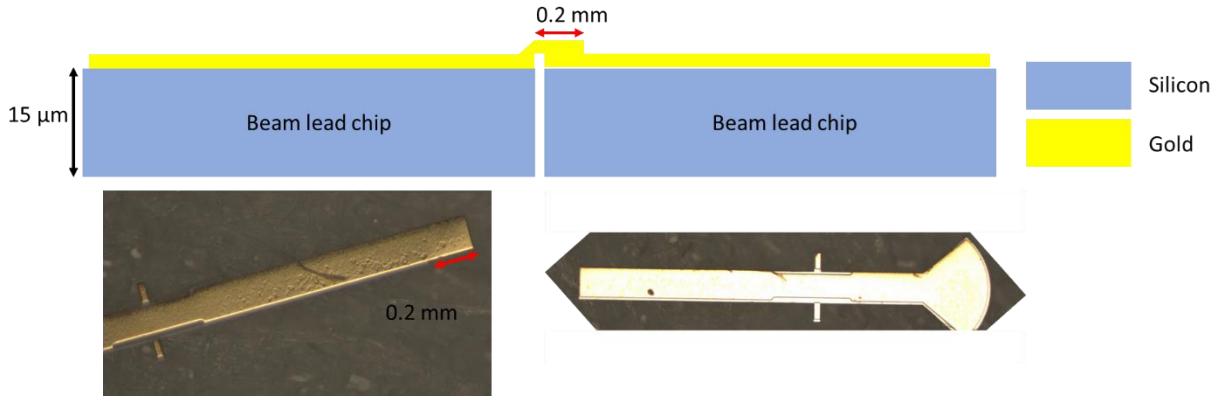


Figure 3.32:Beam lead chip conception demonstration.

Beam-lead interconnection is a potential solution for chip-to-chip interconnects, but it is not ideal for multiple connections and disconnections, similar to wire bonding solutions. The design of beam-lead interconnects is intended to provide a non-detachable and permanent connection. The beam-lead chips, as shown in Figure 3.32, are based on the through chip design. The beam lead part of the chip is 200 µm in size. The beam lead interconnector is bonded onto another chip through a chip bonding machine using high pressure and high temperature to firmly join the gold pads together.

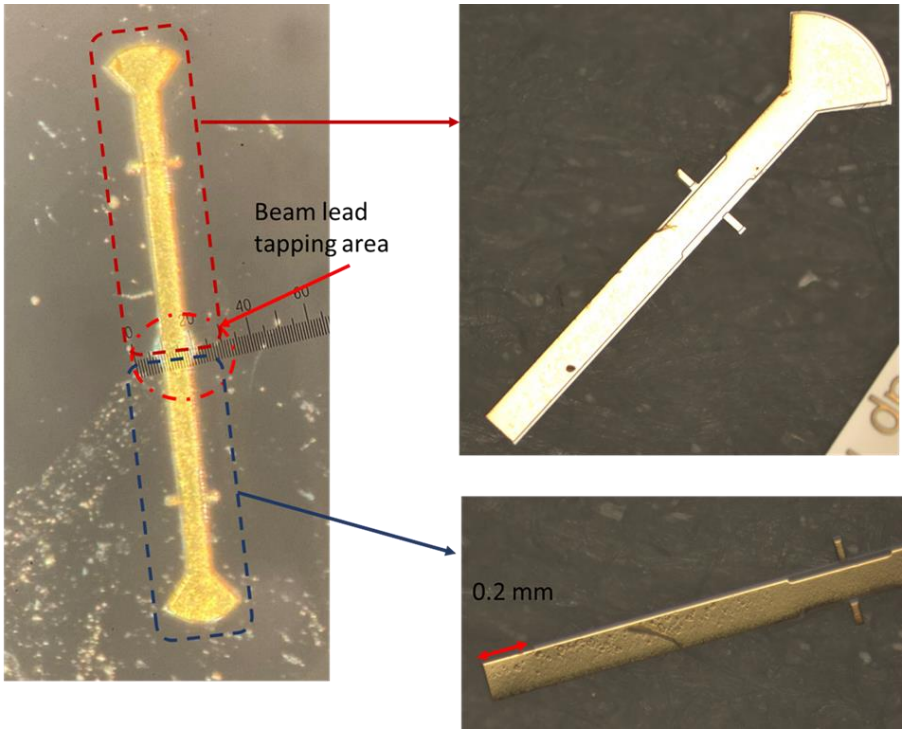


Figure 3.33:Assembled beam lead chips and separated beam lead chips

Figure 3.33 depicts a beam lead chip that has been fabricated on a 15 μm thick silicon on insulator (SOI) wafer. To assemble the beam lead chip, the chips are positioned within the alignment wafer as shown in Figure 3.23. Once the chips are placed within the channel of the alignment wafer, the bonding machine is applied to compress the beam lead chips together.

After the beam lead chips bonded together, the chips are placed inside the aluminum waveguide house for measurement. The measured results are shown in Figure 3.34. In Figure 3.34, the return loss and insertion loss of the beam lead chip and through chip are compared. As Figure 3.34 shows, the insertion loss of the beam lead chip is between 1.1 dB to 1.3 dB from 140 GHz to 220 GHz. The return loss of the beam lead chip is between 16 dB to 28 dB from 140 GHz to 220 GHz.

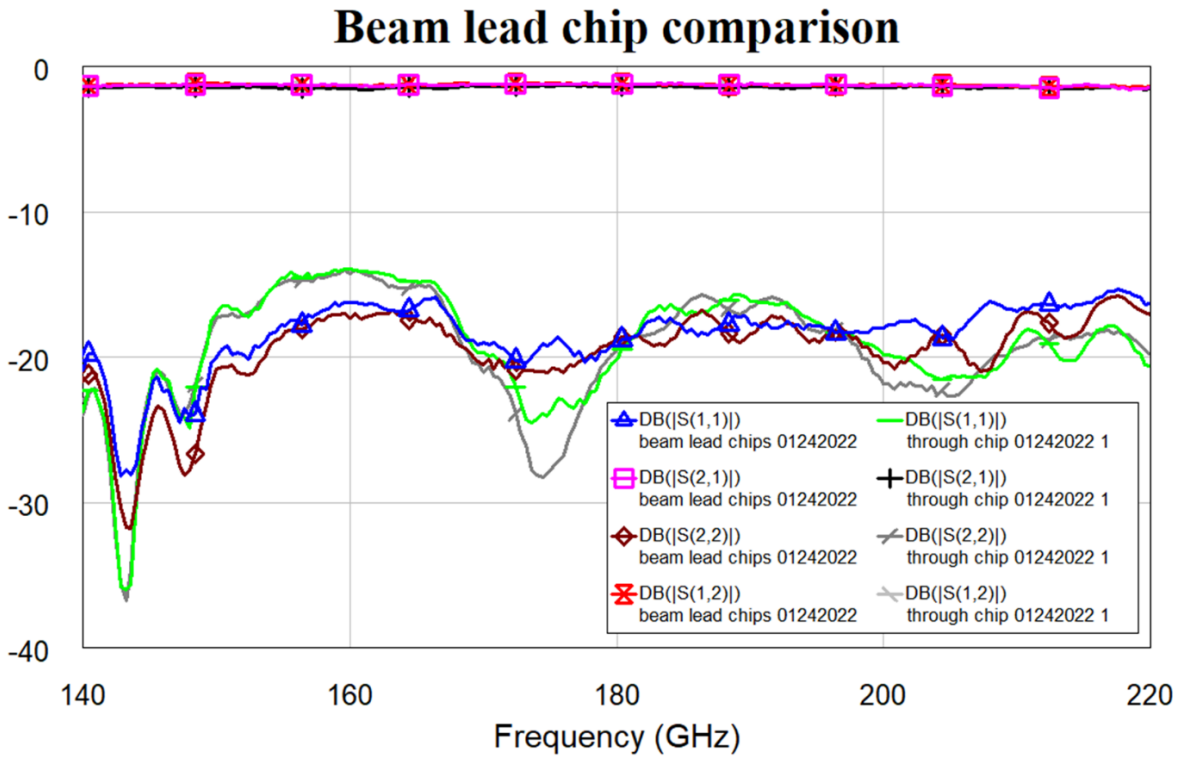


Figure 3.34:Through chip and beam lead chip measurement comparison.

The measured results of the beam lead chip exhibit a slightly superior performance compared to the through chip results. The loss factor of the beam lead chip is between 0.2 and 0.27 which is lower than through chip. This enhanced performance can be attributed to the beam lead chip's ability to withstand external forces without fracturing. After bonding the beam lead chips, the application of a needle was employed to compress the end of the chip and rectify any induced bending. As such, the degree of deformation experienced by the beam lead chip was minimized in comparison to that of the through chip.

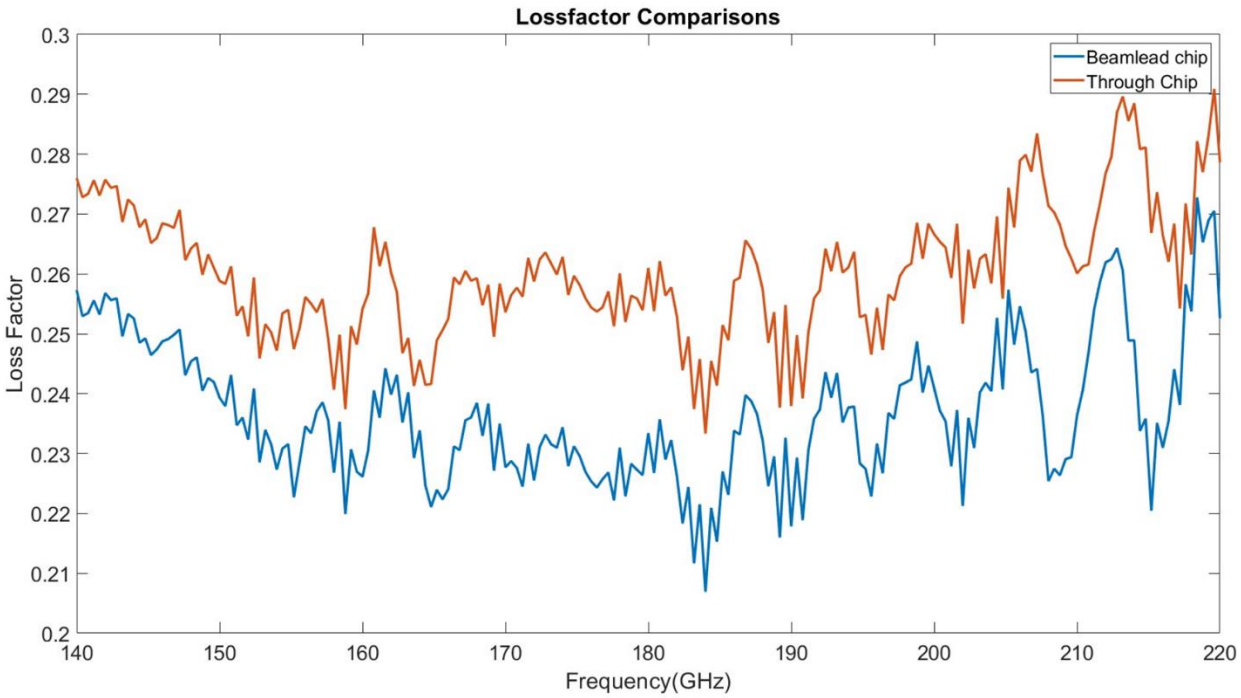


Figure 3.35:Lossfactor comparison of beam lead chip and through chip.

3.6 Electrical design review

This chapter offers an overview of the electrical design of the chip-to-chip interconnect chip, through chip, and beam lead chip prototypes. To enhance the efficacy of the design and enable the measurement of chip-to-chip interconnects, the design procedure commences with the waveguide housing and through chip.

The through chip design also helps verify the performance of the E-plane probe and waveguide housing design. The chip-to-chip interconnect design is derived from the through chip design, with certain modifications. Alternatively, the beam lead chip design presents an alternative chip-to-chip integration solution. The insertion loss in this design is lower than that of the chip-to-chip interconnect, while the return

loss is higher. However, it is not possible to disconnect the beam lead integration without risking damage to the gold pad. Therefore, the beam lead integration should be regarded as a non-detachable chip-to-chip connection.

Figure 3.36 compares return loss of through chip, chip-to-chip interconnect and beam lead chip measurements. Figure 3.37 shows the comparison of insertion loss of through chip, chip-to-chip interconnect, and beam lead chip measurements.

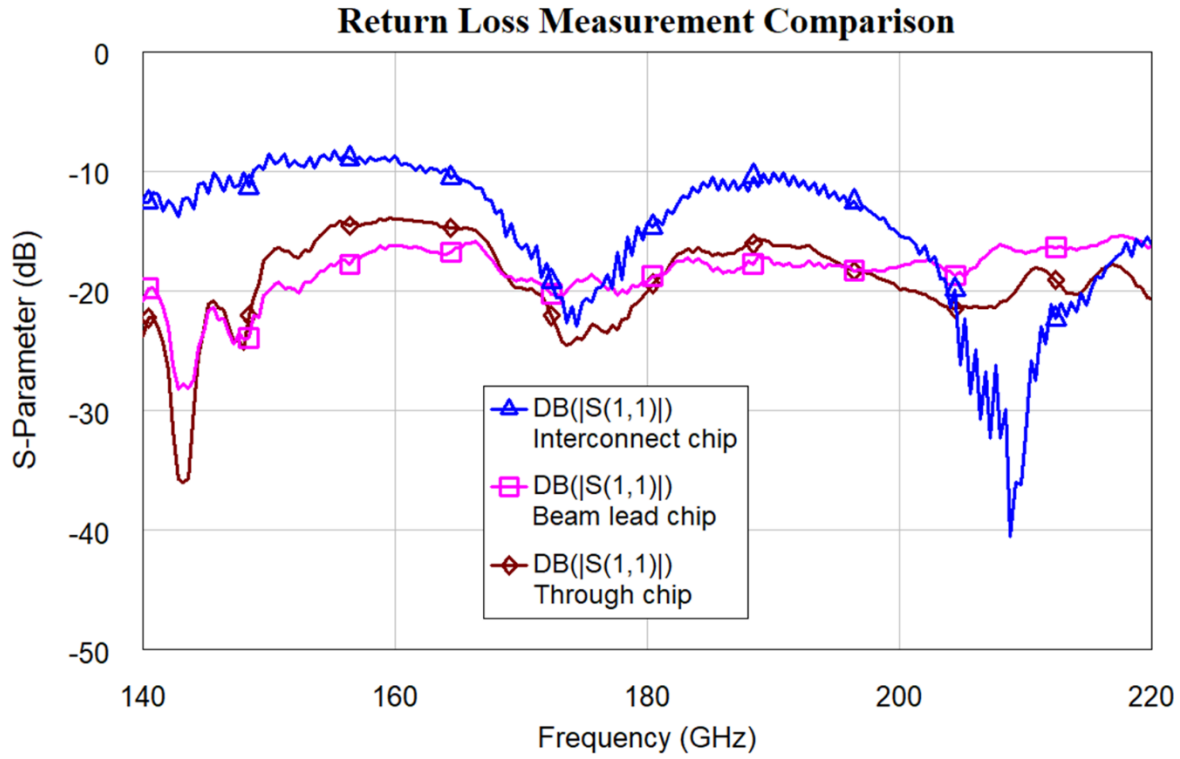


Figure 3.36:Insertion loss comparison of through chip, interconnect chip and beam lead chip.

The return loss measurements presented in Figure 3.36 indicate that the beam lead chip has a higher return loss than both the through chip and the interconnect chip. Additionally, the insertion loss measurements in Figure 3.37 show that the beam lead chip has a lower insertion loss than both the through chip and the interconnect chip. The loss factor of the interconnect chip, through chip, and beam lead chip are compared in Figure 3.38.

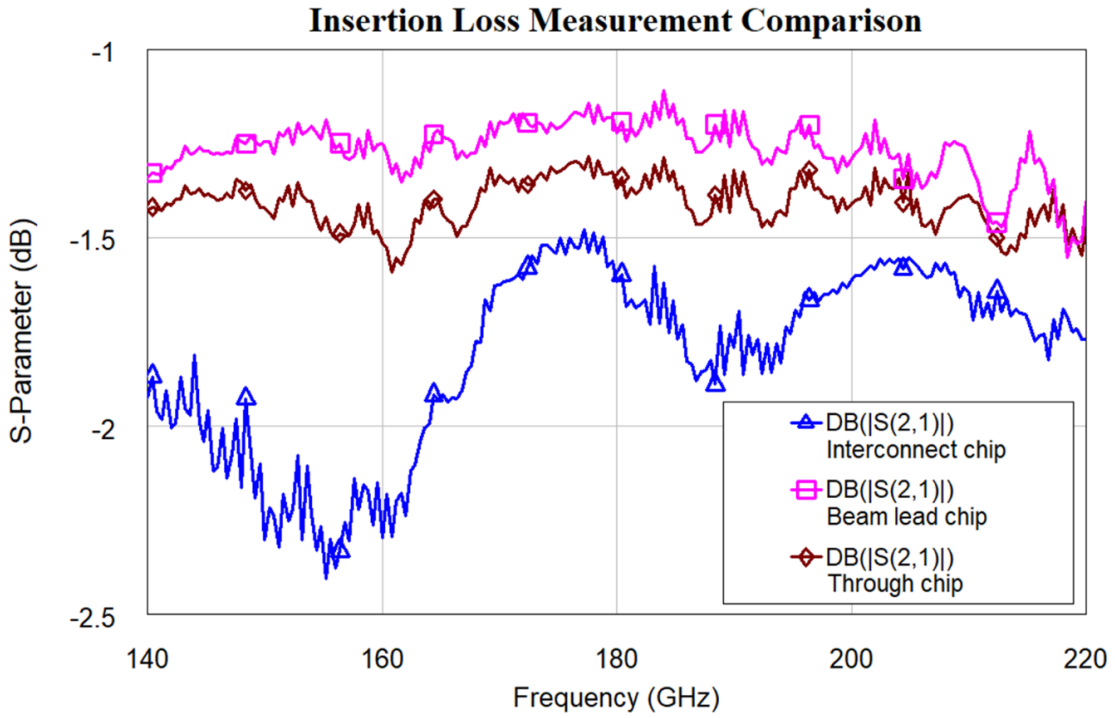


Figure 3.37:Return loos comparison of through chip, interconnect chip and beam lead chip.

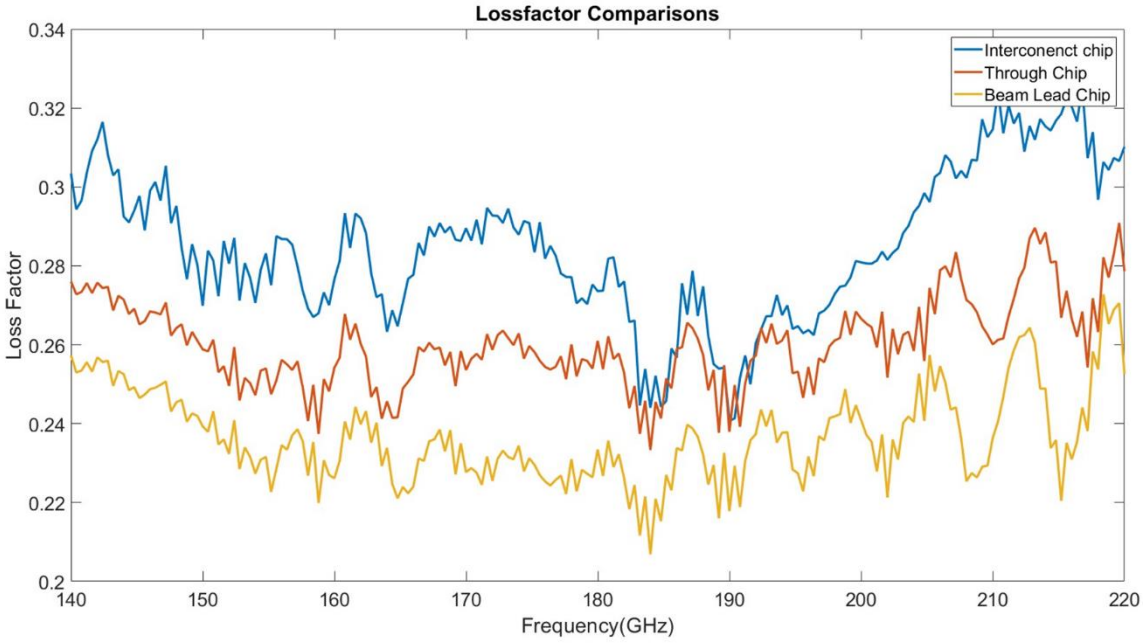


Figure 3.38:Interconnect chip, through chip and beam lead chip loss factor comparison.

In summary, this chapter presents the successful development of a detachable chip-to-chip interconnect that operates within the THz frequency range. The measured results demonstrate good return loss and low insertion loss, indicating a good electrical interface between the chips with low contact resistance. The design of this interconnect has the potential to be scaled to even higher frequencies, making it a promising solution for future THz-frequency compact detachable interconnects.

4 Conclusion and Future Work

4.1 Conclusion

This study presents a novel detachable chip-to-chip interconnect that operates within the frequency range of 140 GHz to 220 GHz. Our investigation involves comprehensive evaluations of both electrical and mechanical performance of the interconnect. Specifically, we place emphasis on S-parameter measurement as a metric for electrical performance, whereas we assess the assembly force, disassembly force, contact resistance, and lifetime of the interconnect for mechanical performance analysis. To the best of our knowledge, this work represents the first successful demonstration of such a detachable chip-to-chip interconnect in this frequency range.

4.1.1 Electrical Performance

This work has presented the design, simulation, and measurement of a detachable chip-to-chip interconnect operating from 140 to 220 GHz. The design uses a 15-μm thick silicon substrate and is based on a self-holding interference taper which provides a self-aligned mechanical contact with sufficient force to ensure a low contact resistance.

Chapter 3 provides an overview of the mode transmission in the interconnect chip, as well as an analysis of the current distribution on the through chip. The through chip serves as a means of understanding the impact of the E-plane probe and clamp structures, and we compare its performance with and without cut structures. Subsequently, we proceed to design the detachable interconnect based on the through chip, but with the middle section replaced by an interconnector. To address fabrication limitations and mitigate the effects of parasitic capacitance, we opt to flip one of the interconnect chips to reduce parasitic capacitance and prevent deformation of the nickel thin film.

The measured results demonstrate good return loss across the WR5.1 band and better than 10 dB from 165 to 220 GHz. The measured insertion loss is better than 2 dB across the band and no more than 0.5 dB higher than the through chip, indicating a good electrical interface between the chips with low contact resistance.

Future work will investigate the reliability of this design after repeated connections as well as improvements in the chip alignment within the channel. This chip-to-chip interconnect design may ultimately lead to a future THz-frequency compact detachable interconnect that can be scaled to 1 THz and beyond.

4.1.2 Mechanical Performance

The present study initiates the design of a detachable chip-to-chip interconnect, utilizing the uniformly socketed chip beams design. A stress analysis of the initial prototype is presented in Chapter 2, which indicates that the interconnect chips experience stress levels ranging from approximately 3 to 3.5 GPa, resulting in the failure of the socket interconnect beams. A considerable number of prototype chips, numbering in the hundreds, were tested; however, none of the chips were successfully assembled together. The assembly process was further complicated by frequent misalignments, which caused the breakdown of the socketed chips' beams. The images of the broken prototype socketed chips are presented in Figure 2.14.

Thus, we have adopted the Morse taper design as a point of reference and have introduced modifications to both the plug and socket chips, incorporating a non-prismatic beam structure. This structural adjustment has the added benefit of facilitating alignment of the interconnect chips during the assembly process. Additionally, we have implemented measures to reduce the deformation of the socket chip beam during assembly, thereby minimizing the stress experienced by the socket chip interconnect, lowering it to 3 GPa.

In order to gain a deeper understanding of the force required to assemble and disassemble the interconnect chips, we have made further modifications to the design. Specifically, we have developed DC chips that are specifically intended for DC measurement, as illustrated in Figure 2.23. We also figure out a setup to measure the assembly force, contact resistance and disassembly force for the DC interconnect chip.

Our findings indicate that the measured assembly force for a chip with a 3 μm offset is in excess of 120 mN, ultimately resulting in failure. This outcome suggests that the 3.5 GPa design surpasses the acceptable limit. We think in the future work, the 3 μm offset design can be eliminated and the highest stress on the socket chip should be controlled under 2.5 GPa or lower. Conversely, the measured assembly force for a 2

μm offset chip ranges from 90 mN to 70 mN. Furthermore, the measured assembly force for a 1 μm offset chip ranges from 80 mN to 60 mN.

Furthermore, we have conducted measurements to determine the contact resistance for both the 2 μm offset chip and 1 μm offset chip, without applying any additional force to the chip. Our results indicate that the measured contact resistance for the assembled chip is approximately 3 Ω. In theory, an additional resistance of 1 Ω in the interconnect chip can result in an increase of 0.1 dB in insertion loss. Remarkably, the measured contact resistance aligns with our measurements of the interconnect chips' insertion loss.

However, we observed that the measured insertion loss for the interconnect chip is approximately 0.1 to 0.2 dB higher than through-chip measurements.

Regarding the disassembly force measurement, our results indicate that for the 2 μm offset chip, a force of 70 mN to 80 mN is required to detach the interconnect chips. Similarly, for the 1 μm offset chips, disassembly forces range from 60 mN to 80 mN.

Our most recent measurements involved conducting lifetime tests on the interconnect chips. We were able to repeatedly assemble the 2 μm offset chip for more than 50 times and the 1 μm offset chip for over 100 times. Notably, our findings suggest that it is unnecessary to push the interconnect chip to its highest stress situation. During the lifetime measurement, we precisely controlled the assembly force below 70 mN for the 2 μm offset chip and 60 mN for the 1 μm offset chip.

In future designs, we believe that there will be a trade-off between the lifetime of the interconnect and the contact resistance.

4.2 Mechanical Measurement

In terms of future work related to mechanical design and measurement, several potential areas of improvement can be identified. First, to improve the accuracy of contact force and contact resistance measurements and prevent the nickel thin film from coming into contact with each other, it may be beneficial to flip the plug chip, as demonstrated in Figure 4.1.

Moreover, to enhance the accuracy of contact resistance measurements, it may be useful to establish a connection between the gold transmission line and the pads on the backside of the chip through the use of holes. Such modifications would likely simplify the measurement process and enable more accurate determination of contact resistance and contact force.

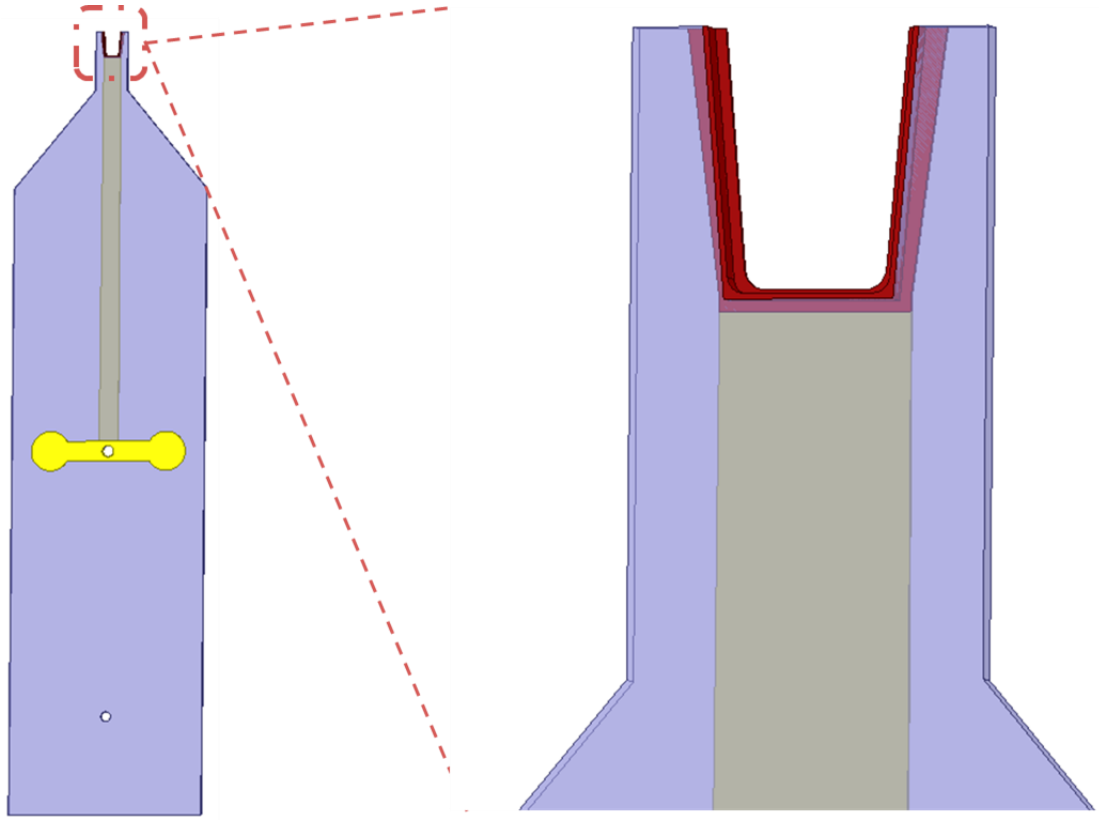


Figure 4.1: Modified interconnect DC socket chip.

The assembled interconnect DC chips would as Figure 4.2 shows. The gold transmission line on the socket chip connect to the front side pad through a gold plated via hole.

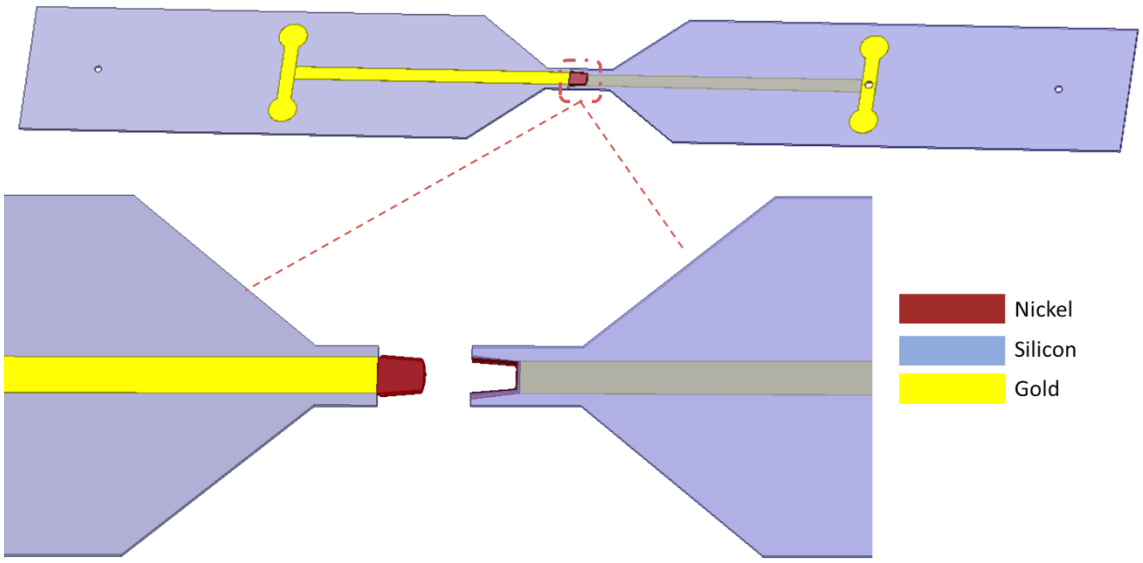


Figure 4.2:Modified DC chip with flipped assembly.

The current assembly process is heavily reliant on manual labor, which poses a significant risk of decreased success rate. To address this issue, we recommend implementing an automated measurement process, whereby the socket chip is connected to a load cell, and the plug chip is connected to a motor equipped with displacement value feedback. Our experience with motors indicates that they need to move smoothly and gently. However, the use of a motorized plug chip may give rise to the problem of chip misalignment and alignment wafer crashing, which we have encountered on several occasions, leading to chip breakage.

Furthermore, the present approach utilized for quantifying the disassembly force of the joined interconnect involves landing and pushing the force, followed by lifting the needle after the assembly process is completed. The lifting of the needle helps to reset the load cell spring to null, after which the probe is landed again and pulled.

However, the needle lift process may induce undesirable vibrations on the chip, which could significantly affect the accuracy of the measured results. Additionally, this process increases the risk of chip breakage, which is not desirable. Therefore, we propose a potential solution to this issue, which involves attaching an electromagnet to the tool used to handle the plug chip. Instead of lifting the needle, we can detach the plug chip and motor by turning off the power to the electromagnet. In implementing this solution, careful consideration must be given to selecting the appropriate size of the magnetic material to ensure it is not too

heavy and does not affect the spring in the load cell, which returns to null after the assembly force measurement is completed. The modified assembly and disassembly force measurement set is like Figure 4.3 shows. We think the electromagnet should be under the 3D-printed tool so it can provide the vertical support to the 3D-printed tool otherwise the tool would fall down and tilt the interconnect chip.

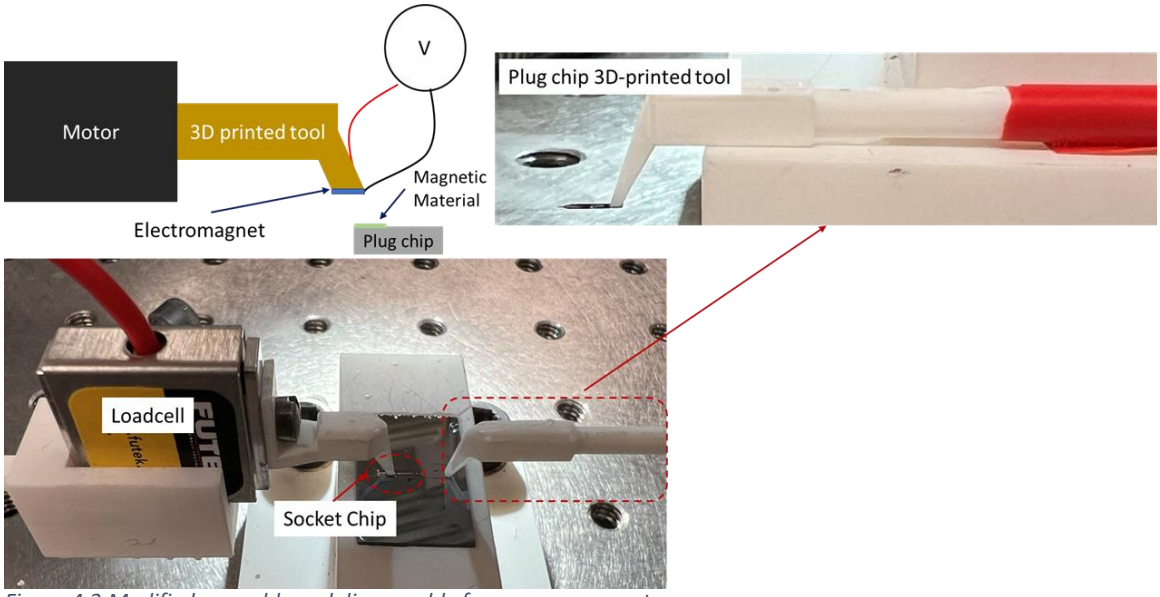


Figure 4.3:Modified assembly and disassembly force measurement.

4.3 Electrical Measurement

4.3.1 Clamp Structure Modification

In terms of electrical measurements, there is room for improvement, particularly with regards to the clamp structure used to secure the interconnect chips within the aluminum waveguide. The current clamp structure is fragile and susceptible to damage during the assembly process. Particularly during the insertion of assembled interconnect chips into the aluminum waveguide, the gap between the clamp structures and waveguide housing is only 5 μm, making it difficult to observe under the microscope. Even a slight misalignment between the interconnect chips and waveguide housing can result in broken clamps and inaccurate measurements. The broken clamps inside the waveguide housing, occurring during the assembly process and after measurements, are shown in Figure 4.4. Our observations indicate that more than 50% of assembly failures are caused by clamp breaks.

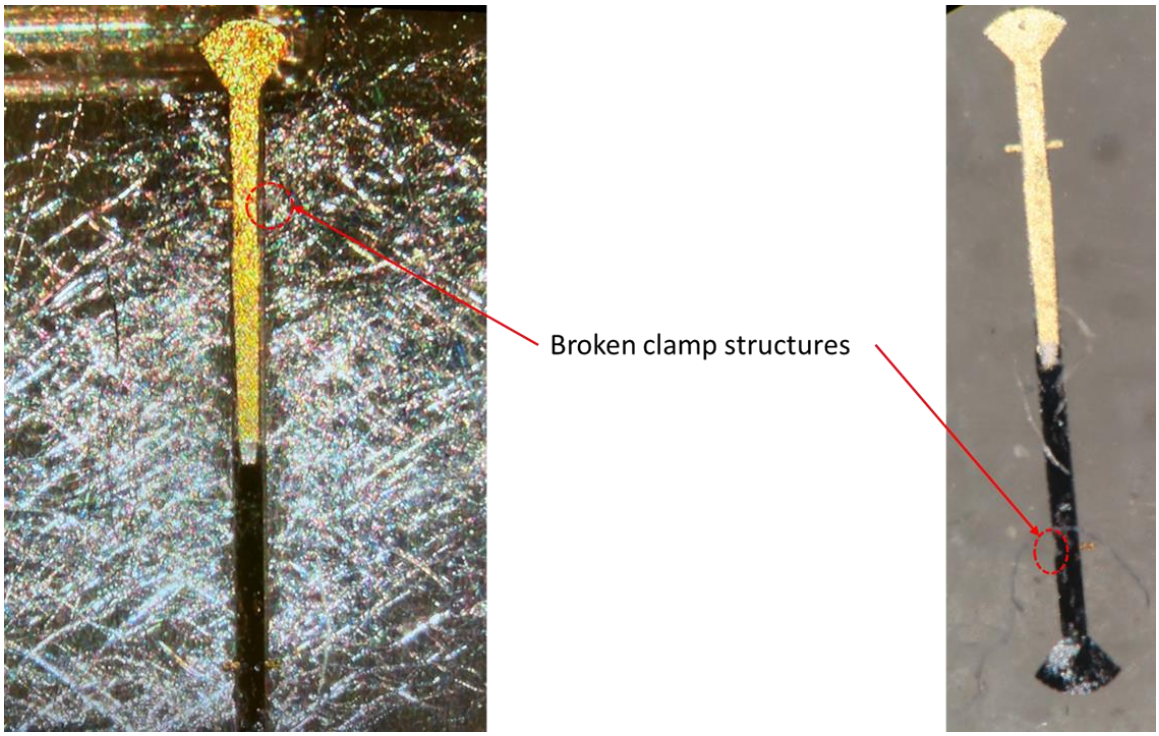


Figure 4.4:Images of broken clamp structures during assembly process.

A prospective approach towards addressing the issue of fragile clamp structures is to substitute them with beam leads made of gold or nickel, which possess a thickness of approximately 2 μm and are tightly

integrated into the walls of the aluminum waveguide. Nonetheless, such a modification may necessitate alterations to the cut structure as well.

4.3.2 Silicon Chip Bending

The through chip utilized in the measurement has a silicon substrate of dimensions 4.2 mm in length, 165 μm in width, and 15 μm in thickness, with a 4.1 mm long gold plating deposited on top of the substrate. As a result of the cohesive forces of the gold plating, the silicon substrate experiences bending, causing the through chip to tilt up to 75 μm on both sides. This bending effect was observed in Figure 3.26 of Chapter 3, resulting in a decrease of approximately 5 dB in return loss between 140 to 220 GHz. To overcome this issue, we propose plating gold on the backside of the silicon substrate, which is anticipated to effectively address the bending problem. Figure 4.5 shows the through chip with back side gold plating for overcoming the bending problem.

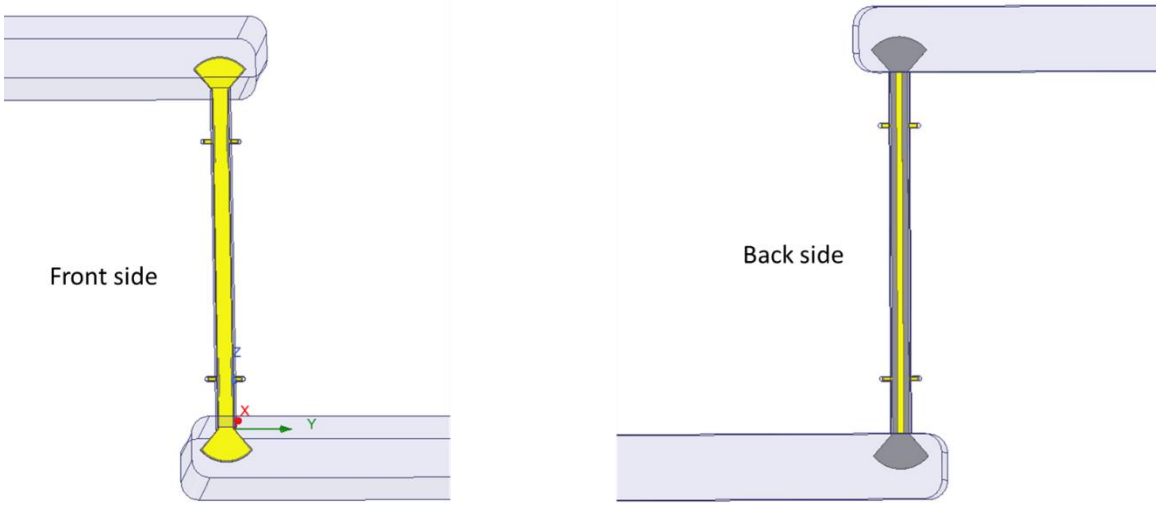


Figure 4.5:Back side gold plating for bending overcome.

The S-parameter of the through chip with back side gold plating is illustrated in Figure 4.6. Although some modifications may be required in terms of the position of the clamp gold and wire width to improve impedance matching, the impact on insertion loss and return loss is not considerable. The back side gold plating reduces the return loss by 3 dB from 150 to 160 GHz; nonetheless, the overall return loss remains higher than 18 dB from 140 to 220 GHz.

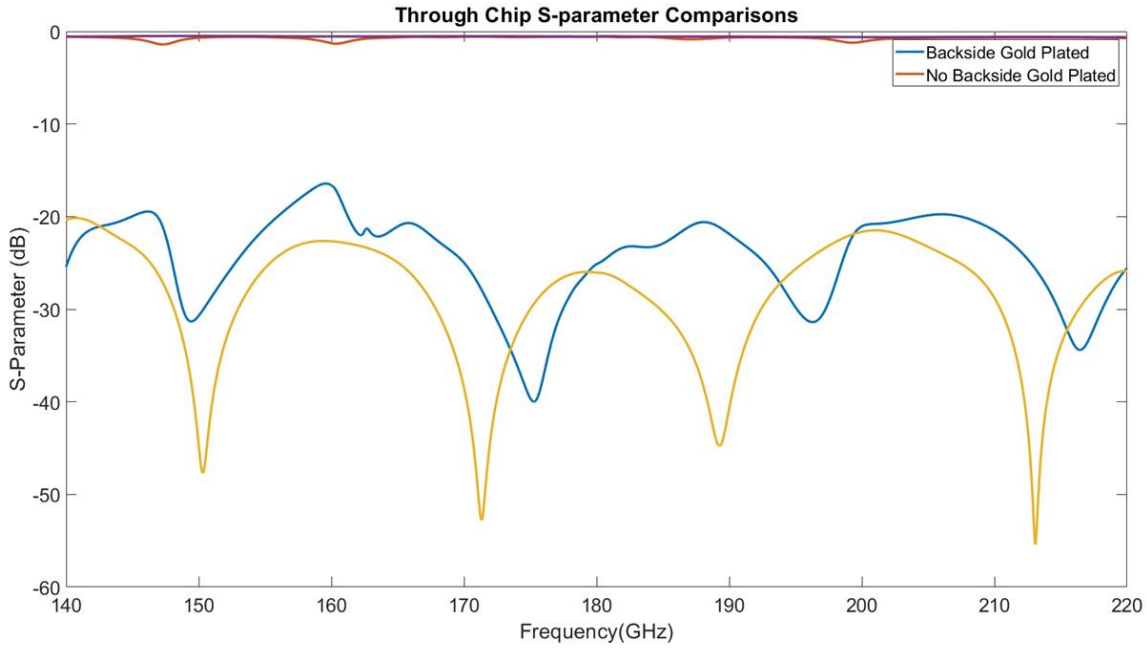


Figure 4.6:Through chip simulation comparison.

4.3.3 Interconnect chip electrical repeatedly measurement

Our research team is interested in exploring the potential for repeated electrical measurements on the RF chip we have designed. However, once the chip is assembled, it becomes difficult to separate it. This is partly due to the fact that there is no designated area on the assembled chip for the needle probe to land on and pull the chips apart.

Based on the simulation results presented in Chapter 3, Figure 3.5, the current flow at the edge of the E-plane probe and gold transmission line, which allows for modifications to be made at the center of the E-plane probe without negatively impacting the performance of the interconnect chips. With this in mind, our research team proposes a solution for repeated electrical measurements. Figure 4.7 illustrates our approach, which involves adding two via holes to the E-plane probes on either side of the chip. The via hole located in the middle of the E-plane probe allows the needle probe to be inserted and disassemble the joined chips. By doing so, we can accurately measure the insertion loss and return loss of the assembled interconnect chip after multiple assembly and disassembly cycles.

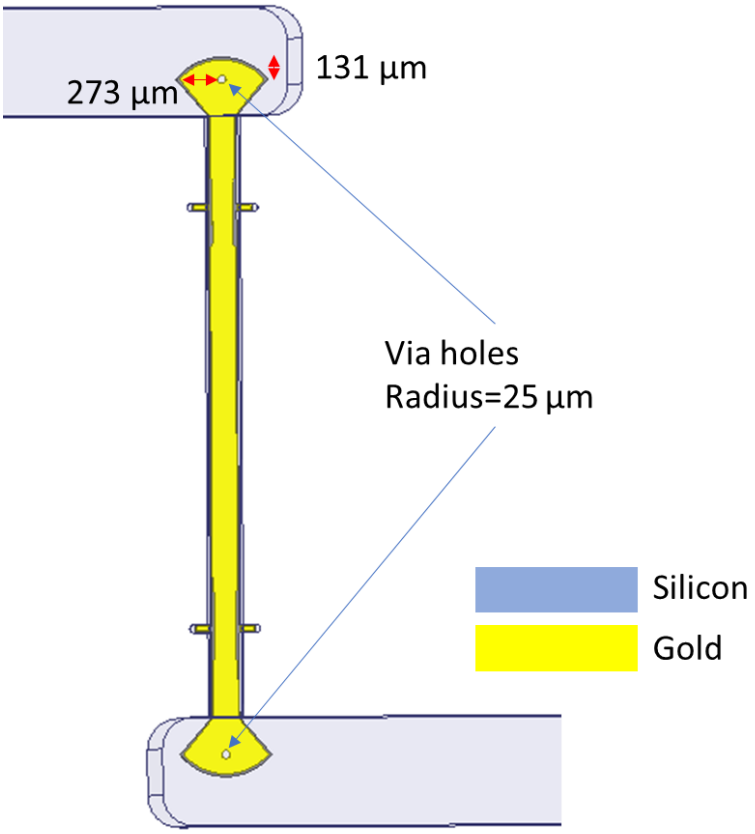


Figure 4.7:Through chip with via holes on the E-plane probes.

The presented design modification, as illustrated in Figure 4.7, incorporates via holes in the E-plane probes with a radius of 25 µm. This size is slightly larger than the radius of the needle probe, but it allows for easier operation under the microscope. The impact of this modification on the performance of the through chip was evaluated using HFSS simulation, and the results are shown in Figure 4.8. The simulation indicates that the insertion loss changes by less than 0.05 dB from 140 to 220 GHz, and the return loss slightly decreases by approximately 1 dB in the same frequency range. However, the simulation results suggest that the effect of the via holes on the chip's performance is not significant.

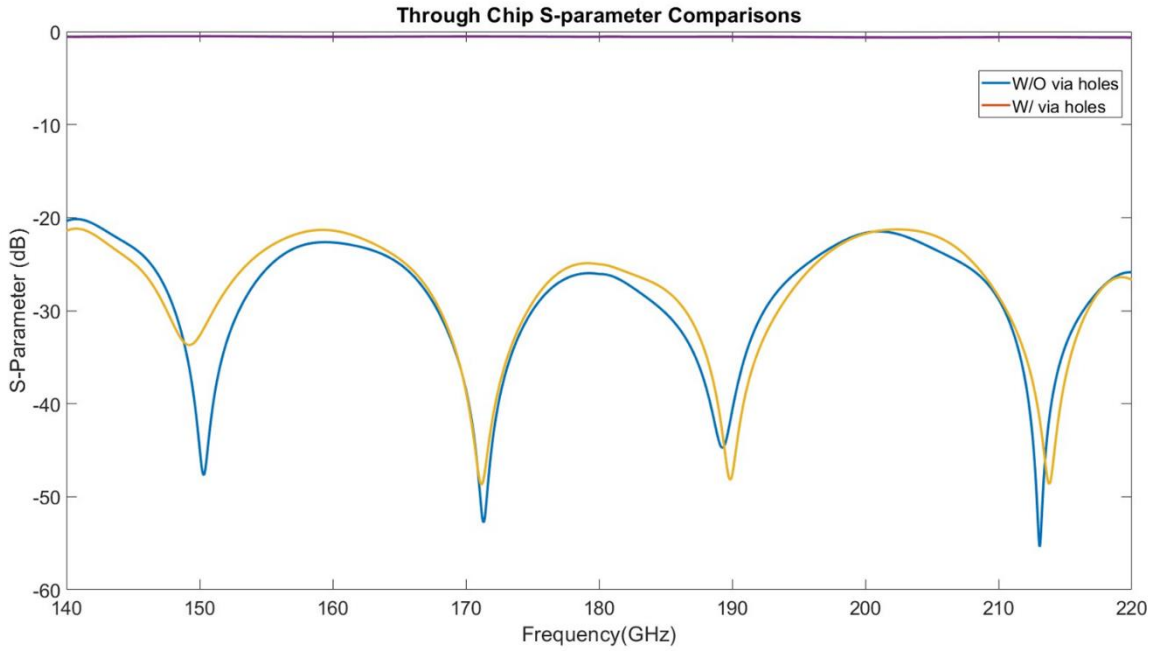


Figure 4.8:Simulation comparison of through chip with and without via holes.

4.3.4 Coplanar Waveguide Chip-to-chip Interconnect

Our current interconnect design draws inspiration from the micromachine probe design [ref], which suspends the interconnect inside the RF channel as a coaxial line. However, the coaxial mode requires a metal waveguide as the ground plane, limiting the design of the interconnect chip. Therefore, we propose a coplanar waveguide (CPW) mode interconnect as an alternative. The CPW mode design involves three interconnects as ground, signal, and ground. The advantages of the CPW mode design include the elimination of clamp structures and E-plane probes, as well as the ability to complete both electrical and mechanical measurements on a single chip. In the long run, this design can accommodate more devices and ICs to achieve the integration of the Terahertz communication system chip, as illustrated in Figure 4.9.

This work presents a novel approach for chip-to-chip integration solutions, which can be utilized in combination with various other devices, such as power amplifiers made of GaAs or antenna arrays. The proposed solution offers a unique means for integrating RF ICs with other devices, and holds potential for a wide range of applications in the field of chip integration.

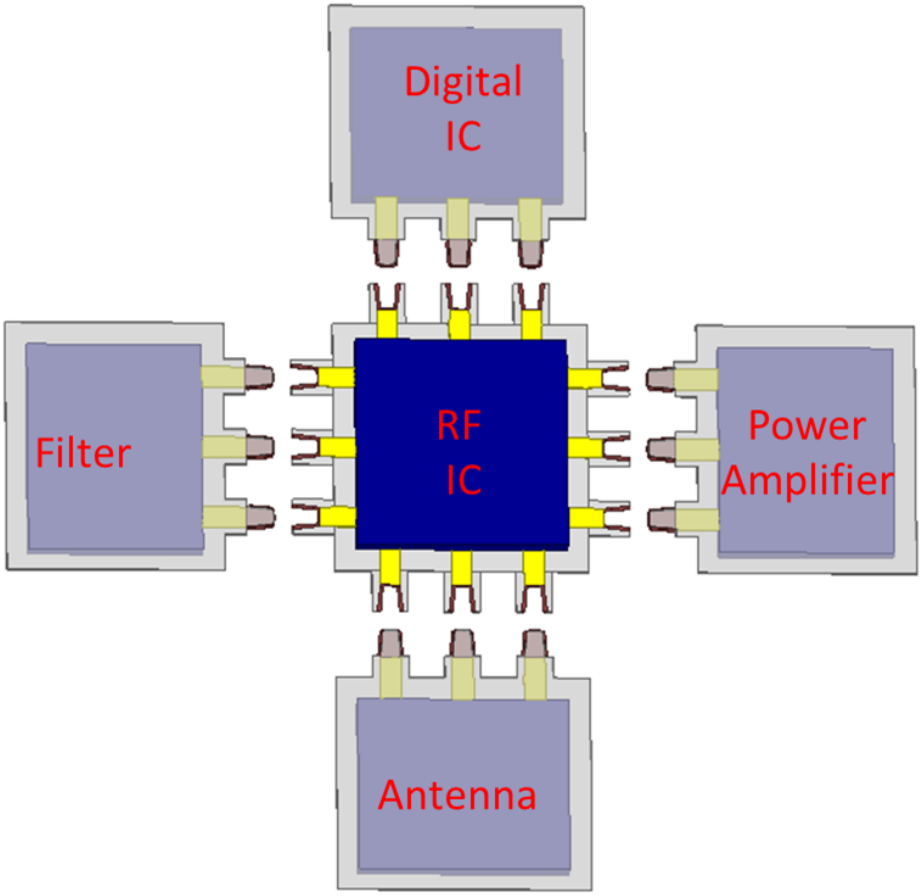


Figure 4.9: Chip-to-chip interconnect on CPW mode and system concept.

The present study displays simulation outcomes for a coplanar waveguide (CPW) configuration with a separable interconnect, as depicted in Figure 4.10. The simulation focused on a 2 mm segment located at the midpoint of the waveguide, and the resulting data is represented in Figure 4.11. The findings demonstrate that the return loss is greater than 10 dB, and the insertion loss is less than 2 dB across the frequency range of 140 GHz to 220 GHz.

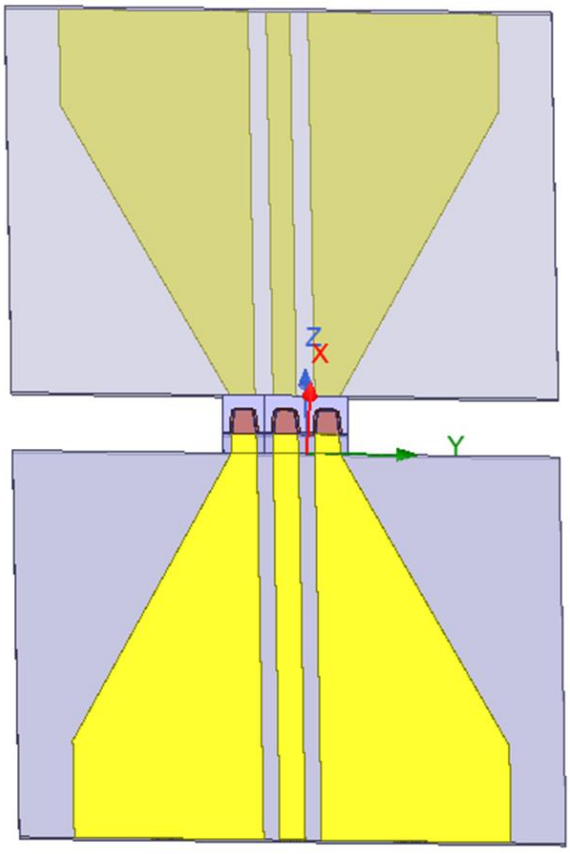


Figure 4.10:CPW line with detachable interconnect.

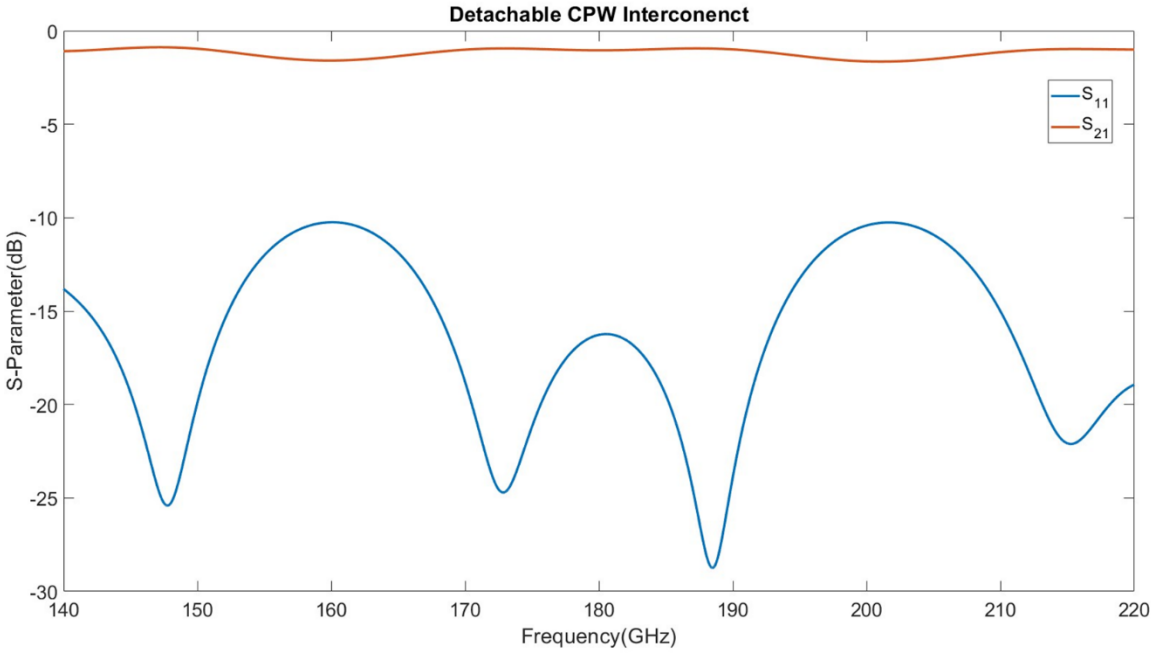
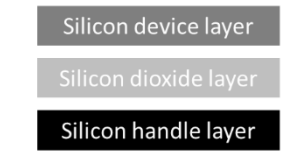


Figure 4.11: Simulation results of CPW line with interconnect.

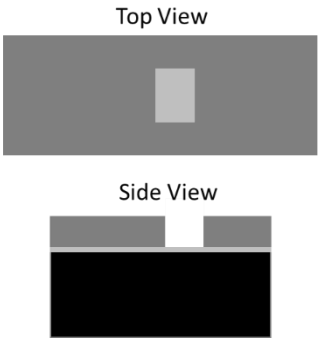
Appendix

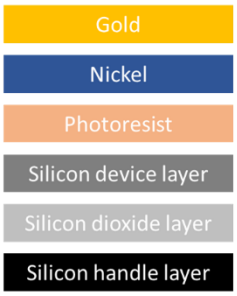
A. Fabrication Process



Mask 1: Via hole etch

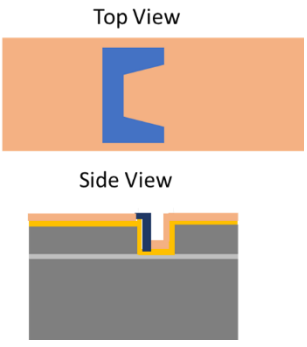
1. Clear Pattern Mask
2. Spin positive photoresist
3. Photolithography patterned (Interconnects outline)
4. Deep reactive ion etching (DRIE) silicon device layer to SiO2 handle layer (15µm)
5. Strip photoresist
6. Ti/Au/Ti seed layer sputtering





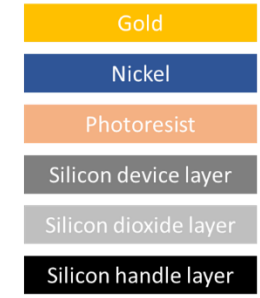
Mask 2: Nickel plating

1. Spin positive photoresist
2. Photolithography patterned (*Nickel pattern outline*)
   Double developed to fully develop the photoresist in the vias
3. Nickel electroplate for 2 µm (*strike under room temperature for 1 min before plate*)
4. Strip photoresist
5. Ti seed layer clean. (Ion etch)
   Ti DRIE will cause seed layer under cut for nickel coating.



Mask 3: Gold plating

1. Spin positive photoresist
2. Photolithography patterned (*Gold transmission line pattern outline*)
3. Gold electroplate for 2 µm
4. Strip photoresist
5. Au seed layer and Ti seed layer clean. (wet etch)
   Buffered oxide etch (BOE) remove the Ti seed layer immediately after Au layer remove

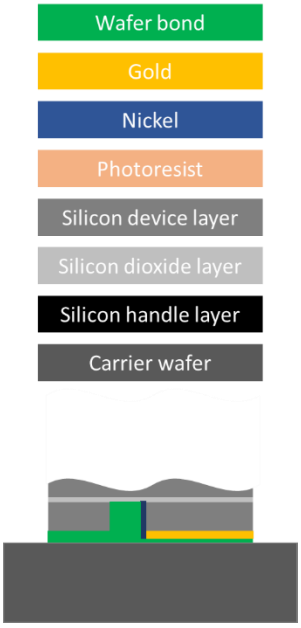


Top View

Side View

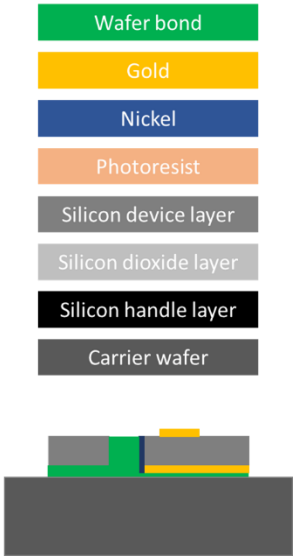
Flip Bond

1. Flip chip bond the SOI wafer on another carrier wafer
2. Remove silicon handle layer
   First diced the handle layer with the hubless saw then silicon DRIE etch
3. Remove silicon dioxide layer with *Buffered oxide etch (BOE)*
4. Backside Ti/Au seed layer sputter.



Mask 4: Backside gold plating

1. Spin positive photoresist
2. Photolithography patterned (*Gold backside pattern*)
3. Gold electroplate for 2 µm
4. Strip photoresist
5. Au seed layer and Ti seed layer clean. (wet etch)
   Buffered oxide etch (BOE) remove the Ti seed layer immediately after Au layer remove
6. Chip lease



B. Fabrication Notes

The fabrication process employed in this study was adapted from the methodology developed by Dr. Zhang [51]. Our approach, however, distinguishes itself through the inclusion of nickel plating. Specifically, the nickel plating applied to the interconnector side wall represents a pivotal step in our fabrication process.

In our fabrication process, the definition of the interconnector outline was achieved through the use of deep reactive ion etching (DRIE), as outlined in Mask 1. Notably, the device layer used in this process has a thickness of 15 μm. One significant challenge encountered during our approach pertained to the electroplating of nickel onto the 15 μm high side wall of the interconnector. Overcoming this obstacle was a key focus of our investigation.

To facilitate the electroplating of nickel onto the interconnector, a Ti/Au/Ti seed-layer was employed in our process. Notably, during the prototype interconnector process, a Ti/Au seed-layer was utilized in lieu of the aforementioned seed-layer.

Figure B.1 illustrates that the electroplating of nickel onto a gold seed-layer results in poor nickel quality. Additionally, it was observed that during the plating of the plug interconnect, only a portion of the interconnector head was successfully plated, with nickel accumulating primarily at the edge of the via hole.

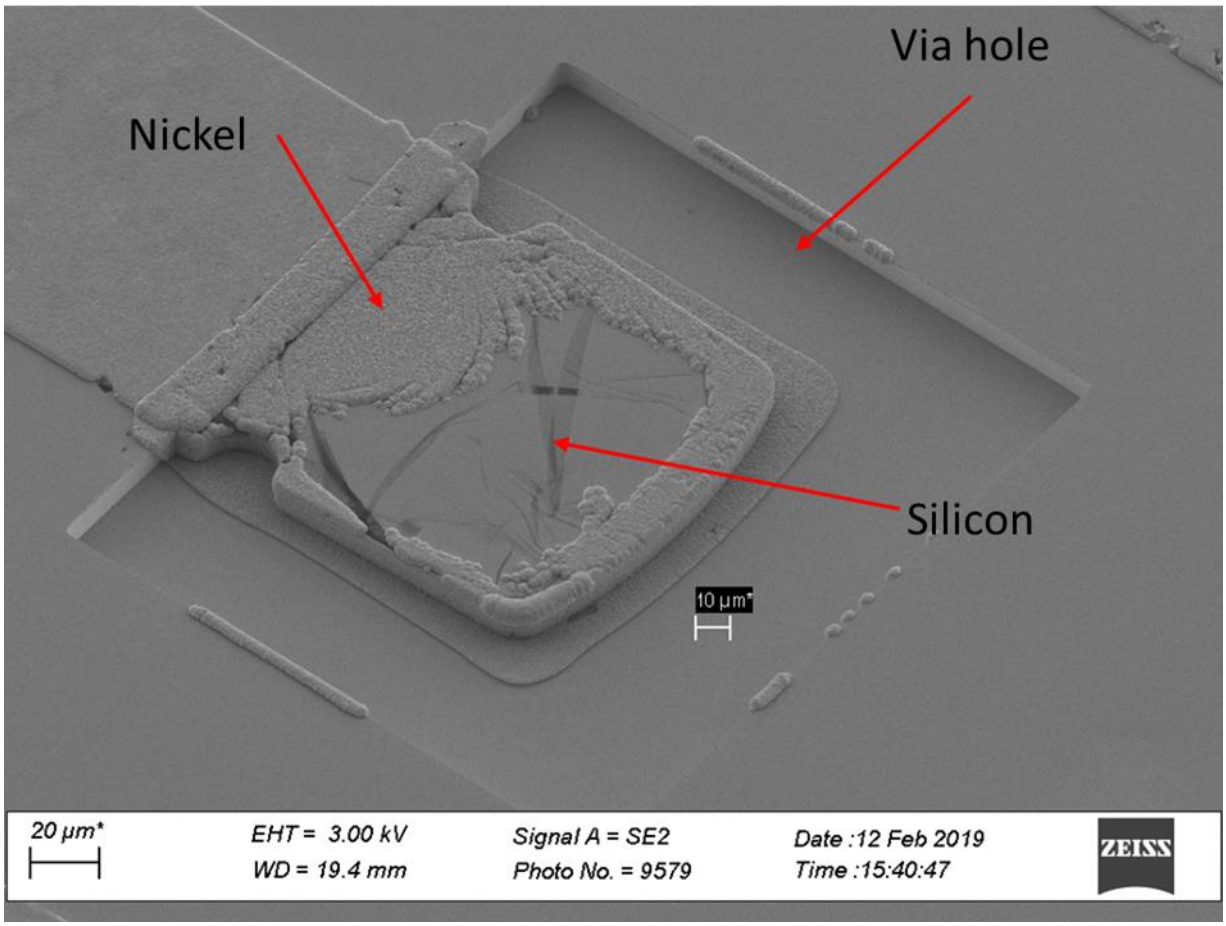


Figure B. 1: Nickel electroplated on Ti/Au Seed-layer.

Upon transitioning from a Ti/Au seed-layer to a Ti/Au/Ti seed-layer, a marked improvement in the quality of the nickel electroplating was observed. This is depicted in Figure B.2, which illustrates the nickel plating quality achieved using the Ti/Au/Ti seed-layer.

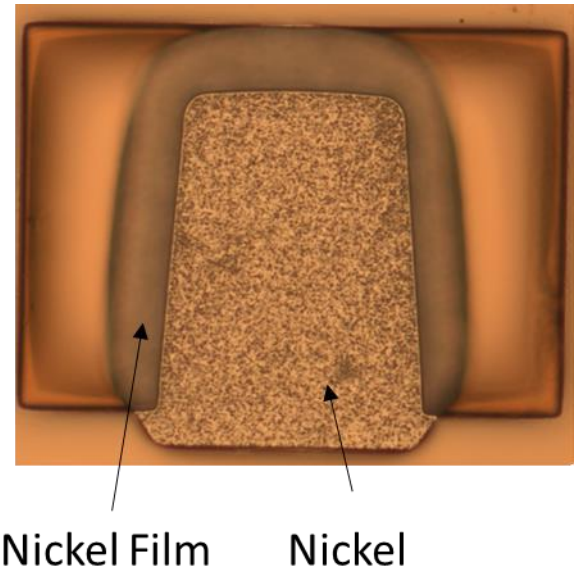


Figure B. 2:Nickel electroplated on Ti/Au/Ti Seed-layer.

Following the determination of the appropriate seed-layer for the nickel electroplating process, the next step involved photoresist lithography. However, during the photoresist spinning process, the photoresist was observed to accumulate inside the via hole and along the side wall. As a result, exposing the photoresist in these areas, particularly in proximity to the side wall, emerged as a crucial aspect of the nickel plating photo lithography process.

To ensure the complete removal of the photoresist inside the via hole and side wall, a multiple-step photolithography process was employed. Typically, three to four cycles of this process were required to fully remove the photoresist from within the via hole. Figure B.3 provides a visual representation of this process.

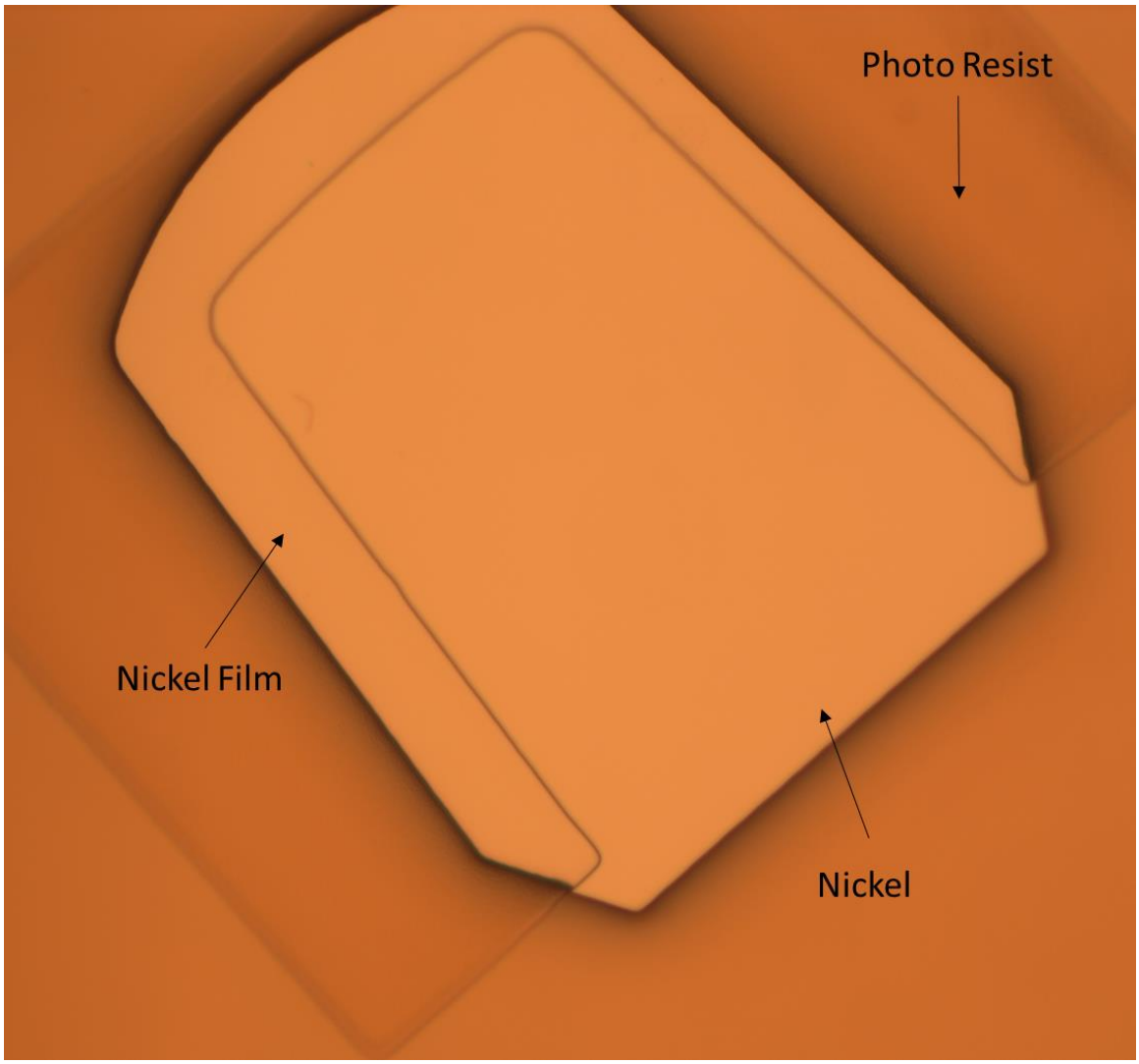


Figure B. 3:Photolithography of AZ-4330 in Via hole.

Upon completion of the nickel and gold electroplating process, it is necessary to remove the gold (Au) seed-layer and titanium (Ti) seed-layer. We recommend using ion etching to remove the Au film, in order to prevent the Ti seed-layer from undercutting beneath the nickel layer. This is critical, as the Au seed-layer undercutting can result in the nickel coating being peeled off under high stress.

The removal of the Au seed-layer can be achieved using HG-400 or Ar (Argon) RIE. However, it should be noted that HG-400 may attack the Au seed-layer underneath the nickel coating, resulting in easy peeling of the nickel coating, as shown in Figure B.4. Therefore, we recommend using Ar RIE etch for the removal of the Au seed-layer. The Ar RIE etch receipt is provided as follows:

RIE 140 W, Ar 50 SCCM, 10 mTorr, 10 C for around 5 min

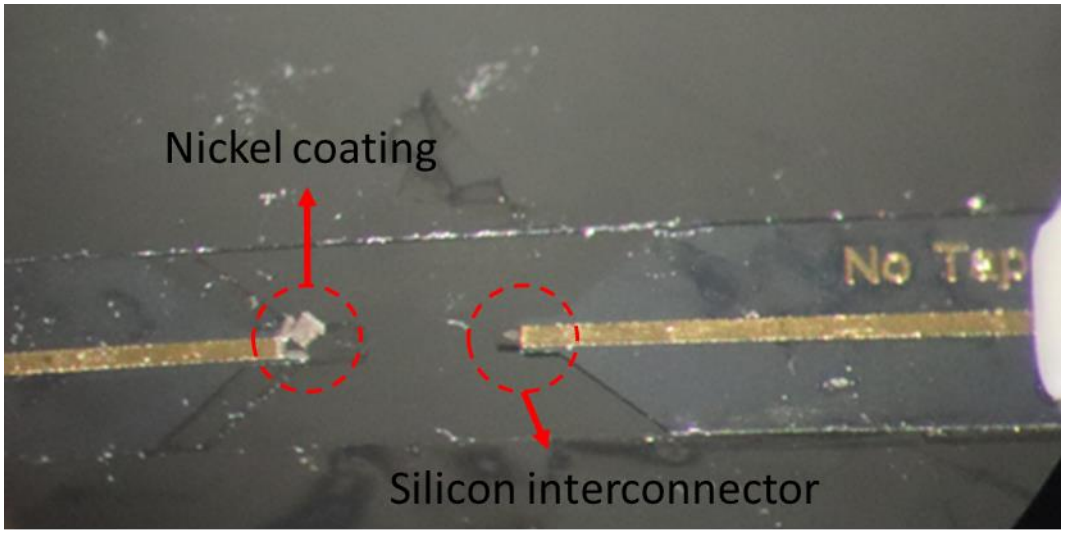
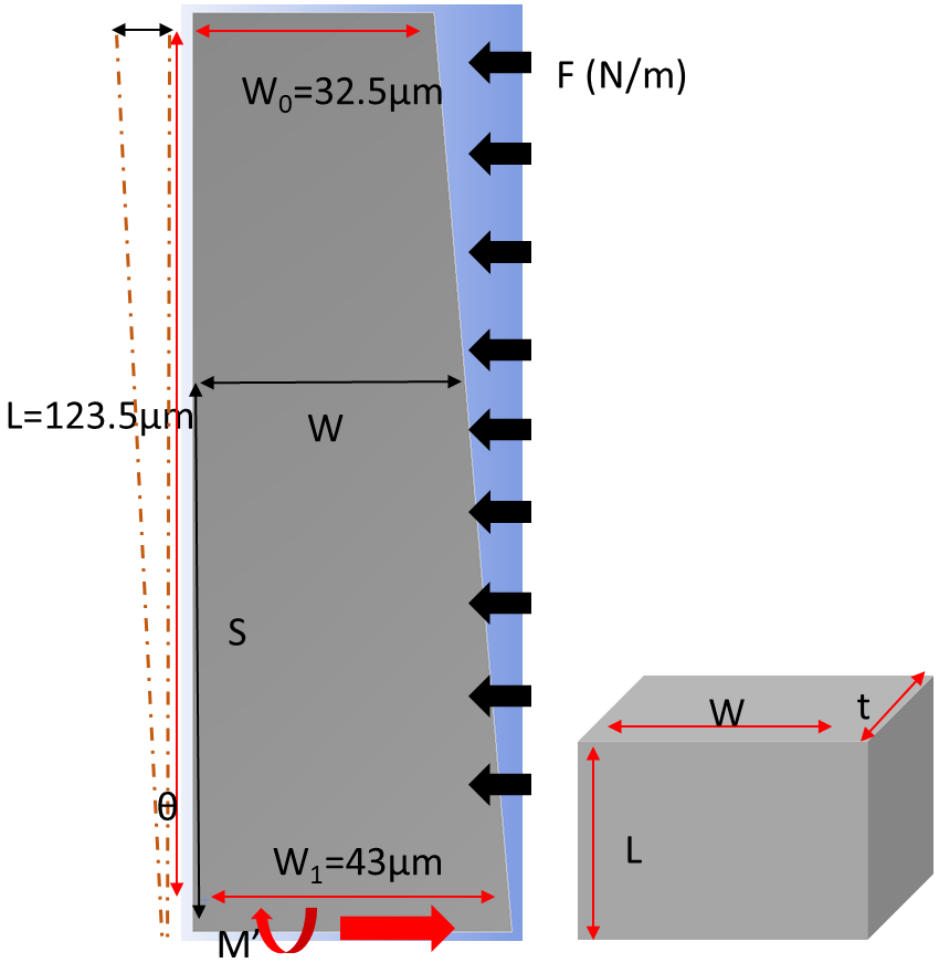


Figure B. 4: Nickel coating peeled off during assembly process.

C. Detachable Interconnect Load, Stress and Deformation Model

i. Formula Derivation



$$\frac{d^2\delta}{ds^2} = \frac{M(s)}{EI} = \frac{FLS - \frac{1}{2}FL^2 - \frac{1}{2}FS^2}{E \times \frac{1}{12} \times t \times (W_1 - \frac{W_1 - W_0}{L} \times S)^3}$$

$$\frac{d\delta}{ds} = \int \frac{FLS - \frac{1}{2}FL^2 - \frac{1}{2}FS^2}{E \times \frac{1}{12} \times t \times (W_1 - \frac{W_1 - W_0}{L} \times S)^3} ds$$

$$\delta = \iint \frac{FLS - \frac{1}{2}FL^2 - \frac{1}{2}FS^2}{E \times \frac{1}{12} \times t \times (W_1 - \frac{W_1 - W_0}{L} \times S)^3} \mathrm{d}S^2$$

$$F = 400x^{-0.2} - 5 \times 10^{-9}x^4 + 100x^{0.3} - x + 280$$

Boundary Condition:

$\frac{d\delta}{dS} = 0(@S = 0)\ ; \delta = 0(@S = 0)$

$\frac{d\delta}{ds}$=$\int \frac{FLS}{E\times\frac{1}{12}\times t\times(W_1-\frac{W_1-W_0}{L}\times S)^3}ds$-$\int \frac{\frac{1}{2}FL^2}{E\times\frac{1}{12}\times t\times(W_1-\frac{W_1-W_0}{L}\times S)^3}ds$-$\int \frac{\frac{1}{2}Fs^2}{E\times\frac{1}{12}\times t\times(W_1-\frac{W_1-W_0}{L}\times S)^3}ds$

$\rightarrow \frac{d\delta}{ds} = \int \frac{\left(400s^{-0.2}-5\times10^{-9}s^4+100s^{0.3}-s+280\right)Ls}{E\times\frac{1}{12}\times t\times\left(W_1-\frac{W_1-W_0}{L}\times S\right)^3}ds$-$\int \frac{0.5L\left(400s^{-0.2}-5\times10^{-9}s^4+100s^{0.3}-s+280\right)^2}{E\times\frac{1}{12}\times t\times\left(W_1-\frac{W_1-W_0}{L}\times S\right)^3}ds$

-$\int \frac{\left(400s^{-0.2}-5\times10^{-9}s^4+100s^{0.3}-s+280\right)s^2}{E\times\frac{1}{12}\times t\times\left(W_1-\frac{W_1-W_0}{L}\times S\right)^3}ds$

$\int \frac{\left(400s^{-0.2}-5\times10^{-9}s^4+100s^{0.3}-s+280\right)s^2}{E\times\frac{1}{12}\times t\times\left(W_1-\frac{W_1-W_0}{L}\times S\right)^3}ds$=$(L\ (-455606./(0.000505762\ -\ x)\ +\ 115.214/$
$(0.000505762\ -\ x)\text{^}2\ -\ 4.89325\times10\text{^}11\ x\text{^}1.3\ 2F1(1.3,2,2.3,1977.21\ x)\ +\ 4.89325\times$
$10\text{^}11\ x\text{^}1.3\ 2F1(1.3,3,2.3,1977.21\ x)\ -\ 3.18061\times10\text{^}12\ x\text{^}0.8\ 2F1(0.8,2,1.8,1977.21\ x)\ +$
$3.18061\times10\text{^}12\ x\text{^}0.8\ 2F1(0.8,3,1.8,1977.21\ x)\ +\ 2.71195\times10\text{^}-6\ x\text{^}3\ +\ 6.17221\times10\text{^}-$
$9\ x\text{^}2\ +\ 1.24867\times10\text{^}-11\ x\ +\ 1627.17\ log(10621\ -\ 2.1\times10\text{^}7\ x)))/200000\ +\ constant$

-$\int \frac{\frac{1}{2}FL^2}{E\times\frac{1}{12}\times t\times(W_1-\frac{W_1-W_0}{L}\times S)^3}ds$= -(0.5 L^2 (400/x^0.2 - 5×10^(-9) x^4 + 100 x^0.3 - x + 280))/(2×10^5 (43×10^(-6) - (21 x)/247)^3) dx = -1.88365×10^11 L^2 ((3.02343×10^-12)/(0.000505762 - x)^2 + 0.0128408 x^1.3 2F1(1.3, 3, 2.3, 1977.21 x) + 0.0834649 x^0.8 2F1(0.8, 3, 1.8, 1977.21 x) - 1.6693×10^-13 x^5 2F1(3, 5, 6, 1977.21 x) - (0.0000834649 x^2)/(1 - 1977.21 x)^2) + constant

$-\int \frac{\left(400s^{-0.2}-5\times10^{-9}s^4+100s^{0.3}-s+280\right)s^2}{E\times\frac{1}{12}\times t\times\left(W_1-\frac{W_1-W_0}{L}\times S\right)^3}ds$= (400/x^0.2 - 5×10^(-9) x^4 + 100 x^0.3 - x + 280) x^2)/(2×10^5 (43×10^(-6) - (21 x)/247)^3) dx = -(2.91355×10^-7)/(0.000505762 - x)^2 - 1237.41 x^1.3 2F1(1, 1.3, 2.3, 1977.21 x) + 2474.82 x^1.3 2F1(1.3, 2, 2.3, 1977.21 x) - 1237.41 x^1.3 2F1(1.3, 3, 2.3, 1977.21 x) - 8043.16 x^0.8 2F1(0.8, 1, 1.8, 1977.21 x) + 16086.3 x^0.8 2F1(0.8, 2, 1.8, 1977.21 x) - 8043.16 x^0.8 2F1(0.8, 3, 1.8, 1977.21 x) - 1.01698×10^-11 x^4 - 2.0574×10^-14 x^3 - 3.12167×10^-17 x^2 - 0.00813585 x - 0.00230428/(x - 0.000505762) + 2.27803 log(10621 - 2.1×10^7 x) + constant

$\int\int \frac{\left(400s^{-0.2}-5\times10^{-9}s^4+100s^{0.3}-s+280\right)s^2}{E\times\frac{1}{12}\times t\times\left(W_1-\frac{W_1-W_0}{L}\times S\right)^3}dsds$= (L (-5.70901×10^11 x^2.3 _2 F^~_1(1.3, 2;3.3;1977.21 x) + 5.70901×10^11 x^2.3 _2 F^~_1(1.3, 3;3.3;1977.21 x) - 2.96237×10^12 x^1.8 _2 F^~_1(0.8, 2;2.8;1977.21 x) + 2.96237×10^12 x^1.8 _2 F^~_1(0.8, 3;2.8;1977.21 x) + 455606. log(0.000505762 - x) + 6.77988×10^-7 x^4 + 2.0574×10^-9 x^3 + 6.24333×10^-12 x^2 - 1627.17 x - 115.214/(x - 0.000505762) - 0.0000774843 (10621 - 2.1×10^7 x) log(10621 - 2.1×10^7 x)))/20000 + constant

$\int\int \frac{\frac{1}{2}FL^2}{E\times\frac{1}{12}\times t\times(W_1-\frac{W_1-W_0}{L}\times S)^3}dsds$= -1.88365×10^12 L^2 (0.0149815 x^2.3 _2 F^~_1(1.3, 3;3.3;1977.21 x) + 0.0777378 x^1.8 _2 F^~_1(0.8, 3;2.8;1977.21 x) - 2.00316×10^-11 x^6 _2 F^~_1(3, 5;7;1977.21 x) - 0.0000278216 x^3 2F1(2, 3, 4, 1977.21 x) - (3.02343×10^-12)/(x - 0.000505762))

$\int\int \frac{(400s^{-0.2}-5\times10^{-9}s^4+100s^{0.3}-s+280)s^2}{E\times\frac{1}{12}\times t\times\left(W_1-\frac{W_1-W_0}{L}\times S\right)^3}\,ds\,ds$=-1443.7 x^2.3 _2 F^~_1(1, 1.3;3.3;1977.21 x) + 2887.4 x^2.3 _2 F^~_1(1.3, 2;3.3;1977.21 x) - 1443.7 x^2.3 _2 F^~_1(1.3, 3;3.3;1977.21 x) - 7491.27 x^1.8 _2 F^~_1(0.8, 1;2.8;1977.21 x) + 14982.5 x^1.8 _2 F^~_1(0.8, 2;2.8;1977.21 x) - 7491.27 x^1.8 _2 F^~_1(0.8, 3;2.8;1977.21 x) - 0.00230428 log(0.000505762 - x) - 2.03396×10^-12 x^5 - 5.1435×10^-15 x^4 - 1.04056×10^-17 x^3 - 0.00406793 x^2 - 2.27803 x + (2.91355×10^-7)/(x - 0.000505762) - 1.08477×10^-7 (10621 - 2.1×10^7 x) log(10621 - 2.1×10^7 x)

ii. Matlab code

```
clear all;
clc;
ss=linspace(0,247,248);
s=ss.*0.5E-6;
l=123.5e-6;

ansys_matrix = readmatrix('Nonprismatic beam modified E model deformation 3um.csv');
ansys_position = ansys_matrix(:,1);
ansys_deformation = ansys_matrix(:,5);

hyper_A1 = hypergeom([1.3,2],3.3,1997.21.*s);
hyper_A2 = hypergeom([1.3,3],3.3,1997.21.*s);
hyper_A3 = hypergeom([0.8,2],2.8,1997.21.*s);
hyper_A4 = hypergeom([0.8,3],2.8,1997.21.*s);

hyper_B1 = hypergeom([1.3,3],3.3,1997.21.*s);
hyper_B2 = hypergeom([0.8,3],2.8,1997.21.*s);
hyper_B3 = hypergeom([3,5],7,1997.21.*s);
hyper_B4 = hypergeom([2,3],4,1997.21.*s);

hyper_C1 = hypergeom([1,1.3],3.3,1997.21.*s);
hyper_C2 = hypergeom([1.3,2],3.3,1997.21.*s);
hyper_C3 = hypergeom([1.3,3],3.3,1997.21.*s);
hyper_C4 = hypergeom([0.8,1],2.8,1997.21.*s);
hyper_C5 = hypergeom([0.8,2],2.8,1997.21.*s);
hyper_C6 = hypergeom([0.8,3],2.8,1997.21.*s);

D= 27.2796.*s.*1e-3;

A = (l/20000).*1e-3.*(-5.70901e11.*(s.^2.3).*hyper_A1+5.70901e11.*(s.^2.3).*hyper_A2 ...
    -2.96237e12.*(s.^1.8).*hyper_A3+2.96237e12.*(s.^1.8).*hyper_A4 ...
    +455606.*log10(0.000505762-s)+6.77988e-7.*(s.^4)+2.0574e-9.*(s.^3)+6.24333e-12.*(s.^2)-1627.17.*s ...
    -(115.214./(s-0.000505762))-0.0000774843.*(10621-2.1e7.*s).*log10(10621-2.1e7.*s));

B = -1.88365e12.*(l.^2).*1e-3.*(0.0149815.*(s.^2.3).*hyper_B1+0.0777378.*(s.^1.8).*hyper_B2-2.00316e-11.*(s.^6).*hyper_B3-0.0000278216.*(s.^3).*hyper_B4- ...
    3.02343e-12./(s-0.000505762));

C = 1e-3.*(-1443.7.*(s.^2.3).*hyper_C1+2887.4.*(s.^2.3).*hyper_C2-1443.7.*(s.^2.3).*hyper_C3-7491.27.*(s.^1.8).*hyper_C4+ ...
    +14982.5.*(s.^1.8).*hyper_C5-7491.27.*(s.^1.8).*hyper_C6-0.00230428.*log10(0.000505762-s)-2.03396e-12.*(s.^5)-5.1435e-15.*(s.^4)- ...
    2.03396e-12.*(s.^5)-5.1435e-15.*(s.^4)-1.04056e-17.*(s.^3)-0.00406793.*(s.^2)-2.27803.*s+(2.91355e-7./(s-0.000505762))- ...
    1.08477e-7.*(10621-2.1e7.*s).*log10(10621-2.1e7.*s));
const = -(A(1)+B(1)+C(1));

deform = -(A+B+C+D+const);
```

References

[1] T. G. P. a. J. Keene, "Submillimeter astronomy (heterodyne spectroscopy)," *Proceedings,* vol. 80, no. 11, pp. 1662-1678, 1992.

[2] S. S. H. K. B. ADUSUMALLI MALLIKHARJUNA RAO, "OVERVIEW OF MILLIMETRE WAVE BAND TO BE USED IN 5G," *International Journal of Electronics and Communication Engineering (IJECE),* vol. 5, no. 3, pp. 29-40, 2016, May.

[3] J. W. W. e. al, "The Earth observing system microwave limb sounder (EOS MLS) on the aura Satellite," *Transactions on Geoscience and Remote Sensing,* vol. 44, no. IEEE, pp. 1075-1092, 2006.

[4] C. E. G. C. Y. D. d. G. C. R. T. S. G. N. A. W. L. P. H. S. Christopher K. Walker, "Far-infrared array reciever (FAR) for SOFIA,," *Airborne Telescope Systems,* vol. 4014, no. International Society for Optics and Photonics, pp. 125-136, June 2000.

[5] A. R. P. S. K. C. S. M. D. P. L. A. W. E. J. E. &. L. E. F. Kerr, "Development of the ALMA band-3 and band-6 sideband-separating SIS mixers," *Transactions on Terahertz Science and Technology,* no. IEEE, pp. 201-212, 2014.

[6] M. v. E. a. D. R. Grischkowsky, "Characterization of an optoelectronic terahertz beam system," *IEEE Transactions on Microwave Theory and Techniques,* vol. 38, pp. 1684-1691, 1989.

[7] D. C. M. K. P.U. Jepsen, "Terahertz spectroscopy and imaging – Modern techniques and applications," *Laser Photonics,* vol. 5, pp. 124-166, 2011.

[8] D. M. G. M. N. R. B. R. G. R. J. V. &. K. M. Mittleman, "ecent advances in terahertz imaging," *Applied Physics B,* vol. 68, no. 6, pp. 1085-1094, 1999.

[9] D. B. C. G. T. S. C. H. H. L. L. R. &. M. P. Schoenherr, "Extremely broadband characterization of a Schottky diode based THz detector," in *International Conference on Infrared, Millimeter, and Terahertz Waves*, 2010.

[10] V. R. H. P. A. &. B. V. Desmaris, "Design, simulations and optimization of micromachined Golay-cell based THz sensors operating at room temperature," *Procedia Chemistry,* pp. 1175-1178, 2009.

[11] Z. Y. Z. T. C. J. C. &. L. H. Tan, "Terahertz imaging with quantum-cascade laser and quantum-well photodetector," *Photonics Technology Letters,* vol. 25, no. 14, pp. 1344-1346, 2013.

[12] L. L. J. Y. a. N. W. Z. Liu, "A fully-integrated 860-GHz CMOS terahertz sensor," in *Asian Solid-State Circuits Conference*, Xia'men, 2015.

[13] S. Hu, "Millimeter-wave/terahertz chips for high-speed communication and biomedical imaging," in *Asia-Pacific Microwave Conference*, Nanjing, 2015.

[14] J. G. R. J. a. U. R. P. P. Hillger, "Terahertz Imaging and Sensing Applications With Silicon-Based Technologies," *IEEE Transactions on Terahertz Science and Technology,* vol. 9, pp. 1-19, 2019.

[15] D. M. J. M. J. a. Y. K. V. Petrov, "Exploiting Multipath Terahertz Communications for Physical Layer Security in Beyond 5G Networks," in *INFOCOM 2019 - IEEE Conference on Computer Communications Workshops (INFOCOM WKSHPS)*, Paris,France, 2019.

[16] X. L. S. V. a. B. T. K. Sengupta, "Physically Secure mm-Wave Wireless Links with Spatio-temporal Modulated Arrays," in *Third International Workshop on Mobile Terahertz Systems (IWMTS)*, Essen, Germany, 2020.

[17] J. Q. a. M. Alouini, "Secure Transmission for Intelligent Reflecting Surface-Assisted mmWave and Terahertz Systems," in *Wireless Communications Letters*, 2020.

[18] H. S. a. T. Nagatsuma, "Present and Future of Terahertz Communications," *Transactions on Terahertz Science and Technology,* vol. 1, pp. 256-263, Sept 2011.

[19] Z. G. M. S. J. H. a. M. J. W. R. M. Urteaga, "InP HBT Technologies for THz Integrated Circuits,," *Proceedings,* vol. 105, no. 6, pp. 1051-1067, 2017.

[20] J. H. e. al, "THz MMICs based on InP HBT Technology," in *2010 IEEE MTT-S International Microwave Symposium*, 1126-1129, 2010.

[21] M. S. e. a. Kulya, "Computational terahertz imaging with dispersive objects," *Journal of Modern Optics,* vol. 64, no. 13, pp. 1283-1288, 2017.

[22] M. D. a. M. Shur, "Detection, mixing, and frequency multiplication of terahertz radiation by two-dimensional electronic fluid,," *IEEE Transactions on Electron Devices,* vol. 43, no. 3, pp. 380-387, 1996.

[23] A. e. a. El Fatimy, "Terahertz detection by GaN/AlGaN transistors," *Electronics Letters,* vol. 42, no. 23, pp. 1342-1344, 2006.

[24] E. e. a. Alekseev, "GaN-based NDR devices for THz generation," in *Proc. of the Eleventh Int. Symp. on Space Terahertz Technology*, 2000.

[25] P. C. P. N. C. W. Z. C. a. P. H. Z. Wang, "A CMOS 210-GHz Fundamental Transceiver With OOK Modulation," *IEEE Journal of Solid-State Circuits,* vol. 49, no. 3, pp. 564-580, 2014.

[26] P. &. V. B. &. S. K. &. B. J. &. D. M. &. L. D. &. H. V. &. P. G. &. M. A. &. P. B. &. G. C. &. S. V. &. C. N. &. J. M. &. D. Wambacq, "The Potential of FinFETs for Analog and RF Circuit Applications," *IEEE Transactions on Circuits and Systems,* vol. 54, no. 11, pp. 2541-2551, 2007.

[27] A. Coucoulas, "Bonding with a compliant medium". USA Patent US3533155A, 1 July 1968.

[28] P. technology, "PTI Blog," 2014.

[29] T. P. Budka, "Wide-Bandwidth Millimeter-WaveBond-Wire Interconnects.," *TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES,* vol. 49, 2001.

[30] A. S. J. L. U. G. U. Johannsen, "Bond-Wires: Readily Available Integrated Millimeter-Wave Antennas," *European Microwave Conference,* p. 197, 2012.

[31] H.-Y. Lee, "Wideband characterization of a typical bonding wire for microwave and millimeter-wave integrated circuits," *IEEE Transactions on Microwave Theory and Techniques,* vol. 43, pp. 63-68, 1995.

[32] H. D. M. C. VIVEK DIXIT, "Wire Bonding Considerations," in *Advanced electronic packaging*, 2006.

[33] C. H. C. C. K. Y. C. L. Wen Shan Tsai, "Generational Changes of Flip Chip Interconnection Technology," in *12th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)*, Taipei, 2017.

[34] L. Chen, Micromachined Millimeter-and-submillimeter-wave Circuits for test and Integration, Charlottesville, VA, 2012.

[35] Q. F. P. &. B. G. H. (. Liu, "A novel scheme for wide bandwidth chip-to-chip communications," *microelectronics and electronic packaging,* pp. 4(1), 1-7., 2007.

[36] T. J. C. L. Z. C. G. C. X. H. A. A. Reck, "Micromachined on-wafer probes," in *IEEE MTT-S International Microwave Symposium*, May, 2010.

[37] M. B. N. S. B. R. M. W. a. A. W. L. C. Zhang, "A W-Band Micromachined On-Wafer Probe With Integrated Balun for Characterization of Differential Circuits," in *IEEE Transactions on Microwave Theory and Techniques*, 2016.

[38] L. Xie, C. M. Moore, M. E. Cyberey, S. Nadri, N. D. Sauber, M. F. Bauwens, A. W. Lichtenberger, N. S. Barker and I. Robert M. Weikle, "Micromachined probes with integrated GaAs Schottky diodes for on-wafer temperature sensing," in *IEEE International Instrumentation and Measurement Technology Conference*, 2018.

[39] M. B. C. Z. A. W. L. R. M. W. a. N. S. B. Q. Yu, "Integrated strain sensor for micromachined terahertz on-wafer probe," in *2013 IEEE MTT-S International Microwave Symposium Digest (MTT), Seattle*, Seattle, 2013.

[40] M. F. B. C. Z. A. W. L. R. M. W. a. N. S. B. Q. Yu, "Improved Micromachined Terahertz On-Wafer Probe Using Integrated Strain Sensor," *IEEE Transactions on Microwave Theory and Techniques,* vol. 61, no. no. 12, pp. pp. 4613-4620, 2013.

[41] B. J. a. J. M. G. Goodno, Mechanics of materials, Cengage learning, 2020.

[42] W. D. N. a. T. W. K. M. A. Hopcroft, "What is the Young's Modulus of Silicon?," *Microelectromechanical Systems,* vol. 19, no. 2, pp. 229-238, April, 2010.

[43] T. J. R. e. al., "Micromachined on-wafer probes," in *MTT-S International Microwave Symposium*, Anaheim, CA, 2010.

[44] L. D. T. C. R. S. S. M. C. E. Bressan E, "Experimental and computational investigation of Morse taper conometric system reliability for the definition of fixed connections between dental implants and prostheses.," *Proc Inst Mech Eng H,* vol. 228, no. 7, pp. 674-681, 2014 Jul.

[45] D. a. S. M. Bozkaya, "Mechanics of the tapered interference fit in dental implants," *Journal of Biomechanic,* vol. 36, no. 11, pp. 1649-1658, 2003.

[46] E. a. F. D. J. Oberg, Machinery's Handbook for Machine Shop and Drafting-room: A Reference Book on Machine Design and Shop Practice for the Mechanical Engineer, Draftsman, Toolmaker and Machinist, Industrial press, 1914.

[47] D. M. Pozar, Microwave engineering, John wiley & sons, 2011.

[48] T. Reck, Submillimeter Wavelength Metrology Components, 2010.

[49] J. e. a. Krupka, "Dielectric properties of semi-insulating silicon at microwave frequencies," *Applied Physics Letters ,* vol. 107.8, p. 082105, 2015.

[50] J. R. E. D. M. a. R. T. W. Reid, "Micromachined rectangular-coaxial transmission lines," *IEEE Transactions on Microwave Theory and Techniques,* vol. 54, no. 8, pp. 3433-3442, 2006.

[51] C. Zhang, Development of Single-ended and Balun Integrated Probes for THz Applications., Charlottesville: University of Virginia, 2014.

[52] P. Q. S. &. F. L. C. H. Hernigou, "One hundred and fifty years of history of the Morse taper: from Stephen A. Morse in 1864 to complications related to modularity in hip arthroplasty," *International orthopaedics,* vol. 37, pp. 2081-2088, 2013.