Power Management in Ultra-Low Power Systems

A Dissertation

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APPROVAL SHEET

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Abstract

The evolving vision of the Internet-of-Things (IoT) will revolutionize various applications such as remote health monitoring, home automation and remote surveillance. It has been projected that by 2025, there will be 1 trillion IoT devices influencing our daily lives. This will result in the generation of an enormous amount of data, which will have to be stored, processed and transmitted efficiently and reliably. Although advancements in Integrated Circuit (IC) design and the availability of various Ultra-low Power (ULP) circuit components have helped us to visualize an ecosystem of numerous internet-connected devices, the overall system integration will become a major challenge. A System-on-Chip (SoC), catering to IoT applications is expected to contain many different circuit components such as sensors and Analog-Front-Ends (AFEs) for real-time signal acquisition, analog-to-digital converters, digital signal processors, memories, wireless transceivers etc. All these components have different supply voltage requirements and power profiles. Hence, power delivery to such components in an SoC will play an important role in the overall system architecture. Although, battery-powered systems have traditionally worked well in portable electronics but in an IoT ecosystem, the cost of battery replacement in a trillion-sensor node network will be enormous. In many applications, such as remote surveillance, systems require a long operational lifetime. Moreover, system deployment should be unobtrusive and hence such systems should have small form factors. The above requirements are hard to meet using conventional battery-powered systems. Hence, in most IoT SoCs, there is a strong motivation for an integrated Power Management Unit (PMU), with energy harvesting capability for near-perpetual battery-less operation, which

can provide a range of supply voltage rails to satisfy the electrical specifications of different functional units.

This dissertation addresses the design challenges related to energy autonomy and power-delivery in a wireless sensor node. This work presents an energy harvesting platform in context of a self-powered System-in-Package (SiP) with a capability to harvest from either photovoltaic or thermoelectric generators (TEGs). The SiP consists of an SoC for processing and storage, non-volatile memory, a wireless transceiver and various off-the-shelf sensors. To deliver power and to meet the electrical specifications of these different components of the sensor node, this work presents an efficient, low quiescent power, supply-voltage regulation scheme. In addition to power delivery, this dissertation also demonstrates several ULP digital and mixed-signal circuit components, commonly used in energy-autonomous and always-ON systems such as an event-driven wakeup receiver. This work describes circuit solutions and techniques related to power delivery that will enhance the operational lifetime, reduce the overall form-factor and contribute towards attaining energy-autonomy to facilitate a wide range of applications related to the IoT.

In the midst of chaos, there is also opportunity
-Sun Tzu, The Art of War

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The last four years at the University of Virginia has been an enriching experience and I will cherish the memories for the rest of my life. I've had the pleasure of meeting and working with some exceptionally talented individuals over the years and I give them all the credit for where I stand today.

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Contents

List of Tables

List of Figures

List of Acronyms

IoT Internet-of-Things

SoC System-on-Chip

SiP System-in-Package

ULP Ultra-low Power

DSP Digital Signal Processing

ISA Instruction Set Architecture

FIR Finite Impulse Response

ECG Electrocardiogram

CMOS Complementary Metal Oxide Semiconductor

NMOS n-channel Complementary Metal Oxide Semiconductor

PMOS p-channel Complementary Metal Oxide Semiconductor

SOI Silicon on Insulator

FDSOI Fully Depleted Silicon on Insulator

PDSOI Partially Depleted Silicon on Insulator

PE-ALD Plasma-Enhanced Atomic Layer Deposition

DDC Deeply Depleted Channel

FET Field Effect Transistor

NFET n-channel Field Effect Transistor

PFET p-channel Field Effect Transistor

TT Typical-Typical

HCI Hot Carrier Injection

FMAX Maximum Operating Frequency

DVS Dynamic Voltage Scaling

DVFS Dynamic Voltage and Frequency Scaling

TEG Thermoelectric Generator

PV Photovoltaic

MPP Maximum Power Point

MPPT Maximum Power Point Tracking

HC Hill Climbing

P&O Perturb and Observe

P-V Power vs. Voltage

LS Low-Side

HS High-Side

PWM Pulse Width Modulation

PFM Pulse Frequency Modulation

DCM Discontinuous Conduction Mode

CCM Continuous Conduction Mode

SC Switched Capacitor

SCN Switched Capacitor Network

SSL Slow Switching Limit

FSL Fast Switching Limit

MiM Metal-Insulator-Metal

I_Q Quiescent current

LDO Low Drop Out

EA Error Amplifier

EH-PMU Energy Harvesting and Power Management Unit

EH Energy-Harvesting

PMU Power Management Unit

SIMO Single Inductor Multiple Output

POR Power-on-Reset

VR Voltage Regulator

BGR Bandgap Reference

CTAT Complementary to Absolute Temperature

PTAT Proportional to Absolute Temperature

CMU Current Mirror Unit

PSRR Power Supply Rejection Ratio

PSR Power Supply Rejection

LS Line Sensitivity

TC Temperature Coefficient

WRX Wake-up radio

FIR Finite Impulse Response

RO Ring Oscillator

E-D Energy-Delay

LFSR Linear Feedback Shift Register

PSN Power Supply Noise

PGA Pin Grid Array

PMEM Program Memory

DMEM Data Memory

SRAM Static Random Access Memory

UART Universal Asynchronous Receiver/Transmitter

Chapter 1

Introduction

1.1 Energy harvesting and power management

Technology scaling and shrinking device dimensions have helped a circuit designer to implement battery-operated computing systems with a high level of system integration such as laptops, smartphones, tablets etc. However, applications such as surveillance and remote health monitoring need unobtrusive solutions which require systems to have small form-factors and a longer shelf life. In such applications, battery-powered systems will be mostly constrained by the size of the battery since batteries do not scale at the same rate as CMOS integrated circuits. Moreover, large scale battery replacement will be expensive. In such scenarios, energy harvesting from ambient sources such as solar energy, thermal and vibration provides a viable solution. The harvested energy can be stored in an energy reservoir such as a supercapacitor and can be used by the system when required. Thus, harvesting energy from ambient sources can theoretically provide a near-perpetual system lifetime and enable further shrinking of the overall system volume. However, a self-powered system design comes with the following design challenges:

1.1.1 System sustainability

Systems which can harvest from only one ambient source need to address a major limitation i.e. how the system will operate when the ambient source is unavailable. In such a scenario, a duty-cycled approach can limit the supported features of the system in order to prevent the complete discharge of the energy reservoir. However, this method also significantly limits the performance and the range of desired applications. Another approach to address this limitation would be to design system components especially circuits which are always ON to consume extremely low power in the order of the self-discharge rate of a battery or the leakage power of a supercapacitor which range from tens to hundreds of nW. The advantage of this approach is that it not only enhances the overall system lifetime in the absence of harvesting but also enables the scaling of the energy transducer (TEG/PV) and the storage device, reducing the overall volume of the system. It also enables the system to include more functionality, such as additional sensor interfaces for motion, environmental sensing and to incorporate a higher duty-cycle for periodically active components, such as accelerometers for motion sensing, wireless transmitters and digital processors. Figure 1.1 describes a typical

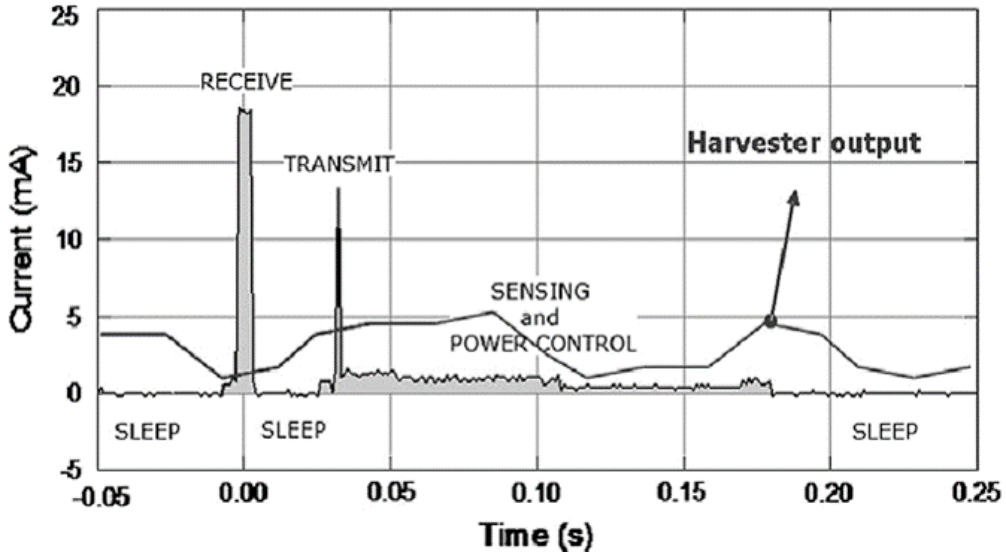


Figure 1.1: Harvester and load current profile of a wireless sensor node in time-domain. [3]

load current profile and the available power from the harvester in time-domain. For a near

perpetual system operation, the time integral of the power consumed by the load which includes the system, leakage of the storage device etc. needs to be lower than the time integral of the available power from the harvester which is primarily dependent on the the environment and characteristics of the transducer. In other words, the system can draw higher peak power (e.g. during wireless transmission) as compared to the instantaneous power provided by the harvester during certain time intervals as long as the average power of the system is lower than the average harvested power. The storage buffer supports the peak current demands of the system during such time intervals. In this work, we investigate power-efficient harvesting and voltage regulator circuits which consume low quiescent power. This work also presents the design of ultra-low power system components such as microcontrollers and always-ON systems such as an event-driven wake-up receiver.

1.1.2 System start-up

In a battery-less, self-powered system, it is essential that the minimum voltage on the storage buffer(V_{STORE}) is greater than the minimum operational voltage (V_{KILL}) of the always-ON circuits, such as converter control (bias generators, references, comparators, digital logic etc.) of the chargers and regulators, at all times but especially during the time intervals when the storage buffer is responsible to meet the peak current demands of the system. Thus, a lower operational/startup voltage of circuits, such as converter controllers is crucial for achieving reliability and lifetime improvements of the system.

To enable this design requirement, a cold-start mechanism is necessary to generate a Power-on-Reset (POR) sequence and kick-start system operation. The control logic of the energy harvester, as well as other circuit components, which are usually implemented using CMOS technology, can only operate at a certain minimum voltage. In the worst-case scenario, the start-up mechanism needs to be designed assuming that the storage reservoir is completely empty. If the energy harvester can cold-start at a low input voltage, then the system can achieve a greater degree of energy-autonomy. In this work, we will investigate ultra-low-

voltage cold-start circuits to enable energy harvesting and power management at ultra-low voltage levels.

1.1.3 Power-efficiency

Achieving high end-to-end power efficiency is a key requirement especially in scenarios or environmental conditions where the volume-constrained harvester e.g. wearable TEGs, can provide only 10s of μW of power. In such scenarios, it is essential to minimize the power loss in the Energy Harvesting and Power Management Unit (EH-PMU) such that nearly all of the available energy can be extracted and stored in the reservoir. Hence, the powertrain architecture and the control circuits of the EH-PMU need to be designed to minimize power loss. Another method to maximize power-conversion efficiency is to track the maximum power point of the harvester for a given environmental condition using a Maximum-Power-Point-Tracking (MPPT) scheme. In this work, apart from designing the powertrain architecture and control circuits to be power-efficient, we explore various MPPT schemes, which can work for multiple sources such as TEGs and photovoltaic cells especially at power levels in the order of a few μW.

1.2 Integrated supply voltage regulation

Integrated voltage regulators have become common in modern SoCs, which involve a high degree of system integration. Moreover, with technology scaling, the efficiency and performance of these integrated regulators have improved significantly. Supply regulation plays a major role in delivering power to various hardware components in an SoC/SiP such as microprocessor cores, memories, I/O interfaces, wireless transceivers and other analog and mixed-signal circuits. For instance, Figure 1.2 shows the system architecture of a self-powered SoC which supports various biomedical applications such as ECG and heart rate monitoring. The SoC consists of different analog/mixed signal and digital components such as ADC,

memories, various DSP accelerators and a wireless transceiver, which require regulated rails with different electrical specifications such as output voltage, load/line regulation and PSRR. Applications, which require maintenance-free sensing systems, such as self-powered SoCs,

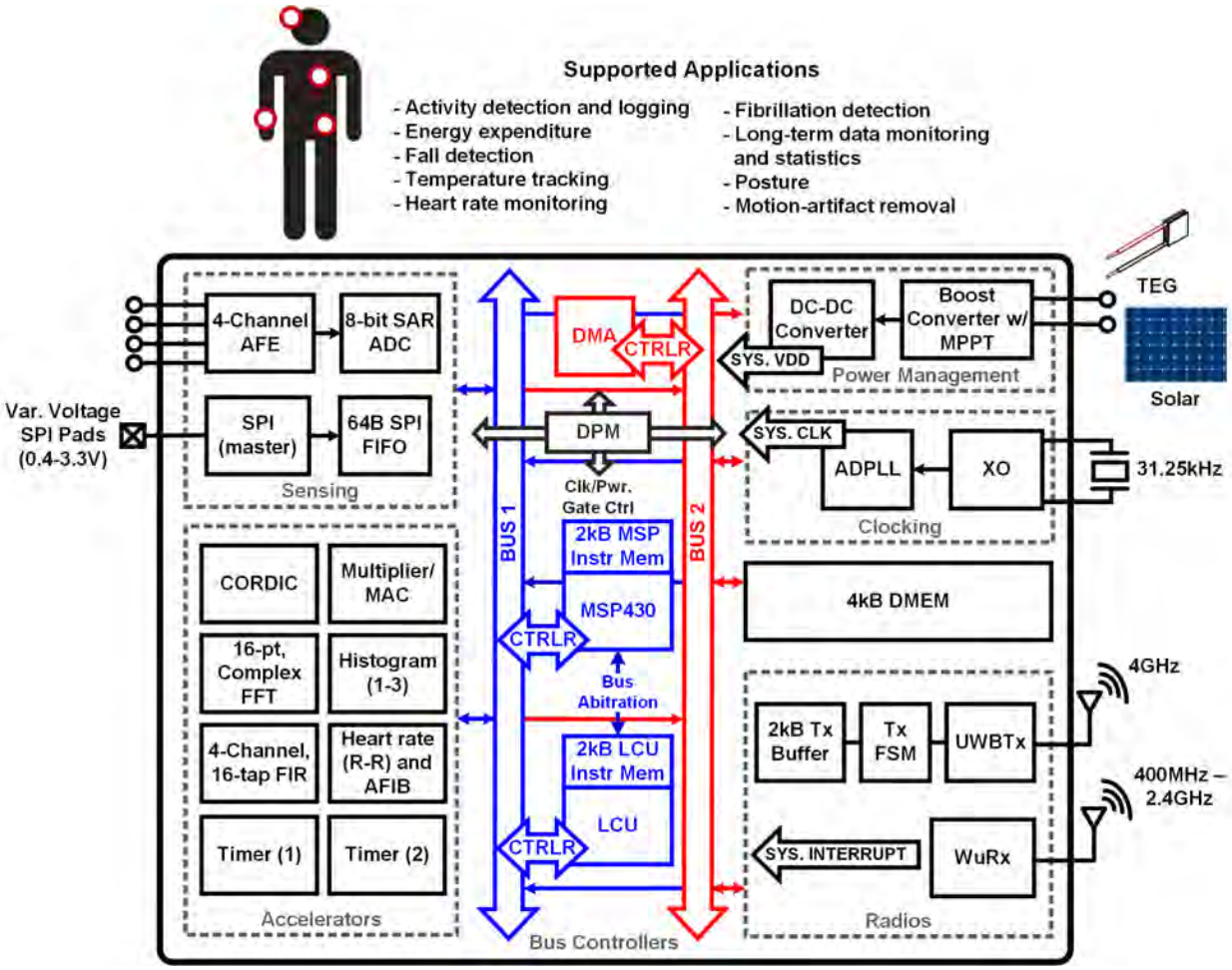


Figure 1.2: System architecture of a self-powered SoC used in biomedical applications [4]

incorporate integrated voltage regulators which present the following key design challenges:

1.2.1 Support electrical specifications of diverse SoC components

The various circuit components in an IoT SoC such as ADCs, memories, processors and I/O interfaces consume minimum power or achieve energy-efficiency at different voltage levels. Digital circuits often employ Dynamic Voltage and Frequency Scaling (DVFS) to achieve energy-efficiency. Usually, the power distribution networks of digital and analog components

are isolated, since analog components are more sensitive to power supply noise and thus have less tolerance to power supply variations. Hence, an integrated power management unit needs to provide independent supply rails to these components and also meet the electrical characteristics such as ripple, Power Supply Rejection Ratio (PSRR), maximum load currents and settling time. The number of independent voltage regulators, is limited based on the overall system-level power efficiency, area and design complexity. In this work, we investigate the above challenges related to integrated voltage regulation and recommend best design practices for supply regulation in IoT SoCs.

1.2.2 Power efficiency

Similar to energy-harvesters, integrated voltage regulators need to be power-efficient, especially in micropower IoT systems. Various circuit components of an IoT SoC are designed to operate at very low power levels mostly in the μW range. Lack of power efficiency in voltage regulation will drain the storage buffer or load the energy harvester unnecessarily. Power-hungry components such as wireless transceivers are extensively duty-cycled to transmit data, only when required. Thus, integrated voltage regulators in such systems should support transients in load current with high power efficiency. In this work, we investigate different converter topologies and associated controller designs to enable power-efficient supply regulation at ultra-low load currents.

1.2.3 Area and eliminating the need for off-chip passives

Although, different components of an SoC might require entirely different supply voltage levels or electrical characteristics, implementing dedicated voltage regulators for each component will be highly inefficient due to greater area and power overheads. An optimal design strategy is desired which limits the number of integrated voltage regulators or re-configures the existing regulator topologies to support different conversion ratios. Power-efficient, switching regulators conventionally need off-chip passives for operation, which increases the package

pin count, inflating the cost and overall form-factor of the system. Fully integrated regulators are limited by their peak power efficiency but can be leveraged in a volume-constrained system. In this work, we explore circuit design techniques to reduce the number of passives and implement multiplexing schemes to re-use off-chip passives. We also investigate fully integrated regulators to eliminate the need for off-chip passives.

1.3 Ultra-low-power analog/mixed signal and digital circuit components in self-powered systems

Applications such as remote surveillance and environmental monitoring need systems with small form-factors and near perpetual operational lifetimes. Hence, in most cases, such systems are severely energy-constrained. It is imperative that circuit components, which reside in such systems, are designed to consume very low active energy and ultra-low standby power. Processors, custom accelerators and "always-ON" circuits such as a wakeup-receiver form an integral part of such systems. In this work, we investigate the role of current state-of-the-art CMOS technology in designing energy-efficient digital circuits such as processors and accelerators. We also study the role of technology in improving circuit robustness during subthreshold operation. This work also presents the design of ultra-low power comparators in power-constrained applications such as wakeup-receivers.

1.4 Thesis Contributions

This dissertation addresses the challenges attributed to self-powered operation discussed above. This work enables the deployment of maintenance-free systems catering to a wide range of IoT applications, such as infrastructure monitoring, health-care and environmental sensing. Figure 1.3 highlights the core areas, this work focuses on and enhances the state-of-the-art to achieve energy autonomy. The boost converter and charger circuits presented in this

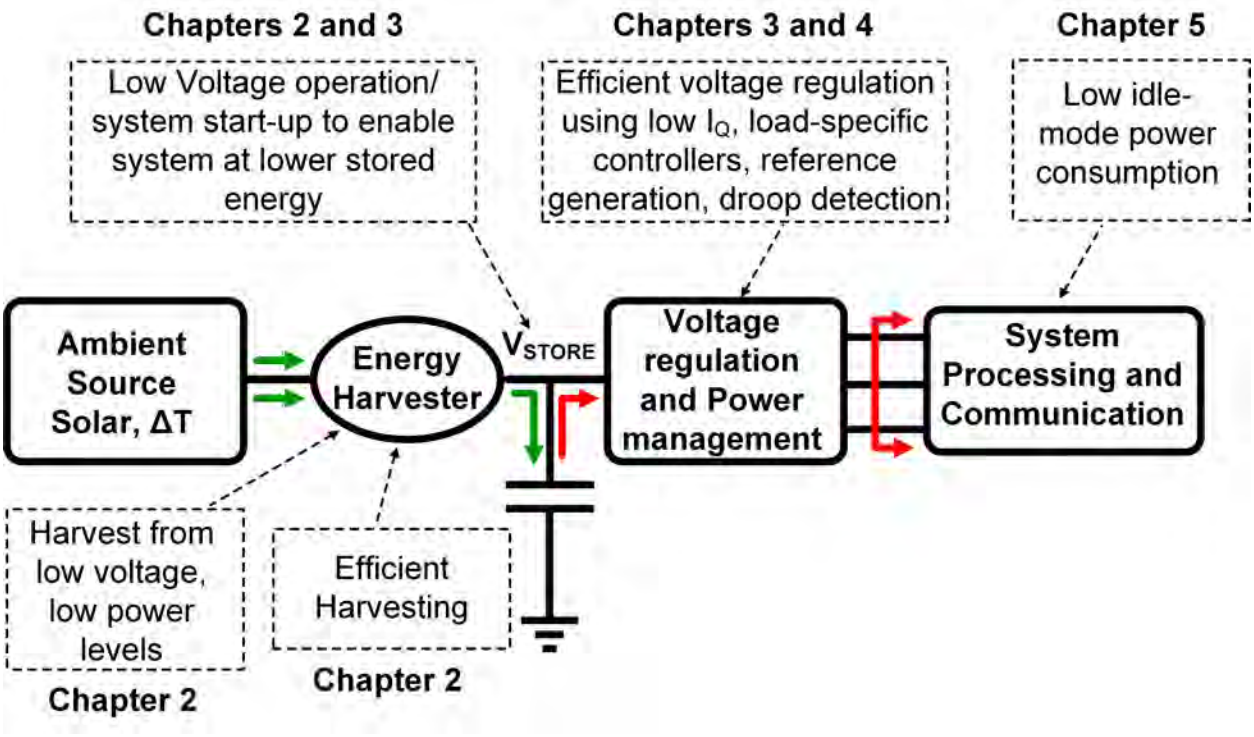


Figure 1.3: Energy flow in a self-powered IoT device. Critical points and thesis contributions have been highlighted where optimization has been performed to enable energy-autonomy

work (Chapter 2) can harvest from both thermal and photovoltaic sources, achieving a peak efficiency of 90.7% at 1V and 47% at 30mV, which is 7-10% higher than existing works at similar voltage or power levels (i.e. 1-30μW) [14] [6] [15] [16]. To a first order, a 7-10% improvement in conversion efficiency corresponds to a 7-10% improvement in harvesting and storing usable energy under poor environmental conditions such as low illumination levels in indoor light ($<$ 200lux), encountered in solar-powered, building automation devices [3] and low temperature differentials, encountered commonly in TEG-based wearable systems, such as body sensor nodes [3]. Since the power available from harvesters is proportional to its size [3], a 7-10% improvement in conversion efficiency and the ability to harvest from low voltage levels (10mV) translates to corresponding gains in reducing the overall size of the harvester, which is critical in volume-constrained systems, such as implantable intraocular pressure monitors in health-care [17] [18] or ECG monitors in biomedical applications [19]. The boost converter presented in Chapter 2 supports a maximum of 3V on the storage device

(which can be either a battery or a supercapacitor). Compared to existing works [15] [14] [6], which employ a similar sized storage capacitor (10mF), this work presents a 2X improvement in the maximum voltage level resulting in quadratic savings (CV^2) in the energy storage capacity of the system. In the absence of harvesting sources, for a given load, leakage profile and capacity of the storage device, this results in approximately V^2 or a 4X improvement in the overall system lifetime as compared to existing works such as [15] [14] [6], .

The minimum operational voltage of power delivery circuits such as regulators are limited by conventional reference generator architectures such as Bandgap references which typically need a minimum headroom greater than 1V [20]. This work presents a buck-boost regulator and a novel reference generator circuit (Chapter 3) which are operational from low voltage levels. Thus, this work enables power delivery at ∼75% lower energy levels on the storage capacitor translating to an equivalent improvement in energy autonomy, in the absence of harvesting. The regulator circuits presented in this work (Chapter 3) are optimized to meet different electrical specifications associated with each voltage domain by leveraging independent load-specific, closed-loop controller designs. This work introduces the concept of "sloppy yet power-efficient voltage regulation" in context of efficient power delivery at sub-μW loads (Chapter 3). By relaxing line/load regulation constraints and allowing optimal load-specific supply voltage ripple (which is governed by component-level specifications), the "always-ON" quiescent power of the regulators is reduced by ∼10X as compared to existing works, such as [21]. In addition to regulators, this work also presents several other "always-ON" components, such as an ULP reference generator (Chapter 3) and an event-driven wakeup receiver (Chapter 5), which achieves the lowest DC power consumption (7.4nW) as compared to other existing receivers [22], which have reported a sensitivity greater than -70dBm. Reducing the quiescent power overhead of "always-ON" components, such as regulators by 10X and extending the end-to-end efficiency of the EH-PMU by 25-30% (Chapter 3) as compared to [23],[24],[25] allows a system designer correpsondingly higher flexibility to integrate additional functionality in the form of more duty-cycled, application-

specific accelerators, processors [10] and sensor interfaces such as accelerometers [26], imagers [27] and ozone sensors[28]. The power converters presented in this work (Chapter 3) provides different regulated outputs (1.8V, 1V and 0.5V) to meet the electrical requirements of various sensor components, allowing the overall system to be flexible and fit into a variety of industrial, health-care and environmental sensing applications, which contribute to the IoT and ultimately impact our daily lives.

1.5 Dissertation Organization

This dissertation is organized as follows. Chapter 2 presents a single inductor boost converter for harvesting energy from either TEGs or photovoltaic cells. The converter consists of a Maximum Power Point Tracking circuit and an adaptive peak inductor current controller to support high efficiency across a wide range of available power from the harvester. A low-voltage cold start mechanism and an all-digital, low power zero crossing detector circuit is presented. The second contribution of this chapter is a tool-flow and design methodology to assist a circuit designer to evaluate the powertrain and converter control during various stages of the design cycle.

Chapter 3 presents a single inductor multiple output buck-boost converter, operational from low input voltages (0.7V) for voltage regulation in context of ultra-low power systems. To minimize the need for off-chip passives in volume-constrained applications and enable a modular approach to design power-efficient voltage regulator circuits in ultra-low power ($< 1\mu$W) systems, a low-I_Q fully-integrated, Power Management Unit with start-up control is presented.

Chapter 4 addresses the impact of power supply variation in ULP systems. Latch and register-based digital circuits are compared for robustness and energy efficiency in presence of low frequency(<1kHz) power supply droop. All-digital droop detection and measurement circuits are described which consume low static power($< 1\mu$W) and can be leveraged in

converter control at light-loads.

Chapter 5 presents a subthreshold MSP430 processor designed in a low-leakage FDSOI technology and an FIR filter designed in a custom low-leakage DDC technology, highlighting the benefits of process technology in reducing the standby power of system components with minimal degradation in performance. The second contribution of this chapter is an event-driven, always-ON wake-up receiver system, which consumes low power (7.4nW) in the order of the self-discharge rate of a battery. Ultra-low power comparator circuits with a novel offset controller, oscillator , digital correlators and operating in the subthreshold region enable the system to achieve a high sensitivity (-76dBm) with a low power overhead (7.4nW).

Chapter 2

Energy Harvesting from Ambient DC sources

2.1 Motivation

Advancements in integrated circuit design have led to the development of ULP electronics, such as wireless sensor nodes for surveillance, health monitoring and home automation applications. These new generation of smart electronic sensors and devices need to have small form factors, especially in biomedical applications, such that they are non-invasive. Today, batteries represent the dominant source of energy in electronic systems but they largely dictate the overall size, making the system bulky and not scalable. In case of surveillance applications, such systems need to be deployed in large numbers and in remote locations. Hence, the cost of battery replacement is high. Thus, such systems need a compact, low-cost and near-perpetual source of energy for a long operational lifetime. Energy harvesting from ambient sources, such as solar and thermoelectric energy, vibration/motion and RF, provides a viable alternative to battery-powered systems. The overall system reliability and the ability of the energy harvesting charger to provide more usable energy to the system can be further enhanced if the charger has the the necessary electronics to harvest from multiple harvesting

modalities.

2.2 Background

The primary goal of any energy scavenging system is to harvest energy from ambient sources, such as light, motion, thermoelectric energy etc. and store it in a storage device or an energy buffer, such as a supercapacitor. Another approach is to use the harvested energy to charge a re-chargeable battery. However, most state-of-the-art high energy-density rechargeable batteries have limited charge-discharge cycles, making battery-replacement unavoidable and thus restricting the system lifetime. A good supercapacitor can support more than 10000 charge-discharge cycles [3] and thus can be leveraged in energy-autonomous systems, provided that the supercapacitor has low leakage and has a small form factor to meet the size restrictions of a wireless sensing node. Energy storage in a wireless sensor node is necessary because the peak currents needed during wireless transmission cannot be supported directly by an energy harvester. Hence, in such scenarios, a storage device such as a supercapacitor or a small re-chargeable battery acts as a buffer to support the peak current requirements of the system. Based on the overall powertrain architecture, integrated energy harvesters can be broadly classified into two categories:

1. Inductor-based Boost or Boost-Buck converters.

2. Voltage multipliers or charge-pumps based on switched-capacitor topologies.

Inductor-based topologies have been found to be more power-efficient in scenarios where a wide range of input voltage is available from TEGs, solar cells etc. Inductor-based topologies also provide a better efficiency than a charge-pump for a wide range of load currents. However, inductor-based switching converters need off-chip passives such as high-Q inductors and extra package pins, which increases the cost. Charge-pump circuits can be fully integrated in modern fabrication processes and hence can be incorporated in systems requiring smaller form factors.

2.2.1 Sources of energy harvesting in micropower systems

Most self-powered wireless sensing systems are designed to harvest energy broadly from three different ambient sources: thermal energy, indoor/outdoor light energy and energy from vibration/motion/RF. In this work, we will focus on energy harvesting from solar and thermoelectric energy and hence we will only discuss the physics and the operating principles of thermoelectric generators and photovoltaic cells.

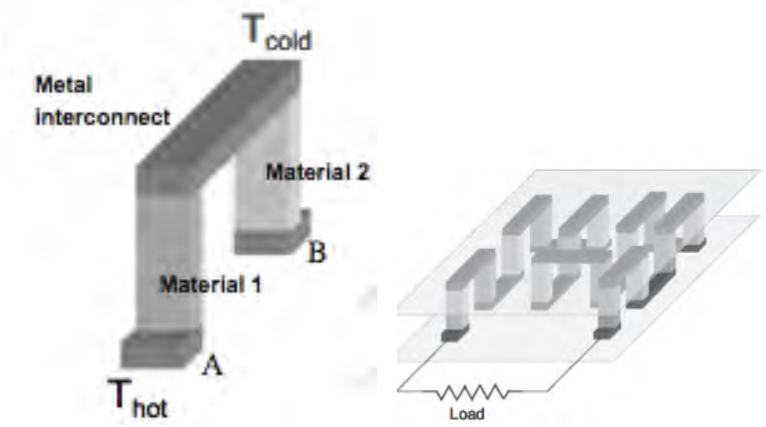
Thermoelectric energy /Thermoelectric generators (TEG) Thermal energy harvesters are based on the principle of Seebeck effect i.e. when two junctions, made of two different conductors, are kept at different temperatures; an open circuit voltage develops between them. Figure 2.1a shows a diagram of a thermocouple, which is the most basic voltage generator based on the Seebeck effect. The two pillars, or legs, are made of two different materials and connected by a metallic interconnect. When a temperature differential, ΔT is established between the bottom and the top pillars, a voltage, V develops between the points A and B. This voltage is given by:

$$V = S.\Delta T, \tag{2.1}$$

where S is the overall Seebeck coefficient.

The primary component inside a TEG is a thermopile (shown in Figure 2.1b), which is constructed by connecting a large number of thermocouples electrically in series such that the contribution of each thermocouple to the voltage adds up.

Other components of a TEG may include a radiator or a heat sink for efficient heat dissipation into the ambient or structures such as thermal shunts to direct the heat absorbed into the legs of a thermocouple for higher efficiency. Figure 2.2 shows the equivalent electrical model of a TEG. The electrical resistance R_{EL} of the thermopile is proportional to the



(a) (b)

Figure 2.1: Basic structure of (a) Thermocouple and (b) Thermopile [3]

resistivity ρ of thermoelectric material and to the number of thermocouples. Hence,

$$R_{EL} = \frac{2\eta\rho h}{a^2} \tag{2.2}$$

where, η is the number of thermocouples connected in series, h is the height of the legs and a is the lateral dimension of the pillars. The maximum available output power on a matched load ($Z_{LOAD} = R_{EL}$) is thus given by

$$P = \frac{V^2}{4R_{EL}} \tag{2.3}$$

Light/Solar and Photovoltaic (PV) energy harvesters Light or solar power panels provide an inexhaustible source of energy, especially in outdoor conditions. The principle of photovoltaic energy harvesters is based on the photoelectric effect, which is the ability of photovoltaic materials such as crystalline and amorphous silicon, to emit electrons after absorbing light. The number of photons depends on the light intensity and if there are a sufficient number of photons incident on a photovoltaic material, electricity can be obtained. Hence, the power, which can be harvested from a solar cell, depends on the light intensity. However, the main disadvantage of using a photovoltaic source is the reduced output power

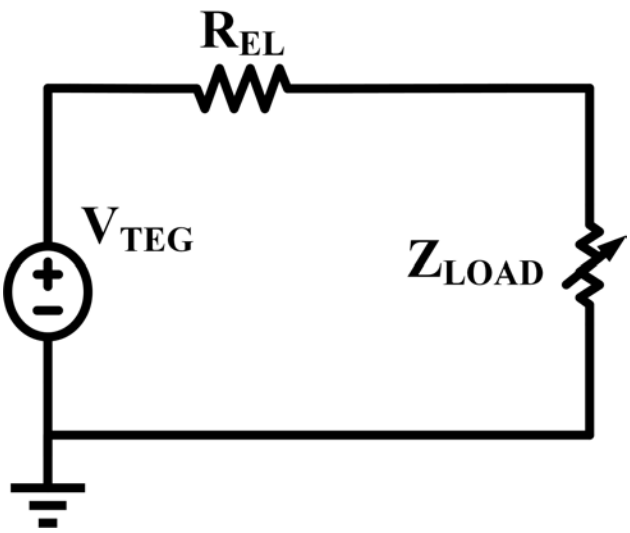


Figure 2.2: Electrical model of a TEG

Table 2.1: Comparison of solar, TEG and other power harvesting sources in indoor and outdoor conditions [1]

Energy Harvester	Power Densities	
	Indoor condition	Outdoor condition
Solar Panel	$100\mu W/cm^2$ @$10W/cm^2$	$10mW/cm^2$ @STC
Wind turbine-generator	$35\mu W/cm^2$ @ <1m/s	$3.5mW/cm^2$ @8.4m/s
Thermoelectric generator	$100\mu W/cm^2$ @ 5°C gradient	$3.5mW/cm^2$ @30°C gradient
Electromagnetic generator	$4\mu W/cm^3$ @ human motion-Hz	
	$800\mu W/cm^3$,@ machine-kHz	

in indoor light conditions or in conditions where the light intensity is not consistent. Table 2.1 describes the comparison of both photovoltaic, thermoelectric, and wind/motion power sources in outdoor/industrial and indoor conditions.

The power-efficiency of indoor photovoltaic cells reduces drastically in indoor conditions. Connecting multiple solar cells electrically in series can increase the power generated from a solar panel but also increases the output impedance and limits the total available power. Figure 2.3 shows the equivalent electrical model of a solar cell [1]. The current source, I_L, models the generated photoelectric current, which depends on the light intensity. I_D denotes

the current due to recombination of carriers. The shunt (R_{SH}) and series (R_S) resistance accounts for the solar cell non-idealities and second-order effects such as leakage currents around the edge of the cell, contact resistance and resistance of the material. I_{PV} is the equivalent photovoltaic current and V_{PV} is the equivalent output open-circuit voltage. Hence, the available power from a solar cell is given by:

$$P(V_{PV}) = V_{PV} I_{PV} \tag{2.4}$$

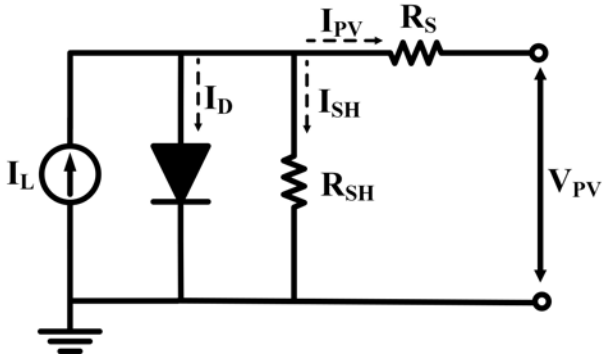


Figure 2.3: Electrical model of a PV/solar cell

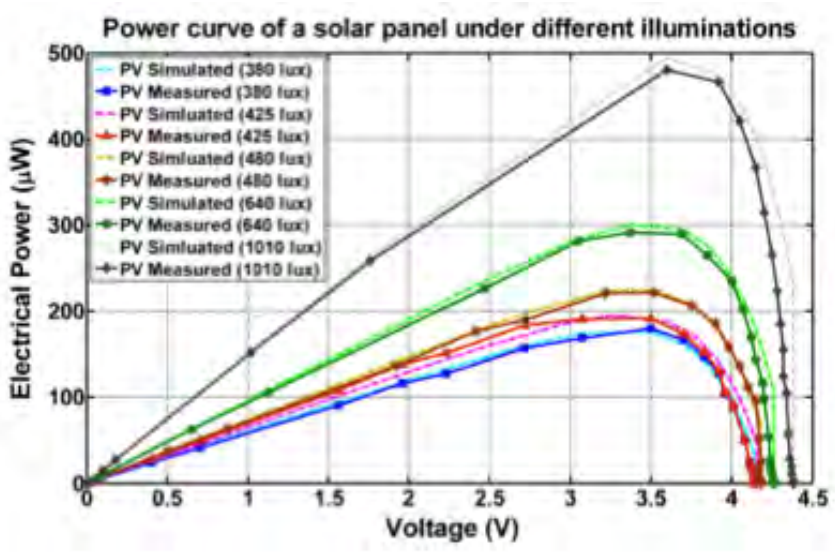


Figure 2.4: P-V curves of a solar cell at different light intensities [1]

Figure 2.4 shows the measured and simulated output power and voltage characteristics of a solar cell subject to different levels of illumination. Figure 2.4 shows that the peak power available at different illumination levels occurs between 70-78% of the open circuit voltage.

2.2.2 Maximum-Power-Point-Tracking

High end-to-end power efficiency in self-powered systems across a wide range of environmental conditions is a necessity. Since the maximum power available from TEGs and solar cells varies significantly with environmental conditions, a built-in method, which keeps track of the Maximum Power Point (MPP) with changing conditions, is extremely useful. By keeping track of the MPP, which is roughly around 50% of the open-circuit voltage [29] of a TEG or around 73-80% [29] of the open-circuit voltage of an indoor solar cell, the system can extract the maximum power available in any condition. A Maximum Power Point Tracking (MPPT) scheme is even more useful if the system needs the flexibility to harvest energy from multiple modalities such as TEG, solar, piezo etc. The basic idea behind MPPT is that a boost converter or a charge-pump interface needs to provide an optimal input impedance such that the source operates at its MPP under different environmental conditions. In case, the system needs the flexibility to harvest from multiple modalities, the range of input impedance required for MPP varies significantly. For instance, in [1] the output impedance of a solar cell at different MPPs, subject to varying degrees of illumination, varies between 27-68kΩ whereas the output impedance of a TEG at MPP is roughly fixed at 82kΩ. Thus, if the system needs the capability to harvest maximum power from diverse harvesting modalities, the MPPT circuit needs to tune the input impedance of the boost converter or the charge pump interface to match the output impedance of the source across a wide range. Several techniques to implement MPPT have been discussed in the literature. We will discuss the theory behind some of the more common methods, which are implemented in ULP systems.

Hill Climbing/Perturb and Observe Hill Climbing (HC) involves perturbing the duty-cycle of a power converter while Perturb and Observe (P&O) involves disturbing the voltage provided by a TEG or a solar cell. By allowing the output voltage from a TEG or a solar cell to increase or decrease, the output power is monitored using a voltage and/or a current sensor. With the increase in voltage, if the power increases then the perturbation is continued in the same direction (voltage is increased by a finite step) but if with the increase in voltage, the power decreases, then the direction of perturbation is reversed (voltage is decreased by a finite step). This process is repeated in an iterative fashion, such that the final operating point oscillates around the MPP. The degree of oscillation can be controlled using a smaller step size or fine-grained resolution but this usually results in a longer response time to achieve MPP operation. However, under sudden changes in environmental conditions, especially when conditions change rapidly before the MPPT circuit responds, the HC/P&O methods do not provide an optimal solution.

Incremental Conductance The theory behind the incremental conductance method is that the slope of the Power vs. Voltage (P-V) curve of a TEG or a solar cell is zero at the MPP. The slope is positive toward the left of the P-V curve and changes direction to the right of the P-V curve.

$$P = VI \tag{2.5}$$

$$\frac{\Delta P}{\Delta V} = I + V\frac{\Delta I}{\Delta V} \tag{2.6}$$

where, V and I are the instantaneous output voltage and current and P is the instantaneous power from a TEG or solar cell. ΔP and ΔI represents the change in instantaneous power and current subject to an instantaneous change in output voltage, ΔV. Hence, by keeping track of instantaneous conductance, $\frac{I}{V}$ and incremental conductance, $\frac{\Delta I}{\Delta V}$, MPP operation can be achieved.

Fractional Open-Circuit Voltage From the P-V curves in Figure 2.4 (Section 2.2.1), it is evident that the output voltage at MPP (V_{MPP}) is a fraction of the open-circuit voltage (V_{OC}) of a solar cell. This fraction varies roughly between 0.71 and 0.78 [29] with varying solar irradiance conditions, since V_{OC} and the output power changes with light intensity. For a TEG, with varying degrees of temperature differential (ΔT), V_{MPP} is roughly 50% of V_{OC} [1]. Hence for MPP operation,

$$V_{MPP} = kV_{OC} \tag{2.7}$$

Where, k varies from 0.71-0.78 in the case of solar cells while it is approximately 0.5 for TEGs. Thus, k needs to be determined empirically by characterizing a TEG or a solar cell under varying environmental conditions. Once k is known, V_{MPP} can be computed and the output voltage of a TEG/solar cell can be compared with V_{MPP} using an on-chip comparator to determine whether the system operates at MPP. Although this method provides a low-cost, low-power solution, it is not accurate with changing environmental conditions. For instance, in solar-energy harvesting, k varies significantly with environmental conditions, such that the system operates at near-MPP but not at the actual MPP. Additionally, if the system needs the capability to harvest from multiple harvesting modalities, different values of k are necessary which need to be adjusted dynamically resulting in a more complicated implementation, which might consume higher power.

Fractional Short-Circuit Current This method is similar to the fractional open-circuit voltage method but this scheme leverages short circuit current (I_{SC}) instead of open-circuit voltage (V_{OC}) to estimate the MPP. Just like the fractional open circuit voltage method, the current supplied during MPP (I_{MPP}) is a fraction of I_{SC} and this fraction needs to be empirically evaluated. However, measuring I_{SC} during operation can be difficult because a separate control scheme is needed to periodically short-circuit the harvester and a current sensor is needed to measure I_{SC}, which increases the number of components and cost.

Most of the above techniques have been implemented in ULP energy harvesting systems.

The MPPT circuit in [15] uses a fractional open-circuit voltage method and assumes that the MPP of a TEG is 50% of the open-circuit voltage [1] while the MPP of a solar cell is 73-80% of the open-circuit voltage [29]. The MPPT circuit in [15] uses an external resistive divider to sample the MPP voltage (V_{MPP}). When the boost converter is functional, the energy source is loaded and its output voltage, V_{IN} goes down. An on-chip comparator monitors V_{IN} and compares it with V_{MPP}. As soon as V_{IN} is less than V_{MPP}, the comparator issues a signal to disable the boost converter, such that the energy source is again unloaded and V_{IN} rises. Again, when V_{IN} is greater than V_{MPP}, the comparator issues a pulse to engage the boost converter and the cycle is repeated. A similar method for MPPT is proposed in [16]. In [30], the switching frequency is tuned using digital circuits to modulate the input impedance of the boost converter. The disadvantage of this method is that the frequency range is limited. Hence, the range over which the input impedance of the converter can be tuned, is limited.

2.2.3 Converter topologies

Inductor-based switched-mode boost converters

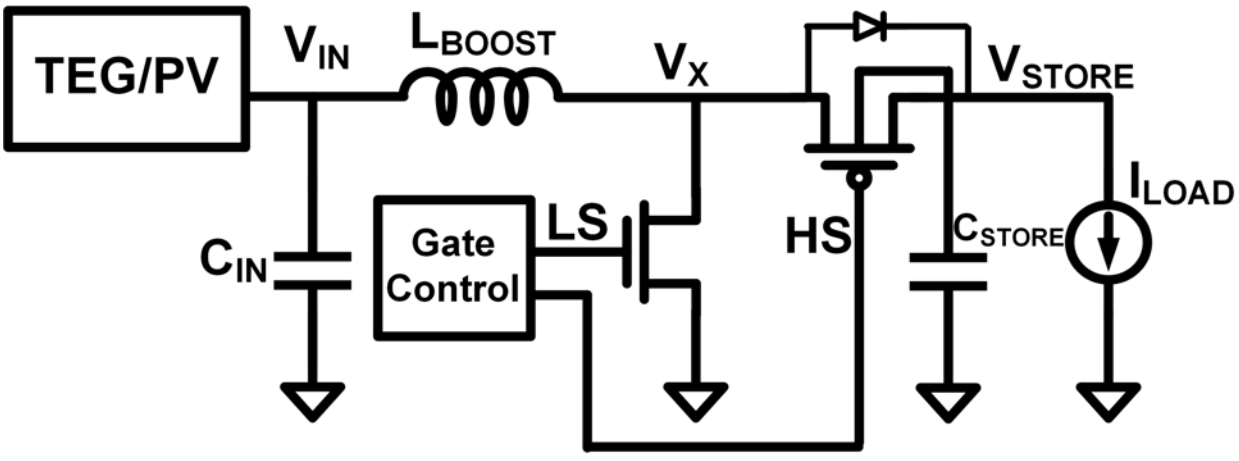


Figure 2.5: Powertrain of an inductor-based boost converter with synchronous rectification

Figure 2.5 shows the powertrain of a conventional inductor-based boost converter. It consists of an off-chip inductor (L_{BOOST}), a Low-Side (LS) and a High-Side (HS) on-chip

power transistor (denoted by M_{LS} and M_{HS} respectively). The energy source, such as a TEG or a solar cell is connected to the input, V_{IN} and the harvested energy is accumulated on a storage capacitor, charging it up to V_{STORE}. The storage capacitor supports the load current of the system, I_{LOAD}. The on-chip control circuits generate pulse-width modulated (PWM) or pulse-frequency modulated (PFM) pulses at the gates of M_{LS} and M_{HS} to transfer power from V_{IN}. Based on V_{IN} and I_{LOAD}, the converter operates either in Discontinuous Conduction Mode (DCM) or Continuous Conduction Mode (CCM). At ultra-low power levels, the boost converter mostly operates in DCM. The operation in DCM can be divided into two phases: LS and HS. In the LS phase, M_{LS} is enabled by the Pulse Width Modulation (PWM) or PFM modulated pulse and the inductor current ramps up, thereby storing energy in the inductor. As a first order approximation, neglecting the parasitic DC resistance of the inductor and assuming that M_{LS} has negligible voltage drop, we have:

$$L\frac{di}{dt} = V_{IN} \tag{2.8}$$

$$L\int_0^{I_{PEAK}} di = V_{IN}\int_0^{T_L} dt \tag{2.9}$$

$$T_L = L\frac{I_{PEAK}}{V_{IN}} \tag{2.10}$$

Where L = L_{BOOST};

I_{PEAK} = peak inductor current in the inductor;

T_L = ON-time of the LS power transistor which is governed by the pulse width of the LS pulse.

In the HS phase, the peak inductor current ramps down to zero and the stored energy in the inductor is delivered to the load through M_{HS} by synchronous rectification. In the HS phase, it is important that M_{HS} turns off when the inductor current reaches zero. If M_{HS} turns off when the inductor current changes direction, then V_{STORE} is discharged due to reverse conduction. If M_{HS} turns off early then the node, V_X goes high turning on the

p-n junction diode of M_{HS} and the extra energy is dumped across the diode. In either case, there is a loss in efficiency as some amount of energy is lost either during reverse conduction or wasted across the diode. Ignoring parasitic DC resistance of the inductor and assuming negligible voltage drop across M_{HS} we have:

$$L\frac{di}{dt} = V_{IN} - V_{STORE} \tag{2.11}$$

$$L\int_{I_{PEAK}}^{0} di = (V_{IN} - V_{STORE})\int_{0}^{T_H} dt \tag{2.12}$$

Thus in an ideal case, the boost conversion factor is given by:

$$\frac{V_{STORE}}{V_{IN}} = 1 + \frac{T_L}{T_H} \tag{2.13}$$

where, T_L is the ON-time of M_{LS}, which is governed by the pulse width of the Line Sensitivity (LS) pulse and

T_H is the ON-time of M_{HS}, which is governed by the pulse width of the HS pulse.

Hence, by modulating T_L and T_H, the required voltage gain can be achieved. However, in 2.13, the conduction losses in the inductor and power transistors as well as the switching losses are not accounted. The total conduction loss during the LS cycle, $E_{CN,L}$ as given by [15] :

$$E_{CN,L} = \int_{0}^{I_{PEAK}} i^2 R_L \frac{L}{V_{IN}} di = \frac{I_{PEAK}^3 L R_L}{3V_{IN}} \tag{2.14}$$

where, R_L is the total resistance including the parasitic resistance of the inductor and the ON resistance of M_{LS}.

Similarly, for the HS cycle, the total conduction loss, $E_{CN,H}$ is given by:

$$E_{CN,H} = \frac{I_{PEAK}^3 L R_H}{3(V_{STORE} - V_{IN})} \tag{2.15}$$

where, R_H is the total resistance including the parasitic resistance of the inductor and the

ON resistance of M_{HS}.

The switching loss, E_{SW} and leakage, E_{LKG} is generally constant for a given control scheme and depends on the dimensions of M_{LS} and M_{HS} [15]. Hence, the total loss is given by:

$$E_{LOSS} = E_{CN,H} + E_{CN,L} + E_{SW} + E_{LKG} \tag{2.16}$$

In DCM mode, the sources of energy loss are due to conduction loss in the inductor and power Field Effect Transistor (FET)s as well as switching loss due to charging-discharging of the gate capacitance and gate-drive circuits of the power FETs. Subthreshold leakage also contributes significantly to the loss, especially when the load currents are extremely small. For ultra-light load systems, such as [31], the leakage and switching loss are more dominant than the conduction loss. Hence in [31], a charge-pump based voltage doubler circuit is proposed in the control scheme to super cut-off the power FETs, resulting in 53% efficiency at 1.2nW load with 544pW of quiescent power being consumed by the converter. In [6], the boost converter, operating in DCM can harvest energy from a TEG with an open-circuit voltage as low as 20mV. To achieve zero crossing detection, a comparator is used to monitor the V_X node and a counter keeps track of the ON-time of the HS power FET. In [32], a multi-modal energy harvesting scheme is proposed which can harvest from TEG, solar or piezoelectric energy harvesting modalities by using a shared inductor scheme. The inductor is multiplexed among multiple harvesting modalities and a dual-path approach is implemented in the powertrain architecture to support a wide range of load currents. In [15], a peak inductor current control scheme is implemented to optimize conduction and switching loss. A fast zero crossing detector with offset compensation is implemented for synchronous rectification. The boost converter in [15] can harvest from a TEG with an open-circuit voltage as low as 10mV and achieves a peak efficiency of 83%. Another important requirement in self-powered energy harvesting systems is that the system needs to be self-starting. Since the output voltage provided by a TEG is below 100mV under ambient conditions, a start-up

scheme is necessary to power the control circuits and enable energy harvesting. The start-up scheme does not need to have a very high efficiency as it is only needed to start the control circuits. There are several start-up techniques discussed in the literature, which leverage technology, process, external kick-start and ambient RF energy to enable start-up. In [15], an on-chip cold-start circuit and an external RF-kickstart mechanism are leveraged to power the control circuits during start-up. The cold start circuit consists of a ring oscillator and a voltage-doubler to generate the control signals for the boost converter to start energy harvesting. The RF-kickstart circuit consists of an RF switch and a broadband rectifier implemented using the Dickson topology and operates in the subthreshold regime. A similar RF-kickstart mechanism is described in [31]. In [30], a mechanically assisted switch is used in an auxiliary boost converter topology to begin energy harvesting and charge a storage capacitor. The auxiliary boost converter with the mechanically assisted switch is disabled when the voltage on the stored capacitor is high enough to power the control circuits of the primary boost converter. In [33], an external transformer and a low-V_{th} NMOS transistor is connected to incorporate positive feedback, such that device noise is able to start oscillations, which are used to transfer and build-up energy on a storage capacitor. In [34], an LC tank oscillator is used for low-voltage DC to AC conversion followed by a voltage multiplier to boost and rectify the AC signal to a higher DC voltage for start-up.

Charge Pumps and Switched-Capacitor topologies

Charge pumps and switched-capacitor based architectures provide a fully integrated solution. An arrangement of Complementary Metal Oxide Semiconductor (CMOS) switches, controlled by clock signals (which are mostly out-of-phase but can be poly-phase) along with charge storage and transfer capacitors form a network known as a Switched Capacitor Network (SCN). One of the key goals is to optimize the overall output impedance of a switched-capacitor based converter. Figure 2.6 shows a simple first-order model of a switched-capacitor converter with a DC voltage gain of N. The voltage drop across the output impedance, R_O models all the

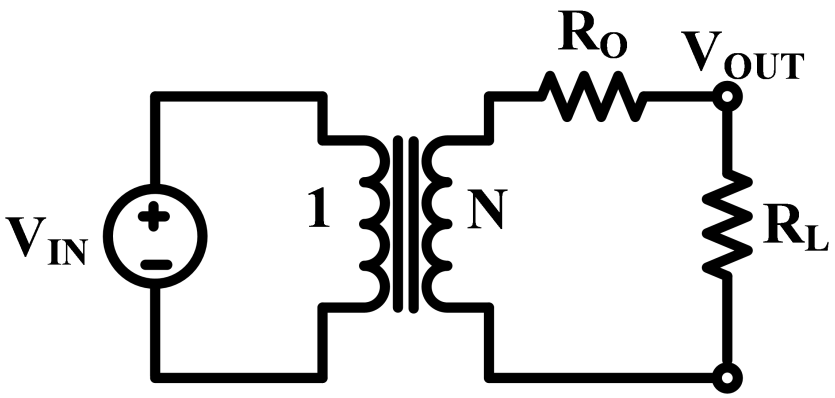


Figure 2.6: Model of a switched capacitor converter [5]

conversion losses such as conduction losses in the switches and during charge re-distribution. Additional switching loss in the gate-driver circuits, short-circuit currents due to overlapping control signals and bottom plate parasitic capacitances can be incorporated into this model. There are two asymptotic limits to the output impedance based on the switching frequency of the control signals. The Slow Switching Limit (SSL) impedance is calculated under the assumption that the switch and interconnect resistances are negligible and accounts for the loss due to charge re-distribution in the transfer capacitors. The Fast Switching Limit (FSL) impedance accounts for the conduction loss through the switch and other resistive components. The SCN topology plays a major role in both the SSL and FSL impedance estimations. The conduction losses due to SSL and FSL impedances [35] are denoted by:

$$P_{SSL} = \frac{I_{LOAD}^2}{M_{CAP} C_{FLY} F_{SW}} \tag{2.17}$$

$$P_{SSL} = \frac{I_{LOAD}^2 R_{ON} M_{SW}}{W_{SW}} \tag{2.18}$$

where, I_{LOAD} is the load current;

F_{SW} denotes the switching frequency of the control signals;

M_{CAP} and M_{SW} are constants determined by the topology;

R_{ON} is the ON resistance density measured in Ω.m

and W_{SW} denotes the total width (in m) for all switches.

Apart from conduction loss in the switches and transfer capacitors, there are shunt losses due to switching of bottom plate parasitic capacitance associated with the flying capacitors. Generally, Metal-Insulator-Metal (MiM) capacitors have lower bottom plate parasitics as compared to the gate capacitance of MOS devices. Power loss due to parasitic bottom-plate capacitors (P_{BOTT}) is given by [35]:

$$P_{BOTT} = M_{BOTT} V_O^2 C_{BOTT} F_{SW} \tag{2.19}$$

where, M_{BOTT} is determined from the topology;
V_O is the voltage swing across the bottom plate parasitic capacitor and
C_{BOTT} is the total bottom plate parasitic capacitance.
There are also switching losses (P_{GATE}) associated with the gate capacitance of transistors in the clocked-control circuit [35] which generate out-of-phase non-overlapping clocks for charge transfer and are expressed by:

$$P_{GATE} = W_{SW} V_{SW}^2 C_{GATE} F_{SW} \tag{2.20}$$

Where, V_{SW} denotes the voltage swing;
C_{GATE} is the gate capacitance density (F/m).
Thus, the total loss (P_{LOSS}) in any switched-capacitor based converter that needs to be minimized is given by:

$$P_{LOSS} = P_{SSL} + P_{FSL} + P_{BOTT} + P_{GATE} \tag{2.21}$$

Thus, for a given input voltage (V_{IN}), load current (I_{LOAD}), output ripple and the desired conversion ratio, it is important to select an appropriate topology, switching frequency and the number of clock phases for maximum efficiency. The area allocation for the switches and capacitors along with parameters such as bottom plate parasitic capacitance and the

switch resistance per unit width, play an important role in realizing the peak efficiency of a switched-capacitor power converter. In [36], an integrated charge pump with a variable number of stages and a constant switching frequency per stage is used to obtain a peak efficiency of 70% and support a wide range of input power levels ranging from 10-1000μW. In [37], the authors have proposed a fully integrated self-oscillating switched-capacitor based energy harvester with 9X-23X configurable voltage conversion ratios. In [37], voltage doublers have been cascaded. Clock generation and level-shifting functions of the control scheme within each doubler are implemented using a self-oscillating architecture, eliminating the need for power-hungry ring oscillators and clock generation circuits. A leakage-based delay element allows frequency control for a wide range of load varying from 5nW-5μW with 40% efficiency and less than 3nW static power consumption.

2.3 Single inductor Boost converter with adaptive peak inductor current control

The electrical characteristics of indoor solar modules and TEGs vary considerably with environmental conditions. For instance, in wearable systems with a form-factor of $1cm^2$, the open-circuit voltage, in case of TEGs can vary in the order of tens of milivolts whereas solar cell modules can provide an open-circuit voltage in the order of hundreds of milivolts [3]. Moreover, in battery-less systems, the role of an energy buffer to meet peak current demands of the system is mostly performed by a low-leakage supercapacitor. Unlike a battery, the voltage on this energy storage node can vary significantly due to change in environmental conditions, power consumed by the system in various operating modes etc. Thus to harvest energy from sources with varying electrical characteristics, such as open-circuit voltage, instantaneous power and varying voltage levels on the storage node, a single-inductor-based Boost converter provides an attractive solution for the powertrain architecture. This section presents a single inductor boost converter which can harvest energy from both indoor solar

and TEGs. Figure 2.7 shows the system architecture of the power converter. Designed to

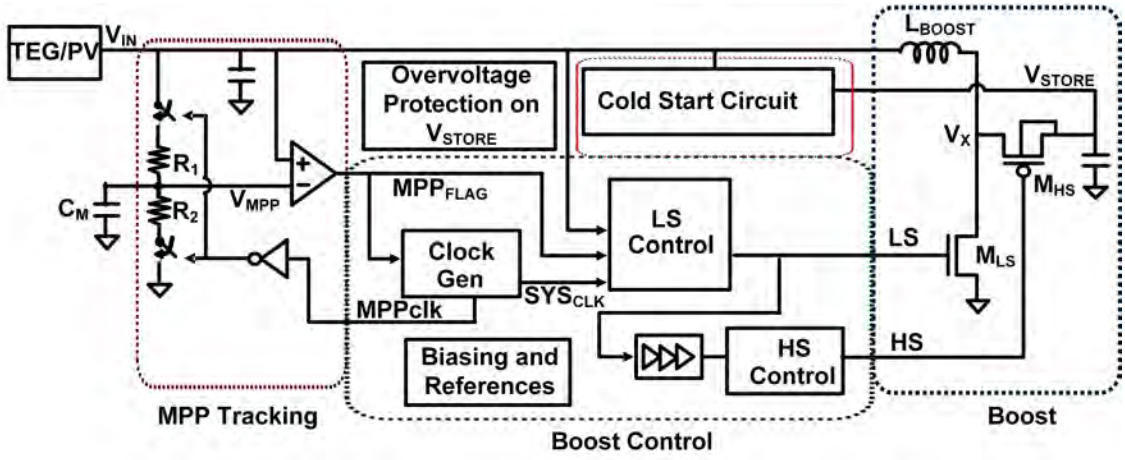


Figure 2.7: System architecture of the boost converter with MPPT, peak inductor current control, synchronous rectification and cold start circuit

operate in DCM, it employs an adaptive peak inductor current current control along with a PFM control loop for achieving high power efficiency across a wide range of conversion ratios. In order to extract maximum power under different environmental conditions, a fractional open circuit voltage MPPT circuit with programmable refresh rate is presented. For synchronous rectification, an all-digital controller is presented which achieves a faster convergence in zero crossing detection. Finally, a low-voltage fully-integrated cold-start circuit is presented.

2.3.1 Design knobs for enhancing power efficiency in Boost Converters

Before designing the control circuits for a single-inductor boost converter it is important to have a solid understanding of the design knobs to enable high power conversion efficiency. This section extends the power conversion loss mechanisms in context of a single inductor boost converter presented in Section 2.2.3. From Equations 2.14, 2.15 and 2.16, we have

$$E_{LOSS} = \frac{I_{PEAK}^3 L R_L}{3V_{IN}} + \frac{I_{PEAK}^3 L R_H}{3(V_{STORE} - V_{IN})} + E_{SW} + E_{LKG} \tag{2.22}$$

Now, efficiency, η can be depicted by:

$$\eta = \frac{E_{IN} - E_{LOSS}}{E_{IN}} = 1 - \frac{E_{LOSS}}{E_{IN}} \tag{2.23}$$

where E_{IN} is the energy transferred to the inductor in a single switching cycle i.e.

$$E_{IN} = 0.5LI_{PEAK}^2 \tag{2.24}$$

From Equation 2.23, for maximum efficiency it is important to minimize $\frac{E_{LOSS}}{E_{IN}}$. From Equations 2.22 and 2.24,

$$\eta_L = \frac{E_{LOSS}}{E_{IN}} = \frac{I_{PEAK}}{1.5V_{IN}}\left(R_L + \frac{R_H}{\frac{V_{STORE}}{V_{IN}} - 1}\right) + \frac{E_{SW} + E_{LKG}}{0.5LI_{PEAK}^2} \tag{2.25}$$

Differentiating η_L with respect to I_{PEAK} and setting $\frac{d\eta_L}{dI_{PEAK}} = 0$, we get

$$I_{PEAK,OPT} = \left[6\frac{(E_{SW} + E_{LKG})V_{IN}}{L(R_L + \frac{R_H}{\frac{V_{STORE}}{V_{IN}} - 1})}\right]^{\frac{1}{3}} \tag{2.26}$$

Equation 2.26 provides an important design insight that to achieve a wide-range power conversion efficiency using a single inductor boost converter with synchronous rectification, the peak inductor current (I_{PEAK}) needs to be controlled as a function of both the voltage at the input (V_{IN}) as well as the voltage on the storage node (V_{STORE}). It has been observed that V_{IN} is mostly a function of the harvester (solar or TEG) configuration , environmental conditions (light intensity for solar, temperature differential for TEG) and size. Similarly, the voltage level on the storage node (V_{STORE}) is dependent on the electrical characteristics such as energy density, leakage, shunt resistance, temperature etc. of the device being used (Supercapacitor or re-chargeable battery) for storage. Thus, in order to maximize efficiency(or minimize η_L), the peak inductor current needs to be controlled in an adaptive fashion with variations in V_{IN} and V_{STORE}. High values of I_{PEAK} would cause efficiency to reduce

linearly whereas low values of I_{PEAK} will result in a quadratic reduction in efficiency. Figure

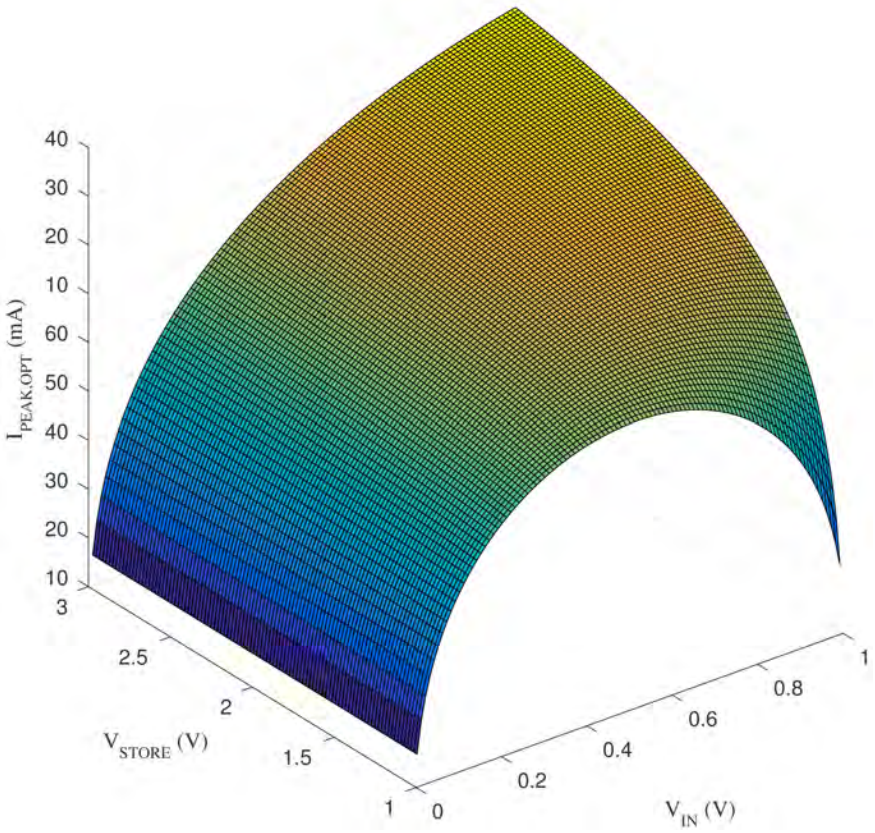


Figure 2.8: Variation of optimum peak inductor current ($I_{PEAK,OPT}$) with input voltage of the harvester (V_{IN}) and voltage on the storage node (V_{STORE}). Values of other parameters are: $R_L = 0.269\Omega$,$R_H = 0.247\Omega$, $E_{SW} = 99$pJ, $E_{LKG} = 1.5$pJ

2.8 shows the variation of the optimum value of I_{PEAK} as a function of both V_{IN} and V_{STORE} as given by Equation 2.26. The values of R_L, R_H, E_{SW}, E_{LKG} are derived from [15]. Reducing switch resistances, R_L and R_H will lower the conduction loss as given in Equations 2.14 and 2.15. However, employing wide transistors to reduce the ON resistance will increase the input capacitance of these devices resulting in higher switching loss (E_{SW}). Employing a lower-V_{th} device will increase leakage (E_{LKG}). Thus the switches need to be carefully sized to account for trade-offs between conduction, switching and leakage related loss mechanisms. From Equations 2.25 and 2.26, it can be observed that using a bigger inductor reduces η_L ($\eta_L \propto L^{\frac{-1}{3}}$) to a first order. However, a bigger inductor will also have higher ESR in series with R_L and R_H, resulting in higher conduction loss. Thus it is important to choose an

inductor with a low ESR. The inductance sets the peak inductor current during the boost converter operation (Equation 2.26). A higher inductance will have a lower I_{PEAK} and for a given switching frequency and load current may push the converter operation towards continuous conduction. Another factor to consider when choosing an inductor is its saturation current (I_{SAT}) limit (i.e. the current at which the rated inductance value tends to roll-off). For a given system, the range of optimum peak inductor current ($I_{PEAK,OPT}$), across V_{IN} and V_{STORE} should be lower than the I_{SAT} limit of the inductor.

2.3.2 Fractional Open-Circuit Voltage Maximum Power Point Tracking scheme

In this architecture, we implemented a Fractional Open-Circuit Voltage (FOCV) MPPT scheme. The main motivation for using an FOCV approach over some of the other methods such as hill climbing discussed in Section 2.2.2 is that the the power profile of harvesters such as solar and TEG is maximally flat around the maximum power point (V_{MPP}). Figure 2.9

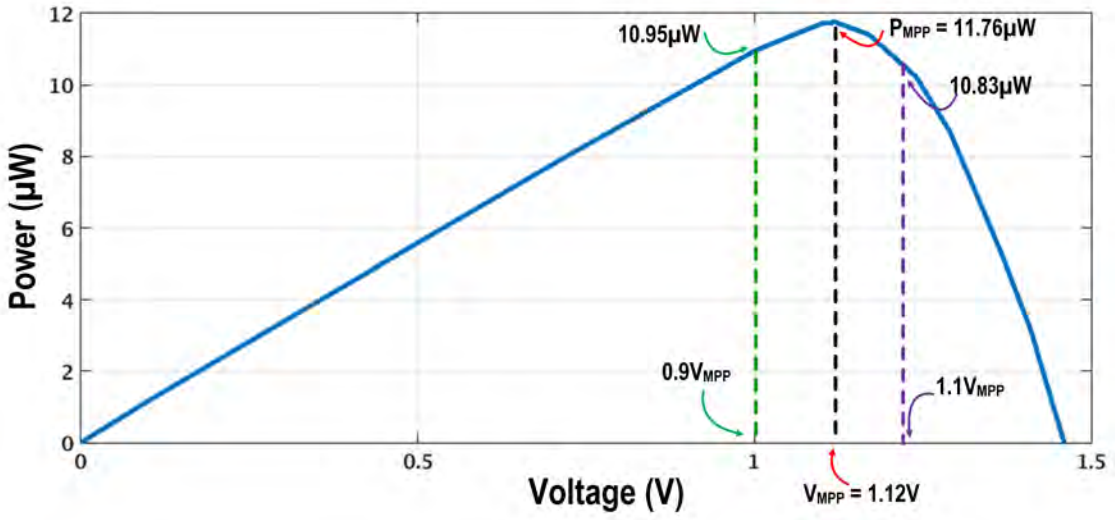


Figure 2.9: Power vs. voltage profile of an indoor PV cell characterized at 200lux showing variation in available power around the maximum power point

shows a power vs. voltage profile of an indoor solar cell characterized at a light intensity of 200lux. It can be observed that with a ±10% change in V_{MPP}, the corresponding change

in available power is 7%. For TEGs, this variation is less than 0.5% for a ±10% change in V_{MPP} [3]. Thus, given the flatness of the power profile around the maximum power point, precise computation of the maximum power point to a resolution of less than tens of milivolts is not necessary. More accurate algorithms such as incremental conductance and hill-climbing can provide accurate computation of MPPT at a cost of increased hardware complexity and power overhead. Given that the peak power from TEGs and indoor PV cells is limited to tens of μWs, implementing sophisticated algorithms such as incremental conductance method can be challenging. Additionally, since the size of the harvester is constrained to a few cm^2, the impacts of partial shading, temperature and its effects on the maximum power point are negligible[38]. Given the small size (few cm^2) and the power constraints (tens of μWs) of indoor solar modules and TEGs, the FOCV method provides a simple and attractive solution in terms of achieving higher conversion efficiency. Figure 2.10 describes the MPPT control

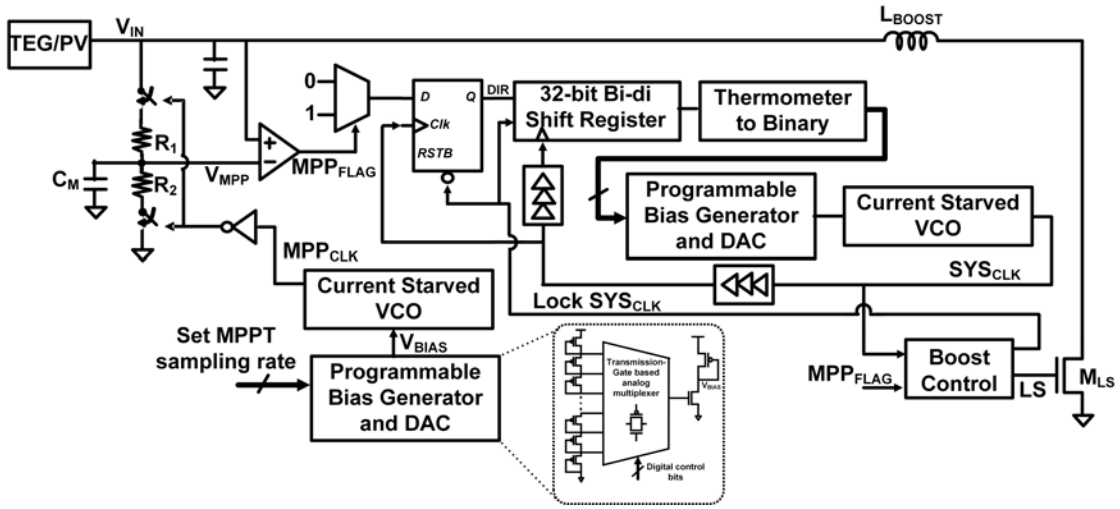


Figure 2.10: Fractional open-circuit voltage MPPT circuit with programmable refresh rate and PFM controller

scheme. The sampling network consists of two off-chip resistors, R_1 and R_2 which form a resistive divider and samples the open-circuit voltage of the harvester periodically and stores it on an off-chip storage capacitor, C_M. The sampled voltage, V_{MPP} is given by:

$$V_{MPP} = \frac{R_2 V_{IN}}{R_1 + R_2} \tag{2.27}$$

Hence resistors R_1 and R_2 must be chosen such that the resistive divider ratio is 0.5 for TEGs. For a solar cell, the ratio can be set to any value between 0.7-0.8. R_1 and R_2 are typically large ($>100k\Omega$) to reduce the ground current during sampling. The sampling switches and the capacitor, C_M need to have low-leakage for a correct estimation of the maximum power point using the FOCV method. Typically the time-constant associated with C_M should be longer than than the sampling rate. In this implementation, the sampling rate is programmable and can be set externally for a given application. For instance, if the environmental conditions are changing rapidly (e.g. motion), or C_M has higher leakage, a higher sampling rate can be set using a programmable bias generator which sets the bias voltage of a current starved VCO which generates the sampling signals for the switches. The sampling rate can vary from 0.1Hz to 1Hz. The converter employs a PFM control loop which works closely with the MPPT scheme. The role of the MPPT controller is to regulate V_{IN} to V_{MPP} by tuning the input impedance of the converter to match the output impedance of the harvester under changing environmental conditions or more generally to enable maximum power transfer. When $V_{IN} > V_{MPP}$, MPP_{FLAG} is set high. The system clock for the controller, SYS_{CLK} is derived from a current-controlled VCO and starts up at the lowest frequency limit. A digitally controlled bias generator sets the frequency of the VCO. A bi-directional shift register and a thermometer to binary encoder controls the bias generator. The direction of the shift is controlled by MPP_{FLAG}. Hence when MPP_{FLAG} is high, the switching frequency continues to increase until $MPP_{FLAG} = 0$ which occurs when $V_{IN} = V_{MPP}$. When $MPP_{FLAG} = 0$, the low-side switch, M_{LS} turns-OFF and the boost converter is essentially disconnected from the harvester and V_{IN} slowly rises. As soon as $V_{IN} > V_{MPP}$ ($MPP_{FLAG} = 1$), the boost controller sends a trigger signal to the PFM loop and locks the system clock frequency to the current switching frequency of the VCO.

2.3.3 Adaptive on-time circuit for controlling peak inductor current

The need to control I_{PEAK} with varying V_{IN} and V_{STORE} was discussed in Section 2.3.1. Equation 2.26 represents the value of I_{PEAK} as a function of V_{IN} and V_{STORE}. As discussed in Section 2.2.3, the peak inductor current depends on the ON-time (T_L) of the switch M_{LS} at a given V_{IN}. To achieve the optimal peak inductor current, $I_{PEAK,OPT}$ for achieving maximum efficiency for a specific V_{IN}, V_{STORE} pair, the optimal ON-time of M_{LS}, $T_{L,OPT}$ is given by:

$$T_{L,OPT} = L\frac{I_{PEAK,OPT}}{V_{IN}} \tag{2.28}$$

$$T_{L,OPT} = \left[6\frac{(E_{SW}+E_{LKG})L^2}{V_{IN}^2(R_L+\frac{R_H}{\frac{V_{STORE}}{V_{IN}}-1})}\right]^{\frac{1}{3}} \tag{2.29}$$

The circuit implementation to achieve $T_L = T_{L,OPT}$ is difficult and computationally expensive, especially in low-I_Q controller design. Figure 2.11 shows the proposed circuit implementation

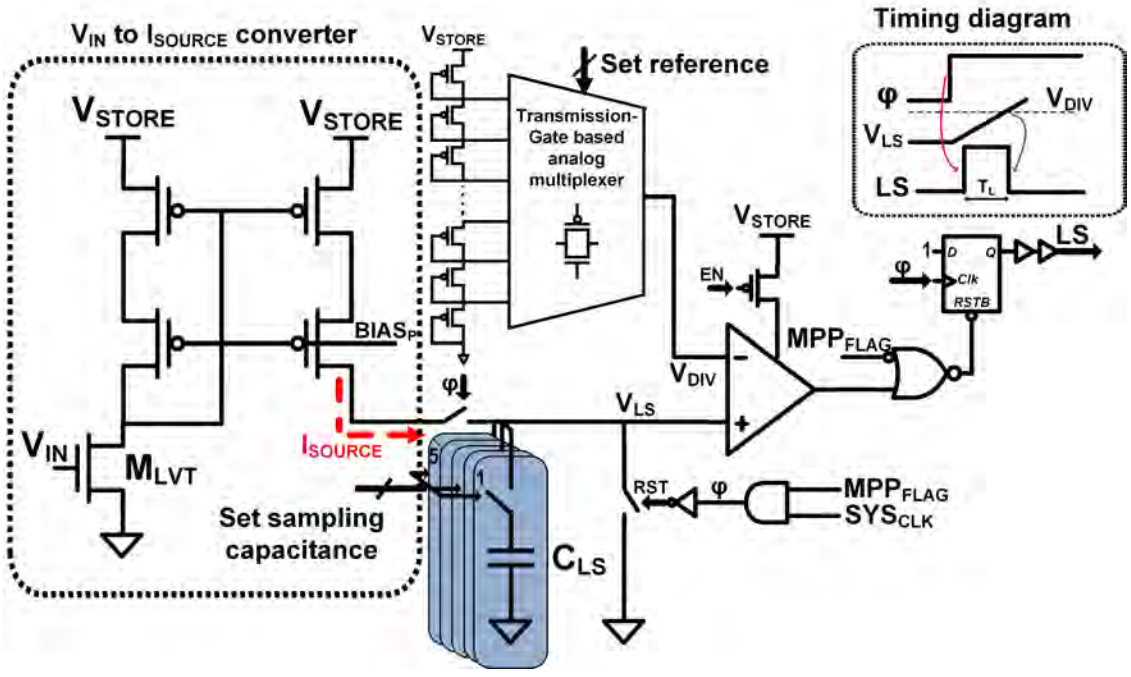


Figure 2.11: Low side control circuit with adaptive ON time control and associated timing diagram to modulate the peak inductor current

for adaptive ON-time control to modulate peak inductor current with changing V_{IN} and V_{STORE}. It consists of an input OTA stage to convert V_{IN} to a current, I_{SOURCE}. A cascode current mirror is used for its high output impedance. When ϕ goes high, the current I_{SOURCE} is used to charge a configurable capacitor bank, C_{LS}. Also, with the rising edge of ϕ, the LS switch is enabled and the inductor current starts to ramp. As the capacitor bank gets charged by I_{SOURCE}, the voltage on C_{LS} (V_{LS}) gets compared to a reference V_{DIV} which is derived from V_{STORE} ($V_{DIV} = k.V_{STORE}$ where k is defined as reference coefficient). A duty-cycled offset compensated comparator is used to compare V_{LS} with V_{DIV}. When $V_{LS} > V_{DIV}$, the comparator toggles and resets the LS control signal to set the peak inductor current. The ON-time of the LS switch is given by:

$$T_L = \frac{C_{LS}.kV_{STORE}}{I_{SOURCE}} \tag{2.30}$$

The transistor M_{LVT} can be biased either in weak-inversion or strong-inversion depending on V_{IN}. Hence, I_{SOURCE} is given by:

$$I_{SOURCE} = \begin{cases} \frac{\beta}{2}(V_{IN} - V_{th,LVT})^2 & V_{IN} > V_{th,LVT} \\ \beta(\eta - 1)V_T^2 \exp[\frac{V_{IN} - V_{th,LVT}}{\eta V_T}] & V_{IN} < V_{th,LVT} \end{cases}$$

Where,

$V_{th,LVT}$= Threshold voltage of M_{LVT}

$\beta = \mu C_{ox} \frac{W}{L}$

μ = mobility of carriers

C_{ox} = gate oxide capacitance per unit area

$\frac{W}{L}$ = device aspect ratio

η = capacitive coupling between the gate of M_{LVT} and silicon surface

V_T = thermal voltage

To compensate for temperature variations, device mismatch and process variations, the

capacitor bank can be configured using programmable digital control bits to set the overall C_{LS}. To account for variations in I_{SOURCE}, the reference coefficient, k can be controlled externally. To reduce errors in computing I_{PEAK}, the comparator needs to have a low-input offset which is achieved by auto-zeroing. Additionally, the propagation delay of the comparator needs to be small (high bandwidth). The comparator is duty-cycled to reduce standby power of the ON-time controller. Figure 2.12 compares the simulated results of $I_{PEAK,OPT}$ obtained from the proposed circuit in Figure 2.11 with Equation 2.26 across different values of V_{STORE}. The reference coefficient k and C_{LS} is configured to reduce process and temperature induced variation in $I_{PEAK,OPT}$ across V_{STORE} ranging from 1.5-3V .

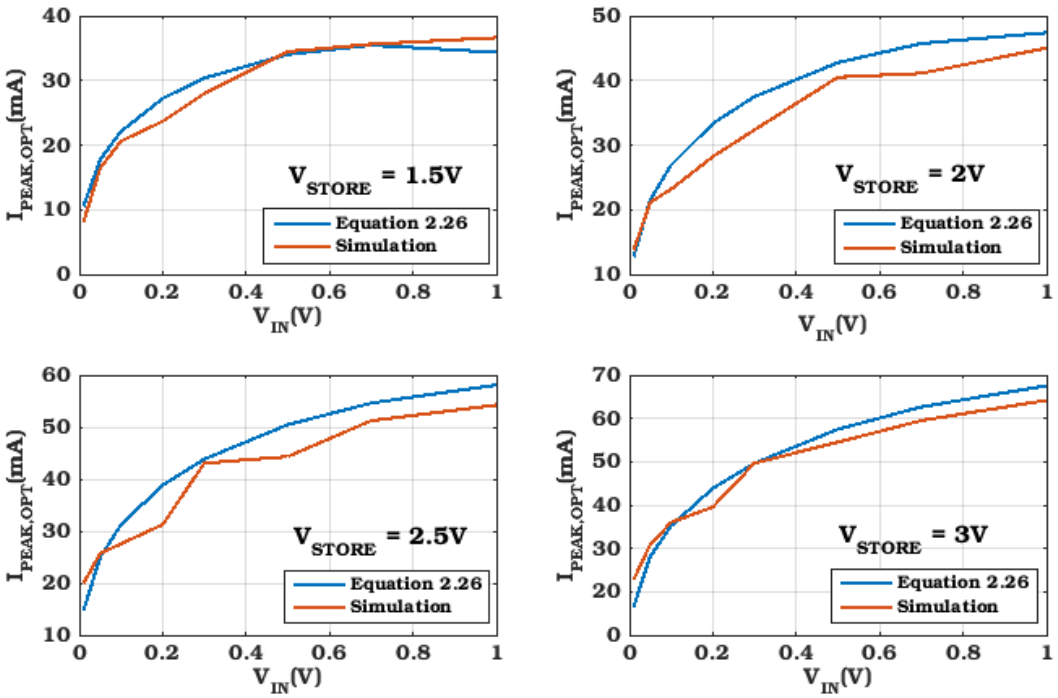


Figure 2.12: Comparison of variation in $I_{PEAK,OPT}$ in simulation and as proposed in Equation 2.26 across different values of V_{STORE}

2.3.4 Zero crossing detection during synchronous rectification

As discussed in Section 2.2.3, an inductor-based boost converter can either operate in Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM). In CCM,

the inductor current ripple (ΔI) is less than the DC component of the inductor current(I_{IN}) whereas in DCM, $\Delta I > I_{IN}$. (Figure 2.14) Thus, while transferring energy from the inductor to the storage node at ultra-light loads, if the boost converter operates in CCM, the inductor current can go negative (for a fixed size of the inductor and switching frequency) (Figure 2.14). A negative inductor current discharges the storage capacitor, reducing the efficiency at light loads which is undesirable. If a diode is used as the HS switch during energy transfer (Figure 2.13), the forward voltage drop of the diode limits the efficiency. Operating in DCM and using a HS power transistor for energy transfer provides the best power conversion efficiency at light loads, with similar sized inductor and switching frequency but requires accurate detection of the inductor current zero-crossing. Thus, the challenge is to synchronize the HS switch with the moment the inductor current falls to zero (T_H in Section 2.2.3) Figure 2.15 describes the synchronization issues related with closing the HS switch and zero crossing of the inductor current. When the switch closes before the inductor current crosses zero, the body diode (Figure 2.13 (c)) starts conducting because the inductor current cannot change polarity instantaneously. Although the storage node (V_{STORE}) still gets charged but additional conduction loss occurs with the diode turning ON. When the switch closes after the inductor current crosses zero, the polarity of the inductor current is reversed and the storage node is drained. Thus precise synchronization is required between inductor zero crossing and ON-OFF control of the HS switch to achieve the correct functionality and higher performance.

To achieve synchronization, typically a feedback loop is required to drive the inductor zero crossing close to the turn-OFF instant of the PFET switch. Prior work in literature have looked into low-latency($< 40ns$) comparators to detect when the PFET becomes reverse-biased and subsequently trigger a pulse to turn-OFF the PFET switch [39]. A continuous always-ON, high bandwidth comparator will consume high quiescent power. Duty-cycling a high-bandwidth, low input-referred offset comparator for synchronous rectification has been proposed [40] but such an architecture still consumes higher quiescent power ($> 10\mu W$)

especially in converters employing adaptive ON-time control(with a wide range of $I_{PEAK,OPT}$). The loop delay of the feedback network needs to be extremely low as significant latency during detection can cause the inductor current to change polarity in the negative direction severely limiting functionality and performance. A systematic offset can be introduced during comparison [41] to counter degradation in latency but this method is sensitive to variations in the slope of I_{FALL} (Figure 2.15) which primarily depends on V_{IN}, V_{STORE} and the size of the inductor.

This section presents an all-digital adaptive correction-based technique for zero crossing detection. As described in Figure 2.15, when the PFET switch is turned OFF before the inductor current crosses zero, the voltage on the switching node, V_X goes high as the body diode starts conducting. If the PFET switch is turned OFF after the inductor current switches polarity, the voltage on V_X will fall very quickly. Thus by detecting the logic-level of V_X, it can be determined whether the switch was turned OFF before or after the inductor current falls to zero. The ON-time of the PFET switch is modulated using a delay line, such that during each switching cycle, the synchronization error, T_{ERR} is minimized incrementally. Figure 2.16 describes the implementation of the controller for zero crossing detection. When the low-side switch, M_{LS} is turned-OFF, the high-side switch, M_{HS} is turned-ON after a fixed delay known as deadtime delay. This is required to prevent simultaneous conduction of M_{LS} and M_{HS} which can drain energy from the storage node.The gate-control signal for M_{HS} (ϕ_{HS}) is essentially derived from the gate control signal of M_{LS} (ϕ_{HS}). The pulse-width of ϕ_{HS} (T_P) is modulated to ensure synchronization between ϕ_{HS} and zero crossing of the inductor current. A pulse generator derived from ϕ_{HS} and a low-input offset clocked comparator is used to evaluate whether the voltage on the switching node, V_X is higher or lower than the voltage on the storage node, V_{STORE}. If $V_X > V_{STORE}$, T_P is lower than the optimal on-time necessary to ensure zero crossing. The comparator decision is used to control the direction of a 32-bit bidirectional shift register. The output word of the shift register is used to control a digitally controlled delay line with coarse resolution. The delay line is used to

increase or decrease T_P to reduce the error between the current ON-time and the optimal ON-time ($T_{P,OPT}$) of M_{HS}. To ensure faster convergence of T_P to $T_{P,OPT}$ and reduce the severity of limit-cycle oscillations, second order compensation is added by using a duty-cycled, high-bandwidth, offset compensated comparator which is used in parallel with the clocked comparator and controls a vernier Time-to-Digital Converter (TDC). The output word of the TDC is used to control a low-resolution delay line to enable fine-grained control of ϕ_{HS}. Thus, this method proposes an adaptive, per-cycle correction-based technique for computing the optimal ON-time of M_{HS} and ensure zero crossing detection. Since this scheme uses mostly digital logic, the static power overhead is lower than implementations employing majority analog circuits and is therefore suitable for low-power energy harvesting.

2.3.5 Fully-integrated low voltage cold-start mechanism

This section presents an implementation of a low-cost, fully-integrated cold-start mechanism for the boost converter. As described briefly in Section 2.2.3, multiple start-up techniques have been proposed in the context of energy harvesting from ambient sources and batteryless systems. Most techniques leverage external components e.g. external transformer [33], alternate energy sources e.g. RF [15] or technology e.g. MEMS switches [30]. Although such techniques allow a lower start-up voltage but also increase the design-complexity, size and overall cost of the system.

The goal of the cold-start circuit is to begin harvesting and transfer energy to the storage node from low-voltage TEGs/PV cells. If the cold-start circuit can harvest from extremely low-voltage levels, the size of the harvester can be scaled but there is a trade-off with the size of the external component or device (e.g. transformer), which enables the cold-start mechanism. Power efficiency is not critical during start-up because the focus is on charging the storage node to a voltage where the primary converter controller can be operational. Another design consideration during start-up is that the load on the boost converter should be as low as possible. For instance, a storage device with high-leakage (greater than the

power envelope of the harvester) can inhibit start-up. Apart from choosing a low-leakage storage device e.g. a super-capacitor, it should be ensured that the loads e.g. regulators, voltage monitors etc. are decoupled from the storage node during start-up.

Figure 2.17 describes the architecture of the cold-start circuit. Initially, during start-up, the logic-level of the signal RST is low which decouples the load from the storage device. The signal, RST also controls a nine-stage ring oscillator powered by the harvester directly. Since the ring oscillator generates the control signals to enable harvesting during start-up, it is essential that the ring-oscillator is operational from a low-supply voltage. Recent work on low-voltage circuits have proposed a Schmitt Trigger based logic family which is operational from 62mV by improving $\frac{I_{ON}}{I_{OFF}}$ ratios at low supply voltages. [42]. A Schmitt Trigger inverter [42] is used as the gain stage of the ring oscillator which provides two non overlapping signals, ϕ and ϕ_B to a twenty-four stage Dickson Charge Pump to enable harvesting during start-up. The charge pump uses low-V_{th} devices as switches and MOS capacitors. Once the voltage on the storage node exceeds 1V, the POR and startup controller enables a sequenced turn-ON of the converter control and the load followed by turning-OFF the cold-start circuits. As described earlier, since the load on the storage node should be minimal at start-up, it is essential that the POR and the startup control logic consumes low static currents (ideally lower than the leakage of the storage device). A low-power POR circuit (Figure 2.17) was implemented and together with the control logic consumes only 300pW.

2.3.6 Measurement Results

A prototype was fabricated in 0.13μm technology to demonstrate energy harvesting from an indoor solar cell. A 30mm X 18mm PV cell from Jameco electronics with an open circuit voltage of 600mV and short circuit current of 20μA was used for characterization. A TEG can also be used as an energy transducer. A 10mF EDLC supercapacitor with an ESR of 500mΩ was used as a storage device. In this system, a re-chargeable battery can also be used for storage. Figure 2.18 demonstrates the measured functional waveforms for the inductor

current, I_{PEAK} and switched-node, V_X and the input voltage, V_{IN}. Adaptive I_{PEAK} control and PFM operation is shown as the harvester converges to the maximum power point, V_{MPP} which was set at 75% of the open circuit voltage after measuring the I-V characteristics of the PV cell. Ideal zero crossing is established after applying correction during each switching cycle. Figure 2.19 shows the inductor current zero crossing after correction. Based on the current measurement results, the system can harvest from an input voltage as low as 30mV. Figure 2.20 shows the measured efficiency as a function of the input voltage, V_{IN}. During this measurement, the voltage on the storage node, V_{STORE} was 2V. The peak efficiency was measured to be 90.7% at $V_{IN} = 1$V while the efficiency at the minimum input voltage ($V_{IN} =$ 30mV) was measured to be 47.8%. Figure 2.21 shows the die photo of the fabricated energy harvester chip. Table 2.2 compares the boost converter presented in this chapter with existing work in literature. An adaptive peak inductor current controller along with a low I_Q all-digital zero crossing detector, enabled during synchronous rectification causes a 2-10X reduction in quiescent power consumption resulting in a 7-10% benefit in peak efficiency at low input, low power levels ($< 20\mu$Ws). This 7-10% improvement in conversion efficiency and the ability to harvest from low input voltage levels (10mV) enables harvesting in poor environmental conditions (i.e. low illumination levels for photovoltaic, low temperature differential for TEGs etc.). Additionally, this work supports a maximum 3V on the storage device resulting in quadratic improvements in the maximum energy capacity of the system. Comparing with existing architectures which leverage a similar sized supercapacitor for storage, this work provides a 4X or CV^2 improvement in the overall energy capacity. In the absence of harvesting, this results in a V^2 or a 4X improvement in the overall lifetime, assuming a similar sized storage element with identical loads and leakage profiles.

Table 2.2: Comparison of the proposed boost converter with existing work

	[15]	[14]	[6]	[16]	**This Work**
Harvesting	TEG/solar	TEG	TEG	TEG/Solar	**TEG/solar**
Min V_{IN}	10mV	100mV	20mV	100mV	**10mV**
Max output voltage	1.2V Supercap	0.5V Supercap	1V Supercap	1.5V Supercap	**3V Battery/Supercap**
Integrated cold-start	✓	×	✓	✓	✓
Cold-start V_{IN}	220mV	-	600mV	330mV	**100mV**
I_Q	300nW	480nW	1μW	∼330nA	**162nW**
MPP tracking	✓	×	×	✓	✓
Peak efficiency	83%	83.4%	75%	80%	**90.7%**
Technology	0.13μm	0.18μm	0.13μm	0.18μm	**0.13μm**

2.4 Performance modeling framework for evaluating various Boost converter controller algorithms

In this section, a design methodology and tool flow is described to perform design space exploration for energy harvesting and other power conversion circuits. Figure 2.22 describes the tool flow.

System-level design specifications such as volume, power density etc. are used as inputs along with electrical specifications such as short-circuit current, open circuit voltage, I-V characteristics etc. to create behavioral models (in CSV or Verilog-A format) of harvesting sources such as TEGs and indoor solar cells. Similar models are created for storage devices such as a battery or a supercapacitor where additional parameters such as leakage and temperature can be taken into account. These behavioral models of the harvester and storage devices serve as an input to a Verilog-A/HSPICE® tool wrapper. Controller algorithms such as MPPT, peak inductor current control in case of inductor-based boost converters etc. can be implemented in Verilog-A and along with behavioral models of components such as comparators, VCOs etc. serve as an input to the Verilog-A/HSPICE® tool wrapper for design-space exploration. After applying the necessary run-time settings, the simulation results can be utilized to evaluate the performance of the different controller algorithms,

feasibility of various components and the overall dynamics of the system. Based on the simulation results such as power efficiency and the system-level design inputs, the user can estimate first-order design specifications of various components and the feasibility of the controller algorithms. Thus, this methodology provides useful design insight to the circuit designer before performing actual circuit design.

Additionally , even during the circuit design phase, the user can replace the behavioral models of the different circuit components to evaluate the performance incrementally and ensure that the system-level specifications are being met. We demonstrate the tool flow and design methodology in the context of a battery-less, self-powered system which needs to have the capability to harvest energy from TEGs/PV cells. Based on existing work in literature and design considerations of a wearable, self-powered system, the size and power density of the harvester was limited to $10cm^2$ and $1\frac{\mu W}{cm^2}$ respectively [3]. A TEG with an open circuit voltage of 30mV and short-circuit current of $50\mu A$ was used in this analysis. A low-leakage (200nA at 1V measured at room temperature) 10mF supercapacitor was assumed for storage. To harvest from low-input voltages, an inductor-based boost converter powertrain was chosen. The controller algorithms for MPPT, adaptive peak inductor current control and zero crossing detection described in Section 2.3 were modeled in Verilog-A. Behavioral models of analog components such as comparators, VCOs and DACs were used in describing the controller operation.

Figure 2.23 shows the functional waveforms of the system obtained from the model. Behavioral description of the different control algorithms were used to generate these results. Pulse frequency modulation and adaptive scaling of the peak inductor current for optimal power efficiency is shown in Figure 2.24. Figure 2.25 shows the MPPT operation. To evaluate the accuracy of the model, estimated, simulated and measured results of power efficiency of the boost converter is plotted in Figure 2.26a. Figure 2.26b shows the absolute error of simulated and modeled power efficiency as a function of the the input voltage. The mean error between simulated and estimated results from the model is around 4.15% and can be

improved, if necessary by more comprehensive behavioral description of the components, such as leakage, delay dependence of comparators on load, power supply variation etc. Overall, the model provides approximate trends for figures of merit such as efficiency and aids the circuit designer in taking design decisions and understanding the overall dynamics of the system.

2.5 List of Contributions

- Evaluated the different design knobs for single-inductor boost converter, operating in DCM. It was found that an adaptive peak inductor current control is necessary for achieving high power efficiency at varying input(10mV-1V) and output voltages(maximum 3V) and with varying power levels(500nW-50μW) available from the harvester(indoor solar or wearable TEG), which is common with changing environmental conditions and load current transients occurring during system operation.

- Introduced a low-power, fractional open-circuit voltage MPPT scheme. Programmable sampling rate(0.1-1Hz) of the Maximum Power Point (MPP) of the transducer is necessary depending on the application (e.g. motion) and leakage of the storage node, holding the MPP.

- Introduced an adaptive peak inductor current control circuit for achieving high power efficiency(90% at 1V and 48% at 30mV input) across varying input voltages(30mV-1V) and power levels. Achieved 7-10% improvement in conversion efficiency over [15] [6] translating to 7-10% improvement in usable energy and harvesting under poor harvesting conditions (low light, low ΔT). This is the first ever implementation of an adaptive peak inductor current control circuit which can support both re-chargeable batteries or supercapacitors for storage and TEG/PV for harvesting

- Presented a low-power, all digital zero crossing detection circuit. The digital implementation consumes an average power of 63nW achieving a ∼150X improvement over [40] and a ∼5X improvement over [30]

- Introduced a low-voltage, fully-integrated cold-start circuit. The minimum cold-start voltage is reduced by 50% as compared to [15]

- Introduced a performance modeling framework for evaluating boost converter/energy harvester architectures with different controller algorithms. The design methodology was shown for a single-inductor boost converter with PFM control and good correlation ($< 5\%$ error) with measured results was achieved.

2.6 Conclusion

This chapter motivates the need for energy harvesting as an alternate mechanism for powering battery-less self-sustaining systems catering to wearable IoT applications. The sources of energy harvesting were constrained to thermoelectric and photovoltaic energy and various aspects of the associated system interface was discussed in detail. An inductor-based boost converter was described which can be used for both TEG and solar harvesting. The system dynamics of a boost converter operating in DCM at ultra-low power levels was discussed. Control schemes, such as adaptive peak inductor current control, fractional open circuit voltage MPPT and a low-power zero crossing detector were described to obtain high power efficiency across a wide range of input-power levels to improve harvesting under poor or varying environmental conditions. A low-voltage cold start mechanism for chargers which use a supercapacitor for storage was discussed to enable efficient harvesting at low energy levels. Finally, a tool flow and design methodology was described which can be used to characterize various energy harvesting powertrain architectures and associated control schemes. The methodology assists a designer to make design decisions, develop intuition and a high level understanding of the system dynamics before proceeding with the actual circuit

implementation. Built around the SPICE® circuit simulation framework, the tool provides good accuracy and the flexibility to be used during design-space exploration as well as during various phases of the actual circuit implementation.

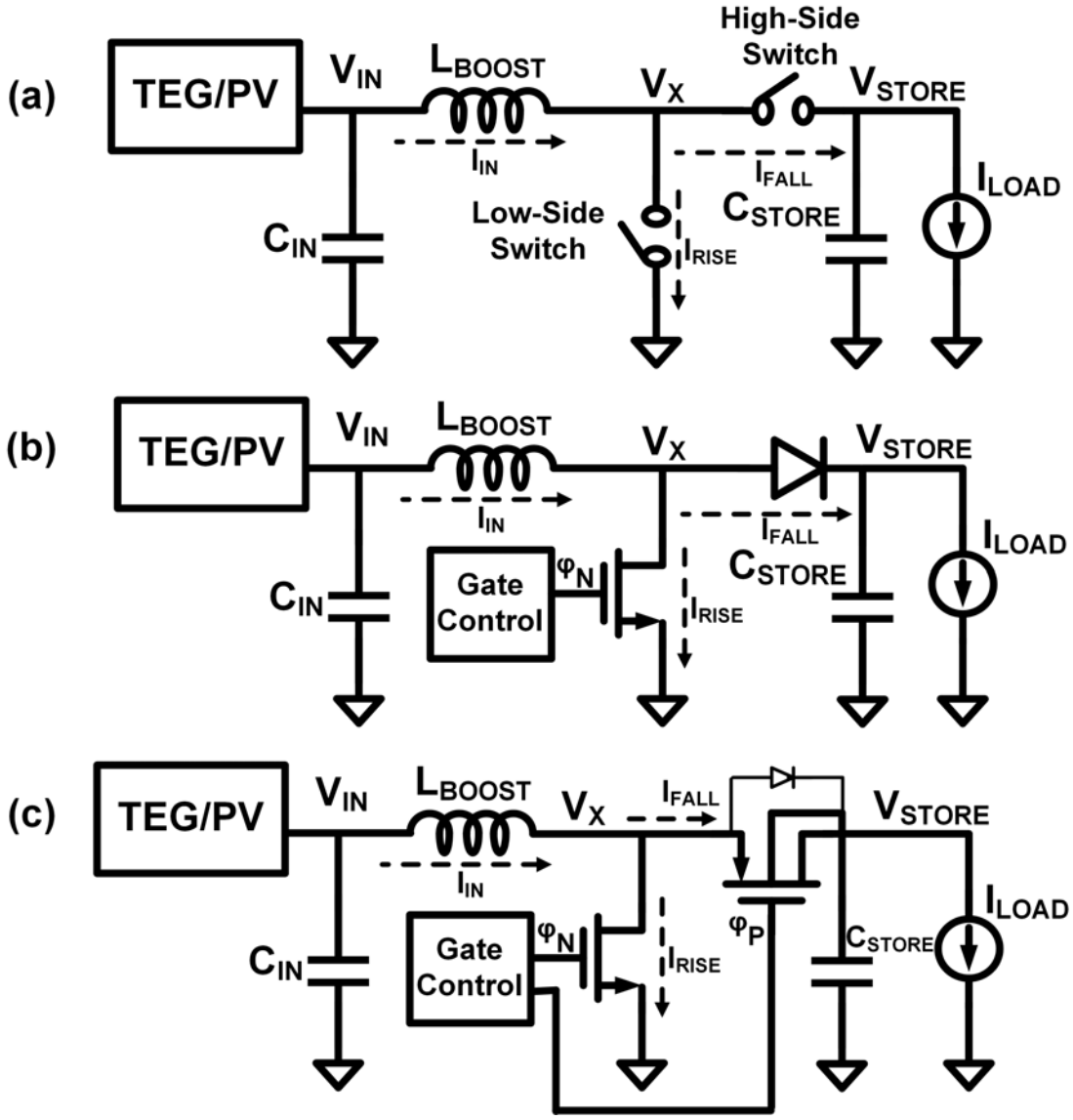


Figure 2.13: Boost converter powertrain with (a) ideal switches (b) diode as an HS switch (c) PFET as an HS switch [6]

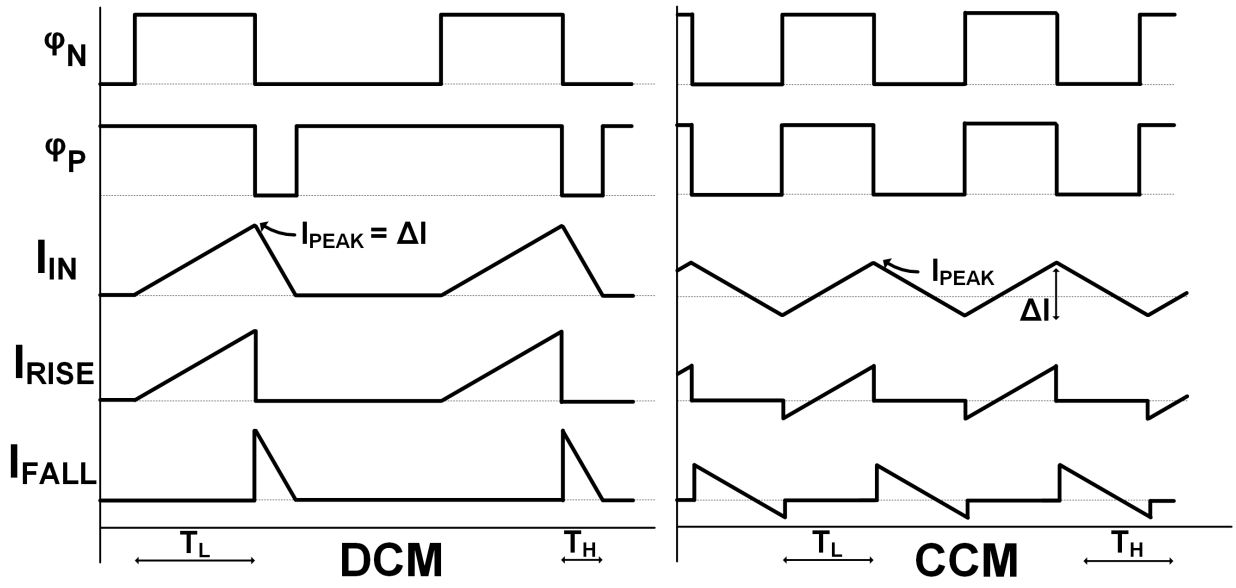


Figure 2.14: Timing diagram in DCM vs. CCM showing the possibility of inductor current to flow negative in case of CCM at light loads degrading performance[6]

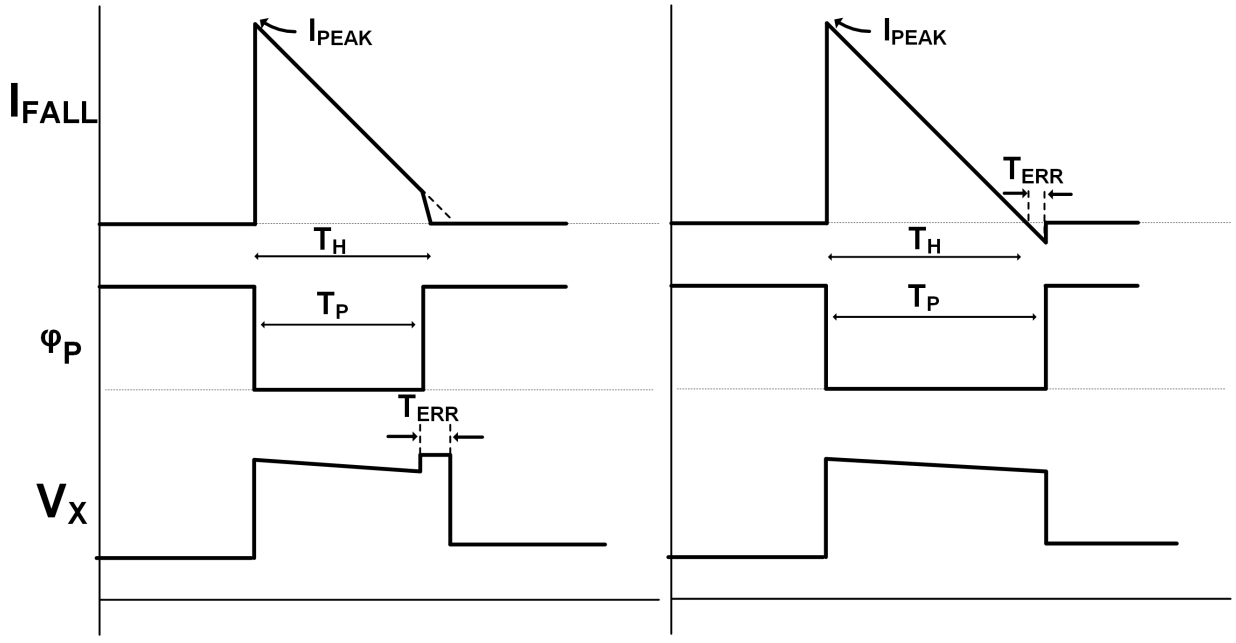


Figure 2.15: Challenges in synchronous rectification. Left: PFET high-side switch turns OFF before inductor current crosses zero. Right: PFET high-side switch turns OFF after inductor current crosses zero and flows in the negative direction. [6]

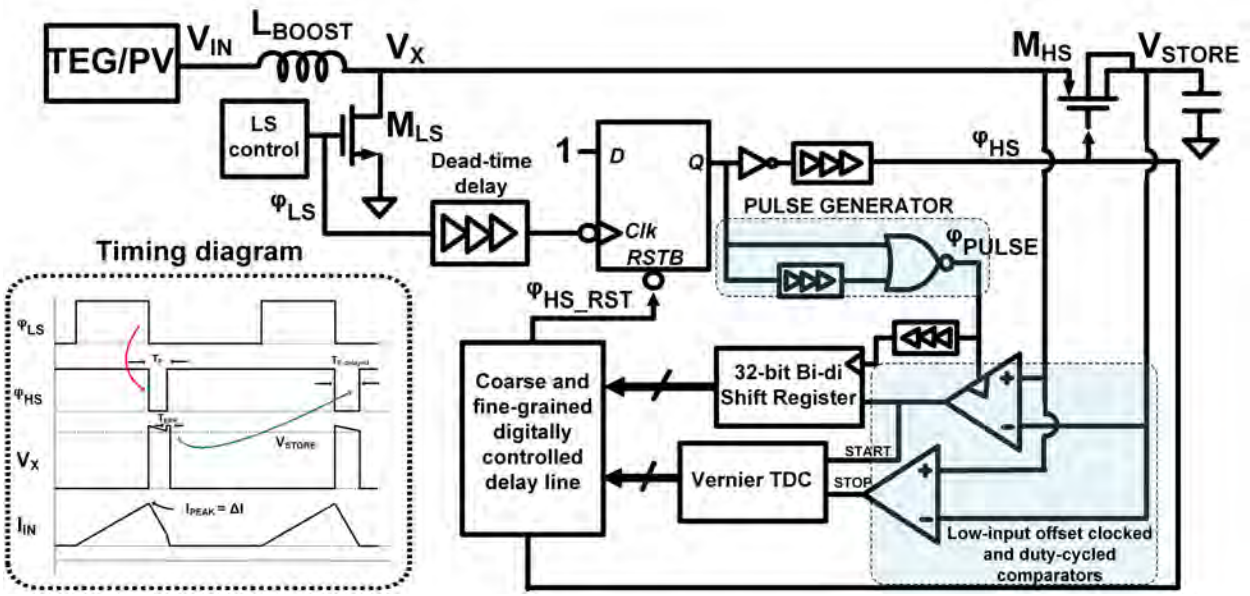


Figure 2.16: Correction-based Zero crossing detection scheme and associated timing diagrams

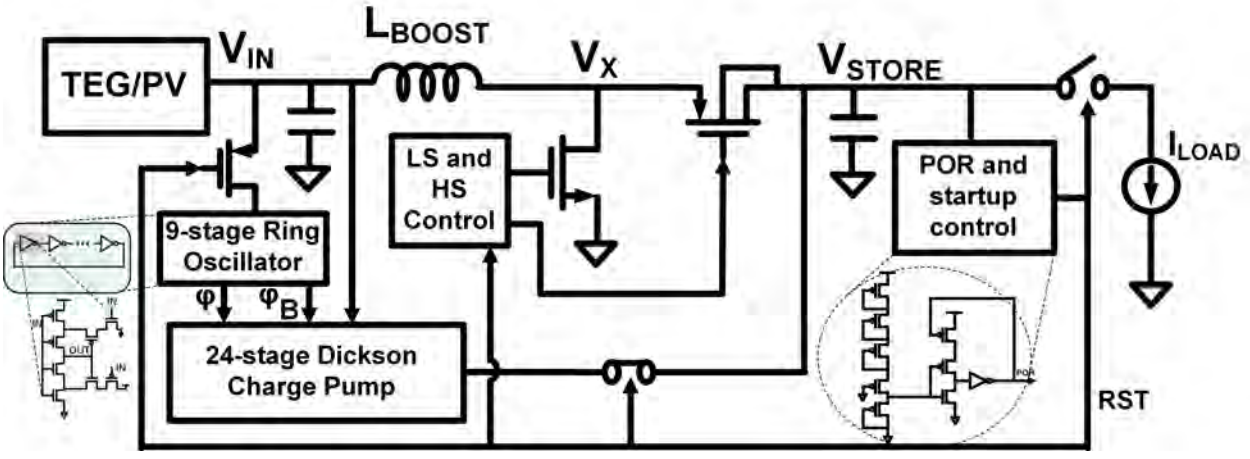


Figure 2.17: Architecture of the cold-start circuit

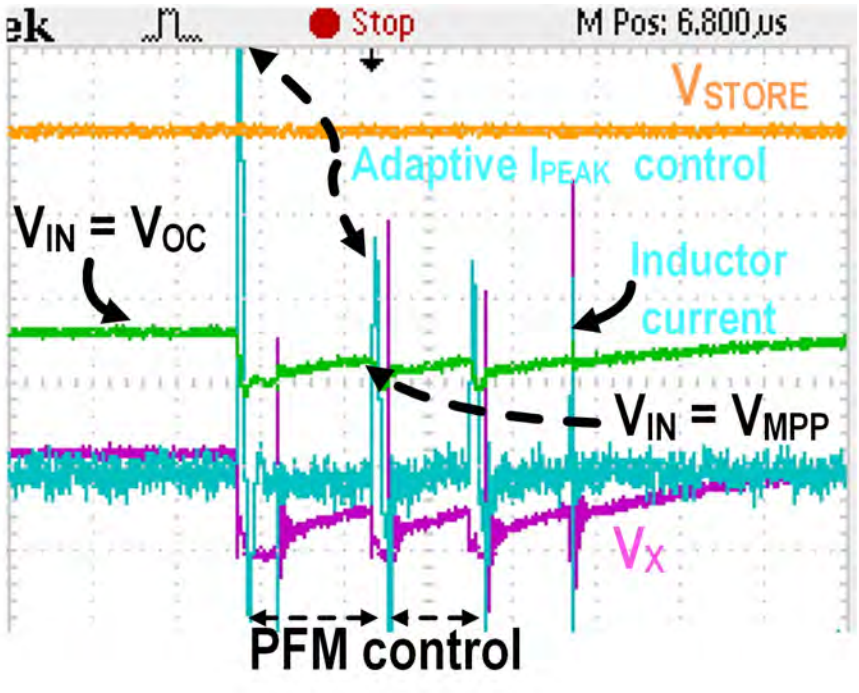


Figure 2.18: Measured functional waveforms of the system demonstrating adaptive peak inductor current control with varying V_{IN}, PFM and MPPT operation

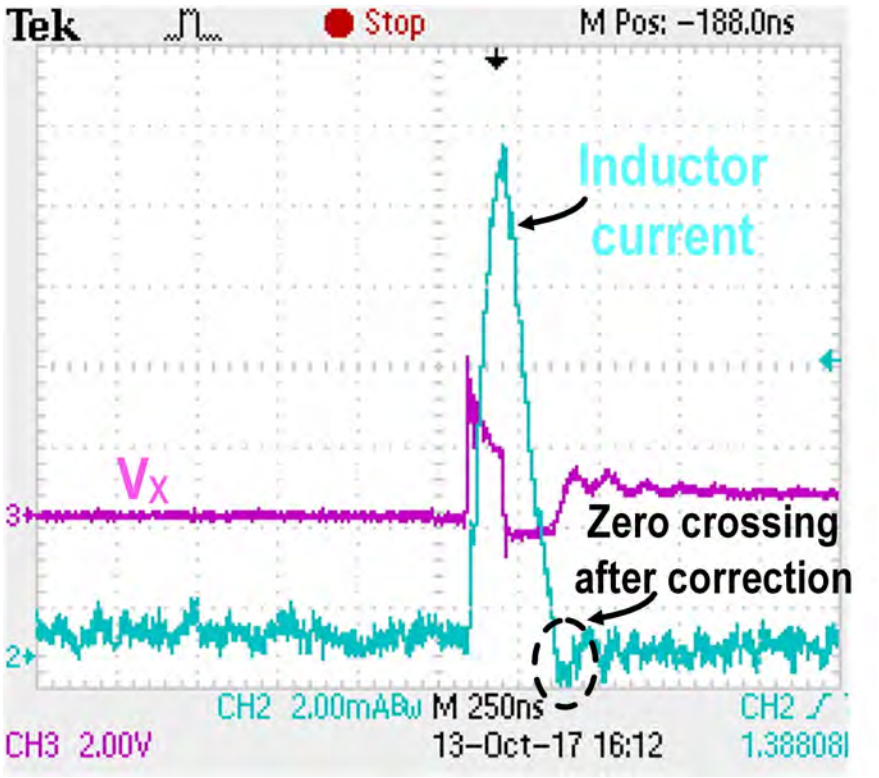


Figure 2.19: Measured peak inductor current and V_X node waveforms showing corrected zero crossing detection

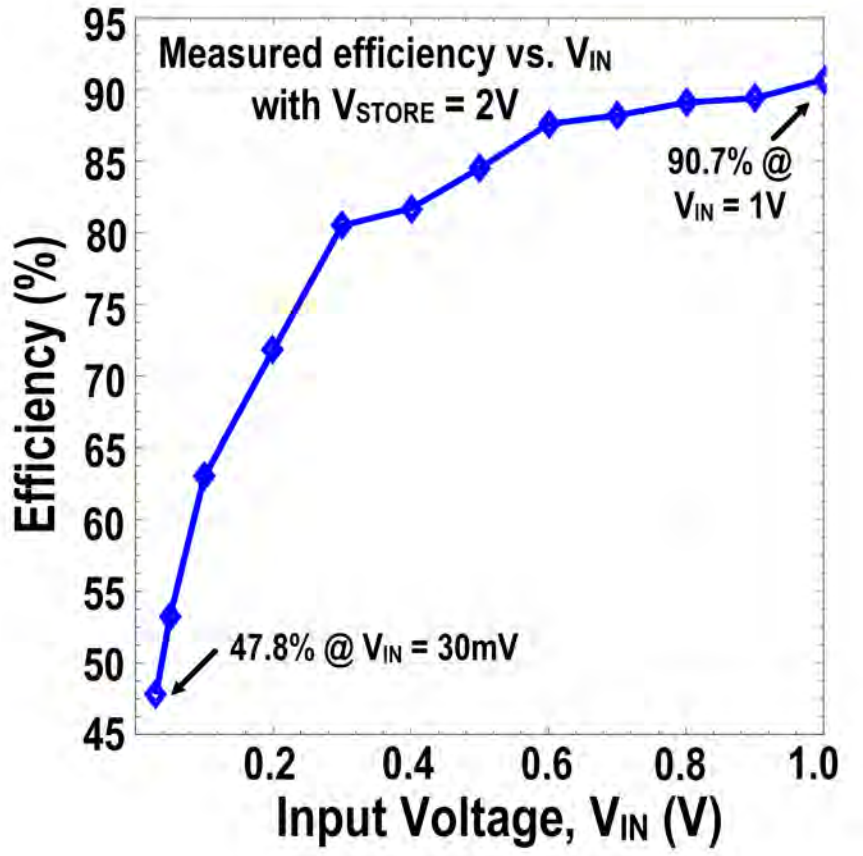


Figure 2.20: Measured Efficiency as a function of the input voltage.

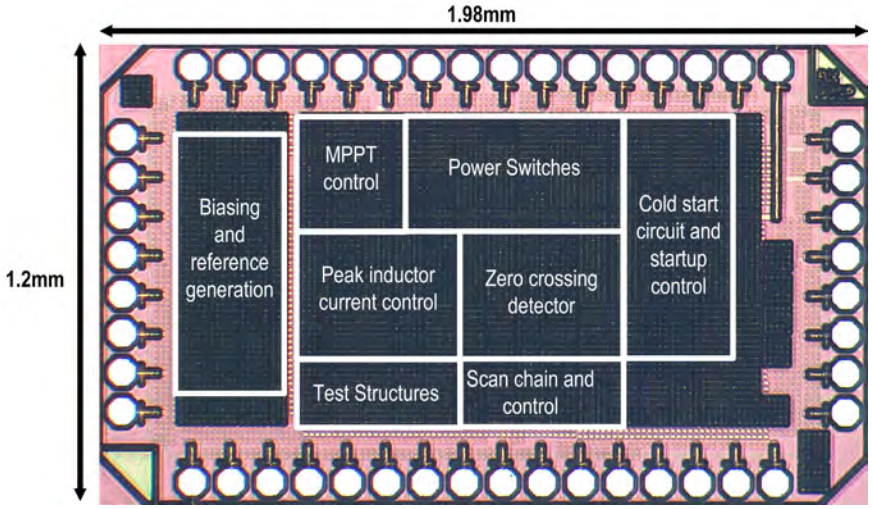


Figure 2.21: Die photo of the prototype energy harvester chip fabricated in 0.13μm technology

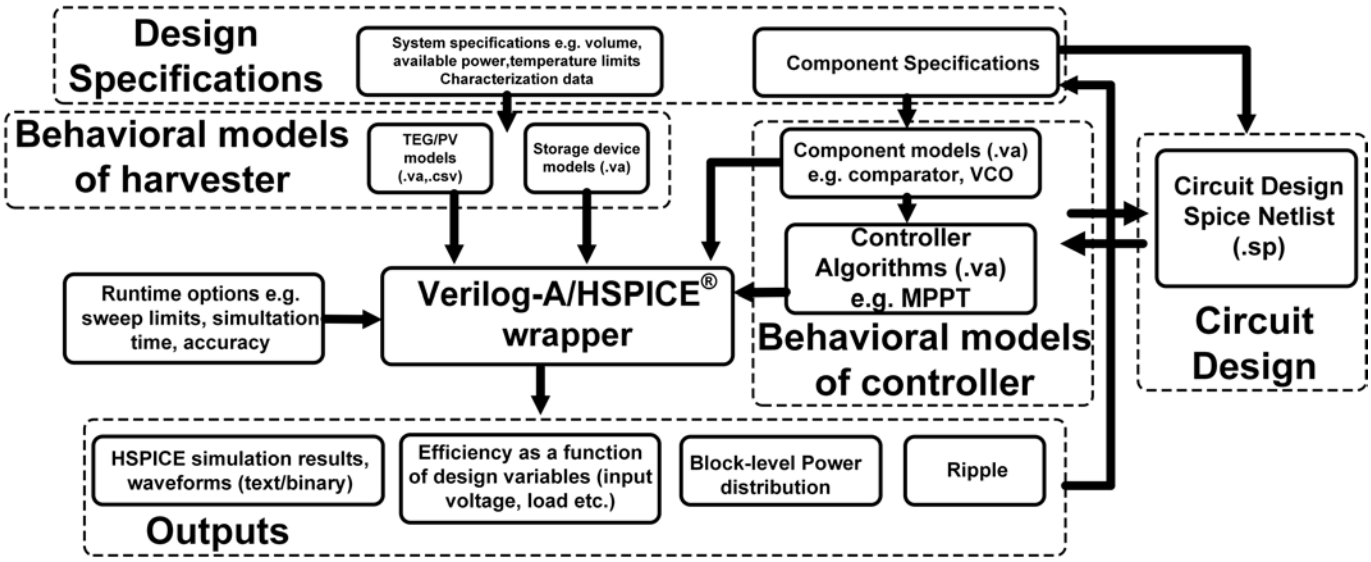


Figure 2.22: Tool flow to evaluate the performance of energy harvesting powertrain and controller circuits

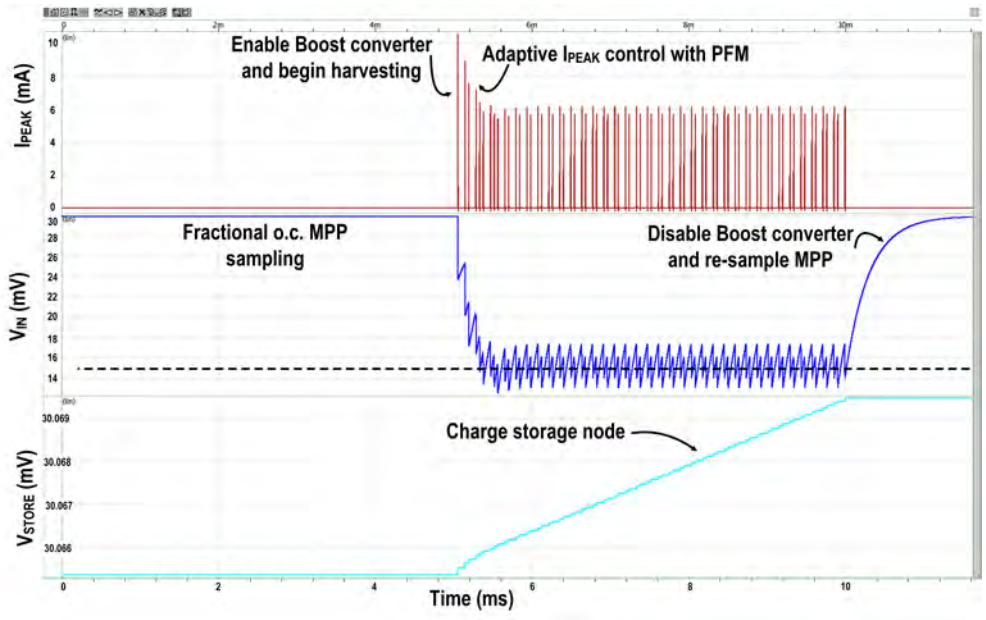


Figure 2.23: Functional waveforms of the boost converter generated using the proposed performance modeling framework. Behavioral models for adaptive peak inductor current control, MPPT and zero crossing detection were implemented in Verilog-A

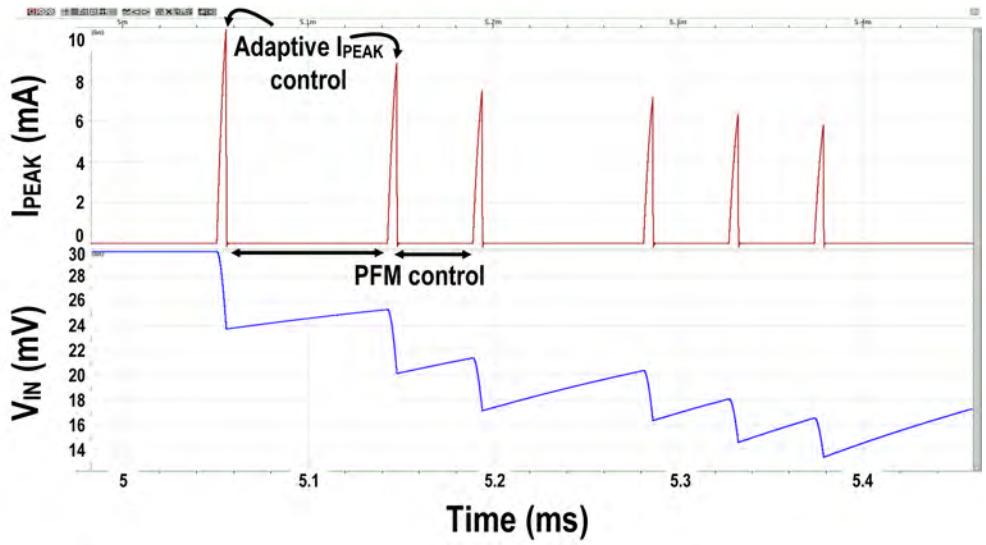


Figure 2.24: Simulation results from the model showing the time-domain behavior of the adaptive I_{PEAK} control algorithm with PFM modulation for achieving optimal power efficiency for a given input power level and output load

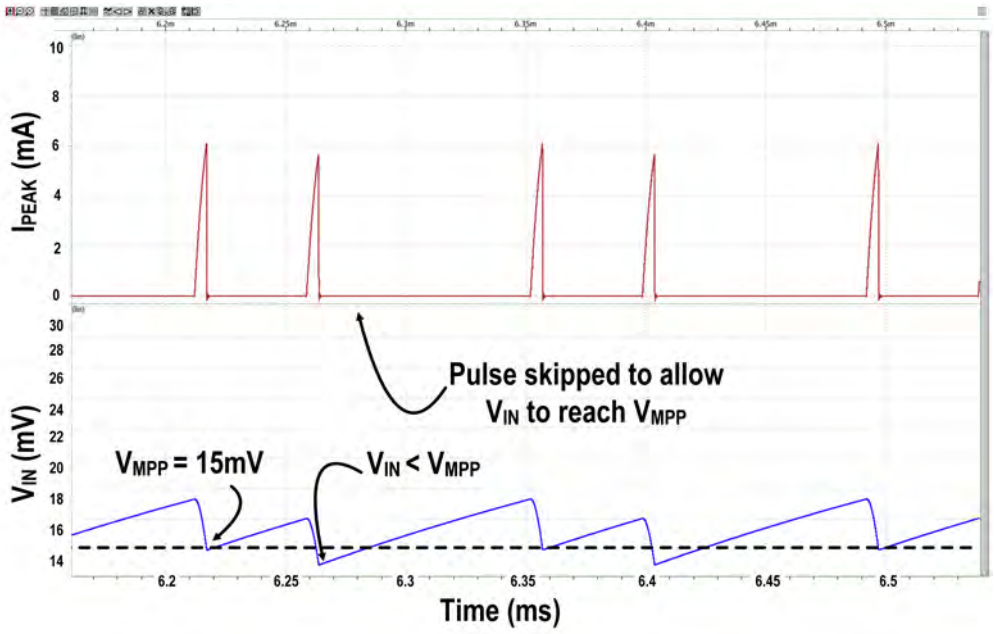
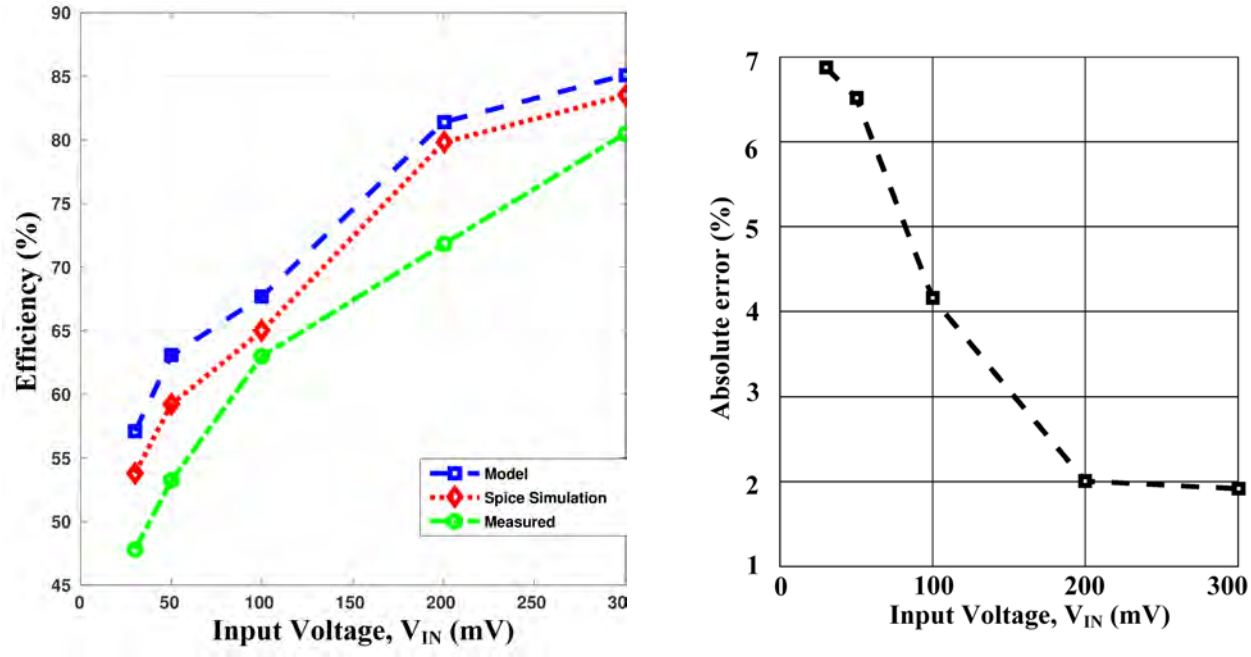


Figure 2.25: Simulation results from the model showing the time-domain behavior of the fractional open-circuit voltage-based MPPT algorithm



(a) (b)

Figure 2.26: (a) Power efficiency as a function of the input voltage from performance modeling, spice simulation and measured results (b) Absolute error between simulated and modeled efficiency as a function of the input voltage

Chapter 3

Ultra low I_Q Supply voltage regulation

3.1 Motivation

Supply regulation plays an important role in delivering power to general-purpose microprocessors and chipsets deployed in smartphones, tablets, laptops, as well as self-powered systems, such as wireless and body sensor nodes. Each system has an application specific power profile. For instance, high-performance systems, such as personal computers consume hundreds of mW, depending on the type of application being executed by the operating system. Battery-powered systems, such as smartphones need to conserve energy to ensure the longevity of the battery and thus operate at much lower power levels in the order of hundreds of μW to a few mW. Wearable, self-powered systems, which operate from energy harvested from ambient sources, have a much stringent power budget. Various components of a system might have entirely different supply voltage specifications. For instance, most analog and mixed-signal components need sufficient voltage headroom for reliable operation whereas digital circuits leverage Dynamic Voltage and Frequency Scaling (DVFS) for energy-efficient operation. Hence, an integrated solution for supply regulation and power

management is essential for delivering power to various analog and digital components in both high-performance as well as battery-operated or self-powered systems.

3.2 Background

Technology scaling has allowed the integration of power delivery circuits resulting in fully integrated voltage regulators with higher power efficiencies as compared to off-chip regulators. Power delivery circuits can be broadly classified into two major categories: energy harvesting circuits and voltage regulators. While voltage regulation is needed in almost all systems to provide a stable power supply and to support variations in load currents, integrated energy harvesting circuits are application-specific. Voltage regulation is typically achieved by regulating battery voltage in the case of battery-powered systems or the voltage on a storage buffer such as a supercapacitor, in case of energy-harvesting systems. Typically, supply regulation involves down-conversion of the battery voltage using buck converters. In some cases, a buck-boost topology is required if the voltage on the storage capacitor or the battery is lower than the desired regulated voltage levels of the system. Buck regulators can be implemented using linear regulators such as Low Drop Out (LDO) regulators; switched-capacitor or inductor-based switching regulators. Buck-boost topologies can be implemented using switching regulators (inductor/switched-cap topologies).

3.2.1 LDO regulators

An LDO is a type of a linear regulator, which can provide a regulated DC supply with input voltages, higher than or nearly equal to the required regulated output. The main advantages of using an LDO over a switching regulator are that it does not inject switching noise on the supply line and does not require off-chip passives for regulation. Hence, an LDO can be fully integrated on-chip and consumes a smaller area as compared to some of the switching regulators, which require external passives and greater silicon real estate. Figure 3.1 shows

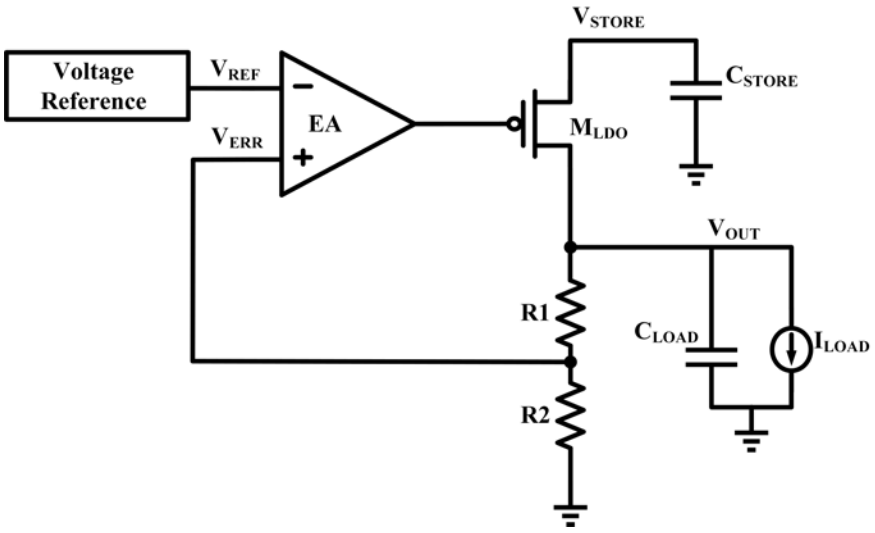


Figure 3.1: LDO topology

the topology of an LDO. It consists of an Error Amplifier (EA), a voltage reference circuit whose output is shown as V_{REF}, a pass transistor (M_{LDO}) and a feedback network shown by resistors R1 and R2. Conventionally, an LDO is mostly used as an output stage of a switching regulator to reduce the ripple and switching noise injected by the switching regulator on the supply line. A low-power bandgap reference circuit, such as [43] or a voltage reference circuit, based on ΔV_T of two CMOS transistors [44] can be leveraged to generate V_{REF}. Ideally, V_{REF} should have low sensitivity to the supply voltage (V_{STORE}) and temperature variations. A fraction of the regulated output voltage, V_{OUT} is fed-back to the error amplifier EA by the resistive feedback network consisting of resistors, R1 and R2. The error amplifier modulates the ON resistance of the pass transistor, M_{LDO} to maintain a regulated V_{OUT}, subject to changes in load current, I_{LOAD}. The response time depends on the bandwidth of the error amplifier, which can be improved by employing compensation techniques, such as dominant pole or lead-lag compensation schemes. The efficiency (η) of an LDO is given by:

$$\eta = \frac{V_{OUT} I_{OUT}}{V_{STORE}(I_{LOAD} + I_{CONTROL})} \tag{3.1}$$

where, $I_{CONTROL}$ represents the total current consumed by the control circuits, such as the voltage reference, error amplifier, leakage and current loss in the feedback network.

3.2.2 Inductor-based Voltage Regulators

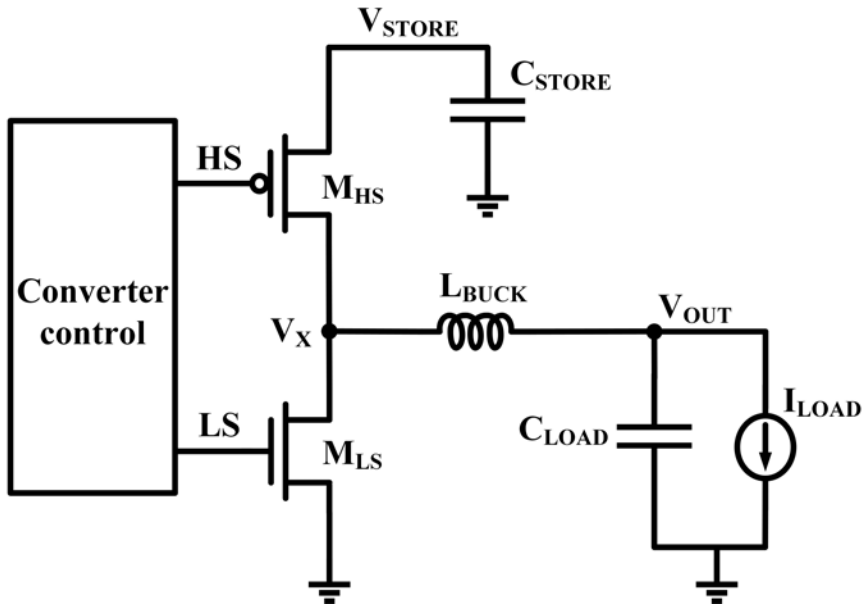


Figure 3.2: Inductor-based switching regulator topology

The advantage of a switching regulator over an LDO is that it can provide a wide range of voltage conversion ratios across a wide range of load currents with high power efficiencies. An inductor-based buck converter is a switching regulator, which uses an inductor as an intermediate storage element to transfer power to the load. The disadvantage of using an inductor-based buck converter is that it needs an off-chip, high quality factor (Q) inductor increasing area and cost. Although the DC-DC converter proposed in [45], implements an integrated on-chip inductor, it is difficult to achieve high power efficiency for high voltage conversion ratios. Moreover, on-chip inductors are not area-efficient. Hence, most inductor-based switching regulators in literature use off-chip high-Q inductors to reduce conduction-loss and achieve greater power efficiencies [46][47][48][21]. Figure 3.2 shows the powertrain topology of an inductor-based buck converter. It consists of two power transistors,

M_{HS} and M_{LS} , which are used to transfer power to the load through the inductor, L_{BUCK} and regulate the output voltage, V_{OUT} at the desired conversion ratio. Depending on the architecture of the control scheme, either V_{OUT} [21] or the inductor current [47] is sensed through a feedback network (not shown in Figure 3.2) to generate pulse-width-modulated (PWM) or pulse-frequency-modulated (PFM) non-overlapping gate control signals of M_{HS} and M_{LS}. During the High-Side (HS) phase, the gate control signals ensure that M_{HS} is ON while M_{LS} is OFF. The inductor is charged up by V_{STORE} and M_{HS}. In the Low-Side (LS) phase, the energy stored in the inductor is transferred to the load by M_{LS} and the inductor current ramps down to zero. Assuming Discontinuous Mode (DCM) operation, the inductor current remains at zero until the next switching cycle. It is important that M_{LS} should turn OFF when the inductor current crosses zero. Thus in an ideal case, the voltage conversion ratio is given by:

$$\frac{V_{OUT}}{V_{STORE}} = \frac{1}{1 + \frac{T_L}{T_H}} \tag{3.2}$$

where, T_L is the ON-time of M_{LS}, which is governed by the pulse width of the LS pulse and T_H is the ON-time of M_{HS}, which is governed by the pulse width of the HS pulse Hence, by modulating T_L and T_H, the desired conversion ratio can be achieved. The HS and LS pulses need to be non-overlapping so that there is no short-circuit current through M_{HS} and M_{LS}. A dead-time controller such as [46][47] can be implemented in the control scheme to ensure that HS and LS pulses are non-overlapping and there is no short-circuit current through M_{HS} and M_{LS}. In 3.2, the conduction losses in the inductor and power transistors, as well as the switching loss, are not considered. The total conduction loss during the HS cycle, $E_{CN,H}$ as given by:

$$E_{CN,H} = \int_0^{I_{PEAK}} i^2 R_H \frac{L}{V_{STORE} - V_{OUT}} di = \frac{I_{PEAK}^3 L R_H}{3(V_{STORE} - V_{OUT})} \tag{3.3}$$

Similarly, for the LS cycle, the total conduction loss, $E_{CN,L}$ is given by:

$$E_{CN,L} = \frac{I_{PEAK}^3 L R_L}{3V_{OUT}} \tag{3.4}$$

where, R_H is the total resistance including the parasitic resistance of the inductor and the ON resistance of M_{HS} and R_L is the total resistance including the parasitic resistance of the inductor and the ON resistance of M_{LS}. The switching loss, E_{SW} and leakage, E_{LKG} is constant for a given control scheme and depends on the dimensions of M_{LS} and M_{HS}. Hence, the total loss, E_{loss} is given by:

$$E_{loss} = E_{CN,H} + E_{CN,L} + E_{SW} + E_{LKG} \tag{3.5}$$

Thus for a given conversion ratio, $\frac{V_{OUT}}{V_{STORE}}$, in order to minimize E_{loss}, it is necessary to tune the peak inductor current, I_{PEAK}, or modulate the ON-resistance of M_{LS} and M_{HS} by an appropriate gate-drive control scheme

3.2.3 Switched-Capacitor Voltage Regulators

Switched-capacitor DC-DC converters are a class of switching regulators, which offer a fully integrated solution to voltage regulation. The arrangement of CMOS switches and transfer capacitors can be reconfigured on-chip to achieve desired conversion ratios. Figure 3.3 shows the topology of a simple 2:1 switched-capacitor based buck converter. The only disadvantage of implementing a switched-capacitor architecture is that the regulator can be targeted for only a limited range of conversion ratios and load currents as compared to inductor-based DC-DC converters. Moreover, precise control signals are required for the switches to prevent undesirable short-circuit or contention currents, which can lower the power efficiency. The sources of power loss are due to the conduction loss in the switches and transfer capacitors, the switching loss in the control circuits and parasitic bottom-plate capacitance of the transfer capacitors. Depending on the load current and output voltage specifications such as ripple,

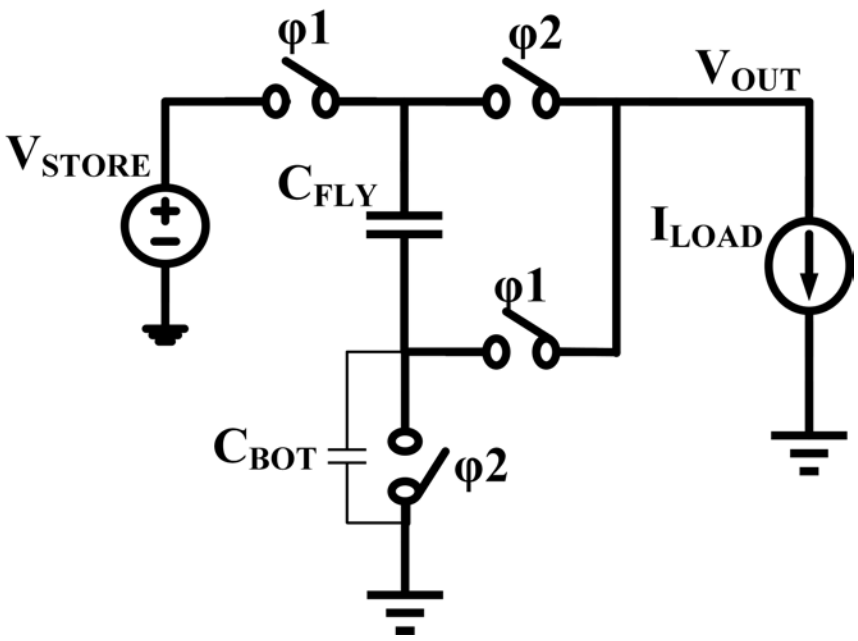


Figure 3.3: Switched capacitor 2:1 buck regulator topology

switching frequency, some sources of power loss may be dominant. At lower load currents, switching loss and bottom-plate parasitic loss are more dominant than conduction loss in the switches. In chapter 2, section 2.2.3, the sources of power loss in switched-capacitor power converters are described in more detail. Existing work in literature, such as [49], implements a reconfigurable switched-capacitor topology and combines interleaved clocking and level shifting in gate-drive circuits. In [50], a hybrid architecture, consisting of switched-capacitor regulators and LDOs, is implemented. In [51], a capacitance modulation scheme is implemented using digital circuits, which controls the amount of transfer capacitance involved with varying load currents.

3.3 Single-Inductor Multiple Output (SIMO) Buck-Boost DC-DC Converter

Computing systems catering to emerging Internet-of-Things (IoT) applications need to be self-powered. Hence such systems can now harvest energy from different sensing modalities

such as TEGs or solar cells where available voltage levels are as low as 10 mV [40][15]. IoT systems operate in an energy-constrained environment where every small amount of stored energy is essential for system operation. The system needs to start-up and operate from very low input voltages to sustain in such an energy-limited environment. However, the system can start only after the power supplies (VDDs) have become operational. Therefore, the power supplies for ULP systems need to be functional at low input voltages. Further, ULP systems require efficient power supplies to minimize losses in voltage conversion. In addition, several VDDs are needed to optimize energy-efficiency in digital and analog processing. In existing literature, power management schemes based on LDO regulators have been proposed for applications such as body sensor nodes [52]. Although LDOs consume lesser area, they provide lower efficiency and require higher input voltage than the regulated output voltage. In [52], the regulators provide output voltages up to 1.2 V, but the system can only start-up if the voltage on the storage capacitor is greater than 1.35 V. The higher system start-up voltage leaves a high percentage of the stored energy unused. Moreover the use of LDOs provides lower efficiencies. A single inductor energy harvesting and power management solution generates multiple voltages for a ULP system using SIMO DC-DC converter design. The solution provides very high efficiency (up to 92%) voltage regulators [21]. However in [21], the system can start-up only after the input voltage goes above 3.3 V, leaving a significant amount of energy on the storage node unused. In [53], the input voltage ranges from 2.6-3.5V to provide an output of 1.5V. In [16], the minimum voltage on the storage capacitor needs to be at least 1.8V for the rails to regulate. In this work, we present a SIMO voltage regulator that supplies VDDs for an ULP IoT activity monitor [23]. The SIMO DC-DC converter uses a buck-boost architecture and generates 1.2 V, 0.5V, and 0.25-0.35 V programmable output VDDs from an input voltage of 0.7 V or higher. The peak efficiency of the proposed design is 95%, and quiescent power consumption is 1.19μW. A 32 nW bandgap reference circuit operational from 0.5 V [43] can be used to provide the reference voltage for the circuit. The proposed design uses a constant peak inductor current control scheme in a buck-boost

architecture to provide high efficiency for a wide range of input voltages delivering a load varying from 1μA-10mA. The design also employs a fast offset compensated zero detection control scheme for synchronous rectification.

3.3.1 SIMO Architecture

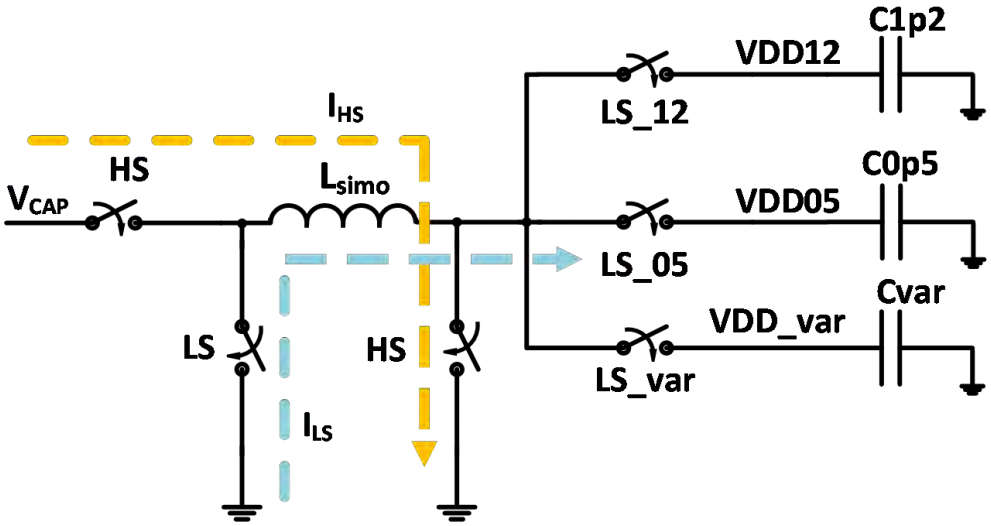


Figure 3.4: Buck-Boost powertrain architecture [4].

Figure 3.4 shows the buck-boost architecture of the SIMO regulator. Initially the HS switch is closed for the inductor to charge up and thus ramping up the inductor current (denoted by I_{HS}). After a fixed dead time, the HS is switched off, and the LS switch is switched on to transfer the energy (using conduction current I_{LS}) to the output rails denoted by VDD_{12}, VDD_{05} and VDD_{var}.

Figure 3.5 shows the block diagram of the control scheme of the SIMO. In Figure 3.6, we discuss the PFM control scheme of the DC-DC regulator. The output V_o is compared with a reference voltage, V_{ref} generated by a bandgap reference circuit such as [43]. As long as V_o is less than V_{ref}, the peak inductor control circuit is enabled to ramp up the inductor current (I_{HS}) and transfer the power to the output (via I_{LS}) by deploying the LS switch after a fixed dead time. The zero detect comparator monitors the V_x node and as soon it is enabled as soon as V_x is pulled below zero.

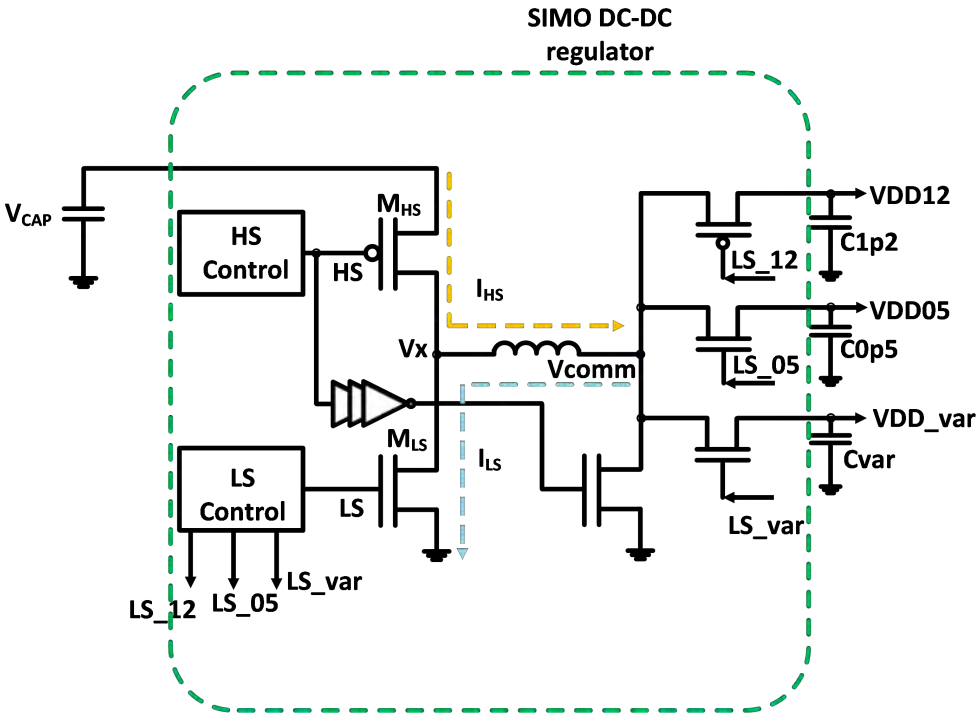


Figure 3.5: Block Diagram of the SIMO power management system [4].

3.3.2 Peak Inductor current control

In Figure 3.7 we describe the peak inductor current control circuit. A constant peak inductor current control scheme is necessary in an inductor based switching regulator for achieving higher efficiency and minimizes conduction losses. A peak inductor current control scheme utilizing the threshold voltage of transistor has been described in [21] for a buck converter and in [15] for a boost converter. In this work, we generate a transistor threshold voltage (V_{th})-based peak inductor current control scheme for a buck-boost architecture. The peak current is constant, but the switching frequency is varied to deliver a power to varying loads from a fixed input voltage. In Figure 3.7, we present a bias generation scheme that is invariant to process mismatches and operational at low input voltages for a buck-boost control scheme. The circuit generates a voltage of $\frac{V_{CAP}}{2} + V_{th,p}$ in two stages. In the first stage, $\frac{V_{CAP}}{2}$ is generated using a diode structure, which provides very high impedance and low current. In the next stage, the voltage $\frac{V_{CAP}}{2} + V_{th,p}$ is generated by dropping this voltage using a p-channel Complementary Metal Oxide Semiconductor (PMOS) device. The transistor M_{PHS}

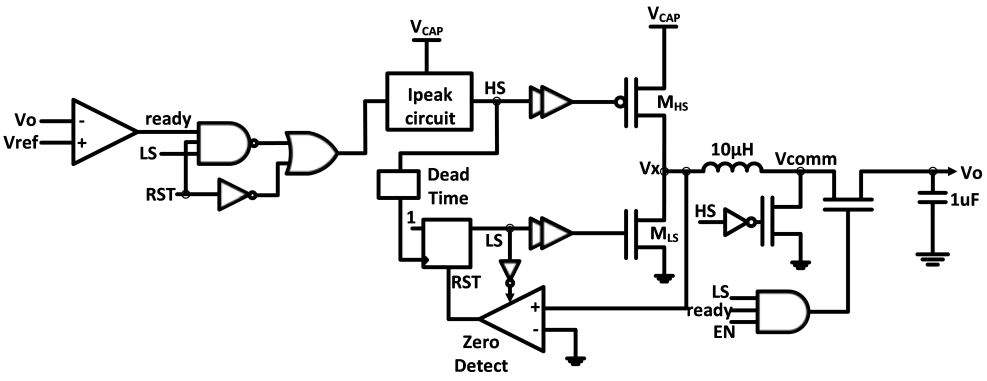


Figure 3.6: PFM control circuit [4].

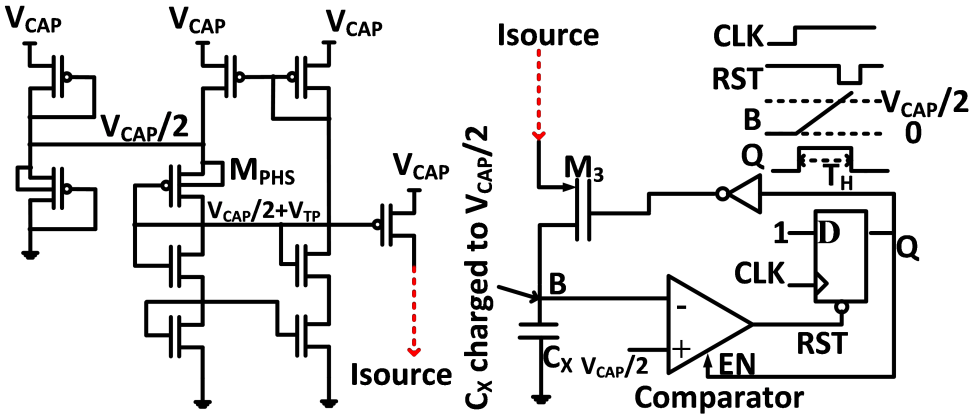


Figure 3.7: Peak inductor current control circuit [4].

is stronger than the other transistor, which sets the output voltage closer to its threshold voltage. It is critical that the current load from the second stage does not load the first stage of the circuit, which will cause the $\frac{V_{CAP}}{2}$ reference to move. The bias current generated for the next stage is fed back in the feedback loop as shown, which ensures that no current flows from the first stage. The current source provides a current denoted by I_{source} given by:

$$I_{source} = K\mu C_{ox}(\frac{V_{CAP}}{2} + V_{th,p} - V_{th,p})^2 \tag{3.6}$$

$$I_{source} = K\mu C_{ox}(\frac{V_{CAP}}{2})^2 \tag{3.7}$$

The Capacitor C_x is charged from 0 to $\frac{V_{CAP}}{2}$ to generate the HS switching time.

$$T_H = C_x \frac{\frac{V_{CAP}}{2}}{I_{source}} = \frac{C_x}{K\mu C_{ox}(\frac{V_{CAP}}{2})} \tag{3.8}$$

Peak Inductor current is approximately given by,

$$I_{PEAK} = \frac{V_{CAP} T_H}{L_{SHR}} \tag{3.9}$$

Hence from 3.8,

$$I_{PEAK} = \frac{2C_x}{K\mu C_{ox} L_{SHR}} \tag{3.10}$$

The expression in 3.10 is independent of input voltage V_{CAP}, the output voltage, or the threshold voltage V_{th} of the transistor. We achieve a constant peak inductor current for a wide input and output range, which is dependent only on the gate oxide capacitance, C_{ox}, and external inductance L_{SHR}. Figure 3.8 shows the simulated results of I_{PEAK} for input voltages ranging between 0.7V to 1.4V.

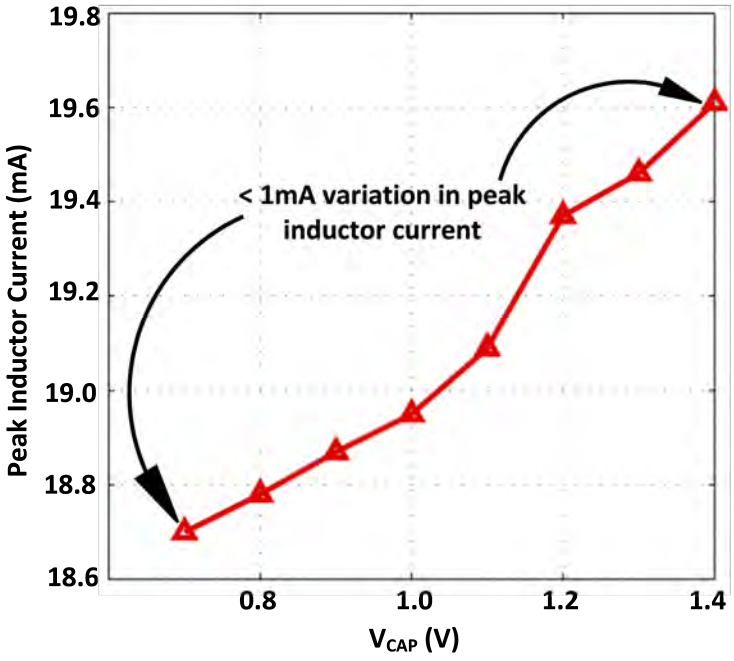


Figure 3.8: Peak inductor current variation with V_{CAP} [4].

3.3.3 Zero Crossing Detection Circuit

For LS control, we present a fast offset compensated zero current detection technique, which is specifically designed to operate at low input voltages. Zero current detection is needed when the inductor current switches direction so that the regulator can operate in discontinuous conduction mode and the power is not delivered across the diode. Hence, zero inductor current crossing detection is needed for achieving higher efficiencies. In this work, the zero crossing comparator (Figure 3.9) uses a common-gate amplifier for better performance and is enabled only when the V_x node is pulled below 0V. The zero detection comparator needs to have a very low input-offset to sense small changes in V_x. Hence offset-compensation is achieved in the first stage with EN = 1 and Off = 1, When V_x goes below 0V, the comparator is enabled with EN = 0 and Off = 0, the LS goes high. As V_x ramps up and crosses 0V, the comparator output goes low to make to LS go low. The comparator is duty-cycled using the EN signal to prevent the higher static current consumed during comparison.

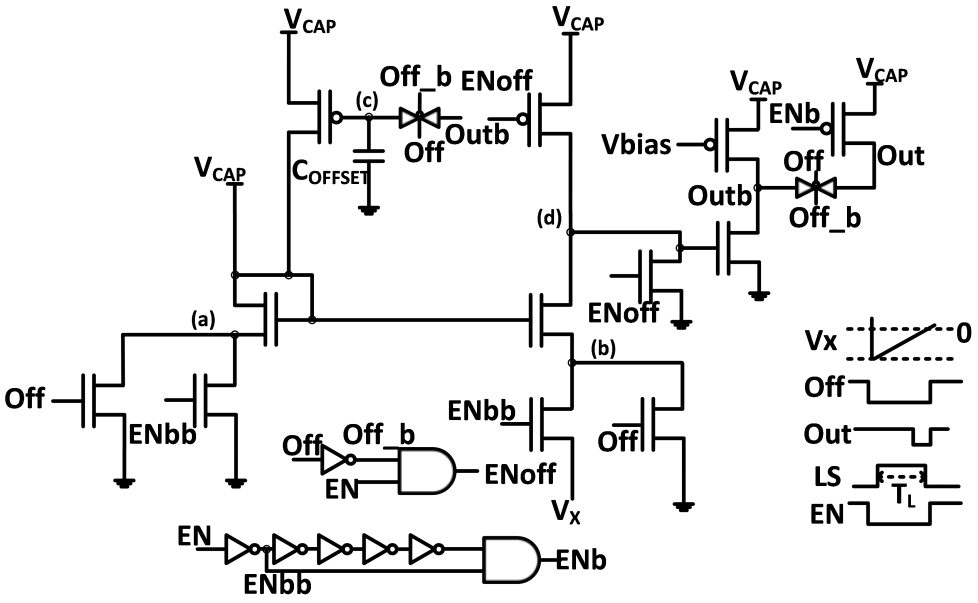


Figure 3.9: Zero crossing detection circuit [4].

3.3.4 Measurement results

The chip was fabricated in a commercial 0.13μm CMOS process. Figure 3.10 shows measurement plots for efficiency of the SIMO regulator for varying amounts of input energy available on the storage capacitor. We use a 100μF storage capacitor at the SIMO input and model the load by connecting discrete load resistors at the output. We find that we achieve a peak efficiency of 95% at a load current of 2.8mA for the 1.2V output. We achieve an efficiency of 85% for the 0.5V output at a load current of 2.9mA. We find that the peak efficiency of 94.8% at 1.2V output is achieved when the voltage on the storage capacitor is 1.1V.

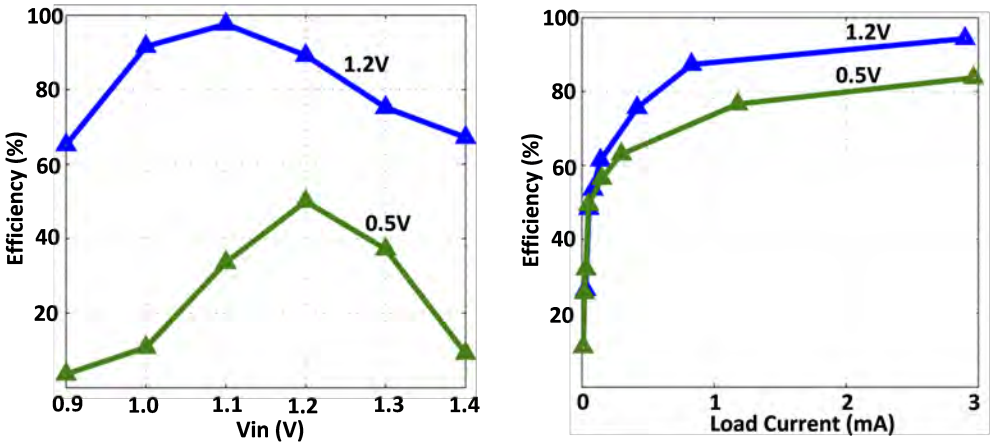


Figure 3.10: Measured Efficiency for 1.2V and 0.5V outputs across varying input voltages and load currents [4].

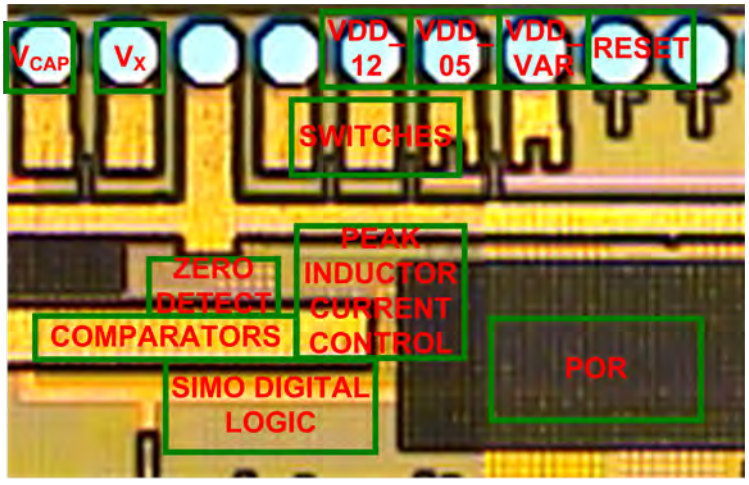


Figure 3.11: Chip Micrograph [4].

Table 3.1: Comparison of SIMO regulator with recent work

	[52]	[21]	[16]	**This Work [4]**
Process	0.13μm	0.13μm	0.35μm	**0.13μm**
# of outputs	4	3	1	**3**
o/p voltages	1.2V, 1V, 0.5V, prog. 0.25-1V	1.2V, 1.5V & 3.3V	0-3.3V	**1.2V, 0.5V, prog. 0.2-0.35V**
Efficiency	38%	92%@high load; 83%@1μA for 3.3V output	80%@0.5V; 95%@3V for Boost	**95%@high load; 83%@100μA for 1.2V output**
Idle Power	3.6μ W	1.2μ W	1μ W	**1.19μW**
Start-up	1.8V	3.5V	1.3V	**0.7V**
Max o/p voltage	1.2V	3.3V	3.3V	**1.2V**
Area (mm^2)	1.7	2.25	-	**1.6**
Max load	-	100mW	25mW	**12mW**
SIMO Reg.	×	✓	×	✓

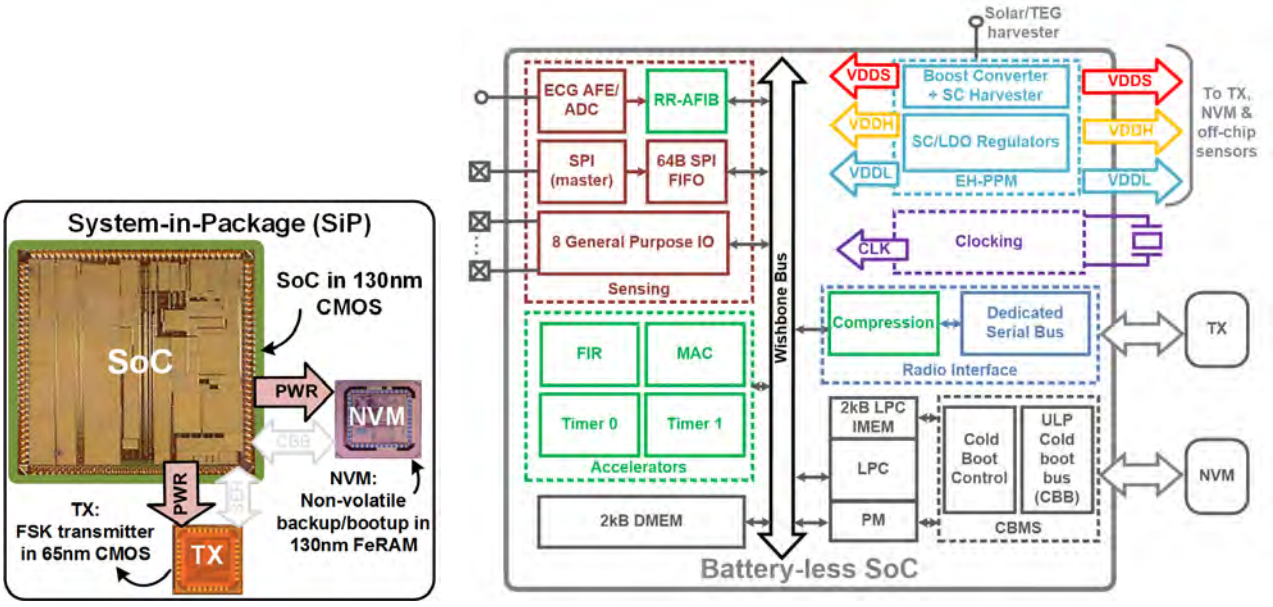
Figure 3.11 and Table 3.1 shows the chip micrograph and comparison of the proposed low-voltage SIMO DC-DC converter with recent work in literature. The proposed SIMO regulator can function at a very low input voltage starting from 0.7V and achieve a peak efficiency of 95% at high load. It consumes quiescent power of 1.19μW with the regulator operating in discontinuous conduction mode.

3.4 Energy Harvesting and Integrated Power Management Unit for sub-μW Power Biomedical Applications

Recent advancements in sensing technologies, embedded processors, and integrated circuit design have triggered the development of wearable as well as implantable ULP systems which cater to a diverse set of applications such as health monitoring, environmental sensing and remote surveillance [19][54][55][23]. Projections indicate as many as 1 trillion of such smart, interconnected devices will become part of our daily lives. Hence, to be effective, such systems must be unobtrusive, low-maintenance, and possess a long system lifetime. Energy

harvesting from ambient sources such as TEGs or PV cells provides an attractive alternative to batteries, which are expensive to replace. However, the available power from such sources is limited to the order of tens of μW due to changing environmental conditions and constrained form-factors leading to the development of sub-μW power systems [19][54][55]. In such <1μW power systems, the lower-bound of the power consumption is governed by the static power overhead of dutycycled components and always-ON circuits such as reference generators, real-time-clocks, etc., which still require a well regulated supply. Hence, power conversion circuits in such sub-μW systems need low-quiescent power overhead and high efficiency at <1 μW loads to extend system lifetime. In addition, the low power density of PV cells in indoor lighting and low- temperature differential of TEGs in wearable health applications make power delivery extremely challenging, especially in volume-constrained systems. In such scenarios, existing power management solutions such as the single-inductor buck-boost converter presented in Section 3.3 as well as [23][24][56][25] have poor power conversion efficiencies (50-65%) due to higher quiescent power ($>$ 1μW) implementations. Thus, there is a need to lower the quiescent power overhead of power conversion circuits in sub-μW power systems.

In this work, we present an EH-PMU implemented in 0.13μm technology that harvests energy from PV cells or TEGs and provides power to sub-μW digital and analog components with 71.1% peak end-to-end efficiency. The EH-PMU forms an integral component in context of a larger SiP-based system (Figure 3.12b) where it is responsible for power delivery to the various in-package components such as an SoC (processing), a non-volatile memory (storage) and an FSK transmitter (wireless communication) as well as external sensors such as an accelerometer. The Energy-Harvesting (EH) interface consists of a single inductor boost converter and also provides an alternate fully-integrated switched-capacitor energy harvester for low-cost, volume-constrained applications. The Power Management Unit (PMU) consists of three fully integrated Voltage Regulator (VR)s which consume low quiescent current (I_Q) facilitated by a gate-leakage based voltage reference generator. The PMU also consists of



(a) (b)

Figure 3.12: Block Diagram of the (a) System-in-Package and (b) the System-on-Chip. The SoC contains the EH-PMU responsible for power delivery [7]

auxiliary circuits such as a startup controller and overvoltage protection unit.

3.4.1 Architecture

The EH-PMU can harvest energy from solar or TEGs, powering sub-μW digital and analog components with high efficiency. Recent ULP System-on-Chip (SoC)s [19][23] need separate regulated rails for noise-sensitive analog circuits, digital processing, etc. Hence, the proposed EH-PMU provides three regulated outputs: 0.5V, 1V, and 1.8V. Figure 3.13 shows the overall system architecture. It consists of a single-inductor boost converter with a Maximum Power Point Tracking (MPPT) controller [23] that harvests and stores energy on a supercapacitor [23] or a re-chargeable battery [56]. Systems used in health applications such as glaucoma monitoring [17] or cochlear implants [31] are severely volume-constrained, limiting the use of external passives for power delivery. Hence, such applications need a fully-integrated, low-cost power management solution. The Energy-Harvesting (EH) interface thus provides a parallel three-stage cascaded auxiliary charge pump harvester (Figure 3.14) to harvest

energy from indoor-solar. An on-chip clamp circuit limits the maximum voltage of the storage device, V_{CAP}, to 1.5V to prevent device damage in this 0.13μm technology. The PMU

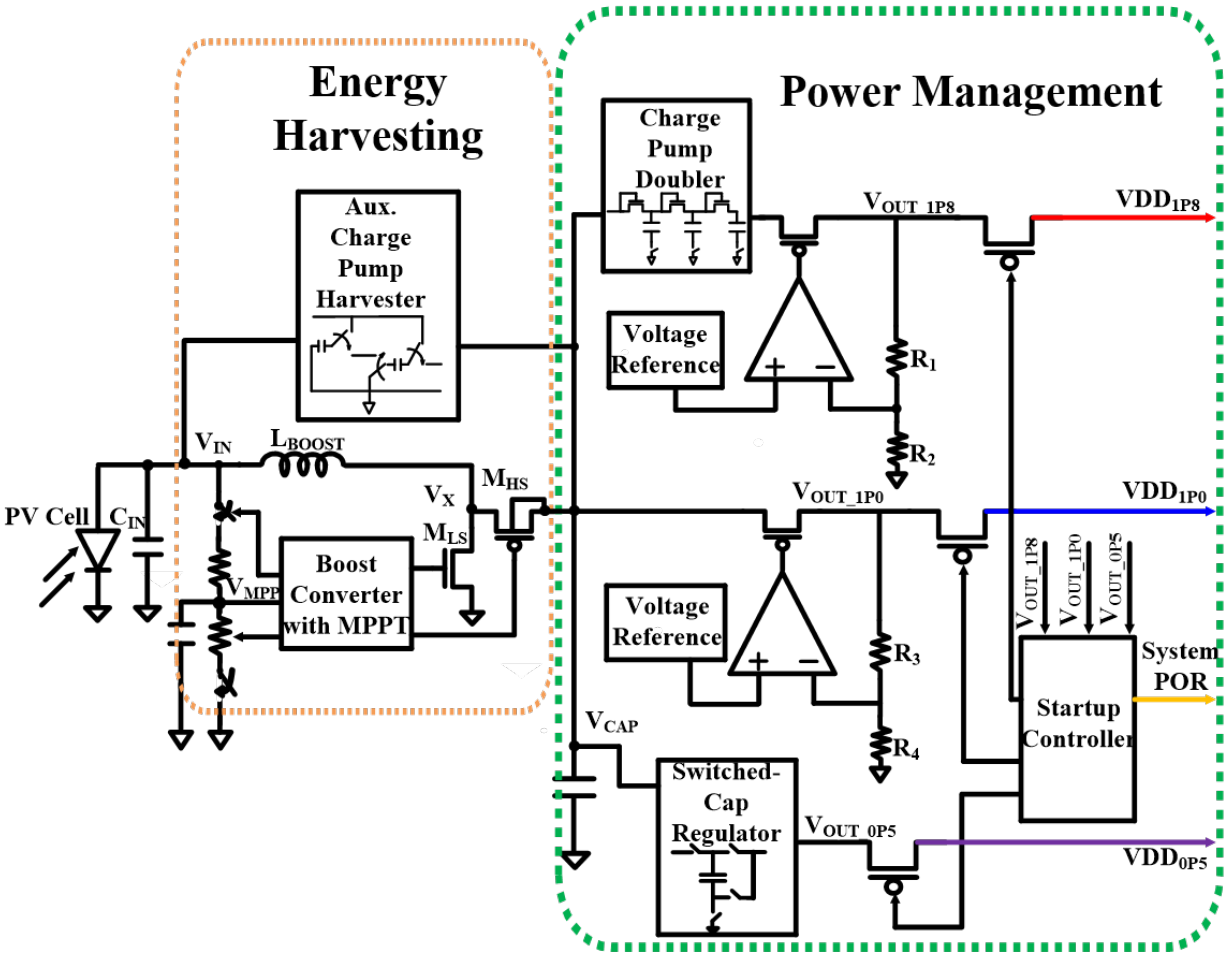


Figure 3.13: Top-level architecture of the proposed EH-PMU [8].

contains a startup controller to ensure a sequenced turn-on of the regulators. Figure 3.14 shows the schematics of the 0.5V, 1V, and 1.8V regulators. The 0.5V regulator consists of a two-way interleaved Switched Capacitor (SC) voltage regulator. PFM control is used in the controller, and the switching frequency can be programmed using a diode-stacked bias generator, which provides voltage biases, V_{BP} and V_{BN}, to a five-stage current-starved ring oscillator for generating control signals. A droop detector circuit [2] can be used to set the maximum allowable ripple and determine the minimal switching frequency. The 1V regulator consists of an analog LDO, where the error amplifier is designed for a gain of 35dB, unity-gain

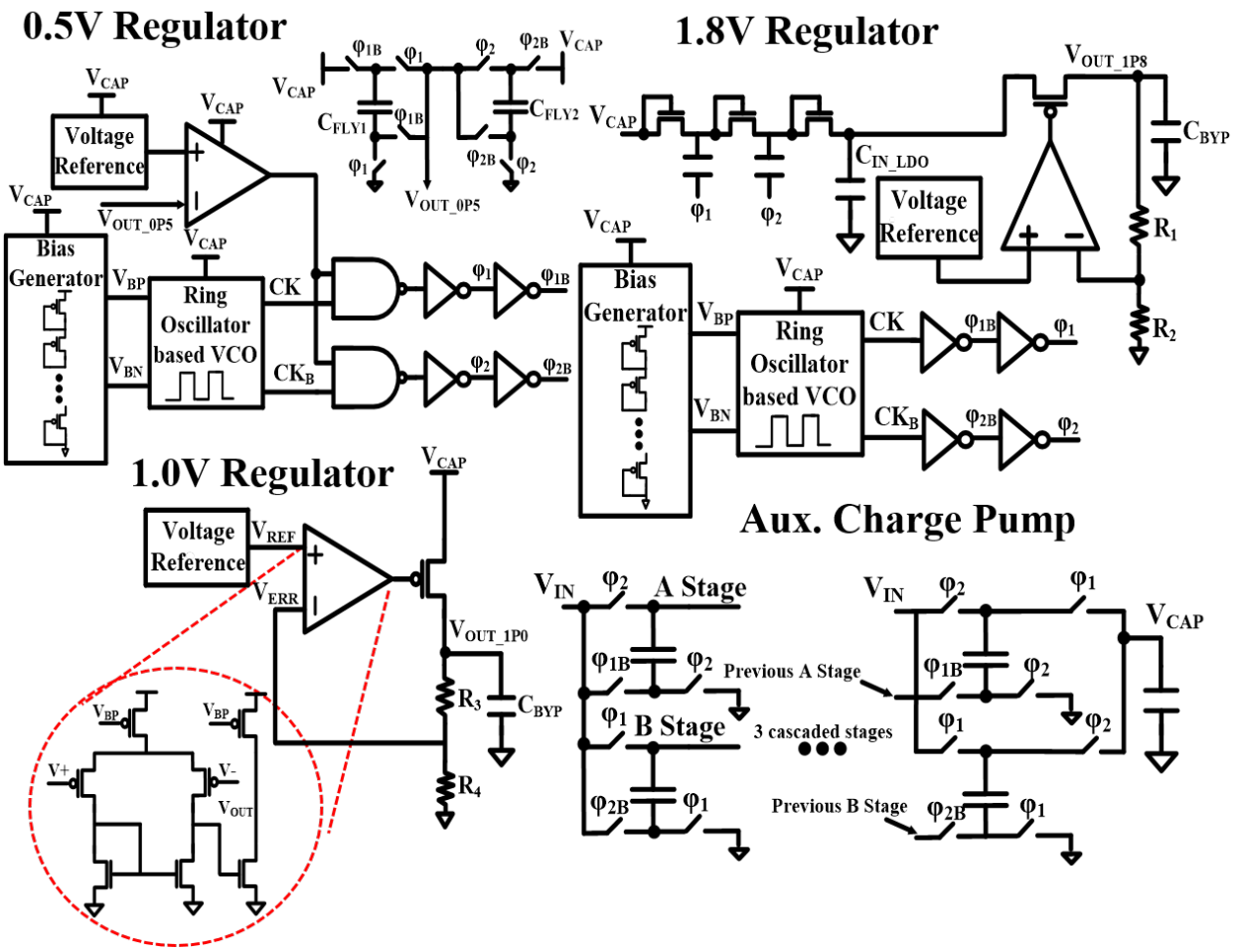


Figure 3.14: Regulator circuits describing powertrain topologies and control schemes [8].

bandwidth of 100 kHz, and 90nW quiescent power. The 1V regulator can support maximum load currents up to 1mA and supports RF applications and sensors that consume high peak currents. The 1.8V regulator consists of a 3-stage Dickson Charge pump topology followed by an LDO. The 1.8V regulator supports a maximum load of 10μW, which is sufficient for digital I/Os and other commercial-off-the-shelf ULP sensors.

3.4.2 Gate leakage based reference generator

In most voltage regulators and power delivery circuits, a stable reference generator is required which provides a reference voltage (V_{REF}) ideally invariant to temperature and power supply variations. Traditionally, Bandgap Reference (BGR) architectures are used in the

design of such reference generators. Although BGR architectures provide good temperature compensation and power supply rejection, they generally require higher voltage headroom to operate, consume higher power (typically 10s of μWs), need a start-up scheme, and are sensitive to process variations. Recently, low-power BGR architectures consuming power in the range of 10s of nW have been proposed [43], which are operational from a low supply voltage but compromise on line and temperature sensitivity. Non-BGR architectures such as [57] consume low power (10s of pW) but provide poor power supply rejection and are highly sensitive to process variation and device noise. In this work, we propose a 1.1nW ULP temperature compensated gate current (I_{GATE}) based reference generator used in all the three regulators to reduce quiescent power.

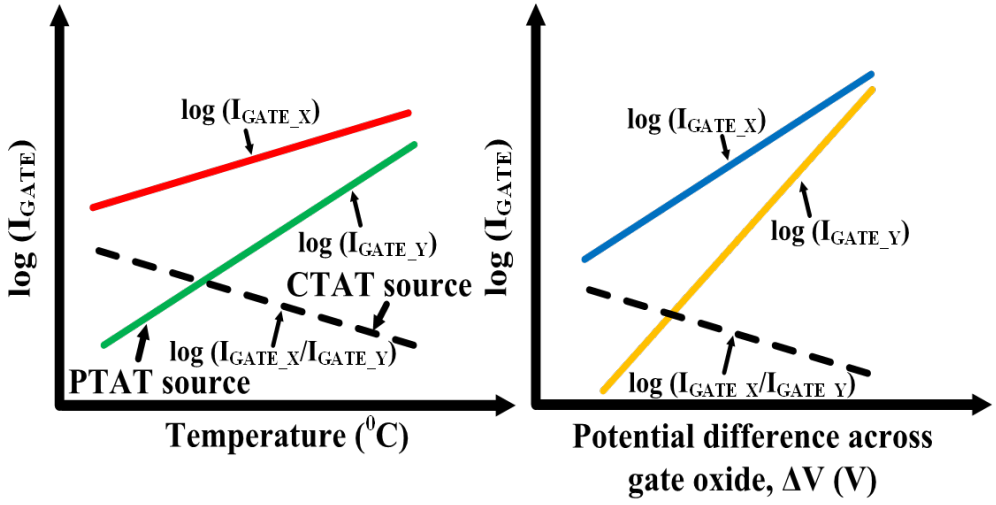


Figure 3.15: Variation of Gate current (I_{GATE}) for devices X and Y with temperature and supply voltage [8].

Figure 3.15 shows the concept of the proposed reference generator. The functions $\log(I_{GATE})$ vs. temperature and $\log(I_{GATE})$ vs. ΔV for both devices X and Y are monotonically increasing and linear to the first order. The slopes of $\log(I_{GATE\_X})$ and $\log(I_{GATE\_Y})$ are different with respect to temperature and ΔV. Hence the function $\log(I_{GATE\_X})$ - $\log(I_{GATE\_Y})$ i.e. $\log(\frac{I_{GATE\_X}}{I_{GATE\_Y}})$ is monotonically decreasing with respect to temperature or ΔV, thus acting as a Complementary to Absolute Temperature (CTAT) source. Either $\log(I_{GATE\_Y})$ or $\log(I_{GATE\_X})$ approximates a Proportional to Absolute Temperature (PTAT)

source. Hence the weighted sum of $\log(I_{GATE\_Y})$ (PTAT) and $\log(\frac{I_{GATE\_X}}{I_{GATE\_Y}})$ (CTAT) should ideally be invariant to temperature and ΔV.

$$V_{REF} = K \log I_{REF} = A \log I_{GATE\_Y} + B.\log \frac{I_{GATE\_X}}{I_{GATE\_Y}} \tag{3.11}$$

where K, A and B are dependent on device sizing (W/L ratios) and technology-specific parameters such as mobility, subthreshold slope, etc.

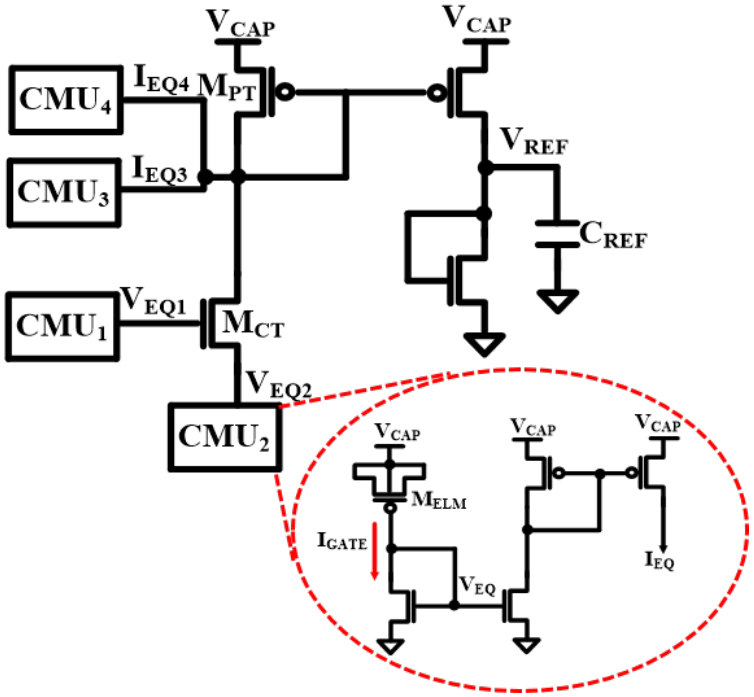


Figure 3.16: Circuit architecture of the proposed reference generator [8].

Figure 3.16 shows the implementation and architecture of the proposed reference generator used in all three regulators to reduce quiescent power. It consists of four Current Mirror Units (CMUs). Each Current Mirror Unit (CMU) consists of a gate-leakage element, M_{ELM}, providing the gate current, I_{GATE}, and $V_{EQ} \sim \log I_{GATE}$. CMUs 1 and 2 consist of low-V_{th} and high-V_{th} PFETs, while CMUs 3 and 4 consist of low-V_{th} and high-V_{th} NFETs. CMU1, CMU2, and M_{CT} provide the CTAT current, while CMU3, CMU4, and M_{PT} provide the PTAT current, which are summed to generate the reference voltage, V_{REF}. Relative sizing of M_{PT}, M_{CT} and M_{ELM} in each of the CMUs ensures a $V_{REF} = 0.2$V, with V_{CAP} ranging from 0.5-

1.2V. To reduce the impacts of device mismatch and process variation, four binary-weighted

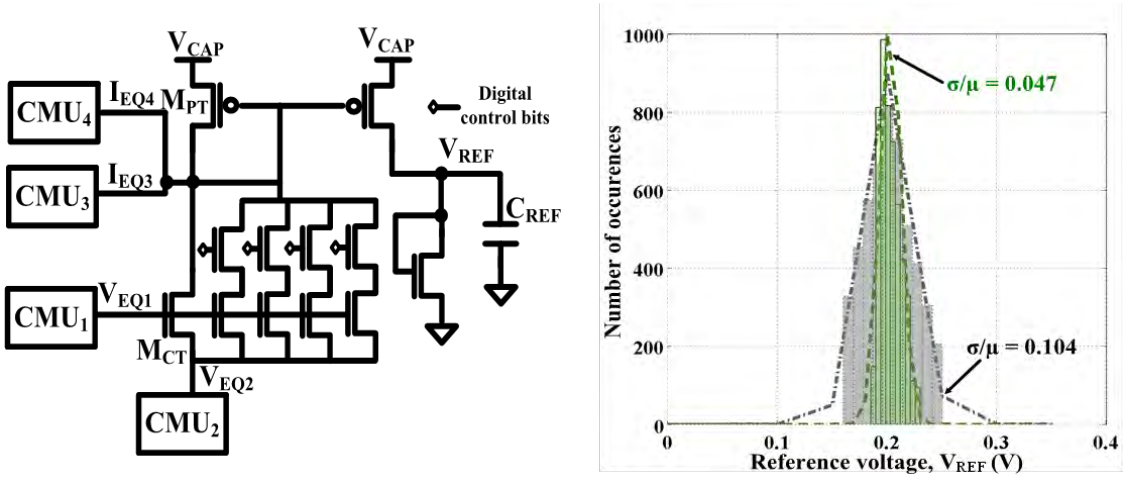


Figure 3.17: Reference generator with digital control bits to limit process variation [8].

digital control bits are added to the reference generator. Figure 3.17 shows the topology of the process compensated variant of the proposed reference generator. We performed 5000-point Monte Carlo simulations across different global corners. At the typical-typical (tt) corner, the $\frac{\sigma}{\mu}$ of V_{REF} in the process compensated version shows an improvement of 54.8% as compared to the uncompensated version. Figure 3.18 shows the simulated Power

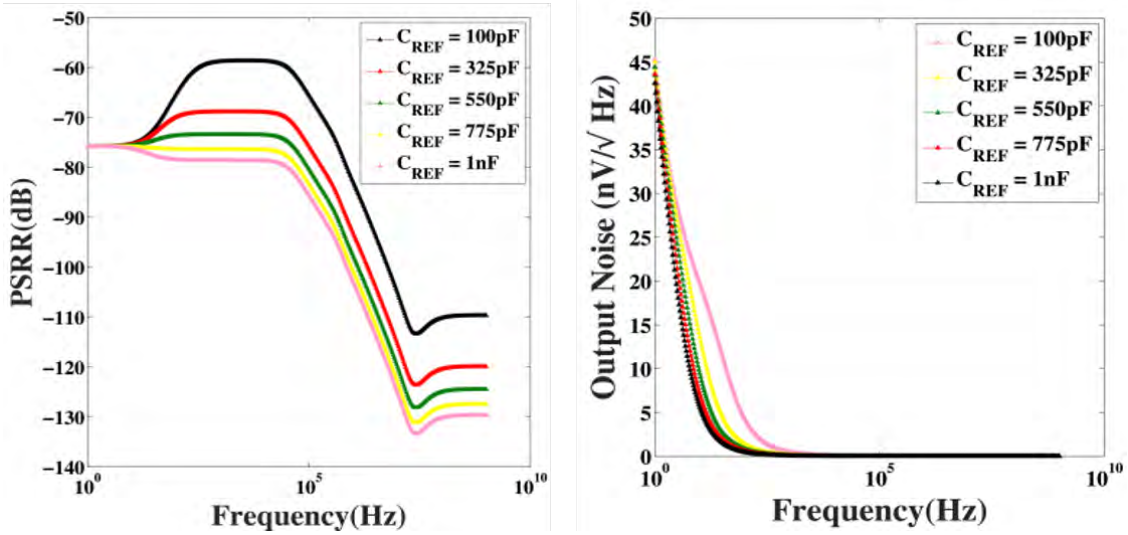


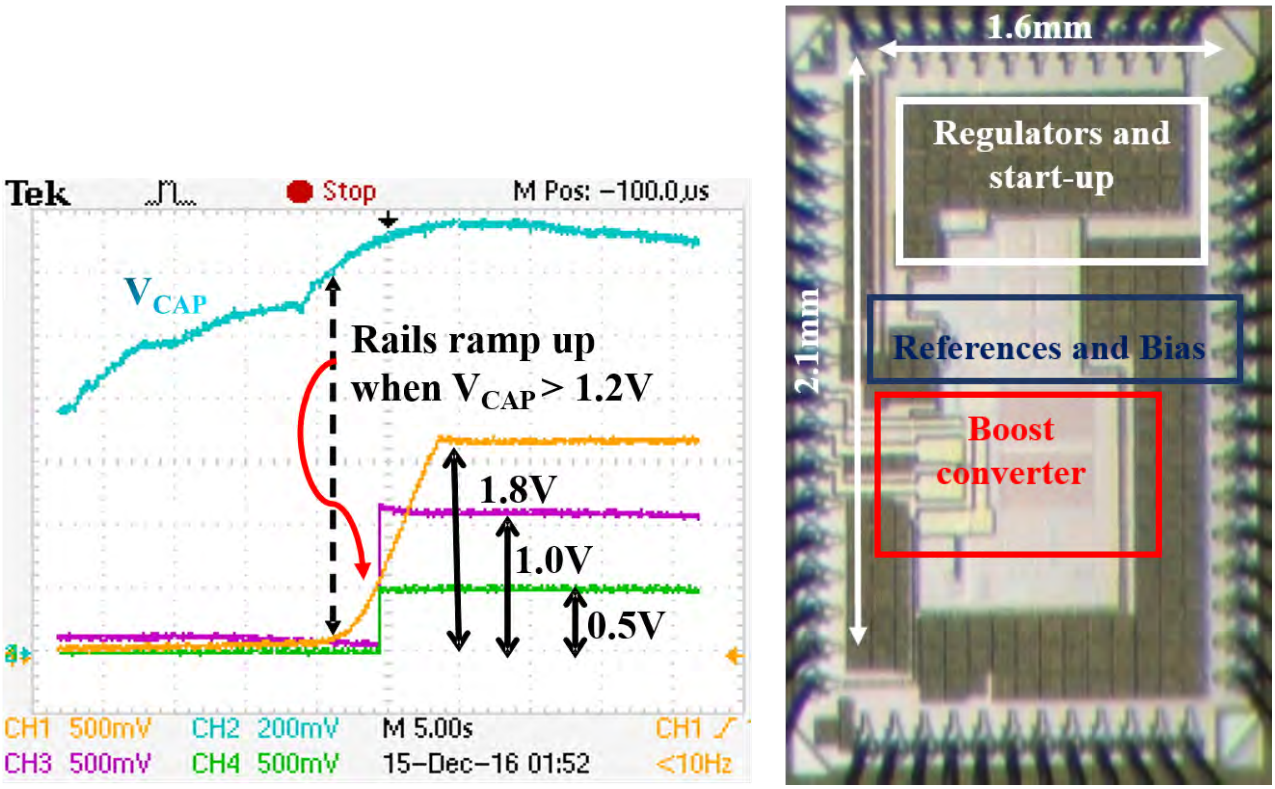
Figure 3.18: Simulated Power supply rejection and output noise spectral density of the reference generator [8].

Supply Rejection Ratio (PSRR) and the output noise vs frequency spectrum of the proposed

reference generator for different values of the filtering capacitance, C_{REF}. Roughly 500pF of on-die filtering capacitance would be sufficient to achieve a low-frequency PSRR of $<$ -75dB and noise density of $< 45\frac{nV}{\sqrt{Hz}}$.

3.4.3 Measurement results

The EH-PMU was fabricated in 0.13μm CMOS technology. Figure 3.19a shows the measured cold-start waveforms of the EH-PMU with an indoor solar cell (open-circuit voltage of 600mV) and a 10mF supercapacitor for storage to demonstrate energy harvesting. When $V_{CAP} >$ 1.2V, the rails ramp up beginning with the 1.8V followed by the 1V and 0.5V rails. Figure



(a) (b)

Figure 3.19: (a) Measured cold-start waveforms (b) Chip micrograph [8]

3.20 shows the measured startup of the proposed gate-leakage based reference generator. The circuit is operational from $V_{CAP} = 0.5$V and has a startup time of 11.2ms which can be

Table 3.2: Comparison of proposed reference generator

	This work[8]	[43]	[57]
Power consumption	**390pW@0.5V (1.3nW@1V)**	32nW@0.5V	2.2pW@0.5V
TC (ppm/°C)	**28.8**	75	19.4
PSR(dB)	**-76@100Hz**	-40@dc	-70@100Hz
LS (%/V)	**0.07**	2	0.033

improved by reducing the size of the filtering capacitor, C_{REF} at the cost of PSRR and higher noise density. Figure 3.21 shows the measured performance of the reference generator, which

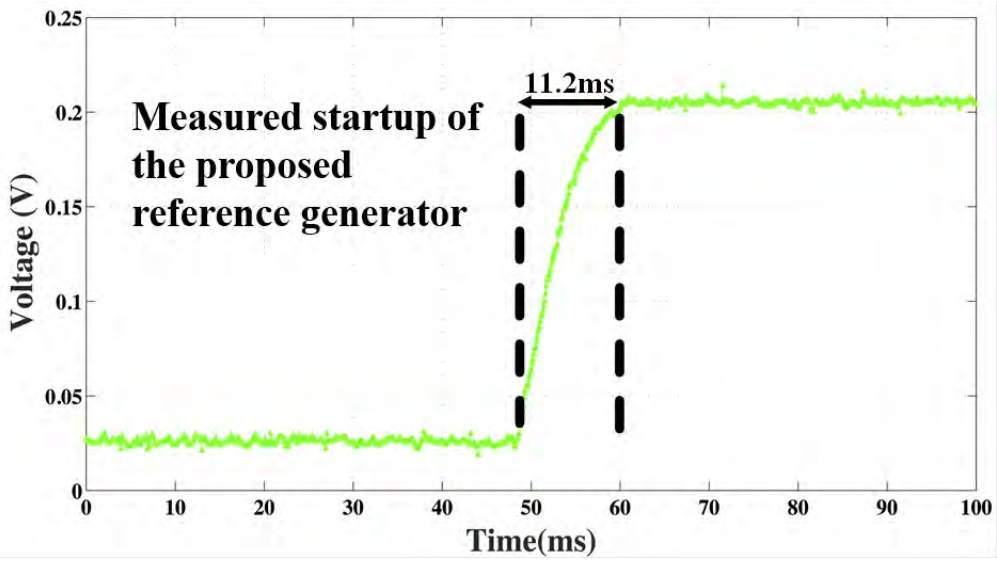


Figure 3.20: Measured startup of the reference generator [8].

achieves an ∼80X reduction in power vs. [43] and improves Power Supply Rejection (PSR) with -76dB at 100Hz vs. [57]. The measured LS and Temperature Coefficient (TC) across 5 chips are 0.07%/V and 28.8ppm/°C, respectively. Table 3.2 compares the proposed reference generator with prior work. Figure 3.22 shows the measured efficiency of the EH-PMU. At V_{CAP} = 1.2V, the regulators achieve peak efficiencies of 88.3%, 82.5%, and 75% for the 1V, 0.5V, and 1.8V rails respectively. Overall, the EH-PMU achieves peak end-to-end efficiency of 71.1% at V_{IN} = 600mV with a 1 μW load. Table 3.3 compares the proposed EH-PMU with prior work.

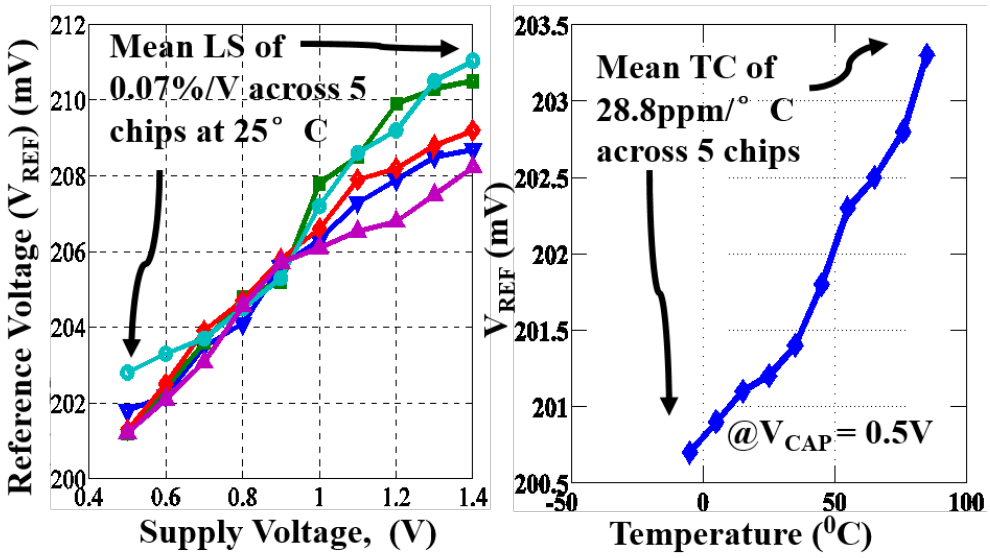


Figure 3.21: Measured performance of the reference generator [8].

Table 3.3: Comparison of EH-PMU with existing work

	This work [8]	[23]	[24]	[25]
Source	**PV,TEG**	PV,TEG	Battery	PV
Storage	**Supercap**	Supercap	-	-
Topology	**Hybrid (Inductor+SC)**	Inductor	SC	SC
# of outputs	**3**	2	3	1
Output voltages	**0.5V, 1V, 1.8V**	0.5V, 1.2V	0.6V, 1.2V, 3.3V	1.4V
Load Power range	**0-1mW@1V 0-500μW@0.5V 0-10μW@1.8V**	0-5mW	20nW-500μW	0-12μW
η@load power	**71.1%@ 1μW end-end harv+reg**	36%@ 1 μW (75%@ 100μW) harv+reg	68%@ 1 μW Only dc-dc reg	58%@ 11μW harv+reg
Process	**0.13μm**	0.13μm	0.18μm	0.13μm

3.5 List of Contributions

- Performed design validation of a Single Inductor Multiple Output(SIMO) DC-DC converter. The buck-boost converter is operational from a low voltage i.e. 0.7V and

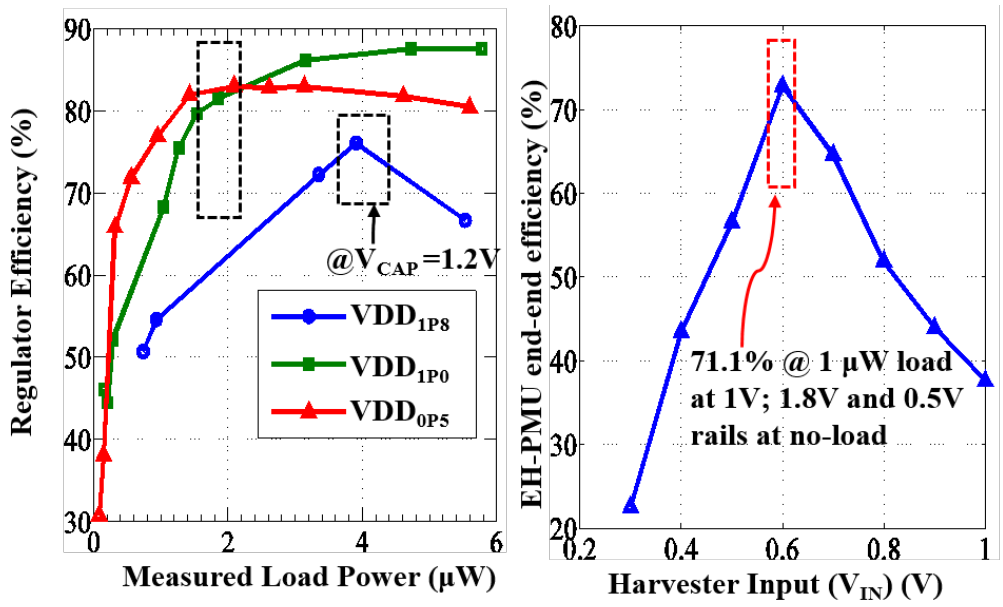


Figure 3.22: Measured efficiency of the EH-PMU and voltage regulators [8].

achieves a peak efficiency of 95% at 4mW load power. Compared to the state-of-the art, this work enables <1V operation for switching converters supporting a similar load power range. Although the SIMO architecture was operational from a low voltage but it was found that its quiescent power consumption ranged in the order of a few μW making it sub-optimal for wearable applications (e.g. BSN). A common powertrain for the different voltage rails resulted in cross-regulation issues.

- Introduced a fully-integrated regulator architecture which provided three separate rails with independent powertrain and control for different categories of load (e.g. analog, digital, external sensors). The end-to-end power efficiency of the regulator and harvester was measured to be 71.1% at 1μW load which provides ~30% improvement over [23].

A 30% improvement in conversion efficiency translates to a 30% improvement in system lifetime in the absence of harvesting. Additionally, a 30% improvement in end-to-end efficiency allows a designer to integrate correspondingly greater functionality, such as more sensing modalities and processing or higher duty-cycle for periodically active components.

- Introduced a novel gate-current based reference generator operational from a low voltage and consuming low power (hundreds of pW to a few nW depending on the voltage on the storage node). The reference generator presented in this chapter achieves an ∼80X reduction in power vs. [43] and improves PSR with -76dB at 100Hz vs. [57]

3.6 Conclusions

This chapter presents a Single Inductor Multiple Output (SIMO) buck-boost DC-DC converter that can regulate from a very low input voltage (starting from 0.7V) and achieve a peak efficiency of 95% at higher load currents ($> 100\mu A$). The buck-boost regulation scheme can offer significant advantages in system lifetime due to its ability to operate from 50% lower voltage or 75% lower energy levels on the storage device as compared to existing work. In the absence of harvesting, for a given load, this amounts to a proportional improvement in operational lifetime. However, it was found that the efficiency of the SIMO is poor at light load currents (below 1μA) due to the high quiescent current consumption(∼2.5-3μA) of the buck-boost control circuits. Moreover, multiplexing a single inductor for generating different voltage rails resulted in cross-regulation issues which reduced the power conversion efficiency. Hence, it was found that a modular design approach was necessary to reduce system complexity, improve system reliability and performance. Regulators for each voltage domain (1.8V, 1V and 0.5V) consisted of independent, load-specific controllers with low I_Q and separate powertrain structures to avoid cross-regulation issues to improve performance during load transients. To improve the power efficiency at light-to-medium loads($< 1\mu A$

to tens of μA) common in self-powered, battery-less systems catering to biomedical and wearable applications, this chapter presents an integrated energy harvesting and power delivery platform with a start-up controller to ensure a sequenced power boot-up necessary for reliable operation. To achieve high end-to-end power efficiency, this chapter presents an ULP process and temperature-compensated gate-leakage based reference generator operational from a low supply voltage (0.5V), used extensively for power delivery. The controller circuits consume 10X lower static power as compared to [21] in order to improve the overall system lifetime in the absence of harvesting. The availability of three different regulated, power-efficient voltage rails provides a system designer to integrate and support additional sensor interfaces and processors as loads. A 25-30% improvement in end-to-end power efficiency over prior work serves to incorporate additional duty-cycling for periodically active components and expands the ability to include correspondingly more "always-ON" components, such as wake-up timers.

Chapter 4

Power Supply Variation in ULP systems

4.1 Motivation

Variation in on-chip power supply continues to be a major challenge in modern CMOS processes due to technology scaling resulting in increasing device densities and operating currents. Since the length of global wires such as power and ground lines does not scale at the same rate as device dimensions, IR-drop continues to increase in deep-sub-micron processes. Since most modern microprocessors operate at clock frequencies in the GHz regime [58], such systems are most susceptible to $\frac{Ldi}{dt}$ events, resulting in power supply overshoots and undershoots. While supply overshoots can cause reliability issues such as gate-oxide breakdown and Hot Carrier Injection (HCI), supply undershoots can result in timing violations such as setup-time and hold-time failures. Thus, power supply droops can limit the Maximum Operating Frequency (FMAX) of a modern microprocessor. In self-powered ULP systems, the magnitude of load current transients is negligible except when the system is in a mode where it needs to acquire physical data or send data over a radio link. Hence, it is hypothesized that line and load regulation requirements for powering digital

circuits in ULP systems can be relaxed to some degree. Variation in the power supply can result in timing errors in low-voltage circuits as well [59]. Additionally, analog and mixed signal components such as the radio or the analog front-end need a tight line and load regulation even in ULP systems. Hence, there is a need for a low-cost, low power method to monitor voltage variation even in ULP systems to account for the trade-off between relaxed voltage regulation and the susceptibility of digital circuits to timing failures.

4.2 Background

An $\frac{Ldi}{dt}$ event occurs if there is a sudden change in the current consumption, especially when the microprocessor switches from one operating mode to another, resulting in high-frequency overshoot or undershoot noise. Resonant supply noise in the mid-frequency range is another source of power supply noise, which results mainly from the resonance of the package inductance and the decoupling capacitors [60]. During Dynamic Voltage Scaling (DVS), the slow transient response time of voltage regulators can result in low-frequency droops. Figure 4.1 describes the two major sources of power supply fluctuations. High-frequency noise is generally induced on the supply due to $\frac{Ldi}{dt}$ events and influences timing in local circuit paths. Noise due to package resonance and low-frequency droops takes time to recover and thus is present for multiple clock cycles and impacts performance globally across the chip. Existing work in literature such as [61] has proposed on-die dynamic voltage monitoring and adaptive clock distribution schemes to enable tolerance to power supply variations across a wide operating range. In [62], techniques for timing error detection and correction are proposed to reduce metastability occurring due to dynamic power supply and temperature variations. Analog techniques have been employed in [9] where on-die sensors are distributed to monitor peak overshoots and undershoots. Adding decoupling capacitors can reduce dynamic IR-drop. Active decoupling capacitors can compensate the noise in the low to mid-frequency range [60]. However adding decoupling capacitors increases gate leakage. Analog droop monitors [9]

and metastability detectors [62] consume higher quiescent currents. Hence such techniques cannot be applied directly in subthreshold processors such as [23][63] which are used in energy-constrained systems such as wireless sensor nodes and other applications related to the IoT. To conclude this section, commonly used techniques to minimize power supply noise are summarized as below:

4.2.1 Decoupling capacitors

Adding decoupling capacitors is a part of the standard physical design flow to resolve issues related to dynamic IR-drop. However, adding a large number of decoupling capacitors increases gate leakage. Thus, the designer needs to be more prudent with adding decoupling capacitors in ULP systems.

4.2.2 Methodology and design automation to analyze IR-drop

Designers mostly use prior experience or back-of-the-envelope calculations to justify the amount of decoupling capacitance in an SoC. This is dependent on the technology, package parasitics, load current profile in different operating modes and the sensitivity of custom macros to power supply variation. Vector-based dynamic-IR analysis is commonly used to optimize the amount of decoupling capacitance required. Vector-based IR-drop analysis enables the designer to address power supply variation, without compromising on leakage.

4.2.3 Active decoupling capacitors/Droop detectors

The basic concept behind active decoupling capacitors is to switch a pair of parallel decoupling capacitors to a series combination to give a local voltage boost in the presence of power supply droops. The control schemes for these switches have been implemented using power-hungry wideband comparators [64] and opamps [60], which will not meet the power constraints of ULP systems. Droop detectors to sense high frequency supply noise need to have a wide

bandwidth. In ULP systems, since high frequency noise is less common, droop detectors can be used to monitor low-frequency supply voltage drift and are commonly used in the control schemes of voltage regulators.

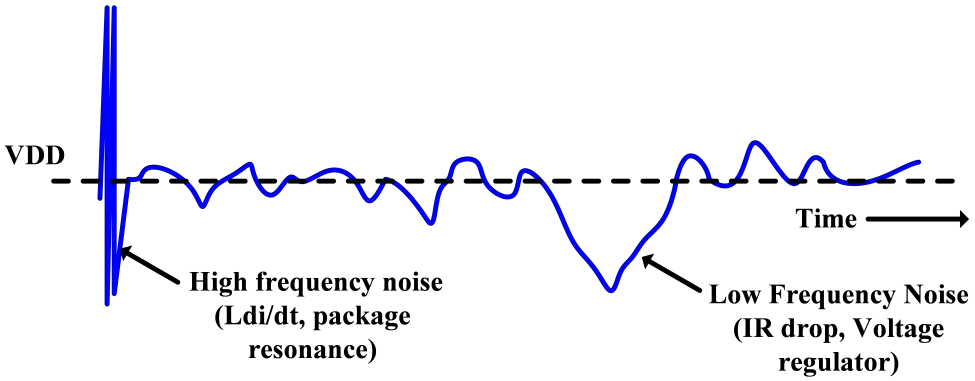


Figure 4.1: Examples of power supply noise [9]

4.3 Comparison of Latch and Register based implementations

A latch-based pipeline stage typically allows the designer to achieve higher performance than a register-based implementation owing to time-borrowing and allowing greater setup-time margin as compared to a flip-flop. Assuming no clock skew, the setup-time constraint for a latch is:

$$T_{clk\_period\_latch} + T_{wind} > T_{d-q} + T_{prop\_delay} + T_{setup\_time} \tag{4.1}$$

where,

T_{wind} = transparency window of a latch

$T_{clk\_period\_latch}$ = clock period of latch-based stage

T_{d-q} = input data to latch output delay

T_{prop_delay} = propagation delay

T_{setup_time} = setup time constraint

Similarly for a flip-flop based design,

$$T_{clk\_period\_FF} > T_{clk-q} + T_{prop\_delay} + T_{setup\_time} \tag{4.2}$$

where,

$T_{clk\_period\_FF}$ = clock period of flip-flop based stage

T_{clk-q} = clock to flip-flop output delay

Hence, $T_{clk\_period\_latch} < T_{clk\_period\_FF}$ which means that a latch-based pipeline stage can operate at a higher clock frequency than a flip-flop-based stage. Moreover, since a latch-based pipeline provides an additional transparency window, the incoming data has an additional setup-time margin equivalent to T_{wind}, which aids in resolving metastability issues arising due to power supply variations and low-frequency supply noise. Short-paths in a latch-based design can be avoided as long as,

$$T_{wind} + T_{hold\_time} < T_{d-q} + T_{prop\_delay} \tag{4.3}$$

where,

T_{hold_time} = hold time constraint

Although a flip-flop based timing path has greater hold-time margin as compared to a latch-based path, employing out-of-phase non-overlapping clock signals can offset this limitation.

To demonstrate the circuit robustness of a latch-based implementation to power supply variation, we analyzed the impact of low-frequency power supply droops on both register-based and latch-based implementations of a 32-tap FIR filter across a wide range of supply voltages. FIR filters play an important role in most low-power as well as high-performance Digital Signal Processing (DSP) applications [65]. We investigate the circuit robustness to power supply variation for both latch-based and register-based versions of the FIR filter by

measuring the Energy-Delay (E-D) trends. We use E-D curves as a metric to evaluate the resiliency of a synthesized digital circuit (in this case an FIR filter) to power supply variations. Figure 4.2a describes the block diagram of the system designed for analyzing and comparing

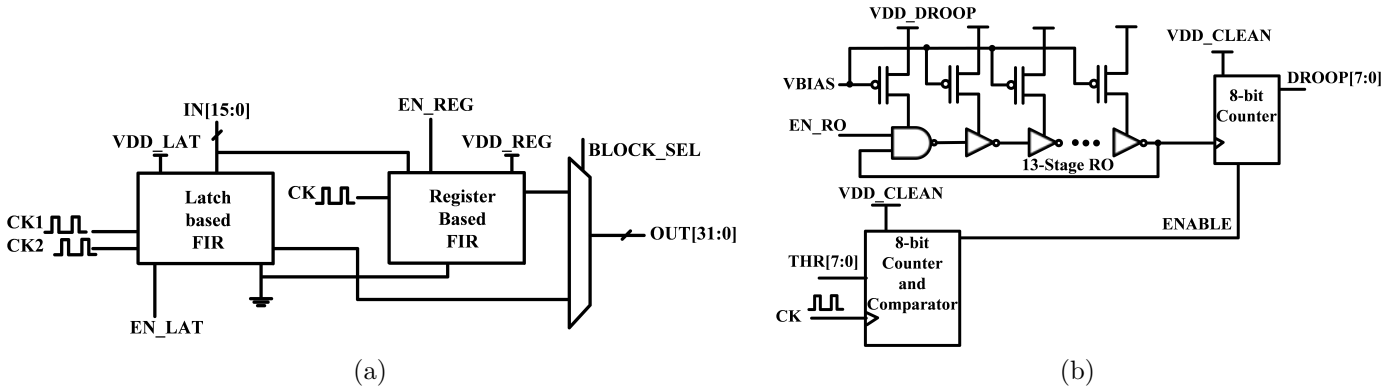


Figure 4.2: (a) Block Diagram and (b) Droop measurement circuit [2]

the impact of power-supply variation on latch-based and register-based versions of the FIR filter. We implement a 16-bit, 32-tap FIR filter using both flip-flops and latches. For the latch-based implementation, we incorporate a dual-phase non-overlapping clock architecture to reduce the probability of hold-time failures. Both the latch- based and register-based FIR filters have dedicated enable signals and supply rails while they share a common reset and ground rail. A global block-select signal helps in selecting the 32-bit output from each FIR filter.

4.4 All digital droop detection and measurement

We implement a low-power technique using digital circuits to measure the low-frequency droop present in the power supply. Figure 4.2b describes the proposed droop measurement scheme. The core of the droop measurement circuit is an on-chip 13-stage current-starved RO operating from the supply rail, VDD_DROOP, which contains voltage droops. The ring oscillator is biased in subthreshold by an external bias signal, VBIAS, which can be generated by an ultra-low-power bandgap reference such as [43]. An 8-bit digital counter and

comparator are powered by a clean, well-regulated supply without ripple, VDD_CLEAN. This 8-bit counter and comparator logic compares the number of clock cycles with a programmable 8-bit user-defined threshold, THR and generates an enable/disable signal to count the number of RO clock cycles denoted by DROOP. The number of RO clock cycles will vary depending on the magnitude of droop present. The difference between DROOP and THR provides an 8-bit digital proxy measurement for the amount of supply droop present. At a system-level, VDD_CLEAN can be obtained from a voltage regulator such as the buck-boost regulator proposed in [23]. An on-chip voltage regulator needs to provide high conversion efficiency for a target load current range. For a fixed conversion efficiency of a regulator, a lower-power droop monitoring circuit would reduce the overhead on the limited power budget of an energy-constrained system. Figure 4.3 describes the droop injection circuit used to inject

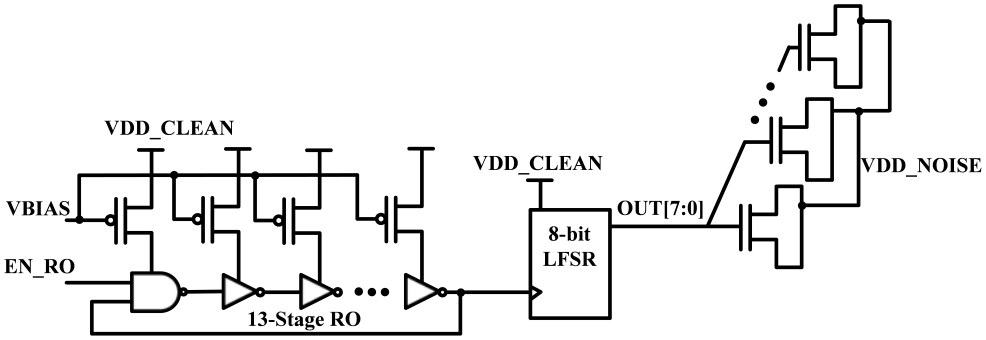


Figure 4.3: Droop injection circuit [2]

supply noise onto the supply rails for test purposes. A 13-stage current starved RO operating from a clean supply voltage devoid of supply noise, VDD_CLEAN provides the clock to an 8-bit Linear Feedback Shift Register (LFSR) unit to generate an 8-bit pseudo-random sequence. This 8-bit sequence couples pseudo-random noise onto the supply rail, VDD_NOISE using MOS capacitors. The RO clock period can be controlled externally using the bias signal, VBIAS, to provide the desired clock frequency. The injected droop can be measured by the droop measurement scheme described in Figure 4.2b

4.5 Measurement results

Fabricated in a 130nm CMOS process, the testchip was packaged in a 64-pin PGA package for testing convenience. A Link Instruments IO3200 pattern generator/logic analyzer module was used to provide input patterns and off-chip clock signals to both latch-based and register-based FIR filters. Current measurements were performed using a Keithley 2401 sourcemeter. External droop was added to the supply with a function generator. A 1 kHz saw-tooth waveform of varying peak-to-peak amplitude was coupled to the power supply. External

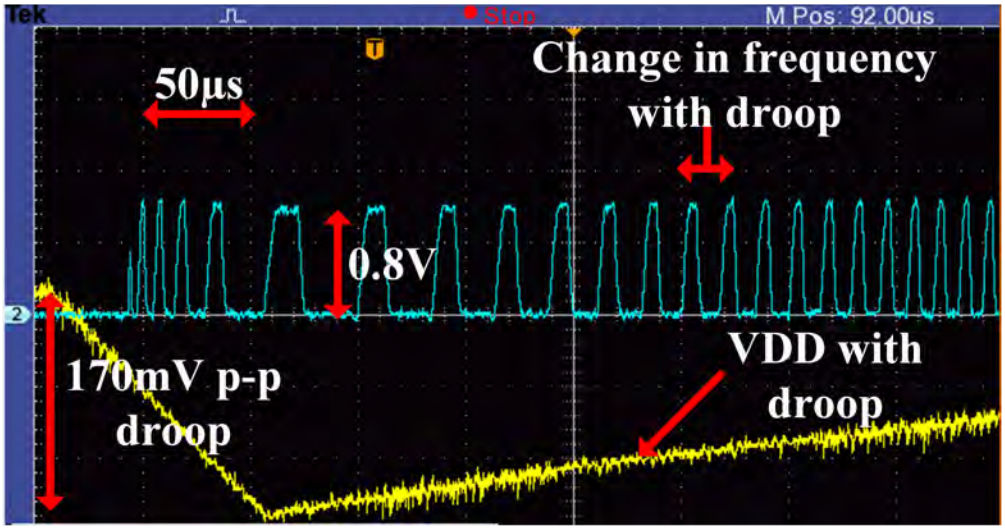


Figure 4.4: Variation in RO frequency with supply voltage variation [2]

noise and supply droop can be injected off-chip by coupling a fast rising ramp signal to the power supply using a large coupling capacitor in the order of 47μF or higher. Figure 4.4 shows the oscilloscope waveform of a power supply where external noise has been added. The variation in frequency of the RO described in Figure 4.2b, which operates at VDD_DROOP, is shown. Table 4.1 shows the measured hex-equivalent of the droop present on a 0.8V supply with THR set at 0xAA. Figure 4.5 shows the variation of power consumption of the droop measurement unit with the supply voltage. The measured power includes power consumption of the ring oscillator, counters and comparator logic. Measurements show that the droop measurement circuit consumes less than 1.5μW across a range of supply voltage ranging from 0.5-0.8V and can be leveraged in ULP systems such as wireless sensor

Table 4.1: Measured HEX equivalent of droop (THR: 0xAA) [2]

VDD (V)	Peak-Peak Droop (mV)	Hex equivalent
0.8	48	0x07
0.8	72	0x19
0.8	104	0x4A
0.8	128	0x6E

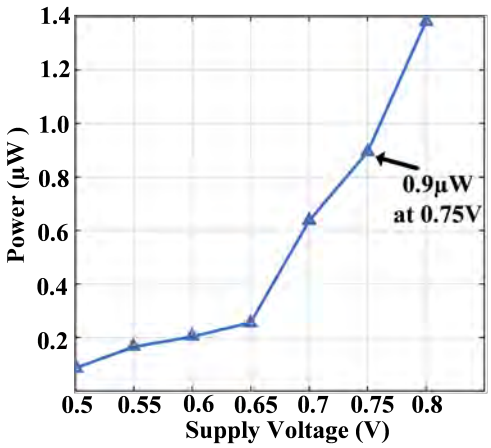


Figure 4.5: Measured power of droop measurement unit [2]

nodes. Figure 4.6 shows the energy-delay trends of both the latch-based and register-based FIR filters both with and without externally injected Power Supply Noise (PSN). Figure 4.6 shows that the latch-based implementation provides 25-37% improvements in energy-efficiency below 0.6V in the presence of 1kHz power supply droop ranging from 44-120mV. At higher voltages and operating frequencies, the register-based implementation provides better energy-efficiency. This is because active-energy dominates at higher voltages and the latch-based implementation has a higher switching capacitance owing to a dual-phase clocking scheme. Figure 4.7 shows a chip micrograph of the implementation. Table 4.2 compares the proposed droop measurement scheme with the existing droop measurement techniques in literature. In [61], a dynamic variation monitor (DVM) is proposed to monitor high-frequency voltage fluctuations and consists of and an adaptive clock distribution (ACD) scheme to tune the system clock frequency. The DVM and ACD consume 2.5mW (1% of the total power consumption). In [9], an on-die high-frequency supply droop detector using analog circuit

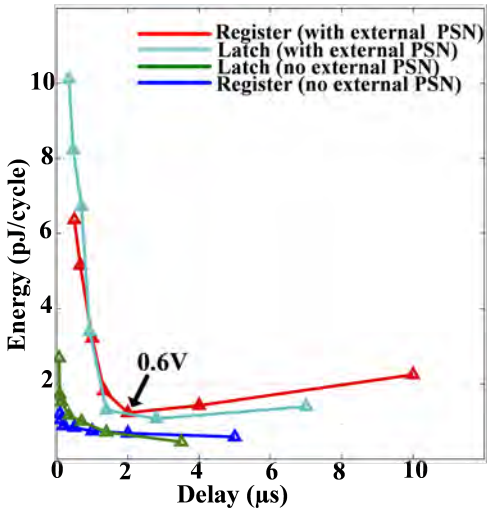


Figure 4.6: Measured Energy-Delay trends of latch-based and flip-flop based FIR filters [2]

Table 4.2: Comparison of Droop Measurement Unit with existing work

	[61]	[9]	[59]	**This Work [2]**
Technology	16nm FinFET	90nm bulk	0.13μm bulk	**0.13μm bulk**
Supply Voltage	0.7-0.95V	0.7V-1.3V	0.74-1.3V	**0.5-0.8V**
Analog/Digital	Digital	Analog	Digital	**Digital**
Area	2590μm^2	–	9060μm^2	**7100μm^2**
Power Consumption	2.5mW at 0.9V	–	46.4-56μW at 0.81V	**0.9μW at 0.75V**
Max Droop Range	90mV at 0.9V	270mV at 1V	189mV at 0.81V	**44-170mV at 0.5-0.8V**
High/Low frequency	High	High	Low	**Low**

techniques is proposed for noise detection and digital circuits are used for measurement and calibration. In [59], an adaptive clocking scheme using a critical path replica is proposed to modulate the global system clock and local clocks in presence of power supply noise. The droop monitoring circuits in both [61] and [59] monitor supply variation above 0.7V and consume higher power as compared to the proposed droop measurement scheme in this paper.

4.6 List of Contributions

- Analyzed the impacts of power supply variation in latch and register based FIR filter implementations using energy-efficiency as a metric. Latch-based implementation was

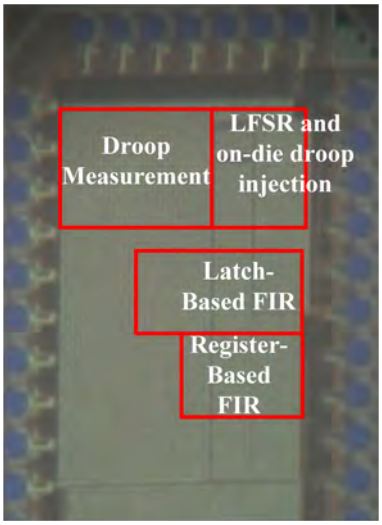


Figure 4.7: Chip Micrograph [2]

found to be more resilient and 25-37% more energy efficient at low-voltages (< 0.6V) subject to a low-frequency(upto 1kHz) supply noise. At higher supply voltages ($>$ 0.6V), active energy is more dominant. Hence, register-based implementation was found to be 60% more energy-efficient, due to greater switching capacitance associated with the latch-based implementation.

- Introduced a low power, supply voltage droop measurement circuit, implemented using all-digital logic. The circuit achieves a $\sim$50X lower power consumption as compared to [59] and can be leveraged in low I_Q controller designs for regulators and power converters.

4.7 Conclusion

In this chapter, the impact of power-supply variation on the energy and performance of latch-based and register-based synthesized digital circuits is compared across a wide-operating range. An all-digital, power-efficient droop measurement and noise-injection technique is discussed. Measurements show that latch-based circuits provide better energy-efficiency and

tolerence to supply variations at lower voltages. Hence a latch-based architecture can be employed in subthreshold processors with variable supply for IoT applications.

Chapter 5

Ultra-low power circuit components

5.1 Motivation

The design of ULP systems for IoT applications, such as health monitoring, surveillance and home automation involves a high degree of system integration, consisting of a variety of circuit components, such as ULP processors, subthreshold DSP accelerators, wakeup radios etc. While power delivery to such components plays a major role in defining the overall system-level power budget and electrical specifications, it is important to investigate circuit or architectural techniques to design and optimize such components for lower power. Before an energy harvesting or a voltage regulation scheme can be designed, it is imperative to understand the power or energy characteristics of such macros and analyze the circuit performance to power supply variations. Technology also plays a major role not only in the design of high-efficiency DC-DC converters and but also assists in lowering the energy or power consumption of circuit components. In this chapter, we will present an energy-efficient MSP430 processor designed in an FDSOI process optimized for subthreshold operation. We will evaluate the energy-delay and leakage power characteristics of a 32-tap FIR filter in a 55nm Deeply Depleted Channel (DDC) technology. Then we will discuss the need for a ULP comparator with a low input-referred offset in a 10nW wakeup radio for ULP applications.

5.2 Background

Wearable sensors, portable biomedical electronics such as Electrocardiogram (ECG) monitors, and self-sustaining surveillance systems need to achieve energy-efficiency and ultra-low standby power. In this section, we will discuss the circuit architecture and implementation of two major components, which play an integral role in such systems.

5.2.1 Subthreshold processors and accelerators

The restrictions in size and the need for a longer operational lifetime render self-powered systems severely energy-constrained. Within the limited energy budget, such systems need to run application-specific programs and sub-routines such as ECG monitoring [23][19]. Hence, energy-efficient processing at the circuit and at the system level is essential to minimize the energy per operation in such systems. Existing work in literature has reported systems or processor implementations consuming nW to μW power levels by operating the system near the threshold voltage (V_{th}) of a transistor [66][55][19][18]. Operating a digital circuit in the subthreshold regime causes transistor leakage to be a dominant source of energy consumption because of exponentially large delays. Prior work in literature such as [55] has proposed digital logic styles to suppress subthreshold leakage of conventional bulk devices. Hence optimizing the leakage characteristics of a device can result in significant benefits at the overall system level. However, low voltage transistor operation presents four key challenges:

1. Minimize the subthreshold swing and achieve maximum ON current below V_{th}
2. Minimize static leakage current
3. Minimize V_{th} variation
4. Minimize device capacitances.

Thus, if the process technology provides CMOS transistors, optimized for lower subthreshold leakage with reduced V_{th} variation and minimal degradation in performance, then

energy-efficient and reliable digital processors and circuits can be implemented for ULP applications.

5.2.2 Detection and digital processing in ULP wakeup radios

To conserve energy, self-powered systems such as wireless sensor nodes spend most of the time in standby mode and perform active operation only when required. To synchronize with the base station and bring the system out of standby mode, a Wake-up radio (WRX) can provide a viable solution. Since a WRX is always active and listens to an incoming RF signal or pattern, the active power of a WRX needs to be lower than the overall standby power of the system, which tends to be in the nW range for digital components. Reducing the power consumption of a WRX comes at the cost of reduced sensitivity to the incoming RF signal. Existing work in literature, such as [67][68] implement a WRX architecture similar to Figure

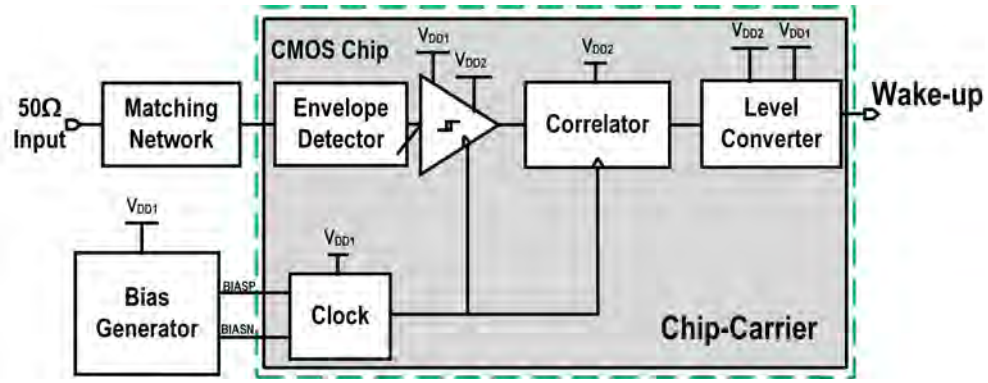


Figure 5.1: Architecture of a Wake-up radio

5.1, where the incoming RF signal is rectified and the output DC voltage from the rectifier is sampled using a low-power comparator. A ULP baseband correlator processes the sampled output from the comparator, compares the sample with an expected code word and issues a wake-up signal. The size of the correlator and the sampling frequency is determined by the overall receiver sensitivity and power budget, which is typically in the nW range. Since the input RF-signal energy is typically limited, the rectified output voltage is restricted to less than 10s of millivolts. As a result, the comparator needs to have a very low input-referred

offset. Moreover, the threshold of the comparator should be controllable to avoid false system wake-ups in the presence of noise or interference. Thus, the comparator needs a mechanism for offset control. Since a WRX is severely power-constrained, the comparator should consume a very low quiescent current (typically less than 10nA). The clocked comparator used in [67] uses a current DAC for setting the bias currents in both the pre-amplifier and the regenerative feedback circuit with the input common mode referenced to ground. The dynamic comparator in [69] consumes very low static current and uses a combination of high-V_{th} and standard-V_{th} devices to reduce leakage with reduced performance penalty. A dual-rail clocked-comparator architecture is proposed in [70] to provide greater resilience to kickback noise.

5.3 A sub-threshold MSP430 processor for energy-efficient IoT applications

This work presents an implementation of a 16-bit MSP430 processor for ULP systems catering to battery-less wireless sensor nodes, biomedical, and other IoT applications. Implemented in a custom extremely low power (xLP) 90nm FDSOI process, the processor consumes 1.3μW operating at 0.4V while executing a peak detection algorithm at 250 kHz. It supports the standard MSP430 Instruction Set Architecture (ISA) and demonstrates QRS peak detection for an ECG application. The measured energy while executing peak detection at 250 kHz was 5pJ per cycle at 0.4V. The fabricated xLP devices show 55% reduction in threshold voltage (V_{th}) variation compared to similar-sized transistors in a traditional FDSOI process.

5.3.1 xLP FDSOI Process and Device Description

The custom low power 90nm (xLP) FDSOI process technology is optimized for near- and subthreshold operation [71]. Figure 5.2 shows a schematic of the xLP FDSOI transistor and compares it against a typical commercial 90nm Partially Depleted Silicon on Insulator (PDSOI) transistor. xLP transistors are fabricated using 30nm Si on 145nm BOX. The gate dielectric

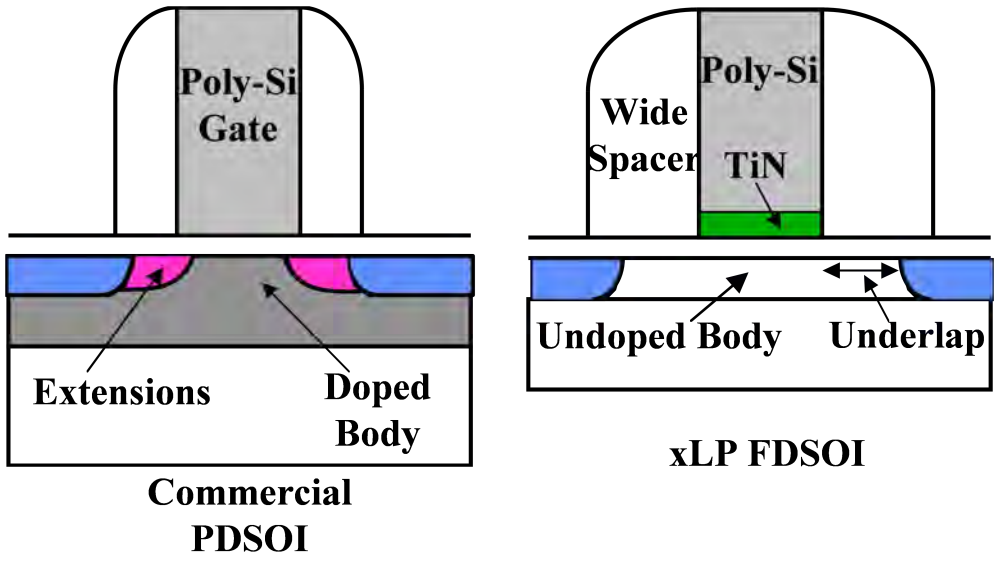


Figure 5.2: Cross-Sectional comparison of a standard PDSOI transistor and the xLP FDSOI transistor [10]

is 3.5nm SiON. Minimum gate lengths of 90nm and gate widths of 120nm are supported. Device engineering includes a 1020°C, 5s rapid thermal anneal, ∼10nm of $CoSi_2$, and a 20-min 400°C hydrogen passivation anneal. The back-end consists of five metal layers of aluminum interconnect and SiO_2 dielectric. Interconnect widths as small as 140nm are supported. Near-ideal subthreshold swing is obtained by using moderately thin FDSOI and maintaining gate lengths of 90nm and longer. Eliminating channel doping reduces the threshold voltage variation caused by non-uniformity in Silicon on Insulator (SOI) thickness and random dopant fluctuations. The threshold voltage and thus leakage current of the transistors is set by a work function-tuned TiN metal gate. A custom Plasma-Enhanced Atomic Layer Deposition (PE-ALD) process for the gate metal was developed. The PE-ALD TiN causes less plasma damage than typical sputtered TiN metal gates resulting in lower gate leakage and less device-to-device variation [72]. By eliminating the source drain extensions and employing wide nitride spacers in the xLP technology, device capacitances are minimized by 76% as compared to commercial FDSOI technology [71]. Figure 5.3 shows the I_{ds}-V_{gs} characteristics of 8μm wide and 150nm long xLP FDSOI n-channel Complementary Metal Oxide Semiconductor (NMOS) and PMOS devices. Inset shows a TEM of a 150nm long

device.

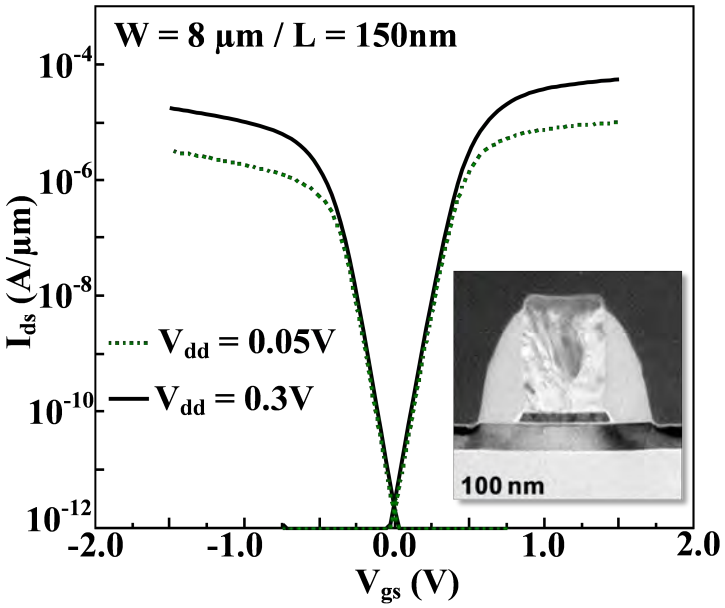


Figure 5.3: I_{ds}-V_{gs} characteristics of FDSOI devices [10]

5.3.2 MSP430 Processor Architecture

The openMSP430 is an open-source MSP430 architecture from opencores.org [73]. It is a 16-bit RISC microcontroller based on the Von-Neumann architecture with a single address space for instructions and data. It is compatible with the MSP430 microcontroller family from Texas Instruments [74]. The core supports a 16 x 16 multiplier, watchdog, and a UART debug interface using standard RS232 serial communication protocols. Figure 5.4 describes the overall architecture of the openMSP430. The UART module in the standard debug interface (SDI) provides 8N1 serial communication with a host computer and enables the processor to be programmed serially [73]. The MSP430 architecture from Opencores supports 1kB of program memory (PMEM) and 128 bytes of data memory (DMEM) [73]. Both the PMEM and DMEM can be accessed using the SDI. The Frontend module fetches the 16-bit instruction from the PMEM and then decodes the instruction. The execution unit comprising of the ALU and the register file executes the decoded instruction. The memory backbone acts

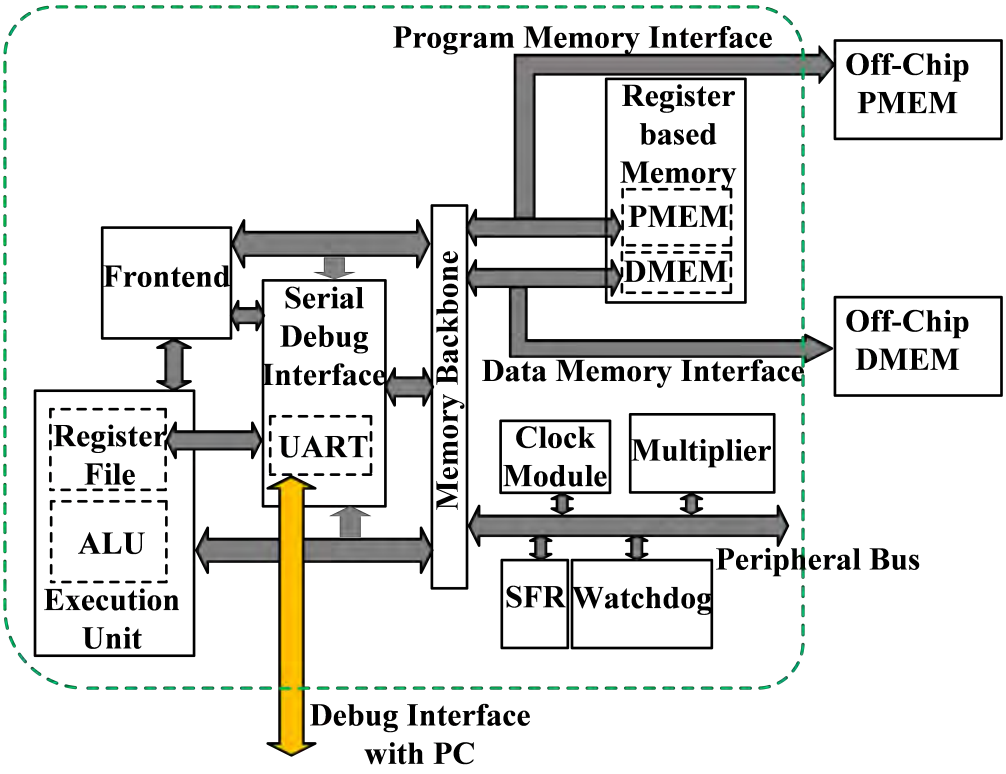
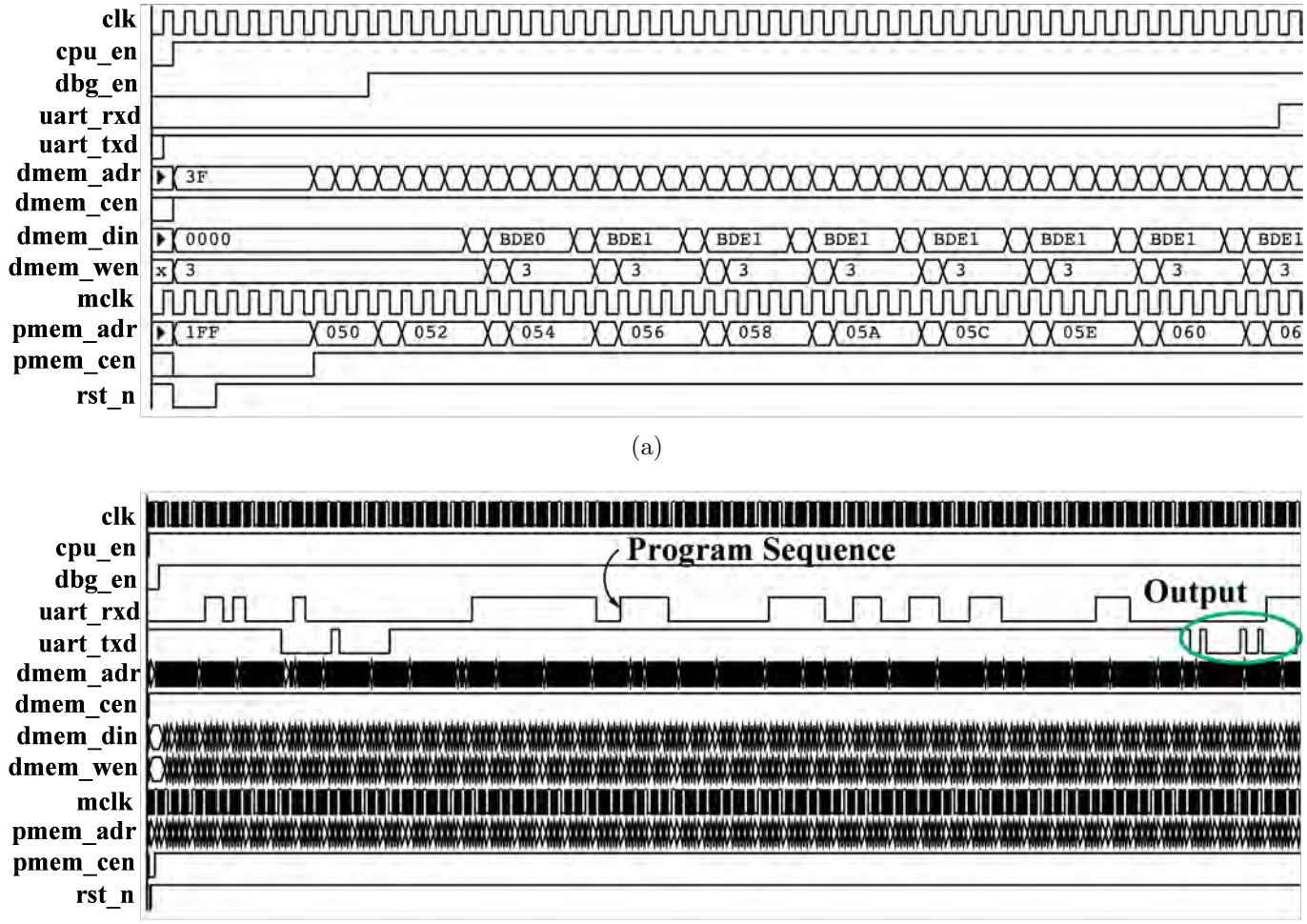


Figure 5.4: OpenMSP430 Architecture [10]

as an arbiter between the frontend, execution unit as well as the SDI and the PMEM/DMEM memories [73]. The architecture supports 512B of memory for peripherals, which include a basic clock module, a hardware multiplier, special function registers (SFRs) and a watchdog unit [74]. Figure 5.5a describes the functional waveforms of the processor after the system comes out of reset followed by loading the PMEM with instructions and DMEM with data for executing a Fibonacci sequence program through the UART interface. Figure 5.5b shows that after the PMEM is loaded with instructions and data, program execution is initiated through the UART and the output is transmitted over UART to the host computer.

5.3.3 Measurement results

Fabricated in the 90nm xLP FDSOI process, the testchip was packaged in a 132-pin Pin Grid Array (PGA) package for testing convenience. The chip was programmed and tested using a Tektronix TLA7012 pattern generator/logic analyzer. Current measurements were performed



(a)

(b)

Figure 5.5: Functional waveforms of MSP430 processor (a) At processor startup (b) Executing a Fibonacci sequence program [10]

using a Keithley 2401 sourcemeter. To demonstrate processor functionality, measurements were taken by executing three different programs: A simple adder program to add and store two unsigned 16-bit integers, a program to generate and store the nth order Fibonacci sequence, where n is a programmable input set by the user, and a QRS peak detection algorithm [75] to detect sparse spikes in a measured ECG datastream. In this implementation, since Program Memory (PMEM) and Data Memory (DMEM) are register-based and not Static Random Access Memory (SRAM)s or custom memories, performance and energy metrics of the memory system is not measured and not taken into consideration. Figure 5.6 shows the measured functional waveforms of the Universal Asynchronous Receiver/Transmitter (UART)

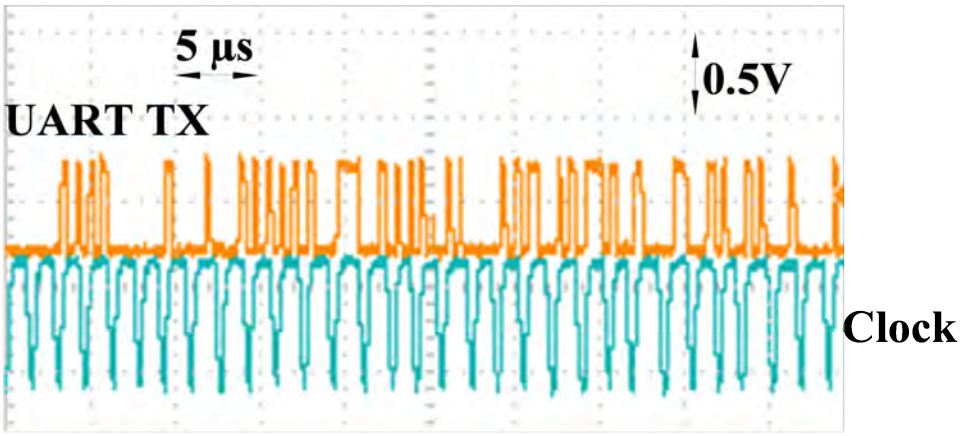


Figure 5.6: Measured UART functional waveforms [10]

debug interface transmitted by the processor and captured on an oscilloscope. Figure 5.7 shows the energy-delay trends of the MSP430 processor for the three programs discussed above. The instructions for the three programs were loaded on to the on-chip register-based

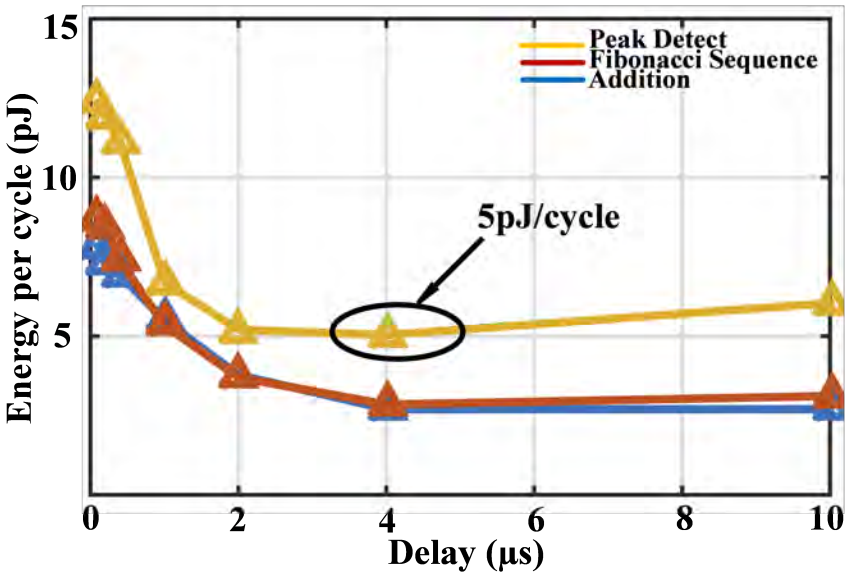


Figure 5.7: Measured Energy vs. Delay trends of the processor [10]

PMEM and the processor was configured to fetch instructions and data from the on-chip PMEM and DMEM respectively. For the peak detection implementation, the processor consumes 5pJ per cycle at 0.4V and 250 kHz. If a higher performance is needed for overall ECG detection at the system level, the processor can operate at 1MHz at 0.6V, consuming

6.7pJ per cycle. Hence, if a higher performance is desired, by sacrificing 34% energy, 4X performance improvement can be achieved. Since the chip was fabricated in an FDSOI process, a back-gate bias ranging from -5V to 5V was applied to tune the V_{th} of the transistors to achieve optimum performance. Measured results show 55% reduction in V_{th} variation of the fabricated devices in the xLP FDSOI process as compared to a standard FDSOI process. Measured minimum energy across 8 functional dies show a $\frac{\sigma}{\mu}$ of 0.0405. Figure 5.8 shows the

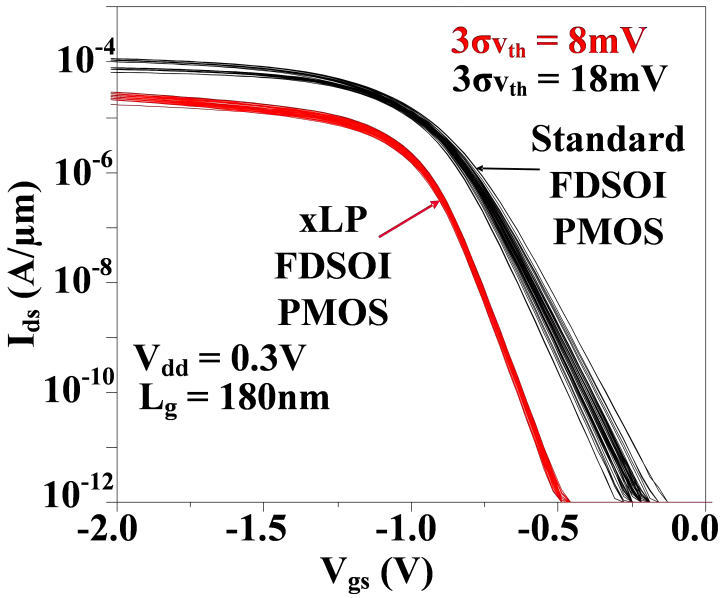
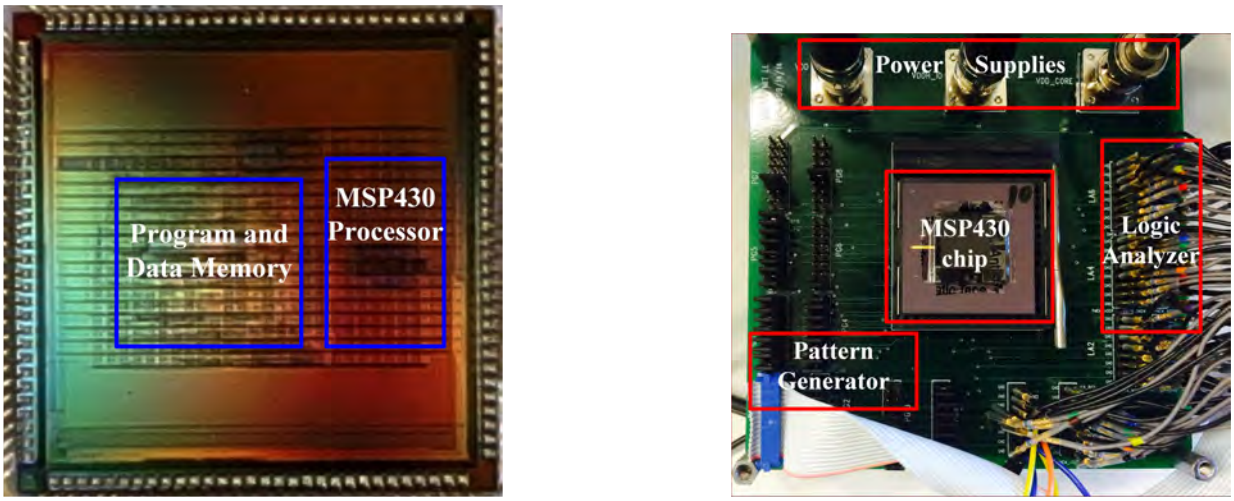


Figure 5.8: Measured V_{th} variation in xLP FDSOI and comparison with standard FDSOI process [10]

$I_{ds} - V_{gs}$ measurements of 46 PMOS transistors across two wafers. The 3σ variation in V_{th} was found to be 8mV for a device with channel length, L_g = 180nm and V_{ds} = 0.3V. The reduced variation in V_{th} was achieved due to reduced V_{th} sensitivity to silicon thickness. Absence of random dopant fluctuations and reduced channel length sensitivity to source drain anneal variations further minimize V_{th} variation. Table 5.1 compares the performance of the proposed implementation with state-of-the-art processors published in literature. This 16-bit MSP430 implementation in the xLP FDSOI process consumes 67% less energy as compared to [76]. The implementation in [66] consumes 6-10pJ/cycle at 0.5V for individual CPU instructions such as LOAD/STORE, AND, XOR etc. while the proposed implementation consumes

5pJ/cycle executing a peak detection algorithm. The implementation in [77] operates over a limited range of 0.32-0.48V while [55] and [18] have a limited range of operating frequencies and consumes higher energy per cycle as compared to the current implementation. Figure



(a) (b)

Figure 5.9: Chip Micrograph and measurement setup (a) Chip Micrograph(b) Measurement setup [10]

5.9a shows the chip micrograph and Figure 5.9b shows the measurement setup. The 16-bit MSP430 processor consumes an area of 0.44 mm^2. The total die size including the processor and register-based memories is 3.372mm X 3.372mm.

5.4 FIR filter design in 55nm ULL DDC technology

This work presents an Ultra-Low Leakage (ULL) 55nm Deeply Depleted Channel (DDC) process technology co-optimized with memory and logic circuit designs for low-power Internet of Everything (IoE) applications. The DDC ULL devices demonstrate a reliable sub-threshold operation by reducing threshold voltage (V_{th}) variation due to Random Dopant Fluctuation (RDF) by 67%. The optimized DDC process enables a higher degree of reverse body biasing (RBB) while controlling the junction current, resulting in ∼100X effective leakage reduction across supply voltages (VDDs). Circuit techniques such as sub-threshold operation and reverse body biasing (RBB) are co-designed with the technology to maximize the energy/power

Table 5.1: Comparison of xLP MSP430 with existing work

	[66]	[55]	[18]	[77]	[76]	**This Work[10]**
Technology	65nm	180nm	180nm	65nm	130nm	**90nm FDSOI**
Architecture	16-bit MSP430 compatible	ARM Cortex M0+	ARM Cortex M0	16-bit MSP430 compatible	16-bit MSP430 compatible	**16-bit MSP430 compatible**
Operating Voltage	0.3-0.6V	0.16-1.15V	0.6V	0.32-0.48V	0.55-1.2V	**0.38-0.9V**
Min. Energy	6-10pJ/cycle @0.5V	44.7pJ/inst @0.55V	17.2pJ/inst @0.26V	2.6pJ/cycle @0.375V executing FIR filtering	14.8pJ/cycle @0.6V	**5pJ/cycle @0.4V executing peak detection**
Operating Frequency	8.7kHz-1MHz	2Hz-15Hz	160-330kHz	25-71MHz	-	**100kHz-10MHz**
Area	$1.62mm^2$	$2.04mm^2$ (CPU+Mem)	$1.7mm^2$	$0.42mm^2$	$5.12mm^2$ (CPU+ Mem+Accl)	**0.44**mm^2

saving. A test chip implements a 16-bit, 32-tap FIR filter to showcase the effectiveness of the technology and RBB as design knob to minimize energy for IoE. The FIR filter consumes only 4.5pJ/cycle operating at 0.36V at 200 KHz.

5.4.1 DDC Technology

In the sub-threshold region, leakage energy often dominates the active energy. The total leakage current of a device consists of sub-threshold, gate, and junction leakage. Increasing the dosage of impurities in the channel raises V_{th} and lowers the sub-threshold current. Unlike dopant changes, an increase in the impurities makes RDF worse and increases junction leakage [78]. A DDC technology for 65nm [79][78] is designed to optimize the trade-off between V_{th} variation and sub-threshold leakage. This paper describes new ULL devices in a 55nm DDC technology that target total leakage current reduction with RBB. Once sub-threshold leakage is reduced sufficiently, gate leakage dominates the total leakage. The gate leakage strongly depends on the thickness of the gate dielectric (T_{OX}). However, thicker T_{OX} leads to a larger V_{th} variation and results in 1) higher RDF and 2) more V_{th} mismatch

between devices. However, with ULL DDC devices, the V_{th} degradation with a thicker gate dielectric is relaxed by 60% compared to the conventional device at the same gate dielectric thickness as shown in Figure 5.10. Figure 5.11 shows the TEM representation of a 55nm ULL

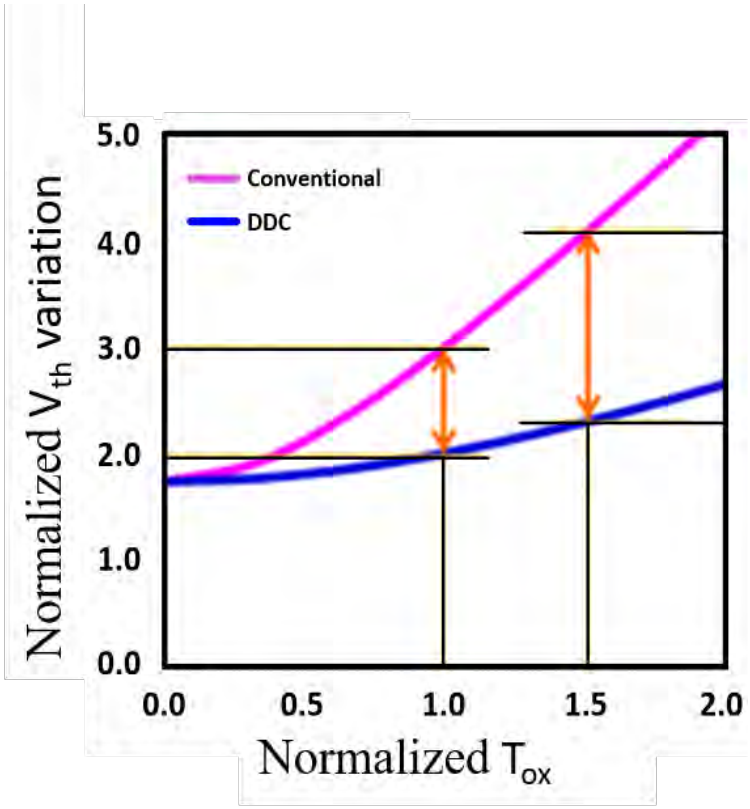


Figure 5.10: Impact of increase in Gate-Oxide (T_{OX}) on V_{th} variation [11]

device in DDC technology. The un-doped channel and highly doped screen layer reduce V_{th} variation in DDC [78]. The ULL device using DDC further reduces leakage using an optimal selection of channel lengths combined with body biasing. Figure 5.12 shows the measured I_D vs. V_{GS} curves including local and global variations. Here, DDC process matches PMOS and NMOS roll-off with an optimal selection of PMOS with Lightly Doped Drain (LDD). Higher local and global variation disturbs the circuit functionality in sub-threshold due to the exponential dependence of current on V_{th}. Figure 5.13 shows V_{th} roll-off for a ULL device in the DDC technology compared to conventional standard (SVT) and Low V_{th} (LVT) devices in a non-DDC technology. ULL DDC shows a strong control over V_{th} across a wide range of channel lengths. Reduced V_{th} variation enables further supply scaling with over-margined

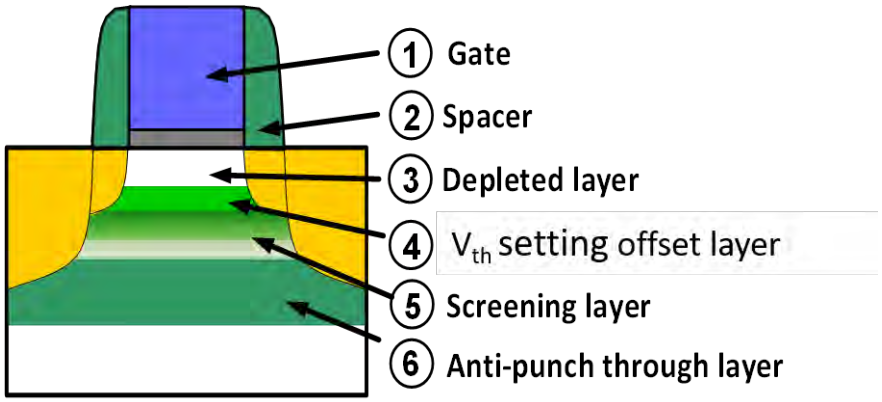


Figure 5.11: Structure representation of the DDC ULL device structure [11].

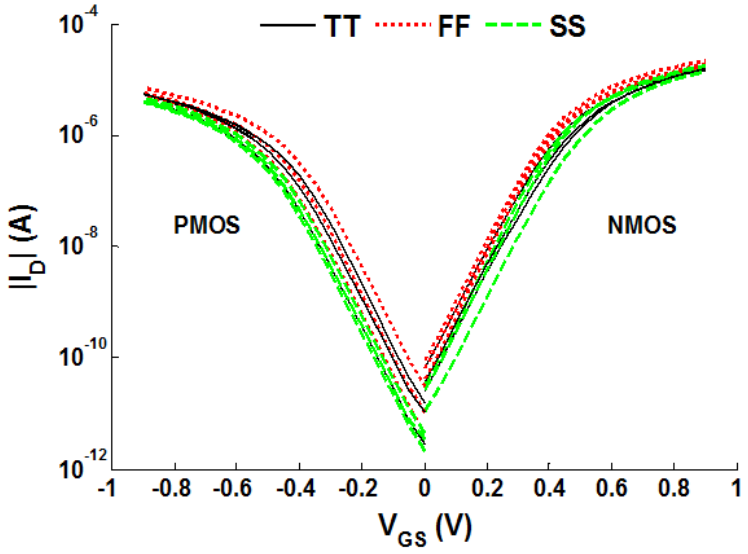


Figure 5.12: I_D vs. V_{GS} across multiple samples and process corners [11]

design optimization. ULL DCC is an attractive technology to address the two most pressing challenges for sub-μW systems: 1) reduced drive strength, and 2) lower yield due to V_{th} variation.

5.4.2 Leakage minimization using Reverse Body Biasing

The battery life in present state-of-the-art ULP applications depends on the total standby power of the system. Figure 5.14 shows various leakage components contributing to the total leakage of the device [80]. In Section 5.4.1, we discussed how the DDC technology minimizes

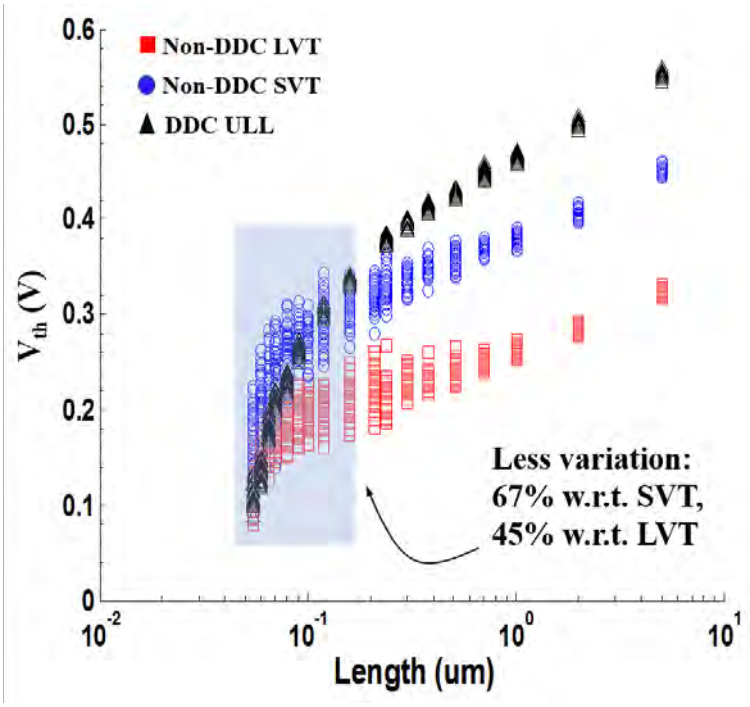


Figure 5.13: V_{th} roll-off comparison between DDC and non-DDC devices (W=1μm, V_{DS}=0.9V) [11].

the gate leakage (I_3) by optimal selection of t_{OX} while reducing the V_{th} variation (Figure 5.10). The Gate Induced Drain Leakage (GIDL) (I_4) increases total leakage at higher gate voltages and therefore has an insignificant contribution in sub-threshold ($V_{GS} \leq V_{th}$) [81]. In sub-threshold, where sub-threshold leakage (I_1) dominates the total leakage, controlling threshold voltage using body (called body-biasing) reduces total leakage current significantly. The triple well structure in DDC allows RBB to accentuate the inherent benefits of ULL devices for extra power savings at low VDD.

$$V_{th} = V_{th0} + \gamma(\sqrt{|V_{SB} + 2\phi_B|} - \sqrt{|2\phi_B|}) \tag{5.1}$$

$$I_{sub} = \frac{\mu C_{OX} W}{L}(\eta - 1)V_T^2 \exp[\frac{V_{GS} - V_{th}}{\eta V_T}](1 - \frac{-V_{DS}}{V_T}) \tag{5.2}$$

Where,

V_{th0}= threshold voltage when source is connected to the bulk ($V_{SB} = 0$)

ϕ_B = Fermi potential

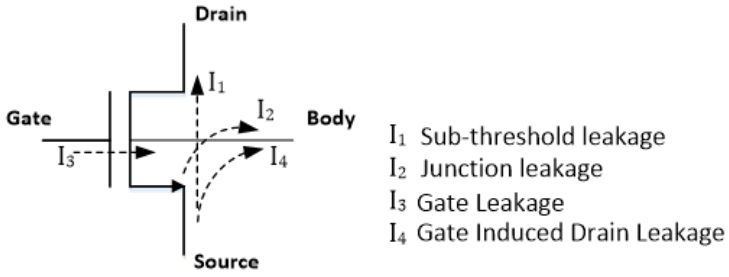


Figure 5.14: Major contributing leakage currents [11]

μ = mobility of carriers

C_{ox} = gate oxide capacitance per unit area

(W/L) = device aspect ratio

η = capacitive coupling between the gate and silicon surface

V_T = thermal voltage

As shown in Equation 5.1, the source-to-body biasing (V_{SB}) controls the threshold voltage (V_{th}) [82][83]. The device is reverse body biased (RBB) by applying a negative voltage to the bulk in the case of NMOS and applying > VDD voltage to the bulk of the PMOS to increase the V_{th}. Equations 5.1 and 5.2 represents how the change in V_{th} controls the sub-threshold current [80]. While RBB provides an effective knob to reduce sub-threshold leakage (Equation 5.2), it also reduces ON current and increases junction leakage current. Figure 5.15 shows ON current (I_D) degradation across V_{GS} with increasing degree of RBB. The I_D vs. V_{GS} trend indicates that there is insignificant degradation in I_D at higher V_{GS} due to the RBB. While at lower V_{GS} (< 0.5), I_D degradation remains much lower compared to other technologies [84]. The higher degree of RBB also increases the junction leakage current (I_2) across reverse-biased substrate-to-source/drain junction of the device. However, the lightly doped n and p regions in DDC ULL devices help to attenuate Band-to-Band Tunneling (BTBT) dominating the p-n junction leakage. Figure 5.16 shows measured sub-threshold leakage and junction leakage at varying degrees of RBB and a corresponding increase in the junction current (I_{junc}) and decrease in sub-threshold leakage (I_{sub}). Across VDD, varying degrees of RBB results in

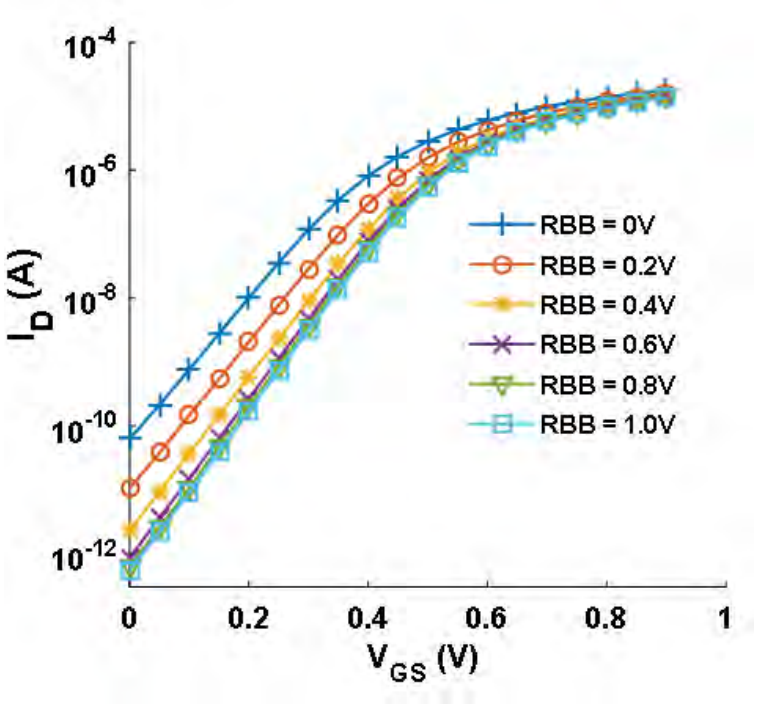


Figure 5.15: I_{ON} degradation with increasing degree of RBB [11]

~100X total leakage reduction (I_{sub} - I_{junc}).

5.4.3 Measurement results of the FIR filter

To demonstrate energy-efficient DSP for IoT applications, a 16-bit, 32-tap FIR filter in the custom 55nm DDC technology was implemented. The filter has a word size of 16-bits and the total buffer size is 512 words. The FIR filter is implemented using custom standard cells characterized at 0.5V and synthesized using auto place and route (APR) tools. Timing closure was achieved at 0.5V and 1MHz. To achieve energy-efficient operation, adaptive body-biasing techniques can be applied to both PMOS and NMOS devices. Figure 5.17 shows that the minimum energy per cycle for the FIR filter (at 0.36V) is ~5X lower than [85], and RBB of 0.25V gives 39.4% more reduction due to lower leakage energy. Figure 5.18 shows a die photo of the fabricated chip in DDC technology

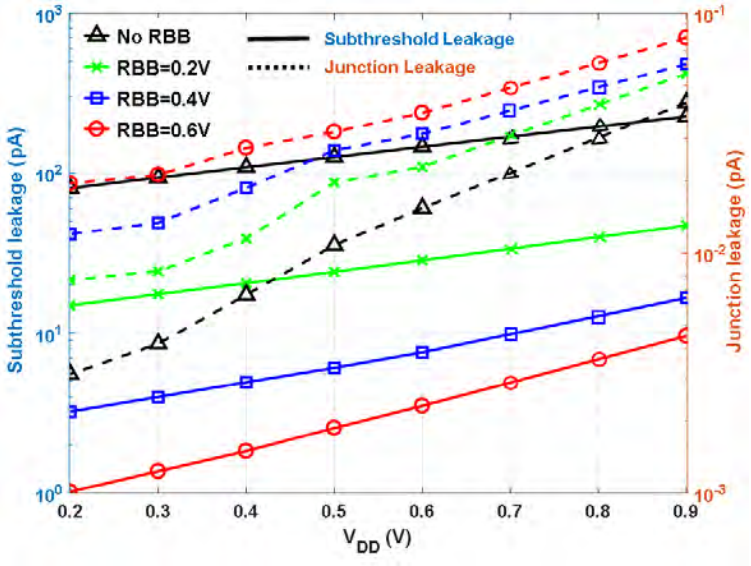


Figure 5.16: Effective leakage reduction using RBB – Increasing degree of RBB reduces sub-threshold leakage ∼100X while increases junction current increases by less than 10X across supply voltages [11]

5.5 Ultra low power detection circuits in wakeup receiver systems

Event driven wake-up receivers form an integral component in emerging remote IoE sensing applications. This has become a major driving force for researchers to develop sensor nodes operating under stringent power consumption limits in the order of several nano-Watts. The sensor can remain in an asleep yet aware state and switch operating modes upon receiving RF wake-up signals. Owing to the low power consumption, such sensors require very little maintenance over several years [86]. However, false wake-up events can increase the energy overhead of the node due to temporary changes in the operating state. This indicates that very low false alarm rates are required as these events carry a significant energy penalty associated with them. For event driven wake-up receiver applications, the information transmitted to the receiver can be viewed as a single bit signal that informs the node to wake-up, with data rates ranging from once a minute to once per year depending on application and network activity factor, indicating that total dc power consumption and RF power sensitivity are the

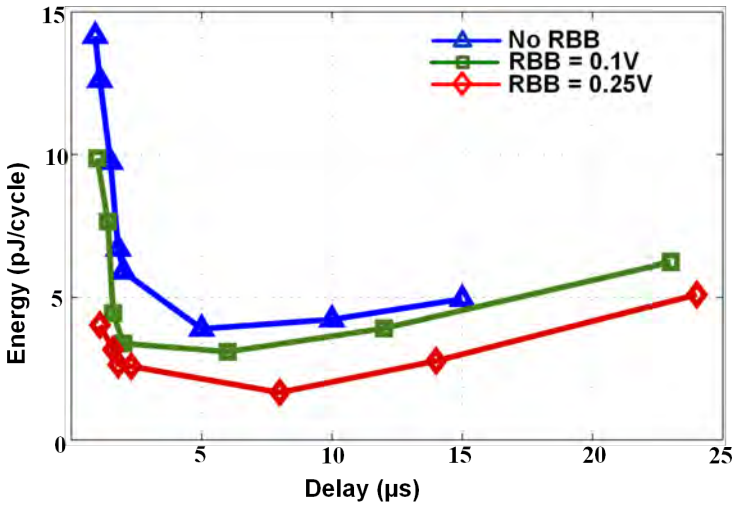


Figure 5.17: Effectiveness of RBB on active energy: 16-bit FIR [11]

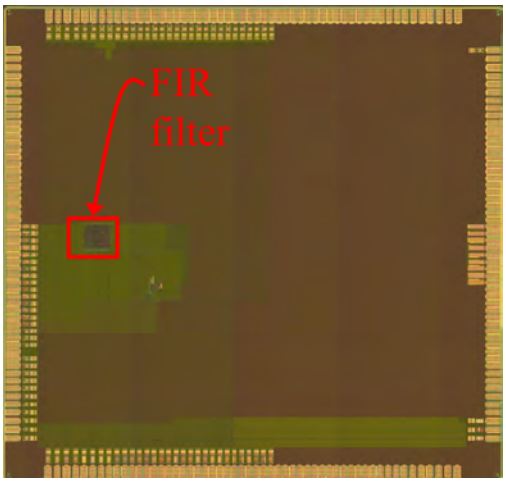


Figure 5.18: Fabricated chip with a 16-bit FIR block [11]

critical design requirements. In this section, different ULP comparator architectures used in such systems are discussed. An ULP clock generator used for sampling and processing is discussed and finally a baseband correlator architecture is presented.

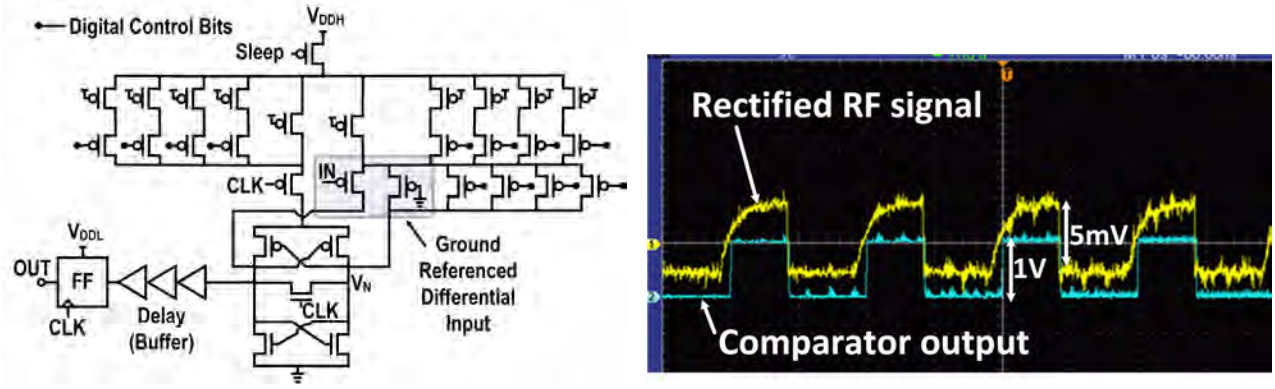
5.5.1 Ultra low power comparators

In a wakeup-receiver, a decision circuit is required to sample the incoming RF signal as a binary 1 or 0. In the absence of an RF signal or in the presence of interferer signals , the threshold of the decision circuit should be adaptive to reduce the overall bit-error rate. A

comparator acts as a 1-bit analog to digital converter in such systems. The threshold of the comparator needs to be programmable. One such algorithm which dynamically sets the threshold of the comparator is discussed in this section. The minimum threshold and the step size determines the overall sensitivity of the receiver. The power consumption of the comparator and other baseband circuits should be minimized to enhance the overall lifetime of the system. Two clocked comparator architectures and one continuous time comparator used in the context of wakeup receivers are discussed.

ULP Clocked comparators

The ground referenced comparator architecture shown in Figure 5.19a was optimized for both low-power operation and low decision threshold-voltage. This comparator has been



(a) (b)

Figure 5.19: (a)Schematic of the ground referenced comparator with controllable decision threshold-voltage, capable of detecting sub-mV baseband signals [12](b) Measured functional waveforms of the comparator subject to a 5mV input RF signal

adapted from [67] and consists of a pre-amplifier with one of the inputs referenced to ground and the other input (IN) driven by the rectifier output. A bias current generated by a 4-bit binary-weighted programmable current DAC sets the gain of the pre-amplifier. The clocked stage of the comparator incorporates regenerative feedback. The pre-amplifier amplifies the input when the clock is low (clk=0) and the compared result is latched at the next rising edge of the clock. The input threshold can be tuned by adjusting the input offset using the

4 bits, offset1-4 from a minimum of 2mV to a maximum of 32mV with a minimum step size of 700μV. Measurement results (Figure 5.19b) show that when a 5mV signal is applied at the input of the comparator being clocked at 50kHz, the comparator changes state at the next rising edge of the clock signal. The clock signal can be obtained from the on-chip oscillator. This comparator operates at a supply of 1-1.2V and consumes an average power of 4.8nW at 1V. To summarize, this comparator utilizes current reuse through its pre-amplifier into a latch which provides regenerative feedback. The decision voltage of the comparator is determined by a designed mismatch creating an offset voltage between the two legs of the differential amplifier, where the non-signal leg has a digitally controllable width allowing for decision threshold voltage control and compensation. The output of this stage is amplified further and fed into a latch which can then be processed by a digital correlator or used as a wake-up signal.

In order to improve the sensitivity to <-70dBm for a given RF front-end architecture, it is important to detect signal levels below 2mV. The comparator described in Figure 5.19a has a major limitation that it can only trip when the signal level is greater than atleast 2mV. Also to reduce offset errors due to process, voltage and temperature induced variation as well as for an improved response to higher power interferer signals, it is important that the comparator should have a wider range (>30mV) of programmable thresholds with a step size limited to <500μVs. Moreover, clock feedthrough and kickback noise limits the performance of the detector when the output impedance of the RF front-end circuits driving the comparator exceeds 100MΩs which is common in ULP receiver front-ends.

Figure 5.20 shows the schematic of an improved clocked comparator circuit. The clocked comparators sampler consists of a pre-amplifier with a p-channel Field Effect Transistor (PFET) input stage with one input referenced to ground and the other input driven by the output of the RF front-end. The cross-coupled inverter pair provides regenerative feedback. When CLK=0, the comparator is reset. When CLK=1, the comparator enters into evaluation mode where it samples the incoming signal which gets latched during the rising edge of

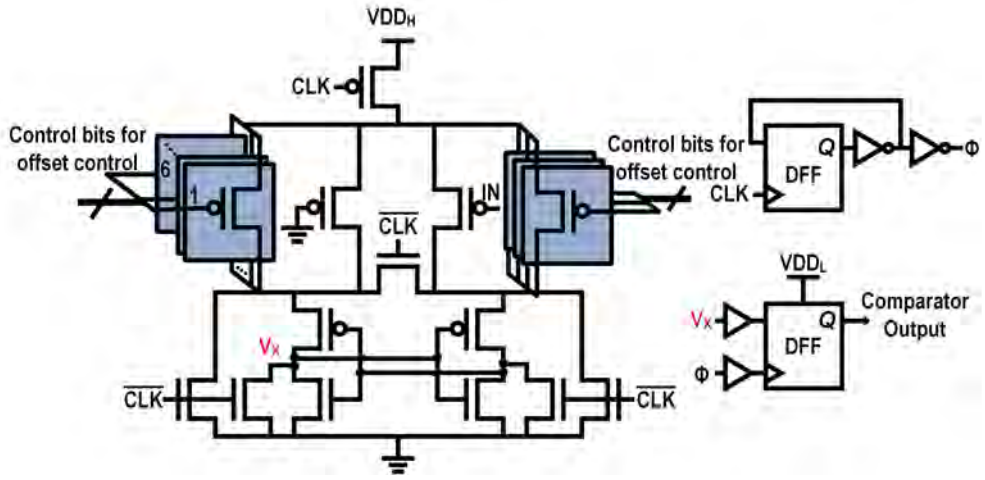


Figure 5.20: Improved ground-referenced clocked comparator with a lower minimum trip voltage and wider range of configurable comparator offsets [13]

ϕ. The comparator threshold is controlled through six-bits of fine-grained binary-weighted control bits, which are set by the automatic offset control loop with minimum step size of ∼280 μV. Three bits of coarse-grained digital control set the range of the comparator threshold. For instance, with a coarse setting of 000, the simulated comparator threshold ranges from -6 mV to 35 mV. The circuit consumes a total DC power of 1.7nW @ VDD_H = 1V with a clock frequency of 1kHz, provided by an on-chip oscillator. The latch operates at a minimum supply voltage, VDD_L = 0.5V and enables the comparator to interface with the digital backend.

Low voltage ULP Continuous time comparator

In most self-powered systems catering to IoT applications, low voltage operation is essential for enhancing the overall lifetime of the system. In addition, if the entire system operates from a single power source i.e. a single voltage rail, power loss at the interface (e.g. due to level conversion) can be eliminated. The ground-referenced clocked comparator described in Figure 5.20 requires two voltage rails: 1V for the sampler and 0.5V for the latch interface. Power overhead due to level conversion can be as high as 500pW accounting for nearly 33% of the total power budget of the comparator. As discussed in earlier sections that for low

power and energy efficient operation, the digital processing circuits are generally operated in the subthreshold region with supply voltages as low as 0.5V. If the comparator can operate at voltage levels as low as 0.5V, issues such as power overhead due to level conversion and the need for extra voltage rails can be resolved.

The response time of ULP, low sensitivity wakeup receivers are dictated by the RF front-end which can range in the order of a few milliseconds. Hence, the conversion speed is not critical as long as it is significantly lower than the charge time of the envelope detector in the RF-front end. Thus by trading off bandwidth for a lower power consumption, a continuous time, analog comparator biased in weak inversion can be a potential candidate for the comparator architecture. Apart from benefits in power and low voltage operation, a continuous time comparator provides better immunity against kickback noise as compared to a clocked comparator since the high impedance input to the comparator is isolated from the clock signal.

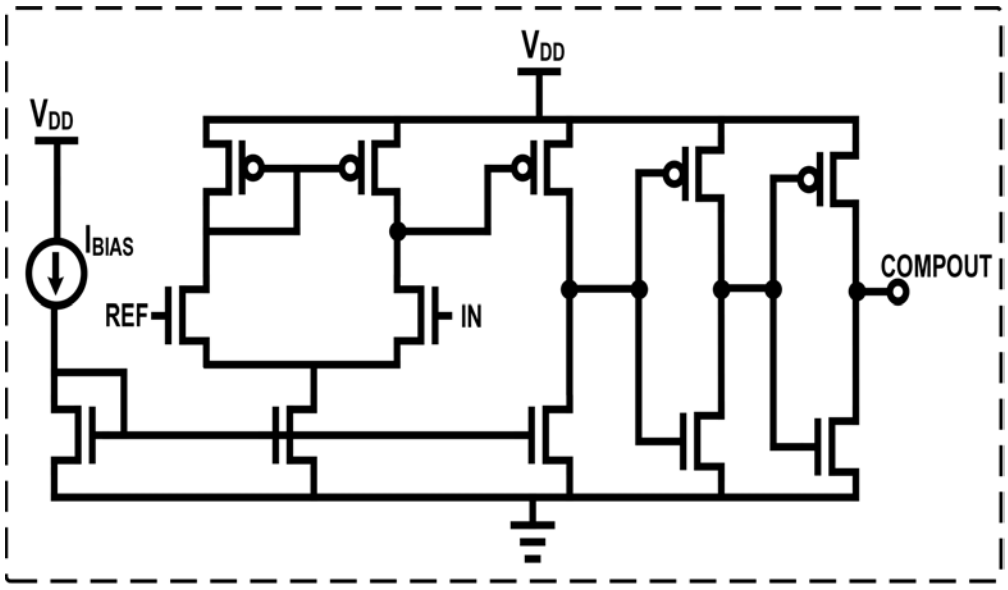


Figure 5.21: Continuous time comparator operational from 0.5V

Figure 5.21 describes the circuit schematic of the low voltage analog comparator. The two-stage architecture consists of an n-channel Field Effect Transistor (NFET) input differential

amplifier with a PFET current mirror load followed by a PFET common-source amplification stage. An external current source, I_{BIAS} can be used to provide tail current to the differential amplifier and voltage bias to the active load of the common-source stage. The circuit is designed for varying I_{BIAS} ranging from 200pA to 1.5nA. The input terminal, IN of the differential pair is driven by the RF signal while the input terminal, REF is driven by a reference signal provided by the RF front end. The DC input common mode range can vary from 35% to 65% of the supply voltage, V_{DD}. Drivers following the common-source stage enable a rail-to-rail swing at the output. Simulation results show a power consumption of 1.4nW operating at $V_{DD} = 0.5$V with $I_{BIAS} = 500$pA. Similar to the clocked comparator described in Figure 5.20, the continuous time comparator consists of programmable offset bits, supporting a wide range of trip voltages ranging from -10mV to 20mV with a step size of $\sim 300\mu$V

Controlling the comparator threshold for optimal receiver performance

For optimal detection in presence of on-off-keyed (OOK) RF interferer signals and to ensure self-calibration to overcome PVT variation, an offset controller algorithm is required which sets the decision threshold of the comparator automatically to achieve the highest sensitivity achievable at a given false alarm rate. One significant challenge for event driven wakeup receivers is that the entirety of the offset control must be accomplished in the absence of an RF signal. For receiver power levels below 10nW, an on-chip RF calibration source is not feasible, so the offset of the comparator must be set from information available in the RF off state. The compensation loop, shown in Figure 5.22, sets the comparator (described in Figure 5.20) offset to a level that provides a desired false positive rate for a trade-off between low false alarm rate and high sensitivity. In this work, the false positive rate is set to be 1.5% to achieve a false wakeup event rate of <1/hr The algorithm consists of two separate programmable thresholds (THR_Z and THR_O) which sets the rate of incrementing or decrementing the comparator threshold based on whether the sampled signal is evaluated

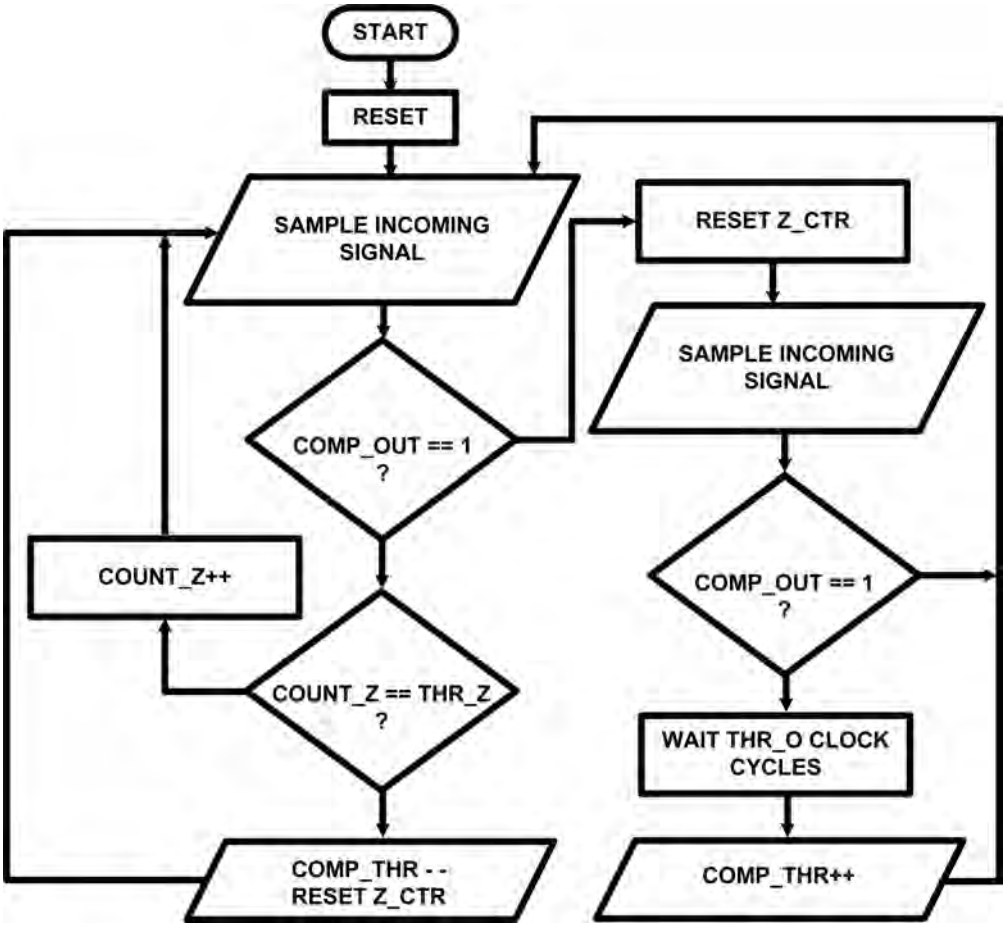


Figure 5.22: Flowchart showing the offset control algroithm [13]

to be a binary 1 or a 0. The algorithm is implemented in verilog and the synthesized logic consists of custom standard cells characterized at 0.5V. Operating at 0.5V, the controller consumes 1nW of DC power. Figure 5.23 describes the measured operation of the offset control algorithm. After coming out of reset, the controller sets the comparator threshold bits so that the comparator has the least offset, resulting in majority 1's being detected by the comparator. The controller waits THR_O clock cycles before incrementing the comparator threshold till the comparator starts detecting majority 0's. While waiting for THR_Z clock cycles (after which the controller starts decrementing the threshold), the wake-up sequence is detected. Then in presence of interferers, the controller further raises the comparator threshold. When a higher power (-72dBm) sequence is sent by the transmitter , the receiver still responds and issues a wakeup even in presence of interferers.

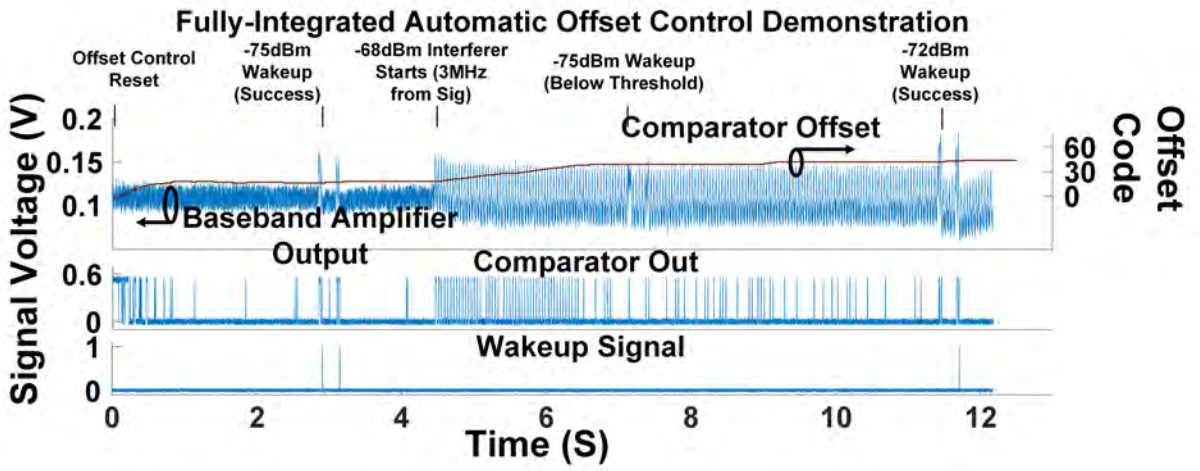


Figure 5.23: Demonstration of receiver with automatic offset control in the presence of non-constant envelope interferers [13]

5.5.2 Ultra low power clock generator

The system clock was implemented using a five-stage current-starved ring oscillator as shown in Figure 5.24. Current starving was achieved by using two voltage bias signals, VBN and VBP which set the frequency of oscillation. VBN and VBP were generated on board using a giga ohm resistive divider that consumes negligible power. The oscillator is operational from 0.5V and generates two non overlapping clock signals, CLK and CLKB . The oscillator can

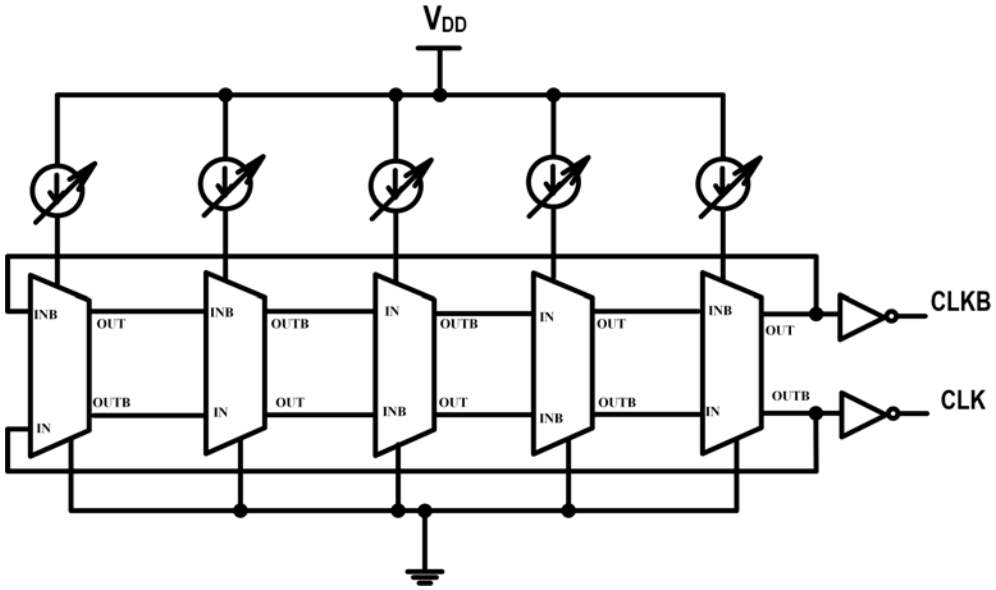


Figure 5.24: Current starved ring oscillator circuit [12]

cover a frequency range from 250Hz to 110kHz operating at V_{DD} = 1V. Utilizing a higher clock rate can reduce the total transmitted energy required for a wake-up, but would increase the clock dc power consumption and degrade the power sensitivity if the detector is not able to fully charge. Figure 5.25 shows the measured performance of the current starved oscillator operating at V_{DD} = 1V. Power measurements are recorded by sweeping VBN= 0.1V, VBP = 0.9V to VBN=0.9V, VBP = 0.1V

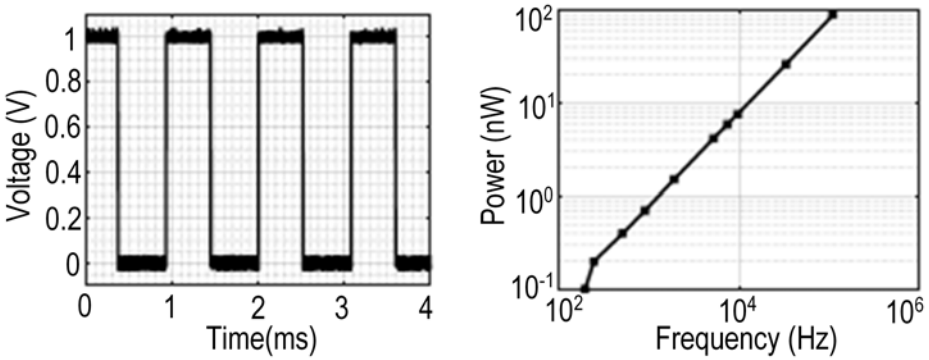
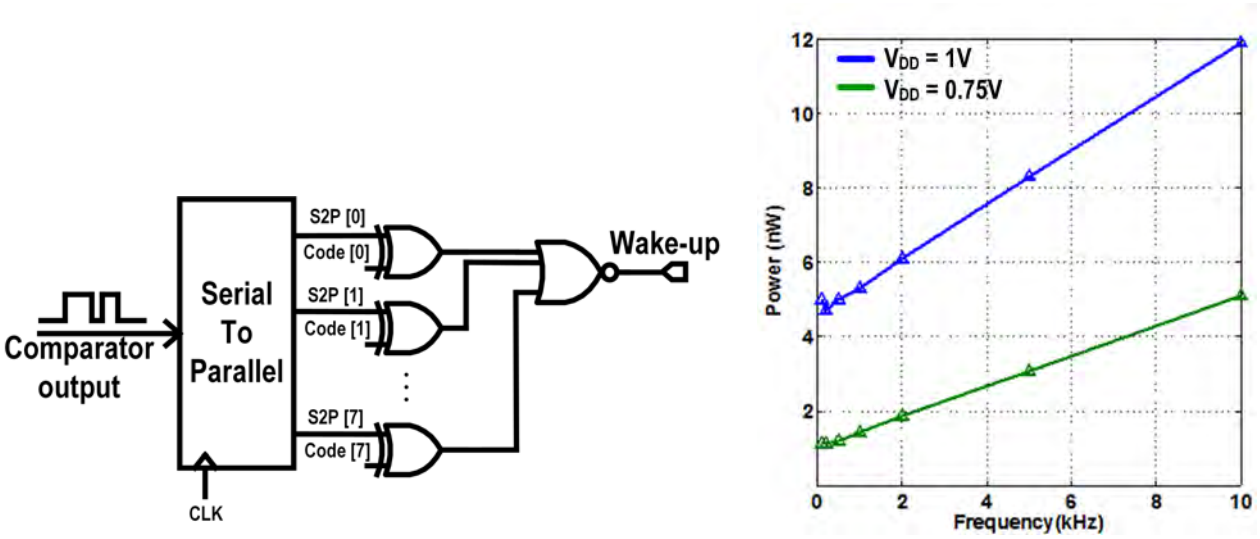


Figure 5.25: Measured performance of the oscillator [12]

5.5.3 Ultra low power baseband correlator

In order to detect a wakeup event, an 8-bit shift register XOR-based correlator with programmable reference code is implemented with sub-threshold logic to minimize dc power (Figure 5.26a). The wakeup signal is two back-to-back 8-bit OOK codes separated by a half clock cycle delay to account for possible phase mismatch between the transmitter and receiver. Figure 5.26b shows the measured power vs. frequency trends of the correlator for two different supply voltages (V_{DD}) The on-chip clock consists of a five-stage current starved ring-oscillator architecture described in Section 5.5.2. Figure 5.27 demonstrates the functionality of the correlator in presence of interferer signals. When the clocked comparator (Figure 5.19a) samples the phase shifted OOK signal, the correlator establishes a match with the pre-programmed reference code to issue a wakeup signal in presence of interferers.



(a) (b)

Figure 5.26: (a)Structure of the digital correlator (b) Measured power vs. operating frequency of the digital correlator

5.5.4 A -76dBm, 7.4 nW Wakeup Receiver for Event Driven Sensing Applications

In this section, the system level performance of a wakeup receiver is described. Figure 5.28 describes the overall architecture of the wakeup receiver. The tapped capacitor matching network, envelope detector and the baseband amplifier constitute the RF front-end. The clocked comparator , offset controller algorithm and the oscillator designs are described in Figure 5.20, Figure 5.22 and Figure 5.24 respectively. The correlator described in Section 5.5.3 can be used for baseband processing.

The system achieves -76dBm sensitivity in the 151.8 MHz MURS band and -71dBm sensitivity in the 433 MHz ISM band while consuming 7.4nW dc power (Figure 5.29). Wakeup sensitivity of -76 dBm, with 10^{-3} probability of missed detection and false wakeup rate <1hr is achieved using the full wakeup code including the correlator with no synchronization and a symbol bit rate of 0.2 kbps (Figure 5.29). The offset word is fixed to ensure constant voltage threshold throughout this measurement. Rejection of interferers is observed with -76dBm sensitivity for 10^{-3} missed detection rate measured for -46dBm (-30dB carrier to interferer

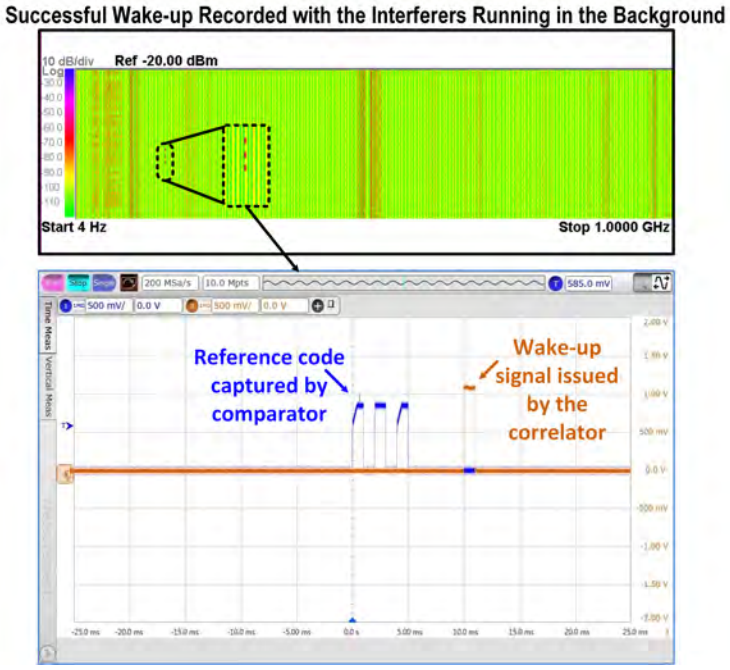


Figure 5.27: Performance of the shift register based correlator in presence of interferer signals

ratio (CIR) constant envelope interference with a 3 MHz offset from the signal. An example of the system robustness to non-constant envelope interferers with automatic offset control enabled is shown in Figure 5.23. A successful -75dBm wakeup signal is observed in a quiet environment. After a -68dBm 0.1 kbps OOK signal 3 MHz away briefly jams the radio, the offset control automatically raises the threshold. Rather than being unusable, the receiver remains functional at a lower sensitivity, as the final -72dBm wakeup signal shows. The DC power of the system is 7.4nW and its performance is compared to state-of-the-art WuRxs in Figure 5.30, showing 7dB improvement over prior sub-10nW wakeup radios. Figure 5.31 shows die and PCB photos of the system

5.6 List of Contributions

- Explored the benefits of technology to achieve low-power and/or energy efficient operation in digital circuits. An MSP430 processor was implemented in an FDSOI technology optimized for subthreshold operation. The processor consumes 67% less energy as

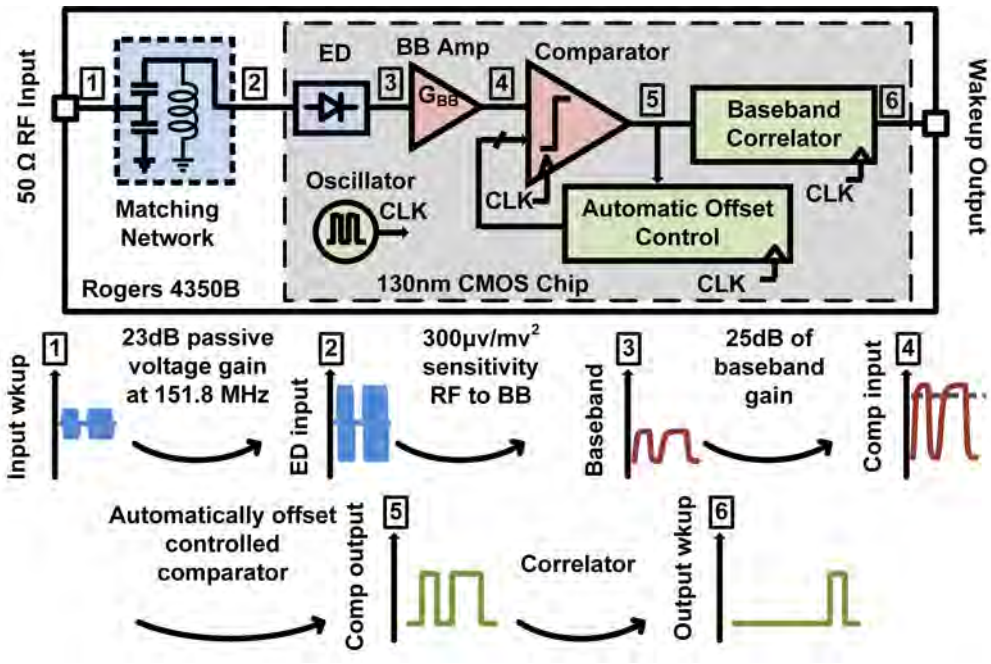


Figure 5.28: System architecture of the wakeup receiver showing waveforms from RF input through digital wakeup output [13]

compared to [76]. An FIR filter was implemented in DDC technology optimized for low-leakage. The minimum energy per cycle for the filter is ∼5X lower than [87].

- Introduced several low-power analog/digital and other mixed signal circuit components in context of a wakeup-receiver platform.

  - Introduced several low-power comparator architectures in context of a wake-up receiver platform. The lowest power clocked comparator presented in this work provides a ∼15X improvement in power consumption as reported in [88] and a ∼4X improvement as compared to [68].

    * While a low-input offset or threshold is desired for achieving high-sensitivity, a programmable control (on the comparator offset) is necessary for interferer rejection as well as process, voltage and temperature variation. Introduced a novel, low-power offset cancellation algorithm using digital logic for interferer rejection and allowing receiver functionality in presence of interferers.

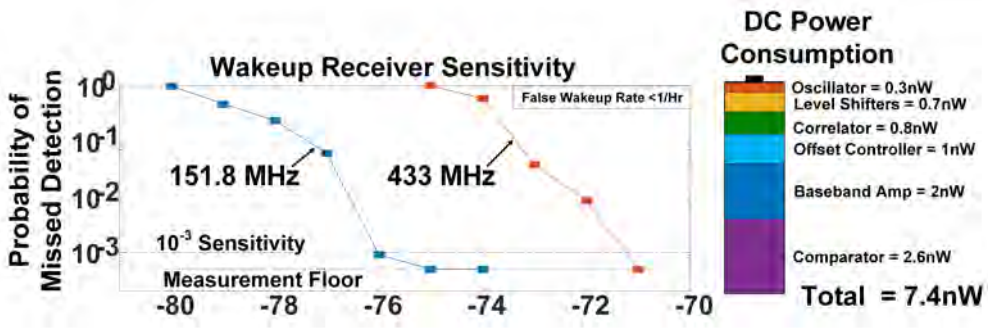


Figure 5.29: System-level measurements of sensitivity and dc power consumption of the wakeup receiver [13]

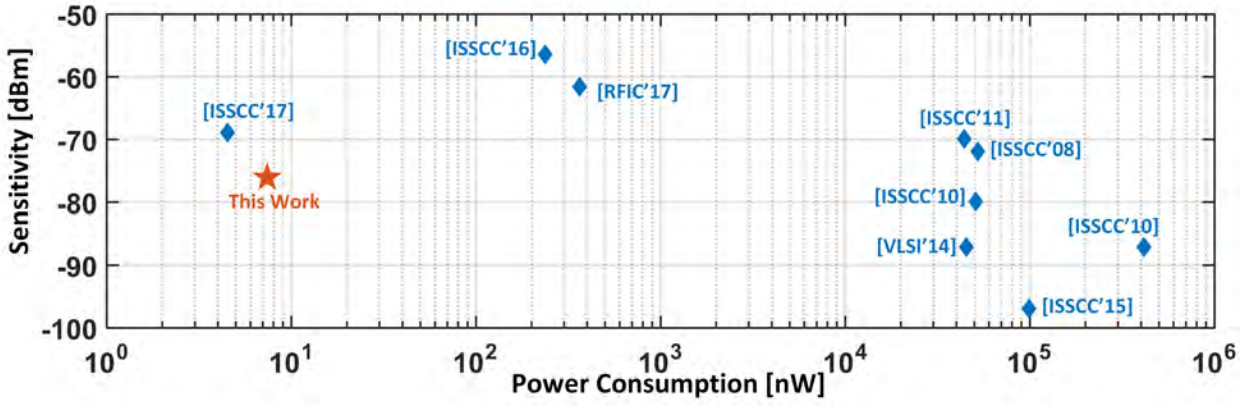


Figure 5.30: Comparison of the wakeup radio system with prior work [13]

  * In clocked comparators, kickback noise was found to be a major limiting factor to achieve high sensitivity, when interfacing with a high output impedance RF front-end. A low-voltage, low -power continuous time comparator was introduced to resolve kickback noise.

- Designed low-power, voltage controlled oscillator operational from a low supply voltage. Used extensively to provide clock signals to comparators and digital circuit implementations in the wakeup-receiver

- Designed a low-power baseband correlator for a wakeup-receiver using shift registers and digital logic. Power consumption was found to scale linearly with the number of correlator bits hence an 8-bit architecture was chosen for a given power budget of 10nW and 1V operation.

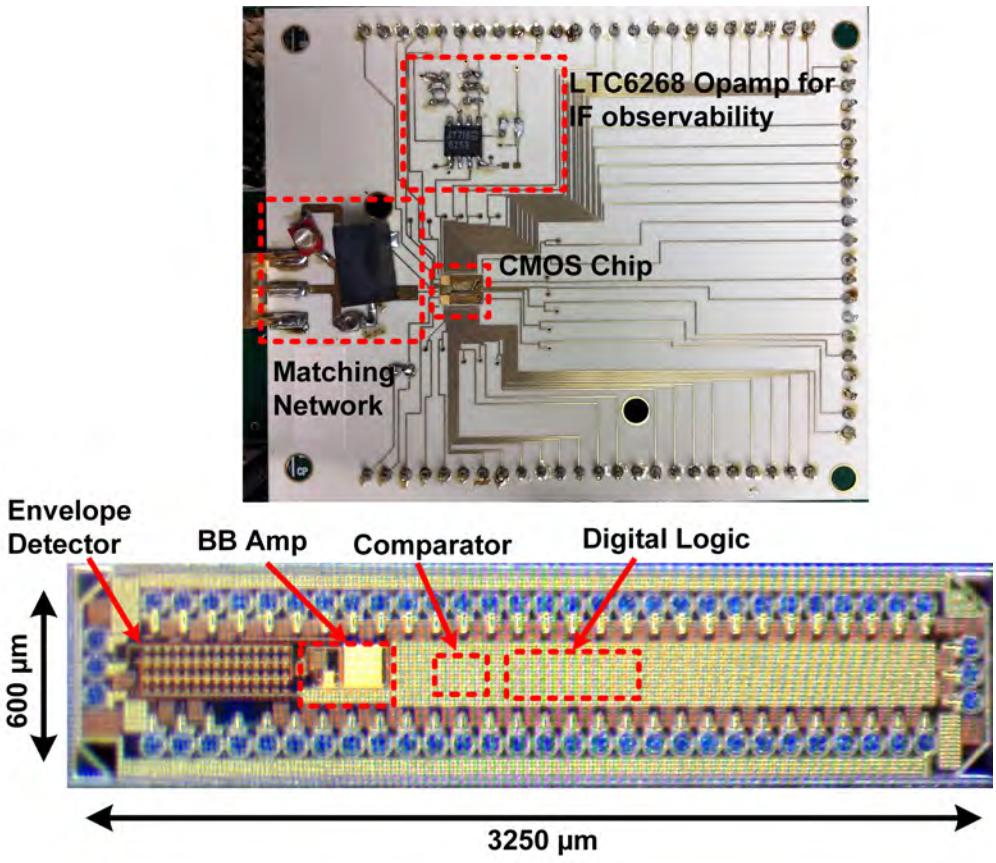


Figure 5.31: Die and PCB photos of the wakeup receiver [13]

5.7 Conclusion

In this chapter, the benefits of technology and circuit co-design are explored in the context of ULP systems consuming power in the range of tens of nW to a few μWs. This chapter presents an implementation of a 16-bit MSP430 processor in a custom extremely low power (xLP) 90nm FDSOI process catering to battery-less wireless sensor nodes. The processor consumes 1.3μW operating at 0.4V while executing a peak detection algorithm at 250 kHz and can be used in biomedical, and other applications related to the IoT. Techniques such as RBB were used in a 55nm DDC process to improve the energy efficiency of FIR filters commonly used in digital accelerators and low-power DSP applications. This chapter also discussed several ULP implementations of circuit components used in an "always-on" system such as a wakeup receiver. Potential candidates for comparators were explored and design-space

trade-offs between power consumption and conversions speeds were discussed. A low-power offset control scheme was presented to ensure low sensitivity and functionality in presence of interferer signals. The design of a shift register XOR-based correlator and a five-stage, dual phase current-starved oscillator circuit is presented. A system architecture of a 7.4nW wakeup-receiver with a -76dBm sensitivity is presented. To enhance the overall lifetime of the system, this chapter focuses on techniques to lower the standby power consumption of digital processors, accelerators as well as the quiescent power of mixed signal components such as comparators and oscillators. The need to lower the power consumption overhead of such circuit blocks is emphasized in addition to enhancing the power conversion efficiency of power delivery circuits such as regulators and energy harvesters.

Chapter 6

Conclusion and future research directions

The emerging applications catering to the IoT and advancements in sensing technologies have resulted in an increased demand for ULP systems. A wide range of applications have emerged where such systems can be useful, such as health-care (e.g. ECG, EEG), industrial, infrastructure monitoring, remote surveillance etc. Energy autonomy and self-powered operation is a necessity to enhance the life-span of such sensing systems and reduce the costs associated with battery replacement in scenarios where large-scale interconnected sensor networks need to be deployed. Niche applications such as Body-sensor networks and implantables for healthcare restrict the overall volume of the sensing system. Recent works in literature have focused on solving these problems of energy-autonomy and power-delivery within a constrained power and area budget. However, most of these research efforts have only yielded point solutions, which restrict the usage of such systems to a narrow application space. Hence, to improve the energy autonomy and the overall life-span of these emerging, diverse sensing systems, a more comprehensive system-level approach is necessary.

This dissertation addresses the open problems related to power management in wireless sensors in the following ways: energy harvesting techniques to harvest from indoor solar/TEGs using

a single inductor or a switched-capacitor based harvester for volume-restricted applications, low-quiescent power voltage regulators which support the electrical requirements of various components, reduced static power overhead and enhanced energy-efficiency of different analog/mixed-signal/digital components which need to be supported by the regulators.

6.1 Summary of Contributions

6.1.1 Energy harvesting from ambient DC sources

- Evaluated the different design knobs for single-inductor boost converter operating in DCM. Found that an adaptive peak inductor current control is necessary for achieving optimal optimal power efficiency especially with varying input(10mV-1V) and output voltages(maximum 3V), varying power levels (500nW-50μW), which are common in TEG/solar harvesters with changing environmental conditions and load current transients, occurring during system operation.

- Introduced a low-power, fractional open-circuit voltage MPPT scheme. Programmable sampling rate(0.1Hz-1Hz) of the Maximum Power Point (MPP) of the transducer is necessary depending on the application (e.g. motion) and leakage of the storage node, holding the MPP.

- Introduced an adaptive peak inductor current control circuit for achieving high power efficiency(90% at 1V; 48% at 30mV input) with varying input voltage from the harvester and the voltage on the storage node. This is the first ever implementation of an adaptive peak inductor current control circuit which can support both re-chargeable batteries or supercapacitors for storage and TEG/PV for harvesting.

- Presented a low-power, all digital zero crossing detection circuit. The digital implementation consumes an average power of 63nW achieving a ∼150X improvement over [40] and a ∼5X improvement over [30].

- Introduced a low-voltage, fully-integrated cold-start circuit. The minimum cold-start voltage is reduced by 50% as compared to [15] which guarantees charging at correspondingly lower energy levels in poor harvesting conditions (e.g. low light, less ΔT).

- Introduced a performance modeling framework for evaluating boost converter/energy harvester architectures with different controller algorithms. The design methodology was shown for a single-inductor boost converter with PFM control and good correlation ($<$ 5% error) with measured results was achieved.

6.1.2 Ultra-low I_Q voltage regulation

- Performed design validation of a Single Inductor Multiple Output(SIMO) DC-DC converter. The buck-boost converter is operational from a low voltage i.e. 0.7V and achieves a peak efficiency of 95% at 4mW load power. Compared to the state-of-the art, this work enables <1V operation for switching converters supporting a similar load power range. Although the SIMO architecture was operational from a low voltage, it was found that its quiescent power consumption ranged in the order of a few μW making it sub-optimal for wearable applications (e.g. BSN). A common powertrain for the different regulated rails resulted in cross-regulation issues.

- Introduced a fully-integrated regulator architecture which provided three separate rails with independent powertrain and control for different categories of load (e.g. analog, digital, external sensors). The end-to-end power efficiency of the regulator and harvester was measured to be 71.1% at 1μW load which provides >30% improvement over [23].

- Introduced a novel gate-current based reference generator operational from a low voltage and consuming low power (hundreds of pW to a few nW depending on the voltage on the storage node). The reference generator presented in this work achieves an ~80X reduction in power vs. [43] and improves PSR with -76dB at 100Hz vs. [57]. Reducing

the minimum operational voltage of the reference generator by 50% as compared to traditional Bandgap references [20] enables converter control to be functional at lower energy levels (quadratic improvement) on the storage node contributing to equivalent improvement in system lifetime, in the absence of harvesting.

6.1.3 Power supply variation in ULP systems

- Analyzed the impacts of power supply variation in latch and register based topologies using energy-efficiency as a metric. Latch-based designs were found to be more resilient and 25-37% more energy efficient at low-voltages (< 0.6V) subject to a low-frequency(upto 1kHz) supply noise. At higher supply voltages (> 0.6V), active energy dominates. Hence, register-based architectures were found to be 60% more energy-efficient, due to greater switching capacitance associated with latch-based implementation.

- Introduced a low power, supply voltage droop measurement circuit, implemented using all-digital logic. The circuit achieves a ∼50X lower power consumption as compared to [59] and can be leveraged in low I_Q controller designs for regulators and power converters.

6.1.4 Ultra-low power load circuits and components

- Explored the benefits of technology to achieve low-power and/or energy efficient operation in digital circuits. An MSP430 processor was implemented in an FDSOI technology, optimized for subthreshold operation. The processor consumes 67% less energy as compared to [76]. An FIR filter was implemented in DDC technology optimized for low-leakage. The minimume energy per cycle for the filter is ∼5X lower than [87].

- Introduced several low-power analog/digital and other mixed signal circuit components in context of a wakeup-receiver platform.

- Introduced several low-power comparator architectures in context of a wake-up receiver platform. The lowest power clocked comparator presented in this work provides a ∼15X improvement in power consumption as reported in [88] and a ∼4X improvement as compared to [68].
  - While a low-input offset or threshold is desired for achieving high-sensitivity, a programmable control (on the comparator offset) is necessary for interferer rejection as well as process, voltage and temperature variation. Introduced a novel, low-power offset cancellation algorithm using digital logic for interferer rejection and allowing receiver functionality in presence of interferers.
  - In clocked comparators, kickback noise was found to be a major limiting factor to achieve high sensitivity, when interfacing with a high output impedance ($> 100M\Omega$) circuits, such as envelope detectors and RF front-end. A low-voltage(operational from 0.5V), low -power (1.7nW) continuous time comparator was introduced to resolve kickback noise.
- Designed low-power (300pW operating at 1V), voltage controlled oscillator operational from a low supply voltage (0.5V). Used extensively to provide clock signals(frequency range 250Hz to 110kHz at 1V supply) to comparators and digital circuit implementations in the wakeup-receiver.
- Designed a low-power baseband correlator for a wakeup-receiver using shift registers and digital logic. Power consumption was found to scale linearly with the number of correlator bits hence an 8-bit architecture was chosen for a power budget of 10nW, operating at 1V.

6.2 Open Problems and research directions

With increasing popularity and the number of new applications related to the IoT in recent years, power delivery has become an important design problem, both from a system design

as well as from an IC design perspective. This work has addressed many of the challenges related to power delivery and lifetime improvement of IoT devices and systems. However many important research problems remain to be solved.

As discussed in Chapter 2, the main challenge in self-powered devices is system operation, in the absence of energy harvesting or under poor harvesting conditions. One of the approaches could be the ability to harvest from more than one source simultaneously to store more usable energy. By evaluating the instantaneous power available from multiple sources, under any environmental condition, the highest power source can be used for harvesting. The interface will require a power monitor or a method to calculate instantaneous power. To design the power monitor, one approach could be to measure the ON-time (T_{HS}) of the High-Side(HS) switch of the boost converter at a given peak inductor current (I_{PEAK}). This time-domain estimation can serve as a proxy measurement of the instantaneous power available from the harvester. Another approach could be to incorporate time-multiplexing between different energy transducers and extracting energy from different sources within their respective time-slot. The length of the time-slot can vary based on the instantaneous power estimate.

Apart from DC sources such as TEGs or indoor PV cells, energy harvesting from AC sources can also be looked at to expand the number of possible sources. Piezo-electric, electromagnetic and near-field RF harvesting can be explored to extend this work.

The use of storage devices such as re-chargeable batteries or supercapacitors depend on the application. However, the behavior of such devices with varying temperature, voltage and the dependence of their storage capacity during charging or discharging is not well understood. Auxiliary circuits, such as fuel gauging and battery lifetime predictors need to be explored in the context of self-powered systems for reliable operation and further enhancement of the life-span of a sensor node.

This dissertation contributes to the development of a modular architecture for supply voltage regulation in the context of self-powered devices, subject to different electrical specifications of system components. However, further enhancements can be made, especially in scenarios

when a higher down-conversion ratio is desired. One approach could be an independent Power Management IC (PMIC) within the SiP platform consisting of the energy harvesting interface and a switching regulator. Each of the constituent ICs within the SiP can have its own independent LDO or regulator, responsible for supporting local load current transients and which can interface with the switching regulator/PMIC. Before actual circuit design, the powertrain and control mechanisms can be modeled using a framework similar to the version presented in chapter 2.

Chapter 4 discusses an ULP droop measurement circuit. One of the limitations of this work is the need for a clean, low-ripple voltage rail for calibration. Since, only a periodic calibration is necessary, techniques which use a high PSRR Bandgap Reference (BGR) can be used to avoid the need for a separate voltage rail. Power consumption can be lowered by duty-cycling the BGR.

Chapter 5 presents an always-ON, high sensitivity, low DC power wakeup receiver, used extensively in self-powered sensor nodes during wireless communication. Further improvements can be made to lower the temperature variation and drift of the oscillator. A temperature compensation loop can be designed to configure the bias voltages VBN and VBP which are currently set externally. Improvements can be made to the current offset compensation algorithm for faster convergence. Improvements can be made to the comparator architecture to lower the DC-Power/Bandwidth ratio. For reducing the impacts of kickback noise, which manifests itself at the RF front-end/comparator interface degrading sensitivity and performance, one important research question is whether to choose a low-output impedance buffer followed by a clocked-comparator architecture or whether to allocate the power consumed by the buffer to improve the bandwidth of a continuous-time comparator.

6.3 Conclusion and outlook

Recent advances in sensing technology, IC design and the internet of things have created a potentially huge market for ultra-low power sensors which are relevant in a variety of applications ranging from remote health-care, infrastructure, surveillance to environmental monitoring. Usually, in most applications, a large number of these low power sensor nodes must co-exist and communicate with each other, typically over a wireless link. To be cost effective, a long sensor lifetime (usually $>$ 10 years) and maintenance-free operation are essential for these interconnected sensing devices. In such scenarios, monitoring battery-life and performing battery replacement in large numbers will be expensive. Energy harvesting from ambient sources provides an attractive solution to this problem. However limited power densities of energy harvesters, due to the constrained form-factors of these sensor nodes and strong dependence of the available power for harvesting on the environment makes power delivery extremely challenging. Moreover, these ultra-low power sensors consist of various components which perform different tasks. These components have independent power specifications and voltage ratings. Thus, a system-level approach is necessary to address issues and design the power management infrastructure of a sensor node.

In recent years, there has been an increase in research efforts which focus on solving the problems related to power delivery as stated above. Most of these research efforts provide point solutions targeting specific application areas and design spaces. This dissertation addresses some of the system-level issues related to power management in ultra-low power sensors and the factors limiting the lifespan of these sensing systems. To ensure battery-less, self-powered operation, this work presents a single-inductor boost converter which is capable of harvesting both solar and thermoelectric energy. Efficient harvesting under varying power levels and from low input voltages ensure improvements in charging the storage node and store more usable energy under poor environmental conditions. To support the different electrical requirements of a sensing system consisting of an SoC, a wireless transmitter and a non-volatile memory contained in an SiP along with external components, this work presents

a modular power management and voltage regulation architecture.

It is found that reducing the quiescent power of components which are "always-ON", such as voltage regulators, reference generators and lowering the standby power of duty-cycled components such as digital accelerators is essential for achieving maximum benefits on sensor lifetime, in the absence of harvesting. Efficient regulation also provides a designer the flexibility to integrate additional "always-ON" components and functionality, such as wake-up timers. It also enables the designer to allocate more duty-cycle to periodically active components such as transmitters. Apart from reducing the quiescent power of power management circuits to improve the conversion efficiency, this work also attempts to lower the standby power of various sensor components supported by the voltage regulators such as microprocessors, digital filters and wakeup receiver. Also low-power techniques to monitor supply voltage variation are described.

To conclude, power management will continue to play a major role in the context of emerging applications pertaining to the IoT. With the advances in sensing technologies, such as electromagnetic and piezoelectric harvesters as well as storage devices, such as batteries and supercapacitors, the power management infrastructure needs to be tailored appropriately. The availability of different harvesting mechanisms and sensor components with different electrical requirements creates a design space with numerous possibilities and configurations. The benefits of such configurations and associated design knobs can be evaluated using a performance evaluation infrastructure similar to the modeling framework and tool flow discussed in this work.

Appendix A

Publications

AR1 **A. Roy**, B.H. Calhoun, "A 71% efficient Energy Harvesting and Power Management Unit for sub-μW power biomedical applications", 2017 IEEE Biomedical Circuits and Systems Conference (BioCAS), Turin, Italy, 2017

AR2 **A. Roy**, B.H. Calhoun, "Exploring circuit robustness to power supply variation in low-voltage latch and register-based digital systems", 2016 IEEE International Symposium on Circuits and Systems (ISCAS), Montreal, QC, 2016

AR3 **A. Roy**, A. Klinefelter, F.B. Yahya, X. Chen, P. Gonzalez, C.J. Lukas, D. Akella, J. Boley, K. Craig, M. Faisal, S. Oh, N.E. Roberts, Y. Shakhsheer, A. Shrivastava, D. Vasudevan, D.D. Wentzloff, and B.H. Calhoun, "A 6.45μW Self-Powered SoC With Integrated Energy-Harvesting Power Management and ULP Asymmetric Radios for Portable Biomedical Systems", in Biomedical Circuits and Systems, IEEE Transactions on , vol. 9, no. 6, pp. 862-874, Dec 2015.

AR4 F.B. Yahya, C.J. Lukas, J. Breiholz, **A. Roy**, H.N. Patel, N. Liu, X. Chen, A. Kosari, S. Li, D. Akella, O. Ayorinde, D. Wentzloff, B.H. Calhoun, "A Battery-less 507nW SoC with integrated platform power manager and SiP interfaces", Symposium on VLSI Circuits, Kyoto, Japan, 2017

AR5 A. Klinefelter, N. Roberts, Y. Shakhsheer, P. Gonzalez, A. Shrivastava, **A. Roy**, K. Craig, M. Faisal, J. Boley, S. Oh, Y. Zhang, D. Akella, D. Wentzloff, B.H. Calhoun, "21.3 A 6.45μW self-powered IoT SoC with integrated energy-harvesting power management and ULP asymmetric radios", in Solid- State Circuits Conference - (ISSCC), 2015 IEEE International , Feb. 2015

AR6 J. Moody, P. Bassirian, **A. Roy**, N. Liu, S. Pancrazio, N.S. Barker, B.H. Calhoun, S.M. Bowers, "A -76dBm 7.4nW Wakeup Radio with Automatic Offset Compensation", in Solid- State Circuits Conference - (ISSCC), 2018 IEEE International , Feb. 2018

AR7 **A. Roy**, P. Grossmann, S. Vitale, B.H. Calhoun, "A 1.3μW, 5pJ/cycle sub-threshold MSP430 processor in 90nm xLP FDSOI for energy-efficient IoT applications", 2016 17th International Symposium on Quality Electronic Design (ISQED), Santa Clara, CA, 2016

AR8 H.N. Patel, **A. Roy**, F.B. Yahya, N. Liu, K. Kumeno, M. Yasuda, A. Harada, T. Ema, B.H. Calhoun, "A 55nm Ultra Low Leakage Deeply Depleted Channel technology optimized for energy minimization in subthreshold SRAM and logic", ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference, Lausanne, Switzerland, 2016

AR9 J. Moody, P. Bassirian, **A. Roy**, Y. Feng, S. Li, R. Costanzo, N.S. Barker, B.H. Calhoun, and S.M. Bowers, "An 8.3 nW -72dBm Event Driven IoE Wake Up Receiver RF Front End", accepted to European Microwave Integrated Circuit Conference (EuMIC), Nuremberg, Germany, Oct 2017.

AR10 D. A. Kamakshi, H. N. Patel, **A. Roy**, B. Calhoun, "A 28 nW CMOS Supply Voltage Monitor for Adaptive Ultra-Low Power IoT Chips", IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), San Francisco, CA, Oct 2017

Patent

AR11 **A. Roy**, B.H. Calhoun, "Gate leakage based reference generator", US Provisional Patent Application 62/513,573, filed on Jun 1, 2017

Planned/Upcoming Publications

AR12 "Wide input power range, 90% peak efficiency energy-harvesting charger with adaptive peak current control and fully integrated cold-start for emerging IoT applications"

AR13 "Design considerations for baseband circuits in ultra-low power event driven wakeup receivers"

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