Millimeter-Wave Planar Varactor Frequency Doublers

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Abstract

A pair of millimeter-wave frequency multipliers, a 40/80 GHz balanced doubler and an 80/160 GHz balanced doubler, were designed using advanced three dimensional electromagnetic simulation tools. The doublers comprise a mechanically rugged planar GaAs Schottky varactor chip mounted on a quartz circuit housed in a split waveguide block. The doublers are designed for wide-band, fixed-tuned operation. Methodologies for designing the planar varactor chips and circuits were developed. The 40/80 GHz doubler exhibits record fixed-tuned bandwidth, output power and efficiency. Moreover, there exists a high level of agreement between the simulated and measured results, validating the design methodology and the simulation tools.

The 40/80 GHz doubler exhibits a measured 3 dB bandwidth of 17% at an input power of 200 mW. At 41/82 GHz, the measured efficiency is 51% at an input power of 150 mW. The efficiency drops to 48% at an input power of 200 mW. The measured and simulated bandwidths are nearly identical and the measured peak output power is within 1.8 dB of the simulated result. The 40/80 GHz doubler is also evaluated at cryogenic temperatures in a calibrated dewar. The measured efficiency is 61% at an input power of 150 mW and a block temperature of 14 K. The efficiency drops to 48% at an input power of 365 mW and output power of 175 mW.

Simulations for the 80/160 GHz doubler show efficiency and bandwidth similar to the 40/80 GHz design. Measured results indicate a peak efficiency of 21%, peak output power of 16 mW, and fixed-tuned bandwidth of 15%.

Table of Contents

List of Tables

List of Figures

List of Abbreviations

Au.....Gold.

BWO ..... Backward Wave Oscillator.

CPW.....Coplanar waveguide.

CW ..... Continuous-wave.

EM.....Electro-Magnetic.

EMF .....Electromotive force.

FEA.....Finite Element Analysis.

fF .....Fempto-Farad (10^{-15}).

FIR .....Far-Infrared.

GaAs .....Gallium-arsenide.

Ge..... Germanium.

GHz.....Gigahertz (10^{9}).

HFSS.....High Frequency Structure Simulator™

HMDS.....HexaMethylDiSilizane.

IF ..... Intermediate frequency.

In .....Indium.

LHe .....Liquid helium (~4 K).

LN_2.....Liquid nitrogen (~77 K).

LNA .....Low noise amplifier.

LO .....Local oscillator.

MDS.....Microwave Design System ™.

MMIC ..... Monolithic Microwave Integrated Circuit.

MMW.....Millimeter wave.

Q..... Quality factor.

RF..... Signal frequency.

RTD..... Resonant Tunneling Diode.

SB13T1 ..... UVA varactor designation.

SDL..... Semiconductor Device Laboratory.

SMMW ..... Submillimeter wave.

SWR.....Standing wave ratio.

TCA..... TriChloroEthane.

TED.....Tranferred Electron Device.

TEM ..... Transverse Electro-Magnetic.

TEO.....Transferred Electron Oscillator.

THz .....Terahertz (10^{12}).

TK .....Thomas-Keating.

TWT ..... Travelling Wave Tube.

UVA.....University of Virginia.

List of Symbols

Arabic Symbols

A_a ..... Anode cross-sectional area.

A_{ohmic} ..... Ohmic contact area.

C_{avg} ..... Time average junction capacitance.

C_{fp} ..... Parasitic finger-to-pad capacitance.

C_j ..... Nonlinear junction capacitance.

C_{j0} ..... Zero biased junction capacitance.

C_{pp} ..... Parasitic pad-to-pad capacitance.

D ..... Anode diameter.

f_{LO} ..... Local oscillator frequency.

I_{peak} ..... Peak value of the time domain current.

I_s ..... Reverse saturation current.

I_{sat} ..... Velocity saturation current.

K ..... Kelvin.

k ..... Boltzmann's constant (1.380×10^{-23} J/K).

k_z ..... Mode propogation constant.

L_f ..... Finger inductance.

m_o m_e ..... Effective electron mass.

mW ..... Milliwatt.

$\hat{n}$ ..... Unit normal vector.

N_D ..... Epitaxial layer doping.

P_{av} ..... Available power.

P_{dis} ..... Dissipated power in the varactor.

P_{in} ..... Input power.

P_{out} ..... Output power.

P_{refl} ..... Reflected input power.

q ..... Charge of electron (1.602×10^{-19} C).

Q ..... Charge.

r_a ..... Anode radius.

r_{oc} ..... Ohmic contact radius.

R_1 ..... Embedding resistance at ω_0.

R_2 ..... Embedding resistance at $2\omega_0$.

R_{buf} ..... Series resistance in the buffer layer.

R_j ..... Nonlinear junction resistance.

R_{ohmic} ..... Series resistance in the ohmic contacts.

R_s ..... Total varactor series resistance.

R_{spread} ..... Spreading resistance.

S_{xx} ..... Scattering parameter.

[S] ..... Scattering matrix.

t_{buf} ..... Buffer layer thickness.

t_{epi} ..... Epitaxial layer thickness.

T ..... Temperature (Kelvin).

T_0 ..... Ambient temperature (290 K).

TE_{xx} ..... Transverse electric mode.

TM_{xx} ..... Transverse magnetic mode.

UV ..... Ultraviolet.

V_0 ..... $\eta kT/q$.

V_b ..... Reverse breakdown voltage.

V_{bi} ..... Built-in voltage.

V_d ..... V_j plus voltage across R_s.

V_{DC} ..... DC bias voltage.

V_g ..... Source voltage.

V_j ..... Junction voltage.

V_T ..... Thermal voltage.

$w(V_j)$ ..... Depletion width.

X_1 ..... Embedding reactance at ω_0.

X_2 ..... Embedding reactance at $2\omega_0$.

Z_0 ..... Intrinsic impedance.

$Z_1(\omega_0)$ ..... Input frequency embedding impedance.

$Z_2(2\omega_0)$ ..... Output frequency embedding impedance.

Z_{em} ..... Embedding impedance.

Z_g ..... Source impedance.

Z_{in} ..... Input frequency embedding impedance.

Z_{out} ..... Output frequency embedding impedance.

Z_{pi} ..... Characteristic impedance based on power-current relation.

Z_{pv} ..... Characteristic impedance based on power-voltage relation.

Z_{vi} ..... Mean of Z_{pi} and Z_{pv}.

Z_T ..... Characteristic impedance of Teflon loaded waveguide.

Greek Symbols

α ..... Attenuation coefficient.

Γ ..... Reflection coefficient.

δ_{buf} ..... Buffer layer skin depth.

ε ..... Permitivity.

ε_r ..... Relative permittivity.

ε_s ..... GaAs dielectric permittivity.

η ..... Varactor ideality factor.

η_m ..... Multiplication efficiency.

λ ..... Wavelength.

μ ..... Permeability or mobility.

μm ..... Micron.

σ ..... Conductivity.

Ω ..... Ohm.

ω_r ..... Resonant frequency.

ω_0 ..... Radian input frequency.

Chapter 1

Introduction

There is a demand for millimeter-wave (MMW) and submillimeter-wave (SMMW) power sources. These sources are employed primarily as local oscillators (LO) in sensitive heterodyne radiometers used for remote sensing, atmospheric physics, and radio astronomy. However, there is also a need for MMW and SMMW sources for other applications including laboratory and industrial spectroscopy, collision avoidance radar, compact radar ranges, and a wide variety of laboratory measurements. The ideal source for most of these applications would exhibit high output power and efficiency, large electronically tuned bandwidth (fixed mechanical tuning), high tolerance to mechanical and thermal stress, high reliability, low noise, low mass and low cost. Unfortunately, current MMW and SMMW sources lack many of these features. Table I provides a partial list of some of the most important MMW and SMMW fundamental oscillator and amplifier technologies available today and provides a short summary of their strengths and weaknesses. More thorough technological reviews may be found in [Bradley, 1992] and [Kimmitt, 1997].

An alternative to a fundamental oscillator operating in the MMW or SMMW regime is a lower frequency fundamental oscillator used in conjunction with a frequency multiplier. In theory, GaAs Schottky varactor frequency multipliers pumped by electronically tunable low noise fundamental oscillators can achieve all of the desired qualities listed earlier. However, most current state of the art frequency multipliers exhibit very narrow

Technology	Frequency	Advantages	Disadvantages	Reference
Lasers				
FIR gas	0.1 - 30 THz	CW, high power, low noise high frequency	discrete spectrum, expensive, bulky, bandwidth ~ 200 MHz	Douglas, 1989
Free electron	MMW - visible	continuously tunable	very expensive, bulky, pulsed	Ramain, 1992
Semiconductor	1 - 4 THz	(p-Ge), high frequency	pulsed, cooled ~ 15 K	Bründermann,1996
Tubes				
BWO Carcinotron	to ~ 1.2 THz	CW, 1 mW at 1.2 THz, broadband (30%)	multi-moded	Kimmitt, 1997
Gyrotron	< 300 GHz	high power	pulsed, frequency limitations, requires high magnetic field	Idehara, 1996
TWT	< 50 GHz	CW, high power, wide-band	low frequency	Pozar, 1998
Ledatron	to several THz	CW, 30% bandwidth	~ 25 kV beam voltage, expensive	Smith et al, 1953
Orotron				Kimmitt, 1997
Klystron		CW, high power	high-Q, narrow-band, mech.tuners	Pozar, 1998
Semiconductors				
RTD	to 800 GHz	CW	low power (0.5 μW at 712 GHz)	Brown, 1995
TED (Gunn)	< 200 GHz	CW, low noise, high power	high Q, mech. tuners	Carlstrom, 1989
MMIC	< 200 GHz	CW, integration	heat dissipation, design	

Table 1.1. State of the art MM-wave fundamental oscillator technologies.

instantaneous bandwidths and rely on at least one or more mechanical tuners to achieve acceptable conversion efficiency. Moreover, most of the MMW and SMMW frequency multipliers described in the literature employ whisker contacted Schottky varactors.

As advances in semiconductor technology have steadily produced devices with higher operating frequencies, two terminal devices (varistors and varactors) with whisker contacts have historically led the way. This is due primarily to the extremely low parasitics associated with the whisker contacts and the simplicity of the two terminal device. However, whisker contacts are rather fragile and therefore can significantly reduce the reliability of the frequency multiplier. It is very difficult and time consuming to space qualify whisker contacted devices. If the whisker contact fails during launch or while in space, an entire receiver may be jeopardized. Whisker contacted devices are also difficult and costly to assemble.

As semiconductor technology matures, whisker contacted devices are being supplanted by planar devices wherein the fragile whisker is replaced with a mechanically robust integrated finger [Bishop et al, March 1993]. At a given frequency, the parasitics associated with a planar device are never quite as low as those of a comparable whisker contacted device, but the parasitics in a planar device can often be reduced to acceptable levels. Aside from the mechanical advantages inherent in planar devices, there are a number of important electrical advantages. It is extremely difficult to employ multiple whisker contacted devices in a circuit, although it has been demonstrated [Erickson, 1990]. Conversely, it is easy to integrate multiple planar devices in a wide variety of configurations and with a great deal of control over the geometry. The use of multiple devices not only

leads to higher power handling capability, but also allows balanced configurations which can give higher multiplier efficiency. The advantages of balanced multiplier designs will be described in detail in chapter 2.

To date, frequency multipliers reported in the literature tend to exhibit either narrow fixed-tuned bandwidths or low conversion efficiencies (most exhibit both deficiencies). This is somewhat surprising since theory suggests that Schottky varactor multipliers can achieve 100% conversion efficiency if the embedding impedances provided by the circuit to the device at the input, output, and idler frequencies are optimum and parasitic ohmic losses are zero [Penfield and Rafuse, 1962]. In practice there is always ohmic circuit loss and uncertainty in the embedding impedances, but very high efficiencies are still predicted. This work will show that the discrepancy between theory and practice often arises from lack of an accurate nonlinear device model and also from a failure to provide the correct embedding impedances with a low loss circuit. In addition, since MMW and SMMW devices are often “electrically long”, their supporting structures present non-negligible parasitics which are not accurately modeled with lumped-element circuits.

Circuit designers have traditionally overcome this problem using a heuristic or trial and error approach. The heuristic approach can be very powerful, especially when practiced by designers who possess a great deal of intuition in microwave design. However, this approach is time consuming and is only used by necessity. With the advent of robust 2-D and 3-D electromagnetic (EM) computer simulation software in the last decade, we are now able to abandon the heuristic approach and obtain accurate EM solutions to arbitrary and complex geometries [Hewlett-Packard, 1997]. It will be shown in this work that a commercially

available and robust 3-D simulator can be used to design frequency multipliers that work as expected on the first attempt.

The goal of this research was to develop an efficient, mechanically robust, easy to build, high-power, wide-band, fixed-tuned, well understood, MM-wave frequency multiplier. To achieve high efficiency requires that the multiplier be a varactor rather than a varistor since varistor mode efficiencies are theoretically limited to $1/N^2$, where N is the multiplication factor [Page, 1956]. Also, high efficiency operation requires a minimum of ohmic losses in the varactor and embedding circuit. To be mechanically robust, the multiplier should use planar varactors rather than whisker contacted varactors. The use of planar varactors also simplifies the assembly of the multiplier. Additionally, higher power handling can be achieved through the use of multiple devices on a single chip. Achieving wide-band operation without the aid of mechanical tuners requires that the embedding circuit be well characterized. This is done using a 3-D EM simulator in conjunction with standard microwave circuit models.

As a starting point in this research, effort was focused on the development of a pair of planar balanced doublers based on the circuit topology described in the literature [Erickson, 1990]. Erickson's 87/174 GHz doubler achieved high output power and efficiency by using a balanced configuration in conjunction with low loss transmission media. However, it exhibited a very narrow fixed-tuned bandwidth and employed three mechanical tuners. By using an advanced 3-D EM simulator, the tuners can be eliminated and the fixed-tuned bandwidth can be significantly improved.

To this end, two frequency multipliers were built and tested; (i) a 40/80 GHz planar

balanced doubler and (ii) an 80/160 GHz planar balanced doubler. These doublers exhibit record fixed-tuned bandwidth and output power. Additionally, there exists an unprecedented high level of agreement between the simulated and measured results.

Chapter 2 describes the basic design philosophy of the new planar balanced frequency doublers. The important advantages inherent in planar balanced doublers is discussed in more detail. The novel balanced doubler [Erickson, 1990] which served as the prototype for the new designs is reviewed. Finally, the new 40/80 GHz and 80/160 GHz planar balanced doubler designs are presented.

As part of this work, I designed the varactor chips used in the 40/80 GHz and 80/160 GHz balanced doublers. However, the fabrication of the varactor chips was done by William Bishop at the University of Virginia Semiconductor Device Laboratory. Chapter 3 covers basic varactor theory and provides some guidelines for the design of planar varactor chips. The design process for the varactors used in the 40/80 GHz and 80/160 GHz doublers will be used as examples. Chapter 4 discusses linear circuit analysis and the practical use of the 3-D EM simulator HFSS (Hewlett Packard's High Frequency Structure Simulator).

Chapter 5 describes the experimental test procedures and equipment used to measure the doubler performance. Test systems for room temperature and cryogenic measurements are described. A technique for evaluating the output frequency match is also described. The test results will be presented in Chapter 6. A comparison of the simulated and measured results and some final conclusions are presented in Chapter 7.

Chapter 2

Design Philosophy and Methodology

2.1 Introduction

The basic goal of a frequency doubler is to efficiently convert power incident from an external source at frequency ω_0 to power at frequency $2\cdot\omega_0$. Thus, we can think of a frequency doubler as a two port device as illustrated in Fig. 2.1. The multiplication efficiency, η_m, is dependent primarily on the nonlinear device, the embedding impedances provided by the circuit, ohmic losses in the circuit and nonlinear device, and the "pump" power. If the optimum embedding impedances are presented to a lossless varactor by a lossless circuit, then η_m is theoretically 100 % [Manley and Rowe, 1956]. The output filter is necessary to ensure that power from the external source at frequency ω_0 does not propagate beyond the varactor and become absorbed by the load, Z_L, or other ohmic elements in the output matching circuit. Similarly, the input filter prevents the output power at frequency $2\cdot\omega_0$ from propagating back to the source and becoming absorbed in the source impedance, Z_g, and other ohmic elements in the input matching network. The isolation provided by the filters also helps to reduce or eliminate the interdependency between the input and output

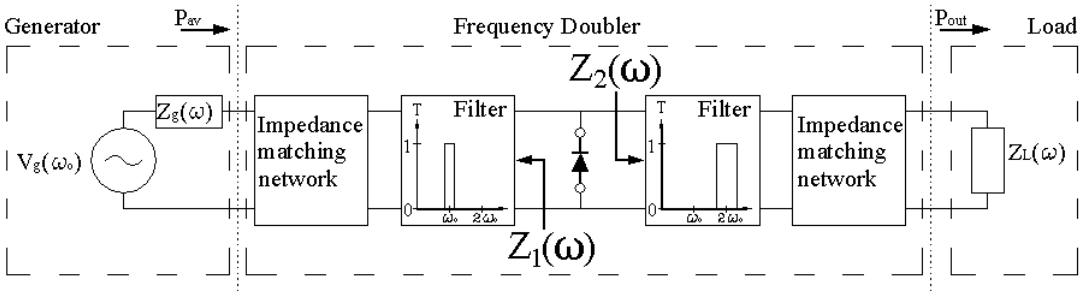


Fig. 2.1 Frequency doubler block diagram.

matching circuits, thus simplifying the design.

Since the frequency dependent embedding impedance, $Z_e(\omega)$, is the parallel combination of $Z_1(\omega)$ and $Z_2(\omega)$, it is important that the filters provide a high impedance in the respective rejection bands and do not short out the varactor at ω_0 and $2\omega_0$. In the MMW and SMMW regime, there are no true "lumped elements", and thus filters and impedance matching networks are usually distributive networks. Distributive filters tend to be lossy, take up a relatively large amount of physical area in the circuit, and degrade the bandwidth of the multiplier.

2.2 Balanced Doublers

A balanced doubler design can be used to achieve the required isolation between the input and output circuits without employing distributive filters. In this case, pairs of varactors are placed in anti-series at the junction between balanced and unbalanced transmission lines as illustrated in Fig. 2.2. If the incident power on the diodes at frequency ω_o is in a balanced mode, then the output radiation at $2\cdot\omega_o$ is generated in an unbalanced mode. Furthermore, if the unbalanced line does not support a balanced mode, then isolation is achieved.

Examples of balanced transmission lines include rectangular waveguide (TE_{10} mode), twin lead, finline, microstrip and slotline. Unbalanced lines include coaxial, stripline and coplanar waveguide (CPW). The transition from slotline to CPW is attractive for MMIC applications since both of these transmission media are planar and easily fabricated on wafers. However, there are a number of problems with these types of transmission lines. Both lines tend to be lossy due to power radiated from the circuit. It is also difficult to

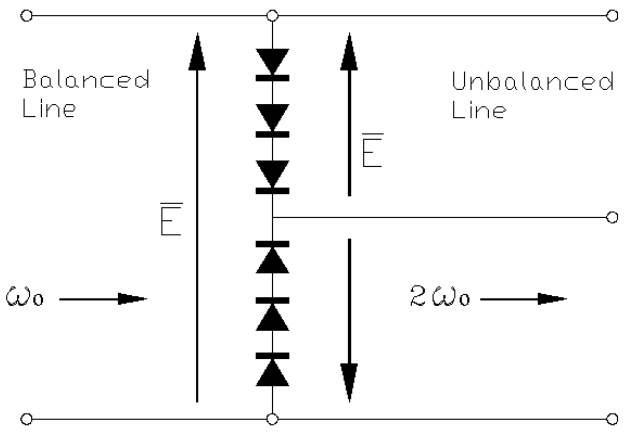


Fig. 2.2. Balanced doubler schematic.

realize low impedance lines in CPW and slotline because of the resulting narrow gap between the conductors. Narrow gaps are not only difficult to fabricate but lead to high current densities near the metal edge, resulting in higher ohmic losses.

A more attractive approach was implemented in a pair of balanced doublers operating at 80/160 GHz and 165/330 GHz reported by [Erickson, 1990]. The two designs were similar and incorporated a pair of whisker contacted diodes mounted on a machined cylindrical metal pin. The pin acted as the center conductor in a coaxial structure that supports an unbalanced TEM mode. The pin also functioned as an output waveguide probe and DC bias line. Erickson later reported an 87/174 GHz balanced doubler wherein he replaced the two whisker contacted diodes with a planar diode package [Erickson et al, 1993]. This modification resulted in higher output power and efficiency, easier assembly and a more mechanically rugged device.

Fig. 2.3 shows a diagram of Erickson's modified 87/174 GHz planar balanced doubler. The planar diode chip is soldered at each end to the waveguide block and at the center to the metal pin. The input radiation is incident on the diodes in a balanced mode

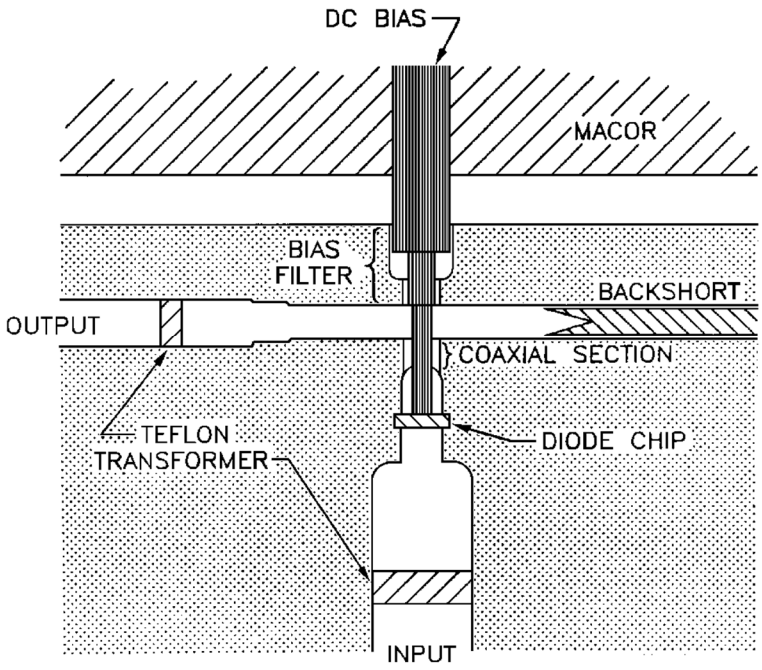


Fig. 2.3. Block diagram of Erickson's 87/174 GHz planar balanced doubler.

(TE_{10}) from reduced height rectangular waveguide. The output frequency is generated by the diodes in an unbalanced mode (TEM) and is free to propagate along the pin to the output waveguide. There are a number of propagating modes supported by the input waveguide at the output frequency. The lowest order of these modes which can couple to the output frequency unbalanced field distribution is the TM_{11}. However, the TM_{11} mode can be cutoff by sufficiently reducing the input waveguide height (typically ½ height or less). The length of the reduced height waveguide between the diodes and the full-height input waveguide is a parameter in the design that can be varied to achieve an acceptable input match.

The fundamental frequency can propagate beyond the diode chip toward the output waveguide. The metal pin in this quasi-coaxial region perturbs the input TE_{10} field distribution, affecting the propagation constant and characteristic impedance. At some point

between the diode chip and the output waveguide, the width of the quasi-coaxial waveguide section must be sufficiently reduced to cut off propagation of the fundamental frequency. This reduction in width creates an effective input frequency backshort and the position of this backshort can be used as another design element for the input frequency embedding impedances.

There are four important advantages in Erickson's balanced multiplier; (i) the balanced design eliminates the need for lossy distributed filters, (ii) the rectangular waveguides and the coaxial line have low loss, (iii) DC bias is easily provided to the varactors through the metal pin, and (iv) the design is amenable to the use of multiple varactors in a planar package, resulting in high power handling and reliability. There are also, however, two important limitations; (i) it is difficult to mount the pin in the waveguide block and to solder the varactor chip to the pin, and (ii) the output frequency matching circuit is limited by the pin geometry resulting in a rather narrow fixed-tuned bandwidth. A pair of Teflon impedance transformers located in the input and output waveguides improve the multiplier efficiency by providing a wide range of mechanical tuning. However, these transformers cannot be adjusted during operation. Also, the transformers are located some distance away from the varactors which further compromises the instantaneous bandwidth.

2.3 The New 40/80 GHz and 80/160 GHz Balanced Doublers

The new 40/80 GHz and 80/160 GHz doubler designs developed in this work retain all of the important advantages of Erickson's multiplier. However, there is a much higher degree of control over the second harmonic embedding impedances in the new designs which

has resulted in a significant increase in the fixed-tuned bandwidth and an unprecedented level of agreement between simulations and the measured data. Additionally, the new designs are more planar which makes them easier to assemble and may lead to further integration of the varactor and circuit. Fig. 2.4 shows a sketch of the new 40/80 GHz design.

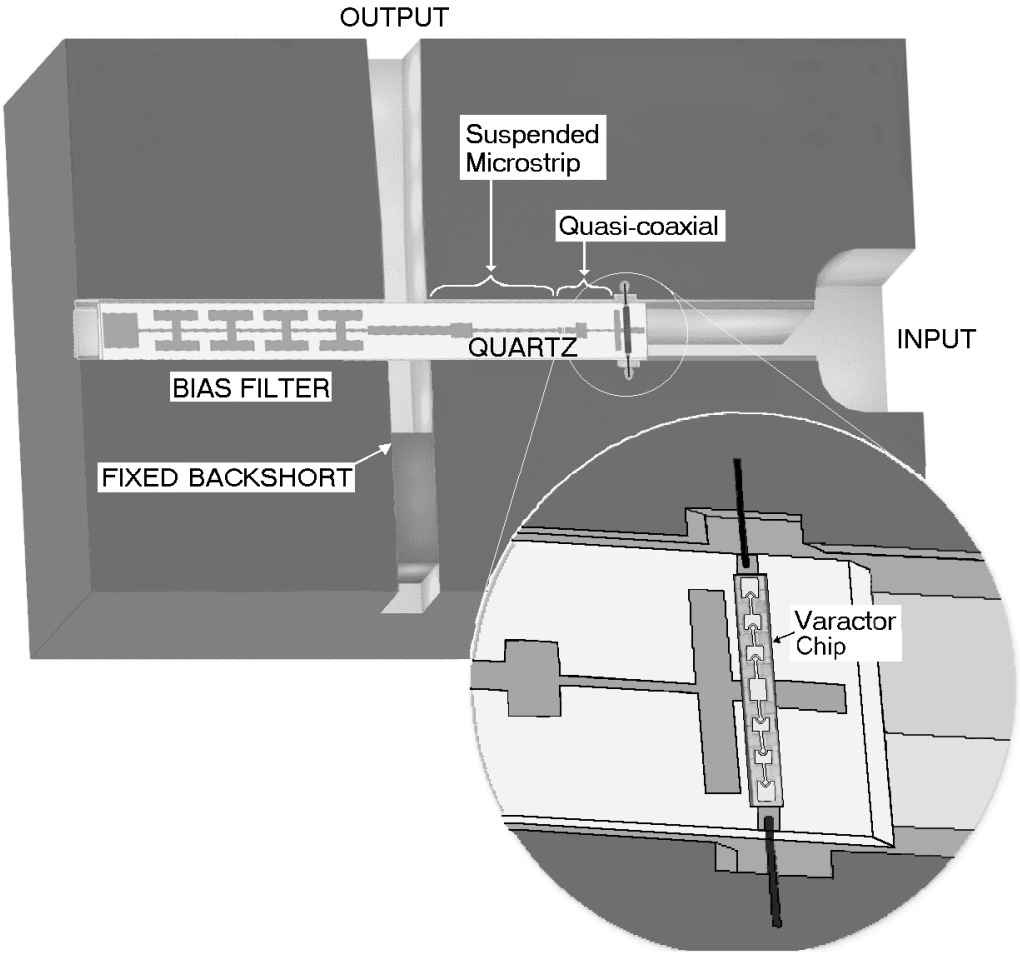


Fig. 2.4. 40/80 GHz planar balanced doubler. The varactor is shown facing upward to illustrate the distinguishing features of the chip.

There are no adjustable mechanical tuners in this design, but rather a fixed indium backshort. The metal pin in Erickson's design has been replaced with a quartz circuit. The center conductor for the TEM line, an output waveguide probe and an RF blocking filter for

the DC bias network are photolithographically formed on the quartz substrate. This allows for a high degree of flexibility and control of the center conductor dimensions and therefore substantial control over the output frequency embedding impedance. Another advantage of the new design is the ease and low cost of producing the quartz circuits in large numbers. In future designs, the planar quartz circuit could be integrated with the planar varactor chip.

The theory of operation is identical to Erickson's doubler. The input radiation is incident on the varactors in a balanced mode (TE_{10}) in reduced-height Q-band waveguide. However, the input radiation can propagate beyond the varactor chip toward the E-band output waveguide. The center conductor and quartz dielectric in this quasi-coaxial region only slightly perturb the TE_{10} mode. Increasing the center conductor width increases the propagation constant and reduces the characteristic impedance and cutoff frequency. At a point between the varactor chip and the output waveguide, the width of the quasi-coaxial waveguide section is sufficiently reduced to cut off propagation of the TE_{10} mode, creating a reactive termination (backshort) at the input frequency. The reduced-width section, more appropriately termed as enclosed suspended microstrip, extends to the output waveguide. The position of the backshort and the length of the reduced-height waveguide section between the varactors and the full-height input waveguide are design parameters that were used to obtain an acceptable input frequency embedding impedance. The output frequency is generated by the varactors in an unbalanced mode (TEM) and is free to propagate to the output waveguide. The TM_{11} mode in the input waveguide is cutoff by sufficiently reducing the input waveguide height.

The machining of the block is straightforward and can be accomplished on a

computer controlled milling machine. The formation of the fixed indium backshort is a relatively simple task and can be performed with a hand-held probe and a machined metal insert with a flat surface on one end which fits into the output waveguide. The mounting of the varactor chip and circuit are also relatively simple. Circuit fabrication and varactor mounting techniques are covered in depth in Appendix E.

The 80/160 GHz doubler shown in Fig. 2.5 is essentially a scaled version of the 40/80 GHz doubler, with two notable exceptions; (i) the overall length of the varactor chip could not be scaled down by a factor of two and thus the reduced height waveguide at the varactors is not a true scaled version of the 40/80 GHz block and, (ii) there is a further reduction in the waveguide height between the varactors and the full height input guide in the 80/160 GHz version which does not appear in the 40/80 GHz version.

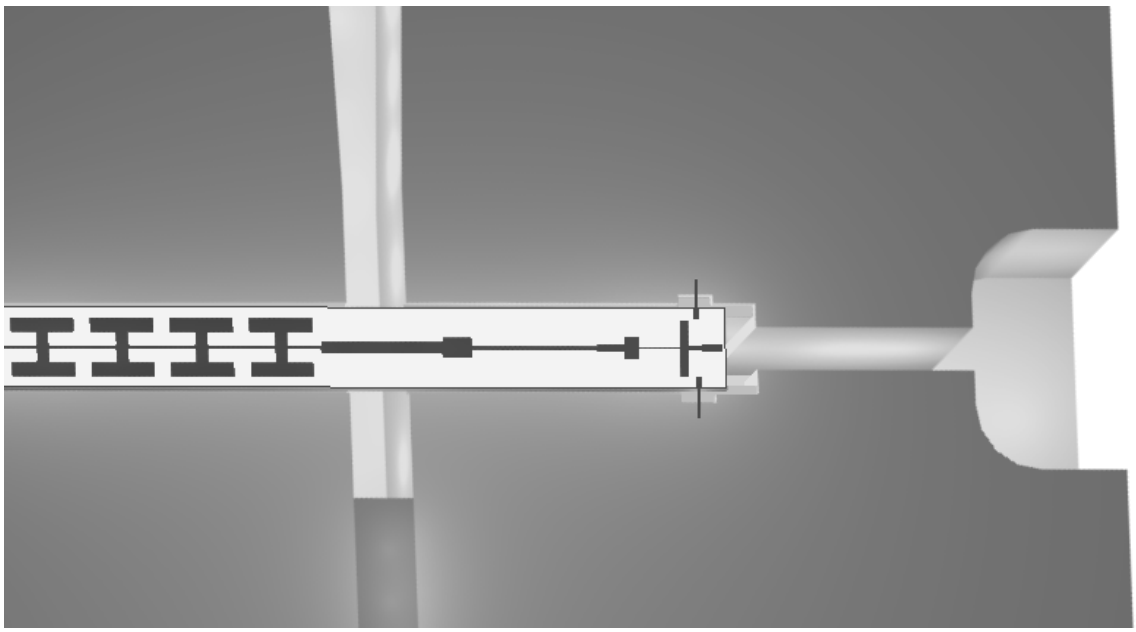


Fig. 2.5. Enlarged view of the 80/160 GHz planar balanced doubler showing the modified reduced height input waveguide. The varactor is not shown in order to reveal the mounting pads and bond wires.

The 40/80 GHz doubler employs a UVA type SB13T1 varactor chip comprising a linear array of 6 GaAs planar Schottky varactors with an epitaxial layer doping of $1x10^{17}$ cm^{-3}. The 80/160 GHz doubler employs a linear array of 4 GaAs planar Schottky varactors with an epitaxial layer doping of $2x10^{17}cm^{-3}$. A more thorough description of the varactor chips is presented in Chapter 3.

2.4 Summary

The fundamental requirements for a multiplier circuit were covered in Section 2.1. Section 2.2 explained the advantages inherent in a balanced multiplier configuration. A unique balanced doubler which served as the prototype for the new 40/80 GHz and 80/160 GHz doublers was also discussed. It was shown that the prototype had many desirable features such as high efficiency, high power, and low loss, but that it also exhibited a narrow fixed-tuned bandwidth and was difficult to assemble. The prototype also employed three mechanical tuners which made it difficult to optimize at a given frequency.

The basic topology for the 40/80 GHz and 80/160 GHz balanced doublers developed in this work was shown in Section 2.3. These new doublers maintain all of the advantages of the prototype while eliminating the mechanical tuners and significantly increasing the fixed-tuned bandwidth. Also, the new designs use a planar circuit which makes them less expensive and easier to assemble and may lead to future integration of the varactor and circuit.

Chapter 3

Planar Schottky Varactor Design

3.1 Overview

The basic circuit topology of the 40/80 GHz and 80/160 GHz planar balanced doublers was shown in Chapter 2. A brief description of the varactor chips used in the doublers was also given. This chapter explains the methodology used to design the planar varactor chips and provides some basic guidelines that may be generally useful for other varactor designs.

The primary design parameters for a planar varactor chip include the epitaxial layer doping, N_D , the anode diameter, D , the number of anodes and the physical geometry of the chip including the ohmic contact area and the finger length. Although there are only a limited number of parameters, the design is a rather complicated process involving numerous tradeoffs. In order to fully understand how each of the design parameters effects the varactor's performance, it is necessary to perform a nonlinear analysis on an equivalent circuit model of the device. A large signal equivalent circuit model for a planar Schottky varactor and the basic varactor theory necessary to understand the individual circuit components is presented Section 3.2. Emphasis is placed on determining approximate values for the breakdown voltage, junction capacitance, depletion width and series resistance. Two higher order effects which can adversely affect the multiplier efficiency, velocity saturation and plasma resonance, are also discussed.

The design process used for the planar varactors is described in Section 3.3. The equivalent circuit model developed in Section 3.2 is used in nonlinear simulations to predict

the multiplier efficiency, output power, input power handling ability, optimum embedding impedances, and power dissipated in the series resistance. These quantities are plotted as a function of the various design parameters and the tradeoffs are evaluated.

3.2 Schottky Varactor Theory

A planar Schottky varactor comprises three distinct material interfaces: (i) a metal/epitaxial interface, (ii) an epitaxial/buffer interface, (iii) and an ohmic interface, as illustrated in Fig. 3.1. The nonlinear behavior of the varactor is caused by the Schottky barrier created at the metal/epitaxial interface. The other two interfaces provide a low impedance from the epitaxial layer to the metal.

The buffer layer is highly doped, typically on the order of 5×10^{18} cm^{-3}, to provide

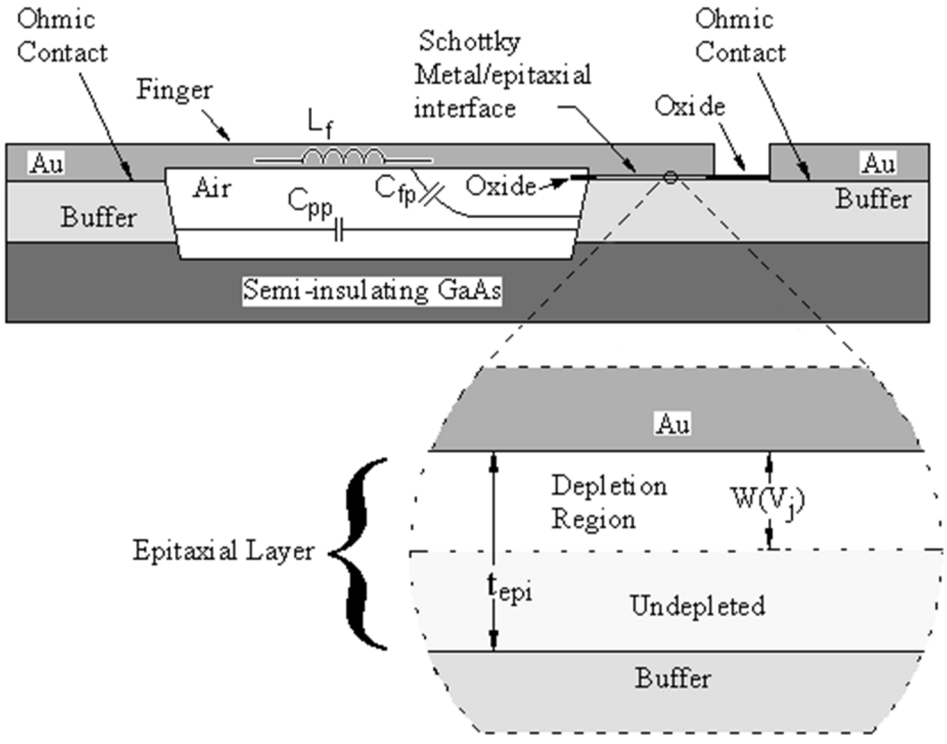


Fig. 3.1. Sketch of a planar Schottky varactor.

low resistance. Typical epitaxial layer doping for MMW and SMMW Schottky varactors is in the range 1×10^{16} - 8×10^{17} cm^{-3}. Three parasitic elements, the pad-to-pad capacitance, C_{pp}, the finger-to-pad capacitance, C_{fp} , and the finger inductance, L_f , are also shown in Fig. 3.1. The capacitive parasitics, C_{pp} and C_{fp} , limit the high frequency operation of the varactor. Devices fabricated at the University of Virginia have the GaAs removed below the finger to minimize these capacitances [Bishop et al, 1987], [Koh et al, 1996]. Extending the length of the finger can further reduce the pad-to-pad capacitance. However, increasing the finger length also increases inductance. This is not a problem in the 40/80 GHz and 80/160 GHz doublers since the finger inductance acts as a crucial tuning element to offset the junction capacitance.

The conduction current in a Schottky diode is given by equation 3.1,

$$I(V_j) = I_0\left(e^{\frac{V_j}{V_0}} - 1\right), \qquad -V_{br} < V_j < V_{jmax} \tag{3.1}$$

where, $I(V_j)$ is the junction current, V_j is the junction voltage, I_0 is the reverse saturation current, V_0 is the thermal voltage (kT/q), V_{br} is the reverse breakdown voltage and V_{jmax} is the threshold where currents become large enough that the assumptions of the thermionic emission theory breaks down due to heating effects. The reverse breakdown voltage, V_{br}, is the threshold for high reverse currents resulting from avalanche breakdown or quantum mechanical tunneling. To express the conduction current as a function of the voltage across the diode terminals, $I(V_d)$, one must include a correction for the series resistance, $V_d = V_j + I\cdot R_s$. Fig. 3.2 shows a typical voltage/current relationship for a GaAs Schottky varactor.

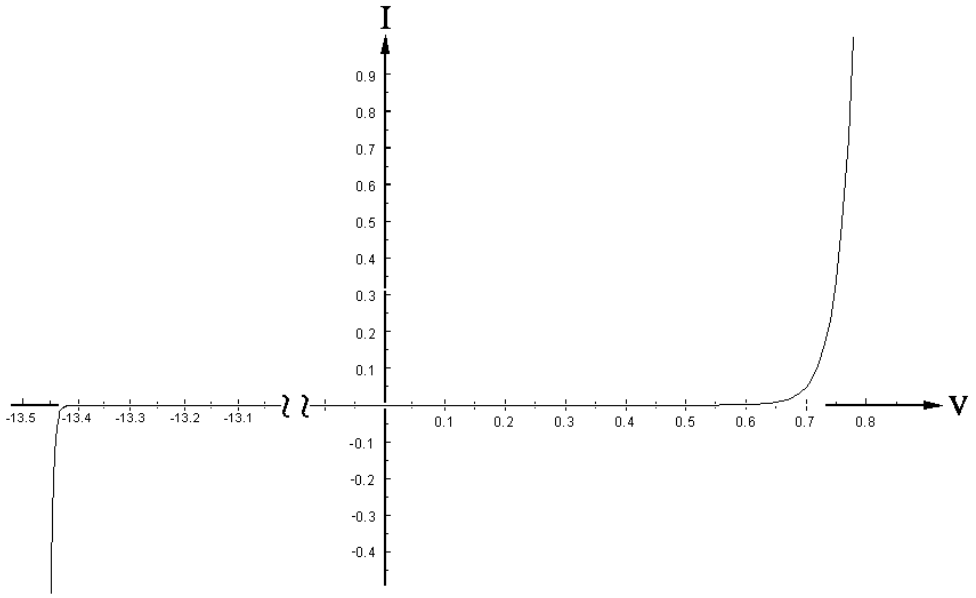


Fig. 3.2. Schottky varactor IV curve.

Reverse Breakdown Voltage

Measured values of V_{br} are typically given as the voltage at which the reverse current achieves some specified level, e.g. 1 μA. Theoretical calculations of reverse breakdown voltage as a function of epitaxial doping, $V_{br}(N_D)$, are given by Sze [Sze and Gibbons, 1966]. Sze calculates $V_{br}(N_D)$ using an ionization integral, plots the calculated data in a graph, and gives a simplified algebraic expression for $V_{br}(N_D)$ derived from the defining integral. Sze's graphical data for $V_{br}(N_D)$ in GaAs gives reasonable agreement with measured values. However, values of $V_{br}(N_D)$ calculated from the algebraic expression do not compare well with measured results. Fig. 3.3 shows the $V_{br}(N_D)$ data from Sze's graph, a curve fit to Sze's data, and some measured data from varactors fabricated at the University of Virginia (UVA) Semiconductor Device Laboratory (SDL). The UVA measured data is taken at a reverse current of 1 μA. Eq. 3.2 is the curve fit to Sze's data used in Fig. 3.3.

$$V_{br} \sim 2.9 + 1.4 \times 10^{14} \cdot N_D^{-0.77} \tag{3.2}$$

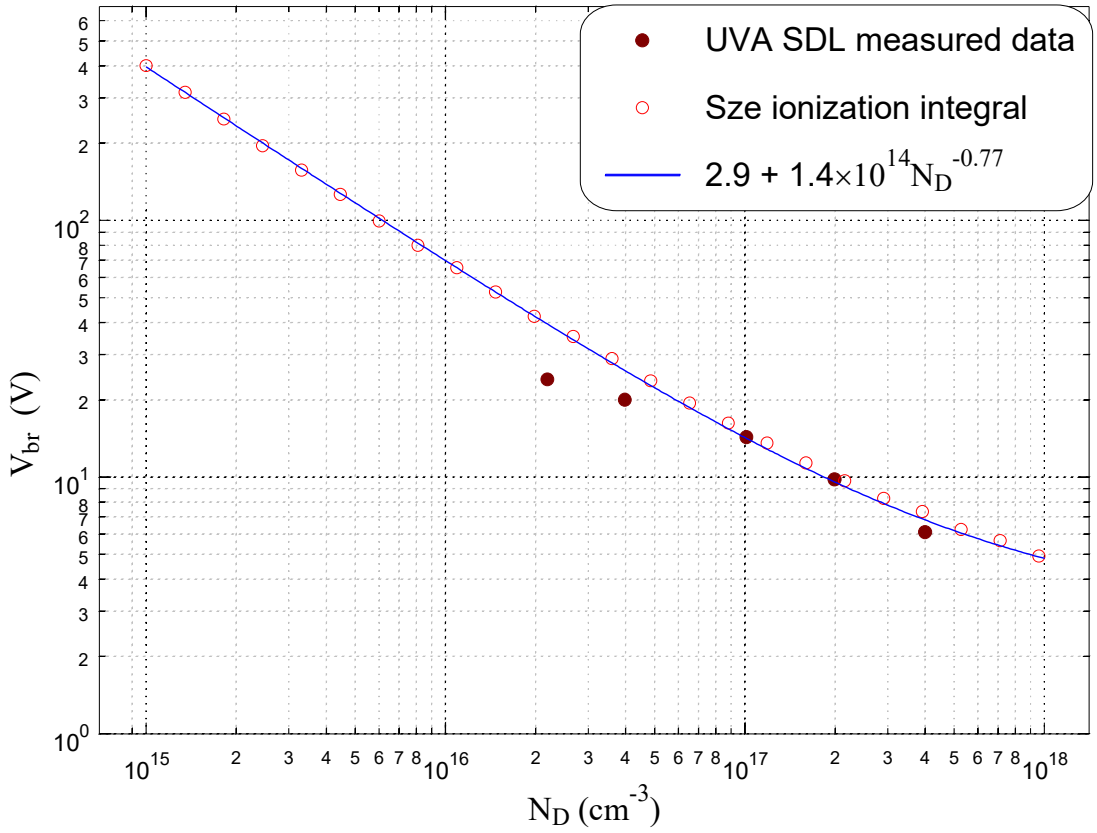


Fig. 3.3. Reverse breakdown voltage versus epitaxial layer doping.

Sze's calculations were based on a perfect abrupt junction p-n interface and should be valid for an ideal metal semiconductor interface. However, edge defects and interface defects can lead to reverse breakdown voltages below those predicted by Sze. There is also empirical evidence suggesting that V_{br} can be lowered by stresses caused by the oxide passivation layer around the anode (see Fig. 3.1) [Sherrill, 1990]. For example, the SB13T1 varactor, doped at 1×10^{17} cm^{-3}, had a measured breakdown voltage at 1 μA in the 8-11 V range with the oxide present and 14.3 V after removal of the oxide layer.

Equivalent Circuit Model

The equivalent circuit model for a planar Schottky varactor is shown in Fig. 3.4. The nonlinear junction resistance, R_j , and nonlinear capacitance, C_j , arise from the Schottky barrier at the metal/epitaxial interface. The series resistance, R_s , arises predominantly from ohmic losses in the epitaxial and buffer layers, but also from ohmic losses in the metals and the ohmic contact. The finger-to-pad capacitance, C_{fp} , pad-to-pad capacitance, C_{pp} , and finger inductance, L_f , arise from the physical geometry of the planar package, as illustrated in Fig. 3.1.

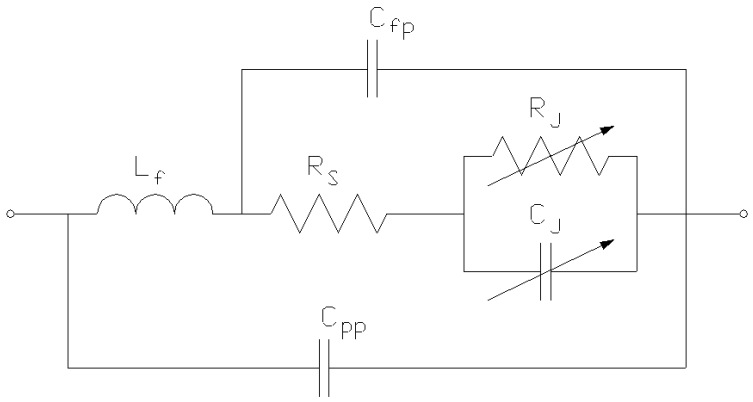


Fig. 3.4. Equivalent circuit for a planar Schottky varactor.

When the device is operated in a varactor mode ($|I_{DC}| << |I_{AC}|$), the junction resistance, R_j , is very large and can be eliminated from the model. Also, the parasitic elements C_{fp} , C_{pp} , and L_f can be treated as part of the linear external circuit, leaving only the nonlinear junction capacitance C_j and the series resistance, R_s , in the varactor equivalent circuit model. It is also possible to include the series resistance as part of the external circuit. However, including the series resistance in the nonlinear device simulations can provide valuable insights when designing planar varactor chips.

Junction Capacitance

The depletion width, shown in Fig. 3.1, can be expressed as,

$$w(V_j) = \sqrt{\frac{2 \cdot \varepsilon_s \cdot (V_{bi} - V_j)}{q \cdot N_D}} \tag{3.3}$$

where $w(V_j)$ is the depletion region width, V_j is the voltage across the Schottky junction, V_{bi} is the built-in voltage, ε_s is the GaAs dielectric permittivity, q is the electron charge, and N_D is the epitaxial layer doping. The charge displaced from the depletion region is given by eq. 3.4, where, $Q(V_j)$ is the charge and A_a is the anode cross-sectional area.

$$Q(V_j) = q \cdot N_D \cdot A_a \cdot \sqrt{\frac{2 \cdot \varepsilon_s \cdot (V_{bi} - V_j)}{q \cdot N_D}} = q \cdot N_D \cdot A_a \cdot w(V_j) \tag{3.4}$$

The nonlinear junction capacitance, $C_j(V_j)$, may be considered as a parallel plate capacitance with voltage dependent plate separation. We can view the plates as being located on either side of the depletion region and separated by the depletion width. Using the expression for the depletion width given in eq. 3.3, $C_j(V_j)$ can be written as,

$$C_j(V_j) = \frac{\varepsilon_s \cdot A_a}{w(V_j)} \cdot \gamma(V_j) = A_a \cdot \gamma(V_j) \cdot \sqrt{\frac{q \cdot N_D \cdot \varepsilon_s}{2 \cdot (V_{bi} - V_j)}} \tag{3.5}$$

The $\gamma(V_j)$ term in eq. 3.5 is a correction to account for fringing fields at the periphery of the epitaxial layer [Copeland, 1970].

$$\gamma(V_j) = 1 + \frac{3 \cdot w(V_j)}{D} \tag{3.6}$$

The zero biased junction capacitance, C_{j0}, is defined as the junction capacitance with zero applied voltage ($V_j = 0$).

$$C_{j0} = A_a \cdot \gamma(0) \cdot \sqrt{\frac{q \cdot N_D \cdot \varepsilon_s}{2 \cdot V_{bi}}} \tag{3.7}$$

There is a second correction to eq. 3.5 that places an upper limit on the junction capacitance near flatband. Eq. 3.5 suggests that the junction capacitance becomes infinitely large near flatband, but measurements show that it peaks just below flatband and then rolls off as V_j is increased [P. H. Siegel et al, 1991]. Eq. 3.5 is based on the depletion approximation which ignores the "tails" in the spatial electron distribution, which become important as the depletion width approaches zero. However, this phenomena is of little consequence in varactor multipliers since high ohmic losses resulting from large forward currents preclude operation near flatband. Fig. 3.5 shows the C-V curve for the SB13T1 varactor with C_{j0} = 130 fF. This C-V curve was calculated using eq. 3.5. A second curve is shown that includes a flatband correction.

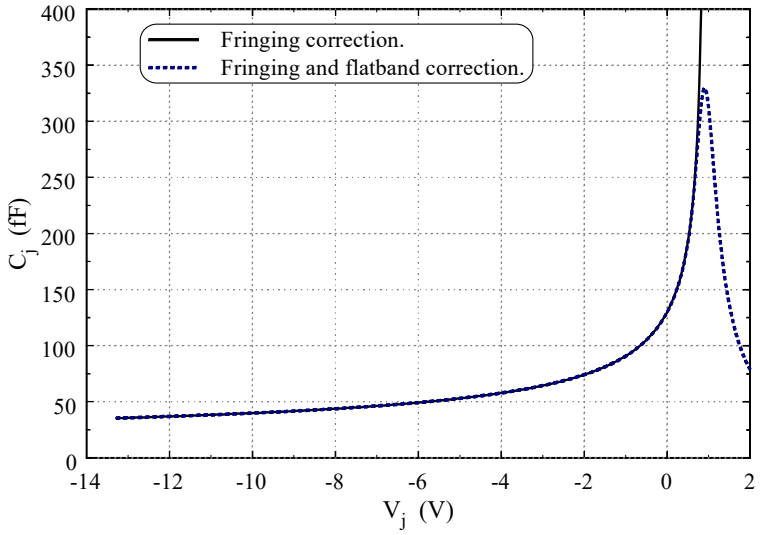


Fig. 3.5. Corrected C-V curves for the UVA type SB13T1 varactor with C_{jo} = 130 fF.

Harmonic balance simulations require that functions for C_j and its first derivative be continuous everywhere. The simple flatband correction of eqs. 3.8 and 3.9 satisfies these requirements. Using these expressions, C_j has a maximum value of $\beta \cdot C_{j0}$ at $V_j = V_{bi}$.

$$C_j(V_j) = \begin{cases} A_a \cdot \gamma(V_j) \cdot \sqrt{\dfrac{q \cdot N_D \cdot \varepsilon_s}{2 \cdot (V_{bi} - V_j)}}, & V_j < \delta \\ A_a \cdot Re\left(\gamma(V_j)\right) \cdot \sqrt{\dfrac{q \cdot N_D \cdot \varepsilon_s}{2 \cdot V_{bi} \cdot \left(\alpha \cdot (V_{bi} - V_j)^2 + \sigma\right)}}, & V_j > \delta \end{cases} \tag{3.8}$$

$$where, \quad \sigma = \left(\frac{1}{\beta}\right)^2, \quad \delta = V_{bi} \cdot (1 - 2 \cdot \sigma), \quad \alpha = \frac{1}{4 \cdot \sigma \cdot V_{bi}^2} \tag{3.9}$$

Series Resistance

The series resistance comprises resistance in the epitaxial layer, spreading resistance in the buffer, resistance in the buffer layer and resistance in the ohmic contacts.

$$R_s = R_{epi} + R_{spread} + R_{buf} + R_{ohmic} \tag{3.10}$$

The resistance of the epitaxial layer varies with depletion width and thus has some degree of nonlinearity. Typically, this nonlinear effect is ignored and the epitaxial layer resistance is calculated at its maximum value (eq 3.11), where t_{epi} and σ_{epi} are the epitaxial layer thickness and conductivity respectively. Eq. 3.11 shows that the epitaxial resistance is directly proportional to the epitaxial thickness. Since R_{epi} is typically the largest single contribution to R_s , t_{epi} should be chosen to be as small as possible with the constraint that t_{epi}

should be larger than the maximum depletion width.

$$R_{epi} = \frac{t_{epi}}{\sigma_{epi} \cdot A_a} = \frac{t_{epi}}{q \cdot A_a \cdot \mu_{epi} \cdot N_D} \tag{3.11}$$

A commonly used empirical formula for the electron mobility in high purity GaAs is given by eq. 3.12.

$$\mu = \frac{10^4}{1 + \sqrt{\frac{N_D}{10^{17}}}}, \qquad \left(\frac{cm^2}{V \cdot s}\right) \tag{3.12}$$

The conductivity is given by,

$$\sigma = q \cdot \mu \cdot N_D \tag{3.13}$$

The spreading resistance, given by eq. 3.14, arises from ohmic losses occurring in the buffer layer directly beneath the anode where electrons spread out from the two dimensional epitaxial/buffer interface into the three dimensional buffer layer. A rigorous examination of this phenomena is given by [Dickens, 1967], [Champlin, 1978].

$$R_{spread} = \frac{1}{4 \cdot \pi \cdot \delta_{buf} \cdot \sigma_{buf}} \tag{3.14}$$

The resistance of the buffer layer in the semi-cylindrical region between the outer radius of the anode and the inner radius of the ohmic contact is given by eq. 3.15.

$$R_{buf} = \frac{1}{2 \cdot \pi \cdot \delta_{buf} \cdot \sigma_{buf}} \cdot ln\left(\frac{r_{oc}}{r_a}\right) \tag{3.15}$$

The buffer layer skin depth, δ_{buf}, is given by eq. 3.16. For discussions on the skin effect, see [Pozar, 1990], [Collin, 1992].

$$\delta_{buf} = \frac{1}{\sqrt{\pi \cdot f \cdot \mu_0 \cdot \sigma_{buf}}} \tag{3.16}$$

If the buffer layer thickness, t_{buf} , is less than the skin depth, δ_{buf} , then t_{buf} should replace δ_{buf} in eq. 3.15. The equation for R_{buf} tends to underestimate the resistance because not all of the electrons transfer from the buffer to the metal at radius r_{oc}. This error can be corrected using a value slightly larger than r_{oc} in the equation [Bhaumik, 1992]

Ohmic contact resistivity is typically in the range of 10^{-6}-10^{-5} Ω·cm^2. Calculations of R_{ohmic} may underestimate the resistance if the full ohmic contact area is used since the current is not spread evenly over the interface [Bhaumik, 1992]. The ohmic contacts for the varactors used in the balanced doublers were constrained to be large enough so that R_{ohmic} was negligible (typically less than 0.2 Ω). However, at higher frequencies this may not always be possible.

Higher Order Effects

Two higher order effects can adversely affect the performance of multipliers operating at high frequencies. One of these is the resonance between inertial effects in the conduction electrons (inductive) and the displacement of the valence electrons (capacitive). This is known as plasma resonance and the resonant frequency is given by eq. 3.17,

$$\omega_p = q \cdot \sqrt{\frac{N_D}{m_0 \cdot m_e \cdot \varepsilon_s}} = 2 \cdot \pi \cdot f_p \tag{3.17}$$

where, N_D is the doping and $m_0 \cdot m_e$ is the effective electron mass [Champlin et al, 1978]. Typically, plasma resonance is not a problem for varactor multipliers since f_p is

approximately 950 GHz for an epitaxial doping of 1×10^{16} cm^{-3} and rises to 3 THz for an epitaxial doping of 1×10^{17} cm^{-3}.

The second effect is known as velocity saturation. This phenomenon is of more concern since it may occur at lower frequencies. For low electric fields in GaAs, the steady-state, average electron velocity, v, is proportional to the low field mobility, μ.

$$\bar{v} = \mu \cdot \bar{E} \tag{3.18}$$

However, eq. 3.18 does not hold for high electric fields. The average electron drift velocity reaches a maximum value, v_{max}, and then rolls off as the field increases [Sze, 1985], [Shur, 1990]. The maximum average electron velocity in GaAs is approximately 2×10^5 m/s. Most nonlinear circuit simulators implicitly assume that the average electron velocity is governed by eq. 3.18 for all electric field magnitudes and thus often yield optimistic solutions. Velocity saturation sets a limit on the peak value of current in the varactor given by eq. 3.19 [Kollberg et al, 1992].

$$I_{sat} = q \cdot N_D \cdot A_a \cdot v_{max} \tag{3.19}$$

Results from nonlinear device simulations must be checked to ensure that the simulated peak current does not exceed I_{sat} . If this happens, our philosophy is to increase the epitaxial doping. If this approach proves impractical, a simulator which includes velocity saturation effects should be used [Jones, 1995].

3.3 Planar Varactor Design

This section describes the design process for varactors employed in the 40/80 GHz and 80/160 GHz doublers and provides guidelines for the design of other planar varactor chips. A

variety of graphs present data based on the equations in section 3.2 and the nonlinear analyses of [Penfield and Rafuse, 1962], [Siegel et al, 1983], and [Hewlett-Packard (MDS), 1994]. Most of the graphs are based on single varactor analysis, so the designer must multiply these quantities by the number of varactors on the chip being designed. The procedure used to design the UVA type SB13T1 varactor is used as an example.

The first step in the design process is to choose the input and output frequencies and the desired output power and bandwidth. These decisions are tempered by the availability of a suitable source to drive the frequency multiplier with sufficient power over the desired bandwidth. For the design of the SB13T1, there was approximately 200 mW of available power in the 35-45 GHz band from various Klystrons and a Gunn oscillator in the lab. Given this constraint on the available input power to the doubler, the goal was to maximize the doubler output power in the corresponding 70-90 GHz band.

Power Handling

The next step is to match the input power requirements of the varactor chip to the available pump power. This is done by adjusting the number of anodes, the anode diameter and the epitaxial doping. There are many solutions to the power equation, but most will fail to satisfy other important requirements such as adequate heat dissipation or frequency response. The maximum input power for a given anode size and doping is easily found using the analysis of Penfield and Rafuse. The Penfield-Rafuse analysis considers only the nonlinear capacitance and series resistance shown in the equivalent circuit model in Fig. 3.4. Also, this analysis considers only the fundamental and second harmonics. However, the results from the

Penfield-Rafuse analysis are usually found to be within 10% of the values predicted by multi-tone harmonic balance simulations.

The data plotted in Fig. 3.6 shows that for a given anode size, power handling in a varactor can be increased by lowering the epitaxial layer doping. Since this relationship may not be intuitive, further analysis is provided in appendix B. The input powers shown in Fig. 3.6 are the values required to achieve maximum efficiency when the doubler is presented with the optimum embedding impedances. The varactor can be pumped at higher power levels and achieve higher output powers, but the efficiency will roll off due to the increase in R_s and R_j.

Decreasing the epitaxial doping increases power handling, but also increases series resistance which may result in higher power dissipation and higher operating temperatures.

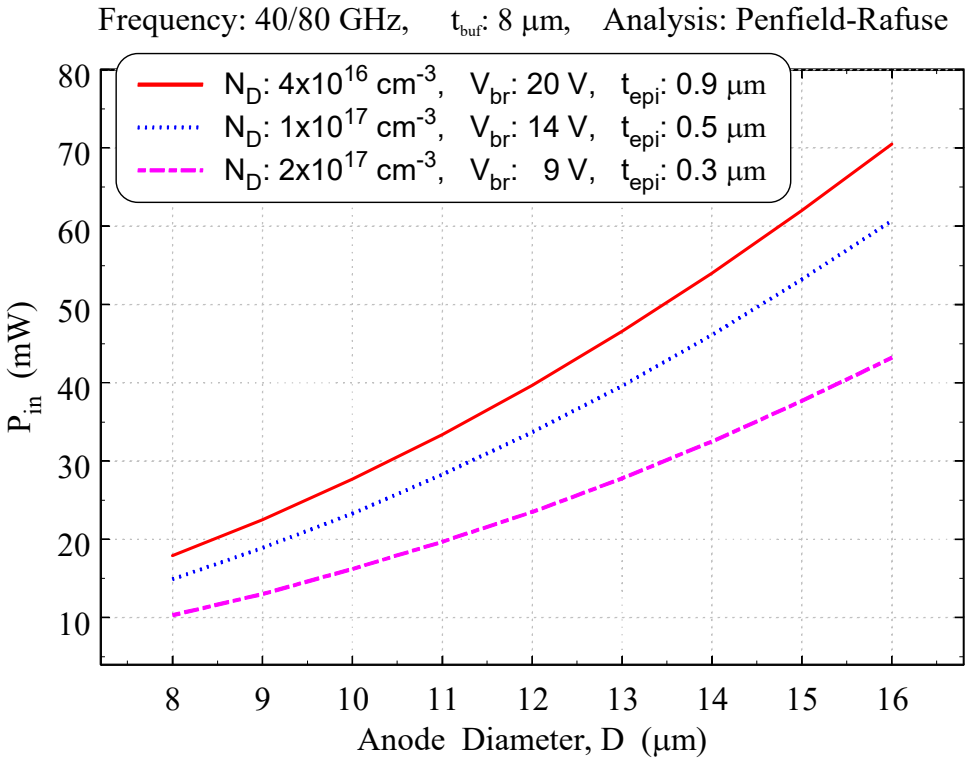


Fig. 3.6. Maximum input power per anode for optimum efficiency.

Fig. 3.7 shows that the dissipated power per anode increases as the doping decreases or the anode size increases. The relationship between dissipated power and doping for a given input power level is somewhat more complex.

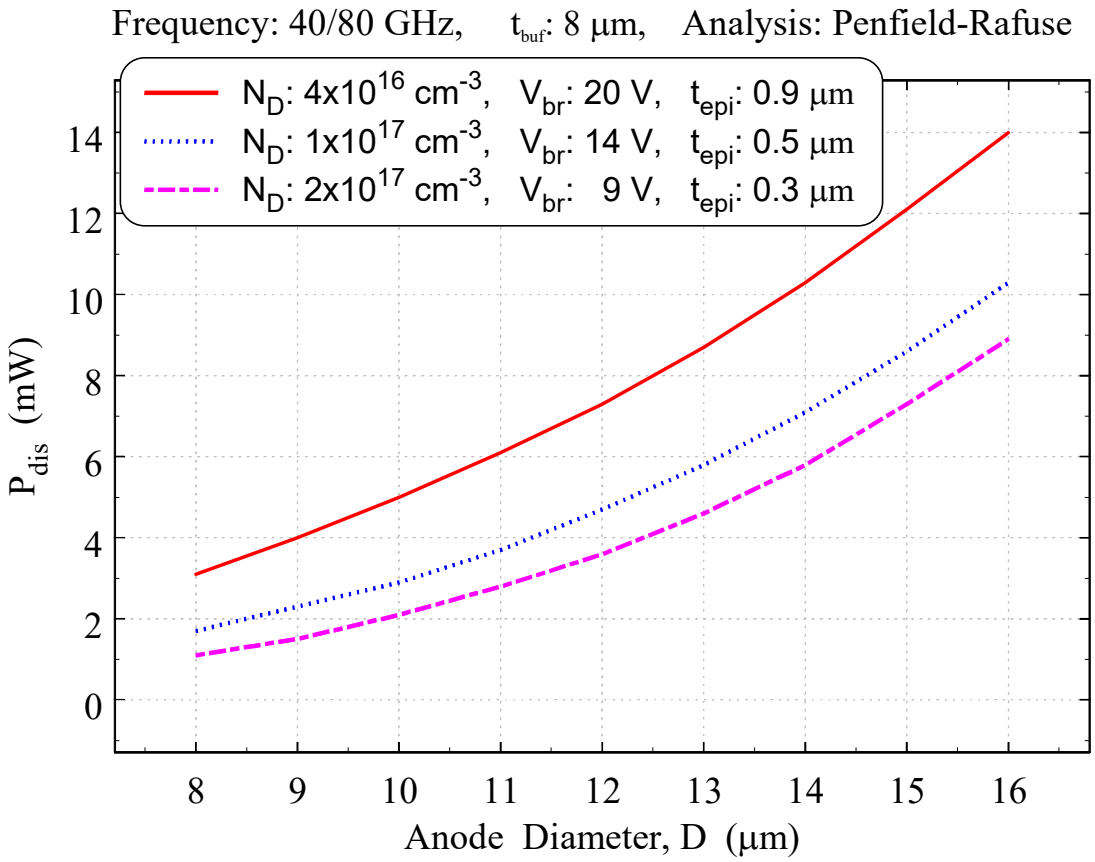


Fig. 3.7. Dissipated power per anode versus anode diameter.

Table 3.1 contains several combinations of anode size, number of anodes and doping for an input power level of 200 mW. The table also shows the series resistance per anode and the dissipated power per anode. It is interesting to note that the 1×10^{17} cm^{-3} epitaxial material yielded the smallest levels of dissipated power in all cases shown.

Table 3.1. Several ways to achieve 200 mW varactor designs at 40/80 GHz.

Number of anodes	D (μm)	N_D (cm^{-3})	R_s (Ω)	P_{dis} (mW)
6	11.0	4×10^{16}	2.8	6.0
6	11.9	1×10^{17}	0.9	4.5
6	14.2	2×10^{17}	0.5	5.9
4	13.5	4×10^{16}	2.0	9.4
4	14.6	1×10^{17}	0.7	7.8
4	17.2	2×10^{17}	0.4	11.0

Fig. 3.6 shows that for a given epitaxial doping, larger anodes can handle more power. However, optimum embedding impedances are inversely proportional to anode size and there are practical limits on the range of impedances that can be matched. Fig. 3.8 shows the optimum embedding impedances for a 40/80 GHz doubler using 1×10^{17} cm^{-3} doping.

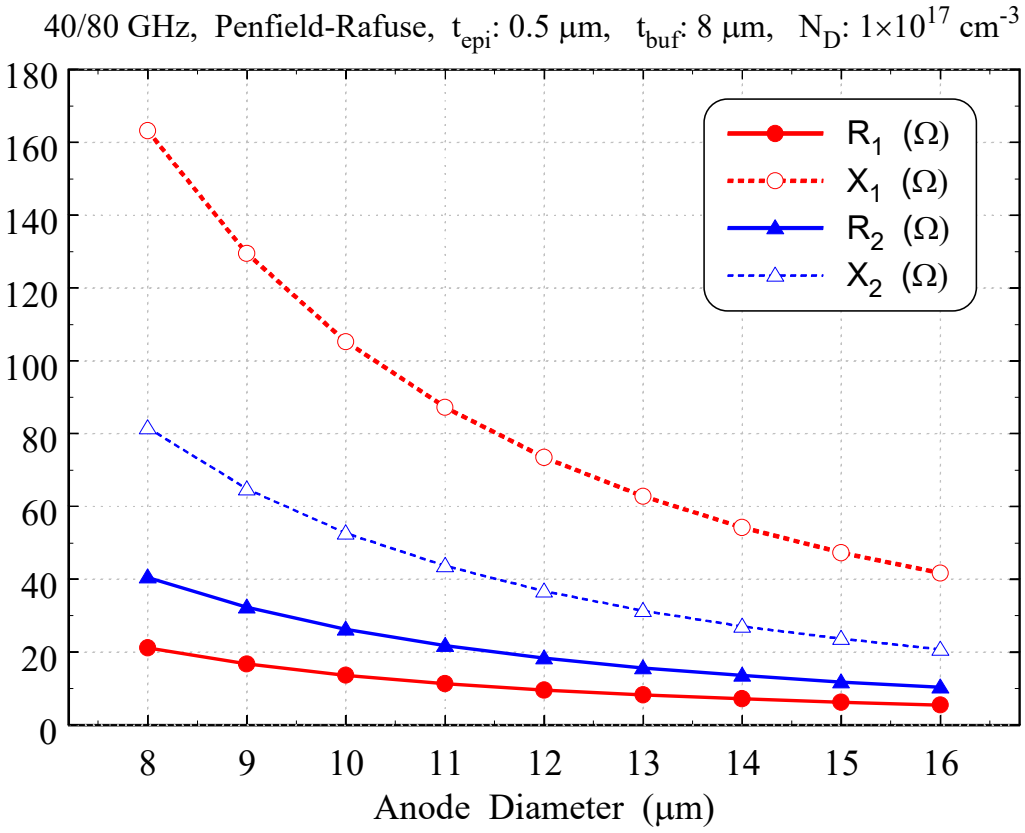


Fig. 3.8. Optimum embedding impedances for 40/80 GHz and $1x10^{17}$ cm^{-3}.

In the course of this work, it was observed that eqs. 3.20 and 3.21 can be used to obtain a rough estimate of the optimum embedding impedances. If the average junction capacitance is C_{avg} , the input embedding impedance is $R_1 + jX_1$ and the output embedding impedance is $R_2 + jX_2$, then

$$X_1 \sim \frac{1}{\omega_0 \cdot C_{avg}}\ , \quad X_2 \sim \frac{1}{2 \cdot \omega_0 \cdot C_{avg}}\ , \quad R_1 \sim \frac{X_1}{7}\ , \quad R_2 \sim \frac{X_2}{2} \tag{3.20}$$

$$C_{avg} \sim \frac{1}{V_{br}} \cdot \int_0^{-V_{br}} C_j \cdot dV_j \tag{3.21}$$

Physical Constraints

Increasing the number of anodes to allow higher input power levels is appealing. This has the added benefit of spreading out the heat generation over a broader area of the chip. However, there are constraints placed on the size of the varactor chip by the external circuit. The constraints imposed by the circuit will be a function of frequency and the types of transmission lines used. In the case of the 40/80 GHz and 80/160 GHz doublers, the constraint is imposed by the input waveguide height. Also, to avoid creating a resonant dielectric cavity the width and thickness of the chip is constrained to be much less than a half wavelength of the output frequency.

Epitaxial and Buffer Layer Thickness

The resistance of the epitaxial and buffer layers are typically the largest contributors to the series resistance and their contributions should be minimized by choosing appropriate

values for t_{epi} and t_{buf} .The epitaxial layer thickness should be greater than the depletion width at V_{br} to avoid punch-through and to maximize power handling. However, t_{epi} should be as thin as possible to minimize the series resistance. Fig 3.9 shows the depletion width at the reverse breakdown voltage.

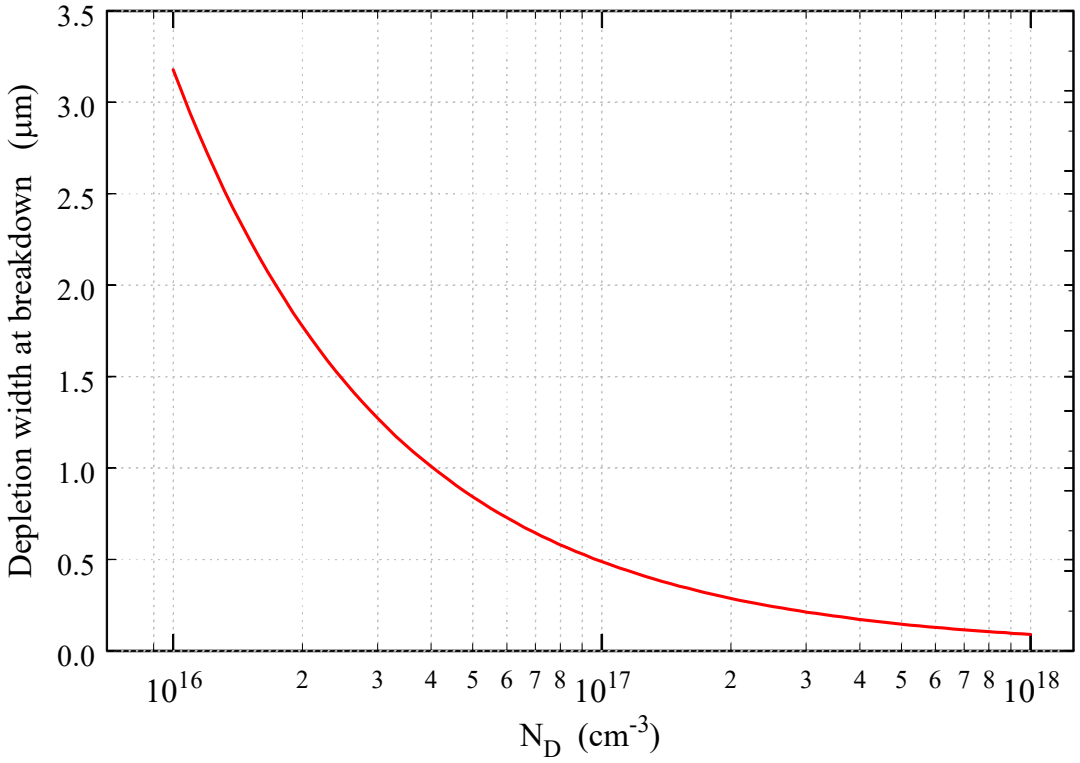


Fig. 3.9. Depletion width at breakdown versus epitaxial doping.

Buffer doping levels in the 5×10^{18} cm^{-3} range are commercially available in GaAs and should be chosen as high as possible to minimize the series resistance. The buffer thickness should be greater than a skin depth at the input frequency, but thicknesses greater than 8 µm are difficult to grow in GaAs. This limitation has the greatest impact at lower frequencies where the skin depth is larger. Fig. 3.9 shows plots of skin depth versus frequency for several doping levels.

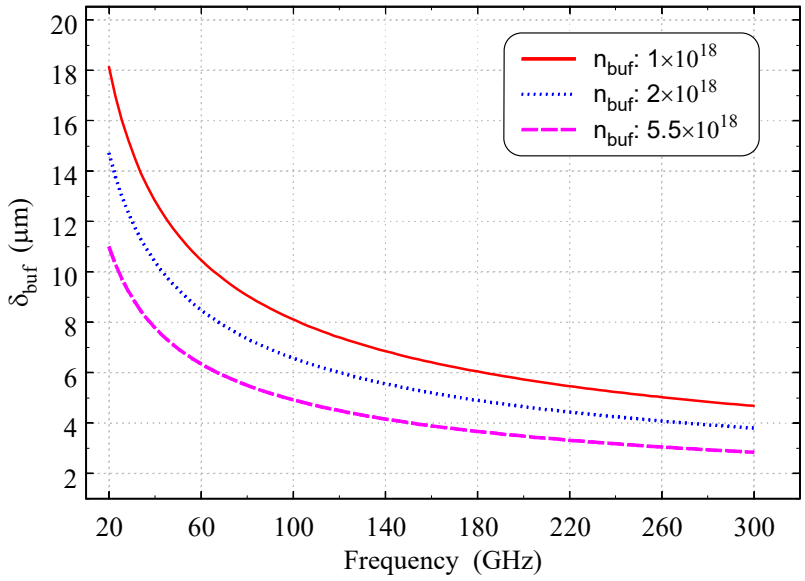


Fig. 3.10. Skin depth versus frequency for three doping levels.

SB13T1 Varactor

The SB13T1 varactor, shown in Fig. 3.11, was designed for the 40/80 GHz doubler. This chip comprises a linear array of 6 varactors with an epitaxial layer doping of $1x10^{17}$ cm^{-3} and a buffer layer thickness of 8 μm. The finger lengths are 50 μm, the ohmic contact pads are 3200 μm^2, and the semi-insulating GaAs substrate is 75 μm thick. The overall chip dimensions are 800x90x75 μm. Three versions of the SB13T1 chip were fabricated with anode diameters of 12, 13 and 14 μm. The calculated series resistance is 0.8 Ω per varactor (13 μm anodes) and the reverse breakdown voltage is measured to be 14.3 V.

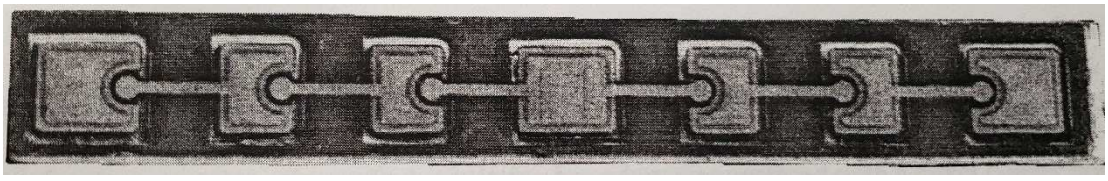


Fig. 3.11. Scanning electron micrograph of the UVA type SB13T1 varactor.

The velocity saturation current, I_{sat} , was calculated to be greater than 400 mA. Harmonic balance simulations for the SB13T1 varactor indicated peak currents of approximately 90 mA at an input power level of 200 mW, indicating that velocity saturation is not a problem in this design.

Thermal Analysis of the SB13T1

Heat is generated in Schottky varactors due to power dissipation in the series resistance. Most of the heat is generated in or near the epitaxial layer since R_{epi} typically represents the largest contribution to the series resistance. In this analysis, the heat is modeled as a point source located in the epitaxial layer. This procedure should somewhat overestimate the ambient temperature near the anodes. A detailed description of the analysis is provided in Appendix C.

A value of 7 mW per anode was used in the analysis although the dissipated power per anode was calculated to be closer to 5 mW at an input power level of 200 mW (see Fig. 3.7). The quartz substrate is made from fused silica which has a poor thermal conductivity of approximately 1.4 $W \cdot m^{-1} \cdot K^{-1}$. For this reason, the simulation was run with a perfect insulating boundary condition at the center of the varactor chip, ie. no heat flowed out from the center mounting pad to the external circuit. Under these constraints, the peak temperature was calculated to be 90° C at the anode closest to the center pad.

If a substrate with a better thermal conductivity were used (such as Z-cut crystalline quartz), then the heat conduction path would be significantly improved. The simulation was run for the case where the perfect insulating boundary was replaced with a direct connection

to an infinite heat well at T_0 = 27° C. Under these conditions, the peak temperature was calculated to be 44°C.

3.4 Summary

Section 3.2 showed a nonlinear circuit model for a planar varactor and provided equations governing the individual circuit components. Section 3.3 presented some basic guidelines for designing a planar varactor chip by analyzing the behavior of the nonlinear circuit as a function of the varactor design parameters.

A flow chart summarizing the design procedure is shown in Fig. 3.12. For MMW and SMMW multipliers, the goal is usually to obtain as much output power as possible. The output power is constrained by the available pump power and the efficiency of the multiplier. Once the available input power is determined, a suitable combination of epitaxial doping, number of anodes and anode size is chosen. These choices must be tempered by an evaluation of the required embedding impedances, dissipated power levels in the series resistance and higher order effects such as velocity saturation and plasma resonance which can adversely impact the multiplier performance.

The epitaxial layer thickness and buffer layer thickness depend on the epitaxial doping and input frequency respectively. To minimize series resistance in the buffer layer, the buffer doping is chosen to be the highest value available commercially. The physical geometry of the varactor chip is constrained by the external embedding circuit and by the output frequency.

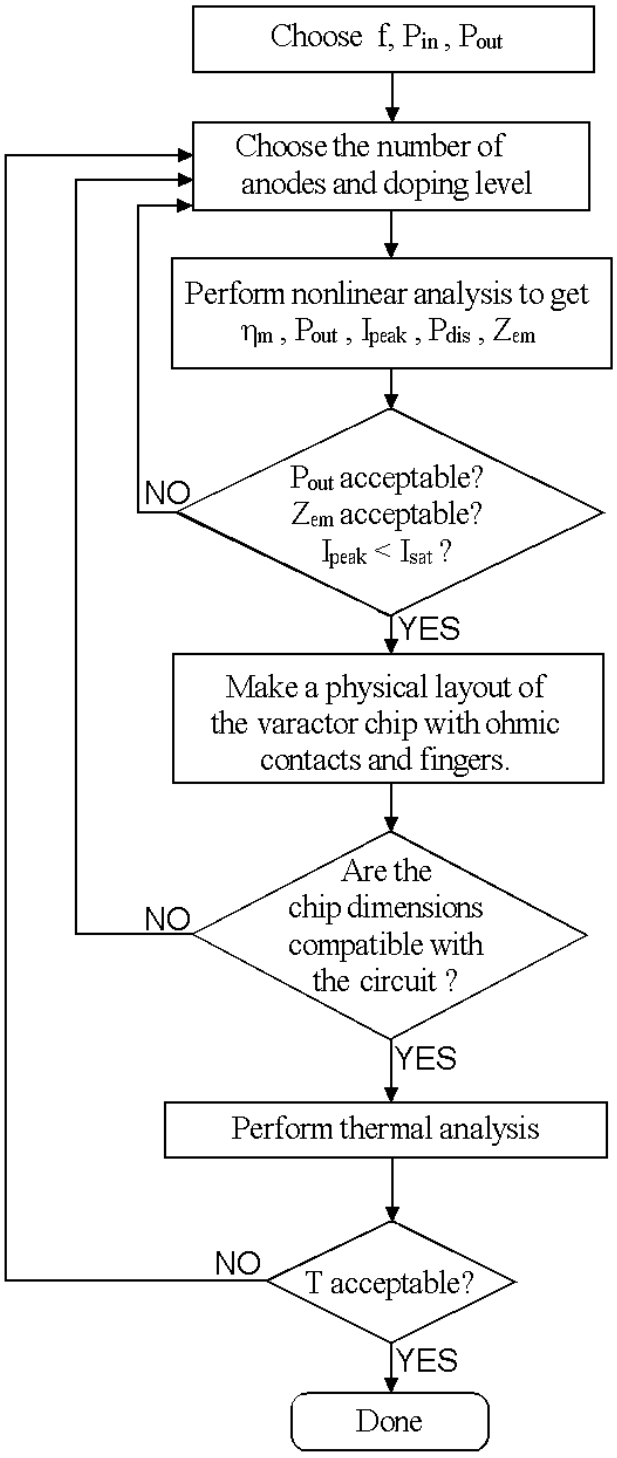


Fig. 3.12. Planar varactor design flow chart.

Chapter 4

Circuit Design

4.1 Overview

This chapter shows how the linear embedding circuits for the 40/80 GHz and 80/160 GHz doublers were designed. The primary design tools were Hewlett-Packard's High Frequency Structure Simulator (HFSS) and Microwave and RF Design Systems (MDS). Section 4.2 provides a brief overview of HFSS and its implementation of the finite element analysis (FEA). For a more in depth discussion on FEA, refer to [Hewlett-Packard, 1997], [Salazar-Palma et al, 1998].

Section 4.3 shows how HFSS and MDS were used to design the input circuits for the doublers. Section 4.4 shows a similar analysis for the output circuit design. The design of the DC bias filter, output waveguide probe, and the reduced-height to full-height output waveguide transition are the subjects of Sections 4.5, 4.6, and 4.7. A summary of the embedding impedance simulations is given in Section 4.8.

4.2 High Frequency Structure Simulator (HFSS)

HFSS uses a finite element analysis (FEA) to solve for the electromagnetic fields everywhere inside an arbitrary three dimensional structure. In FEA, an arbitrary 3-D space is divided into many smaller tetrahedral regions. The individual tetrahedra comprise four equilateral triangles. Thus, at defined plane boundaries and at planar material interfaces, a two dimensional mesh of equilateral triangles exists. Magnetic and electric fields are

calculated within the tetrahedra by interpolating data from the vertices of the tetrahedra. The data for the vertices comes from the tangential and normal vector fields at the three edges of the tetrahedron. In this manner, Maxwell's equations are transformed into matrix equations and solved numerically. The final solution for the 3-D structure is in the form of an N-port scattering matrix.

Since the field solutions are in matrix form, the analysis inherently requires a large amount of computer memory. The memory required for the matrices used in the solution of even moderately sized 3-D models can easily exceed 256 MB. When the computer runs out of RAM and begins using disk swap space, the solution time can increase dramatically. The total time required for the solution depends on the speed of the computer, the amount of RAM available, the physical size of the structure in relation to the wavelength of the solve frequency, and the aspect ratio of the smallest to largest feature in the model.

Since the size of the matrices is directly proportional to the physical size of the model, it is advantageous to minimize the model size. This is done by subdividing the original model into several smaller structures, solving the smaller structures, and then recombining the S-parameters in a microwave simulator such as MDS. Symmetric models can often be reduced in size by splitting the structure with electric or magnetic walls, but caution must be used since physical symmetry alone is not a sufficient criterion. The conditions that must exist at all points on a plane to justify a magnetic or electric wall are given by eqs. 4.1 and 4.2, where $\hat{n}$ is the unit normal to the surface. An in-depth discussion on how magnetic and electric walls were used in the balanced doubler simulations is given in Sections 4.3 and 4.4.

$$\hat{n} \times \bar{E} = 0, \ for\ an\ E - wall \tag{4.1}$$

$$\hat{n} \times \bar{H} = 0, \ for\ an\ H - wall \tag{4.2}$$

Ports

Ports are a special type of boundary used in HFSS to excite and absorb EM fields in a 3-D model. The user need only specify the plane for the port and set the number of modes. Typically, each physical port in the 3-D model is assigned to have a single mode. HFSS analyzes the port geometry, determines the field distribution for the dominant mode, and calculates the characteristic impedance and complex propagation constant of a transmission line with the same cross-section as the port. Only EM fields in that mode can be absorbed or excited at the port boundary and all fields orthogonal to the mode are reflected. If, for example, only one port is defined in the model and the number of modes for that port is set by the user to N, then the results of the HFSS analysis is an N-port scattering matrix [S]. Thus, even though there exists only one physical port, HFSS treats the model as though there were N electrical ports. The n^{th} electrical port, n = 1..N, in the scattering matrix corresponds to the scattered fields of the n^{th} mode of the port.

Since EM fields in modes orthogonal to those defined for a port are reflected at the port boundary, it is imperative that these modes be included in the port definition if they are excited by sources or physical discontinuities in the model. Alternatively, one may choose a port geometry that only supports a single propagating mode and extend the port some distance away from the nearest discontinuity along a uniform transmission line with a cross-section identical to the port. The length of this section should be sufficient so that

evanescent modes at the discontinuity decay before reaching the port. After solving the model, the S-parameters can be de-embedded back to the discontinuity.

Probes

Ports can be attached to small probes within a 3-D model to determine the driving point impedances at any location. This technique was used extensively in the design of the input and output embedding circuits of the balanced doublers by placing probes at each varactor anode as illustrated in Fig. 4.1. The circular cross-section of the anode metal at the finger is extended into the buffer layer to within a very short distance of the semi-insulating substrate. A cylindrical volume with a radius slightly larger than the anode is removed from the buffer layer as well. Since the buffer layer has a high conductivity, the result is an air filled coaxial line with the center conductor extending to the bottom of the finger. The port is defined at the end of the coaxial line at plane AA'.

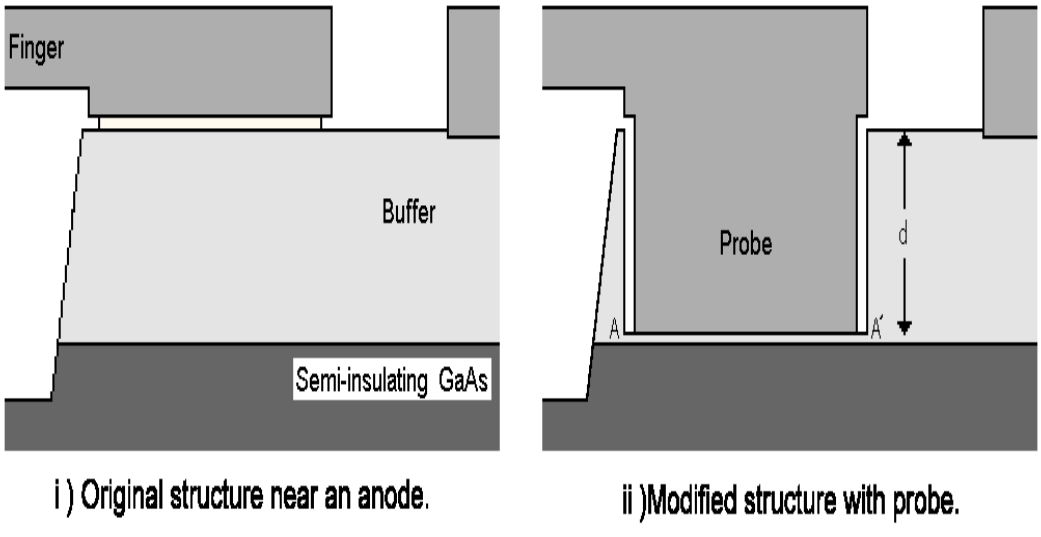


Fig. 4.1. Geometry for an HFSS planar varactor anode probe.

HFSS does not support enclosed ports, so each port in the device must be in contact with the outside world (this may change with future versions). This problem was overcome in the planar varactor doubler models by tunneling through the conducting portions of the structure as illustrated in Fig. 4.2. HFSS treats all boundaries with the outside world as perfectly conducting surfaces unless the user specifically gives an alternative boundary condition. For example, when the bond-wire is subtracted from the waveguide, the interior of the bond-wire becomes part of the outside world and the surface of the bond-wire becomes a perfect conductor. This procedure is repeated, in the order shown in Fig. 4.2, until all of

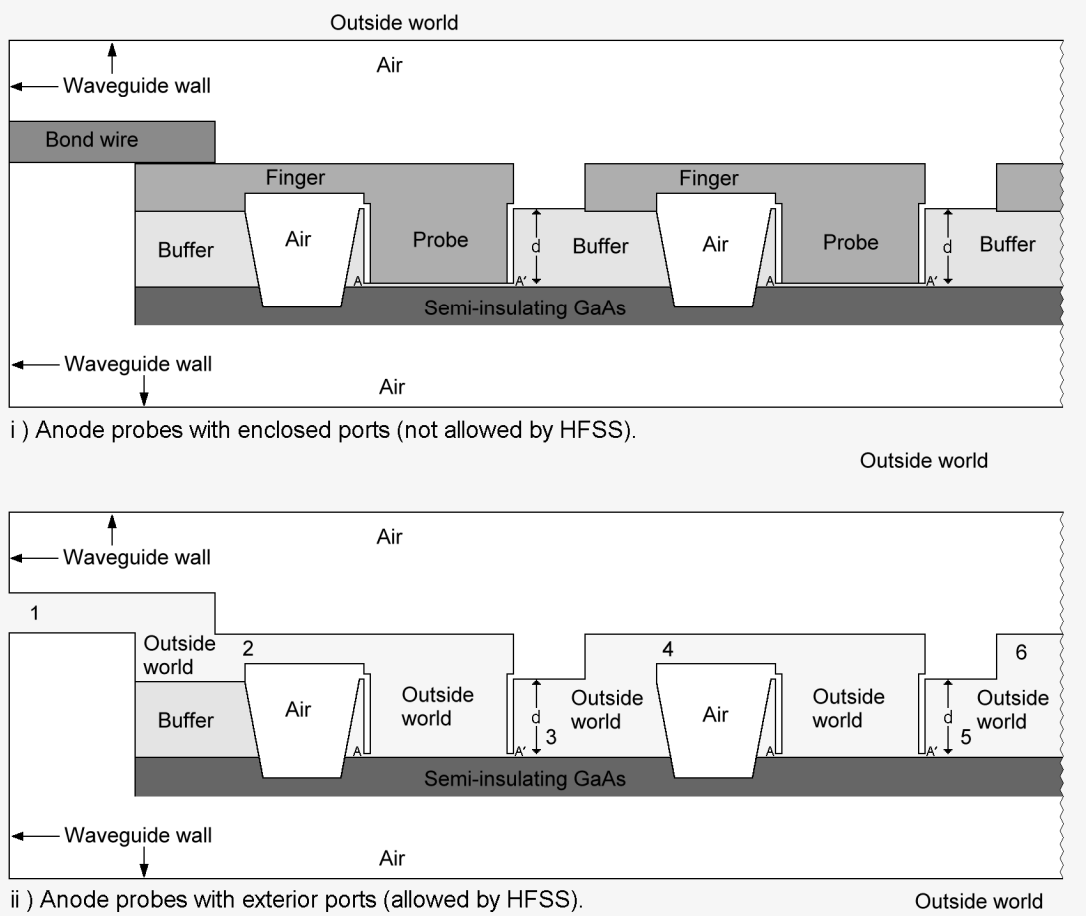


Fig. 4.2. Probes for a multiple anode varactor in HFSS.

the conducting materials in the varactor chip (buffer and metals) have been subtracted from the model. The order of the subtraction is important since each element to be subtracted from the model must border the outside world. The final step is to define ports at the planes labeled AA'.

Interpretation of the HFSS Data

The output from an HFSS simulation is in the form of a generalized scattering S-matrix. The S-matrix gives the scattered waves at the port planes when each port in the model is connected to the outside world with transmission lines having the same geometries as the ports. The S-matrix is not normalized to a single characteristic impedance. HFSS allows the user to renormalize the S-parameters before exporting them in Touchstone, Compact, or Citifile formats. This is an important consideration since many microwave simulators implicitly assume that imported S-matrices are normalized to 50 Ω.

HFSS allows the user to select one of three characteristic impedance definitions for an arbitrary port geometry and the renormalizing impedance for the port. The three impedance definitions used by HFSS are Z_{pi}, Z_{pv}, and Z_{vi}. Definitions for these characteristic impedances are given below.

$$Z_{pi} = \frac{P}{|I|^2} \tag{4.3}$$

$$Z_{pv} = \frac{VV^*}{P} \tag{4.4}$$

$$Z_{vi} = \sqrt{Z_{pi}\, Z_{pv}} \tag{4.5}$$

$$P = \oint_s \bar{E} \times \overline{H^*} \cdot \overline{ds} \tag{4.6}$$

$$|I| = \frac{1}{2} \oint_l \left| \overline{H} \cdot \bar{d}l \right| \tag{4.7}$$

$$V = \int_l \bar{E} \cdot \bar{d}l \tag{4.8}$$

The Z_{pi} characteristic impedance definition relates the power passing through a cross-section of a transmission line to the z-directed currents on the conducting surfaces. The Z_{pv} characteristic impedance definition relates the power passing through a cross-section of a transmission line to the voltage across the line. However, the calculation of the voltage, V, in eq. 4.8 requires that the user specify an impedance line for the integration. Thus HFSS cannot calculate Z_{pv} or Z_{vi} unless the impedance line is specified by the user. Values for Z_{pi} are always calculated since the power and currents are always known.

4.3 Input Circuit Design

There are few design parameters for the input circuit topology of the 40/80 GHz and 80/160 GHz doublers, but these parameters allow a wide range of tuning for the input frequency embedding impedances. The permittivity of the quartz circuit and GaAs substrate have a strong influence on the input embedding impedances, but their dimensions are known since the dimensions of the GaAs chip are determined in the varactor design phase, the

width of the quartz circuit is determined by the reduced-height waveguide and the quartz thickness is simply chosen at a reasonable value that provides sufficient mechanical strength.

Most of the remaining input circuit design parameters are shown in Fig. 4.3. The input waveguide width, a, is determined by the input frequency range since it sets the dominant TE_{10} mode cutoff frequency. The width, c, needs to be sufficiently small to cut off the input TE_{10} mode. The exact value has a stronger influence on the output matching circuit. The remaining dimensions are the waveguide height, b, the distance from the varactors to the TE_{10} cutoff plane, d, and the distance from the varactor chip to the full-height input waveguide, e. These three dimensions have a strong impact on the input circuit embedding impedance and almost no impact on the output frequency embedding impedance.

Another tuning element was used in the balanced doublers that is not shown explicitly in Fig. 4.3. The length of the bond wires that run from the gold mounting pads on the quartz circuit to the waveguide block was extended by milling out a small rectangular section in the waveguide block. The cross-section of this milled out volume is small

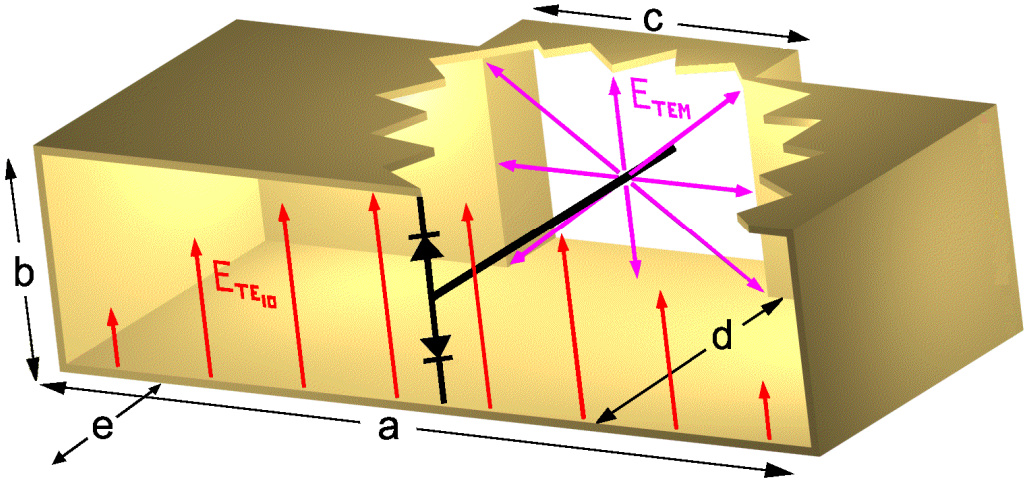


Fig. 4.3. Conceptual sketch showing the input circuit design parameters.

compared to the waveguide dimensions. Therefore, it has little effect on the embedding impedances except to add series inductance due to the increased length of the bond-wire. This added inductance is also seen at the output frequency and thus affects the output embedding circuit. In a doubler, the optimum input embedding impedance tends to have an inductive reactance that is roughly twice the optimum value for the output frequency. Thus, the bond-wire length is chosen as a compromise value.

The real part of the optimum embedding impedances for most varactors is much less than the characteristic impedance of the waveguide. Thus, it is beneficial to reduce the waveguide height as much as possible near the varactors. In this work, a varactor was designed using the criterion set forth in Chapter 3, reasonable dimensions were sketched for the varactor chip, and the waveguide height was set to a value slightly larger than the chip length.

The remaining unknowns are the distance from the varactors to the TE_{10} cutoff plane, d, the distance from the varactors to the full-height input waveguide, e, and the length of the bond-wires. The next step is to create an HFSS model of the varactor chip and circuit inside the reduced-height waveguide as shown in Fig. 4.5. To reduce the solve time, the model is split with an E-wall at b/2 as indicated in Fig. 4.4.

A magnetic wall at a/2 cannot be used due to the asymmetry caused by the quartz circuit and varactor chip. For the 40/80 GHz doubler, ports 1-3 were defined at the varactor anode probes (SB13T1). Port 4 was defined at the end of the bond-wire. Ports 5 and 6 were defined in the reduced-height waveguide at a suitable distance from the varactor chip.

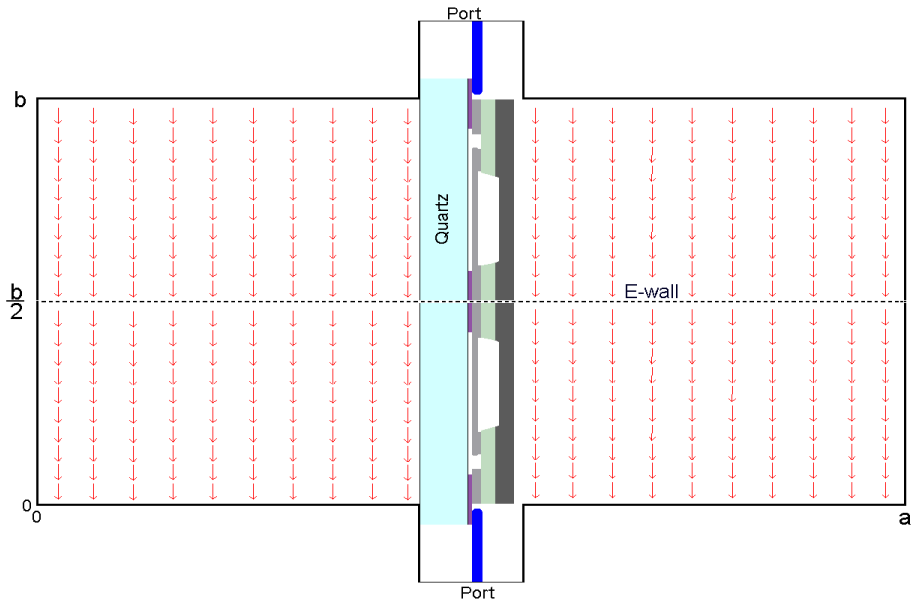


Fig. 4.4. Conceptual sketch of the cross-section of an HFSS input circuit model showing the TE_{10} E-field, E-wall and bond-wire ports.

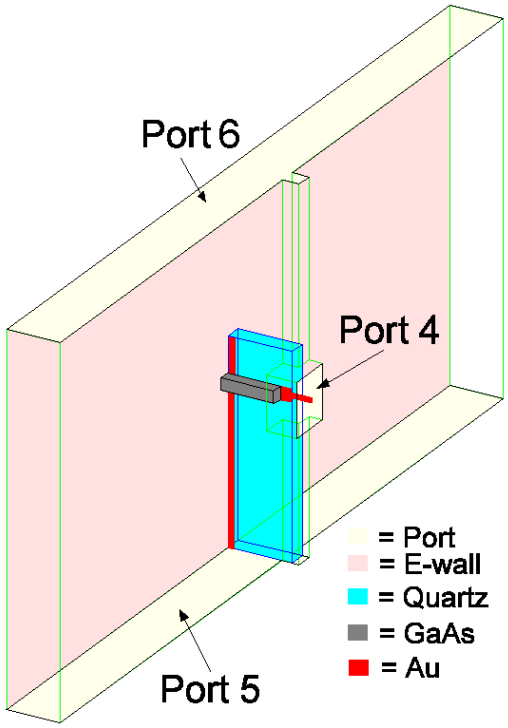


Fig. 4.5. HFSS input circuit model for the 40/80 GHz doubler.

An adaptive analysis and frequency sweep of the HFSS model was performed, the S-parameters de-embedded and renormalized, and the results saved to a Touchstone, Citifile, or SuperCompact file and imported to a microwave simulator such as Hewlett-Packard's MDS. In MDS, ideal transmission lines were attached to the waveguide and bond-wire ports of the S-parameter model as indicated in Fig. 4.6. The characteristic impedance and propagation constant of these lines were set equal to those of the corresponding ports in the original HFSS model. The characteristic impedances correspond to those used in the renormalization of the S-parameters.

The anode probe ports were attached in parallel to an MDS S-parameter source so they could be driven in phase. The resulting reflection coefficient of the parallel connection was used to compute the average embedding impedance. A full-height WR-22 input waveguide impedance was attached to the other end of the transmission line on port 6. A short was placed at the end of the transmission line attached to the bond-wire port (port 4) because the bond-wire terminates in a short to the waveguide block. Another short was placed at the end of the transmission line attached to the other reduced-height waveguide port (port 5) to model the TE_{10} mode cutoff. Simulations were run to determine the

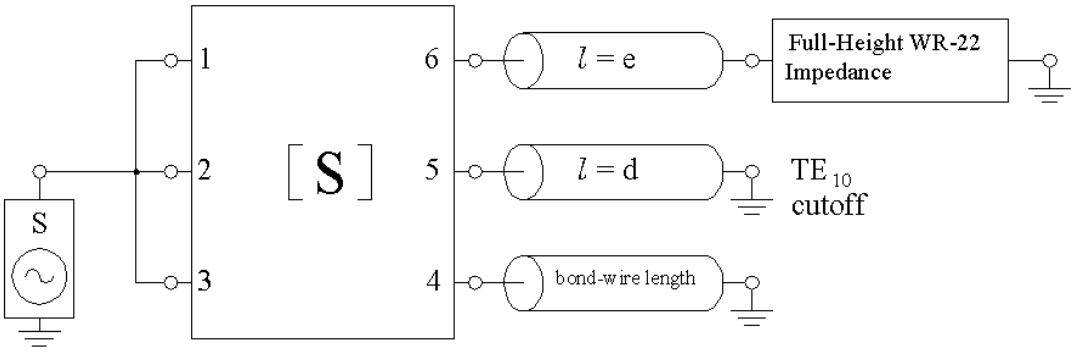


Fig. 4.6. MDS input circuit model for the 40/80 GHz doubler.

transmission line lengths that gave the optimum embedding impedances in the desired frequency range. These results were verified with HFSS simulations on a model that had the actual waveguide discontinuities at the locations determined in MDS.

Simulations run on the model in Fig. 4.6 yield an average embedding impedance for the three anodes. This simple model drives all of the varactors in phase and allows a quick and easy calculation of the embedding impedance. The spread in the individual embedding impedances was examined by attaching separate small-signal AC sources to each of the three anode ports. The sources were driven in phase and the impedances were calculated by monitoring the voltage and current at the anode ports. For the 40/80 GHz doubler, the spread in the embedding impedances for the six anode SB13T1 varactor was found to be negligible. An HFSS model of a varactor with eight anodes was also examined (4 anodes in the half-space model), but the spread in the impedances was more pronounced and this design was rejected in favor of the six anode design. A four anode chip design was never attempted for the 40/80 GHz doubler because of the low value of the real part of the required embedding impedances predicted in the nonlinear simulations (~5 Ω).

The final input circuit simulation results for the 40/80 GHz and 80/160 GHz balanced doublers are presented in the summary in Section 4.8. The final circuit design represents one possible solution to the impedance matching problem. More elaborate matching structures could be used on the full-height input waveguide side of the model as long as the evanescent TM_{11} mode fields are sufficiently attenuated.

4.4 Output Circuit Design

The output circuit design procedure was very similar to that used for the input circuit. Since the varactor, quartz, and waveguide dimensions (a, b, d, e, shown in Fig. 4.3) are fixed, the only remaining parameters to be adjusted are the center conductor dimensions on the quartz circuit and the waveguide width, c. In the region between the varactor chip and the TE_{10} cutoff plane, the center conductor perturbs the input frequency TE_{10} mode. However, if the center conductor is relatively small (approximately 2/3 of the waveguide height or less), then the effect on the input embedding impedances is negligible. In the suspended microstrip region, the waveguide block and center conductor dimensions effect only the output embedding impedance.

The electric wall at b/2 used to divide the input model was replaced with a magnetic wall in the output model (see Fig. 4.8). The reduced-height input waveguide supports several propagating modes at the output frequency that do not satisfy the magnetic wall boundary conditions (TE_{10}, TE_{20}, and TE_{30}). However, these modes are not excited due to the symmetry of the varactors and the waveguide discontinuities. Thus, the magnetic wall boundary conditions are not violated. There are also an infinite number of evanescing modes excited by the varactors, including the TM_{11}, but they do not violate the magnetic wall boundary conditions. Fig. 4.7 shows the electric field vectors for the TE_{10}, TE_{20}, TE_{11}, and TM_{11} modes for rectangular waveguide. The TEM mode E-fields look similar to the TM_{11}.

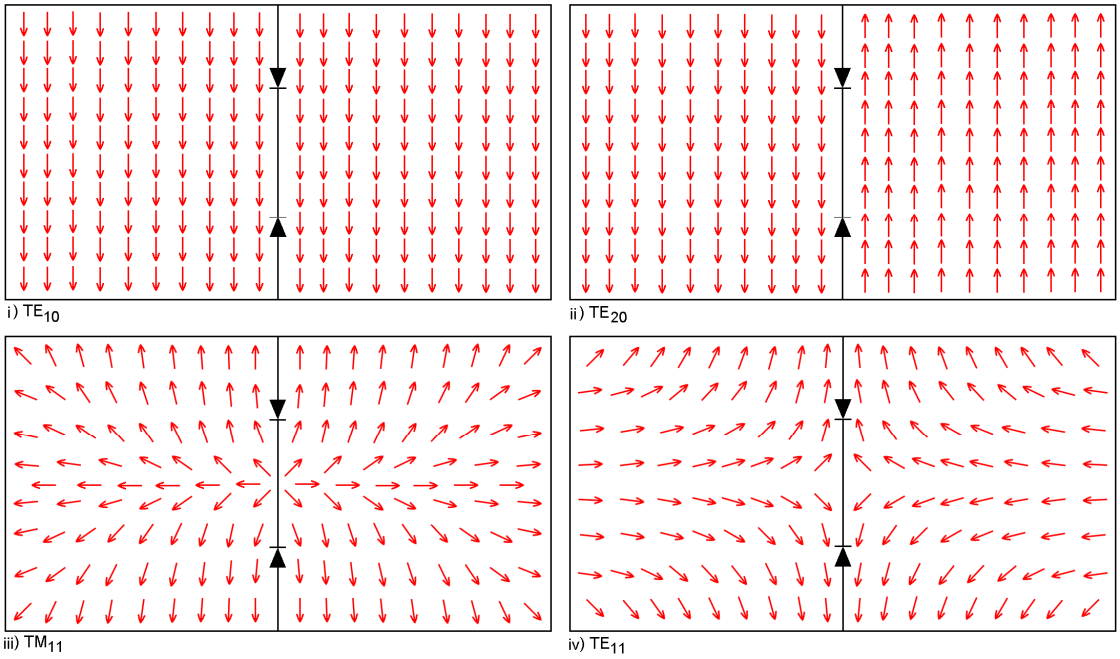


Fig. 4.7. Electric fields for the waveguide modes, i) TE_{10}, ii) TE_{20}, iii) TM_{11}, iv) TE_{11}.

The HFSS output circuit model, shown in Fig. 4.9, is a modified version of the input circuit model. The input port of the reduced-height waveguide is eliminated because no propagating modes are supported without the center conductor. However, the reduced-height input guide length is kept long enough to sufficiently attenuate evanescent modes before they reach the perfectly reflecting boundary at the edge of the model space. Fig. 4.8 shows a conceptual sketch of the cross-section of a full HFSS model prior to the split.

The results from the HFSS simulations are exported to MDS. In MDS, ideal transmission lines are attached to the waveguide and bond-wire ports of the S-parameter model and the anode probe ports are attached to an S-parameter source. The length of the transmission line on the bond-wire port is constrained to have the same physical length used in the input circuit simulation. Since the length of the bond-wire perturbs the embedding

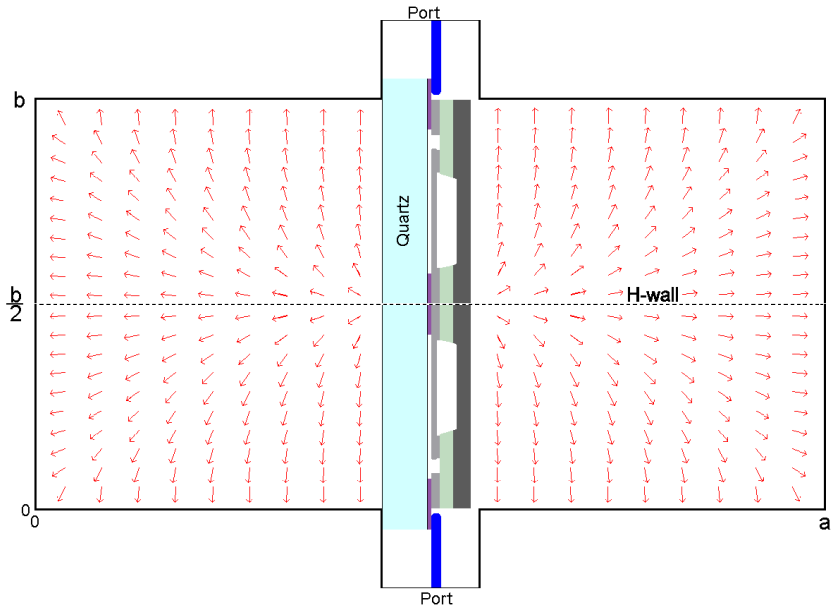


Fig. 4.8. Conceptual sketch of the cross-section of an HFSS output circuit model showing the TEM E-field, H-wall and bond-wire ports.

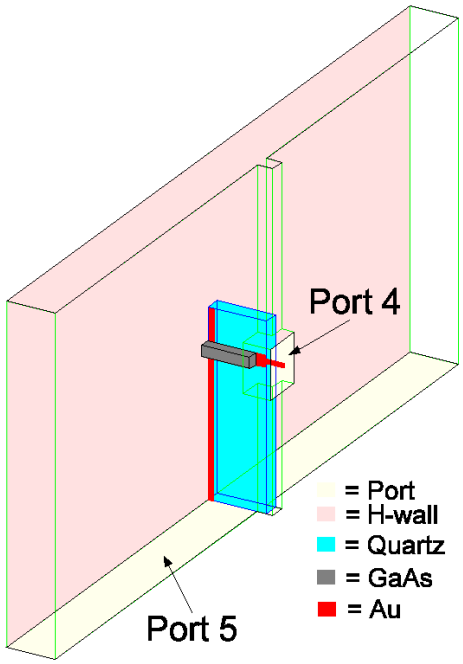


Fig. 4.9. HFSS output circuit model for the 40/80 GHz doubler.

impedances at both the input and output frequencies, the input and output circuit models have to be run interactively in MDS to obtain a final bond-wire length that gives the best tradeoff in performance.

A series of transmission lines attached to the reduced-height waveguide (Port 5) simulate variations in the width of the center conductor. The electrical lengths and characteristic impedances of these lines are constrained to realistic values. The range of attainable impedances in this region are largely determined by the center conductor width, the reduced waveguide height, b, and the reduced waveguide width, c. The width, c, is set large enough so that small perturbations caused by machining tolerances do not significantly perturb the characteristic impedances of the suspended microstrip line. A range of realizable values is obtained from HFSS using port solves with varying center conductor widths. In the quasi-coaxial region between the diodes and the TE_{10} cut-off plane, the range of attainable characteristic impedances is approximately 50-190 Ω. In the suspended microstrip region, the characteristic impedances range from 30-160 Ω. Characteristic impedances outside of the specified ranges are possible but require the center conductor to be either very narrow (and lossy) or very wide and close to the waveguide walls. Fig. 4.10 shows the MDS output circuit model.

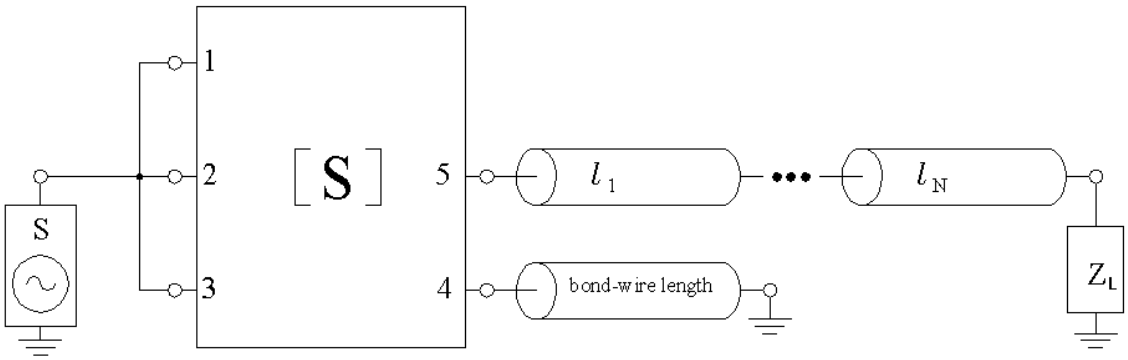


Fig. 4.10 MDS output circuit impedance matching model.

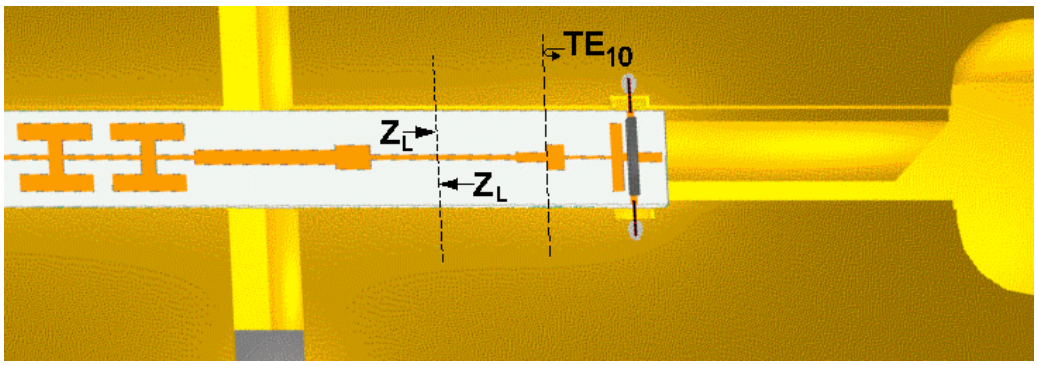


Fig. 4.11. Split in the HFSS output model.

In this work, the output model is split along the suspended microstrip section as indicated in Fig. 4.11. The output waveguide probe model and output impedance matching model can then be solved separately by introducing a fixed load impedance, Z_L , in the MDS circuits. This technique greatly simplifies the matching problem. The fixed impedance at the split is constrained to a reasonable value for the suspended microstrip geometry. The value used for Z_L, has a significant impact on the bandwidth of the microstrip-to-waveguide transition. Values near 100 Ω are used for the 40/80 GHz and 80/160 GHz doublers.

The final output circuit simulation results for the 40/80 GHz and 80/160 GHz balanced doublers are presented in Section 4.8. Again, these designs represent only one possible solution to the impedance matching problem.

4.5 DC Bias Filter

The hammer-head filter shown in Fig. 4.12 is used to block RF signals on the DC bias line. Hammer-head filters have much higher RF rejection than simple high/low impedance filters of comparable dimensions. The unit cell size is approximately a quarter wavelength. The exact dimensions of the various features are initially set arbitrarily and

adjusted based on successive HFSS simulation results. The final simulation results are shown in Fig. 4.13.

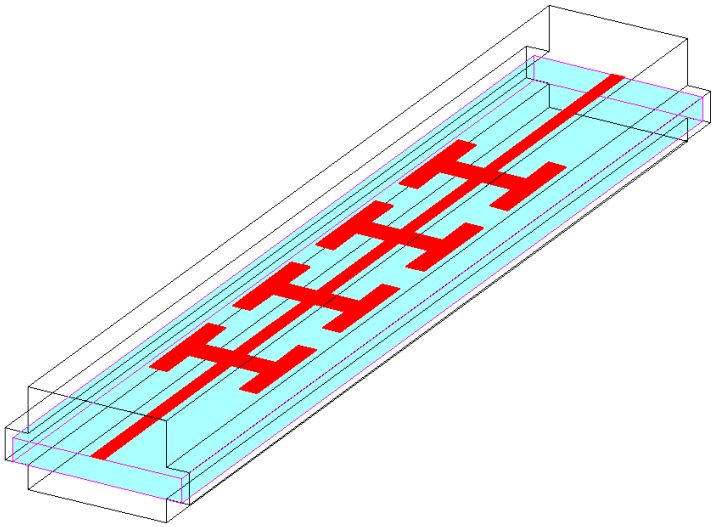


Fig. 4.12. Hammer-head RF filter.

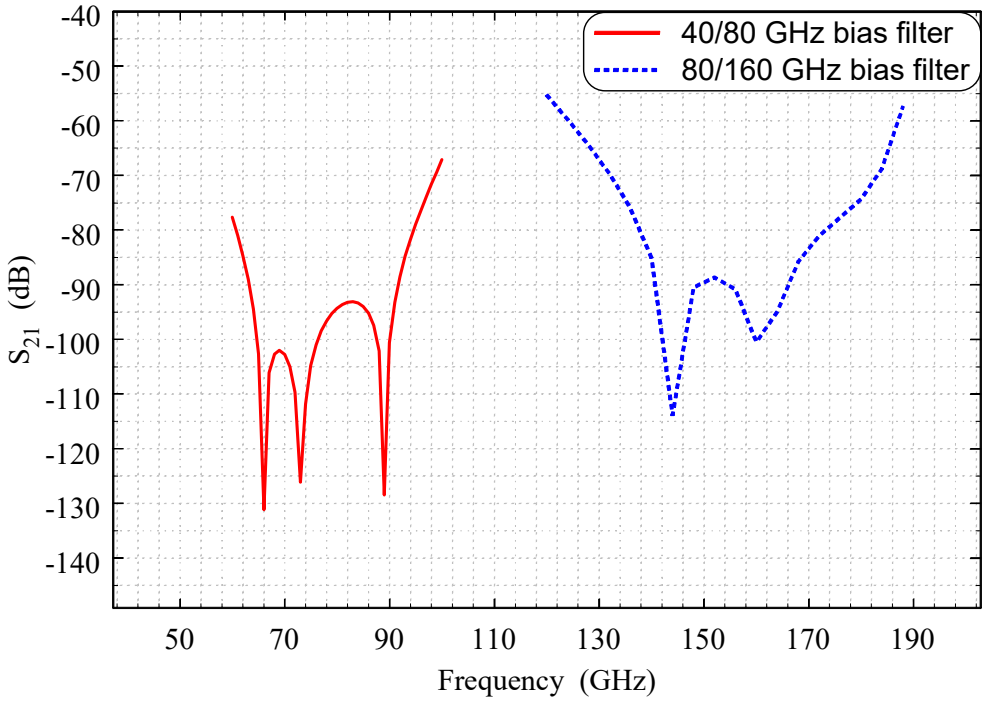


Fig. 4.13. Hammer-head filter simulation results.

4.6 Microstrip-to-Waveguide Transition

The HFSS model for the microstrip-to-waveguide transition (output waveguide probe) is shown in Fig. 4.14. Port 1 is defined in reduced-height output waveguide and Port 2 is defined in the suspended microstrip that leads to the varactors. The use of reduced-height waveguide results in a much broader bandwidth for the transition. Initially, the fixed backshort is replaced with a port so the optimum position can be determined in MDS using a variable length transmission line. Also, the initial HFSS models do not include the hammer-head filter but rather a second microstrip port. Again, a variable length transmission line is connected to this port in MDS to determine the optimum location for a short or open circuit. This data is compared to the hammer-head filter simulation to determine the exact location for the hammer-head filter.

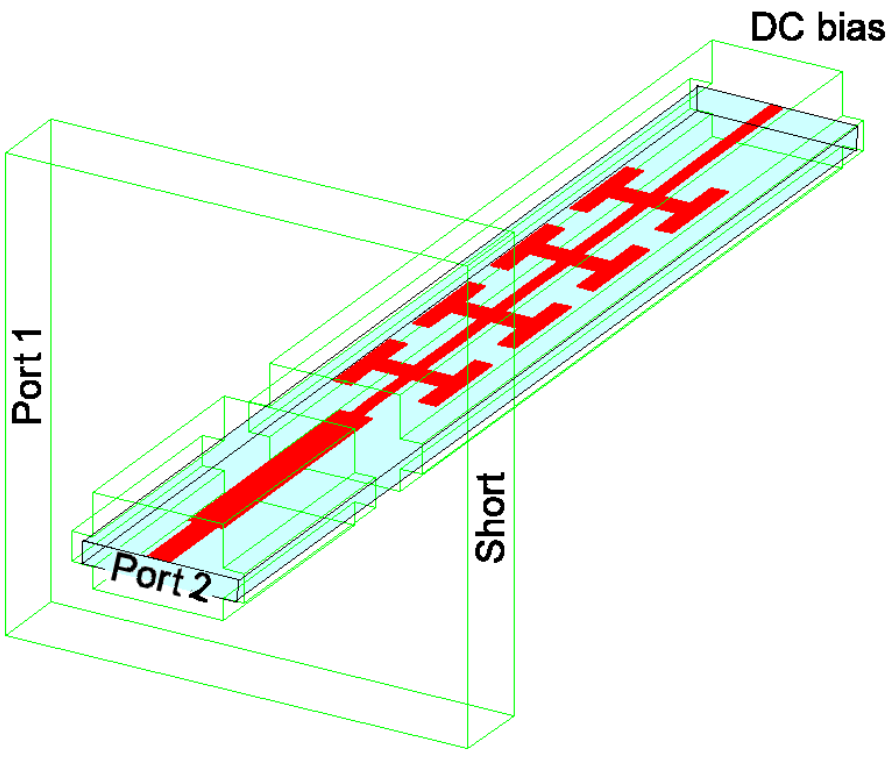


Fig. 4.14. HFSS output probe model.

Fig. 4.15 shows the simulation results for the two port HFSS model with fixed backshort and hammer-head filter. In order to significantly reduce the solve time for the HFSS model, lossless conductors and dielectric materials were used. Therefore, the values of insertion loss shown in the graph are lower than expected for the actual transition.

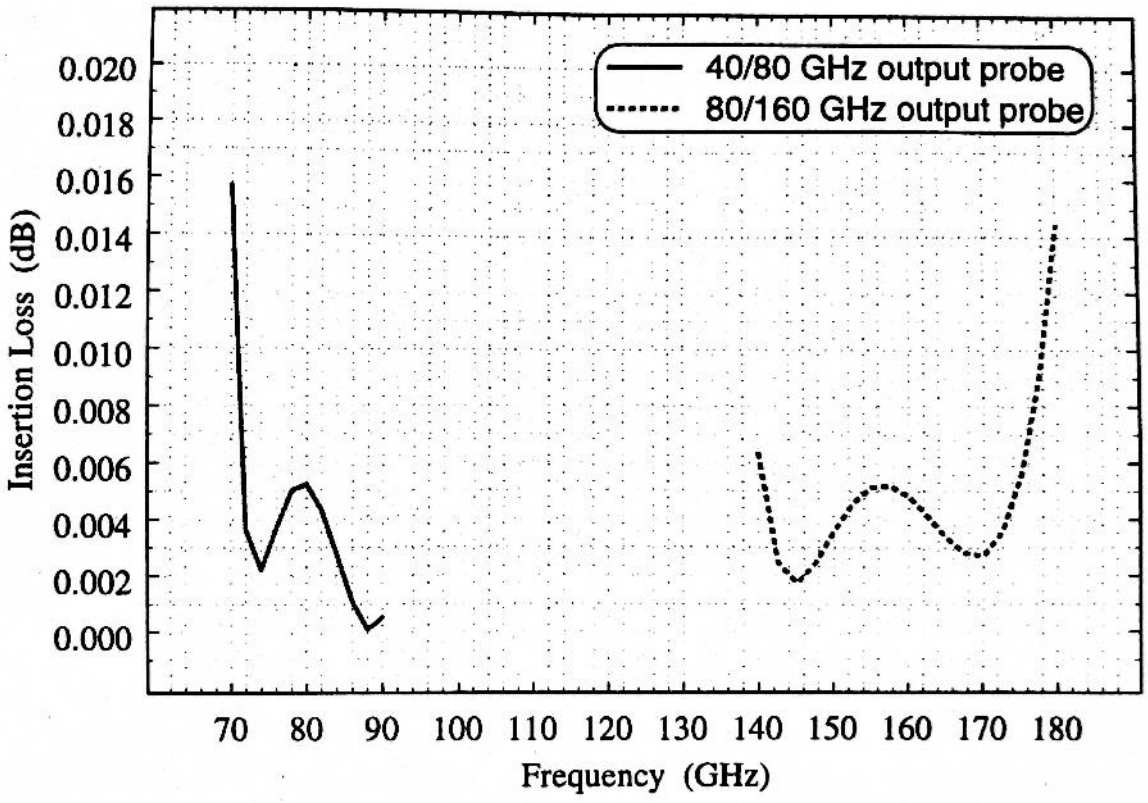


Fig. 4.15. Simulated insertion loss for the output waveguide probes.

4.7 Linear Waveguide Taper

A linear waveguide taper is used to transition from reduced-height waveguide near the probe to full-height output waveguide. Linear tapers are not the optimum waveguide transitions (they take up more space than some other transitions require), but they are easy to design and machine, and have excellent electrical properties if the transition is at least several wavelengths long. The minimum dimensions for the waveguide blocks are constrained by the size of the flanges and the placement of the alignment pins and screws. The blocks did not have to be enlarged to accommodate the linear output waveguide taper. The simulation results for the linear tapers used in the 40/80 GHz and 80/160 GHz doublers is shown in Fig. 4.16. Perfect conductors are used in the simulations and thus the actual insertion loss of the transition is higher due to ohmic losses.

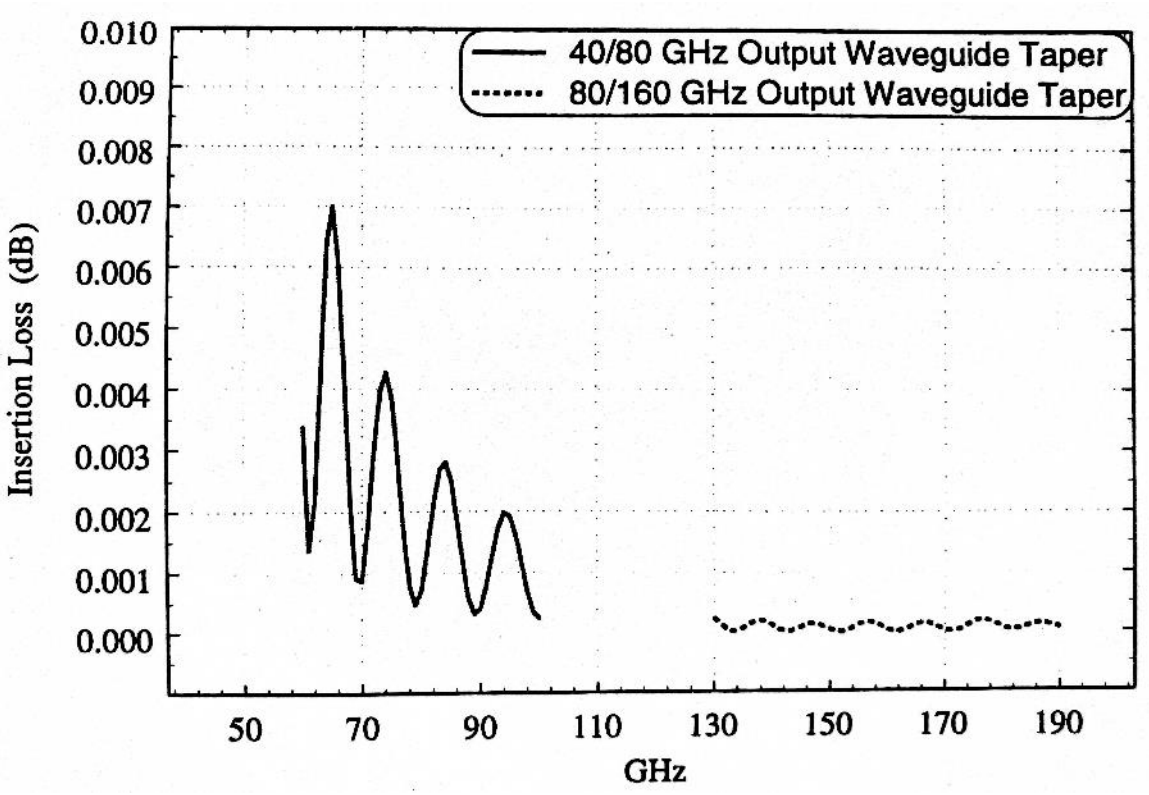
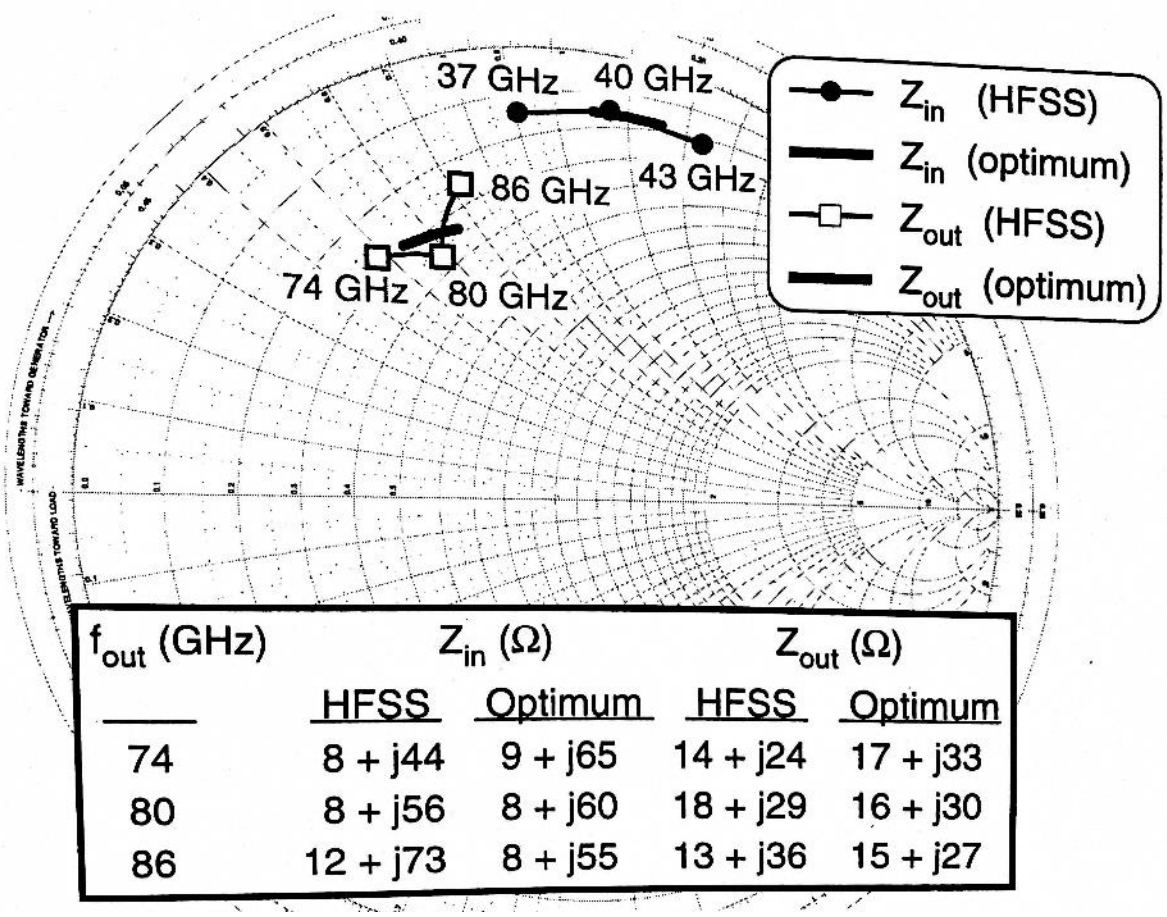


Fig. 4.16. Simulation results for the output waveguide linear tapers.

4.8 Final Embedding Impedance Simulation Results

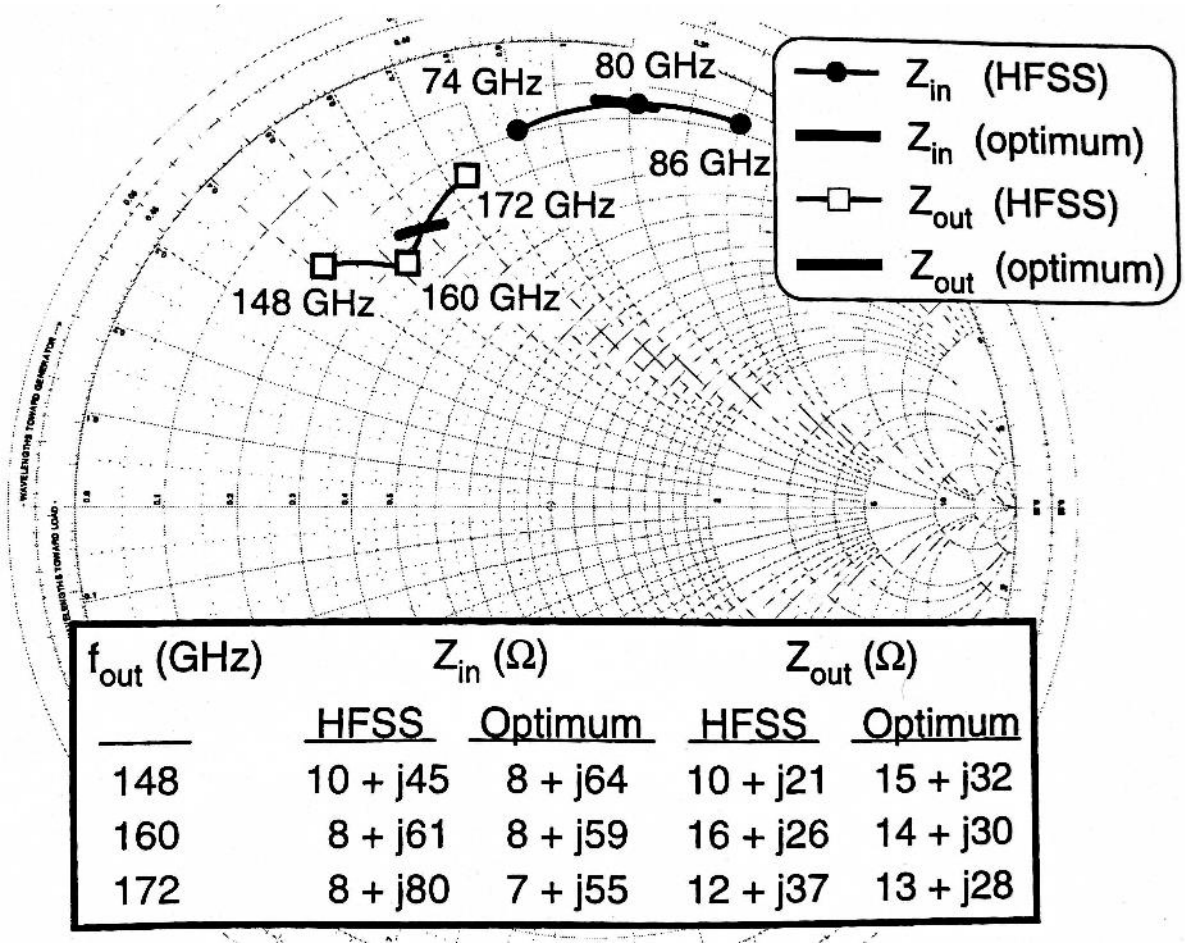
Fig. 4.17 shows the optimum embedding impedances and the HFSS calculated embedding impedances for the final circuit/block design of the 40/80 GHz balanced doubler. The embedding impedances are those of the individual anodes. The optimum embedding impedances were calculated using a Penfield Rafuse analysis with C_{j0} = 130 fF, V_{br} = 14 V, $N_D = 1\times10^{17}$ cm^{-3}, R_s = 0.8 Ω, and a total input power of approximately 200 mW.



f_{out} (GHz)	Z_{in} (Ω)		Z_{out} (Ω)	
	HFSS	Optimum	HFSS	Optimum
74	8 + j44	9 + j65	14 + j24	17 + j33
80	8 + j56	8 + j60	18 + j29	16 + j30
86	12 + j73	8 + j55	13 + j36	15 + j27

Fig. 4.17 Optimum and HFSS calculated embedding impedances for the 40/80 GHz balanced doubler circuit.

Fig. 4.18 shows the optimum embedding impedances and the HFSS calculated embedding impedances for the final circuit/block design of the 80/160 GHz balanced doubler. The embedding impedances are those of the individual anodes. The optimum embedding impedances were calculated using a Penfield Rafuse analysis with C_{j0} = 63 fF, V_{br} = 10 V, $N_D = 2\times10^{17}$ cm^{-3}, R_s =1.2 Ω, and a total input power of approximately 80 mW.



f_{out} (GHz)	Z_{in} (Ω)		Z_{out} (Ω)	
	HFSS	Optimum	HFSS	Optimum
148	10 + j45	8 + j64	10 + j21	15 + j32
160	8 + j61	8 + j59	16 + j26	14 + j30
172	8 + j80	7 + j55	12 + j37	13 + j28

Fig. 4.18. Optimum and HFSS calculated embedding impedances for the 80/160 GHz balanced doubler circuit.

4.9 Summary

This chapter described how HFSS and MDS were used to design the embedding circuits for the 40/80 GHz and 80/160 GHz balanced doublers. The simulation results shown for the RF blocking filters, output waveguide probes and hammer-head RF filters showed excellent performance over a wide bandwidth. This suggests that these components did not play a significant role in limiting the doubler performance. The embedding impedances calculated by HFSS for the final circuit/block designs and the optimum impedances calculated using a Penfield-Rafuse analysis were shown in Section 4.8. The HFSS calculated embedding impedances were very close to the optimum embedding impedances in the frequency ranges indicated in Fig. 4.17 and Fig. 4.18. The HFSS calculated embedding impedances are used in Chapter 7 in harmonic balance simulations to predict the multiplier output power, bandwidth, and efficiency for comparison to the actual measured data.

Chapter 5

Balanced Doubler Test Systems

5.1 Overview

This chapter describes how the doubler test measurements were made. Section 5.2 briefly describes the fundamental sources and section 5.3 describes the power sensors. The test system used to evaluate the performance of the 40/80 GHz doubler at room temperature is described in section 5.4 and a similar system for cryogenic measurements is described in section 5.5. The test system for the 80/160 GHz doubler is described in section 5.6. Section 5.7 describes a measurement technique used to evaluate the output match of the 40/80 GHz doubler.

5.2 Millimeter-Wave Sources

MMW Gunn oscillators have excellent power, bandwidth and frequency stability, but require mechanical tuners to achieve wide band operation. However, they are otherwise very easy to use and make excellent and reliable MMW bench top sources. When choosing a Gunn oscillator, there is always a trade-off between tunable bandwidth and output power. The Gunn oscillator purchased for the 40/80 GHz doubler measurements is capable of delivering over 200 mW in the entire band from 37 GHz to 43 GHz and employs a single mechanical tuner. Fig. 5.1 shows a graph of the measured output power from the Gunn.

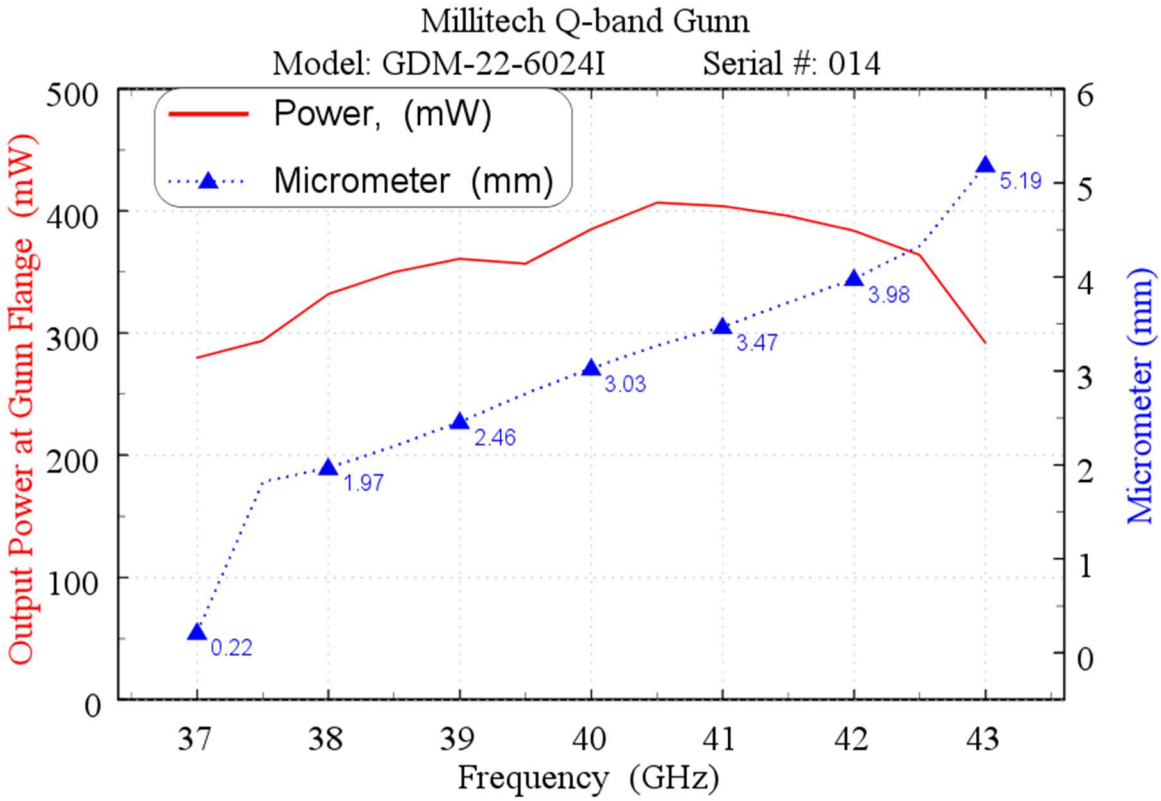


Fig. 5.1. Gunn oscillator output power and micrometer setting versus frequency.

Several Klystrons on loan from the National Radio Astronomy Observatory were also used to provide power in the band from 34 GHz and 45 GHz. The klystrons were run open loop and thus exhibited some frequency and power instability. However, these instabilities represented less than 1% of the nominal values, ie. the frequency instability at 40 GHz was typically less than 400 MHZ. The klystrons were only used at frequencies outside the tunable range of the Gunn, or to obtain power levels beyond the range of the Gunn.

An E-band (60-90 GHz) Gunn and a W-band (75-110 GHz) Gunn purchased from John Carlstrom were used to provide input power for the 80/160 GHz doubler. Both Gunn oscillators employ a pair of mechanical tuners to achieve a 3 dB bandwidth of approximately 25% and maximum output power in excess of 100 mW.

5.3 Millimeter-Wave Power Sensors

Hewlett-Packard model HP-437B power meters were used to measure power below 110 GHz using WR-22 (33-50 GHz) and WR-10 (75-110 GHz) waveguide power sensors. The power sensors employ diode detectors and thus have relatively fast response times. The meters and power sensors are calibrated and traceable to NIST. However, the calibration for the WR-10 power sensor is given only in the range of 75-110 GHz, and thus power measurements outside this range are not traceable to NIST.

Power measurements of the 80/160 GHz doubler were made with a Thomas-Keating (TK) absolute power meter. The TK meter is a cell made of a thin metal film sandwiched between two TPX plates. The cell is oriented at the Brewster angle to an incident plane wave. The cell absorbs part of the incident power and converts it to heat. The incident wave is optically chopped, thus modulating the generated heat. This modulated heat gives rise to a modulated pressure within the cell which is converted to electrical energy by a pressure transducer. The transmission of the TPX plates and the absorption of the metal film are carefully calibrated by Thomas-Keating Ltd. over the frequency range of 30 GHz to 3 THz.

Because the TPX transmission and metal film absorption are known, the fraction of incident power from the plane wave absorbed by the meter is known. The only calibration required is for the pressure transducer. This calibration is performed by applying a square wave voltage of known amplitude and duty cycle to the film. The film resistance can be measured directly, and thus the absorbed power from the calibrating signal can be easily calculated. This power is compared to the output signal from the pressure transducer and the calibration is complete. Power measurements made at UVA in W-band with the TK meter compare well with the HP-437B measurements.

5.4 40/80 GHz Test System

The test system for the 40/80 GHz doubler is shown in Fig. 5.2. Most of the power from the Gunn oscillator passes through the isolator and the directional coupler to the plane labeled FF′. Using the manual waveguide switch, the power incident at FF′ can be directed toward any of the three equidistant planes AA′, BB′ or CC′. Under the assumptions that each of the three equal length paths are identical and reflections in the waveguide components are small, then the available power, P_{av} , at the three planes AA′, BB′, and CC′ is equal. P_{av} is measured by setting the waveguide switch to direct power to the sensor at AA′.

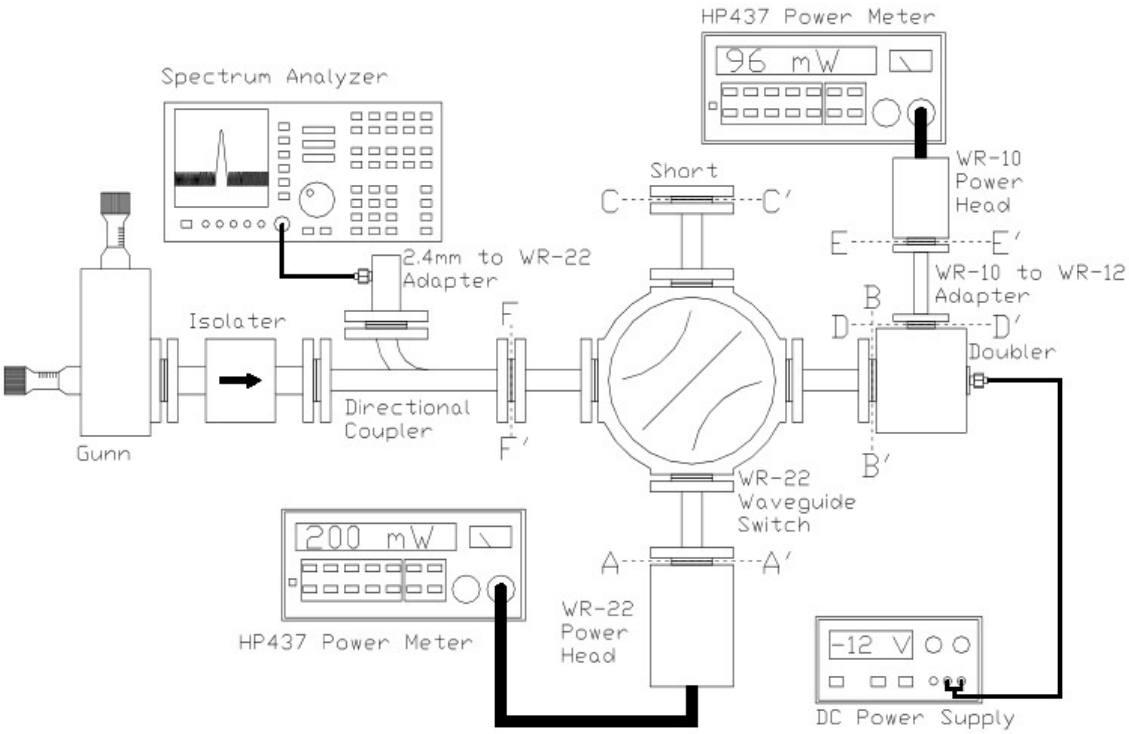


Fig. 5.2. Room temperature measurement system for the 40/80 GHz doubler.

A spectrum analyzer is used to measure reflected power and frequency. Reflected power from any of the three planes AA′, BB′, or CC′ is partially coupled to the spectrum analyzer and the rest is absorbed in the isolator. The power readings on the spectrum analyzer are thus a function of the available power, P_{av} , the reflection coefficient at the plane AA′, BB′, or CC′, the coupling coefficient of the directional coupler, and losses in the waveguide components, waveguide-to-2.44 mm converter, and coaxial cable. However, the reflected power from the three planes travels a nearly identical path and thus is subject to the same losses and coupling. The only difference in the measured values is due to waveguide reflections and differences in the reflection coefficients at the planes.

If the measured power reflected from plane CC′ is P_{RS} , and the measured power reflected from plane BB′ is P_{RL} , then the input reflection coefficient for the frequency doubler, Γ, is given by eq. 5.1.

$$|\Gamma|^2 \sim \frac{P_{RL}}{P_{RS}} \tag{5.1}$$

Eq. 5.1 is exact if reflections in the waveguide components is zero. For small reflections in these components, a reasonable assumption in Q- and W-band, eq. 5.1 gives a good approximation for Γ. The reflected power measurements in this system are self-calibrating and detailed knowledge of the coupling values and losses are not required. In fact, the absolute value of the power levels on the spectrum analyzer need not be correct. The only requirement is that the power measurements are linear over the dynamic range of the instrument.

5.5 40/80 GHz Cryogenic Test System

The 40/80 GHz cryogenic test system of Fig. 5.3 is similar to the test system described in section 5.4 except for some additional waveguide components associated with the dewar. The losses in the WR-22 waveguide between planes BB′ and GG′ and WR-12 waveguide between planes HH′ and DD′ were calibrated as a function of temperature.

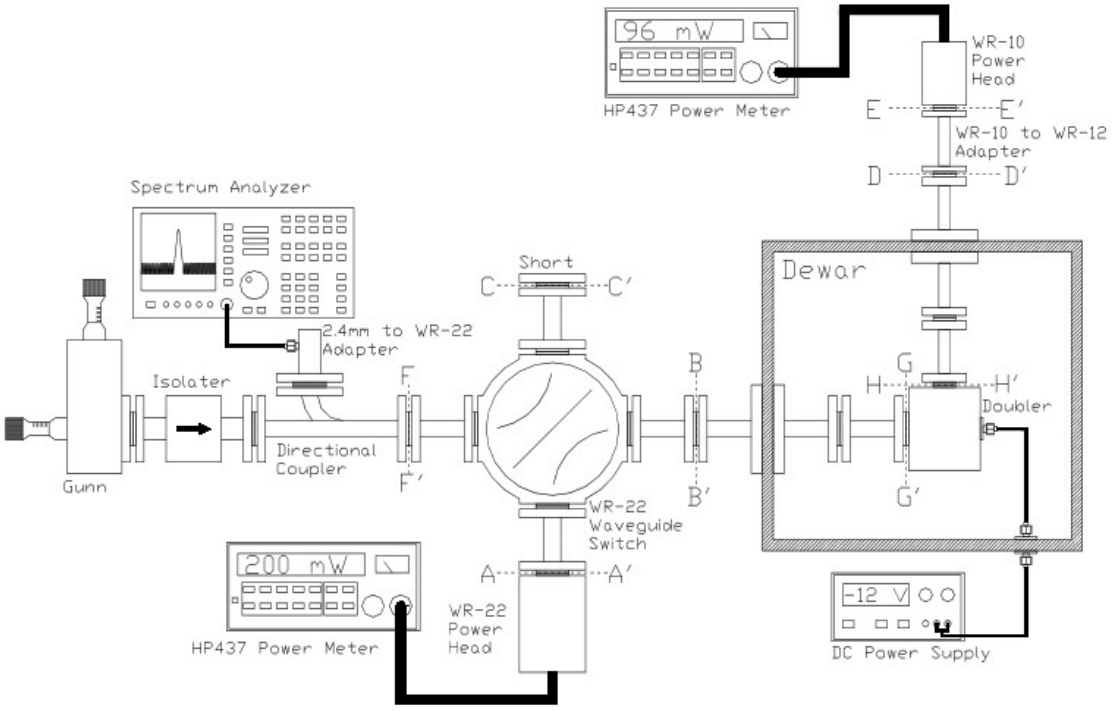


Fig. 5.3. Cryogenic test system for the 40/80 GHz doubler.

5.6 80/160 GHz Test System

The 80/160 GHz test system is shown in Fig. 5.4. It is similar to the other two test systems except that a Thomas-Keating power meter is used to measure output power, an Anritsu power meter is used to measure reflected input power, and a W-band harmonic mixer is employed for frequency measurement. Input power is provided by a Gunn oscillator.

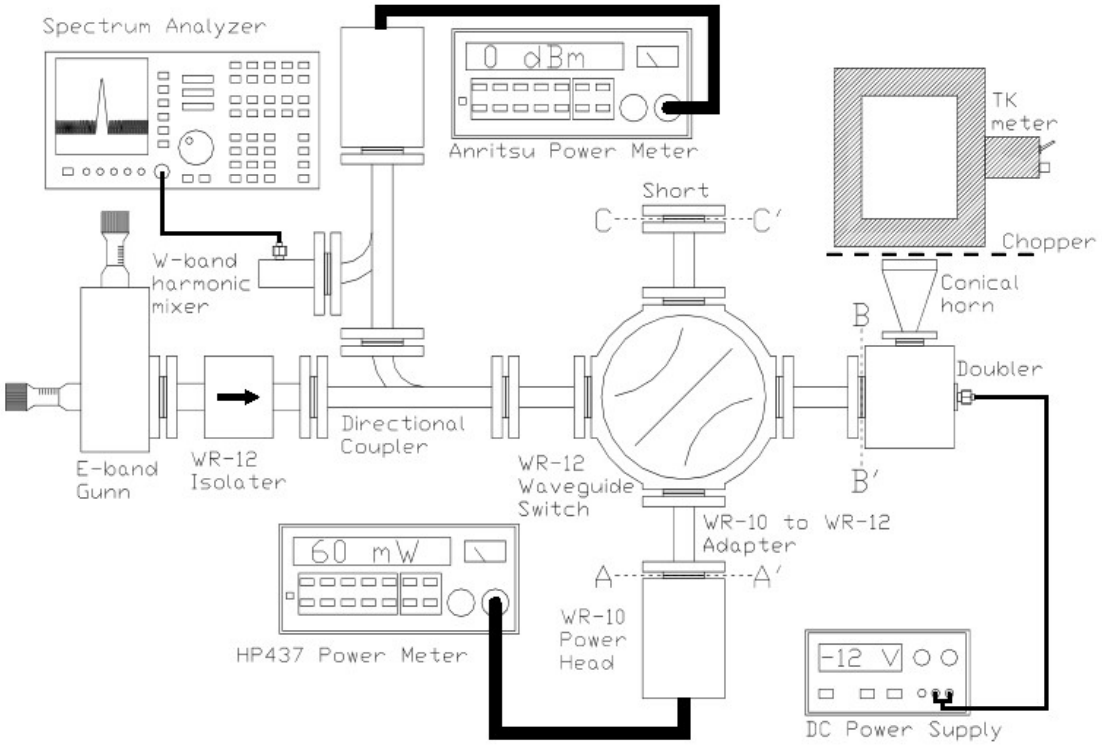


Fig. 5.4. 80/160 GHz doubler test system.

5.7 Quarter-Wave Transformer Test

Evaluation of the input match is straightforward since the reflected input power can be measured through the directional coupler. Evaluation of the output match is somewhat more difficult. A vector network analyzer could be used to measure the reflection at the output port directly, but this would have to be done with the varactor in an unpumped state and the information obtained would be of questionable value.

However, another method exists to evaluate the output match using a Teflon quarter-wave transformer in the output waveguide and measuring the output power as a function of the transformer position. This is done by removing the power sensor between readings and moving the Teflon transformer with a micrometer. If the measured output power prior to

insertion of the Teflon transformer is denoted as P_{out} , and the output power as a function of the transformer position is denoted as $P_T(x)$, then the reflection coefficient at the doubler output waveguide flange, Γ, and the maximum achievable output power, P_{av} , are found as,

$$P_{av} = \frac{P_{Tmax} \cdot (Z_T^2 + Z_0 \cdot Z_L)^2}{4 \cdot Z_T^2 \cdot Z_0 \cdot Z_L} \tag{5.2}$$

$$|\Gamma| = \sqrt{1 - \frac{P_{out}}{P_{av}}} \tag{5.3}$$

where, Z_0 is the characteristic impedance of the output waveguide, Z_T is the characteristic impedance of the output waveguide with the Teflon dielectric, P_{Tmax} and P_{Tmin} are the extrema of $P_T(x)$ and P_{Tr} and Z_L are given by eq. 5.4 and eq. 5.5 respectively.

$$P_{Tr} = \frac{P_{Tmin}}{P_{Tmax}} \tag{5.4}$$

$$Z_L = \frac{2 \cdot Z_0^3 \cdot Z_T^2 \cdot (1 - P_{Tr}) - \sqrt{4 \cdot Z_0^6 \cdot Z_T^4 \cdot (P_{Tr} - 1)^2 - 4 \cdot Z_0^2 \cdot (P_{Tr} \cdot Z_T^4 - Z_0^4) \cdot (P_{Tr} \cdot Z_0^4 - Z_T^4)}}{2 \cdot (P_{Tr} \cdot Z_T^4 - Z_0^4)} \tag{5.5}$$

The characteristic impedances Z_T and Z_0 depend on the waveguide impedance definition used, ie. Z_{pi} , Z_{pv} , or Z_{vi} and on the waveguide dimensions and the permittivity of the dielectric material. A simple formula for Z_{pv} for a TE_{10} mode is given by eq. 5.6.

$$Z_{pv} = \frac{2 \cdot b \cdot \omega \cdot \mu}{a \cdot \sqrt{\omega^2 \cdot \mu \cdot \varepsilon - \left(\frac{\pi}{a}\right)^2}} \tag{5.6}$$

A simple formula for Z_{pi} for a TE_{10} mode is given by eq. 5.7.

$$Z_{pi} = \frac{\pi^2 \cdot b \cdot \omega \cdot \mu}{8 \cdot a \cdot \sqrt{\omega^2 \cdot \mu \cdot \varepsilon - \left(\frac{\pi}{a}\right)^2}} = Z_{pv} * \left(\frac{\pi}{4}\right)^2 \tag{5.7}$$

This technique assumes that the available power from the doubler is unperturbed by the insertion of the Teflon transformer or by the position of the transformer. This assumption is not strictly true, but the technique should give a reasonable estimate of the output match. A derivation of this technique is given in Appendix B.

5.8 Summary

The test systems and techniques used to measure the 40/80 GHz and 80/160 GHz doublers were described. Since accurate absolute power measurements are difficult to make in the MMW and SMMW, a description of the power sensors was also provided. A special technique using quarter-wave Teflon transformers to measure the quality of the output match was briefly described with a detailed derivation provided in Appendix B.

Chapter 6

Measurement Results

6.1 Overview

Test results for the 40/80 GHz balanced doubler are presented in this chapter. Room temperature test results are given in Section 6.2. and cryogenic test results are given in Section 6.3. Test results for the 80/160 GHz doubler are included in Appendix G. A summary of the 40/80 GHz doubler results is given in Section 6.4.

6.2 40/80 GHz Doubler Test Results at 290 K

Test results presented in this section were obtained using the measurement system shown in Fig. 5.2 (page 65). Power levels were measured using HP437B meters with Q-band (WR-22, 33-50 GHz) and W-band (WR-10, 75-110 GHz) power sensors. All input power measurements are referenced to the input waveguide flange of the doubler block (plane BB′ in Fig. 5.2). Since the doubler block incorporates a WR-12 output waveguide flange and the output power sensor incorporates a WR-10 waveguide flange, a WR-12-to-WR-10 waveguide adapter was used. All output power measurements are referenced to the WR-10 waveguide flange of the power sensor (plane EE′ in Fig. 5.2). No corrections were made for losses within the multiplier block or in the waveguide adapter. These losses are addressed in Chapter 8 where the simulated and measured data for the 40/80 GHz doubler are compared.

The graph in Fig. 6.1 shows measured output power and efficiency versus input power for SB13T1 varactors with 12 μm and 13 μm anodes. The quartz circuit is the same in both cases. The peak efficiency is 48% at 82 GHz for the varactor chip with 12 μm anodes and 46% at 78 GHz for the varactor chip with 13 μm anodes. For both varactors, the peak efficiency occurs for an input power of approximately 175 mW. Input power was provided from a Millitech Gunn-effect oscillator with available power of 200 mW in the 37-43 GHz band (see Fig. 5.1, page 63) and from several klystrons operating in the 35-45 GHz band with output power typically in excess of 300 mW. No corrections for loss have been made to this data.

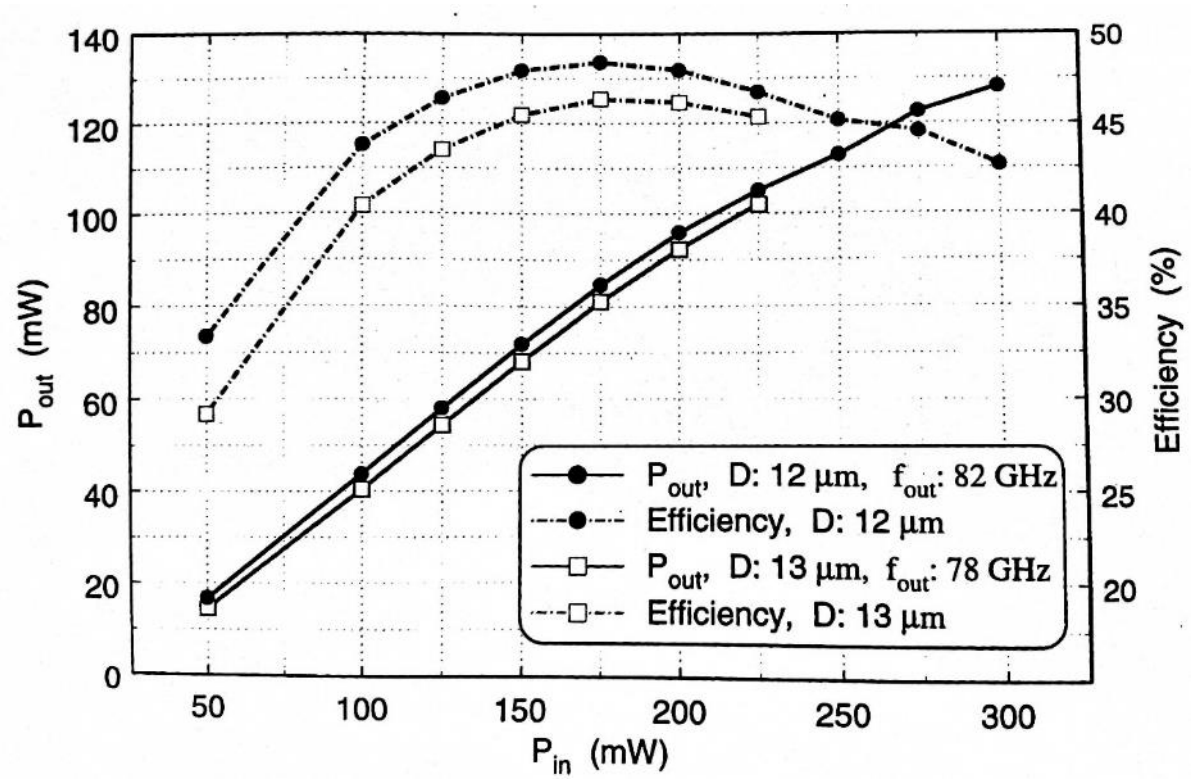


Fig. 6.1. Measured output power and efficiency versus input power for two different varactor chips.

Fig. 6.2 shows output power as a function of input power at an output frequency of 82 GHz. The varactor is an SB13T1 with 12 µm anodes, although not the same chip used in the measurements shown in Fig. 6.1. The peak efficiency of 51% for this varactor occurs at an input power level of 150 mW. This varactor has the highest efficiency at room temperature of any of the chips that were tested. The variances in peak efficiency for the SB13T1 varactors with 12 µm anodes shown in Fig. 6.1 (48%) and Fig. 6.2 (51%) arise from small variations in the assembly of the doubler. Unfortunately, there is no additional data for this varactor because klystrons were unavailable at the time the tests were made.

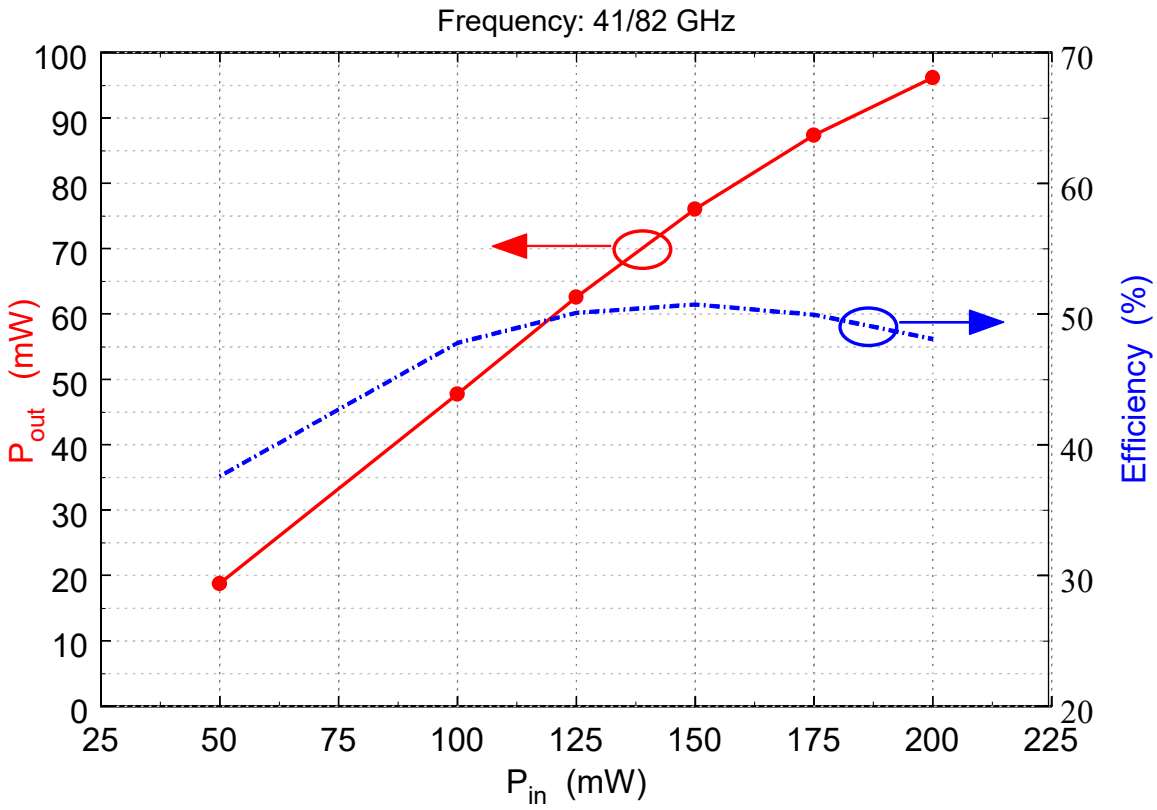


Fig. 6.2. Output power versus input power for the 40/80 GHz doubler using an SB13T1 varactor with 12 µm diameter anodes. This varactor chip yielded the best efficiency (51%) obtained at room temperature.

Fig. 6.3 shows measured output power versus output frequency for the same 12 μm and 13 μm anode varactors used in the graph of Fig. 6.1. The input power for these measurements was 200 mW. Tuning was provided through an external electronic DC bias supply. The peak efficiency for the SB13T1 varactor with 12 μm anodes occurred at 82 GHz. The peak efficiency for the SB13T1 varactor with 13 μm anodes occurred at 78 GHz. The measured 3 dB fixed-tuned bandwidth of 17% (~ 14 GHz) is typical for all of the varactors and circuits that were tested.

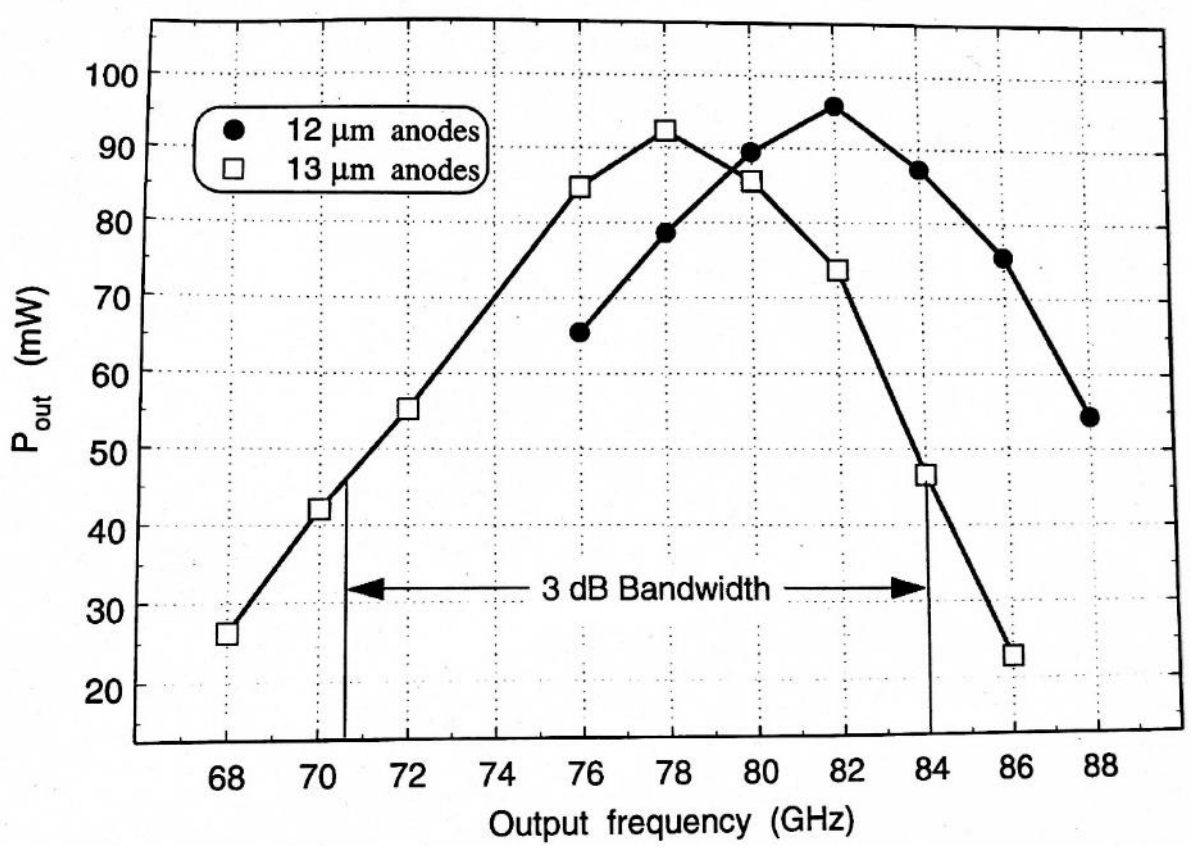


Fig. 6.3. Measured output power versus output frequency for P_{in} = 200 mW.

Fig. 6.4 shows the measured reflected input power versus output frequency for the 12 μm and 13 μm anode chips. The data corresponds to the same two varactor chips used in the graphs of Fig. 6.1 and Fig. 6.3. The reflected power measurements were made with an HP8565E spectrum analyzer through a 20 dB directional coupler. The spectrum analyzer was also used to monitor the input frequency. Reflected power levels were typically less than 1% of the incident power at the band center, indicating a good input impedance match.

The quality of the output impedance match was evaluated by attaching a 1 inch section of E-band waveguide to the doubler output waveguide flange, inserting a Teflon quarter-wave transformer, and measuring the output power as a function of the transformer position. The input power level was held constant at 200 mW. The output power was

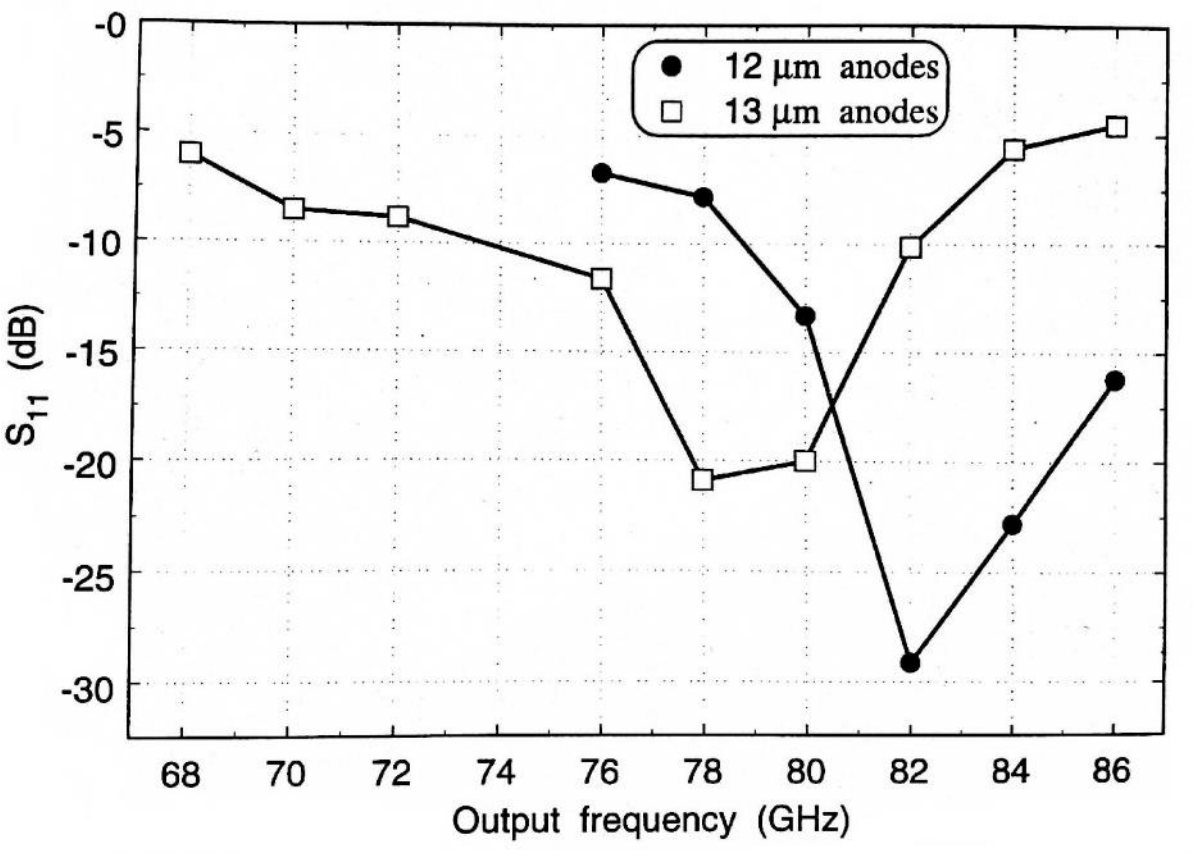


Fig. 6.4. Measured input power reflection coefficient vs output frequency at P_{in} = 200 mW.

measured to be 94.4 mW prior to the insertion of the Teflon. With the Teflon transformer inserted in the output waveguide, the measured output power extrema were 72 mW and 85 mW. Using this data, we calculated the SWR in the output waveguide to be less than 1.6 (without the Teflon transformer), indicating a very good output impedance match. This calculation assumes that the available output power from the doubler is constant and unaffected by the transformer position. However, the asymmetry in the measured data shown in Fig.6.5 may indicate a perturbation of the available output power. A detailed description of the quarter-wave Teflon transformer technique is given in Appendix D.

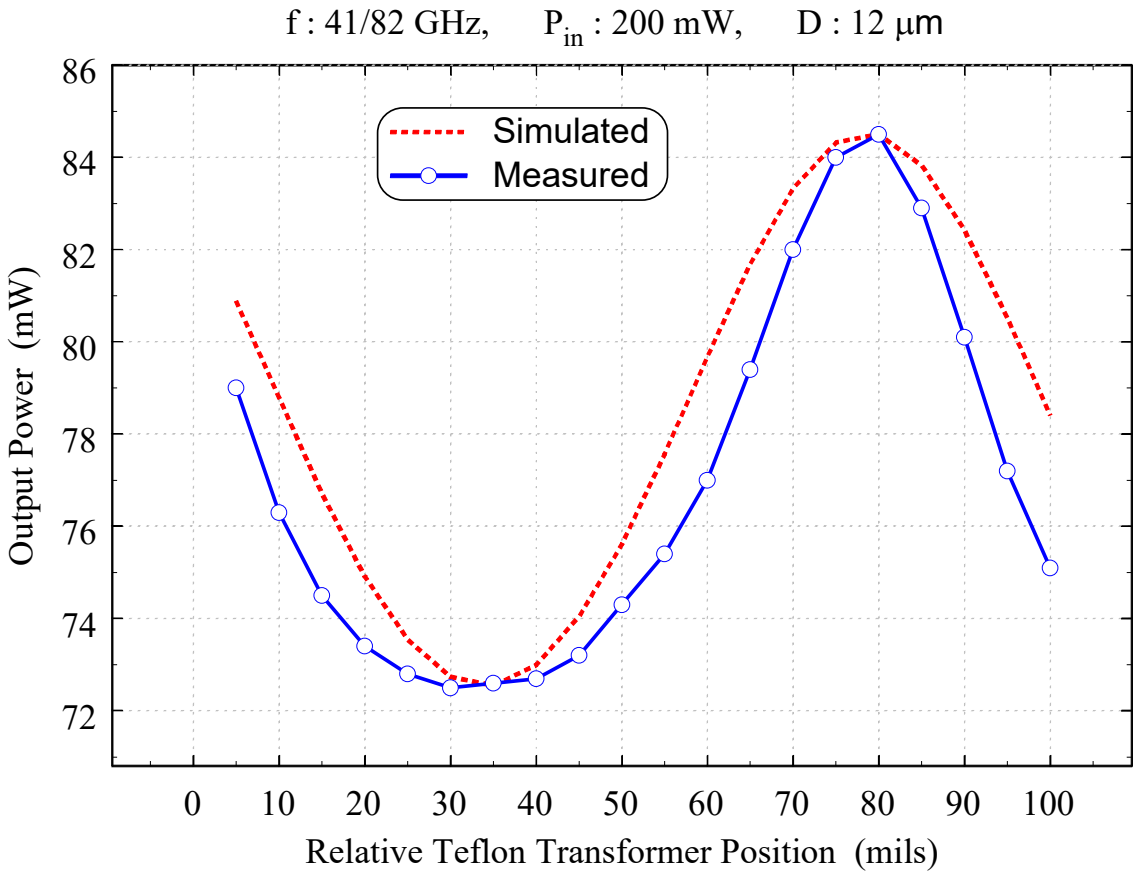


Fig. 6.5. Measured and simulated data from the quarter-wave Teflon transformer test.

A graph of measured DC bias voltage and current versus output frequency is shown in Fig. 6.6. These curves were obtained from measurements with the 13 μm anode chip and 200 mW input power, but are typical for all of the chips that were tested. The voltages and currents shown in Fig. 6.6 are those measured at the DC supply and thus the voltage across each varactor is one third that shown in the graph and the current through each varactor is one half that shown in the graph (perfect balance is assumed). The graph in Fig. 6.3 shows that the peak efficiency for this varactor occurred at 78 GHz. At this frequency, the bias current through each varactor was 100 μA. Forcing the DC current to zero resulted in only a very small degradation in efficiency, indicating that the peak performance was obtained in a predominantly varactor mode of operation.

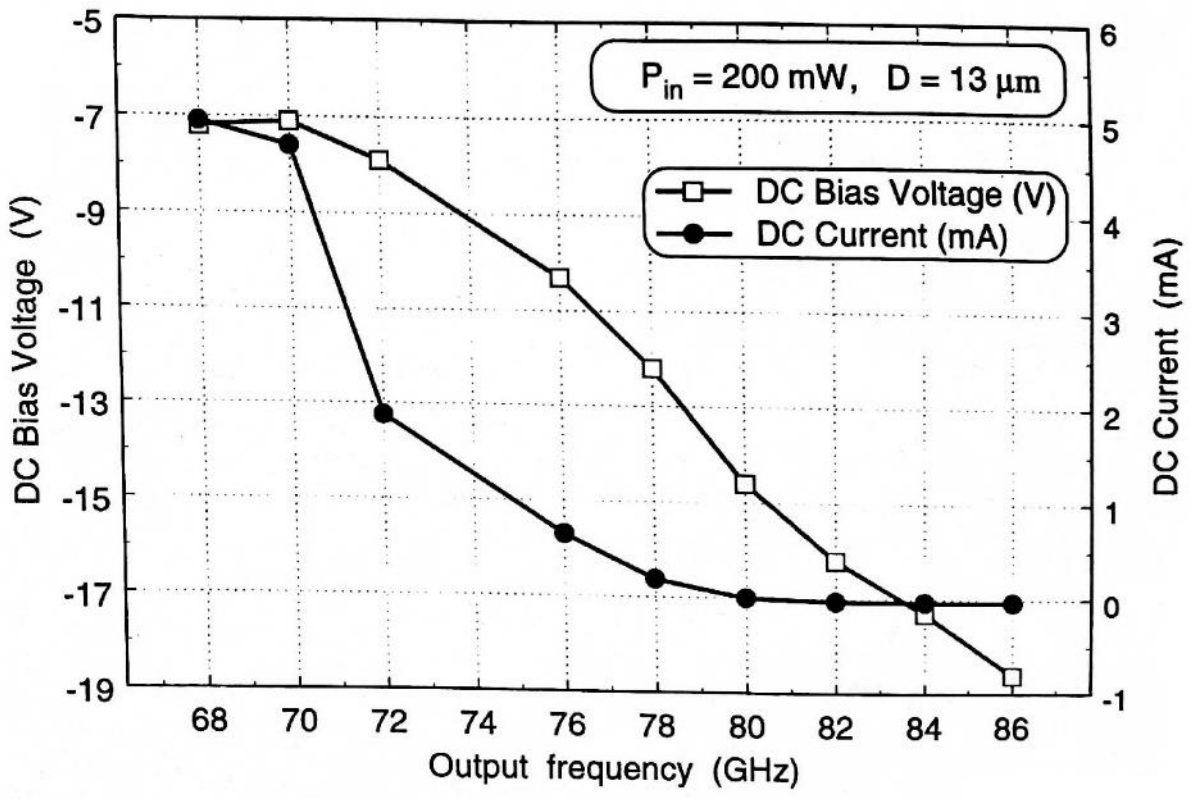


Fig. 6.6. Measured DC current and bias voltage vs output frequency for the 13 μm anode chip.

6.3 Cryogenic Results for the 40/80 GHz Doubler

For many applications, particularly in radio astronomy, it may be feasible to cool the multiplier. For these applications, it is necessary to determine the temperature dependence of the multiplier output power, efficiency and bandwidth and to determine if the multiplier can survive thermal cycling. Only a minor temperature dependence is expected in the circuit losses and embedding impedances. However, the electron mobility in GaAs has a strong temperature dependence. There is a peak in the electron mobility near 100 K for an epitaxial doping of $1x10^{17}$ cm^{-3} [Stillman et al, 1970], [Ruch et al, 1970]. Because series resistance is inversely proportional to electron mobility, an increase in multiplier efficiency is expected at cryogenic temperatures [Louhi et al, 1993]. A reduction in dissipated power in the varactor will also improve the reliability of the multiplier.

The cryogenic performance of the doubler was measured in a dewar outfitted with waveguides and vacuum windows at the input and output frequencies. These components were calibrated by measuring the insertion loss as a function of temperature. The dewar and its associated components were provided by the National Radio Astronomy Observatory's Central Development Laboratory. The input and output power measurements shown below are referred to the waveguide flanges on the doubler block and thus include corrections for the losses in the dewar waveguides. The specified temperatures are referenced to the multiplier block. The Schottky junction temperatures are expected to be somewhat higher due to power dissipation in the device.

Fig. 6.7 shows the output power as a function of the waveguide block temperature. The varactor was an SB13T1 with 13 µm anodes. The input power was held constant at 200 mW at plane BB′ (see Fig. 5.3, page 67). However, the input and output waveguide losses in the dewar were temperature dependent, and thus the power at the input waveguide flange on the doubler block (plane GG′) varied from 179 mW at 290 K to 181 mW at 14 K. This slight variation in the input power accounts for the apparent discrepancy in the slopes of the output power and efficiency curves in Fig. 6.7. The output power measurements shown in Fig. 6.7 are not corrected for losses in the WR-12-to-WR-10 waveguide adapter and thus the output power and efficiency at 290 K agree with the data in Fig. 6.1.

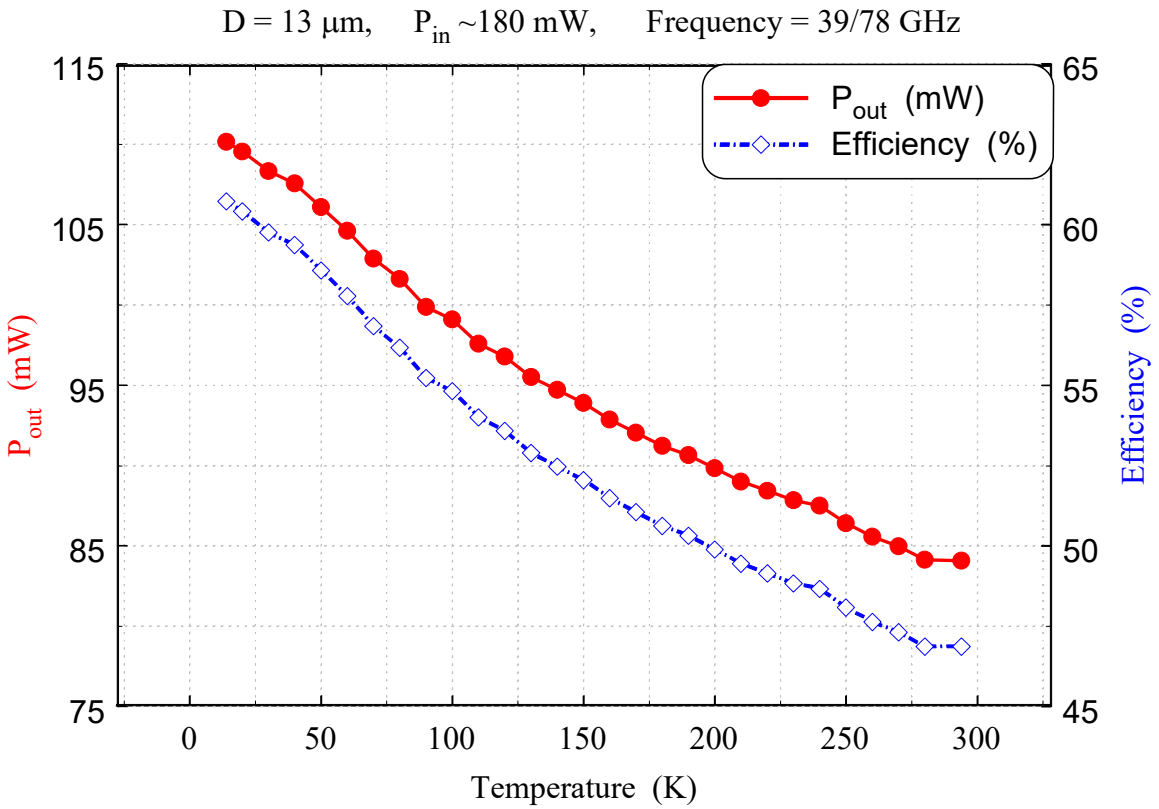


Fig. 6.7. Output power versus temperature for an input power of approximately 180 mW. The input and output power levels are referenced to the waveguide flanges on the block and thus the input power is a weak function of the block temperature.

Fig. 6.8 shows a measured efficiency of 61% at 78 GHz for an input power level of 150 mW, output power of 92 mW, and a block temperature of 14 K. The efficiency rolls off to 48% at an input power of 365 mW and output power of 175 mW. The 175 mW output power level should be sustainable since the Schottky junction temperature is probably still well below room temperature when the block is cooled.

Fig. 6.9 shows measured efficiency versus input power at four different temperatures. There is an increase in efficiency from 46% at 295 K to 61% at 14 K as the doubler block is cooled. Also, the input power level for peak efficiency drops as the block temperature decreases. Both of these phenomena are attributable to the temperature dependent electron mobility in GaAs.

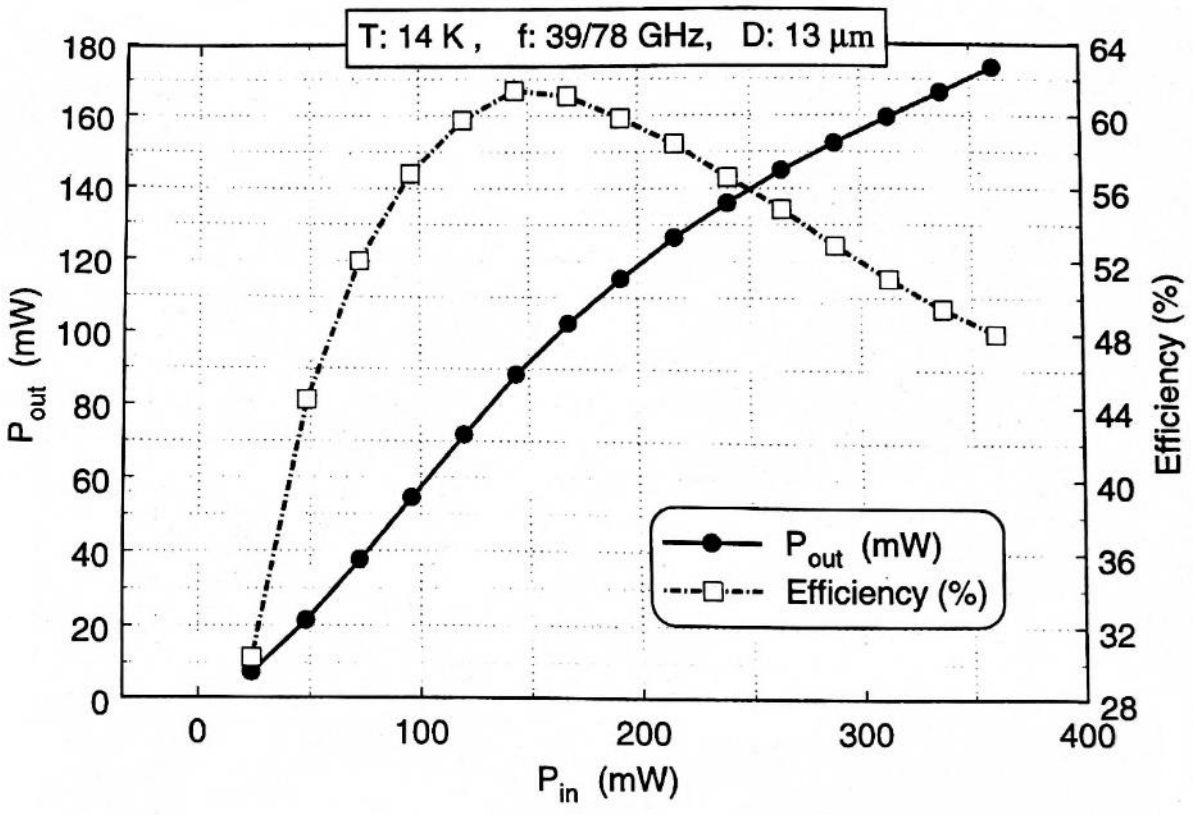


Fig. 6.8. Measured output power and efficiency vs input power at 14 K.

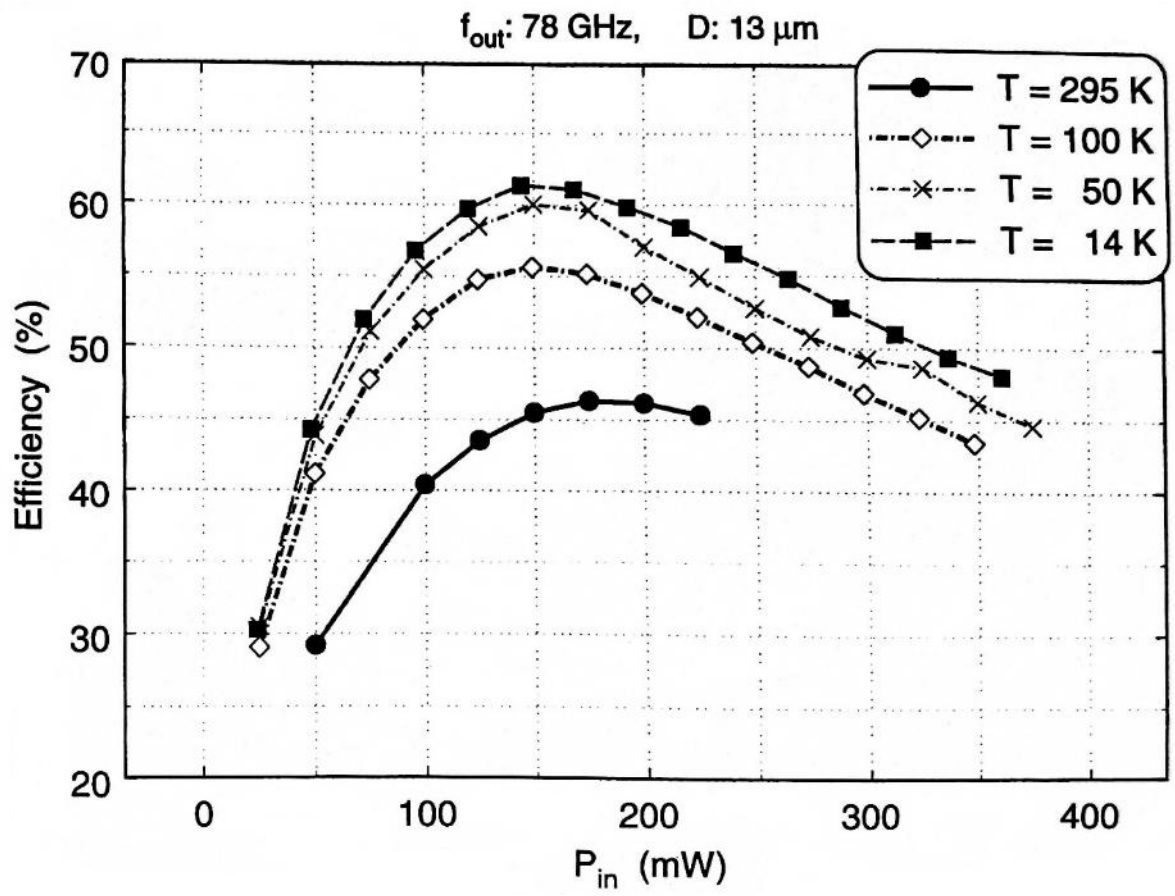


Fig. 6.9. Measured efficiency vs input power for various block temperatures. The output frequency is 78 GHz.

The fixed-tuned 3 dB multiplier bandwidth is largely dependent on the embedding impedances provided by the circuit. Since these impedances have only a very small temperature dependence, the fixed-tuned bandwidth is not expected to have a strong temperature dependence. The two plots in Fig. 6.10 show measured efficiency for the 13 µm anode chip as a function of frequency at block temperatures of 295 K and 14 K. The input power in both cases was held constant at 200 mW. The fixed-tuned 3 dB bandwidth for both curves is approximately 17%.

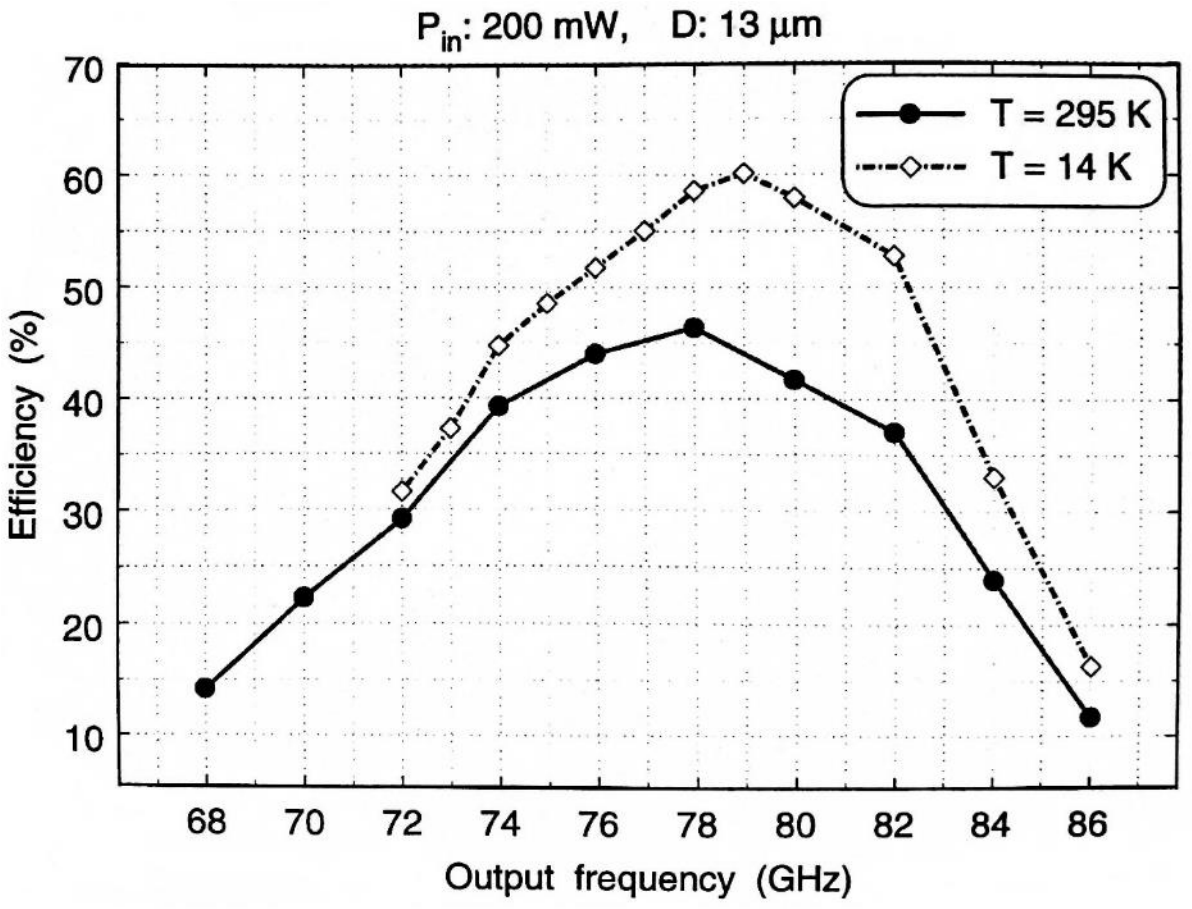


Fig. 6.10. Measured efficiency vs frequency at block temperatures 295 K and 14 K.

6.4 Summary

With the 40/80 GHZ doubler waveguide block at room temperature, the measured 3 dB fixed-tuned bandwidth was 17% for an input power of 200 mW. The peak efficiency of 51% occurred at an output frequency of 82 GHz and input power of 150 mW.

The 40/80 GHz doubler was also evaluated at cryogenic temperatures in a calibrated dewar. The measured peak efficiency for the varactor was 46% at room temperature with an input power level of 175 mW. The measured efficiency increased to 61% at an input power

of 150 mW and a block temperature of 14 K. With the block at 14 K, the efficiency dropped to 48% as the input power was raised to 365 mW, resulting in an output power of 175 mW. The 175 mW output power level should be sustainable at cryogenic temperatures. The 3 dB output power bandwidth was approximately 17% at both 14 K and 295 K, and exhibited only a weak temperature dependence.

Chapter 7

Conclusion

7.1 Overview

In this chapter, the simulated and measured data are compared and final conclusions are drawn. Section 7.2 provides a comparison of the simulated and measured results for the 40/80 GHz doubler. The simulation results for the 80/160 GHz doubler are presented in Section 7.3. Measured results for the 80/160 GHz doubler are included in Appendix G. Final conclusions based on the measured and simulated data are presented in Section 7.4 and suggestions for future research are given in Section 7.5.

7.2 Comparison of 40/80 GHz Simulated and Measured Results

The waveguide and circuit losses for the 40/80 GHz doubler were estimated using HFSS port solves at each distinct cross section in the block. The electrical conductivity of gold and the loss tangent of quartz were taken to be 4.1×10^7 S/m and 10^{-4} respectively. No corrections were made for conductor surface roughness, although actual measured waveguide losses are typically a factor of two higher than those based on conductivity and skin depth [Edwards, 1985], and thus the calculated losses represent minimum estimates of the actual values. The loss in the E-W waveguide adapter was measured using an HP8510 vector network analyzer. The waveguide probe, hammerhead filter and indium backshort losses were estimated using a full HFSS adaptive analysis. The results are summarized in Table 7.1.

Table 7.1. Minimum estimated losses for the 40/80 GHz doubler circuit. Losses are based on Au conductivity, $\sigma_{au} = 4.1 \times 10^7$ S/m, and quartz loss tangent, $\delta_{qtz} = 10^{-4}$.

Loss location	Frequency	Loss (dB)
Input waveguide	40 GHz	0.02
Quartz circuit	40 GHz	0.01
Quartz circuit	80 GHz	0.14
Output probe and filter	80 GHz	0.04
Indium backshort	80 GHz	0.01
Output waveguide	80 GHz	0.05
Waveguide adapter	80 GHz	0.15
Total		0.42

Two measured output power curves and three simulated output power curves for the 40/80 GHz doubler are shown in Fig. 7.1. The measured curves are the same as shown in Fig. 6.3. The simulated curves were generated using a harmonic balance analysis with an input power of 200 mW, zero biased junction capacitance of 140 fF and the circuit embedding impedances calculated by HFSS. The peak simulated output power of 145 mW occurred for the case of a calculated series resistance of 0.8 Ω per varactor and the estimated external circuit losses of 0.42 dB from Table 7.1. The discrepancy between the peak output power of this simulated curve and the measured peak output power is approximately 1.8 dB.

The calculated series resistance of 0.8 Ω and the calculated circuit losses of 0.42 dB represent minimum estimates of the actual values. Calculations for the series resistance tend to underestimate the actual value in a planar device as explained in Chapter 3. DC measurements of the SB13T1 varactor with 12 μm anodes tend to yield values near 1.2 Ω. The series resistance at millimeter-wave frequencies should be even higher due to the skin

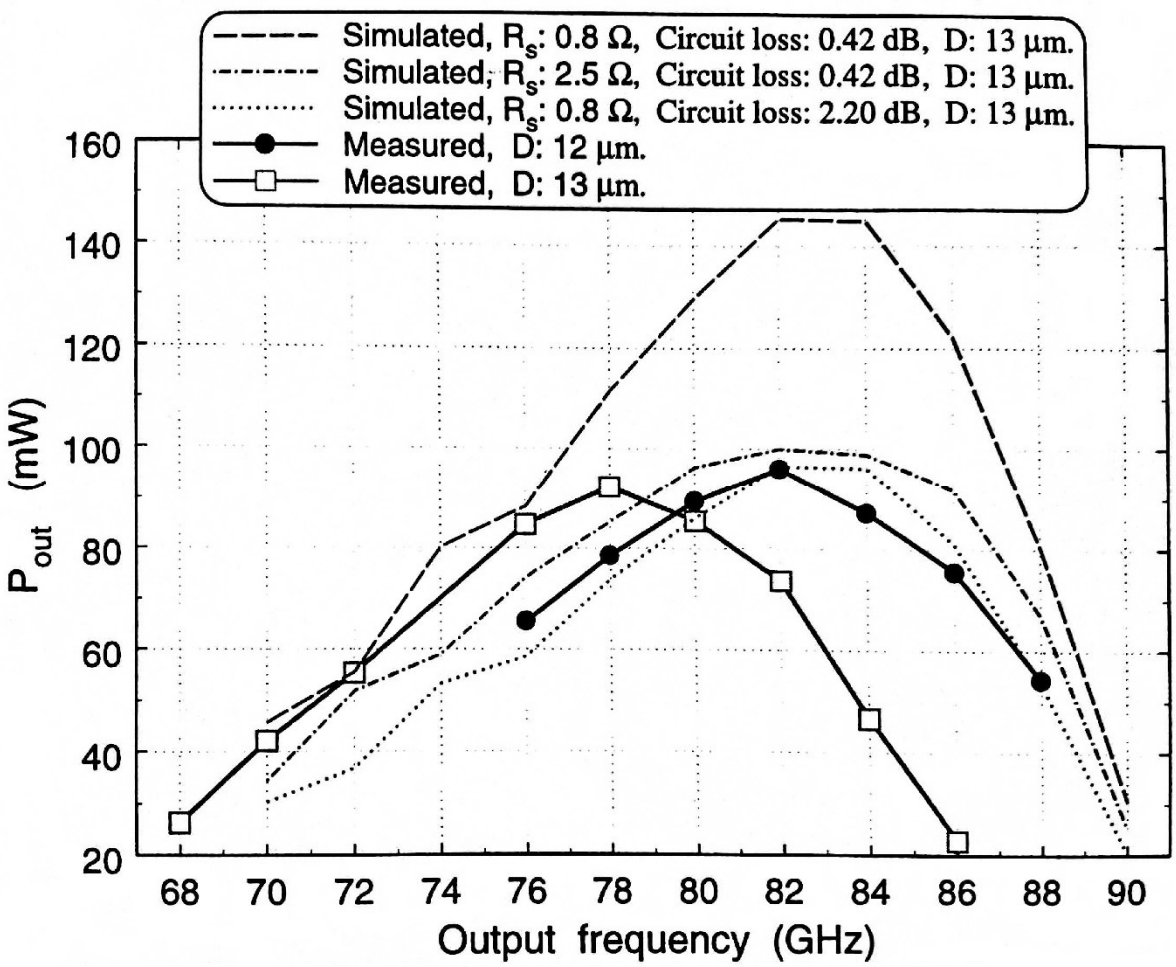


Fig. 7.1. Simulated and measured output power vs output frequency for the 40/80 GHz doubler at P_{in} = 200 mW.

effect. In addition, the series resistance is expected to be elevated due to heating. The actual circuit losses are also expected to be higher than the calculated values in Table 7.1 since the calculated losses do not include corrections for surface roughness.

The two remaining simulated curves in Fig. 7.1 were generated by introducing additional loss mechanisms sufficient to equate the simulated to the measured output power. In one case this was done by using an elevated series resistance of 2.5 Ω instead of the calculated value of 0.8 Ω. In the second case, the calculated 0.8 Ω series resistance and a total

of 2.2 dB in unspecified external circuit losses were used. The actual losses probably result from a combination of both mechanisms.

There are three additional factors which reduce the multiplier efficiency; (i) some power is converted to higher harmonics, (ii) the real part of the embedding impedance is somewhat higher than the simulated values due to circuit losses and (iii) there is an imbalance in the embedding impedances for varactors near the center conductor and varactors near the waveguide walls. The imbalance is negligible for the TE_{10} mode at the input frequency but is more important for the radially dependent EM field distribution at the output frequency. It may be possible to reduce or eliminate this effect by adjusting the spacing between the varactors.

There is a discrepancy in the peak frequency of the measured and simulated data in Fig. 7.1. The simulated data was generated using a zero biased junction capacitance of 140 fF which corresponds to the calculated value for an anode diameter of 13 μm and epitaxial layer doping of $1x10^{17}$ cm^{-3}. However, the simulated peak frequency of 82 GHz corresponds to the measured peak frequency for the 12 μm anodes. This discrepancy may arise from uncertainties in the actual varactor anode diameter and epitaxial layer doping.

Fig. 7.2 contains several plots of simulated and measured output power versus input power for the 40/80 GHz doubler. The graph also contains plots of simulated and measured DC current. The three simulated results were obtained using the calculated embedding impedances from HFSS and the calculated series resistance of 0.8 Ω per varactor. The measured output power for the 12 μm anode chip is the same as shown in the graph of Fig. 6.1 on page 72. Again, good agreement is obtained between the simulated and measured data when an additional 2.2 dB of loss is included in the simulation.

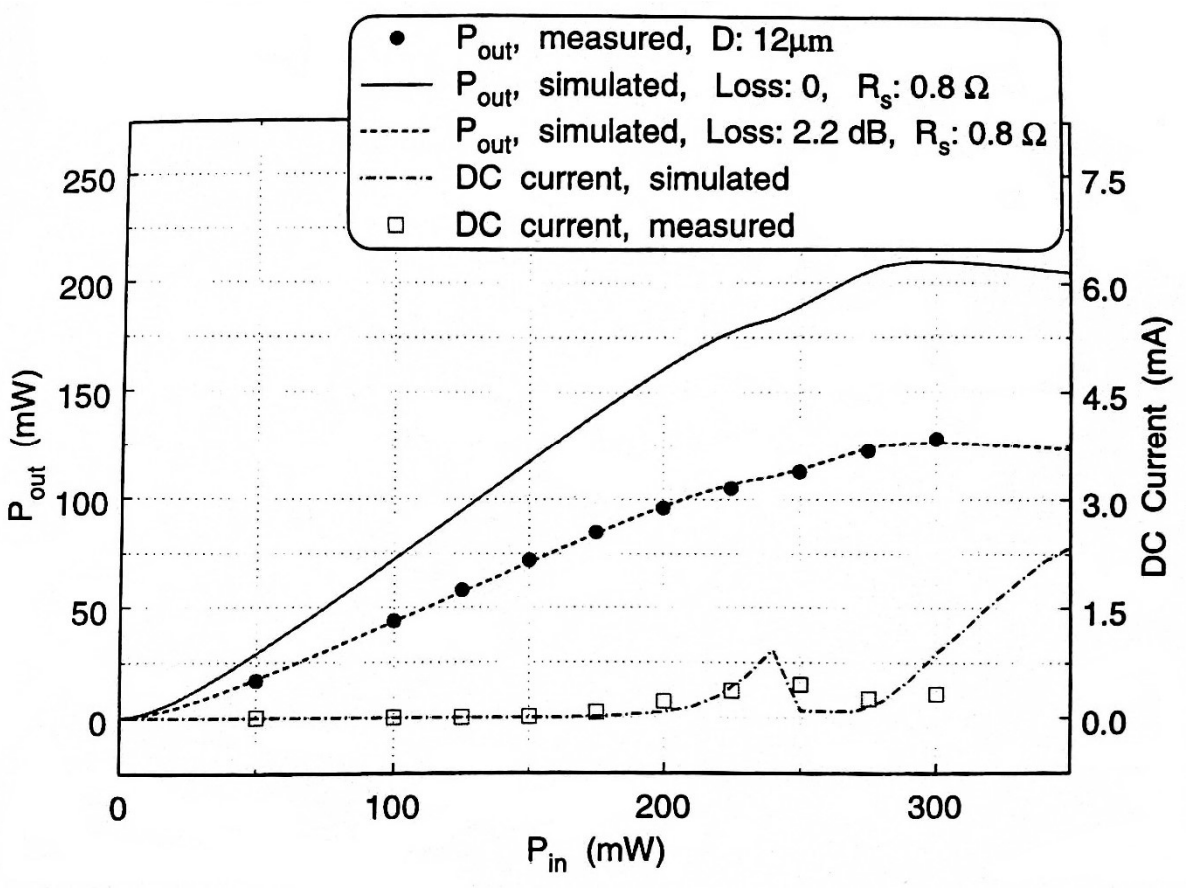


Fig. 7.2. Simulated and measured output power and DC current vs input power at 41/82 GHz.

For input powers in the range of 200-250 mW, there is an inflection in the simulated output power curves which coincides with an inflection in the measured data. Parametric oscillation [Penfield and Rafuse, 1962] can be ruled out as a cause for the inflection because the harmonic balance simulations do not model this effect. The inflection may be interpreted as a crossover between two operating regimes. For input power levels below 200 mW, optimum efficiency is achieved by steadily increasing the reverse bias voltage as the input power increases. In this regime, the DC current remains near zero (indicating a varactor mode of operation) and the bias voltage essentially tunes the average varactor capacitance to yield

the best impedance match to the circuit. For input power levels above 250 mW, the optimum operating point is dominated by the need to minimize power dissipation in the series and junction resistances.

7.3 Simulated Results for the 80/160 GHz Doubler

Harmonic balance simulations were used to predict the output power, bandwidth and multiplication efficiency of the 80/160 GHz doubler. The harmonic balance simulations were run with 5 harmonics, the HFSS calculated embedding impedances at the first (fundamental) and second harmonics, and shorts at the higher harmonics.

The graph in Fig. 7.3 shows simulated output power and efficiency versus input power for the 80/160 GHz doubler at an output frequency of 160 GHz. The nonlinear device used in the harmonic balance and HFSS simulations was based on a GaAs chip containing four varactors with an epitaxial layer doping of 2×10^{17} cm^{-3}. Each of the four anodes had a nominal 7 μm diameter (C_{j0} = 63 fF), a reverse breakdown voltage of 10 V, finger length of 30 μm, and buffer thickness of 5 μm. The thickness of the semi-insulating GaAs substrate was assumed to be 2 mils and the quartz thickness was 3 mils. The series resistance per anode for this varactor was calculated to be approximately 1.6 Ω per anode, but an assumed value of 3 Ω per varactor was used in the simulations. The peak simulated efficiency was 51% for an input power of 110 mW and an output power of 56 mW. The efficiency drops to 45% at an input power of 150 mW and an output power of 68 mW.

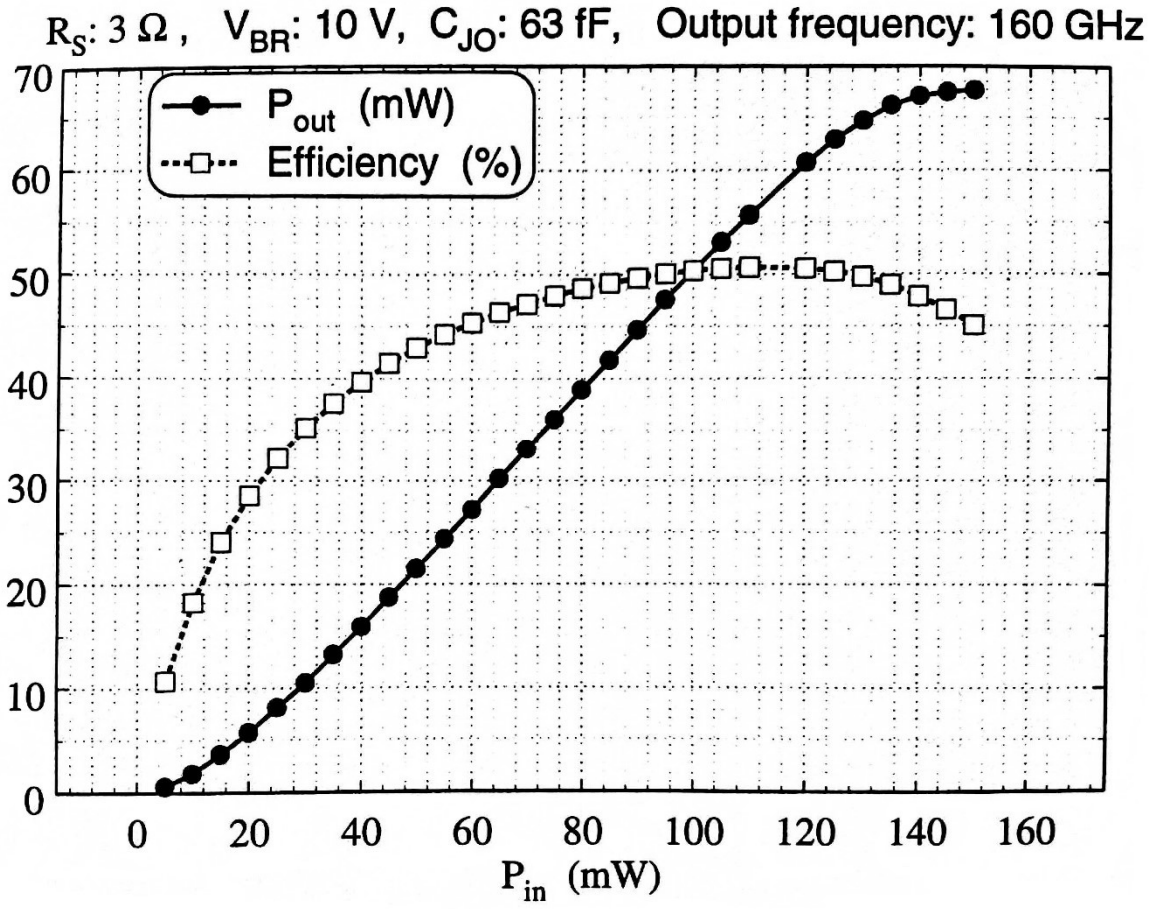


Fig. 7.3. Simulated output power and efficiency versus input power at 160 GHz.

The graph in Fig. 7.4 shows simulated output power and efficiency versus output frequency for an input power of 80 mW. The simulation environment was the same as described in the preceding paragraph. The peak output power is approximately 40 mW at 160 GHz and the corresponding peak efficiency is approximately 50%. The 3 dB output power bandwidth is approximately 16% which is similar to the bandwidth for the 40/80 GHz doubler.

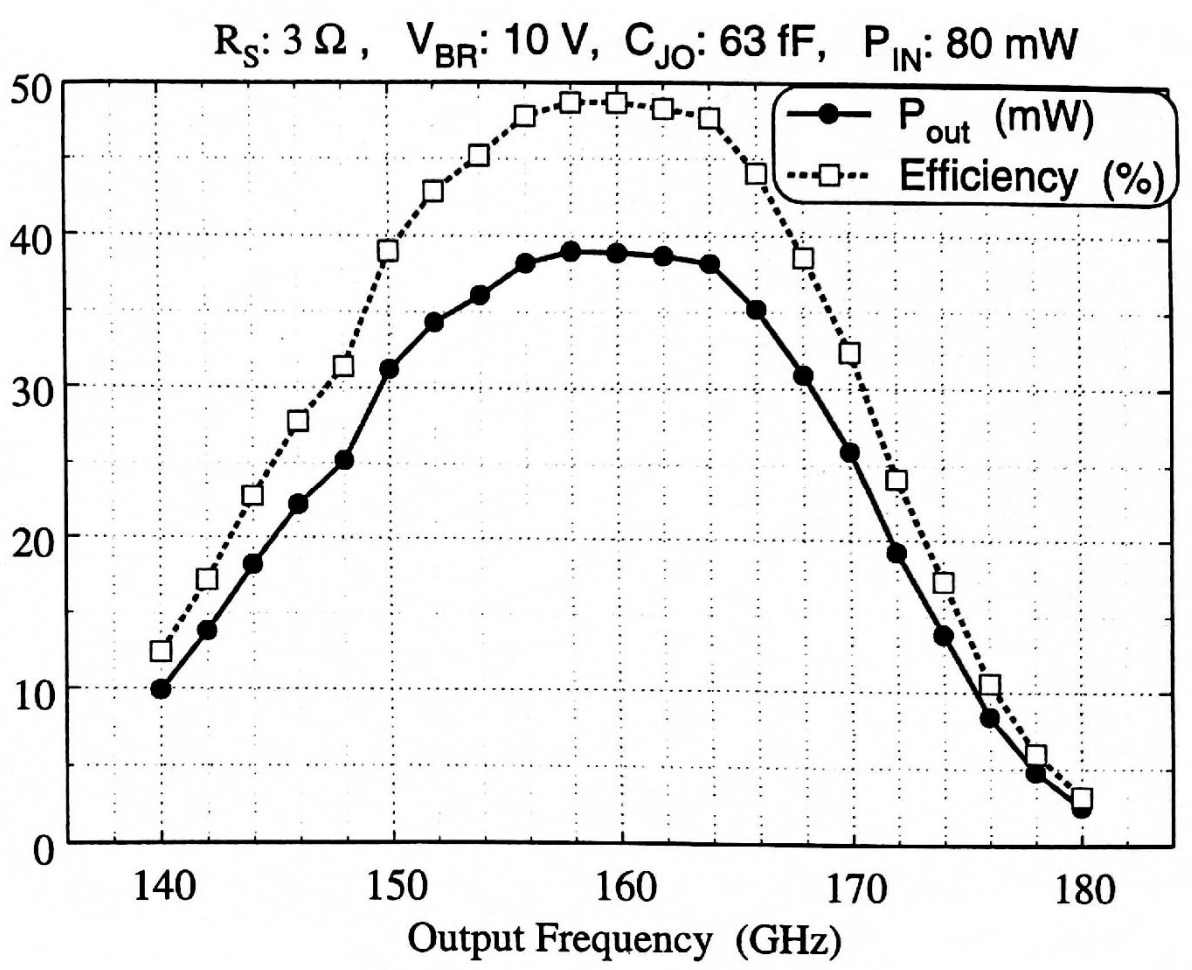


Fig. 7.4. Simulated output power and efficiency vs frequency for an input power of 80 mW.

7.4 Final Conclusions

A high-power, wide-band, fixed-tuned 40/80 GHz balanced frequency doubler has been designed and evaluated. The doubler uses a single SB13T1 GaAs chip comprising a linear array of 6 planar Schottky varactors connected in anti-series. The varactor chip and a quartz circuit are housed in a split waveguide block. The mounting of the varactor chip to the quartz circuit and the assembly of the block are relatively simple.

With the waveguide block at room temperature, the measured 3 dB fixed-tuned

bandwidth was 17% for an input power of 200 mW. The peak efficiency of 51% occurred at an output frequency of 82 GHz and input power of 150 mW. The peak efficiency for an input power of 200 mW was 48%. The measured results were compared to harmonic balance simulations using the calculated embedding impedances from HFSS. The measured fixed-tuned bandwidth of 17% was in excellent agreement with the simulated bandwidth and the measured peak output power was within 1.8 dB of the simulated result. The 1.8 dB discrepancy between the measured and simulated results is largely attributable to additional circuit losses and an elevated temperature dependent series resistance in the varactors.

The multiplier was also evaluated at cryogenic temperatures in a calibrated dewar. The measured efficiency was 61% at an input power of 150 mW and a block temperature of 14 K. The efficiency dropped to 48% at an input power of 365 mW and output power of 175 mW. The 175 mW output power level should be sustainable at cryogenic temperatures. The 3 dB output power bandwidth was approximately 17% at both 14 K and 295 K, and exhibited only a weak temperature dependence.

A major emphasis of this work was the development of robust design methodologies for the planar varactor chip and the doubler circuit. A detailed description of the design philosophy for the nonlinear planar varactor chips was given in Chapter 3. The inherent tradeoffs between power handling, epitaxial doping, physical geometry, and power dissipation were discussed. The design methodology used for the linear doubler circuits was described in Chapter 4. The close agreement between the measured and simulated results provides a great deal of confidence in the simulation tools and the design techniques.

A broadband, fixed-tuned, high power 80/160 GHz frequency doubler was also

designed. The 80/160 GHz doubler is essentially a scaled version of the 40/80 GHz doubler. However, whereas the 40/80 GHz doubler employed an SB13T1 varactor chip with six anodes, the 80/160 GHz doubler employed a four anode chip. The reduction in the number of anodes was necessary due to the reduction in the waveguide height.

Simulations for the 80/160 GHz doubler show efficiency and bandwidth similar to the 40/80 GHz design for the case of an assumed 3 Ω per varactor series resistance. Circuit losses in the waveguide, microstrip and quartz are expected to be less than 1 dB. The circuit losses should have little effect on the bandwidth but will slightly reduce the efficiency and output power.

7.5 Suggestions for Future Research

The circuits developed for the balanced doublers, although very successful, represent only one possible solution. Major scientific projects such as the National Radio Astronomy's Millimeter-Wave Array require millimeter-wave and submillimeter-wave sources with very large bandwidths. Redesigns of the 40/80 GHz and 80/160 GHz doublers could be undertaken to cover entire waveguide bands (typically 35% bandwidth). There will have to be a trade-off in output power and efficiency to achieve the higher bandwidth. The input frequency matching circuit used in the 40/80 GHz and 80/160 GHz doublers is very simple and a more elaborate impedance matching network may yield the necessary bandwidth.

A 160/320 GHz doubler and perhaps a 320/640 GHz doubler could be designed with the same basic topology used in the 40/80 GHz and 80/160 GHz doublers. The new doublers would require new varactor chip designs and a reduction in the number of anodes on the chip.

Higher order effects such as velocity saturation and plasma resonance will become more of a problem at the higher frequencies. Also, the parasitic capacitances, C_{pp} and C_{fp}, will eventually begin to dominate the junction capacitance and significantly impact the multiplication efficiency. Methods for reducing these parasitics should be investigated such as removing the semi-insulating GaAs substrate.

The reliability of the design process should lead to further integration of the planar varactor chip and the embedding circuit. This integration may not be feasible for the 40/80 GHz doubler where the circuit dimensions were approximately 800×8000 μm. However, at higher frequencies where the circuit dimensions are smaller and the uncertainties in the alignment of discrete varactor chips and circuits becomes more of a problem, the integration of the circuit and chip becomes a much more appealing alternative. Integration also reduces the number of steps required to achieve final assembly of the doubler. Alternative waveguide block technologies should also be pursued such as Si micro-machining in order to achieve tighter tolerances on the waveguide dimensions which becomes more important at the higher frequencies.

Appendix A

Penfield-Rafuse Varactor Frequency Doubler Analysis

Units $mW := 10^{-3}\cdot watt \quad \mu m \equiv 10^{-6}\,THz \equiv 10^{12}\cdot Hz \quad mils \equiv 10^{-3}\cdot inch \quad fF := 10^{-15}\cdot farad$

GaAs constants

$\varepsilon_r := 13.1$ Relative permittivity of GaAs

$N_c := 4.7\cdot 10^{17}\cdot cm^{-3}$ Effective density of states in the conduction band

$\phi := 0.95\cdot volt$ Barrier height (not built in voltage)

$m_e := 0.068$ Effective mass coefficient

$RC := m_e\cdot 120\cdot amp\cdot cm^{-2}\cdot K^{-2}$ Richardson constant (Material dependent)

$T := 300\cdot K$ Ambient temperature

$\nu_{max} := 2\cdot 10^{7}\cdot cm\cdot sec^{-1}$ Maximum average electron velocity

Physical constants

$k := 1.38\cdot 10^{-23}\cdot joule\cdot K^{-1}$ Boltzmann's constant

$q := 1.602\cdot 10^{-19}\cdot coul$ Electron charge

$\varepsilon_o := 8.854\cdot 10^{-14}\cdot farad\cdot cm^{-1}$ Permittivity of free space

$\mu_o := 4\cdot\pi\cdot 10^{-9}\cdot henry\cdot cm^{-1}$ Permeability of free space

$m_o := 0.911\cdot 10^{-30}\cdot kg$ Electron mass

Breakdown voltage (curve fit to Sze's data)

$$V_{br1} := 10^{29.38-2.733\cdot\log\left(N_D\cdot cm^3\right)+0.06323\cdot\log\left(N_D\cdot cm^3\right)^2}$$

Misc. Calculations

$r_a := \frac{D}{2}$ $A_a := \pi\cdot r_a^{\,2}$ $\omega_o := 2\cdot\pi\cdot f_o$

Mobility and conductivity

$$\mu_{epi} := \frac{10^4}{1+\sqrt{\frac{N_D}{10^{17}\cdot cm^{-3}}}}\cdot cm^2\cdot volt^{-1}\cdot sec^{-1}$$ Epi layer mobility

$$\mu_{buf} := \frac{10^4}{1 + \sqrt{\frac{n_{buf}}{10^{17}\cdot cm^{-3}}}} \cdot cm^2 \cdot volt^{-1} \cdot sec^{-1}$$ n+ buffer mobility

$\sigma_{epi} := q \cdot \mu_{epi} \cdot N_D$ Epi layer conductivity

$\sigma_{buf} := q \cdot \mu_{buf} \cdot n_{buf}$ n+ buffer conductivity

Series resistance and skin depth

$$\delta_{buf} := \frac{1}{\sqrt{\pi \cdot f_o \cdot \mu_o \cdot \sigma_{buf}}}$$ Skin depth in buffer

In the calculation of the spreading resistance, use the buffer thickness instead of the buffer skin depth if the thickness is less than the skin depth.

$d_{buf} := if(\delta_{buf} > t_{buf}, t_{buf}, \delta_{buf})$

$$R_{epi} := \frac{t_{epi}}{\sigma_{epi} \cdot A_a}$$ Series resistance from epi layer

$$R_{skin} := \frac{1}{2 \cdot \pi \cdot d_{buf} \cdot \sigma_{buf}} \cdot \ln\left(\frac{r_{oc}}{r_a}\right)$$

$$R_{spread} := \frac{1}{4 \cdot \pi \cdot d_{buf} \cdot \sigma_{buf}}$$ Spreading resistance in the buffer.

$$R_{ohmic} := \frac{2 \cdot 10^{-6} \cdot ohm \cdot cm^2}{A_{ohmic}}$$ Series resistance of ohmic contact.

$R_s := R_{epi} + R_{skin} + R_{spread} + R_{ohmic}$ Total series resistance (ohms)

Plasma resonance

$$\omega_d := \frac{\sigma_{epi}}{\varepsilon_r \cdot \varepsilon_o}$$ GaAs frequency

$$\omega_s := \frac{q}{m_o \cdot m_e \cdot \mu_{epi}}$$ Substrate frequency

$\omega_p := \sqrt{\omega_d \cdot \omega_s}$ Plasma resonance radian frequency

$$f_p := \frac{\omega_p}{2 \cdot \pi}$$ Plasma resonance frequency

$b := 1.5$ Fringing capacitance fit parameter (Copeland, IEEE-ED17 1970)

$V_n := \frac{-k \cdot T}{q} \cdot \ln\left(\frac{N_D}{N_c}\right)$ (Ec-Ef)/q

$V_{bi} := \phi - V_n$ Built in voltage.

$W_{bi} := \sqrt{\frac{2 \cdot V_{bi} \cdot \varepsilon_r \cdot \varepsilon_o}{q \cdot N_D}}$ Zero bias depletion width.

$W_{br} := \sqrt{\frac{2 \cdot V_{br} \cdot \varepsilon_r \cdot \varepsilon_o}{q \cdot N_D}}$ Breakdown depletion width.

$\gamma := 1 + \frac{b \cdot W_{bi}}{r_a}$ Fringing capacitance factor

$C_{jo} := \frac{\gamma \cdot \varepsilon_r \cdot \varepsilon_o \cdot A_a}{W_{bi}}$ Zero bias junction capacitance

$C_{jo} := \sqrt{\frac{q \cdot N_D \cdot \varepsilon_r \cdot \varepsilon_o}{2 \cdot V_{bi}}} \cdot A_a \cdot \gamma$ Zero bias junction capacitance

Saturation current

$I_{sat} := RC \cdot A_a \cdot T^2 \cdot e^{-\frac{q \cdot \phi}{k \cdot T}}$ Reverse saturation current

Velocity Saturation

$I_{max} := q \cdot N_D \cdot A_a \cdot \nu_{max}$ Velocity saturation current

Begin Penfield-Rafuse doubler analysis

Junction capacitance extrema

$C_{min} := \sqrt{\frac{q \cdot N_D \cdot \varepsilon_r \cdot \varepsilon_o}{2 \cdot (V_{bi} + V_{br})}} \cdot A_a \cdot \gamma$ Junction capacitance at reverse breakdown.

$C_{max} := \sqrt{\frac{q \cdot N_D \cdot \varepsilon_r \cdot \varepsilon_o}{2 \cdot (V_{bi} - 0.7 \cdot volt)}} \cdot A_a \cdot \gamma$ Junction capacitance near flatband.

$S_{max} := \frac{1}{C_{min}}$ Maximum elastance (at breakdown)

$S_{min} := \frac{1}{C_{max}}$ Minimum elastance (at flatband)

Cutoff frequency and normalization power

$\omega_c := \frac{S_{max} - S_{min}}{R_s}$ Cutoff radian frequency

$f_c := \frac{\omega_c}{2 \cdot \pi}$ Cutoff frequency

$P_n := \frac{(V_{br} + V_{bi})^2}{R_s}$ Normalization power

$c1 := \frac{\omega_c}{2 \cdot \omega_o}$

Solve for modulation ratios

$i := 1 .. 25$

$m1_i := 0.01 \cdot i$

$m2_i := \frac{-\frac{1}{c1} + \sqrt{\frac{1}{c1^2} + (m1_i)^2}}{2}$ $m2p_i := \frac{-\frac{1}{2 \cdot c1} + \sqrt{\frac{1}{4 \cdot c1^2} + \frac{(m1_i)^2}{2}}}{2}$

$x1 := 0.1$ $x2 := 0.1$ *Initial values*

Given

$$0 = \frac{1}{\left[3 + \sqrt{1 + 32 \cdot \left(\frac{x2^2}{x1^2}\right)}\right] \cdot \sqrt{\frac{1}{2} + \left(\frac{x1^2}{32 \cdot x2^2}\right) \cdot \left[\sqrt{1 + 32 \cdot \left(\frac{x2^2}{x1^2}\right)} - 1\right]}} - x1$$

$x2 > 0$

$f(x1) := \text{Find}(x2)$

$ff_i := f(m1_i)$

Given

$$0 = \frac{1}{\left[3+\sqrt{1+32\cdot\left(\frac{x2^2}{x1^2}\right)}\right]\cdot\sqrt{\frac{1}{2}+\left(\frac{x1^2}{32\cdot x2^2}\right)\cdot\left[\sqrt{1+32\cdot\left(\frac{x2^2}{x1^2}\right)}-1\right]}} - x1$$

$$0 = \frac{-\frac{1}{2\cdot c1}+\sqrt{\frac{1}{4\cdot c1^2}+\frac{x1^2}{2}}}{2} - x2$$

$$\begin{pmatrix} optm1 \\ optm2 \end{pmatrix} := \text{Find}(x1, x2)$$

Optimum embedding impedances

$R_1 := R_s\cdot(2\cdot optm2\cdot c1 + 1)$ Input embedding resistance

$R_2 := R_s\cdot\left(\frac{optm1^2}{2\cdot optm2}\cdot c1 - 1\right)$ Output embedding resistance

Average capacitance

$$C_{avg} := \left[\frac{1}{(V_{br}+V_{bi}-0.1\cdot volt)}\right]\cdot\int_{-V_{br}}^{V_{bi}-0.1\cdot volt}\sqrt{\frac{q\cdot N_D\cdot\varepsilon_r\cdot\varepsilon_o}{2\cdot(V_{bi}-V_d)}}\cdot A_a\cdot\gamma\, dV_d$$

$X_1 := \frac{1}{(\omega_o\cdot C_{avg})}$ Input reactance

$X_2 := \frac{1}{(2\cdot\omega_o\cdot C_{avg})}$ Output reactance

$Z_1 := R_1 + j\cdot X_1$ Input embedding impedance

$Z_2 := R_2 + j\cdot X_2$ Output embedding impedance

Optimum doubler efficiency and power

$$\eta := \frac{c1-\frac{2\cdot optm2}{optm1^2}}{c1+\frac{1}{2\cdot optm2}}\cdot 100$$ Doubler efficiency

$$P_{in} := 8\cdot P_n\cdot\left(\frac{S_{max}-S_{min}}{S_{max}+S_{min}}\right)^2\cdot\left(\frac{1}{2\cdot c1}\right)^2\cdot optm1^2\cdot(2\cdot optm2\cdot c1+1)$$ Input power

$$P_{out} := 8 \cdot P_n \cdot \left(\frac{S_{max} - S_{min}}{S_{max} + S_{min}} \right)^2 \cdot \left(\frac{1}{c1} \right)^2 \cdot optm2^2 \cdot \left(\frac{optm1^2}{2 \cdot optm2} \cdot c1 - 1 \right)$$ Output power

$$P_{diss} := 8 \cdot P_n \cdot \left(\frac{S_{max} - S_{min}}{S_{max} + S_{min}} \right)^2 \cdot \left(\frac{1}{2 \cdot c1} \right)^2 \cdot \left(optm1^2 + 4 \cdot optm2^2 \right)$$ Dissipated power

Semiconductor device parameters (Operator input required)

$N_D \equiv 1 \cdot 10^{17} \cdot cm^{-3}$ Epi doping concentration

$n_{buf} \equiv 5.5 \cdot 10^{18} \cdot cm^{-3}$ n+ (buffer) doping density

$V_{br} \equiv 14.0 \cdot volt$ Reverse breakdown voltage

$t_{epi} \equiv 0.5 \cdot \mu m$ Epi layer thickness

$t_{buf} \equiv 8.0 \cdot \mu m$ Buffer (n++) layer thickness

$D \equiv 13 \cdot \mu m$ Anode diameter

$A_{ohmic} \equiv 1600 \cdot \mu m^2$ Ohmic contact area

$r_{oc} \equiv \frac{D}{2} + 6 \cdot \mu m$ Radius of ohmic contact

$f_o \equiv 40 \cdot GHz$ Doubler input frequency

Computed Values

$P_{in} = 39.6 \cdot mW$ Input power

$P_{out} = 33.9 \cdot mW$ Output power

$P_{diss} = 5.7 \cdot mW$ Power dissipated in the series resistance

$\eta = 85.6$ % Multiplier efficiency

$R_s = 0.82 \cdot ohm$ Total series resistance

$C_{jo} = 138 \cdot fF$ Zero bias junction capacitance

$Z_1 = (8.3 + 62.8i) \cdot ohm$ Input embedding impedance

$Z_2 = (15.7 + 31.4i) \cdot ohm$ Output embedding impedance

$R_{epi} = 0.47 \cdot ohm$ Series resistance in epi layer

$R_{skin} = 0.128 \cdot ohm$ Series resistance in buffer

$R_{spread} = 0.098 \cdot ohm$ Spreading resistance in buffer

$R_{ohmic} = 0.125 \cdot ohm$ Ohmic contact resistance

$I_{sat} = 0 \cdot amp$ Saturation current (A)

$W_{bi} = 0.1148 \cdot \mu m$ Zero bias depletion width

$W_{br} = 0.4502 \cdot \mu m$ Breakdown depletion width

$t_{buf} = 8 \cdot \mu m$ Buffer layer thickness

$\delta_{buf} = 7.7774 \cdot \mu m$ Skin depth in buffer

$\phi = 0.95 \cdot volt$ Barrier voltage

$V_{bi} = 0.91 \cdot volt$ Built in voltage

$V_{br1} = 15.6$ Curve fit to Sze table

$n_{buf} = 5.5 \cdot 10^{18} \cdot cm^{-3}$ n++ doping concentration

$\mu_{epi} = 5 \cdot 10^{3} \cdot cm^{2} \cdot volt^{-1} \cdot sec^{-1}$ Epi layer mobility

$\mu_{buf} = 1.188 \times 10^{3} \cdot s^{-1} \cdot cm^{2} \cdot volt^{-1}$ n++ mobility

$\sigma_{epi} = 8.01 \times 10^{3} \cdot C^{2} \cdot m^{-3} \cdot s \cdot kg^{-1}$ Epi layer conductivity

$\sigma_{buf} = 1.047 \times 10^{5} \cdot C^{2} \cdot m^{-3} \cdot s \cdot kg^{-1}$ n++ conductivity

$f_c = 5.024 \cdot THz$ Cutoff frequency

$f_p = 3.0079 \cdot THz$ Plasma resonance frequency

$\frac{X_1}{R_1} = 7.6$ Input Q, Xin/Rin

$\frac{X_2}{R_2} = 2$ Output Q, Xout/Rout

$C_{min} = 34 \cdot fF$ Minimum capacitance

$C_{max} = 286.6 \cdot fF$ Maximum capacitance

$C_{avg} = 63.4 \cdot fF$ Average capacitance

$\frac{C_{max}}{C_{min}} = 8.43$

$I_{max} = 0.4253 \cdot amp$ Velocity saturation current

Appendix B

An Analysis of Energy and Power in a Varactor

It was shown in Chapter 3 that the maximum power level that a varactor can handle is dependent on the epitaxial doping, the anode diameter, and the heat conduction path. The analysis in Chapter 3 was based on data obtained from harmonic balance and Penfield-Rafuse simulations. In the analysis presented here, only the nonlinear junction capacitance is considered and therefore the problems with heat conduction arising from power dissipation in the series resistance are ignored.

As a starting point, an algebraic expression for the total energy required to remove all electrons in the epitaxial layer from the region between w(0) and w(-V_{br}) is derived. This energy represents the maximum energy, U_{max} , that can be stored in the varactor. It will then be possible to relate U_{max} to a maximum average power. Eq. B.1 gives an expression for the maximum energy.

$$U_{max} = \int_{depletion\ region} (V_{bi} - V_j) \cdot dQ = \int_{w(0)}^{w(-V_{br})} (V_{bi} - V_j) \cdot q \cdot N_D \cdot A_a \cdot dw \qquad \text{(B.1)}$$

Using eq. 3.3 in eq. B.1 yields,

$$U_{max} = \int_{w(0)}^{w(-V_{br})} \left(\frac{w^2 \cdot q \cdot N_D}{2 \cdot \varepsilon_s} \right) \cdot q \cdot N_D \cdot A_a \cdot dw \qquad \text{(B.2)}$$

For abrupt junction varactors, the solution to eq. B.2 is given by eq. B.3.

$$U_{max} = A_a \cdot (2 \cdot q \cdot \varepsilon_s \cdot N_D)^{\frac{1}{2}} \cdot \left[\frac{1}{3}(V_{br} + V_{bi})^{\frac{3}{2}} - V_{bi}(V_{br} + V_{bi})^{\frac{1}{2}}\right] \quad \text{(B.3)}$$

Eq. B.3 shows that U_{max} is directly proportional to the anode area. The relationship between the energy and the doping is somewhat more complex. Eq. B.3 shows that $U_{max} \propto N_D^{0.5}(V_{br}^{1.5} - V_{br}^{0.5})$ and Eq. 3.2 gives $V_{br} \propto N_D^{-0.77}$. Combining these results yields $U_{max} \propto (N_D^{-0.655} - N_D^{0.115})$.

Fig. B.1 shows a plot of energy versus doping as calculated in eq. B.3, a curve fit to the data using the proportionality described above, and a plot of the total number of electrons swept out of the region between $w(-V_{br})$ and $w(0)$. The data in Fig. B.1 shows that the total energy required to remove all of the electrons between $w(0)$ and $w(-V_{br})$ decreases as the doping increases. Also, the total number of electrons moved increases in higher doped materials. Neither of these results may seem intuitive, and taken together, the two results may even appear contradictory. The dominant mechanism at work is the relationship between the doping level and the reverse breakdown voltage. The energy required to move a charge is dependent on the junction voltage, and although fewer charges are moved in lower doped materials, many of those charges are moved at higher potentials and thus more energy is required to move them.

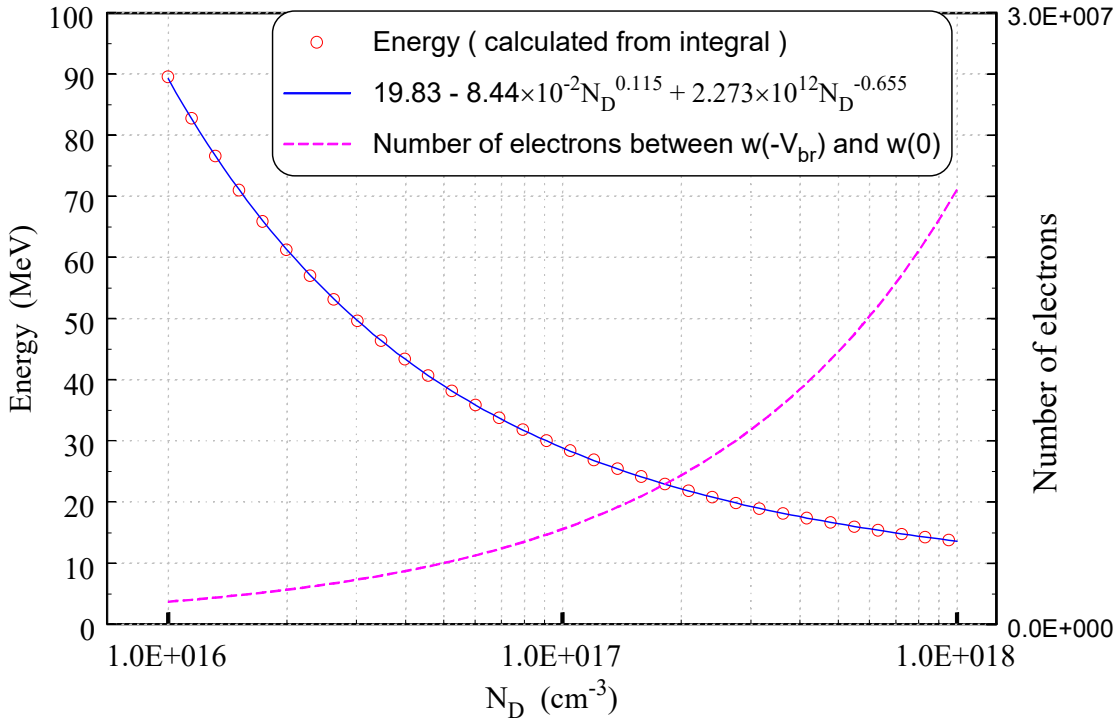


Fig. B.1. Calculated energy, energy curve fit, and number of electrons moved.

If we assume a sinusoidal excitation of the varactor at frequency f_0 , then the maximum average power that could be absorbed by the varactor would be given by dividing the maximum energy by the period of the excitation.

$$P_{max} = U_{max} \cdot f_0 \tag{B.4}$$

Appendix C

A Simple Equivalent Circuit for Heat Flow

A simple heat flow model analogous to an electrical circuit is developed in this section and a simple example is presented. The basic concepts are extended to construct a slightly more complicated model to examine heat flow in the SB13T1 planar varactor chip and the embedding circuit of the 40/80 GHz doubler. The goal is to obtain an estimate of the ambient temperature in the SB13T1 varactor and determine if there are any hot spots in the device since high operating temperatures can damage a varactor and significantly reduce the lifetime of the device. If high temperatures are found, then corrective action may be advisable such as lowering the input power or improving the heat conduction path by redesigning the varactor chip or the circuit.

The ability of a material to conduct heat is characterized by a quantity known as the thermal conductivity, σ_T , which has units of $W \cdot m^{-1} \cdot K^{-1}$. The thermal resistance, R_T , of a homogenous material with uniform cross-sectional area, A, and length, l, is given by,

$$R_T = \frac{l}{\sigma_T \cdot A}, \left(\frac{K}{W}\right) \tag{C.1}$$

A simple equivalent electrical circuit can be constructed using thermal resistances in conjunction with heat sources. The equivalencies are given in eq. C.2 along with appropriate units.

$$\begin{aligned} Thermal\ resistance,\ R_T,\ \left(\frac{K}{W}\right) &\leftrightarrow Electrical\ resistance, R, (\Omega) \\ Heat\ flow,\ q_T,\ (W) &\leftrightarrow Electrical\ current, I, (A) \\ Temperature,\ T, (K) &\leftrightarrow Voltage, V, (volts) \\ Heat\ source &\leftrightarrow Current\ source \end{aligned} \tag{C.2}$$

Fig. C.1 shows the equivalent circuit for a Au rod with σ_T = 298 W·m^{-1}·K^{-1}, l = 10 mils, A = 0.785 mil^2 (1 mil diameter gold wire). The rod is connected to a heat source of 21 mW at one end and an infinite heat well at T_0 = 300 K at the other end. The temperature, T, of the end of the rod connected to the heat source is given by eq. C.3.

$$T = T_0 + q_T \cdot \left(\frac{l}{\sigma_T \cdot A}\right) = 300K + (21mW) \cdot \left(\frac{10mil}{\left[7.57\frac{mW}{mil \cdot K}\right] \cdot [0.785mil^2]}\right) = 335\ K \qquad \text{(C.3)}$$

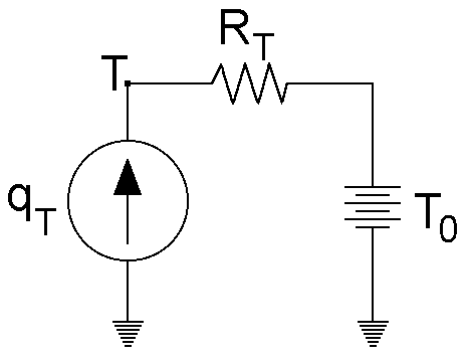


Fig. C.1. Heat flow model for a simple rod.

Heat is generated in Schottky varactors due to power dissipation in the series resistance. Most of the heat is generated in or near the epitaxial layer since R_{epi} typically represents the largest contribution to the series resistance. In this analysis, the heat is modeled as a point source located in the epitaxial layer. This procedure should somewhat overestimate the ambient temperature near the anodes.

Fig. C.2 shows a heat conduction circuit superimposed on a sketch of the SB13T1 varactor chip mounted in the 40/80 GHz doubler block. Only one half of the chip is shown since the heat conduction model is symmetric. The full SB13T1 varactor has 6 anodes, so the heat model has three sources. The chip is flip mounted onto metal pads on a quartz substrate.

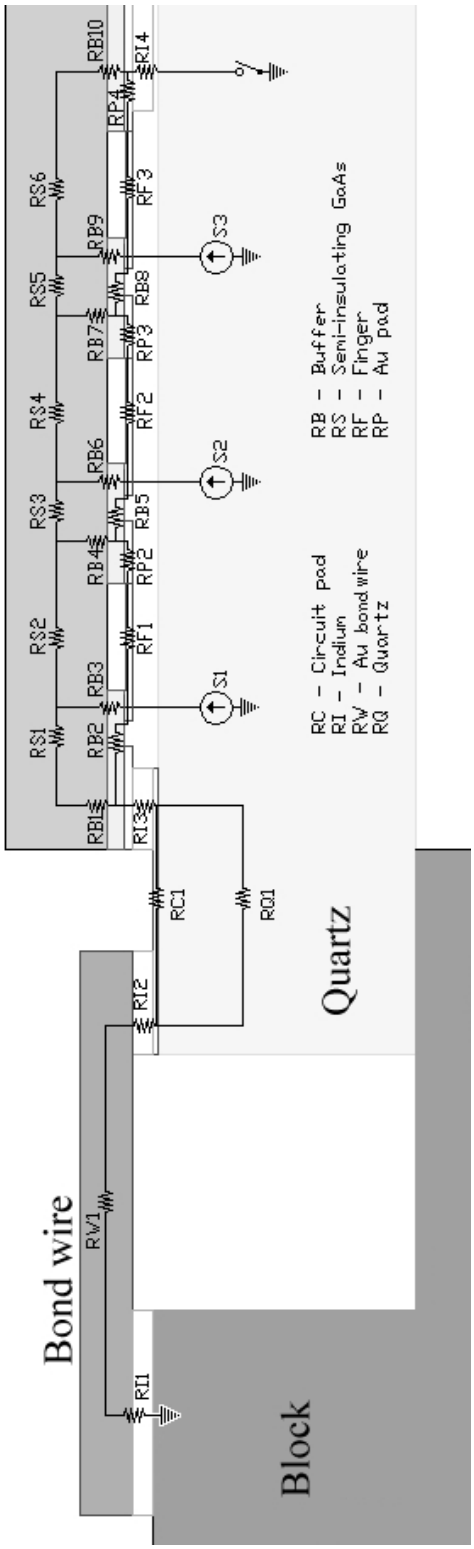


Fig. C.2. Heat flow model for the SB13T1 varactor mounted in the 40/80 GHz doubler.

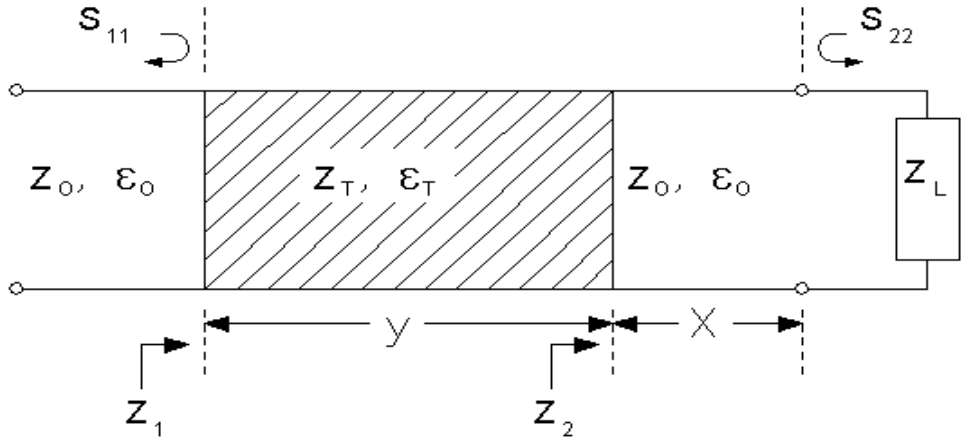
A 1 mil diameter gold bond wire runs from the circuit pad at the edge of the quartz substrate to the metal block. Heat energy is restricted to flow from the anodes, through the GaAs chip (σ_T = 46 W·m^{-1}·K^{-1}), out the end of the GaAs chip to the bond wire (σ_T = 298 W·m^{-1}·K^{-1}), and through the bond wire to the metal block. The metal block is treated as an infinite heat well at temperature, T_0 = 27° C. Radiative cooling is ignored.

A worst case estimate of 7 mW/source was used in the analysis although the dissipated power per anode was calculated to be closer to 5 mW at an input power level of 200 mW. The quartz substrate was actually made from fused silica which has a poor thermal conductivity (σ_T = 1.4 W·m^{-1}·K^{-1}). For this reason, the simulation was run with a perfect insulating boundary at the split in the varactor chip, ie. the model was open circuited at that point. Under these constraints, the peak temperature was calculated to be 90° C at the anode closest to the open circuit (at source S3 of Fig. C.2).

Some heat would actually flow out to the quartz circuit through the center contact pad of the varactor. If a substrate with a better thermal conductivity were used such as Z-cut crystalline quartz, aluminum nitride or diamond, then the thermal situation would be greatly improved. The simulation was rerun for the case where the perfect insulating boundary was replaced with a direct connection to an infinite heat well at T_0 = 27° C. The peak temperature was calculated to be 44° C at the center anode of the diagram in Fig. C.2 (at source S2).

Derivation of the Quarter-Wave Teflon Transformer Technique

This MathCad program describes the quarter-wave Teflon transformer technique used to evaluate the output match of the 40/80 GHz balanced doubler.



Misc. data for E-band waveguide (60-90 GHz) at f = 82 GHz.
Dimensions: a=3100 μm, b=1550 μm

Parameter	(Teflon)	(air)
Zpi (S)	176	288
Zpv (S)	285	467
Zvi (S)	224	366

Procedure:

1 - Measure the output power, P_m, of the device for some given input power and bias.

$P_m := 94.4$ Measured output power, Pin=200 mW, η = 48 %.

2 - Insert a Teflon transformer and measure the output power as a function of transformer position.

This need only be done for $\Delta x = \lambda/2$, but $\Delta x = \lambda$ is recommended. Call these values $P_T(x)$.

3 - Divide the minimum value of $P_T(x)$ by the maximum value of $P_T(x)$. Call this quantity P_{TR} .

$P_{Tmax} = 84.5$ Measured maximum output power using Teflon transformer, Pin=200 mW.

$P_{Tmin} = 72.5$ Measured minimum output power using Teflon transformer, Pin=200 mW.

$$P_{Tr} = \frac{P_{Tmin}}{P_{Tmax}}$$ Ratio of the measured power extrema with the Teflon transformer. [1]

Derivation of Equations

Referring to the diagram above, we can calculate Z_2 as,

$$Z_2(x) = Z_0 \cdot \frac{Z_L + j \cdot Z_0 \cdot \tan(\beta x)}{Z_0 + j \cdot Z_L \cdot \tan(\beta x)} \quad [2]$$

Similarly, we can calculate $Z_1(x,y)$ in terms of $Z_2(x)$ and the length, y, of the Teflon transformer as,

$$Z_1(x,y) = Z_T \cdot \frac{Z_2(x) + j \cdot Z_T \cdot \tan(\beta y)}{Z_T + j \cdot Z_2(x) \cdot \tan(\beta y)} \quad [3]$$

If the Teflon transformer is $\lambda/4$ in length, then $\beta y = \pi/2$ and we can write,

$$Z_1(x) = Z_T \cdot \frac{Z_2(x) + j \cdot Z_T \cdot \tan\left(\frac{\pi}{2}\right)}{Z_T + j \cdot Z_2(x) \cdot \tan\left(\frac{\pi}{2}\right)} = \frac{{Z_T}^2}{Z_2(x)} \quad [4]$$

Inserting the expression for $Z_2(x)$ [2] into [4] gives,

$$Z_1(x) = \frac{{Z_T}^2}{Z_0} \cdot \frac{\left(Z_0 + j \cdot Z_L \cdot \tan(\beta x)\right)}{\left(Z_L + j \cdot Z_0 \cdot \tan(\beta x)\right)} \quad [5]$$

We can now generate values for the reflection coefficient, S_{11}, looking into the doubler block (and the Teflon transformer) from the output waveguide flange.

$$S_{11}(x) = \frac{Z_1(x) - Z_0}{Z_1(x) + Z_0} \quad [6]$$

We can also calculate the standing wave here.

$$SWR(x) = \frac{\left(1 + \left|S_{11}(x)\right|\right)}{\left(1 - \left|S_{11}(x)\right|\right)} \quad [7]$$

We now calculate a normalization power and the ratio of the maximum to minimum normalized power.

$$P_{norm}(x) = 1 - \left(\left|S_{11}(x)\right|\right)^2 \quad [8]$$

$$P_{nr} = \frac{\min\left(P_{norm}(x)\right)}{\max\left(P_{norm}(x)\right)} \quad [9]$$

In the following analysis, we assume that the available second harmonic power generated by the varactors, P_{av}, is independent of the output match (ie. the varactor chip is a perfect isolated power source). This assumption is of course not absolutely true. 111

There are a number of interesting features in the above equations. Values of $S_{11}(x)$ lie on a circle which is centered on the real axis on the left half of the Smith chart. This is true for all possible complex values of Z_L. (Circles centered on the right side of the real axis require a transformer impedance, Z_T, greater than the air filled waveguide impedance, Z_0.)

The extrema of $|S_{11}(x)|$ lie on the real axis.

$$\max\left(\left|S_{11}(x)\right|\right) = \left|\frac{\min\left(\mathrm{Re}\left(Z_1(x)\right)\right) - Z_0}{\min\left(\mathrm{Re}\left(Z_1(x)\right)\right) + Z_0}\right| \quad [10]$$

$$\min\left(\left|S_{11}(x)\right|\right) = \left|\frac{\max\left(\mathrm{Re}\left(Z_1(x)\right)\right) - Z_0}{\max\left(\mathrm{Re}\left(Z_1(x)\right)\right) + Z_0}\right| \quad [11]$$

The extrema of $\mathrm{Re}(Z_1(x))$ occur for $\beta x = 0, \pi/2$ and are given as,

$$\max\left(\mathrm{Re}\left(Z_1(x)\right)\right) = \frac{Z_T^{\,2}}{Z_L} \quad [12]$$

$$\min\left(\mathrm{Re}\left(Z_1(x)\right)\right) = \left(\frac{Z_T}{Z_0}\right)^2 \cdot Z_L \quad [13]$$

We can insert the expressions [12, 13] into expressions [10, 11] to get,

$$\max\left(\left|S_{11}(x)\right|\right) = \left|\frac{Z_T^{\,2} \cdot Z_L - Z_0^{\,3}}{Z_T^{\,2} \cdot Z_L + Z_0^{\,3}}\right| \quad [14]$$

$$\min\left(\left|S_{11}(x)\right|\right) = \left|\frac{Z_T^{\,2} - Z_0 \cdot Z_L}{Z_T^{\,2} + Z_0 \cdot Z_L}\right| \quad [15]$$

Since Z_T, Z_L, and Z_0 are all positive and > 0,

$$\max\left(\left|S_{11}(x)\right|\right) = \frac{\left|Z_T^{\,2} \cdot Z_L - Z_0^{\,3}\right|}{Z_T^{\,2} \cdot Z_L + Z_0^{\,3}} \quad [16]$$

$$\min\left(\left|S_{11}(x)\right|\right) = \frac{\left|Z_T^{\,2} - Z_0 \cdot Z_L\right|}{Z_T^{\,2} + Z_0 \cdot Z_L} \quad [17]$$

To calculate P_{norm} in expression [8], we need expressions for the $|S_{11}|^2$ extrema. It is advantageous to note that the value to Z_L is in general complex, but we need only consider real values. This is equivalent to moving our initial reference plane for $|S_{22}|$ closer to the varactors or further from the varactors along the transmission line of impedance Z_0 to one of the two points where Z_L is purely real. This allows us to simplify the expressions for the $|S_{11}|^2$ extrema.

$$\max\left[\left(\left|S_{11}(x)\right|\right)^2\right] = \frac{\left(\left|Z_T^2 \cdot Z_L - Z_0^3\right|\right)^2}{\left(Z_T^2 \cdot Z_L + Z_0^3\right)^2} = \frac{\left(Z_T^2 \cdot Z_L - Z_0^3\right)^2}{\left(Z_T^2 \cdot Z_L + Z_0^3\right)^2} \quad [18]$$

$$\min\left[\left(\left|S_{11}(x)\right|\right)^2\right] = \frac{\left(\left|Z_T^2 - Z_0 \cdot Z_L\right|\right)^2}{\left(Z_T^2 + Z_0 \cdot Z_L\right)^2} = \frac{\left(Z_T^2 - Z_0 \cdot Z_L\right)^2}{\left(Z_T^2 + Z_0 \cdot Z_L\right)^2} \quad [19]$$

The extrema of P_{norm} in [8] can now be written in terms of the $|S_{11}|^2$ extrema in [18, 19].

$$\max\left(P_{norm}(x)\right) = \left[1 - \frac{\left(Z_T^2 - Z_0 \cdot Z_L\right)^2}{\left(Z_T^2 + Z_0 \cdot Z_L\right)^2}\right] = \frac{4 \cdot Z_T^2 \cdot Z_0 \cdot Z_L}{\left(Z_T^2 + Z_0 \cdot Z_L\right)^2} \quad [20]$$

$$\min\left(P_{norm}(x)\right) = \left[1 - \frac{\left(Z_T^2 \cdot Z_L - Z_0^3\right)^2}{\left(Z_T^2 \cdot Z_L + Z_0^3\right)^2}\right] = \frac{4 \cdot Z_T^2 \cdot Z_L \cdot Z_0^3}{\left(Z_T^2 \cdot Z_L + Z_0^3\right)^2} \quad [21]$$

Insert expressions [20, 21] into expression [9] for P_{nr} to get,

$$P_{nr} = \frac{\left[1 - \frac{\left(Z_T^2 \cdot Z_L - Z_0^3\right)^2}{\left(Z_T^2 \cdot Z_L + Z_0^3\right)^2}\right]}{\left[1 - \frac{\left(Z_T^2 - Z_0 \cdot Z_L\right)^2}{\left(Z_T^2 + Z_0 \cdot Z_L\right)^2}\right]} = \frac{\frac{4 \cdot Z_T^2 \cdot Z_L \cdot Z_0^3}{\left(Z_T^2 \cdot Z_L + Z_0^3\right)^2}}{\frac{4 \cdot Z_T^2 \cdot Z_0 \cdot Z_L}{\left(Z_T^2 + Z_0 \cdot Z_L\right)^2}} = \frac{Z_0^2 \cdot \left(Z_T^2 + Z_0 \cdot Z_L\right)^2}{\left(Z_T^2 \cdot Z_L + Z_0^3\right)^2} \quad [22]$$

The value of P_{nr} (the ratio of min to max normalized output powers) is unique for a given S_{11} circle. Thus, if you measure the standing wave with a $\lambda/4$ Teflon transformer, you can uniquely map P_{nr} to P_{Tr}. It is at this point that we make the assumption that P_{av} is constant and unperturbed by the Teflon.

$$P_{nr} = P_{Tr} \quad [23]$$

It is interesting to note that for the case of a perfect output match ($Z_L = Z_0$), insertion of the Teflon transformer causes the output power to drop by a factor of 0.792 for all transformer positions, $P_{nr} = 1$, and SWR = 2.68 .

All quantities in [22] are known except for Z_L. With some manipulation, we can solve for Z_L. 113

$$ZL = \frac{2\cdot Z_0^{\,3}\cdot Z_T^{\,2}\cdot\left(1-P_{nr}\right) \quad " \quad \sqrt{\left[2\cdot Z_0^{\,3}\cdot Z_T^{\,2}\cdot\left(P_{nr}-1\right)\right]^2 - 4\cdot\left(P_{nr}\cdot Z_T^{\,4} - Z_0^{\,4}\right)\cdot Z_0^{\,2}\cdot\left(P_{nr}\cdot Z_0^{\,4} - Z_T^{\,4}\right)}}{2\cdot\left(P_{nr}\cdot Z_T^{\,4} - Z_0^{\,4}\right)} \qquad [24]$$

We know that Z_L is positive and that the denominator in expression [24] is negative since $Z_0 > Z_T$ and $1 > (P_{nr} = P_{Tr}) > 0$, so we can exclude one root because it cannot yield a positive number. Therefore,

$$Z_L = \frac{\left[2\cdot Z_0^{\,3}\cdot Z_T^{\,2}\cdot\left(1-P_{Tr}\right)\right] - \sqrt{\left[2\cdot Z_0^{\,3}\cdot Z_T^{\,2}\cdot\left(P_{Tr}-1\right)\right]^2 - 4\cdot\left(P_{Tr}\cdot Z_T^{\,4} - Z_0^{\,4}\right)\cdot Z_0^{\,2}\cdot\left(P_{Tr}\cdot Z_0^{\,4} - Z_T^{\,4}\right)}}{\left[2\cdot\left(P_{Tr}\cdot Z_T^{\,4} - Z_0^{\,4}\right)\right]} \qquad [25]$$

Equation [25] gives us a value for Z_L based on measured or calculated values of Z_0, Z_T, and P_{Tr}. We can use this value of Z_L in equations [1]..[9] to find all other circuit quantities. We have lost phase information, but there is a lot of information in the magnitude data.

The available power from the varactors (for the case of a perfect match) can actually be calculated using the maximum output power with the Teflon transformer and the maximum value of the normalized power, P_{norm} ,

$$P_{av} = \left(\frac{P_{Tmax}}{\max\left(P_{norm}\right)}\right) = \frac{P_{Tmax}\cdot\left(Z_T^{\,2} + Z_0\cdot Z_L\right)^2}{\left(4\cdot Z_T^{\,2}\cdot Z_0\cdot Z_L\right)} \qquad [26]$$

Since we know the available power and the measured power without the Teflon transformer, P_m, we can calculate the magnitude of the reflection coefficient and SWR for our original circuit prior to installation of the Teflon transformer.

$$P_m = \left[1 - \left(\left|S_{11}\right|\right)^2\right]\cdot P_{av} \qquad [27]$$

$$\left|S_{11}\right| = \sqrt{1 - \frac{P_m}{P_{av}}} \qquad [28]$$

$$SWR = \frac{1 + \left|S_{11}\right|}{1 - \left|S_{11}\right|} \qquad [29]$$

Operator input required

$P_m := 94.4$ Measured output power, Pin=200 mW, η = 48 %.

$P_{Tmax} := 84.5$ Measured maximum output power using Teflon transformer, Pin=200 mW.

$P_{Tmin} := 72.5$ Measured minimum output power using Teflon transformer, Pin=200 mW.

$\rho := 1.0661$ Adjustment to get the last value of X at 100. (Shows some error in calculation of β).

$\sigma := 0.55$ Phase offset to get data match to equations. (No implied error. See graphs below).

$\beta := 1388 \cdot 25.4 \cdot 10^{-6}$ β in mils^-1

$n := 0 .. 19$ Index for arrays (had 20 data points in the measurement)

$\beta l_n := \left(\frac{\rho \cdot \pi \cdot n}{19}\right) + \sigma$ Generate values of βl .

$X_n := \left(\frac{\rho \cdot \pi \cdot n}{19 \cdot \beta}\right) + 5$ Generate values of X from 5 mils to 100 mils. $X_{19} = 100$

$Z_0 := 288$ Zpi for air filled full-height E_band waveguide at 82 GHz

$Z_T := 176$ Zpi for Teflon filled full-height E-band waveguide at 82 GHz

$P_{mt} :=$

5	79
10	76.3
15	74.5
20	73.4
25	72.8
30	72.5
35	72.6
40	72.7
45	73.2
50	...

This is actual measured output power in mW and Teflon transformer position in mils.

X-Y chart to Smith chart synthesizer

This section contains data and equations to convert an x-y rectangular plot into a Smith chart.

The variable, X153, is a table downloaded from a MATHSOFT web site which contains the data to draw the lines for a Smith chart on an x-y rectangular plot.

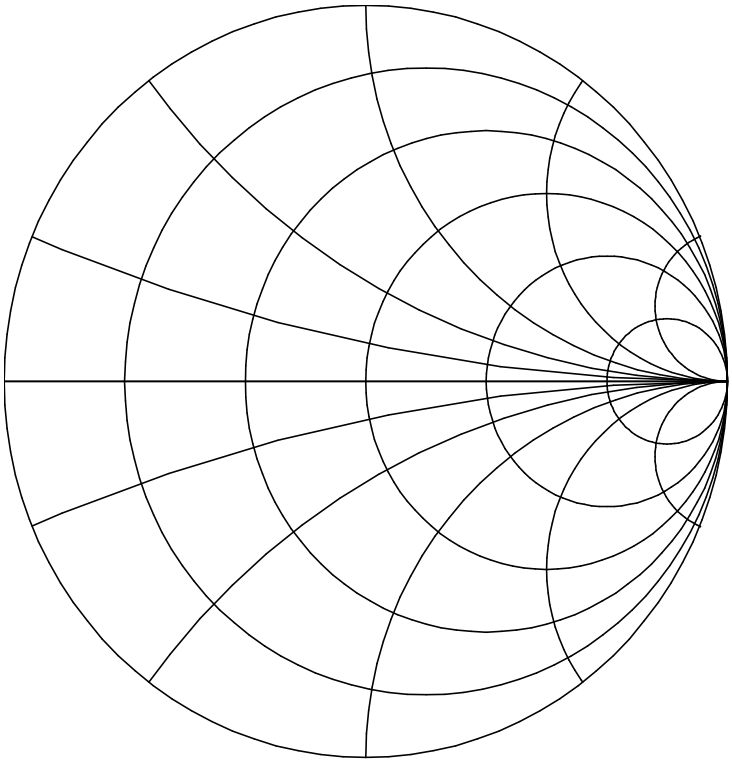
$$k153 := 0 .. rows(X153) - 1$$

$$SR153 := X153^{\langle ORIGIN \rangle}$$

$$SI153 := X153^{\langle ORIGIN+1 \rangle}$$

$X153 :=$

1	0
1	0.06
0.99	0.13
0.98	0.19
0.97	0.25
0.95	0.31
0.93	0.37
0.91	0.43
0.88	0.48
0.84	0.54
0.81	0.59
0.77	...



Smith chart

Calculations

$$P_{Tr} := \frac{P_{Tmin}}{P_{Tmax}} \qquad P_{Tr} = 0.858$$

$$Z_L := \frac{\left[\left[2\cdot {Z_0}^3\cdot {Z_T}^2\cdot\left(1 - P_{Tr}\right)\right] - \sqrt{\left[2\cdot {Z_0}^3\cdot {Z_T}^2\cdot\left(P_{Tr} - 1\right)\right]^2 - 4\cdot\left(P_{Tr}\cdot {Z_T}^4 - {Z_0}^4\right)\cdot {Z_0}^2\cdot\left(P_{Tr}\cdot {Z_0}^4 - {Z_T}^4\right)}\right]}{\left[2\cdot\left(P_{Tr}\cdot {Z_T}^4 - {Z_0}^4\right)\right]}$$

$$Z1_n := \frac{{Z_T}^2}{Z_0}\cdot\frac{\left(Z_0 + j\cdot Z_L\cdot\tan\left(\beta l_n\right)\right)}{\left(Z_L + j\cdot Z_0\cdot\tan\left(\beta l_n\right)\right)}$$

$$S11_n := \frac{Z1_n - Z_0}{Z1_n + Z_0}$$

$$SWR_n := \frac{\left(1 + \left|S11_n\right|\right)}{\left(1 - \left|S11_n\right|\right)}$$

$$P_{norm_n} := 1 - \left(\left|S11_n\right|\right)^2$$

$$P_{nr} := \frac{\min\left(P_{norm}\right)}{\max\left(P_{norm}\right)} \qquad P_{nr} = 0.859$$

$$P_{av} := \frac{P_{Tmax}}{\max\left(P_{norm}\right)} \qquad P_{av} = 99.439$$

Output power for perfect match.

$$S_{11mag} := \sqrt{1 - \frac{P_m}{P_{av}}} \qquad S_{11mag} = 0.225$$

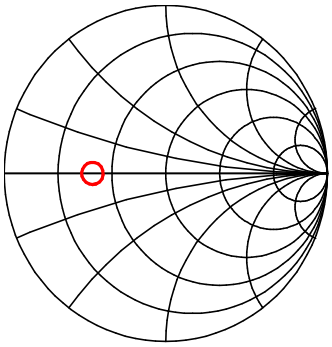
Output reflection (no Teflon).

$$SWR_{mag} := \frac{\left(1 + S_{11mag}\right)}{\left(1 - S_{11mag}\right)} \qquad SWR_{mag} = 1.581$$

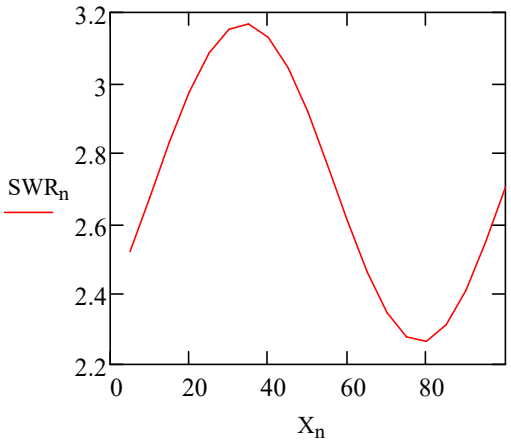
Output standing wave (no Teflon)

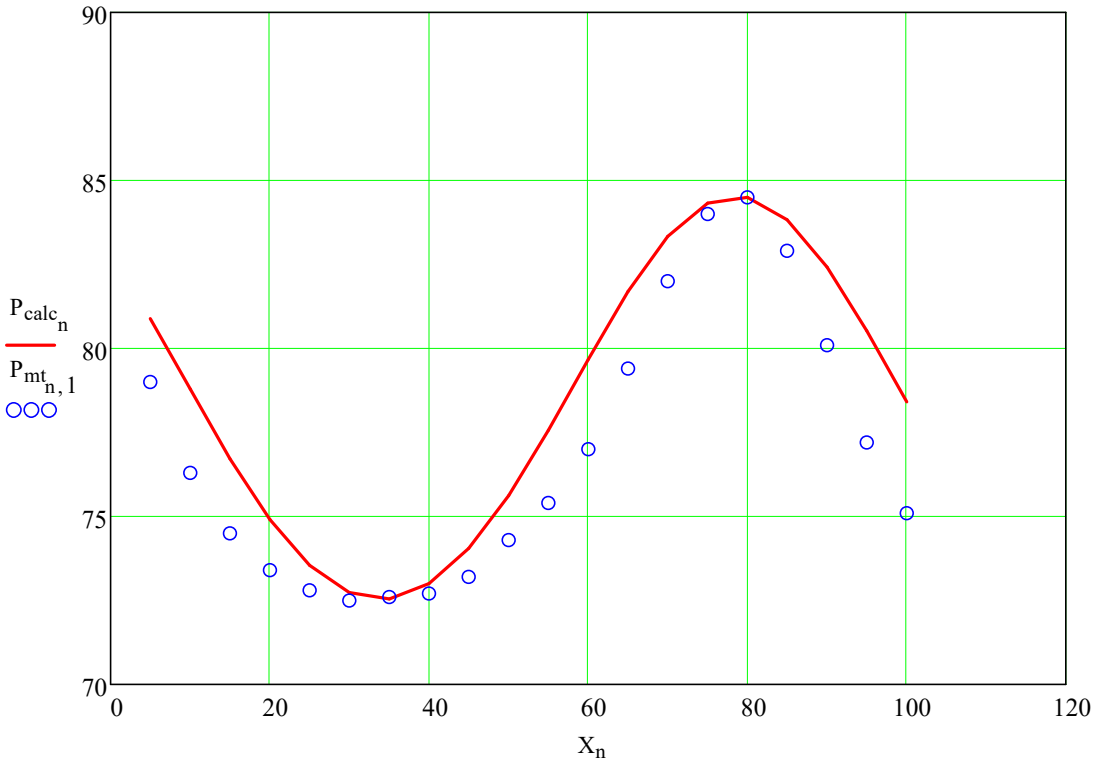
$$P_{calc_n} := P_{norm_n}\cdot P_{av}$$

The Smith chart is normalized to the output waveguide impedance Zo.



S11





$P_m = 94.4$ Measured output power with no transformer.

$P_{av} = 99.439$ Calculated output power for perfect match.

$S_{11mag} = 0.225$ Calculated output reflection (no Teflon).

$SWR_{mag} = 1.581$ Calculated output standing wave (no Teflon)

$P_{nr} = 0.859$

Appendix E

Fabrication and Assembly

Overview

This appendix describes techniques for fabricating the doubler circuits, mounting the varactors to the circuit, and mounting the circuit and varactor chip in the waveguide block. Enough detail is provided so that the reader should be able to understand the tasks involved.

Circuit Fabrication

The impedance matching networks in the 40/80 GHz and 80/160 GHz balanced doublers are composed of a circuit housed in a waveguide block. The circuit comprises a quartz substrate with a metallization pattern on one side. The term circuit is used rather loosely here since the impedance matching networks also depend on the geometry of the waveguide block. The 40/80 GHz and 80/160 GHz circuits use 127 μm (5 mil) and 76 μm (3 mil) thick quartz substrates respectively. The quartz substrates used for circuit fabrication are circular with a 2.54 cm diameter and highly polished on both sides.

The first step in the circuit fabrication process is to mount the rather fragile quartz substrate onto a thicker Si support substrate using G-wax. The wafer is then cleaned with Ethanol, Methanol, and Tetrachloroethane in a spin cleaner. A 50 A chrome seed layer is then sputtered onto the surface of the quartz, followed by a 500-1000 A gold seed layer. The chrome seed layer provides good adhesion to the quartz surface, but has a much lower conductivity than gold. To minimize circuit losses, the chrome layer is typically very thin.

A 3.8 μm photoresist layer is spun onto the gold surface, exposed to UV through a photomask and developed. A nominal 3 μm gold layer is then plated on the exposed gold seed layer. The photoresist is then removed and the wafer was exposed to a short gold etch followed by a short chrome etch to remove the unwanted exposed seed layers. The wafer is then diced and the circuits separated. A detailed recipe for the circuit fabrication is given below.

Quartz Circuit Recipe

1. *Quartz Substrate Mounting to Si Wafer*
    a. Scribe Si wafer into squares slightly larger than quartz substrate
    b. Place Si wafer on hot plate at 200°C.
    c. Coat Si wafer with G-wax.
    d. Place quartz substrate on Si wafer.
    e. Remove excess G-wax with acetone on spin cleaner.
2. *Metal Deposition*
    a. Sputter ≈50 Å Cr then 500-1000 Å Au on the quartz.
3. *Photolithography*
    a. Spin clean wafer with ETH, TCA, METH.
    b. Hotplate dehydration bake at 120°C for 5 minutes.
    c. HMDS exposure for 10 minutes.
    d. Spin AZ P4330 at 3000 RPM for 30 sec. (3.8 um resist)
    e. Hotplate bake at 90°C for 1 minute.
    f. 30 second UV exposure through photomask (10 mW/cm^2).

g. Develop using AZ400K:DI (1:4) for 70 seconds, DI rinse.

h. Choose either procedure (i) or (ii):

i. Hotplate bake at 120°C for 1 minute.

ii. Deep UV cure 30 min. Oven bake at 120°C for 20 minutes.

4. *Gold Electroplating*

a. Clean wafer with 5 minute O_2 plasma exposure. (optional)

b. Mount wafer on mousetrap (use blackwax).

c. Pickle {place wafer in HCl:DI [1:1] solution for 5 minutes}. (optional)

d. DC plate Au. BDT-200 at 50°C.

The optimal plating rate is $3A/ft^2$ or $32pA/\mu m^2$ yielding 0.2 μm/min.

40/80 GHz circuit: 2.4 mA for 15 min yields nominal 3.0 um Au.

80/160 GHz circuit:

{Au plate area = 0.008 ft^2 or 74,838,100 μm^2 for photomask DWP1.}

e. DI rinse.

f. Clean wafer in TCA to remove black wax.

5. *Metallic Etch*

a. Clean in heated AZ300T to remove photoresist.

b. Method 1: Use a sputter etch technique to remove the Au and Cr seed layers.

c. Method 2: Wet etch Au and Cr seed layers.

6. *Dice and Separate*

   a. Cover wafer in AZPC, spin 2000 RPM for 30 sec. Bake 1 minute at 100°C. Repeat 3 times.

   b. Post bake for 2 minutes at 100°C and 2 minutes at 120°C.

   c. Dice.

   d. Remove AZPC in heated AZ300T.

   e. Remove the G-wax with acetone. The circuits will fall off of the Si wafer.

Mounting and Assembly

Before mounting the varactor, it is necessary to attach three bond-wires to the circuit as shown in Fig. E.1. All three bond-wires are 1 mil diameter Au. Two of the bond-wires are mounted to the outer varactor chip mounting pads on the left end of the quartz substrate. These bond-wires extend out from the quartz approximately 10 mils. The bonds are restricted to an area no larger than 3×3 mils at the very outer edge of the circuit pads so that they do not interfere with the subsequent mounting of the varactor chip. The free hanging ends of these bond-wires are later attached to the block.

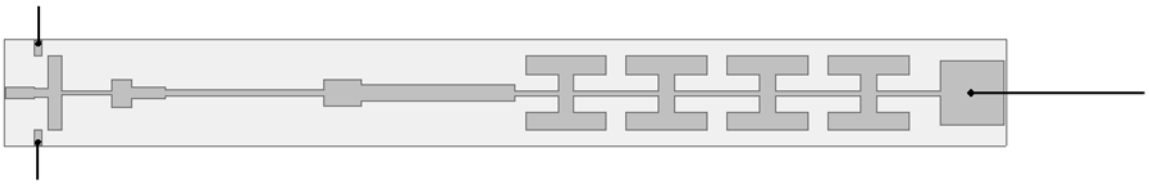


Fig. E.1. Bond-wire locations for the balanced doubler circuits.

The third bond-wire is attached at the large pad on the opposite end of the quartz circuit and is approximately 7.6-12.7 mm (300-500 mils) long. The free hanging end of this bond-wire is later soldered to an SMA connector for DC bias. The bond-wire is trimmed to the appropriate length at that time.

The circuit is then mounted on a miniature hot plate. A small amount of a relatively high temperature solder, [Indium Corp. of America, Indalloy #2, 149-155° C], is applied to the two bonds at the left edge of the circuit as illustrated in Fig. E.2. The solder reinforces the bond and improves the heat conduction path from the circuit pad to the bond-wire. The thermal conduction path through the bond alone is poor since the metal-to-metal adhesion tends to be spotty over the bond area.

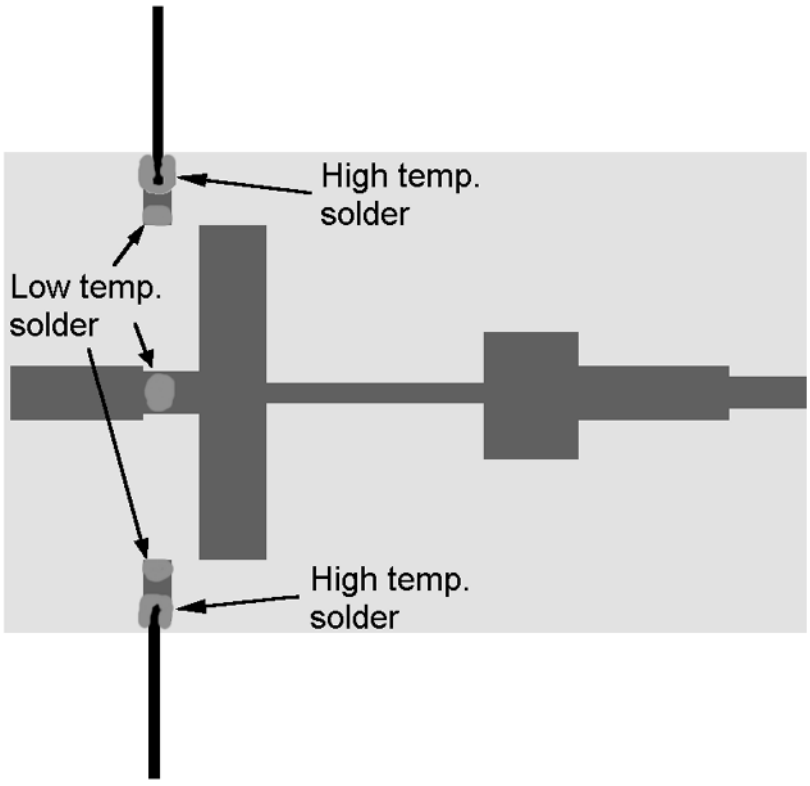


Fig. E.2. Solder location.

A larger amount of the high temperature solder is used to strengthen the bond at the DC bias wire. Solder flux [Superior Flux & Mfg. Co., Supersafe No. 30] is used to promote solder flow. After heating, the flux is removed with warm water.

Next, a small amount of low temperature solder [Indium Corp. of America, Indalloy #1, 118-125° C] is applied to the three points on the circuit corresponding to the three varactor chip mounting pads as shown in Fig. E.3. Again, the solder flux is rinsed away with warm water. A metal probe is used to flatten the rounded surfaces of the low temperature solder and a small amount of solder flux is reapplied. The varactor is placed on top of the solder as shown in Fig. E.3. Downward pressure is applied to the varactor chip and the solder is reheated.

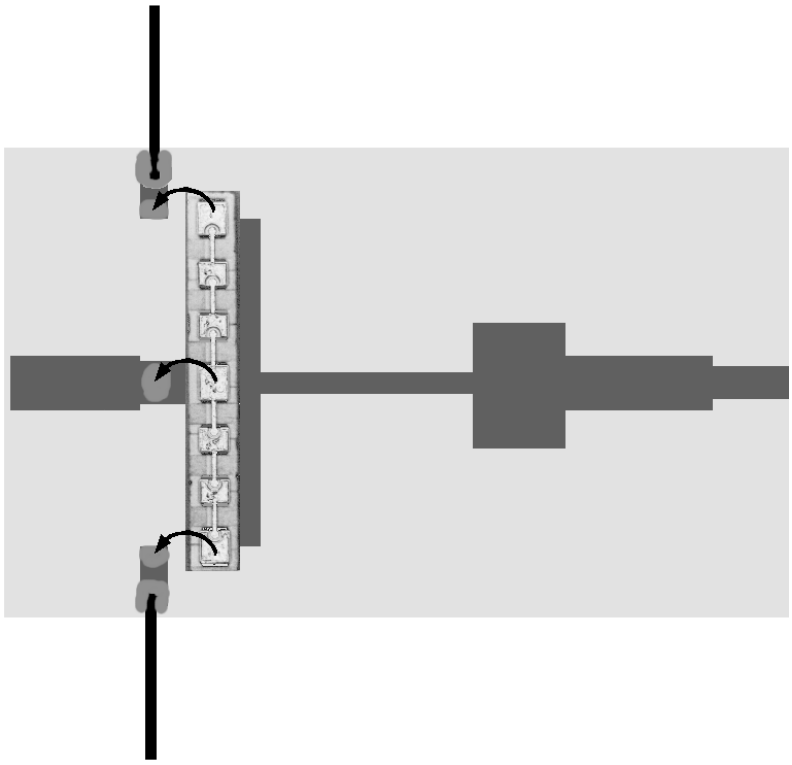


Fig. E.3. A varactor chip lying on a circuit near the three circuit pads. The varactor is flipped over and soldered face down to the circuit pads as indicated in the sketch.

When the solder begins to flow, the heat is removed and the circuit is actively cooled to prevent thermal damage to the semiconductor. Residual solder flux is removed with warm DI water. DC bias tests are performed on the varactor to ensure all three of the electrical connections are good.

The circuit is placed in the metal waveguide block and the bond-wires protruding from the ends of the varactor are fastened to the block by packing them in soft Indium (99.99 % pure In). Alternatively, the block can be heated and a low temperature solder (Indalloy #1) can be used. The pure Indium adheres to the block when the surface is scratched and pitted with a metal probe. The DC bias wire is soldered to the SMA pin with a solder iron. The DC continuity from the SMA pin to the block is checked. The block is assembled and the DC IV curve is retested. Fig. E.4 shows an enhanced photograph of the SB13T1 varactor and quartz circuit mounted in the 40/80 GHz doubler block. The distinguishing features of the SB13T1 varactor are not visible since the chip faces down on the circuit.

Fig. E.4. Enhanced photograph of the varactor and circuit mounted in the block.

Appendix F

Mechanical Drawings

This appendix contains mechanical drawings for the 40/80 GHz and 80/160 GHz doubler blocks and quartz circuits. The doubler circuits were actually made from fused silica which has a relative dielectric permittivity of approximately 3.8 rather than Z-cut crystalline quartz which has a dielectric constant closer to 4.6. The thickness of the quartz circuit is 5 mils for the 40/80 GHz doubler and 3 mils for the 80/160 GHz doubler.

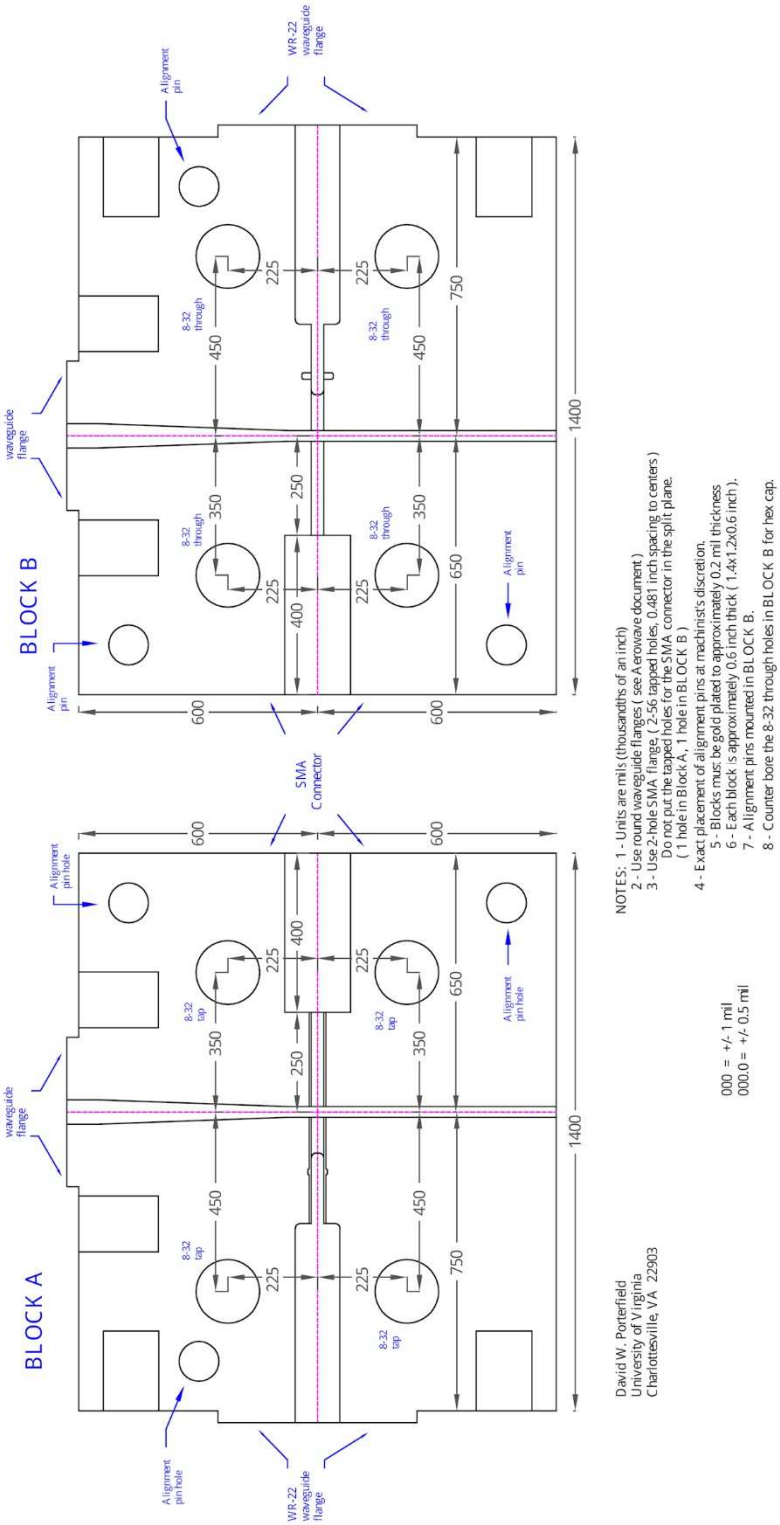


Fig. F.1. Mechanical drawing for the 40/80 GHz doubler block, page 1 of 7.

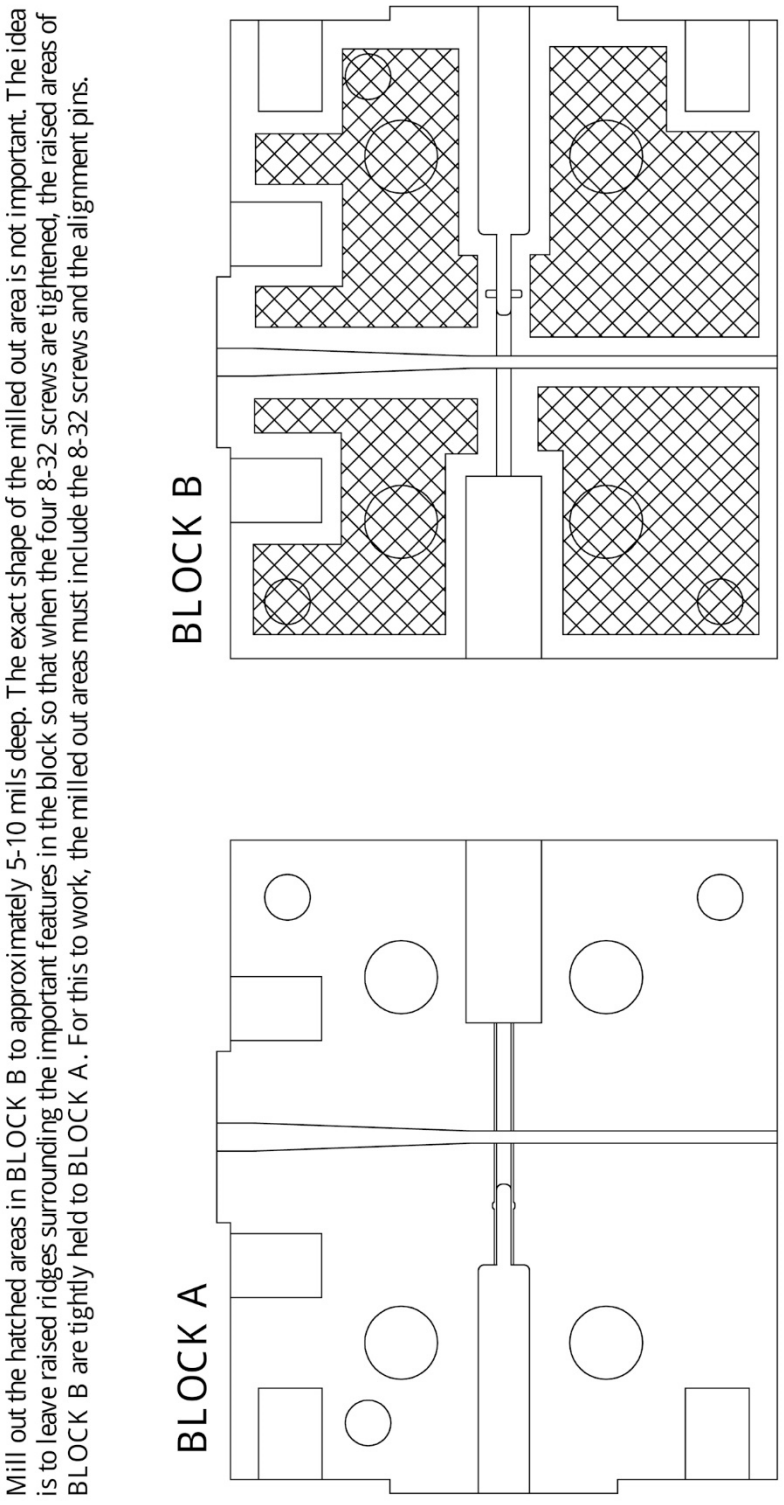


Fig. F.2. Mechanical drawing for the 40/80 GHz doubler block, page 2 of 7.

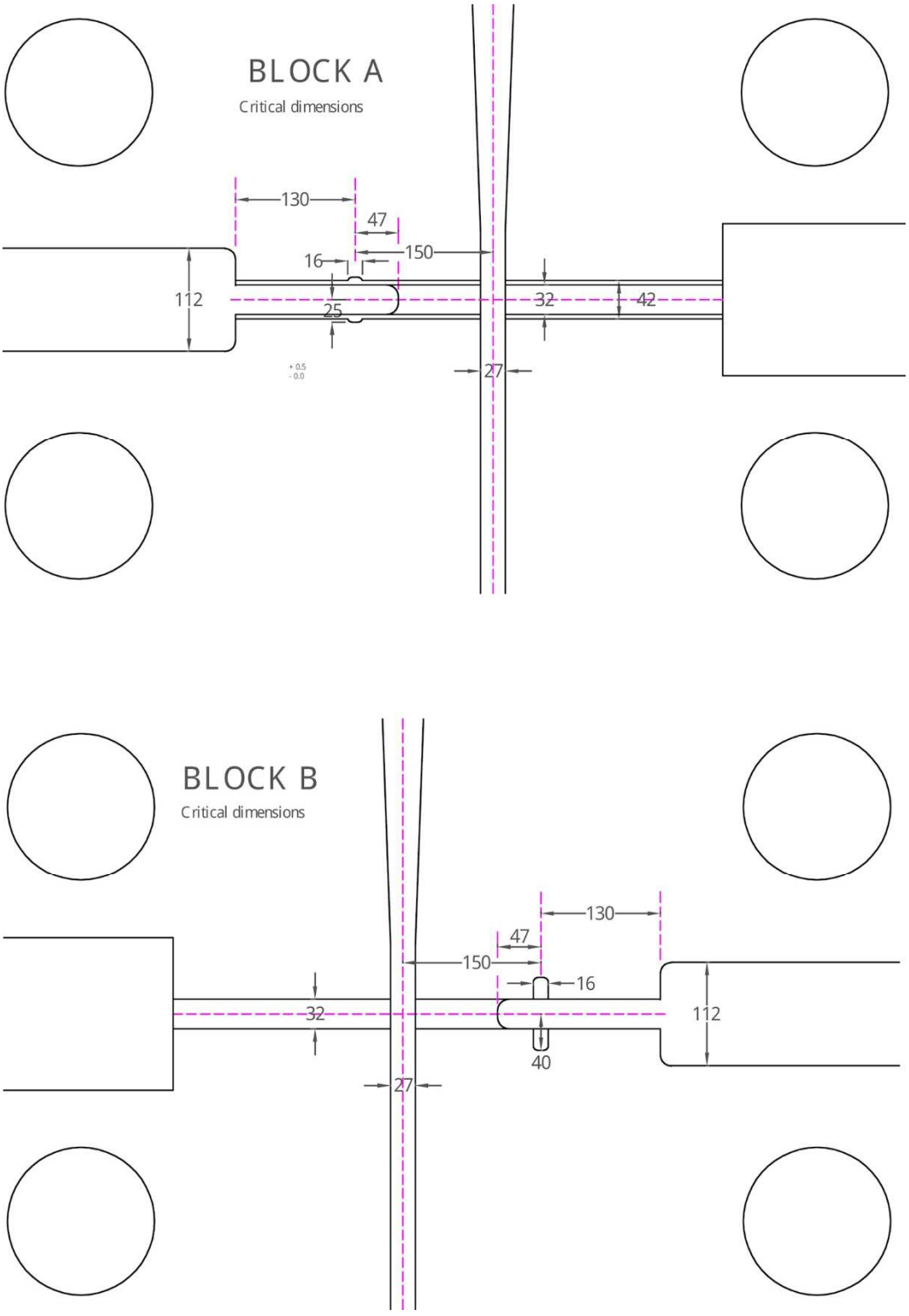


Fig. F.3. Mechanical drawing for the 40/80 GHz doubler block, page 3 of 7.

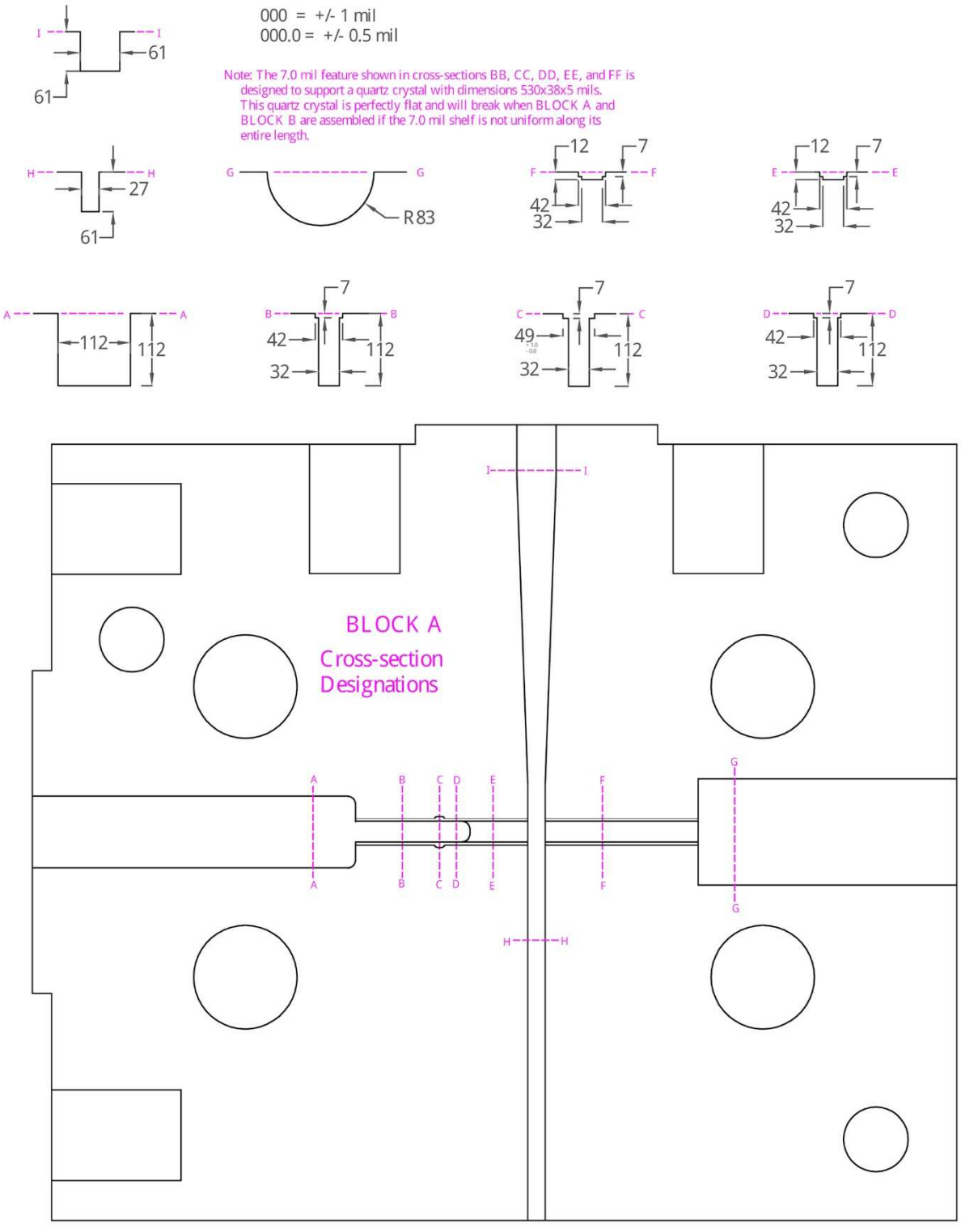


Fig. F.4. Mechanical drawing for the 40/80 GHz doubler block, page 4 of 7.

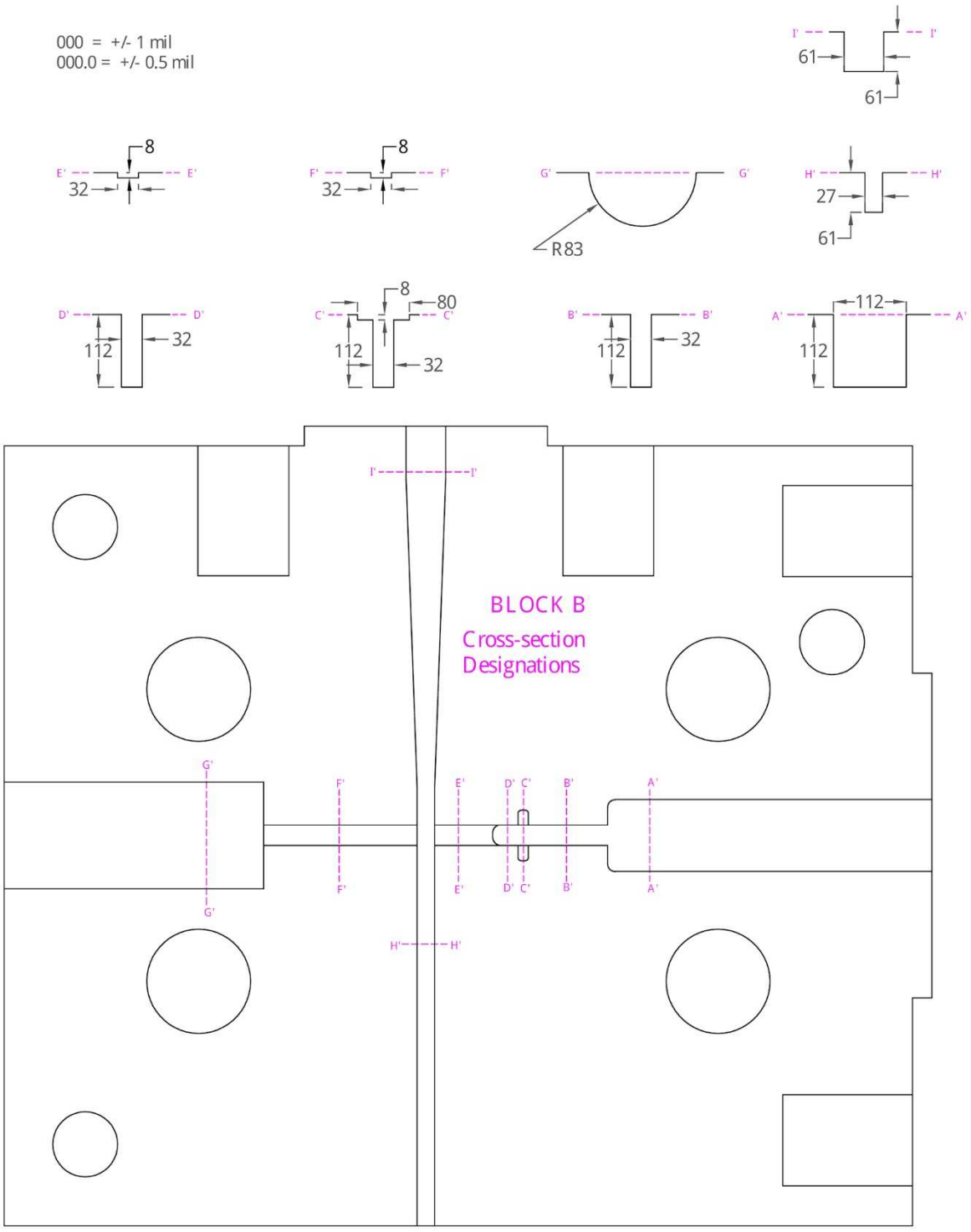


Fig. F.5. Mechanical drawing for the 40/80 GHz doubler block, page 5 of 7.

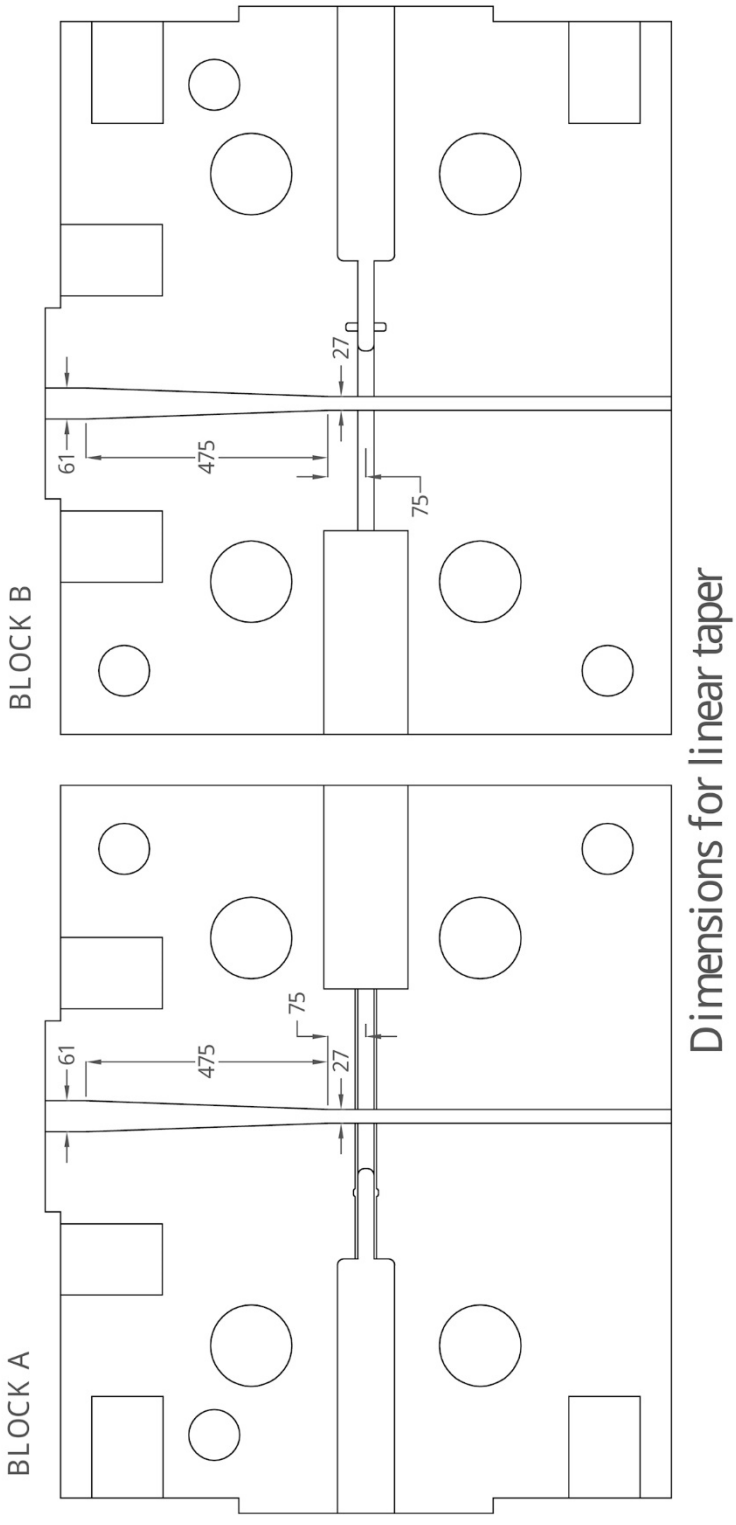


Fig. F.6. Mechanical drawing for the 40/80 GHz doubler block, page 6 of 7.

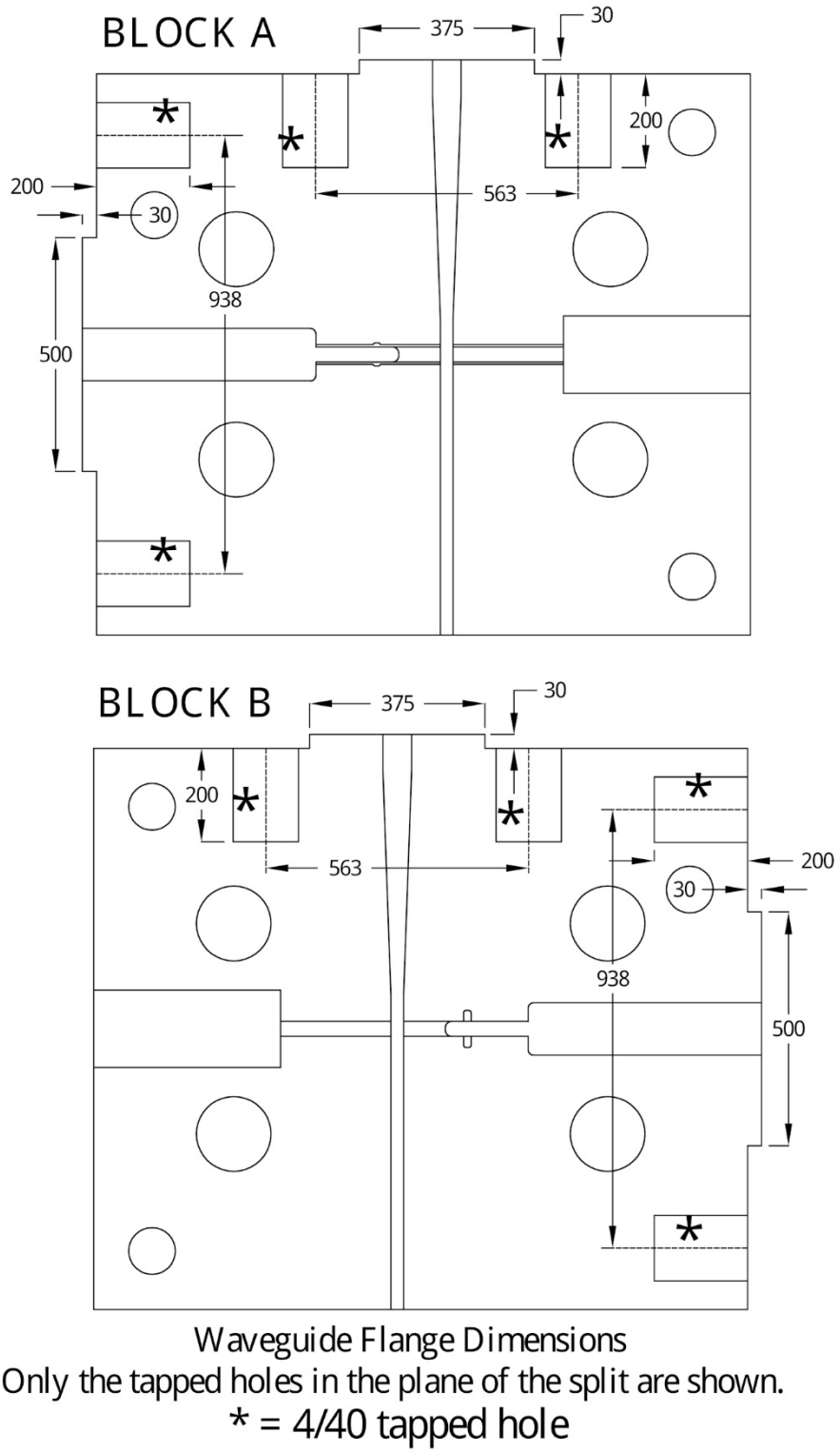


Fig. F.7. Mechanical drawing for the 40/80 GHz doubler block, page 7 of 7.

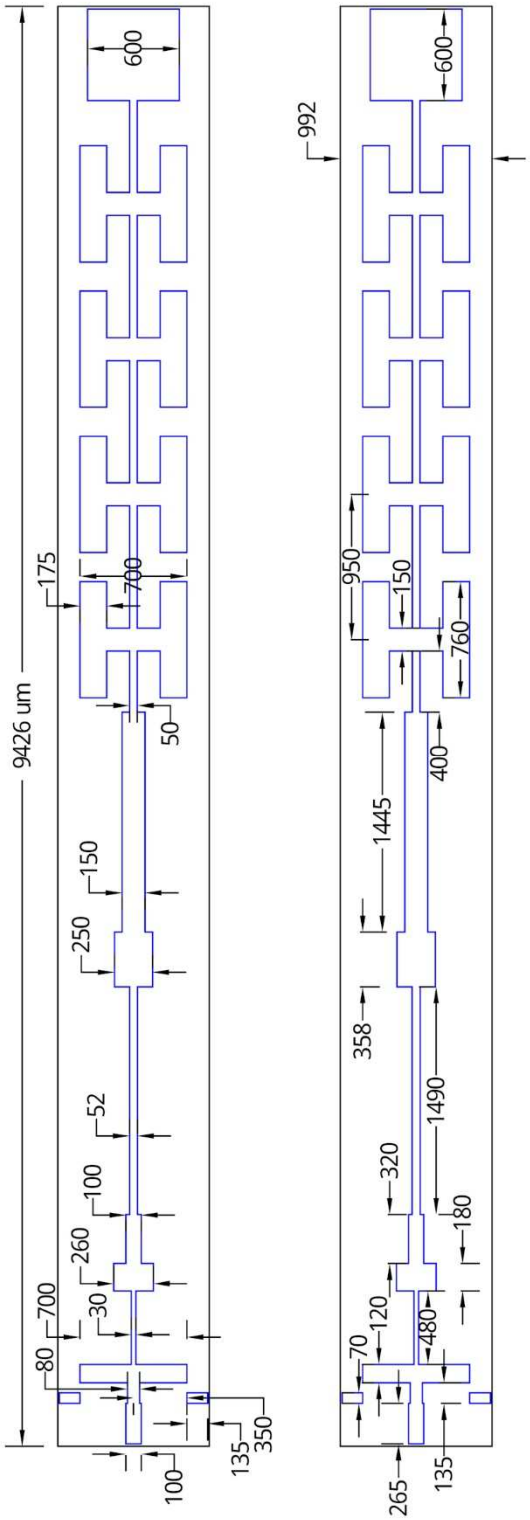


Fig. F.8. Mechanical drawing for the 40/80 GHz circuit, page 1 of 1.

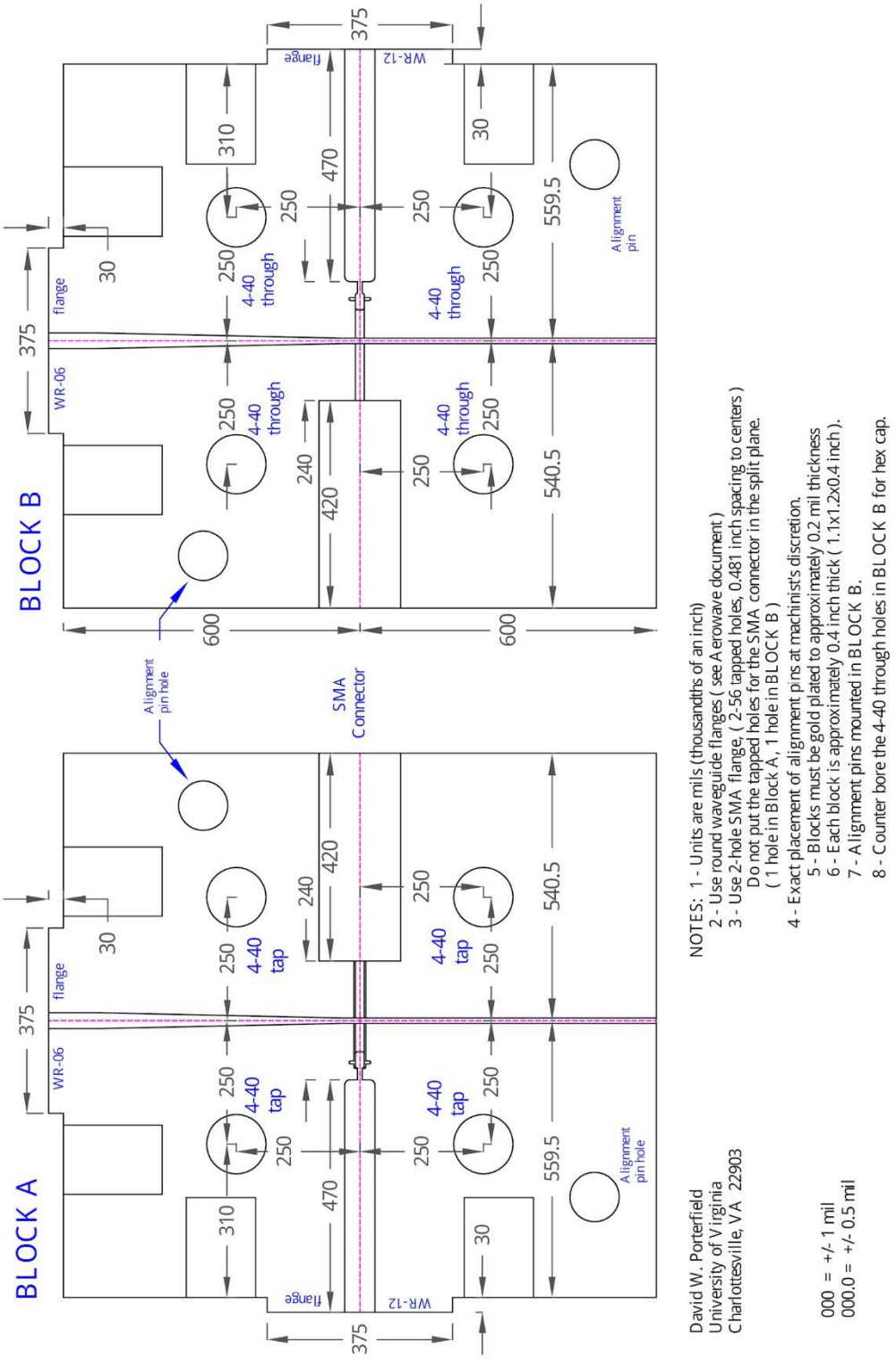


Fig. F.9. Mechanical drawing for the 80/160 GHz doubler block, page 1 of 9.

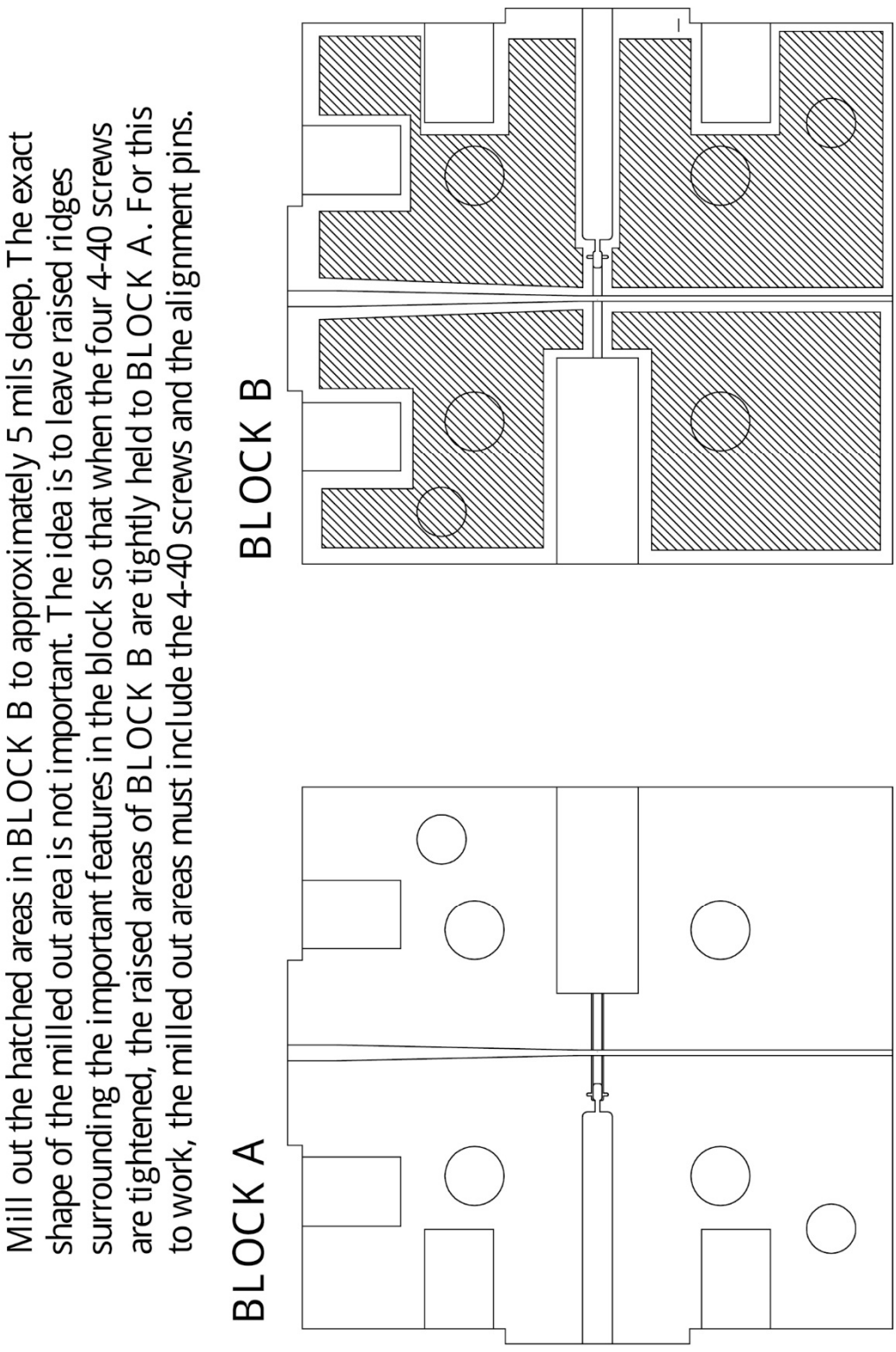


Fig. F.10. Mechanical drawing for the 80/160 GHz doubler block, page 2 of 9.

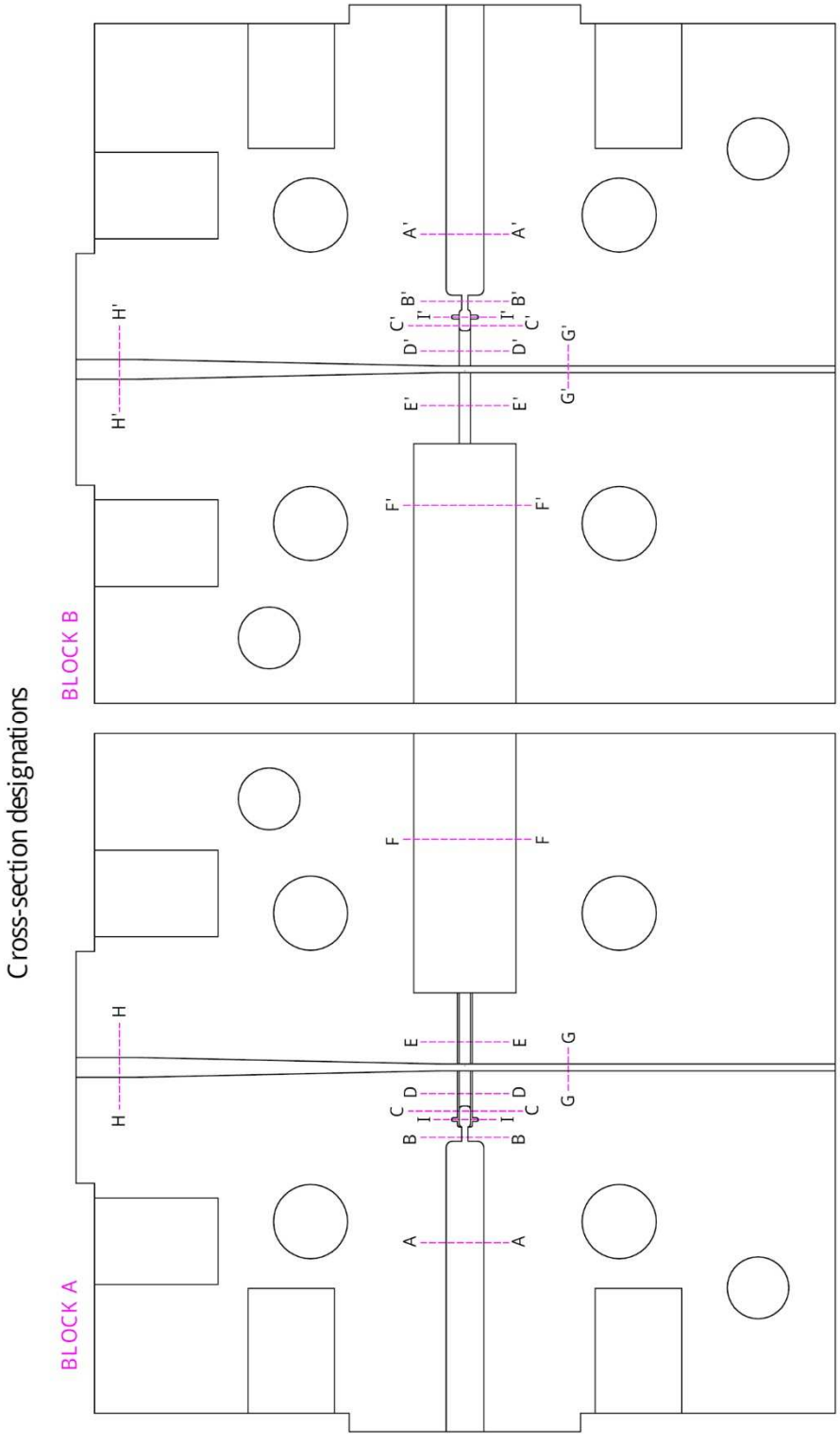


Fig. F.11. Mechanical drawing for the 80/160 GHz doubler block, page 3 of 9.

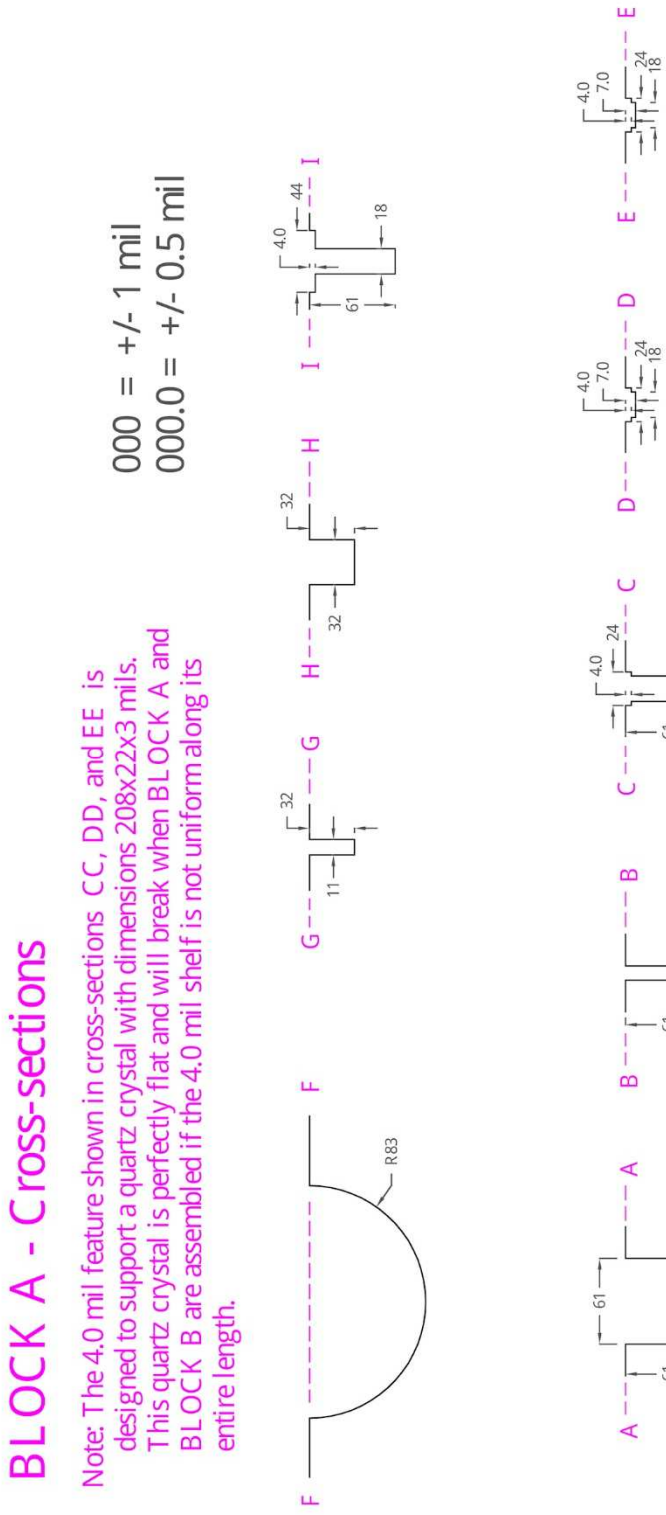


Fig. F.12. Mechanical drawing for the 80/160 GHz doubler block, page 4 of 9.

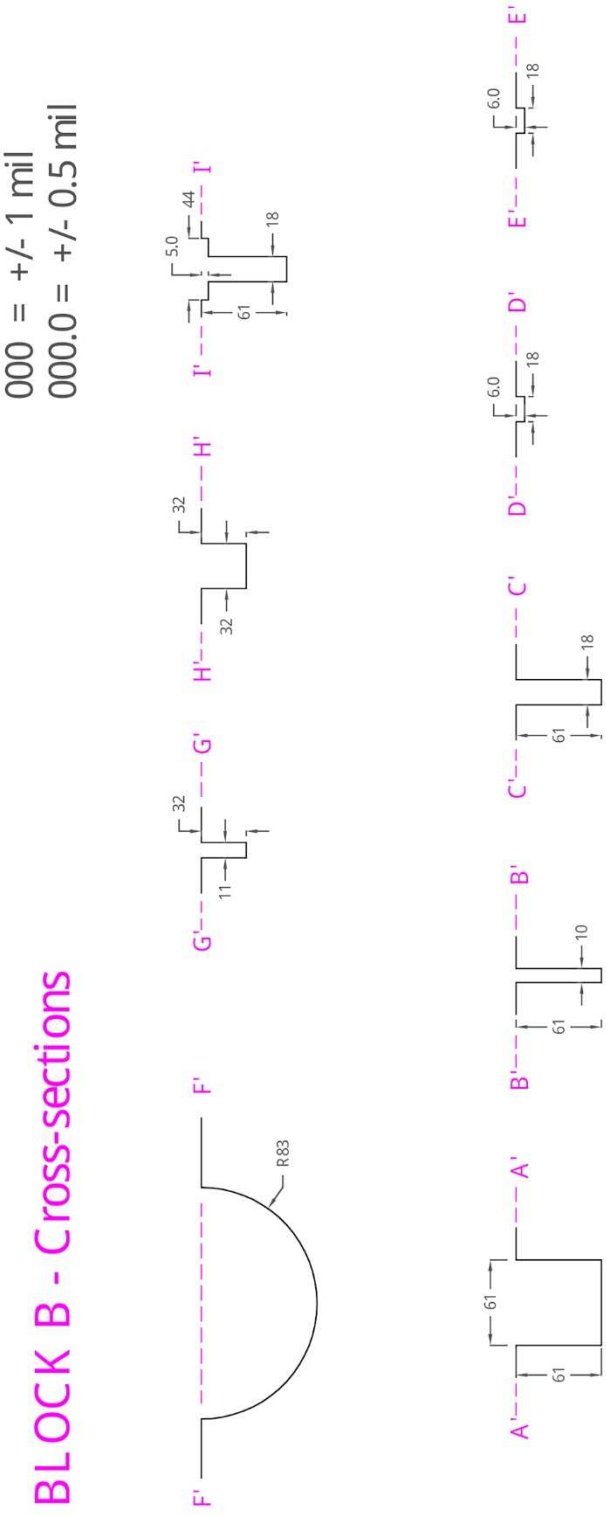


Fig. F.13. Mechanical drawing for the 80/160 GHz doubler block, page 5 of 9.

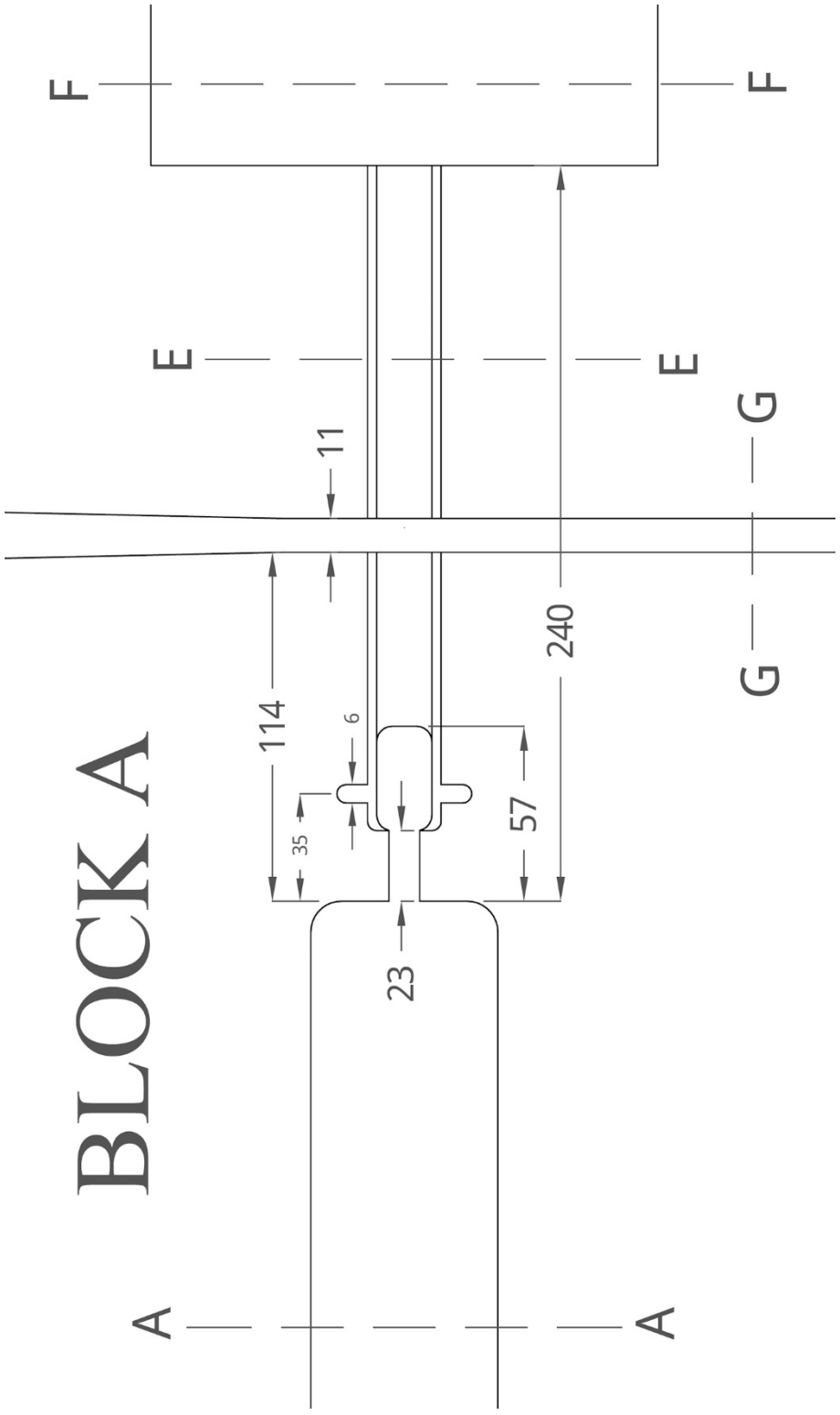


Fig. F.14. Mechanical drawing for the 80/160 GHz doubler block, page 6 of 9.

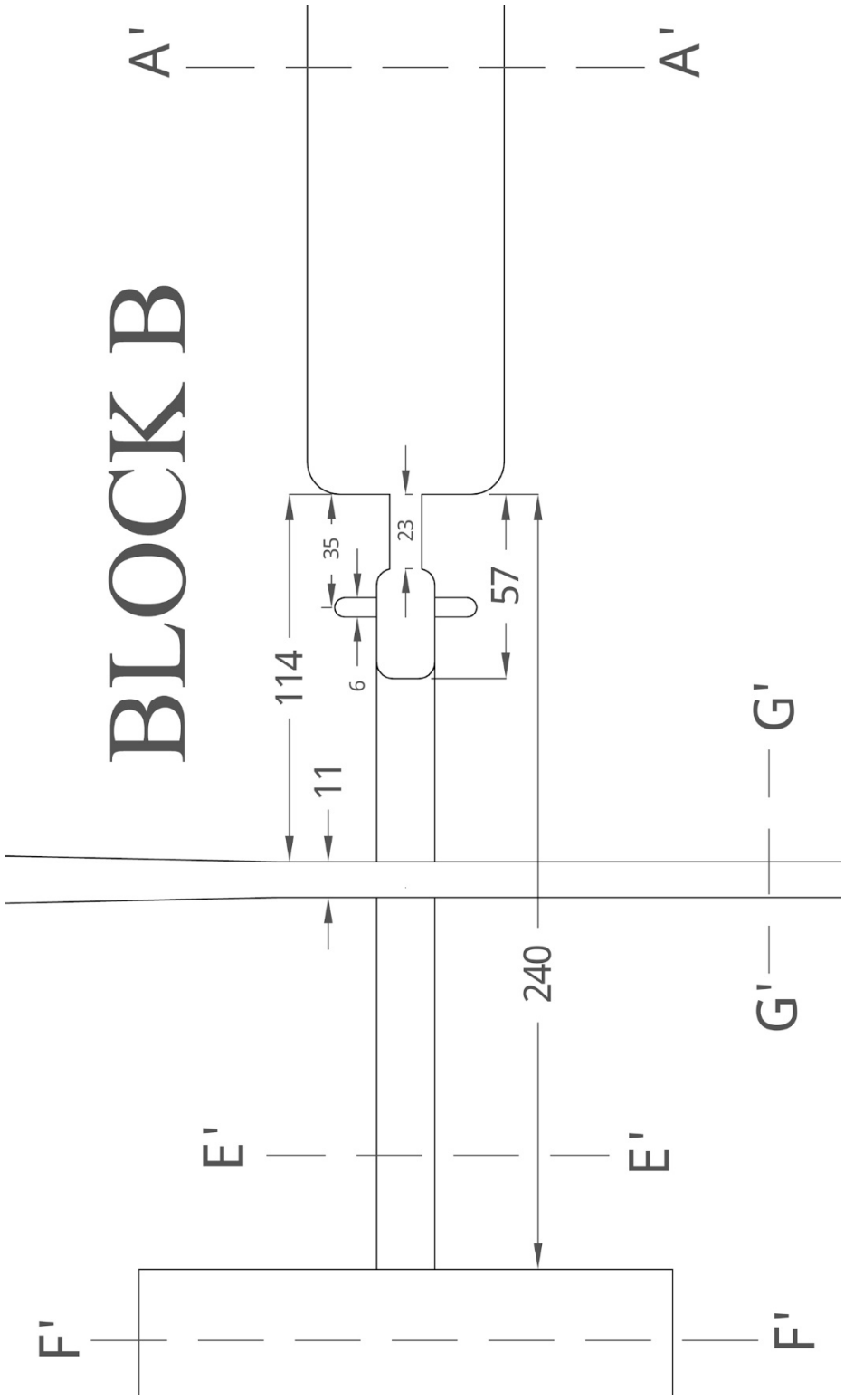


Fig. F.15. Mechanical drawing for the 80/160 GHz doubler block, page 7 of 9.

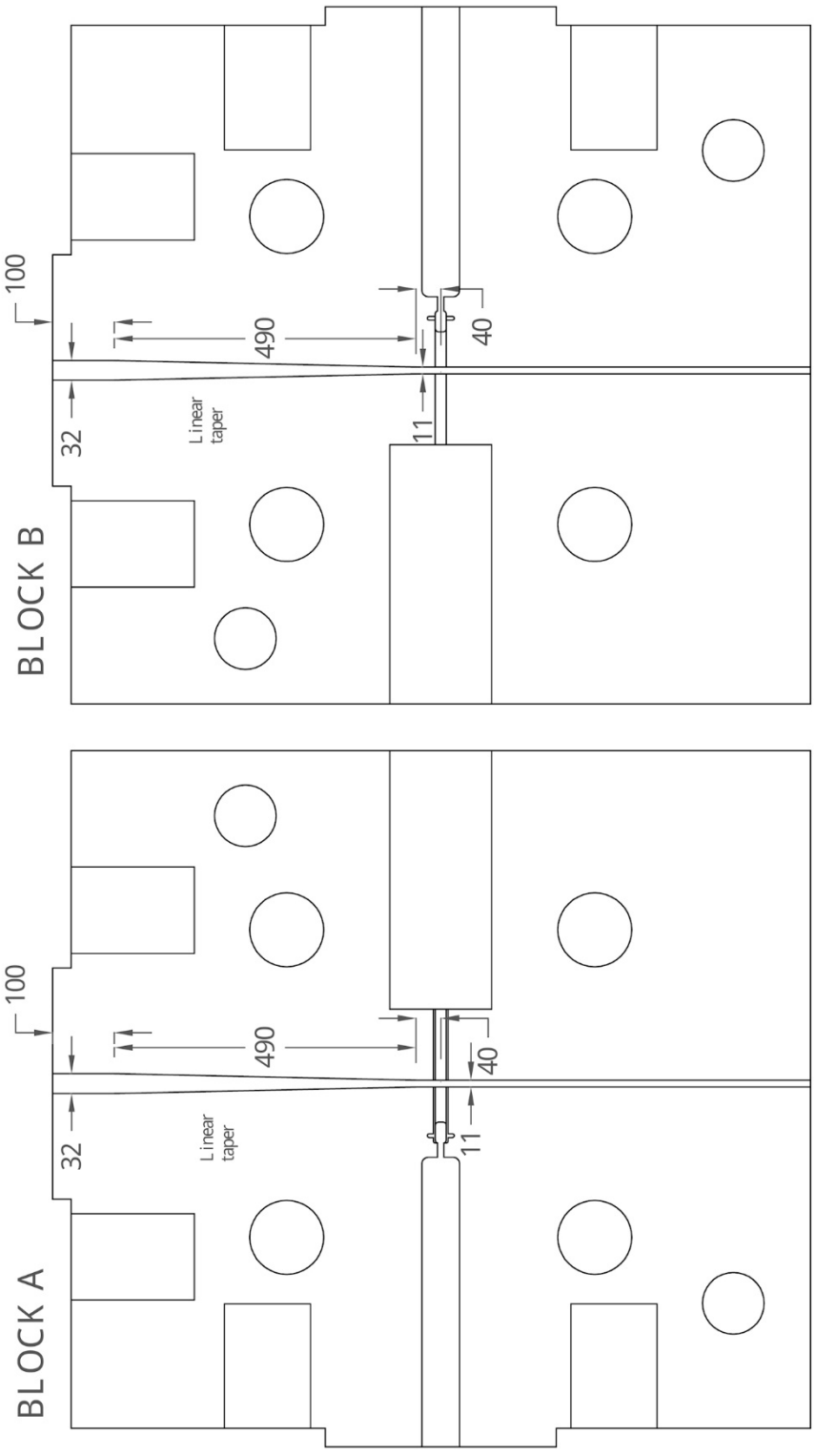


Fig. F.16. Mechanical drawing for the 80/160 GHz doubler block, page 8 of 9.

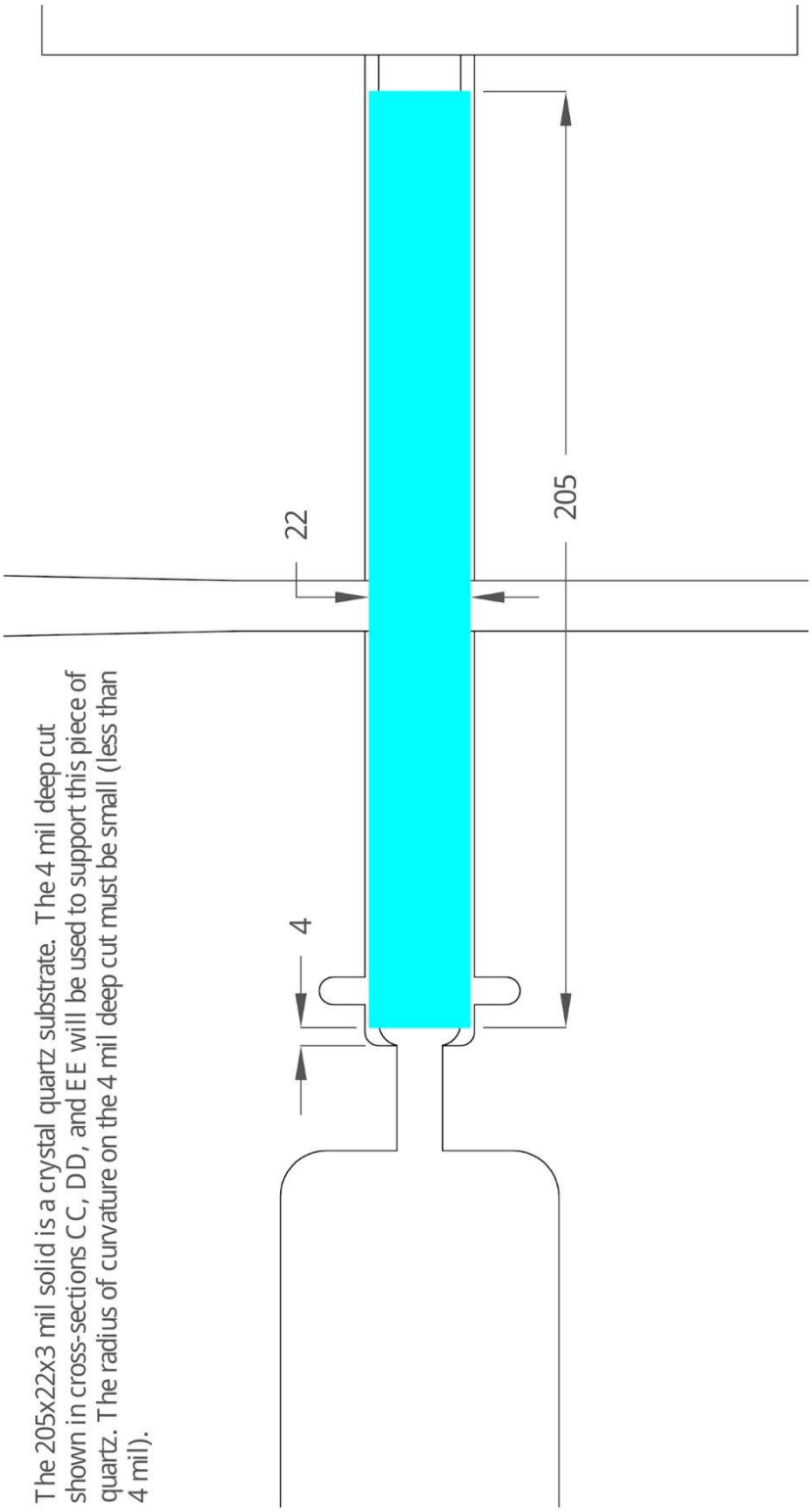


Fig. F.17. Mechanical drawing for the 80/160 GHz doubler block, page 9 of 9.

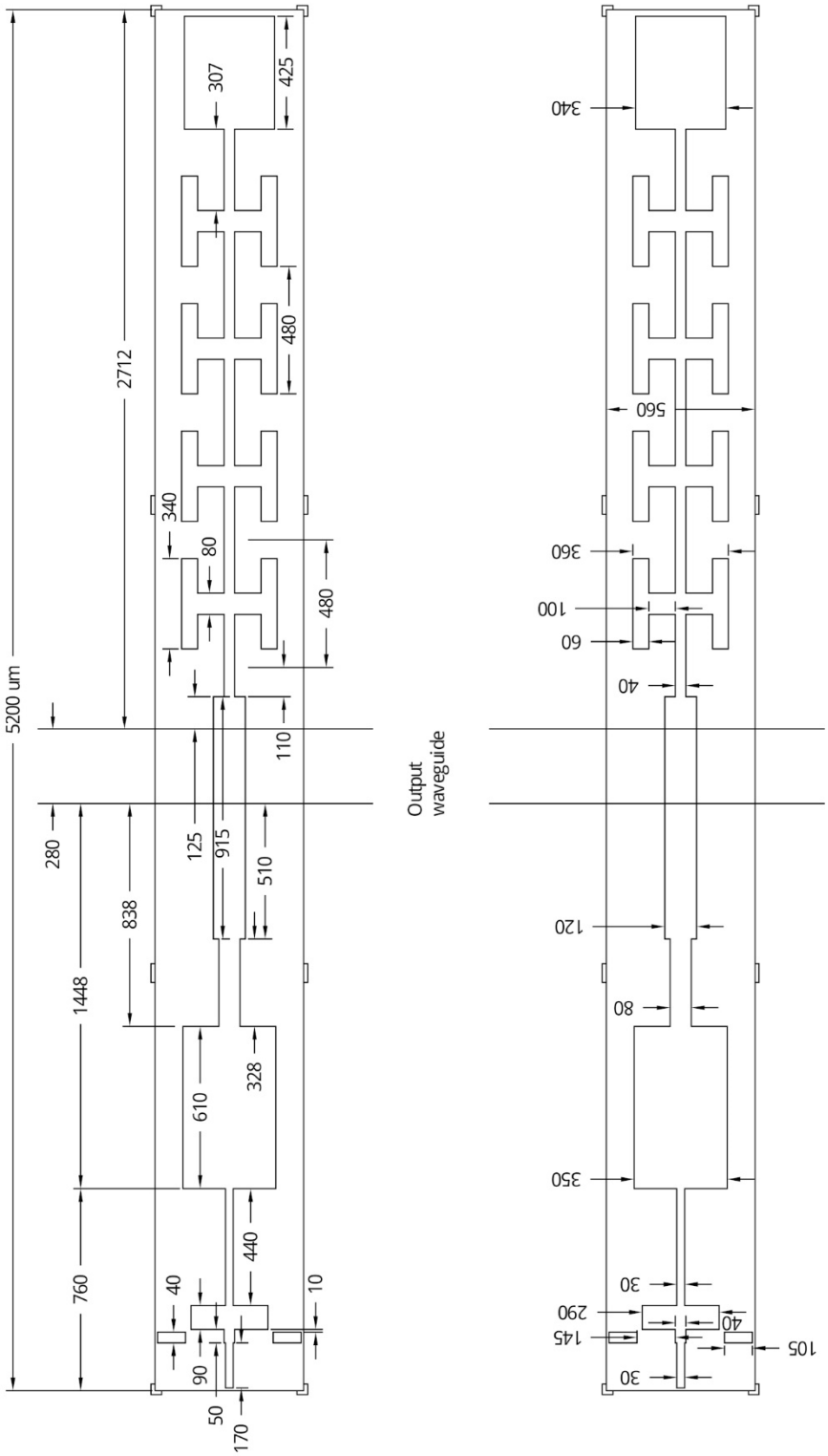


Fig. F.18. Mechanical drawing for the 80/160 GHz circuit, page 1 of 1.

Appendix G

80/160 GHz Test Results

G.1 Overview

The preliminary test results for the 80/160 GHz balanced doubler are presented here. These results represent measured data from the only varactor chip and quartz circuit mounted and tested in the 80/160 GHz doubler block prior to the writing of this dissertation. Improvements in the doubler performance should be attainable with additional testing of other quartz circuits and varactor chips.

G.2 Varactor Chip

The varactor chip tested in the 80/160 GHz doubler comprises four anodes with anode diameters of 7 μm, finger lengths of 30 μm, epitaxial layer doping of 2×10^{17} cm^{-3}, epitaxial layer thickness of 3000 A, and an estimated series resistance of 3 Ω per anode. The overall dimensions of the chip are approximately 540×90×50 μm. I designed the varactor chip specifically for use in the 80/160 GHz doubler. Several versions of the chip were fabricated by William Bishop at the University of Virginia Semiconductor Device Lab with anode sizes ranging from 4.5-7.5 μm. Three scanning electron micrographs (SEM) of a varactor chip with 7 μm anodes appear in Fig. G.1.

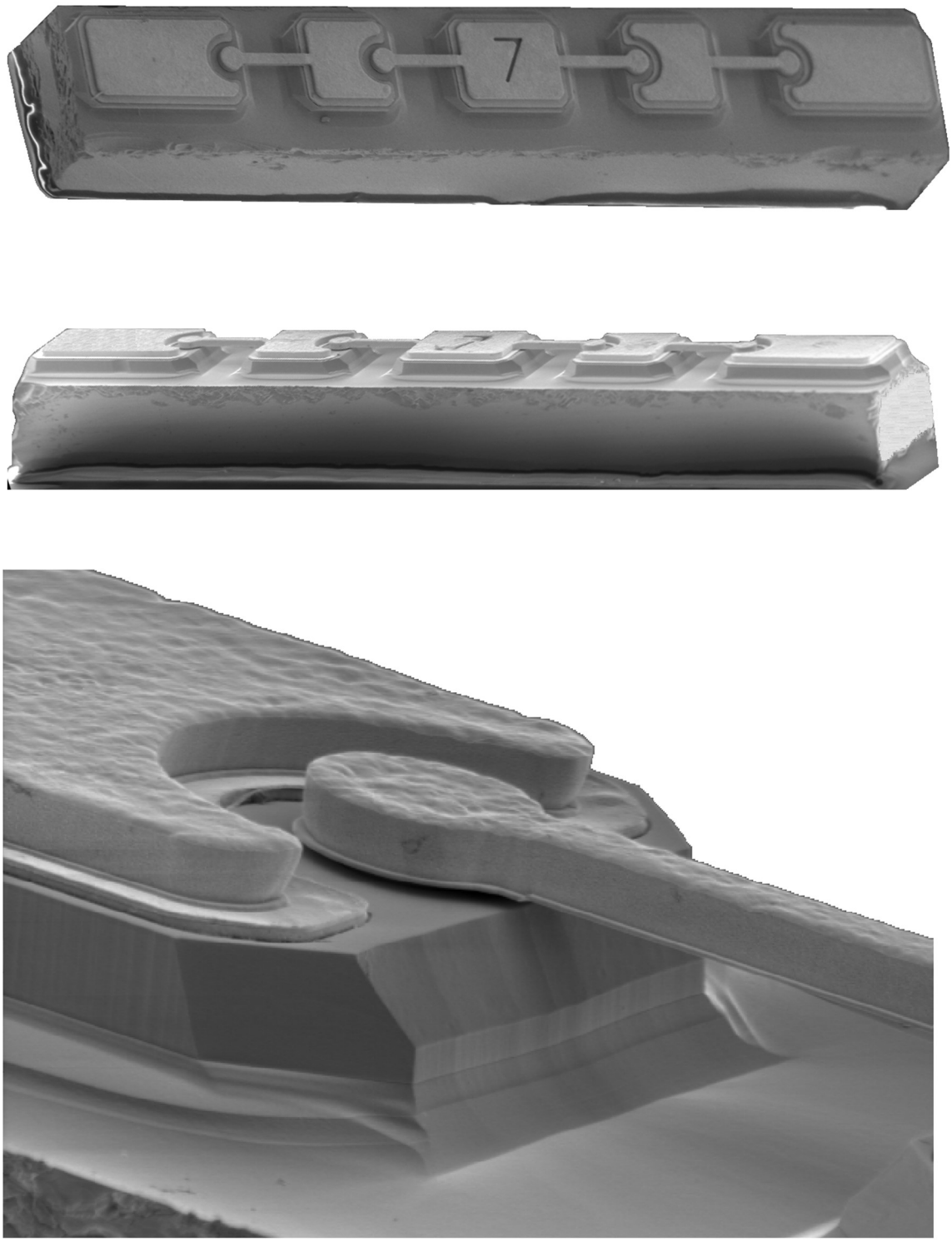


Fig. G.1. SEM's of the varactor chip used in the 80/160 GHz doubler.

The measured C-V curve for the varactor chip (7 µm anodes) is shown in Fig. G.2. The curve fit to the data corresponds to a varactor with C_{j0} = 52 fF and a parasitic shunt capacitance of 7 fF. The circuit design and simulations were made for a varactor with C_{j0} = 63 fF, and thus the measured peak efficiency of the doubler is expected to occur at a frequency somewhat higher than the design frequency of 160 GHz.

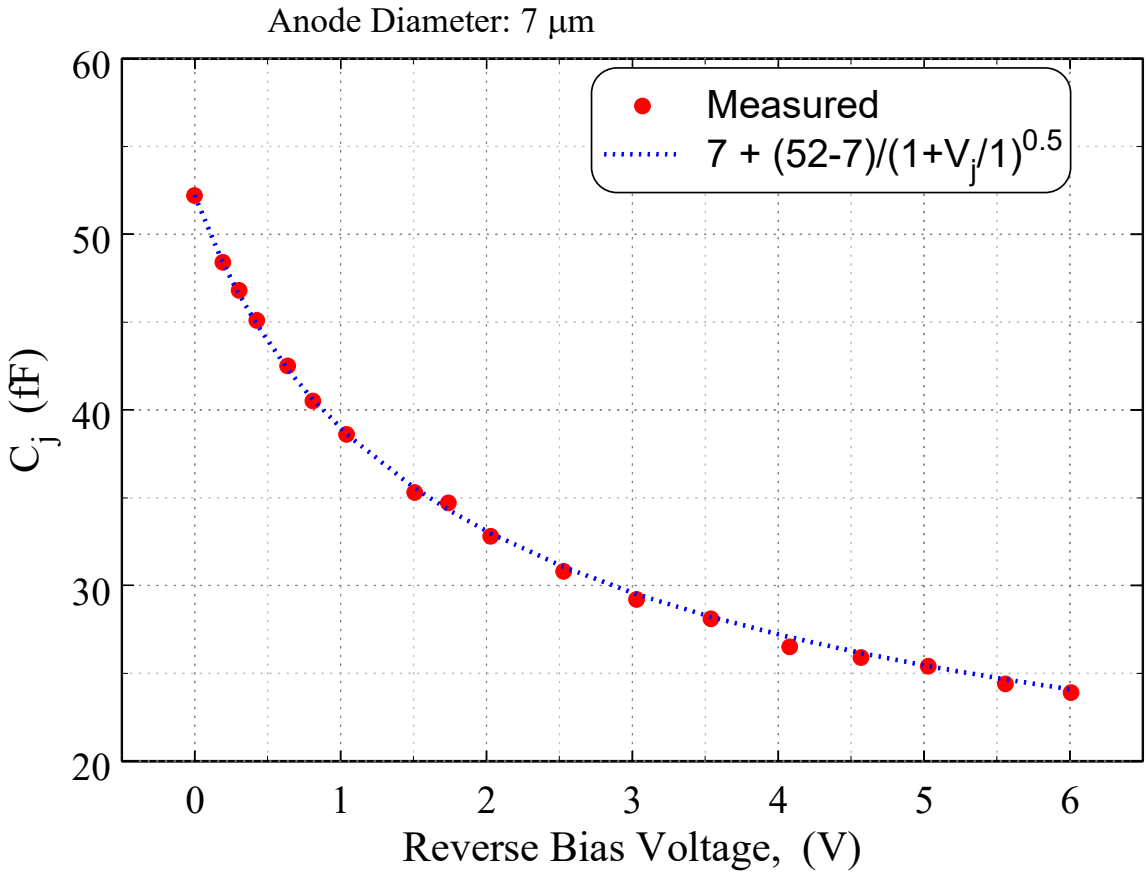


Fig. G.2. Measured C-V curve for a varactor chip with 7 µm anodes.

The measured reverse breakdown voltage at 1 µA was typically in the 5-8 V range prior to removal of the oxide layer. After removal of the oxide layer, the measured reverse breakdown voltage at 1 µA tended to increase to the 8-9 V range. The graph in Fig. G.3 shows

a typical measured reverse breakdown voltage curve prior to removal of the oxide layer. The voltage is approximately 6.65 V at 1 μA and increases to greater than 9.1 V at 50 μA.

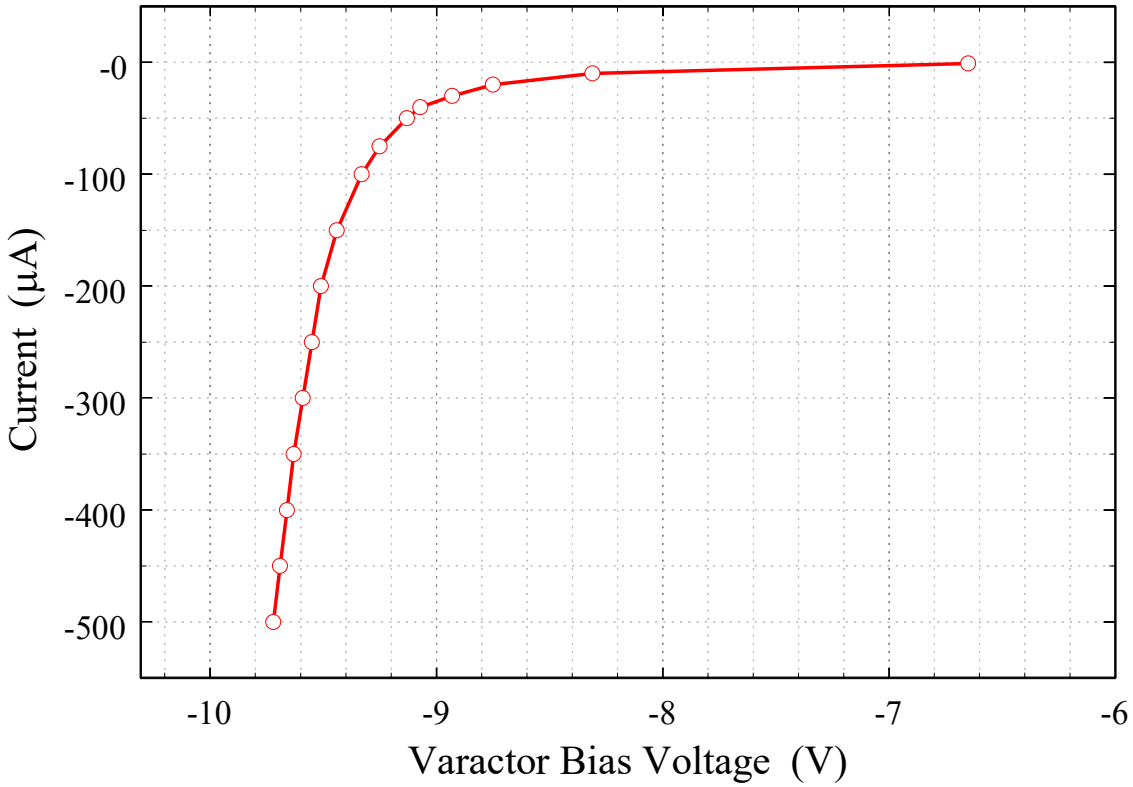


Fig. G.3. Measured reverse breakdown curve with oxide passivation layer.

G.3 Test Results

Test results presented in this section were obtained using the measurement system shown in Fig. 5.4 (page 68). Input power was measured using an HP437B meter with a W-band (WR-10, 75-110 GHz) power sensor. All input power measurements are referenced to the input waveguide flange of the doubler block (plane BB′ in Fig. 5.4). Output power was measured using a Thomas-Keating meter. A WR-6 (110-170 GHz) conical horn with a

rectangular-to-circular waveguide transition was attached to the WR-6 output waveguide flange of the doubler. No corrections were made to the measured data for ohmic losses in the multiplier block and quartz circuit, ohmic losses in the conical horn or optical coupling losses.

The graph in Fig. G.4 shows measured output power and efficiency versus input power at 84/168 GHz. The peak efficiency is 21% at an input power level of approximately 70 mW and output power of 15 mW. The efficiency drops to 20% at an input power level of 80 mW and corresponding output power of 16 mW. Input power was provided from a Carlstrom Gunn-effect oscillator with output power of >90 mW in the 75-85 GHz band.

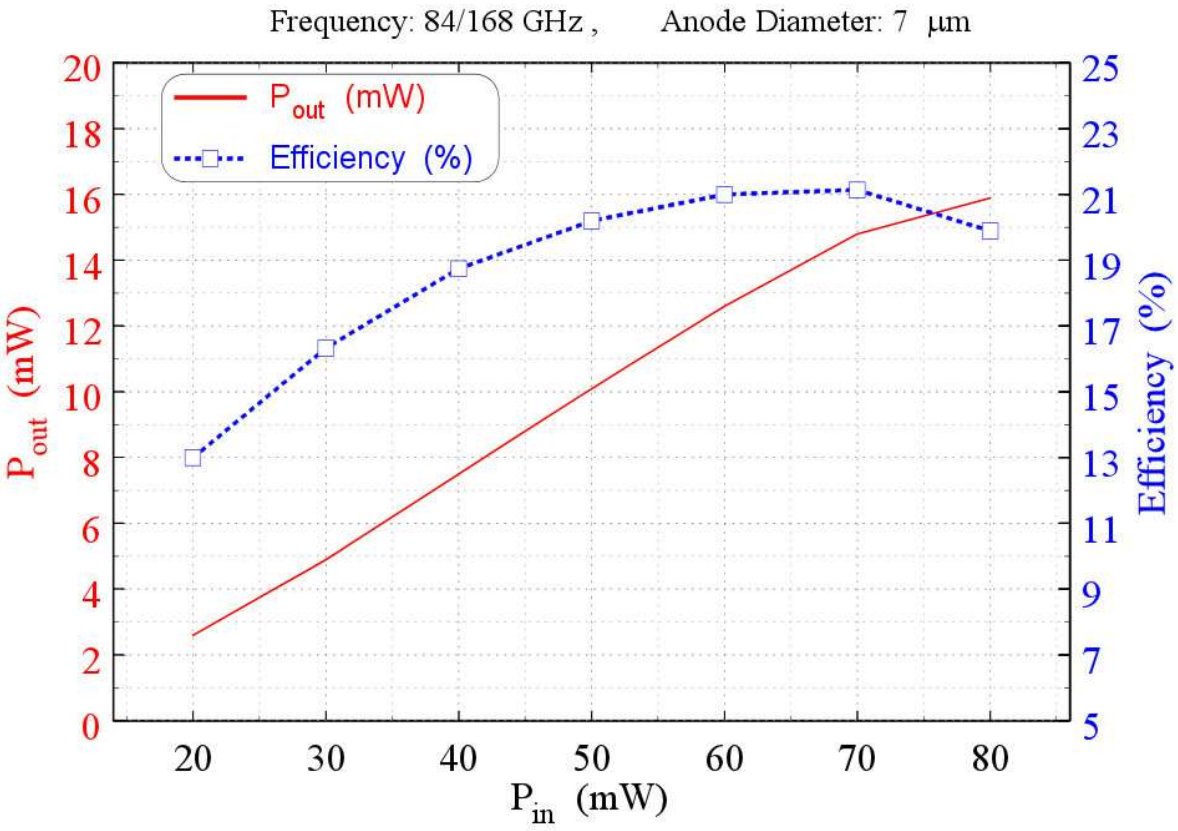


Fig. G.4. Measured output power and efficiency versus input power.

Fig. G.5 shows measured output power versus output frequency for an input power of 60 mW. Tuning was provided through an electronic DC bias supply. The peak efficiency of 21% occurred at 84/168 GHz. The measured 3 dB fixed-tuned bandwidth is > 15% (> 26 GHz). The output power is greater than 2 mW over the entire band from 144-178 GHz.

Figs. G.6 and G.7 show the measured reflected input power both as a function of frequency and input power. The reflected power measurements were made with an Anritsu power meter through a 10 dB directional coupler. Reflected power levels were typically less than 10% of the incident power at 84/168 GHz. However, the input reflected power increased for frequencies below 85/170 GHz, indicating a better input impedance match at the higher frequencies. This is consistent with a varactor chip with too low capacitance for 80/160 GHz operation.

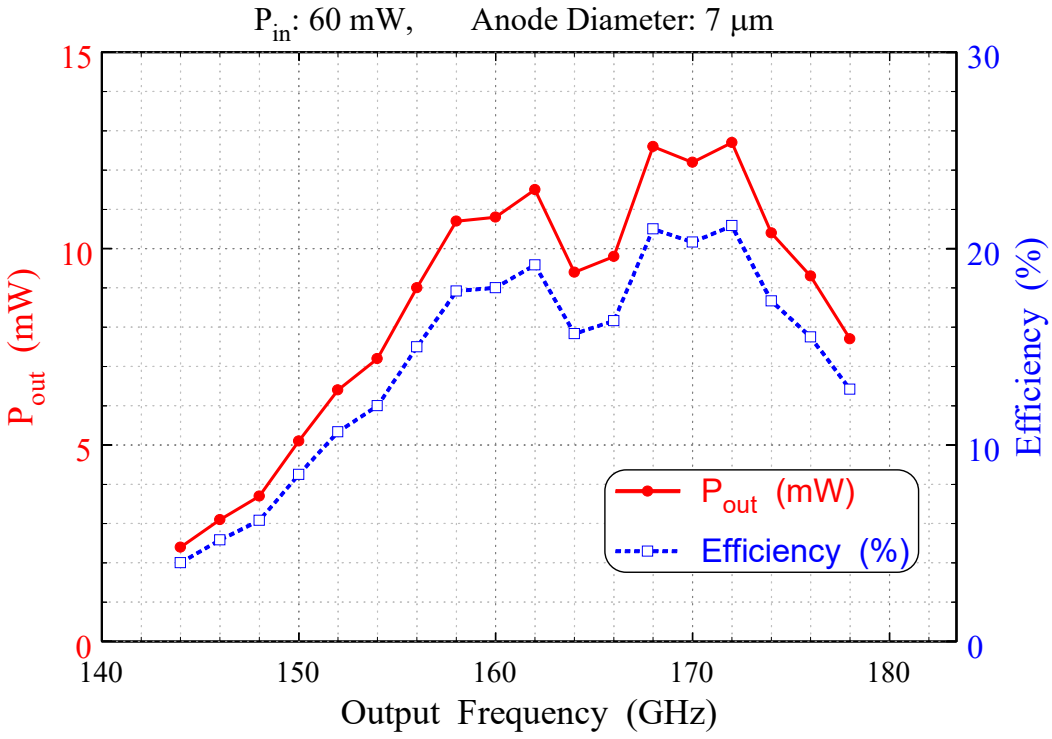


Fig. G.5. Measured output power versus output frequency for P_{in} = 60 mW.

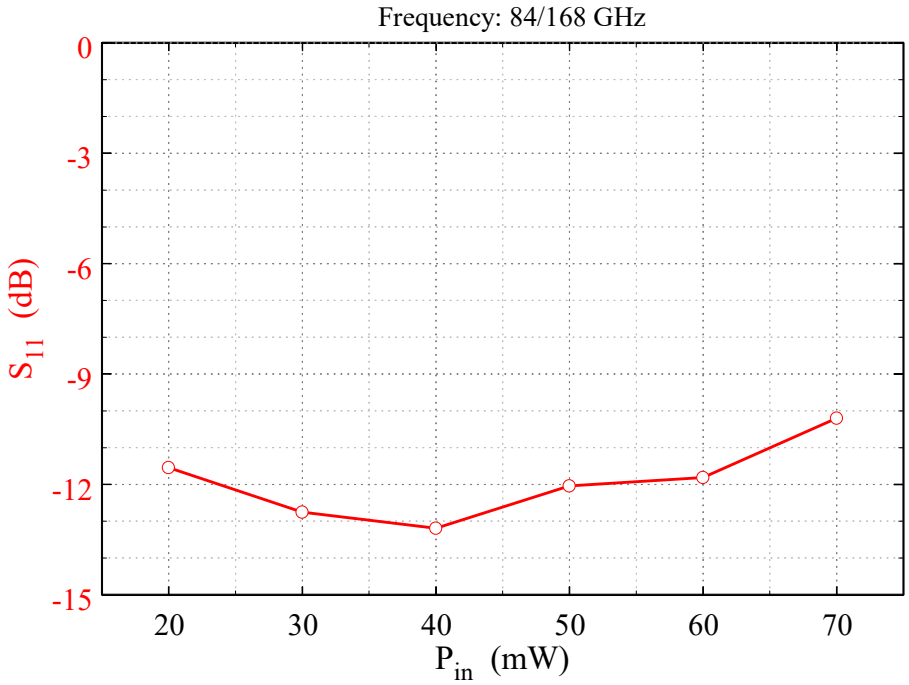


Fig. G.6. Measured input power reflection coefficient at 84/168 GHz.

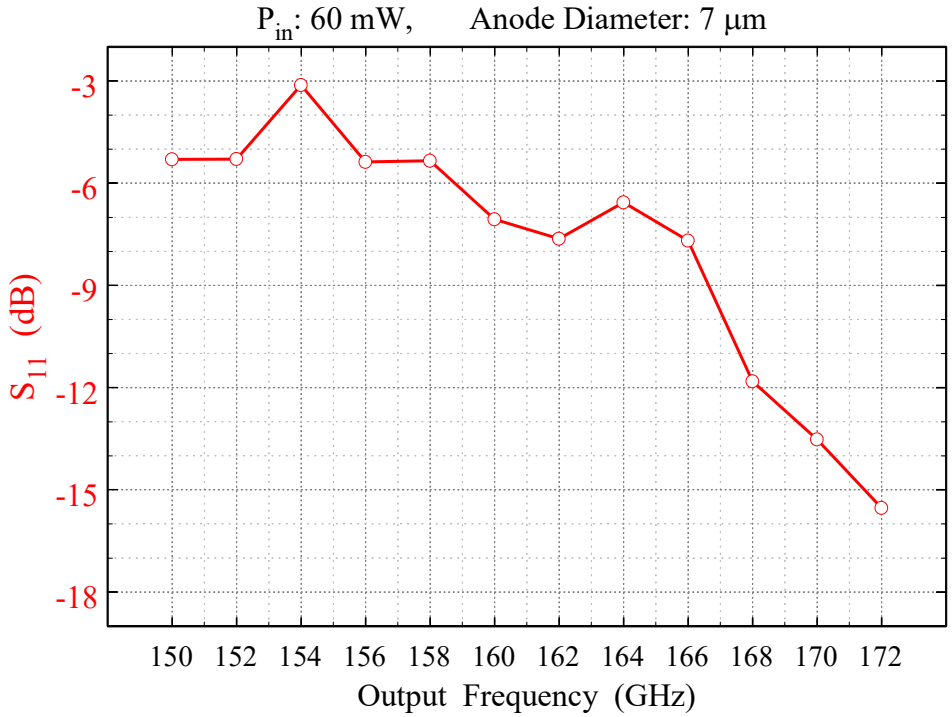


Fig. G.7. Measured reflected input power versus frequency for P_{in} = 60 mW.

A graph of measured DC bias voltage and current versus output frequency is shown in Fig. G.8. The voltages and currents shown in Fig. G.8 are those measured at the DC supply and thus the voltage across each varactor is one half that shown in the graph and the current through each varactor is one half that shown in the graph. The graph in Fig. G.5 shows that the peak efficiency for this varactor occurred at 84/168 GHz. At this frequency, the bias current through each varactor was less than 100 μA, indicating that the peak performance was obtained in a predominantly varactor mode of operation.

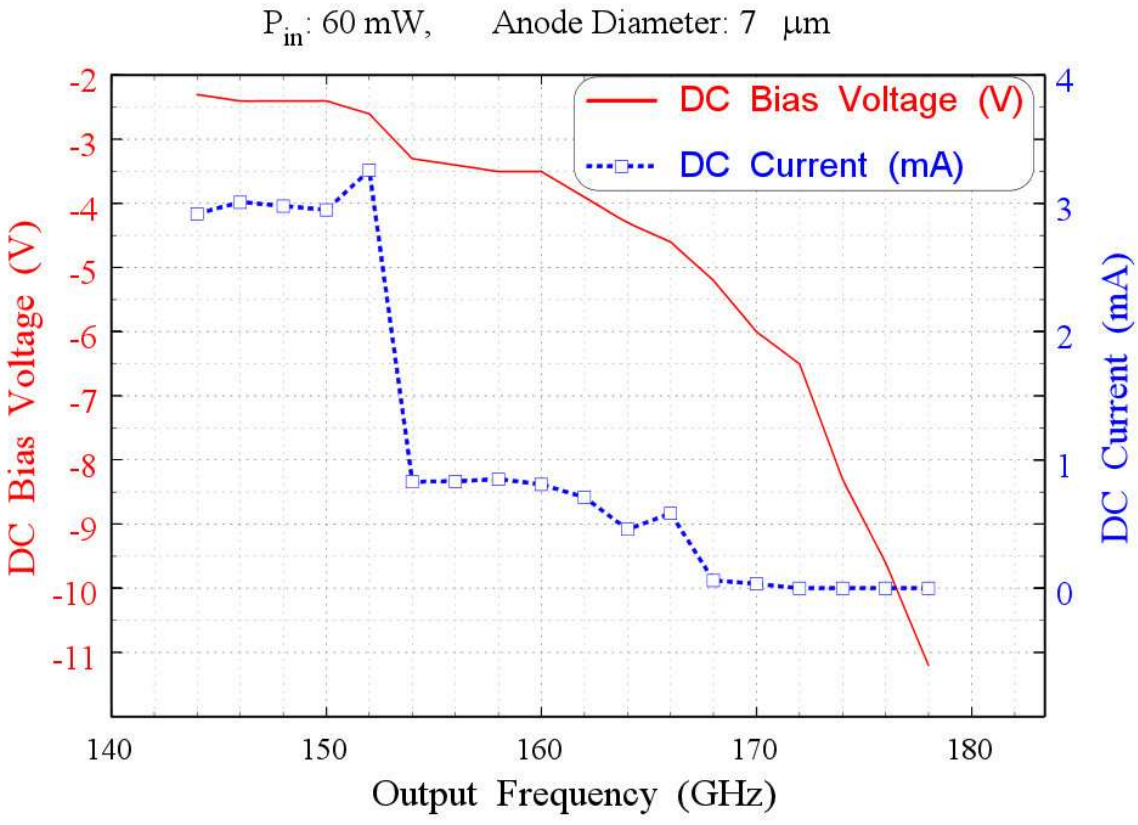


Fig. G.8. Measured DC current and bias voltage.

G.4 Summary

The preliminary tests for the 80/160 GHz doubler indicate a measured peak efficiency of 21%, peak output power of 16 mW and fixed-tuned bandwidth of greater than 15%. The measured output power is greater than 2 mW over the entire band from 144-178 GHz. DC current and bias voltage measurements indicate that the doubler is operating in a varactor mode when the peak efficiency is achieved.

The circuit and block were designed for a varactor chip with a zero biased junction capacitance of 63 fF. However, the measured zero biased junction capacitance for the tested varactor chip is 52 fF. The lower than expected capacitance causes the peak efficiency to occur at 84/168 GHz rather than the design frequency of 80/160 GHz and may additionally result in a reduced peak efficiency and output power. The tested varactor chip comprises 4 Schottky varactors with 7 μm anodes. Varactor chips with 7.5 μm anodes were fabricated in the same batch and these chips should yield improved performance.

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