# Fabrication, Characterization, and Application of Heterogeneously Integrated GaAs Schottky Diodes

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# APPROVAL SHEET

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# Abstract

Gallium arsenide Schottky diodes remain the predominant device technology for implementing sources, detectors, and heterodyne-based components for instruments operating from 100 GHz to more than 4 THz. Developments in submillimeter-wave diode technology have been aimed at improving fabrication yields, lowering device parasitics which degrade the electrical performance, and improving thermal management. In this process, the geometry and implementation of GaAs diodes have evolved from a stand alone "whisker" contact device to a planar Schottky diode integrated with various passive circuit components. In 2015, Alijabbari developed an initial process for integrating quasi-vertical gallium arsenide Schottky diodes on silicon substrates. Using this process, a 40-160 GHz frequency multiplier source was implemented, exhibiting high frequency translation efficiency (29%) and large output power (70 mW). However, the fabrication process suffered from low to modest yields. The focus of this thesis is to improve the fabrication process and assess the electrical and thermal characteristics of quasi-vertical GaAs diode heterogeneously integrated on Si. The improved process eliminates thermal fabrication steps, including ohmic contact annealing and high-temperature wafer bonding, which lead to wafer fracture and delamination. After that, a new method for extracting diode parasitics based on measurements of passive open and short circuited structures, fabricated on the same wafer as the diodes, is presented. Furthermore, the thermal behavior of the quasi-vertical diodes is investigated for the first time using a thermo-reflectance measurement technique. Finally, the robustness of the new fabrication process is further assessed through the implementation of a WR-5 (140-220 GHz) quasi-optical diode array.

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# Chapter 1

# Introduction

## 1.1 Terahertz Applications

The terahertz frequency band (300 GHz and 3 THz), which partly overlaps with the loosely-defined submillimeter-wave band (100 GHz to 1 THz), has been described as the final unexplored area of the electromagnetic spectrum. Because this spectral range (Fig. 1.1) lies at the transition between microwave and infrared/optical technologies, it exhibits a number of unique features and challenges that have been well documented [2], [3].

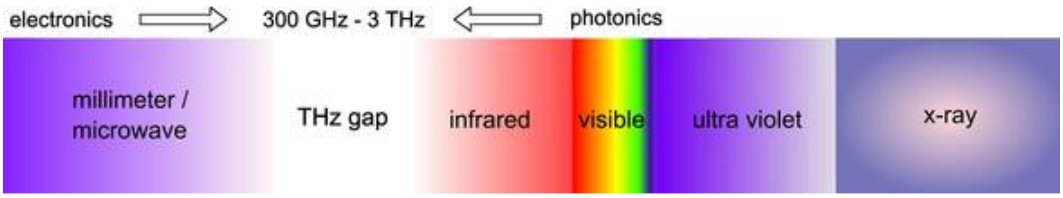



Figure 1.1: Frequency spectrum.

The energy ($h\nu$=1.2–12.4 meV) of terahertz radiation corresponds to many molecular modes and spectroscopic absorption lines, that cannot be observed in the microwave and infrared (IR) regimes. For instance, rotational and torsional modes of gas molecules (such as carbon monoxide, nitrous oxide, and propane), as well as vibrational modes of large biomolecules (such as DNA and proteins), can be studied in this region of the frequency spectrum [3], [4].The ability to measure molecular dynamics in all states of matter makes THz spectroscopy an important tool for radio astronomy. In security ap-

plications, THz waves permit the diagnostic and identification of gases and unknown compounds related to illegal drugs and explosives, for example [5]. The terahertz band is also attractive for imaging and radar applications due to the significant penetration of THz waves in many materials such as clothing and dielectrics, as well as the high resolution of the shorter wavelengths compared to millimeter waves. THz waves also have lower energy than x-rays and ultraviolet light, and are consequently non-ionizing. This property makes them an attractive alternative to high-energy imaging methods, paving the way for future medical applications. Finally, THz radiation could help overcome spectrum scarcity problems and capacity limitations of current wireless communication networks, by providing an unprecedentedly large bandwidth.

Although terahertz technology offers many advantages, progress in this area has long been hindered by a number of technical obstacles. These obstacles are imposed either by the propagation characteristics of medium, or due to the lack of suitable device technologies. Regarding the fundamental limitations, terahertz propagation suffers from poor atmospheric transmission and the large attenuation due to water vapor [6]. In addition, material characterization and measurements can be difficult due to increases in conductor and dielectric losses with frequency.

Concerning the device aspect, very few solid state technologies are available to access the THz spectrum. Below 100 GHz, electronic components such as amplifiers and oscillators are common. Above 10 THz, solid-state lasers, light-emitting diodes, and optical detectors are available [7]. In the terahertz transition region, neither of these technological approaches is dominant. The main device technologies available in the THz band, discussed in the following section, are superconductor-insulator-superconductor tunnel junctions (SIS), Microwave Monolithic Integrated Circuits (MMIC) technology, and Schottky diodes.

## 1.2 Device Technologies for Accessing the THz Spectrum

SIS tunnel junctions consist of two superconducting electrodes separated by a thin (on the order of a nanometer thick) insulating barrier. These junctions ideally possess a sharp current-voltage non-linearity and are often employed as heterodyne mixing elements [8]. The sensitivity of SIS based heterodyne receivers can approach the quantum limit (i.e. the noise temperature is below $3h\nu/kT$) [9]. As a result, SIS tunnel junctions are the work horse of most high-sensitivity radio-astronomy THz receivers. Another advantage of SIS based heterodyne receivers is that they require much lower local oscillator (LO) pump power levels. For example, a single pixel SIS mixer typically requires 40-100 μW of LO power, while a Schottky diode mixer requires at least 1mW [10]. Despite these advantages, SIS junctions are limited to operating at temperatures below 1 Kelvin (typically T<300 mKelvin) which restricts their use to cryogenic applications. High temperature superconductor SIS devices are still under investigation [10], however this subject is outside the scope of this dissertation.

Terahertz Microwave Monolithic Integrated Circuits (MMIC) technology, which encapsulates transistor, integrated circuit, and amplifier technologies, has made significant progress in the recent years towards operation in the THz spectrum. Under the sponsorship of the Defense Advanced Research Projects Agency (DARPA), improvements to the heterojunction bipolar transistor (HBT) and high electron mobility transistor (HEMT) device technologies have led to transistors operating with power gain cutoff frequencies $f_{max}$ approaching or exceeding 1 THz [11], [12]. Indium phosphite (InP) is the prime substrate technology for high frequency transistors. On one hand, HEMT devices outperform HBTs in terms of their high-frequency noise figure and high frequency operation. On the other hand, the critical dimension of the HBT is the base width (vertical dimension), which makes scaling independent of the lithography process. Furthermore, HBTs have higher current and power densities due to vertical current transport, which allows more compact device architectures [13]. Northrop Grumman's 1 THz HEMT MMIC based on 25 nm InP technology is currently the highest frequency MMIC circuit, with a fre-

quency range of 0.95 to 1.05 THz and an estimated 0.25 mW of output power. By scaling the gate length to 20 nm and under, and by keeping the gate to source parasitic capacitance $C_{gs}$ below 0.4 pF/mm and source resistance $R_s$ below $0.1\Omega.mm$, THz MMIC circuits will be attempted for $f_{max} > 1$ THz [14]. Most likely, THz MMICs will compliment the more mature Schottky diode-based multiplier technology, to provide high power sources and components for future receiver systems.

Presently, gallium arsenide (GaAs) Schottky barrier diodes are the most important room-temperature solid state devices for terahertz harmonic generation, upconvertion, and detection. The choice of the Schottky diode is due mostly to its high cutoff frequency, modest parasitics, and ability to be integrated into monolithic circuits. GaAs offers a combination of high mobility, large bandgap (which increases the barrier height, thus reducing leakage current), processing cost, maturity, and robustness [7]. Other III-V materials or device topologies (such as the Heterostructure Barrier Varactor [15]) are used in certain applications, but GaAs Schottky diodes remain the dominant technology for terahertz circuits. In terms of sources, frequency multipliers based on Schottky diodes dominate over other submillimeter-wave sources above 150 GHz all the way up to 1.2 THz. The principle behind these multipliers consists of up-converting the power at millimeter-wave frequencies, by cascading doubler and tripler stages all the way to the desired frequency. The non-linearity of the Schottky diode is utilized to achieve this frequency translation. The ability of THz Schottky diodes to efficiently up and down convert frequency signals has led to innovations such as the Virginia Diodes, Inc. (VDI) frequency extender modules (Fig. 1.2), which use diode mixers and multipliers to translate the operation of vector network analyzers (VNA) from 40-67 GHz (depending on the VNA unit) all the way up to 1.1-1.5 THz [16]! In order to achieve such a performance, the Schottky diode technology had to evolve significantly over the past decades. The next section discusses this evolution and the remaining challenges.

Figure 1.2: VDI frequency extension modules shown for size comparison to a typical VNA.

## 1.3 THz Schottky Diodes: Operation, Geometry, and Challenges

### 1.3.1 Operation

A Schottky barrier is formed when a metal is placed in intimate contact with a semiconductor such as GaAs. Both n- and p-type semiconductors can be used. However, for THz applications, n-type GaAs is the dominant semiconductor type due to its high electron mobility ($\mu_n = 8000$ cm$^2$/V . s) and the relatively low current leakage through the Schottky barrier (due to a large bandgap energy $E_g = 1.42$ eV) [17]. The energy band diagram for a Schottky barrier prior and post contact is shown in Fig. 1.3. For an ideal contact, the barrier height $\phi_b$ is calculated as the difference between the metal work function $\phi_m$ and the semiconductor electron affinity $\chi_s$. However, the barrier heights for various combination of metals have been measured experimentally, and are all close to 0.8 eV. This discrepancy is considered to be caused by the large density of surface states present on the GaAs material [18]. In thermal equilibrium, the semiconductor region adjacent to the metal is depleted of electrons. A built-in

potential $\psi_{bi}$ prevents the transport of electrons from the semiconductor side to the metal, which results in no current flow.

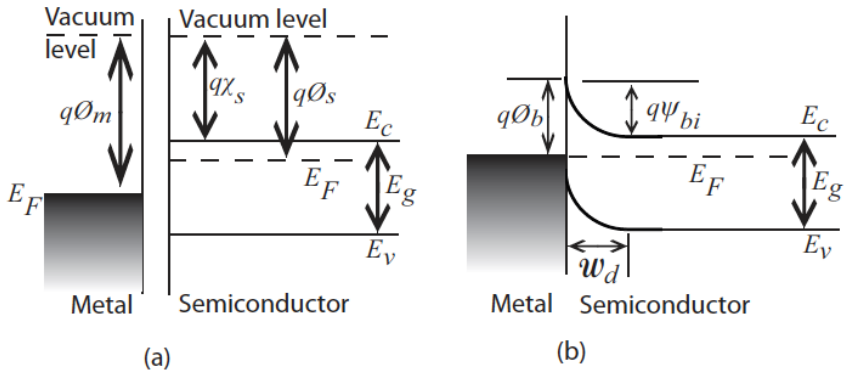



Figure 1.3: Energy-band diagram of a metal-semiconductor system: (a) prior contact; (b) ideal contact. $E_F$ is the Fermi energy, $E_g$ is the semiconductor bandgap energy, $E_C$ is the bottom edge of the conductance band, $E_V$ is the top edge of the valence band, $\phi_s$ is the semiconductor work function, and $\psi_{bi}$ is the built-in potential (from [17]).

If a positive voltage bias is applied, the barrier is lowered which allows the flow of electrons. Carrier transport is governed for an ideal junction by thermionic emission, and leads to the characteristic diode current-voltage (I-V) relation:

$$I(V,T) = I_S(e^{\frac{qV}{\eta KT}} - 1), \tag{1.1}$$

where $I_S$ is the reverse saturation current, q is the electronic charge, K is Boltzmann's constant, and T is the temperature. Diode which are meant to operate under the forward-bias condition utilize the voltage-controlled resistance property of the junction and are called varistors. Varistors are used in various applications which prioritize bandwidth over efficiency, such as broadband frequency multipliers.

When a negative voltage bias is applied, the barrier height is increased, resulting in zero current flow. In practice, a small current still flows, and is called reverse saturation current $I_S$. The depletion region is widened, resulting in a voltage-controlled capacitor. Therefore, Schottky diodes operating under the reverse-bias condition are called varactors.These devices are designed with

minimal series resistance, since it is not the parameter of interest, resulting in a highly efficient frequency translation process. However, the designs rely on a narrow range of capacitance values, which makes varactor-based circuits narrow band in nature. The capacitance-voltage characteristic of reverse-biased Schottky diodes is given as:

$$C_j(V) = \frac{C_{j0}}{\sqrt{1 - \frac{V}{\psi_{bi}}}}, \tag{1.2}$$

where $C_{j0}$ is the zero-bias junction capacitance, which can be written as:

$$C_{j0} = A\sqrt{\frac{q\varepsilon N_{epi}}{2\psi_{bi}}}, \tag{1.3}$$

where $\varepsilon$ is the semiconductor's dielectric constant, $N_{epi}$ is the donor level doping of the semiconductor, and A is the area. The remainder of this doctoral dissertation will be focused on varactor diodes. However, the concepts developed here can very easily be applied to varistor diodes.

### 1.3.2 Schottky Diode History

In 1874, Ferdinand Braun (a graduate student at the University of Berlin) noted that electrical rectification occurs between metals and certain crystal materials. In 1901, Jagadish Chandra Bose, a professor in Calcutta, India, filed a U.S patent for a galena crystal point-contact semiconductor diode for detecting radio signals. He invented the crystal detector. A year later, in 1902, Greenleaf W. Pickard, an engineer at AT&T filed a patent for a silicon point-contact detector in 1906 which was marketed as a "cat's whisker" crystal radio detector. A photograph image of a galena cat's whisker detector from the early 1900's [19] is shown in Fig. 1.4.

Early THz Schottky diodes (shown in Fig. 1.5) were all based a whisker metal in contact with an n-type semiconductor GaAs material. The whisker diodes exhibited very low parasitic series resistance and parasitic capacitance due to the proximity of the ohmic contact and geometry of the whisker connection to the Schottky anode. However, these metal-semiconductor diodes were not easily reproduced, and were mechanically unstable. Whisker diodes were

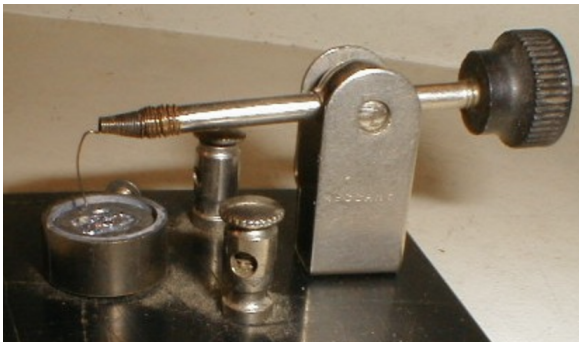


Figure 1.4: A galena cat's-whisker detector, an early radio wave detector used in crystal radio receivers from about 1905 to the 1940s (from [19]).

replaced with planar diodes, which are lithographically defined, thus improving process robustness and mechanical stability.

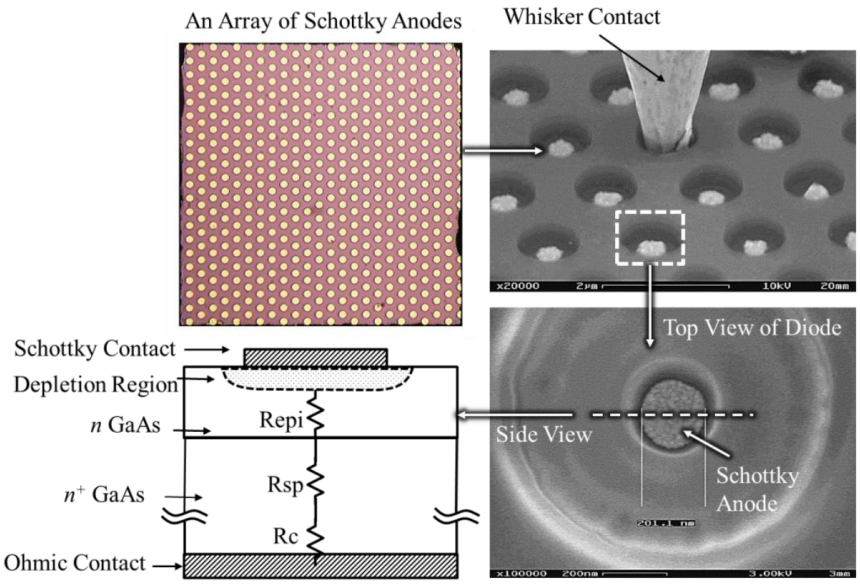



Figure 1.5: Whisker contacted Schottky diode (from [24]).

### 1.3.3 Improving Process Robustness: The Rise of the Planar Diode

In the mid-1980's, laterally oriented planar Schottky diodes began to replace single-element whisker-contacted diodes. Planar diodes are defined lithographically, which significantly improved the robustness and mechanical stability

of these devices. Furthermore, planar diodes enabled multiple anode circuit topologies, which were unrealizable with whisker diodes. Fig. 1.6 shows scanning electron microscope images (SEM) of a chip fabricated at the University of Virginia (UVA), which contains four Schottky diodes in an anti-series configuration. The diodes are connected using air bridge fingers which hover over a surface channel etched in GaAs (Fig. 1.6 (b)) [20].

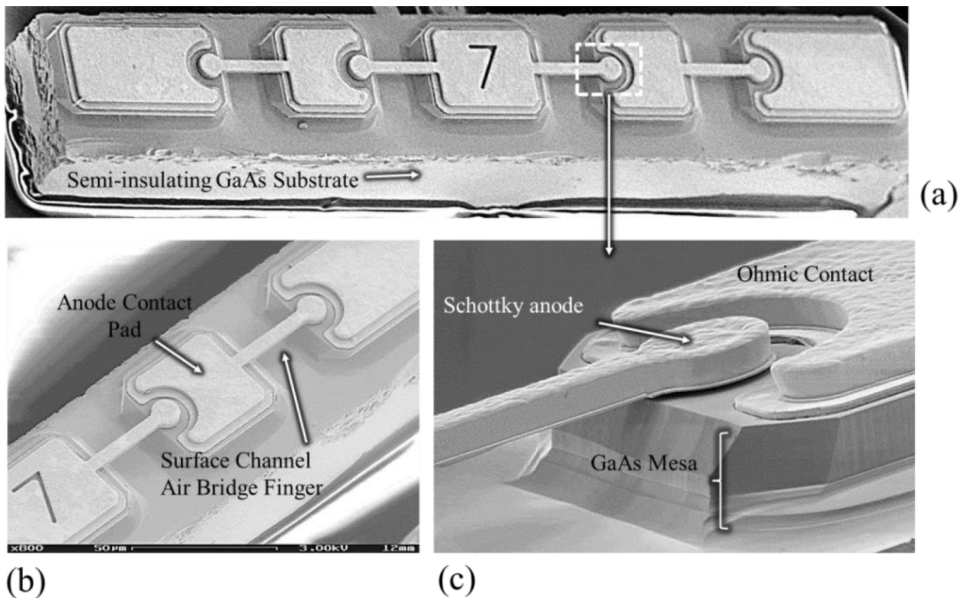



Figure 1.6: (a) Planar diode chip with 4 anodes (b) Close-up on the surface channel air bridge finger aimed at reducing the device parasitics (c) Close-up on the Schottky and ohmic contact.

The planar diode chips developed at UVA in the 1990's are flip-chip mounted devices. This means that once fabricated on a semi-insulating GaAs substrate (Fig. 1.6), they are transferred to a host substrate, which contains the necessary biasing and matching circuitry. This integration technique is hard to scale at high frequencies (>300 GHz), because the assembly becomes difficult, and the effects of the host substrate thickness, as well as the device positioning within its embedding network become very crucial to the circuit performance. An alternative method to flip-chip mounting is to fabricate the circuit on thick gallium arsenide, followed by a backside thinning process using lapping or dry etching to reduce the substrate thickness to the desired value. This method was developed at NASA's Jet Propulsion Laboratory (JPL), and many diode-

based circuits such as frequency doublers and triplers have been successfully implemented and deployed in space missions [21], [22].

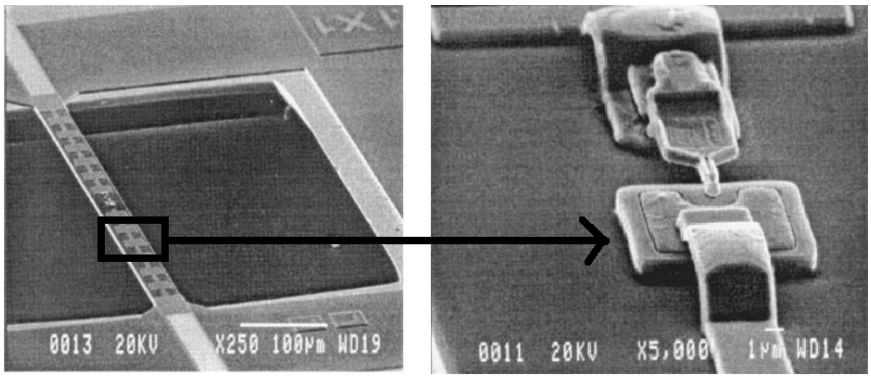



Figure 1.7: SEM micrographs of completed membrane and frame with 2.5-THz Schottky diode and RF low-pass filter structure. Frame dimensions are 1 mm x 1.4 mm 50 µm thick. Membrane is 36 µm x 600 µm 3 µm thick (from [21]).

The flip-chip bonded planar diodes as well as the GaAs membrane diodes offer significant advantages compared to the whisker diodes. However, these planar diodes do have some drawbacks. First, the planar geometry results in a more complex parasitic environment, often resulting in higher parisitics, especially series resistance [23]. Since the ohmic contacts of planar-oriented diodes typically subtend only half the anode circumference (Fig. 1.6), their associated series resistance tends to be twice what could be achieved with a fully encircled anode. Moreover, numerical studies comparing diodes with identical device parameters, but differing geometries, indicate that the series resistance of vertically-oriented diodes can be 20 to 30% lower than that of comparable planar devices. This reduction in resistance is attributed primarily to the reduction in dimensions of the GaAs mesa, thus mitigating current crowding due to the skin effect, and bringing the ohmic contact in closer proximity with the diode active region [24].

The other disadvantages of the thin membrane planar diodes are related to the material properties of GaAs which do not contribute to the active device performance. First, GaAs has a low modulus of resilience (50 MPa), which makes the thin ($<$50 µm) membranes mechanically fragile. As a point of reference, silicon has a modulus of resilience of 130 MPa. Second, GaAs has a relatively large dielectric constant (12.9), which exacerbates diode parasitics,

as well as critical dimensions of the passive circuitry (especially microstrip lines). Finally, GaAs is not a very good thermal conductor ($\kappa = 44$ W/m-K), which leads to thermal management concerns and, in some cases, device failures. Fig. 1.8 shows the performance of a 240 GHz frequency tripler operated at room temperature, based on the thin GaAs membrane technology [25]. The devices in the frequency multiplier failed at 240 mW of input power. C. Lee et al. [25] have attached a CVD diamond film as a heatspreader to the frequency tripler chip in order to improve its power handling capability. The frequency multiplier with the diamond heat spreader did not fail and was able to produce 40 mW for 350 mW of input power.

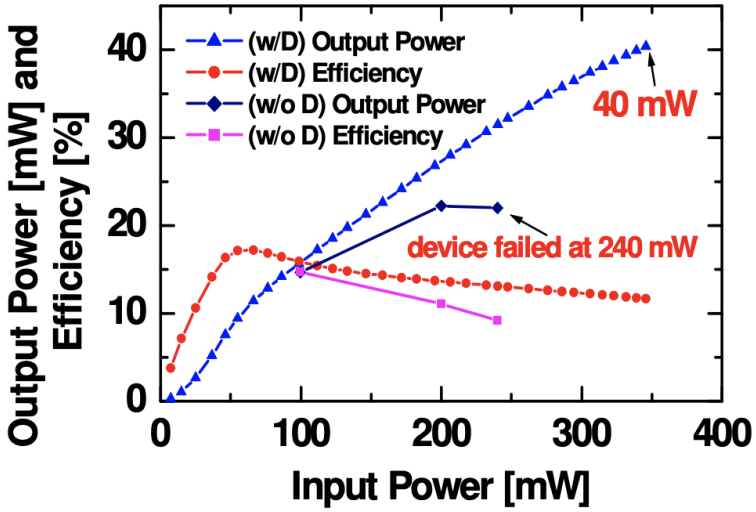



Figure 1.8: Output power and efficiency versus input power measured at 240 GHz for triplers operated at room temperature both with and without diamond heat-spreaders (from [25]).

Recognizing that no single material possesses all the necessary electrical, thermal, and mechanical properties required for optimum performance prompted terahertz researchers to investigate heterogeneous integration methods, which combine two or more dissimilar materials onto a single platform.

## 1.4 Heterogeneous Integration of THz Diodes and Quasi-Vertical Geometry

### 1.4.1 Heterogeneous Integration on Quartz

As discussed in the previous section, the loss, fragility, and poor thermal properties of semi-insulating GaAs has motivated the development of heterogeneous integration techniques, through which the GaAs device layer is transferred to a host substrate with superior mechanical and thermal properties. Table 1.1 summarizes the material properties [26], [27] relevant to heterogeneous integration of GaAs diode onto quartz or silicon.

Table 1.1: Substrate properties for GaAs, Si, and quartz: relative dielectric constant [26], loss tangent (at 10 GHz) [26], modulus of resilience (in MPa) [26], thermal conductivity (W/m-K) [27], and coefficient of thermal expansion ($10^{-6}$/°C) [27].

| Substrate | εr | tan δ | R | k | α |
|---|---|---|---|---|---|
| GaAs | 12.9 | .006 | 50 | 50 | 6.8 |
| Silicon | 11.9 | .004 | 130 | 157 | 2.3 |
| Quartz | 3.78 | .0001 | 2 | 6.2-12 | 0.5 |

Since the early 2000's, quartz has been the substrate of choice for heterogeneous integration of Schottky diodes at the University of Virginia and Virginia Diodes, Inc. due to its low dielectric constant (3.78) and low loss tangent (0.0001). The initial process development was done by Bishop [20], followed by Marazita [28], Schoenthal [29], and Midkiff [30]. In this process, the GaAs epitaxial layers are bonded on a temporary carrier. Then, the semi-insulating (SI) GaAs handle and AlGaAs layer are lapped and etched away, revealing the device layers. The temporary carrier with the device layers is subsequently bonded to a quartz substrate using Filmtronic's spin-on-glass (SOG). The silicon handle is then detached from the epilayers leaving the GaAs epitaxial layers attached to the quartz substrate. The quartz is then lapped to the desired thickness and diced to release individual chips. The quartz transfer process allowed the fabrication of the GaAs active devices with the matching/filtering circuitry all in one chip. However, quartz did not

permit the creation of beamleads, which are gold tabs that protrude out of a chip and allow a connection to be made with the outside world (typically a waveguide housing) [24]. Consequently, indium or silver epoxy must be used for bonding independently created beamleads to the matching network on the quartz substrate (as shown in Fig. 1.9), and the positioning and attachment of these beamleads require considerable dexterity and skill. Furthermore, the quartz substrate is not a good thermal conductor, and indium has a melting temperature of 150 °C, which limits the maximum circuit operating temperature. Attaching the quartz circuit using an adhesive also complicates circuit replacement and repair. An alternative to quartz was needed. As we will see in the section 1.4.3, that alternative will be silicon. But before we discuss the integration on silicon, we need to discuss one more evolution: the switch from planar diodes to quasi-vertical diodes.

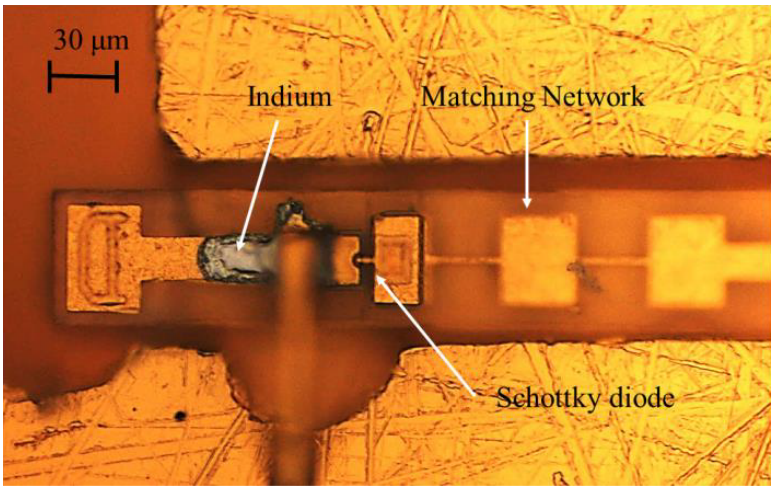



Figure 1.9: 1.6 THz integrated varactor side band generator circuit fabricated by Virginia Diodes, Inc. and assembled by Alijabbari (from [24]).

### 1.4.2 Quasi-Vertical Diodes

The planar diodes fabricated at the University of Virginia in the early 2010's suffered from high parasitic series resistances, which significantly affected the performance of the circuits fabricated using this technology such as phase shifters [24] and sideband generator arrays [23]. This served as a primary motivation to investigate quasi-vertical diodes which, like whisker diodes, have the

potential for smaller device parasitics compared to laterally oriented diodes. Fig. 1.10 compares diagrams showing a laterally and quasi-vertically oriented diode (QVD), both on a planar circuit. Details of the initial development and fabrication process for QVDs at the UVA can be found in [24]. Other institutions such as Damstadt University have developed other kinds of QVD, with different fabrication processes and performance [31]. The final development by Alijabbari at UVA was to combine the quasi-vertical geometry with heterogeneous integration on silicon.

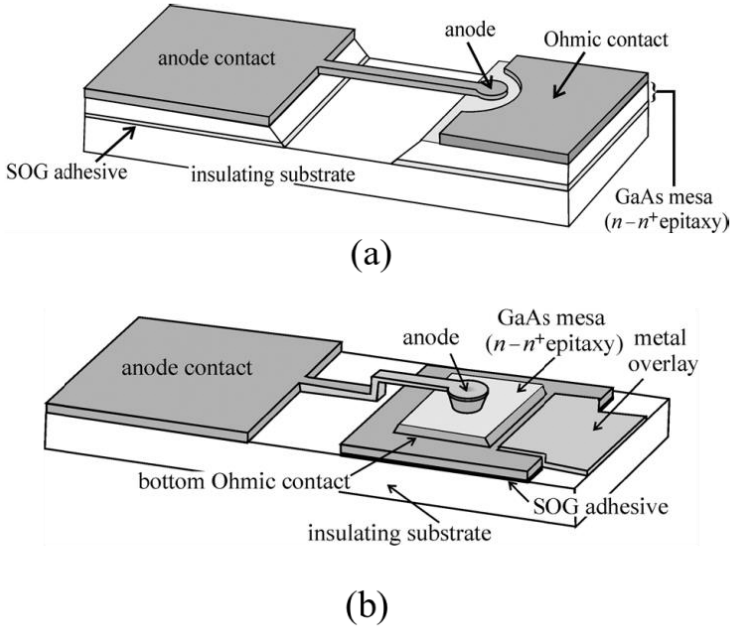



Figure 1.10: Diagrams showing the geometry of (a) a laterally-oriented planar diode and (b) a quasi-vertical diode integrated into a planar circuit.

### 1.4.3 Heterogeneously Integrated Quasi-Vertical Diodes

The high thermal and mechanical properties of silicon, as well as the low parasitics of the quasi-vertical geometry, have led Alijabbari in 2015 to develop a process of integrating quasi-vertical GaAs Schottky diodes on silicon substrates [32]. Additionally, the ability to grow very thin (as low as 1 $\mu$m) silicon layers on silicon dioxide (silicon-on-insulator a.k.a SOI technology) enabled Alijabbari (*et al.*) to build a 6-element 40-80 GHz frequency doubler (shown in

Fig. 1.11), and a 12-element 160 GHz frequency quadrupler, both integrated on 15 µm thick silicon substrates [1].

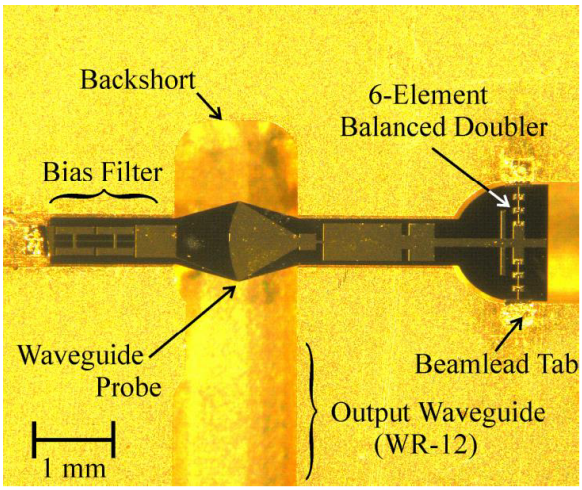



Figure 1.11: Image of frequency doubler mounted in a waveguide housing based on integrating quasi-vertical diodes on 15 µm silicon.

Fig. 1.12 summarizes the state of the art for the various THz Schottky diode technologies [33]. The QVD on Si technology developed at UVA compare well, and often outperforms competing technologies at similar operating frequencies (around 160 GHz), in terms of output power and efficiency.

Despite the success of the initial doubler and quadrupler circuits fabricated using QVD on Si, the quasi-vertical fabrication process suffers from many issues that limited the device yields (<10%), making this integration scheme impractical and prohibitive. A significant portion of this dissertation is dedicated to redeveloping the fabrication process to increase its robustness and improve the processing yields.

## 1.5 Thesis Outline

This doctoral research aims at the following goals: 1) to develop an improved fabrication process for gallium arsenide Schottky diodes integrated on silicon, which addresses the low yield issues 2) to evaluate the equivalent circuit model and parasitic extraction of quasi-vertical diodes on silicon, 3) to evaluate the thermal performance of the devices fabricated using the new diode process, 4)

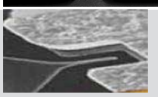
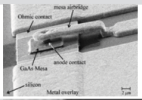
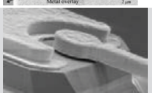
| Institution | Key technological features | Highest Freq. Mixer | Highest Freq. Multiplier | Highest reported efficiency (Output power) | Representative image |
|---|---|---|---|---|---|
| ACST GmbH, Germany | Quasi-vertical structure | 660 GHz (by RPG) | 600 GHz tripler | 30% @332 GHz doubler (14mW) |  |
| Chalmers Univ. of Technology, Sweden | Surface Channel Etch | 1200 GHz, Trec=3,000K (DSB) | 440 GHz doubler | 35% @ 170 GHz doubler (3.5 mW) |  |
| Farran Tech., Ireland | Not disclosed | 370 GHz, Tmix N/A | 325 GHz | 42.5% @190 GHz (80 mW) | Not provided |
| Jet Propulsion Lab., USA | Re-flow photoresist process, membrane diodes | 2,514 GHz, Tmix=9,000 K (with laser LO); 1200 GHz, Tmix=2800 K, | 2,700 GHz tripler | 25%@180 GHz doubler (120 mW) |  |
| Observatory de Paris, France | Re-flow photoresist process, membrane diodes | 1200 GHz, Trec=3,500K (DSB) | 300 GHz doubler | 27% 295 GHz doubler (10.5 mW) |  |
| Rutherford Appleton Lab., UK | Surface Channel Etch | 664 GHz, Tmix=3,500K | 220 GHz doubler | 29.4% @168 GHz (14 mW) |  |
| United Monolithic Semiconductors, France | BES Process | 380 GHz Tmix=4000 | 200 GHz | 7% @ 190 GHz (3mW) |  |
| University of Virginia | Quasi-vertical structure | - | 172 GHz quadrupler (x4) | 29% @160 GHz quadrupler (70mW) |  |
| Virginia Diodes Inc. , USA | Surface Channel Etch | 1,570 GHz, Tmix=5,900 | 3,100 GHz tripler | 25% @160 GHz, doubler (125mW) |  |

Figure 1.12: Summary of the various THz diode technologies reported in the literature (from [33]).

and finally, to assess the robustness of the new fabrication process by developing a diode phase shifter array based on QVDs on thin silicon membranes. The work performed in this thesis is divided into five remaining chapters:

- Chapter 2 describes the fabrication process development novelties.

- Chapter 3 discusses the RF characterization of quasi-vertical Schottky diodes and parasitic extraction.

- Chapter 4 discusses the thermal characterization and modeling of quasi-vertical Schottky diodes.

- Chapter 5 discusses the design, fabrication, and testing of the WR-5 (140-220 GHz) phase shifter array.

- Chapter 6 offers a conclusion and discusses future work.

# Chapter 2

# Process Development for Heterogeneously-Integrated Quasi-Vertical Schottky Diodes

An epitaxy transfer method developed by Alijabbari (detailed in [32]) allowed, for the first time, formation of quasi-vertical gallium arsenide (GaAs) Schottky diodes on silicon (Si). In contrast to diodes with planar (lateral) geometry in which anode and cathode contacts are formed on the same side of the GaAs, the quasi-vertical configuration incorporates a bottom cathode that serves as a low-resistance ohmic contact and thermal heat sink (Fig. 1.10) [32]. Although these devices have exhibited low parasitics at submillimeter-wave frequencies, the integration process developed by Alijabbari to fabricate quasi-vertical diodes suffers from low-to-modest yields ($< 10\%$ successful runs), largely arising from various thermal processes employed. In this chapter, an improved process is described for fabricating quasi-vertical GaAs Schottky diodes on Si. The process employs a non-alloyed ohmic contact. Furthermore, this effort develops an SU-8 bonding process that relies on low temperature curing, and does not, unlike previously reported SU-8 bonding processes [34], require a transparent substrate (processes that involve backside UV curing are limited to a few transparent substrates such as quartz). In fact, many existing processes require a transparent substrate such as quartz to perform backside UV curing of the SU-8. Schottky diodes fabricated using this method are characterized and compared to previously reported diodes, exhibiting compa-

rable performance with significantly better yield. The process development work, which was published in *IEEE Electron Device Letters* (2017) (publication #6 under List of Publications), was done in collaboration with Xie, who co-developed the process detailed in this chapter.

## 2.1 Prior Implementation

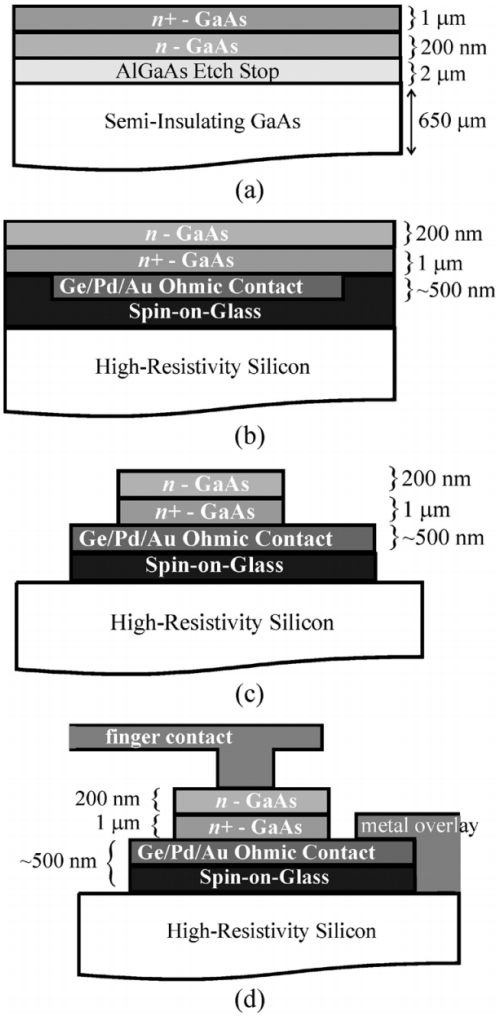



Figure 2.1: Outline of the quasi-vertical diode fabrication process: (a) GaAs epitaxy; (b) wafer bonding to silicon substrate; (c) mesa etch; and (d) final anode and cathode contact formation. Note the epitaxial layers shown in the figure are not to scale. (From [24])

The fabrication process developed by Alijabbari was based on a diode epitaxy consisting of a semi-insulating 650 µm GaAs handle, with three layers grown by Sumitomo Chemical Company, Ltd. (formerly known as Sumika), using metal organic chemical vapor deposition (MOCVD). These epilayers include a 1 µm AlGaAs etch stop layer, 280 nm n-GaAs ($2$ x $10^{17}$ $cm^{-3}$) and 1 µm n+-GaAs ($5$ x $10^{18}$ $cm^{-3}$) device layers as shown in Fig 2.1 (a).

Ohmic pads were formed using e-beam evaporation, followed by a liftoff process. More specifically, a Ge/Pd/Au (30/40/30 nm) metallization was evaporated, followed by gold electroplating (350 nm), and a second metal evaporation consisting of Ti (20 nm). After liftoff, the contact was annealed using a rapid thermal annealing tool (RTA) at 335 °C for 90 seconds, obtaining a low specific contact resistance of $5$ x $10^{-7}$ $\Omega.cm^2$ (measured using the standard transmission line method described in [18], [35]). A microscope image of a correctly annealed contact ("correct" as defined in [18], Chapt. 11) feature (alignment markers in this case) is shown in Fig. 2.2(a). The surface is smooth, with roughness of less than 100 nm, measured using a profilometer.

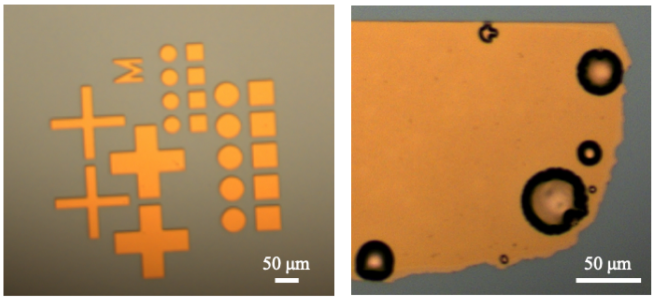



Figure 2.2: Microscope image showing a Ge/Pd/Au/Ti ohmic contact, annealed correctly. The surface is smooth (less than 100 nm), making it compatible with the subsequent bonding steps.

The annealing quality was very sensitive to a range of parameters including: the evaporation conditions in the e-beam tool, possible contaminants present in the solvents used during the surface pre-clean step (BOE and ammonium hydroxide), wafer cleanliness, and the RTA conditions. Among the relevant RTA conditions were the chamber cleanliness, calibration of the RTA's thermocouple, annealing temperature and time, and annealing ramp-up and ramp-down times. It was extremely difficult to control with a high level of reproducibil-

ity all the annealing process parameters in our laboratory environment, which lead a majority of the ohmic contacts to be either under- or over-annealed (see [18], Chapt. 11). Furthermore, almost all the ohmic contact runs ($>$ 80%) suffered from "balling-up", as illustrated in the microscope image shown in Fig. 2.2(b). The height of the balled-up area is more than 1µm larger than the rest of the sample surface (measured using a profilometer). This surface non-topography lead to complications in the bonding/thinning process, since the adhesive used for bonding (discussed in the next paragraph) couldn't be spun uniformly slower than 2.5 krpm (leading to roughly 1 µm thin film), and did not adhere well to the balled-up pads, which ended up peeling off from the surface after the bonding/thinning steps.

After the ohmic contact formation, the III-V substrate which included topographical features (ohmic pads), was bonded onto a high-resistivity ($\rho > 10$ $k\Omega.cm$) silicon substrate using a 500 nm spun coated spin-on-glass (Filmtronics FG65) film, cured at 195 °C. The thick GaAs handle was wet etched using a fast nitric acid based solution, followed by a slower citric acid based etch. The AlGaAs etch stop layer was removed in HF, exposing the n-type GaAs device layers (Fig 2.1 (b)). The thinning process rarely resulted in a smooth defect-free GaAs epitaxy film. In fact, the defect-free GaAs epitaxy, which was never achieved on a sample with balled-up features, only occurred in 1% of the total samples processed. Some samples (19% of total samples) suffered from a tolerable level of cracking (at least one crack) and delamination (usually around the edges) of the thin GaAs epitaxy bonded to silicon, as illustrated in Fig. 2.2(a), which decreased the effective area that could undergo the remaining diode processing steps. The vast majority of the samples (80%) suffered from severe cracking and delamination (shown in Fig. 2.2(b)), which prevented further processing.

The final diode processing steps included the device mesa and anode formations. The device mesa was formed lithographically, followed by another citric acid wet etch to remove the un-needed GaAs. The residual SOG remaining on the substrate was removed using reactive ion etching (Fig 2.1 (c)). Finally, the finger Schottky contact, metal overlay, and other circuit features were formed using standard lithography steps, metal seedlayer sputtering, and electroplating, resulting in the structure shown in Fig 2.1 (d) and Fig. 2.4.

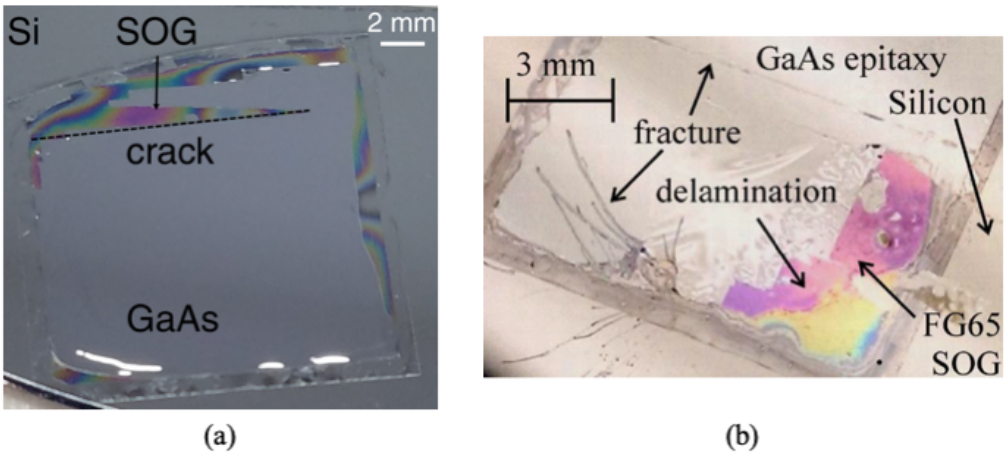



Figure 2.3: Microscope images showing the GaAs active device epitaxy after bonding and thinning. The surface suffers from cracks and delamination of the GaAs epitaxy.

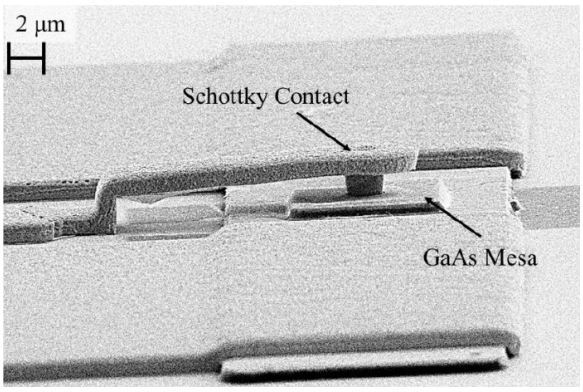



Figure 2.4: SEM image of a completed GaAs QVD Schottky diode heterogeneously integrated on Si using the process developed by Alijabbari.

Diodes fabricated using this process were measured at DC and RF frequencies, exhibiting low parasitic resistance values (3-6 Ω at DC, <15 Ω from 500-750 GHz) and low parasitic capacitance values (<5 fF) [24], [32]. This lead Alijabbari to successfully implement and characterize a 40-160 GHz quadrupler based on this technology, with 29% efficiency and 70 mW of output power [24], [1]. However, as described earlier, the diodes fabricated using the process developed by Alijabbari suffered from low-to-modest yields (only 1% of the samples were defect-free past the bonding/thinning steps!). The remainder of this chapter discusses the process modifications which address this major

problem. The two process steps identified to be limiting the fabrication yields have been identified as the ohmic contact formation, and the epitaxial transfer steps.

## 2.2 Ohmic Contact

The function of the ohmic contact is to provide a low resistance junction, that allows the current to flow from the diode to the outside circuit. The contact should have a linear I-V characteristic, and be stable over time and temperature. For terahertz Schottky diodes, the ohmic contact resistance can dominate the overall parasitic series resistance of the device. Reducing this series resistance is crucial to achieving good device performance, critical in applications such as high efficiency frequency multipliers, mixers, and other varactor based circuits.

### 2.2.1 Background

Forming an ohmic contact to GaAs is not a trivial task, and has been the subject of a large amount of solid-state physics and experimental development [18]. In fact, any metal that contacts a wide bandgap semiconductor such as GaAs will result in a rectifying barrier (refer to Fig. 1.3), rather than an ohmic contact. The Schottky barrier results from bending of the valence and conduction bands to make the Fermi levels on both sides of the junction equal under thermal equilibrium. As illustrated by the band diagrams shown in Fig. 2.5 [36], increasing the doping concentration of the n-type GaAs and/or lowering the barrier height are the two means for creating an ohmic contact. In the next subsection (2.2.2), we will investigate various choices of metal stacks which, once annealed, diffuse dopants into the n-type GaAs material, thus forming an ohmic metal. We will see that the annealed contact strategy cannot guarantee the surface planarity that is necessary to the QVD epitaxial transfer process (bonding GaAs to Si). We will then investigate in Section 2.2.3 a method of barrier height lowering through bandgap engineering.

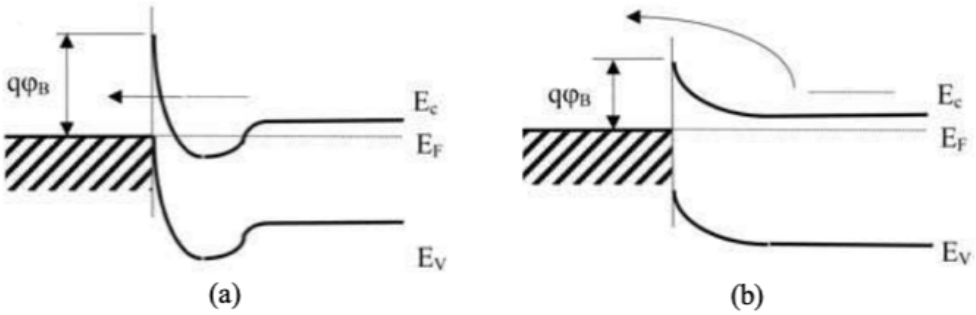



Figure 2.5: Band diagram of a metal/n-GaAs ohmic interface using: (a) tunneling achieved through a high level of doping (b) thermionic field emission through barrier height lowering (From [36]).

### 2.2.2 Annealed Contact

To form an ohmic contact on n-type doped GaAs, the necessary doping level is at least $10^{19}$ $cm^{-3}$. These levels are not commonly achieved using the most cost-effective options for growth production which include ion implantation and MOCVD [18]. Many factors contribute to the difficulty in doping n-GaAs beyond $10^{19}$ $cm^{-3}$. Silicon, which is the most common n-GaAs donor, has a maximum doping concentration of 5 x $10^{18}$ $cm^{-3}$ due to solubility limits of silicon dopants in GaAs [37], and charge compensation mechanisms [38]. Even Si doped n-GaAs wafers grown using MBE (molecular beam epitaxy) methods exhibit considerable self-compensation beyond doping levels of $10^{19}$ $cm^{-3}$ [39]. The growth of GaAs doped with other atoms such as tellurium (Te) by MOCVD has not been widely used because of its surfactant nature (small amounts of Te atoms modify the processes on the surface), which adds an extra degree of complexity and freedom to the growth [40].

Due to the challenges in achieving doping concentrations $>10^{19}$ $cm^{-3}$ using growth methods, dopants are typically introduced instead through metal deposition and diffusion after annealing. The most common way to form an ohmic contact to n-GaAs is to use a gold-based metallization, which is heat treated for a short time period at temperatures in the range of 300-500 °C. The contact schemes are designed to supply a suitable dopant (Ge for example) and possibly an additional element improving contact adhesion and/or its morphology (such as Pd) [41]. As discussed before, the Ge/Pd/Au/Ti scheme

results in a very low specific contact resistance ($5$ x $10^{-7}$ $\Omega.cm^2$). However, the resulting surface roughness and ball-up (Fig 2.2) which is on the order of hundreds of nanometers, as well as alloy and surface tensions, make this scheme incompatible with the stringent surface flatness requirement of wafer bonding.

A nickel-based metallization was also considered to replace the Ge/Pd/Au/Ti metal stack. Ni was historically included to act as a wetting agent and prevent the AuGe metal from balling-up during alloy [18]. Diodes were fabricated using a Ni/Ge/Au/Ti metallization, which was annealed at temperatures which varied from 420 to 450 °C. The nickel was successful in alleviating balling-up issues, however the surface morphology was very poor. The nickel based contacts exhibited surface roughness on the order of hundreds of nanometers (as shown in Fig. 2.6) and a very large series resistance ($>$ 20 $\Omega$).

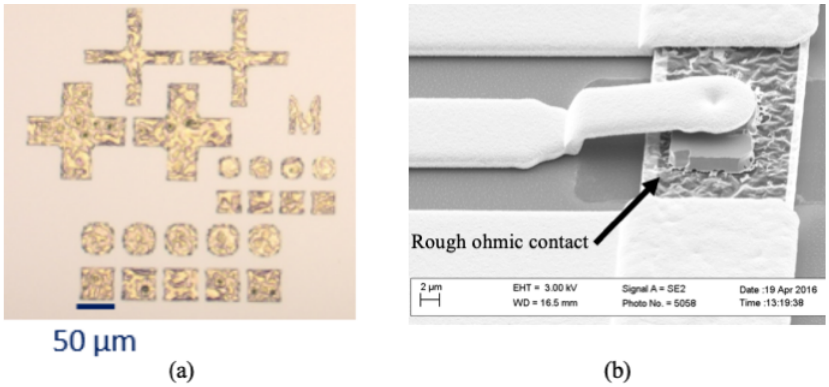



Figure 2.6: Rough surface ($>$ 100 nm) of ohmic pads features fabricated using a Ni-based alloy shown in: (a) a microscope image of alignment markers, and (b) SEM image of a completed diode using the Ni-metallization.

A final attempt was made at making QVD with a Ti/Au/Ti metallization, without any annealing. Single diodes DC measurements showed very large series resistance ($>$ 50 $\Omega$), and a 40-160 GHz quadrupler implemented using this unalloyed metal stack gave zero output power. The struggles in making quasi-vertical GaAs diodes on silicon using annealed contacts lead us to investigate non-annealed ohmic contacts to GaAs through bandgap engineering, by adding InGaAs layers to the GaAs epitaxy.

### 2.2.3 Adding InGaAs Cap Layers

InAs is an attractive material choice for un-annealed ohmic contact formation to GaAs [42], due to its small bandgap of <0.4 eV (see Fig. 2.7 [43]), and a surface Fermi level that is pinned in the conduction band [35]. Consequently, InAs and InGaAs are often used as epitaxial surface contact layers for non-alloyed ohmic contacts, when the device structure allows it [35], such as the emitter surface of HBTs [44]. However, the incorporation of indium into gallium arsenide increases the lattice constant (Fig. 2.7), and produces compressive strain. For typical indium concentrations of 30-50%, the cap relaxes by creating point defects [35]. It is necessary to design the cap layer in a way that minimizes these effects.

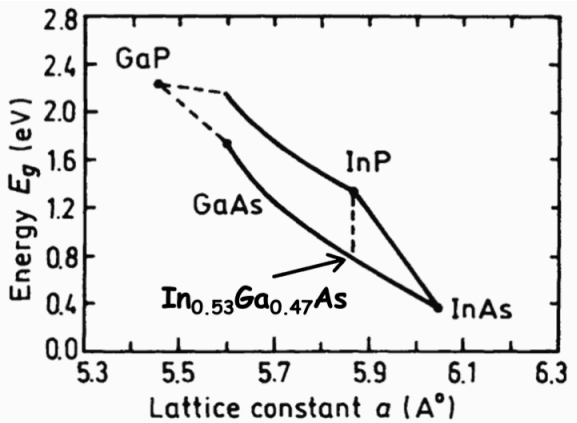



Figure 2.7: Energy gap versus lattice constant for InGaAs. The band gap decreases with In content. Note that $In_{0.53}Ga_{0.47}As$ is lattice matched to InP (From [43]).

The approach of adding InGaAs cap layers for ohmic contact formation is new in the context of quasi-vertical diodes. However, it has been well-established for forming ohmic contacts in heterojunction bipolar transistors, both in academic research and industry [44]. The cap layers for our diodes are grown on top of the GaAs device layers by Sumitomo Chemical Company, Ltd. using MOCVD. The design of these cap layers, summarized in Table 2.1, is based on the Sumimoto's established commercial HBT process. The cap layers consist of a highly doped ($> 10^{19}\ cm^{-3}$) $In_xGa_{1-x}As$ layer with a high indium content (x $\approx$ 0.60 [37]), grown on top of a highly doped $In_xGa_{1-x}As$

Table 2.1: New GaAs epitaxy for quasi-vertical diodes with InGaAs cap layers

| Epitaxial Structure | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| No. | Material | Composition | Thickness Target (um) | Thickness Tol. | C/C ($cm^{-3}$) Target | C/C Tol. | Dopant | Carrier Type |
| 6 | $In_yGa_{1-y}As$ | y = 0.60 | 0.0400 | ±10% | >1.0E19* | N/A | Te | N++ |
| 5 | $In_yGa_{1-y}As$ | y = 0 → 0.60 | 0.0500 | ±10% | >1.0E19* | ±10% | Te | N++ |
| 4 | GaAs | | 1.000 | ±10% | >5.0E18 | ±10% | Si | N++ |
| 3 | GaAs | | 0.2800 | ±10% | 2.0E17 | ±10% | Si | N |
| 2 | $Al_xGa_{1-x}As$ | x=0.50 | 1.0000 | ±10% | -- | N/A | -- | -- |
| 1 | GaAs | | | ±10% | -- | N/A | -- | -- |
| Substrate | | | | | | | | |

graded layer (x: 0→0.6). The graded layer avoids the large conduction band discontinuity, and therefore barrier for charge transport, that would otherwise result from a sharp transition between two materials with a large bandgap mismatch (InAs and GaAs) [42]. The layer thicknesses are 40 nm and 50 nm, for the graded and constant indium concentration layers respectively. The resulting band diagram for the ohmic contact is shown in Fig. 2.8.

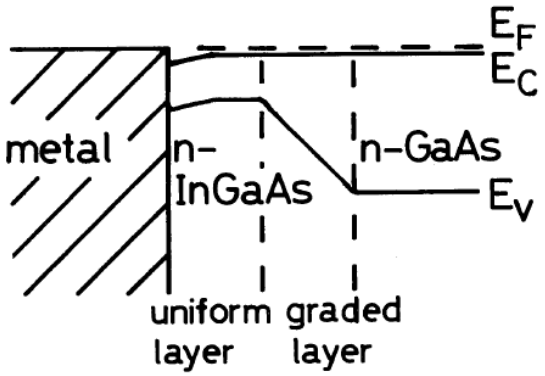



Figure 2.8: Band diagram for metal-InGaAs ohmic contact interface (From [37]).

The ohmic metal stack consists of Ti/Pd/Au/Ti layers, which are sequentially e-beam evaporated (in-situ) on the III-V surface. Titanium serves the purpose of an adhesion layer. The thickness of those layers are set to 20 nm for Ti, and 40 nm for Pd [45]. The gold thickness varies depending on the design frequency of operation, but is generally chosen to be thicker than one skin depth.

The transmission line method (TLM) is used to characterize the specific contact resistance of this ohmic contact scheme. The TLM method employs

a test pattern composed of differently spaced ohmic contacts, as illustrated by the diagram in Fig. 2.9. Ohmic contacts are formed on a semiconductor surface and separated by distances L (see Fig. 2.9). The contacts have a width W, and the pattern is isolated to restrict current to flow only across the distance L (the current flows in the region colored in blue in Fig. 2.9) [18].

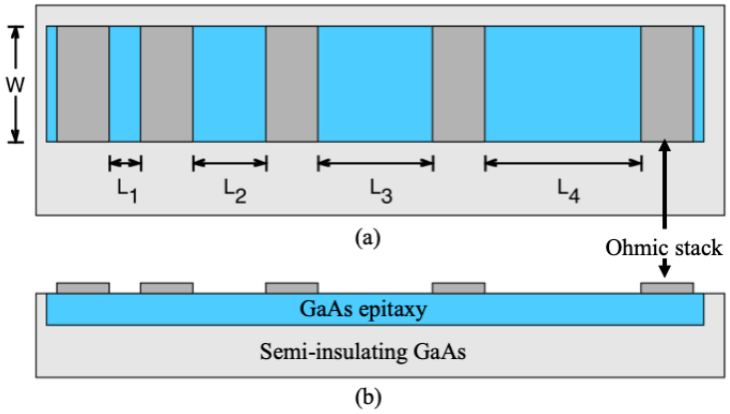



Figure 2.9: Diagram illustrating the TLM method: (a) top view of the wafer, (b) side-view.

To perform the TLM method on the new GaAs epitaxy, ohmic pads with various separations (12 µm, 16 µm, 22 µm, 30 µm, 42 µm, 52 µm, and 102 µm) are formed on the InGaAs/GaAs substrate (Fig. 2.10) using e-beam evaporation, and a liftoff process. The pads are isolated using a citric acid based etch. Since the GaAs surface is reactive and can form oxides, a surface treatment is usually performed before metal evaporation. Two different surface treatment preparations are investigated on two samples [46] to remove native oxide pre-metal deposition. The first sequence (sample A) consists of an immersion in buffered oxide etch (BOE) solution for 2 mins, followed by a dip in a diluted ammonium hydroxide ($NH_4OH$) solution (1:10 dilution in deionized water) for 20 secs, DI rinse and ($N_2$) blow dry. Ammonium hydroxide is used for sample A because it has been shown to reduce the surface oxygen content, along with gallium and arsenic oxides on the surface [47]. The second sequence (sample B) is similar to the previous one, except that the ammonium hydroxide step is omitted. After that, the two samples are loaded in an electron beam evaporator chamber that is evacuated to a pressure of $2\text{x}10^{-7}$ torr. The Ti (20 nm)/ Pd (40 nm) / Au (200 nm) metallization is deposited on the two samples,

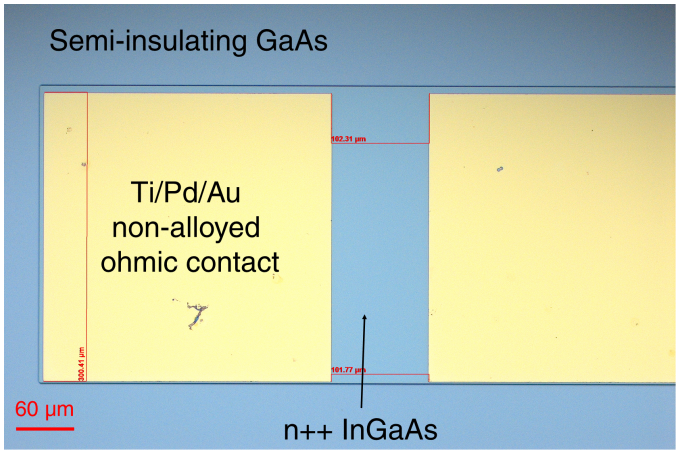



Figure 2.10: Microscope image showing two rectangular pads on a mesa used in the TLM measurement.

followed by liftoff. The square patterns are then isolated into a large mesa, in order to confine the current strictly to the area in between two consecutive pads. This is achieved by a citric wet etch, followed by AlGaAs removal in HF.

The resistance of each contact pair is measured using a four-point probe method, and is plotted versus contact separation for the two samples, as shown in Fig. 2.11. Each sample contains two sets of identical TLM structures. The y-intercept of the graph in Fig. 2.11 corresponds to twice the contact resistance (2*$R_c$). The transfer length, which is the average distance traveled by an electron in the semiconductor beneath the contact before flowing into it, corresponds to half the x-intercept value. The specific contact resistance is the product of the contact resistance, transfer length, and pad width (300 µm). The transfer lengths $L_T$ and $L'_T$ (corresponding to each set), along with the specific contact resistance $\rho_c$ and $\rho'_c$ measurement results are summarized in Table 2.2 below:

Table 2.2: Summary of the TLM specific contact resistance measurement

| Sample | $L_T$ (µm) | $L'_T$ (µm) | $\rho_c$ ($\Omega.cm^2$) | $\rho'_c$ ($\Omega.cm^2$) | $\rho_c^{avg}$ ($\Omega.cm^2$) |
|---|---|---|---|---|---|
| A | 49.3 | 54.8 | $7.25 * 10^{-7}$ | $9.14 * 10^{-7}$ | $8.19 * 10^{-7}$ |
| B | 54.4 | 52.5 | $8.92 * 10^{-7}$ | $8.19 * 10^{-7}$ | $8.55 * 10^{-7}$ |

We can see from Table 2.2 that the two different surface pre-treatments resulted in a similar specific contact resistance of $\sim 8 * 10^{-7}$ $\Omega.cm^2$, which is

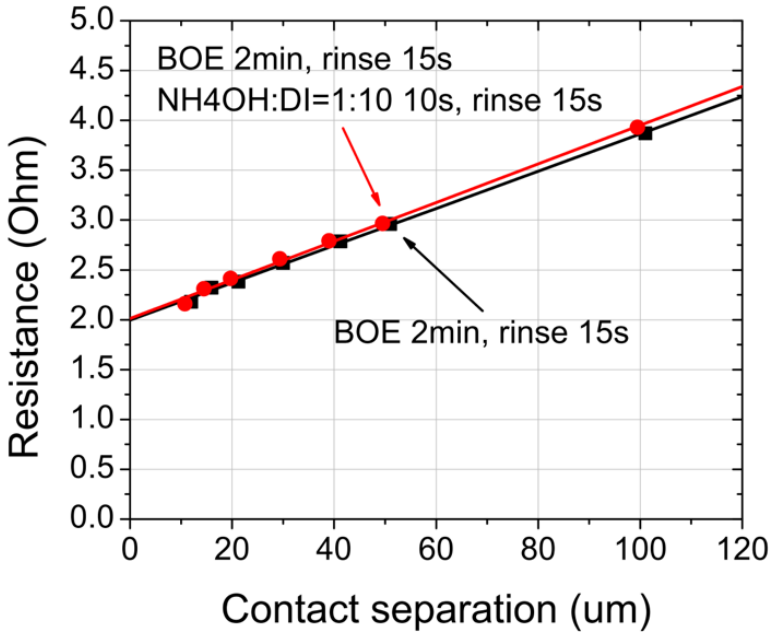



Figure 2.11: TLM plot showing the resistance for different adjacent pad separations. Two surface preparations are investigated.

comparable to, but 60% higher than the value obtained using the annealed ohmic contact process ($5 * 10^{-7}$ $\Omega.cm^2$). In conclusion, this non-annealed method offers a sufficiently low specific contact resistance value which is suitable for our applications, eliminates the need for an annealed contact, and makes the ohmic contact formation step more reliable and repeatable.

## 2.3 Epitaxy Transfer and Bonding

The second critical fabrication step investigated in this work is the epitaxial transfer of the GaAs substrate onto silicon. Heterogeneous integration, which aims at combining the electrical properties of GaAs with the superior mechanical and thermal properties of Si, can be achieved in numerous ways. These methods include direct bonding, anodic bonding, metal bonding, and adhesive bonding. Direct bonding describes a method to join mirror-polished semiconductor wafers at room temperature without the addition of any glue or external forces [48]. Because the quasi-vertical geometry requires the formation of the ohmic metal prior to bonding, direct bonding cannot be considered.

Anodic bonding provides high-quality hermetic seals between two materials with similar thermal expansion coefficients such as silicon-silicon (using a thin intermediate glass film) or silicon and glass [48]. Even though anodic bonding can tolerate rougher surfaces compared to direct bonding, this process makes use of alkali-containing glasses and necessitates strong electric fields and high temperatures (300-450 °C) [48], which makes it incompatible with our diode process. In this work, we choose to focus on adhesive bonding for its relative low curing temperatures, simplicity, robustness to the wafer surface topology, and compatibility with many materials [49]. Finally, metal bonding uses a metal as the intermediate layer between the two surfaces to be bonding. This process could therefore be compatible with the QVD process. However, it is more complex than adhesive bonding, and requires dedicated bonding equipment.

The previous process developed by Alijabbari employed spin-on-glass as the adhesive. The silicon and GaAs epitaxy were pressed against each other in a bonding jig under vacuum, while applying a force of $\sim$ 250 N and a temperature of 195 °C [32].

Si and GaAs have dissimilar coefficients of thermal expansion. Moreover, SOG films are prone to cracking, because large volume shrinkage is associated with the curing process [50]. Therefore, the bonding process using spin-on-glass (SOG) often results in cracking in the GaAs device layers post handle removal (refer to Fig. 2.3). To improve the yield of the fabrication process, the SOG is replaced with SU-8 (Microchem), a negative epoxy-based photoresist commonly used in MEMS packaging applications to produce high-aspect ratio features [51]. The relatively low curing temperature of SU-8 (100—140 °C) compared to SOG ($\sim$ 200 °C), coupled with its relatively lower percent volume shrinkage after cross-linking results in a more robust epitaxy transfer.

The new bonding process starts with extensive cleaning of the silicon and III-V substrates (detailed in Appendix A). The Si substrate is then spin coated with SU-8 (9700 rpm, 35s). After that, the coated sample's backside and edge bead are cleaned using an AZ-EBR solution. The silicon sample is then mounted on a transparent glass force distribution plate using a drop of L-grease. The mounted sample is soft baked for 1 minute at 110 °C on a hot plate, and UV exposed (280 mJ/cm$^2$). The remaining steps are performed in a

bonding jig shown in Fig. 2.12 [24]. The III-V is placed in the jig as shown in the schematic (Fig. 2.13). The silicon is positioned face down above the III-V. The Si and III-V samples are initially separated by a gap as shown in Fig. 2.13 (a). Even though this bonding press does not have any alignment capability, the use of a transparent force distribution plate, and the fact that the GaAs sample is diced smaller than the silicon sample (40% smaller) simplify manual hand alignment. After a 40-minute outgasing period, the two samples are pressed together and cured at 140 °C for 40 mins as shown in Fig. 2.13 (b). The final adhesive layer of SU-8 is approximately 250 nm thick.

Figure 2.12: Bonding press used in this work [24].

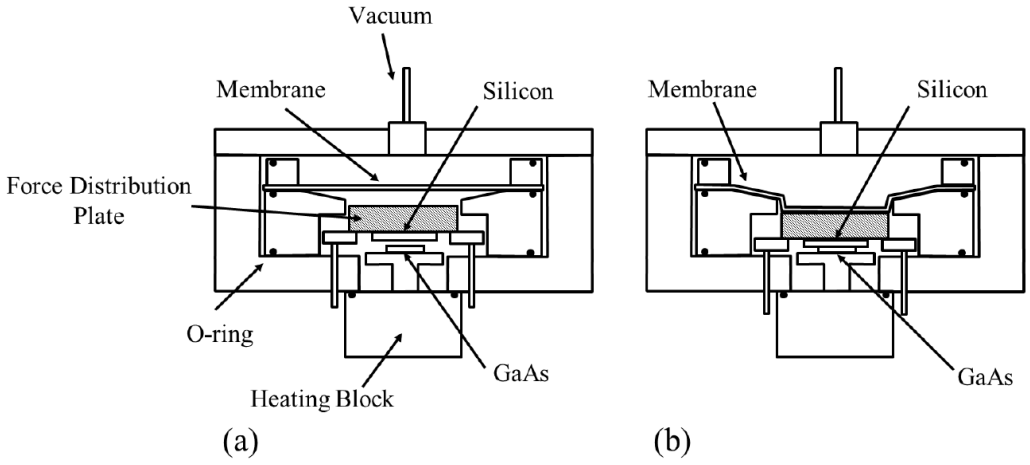



Figure 2.13: (a) cross section view of the membrane press before bonding GaAs to SOI, (b) view of the press during bonding.

One issue that needed to be addressed is that SU-8 does not adhere well to the highly doped InGaAs layer, which results in peeling of the device layers after removal of the GaAs handle as shown in Fig. 2.14. Furthermore, the III-V surface contains topography, which consists of the ohmic pads formed prior to bonding (see Section 2.1). The lack of surface planarity results in complications during bonding such as cracking and delamination (refer to Fig. 2.3). Consequently, the decision was made to planarize the III-V surface prior to bonding using the ohmic metal stack. The top titanium layer serves as adhesion for the SU-8, thus alleviating the issue pertaining to the non-adhesion of SU-8 on doped n-type InGaAs. This results in a repeatable and reliable bonding, with the cracking issue resolved and very few runs ($< 25\%$) experiencing delamination. The delamination problem can be eliminated completely by carefully cleaning the GaAs and Si surfaces (see Appendix A for details) and obtaining defect-free GaAs wafers from Sumimoto. The bonding interface is uniform and free of voids as shown in Fig. 2.15.

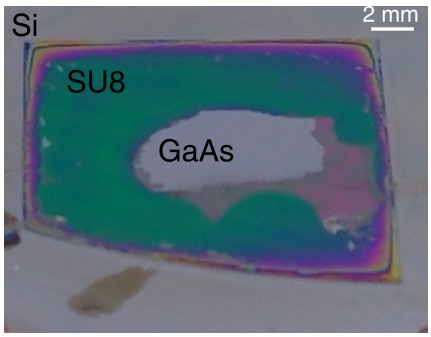



Figure 2.14: Lack of adhesion of SU-8 to highly doped InGaAs resulting in peeling of the device layers

Not only did this bonding process flow lead to the successful integration of gallium arsenide on silicon for terahertz Schottky diodes, but it has also been used for the integration of high performance III-V photodiodes on silicon, through a collaboration with Professor Beling's research group [52]. The next section will present the full diode process flow, which incorporates the new processes discussed in Sections 2.2 and 2.3.

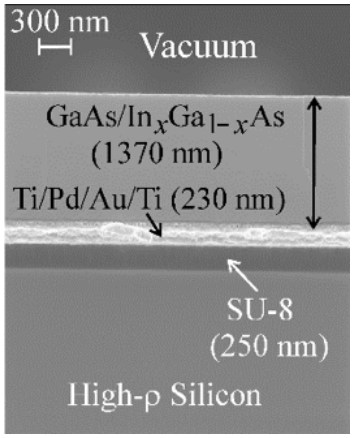



Figure 2.15: Side view cross-sectional SEM view of the gallium epitaxial device layers on silicon, after bonding and handle layer removal. The bonding interface is uniform and lacks voids.

## 2.4 New Process Flow

The new process flow for heterogeneously integrating GaAs Schottky diodes on silicon platforms is described in this section. The fabrication process starts with a semi-insulating gallium arsenide handle with device layers (also referred to as the III-V) epitaxially grown using MOCVD as described in Table 2.1. The ohmic metallization which consists of Ti/Pd/Au/Ti is deposited on the III-V surface using e-beam evaporation (Fig. 2.16(a)). The diode epitaxy is then bonded on a high resistivity silicon substrate, as described in Section 2.3 (Fig. 2.16(b)). Once bonded to the silicon substrate, the GaAs handle is removed in a nitric acid solution ($HNO_3$ : $H_2O_2$ : DI at 50 °C), followed by a slow citric acid etch ($C_6H_8O_7$ : $H_2O_2$ : DI at 50 °C). The nitric acid etch lasts 23 minutes, with a sample rotation and DI rinse every 5 minutes for the first 15 minutes. The citric acid etch lasts 30-45 minutes, until the AlGaAs etch stop layer is exposed. After a 5 minute over-etch, the sample is rinsed sequentially in 2 DI beakers, with very minimal air exposure. The sample is then immersed in hydrofluoric acid (HF) for 1 minute, which removes the AlGaAs layer, thus revealing the GaAs device layer field (Fig. 2.16(c) and Fig. 2.17). The sample is then transferred to a DI beaker for 10 minutes, followed by a methanol spin clean (with swab) to ensure that the top device layer is free of any contaminant.

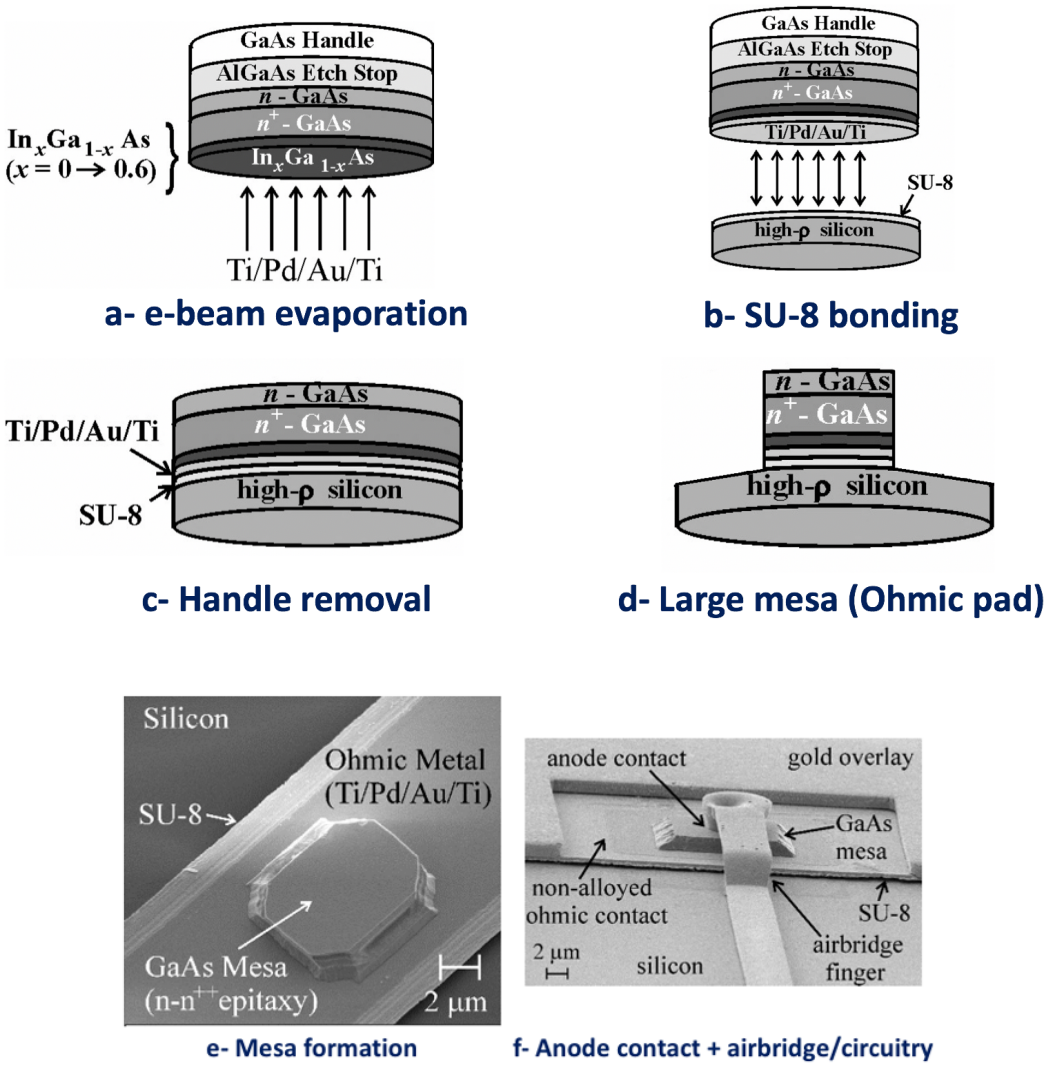



Figure 2.16: New fabrication process flow (a) e-beam evaporation of the ohmic metal stack, (b) bonding of the diode epitaxy on silicon using SU-8, (c) GaAs handle layer removal, (d) diode ohmic mesa area definition, (e) final device mesa definition, (f) SEM of the quasi-vertical diode profile (diameter = 3 µm) showing the device mesa, underlying ohmic contact, and anode contact airbridge.

The diode mesa areas (called large mesas) are defined photo-lithographically using AZ-4210 positive photo-resist spun at 4000 revolutions per minute (rpm), yielding a resist masking layer thickness of 2 µm. The large mesas are then formed by a sequence of selective etches that stop on the silicon surface (Fig. 2.16(d)). A wet etchant consisting of $H_2SO_4$ : $H_2O_2$ : DI (1:8:160) is used to

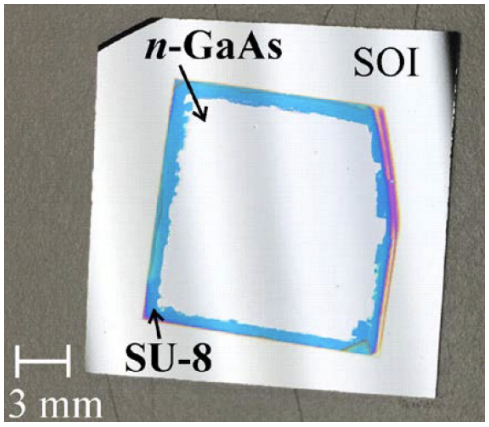



Figure 2.17: GaAs epitaxy bonded to SOI (thinned to ~ 1 μm).

remove GaAs in the areas between the final device mesas, at a rate of ∼350 nm/min. Following this, the exposed ohmic metal stack is removed using a combination of reactive ion etching (RIE), sputter etching, and wet chemical etching. The thin Ti layers are removed in a CHF3/SF6 RIE and the Pd with 10 seconds in transene gold etchant (TFA) wet etch. The TFA must be diluted in DI (2:1). The thick gold layer is removed with an Ar sputter etch, followed by a brief potassium iodide wet etch. Since Ar sputter etching is used to remove the thick gold layer, back sputtering of the gold atoms on the resist, and eventually on the large mesa is inevitable. However, this etch sequence is carefully designed to substantially minimize this effect. Once the ohmic metal layers have been removed, the exposed SU-8 adhesive layer is etched using a CF4 RIE. Table 2.3 summarizes the RIE dry etching parameters used in forming the large mesas (shown in Fig. 2.18), which include the type of gas, pressure, flow, RF power and etch times. All these etches are performed using a Semigroup RIE tool.

Table 2.3: RIE Dry Etch Parameters

| Etch | $SF_6$ (sccm) | $CHF_3$ (sccm) | $N_2$ (sccm) | Ar (sccm) | $CF_4$ (sccm) | Pressure (mTorr) | RF (W) | Time (min) |
|---|---|---|---|---|---|---|---|---|
| Ti | 20 | 5 | 0.6 (glow only) | - | - | 35 | 150 | 2 (for 20 nm) |
| Au | - | - | - | 70 | - | 30 | 120 | Inspection |
| SU-8 | - | - | - | - | 30 | 25 | 100 | ~15 |

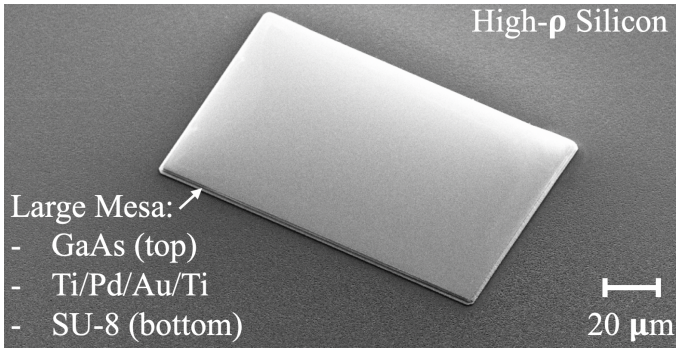



Figure 2.18: SEM image of a large mesa. The exposed layers are the GaAs device layers. The Ti/Pd/Au/Ti ohmic contact, which is bonded to silicon using SU-8, lies underneath the GaAs layers.

The final device mesa sits atop the ohmic metal pedestal (Fig. 2.16(e)). The mesa is defined by the same GaAs sulfuric acid based etch used during the large mesa step. Another SEM image showing two device mesas is shown in Fig. 2.19.

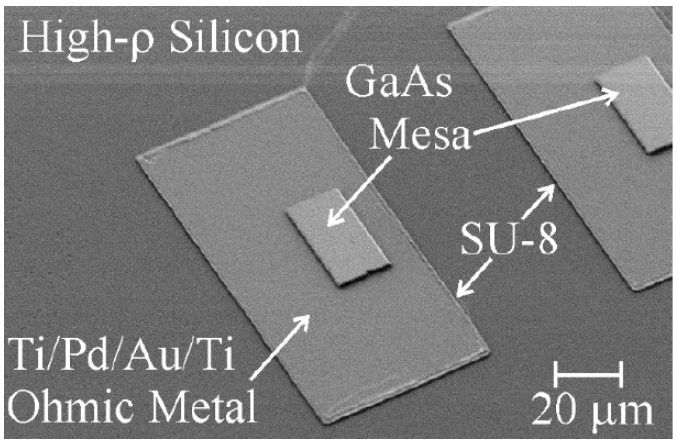



Figure 2.19: SEM image of two GaAs mesas on ohmic metal bonded to high-ρ silicon carrier.

The remaining steps utilize standard lithographic patterning to form the anode, airbridge finger contact, ohmic contact overlay metallization, and other circuit features on the silicon surface. Full details of these fabrication steps can be found in the process sheet located in Appendix A of this document. An SEM image of a completed quasi-vertical diode is shown in (Fig. 2.16(f) and Fig. 2.20). A coplanar waveguide (CPW) feed to the diode permits on-wafer

S-parameter characterization of the device.

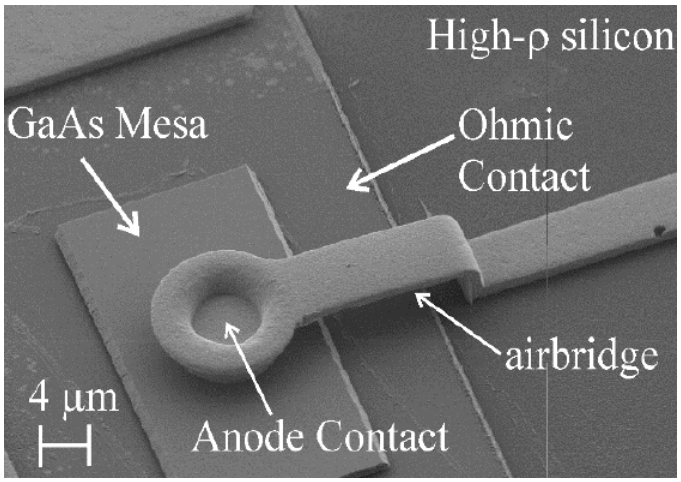



Figure 2.20: Anode and circuit metallization.

## 2.5 DC Characterization

Current-voltage (I-V) characterization of the quasi-vertical diodes fabricated with the new process is performed using a Keithley 236 source-measurement unit, and a four point probe technique. Fig. 2.21 shows a typical DC characteristic on a logarithmic scale for a 3 μm diameter quasi-vertical device. Fitting of the measured current-voltage characteristic provides estimates of the reverse saturation current, ideality factor, and series resistance provided in Table 2.4. The silicon substrate contributes a leakage resistance of $\sim$ 230 kΩ, which is noticeable in the dc current-voltage characteristic, but is usually inconsequential compared to the typical diode impedance at submillimeter-wave frequencies [24]. The series resistance and ideality factor extracted from the dc measurements are comparable to those achieved with previous quasi-vertical diodes that utilized annealed contacts [32]. The breakdown voltage is found to be $\sim$ 9.5 V from dc measurement under reverse bias. The RF on-wafer characterization of these diodes is presented in the next chapter.

Table 2.4: Extracted DC parameters for a 2.4 μm, 3 μm, and 4.0 μm diameter quasi-vertical diode. Conductance and saturation current normalized to the anode area are presented

| Diode diameter | Ideality factor | Resistance | Saturation current | Normalized conductance | Normalized saturation current |
|---|---|---|---|---|---|
| 2.4 μm | 1.26 | 7.00 Ω | 0.093 pA | 31.58 mS/μm$^2$ | 0.021 pA/μm$^2$ |
| 3.0 μm | 1.19 | 4.20 Ω | 0.100 pA | 33.7 mS/μm$^2$ | 0.014 pA/μm$^2$ |
| 4.0 μm | 1.23 | 2.92 Ω | 0.342 pA | 27.25 mS/μm$^2$ | 0.027 pA/μm$^2$ |

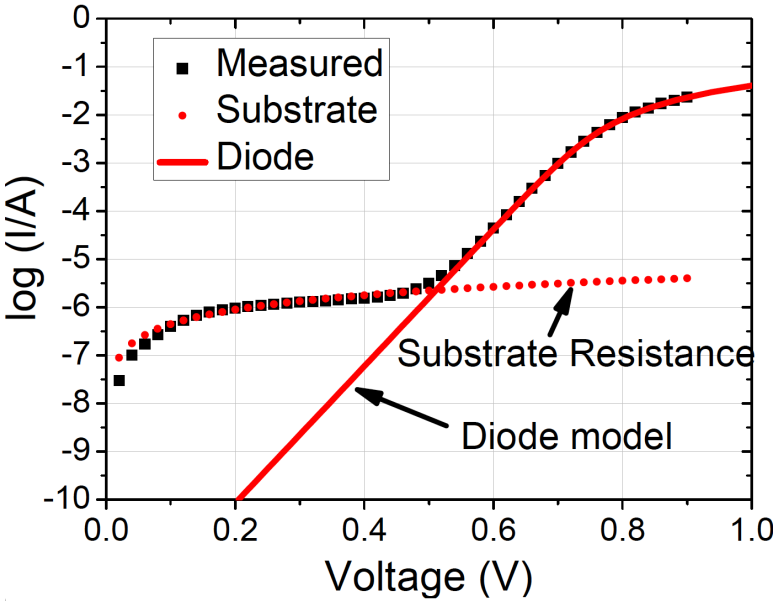



Figure 2.21: Measured current-voltage characteristic of a quasi-vertical diode with 3 μm diameter anode (dots), current-voltage characteristic of the contact pads without diode (dotted) and fitted current-voltage curve from the diode equation (solid).

## 2.6 Application: Integrated Quadrupler

To assess the performance of the newly developed fabrication process described in the previous sections of this chapter, a 40-160 GHz quadrupler was fabricated. This quadrupler incorporates 18 varactor diodes on a single chip.

This quadrupler utilizes the same design developed by Alijabbari, however the lithography masks were modified to reflect the changes in the process. We first give an overview of the circuit architecture and design, discussed in length in [1], [24]. We then go over the fabrication of the quadrupler based on the new process. Testing of the quadrupler will be presented in the next chapter.

### 2.6.1 Overview of Circuit Architecture and Design

The circuit architecture for the balanced quadrupler developed by Alijabbari is depicted in Fig. 2.22(a). The input feeds a quadrature hybrid coupler that, in turn, drives two balanced frequency doublers. The outputs of these doubler stages are of equal amplitude and out-of-phase. Consequently, they can directly drive an output balanced doubler stage, thus producing a frequency quadrupler. Provided the input stages of the multiplier are identical, no power is reflected at the input port. Mismatches associated with the input doublers result in power scattered to the isolation port of the hybrid, which acts as a power dump. The input of the quadrupler, as a result, is matched over the operating bandwidth of the hybrid coupler, resulting in a unilateral multiplier.

Varactor diodes used for this quadrupler implementation are based on the epitaxy described in Section 2.2. Harmonic balance analysis performed on 9.6 µm and 8 µm diameter varactors fabricated from this epitaxy, determined the optimum impedances to be 10+j70 Ω for the input at 40 GHz and 10+j50 Ω for the second stage input at 80 GHz.

A layout of the full quadrupler chip is shown in Fig. 2.22(b). The circuit incorporates three sets of balanced doublers comprising a total of 18 varactor diodes, and includes intermediate matching and filter networks, an output waveguide probe, and integrated beamleads for biasing. The chip is 7.5 mm from end-to-end and made of 15 µm thick, high-resistivity $>$ 10 kΩ-cm) silicon onto which the GaAs varactors have been integrated.

### 2.6.2 Fabrication Process

The process developed in prior sections was applied to fabricate the integrated quadrupler shown in Fig. 2.22(b). The process consists of two primary

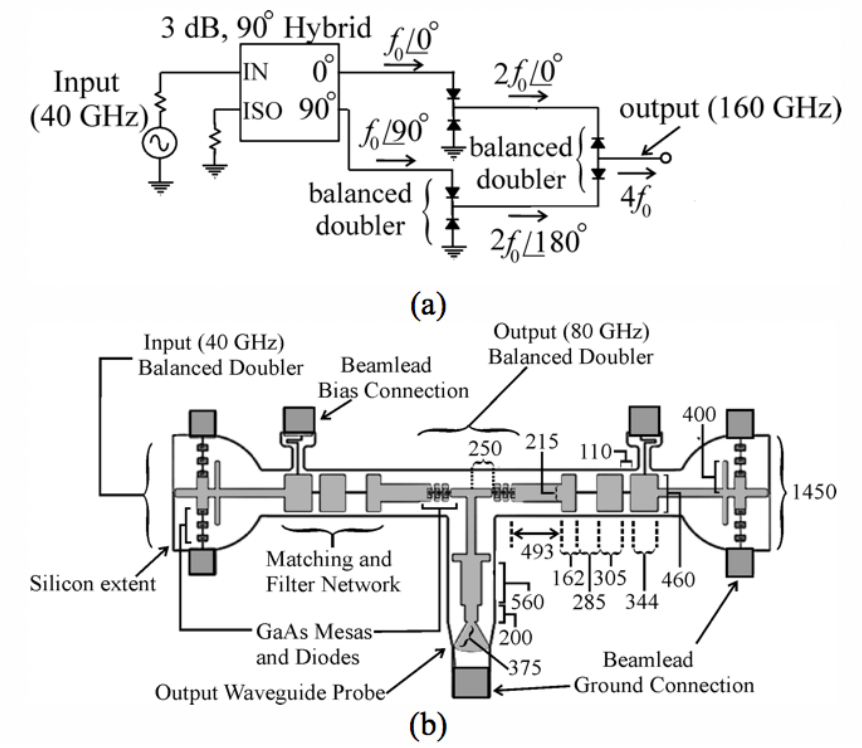



Figure 2.22: (a) Quadrupler circuit architecture and (b) layout of the integrated quadrupler chip. The quadrature hybrid is implemented off-chip (in waveguide) and all dimensions noted are in μm.

steps. First, a frontside process transfers the GaAs material onto a silicon-on-insulator (SOI) substrate, and defines the diodes and RF circuitry associated with the quadrupler (matching circuits, filters, etc.). Note that SOI is used instead of thick high resistivity silicon, in preparation for the second phase of the process, which is the backside process. The SOI wafer consists of a 15 μm high resistivity silicon device layer ($\rho > 10\ k\Omega.cm$), on top of a 1 μm thick silicon dioxide layer. Both layers are grown on a 450 μm low resistivity silicon handle layer. The 4″ SOI wafers are provided by Ultrasil Corporation. They are then laser cut into 1.3″ diameter circular wafers. The laser cutting job is performed by Questech Services Corp. Photoresist is spun and baked on the SOI wafers before laser cutting to protect the device layer.

The frontside process steps are summarized in Table 2.5. They are identical to the fabrication steps described in Section 2.4, except for the addition of step 6: the via lithography and etching. This step is necessary to define the

alignment markers, which will be used during backside processing to define the shape of the quadrupler chips using a silicon extents etch. The via lithography step is done using the MJB4 aligner. AZ 4330 positive photoresist is spun on the wafer at 2500 rpm to obtain a 4 μm thick resist. This step only defines two features on the wafer: a large circle at the center of the wafer, and extent etch alignment markers. These features are shown on the simplified mask CAD drawing (Fig. 2.23). The silicon extent etch step, which aligns to the markers defined during the via step, outlines the shape of the quadrupler chips as shown in Fig. 2.23.

Table 2.5: Summary of the frontside processing steps.

| **Step number** | **Step name** |
|---|---|
| 1 | Ohmic evaporation |
| 2 | Wafer bonding |
| 3 | GaAs handle removal |
| 4 | Large mesa lithography and etching |
| 5 | Small mesa lithography and formation |
| 6 | Via lithography and etching |
| 7 | Sacrificial resist lithography |
| 8 | Seed-layer sputtering |
| 9 | Plating lithography and plating |
| 10 | Seedlayer and photo-resist removal |

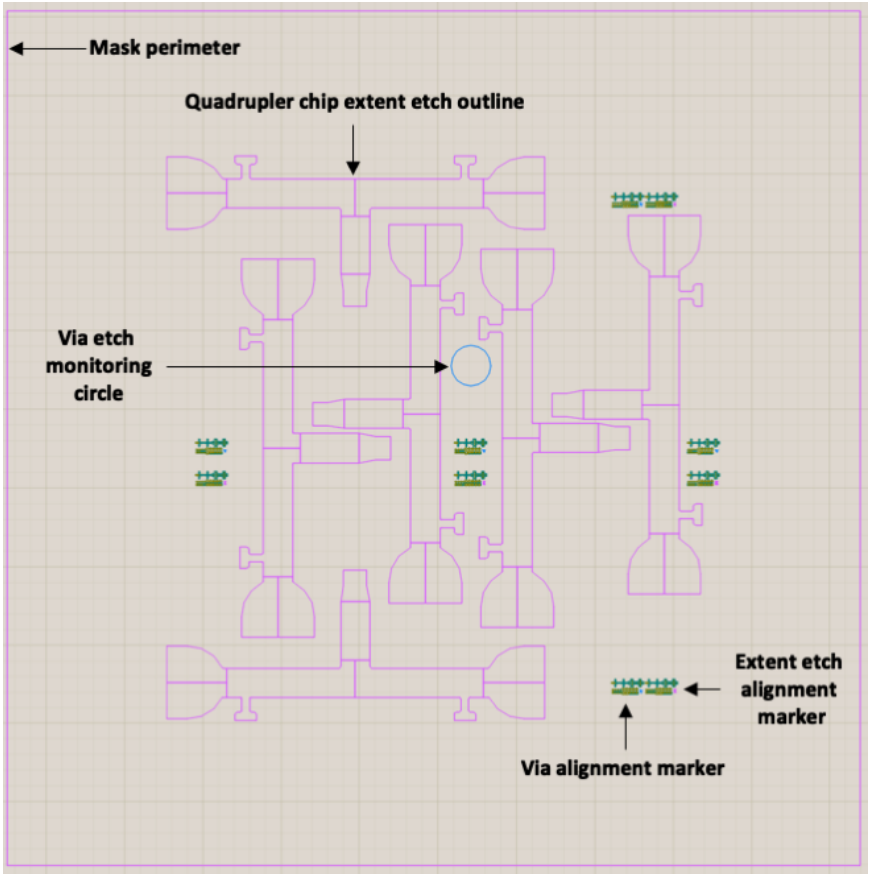



Figure 2.23: Simplified CAD drawing for the via and extent mask steps.

After the via exposure, the resist is baked on a hot plate at 110 °C for 10 mins to make it more resilient to the subsequent RIE/ICP etch. The sample is then mounted on a 4″ quartz carrier using L-grease, and loaded into an Oxford RIE/ICP dry etching tool. The Si dry etch recipe is summarized in Table 2.6. The endpoint detection laser beam is moved on top of the silicon area opened

Table 2.6: Si dry etch Oxford recipe.

| Etch | $C_4F_8$ (sccm) | $SF_6$ (sccm) | Pressure (mTorr) | He (Torr) | Temperature (°C) | RF (W) | ICP (W) | Time (min) |
|---|---|---|---|---|---|---|---|---|
| Si | 30 | 30 | 15 | 5 | 0 | 40 | 500 | End Point |

during the via lithography step (circle see Fig. 2.23). The reflectance of the beam is monitored during the etch to obtain an etch rate, and in order to stop the etch when all the device silicon has been removed (when the silicon dioxide

is reached). Fig 2.24 shows an example of the reflectance curves obtained using the endpoint detection features of the Oxford. The curves are standing waves which repeat every half wavelength in Si, which is 132 nm given the dielectric constant of silicon (11.67), and the wavelength of the laser which is 905 nm. The silicon etch rate varies between 500 nm/min and 1 µm/min. Running a long chamber clean often results in an improved etch rate.

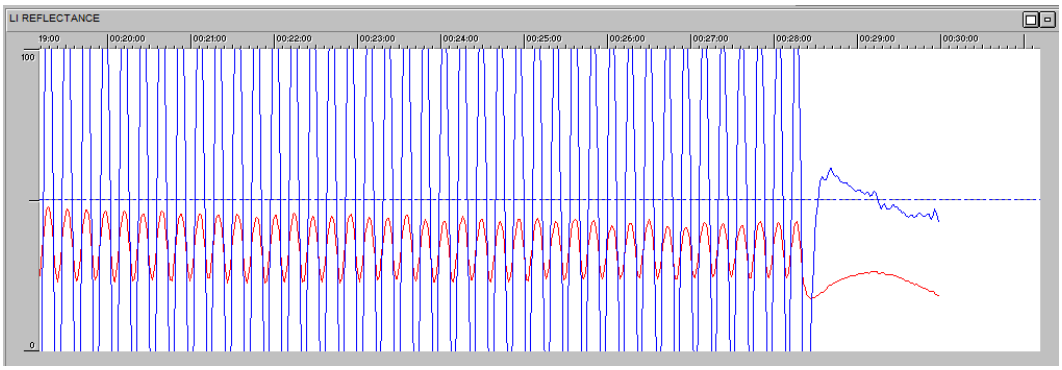



Figure 2.24: Screenshot showing the end point detection curves for the silicon etch step in the Oxford tool.

Fig. 2.25 shows a scanning electron microscope image of the extent etch alignment markers formed on the silicon surface. The RIE/ICP etch results in vertical side walls, and little shape distortion. The via etch step is followed by steps 7-10 in Table 2.5. For the quadrupler implemented in this work, the

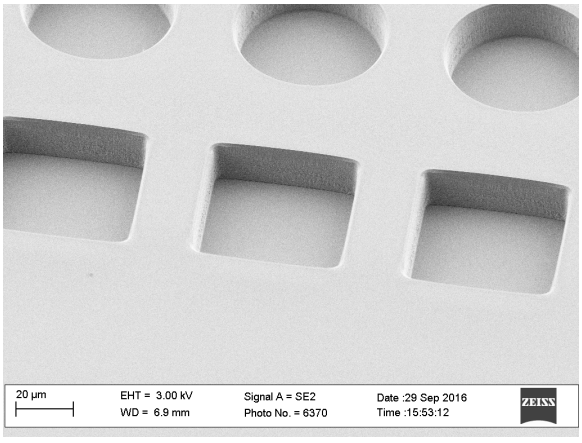



Figure 2.25: Scanning electron micrograph of the extent etch alignment markers, defined during the via etch step.

diameters of the diodes formed during step 7 are 9.6 µm for the input stage doublers and 8 µm for the output stage doubler.

Once fabrication of the diodes is completed (frontside), the silicon carrier to which they are bonded is micromachined to form an integrated chip with geometry tailored to fit the waveguide housing to which it will be affixed. Initially, the surface of the wafer with diode circuitry is attached to a sacrificial carrier using wafer-bond adhesive. Following this, the thick "handle" silicon layer of the SOI is removed through a combination of lapping and plasma etching. The buried oxide is then removed with a buffered oxide etch. At this point, the extent etch alignment markers formed during the via etch step are now visible and can be used to perform the final lithography step. In the final step, backside lithography defines the chip geometry (Fig. 2.23), including integrated beamleads, and a silicon etch (Table 2.6) forms the final 15 µm thick chips. Individual chips are then released by removing the sacrificial carrier. The details of the backside process for the quadrupler circuit are included as an appendix at the end of this document (Appendix B). Fig. 2.26 shows an image of the backside lithography prior to release from the sacrificial carrier wafer. An SEM image of the completed quadrupler chips is shown in Fig. 2.27(a). Fig. 2.27(b) shows a photograph of the chip mounted to its housing. Note that the 40 GHz input quadrature hybrid is implemented in waveguide, but is not shown in Fig. 2.27(b) due to its relatively large size. The RF characterization of the quadrupler is summarized in Chapter 3.

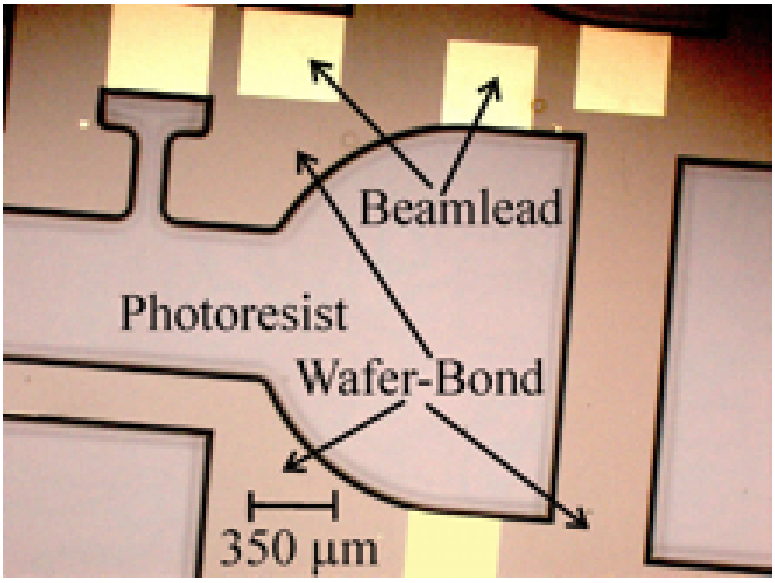



Figure 2.26: Backside lithography used to define the chip geometry.

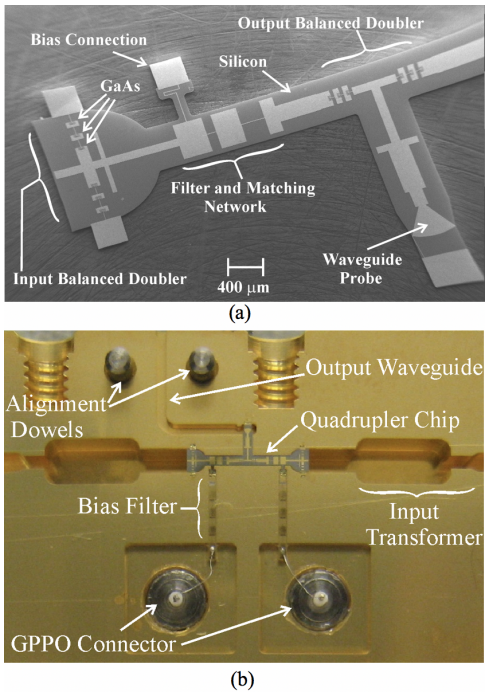



Figure 2.27: (a) SEM image of the completed quadrupler chip. (b) The quadrupler chip mounted to its waveguide housing. The quadrature hybrid is not shown.

# Chapter 3

# RF Characterization of Quasi-Vertical Diodes

The previous chapter introduced a revised process for fabricating quasi-vertical GaAs diodes integrated on silicon. Using that process, diodes integrated on thick silicon substrates were fabricated to characterize the electrical performance of the diodes using on-wafer measurements. In addition, the fabrication of a 40-160 GHz quadrupler, based on prior art, was outlined, which adds a SOI backside fabrication step. In this chapter, we start by presenting the on-wafer RF characterization of the quasi-vertical diodes (published in *IEEE Electron Device Letters* (2017)). The equivalent circuit parameters are compared with previous diodes (Section 3.1) which were fabricated using the prior implementation. In Section 3.1, the parasitic circuit elements associated with the diode geometry are obtained using finite-element simulations. Section 3.2 revisits this approach, by introducing a new method of extracting the diode parasitics that relies on measurements of passive short and open circuited diodes, which together capture the parasitic environment associated with the diode. The work presented in Section 3.2 is based on a paper which was submitted to *IEEE MWCL 2019 (*publication #1 under List of Publications). Finally, Section 3.3 presents the RF characterization of the quadrupler circuit, which is based on work presented at *IMS 2018* (publication #3 under List of Publications).

## 3.1 Scattering-Parameter Measurement

In this section, the RF characterization of the diodes described in the previous chapter (Section 2.4) is presented. The measurements are performed in the WR-2.2 (325—500 GHz) band using an Agilent PNAX vector network analyzer and Cascade Microtech PA200 probe station equipped with WM-570 frequency extenders from Virginia Diodes, Inc. and WR-2.2 on-wafer probes manufactured by Dominion MicroProbes, Inc [53], [54]. An on-wafer calibration is performed using standards fabricated on the same substrate as the diodes.

Fig. 3.1 shows a Smith chart plot of the measured reflection coefficient data over the full WR-2.2 (325-500 GHz) band for a 3 μm diameter QVD fabricated using the new process, for various bias levels (0.6 V, 0 V, -2 V, -4 V, -6 V).

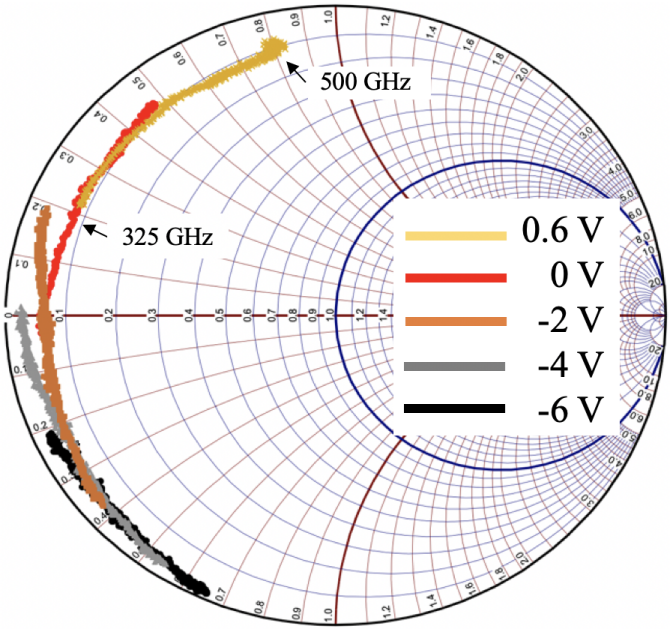



Figure 3.1: WR-2.2 on wafer measurement results: S11 vs voltage from 325 GHz to 500 GHz.

The measured reflection coefficient data taken at midband (425 GHz) are plotted as a function of bias voltage in Fig. 3.2, along with the data from an old process ohmic contact diode (also 3 μm in diameter) measured by Alijabbari [32]. The difference in sweep range versus bias is due to a difference in the measurement reference plane for this work compared to [32].

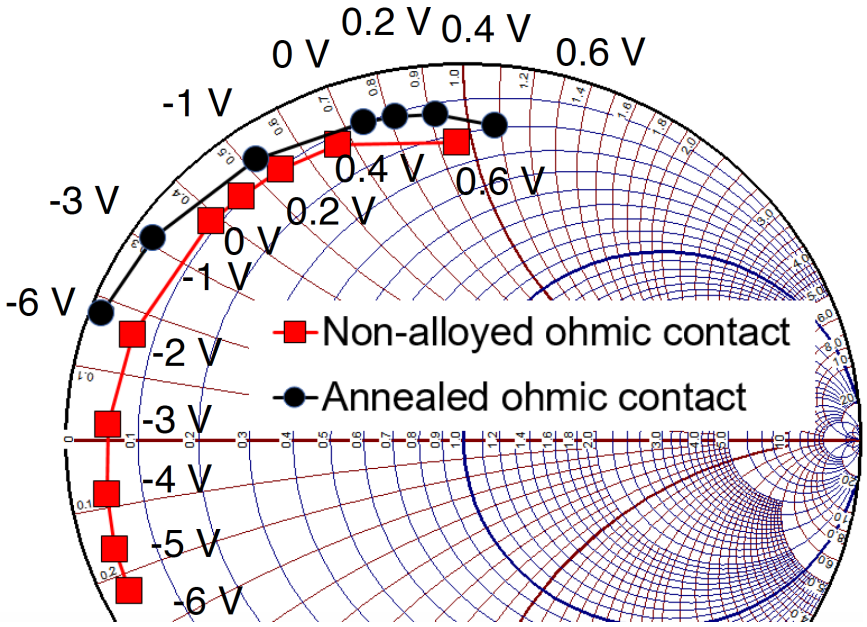



Figure 3.2: WR-2.2 on wafer measurement results: S11 vs voltage at 425 GHz.

In order to extract the diode model's intrinsic parameters (junction capacitance and series resistance), the data shown in Fig. 3.2 is fitted to an equivalent circuit model. The model used in this study (shown in Fig. 3.3) is described in [32], and consists of a coplanar feed line, a parasitic inductor $L_f$ associated with the finger, and a parasitic capacitance $C_{fp}$ between the finger and the ohmic. A more complete model will be described in the next section. The parasitic values are found to be: $L_f = 11.55$ pH and $C_{fp} = 3.59$ fF, by simulating the device structure in Ansoft's High Frequency Structure Simulator (HFSS) and fitting to the equivalent circuit model of Fig. 3.3.

The diode junction capacitance and series resistance, obtained from the S-parameter data, are shown in Fig. 3.4 and Fig. 3.5. The extracted junction capacitance for the annealed and un-annealed diodes are, as anticipated the same. The normalized zero bias junction capacitance to anode area is 1.78 fF/$\mu m^2$. The series resistance extracted from these measurements indicate approximately 1 $\Omega$ lower value than that obtained with annealed ohmic contact diodes fabricated using the process described in [32]. The normalized zero bias series conductance to anode area is 38.4 mS/$\mu m^2$.

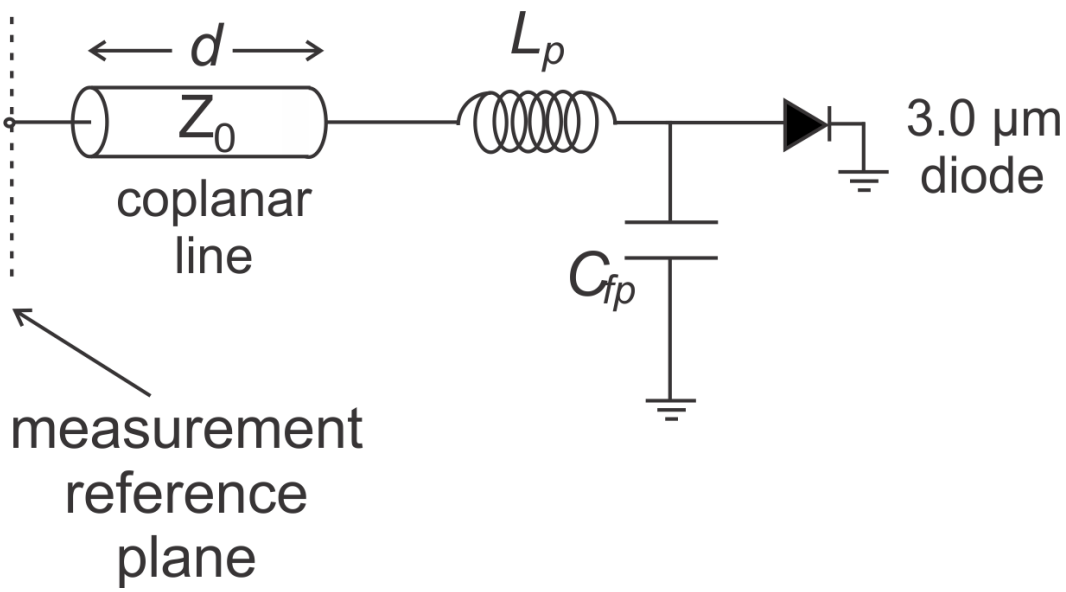



Figure 3.3: Equivalent circuit model used to de-embed the diode junction capacitance and series resistance from the measured S-parameter data.

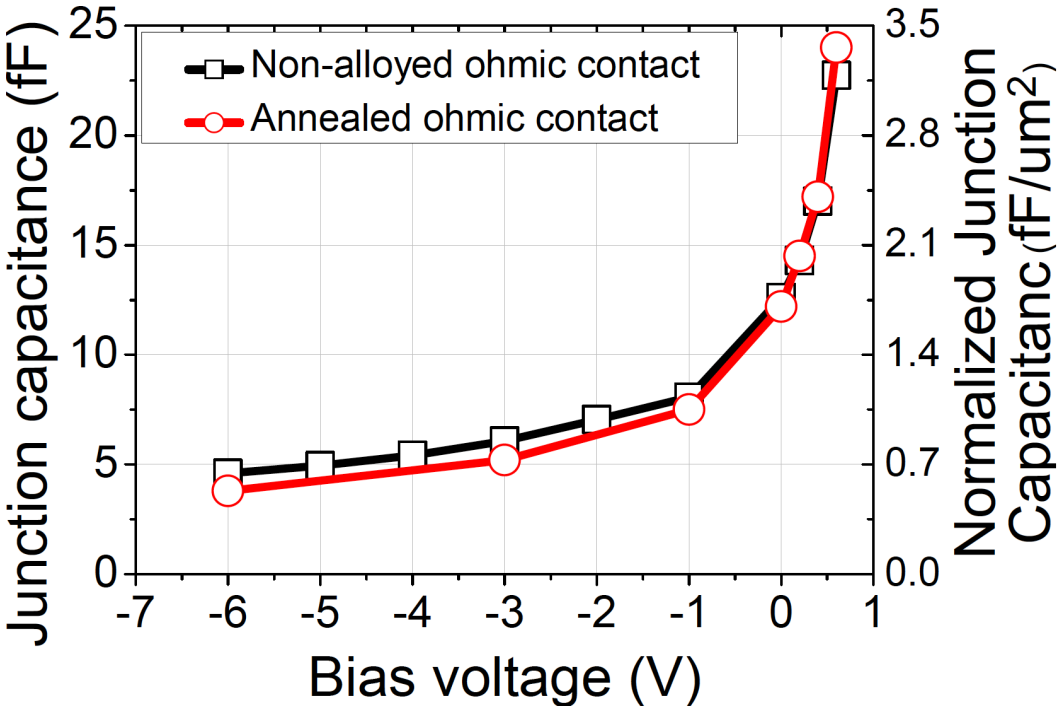



Figure 3.4: WR-2.2 on wafer measurement results: Extracted junction capacitance.

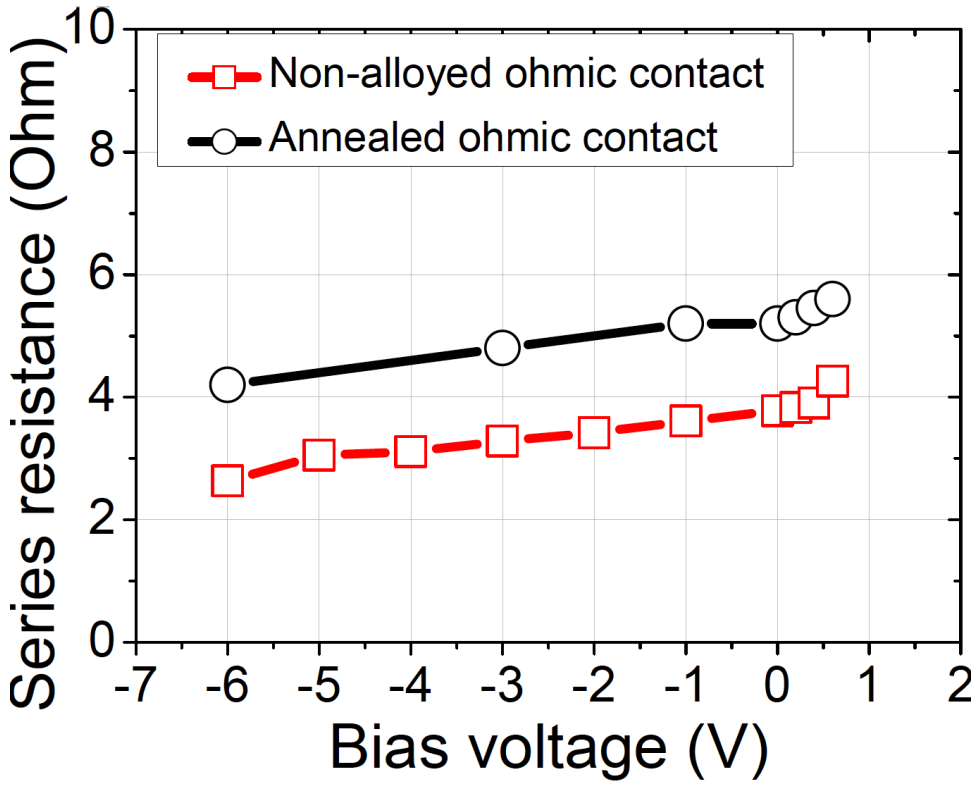



Figure 3.5: WR-2.2 on wafer measurement results: Extracted series resistance.

In summary, the diodes fabricated using the new process exhibit excellent RF characteristics, which makes them suitable for use in various submillimeter-wave circuits such as quadruplers (Section 3.3) and phase shifters (Chapter 5).

## 3.2 Extraction of Diode Parasitic Elements

A thorough understanding of the parasitic environment associated with the diode's geometric features is necessary to achieving state-of-the-art performance at frequencies greater than 100 GHz. The device parasitic environment is generally described by an equivalent circuit representation, which is suitable for use with software design tools. Established approaches for characterizing the electromagnetic fields near the diode and its associated parasitics include simulation of the structure of the device with numerical field solvers (which was used in Section 3.1), scaling the parameters of devices measured at lower frequencies [55], or inferring from measurements of global system parameters of

the overall circuit (such as the efficiency of diode-based frequency multipliers).

With the development of submillimeter-wave wafer probes, extraction of equivalent circuit models for diodes based on calibrated scattering parameter measurements is now possible in submillimeter-wave frequencies. In [56], the parasitics of planar diodes are extracted using a combination of low-frequency capacitance measurements, simulations, and S-parameter measurements up to 110 GHz. In [32], quasi-vertical diodes were measured at submillimeter-wave frequencies, and a parasitic model was adopted based on electromagnetic simulations. In this section, the parasitic environment associated with the quasi-vertical Schottky diode architecture is characterized directly, for the first time, at 325—500 GHz using on-wafer probe scattering parameter measurements of passive diode structures fabricated on the same wafer as the diodes.

### 3.2.1 Diode Geometry

The diode studied in this section is shown in Fig. 3.5(a). Fig. 3.5(b) shows the diode geometry overlaid on the circuit model commonly used to represent the parasitic environment near the anode [57]. The parasitic elements include a pad-to-pad anode capacitance ($C_p$), finger inductance and resistance ($L_f$ and $R_f$), a finger-to-mesa capacitance ($C_f$), and a frequency-dependent series resistance ($R_s$) representing conduction through the doped mesa epilayers. The junction of the device is modeled with the diode's current-voltage and capacitance-voltage characteristic [32].

The diode in Fig. 3.6(a) is integrated into a 44 Ω coplanar transmission line with center conductor width 4.2 μm, gap width 4 μm, and length of 94 μm. The diode has anode diameter of 3 μm, airbridge finger length of 30 μm, and finger width 4 μm. Coplanar contact pads allow the device to be measured using wafer probes with pitch (center conductor-to-ground spacing) of 25 μm.

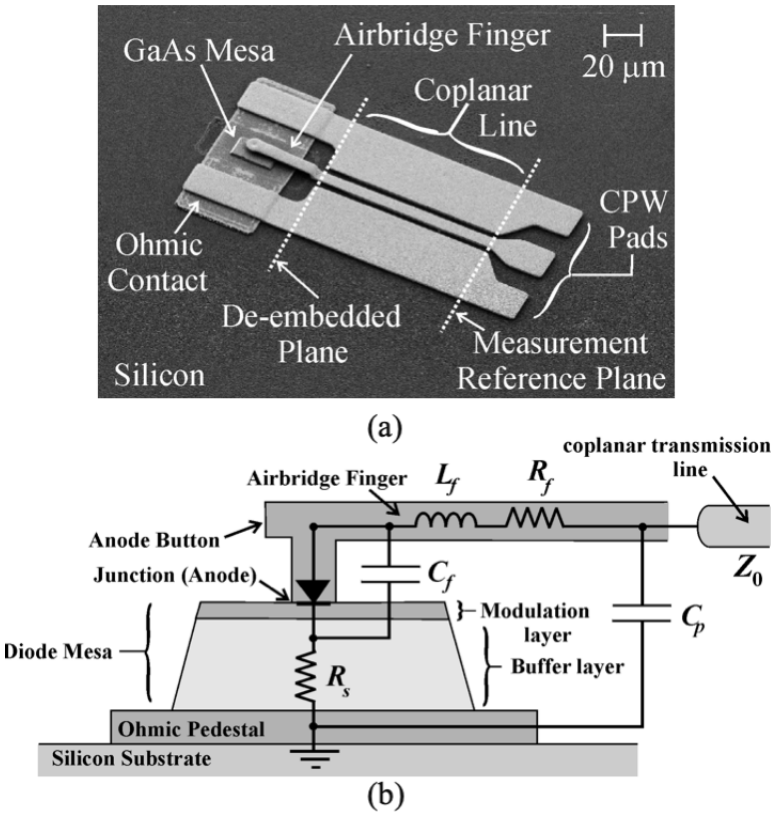



Figure 3.6: (a) Scanning electron micrograph of a quasi-vertical Schottky diode with coplanar feed for S-parameter measurement. (b) Diagram showing the diode geometry superimposed on the conventional circuit model used to represent the device parasitics.

### 3.2.2 Calibration

To characterize the parasitic environment of the diode, an on-wafer two-port calibration is performed over the WR-2.2 (325—500 GHz) band using two sets (one for each port) of open and short-circuited coplanar transmission line standards, a thru line, and 90° and 270° delayed lines (electrical length offsets with respect to the thru line). The standards are fabricated on the same substrate as the test devices and have lengths of 64 μm (open and short), 128 μm (thru), 196 μm (90° delayed line), and 332 μm (270° delayed line). As indicated in Fig. 3.6(a), the measurement reference plane is set at the end of the wafer probe contact pads. Calibration and error-correction are implemented using the WinCal XE software package and Fig. 3.7 shows the resulting error-

corrected measurement of the coplanar calibration standards. From WinCal, the complex propagation constant of the coplanar lines is found, which subsequently is used to de-embed the scattering parameters from the measurement reference plane to the diode end of the transmission line (indicated as the de-embedded reference plane in Fig. 3.6(a)).

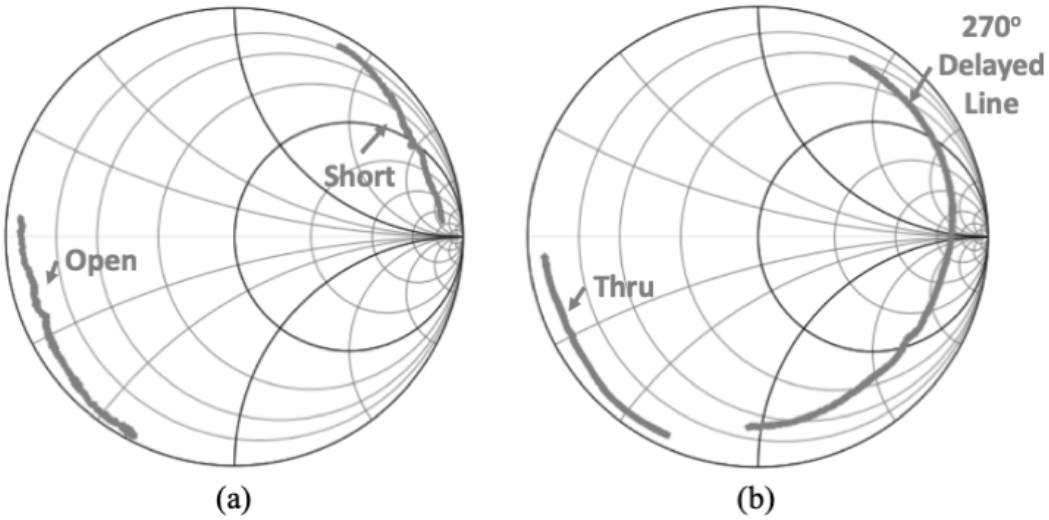



Figure 3.7: Measured S-parameters of the on-wafer calibration standards from 325 to 500 GHz. (a) reflection coefficient of the reflect standards (open and short) (b) transmission coefficient of the through and line.

### 3.2.3 Diode Test Structures

A set of "passive" structures with identical geometry as the diodes are fabricated on the substrate along with the CPW calibration standards. These passive structures, shown in Fig. 3.8, include the coplanar feed line, airbridge finger, ohmic contact pedestal, and anode contact "button," but terminate in either a short-circuit or open-circuit instead of a Schottky contact. The short-circuited diode structure is formed by eliminating the mesa formation step of the fabrication process, resulting in the anode button directly contacting the ohmic metal pedestal (Fig. 3.8(a)). To form the open-circuited structure, the diode mesa is coated with photoresist during formation of the airbridge finger and anode button. After metal plating of these features, the resist is stripped, leaving a free-standing airbridge suspended over the GaAs mesa (Fig. 3.8(b)).

The "passive" diode structures shown in Fig. 3.8 permit the parasitic elements associated with the diode geometry to be characterized independently of the Schottky junction through fitting of the parasitic equivalent circuit model to the de-embedded S-parameters.

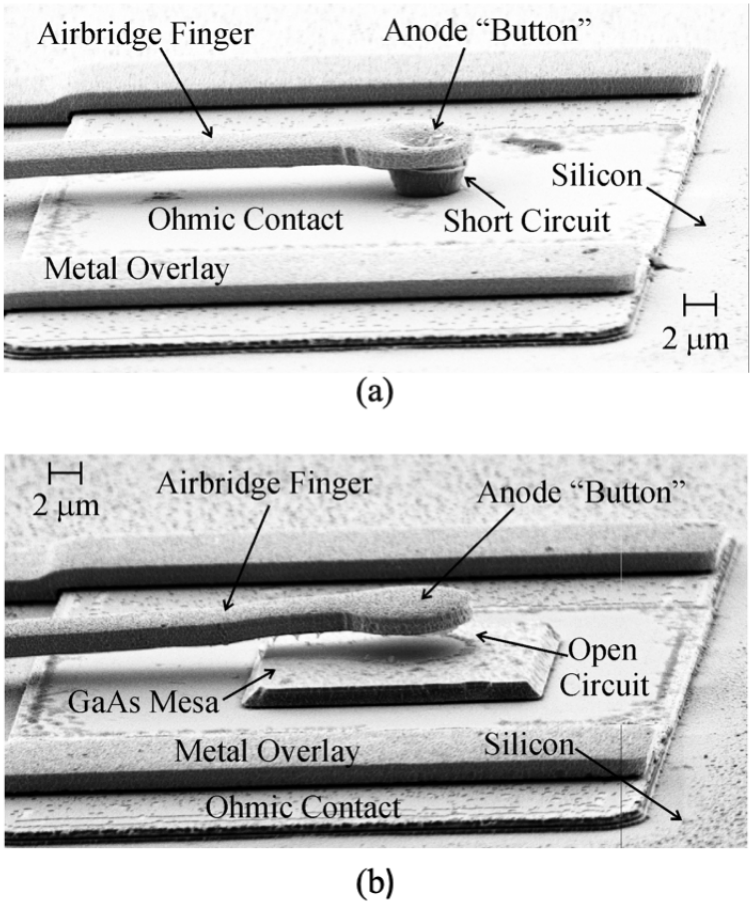



Figure 3.8: Scanning electron micrograph images of passive structures used to characterize the diode's parasitic environment. (a) Short-circuited termination with finger directly contacting the ohmic pedestal, and (b) open-circuited diode structure with anode "button" suspended over the mesa and ohmic contact.

### 3.2.4 Measurement and Analysis

Fig. 3.9 shows the error-corrected reflection coefficients obtained from measurement of the short and open-circuited diode structures of Fig. 3.8. Data is provided for both the measurement reference plane and the de-embedded

plane indicated in Fig. 3.6(a). The de-embedded reflection coefficient data shown in Fig. 3.9 is obtained using the frequency-dependent complex propagation constant found from WinCal XE for the coplanar transmission line standards to unwrap the phase and compensate for the attenuation of the 94 μm long coplanar feed line of the diode structures.

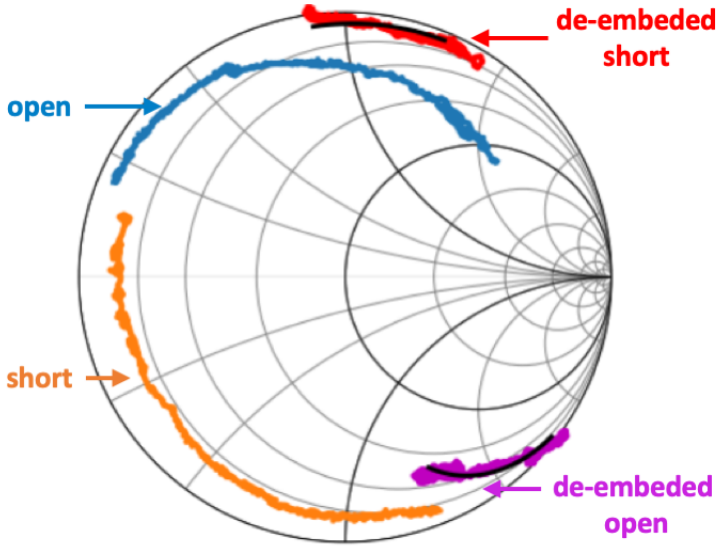



Figure 3.9: Measured reflection coefficients of the short-circuited and open-circuited diode structures. Data is presented at both the measurement reference plane and the de-embedded plane shown in Fig. 3.5(a). The response of the circuit models are shown for comparison (as solid lines).

The response of the short-circuited structure exhibits an inductance and largely follows a constant resistance contour with frequency, as anticipated from its equivalent circuit model (shown in Fig. 3.10(a)). The resistance for the short-circuited case ($R_{short}$) is not frequency dependent and is a sum of the resistances from the finger and ohmic metal. Similarly, the reflection coefficient of the open-circuited diode structure is capacitive with series resistive component $R_{open}$ that increases with frequency. Again, this measured characteristic can be represented with the conventional equivalent circuit of Fig. 3.10(b) in which the diode junction is open-circuited and the finger capacitance couples directly to conduction through the device mesa. Tang and others [57] have described in detail the effective increase of diode series resistance with frequency, which is due to a combination of the skin effect, induced eddy currents, and

proximity effects that become important above 200 GHz for typical Schottky diode geometries. The series resistance frequency dependence is given from [57] as:

$$R_{open}(f) = R_{DC}(1 + 0.1 * (\frac{f}{f_1})^2 + 0.1 * (\frac{f}{f_2})^4), \tag{3.1}$$

where $R_{DC}$ represents the DC resistance, and $f_1$and $f_2$ fitting parameters [57].

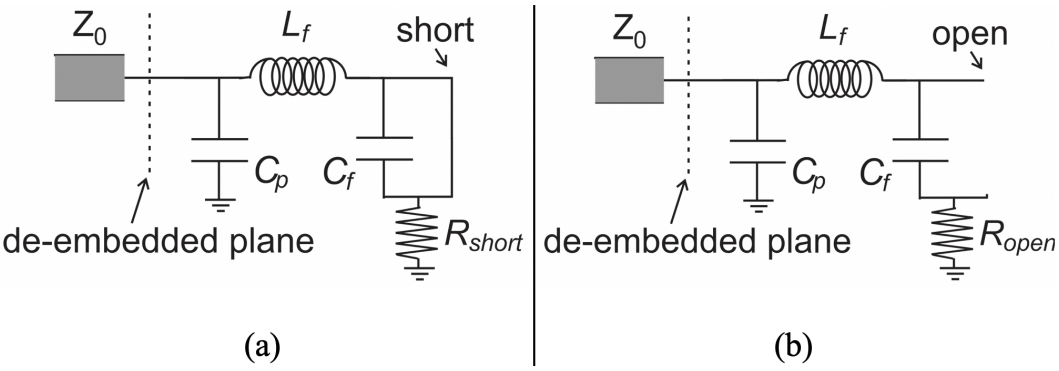



Figure 3.10: Equivalent circuit representations of (a) the short-circuited and (b) open-circuited diode structures shown in Fig. 3.6.

Table 3.1 provides the fitted parasitic circuit parameters based on the measured S-parameters of Fig. 3.9 and the equivalent circuit models of Fig. 3.10. The fitted parameters are extracted in four steps. First, the phase of $S_{11}$ for the short-circuited parasitic measurement is fitted to the circuit model in Fig. 3.10(a) to obtain the pad-to-pad anode capacitance and finger inductance with values: $C_p$ = 2.33 fF and $L_f$ = 15.05 pH. Next, the magnitude of $S_{11}$ for the short parasitic measurement is fitted to the same model (Fig. 3.10(a)) to obtain $R_{short}$ = 1.03 Ω. After that, the phase of $S_{11}$ for the open structure is used to find the finger capacitance based on the model in Fig. 3.10(b)). The extracted value of $C_f$ is 1.68 fF. Finally, the magnitude of $S_{11}$ for the open structure provides us with $R_{DC}$, $f_1$, and $f_2$ (see Table 3.1). The uncertainties associated with the least-squares fitting are summarized in Table 3.2. These fitting errors are calculated by evaluating the residual errors for each frequency point. The magnitudes of these errors are then squared, and the squared magnitudes are then averaged over frequency.

Table 3.1: Summary of the parasitic element values with uncertainties.

| $C_p$ (fF) | $L_f$ (pH) | $R_{short}$ ($\Omega$) | $C_f$ (fF) | $R_{DC}$ ($\Omega$) | $f_1$, $f_2$ (GHz) |
|---|---|---|---|---|---|
| 2.33 ($\pm$0.14) | 15.05 ($\pm$0.47) | 1.03 ($\pm$0.06) | 1.68 ($\pm$0.13) | 0.1 ($\pm$0.01) | 368, 50 ($\pm$81, 2) |

Table 3.2: Reflection coefficient magnitude and phase errors associated with least-squares fitting.

| Phase (short structure) | Magnitude (short structure) | Phase (open structure) | Magnitude (open structure) |
|---|---|---|---|
| 0.34° | 0.97 dB | 0.46° | 1.42 dB |

Fig. 3.11 shows the phase of the de-embedded S-parameters compared to those of the equivalent circuit models with fitted parameters. Errors associated with alignment and positioning of the coplanar probes onto the contact pads result in measurement uncertainty. Using the extracted phase and attenuation constants from WinCal XE, a typical probe skating distance of $\pm$3 μm, for instance, will produce a phase uncertainty of $\pm$3.5° at midband (420 GHz). This uncertainty propagates into estimations of the value for the parasitic circuit elements associated with the diode geometry. The uncertainties in these estimates, based on a $\pm$3 μm skating error of the probes, are indicated in parenthesis in Table 3.1 and using maximum and minimum uncertainty bounds on the S-parameters shown in Fig. 3.11.

The reactive parasitic elements are also found by simulating the passive structures (shown in Fig. 3.8) using the finite-element software package HFSS. The obtained values are: $C_p$ = 0.82 fF, $L_f$ = 19.50 pH, and $C_f$ = 2.05 fF, which are in reasonable agreement with the values presented in Table 3.1. The parasitic elements values are also comparable to those reported in [57]. The resistive parasitic elements are more difficult to compare, since they depend heavily on the intrinsic diode epilayer, anode area, and processing conditions. However, note that the extracted DC resistance (0.1 $\Omega$) is much lower than predicted from 4 point I-V measurements of 3 μm diameter quasi-vertical diodes reported in Section 2.5 (4.2 $\Omega$). This is expected since the fields from the anode button couple directly to the full mesa in the open passive case, while for a

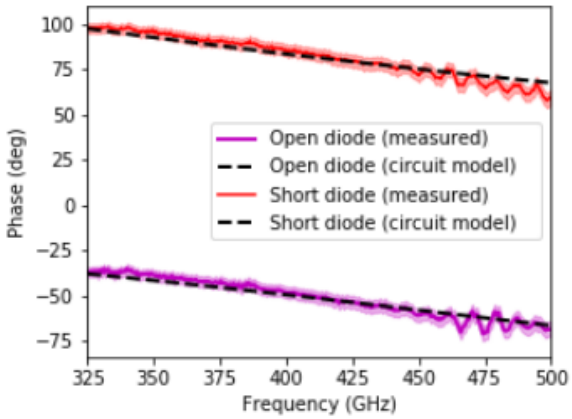



Figure 3.11: Phase of the de-embedded S-parameters for the short-circuited (top) and open (bottom) diode structures, with minimum and maximum confidence bounds that quantify the uncertainty associated with skating of the wafer probe. The response of the circuit models are shown as dashed lines, for comparison.

Schottky contact the coupling is through the area defined by the anode contact (smaller than the area of the mesa). Also, note that the extracted value of $C_f$ is about 3% larger than that of the actual diode, since the open circuited structure adds a capacitance contribution in air between the button and the mesa, which was estimated using a parallel plate approximation.

### 3.2.5 Summary

In this section, we have presented the first direct measurement and extraction of parasitic parameters for quasi-vertical Schottky diodes based on submillimeter-wave on-wafer measurements of passive structures. The values of the parasitic elements obtained using on-wafer measurements are consistent with those found from simulation and published in the literature for diodes with comparable geometry. The method presented here is simple because it only requires the measurement of two passive structures fabricated on the same wafer as the diodes, and versatile because the losses associated with the substrate and metal conductors (which can be challenging to account for in simulation) can be easily de-embedded from the measured scattering parameter data. Finally, the new model is more complete than that presented in Section 3.1, because each parasitic circuit component corresponds to an element in the diode ge-

ometry.

## 3.3 Characterization of Integrated Quad

The work presented in this section follows that of Alijabbari and is done as a final confirmation that the revised process yields comparable results. The quadrupler measurement setup is shown in Fig. 3.12. The characterization is done using an Agilent E8257D frequency synthesizer followed by a Spacek Labs SP408-35-26 amplifier with 35 dB gain and 36 to 43 GHz bandwidth. An Erickson PM5 power meter is used to measure the multiplier output power in the WR-5.1 band. A WR-22 waveguide switch is used to monitor the available power as well as direct the input signal to the multiplier block. An Erickson PM5 power meter is used to measure the multiplier output power in the WR-5.1 band and a spectrum analyzer placed at the quadrupler isolation port monitors power scattered from the input-stage doublers, permitting the return loss of the multiplier to be measured during operation [24]. Measurement of the quadrupler was done at the University of Virginia and repeated at Virginia Diodes, Inc. to ensure consistent results were obtained.

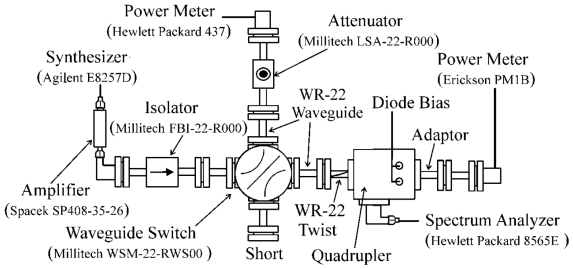



Figure 3.12: Diagram of the quadrupler measurement setup [1].

Fig. 3.13 shows the input-output power relation for an input frequency of 40 GHz and diode (reverse) bias of 12 V. Peak efficiency of 25.5% occurs for an input of 280 mW. Beyond 280 mW, the multiplier begins saturating and the efficiency drops. The output power at peak efficiency for this implementation of the quadrupler is 71.4 mW, which is identical to that obtained with the previous implementation based on the old process ohmic contact diode, which was 70 mW. The efficiency is 3.5 % lower (25.5% vs 29%), which could be

attributed to a slightly larger series resistance for the diodes based on the new implementation (recall in Chapter 2, we found that the contact resistance for the new process was 60% larger than that obtained with the previous process).

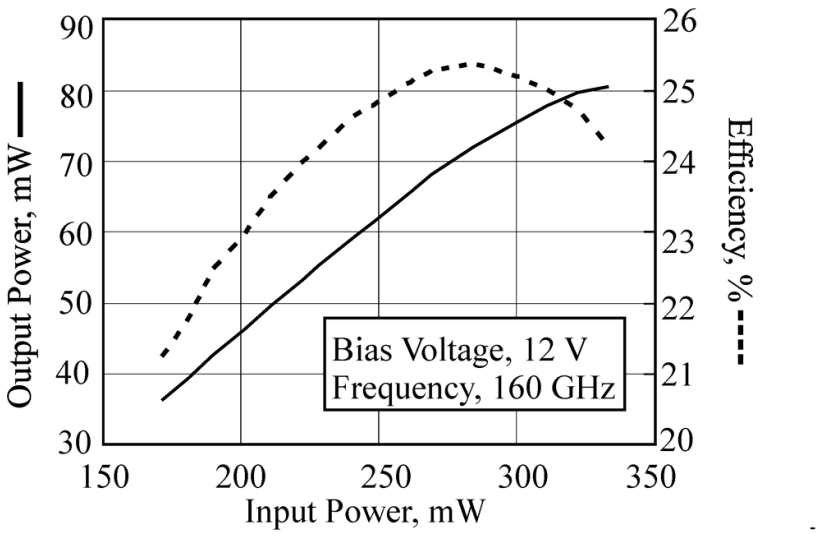



Figure 3.13: Quadrupler output power and efficiency vs. input power.

The output power over the full 36—43 GHz operating band-width of the Spacek power amplifier is shown in fig. 3.14, for an input power level of 285 mW and bias of 12 V. The power measured at the isolation port of the hybrid coupler, normalized to the available power from the input power amplifier, is also shown and provides a measure of the quality of the input match to the quadrupler. The peak power under these operating condition is 72 mW and the output power is greater than 20 mW over an output bandwidth of 146—176 GHz (16% fractional bandwidth).

Finally, output power of the quadrupler as a function of input power near the design frequency (160 GHz) is shown in fig. 3.15. The saturation characteristic of the multiplier is evident and a maximum output power of 100 mW (20 dBm) was measured at 159 GHz. This output power corresponds to an input power of 650 mW and overall quadrupler efficiency of 15%. The decrease in efficiency is a known phenomenon and is due to a combination of velocity saturation effects [58] and diode self-heating [59].

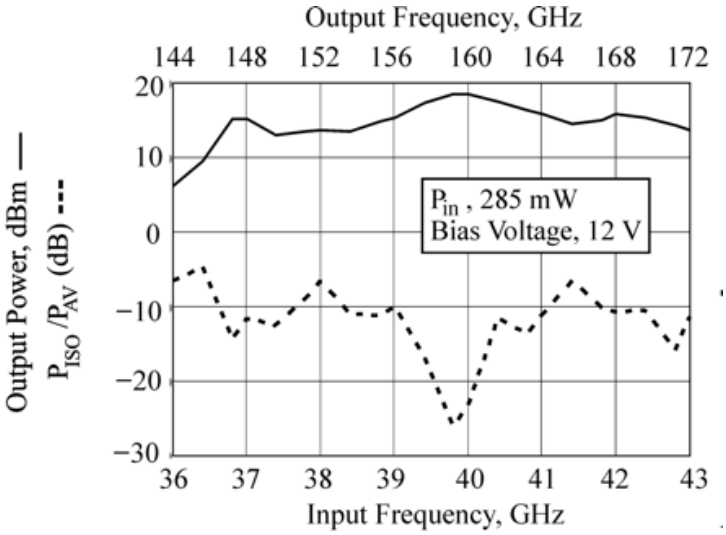



Figure 3.14: Output power and power measured at the isolation port, normalized to available power. vs. frequency.

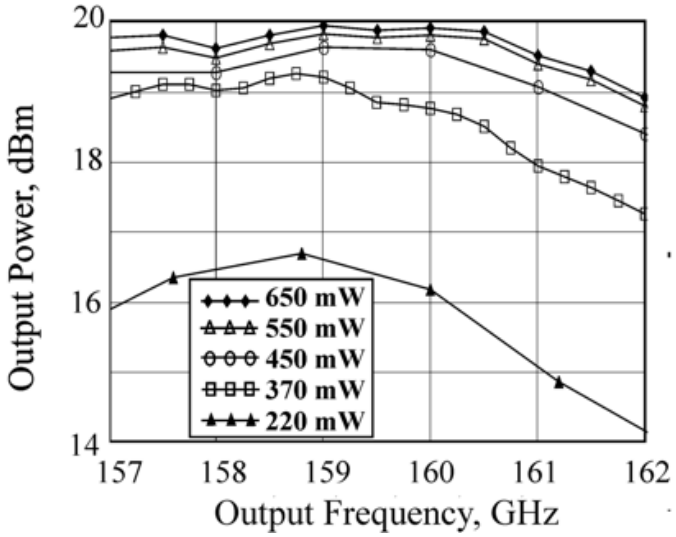



Figure 3.15: Power output vs frequency for different input power levels.

In summary, this subsection has presented a new implementation of the 40-160 GHz integrated frequency quadrupler developed in [1]. The modified fabrication process (described in Chapter 2) that eliminates high-temperature thermal processes and utilizes SU-8 as an adhesive for epitaxy transfer and heterogeneous integration is adopted to realize the circuit. This approach has resulted in a more robust and reliable process for developing III-V based

submillimeter-wave circuits integrated on silicon membrane carriers. The quadrupler fabricated with the new process has produced an output power of 100 mW at 160 GHz and peak efficiency of 25.5%. As multipliers like this quadrupler are driven with higher power levels at their input stage, thermal management become very crucial. Without careful attention to thermal considerations, frequency multipliers can experience significant degradation in electrical performance. The next chapter will focus on characterizing the thermal behavior and properties of the quasi-vertical diodes.

# Chapter 4

# Thermal Characterization of Terahertz Quasi-Vertical Diodes Heterogeneously Integrated on Silicon

The work presented in this chapter is based on a paper presented at *IRMMW-15* (paper #11 under List of Publications) and a paper published in *IEEE Trans. on Electron Devices* (2018) (paper #2 under List of Publications).

Thermal management and design have been understood, for many years, as critical factors in the implementation of submillimeter-wave Schottky diode-based circuits and instruments [60], [61]. Removal of heat is particularly important for frequency multipliers, as these circuits generally exhibit low-to-modest conversion efficiencies and are usually driven with high-power sources to achieve usable output power in the submillimeter-wave region of the spectrum [62]. Elevated diode junction temperatures due to inadequate heat sinking is known to degrade performance, accelerate aging effects (for example, due to electromigration, ohmic contact deterioration, or thermally-induced stress), and can ultimately lead to device failure [25], [63], [64]. The relatively-low thermal conductivity of GaAs (the predominant material technology for submillimeter-wave diodes) [65], coupled with restrictions on diode anode size and geometry needed to minimize parasitics and achieve the device impedances required for high-frequency operation, present significant challenges and trade-

offs between electrical and thermal designs of these devices. Recognition that heating is a major factor limiting efficiency and output power has prompted a number of approaches to mitigate excessive temperature rise in the junction of planar diodes, including the use of AlN or diamond as low-loss substrates that act as heat spreaders [25], [60].

The quasi-vertical Schottky diode on Si technology developed in Chapter 2 offers advantages in terms of thermal management due to the proximity of the device mesa and the ohmic contact heat sink and the integration on silicon, which has a higher thermal conductivity compared to gallium arsenide and quartz. In this chapter, we start by discussing the quasi-vertical geometry and the features that allow it to dissipate heat efficiently (Section 4.1). Then, prior thermal characterizations of planar diodes are summarized (Section 4.2). Next, diode thermal modeling is explained using equivalent circuit models and finite element simulations (Section 4.3). The heating and cooling transient profiles of quasi-vertical diodes are then measured using thermo-reflectance (Section 4.4) and electrical transient (Section 4.5) measurement techniques. The results from both methods are discussed (Section 4.6), and finally a simulation of the full integrated quadrupler chip is presented (Section 4.7). The material parameters used in the thermal simulation of the quadrupler are based on time-domain thermo-reflectance measurements.

## 4.1 Quasi-Vertical Geometry

The quasi-vertical Schottky diode geometry, discussed in Chapter 2, is an alternative to the mature and more common planar diode topology. Planar diodes, also called laterally oriented diodes, are characterized by an anode and ohmic contact which lie on the same plane, separated by a surface channel (Fig. 4.1(a)). Planar diodes are usually fabricated on a semi-insulating GaAs substrate. Unlike planar diodes, the quasi-vertical diode structure (Fig. 4.1(b)) consists of placing the metal ohmic contact under the diode's anode and epitaxial mesa, thus providing a large-area ohmic cathode contact that also serves as an integrated heat sink.

Development of the quasi-vertical diode structure described above was motivated as an effort to reduce device parasitics (series resistance and shunt

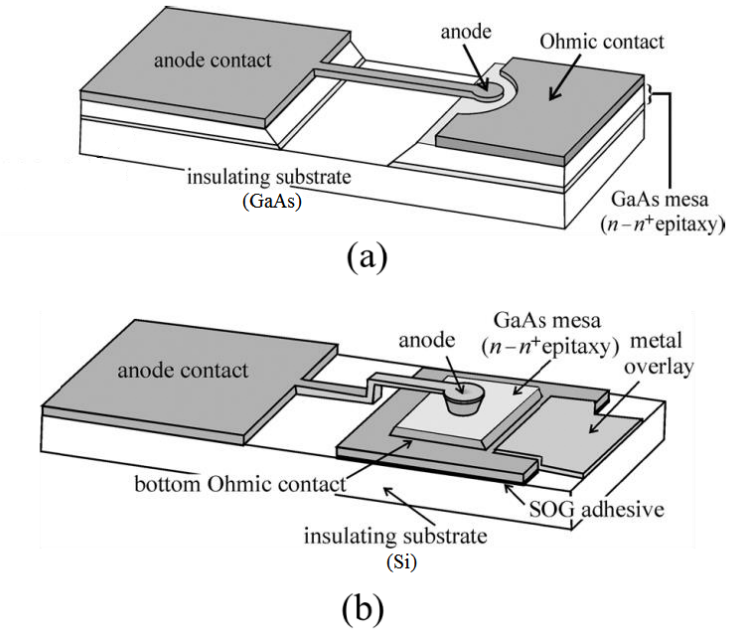



Figure 4.1: Diagrams showing the geometry of (a) a laterally-oriented planar diode and (b) a quasi-vertical diode integrated into a planar circuit.

capacitance) as well as to fabricate devices on a suitable low-loss substrate that can be micromachined to form fully-integrated chips with electrical circuitry and contacts. The high efficiency (>25%) and power output (100 mW) of frequency quadruplers implemented with this technology (as seen in Chapter 3), in addition to estimates of the diode temperature based on electrical measurements [1], suggest the quasi-vertical geometry offers a number of benefits with regard to thermal management in comparison with standard planar diode configurations. Notably, the ohmic contact acts as an integrated heat sink that underlies the full device mesa and can be placed in close proximity to the anode. The use of silicon as a substrate (with a thermal conductivity of 150 W/m-K), provides improved heat spreading and thermal grounding to the circuit housing compared to GaAs (having a thermal conductivity of 55 W/m-K). In addition, the anode finger (Fig. 4.1) is in direct contact with the silicon substrate, thus presenting a secondary thermal path that directly shunts the GaAs mesa.

## 4.2 Prior Work

Electro-thermal modeling of submillimeter-wave Schottky diodes has proven invaluable as a tool to inform the design process and tailor circuit architectures for improvement in efficiency and power handling [60]. In the case of submillimeter-wave frequency multipliers, this requires incorporating the effects of temperature on the design and operation through analyses that couple the electrical and thermal models of the device to achieve a self-consistent solution. These thermal models typically employ analytical tools such as equivalent circuits, finite-difference time-domain solutions of the heat equation, or finite-element simulations of 3-D models [66]. The thermal models are then compared to measured temperature distributions, which can be obtained using imaging methods (thermography). Typically, infrared cameras are utilized to measure thermal radiation emitted from the device [67], [68]. Fig. 4.2 shows the measured and simulated temperature distributions of a multiplier chip with a DC power dissipation level of 7 mW, published by Tang [67]. Although infrared imaging methods can provide information on the temperature distribution over a device (or array of devices), they offer spatial resolutions which are diffraction-limited, and frame rates that usually limit the ability to resolve thermal time constants less than 1 µs.

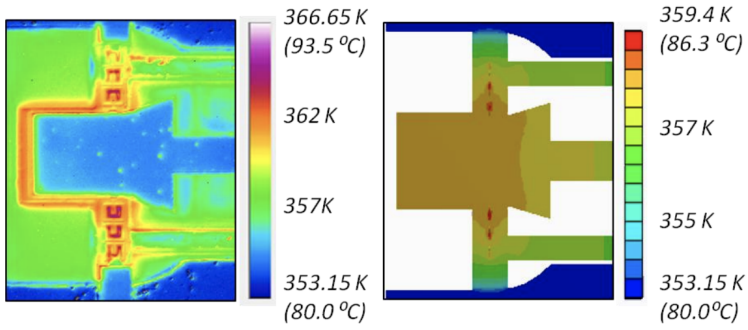



Figure 4.2: Measured and simulated temperature distribution of the multiplier chip from [67].

Experimental characterization of the thermal behavior of submillimeter-wave Schottky diodes can also be performed using electrical techniques, whereby the temperature dependence of the diode current-voltage characteristic is used to estimate the junction temperature [1], [69], [70]. Fig 4.3 shows the thermal

response plots for different anode size planar diodes obtained using the electrical transient method. The transient current measurement technique enabled S. Khanal in [71] to extract the thermal resistances, thermal time constants, and peak junction temperatures of the device shown in Fig. 4.3(b). Unlike imaging methods, estimation of temperature based on electrical measurements allows for the characterization of packaged devices (such as frequency multipliers mounted in a waveguide). This approach, however, does not directly provide spatial information or maps of the temperature distribution over the device geometry. Moreover, the electrical parameters of the device-under-test and measurement instrumentation (resistance and parasitic capacitance) can significantly impact extraction of the device thermal parameters based on measurement of electrical transients. Typically, this requires introducing a delay to allow the electrical transients to decay prior to acquiring data for thermal analysis [71], thus necessitating extrapolation to estimate the operating temperature of the diode junction. Finally, the use of an electrical parameter (e.g., applied voltage) to sense temperature introduces the potential of self-heating of the device and associated errors in estimation of the temperature.

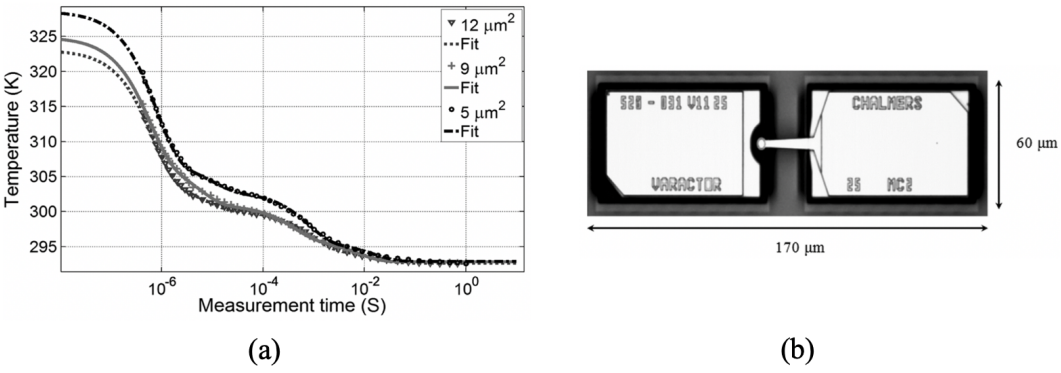



Figure 4.3: (a) Thermal response plots of different anode size planar diodes obtained using the electrical transient method, (b) Microscope photograph of a 9 $\mu m^2$diode under test (from [71]).

In this chapter, two different methods are used and compared to characterize the thermal performance of quasi-vertical diodes integrated on silicon: thermo-reflectance, which is based on the temperature-dependence of the refractive index of a material at optical frequencies and electrical transient measurements that utilize the diode current-voltage characteristic as a

thermometer. But first, we need to develop a thermal device model for the quasi-vertical Schottky diode geometry.

## 4.3 Thermal Device Model

A cross-section of the device epitaxy and structure is shown in Fig. 4.4. The diode mesa lies directly on an ohmic metal pedestal that is bonded to a silicon carrier which serves as a low-loss substrate for RF signal lines and circuitry. A metal overlay of the ohmic pedestal provides the cathode contact, as well as a thermal path for removing heat from the diode to the substrate. The device is fabricated using the process outlined in Chapter 2. Based on this device geometry, two thermal models are developed. The first model is based on equivalent circuits and the second on finite element simulation.

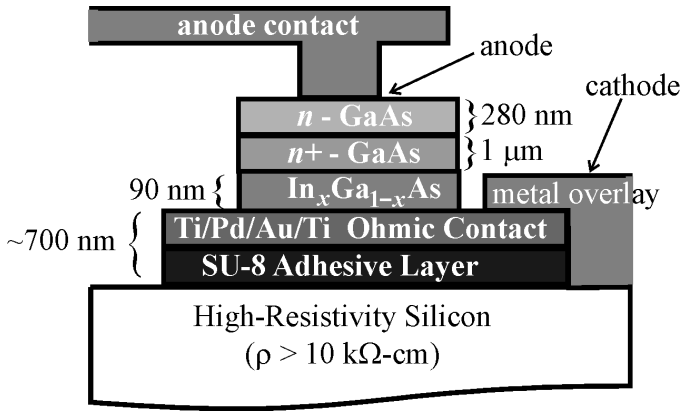



Figure 4.4: Diagram of the diode cross-section and epitaxy. The semi-insulating handle and AlGaAs etch stop layers are removed in the fabrication process and are not shown. Note the device layers are not shown to scale.

### 4.3.1 Thermal Equivalent Circuit Model

Equivalent electrical circuit representations for heat flow [72] are a useful and commonly used tool for understanding thermal transients in devices as well as for identifying thermal bottlenecks. A simplified thermal model of the quasi-vertical diode, superimposed over the device geometry, is shown in Fig. 4.5. In this model, dissipation of electrical power in the diode's junction and series

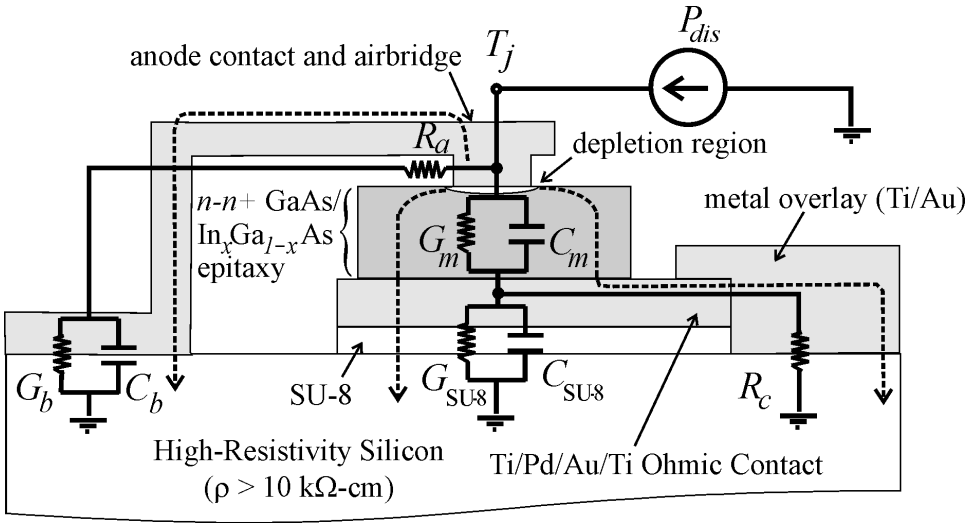



Figure 4.5: Diagram of the quasi-vertical diode geometry showing the paths (dashed lines) for heat flow from the anode to the thermal ground (silicon substrate) and simplified thermal equivalent circuit model.

resistance generates heat that is represented as a current source. This dissipation, in conjunction with conductive cooling mechanisms that are modeled with equivalent thermal impedances, provide paths for heat flow to thermal ground (held at ambient), and determine the instantaneous temperature of the device. As indicated in Fig. 4.5, the thermal impedance of each material layer comprising the diode may be represented as a parallel combination of a thermal conductance G and thermal capacitance C. In the simplified model of Fig. 4.5, the GaAs and $In_xGa_{1-x}As$ layers of the diode mesa are combined into a single effective thermal impedance ($G_m \parallel C_m$). Likewise, parallel conductances and capacitances represent the thermal impedances of the airbridge finger ($G_b \parallel C_b$), SU-8 adhesive layer ($G_{SU-8} \parallel C_{SU-8}$), and cathode ohmic contact metal overlay ($G_c \parallel C_c$). Heating and cooling transients of the diode depend on thermal time constants ($\tau$) associated with each layer (denoted with subscript i),

$$\tau_i = \frac{C_i}{G_i}. \tag{4.1}$$

The capacitance and conductance are given by [73]:

$$G_i = \frac{A\kappa}{t}, \tag{4.2}$$

where $A$ is the cross-sectional area, $\kappa$ is the thermal conductivity, and $t$ is the material's thickness, and

$$C_i = \rho V c_p, \tag{4.3}$$

where $\rho$ is the density, $V$ is the volume, and $c_p$ is the specific heat capacity.

For micro-scale devices, the thermal boundary resistance at material interfaces needs to be considered, since its contribution can sometimes dominate the overall thermal resistance [74]. The diode thermal resistances at the anode and cathode interfaces are respectively denoted in Fig. 4.5 as $R_a$ and $R_c$.

From the thermal model, the steady state junction temperature is found as [73]:

$$T_j - T_0 = R_{th} P_{dis} \tag{4.4}$$

where $R_{th}$ is the total thermal resistance between the diode junction and thermal ground, $T_j$ is the junction temperature, $T_0$ is the ambient temperature (thermal ground), and $P_{dis}$ is the power dissipated in the diode. Using the thermal parameters' temperature independent nominal values, ignoring thermal boundary resistances, and assuming that the diode mesa stack consists only of undoped gallium arsenide, we can obtain a rough estimate for the total thermal resistance and thermal time-constant of a 5.5 µm diameter device:

$$R_{th} = 1000 \, \frac{K}{W}$$

$$\tau = 500 \, ns$$

These estimates are helpful in understanding qualitatively the dominant heat paths in the quasi-vertical diode structure. The thin and poorly conductive SU-8 layer acts as a thermal open-circuit. On the other hand, the highly conductive ohmic behaves as a thermal short. The heat temperature of the hot spot (anode) is therefore governed by the parallel thermal paths formed by the mesa stack and the gold airbridge.

### 4.3.2 Finite Element Model

While simple lumped equivalent circuit analogs provide qualitative information of the thermal properties of the Schottky diode as well as intuitive guidance for thermal design, finite element solvers can provide a more complete representation of the temperature distribution throughout the geometric structure of the device. A finite element solution is acquired using the ANSYS Mechanical [75] simulation tool and the 3-D model used for the quasi-vertical diode is shown in Fig. 4.6, along with the critical geometry dimensions in units of micrometers. The mesh size for the model is adjusted to 3 µm around the critical features (diode stack and airbridge). The airbridge length is 17 µm, width is 5.5 µm, and thickness is 1.35 µm, corresponding to the physical dimensions of the devices tested in this work. The rectangular mesa dimension is 11 µm x 15 µm.

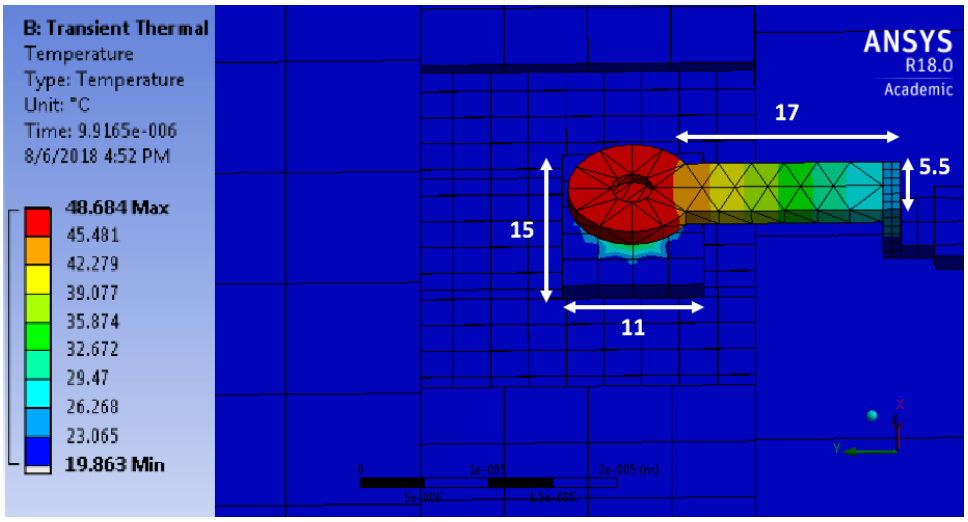



Figure 4.6: 3-D finite element model of the quasi-vertical Schottky diode. Dimensions given in the figure have units of µm.

An input heat flux equal to the net electrical power dissipated divided by anode area is applied directly beneath the diode contact. The bottom and side facets of the substrate are fixed to the ambient temperature (293 K) and remaining surfaces are assumed to be adiabatic. Convection and radiation cooling mechanisms are assumed negligible. The steady state and transient solutions are obtained by solving the heat equation. The relevant material

Table 4.1: Material thermal properties.

| Material | Thermal conductivity (W/m K) | Thermal capacity (J/Kg K) | Mass density ($Kg/m^3$) |
|---|---|---|---|
| Diode Stack | <44 | 350 | 5320 |
| Plated gold | 214 | 129 | 19300 |
| SU-8 | 0.25 | - | - |
| Silicon | 124 | - | - |
| **Boundary** | **Thermal boundary conductance ($MW/m^2$ K)** | | |
| Au/Ti/GaAs | 35 | | |
| InGaAs/Ti/Au | 35 | | |

thermal properties used in this analysis are listed in Table 4.1. The thermal conductivity for the gold metallization is set to 214 W/m-K, based on the measured electrical conductivity (3 x $10^7$ S/m) and the Wiedemann–Franz law (see Section 4.7). The thickness, composition, and doping levels of various films in the device structure will alter the thermal conductivity of various layers in comparison to their bulk values. This makes an estimation of the thermal conductivity of the diode mesa stack, in particular, very difficult. It is also difficult to estimate the effect of doping and interfaces (such as InGaAs/GaAs) on the overall thermal resistance. For example, the Ti/GaAs thermal interface can add a significant thermal boundary resistance and the specific value depends on the fabrication process [76]. Therefore, these layers are lumped into a single layer of thickness 1.37 µm. The effective thermal conductivity of this layer is used as a fitting parameter to model the measured results presented in the following section. In an effort to reduce the number of fitting parameters, the ohmic and anode thermal boundary conductances $G_a$ and $G_c$ are estimated using a time-domain thermo-reflectance (TDTR) measurement (discussed in Section 4.7) to a value of 35 $MW/m^2 - K$. The other material parameters are well established values [67].

## 4.4 Thermo-Reflectance Technique

The thermo-reflectance measurement technique is based on the change in refractive index (and therefore surface reflectivity) with changes in temperature [77]. The fractional change in reflectance ($\Delta$R/R) as a function of temperature change ($\Delta$T) is approximated, to first order, as

$$\frac{\Delta R}{R} = \chi \Delta T. \tag{4.5}$$

The thermo-reflectance calibration coefficient $\chi$ depends on the sample material, wavelength of the illuminating light, angle of incidence (and by extension surface roughness), and the composition of the sample. The thermo-reflectance calibration coefficient typically varies from $10^{-2}$ to $10^{-5}$ $K^{-1}$ [77], with values reported in the literature for plated gold at 530 nm [77], [78], [79], [80] varying over a range of -3 x $10^{-4}$ to -2.3 x $10^{-4}$ $K^{-1}$ . In this work, a value of -2.65 x $10^{-4}$ $K^{-1}$ is chosen and the uncertainty in temperature estimation resulting from this choice is incorporated in error analysis for reported results.

The experimental setup for thermo-reflectance measurements is shown in Fig. 4.7(a). The change in the diode's surface reflectivity under a voltage-pulse heating excitation is measured with a Microsanj NT210A unit [81] which includes a signal generator, a pulse generator, and a control unit. The setup utilizes a green (530 nm) LED light source and a CCD camera to sense the intensity of the reflected signal. 530 nm light is chosen because the reflectivity of a gold surface is sensitive near this wavelength [77].

As the change in surface reflectivity with temperature is small, the signal measured by the CCD camera is averaged over many device thermal excitation cycles. Referring to the timing diagram of Fig. 4.7(b), the CCD records reflectance information only for the duration of the LED illumination pulse. Consequently, the measurement requires synchronizing the device excitation, LED illumination, and image acquisition. Fig. 4.7(b) shows the timing signals involved. A square-wave voltage pulse train excites the diode with the ON voltage level chosen to deliver the desired heating power to the diode. The diode voltage and current are monitored using an oscilloscope connected in shunt with the device, and an ammeter in series with the set up. For each period, the voltage is ON for 50 µs with a 30% duty cycle. These parameters

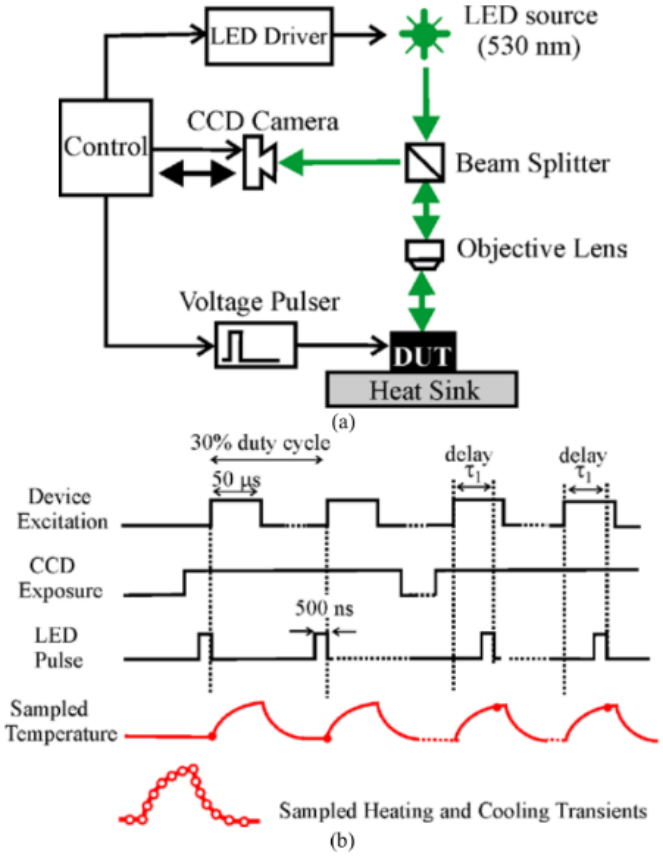



Figure 4.7: (a) Experimental setup for thermo-reflectance characterization of the diode. (b) Time diagram for acquisition of the diode heating and cooling transients.

allow the diode to cool down completely to ambient temperature before the next heating voltage pulse is applied. From these parameters, the Microsanj software calculates the minimum width of the LED pulse and, therefore, the time resolution of the measurement to be 500 ns. The delay of the illumination pulse relative to the device excitation pulse is controllable and the full diode thermal transient can be assembled by acquiring a sequence of images as the illumination pulse delay is adjusted in increments relative to the rising edge of the diode excitation pulse [82]. In this work, for each increment in pulse delay time, the reflected light intensity measured by the CCD camera is averaged for four minutes.

Thermo-reflectance characterization as described above is performed for

two anode size quasi-vertical diodes: 5.5 µm and 3.5 µm diameter anodes. Temperature maps of these devices are obtained using the procedure described above.

Fig. 4.8 shows the top-view of a 5.5 µm diameter diode and Fig. 4.9 shows the two-dimensional temperature maps of this diode at four sample times during cooling. The input electrical power delivered to heat the diode is 6.86 mW. A post-processing shadow algorithm is used to remove data from non-planar surfaces that result in erroneous intensity readings. Consequently, these areas appear as black pixels in the 2-D images. The surface of the gallium arsenide mesa is also shadowed as the thermo-reflectance of this material is not sensitive to light at 530 nm wavelength. The temperature readings of the 2-D images are calibrated to gold, using a thermo-reflectance coefficient of -2.65 x $10^{-4}$ $K^{-1}$.

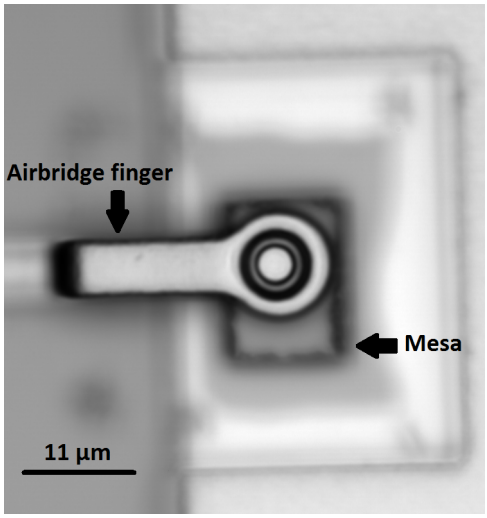



Figure 4.8: Optical image of the 5.5 µm diameter diode from above.

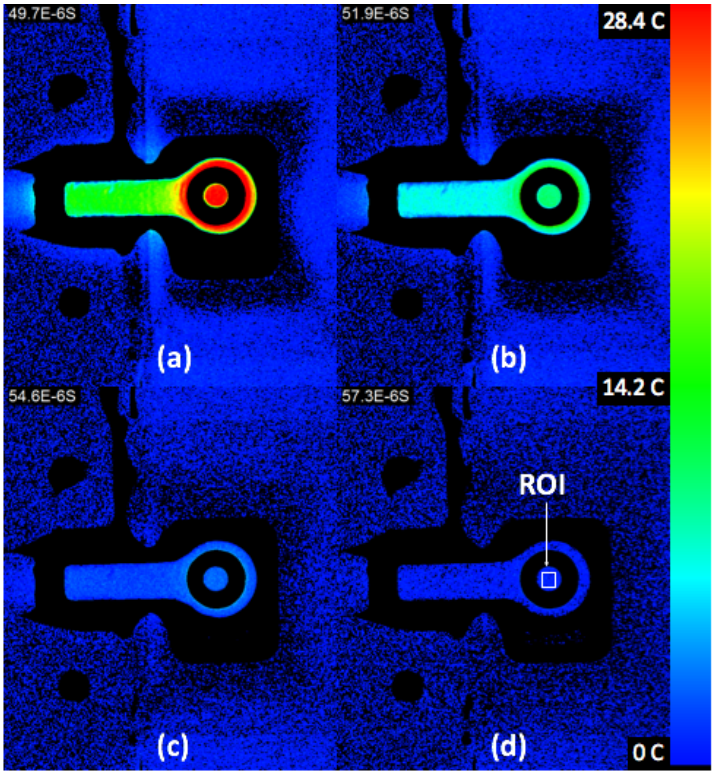



Figure 4.9: Thermal maps of diode D1 obtained at times (a) 49.7, (b) 51.9, (c) 54.6 and (d) 57.3 µs after removal of the heating excitation using thermo-reflectance measurements. Note the temperature scale is indicated on the right.

Heating and cooling curves are obtained from the 2-D temperatures maps and are shown in Fig. 4.10 and 4.11. For the 5.5 µm diodes, the temperature shown has been averaged over a rectangular region of interest (ROI) as indicated in Fig. 4.9(d). This region contains 196 pixels and is located at the top of the anode pillar, as it is the closest visible region to the anode-mesa contact, which is the hottest spot of the device.

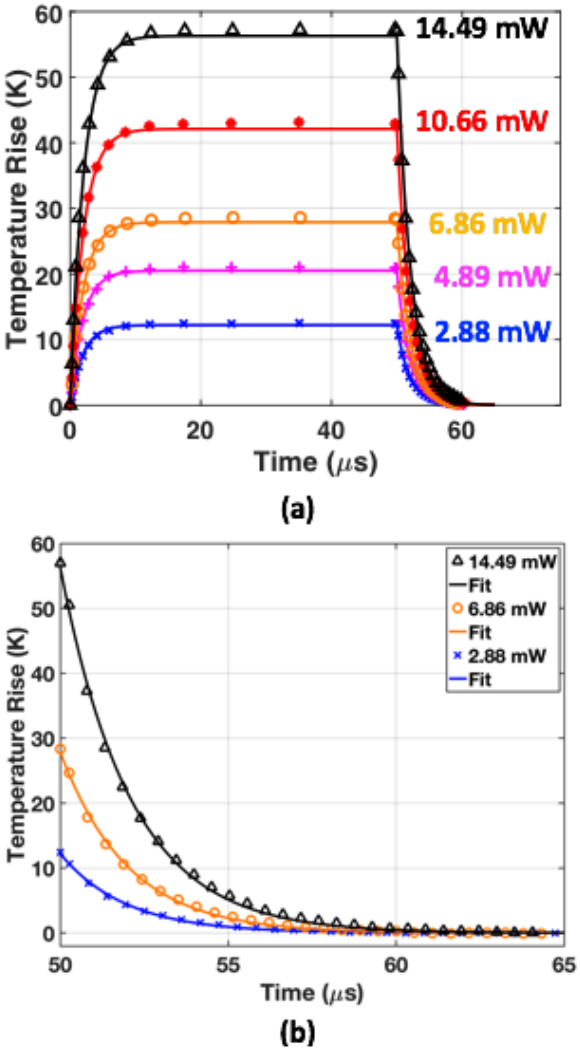



Figure 4.10: (a) Measured and fitted heating and cooling transients of a 5.5 µm diameter diode. The fitted curves utilize a single time constant of 2 µs. (b) Measured cooling transient of this diode compared to the modeled transient using ANSYS Mechanical finite element solver (dashed curve).

The heating and cooling transients at different power excitation levels are presented in Fig. 4.10(a). As the thermo-reflectance imaging measures changes in surface reflectivity, the plot shows the temperature rise relative to ambient (293 K). In this figure as well as all subsequent plots, symbols indicate measured values while lines represent the fitted or modeled temperature. In Fig. 4.10(a), the lines are fitted using an exponential function with a single time constant used for both the heating and cooling transients. The thermal pa-

rameters extracted from these fitted curves are summarized in Table 4.2. As anticipated, the peak diode temperature rise scales linearly with dissipated electrical power in accordance with Eq. (4.4). The fitted value for the temperature rise is in good agreement with the measurement. Furthermore, cooling of the quasi-vertical diode is described with a single time constant of 2 µs. This is in contrast to the planar diodes reported in [71] (Fig. 4.3(a)), which exhibit multiple time constants and much slower thermal processes as a consequence of their geometry and integration using flip-chip bonding.

Table 4.2: Extracted diode thermal parameters for diode (area = 23.76 µm$^2$) vs power.

| Power (mW) | Measured Peak Temperature Rise $T_R$ (K) | Fitted Temperature Rise T (K) | Time Constant τ (µs) | Total Measured Thermal Resistance (K/W) |
|---|---|---|---|---|
| 2.88 (±0.01) | 12.45 (±1.54) | 12.21 (±0.20) | 1.95 (±0.05) | 4322.91 (±551.65) |
| 6.86 (±0.01) | 28.35 (±2.80) | 27.90 (±0.40) | 2.01 (±0.05) | 4132.65 (±414.79) |
| 14.49 (±0.01) | 56.97 (±5.10) | 56.30 (±0.80) | 2.09 (±0.05) | 3931.68 (±354.92) |

Uncertainty in estimation of the peak temperature rise is comprised of two components: the uncertainty in the choice of the coefficient of thermo-reflectance for gold and measurement error. Error due to uncertainty in the thermo-reflectance coefficient ($\chi$) for gold is found is by obtaining the temperatures corresponding to the ROI region given the minimum and maximum values for $\chi$ found in the literature. Measurement error is found from the standard error of the mean using seven thermo-reflectance measurements based on a 95% confidence level. Finally, the fitting error in temperature $T_1$ and time constant $\tau$ correspond to a 95% confidence bound with an R-square value of 0.999.

Fig. 4.11 compares the measured cooling curves under the same power excitation (6.87 mW) for the two diode diameters (5.5 µm and 3.5 µm) with the ANSYS model. Note that the temperature rise for the 3.5 µm diameter diode is higher than 5.5 µm diameter diode. From this analysis, the thermal conductivity of the mesa stack is adjusted to the value of 9.5 W/m-K to fit the measured data. The physical rationale and validity of this fitted value will

be discussed later at the end of this section.

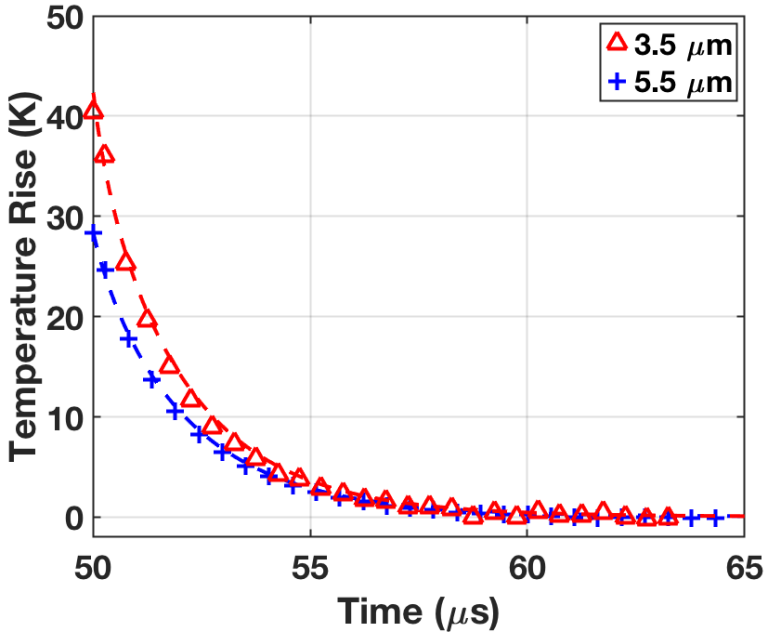



Figure 4.11: Measured cooling transients of a 5.5 µm diameter diode and 3.5 µm diameter diode. The ANSYS curves are shown as dashed lines.

## 4.5 Electrical Transient Method

A second method for temperature characterization, based on electrical transient measurements, was implemented to estimate the diode temperature and thermal time constants as well as to provide a comparison with both the thermo-reflectance method presented above and other results reported in the literature [71]. The electrical characterization method employed utilizes the approach described in detail in [71] and exploits the temperature dependence of the current-voltage (I- V) relationship of the Schottky diode [83] to estimate junction temperature.

In the present work, diodes with 5.5 µm diameter anodes were mounted to a temperature-controlled stage and I-V measurements performed to obtain temperature calibration curves. Fig. 4.12(a) shows the current-voltage characteristic of a 5.5 µm diameter anode quasi-vertical diode at ambient temperature. At low applied voltages, conduction through the high-resistivity silicon substrate dominates the I-V characteristic and appears electrically as a 10 KΩ

resistor shunting the diode. A sensing voltage, $V_M$, between 0.56 V and 0.58 V, is selected in the region of the I-V curve where conduction through the diode is dominant, but remains sufficiently low to minimize self-heating. The resulting calibration curves are shown in Fig. 4.12(b). A third-order polynomial fit (solid line) is used to obtain a temperature-current relationship for each sensing voltage.

Transient current measurements were performed using a Keysight B1500A Semiconductor Parameter Analyzer, with two remote-sense and switch units (RSUs), each connected to a diode terminal. One RSU is used to apply a transient step voltage waveform, that is switched between the heating voltage $V_H$ = 0.75 V, to the sensing voltage $V_M$ . The heating voltage is chosen to deliver 6.92 mW to the diode, a power level near that used for the thermo-reflectance method, and is held for 50 µs so that the diode heating reaches steady-state. After 50 µs, the applied voltage is reduced linearly to $V_M$ over a 10 ns interval and the second RSU measures the transient current. Fig. 4.13 shows the measured electrical transient curves obtained using the three different sensing voltages. A third-order polynomial fit for the measured temperature-current curves of Fig. 4.12 is used to convert the measured transient current to temperature. A 1.4 µs delay is introduced after the voltage is switched to $V_M$ before recording the transient current used for the temperature curves. This delay allows for electrical transients to settle. The measured thermal transients shown in Fig. 4.14 are fit using an exponential decay with time constants indicated in the figure inset. Note that the best fit to the electrical transient method requires two time constants, in contrast with the thermo-reflectance measurement, which exhibits a single time constant.

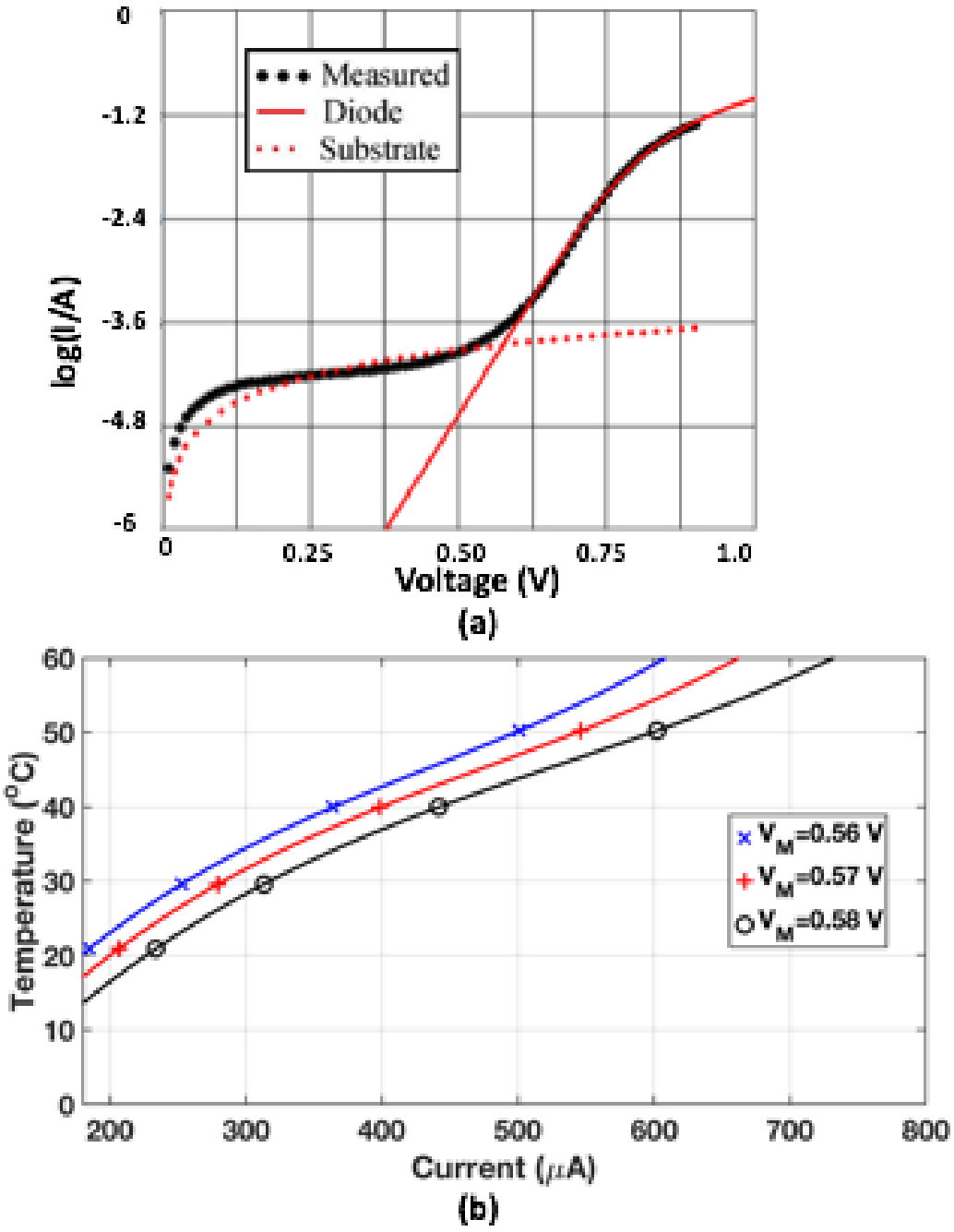



Figure 4.12: (a) Measured and fitted current-voltage relation for a 5.5 µm diameter quasi-vertical diode. (b) Measured diode temperature-current calibration curves for three different sensing voltages, $V_M$.

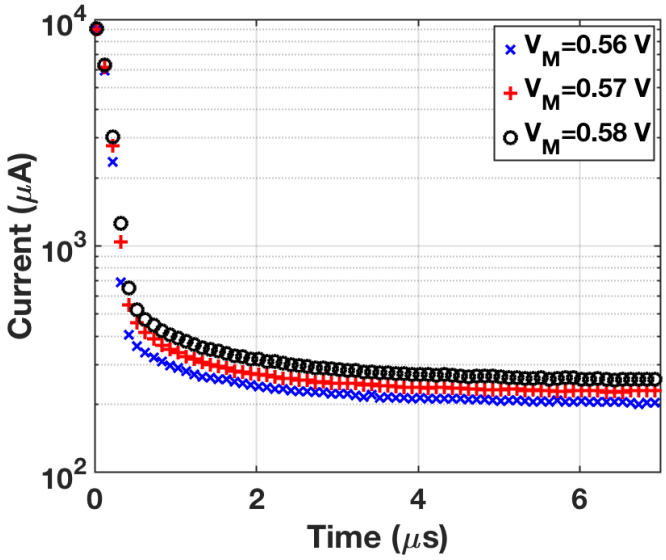



Figure 4.13: Measured transient current curves for a 5.5 µm diameter diode. The device was first held at 0.75 V for 50 µs. Then at t = 0 s in this figure, the voltage was switched to three bias points: 0.56 V, 0.57 V, 0.58 V.

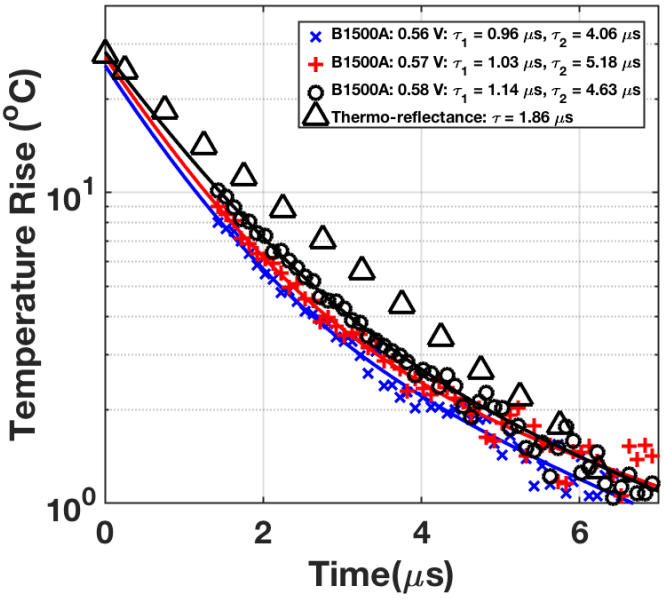



Figure 4.14: Measured and fitted thermal cooling transients for a 5.5 µm diameter quasi-vertical diode using electrical transient measurements. Results obtained from thermo-reflectance measurements (triangles) of the same diode are shown for comparison. Deviation of electrical transient data from a straight line indicates the necessity of two time constants.

## 4.6 Discussion

This work has described the thermal characterization of heterogeneously integrated quasi-vertical Schottky diodes using two distinct and complementary techniques, one based on thermo-reflectance of visible light and a second based on electrical transients. The two methods give comparable results regarding the net time required for these diodes to cool from their operating temperature to ambient — approximately 10 µs — which, notably, is several orders-of-magnitude lower than for GaAs flip-chip mounted diodes reported in the literature [71]. The cooling transients and time constants extracted from the two methods, nevertheless, exhibit some differences that are likely a consequence of the specific physical parameters measured in each case and the inherent limitations of each technique.

Thermo-reflectance provides a method of imaging the temperature distribution over the surface of the device and allows the cooling transient to be extracted by sampling the reflectance of visible light from the metallized (gold) surface of the diode's anode contact. Unlike the electrical characterization approach, this technique permits both the heating and cooling transients to be measured. However, as the thermo-reflectance method samples the surface temperature only, the internal temperature at the junction of the device is not directly monitored and must be inferred. In addition, the necessity to average over many heating and cooling cycles restricts the sample rate for measurement and limits its capacity to observe transients with short time constants.

Characterizing diodes thermal behavior using electrical transients in conjunction with their temperature-dependent current-voltage characteristics is an established method that utilizes standard electrical instruments and provides a means for estimating the internal temperature of the diode junction. This technique is capable of measuring short time constants but is also subject to a number of potential sources of error. As the measured parameter (electrical current) depends on both electrical and thermal transients, the data must be interpreted carefully and necessitates the introduction of a time delay between the removal of the electrical stimulus and collection of data to allow the electrical portion of the transient to settle. The diode junction temperature is estimated through extrapolation and the temperature transient is monitored

by the change in diode current at a fixed low-level "sensing" voltage, which potentially can introduce self-heating of the device. Moreover, this method of thermal characterization is not capable of producing temperature maps or accounting for the effects of non-uniform heating in the device structure.

In this work, a delay of 1.4 µs was introduced for the electrical transient measurement to allow sufficient time for the electrical response of the diode and measurement instrumentation to decay and three different sensing voltages were used to monitor the thermal response. Extrapolation of these transients yield similar operating temperatures (27 °C ± 1.5 °C, Fig. 4.14) that are in good agreement with one another and also with the value obtained using thermo-reflectance (27.82 °C). These results suggest that sufficient time has elapsed and that the transient response after this delay is dominated by cooling of the device and that the sensing voltage does not introduce significant self-heating. Interestingly, the electrical transient measurement data exhibits two time constants (of approximately 1 µs and 5 µs), consistent with the results obtained in [71], while the thermo-reflectance data is described with a single time constant of approximately 2 µs. There are several possible explanations for this. The sampling rate of the thermo-reflectance technique (0.5 µs) under a 50 µs excitation limits its capacity to resolve short time constants that could be associated with rapid thermal processes within the diode. Furthermore, thermo-reflectance deduces temperature based on the optical reflectance from the surface metallization of the anode and finger contact, so data obtained from this method is not influenced by the electrical response of the device which exhibits both electrical and thermal transients. Of particular note is that the two characterization methods essentially probe different regions in the device: thermo-reflectance monitors the surface temperature while the electrical transient measurement provides an estimate of the internal temperature of the diode junction and substrate. As the anode metallization and diode junction are separated thermally by a boundary layer thermal resistance and physically by a Schottky barrier, it is conceivable that these regions of the diode cool with different characteristic time constants. The cooling profile predicted by the ANSYS finite-element model shows good agreement with the thermo-reflectance measurement (Fig. 4.10(b)). It should be noted that this model utilizes a single fitting parameter, representing the effective thermal conduc-

tance of the diode mesa epitaxial stack, with value of 9.5 W/m-K. As the epitaxial stack consists of two n-doped GaAs layers (280 nm and 1 µm) layers, a GaAs/InGaAs interface, and a 90 nm graded $In_xGa_{1-x}As$ layer, it is difficult to predict apriori the thermal boundary resistance of the interfaces and the thermal resistivity of the thin layers. Using bulk material values for the thermal conductivities (44 W/m-K for GaAs, and 5.5 W/m-K for InGaAs) and a measured value (based on time-domain thermal reflectance measurements) for the GaAs/InGaAs thermal boundary conductance of 90 $MW/m^2-K$, the total thermal resistance of the mesa stack $R_m$ (Fig. 4.5) can be estimated to be 2380 W/m-K. Using this value and Eq. 4.2, the equivalent thermal conductivity for the epitaxial stack is estimated to be 24 W/m-K. Noting that the values of thermal conductivities for thin films are typically significantly smaller than their corresponding bulk values (due to size-effects and doping) [84], the fitted thermal conductivity of the mesa (9.5 W/m-K) for the finite-element model is reasonable.

## 4.7 Application: Full Quadrupler Simulation

### 4.7.1 Material Parameter Extraction using Time-Domain Thermo-Reflectance

Heat transport properties of materials, such as thermal conductivity, can vary significantly from the corresponding bulk properties in comparison to micro and nano scale devices [85]. In fact, scattering mechanisms such as boundary and impurity scatterings, which are more pronounced in thin films, lead to a reduction in the thermal conductivity of materials [85]. To account for these phenomena in submillimeter-wave circuit models such as the 160 GHz quadrupler, time-domain thermoreflectance (TDTR) is used to characterize the thermal properties of the material layers comprising this device. The work presented in this section was done in collaboration with Prof. Hopkins group.

The TDTR technique and data analysis method are described in detail elsewhere [86], [87]; as such, the concept is briefly described here. TDTR is a non-contact optical pump-probe measurement, illustrated in Fig. 4.15, that

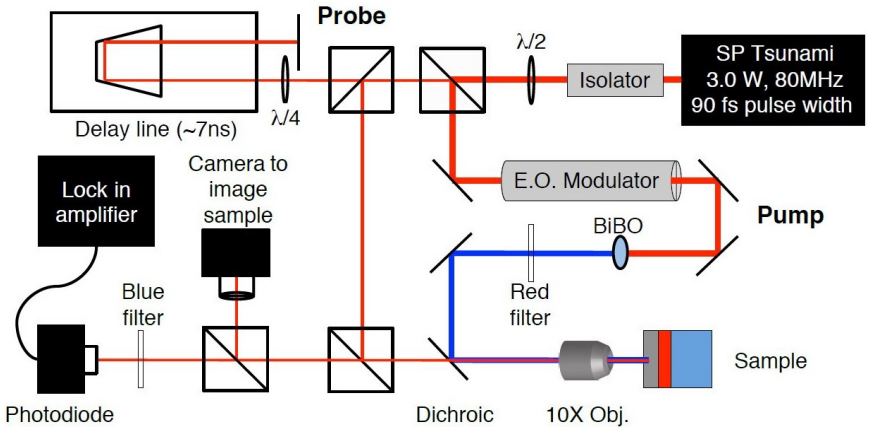



Figure 4.15: TDTR measurement setup.

utilizes a modulated short-pulsed heating event (the pump) to heat the surface of a metal transducer. A time-delayed low-power pulse (the probe) is used to measure changes in thermal decay over time. The pump pulse is modulated via an electro-optical modulator at a driving frequency of 8.8 MHz. The probe pulse is delayed in time, relative to the pump heating event, by a mechanical delay stage at the same spatial point as the pump heating event. An RF lock-in amplifier is used to detect changes in the reflected probe signal at the modulation frequency of the pump heating event. The ratio of the in-phase to out-of-phase voltage (- Vin/Vout) yields information about the thermal properties of the underlying layers via relations which are described in [86], [87]. The thermal conductivity extraction was performed by J.T. Gaskins and B.M. Foley from Prof. Hopkins group. The details of the extraction procedure are outside the scope of this work, but can be found in [86], [87].

Table 4.3 summarizes the thermal conductivity values, measured using TDTR, of the Si layer in the silicon-on-insulator (SOI) wafer, gallium arsenide, and the bonding agent, used in the thermal analysis. In addition, the thermal conductivity of the ohmic contact is also characterized via the electrical resistivity (four-point probe) and the Wiedemann-Franz law, for both an annealed and un-annealed ohmic metallization. The Wiedemann-Franz law is given as:

$$\kappa = \sigma L T,$$

where $\kappa$ is the thermal conductivity, $\sigma$ the electrical conductivity, L is Lorentz

number and is equal to 2.44 x $10^{-8}$ W.Ω.$K^{-2}$, and finally T is temperature.

The results for the two ohmic contact options are summarized in Table 4.4. The thermal conductivity for the un-annealed contact is larger, which further strengthens the potential improvement of the new diode process described in Chapter 2. These material parameters are used in a finite-element analysis of the frequency quadrupler, described in Chapter 2.

Table 4.3: Measured thermal conductivities ($\frac{W}{m-K}$) used in the quadrupler finite element analysis.

| Material | Thickness ($\mu m$) | Bulk | Measured | Meas. uncertainty |
|---|---|---|---|---|
| Si in SOI | 15.00 | 150.00 | 115.00 | 12.4 % |
| GaAs | 1.28 | 46.05 | 42.88 | 7.5 % |
| Bonding Agent | 0.50 | 0.60 | 0.22 | 10.0 % |

Table 4.4: Measured thermal conductivities ($\frac{W}{m-K}$) used in the quadrupler finite element analysis.

| Ohmic metal option | Measured value | Measurement uncertainty |
|---|---|---|
| Annealed | 31.1 | 6% |
| Un-annealed | 108.7 | 5% |

### 4.7.2 Simulation Results

The quadrupler chip analyzed in this work is the 160 GHz balanced quadrupler detailed in Sections 2.6 and 3.3. The finite element method solution to the heat equation is acquired using ANSYS Mechanical with the thermal conductivities measured above. Due to the symmetry of the chip, only half of the quadrupler geometry is simulated as shown in Fig. 4.16. In this analysis, the total power dissipation level is estimated to be 10 mW per anode. This power level per anode assumes a typical drive power of 240 mW, equally divided over the twelve input diodes which have a 50% harmonic generation efficiency (i.e. half the power is converted to the second harmonic frequency and the other half is dissipated as heat). Moreover, only heat conduction is considered and all the non-contact surfaces of the block are assumed to be at room temperature (23.0 °C). The quadrupler chip is designed such that it is suspended in the waveguide block, with protruding gold beam leads clamping it to the waveguide block at

the input and output (see Fig. 4.3(a)). Two additional beamleads protrude from hairpin bias chokes and are bonded to a quartz-supported filter that sits in the block. Fig. 4.16(a) shows the steady state temperature distribution of the original quadrupler chip.

The second stage doubler diodes (magnified in the toggle window) experience the maximum anode temperature of 64.9 °C, due to the lack of proximity of a block heat sink. Fig. 4.16(b) shows the temperature distribution with an extra beam lead close to the second stage diodes. This additional contact to the block reduces the maximum temperature experienced by the diodes to 41.0 °C.

The system level (quadrupler) steady state heat analysis shows that the temperature of the diodes in the second stage can be reduced significantly by introducing a secondary connection the block. The integration on silicon allows the dissipation of heat through a substrate with a high thermal conductivity, compared to GaAs or quartz.

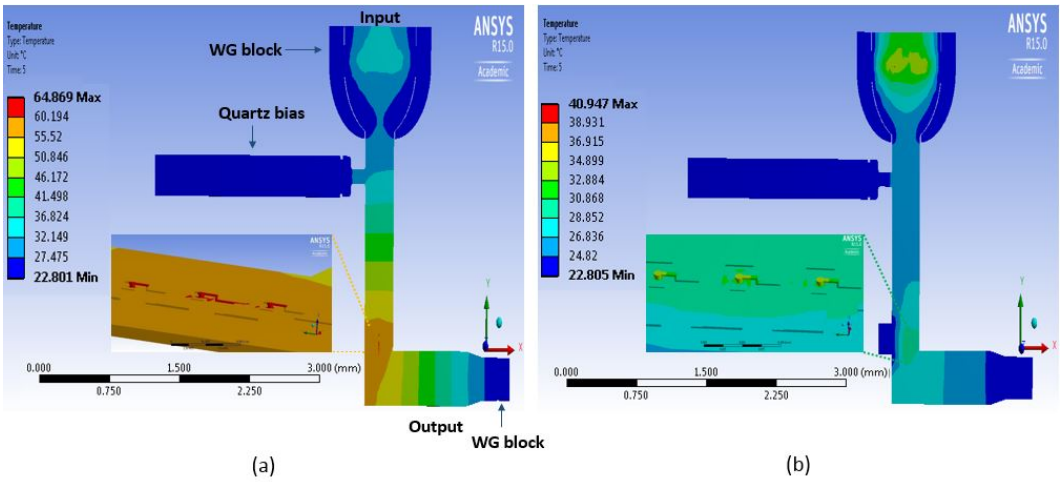



Figure 4.16: Steady-state temperature distribution of: (a) Original quadrupler design, (b) Modified design with an extra beam lead.

# Chapter 5

# WR-5 (140-220 GHz) Quasi-Optical QVD Diode Array

The work presented in this chapter is aimed at assessing the robustness of the new fabrication process described in the previous chapters by designing, fabricating, and testing circuits which contain a large number of heterogeneously integrated diodes: diode arrays. The arrays are intended to interact with electromagnetic energy which propagates in free-space, not confined in a waveguide. Hence, the arrays can be described as quasi-optical arrays. In general, quasi-optics refers to a regime where the wavelength of the electromagnetic radiation (millimeter and sub-millimeter) is comparable to the size of the optical components (lenses and mirrors for example).

Submillimeter-wave diode arrays, especially for imaging applications, have been an important topic of research for the scientific community for decades and they continue to receive significant attention for their use in radio astronomy, imaging spectroscopy, and plasma diagnostics. Moreover, imaging at terahertz or submillimeter-wave frequencies has begun to attract enormous interest because of its large potential impact on defense, security, the biological sciences, medicine, and materials science [10], [88].

The implementation of diode arrays also stems from our research group's history of developing diode arrays for sideband generation (SBG) in tunable laser systems [89], [90]. The frequency of 1.56 THz is of particular interest to the National Ground Intelligence Center (NGIC) for use in compact range radar measurements of scaled targets [91]. An optically pumped far-infrared

molecular laser is used to produce $\sim$ 100 mW at 1.5626 THz, with limited tuning. The array is used to phase modulate tunable sidebands onto the laser. The array architecture is necessary for power handling since it allows the power from the incoming laser beam to be distributed over a large number of elements. The radar system requires a bandwidth of 8 GHz to perform a linear sweep of frequency which is necessary for target range calculation. This tunability can be obtained by mixing the transmitter laser with the output of a microwave synthesizer, through the use of a Schottky diode sideband generator (SBG) up-converter array [91].

In this work, we implement a proof of concept phase shifter quasi-optical diode array at WR-5 frequencies (140 GHz - 220 GHz), based on GaAs quasi-vertical Schottky diodes integrated on a 15 µm silicon membrane. The choice of this frequency band is motivated by the availability of scattering parameter test equipment such as frequency extenders, which allow us to directly measure the magnitude and phase of the reflection coefficient (complex scattering parameters), instead of inferring the phase shift from direct detection measurements, as was done in [89][90]. Prior implementations of diode arrays, which are described in the next section (5.1), have all been limited by fabrication yields issues, as well as high diode parasitic series resistances. The objective of the remaining sections is to describe the design (5.2), fabrication (5.3), and mounting (5.4) of the diode array, and assess the yield (5.5) and DC series resistance (5.6). The final section (5.7) presents the quasi-optical RF characterization of the array at the WR-5 frequency band (140-220 GHz).

## 5.1 Prior Work

Quasi-optical passive and active element arrays were initially developed in the 1980's. Discrete packaged circuit components such as diodes and transistors were integrated into periodic grids, for imaging and power combining applications. Equivalent circuit model analysis techniques based on the induced EMF method [92], and the method of moments [93] were developed to provide engineers with reliable tools to design quasi-optical arrays. Fig. 5.1 shows an image of a 94 GHz monolithic GaAs diode grid with 1600 Schottky-barrier varactor diodes. The GaAs substrate was lapped to a thickness of 230 µm to

suppress unwanted substrate modes. A phase shift of 70° with a 7 dB loss was obtained at 93 GHz when the bias on the diode grid was changed from - 3 V to 1 V [94]. The loss was due to the diode's high parasitic series resistance (20 Ω to 100 Ω).

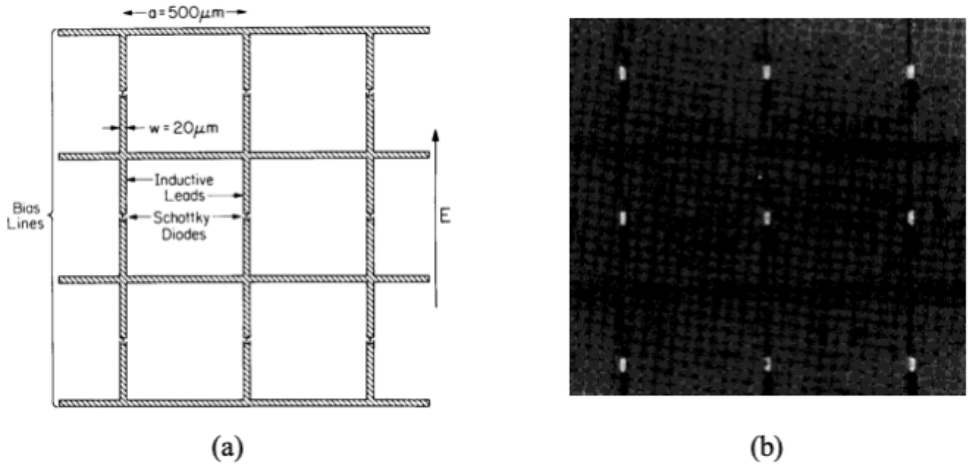



Figure 5.1: (a) Diagram and (b) micrograph of a section of a 94 GHz monolithic GaAs diode grid with 1600 Schottky-barrier varactor diodes developed by W.W. Lam (1988) [94].

The first submillimeter-wave Schottky diode arrays were developed at the University of Virginia during the late 1990's, and were implemented using varistor diodes with planar geometry [89]. Fig. 5.2 shows an image of the first sideband generator array fabricated at UVA, which was developed by Kurtz. The array operated at 1.6 THz, and was integrated on a quartz substrate [89]. The array's sideband conversion loss was measured using a far-infrared laser. The incident power of the laser was spread over many devices (36), which improved the overall power handling. The sideband generator array produced 5.9 $\mu W$ of output power, with a 28 dB double sideband conversion loss [89].

In the 2010's, new implementation of a 1.6 THz sideband generator array was fabricated by Hawasli (shown in Fig. 5.3), based on varactor mode planar GaAs Schottky diodes [23]. A conversion loss value of 26 dB was measured for this SBG implementation. The high conversion loss value was attributed to the high series resistance (58 Ω) and parasitics associated with the planar diode topology and fabrication [90].

All the prior versions of phase-shifter diode arrays suffered from diode

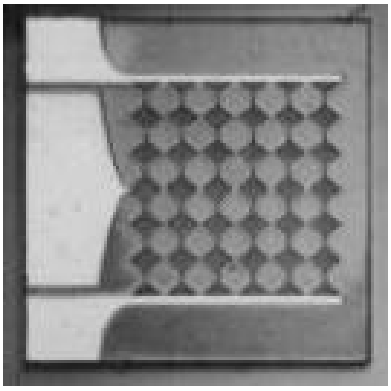


Figure 5.2: 36-Element varistor mode SBG array on quartz developed by D. Kurtz [89].

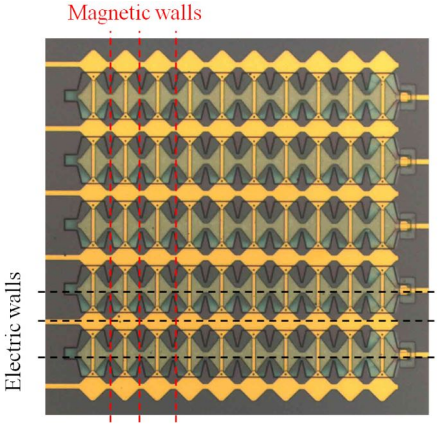



Figure 5.3: 100-Element planar varactor diode SBG array on GaAs developed by Hawasli [23].

parasitics, lack of power handling/thermal management capability, and substrate modes due to the thick host substrate. A new design, which will be presented in the next section, addresses these concerns by utilizing the quasi-vertical GaAs on Si varactor diode technology which simultaneously offers low parasitics (Chapters 2 and 3), a thin host substrate, and superior thermal management properties (Chapter 4).

## 5.2 Design

### 5.2.1 Unit Cell Layout

The basic layout for a unit cell of the diode array described in this work is shown in Fig. 5.4. The unit cell has dimensions of 200 µm x 200 µm x 15 µm. The thin vertical dimension corresponds to the silicon membrane, which is achieved through the SOI process described in Chapter 2. The design is based on a quasi-optical capacitive grid architecture [92], [93]. Most of the unit cell is covered with plated metal (top and bottom metal in Fig. 5.4), with a 14 µm gap at the center forming the grid capacitance. This configuration allows the capacitive coupling of the incoming electromagnetic energy into the varactor quasi-vertical GaAs diode, which is embedded within the unit cell's top metal (Fig. 5.4). An airbridge finger connects the bottom metal, which serves as the diode's anode, to the GaAs mesa which sits atop of the Ti/Pd/Au/Ti ohmic metallization (as shown in Fig. 5.4). The airbridge length is 17 µm, width is 6 µm, and thickness is 2 µm. In this work, two anode size diameters were fabricated: 2.4 µm and 4.0 µm diameter diodes.

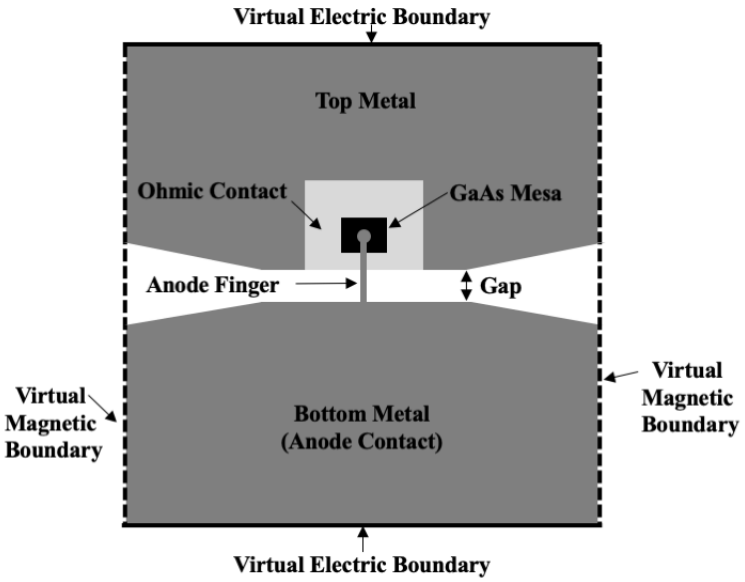



Figure 5.4: Geometry of the array unit cell.

The geometry of the unit cell is mirrored both horizontally and vertically to form the full, symmetric two-dimensional array. Arrays containing 36 and

100 elements are implemented. Fig. 5.5 shows a microscope image of a 100-element (10 x 10) diode array. Also shown on Fig. 5.5 are the lines used to bias each row of diodes.

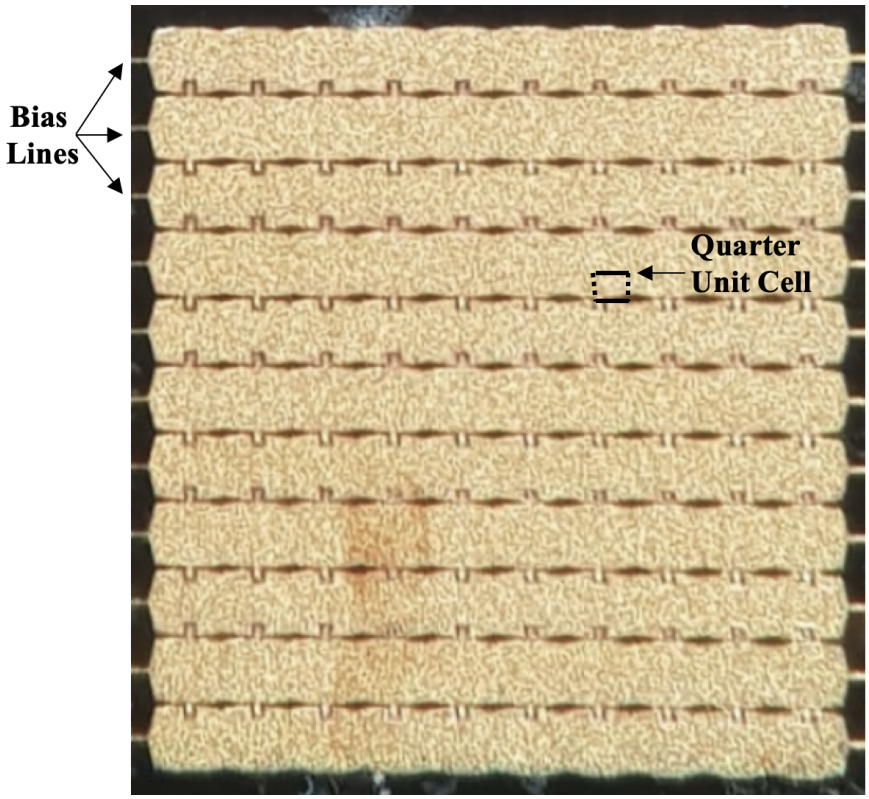



Figure 5.5: Photograph of the full 100-element varactor diode array based on QVD.

### 5.2.2 Equivalent Circuit Model

An equivalent circuit model for the unit cell of an infinite array can be developed by exploiting the array symmetry. Under uniform illumination, and for an infinite array, horizontal symmetry planes can be represented by electric boundaries and vertical symmetry planes represented by magnetic boundaries (shown in Fig. 5.4), thus forming a virtual waveguide for each unit cell.

The capacitive grid is analyzed electromagnetically, within the virtual waveguide, using the induced EMF method [92]. As a result of the symmetry, a quarter of the full unit cell is sufficient for the analysis (see Fig. 5.5). The

induced EMF approach consists of equating the power radiated by the slot gap found using Poynting's Theorem with the power delivered to the feedpoint of the slot antenna, resulting in an expression for the slot gap admittance, and therefore the slot gap capacitance.

The slot gap capacitance is given by the following expression:

$$C_{gap}(\omega) = \frac{1}{j\omega}\frac{2a}{b}\sum_{n=1}^{\infty} sinc^2(\frac{n\pi w}{2b})(Y_{0n}^{TM+} + Y_{0n}^{TM-}), \tag{5.1}$$

where $\omega$ is the angular frequency, a and b represent the dimensions of the quarter cell, w is the width of the finger in the quarter cell (3 µm), $Y_{0n}^{TM+}$and $Y_{0n}^{TM-}$ are the characteristic TM waveguide mode admittances in the + direction (away from the array into the air) and - direction (into the substrate), and n is an integer. Fig. 5.6 shows a plot of $C_{gap}$ versus frequency from 140 GHz to 220 GHz, based on Equation (5.1). The gap capacitance does not vary significantly with frequency, and is approximately equal to 18 fF over the entire WR-5 frequency band.

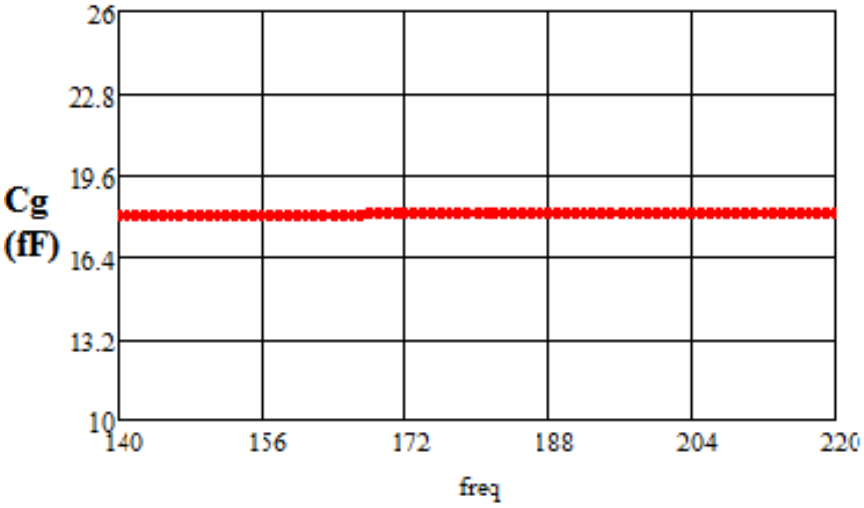



Figure 5.6: Gap capacitance versus frequency (140 GHz - 220 GHz) computed using Equation (5.1).

The finger inductance is more challenging to model since it is suspended off the substrate, with a section of the finger suspended over Si, while the other is suspended over the diode (Fig. 5.4). Thus, the finger inductance value will be used as a tuning parameter. However, the EMF method can estimate the

inductance of a strip of metal across the slot gap, with width w equal to that of the finger airbridge. The series finger inductance is given by the following expression:

$$L_s(\omega) = \frac{1}{j\omega}\sum_{m=1}^{\infty}\left[\frac{2(sinc(\frac{m\pi g}{a})^2}{\sum_{n=0}^{\infty}[[\delta(n).(sinc(\frac{n\pi w}{a}))^2].[\frac{(\frac{n\pi}{b})^2 Y_{mn}^{TM}+(\frac{m\pi}{a})^2 Y_{mn}^{TE}}{(\frac{m\pi}{a})^2+\frac{n\pi}{b})^2}]]}\right], \qquad (5.2)$$

where g is the width of the slot gap for the quarter cell (7 µm), m an integer, and $\delta$(n) is the Neumann factor which is equal to 1 when n=0 and 2 otherwise. Using Equation (5.2), we plot (Fig. 5.7) the series inductance versus frequency from 140 GHz to 220 GHz. The series inductance is equal to 10.6 pH at midband (180 GHz).

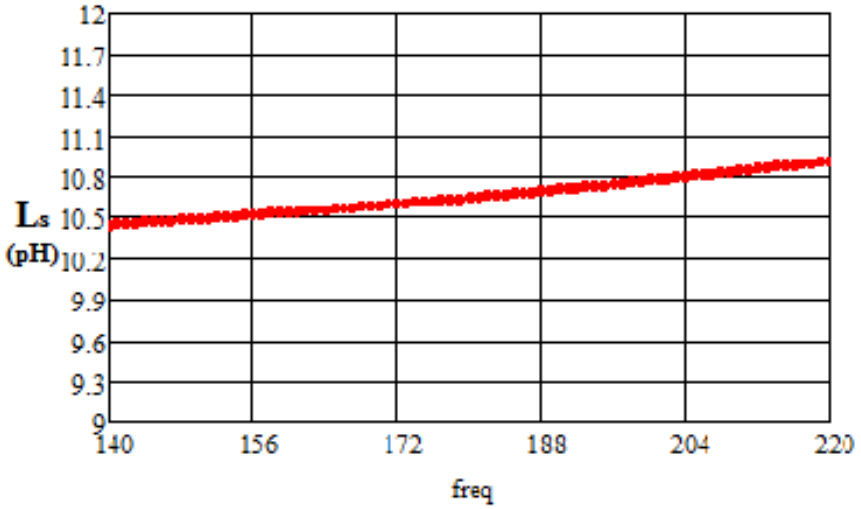



Figure 5.7: Metal strip inductance versus frequency (140 GHz - 220 GHz) computed using Equation (5.2).

At higher frequencies, higher-order modes can be excited in the substrate, which can have a significant effect on the value of the gap capacitance and parasitic inductance. These modes can lead to significant degradation in the diode array's electrical performance. Fig. 5.8 plots $C_{gap}$ and $L_s$ versus frequencies from 335 GHz to 750 GHz. As shown in Fig. 5.8(b), the series inductance changes rapidly in the WR-1.5 band (500-750 GHz). Beyond 666 GHz, it takes a negative value which indicates that, beyond that critical frequency, it is more appropriate to represent it as a parasitic capacitance. To operate

similar capacitive grids at higher frequencies, future circuit designers would need to either use a thinner substrate or shrink the dimension of the unit cell, which will mean having more elements in the array to keep the area of the array constant.

More details about the EMF method derivation and calculations shown is this section can be found in [92], and in Appendix C.

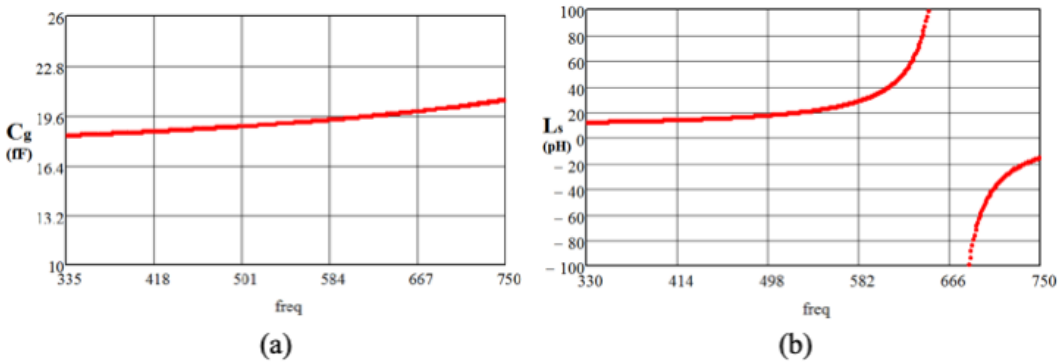



Figure 5.8: (a) Slot gap capacitance computed using Equation (5.1) and (b) Metal strip inductance computed using Equations (5.2) versus frequency (335 GHz - 750 GHz).

The equivalent circuit model for the capacitive grid array is shown in Fig. 5.9. In this model, electromagnetic propagation in free space and the Si substrate is represented as transmission lines with characteristic impedance equal to 377 Ω and 110 Ω, respectively. The free-space transmission line is terminated in a short circuit. During RF characterization (Section 5.7), the short termination will be achieved by a mirror (quasi-optical short circuit). The position of the mirror, and therefore the electrical length of the free-space transmission line, will be tuned to achieve the optimum phase shift for the array. The slot gap effect is represented as a gap capacitance $C_g$. The airbridge finger is represented as an inductance $L_F$. The varactor QVD is represented with its series resistance and depletion capacitance. The diode series resistance is determined through DC current-voltage measurements (refer to Table 2.4 in Chapter 2). A parasitic lumped capacitance $C_f$ is included to account for fringing fields near the airbridge finger (see Chapter 3 for a discussion on diode parasitics).

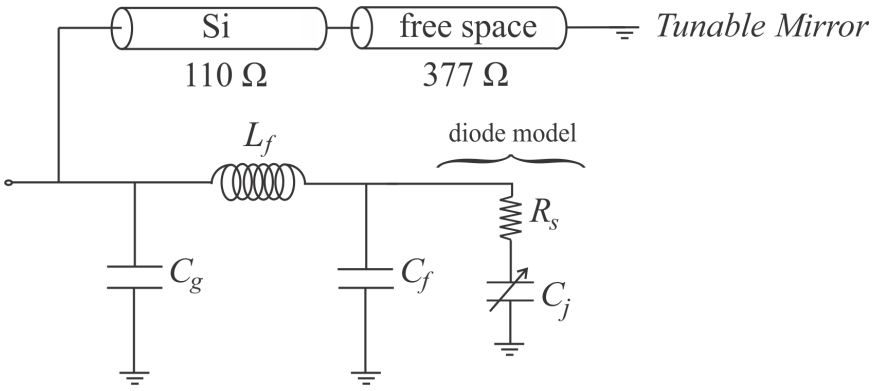



Figure 5.9: Equivalent circuit model for a unit cell.

### 5.2.3 HFSS Simulation Setup

In addition to the equivalent circuit model approach described above, an electromagnetic simulation of the diode array unit cell is performed using the software package HFSS. To reduce the computation time, only half of the array unit cell geometry is simulated, as shown in Fig. 5.10.

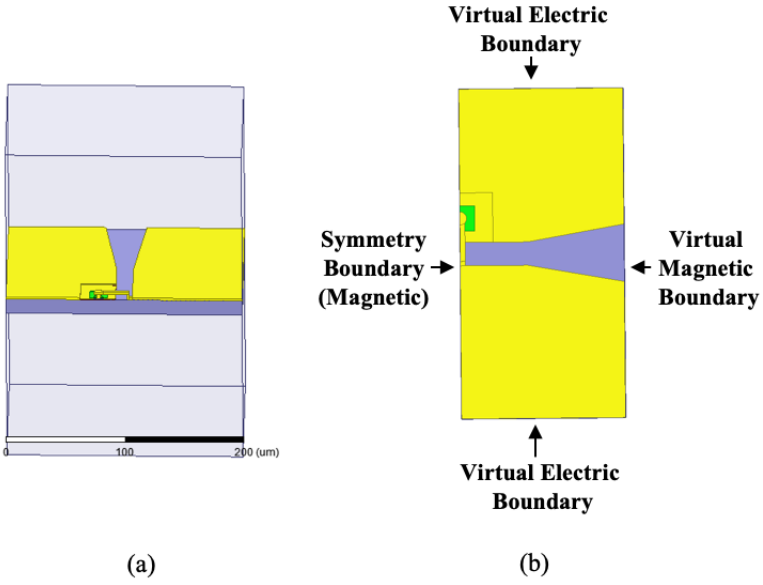



Figure 5.10: HFSS simulation setup (a) unit cell geometry (b) boundary conditions.

The boundary conditions are set to virtual electric and magnetic boundaries, as shown in Fig. 5.4 and 5.10(b). Note that the magnetic boundary,

which splits the diode geometry in half (see Fig. 5.10), is set as a symmetry H-boundary, with a port impedance multiplier equal to 0.5.

In this simulation, the EM waves are excited from two wave ports defined on the top and bottom of the air box surface, as shown in Fig. 5.11(a) and Fig. 5.11(b). An integration line corresponding to the E-field polarization of the incoming EM wave is defined for these two ports, which allows HFSS to calculate the port impedance based on the Zpi definition (calculated by HFSS from values of power and current). For these two wave ports, the solution is de-embedded to the top and bottom face of the silicon substrate. A third port is included (diode port) by making use of the coaxial probe method [95]. The coaxial probe technique consists of inserting a coaxial wave port at the diode junction in HFSS, making it accessible in a circuit simulator, and thus encapsulating all the parasitics in an S-parameter network. The setup for the third wave port is shown in Fig. 5.11 (c).

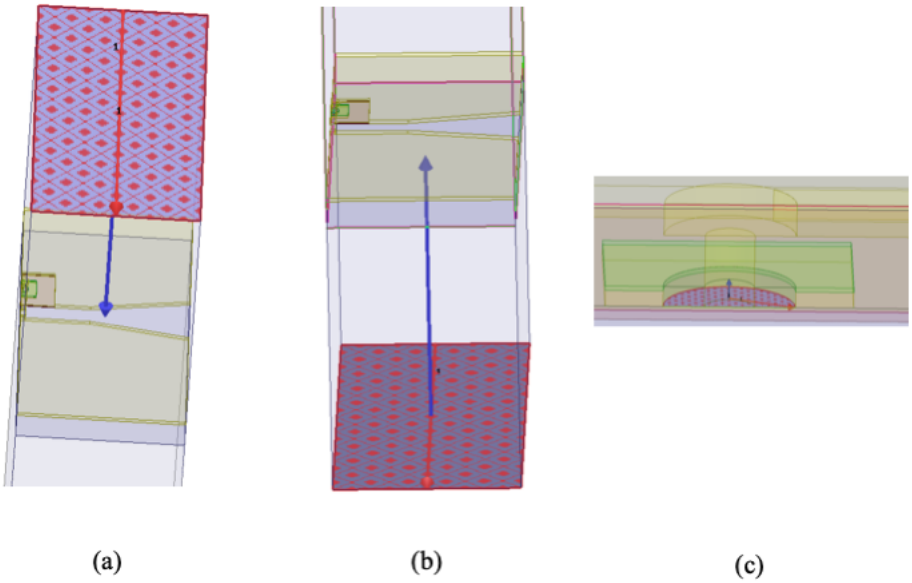



Figure 5.11: HFSS port excitation setup for (a) port 1 (free-space), (b) port 2 (free-space), and (c) port 3 (diode port).

The geometry shown in Fig. 5.10 is simulated in HFSS over the WR-5 frequency band (140 GHz - 220 GHz). The 3-port scattering parameter solution matrix is then imported to Keysight's Advanced Design System(ADS), where the diode circuit model can be added to the diode port, as shown in

Fig. 5.12. Also, free-space transmission lines are connected to the free-space ports to allow tuning of the air length.

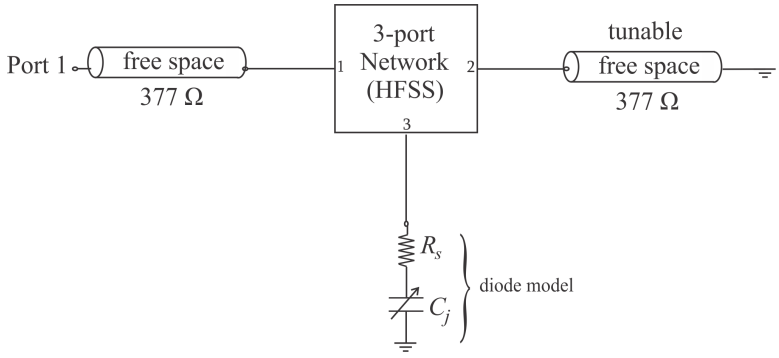



Figure 5.12: ADS simulation setup showing the 3-port S-parameter network obtained using HFSS. Free-space transmission lines are connected to port 1 and port 2 of the HFSS network. Port 3 is connected to the diode model.

### 5.2.4 Simulation Results

Fig. 5.13(a) shows a Smith chart plot of the simulated refection coefficient data over the full WR-5 (140-220 GHz) band for a zero bias 4 μm diameter QVD diode array based on the design outlined in Section 5.2.1. The diode zero bias junction capacitance is 20 fF using Equation 1.3 (Chapter 1) and the series resistance is 2.92 Ω based on the measured value in Table 2.4 (Chapter 2). The length of the free-space transmission line is fixed at 4.5°, which leads to the maximum phase shift. In Fig. 5.13(a), the circuit model is shown as a blue line, whereas the HFSS result is shown as a red dotted line. The value of the circuit elements $C_g$, $L_f$, and $C_f$ (shown in Fig. 5.9) are adjusted so that the circuit model and HFSS results are in close agreement. As such, the value of these parasitic elements are found to be 8.9 fF for $C_g$, 17.2 pH for $L_f$, and 2.7 fF for $C_f$. Fig. 5.13(b) plots the reflection coefficient data for the circuit and HFSS models at the same back short position (4.5°) versus bias from -6 V to 0.6 V.

A similar simulation is performed for the 2.4 μm diameter QVD diode array. Fig. 5.14(a) shows a Smith chart plot of the simulated refection coefficient data over the full WR-5 band (140-220 GHz) for a 2.4 μm diameter QVD diode array. The diode zero bias junction capacitance is 7 fF using Equation

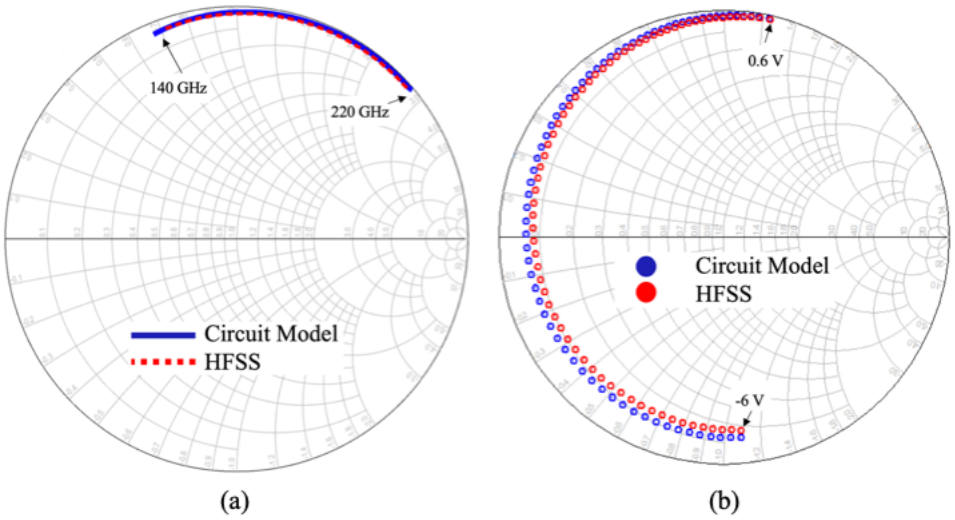



Figure 5.13: HFSS simulation reflection coefficient results (plotted on Smith charts) for 4 μm diameter QVD diode unit cell array: (a) zero-bias data versus frequency from 140-220 GHz, (b) data at 158 GHz vs bias from -6 V to 0.6 V.

1.3 (Chapter 1) and the series resistance is 7.00 Ω, based on the measured value in Table 2.4 (Chapter 2). The length of the free-space transmission line which leads to the maximum phase shift is fixed at 209°. In Fig. 5.14(a), the circuit model is shown as a blue line and the HFSS result is shown as a red dotted line. Fig. 5.14(b) plots the reflection coefficient data for the circuit and HFSS models at the same back short position (209°) versus bias from -6 V to 0.6 V.

By tuning the position of the mirror behind both the 4.0 μm and 2.4 μm quasi-vertical diode arrays, a phase shift can be obtained as the diode bias is swept from -6 V to 0.6 V. The next section describes the fabrication of these quasi-vertical diode arrays.

## 5.3 Array Processing

The fabrication of the quasi-optical diode arrays is based on the quasi-vertical diode process described in Chapter 2. The frontside (diode side) is fabricated using the steps outlined in Section 2.4. The backside is processed using the SOI process described in Section 2.6. The released thin (15 μm) silicon membranes contain the diodes, circuitry (such as the airbridge and the grid pattern), as

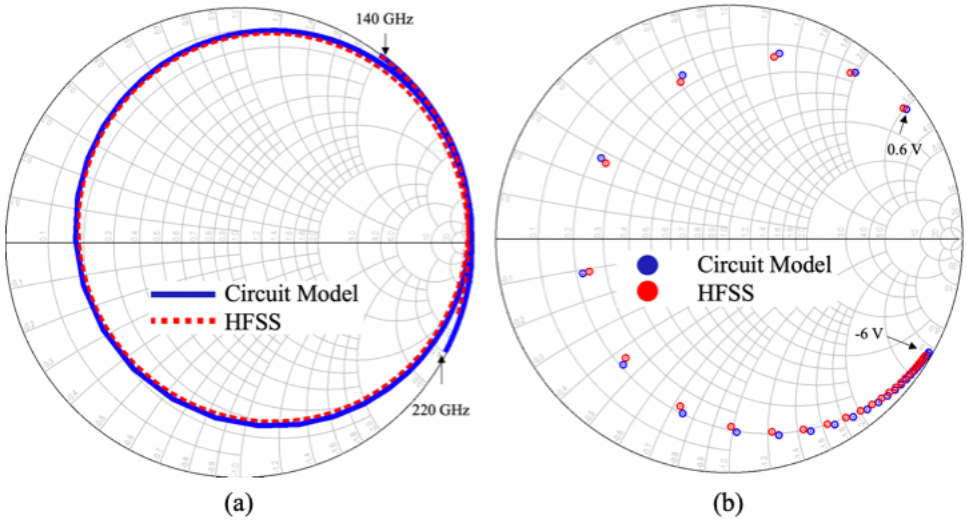



Figure 5.14: HFSS simulation reflection coefficient results (plotted on Smith charts) for 2.4 μm diameter QVD diode unit cell array: (a) zero-bias data versus frequency from 140-220 GHz, (b) data at 158 GHz vs bias from -6 V to 0.6 V.

well as the gold beam leads. The beam leads allow each array to be mounted on a carrier for DC and RF characterization. The design and fabrication of the carrier will be described in Section 5.4. An alternative backside process was also considered. Instead of etching the entire SOI wafer and releasing individual array circuits (SOI process), three arrays were fabricated on the same SOI wafer, and a Bosch deep silicon etch was used to etch a window only in the area directly beneath the array circuits. The advantage of this method is that it alleviates the need to fabricate a separate holder to mount the arrays, and that the arrays are all integrated on a large silicon frame that is easy to handle by hand. Nevertheless, the backside SOI approach was more successful, and will be described first (Section 5.3.1). Then, the backside silicon Bosch approach will be described (Section 5.3.2).

### 5.3.1 QVD Diode Fabrication with Backside SOI Process

The mask used to fabricate quasi-vertical diode arrays based on the backside SOI is shown in Fig. 5.15. The mask contains five 4.0 μm diameter single diodes, and four 2.4 μm diameter single diodes. The single diodes are used for DC characterization and troubleshooting after the front side is completed.

The single diodes are also released at the end of the backside processing steps. The mask also contains eight passive arrays (with either 100 or 36 elements), which are based on the passive structures discussed in Section 3.2. Finally, the mask contains seventeen active arrays (with either 100 or 36 elements), with both 4.0 μm and 2.4 μm diameter diode options.

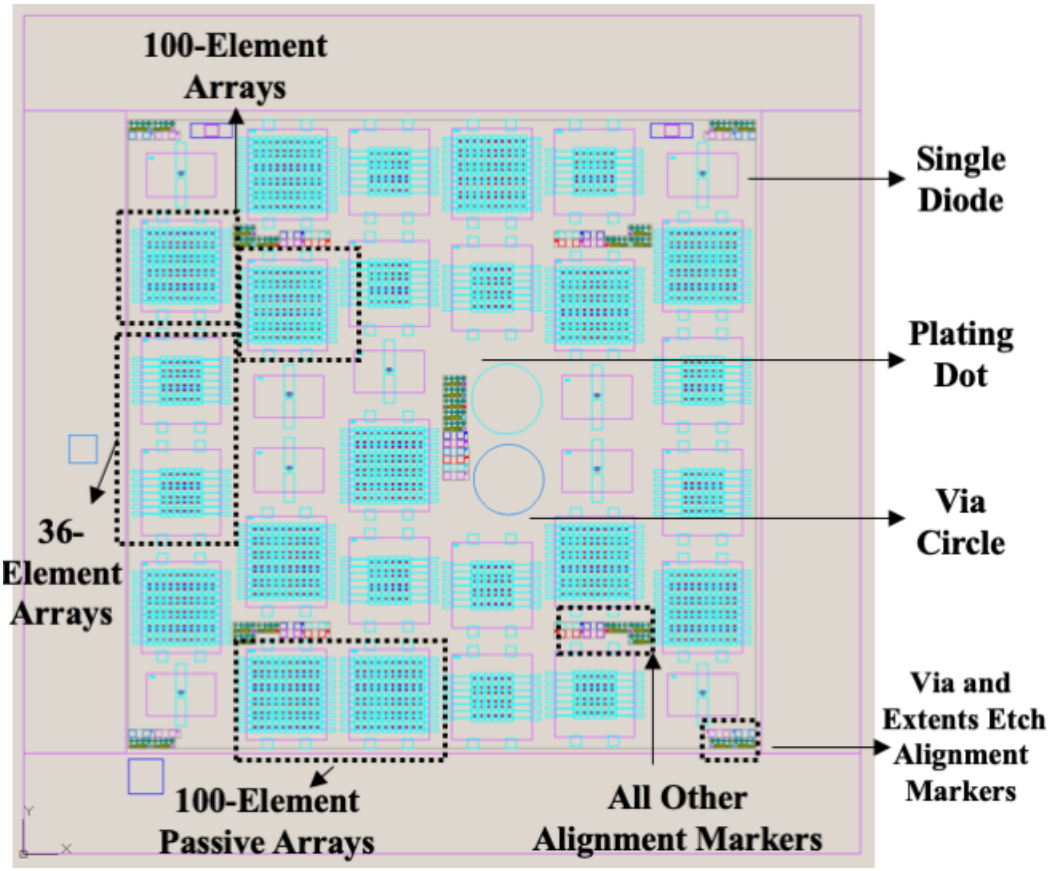



Figure 5.15: CAD drawing for the mask used to fabricate QVD membrane arrays.

The fabrication steps for processing the arrays based on the mask in Fig. 5.15 are summarized in Table 5.1. We starts with a 4-inch GaAs wafer with the new epitaxy (refer to Table 2.1), diced in 24 mm x 24 mm square-shaped pieces. The 4-inch SOI wafer is diced into 32 mm x 32 mm squares. Note that this SOI wafer has a 15 μm device layer, a 1 μm oxide layer, and a 300 μm handle layer.

This process involves six lithography steps: large mesa, small mesa, via

etch, sacrificial resist, plating, and silicon extents etch. The via and silicon extent lithographies are performed using the MJB4 tool, which has more travel range than the EVG aligner. Therefore, the alignment markers for these two steps are placed at the corners of the area of the mask populated with devices, as well as at the center of the mask (see Fig. 5.15). The remaining alignment markers are separated by a distance of 12 mm, which is the travel distance of the EVG's objective. The alignment tolerance between the various lithography steps is set to 7 μm for this mask.

Table 5.1: Summary of the quasi-vertical diode membrane array processing steps.

| **Step number** | **Step name** |
|---|---|
| 1 | Dicing the GaAs and SOI |
| 2 | Metal evaporation |
| 3 | Wafer bonding |
| 4 | GaAs handle removal |
| 5 | Large mesa lithography and etching |
| 6 | Small mesa lithography and formation |
| 7 | Via lithography and etching |
| 8 | Sacrificial resist lithography |
| 9 | Seed-layer sputtering |
| 10 | Plating lithography and plating |
| 11 | Seedlayer and photo-resist removal |
| 12 | Backside SOI process |

The ohmic metallization which consists of Ti(40 nm)/Pd(40 nm)/Au(100 nm)/Ti(20 nm) is deposited on the III-V surface using e-beam evaporation. The diode epitaxy is then bonded on the SOI piece using SU-8 as the bonding agent, as described in Section 2.3. Once bonded to the silicon substrate, the GaAs handle is removed in a nitric acid solution ($HNO_3$ : $H_2O_2$ : DI at 50 °C), followed by a slow citric acid etch ($C_6H_8O_7$ : $H_2O_2$ : DI at 50 °C). The sample is then immersed in hydrofluoric acid (HF) for 1 minute, which removes the AlGaAs layer, thus revealing the GaAs device layer field.

The diode mesa areas (called large mesas) are defined photo-lithographically using AZ-4210 positive photo-resist spun at 4000 rpm (revolutions per minute), yielding a resist masking layer thickness of 2 μm. The large mesas are then formed by a sequence of selective etches that stop on the silicon surface. A

wet etchant consisting of $H_2SO_4$ : $H_2O_2$ : DI (1:8:160) is used to remove GaAs in the areas between the final device mesas, at a rate of ∼350 nm/min. Following this, the exposed ohmic metal stack is removed using a combination of reactive ion etching (RIE), sputter etching, and wet chemical etching. The thin Ti layers are removed in a CHF3/SF6 RIE and the Pd with 10 seconds TFA (Transene gold etchant TFA) wet etch. The TFA must be diluted in DI (2:1). The thick gold layer is removed with an Ar sputter etch, followed by a brief potassium iodide wet etch. Since Ar sputter etching is used to remove the thick gold layer, back sputtering of the gold atoms on the resist, and eventually on the large mesa is inevitable. However, this etch sequence is carefully designed to substantially minimize this effect. Once the ohmic metal layers have been removed, the exposed SU-8 adhesive layer is etched using a CF4 RIE. Fig. 5.16 shows an SEM image of large mesas from a 100-element diode array.

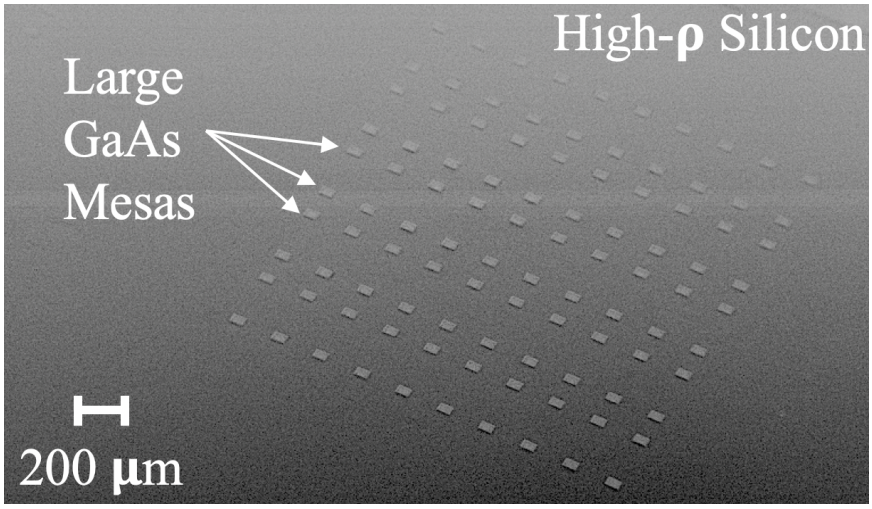



Figure 5.16: SEM image of a 100-element array's large mesas . The exposed layers are the GaAs device layers. The Ti/Pd/Au/Ti ohmic contact, which is bonded to silicon using SU-8, lies underneath the GaAs layers.

The final device mesas sit atop the ohmic metal pedestals. The mesas are defined by the same GaAs sulfuric acid based etch used during the large mesa step. Fig. 5.17 shows SEM images of device mesas for a 36-element diode array.

The remaining steps utilize standard lithographic patterning to form the

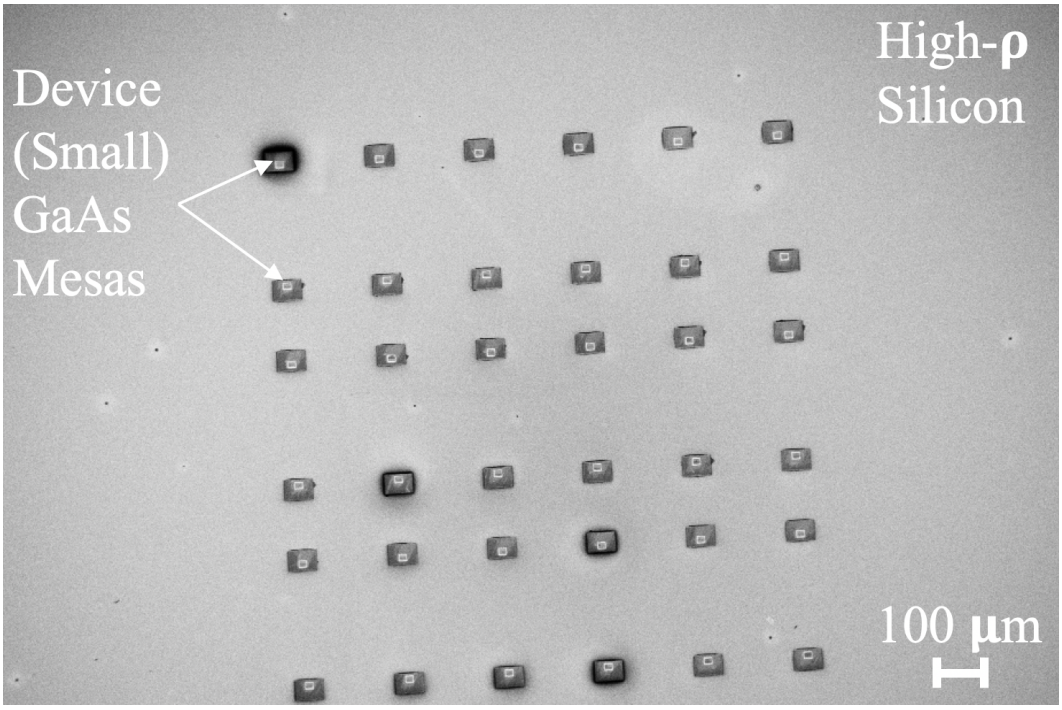



Figure 5.17: SEM image of GaAs device mesas on ohmic metal bonded to high-ρ silicon carrier.

anode, airbridge finger contact, ohmic contact overlay metallization, and other circuit features on the silicon surface. The plating dot shown in Fig. 5.15 allows us to make electrical contact during the plating procedure. Full details of these fabrication steps can be found in the process sheet located in Appendix D of this document. Fig. 5.18 shows a completed 36-element 2.4 µm quasi-vertical diode array. Each row is connected to a beamlead on either side.

Once fabrication of the diodes is completed (frontside), the silicon carrier to which they are bonded is micromachined to form an integrated chip tailored to the desired array chip geometry. Initially, the surface of the wafer with diode circuitry is attached to a sacrificial carrier using wafer-bond adhesive. Following this, the handle silicon layer of the SOI is removed through a combination of lapping and plasma etching. The buried oxide is then removed with a buffered oxide etch. At this point, the extent etch alignment markers formed during the via etch step are now visible and can be used to perform the final lithography step. In the final step, backside lithography defines the chip geometry, including integrated beamleads, and a silicon etch (Table 2.6) forms

the final 15 µm thick chips. Individual chips are then released by removing the sacrificial carrier. The details of the backside process for the array are included in Appendix B.

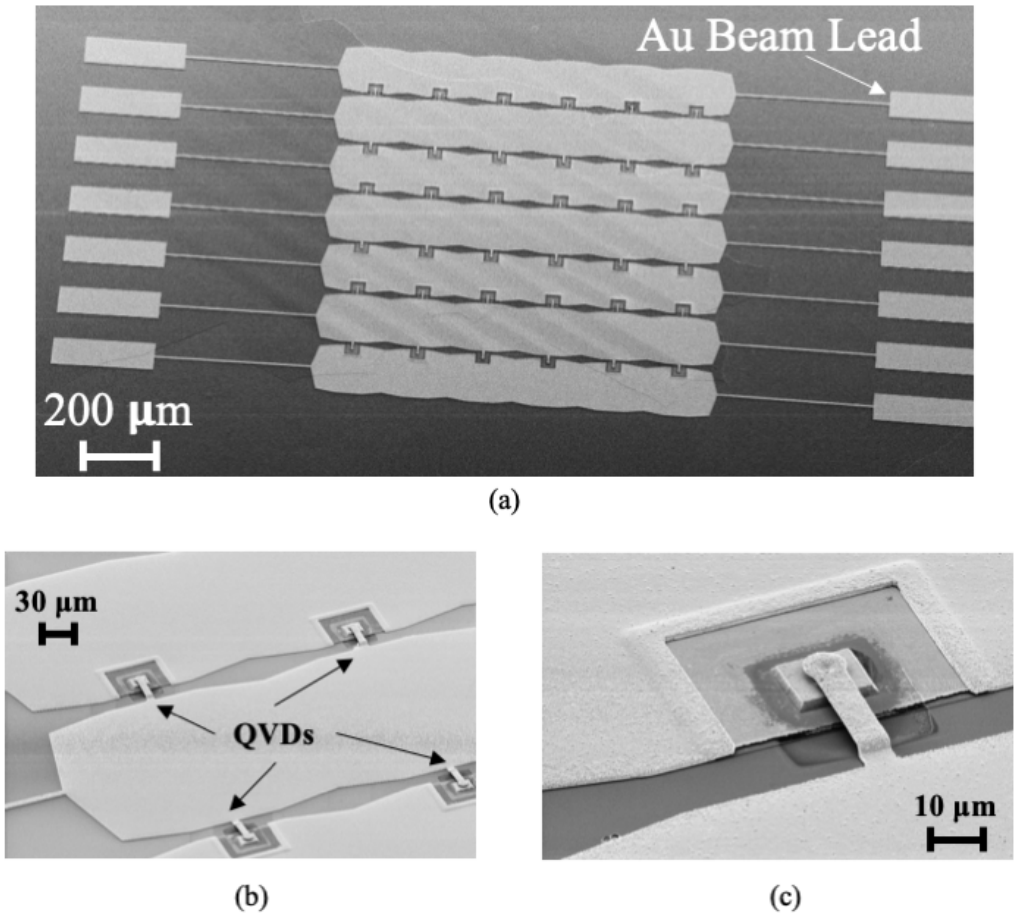



Figure 5.18: SEM image of completed 36-element diode array (a) entire array showing the beam leads connected to each row, (b) zoom-view into 4 diode elements, (c) close look at a single element from the diode array.

### 5.3.2 QVD Diode Fabrication with Backside Silicon Bosch Process

The mask used to fabricate quasi-vertical diode arrays based on the backside silicon Bosch process is shown in Fig. 5.19. The mask contains eight single diodes. The single diodes are used for DC characterization and troubleshooting

after the front side is completed. The mask also contains two passive arrays, which are based on the passive structures discussed in Section 3.2. Finally, the mask contains three active arrays. The rows in the array which correspond to the diode cathode contacts are connected to the outer ground of a long CPW line. All the rows in the array that correspond to the diode anode contacts are connected to the center conductor on the same CPW line. The diodes are therefore all connected in parallel. A method of biasing each individual row in the array was briefly considered, and therefore appears at the center of the mask (Fig. 5.19).

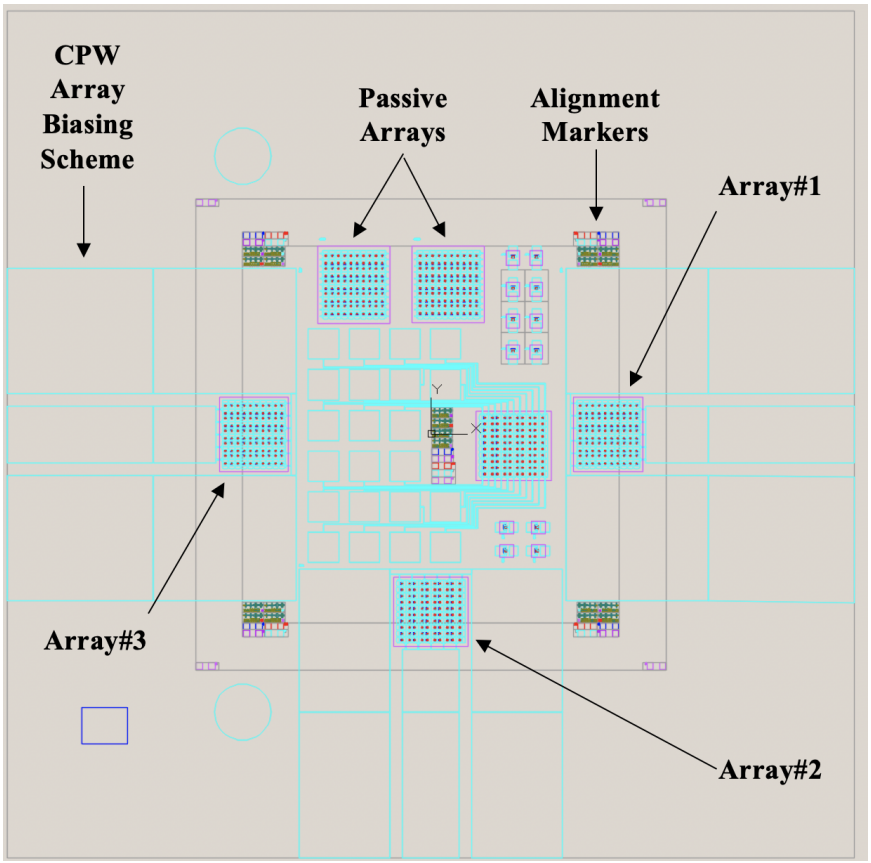



Figure 5.19: CAD drawing for the mask used to fabricate QVD Bosch arrays.

Bosch deep silicon etching can be used to etch a window only in the area directly beneath the array circuits, thus alleviating the need for releasing individual chips through the backside SOI process. This approach has two major disadvantages. First, the biasing circuit (shown is Fig. 5.19) is fabricated on

the same substrate, which takes up a lot of real estate on the wafer. Consequently, the number of arrays fabricated in each run is very small compared to the membrane diode approach (three in Fig. 5.19). Secondly, the biasing structure is fabricated simultaneously with the diode array. Therefore, modifications to the biasing scheme are impossible once the diodes are fabricated. Due to these disadvantages, we believe that the SOI backside process is a better approach compared to the backside Bosch for this application. However, the processing steps described in the next paragraphs could be of value to researchers in the future.

The fabrication steps for processing the arrays based on the mask in Fig. 5.19 are summarized in Table 5.2. The fabrication steps are almost identical to those of the membrane arrays. Therefore, we will only highlight in this section the elements of the process which are different.

Table 5.2: Summary of the quasi-vertical diode Bosch array processing steps.

| **Step number** | **Step name** |
|---|---|
| 1 | Dicing the GaAs and SOI |
| 2 | Metal evaporation |
| 3 | Wafer bonding |
| 4 | GaAs handle removal |
| 5 | Large mesa lithography and etching |
| 6 | Small mesa lithography and formation |
| 7 | Sacrificial resist lithography |
| 8 | Seed-layer sputtering |
| 9 | Plating lithography and plating |
| 10 | Seedlayer and photo-resist removal |
| 11 | Bosch etch lithography and etch |

We starts with a 4-inch GaAs wafer with the new epitaxy (refer to Table 2.1), diced in 20 mm x 20 mm square-shaped pieces. The 4-inch SOI wafer is diced into 27 mm x 27 mm squares. Note that this SOI wafer has a 15 μm device layer, a 1 μm oxide layer, and a 300 μm handle layer. The thickness of the handle layer is chosen to decrease the backside deep silicon etch time.

The frontside is processed according to the same steps described in the previous section (5.3.1), with the exception of the via etch step, which is omitted. Fig. 5.20 shows an SEM image of a completed Bosch array (frontside). The anode terminal rows of the array are connected to the center conductor of a

CPW line (Fig. 5.20), while the cathode terminal rows of the array are connected to the outer grounds (Fig. 5.20). All one hundred diodes are connected in parallel.

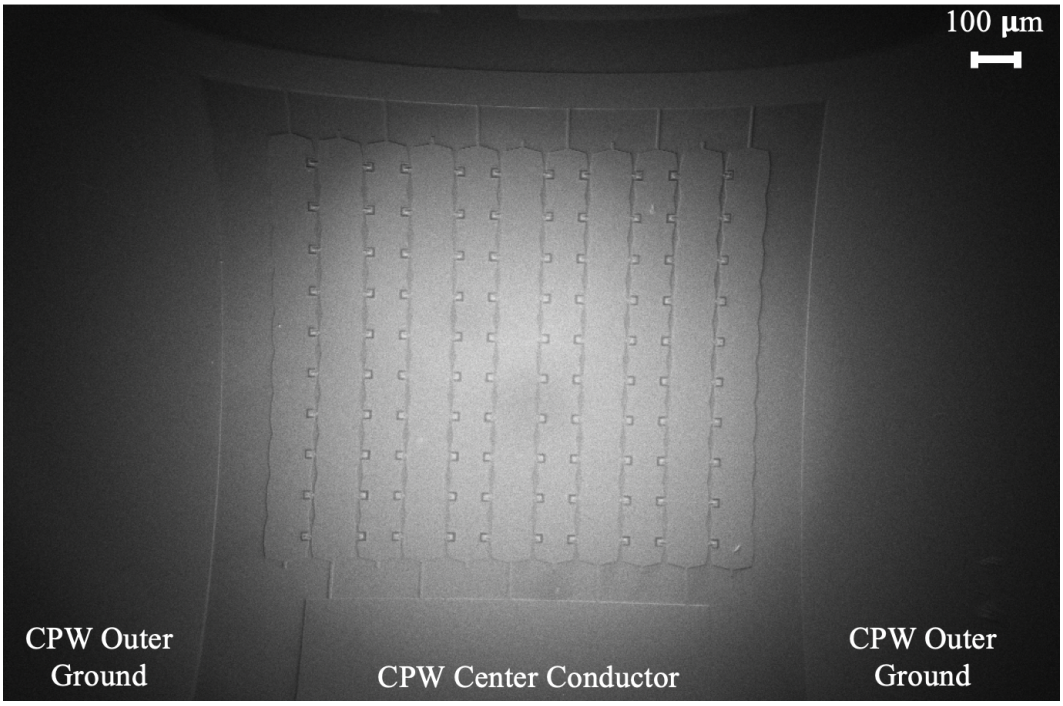



Figure 5.20: SEM image of a completed Bosch array (frontside). The anode terminal rows of the array are connected to the center conductor of a CPW line. The cathode terminal rows of the array are connected to the outer grounds. All 100 diodes are connected in parallel.

Once the frontside is completed, the backside can be processed using a deep silicon etch to form windows beneath the array circuits. First, we spin wafer-bond on the frontside to protect the diodes. Next, the SOI wafer is mounted on a sapphire carrier using L-grease. The backside of the SOI carrier is cleaned using a combination of HNA etch (HF/nitric/acetic acid) and solvents. After that, an SU-8 pattern is defined on the wafer during lithography. This pattern allows certain areas to be masked during the silicon etch, while other areas are exposed to the etch. The details of the backside Bosch lithography process can be found in Appendix E.

Following this step, the deep-silicon etch was performed at the University of Maryland, College Park's NanoCenter facility, using the STS Deep Reac-

tive ion etcher tool. The etch is designed to provide high aspect ratio etching of single crystal silicon using inductively coupled plasma (ICP) reactive ion etching (RIE). With the Advanced Silicon Etch (ASE) licensed Bosch process, hundreds of micrometers thick of microstructures can be obtained up to ~20:1 aspect ratio. By combination of alternate $SF_6$ etch and $C_4F_8$ protection (passivation) process cycles with ICP RIE, high etch rate and high directionality silicon etch is realized. The etch lasts 90 minutes with an etch rate of 3 µm/min. Fig. 5.21 shows an SEM image of a silicon window obtained using the Bosch etch. The window has dimensions of 2 mm x 2 mm. The depth of the etch is 300 µm.

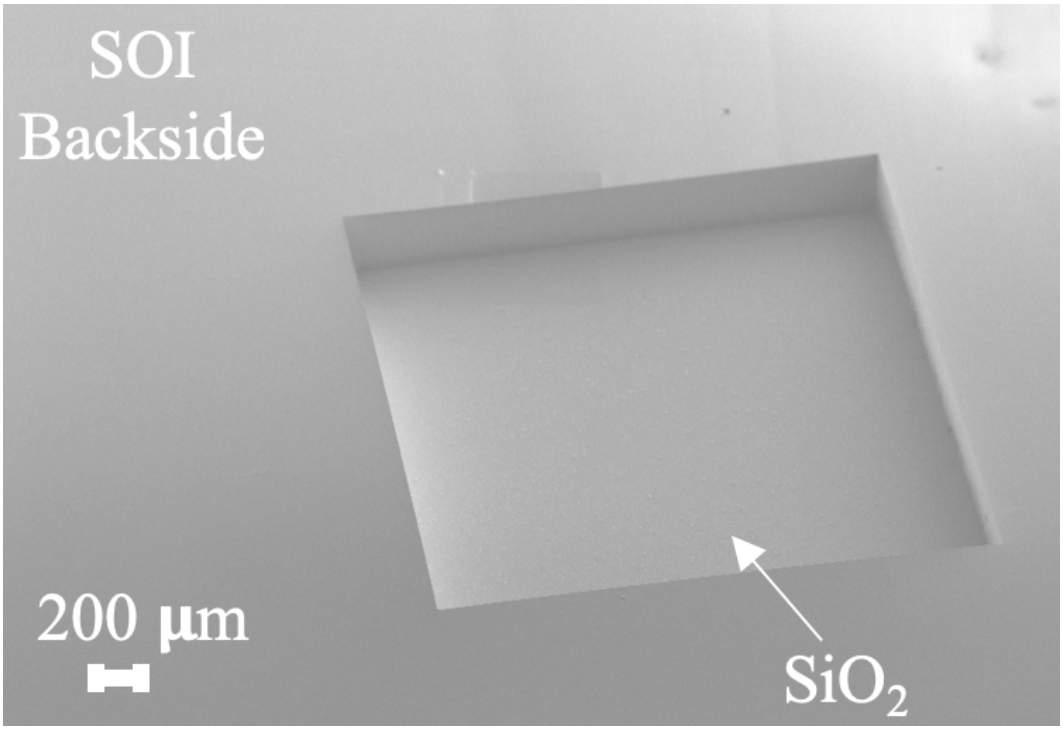



Figure 5.21: SEM image of the backside of the SOI wafer after deep silicon etching of a window.

Finally, the silicon dioxide layer is removed in BOE. The sample is then unmounted from the sapphire carrier and the waferbond is stripped in either TCE or waferbond remover. Fig. 5.22 shows a photograph image of a completed Bosch array.

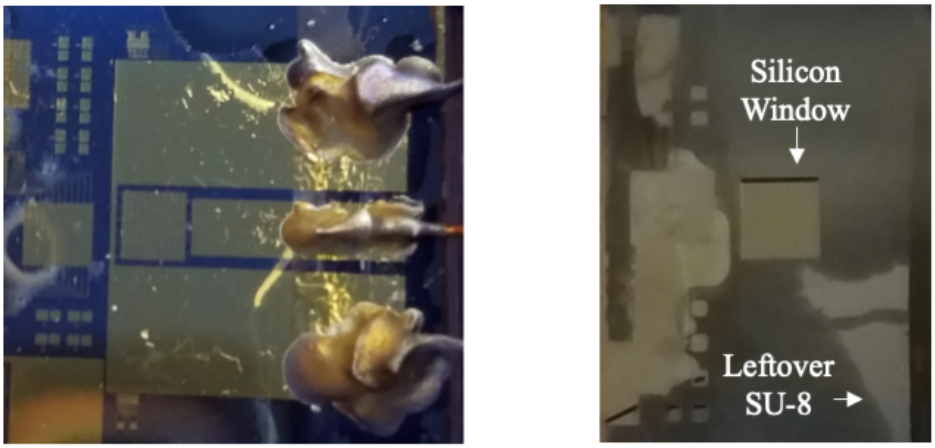



Figure 5.22: Photograph of a completed Bosch array (a) top view, (b) bottom view.

## 5.4 Fixture Design for Membrane Diode Arrays

### 5.4.1 Sapphire Holder

As mentioned in Section 5.3.1, membrane diode arrays fabricated using the backside SOI process need to be mounted on a carrier, prior to DC and RF characterization. The first approach to mount the arrays is to use a sapphire holder shown in Fig. 5.23. The sapphire is 430 μm thick and has lateral dimensions of 27 mm x 27 mm. At the center of the holder, a rectangular window is laser cut to allow the incoming electromagnetic energy (during RF quasi-optical tests) to propagate in free-space on either side of the array.

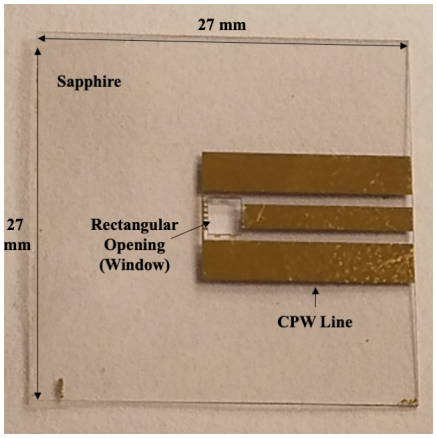



Figure 5.23: Photograph image of the sapphire holder.

Fig. 5.24 shows a diode array mounted on a sapphire holder. Gold pads (shown in Fig. 5.24(b)) are plated on the holder around the window opening to allow tacking of diode arrays' beamleads. These gold pads are then connected to a CPW line, which enables the biasing of the arrays.

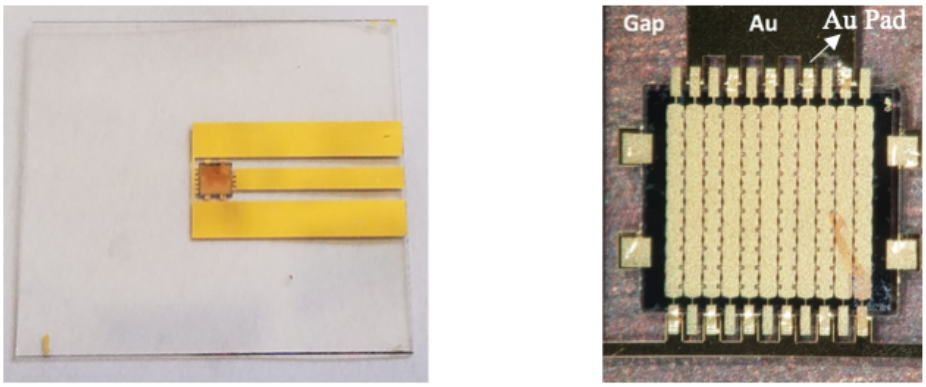



Figure 5.24: Photograph image of a 100-element diode array mounted on the sapphire holder.

Mounting the arrays using this approach has two disadvantages. First, due to the thickness of the sapphire, the minimum distance between the array and the tunable backshort is 430 μm, which is problematic as this limits the range over which the tunable mirror can be adjusted to optimize the performance of

the array. Second, without focusing optics, the size of the quasi-optical beam (at least 4.6 mm in diameter) is larger than the array. During quasi-optical RF characterization, we observed losses from the aperture in the sapphire (not observed on plain sapphire wafers) that is likely due to diffraction effects, as well as unwanted reflections from the large CPW line, that cannot be calibrated out of the measurement. For these reasons, a second scheme for mounting the membrane arrays was investigated, using a thin quartz substrate.

### 5.4.2 Quartz Holder

The second approach for mounting the membrane arrays is to use a thin (260 μm) quartz holder (shown in Fig. 5.25). The holder has lateral dimensions of 27 mm x 27 mm.

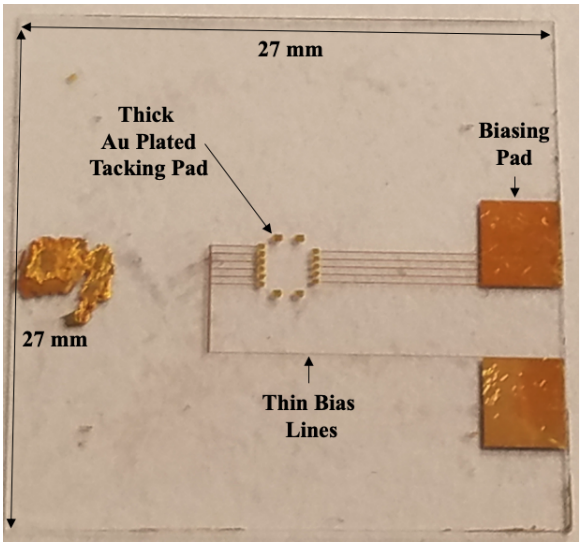



Figure 5.25: Photograph image of the quartz holder.

The quartz holder does not use a CPW line as a biasing scheme. Instead, narrow gold lines (30 μm in width) connect the rows of the array to two biasing pads (shown in Fig. 5.25), which are placed far from the location of the array to avoid interfering with the measurement. The quartz array holder does not have a laser cut window to avoid the issues described in Section 5.4.1. Instead, thick (25 μm) gold pads (Fig. 5.26) are plated, which are used to tack the array's beam leads. Fig. 5.26 shows a photograph image of a 36-element diode

array mounted on the quartz holder. The processing steps for fabricating the quartz holder are detailed in Appendix F.

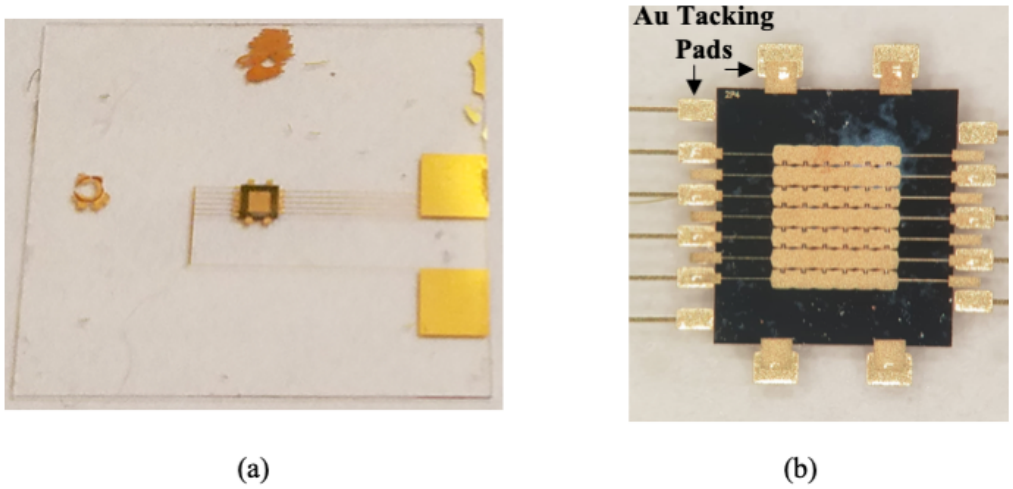



Figure 5.26: Photograph image of a 36-element diode array mounted on the quartz holder.

The RF performance of the array is re-simulated to account for the quartz holder. The EMF method's estimate for the grid capacitance does not change since its value depends strongly on the fields in the silicon substrate near the slot gap of the array. The value of the finger inductance is adjusted to 22 pH. In the equivalent circuit model (refer to Fig. 5.9), a transmission line with characteristic impedance equal to 193 Ω representing propagation of the TEM electromagnetic energy in the quartz is inserted between the silicon and free-space transmission lines. In HFSS, a 260 μm thick quartz material is added to the model geometry (refer to Fig. 5.10(a)).

The simulation is performed for the 4.0 μm diameter QVD diode array which incorporates the quartz substrate. Fig. 5.27(a) shows a Smith chart plot of the simulated refection coefficient data over the full WR-5 (140-220 GHz) band for a 4.0 μm diameter QVD diode array. The length of the free-space transmission line is fixed at 97°, which leads to the maximum phase shift.

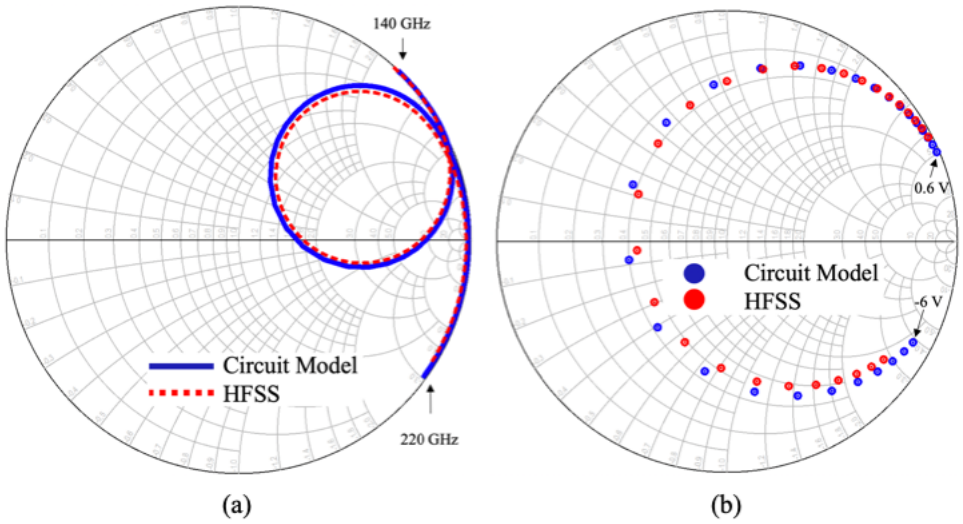



Figure 5.27: HFSS simulation reflection coefficient results (plotted on Smith charts) for 4.0 μm diameter QVD diode unit cell array which incorporates the quartz substrate: (a) zero-bias data versus frequency from 140-220 GHz, (b) data at 158 GHz vs bias from -6 V to 0.6 V.

In Fig. 5.27(a), the circuit model is shown as a blue line, whereas the HFSS result is shown as a red dotted line. Fig. 5.27(b) plots the reflection coefficient data for the circuit and HFSS models at the same back short position (97°) versus bias from -6 V to 0.6 V.

## 5.5 Robustness Assessment

A major limiting factor for prior implementations of diode arrays was the fabrication processing yields (Section 5.1). As discussed in Chapter 2, the new process for fabricating quasi-vertical diodes on silicon substrates alleviated many issues pertaining to the ohmic contact formation, as well as delamination and GaAs fracturing which occurs after the bonding/thinning process. The assessment of the new process described in Chapters 2 and 3 was done based on a fabrication run of discrete probable diodes (Sections 2.4, 2.5, and 3.1), and processing of a frequency quadrupler chip which integrated 18 diodes (Sections 2.6 and 3.3). In contrast, the diode arrays discussed in this chapter integrate up to one hundred elements in each circuit. This large level of integration allows us to further investigate the robustness of the process by addressing

issues that only arise in such a context.

The membrane diode arrays, fabricated using the processing steps outlined in Section 5.3.1, are inspected visually under an optical microscope and using a scanning electron microscope. Based on this inspection, 95% of the diodes present on the mask had the visual characteristics of a successfully fabricated quasi-vertical diode, which include lithography alignments within the 7 μm mask tolerance, well defined anodes and airbridges, and smooth plating (<100 nm surface roughness) of the grid pattern. The single diodes present on the wafer were also DC characterized and exhibited the low series resistance and ideality factor characteristics summarized in Table 2.4 (Section 2.5 in Chapter 2).

Nevertheless, 5% of the diodes on the mask were short-circuited, as illustrated in Fig. 5.28. The anode finger contacted the ohmic metal contact, as opposed to contacting the device mesa, which was unintentionally etched away. A possible explanation for this phenomenon is the sensitivity of the process to the Pd etch in the Transene gold etchant (TFA) which occurs during the large mesa formation step (refer to Chapter 2). This etch can lead to significant lateral undercutting of the ohmic metal's gold and palladium films. The exposed metals could then lead to the erosion and accelerated galvanic etching of the device mesas, which has been observed in industrial manufacturing of GaAs transistors [96].

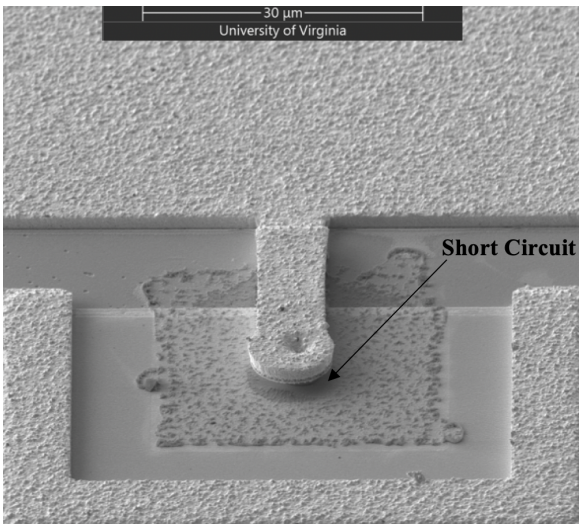



Figure 5.28: SEM image of a short-circuited diode array element.

After mounting the array to the quartz carrier, all the diodes present in the array are connected in parallel. If one of the 100 diode elements is shorted, the entire array is DC shorted. For low frequency diode applications, where the physical dimensions of the diodes are large, short-circuited diodes can be removed from the circuit using a tweezer or a soldering iron tip. These solutions, which are commonly used in PCB circuits, are clearly impractical for submillimeter-wave quasi-vertical membrane diodes.

To address the issue of the shorted diodes, focused ion beam (FIB) milling was used to make a small cut across the diode airbridge finger, thus disconnecting the faulty device from the other diodes in the array. A Helios UC G4 Dual Beam FIB-SEM tool was used for this purpose. The ion source consisted of positively charged gallium ions. The ion beam was accelerated by 30 KV, and the beam current was adjusted to 790 pA. Fig. 5.29 shows the resulting FIB gallium (Ga) cut on a shorted QVD diode array element.

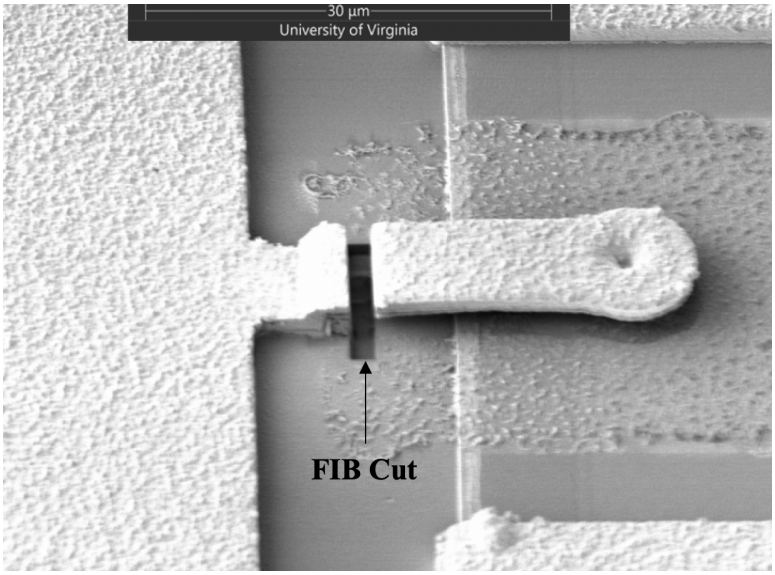



Figure 5.29: SEM image of a gallium FIB cut on a shorted QVD.

After mounting the arrays on the quartz holder, SEM inspection, and FIB ion milling of the faulty devices, the arrays are now ready for DC I-V characterization.

## 5.6 Array DC Characterization

Current-voltage (I-V) characterization of the quasi-vertical diode array is performed using a Keithley 236 source-measurement unit. Fig. 5.30 shows a typical DC characteristic on a logarithmic scale for a 36-element 2.4 μm diameter quasi-vertical diode array. Also plotted on Fig. 5.30 is a typical DC I-V curve for a single 2.4 μm diameter quasi-vertical diode, which was measured and presented in Chapter 2 (Table 2.4). Fitting of the measured current-voltage characteristic provides estimates of the substrate resistance, ideality factor, reverse saturation current, and series resistance provided in Table 5.3. For comparison purposes, Table 5.3 also lists the diode parameters for the single diode.

At bias levels below the diode turn-on voltage ($V < 0.3$ V), the I-V characteristic is dominated by the silicon substrate, which contributes a leakage resistance of $\sim 250$ kΩ . The substrate resistance is noticeable in the dc current-voltage characteristic, but is usually inconsequential compared to the typical diode impedance at submillimeter-wave frequencies [24].

After the diode turn-on voltage, the I-V characteristic is dictated by the diode equation. The ideality factor found through fitting for the diode array is 1.21, which is almost identical to the ideality factor for the single diode (1.26). Note from Fig. 5.30 that the array current is more than an order of magnitude larger than that of the single diode, indicating that most of the array's constitutive diode elements are operational. The reverse saturation current for the array is 2.11 pA, and 0.093 pA for the single diode.

At high bias levels, the IV curves are dominated by the series resistance. The plots begin to deviate from the expected scaling, which results from differences in series resistance [23]. The array has a series resistance of 10.76 Ω, while the single diode has a resistance of 7 Ω. The difference in series resistance is likely due to the additional resistance from the very thin and long bias lines, used in the quartz mount to connect the array to the bias pads (see Fig. 5.25). Nevertheless, this diode array, even when mounted on the quartz carrier, has a series resistance which is six times lower than that of the diode array implemented by Hawasli in 2013 [23]. The diode array's breakdown voltage is measured under reverse bias and found to be $\sim 9.5$ V. The next section will

present the quasi-optical RF characterization of the array.

Table 5.3: Extracted DC parameters for a 36-element 2.4 μm diameter quasi-vertical diode array, compared to the extracted DC parameters of a single 2.4 μm diameter diode.

| | Substrate Resistance | Ideality factor | Resistance | Saturation current |
|---|---|---|---|---|
| Diode array | 266 kΩ | 1.21 | 10.76 Ω | 2.11 pA |
| Single diode | 291 kΩ | 1.26 | 7.00 Ω | 0.093 pA |

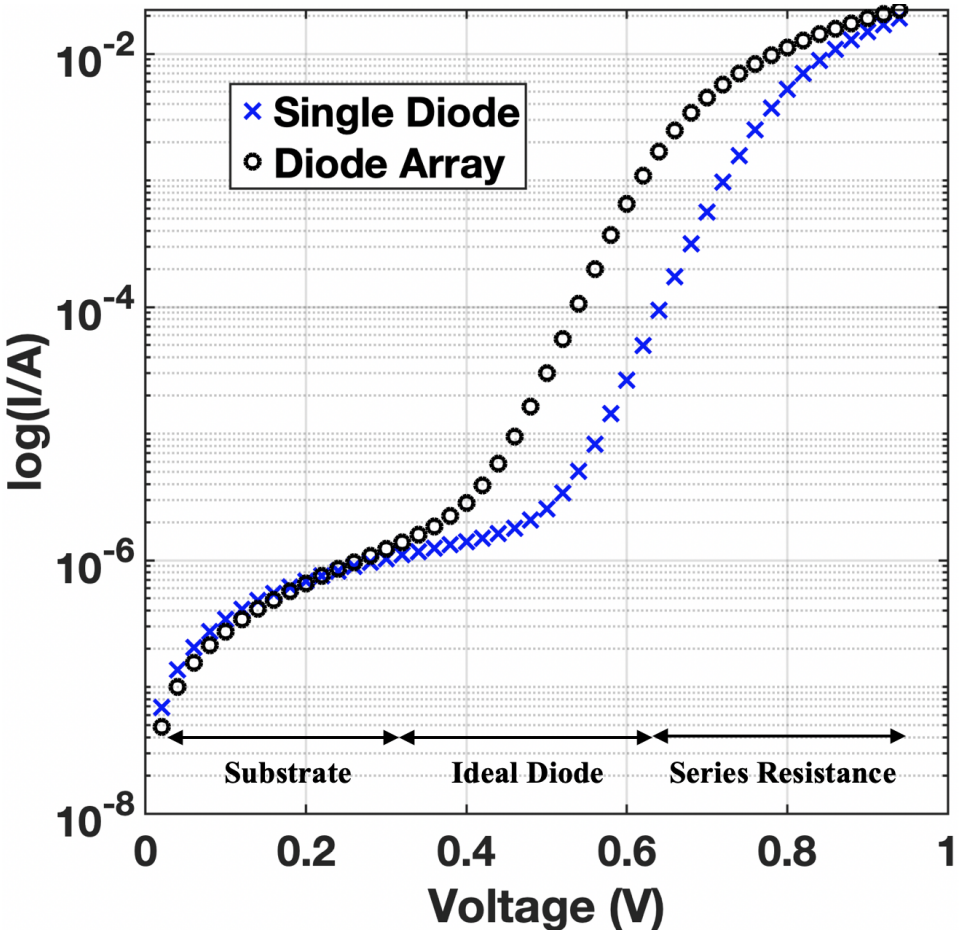



Figure 5.30: Measured current-voltage characteristic of: a 36-element quasi-vertical diode array with 2.4 μm diameter anode (black circle) and a single 2.4 μm diameter anode diode (blue X).

## 5.7 RF Characterization

### 5.7.1 Quasi-Optical Setup

The reflection coefficient of the diode array is measured in the WR-5 frequency band using a ZVA-40 vector network analyzer and a WR-5 VDI extender. As shown in Fig. 5.31, a conical horn antenna is used to transmit the electromagnetic energy to the array. The horn antenna is also used to receive the reflected signal back to the extender and VNA. A 90 degree H-plane bend is used to orient the path of the electromagnetic energy in a direction normal to the array assembly, which is setup on an optical table. The array, which is tacked on the quartz fixture, is mounted on a 3D printed holder. The holder is affixed to a lens holder that is positioned on an XYZ translation stage. An adjustable mirror, which is also set-up on an XYZ translation stage, is placed behind the array assembly. Needle probes are used to apply voltage to the array. The array biasing is performed using a Keithley 236 source-measurement unit.

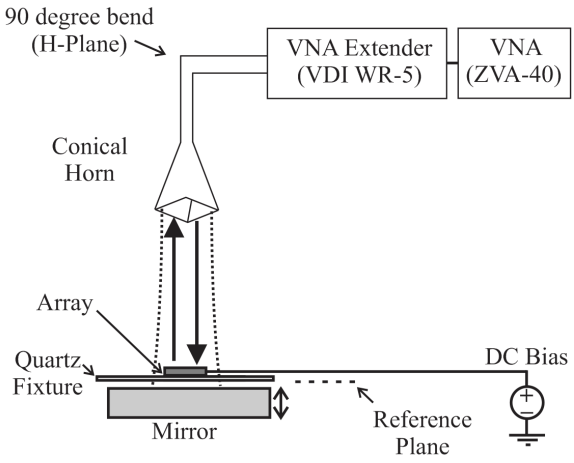



Figure 5.31: Diagram of the experimental setup used to characterize the quasi-vertical diode array. A Chanzon high power LED chip and a Quarton laser module (VLM-650-01 LPA) are used to align the setup.

### 5.7.2 3D Printed Holder

A mounting structure was required to properly measure the diode array in free-space. As mentioned in previous sections, the array was mounted to a

quartz carrier of regular 27 mm square shape. However, the quartz carrier was too thin and brittle to be handled directly. A holder was designed and 3D printed in-house by Sauber using a Prusa Research MKIII MMU2 model; and served as a more robust way to handle the diode array. Fig. 5.32 shows a CAD drawing of the 3D printed holder, which has dimensions of 40 mm x 75 mm x 5 mm. Reliefs are added to the carrier feature to allow easy installation and removal of the quartz.

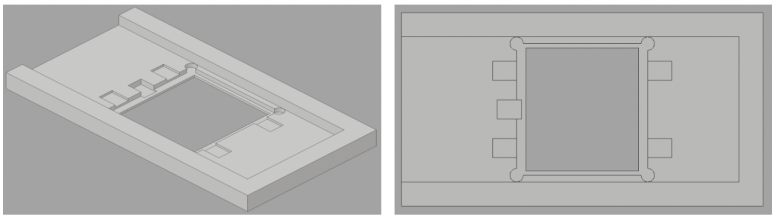



Figure 5.32: CAD drawing of the 3D printed array holder designed to be mounted on a lens holder: (a) tilted view, (b) top view.

An alternative holder designed to be mounted directly (without the lens holder) using a threaded hole is shown in Fig. 5.33. It has dimensions of 40 mm x 40 mm x 5 mm. This holder is designed for optical setups that use focusing optics, which require the placement of the array to be in closer poximity with respect to the focusing mirrors than the holder in Figure 5.32 allows. As biasing using needle probes is not possible in this case, hard contacts are soldered using an indium-silver mixture (90%-10%) to the quartz gold pads and then epoxied through vias on the right of the 3D printed holder.

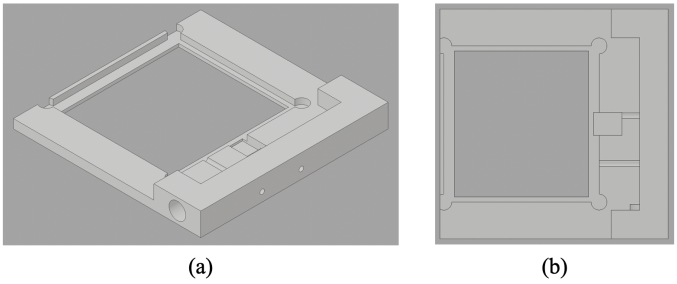



Figure 5.33: CAD drawing of the alternative 3D printed array holder design: (a) tilted view, (b) top view.

### 5.7.3 Calibration

Before useful measurements can be made with the quasi-optical setup, calibration is used to remove the unwanted systematic errors associated with the measurement system [97]. The system must be calibrated by measuring a set of known standards. Delaying the back short mirror (placed 2 cm away from the horn) by known distance increments provides the standards. Note that a piece of microwave absorber was placed around the horn antenna to reduce undesirable backscattered reflections and therefore improve the quality of the calibration. Five delay shorts with delay increments of 130 µm are used as standards. As more standards than necessary are used, the calibration is overdetermined. As a result, an improvement in estimation of the error coefficients of the system can be achieved compared to using a minimum set of three [97]. All the algorithms and calculations used to correct the raw data have been made with the open-source python module scikit-rf [97]. A calibrated measurement of the one-port calibration standards is shown on a Smith chart in Fig. 5.34. The calibration shown in Fig. 5.34 results in a measurement uncertainty of ± 0.4 dB in magnitude and ± 3 degrees in phase.

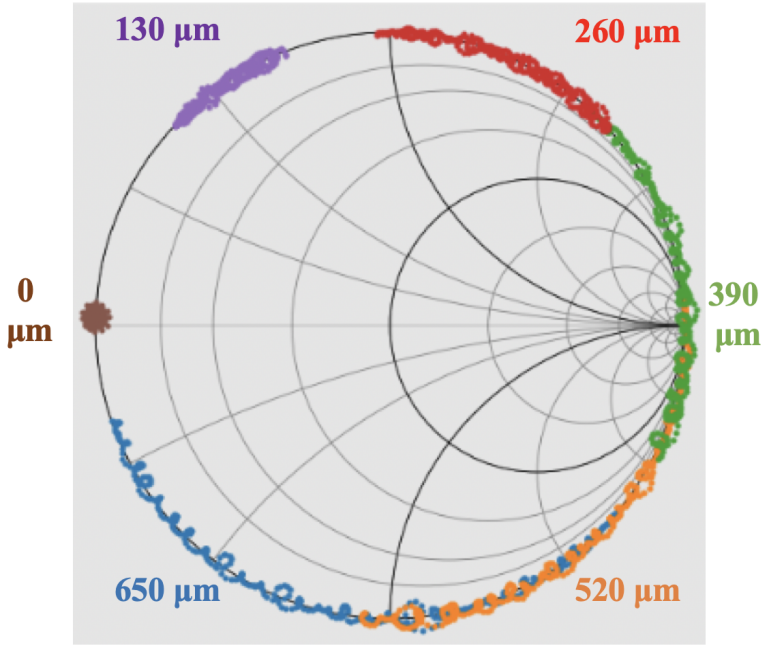



Figure 5.34: Measurement of the corrected system calibration standards from 140-220 GHz shown on a Smith chart.

### 5.7.4 Setup Verification

To verify the measurement setup, a high-resistivity silicon substrate is characterized using the setup shown in Fig. 5.31. Fig. 5.35 shows the magnitude and phase of the measured reflection coefficient for a high-resistivity silicon substrate of thickness 512 µm. The measured data is shown as a blue line and the circuit model is shown as a red dashed line.

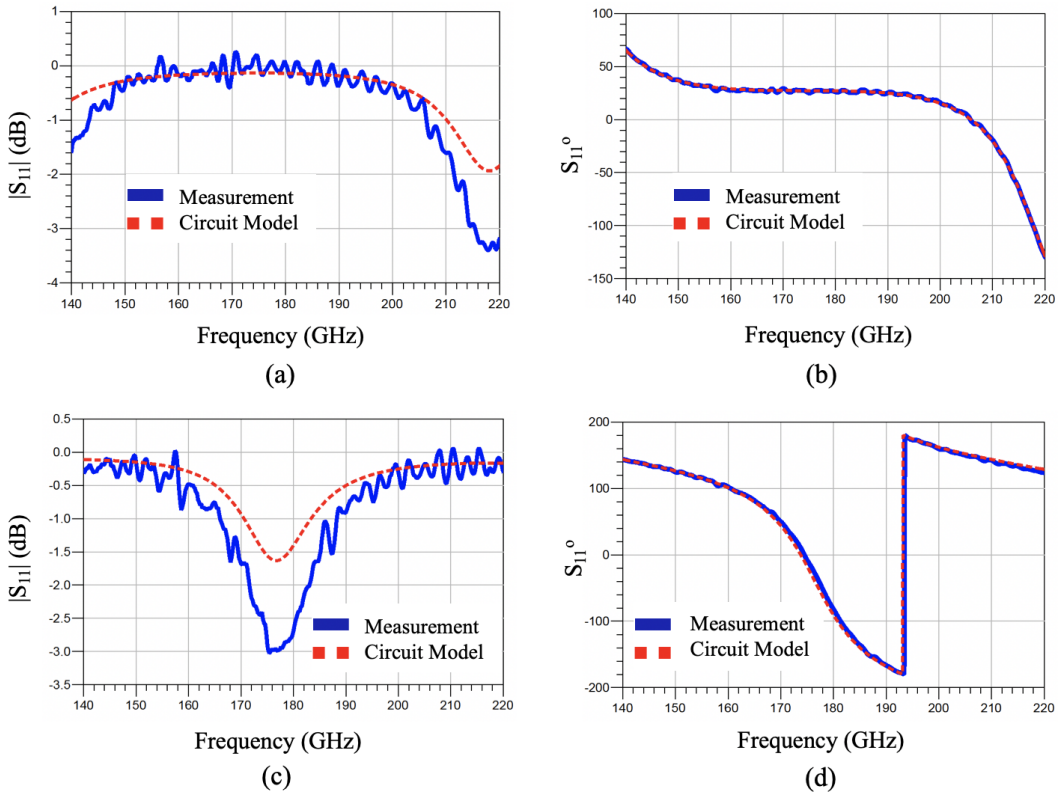



Figure 5.35: Measurement of the reflection coefficient of a high resistivity silicon substrate: (a) magnitude with no air gap, (b) phase with no air gap, (c) magnitude with 72° air gap, (d) phase with 72° air gap.

In Fig. 5.35(a) and Fig. 5.35(b), the sample is placed in direct contact with the backshort mirror. In Fig. 5.35(c) and Fig. 5.35(d), the substrate is mounted on the 3D printed holder and the mirror is placed 72° away from the silicon sample. The phase for the measurement and the circuit model are in very good agreement. From the measurement, we extract the loss tangent of this silicon sample to be equal to 0.009. The discrepancy in the magnitude of the reflection coefficient is likely due to diffraction losses, which increase

as the mirror is placed further away from the sample. The final section of this chapter presents the quasi-optical characterization of a 100-element quasi-vertical diode array with 4.0 μm diameter anodes.

### 5.7.5 Diode Array Characterization

The active array is characterized using the setup shown in Fig. 5.31. The backshort mirror is adjusted by increments of 45 μm to find the position that leads to the maximum reflection coefficient phase shift offset between the two diode array operating bias points of 0 V and -6 V. A maximum phase shift of 30° was measured for a mirror offset of 90° (416 μm). Fig. 5.36 shows the magnitude and phase, at this mirror position, of the diode array's reflection coefficient. As seen in Fig. 5.36, the maximum phase shift of 30° occurs at 158.6 GHz.

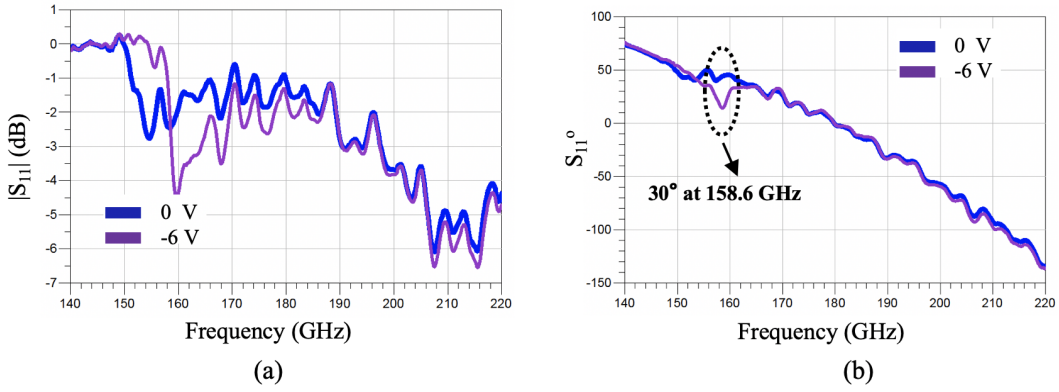



Figure 5.36: Measurement of the reflection coefficient of the diode array for a mirror position of 93° (430 μm) at 0 V (blue curve) and -6 V (purple curve): (a) magnitude, (b) phase.

The reflection coefficient measurement data are modeled using the equivalent circuit model shown in Fig. 5.37. In this circuit model, a free space transmission line represents the air distance between the position of the sample and the reference plane (defined during the calibration procedure). As seen in Fig. 5.36(a), a substantial amount of power is lost, up to 4 dB at 160 GHz and 6 dB at 210 GHz. The frequencies where this loss occurs correspond to the resonant frequencies of the grid [92]. In [92], Weikle postulated that the loss mechanism depended primarily on the grid structure since the capac-

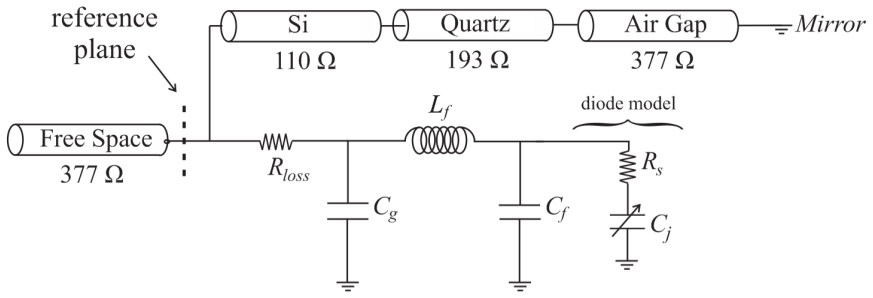



Figure 5.37: Equivalent circuit representation used to model the diode array measurement.

itive grid measurements that he conducted showed significantly higher losses than those of the inductive grids. As such, the losses observed in the diode array measurements probably arise from power coupling into transverse modes which propagate along the horizontal metal lines. In addition, losses could also be due to optical mechanisms, such as diffraction and mirror misalignments, which were observed while measuring the high resistivity silicon piece (Section 5.7.4). As was done in [92], modeling this loss mechanism was attempted by including a resistor to the grid equivalent model, as shown in Fig. 5.37.

The value of the loss resistance $R_{loss}$ is adjusted to a value of 16 Ω to fit the measured data with the circuit model. Fig. 5.38 compares the measured and modeled zero-bias responses for the optimum mirror position of 90° (416 μm). In this figure, the measured data is shown as a blue curve and the model as a dashed line. Fig. 5.39 shows a Smith chart plot of the measured reflection coefficient data of the array at 158.6 GHz for the full range of voltage bias points (0 V, -1 V, -2 V, ..., -6 V). The circuit model response is shown in black circles. As shown in both Fig. 5.38 and 5.39, the equivalent circuit model captures the behavior of the array. A better understanding of the loss mechanisms is needed to develop a more accurate circuit model and design arrays with improved performances.

## 5.8 Conclusion

Diode arrays were designed, fabricated, and characterized for the first time using the quasi-vertical diode on silicon process. To test the arrays, a quartz

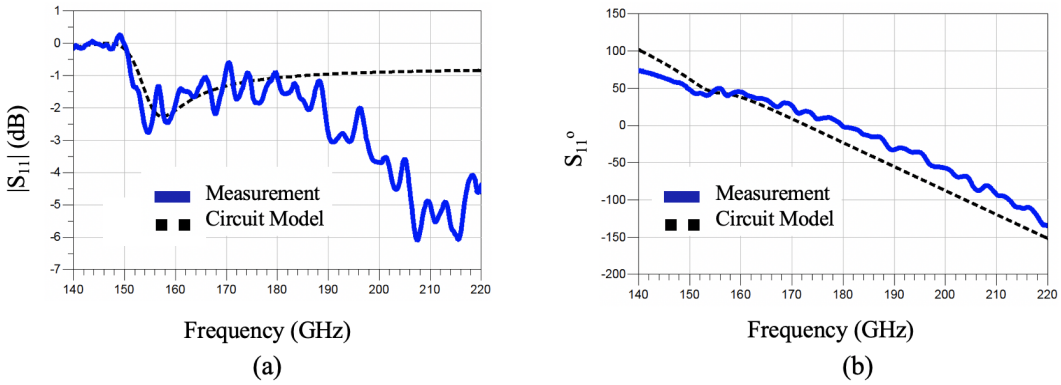



Figure 5.38: Measurement and modeled reflection coefficient response of the diode array for a mirror position of 90° (416 µm) at 0 V: (a) magnitude, (b) phase.

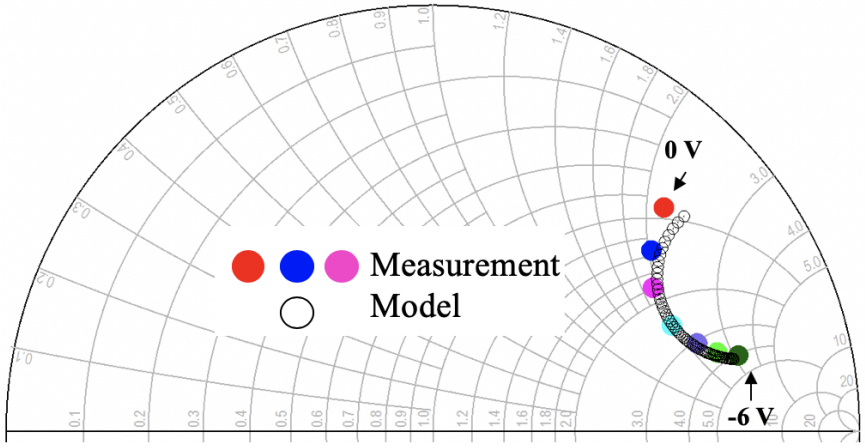



Figure 5.39: Response of the diode array as a function of bias voltage.

fixture was designed, which does not interfere with the measurement of the arrays. Furthermore, the issue of short circuited diodes was addressed by using focused ion beam milling.

The array has a low DC series resistance value of 11 Ω, which is less than the series resistance of the array previously implemented by Hawasli (58 Ω) [90]. Also, a reflection coefficient phase shift of 30° was measured quasi-optically, which is more than the previously measured phase shift of 20° [90].

A better understanding of the loss mechanisms in quasi-optical diode grids is necessary to ensure that the diode arrays can achieve their optimum performance. Fig. 5.40 shows the predicted reflection coefficient of the diode

array, based on the model shown in Fig. 5.37 and circuit element values found from fitting the measured data, when the loss resistor $R_{loss}$ is not present. The predicted phase sweep could enable many applications such as sideband generation and beam steering.

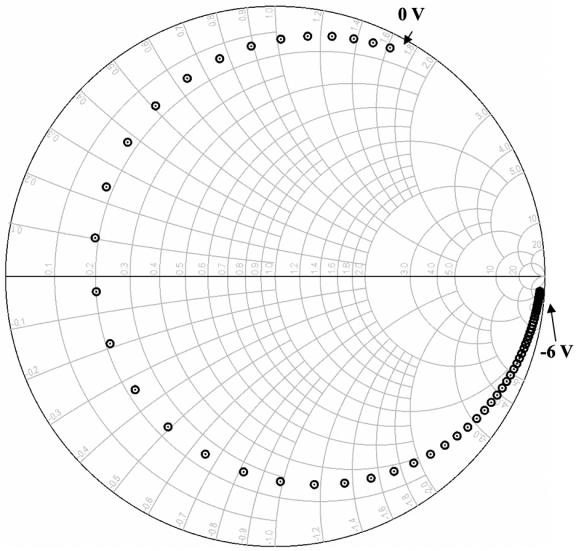



Figure 5.40: Projected performance of a diode array which eliminates all losses except for the diode series resistance.

Future research directions in the field of quasi-optical arrays could include fabricating different passive grid structures on various thicknesses of silicon to study the losses in the grids. Also, implementing larger size arrays (10,000-element for instance) could increase coupling of the quasi-optical beam energy to the diode array. Finally, more research could be done in designing a better array fixture, which would allow the backshort mirror to be placed directly behind the diode array.

# Chapter 6

# Conclusion & Future Work

The focus of this thesis has been to improve the process for fabricating quasi-vertical Schottky diodes heterogeneously integrated on silicon substrates and to characterize these devices electrically and thermally. A new fabrication process was developed to address the low yield issues of the prior process, which suffered from delamination and cracking after the bonding and thinning of the GaAs epitaxy. The new process eliminated many of the problematic thermal process steps by replacing the annealed ohmic contact on n-GaAs with a non-alloyed ohmic contact on an InGaAs cap layer grown epitaxially on n-GaAs. The new process also developed a new low-temperature curing wafer bonding technique that uses SU-8 as the bonding agent. The process which was developed in this dissertation lead to a significant increase in fabrication yields from under 10% to more than 90%. Next, a new method for extracting diode parasitics was developed based on measurements of passive structures fabricated on the same wafer as the diodes. The diodes were also characterized thermally for the first time using thermo-reflectance and the electrical transient method. The electrical and thermal models which were developed in this work will allow future students to design more efficient quasi-vertical diode based circuits. Finally, the robustness of the new fabrication process was assessed through the development of a quasi-vertical diode array. The new contributions of this thesis include:

- The development of a new fabrication process for quasi-vertical Schottky diodes heterogeneously integrated on silicon.

- The development of a new method for extracting diode parasitics using fabricated passive structures.
- The first characterization of quasi-vertical Schottky diodes using thermoreflectance.
- The assessment of the process robustness by developing the first quasi-optical array based on quasi-vertical diodes on silicon membranes.

## 6.1 Future Work

Directions for future research related to this dissertation involve scaling the 40-160 GHz frequency multiplier to higher frequencies to realize multipliers operating at terahertz frequencies. A schematic diagram for a proposed 520 GHz multiplier chain is shown in Fig. 6.1. It consists of a Quinstar micrometer tuned Gunn source (QTM-6718-AI), a Millitech high power amplifier (AMP-15-20050), a 65 to 130 GHz first stage doubler, and, finally, a 130 to 520 GHz quadrupler. The quadrupler is based on a balanced architecture. Therefore, any scattered power due to a mismatch in the output is directed to an isolation port and, consequently, it does not reflect back into the doubler. The chain is designed to have an output power greater than 10 mW at 520 GHz, with a 10% bandwidth. The input frequency and available power determines the varactor anode size, substrate doping, and epilayer thickness. These parameters are summarized in Table 6.1 for the 520 GHz multiplier chain. The 65 to 130 GHz doubler has been designed by Moore and will be fabricated and tested in the next few months. One drawback of varactor based multipliers is the narrow bandwidth (typically 10% fractional bandwidth). One way to address that is to distribute many varactor diodes along the multiplier chip, relatively close together, so as not to generate unwanted standing waves, in order to present a wider range of impedances for conversion. This direction is currently being investigated by Jafari.

Finally, future diode processing research directions include heterogeneously integrating Schottky diodes on other substrates such as diamond or silicon carbide to push the power handling and temperature limits of the quasi-vertical diode technology. Leveraging the advances in diamond on insulator (DOI)

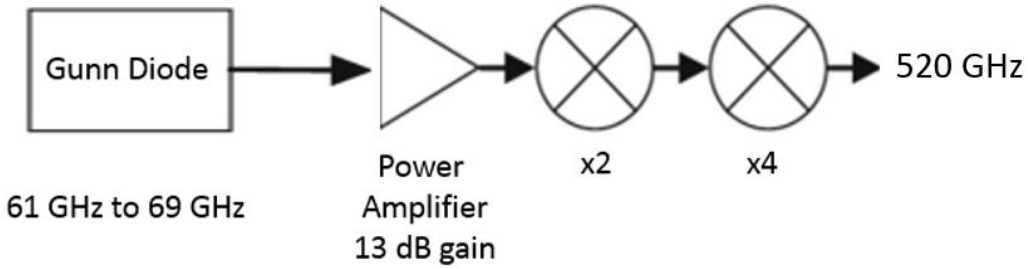



Figure 6.1: Schematic diagram of the proposed 520 GHz multiplier chain.

Table 6.1: Summary of the 520 GHz design parameters

| Parameters | Anode diameter | Device thickness | Device doping |
|---|---|---|---|
| 130 GHz doubler | 9.4 $\mu m$ | 500 nm | $1 * 10^{17} cm^{-3}$ |
| 520 GHz quad (input) | 4.8 $\mu m$ | 280 nm | $2 * 10^{17} cm^{-3}$ |

technology could allow the fabrication of quasi-vertical GaAs diodes on diamond. For silicon carbide, developing selective etches for different dopings of silicon carbide might be necessary. In both cases, beam lead processes will have to be developed. Another interesting research direction relates to the development of new bonding methods which replace the adhesives with metal-metal bonding, which offer superior thermal properties and is compatible with the new diode process.

# List of Publications

1. **S. Nadri**, L. Xie, M. Jafari, M. F. Bauwens, A. Arsenovic, R. M. Weikle, "Measurement and Extraction of Parasitic Parameters of Quasi-Vertical Schottky Diodes at Submillimeter Wavelengths," submitted to *IEEE Microwave and Wireless Components Letters,* March 2019.

2. **S. Nadri**, C. M. Moore, N. D. Sauber, L. Xie, M. E. Cyberey, J. T. Gaskins, A. W. Lichtenberger, N. S. Barker, P. E. Hopkins, M. Zebarjadi, R. M. Weikle, "Thermal Characterization of Quasi-Vertical GaAs Schottky Diodes Integrated on Silicon," *IEEE Transactions on Electron Devices*, vol. 66, no. 1, pp. 349-356, Jan. 2019.

3. **S. Nadri***, L. Xie*, M. Jafari, N. Alijabbari, M. E. Cyberey, N. S. Barker, A. W. Lichtenberger, R. M. Weikle, "A 160 GHz frequency Quadrupler based on heterogeneous integration of GaAs Schottky diodes onto silicon using SU-8 for epitaxy transfer," *Proc. IEEE MTT-S International Microwave Symposium MTT '*18, June 2018, Philadelphia, Pennsylvania, USA. (* First co-authors)

4. L. Xie, C. M. Moore, M. E. Cyberey, S. **Nadri**, N. D. Sauber, M. F. Bauwens, A. W. Lichtenberger, N. S. Barker, R. M. Weikle, "Micromachined probes with integrated GaAs Schottky diodes for on-wafer temperature sensing," *Proc.* 2018 *IEEE International Instrumentation and Measurement Technology Conference (I2MTC)*, May 2018, Houston, Texas, USA.

5. Q. Yu, Y. Wang, L. Xie, **S. Nadri**, K. Sun, J. Zang, Q. Li, R. M. Weikle, A. Beling, "High-performance InGaAs/InP photodiodes on silicon using low-temperature wafer-bonding", *Conference on Lasers and*

*Electro-Optics OSA Technical Digest (online)* (Optical Society of America 2018).

6. L. Xie*, **S. Nadri***, N. Alijabbari, M. E. Cyberey, M. F. Bauwens, A. W. Lichtenberger, N. S. Barker, R. M. Weikle, "An epitaxy transfer process for heterogeneous integration of submillimeter-wave GaAs Schottky diodes on silicon using SU-8," *IEEE Electron Device Lett.*, vol. 38, no. 11, pp. 1516–1519, Nov. 2017, doi: 10.1109/LED.2017.2756920. (* First co-authors)

7. M. B. Eller, N. D. Sauber, A. Arsenovic, **S. Nadri**, L. Xie, R. M. Weikle, "A monostatic coded aperture reflectometer for imaging at submillimeter-wavelengths," *Proc. IEEE MTT-S International Microwave Symposium MTT '*17, June 2017, Honolulu, Hawaii, USA.

8. R.M. Weikle II, H. Li, A. Arsenovic, **S. Nadri**, L. Xie, M. F. Bauwens, N. Alijabbari, N.S. Barker, and A.W. Lichtenberger, "Micromachined Interfaces for Metrology and Packaging Applications in the Submillimeter-Wave Band," *International Microelectronics Assembly and Packaging Society (IMAPS), Device Packaging Conference,* January 2017.

9. S. Hawasli, **S. Nadri**, L. Xie, R.M. Weikle II, "An Integrated 100-Element Schottky Varactor Diode Array for Sideband Generation at 1.6 THz," *Proc. IEEE MTT-S International Microwave Symposium MTT '16*, 22-27 May 2016, San Fransisco, California.

10. R.M. Weikle II, C. Zhang, S. Hawasli, **S. Nadri**, L. Xie, N.S. Barker, and A.W. Lichtenberger, M.F. Bauwens, "Terahertz Diode Arrays and Differential Probes based on Heterogeneous Integration and Silicon Micromachining," *International Microelectronics Assembly and Packaging Society (IMAPS), Device Packaging Conference,* January 2016.

11. **S. Nadri**, L. Xie, N. Alijabbari, J.T. Gaskins, B.M. Foley, P.E. Hopkins, R.M. Weikle II, "Steady-State Thermal Analysis of an Integrated 160 GHz Balanced Quadrupler Based on Quasi-Vertical Schottky Diodes," *40*$^{\text{th}}$ *International Conference on Infrared, Millimeter and Terahertz Wave (IRMMW)*, Hong Kong, August, 2015.

12. **S. Nadri**, R. Percy, L. Kittiwatanakul, A. Arsenovic, J. Lu, S. Wolf, R.M. Weikle II, "Terahertz Coded Aperture Mask using a Vanadium Dioxide Bowtie Antenna Array," *SPIE Optics and Photonics Conference Proceedings*, San Diego, 2014.

# Bibliography


[1] N. Alijabbari, M. F. Bauwens, and R. M. Weikle, "160 GHz Balanced Frequency Quadruplers Based on Quasi-Vertical Schottky Varactors Integrated on Micromachined Silicon," *IEEE Transactions on Terahertz Science and Technology*, vol. 4, no. 6, pp. 678–685, Nov. 2014. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6920095

[2] P. H. Siegel, "Terahertz technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 3, pp. 910–928, Mar. 2002.

[3] A. I. McIntosh, B. Yang, S. M. Goldup, M. Watkinson, and R. S. Donnan, "Terahertz spectroscopy: a powerful new tool for the chemical sciences?" *Chemical Society Reviews*, vol. 41, no. 6, pp. 2072–2082, Feb. 2012. [Online]. Available: http://pubs.rsc.org/en/content/articlelanding/2012/cs/c1cs15277g

[4] A. G. Davies, A. D. Burnett, W. Fan, E. H. Linfield, and J. E. Cunningham, "Terahertz spectroscopy of explosives and drugs," *Materials Today*, vol. 11, no. 3, pp. 18–26, Mar. 2008. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1369702108700166

[5] S. Ergun and S. Sonmez, "Terahertz Technology For Military Applications," *Journal of Military and Information Science*, vol. 3, no. 1, pp. 13–16, 2015. [Online]. Available: http://jmisci.com/article/view/5000086030

[6] Y. Yang, A. Shutler, and D. Grischkowsky, "Measurement of the transmission of the atmosphere from 02 to 2 THz," *Optics*

*Express*, vol. 19, no. 9, p. 8830, Apr. 2011. [Online]. Available: https://www.osapublishing.org/oe/abstract.cfm?uri=oe-19-9-8830

[7] T. W. Crowe, W. L. Bishop, D. W. Porterfield, J. L. Hesler, and R. M. Weikle, "Opening the terahertz window with integrated diode circuits," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 10, pp. 2104–2110, Oct. 2005.

[8] M. Cyberey, "Investigation of Material Growth and Fabrication Processes for THz Frequency SIS Mixers," Ph.D. dissertation, University of Virginia, Apr. 2014. [Online]. Available: https://libraetd.lib.virginia.edu/public_view/pv63g042c

[9] H. Hubers, "Terahertz Heterodyne Receivers," *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 14, no. 2, pp. 378–391, Mar. 2008.

[10] F. Sizov and A. Rogalski, "THz detectors," *Progress in Quantum Electronics*, vol. 34, no. 5, pp. 278–347, Sep. 2010. [Online]. Available: http://linkinghub.elsevier.com/retrieve/pii/S007967271000025X

[11] R. Lai, X. B. Mei, W. R. Deal, W. Yoshida, Y. M. Kim, P. H. Liu, J. Lee, J. Uyeda, V. Radisic, M. Lange, T. Gaier, L. Samoska, and A. Fung, "Sub 50 nm InP HEMT Device with Fmax Greater than 1 THz," in *2007 IEEE International Electron Devices Meeting*, Dec. 2007, pp. 609–611.

[12] M. Seo, M. Urteaga, J. Hacker, A. Young, Z. Griffith, V. Jain, R. Pierson, P. Rowell, A. Skalare, A. Peralta, R. Lin, D. Lin, and M. Rodwell, "InP HBT IC Technology for Terahertz Frequencies: Fundamental Oscillators Up to 0.57 THz," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 10, pp. 2203–2214, Oct. 2011.

[13] Tae-Woo Kim, JesusA del Alamo, Kwang-Seok Seo, Berinder Brar, and Dae-Hyun Kim, "III-V High-Electron-Mobility Transistors toward Terahertz Operation," in *Handbook of Terahertz Technologies*. Pan Stanford, Apr. 2015, pp. 133–150. [Online]. Available: http://www.crcnetbase.com/doi/abs/10.1201/b18381-7

[14] J. D. Albrecht, M. J. Rosker, H. B. Wallace, and T. Chang, "THz electronics projects at DARPA: Transistors, TMICs, and amplifiers," in *2010 IEEE MTT-S International Microwave Symposium*, May 2010, pp. 1118–1121.

[15] J. Stake, T. Bryllert, A. O. Olsen, and J. Vukusic, "Heterostructure Barrier Varactor Quintuplers for Terahertz Applications," in *Microwave Integrated Circuit Conference, 2008. EuMIC 2008. European*, Oct. 2008, pp. 206–209.

[16] D. Koller, S. Durant, C. Rowland, E. Bryerton, and J. Hesler, "Initial measurements with WM164 VNA extenders," in *2016 41st International Conference on Infrared, Millimeter, and Terahertz waves (IRMMW-THz)*. Copenhagen, Denmark: IEEE, Sep. 2016, pp. 1–2. [Online]. Available: http://ieeexplore.ieee.org/document/7758434/

[17] A.-Y. Tang, "Modelling and Characterisation of Terahertz Planar Schottky Diodes," Ph.D. dissertation, Chalmers University, 2013. [Online]. Available: https://research.chalmers.se/publication/172943

[18] R. Williams, *Modern GaAs processing methods /*. Boston :: Artech House,.

[19] "Crystal detector," Feb. 2019, page Version ID: 885391026. [Online]. Available: https://en.wikipedia.org/w/index.php?title=Crystal_detector&oldid=885391026

[20] W. Bishop, E. Meiburg, R. Mattauch, T. Crowe, and L. Poli, "A micron-thickness, planar Schottky diode chip for terahertz applications with theoretical minimum parasitic capacitance," in *IEEE International Digest on Microwave Symposium*. Dallas, TX, USA: IEEE, 1990, pp. 1305–1308. [Online]. Available: http://ieeexplore.ieee.org/document/99818/

[21] P. Siegel, R. Smith, M. Graidis, and S. Martin, "2.5-THz GaAs monolithic membrane-diode mixer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 5, pp. 596–604, May 1999. [Online]. Available: http://ieeexplore.ieee.org/document/763161/

[22] S. Martin, B. Nakamura, A. Fung, P. Smith, J. Bruston, A. Maestrini, F. Maiwald, P. Siegel, E. Schlecht, and I. Mehdi, "Fabrication of 200 to 2700 GHz multiplier devices using GaAs and metal membranes," in *2001 IEEE MTT-S International Microwave Sympsoium Digest (Cat. No.01CH37157)*, vol. 3. Phoenix, AZ, USA: IEEE, 2001, pp. 1641–1644. [Online]. Available: http://ieeexplore.ieee.org/document/967219/

[23] S. Hawasli, "Terahertz Sideband Generation Based on a Schottky Varactor Diode Array," Ph.D. dissertation, University of Virginia, 2013.

[24] N. Alijabbari, "Submillimeter-Wave Quasi-Vertical GaAs Schottky Diodes Integrated on Silicon Membranes," Ph.D. dissertation, University of Virginia, Aug. 2014. [Online]. Available: https://libraetd.lib.virginia.edu/public_view/z603qx61q

[25] C. Lee, J. Ward, R. Lin, E. Schlecht, G. Chattopadhyay, J. Gill, B. Thomas, A. Maestrini, I. Mehdi, and P. Siegel, "A wafer-level diamond bonding process to improve power handling capability of submillimeter-wave Schottky diode frequency multipliers," in *2009 IEEE MTT-S International Microwave Symposium Digest*, Jun. 2009, pp. 957–960.

[26] D. M. Pozar, *Microwave Engineering, 4th Edition*. Wiley Global Education, Nov. 2011, google-Books-ID: JegbAAAAQBAJ.

[27] M. J. Madou, *Fundamentals of Microfabrication: The Science of Miniaturization*, 2nd ed. CRC Press, Oct. 2018. [Online]. Available: https://www.crcpress.com/Fundamentals-of-Microfabrication-The-Science-of-Miniaturization-Second/Madou/p/book/9781315274225

[28] S. M. Marazita, "Integrated planar GaAs Schottky mixers for submillimeter wavelength receivers /," Ph.D. dissertation, University of Virginia, 1999.

[29] G. S. Schoenthal, "Integrated diode circuits for greater than 1 THz," Ph.D. dissertation, University of Virginia, 2003.

[30] J. Midkiff, "A Schottky diode integrated phase shifter for 220 GHz communications /," Ph.D. dissertation, University of Virginia, 2004.

[31] A. Simon, A. Grub, V. Krozer, K. Beilenhoff, and H. L. Hartnagel, "Planar THz Schottky diode based on a quasi vertical diode structure," in *Fourth Int. Symp. Space Terahertz Tech.*, 1993, pp. 392–403.

[32] N. Alijabbari, M. F. Bauwens, and R. M. Weikle, "Design and Characterization of Integrated Submillimeter-Wave Quasi-Vertical Schottky Diodes," *IEEE Transactions on Terahertz Science and Technology*, vol. 5, no. 1, pp. 73–80, Jan. 2015. [Online]. Available: http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6932490

[33] I. Mehdi, J. V. Siles, C. Lee, and E. Schlecht, "THz Diode Technology: Status, Prospects, and Applications," *Proceedings of the IEEE*, vol. 105, no. 6, pp. 990–1007, Jun. 2017.

[34] S. Arscott, P. Mounaix, and D. Lippens, "Transferred InP-based HBVs on glass substrate," *Electronics Letters*, vol. 35, no. 17, pp. 1493–1494, Aug. 1999.

[35] A. Baca and C. Ashby, *Fabrication of GaAs Devices*. London, U.K: The Institution of Engineering and Technology, Oct. 2005.

[36] L. Kolaklieva and R. Kakanakov, "Ohmic Contacts for High Power and High Temperature Microelectronics," *Micro Electronic and Mechanical Systems*, Dec. 2009. [Online]. Available: https://www.intechopen.com/books/micro-electronic-and-mechanical-systems/ohmic-contacts-for-high-power-and-high-temperature-microelectronics

[37] T. Nittono, H. Ito, O. Nakajima, and T. Ishibashi, "Extremely Low Resistance Non-Alloyed Ohmic Contacts to n GaAs Using Compositionally Graded InGaAs Layers," *Japanese Journal of Applied Physics*, vol. 25, no. 10A, p. L865, Oct. 1986. [Online]. Available: http://iopscience.iop.org/article/10.1143/JJAP.25.L865/meta

[38] n. Northrup and n. Zhang, "Dopant and defect energetics: Si in GaAs," *Physical Review. B, Condensed Matter*, vol. 47, no. 11, pp. 6791–6794, Mar. 1993.

[39] A. Mohades-Kassai, "Compensation in MBE-grown GaAs doped with silicon and beryllium," in *ICM 2000. Proceedings of the 12th International Conference on Microelectronics. (IEEE Cat. No.00EX453)*, Oct. 2000, pp. 341–344.

[40] B. Galiana, I. Rey-Stolle, C. Algora, and I. GarcÃa, "Te doping of GaAs using metalorganic vapor phase epitaxy: Volatile versus nonvolatile behavior," *Journal of Applied Physics*, vol. 104, no. 11, p. 114906, Dec. 2008. [Online]. Available: https://aip.scitation.org/doi/10.1063/1.3033398

[41] A. Piotrowska, "Ohmic Contacts to GaAs: Fundamentals and Practice," *Acta Physica Polonica A*, vol. 84, no. 3, pp. 491–504, 1993. [Online]. Available: http://psjd.icm.edu.pl/psjd/element/bwmeta1.element.bwnjournal-article-appv84z309kz

[42] I. Mehdi, U. K. Reddy, J. Oh, J. R. East, and G. I. Haddad, "Nonalloyed and alloyed low resistance ohmic contacts with good morphology for GaAs using a graded InGaAs cap layer," *Journal of Applied Physics*, vol. 65, no. 2, pp. 867–869, Jan. 1989. [Online]. Available: https://aip.scitation.org/doi/abs/10.1063/1.343080

[43] A. G. Foyt, "The electro-optic applications of InP," *Journal of Crystal Growth*, vol. 54, no. 1, pp. 1–8, Jul. 1981. [Online]. Available: http://www.sciencedirect.com/science/article/pii/0022024881902414

[44] K. Nagata, O. Nakajima, T. Yamauchi, T. Nittono, H. Ito, and T. Ishibashi, "Self-aligned AlGaAs/GaAs HBT with low emitter resistance utilizing InGaAs cap layer," *IEEE Transactions on Electron Devices*, vol. 35, no. 1, pp. 2–7, Jan. 1988.

[45] A. M. Crook, E. Lind, Z. Griffith, M. J. W. Rodwell, J. D. Zimmerman, A. C. Gossard, and S. R. Bank, "Low resistance,

nonalloyed Ohmic contacts to InGaAs," *Applied Physics Letters*, vol. 91, no. 19, p. 192114, Nov. 2007. [Online]. Available: http://scitation.aip.org/content/aip/journal/apl/91/19/10.1063/1.2806235

[46] R. Dormaier and S. E. Mohney, "Factors controlling the resistance of Ohmic contacts to n-InGaAs," *Journal of Vacuum Science & Technology B*, vol. 30, no. 3, p. 031209, May 2012. [Online]. Available: http://scitation.aip.org/content/avs/journal/jvstb/30/3/10.1116/1.4705730

[47] M. V. Lebedev, D. Ensling, R. Hunger, T. Mayer, and W. Jaegermann, "Synchrotron photoemission spectroscopy study of ammonium hydroxide etching to prepare well ordered GaAs(100) surfaces," *Applied Surface Science*, vol. 229, pp. 226–232, May 2004. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S0169433204000947

[48] P. Ramm, J. J.-Q. Lu, and M. M. V. Taklo, *Handbook of Wafer Bonding*. John Wiley & Sons, Feb. 2012, google-Books-ID: dG6KvrI0wNUC.

[49] F. Niklaus, G. Stemme, J.-Q. Lu, and R. J. Gutmann, "Adhesive wafer bonding," *Journal of Applied Physics*, vol. 99, no. 3, p. 031101, Feb. 2006. [Online]. Available: http://scitation.aip.org/content/aip/journal/jap/99/3/10.1063/1.2168512

[50] S. Franssila, *Introduction to Microfabrication*. John Wiley & Sons, Jun. 2004, google-Books-ID: 3Mw8fBKgUOAC.

[51] A. d. Campo and C. Greiner, "SU-8: a photoresist for high-aspect-ratio and 3d submicron lithography," *Journal of Micromechanics and Microengineering*, vol. 17, no. 6, p. R81, 2007. [Online]. Available: http://stacks.iop.org/0960-1317/17/i=6/a=R01

[52] Q. Yu, Y. Wang, L. Xie, S. Nadri, K. Sun, J. Zang, Q. Li, R. M. Weikle, and A. Beling, "High-performance InGaAs/InP photodiodes on silicon using low-temperature wafer-bonding," in *Conference on Lasers and Electro-Optics (2018), paper SM2I.1*. Optical Society of America, May 2018, p. SM2I.1. [Online]. Available: https://www.osapublishing.org/abstract.cfm?uri=CLEO_SI-2018-SM2I.1

[53] R. M. Weikle, C. Zhang, S. Hawasli, S. Nadri, L. Xie, N. S. Barker, and A. Lichtenberger, "Terahertz Diode Arrays and Differential Probes based on Heterogeneous Integration and Silicon Micromachining," *Additional Conferences (Device Packaging, HiTEC, HiTEN, & CICMT)*, vol. 2016, no. DPC, pp. 000 924–000 962, Jan. 2016. [Online]. Available: http://imapsource.org/doi/10.4071/2016DPC-TP36

[54] T. J. Reck, L. Chen, C. Zhang, A. Arsenovic, C. Groppi, A. Lichtenberger, R. M. Weikle, and N. S. Barker, "Micromachined Probes for Submillimeter-Wave On-Wafer Measurements Part 2: RF Design and Characterization," *IEEE Transactions on Terahertz Science and Technology*, vol. 1, no. 2, pp. 357–363, Nov. 2011.

[55] H. Xu, G. S. Schoenthal, L. Liu, Q. Xiao, J. L. Hesler, and R. M. W. II, "On Estimating and Canceling Parasitic Capacitance in Submillimeter-Wave Planar Schottky Diodes," *IEEE Microwave and Wireless Components Letters*, vol. 19, no. 12, pp. 807–809, Dec. 2009.

[56] A. Y. Tang, V. Drakinskiy, K. Yhland, J. Stenarson, T. Bryllert, and J. Stake, "Analytical Extraction of a Schottky Diode Model From Broadband S-Parameters," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 5, pp. 1870–1878, May 2013.

[57] A. Y. Tang and J. Stake, "Impact of Eddy Currents and Crowding Effects on High-Frequency Losses in Planar Schottky Diodes," *IEEE Transactions on Electron Devices*, vol. 58, no. 10, pp. 3260–3269, Oct. 2011.

[58] E. L. Kolberg, T. J. Tolmunen, M. A. Frerking, and J. R. East, "Current saturation in submillimeter-wave varactors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 40, no. 5, pp. 831–838, May 1992.

[59] J. T. Louhi, A. V. Raisanen, and N. R. Erickson, "Cooled Schottky varactor frequency multipliers at submillimeter wavelengths," *IEEE Transactions on Microwave Theory and Techniques*, vol. 41, no. 4, pp. 565–571, Apr. 1993.

[60] C. G. Perez-Moreno, J. Grajal, C. Viegas, H. Liu, J. Powell, and B. Alderman, "Thermal analysis of high-power millimeter-wave Schot-

tky diode frequency multipliers," in *2016 Global Symposium on Millimeter Waves (GSMM) ESA Workshop on Millimetre-Wave Technology and Applications*, Jun. 2016, pp. 1–4.

[61] S. Nadri, L. Xie, N. Alijabbari, J. T. Gaskins, B. M. Foley, P. E. Hopkins, and R. M. Weikle, "Steady-state thermal analysis of an integrated 160 GHz balanced quadrupler based on quasi-vertical Schottky diodes," in *2015 40th International Conference on Infrared, Millimeter, and Terahertz waves (IRMMW-THz)*, Aug. 2015, pp. 1–2.

[62] A. Maestrini, B. Thomas, H. Wang, C. Jung, J. Treuttel, Y. Jin, G. Chattopadhyay, I. Mehdi, and G. Beaudin, "Schottky diode-based terahertz frequency multipliers and mixers," *Comptes Rendus Physique*, vol. 11, no. 7, pp. 480–495, Aug. 2010. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1631070510000447

[63] F. Temcamani, J. Fonder, O. Latry, and C. Duperrier, "Electrical and Physical Analysis of Thermal Degradations of AlGaN/GaN HEMT Under Radar-Type Operating Life," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 3, pp. 756–766, Mar. 2016.

[64] J. Stake, L. Dillner, S. H. Jones, C. Mann, J. Thornton, J. R. Jones, W. L. Bishop, and E. Kollberg, "Effects of self-heating on planar heterostructure barrier varactor diodes," *IEEE Transactions on Electron Devices*, vol. 45, no. 11, pp. 2298–2303, Nov. 1998.

[65] S. Adachi, *GaAs and related materials.* Singapore: World Scientific, 1994.

[66] M. A. Saber, "Thermal characterization of THz planar Schottky diodes using simulations," 2012. [Online]. Available: https://aaltodoc.aalto.fi:443/handle/123456789/7657

[67] A.-Y. Tang, E. Schlecht, G. Chattopadhyay, R. Lin, C. Lee, J. Gill, I. Mehdi, and J. Stake, "Steady-State and Transient Thermal Analysis of High-Power Planar Schottky Diodes," *22nd International Symposium on Space Terahertz Technology*, 2011. [Online]. Available: https://research.chalmers.se/en/publication/141051

[68] D. L. Blackburn, "Temperature measurements of semiconductor devices - a review," in *Twentieth Annual IEEE Semiconductor Thermal Measurement and Management Symposium (IEEE Cat. No.04CH37545)*, Mar. 2004, pp. 70–80.

[69] T. Kiuru, J. Mallat, A. V. Raisanen, and T. Narhi, "Schottky Diode Series Resistance and Thermal Resistance Extraction From S Parameter and Temperature Controlled IV Measurements," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 8, pp. 2108–2116, Aug. 2011.

[70] S. Khanal, T. Kiuru, B. Thomas, J. Mallat, C. Pinta, M. Nagel, A. Walber, V. Kangas, M. Perichaud, M. Brandt, T. Narhi, and A. Raisanen, "Characterisation of THz Schottky diodes for MetOp-SG instruments," in *Proceedings of the 26th International Symposium on Space Terahertz Technology, 2015*, 2015, pp. T1–4. [Online]. Available: https://cris.vtt.fi/en/publications/characterisation-of-thz-schottky-diodes-for-metop-sg-instruments

[71] S. Khanal, T. Kiuru, A. Tang, M. A. Saber, J. Mallat, J. Stake, T. Narhi, and A. V. Raisanen, "Thermal Characterization of THz Schottky Diodes Using Transient Current Measurements," *IEEE Transactions on Terahertz Science and Technology*, vol. 4, no. 2, pp. 267–276, Mar. 2014.

[72] J. W. Sofia, "Analysis of thermal transient data with synthesized dynamic models for semiconductor devices," in *Proceedings of 1994 IEEE/CHMT 10th Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM)*, Feb. 1994, pp. 78–85.

[73] A. F. Robertson and D. Gross, "An Electrical-Analog Method for Transient Heat Flow Analysis," *Journal of Research of the National Bureau of Standards*, vol. 61, no. 2, pp. 105–115, Aug. 1958.

[74] T. Zhan, Y. Xu, M. Goto, Y. Tanaka, R. Kato, and M. Sasaki, "Thermal boundary resistance at Au/Ge/Ge and Au/Si/Ge interfaces," *RSC Advances*, vol. 5, no. 61, 2015.

[75] "ANSYS Mechanical."

[76] K. M. Freedy, A. Giri, B. M. Foley, M. R. Barone, P. E. Hopkins, and S. McDonnell, "Titanium contacts to graphene: process-induced variability in electronic and thermal transport," *Nanotechnology*, vol. 29, no. 14, p. 145201, Feb. 2018. [Online]. Available: https://doi.org/10.1088%2F1361-6528%2Faaaacd

[77] D. Kendig, K. Yazawa, and A. Shakouri, "Hyperspectral thermoreflectance imaging for power devices," in *2017 33rd Thermal Measurement, Modeling Management Symposium (SEMI-THERM)*, Mar. 2017, pp. 204–207.

[78] A. Shakouri, A. Ziabari, D. Kendig, J. Bahk, Y. Xuan, P. D. Ye, K. Yazawa, and A. Shakouri, "Stable thermoreflectance thermal imaging microscopy with piezoelectric position control," in *2016 32nd Thermal Measurement, Modeling Management Symposium (SEMI-THERM)*, Mar. 2016, pp. 128–132.

[79] D. Kendig, K. Yazawa, and A. Shakouri, "High resolution thermal characterization of a GaAs MMIC," in *2015 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, May 2015, pp. 51–54.

[80] P. L. Komarov, M. G. Burzo, and P. E. Raad, "A thermoreflectance thermography system for measuring the transient surface temperature field of activated electronic devices," in *Twenty-Second Annual IEEE Semiconductor Thermal Measurement And Management Symposium*, Mar. 2006, pp. 199–203.

[81] "Microsanj NT210a," Kifer Road, Santa Clara, California 95051, USA.

[82] K. Maize, "High Resolution Thermoreflectance Imaging of Power Transistors and Nanoscale Percolation Networks," Ph.D. dissertation, UC Santa Cruz, 2014. [Online]. Available: https://escholarship.org/uc/item/2mg1c0n2

[83] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*. John Wiley & Sons, Nov. 2006.

[84] C. Jeong, S. Datta, and M. Lundstrom, "Thermal conductivity of bulk and thin-film silicon: A Landauer approach," *Journal of Applied Physics*, vol. 111, no. 9, p. 093708, May 2012. [Online]. Available: https://aip.scitation.org/doi/full/10.1063/1.4710993

[85] M. Asheghi, M. N. Touzelbaev, K. E. Goodson, Y. K. Leung, and S. S. Wong, "Temperature-Dependent Thermal Conductivity of Single-Crystal Silicon Layers in SOI Substrates," *Journal of Heat Transfer*, vol. 120, no. 1, pp. 30–36, Feb. 1998. [Online]. Available: http://dx.doi.org/10.1115/1.2830059

[86] D. G. Cahill, K. Goodson, and A. Majumdar, "Thermometry and Thermal Transport in Micro Nanoscale Solid-State Devices and Structures," *Journal of Heat Transfer*, vol. 124, no. 2, pp. 223–241, Dec. 2001. [Online]. Available: http://dx.doi.org/10.1115/1.1454111

[87] P. E. Hopkins, J. R. Serrano, L. M. Phinney, S. P. Kearney, T. W. Grasser, and C. T. Harris, "Criteria for Cross-Plane Dominated Thermal Transport in Multilayer Thin Film Systems During Modulated Laser Heating," *Journal of Heat Transfer*, vol. 132, no. 8, pp. 081 302–081 302–10, May 2010. [Online]. Available: http://dx.doi.org/10.1115/1.4000993

[88] B. Zhu, Y. Chen, K. Deng, W. Hu, and Z. Yao, "Terahertz science and technology and applications," *Proc.PIERS*, pp. 1166–1170, 2009.

[89] D. S. Kurtz, R. M. Weikle II, T. W. Crowe, and J. L. Hesler, "Sideband generators for submillimeter-wave applications," vol. 3617, 1999, pp. 89–96. [Online]. Available: http://dx.doi.org/10.1117/12.347112

[90] S. Hawasli, S. Nadri, L. Xie, and R. M. Weikle, "An Integrated 100-element schottky varactor diode array for sideband generation at 1.6 THz." IEEE, May 2016, pp. 1–4. [Online]. Available: http://ieeexplore.ieee.org/document/7540263/

[91] T. M. Goyette, J. C. Dickinson, J. Waldman, and W. E. Nixon, "A 1.56 THz compact radar range for W band imagery of scale model tactical targets," E. G. Zelnio, Ed., Aug. 2000, pp.

615–622. [Online]. Available: http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=906669

[92] R. M. Weikle, "Quasi-optical planar grids for microwave and millimeter-wave power combining," phd, California Institute of Technology, 1992. [Online]. Available: http://resolver.caltech.edu/CaltechETD:etd-08162007-095038

[93] L. B. Sjogren, "Diode Array Beam Controllers," Ph.D. dissertation, University of California Los Angeles (UCLA), 1993.

[94] W. W. Lam, C. F. Jou, H. Z. Chen, K. S. Stolt, N. C. Luhmann, and D. B. Rutledge, "Millimeter-wave diode-grid phase shifters," *IEEE Transactions on Microwave Theory and Techniques*, vol. 36, no. 5, pp. 902–907, May 1988.

[95] J. L. Hesler, *Planar Schottky Diodes in Submillimeter-wavelength Waveguide Receivers*. University of Virginia, 1996.

[96] K. Cheng, "Effects of Ohmic Metal on Electrochemical Etching of GaAs in pHEMT Manufacturing," 2007.

[97] A. Arsenovic, "Current Problems on the Forefront of the THz Metrology, and Calibration," Doctor of Philosophy, University of Virginia, 2012.

[98] A. Wuttig and R. Riesenberg, "Single element detector and optical modulator contra focal plane array for thermal imaging," *IRS Proceedings*, pp. 103–109, 2002.

[99] R. Percy, "Characterization and Development of Submillimeter Wavelength Devices Incorporating Vanadium Dioxide Thin Films," Ph.D. dissertation, University of Virginia, Sep. 2013. [Online]. Available: https://libraetd.lib.virginia.edu/public_view/sb3978414

[100] A. Crunteanu, F. Dumas-Bouchiat, C. Champeaux, A. Catherinot, A. Pothier, and P. Blondy, "Microwave switching functions using reversible metal-insulator transition (MIT) in VO2 thin films," in *2007 European Microwave Conference*, Oct. 2007, pp. 12–15.

[101] H. Jerominek, F. Picard, and D. Vincent, "Vanadium oxide films for optical switching and detection," *Optical Engineering*, vol. 32, no. 9, pp. 2092–2100, Sep. 1993. [Online]. Available: https://www.spiedigitallibrary.org/journals/Optical-Engineering/volume-32/issue-9/0000/Vanadium-oxide-films-for-optical-switching-and-detection/10.1117/12.143951.short

[102] J. F. De Natale, P. J. Hood, and A. B. Harker, "Formation and characterization of grain oriented VO2 thin films," *Journal of Applied Physics*, vol. 66, no. 12, pp. 5844–5850, Dec. 1989. [Online]. Available: https://aip.scitation.org/doi/10.1063/1.343605

[103] T. Lanskaya, I. Merkulov, and F. Chudnovskii, "Hysteresis effects at the semiconductor-metal phase transition in vanadium oxides," *Sov Phys Solid State (Engl. Transl.)*, pp. 193–197.

[104] S. Hawasli, N. Alijabarri, and R. M. Weikle, "Schottky diode arrays for submillimeter-wave sideband generation," in *2012 37th International Conference on Infrared, Millimeter, and Terahertz Waves*, Sep. 2012, pp. 1–2.

# Appendix A

# On-Wafer Diode Fabrication

Start with a GaAs diode epitaxy, with five layers grown in this order on a 650 µm semi-insulating GaAs handle: 1 µm AlGaAs etch stop layer, 280 nm n-GaAs ($2$ x $10^{17}$ $cm^{-3}$), 1 µm n+-GaAs ($5$ x $10^{18}$ $cm^{-3}$), 40 nm $In_xGa_{1-x}As$ graded layer (x: 0→0.6) ($> 10^{19}$ $cm^{-3}$), and a 50 nm $In_xGa_{1-x}As$ layer (x = 0.6) ($> 10^{19}$ $cm^{-3}$)

**Sample preparation: cleanliness is the key!**
Dice the GaAs epitaxy (also called III-V) 20 mm x 20 mm
Mount on silicon carrier using black wax (don't use too much black wax. If exposed, some of it might vaporize and condense on the sample in the evaporator)
TCE/ACE/Meth clean
Use swab if necessary
Use AZ-400K if necessary
Use toothpick or blade if necessary

**Evaporation using e-beam**
Clean the evaporator
Surface clean: BOE (20 secs), followed by $NH_4OH$ : DI (1:20)
Load the sample into the inner ring of the e-beam (experiences lower temperatures)
Evaporate metals (20% thicker to compensate for crystal error): Ti (48 nm at 1.5 A/s), Pd (48 nm at 0.3 A/s), Au (170 nm at 0.5 A/s), long cool off session, another Au (170 nm at 0.5 A/s), Ti (24 nm at 1.5 A/s)

**Cleaning the GaAs: cleanliness is the key!**
TCE/RA/METH clean
March $O_2$ 200 W

Toothpick or blade if necessaryy

**Cleaning the SOI (usually easier to clean)**
Strip tape from the SOI wafer
Clean the edges with the surgical blade under the LEICA microscope
ACE/METH with swab around the edges
TCE/ACE/METH with swab
March $O_2$ 200 W 10 mins
AZ-400K if necessary

**Pre-bonding**
For this, use SU-8 TF6000.5 with built-in adhesion promoter for thin-film coating ($<$ 1µm)
Clean the transparent force distribution plate (FDP) from L-grease residue
Put the FDP on the 110 °C hot plate, and put a dot of L-grease on top (at the center)
Spin coat 1 mL of SU-8 TF6000.5 on SOI using micropipette (9700 rpm for 35 secs to get 250 nm)
Clean residual SU-8 from backside and edge bead using AZ-EBR and DI water
Transfer the sample on the FDP (which is on the hot plate) for 1 min
Avoid rapid cooling: let sample cool in dish for 10 mins
Expose SU-8: 40 secs using SU-8 filter (MJB3 set to 7 mW/$cm^2$)
Transfer to the bonding jig

**Bonding**
Clean the silicone membrane
Check if the thermal couple is making good contact
Clean copper block
Seperate the cooling block
Seperate the Si and GaAs (frontside screw should read 2")
Use bubble level to level the stage (adjusting thermo-couple)
Put a little amount of L-grease on the copper block, put the GaAs on the copper block
Blow dry both the Si and GaAs and place the Si facing the GaAs
Place the thick aluminum ring, membrane, and thin aluminum ring
Put the lid on
Turn on the jig and set the temperature to 30 °C
Turn on the upper chamber pump S3 (see Fig. A1) for seconds until -30 psi, turn off
Counterclockwise of the left black knob S5 and make the green valve S2 (see Fig. A1) horizontal wait for 40 min for outgassing at 30 °C
Using front screw, put the GaAs and Si in contact (there should be a tiny gap)
Turn on $N_2$: Now, the left gauge should be -27 psi and the right gauge should be -18~-19 psi. If the right gauge is not at the right pressure, use $N_2$ to adjust

Set the temperature to 140 °C for 40 mins, when the temperature reaches 70 °C close all valves

Cool: Turn on the chiller and set the temp to room temp and bring the cooling block in contact

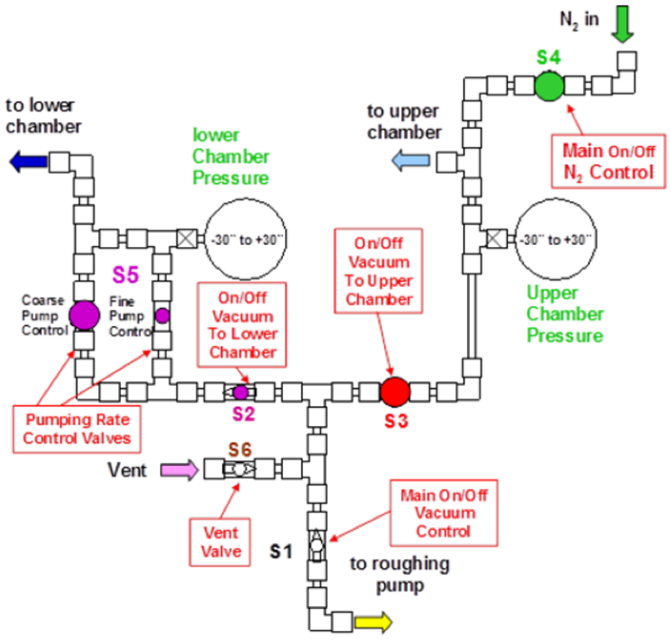



Figure A.1: Diagram of Valve Control System.

**Handle removal**

Clean GaAs handle: TCE to remove L-grease AZEBR and AZ400K to remove rainbow films

Clean the SU-8 on the edge of Si carrier: use the scalpel under LEICA microscope

Solvent clean

March $O_2$ 200 W $>$ 10 mins

Seperate the Si and GaAs (frontside screw should read 2")

Use bubble level to level the stag

Fast GaAs etch (~580 µm, 24 min): $HNO_3$ : $H_2O_2$ : DI at 50 °C, rotate sample 180 degrees twice after 5 mins, and 90 degrees after another 5 mins. Shake sample to get rid of bubbles.

Slow GaAs etch: $C_6H_8O_7$ : $H_2O_2$ : DI at 50 °C: The citric acid etch lasts 30-45 mins, until the AlGaAs etch stop layer is exposed. After a 5 minute over-etch, the sample is rinsed sequentially in 2 DI beakers, with very minimal air exposure. The sample is then immersed in hydrofluoric acid (HF) for 1 minute, which removes the AlGaAs layer, thus revealing the GaAs device layer field. The sample is then transferred to a DI beaker for 10 mins, followed by a methanol spin clean (with swab) to ensure that the top device layer is free of any contaminant.

Spin clean with METH only and swab to clean the sample

**Large mesa formation**
Spin clean using ACE/MET
Spin HMDS @ 4000 rpm for 30 secs
Spin AZ-4210 @ 4000 RPM
Bake 100 °C for 1 min
MJB4 exposure 160 secs (P = 380 W)
Develop
Hard bake 100 °C for 1 min and 130 °C for 5 min
GaAs etch with $H_2SO_4$ : $H_2O_2$ : DI =2.5:20:400 for 4min (watch for the interference pattern, 3 secs over-etch)
Ohmic and Su-8 etch: The thin Ti layers are removed in a CHF3/SF6 RIE and the Pd with 10 secs TFA (Transene gold etchant TFA) wet etch. The TFA must be diluted in DI (2:1). The thick gold layer is removed with an Ar sputter etch, followed by a brief potassium iodide wet etch. Since Ar sputter etching is used to remove the thick gold layer, back sputtering of the gold atoms on the resist, and eventually on the large mesa is inevitable. However, this etch sequence is carefully designed to substantially minimize this effect. Once the ohmic metal layers have been removed, the exposed SU-8 adhesive layer is etched using a CF4 RIE. Table A.1 summarizes the RIE dry etching parameters used in forming the large mesas, which include the type of gas, pressure, flow, RF power and etch times. All these etches are performed using a Semigroup RIE tool

Table A.1: RIE Dry Etch Parameters

| Etch | $SF_6$ (sccm) | $CHF_3$ (sccm) | $N_2$ (sccm) | Ar (sccm) | $CF_4$ (sccm) | Pressure (mTorr) | RF (W) | Time (min) |
|---|---|---|---|---|---|---|---|---|
| Ti | 20 | 5 | 0.6 (glow only) | - | - | 35 | 150 | 2 (for 20 nm) |
| Au | - | - | - | 70 | - | 30 | 120 | Inspection |
| SU-8 | - | - | - | - | 30 | 25 | 100 | ~15 |

**Small mesa formation**
Spin clean using ACE/MET
Spin HMDS @ 4000 rpm for 30 secs
Spin AZ-4210 @ 4000 RPM
Bake 100 °C for 1 min
120 secs exposure in EVG
Develop
Hard bake 100 °C for 1 min and 130 °C for 5 min
GaAs etch with $H_2SO_4$ : $H_2O_2$ : DI =2.5:20:400
March $O_2$ 200 W 20 mins

Spin clean using ACE/MET

**Sacrifical resist**
Spin HMDS @ 4000 rpm for 30 secs
Spin AZ-4210 @ 4000 RPM
Bake 100 °C for 1 min
180 secs exposure in EVG
Develop
March $O_2$ 150 W 5 mins
BOE 20s, $NH_4OH$:DI=1:10 20s, no DI rinse
Load the sample in Sputt3 tool using L-grease
Seedlayer: Ti (1 min 30 secs), Au (2 min 30 secs))

**Plating**
Spin HMDS @ 4000 rpm for 30 secs
Spin AZ-4210 @ 3000 RPM
Bake 100 °C for 1 min
270 secs exposure in EVG
Develop
March $O_2$ 150 W 5 mins
Plate 2 µm (with agitation)
The table below is an example of a typical plating condition, which leads to plating 800 nm of gold

Table A.2: Typical Plating Condition (first plating)

| Current (mA) | 2 | 4 | 7 |
|---|---|---|---|
| Voltage (V) | 0.54 | 0.65 | 0.76 |
| Time (min) | 1 | 1 | 10 |

**PR and seedlayer removal**
Flood exposure 60s in MJB4
Develop in 1:4AZ400K 1min40s
March $O_2$ 200 W 10 mins
HG400 1 min (check), DI*3, DI rinse, BOE 20s flash+15s, DI rinse
$O_2$ Semigroup 120 W 80 sccm 80
ACE/RA/METH spin clean, VERY GENTLE BLOW DRY

# Appendix B

# Backside Process for Quadrupler/Array

**Via etch**

Spin HMDS @ 4000 rpm for 30 secs

Spin on AZ4330 photoresist at 2500 rpm (gives about 4.0 µm thick resist)

Bake 110 °C for 2 min

MJB4 exposure 100 secs (P = 380 W)

Develop

March $O_2$ 200 W 10 mins

Hard bake 110 °C for 10 min

Oxford $O_2$+$SF_6$ and $O_2$ only for 1 hr

Si etch recipe: "Si etch $C_4F_8$=30, $SF_6$=30, ICP=500, EP" using end-point detection

Table B.1: Si dry etch Oxford recipe.

| Etch | $C_4F_8$ (sccm) | $SF_6$ (sccm) | Pressure (mTorr) | He (Torr) | Temperature (°C) | RF (W) | ICP (W) | Time (min) |
|---|---|---|---|---|---|---|---|---|
| Si | 30 | 30 | 15 | 5 | 0 | 40 | 500 | End Point |

**Bonding SOI to carrier**

Need 2" 500 µm Si carrier

Spin Waferbond CR-200 (WB) on sample and carrier at 3500 rpm 40s (ramp up from 0 to)

Clean back of sample and carrier w/ median swab and small amount of TCE sprayed

In Art's jig, outgas the WB for 10 mins at -20 psi

Turn on the hot plate and bake the WB for 25 mins at 150 °C (start timing from the moment the hot plate is turned on)

Proceed to mix the epoxy: In a tilted aluminum foil dish, make a 1:10 mix of epoxy (part B: part A). Thoroughly mix with the stick end of the swab. Outgas the epoxy under vacuum for $>$ 30 mins

Using 500 µL of epoxy, bond the SOI to the carrier (10 mins outgasing, 8 mins curing of epoxy with two samples in contact at 100 °C, cure for $>$30 mins in the lapping jig

**Dicing of the SOI handle**

Measure working thickness

Get the hubless blade for dicing (ALHUB1)

In dicing saw do the hair line alignment to find total thickness of the wafer

Blade height = Working distance –456um+70um (leaving 70um results in ~40min Si etch)

Y index(distance btw cuts)=0.3mm, cut (number of cuts for 30mm wafer is 110 lines), dicing speed= 3mm/s

To remove the remaining silicon, use Oxford Si etch recipe (see via etch)

Extent etch (see via etch)

# Appendix C

# EMF Calculation

The calculation, which are attached to the nex three pages, were performed using Mathcad.

MathCAD Sheet to Calculate Equivalent Circuit and Response of Souheil's diode array

## Grid Parameters

$a := 100$ size of square unit cell in microns

$g := 7$ slot gap in microns

$w := 3$ estimated finger width in microns

$t := 15$ silicon thickness in microns

$d := 450$ air gap in microns

## Physical Parameters

$\varepsilon r := 11.7$ dielectric constant silicon

$\varepsilon q := 3.8$ dielectric constant quartz

$c := 29.98\,10^{4}$ speed of light in vacuum in GHz-microns

$\eta 0 := 377$ intrinsic wave impedance free space in Ohms

## Transmission Line Calculations for Grid Modal Admittances

**Propagation Constants:**

$$\beta 0(f,m,n) := \begin{cases} \sqrt{\left(\frac{2\cdot\pi\cdot f}{c}\right)^2 - \left(\frac{m\cdot\pi}{a}\right)^2 - \left(\frac{n\cdot\pi}{a}\right)^2} & \text{if } f \geq \frac{c}{2\cdot a}\cdot\sqrt{m^2+n^2} \\ -\sqrt{\left(\frac{2\cdot\pi\cdot f}{c}\right)^2 - \left(\frac{m\cdot\pi}{a}\right)^2 - \left(\frac{n\cdot\pi}{a}\right)^2} & \text{otherwise} \end{cases}$$

propagation constant in free space

$$\beta d(f,m,n) := \begin{cases} \sqrt{\left(\frac{2\cdot\pi\cdot f}{c}\right)^2\cdot\varepsilon r - \left(\frac{m\cdot\pi}{a}\right)^2 - \left(\frac{n\cdot\pi}{a}\right)^2} & \text{if } f \geq \frac{c}{2\cdot a\cdot\sqrt{\varepsilon r}}\cdot\sqrt{m^2+n^2} \\ -\sqrt{\left(\frac{2\cdot\pi\cdot f}{c}\right)^2\cdot\varepsilon r - \left(\frac{m\cdot\pi}{a}\right)^2 - \left(\frac{n\cdot\pi}{a}\right)^2} & \text{otherwise} \end{cases}$$

propagation constant in the substrate

**Wave Impedances:**

$$ZTE0(f,m,n) := \eta 0\cdot\left(\frac{2\cdot\pi\cdot f}{c\cdot\beta 0(f,m,n)}\right)$$

TE mode impedance in free space

$$ZTEd(f,m,n) := \eta 0 \cdot \left( \frac{2 \cdot \pi \cdot f}{c \cdot \beta d(f,m,n)} \right)$$ TE mode impedance in the substrate

$$ZTM0(f,m,n) := \eta 0 \cdot \left( \frac{c \cdot \beta 0(f,m,n)}{2 \cdot \pi \cdot f} \right)$$ TM mode impedance in free space

$$ZTMd(f,m,n) := \eta 0 \cdot \left( \frac{c \cdot \beta d(f,m,n)}{2 \cdot \pi \cdot f \cdot \epsilon r} \right)$$ TM mode impedance in the substrate

**Wave Impedances Looking in Forward and Reverse Directions:**
**Assumed one direction faces the array substrate, and air gap and mirror as shown**

$$ZTEp(f,m,n) := ZTE0(f,m,n)$$ TE impedane looking into +z direction (empty space)

$$ZTMp(f,m,n) := ZTM0(f,m,n)$$ TM impedane looking into +z direction (empty space)

$$ZTEs(f,m,n) := i\,ZTE0(f,m,n) \cdot \tan(\beta 0(f,m,n) \cdot d)$$ TE impedane looking at mirror from backside of silicon

$$ZTMs(f,m,n) := i\,ZTM0(f,m,n) \cdot \tan(\beta 0(f,m,n) \cdot d)$$ TM impedane looking at mirror from backside of silicon

$$ZTEm(f,m,n) := ZTEd(f,m,n) \cdot \frac{ZTEs(f,m,n) + i \cdot ZTEd(f,m,n) \cdot \tan(\beta d(f,m,n) \cdot t)}{ZTEd(f,m,n) + i \cdot ZTEs(f,m,n) \cdot \tan(\beta d(f,m,n) \cdot t)}$$

$$ZTMm(f,m,n) := ZTMd(f,m,n) \cdot \frac{ZTMs(f,m,n) + i \cdot ZTMd(f,m,n) \cdot \tan(\beta d(f,m,n) \cdot t)}{ZTMd(f,m,n) + i \cdot ZTMs(f,m,n) \cdot \tan(\beta d(f,m,n) \cdot t)}$$

**Parallel Combination for each set of mode impedances:**

$$Yte(f,m,n) := \frac{1}{ZTEp(f,m,n)} + \frac{1}{ZTEm(f,m,n)}$$

$$Ytm(f,m,n) := \frac{1}{ZTMp(f,m,n)} + \frac{1}{ZTMm(f,m,n)}$$

**Calculation of Grid Circuit**

**Elements**

$NN := 20$ $MM := 20$ number of modes to sum over

$$\delta(m) := \begin{cases} 1 & \text{if } m = 0 \\ 2 & \text{otherwise} \end{cases}$$

The Neumann factor

$$\text{sinc}(x) := \begin{cases} 1 & \text{if } x = 1 \\ \frac{\sin(x)}{x} & \text{otherwise} \end{cases}$$

definition of sinc(x)

**Gap Capacitance (TM modes for m = 0), sum over 50 modes:**

$$Yc(f) := 2 \cdot \sum_{n=1}^{NN} \left[ \left( \text{sinc}\left( \frac{n \cdot \pi \cdot w}{a} \right) \right)^2 \cdot Ytm(f, 0, n) \right]$$

**Series "Inductance" of the finger (TE and TM modes for m>0)**

$$Zl(f) := \sum_{m=1}^{MM} \left[ \frac{2 \cdot \left( \text{sinc}\left( \frac{m \cdot \pi \cdot g}{a} \right) \right)^2}{\sum_{n=0}^{NN} \left[ \left[ \delta(n) \cdot \left( \text{sinc}\left( \frac{n \cdot \pi \cdot w}{a} \right) \right) \right]^2 \cdot \left[ \frac{\left( \frac{n \cdot \pi}{a} \right)^2 \cdot Ytm(f, m, n) + \left( \frac{m \cdot \pi}{a} \right)^2 \cdot Yte(f, m, n)}{\left( \frac{m \cdot \pi}{a} \right)^2 + \left( \frac{n \cdot \pi}{a} \right)^2} \right] \right]} \right]$$

$freq := 220 .. 600$

# Appendix D

# Frontside Diode Array Fabrication

Start with a GaAs diode epitaxy, with five layers grown in this order on a 650 µm semi-insulating GaAs handle: 1 µm AlGaAs etch stop layer, 280 nm n-GaAs ($2$ x $10^{17}$ $cm^{-3}$), 1 µm n+-GaAs ($5$ x $10^{18}$ $cm^{-3}$), 40 nm $In_xGa_{1-x}As$ graded layer (x: 0→0.6) ($> 10^{19}$ $cm^{-3}$), and a 50 nm $In_xGa_{1-x}As$ layer (x = 0.6) ($> 10^{19}$ $cm^{-3}$)

**Sample preparation: cleanliness is the key!**
Dice the GaAs epitaxy (also called III-V) 24 mm x 24 mm
Mount on silicon carrier using black wax (don't use too much black wax. If exposed, some of it might vaporize and condense on the sample in the evaporator)
TCE/ACE/Meth clean
Use swab if necessary
Use AZ-400K if necessary
Use toothpick or blade if necessary

**Evaporation using e-beam**
Clean the evaporator
Surface clean: BOE (20 secs), followed by $NH_4OH$ : DI (1:20)
Load the sample into the inner ring of the e-beam (experiences lower temperatures)
Evaporate metals (20% thicker to compensate for crystal error): Ti (48 nm at 1.5 A/s), Pd (48 nm at 0.3 A/s), Au (120 nm at 0.5 A/s), Ti (24 nm at 1.5 A/s)

**Cleaning the GaAs: cleanliness is the key!**
TCE/RA/METH clean
March $O_2$ 200 W
Toothpick or blade if necessaryy

**Cleaning the SOI (usually easier to clean)**

Dice the SOI 32 mm x 32 mmUnmount the SOI from the dicing carrier
Clean the edges with the surgical blade under the LEICA microscope
ACE/METH with swab around the edges
TCE/ACE/METH with swab
March $O_2$ 200 W 10 mins
AZ-400K if necessary

**Pre-bonding**

For this, use SU-8 TF6000.5 with built-in adhesion promoter for thin-film coating ($<$ 1µm)
Clean the transparent force distribution plate (FDP) from L-grease residue
Put the FDP on the 110 °C hot plate, and put a dot of L-grease on top (at the center)
Spin coat 1 mL of SU-8 TF6000.5 on SOI using micropipette (9700 rpm for 35 secs to get 250 nm)
Clean residual SU-8 from backside and edge bead using AZ-EBR and DI water
Transfer the sample on the FDP (which is on the hot plate) for 1 min
Avoid rapid cooling: let sample cool in dish for 10 mins
Expose SU-8: 40 secs using SU-8 filter (MJB3 set to 7 mW/$cm^2$)
Transfer to the bonding jig

**Bonding**

Clean the silicone membrane
Check if the thermal couple is making good contact
Clean copper block
Seperate the cooling block
Seperate the Si and GaAs (frontside screw should read 2")
Use bubble level to level the stage (adjusting thermo-couple)
Put a little amount of L-grease on the copper block, put the GaAs on the copper block
Blow dry both the Si and GaAs and place the Si facing the GaAs
Place the thick aluminum ring, membrane, and thin aluminum ring
Put the lid on
Turn on the jig and set the temperature to 30 °C
Turn on the upper chamber pump S3 (see Fig. A1) for seconds until -30 psi, turn off
Counterclockwise of the left black knob S5 and make the green valve S2 (see Fig. A1) horizontal wait for 40 min for outgassing at 30 °C
Using front screw, put the GaAs and Si in contact (there should be a tiny gap)
Turn on $N_2$: Now, the left gauge should be -27 psi and the right gauge should be -18~-19 psi. If the right gauge is not at the right pressure, use $N_2$ to adjust

Set the temperature to 140 °C for 40 mins, when the temperature reaches 70 °C close all valves

Cool: Turn on the chiller and set the temp to room temp and bring the cooling block in contact

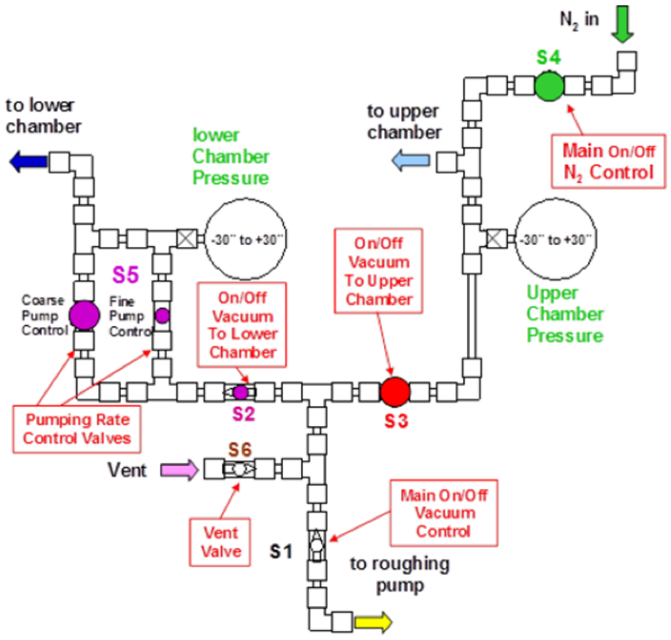



Figure D.1: Diagram of Valve Control System.

**Handle removal**

Clean GaAs handle: TCE to remove L-grease AZEBR and AZ400K to remove rainbow films

Clean the SU-8 on the edge of Si carrier: use the scalpel under LEICA microscope

Solvent clean

March $O_2$ 200 W $>$ 10 mins

Seperate the Si and GaAs (frontside screw should read 2")

Use bubble level to level the stag

Fast GaAs etch (~580 µm, 24 min): $HNO_3$ : $H_2O_2$ : DI at 50 °C, rotate sample 180 degrees twice after 5 mins, and 90 degrees after another 5 mins. Shake sample to get rid of bubbles.

Slow GaAs etch: $C_6H_8O_7$ : $H_2O_2$ : DI at 50 °C: The citric acid etch lasts 30-45 mins, until the AlGaAs etch stop layer is exposed. After a 5 minute over-etch, the sample is rinsed sequentially in 2 DI beakers, with very minimal air exposure. The sample is then immersed in hydrofluoric acid (HF) for 1 minute, which removes the AlGaAs layer, thus revealing the GaAs device layer field. The sample is then transferred to a DI beaker for 10 mins, followed by a methanol spin clean (with swab) to ensure that the top device layer is free of any contaminant.

Spin clean with METH only and swab to clean the sample

**Large mesa formation**
Spin clean using ACE/MET
Spin HMDS @ 4000 rpm for 30 secs
Spin AZ-4210 @ 4000 RPM
Bake 100 °C for 1 min
MJB4 exposure 160 secs (P = 380 W)
Develop
Hard bake 100 °C for 1 min and 130 °C for 5 min
GaAs etch with $H_2SO_4$ : $H_2O_2$ : DI =2.5:20:400 for 4min (watch for the interference pattern, 3 secs over-etch)
Ohmic and Su-8 etch: The thin Ti layers are removed in a CHF3/SF6 RIE and the Pd with 10 secs TFA (Transene gold etchant TFA) wet etch. The TFA must be diluted in DI (2:1). The thick gold layer is removed with an Ar sputter etch, followed by a brief potassium iodide wet etch. Since Ar sputter etching is used to remove the thick gold layer, back sputtering of the gold atoms on the resist, and eventually on the large mesa is inevitable. However, this etch sequence is carefully designed to substantially minimize this effect. Once the ohmic metal layers have been removed, the exposed SU-8 adhesive layer is etched using a CF4 RIE. Table A.1 summarizes the RIE dry etching parameters used in forming the large mesas, which include the type of gas, pressure, flow, RF power and etch times. All these etches are performed using a Semigroup RIE tool

Table D.1: RIE Dry Etch Parameters

| Etch | $SF_6$ (sccm) | $CHF_3$ (sccm) | $N_2$ (sccm) | Ar (sccm) | $CF_4$ (sccm) | Pressure (mTorr) | RF (W) | Time (min) |
|---|---|---|---|---|---|---|---|---|
| Ti | 20 | 5 | 0.6 (glow only) | - | - | 35 | 150 | 2 (for 20 nm) |
| Au | - | - | - | 70 | - | 30 | 120 | Inspection |
| SU-8 | - | - | - | - | 30 | 25 | 100 | ~15 |

**Small mesa formation**
Spin clean using ACE/MET
Spin HMDS @ 4000 rpm for 30 secs
Spin AZ-4210 @ 4000 RPM
Bake 100 °C for 1 min
120 secs exposure in EVG
Develop
Hard bake 100 °C for 1 min and 130 °C for 5 min
GaAs etch with $H_2SO_4$ : $H_2O_2$ : DI =2.5:20:400
March $O_2$ 200 W 20 mins

Spin clean using ACE/MET

**Via Etch**
Spin HMDS @ 4000 rpm for 30 secs
Spin on AZ4330 photoresist at 2500 rpm (gives about 4.0 µm thick resist)
Bake 110 °C for 2 min
MJB4 exposure 100 secs (P = 380 W)
Develop
March $O_2$ 200 W 10 mins
Hard bake 110 °C for 10 min
Oxford $O_2$+$SF_6$ and $O_2$ only for 1 hr
Si etch recipe: "Si etch $C_4F_8$=30, $SF_6$=30, ICP=500, EP" using end-point detection

**Sacrifical resist**
Spin HMDS @ 4000 rpm for 30 secs
Spin AZ-4210 @ 4000 RPM
Bake 100 °C for 1 min
180 secs exposure in EVG
Develop
March $O_2$ 150 W 5 mins
BOE 20s, $NH_4OH$:DI=1:10 20s, no DI rinse
Load the sample in Sputt3 tool using L-grease
Seedlayer: Ti (1 min 30 secs), Au (2 min 30 secs))

**Plating**
Spin HMDS @ 4000 rpm for 30 secs
Spin AZ-4210 @ 3000 RPM
Bake 100 °C for 1 min
270 secs exposure in EVG
Develop
March $O_2$ 150 W 5 mins
Plate 2 µm (with agitation)
The table below is an example of a typical plating condition, which leads to plating 700 nm of gold

**PR and seedlayer removal**
Flood exposure 60s in MJB4
Develop in 1:4AZ400K 1min40s

Table D.2: Typical Plating Condition (first plating)

| Current (mA) | 0.5 | 1 | 2 | 3 | 4 |
|---|---|---|---|---|---|
| Voltage (V) | 0.50 | 0.55 | 0.63 | 0.70 | 0.75 |
| Time (min) | 1.5 | 1.5 | 3 | 6 | 3 |

March $O_2$ 200 W 10 mins
HG400 1 min (check), DI*3, DI rinse, BOE 20s flash+15s, DI rinse
$O_2$ Semigroup 120 W 80 sccm 80
ACE/RA/METH spin clean, VERY GENTLE BLOW DRY

# Appendix E

# Backside Lithography for Bosch Process

**Mounting the sample**

Spin waferbond on the sample to protect the frontside

Mount on sapphire carrier using L-grease

Clean SOI backside using HNA for 5 mins: HF (20 mL) / Nitric acid (35 mL) / Acetic acid (55 mL)

Clean the SOI backside using solvents

**Lithography**

Spin HMDS

Spin SU-8 2015 5 secs then ramp to 2000 rpm

Soft bake 4 mins @ 90 °C

EVG exposure 90 secs using backside alignment: bottom side + overlay + use clear chuck

PEB @ 90 °C 4 mins

Dev in SU8 dev (IPA) Brush the un-patterned areas of the sample using SU-8

Bake 30 mins 120 °C

5-6 hrs 200 W March

# Appendix F

# Array Holder Fabrication

Start with dicing 10 mil quartz into a 27 mm x 27 mm rectangular shaped piece
Mount the quartz on a carrier (in this case 450 µm thick) using black wax: make sure the wax is even and convers the entire surface of the quartz

Evaporate or sputter Ti/Au seedlayer (at least 20 nm each)

**Pre-lithography #1**
Spin clean using TCE/ACE/MET
Spin HMDS @ 4000 rpm
Bake 110 °C for 30 secs
Spin AZ-4330 @ 4000 RPM

Bake 100 °C for 1 min, transfer the sample into black opaque dish

**Lithography #1: micro-writer**
Load the sample (orient such that the area on the right is completely covered with seed-layer)
Focus (height should be around 800 µm)
Find the 4 corners, and center using points (-13.5,13.5) (13.5,13.5) (13.5,-13.5)(-13.5,-13.5)
Load mask 1 (Gold1), and choose multipass 3, expose with dose of 400 mJ/$cm^2$

Develop until done in AZ-300 MIF or DI:AZ-400K (4:1)

**Plating #1**
March 200 W 10 mins
Plate 2 µm (with agitation)

The table below is an example of a typical plating condition, which results in plating 600 nm of gold

Table F.1: Typical Plating Condition (first plating)

| Current (mA) | 1 | 2 |
|---|---|---|
| Voltage (V) | 0.5 | 0.72 |
| Time (min) | 3 | 3 |

**Pre-lithography #2**

Strip resist using March 200 W 20 mins + solvent spin clean
Spin HMDS @ 4000 rpm
Bake 110 °C for 30 secs
Spin AZ-4620 @ 3000 RPM (10 µm)
Bake 100 °C for 2 min
Spin AZ-4620 @ 3000 RPM (10 µm)
Bake 100 °C for 2 min
Spin AZ-4620 @ 3000 RPM (10 µm)
Bake 100 °C for 2 min
Wait 1 hr (rehydration time)
Transfer the sample into black opaque dish

**Lithography #2: micro-writer**

Load the sample (orient it based on the previous lithography)
Focus (height should be around 800 µm) under 10x magnification
Find the actual center of the wafer using "wide field viewer"
Travel to the alignment markers with the following coordinates: (-9.977,7.512) (8.563,7.512) (8.577,-8.702)(-9.964,-8.702)
Using the coordinates above, one can calculate the distance needed to travel to reach the various alignment markers
Align (don't forget to correct for rotation as well!)
Load mask 2 (Gold2), and choose multipass 3, expose with dose of 4000 mJ/$cm^2$
Develop until done in DI:AZ-400K (3:1)

**Plating #2**

March 200 W 30 mins
Plate 25 µm (with agitation)
The table below is an example of a typical plating condition, which results in plating 5.5 µm of gold:

Table F.2: Typical Plating Condition (second plating)

| Current (mA) | 1 | 2 |
|---|---|---|
| Voltage (V) | 0.42 | 0.75 |
| Time (min) | 5 | 30 |

**Final steps**

Strip the resist

Seedlayer removal in HG400 and BOE

Clean the holder

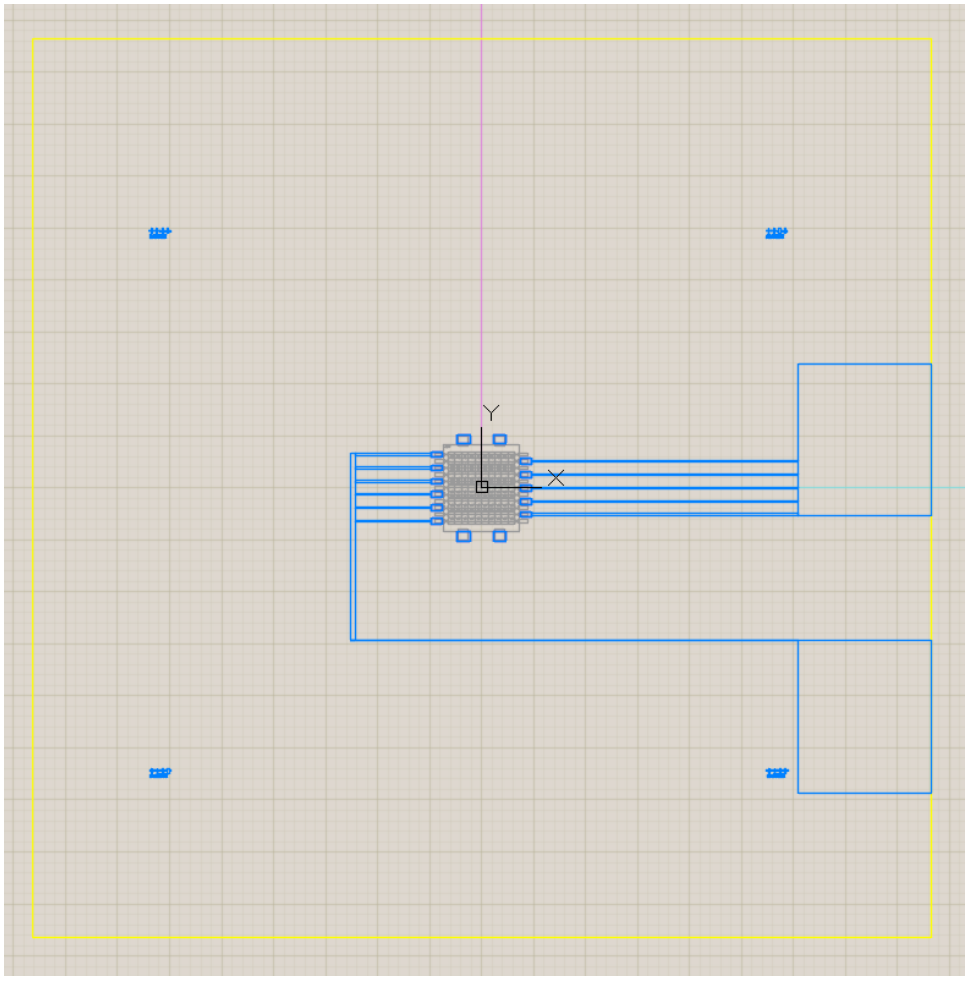


Figure F.1: CAD image of the array holder mask. The bias lines are 50 µm wide. The gold tacking pads are plated twice, during GOLD1 with the rest of the features, and again during GOLD2.

# Appendix G

# $VO_2$ Array

## G.1 Introduction

Millimeter-wave imaging arrays have been an important topic of research for the scientific community for decades and they continue to receive significant attention for their use in a variety of important applications, including radio astronomy, imaging spectroscopy, and plasma diagnostics. Moreover, imaging at terahertz or submillimeter-wave frequencies has begun to attract enormous interest because of its large potential impact on defense, security, the biological sciences, medicine and materials science [88], [10]. Millimeter-wave imaging systems generally fall into one of two fundamentally different categories: scanned systems and focal plane arrays. The use of the former method is limited to applications in which a scene or object being observed does not change rapidly. Moreover, it exhibits a limited signal-to-noise ratio due to practical integration times. The latter method consists of an ensemble of millimeter-wave sensors and a focusing element. Although the principle of focal plane imaging is straightforward, realizing practical architectures for these systems has proven difficult. A primary issue is floor-planning (accommodating the output signals from each pixel). The difficulty lies in designing output feeds for the various elements in the array without significantly disturbing its operation. The challenge of accommodating multiple IF outputs usually precludes the use of heterodyne detection in such arrays. The system requirements of imaging arrays for many present-day applications, however, place such stringent requirements on performance that they either eliminate consideration of

direct detection schemes (due to their low sensitivity compared to heterodyne detection), or push the technology to its fundamental limits (greatly increasing cost and complexity).

An alternative approach to imaging based on the focal plane technique described above is to spatially encode the incoming flux of electromagnetic energy prior to detection. This technique is generally referred to as "coded aperture" or "Hadamard" imaging and it permits multiple image points to be superimposed (or multiplexed) onto a single detector. This technique offers unique advantages. Foremost among them is that spatial encoding and multiplexing can be used to eliminate the need for an array of detectors. Thus, the floor-planning issue, which is inherent to large detector arrays, is eliminated. A second important advantage of the coded aperture approach is that it more readily accommodates heterodyne detection methods. Furthermore, Hadamard imaging offers a significant improvement in signal-to-noise ratio (SNR) compared to comparable scanned imaging system [98].

The central component of a coded aperture imaging system is the mask that modulates the incident wavefront. Traditionally, this mask has consisted of opaque and transparent apertures. Different mask patterns are obtained by moving the mask mechanically, resulting in different unique patterns. In this paper, we report on a vanadium dioxide bowtie array mask in which the mask elements are switched thermally. The array is found to be capable of modulating the transmission of a 500 to 750 GHz signal by up to 28 dB. A 100 nm thick $VO_2$ film located at the antenna feed point modulates the reflectance of the bowtie antenna such that it reflects the submillimeter-wave signal when the VO2 is in the off state (semiconducting) and transmits the signal when it is in the on state (metallic) [99]. A WR-1.5 one-port measurement system was assembled to validate the model of the bowtie antenna array. From measurements, the properties of the sapphire substrate and the $VO_2$ film are extracted. The transmission response of the mask is simulated and its performance predicted. In the final section, we investigate another method of switching the array using laser illumination.

## G.2 $VO_2$

### G.2.1 Background

Vanadium dioxide is a Mott insulator, so that due to electron-electron interactions, a bandgap of 0.7 eV is formed which prevents conduction of electrons at low temperatures. However, $VO_2$ is a material that exhibits an abrupt and reversible semiconductor-to-metal transition (SMT) at a temperature of 67 °C, close to room temperature. This proximity of the transition to room temperature makes $VO_2$ appealing for many applications. Moreover, this transition can be triggered through current injection, application of an electric field [100] or optical pumping [101]. When $VO_2$ undergoes a change from semiconductor to metal, it undergoes large modifications in its electrical and optical properties. The SMT is accompanied by changes in resistivity and reflectivity of the film. The change in resistivity varies from about one-half order of magnitude to five orders of magnitude depending on the transition method and film parameters [101]. A change in transmission of more than 40% is reported between the semiconducting and metallic state at terahertz, infrared, and optical frequencies [99], [102], [100], [101]. These properties make $VO_2$ attractive for a terahertz switch capable of modulating a signal beam.

### G.2.2 Fabrication

The $VO_2$ film used in this work was grown at the University of Virginia NanoSTAR Institute Department of Materials Science using reactive-biased target ion beam deposition (RBTIBD). This technique is used to deposit the $VO_2$ thin film onto a c-plane sapphire substrate. The main reactor chamber is pumped to a base pressure of 5 x$10^{-8}$ Torr, and the stage heater is set to 400-500 °C and allowed to stabilize for 45 minutes. The substrate surface is sputter cleaned using Ar ions and the vanadium target is sputter-cleaned by applying pulsed dc bias. Vanadium was sputtered in an 80/20 mixture of Ar and $O_2$ at a flow rate of 5.0 to 6.0 sccm, which results in a pressure of approximately 1 mTorr. A deposition time of approximately 2 hours results in a film thickness of about 5 nm.

## G.3 Architecture

The switching array consists of a 20 by 20 square matrix of bowtie antennas. The bowtie antennas have an angle of 90°, a diagonal length of 71.7 µm (Fig. D1(a)) and are made of a 150 nm thick layer of gold. Gold is also deposited on either side of the array to serve as electrical contacts seen in Fig. D1(a). These contacts are used to measure the resistance of the array versus temperature and the Mott transition, which is characterized by a change in resistance of two orders of magnitude and a hysteretic behavior [103] (Fig. D2). A $VO_2$ bridge is located at the antenna feed and has a size of 5 µm by 5 µm (Fig. D1(b)).

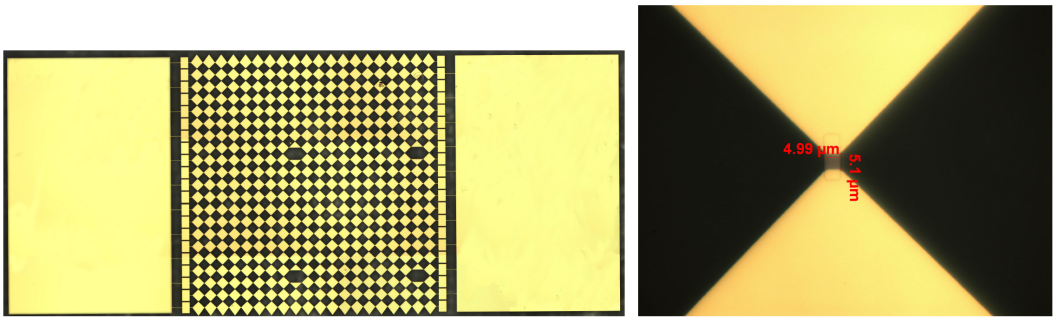



Figure G.1: (a) Microscope image of the bowtie antenna array. The rows are connected in parallel. The gure also shows the two gold contact pads on both sides. Some elements are missing due to defects in the mask. The structure is built on a sapphire substrate.(b) Higher magnication image of a single bowtie. The vanadium dioxide lm is located at the antenna feed.

From symmetry, the array unit cell can be represented as an equivalent waveguide with virtual electric walls along horizontal symmetry planes and virtual magnetic walls along vertical symmetry planes. This equivalent waveguide is represented by the unit cell circuit model shown in Fig. 3(a) [104], and has a size of 69 µm by 69 µm. These dimensions were chosen to only allow TEM mode propagation below 640 GHz. Above this cutoff frequency, the performance of the array deteriorates due to multimode propagation and formation of grating lobes. From the equivalent waveguide model, we can construct a circuit model representation for the array. The bowtie structure itself can be represented as an equivalent transmission line with characteristic impedance

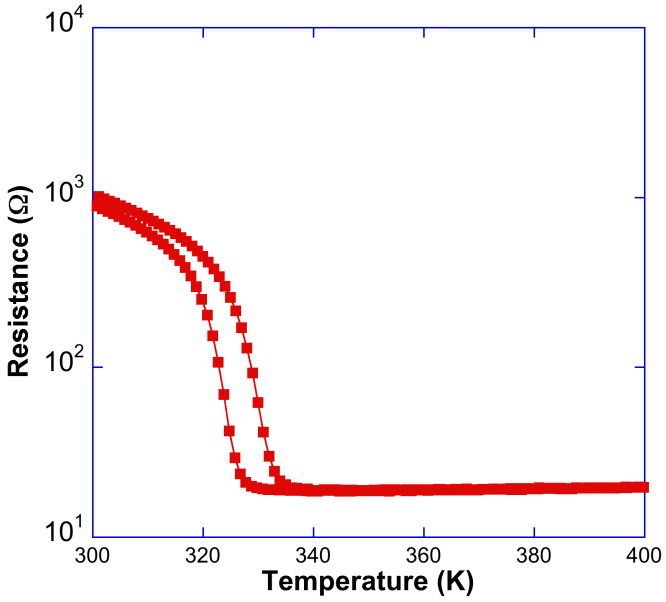



Figure G.2: Resistance vs temperature measurement of the sample. The measurement is done in a chamber that allows very accurate control of the temperature. The resistance changes by about two orders of magnitude and the behavior is hysteretic.

of $Z_{bow}$ and an electrical length of $\theta_{bow}$. The values for these parameters can be found using the EMF method [92] or finite-element electromagnetic simulation with HFSS. Furthermore, the vanadium dioxide bridge is modeled as a shunt temperature-dependent variable resistor. Finally, the air and sapphire substrates are also modeled as transmission lines. A representation of the array circuit model is shown in Fig. D3(b).

## G.4 Measurements

### G.4.1 Aparatus

A reflection coefficient measurement setup to characterize the array is shown in Fig. D4. A Rohde & Schwarz (ZVA-40) vector network analyzer together with a VDI WR-1.5 extension module provide the incident 500-750 GHz radiation through a diagonal horn antenna. The beam is collimated by an initial off-axis parabolic mirror (focal length of 76.4 mm). A second parabolic mirror (f = 76.4 mm) focuses the beam onto the sample (placed on an electronic hot plate)

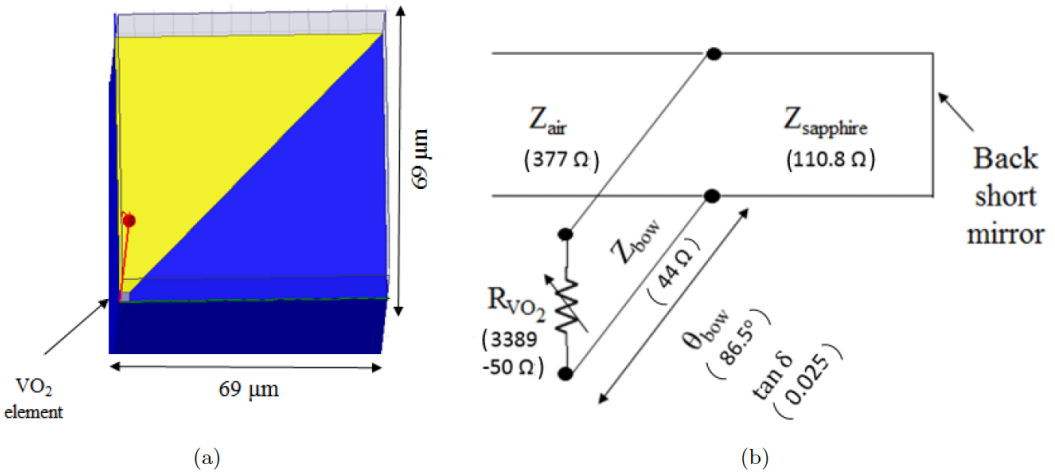



Figure G.3: (a) Layout of the array unit cell represented as an equivalent waveguide. The top and bottom walls are perfect E-walls. The right and left walls are perfect H-walls. The sapphire (in blue) has a thickness of 400 µm. The vanadium dioxide lm lies at the bottom left corner of the unit cell. Both the gold layer (in yellow) and the $VO_2$ have a thickness of 150 nm. (b) Circuit model representing the bowtie antenna array. The vanadium lm is represented as a variable resistor, with value ranging from 3.4 kΩ to 50 kΩ dependent on temperature.

using a 45° mirror. The reflected beam travels back through the same path to be detected by the VNA. For the reflection coefficient($S_{11}$) measurement, a back short mirror is placed behind the device under test (DUT) to eliminate possible absorption from the material of the hot plate surface.

## G.4.2 Calibration

Before useful measurements can be made with the quasi-optical setup system, the system must be calibrated by measuring a set of known standards. Calibration is used to remove the unwanted systematic errors associated with the measurement system [97]. Five delay shorts (with delays increments of 40 µm) and a low reflection load (microwave absorber) are used as standards. The second parabolic mirror, along with the 45° mirror and the hot plate, are mounted to an electronic translation stage. By moving the stage, the phase delay between the measurement reference plane and reflect standard can be adjusted in an accurate and repeatable way. In addition, as more standards than necessary are used, the calibration is overdetermined. As a result, an improvement

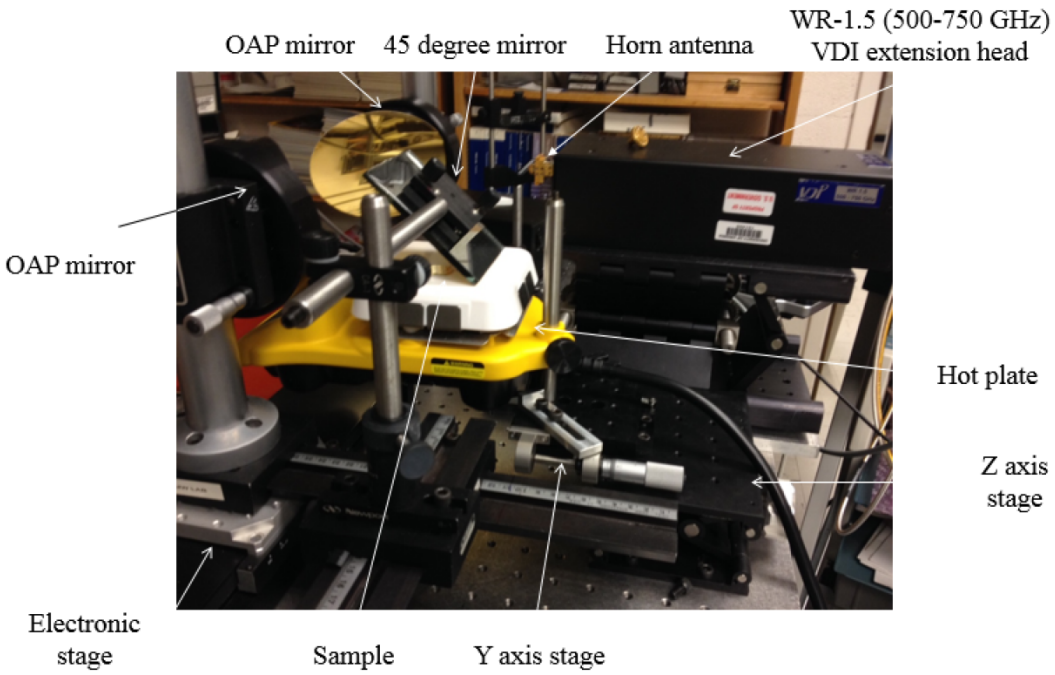



Figure G.4: Reflection coefficient $S_{11}$ measurement setup for the WR-1.5 frequency range. The mirrors are used to direct the beam onto the sample that sits on the electronic hot plate. We can therefore ensure precise control and reading of the temperature of the hot plate and sample.

in estimation of the error coefficients of the system can be achieved compared to using a minimum set of three [97]. All the algorithms and calculations used to correct the raw data have been made with the open-source python module scikit-rf [97]. A calibrated measurement of the one-port calibration standards is shown in Fig. D5.

To verify the measurements, a sapphire($Al_2O_3$) substrate (400 µm thick) with backshort was measured as a verification standard. As seen in Fig. D6(a), sapphire is lossless over the WR-1.5 band and therefore, all the power is reflected back to the VNA. Note that the magnitude of the reflection coefficient in Fig D6(a) wanders above zero at some frequencies which is due to uncorrected measurement error. Furthermore, by fitting the phase measurement to the transmission line model, shown in Fig. D6(b), we find that the reference plane is shifted by 40 µm (due to a misalignment error) and that the dielectric constant of sapphire is 11.58 parallel to the c-axis (in agreement with its nominal value). The model also includes an air gap prior to the reference plane

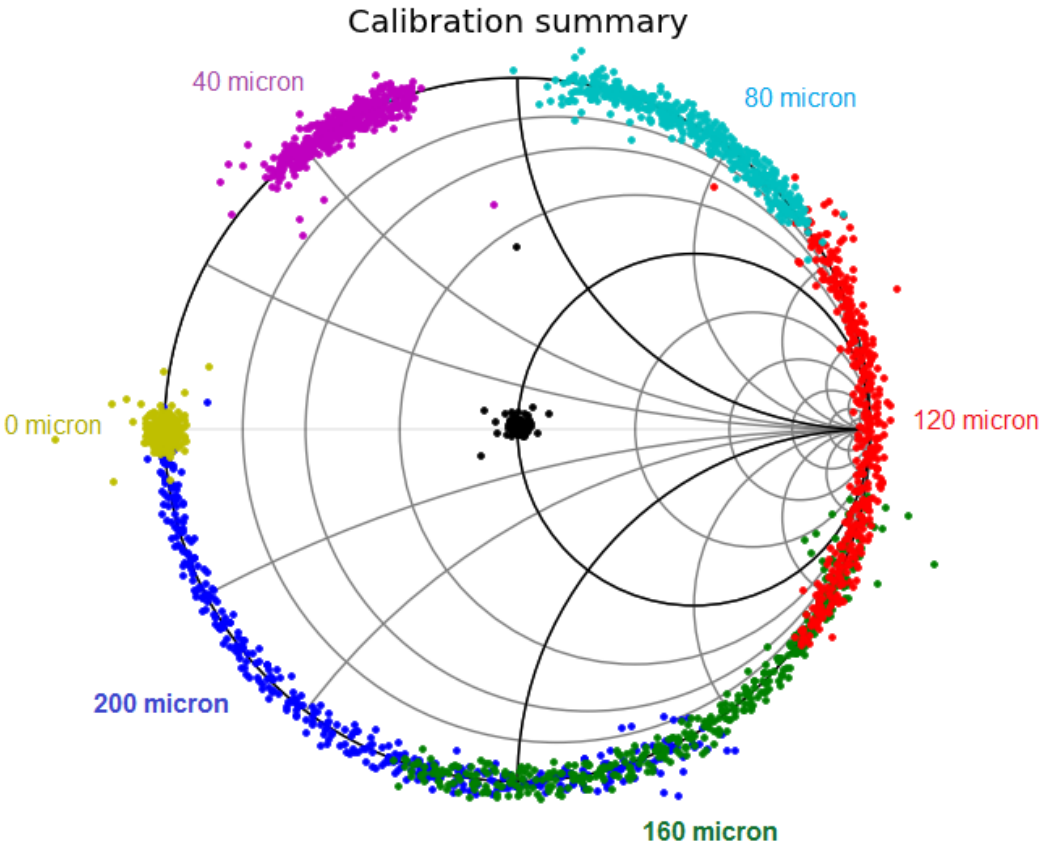
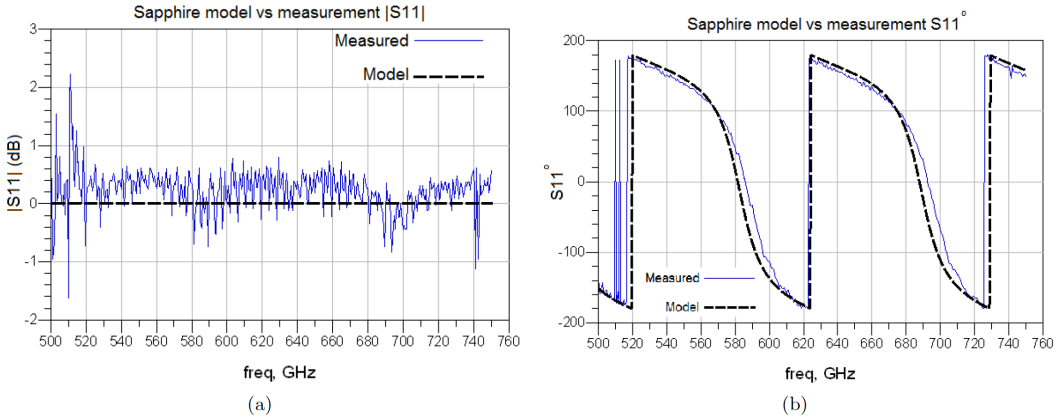



Figure G.5: Measurement of the system calibration standards from 500-750 GHz shown on a Smith chart. Microwave absorber is used as a match, at the center of the smith chart. The delay shorts are on the Smith chart perimeter and do not overlap, as required for a well-behaved calibration.

(due to a slight change of thickness between the calibration standards and the DUT), and an air gap between the sample and the back short.




(a) (b)

Figure G.6: (a) Magnitude of $S_{11}$ for a sapphire substrate with backshort conductor. Sapphire is lossless over the WR-1.5 band and therefore all the energy is reflected back. There is a deviation by ±1 dB due to calibration error. (b) Phase of $S_{11}$ (in degrees) for a piece of sapphire. The thickness of the piece of sapphire is 400 µm. The model also includes an air gap prior to the reference plane, and an air gap between the sample and the back short.

## G.5 Beam Size

The size of the $VO_2$ mask array, excluding the contact pads is 7.2 mm by 7.2 mm. An experiment was set up to determine the beam spot size, which should be no larger than the size of the array being measured. To ensure that this requirement is met, we cut a thin rectangular piece of microwave absorber the size of the array and placed it on a back short mirror on the hot plate. The response shown in Fig. D7 shows little reflection which verifies that the beam is sufficiently focused for this measurement. Note that the reflection peak at 515 GHz is likely associated with error uncorrected by the calibration.

## G.6 Results

The magnitude of the reflection coefficient $|S_{11}|$ of the bowtie array is shown in Figs D8(a) and D8(b) corresponding respectively to the room temperature and the 70 °C response. For both graphs, the curves in blue (solid line) represent the calibrated measured data while the curves in black (dotted line) represent the simulated result using Agilent's Advanced Design System (ADS). As one

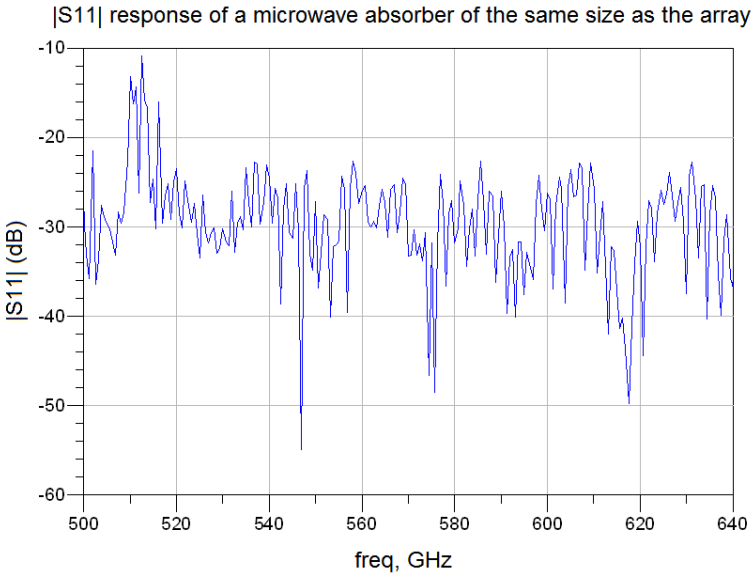



Figure G.7: $S_{11}$ measurement of the absorber used to test the beam size. The absorption is roughly -30 dB which indicates that the beam spot is smaller than the rectangular piece. Note that there is a reflection peak at 515 GHz due to an error uncorrected by the calibration.

can see, there is a sharp absorption dip at 541 GHz for the semiconducting state (Fig 8(a)), which is due to the coupling of energy to the $VO_2$ film. As the temperature increases above the transition temperature (Fig. 8(b)), there is a large change in the response characterized by the absence of the absorption dip. This corresponds to the array being reflective (metallic state). The phase responses corresponding to the magnitude plots are displayed in Figs 9(a) and 9(b). The circuit model is in good agreement with the measured data, although some measured magnitude values exceed 0 dB due to calibration error. We also note that there some discrepancies above 700 GHz due to multimode propagation not accounted for in the model.

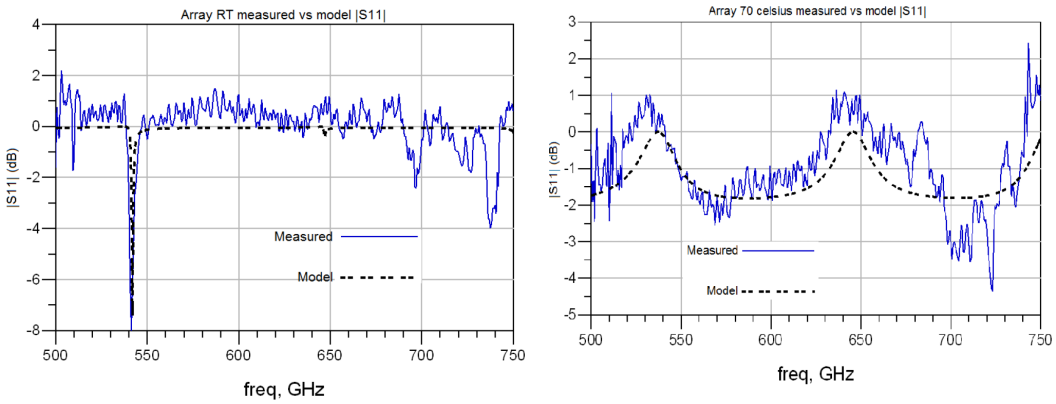



Figure G.8: (a) The magnitude of $S_{11}$ at room temperature in dB (semiconducting state). The absorption dip at 541 GHz shows coupling of the beam to the $VO_2$ film, (b) The magnitude of $S_{11}$ at 70 °C (metallic state). The absorption dip disappears which corresponds to the array being reflective.

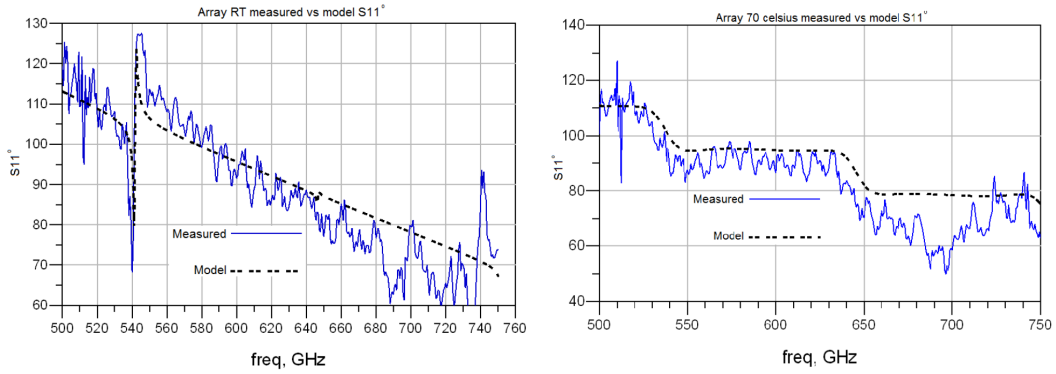



Figure G.9: (a) The phase of $S_{11}$ at room temperature in degrees, (b) The phase of $S_{11}$ at 70 °C.

## G.7 S21 Simulation

Based on the model and the results from the previous section, the transmission response ($S_{21}$) of the mask, shown in Fig. D10, can be predicted. As we can see from Fig. D10(a), there is a change in transmission across the band when the array is heated. The maximum modulation is obtained at 660 GHz and corresponds to a 28 dB change in transmission between the two states. We do note however that in the metallic state, the mask is not completely transmissive (insertion loss of 12 dB).

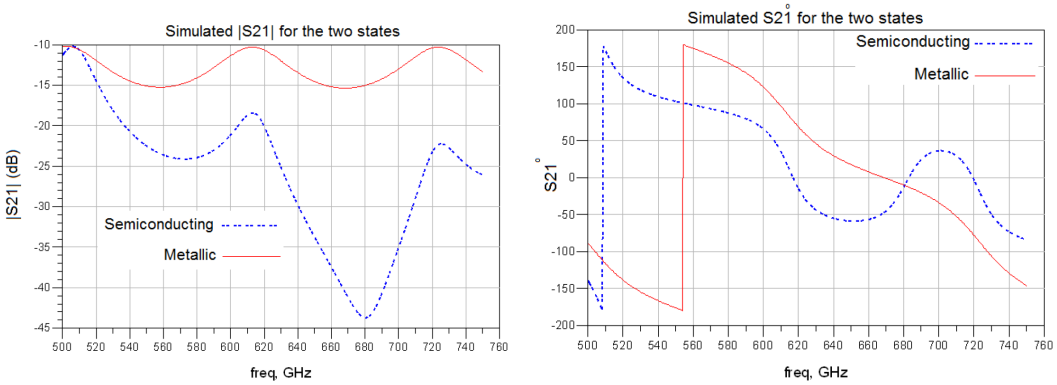



Figure G.10: (a) The simulated magnitude of $S_{21}$ for the semiconducting and metallic state, (b) The simulated phase (in degrees) of $S_{21}$ for the semiconducting and metallic state.

## G.8 Optically Induced Switching

The transition of the $VO_2$ can also be triggered optically using laser illumination. An experiment was set up to demonstrate this. As the power of the laser used is 30 mW and focused on fraction of the array, only a small portion of the $VO_2$ bridges will switch and others will not. By increasing the temperature to 60 °C, the array can be made to operate close to the switching transition. The reflection response at 60 °C is shown in solid blue (Fig. D11). The response under illumination at the same temperature is shown as a dashed line. Finally we increase the temperature to 70 °C switching the entire array (dotted red). As one can see, there is a change in $|S_{11}|$ of approximately 5 dB due to the laser. However, the optical flux in this experiment was not sufficient for a full transition to occur.

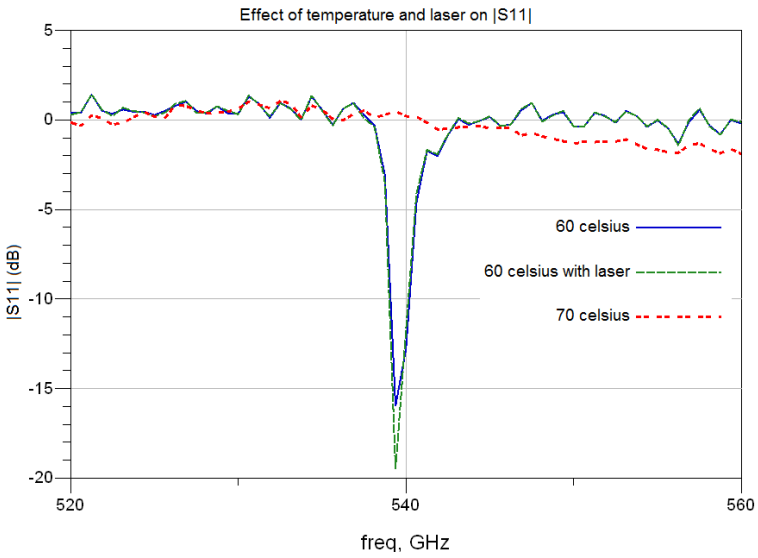



Figure G.11: $|S_{11}|$ measurement of the array that shows the effect of the laser and temperature. Upon illumination with the laser, there is a change is reflection of approximately 5 dB at room temperature . After increasing the temperature, we see that the array switches completely. Our conclusion is that the laser is not powerful enough and does not cover enough of an area to switch all the bowties.

## G.9 Conclusion

We have designed and characterized the reflection response of a bowtie antenna array coded aperture mask with $VO_2$ as the switching element. We have constructed a model for the array that is in good agreement with our measurement. Simulation of the transmission response of the mask shows that modulation of the transmission response between the two states is achieved over the WR-1.5 frequency band, with a maximum modulation of 28 dB at 660 GHz. We have also demonstrated the potential of switching the array optically using a laser.