Electronic Network Analyzer Calibration for Submillimeter Wafer Measurements

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Spencer Crump

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Abstract

Network analyzers determine the S-parameters of RF and microwave devices to describe their circuit behavior. Network analyzers require a calibration procedure to account for the systematic errors within the test environment to provide accurate measurements of devices under test. Coplanar wafer probes are prevalent in submillimeter network analyzer measurements and, due to their unshielded environment, are subjected to leakage at high frequencies. Additionally, coplanar wafer probes are prone to skidding, generating uncertainty about precise probe placement location which contributes to non-systematic errors that cannot be corrected through calibration. Electronic calibration has the potential to address these error sources to provide accurate network analyzer measurements.

This research aims to reduce the effects of calibration errors for on-wafer measurements. This work employs the nonlinear characteristics of a Schottky diode to realize an electronic calibration procedure for the frequency band WR2.2 (325-500 GHz). The electronic calibration reduces the number of variables associated with physically measuring individual calibration standards. This methodology has the potential to improve the accuracy of network analyzer measurements for high leakage systems, specifically coplanar wafer measurements.

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1 Introduction

The RF and microwave communities heavily rely on vector network analyzers (VNAs) to obtain accurate information about devices under test (DUT). VNAs utilize reflectometers to separate the incident and reflected voltage waves of the DUT. The VNA then determines the magnitude ratio and phase difference of the waves to calculate the scattering parameters (S-Parameters), widely used parameters for RF and microwave measurements, of the DUT. A description of load reflections and a definition of S-parameters can be seen in figure 1.

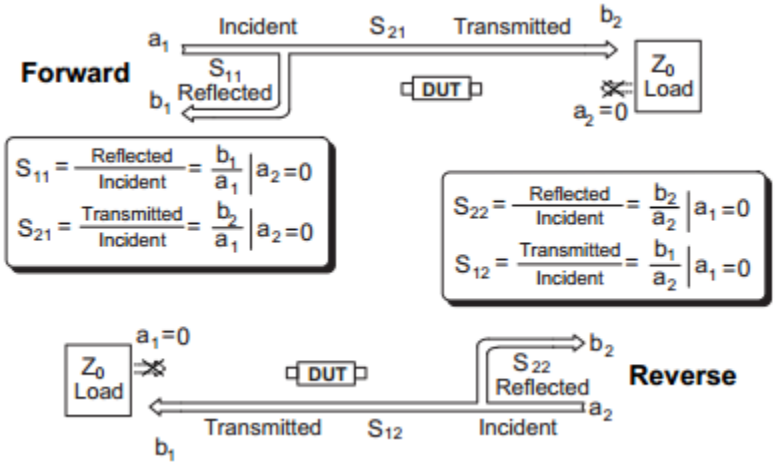

Figure 1. A definition of S-parameters as described by standing waves [1].

At high frequencies, the standing waves vary over the transmission line causing different RF characteristics for the same test measurement depending on the location of a reference plane. Therefore, VNAs require the establishment of a reference plane to relate the measured values to a common phase. Variations in the reference plane will influence the network analyzer measurements accordingly. If the reference plane variations occur during the calibration process, the reference errors will proliferate through to the measurements of the DUTs. A system outlining the importance of setting a reference plane can be seen in figure 2.

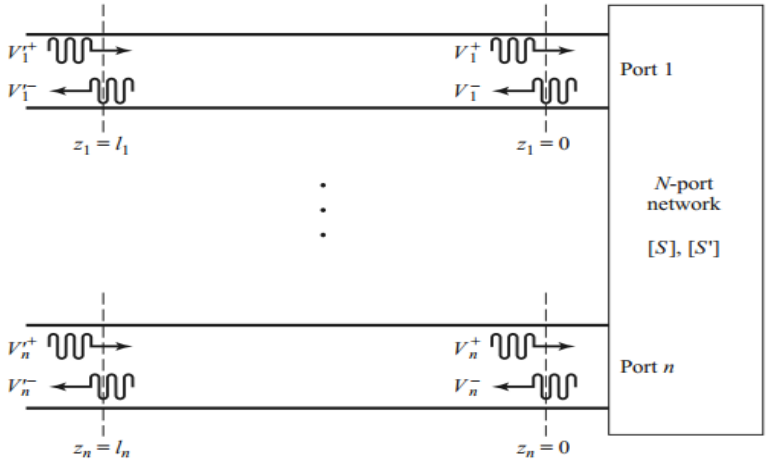

Figure 2. The effects of standing waves. This emphasizes the use of an established reference plane when making RF and microwave measurements [2].

The effects of standing waves contribute several sources of systematic errors within the test environment. Every connector transition, cable length, and non-idealities within the VNA or reflectometer can contribute systematic errors into test environment. These systematic errors are modelled as one, all-encompassing error network that covers all the RF effects from an "ideal" reflectometer to the reference plane of the DUT.

1.1 One Port Network Analyzer Calibration Techniques

There are several techniques for calibrating VNAs but all the methods aim to determine the effects of the error network associated with the non-idealities and scattering between an ideal reflectometer and the DUT. Figure 3 displays the model of the test system for one port VNA calibration.

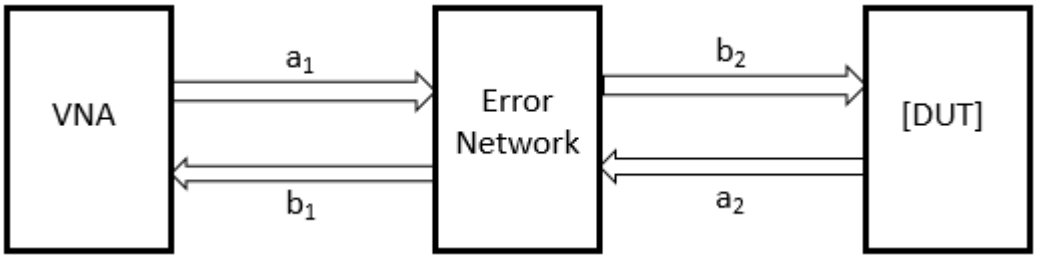

Figure 3. The block diagram of a one port VNA calibration. The error network encompasses everything between the ideal reflectometer within the VNA to the DUT. The error network is a two port network described by an error matrix derived from the input and output wave amplitudes, a and b.

The relationship between the VNA, DUT, and error matrix can be determined mathematically using signal flow graphs. The error matrix consists of the S-parameters E_{11}, E_{21}, E_{12}, E_{22} which describe the reflections seen at each port as well as the forward and reverse gain of the error network. A signal flow graph determining the effects of cascading S-parameters derived from calibration model described in figure 3 can be seen in figure 4. The signal flow graph in figure 3 yields equation 1.

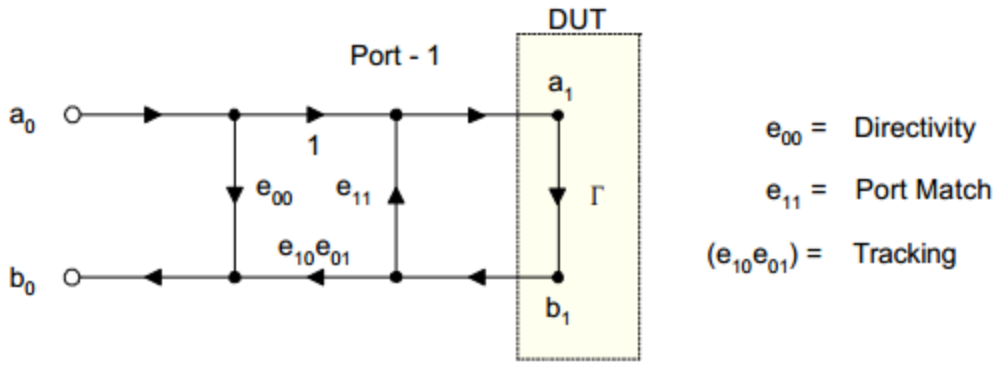

Figure 4. The signal flow graph of a one port calibration test environment [3].

$$S_{11VNA} = E_{11} + \frac{E_{12}E_{21} * S_{11DUT}}{1 - E_{22} * S_{11DUT}} \qquad (1)$$

The S_{11VNA} is the S-parameter measured by the VNA while the parameter of interest is the "true" reflection coefficient of the device or S_{11DUT}. A calibration process is necessary to determine the error coefficients listed in equation 1 and is accomplished through the measurement of known standards. If there are a sufficient number of unique loads, whose reflection coefficients are known, then the measured reflection from the VNA can be used to determine these error coefficients. The E_{12} and E_{21} terms always appear as a product, resulting in three unique unknown error terms. This produces a system of equations that requires a minimum of three unique known loads to be measured for the test environment to be calibrated.

Different calibration techniques utilize different sets of loads to determine the error coefficients. The most commonly used method, the SOL calibration technique, employs a short, open, and a matched load as the standards [4]. These loads have different and well-separated known reflection coefficients which makes this solution the simplest to implement. This measurement is done for the entire desired frequency range and a unique error matrix is stored within the VNA for each frequency point. When the DUT is measured, the known error coefficients are then applied to the measured S_{11} to yield the true S_{11} of the device. A related method for one port calibration is the SDDL technique. This calibration method employs four measurement standards but requires less known information about some of the standards [5]. The SDDL methodology utilizes a short, two delayed shorts, and a matched load for the standards. The short and matched load are the same as in the SOL technique but the two delays realize a unique load through the phase difference between each delay measurement. The phase difference arises from a difference in electrical length between each delayed short. The reflection magnitude of the delay-

delay standard is known and the difference in the measurements allows for the phase of the reflection to be determined, thus generating sufficient information to calibrate the one port test environment.

1.2 Two Port Network Analyzer Calibration Techniques

Two port calibration methods have the same basic goal as one port calibration, to determine the coefficients of the error network. However, this becomes more complex due to the second reference plane of the second measurement port. Figure 5 illustrates the added complexity of the network system developed for two port calibration.

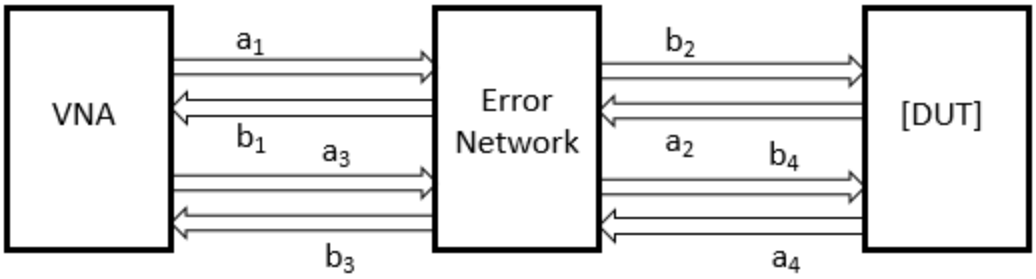

Figure 5. The block diagram of a two port VNA calibration. The error network encompasses everything between ideal reflectometers within the VNA and the DUT. The full error network is a four port network described by an error matrix consisting of sixteen error coefficients.

A full error matrix of the error network contains sixteen error coefficients, however, many of these error terms have little effect in many practical measurement situations so less complicated 8-term and 12-term error models are often employed to simplify the calibrations process [3]. The most commonly used two port error model is the 12-term model which assumes the two ports are externally isolated from one another but also assumes some leakage errors occur within the network analyzer [3]. The 12-term error network model is illustrated in figure 6. These assumptions are practical for measurements involving coaxial or other enclosed media due to the low external leakage of these types of measurement environments. Calibration procedures for 12-term error models commonly follow SOLT or TRL techniques.

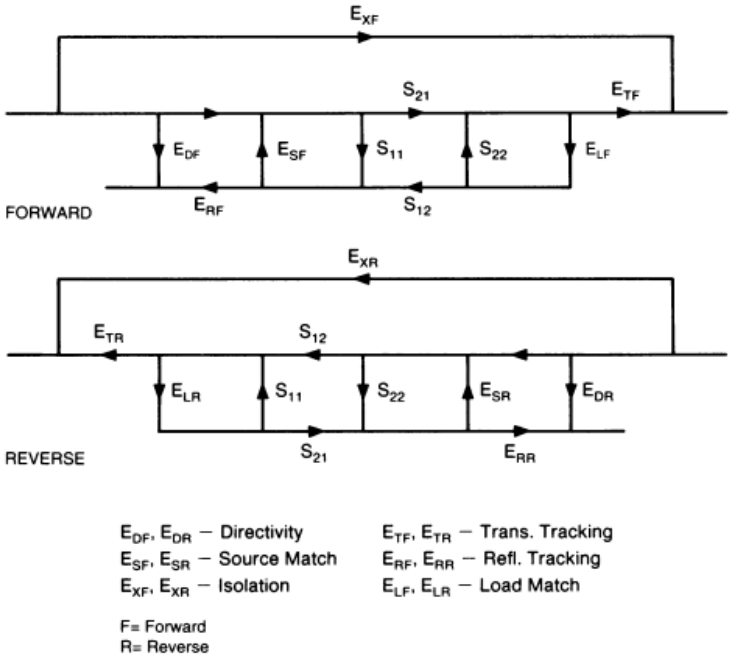

Figure 6. The two port 12-term error model. The forward model shows all the errors associated with the forward path of port 1 to port 2 while the reverse model displays the errors associated with reverse path of port 2 to port 1 [6].

The SOLT technique is similar to the SOL one port calibration procedure but a fourth standard is measured to account for the additional error terms [3]. Each port is calibrated with the usual short, open, and load, exactly the same procedure as in one port calibration. Both the open and short loads account for two error terms each (one term for each port) for a total of four determined error coefficients. The load measurement accounts for an additional 4 error terms; two error coefficients come from measuring the reflection at each port individually, and the last two terms come from the isolation measurement. The isolation measurement measures the leakage directly from port 1 to port 2 when each port is terminated with their own matched load. For most modern, commercial network analyzers the isolation leakage is often assumed to be negligible and is only necessary for measuring devices with very low return loss or insertion loss. The last four error terms are determined from the through measurement which can be done by directly connecting each port together. For the through measurement, each port measures the reflection of the through as well as the forward and reverse transmission between the two ports.

The TRL calibration technique emerged from the difficulty of making accurate, discrete loads for high frequency measurements [6]. TRL calibration can be accomplished through the use of transmission lines as standards. This approach reduces the difficulty in manufacturing wide bandwidth standard

loads and is applicable to a wide range of transmission media. TRL typically accounts for ten error coefficients but can be used to satisfy the 12-term error model. The through and the line measurements each account for four error terms each while the reflect measurement accounts for the last two error terms [6]. The through and line standards measure the reflection and forward/reverse gain of each port, resulting in 4 error coefficients each. The reflect standard is typically made with an open or a short due to the ease of implementation within transmission lines. The same reflection must be presented to both port 1 and port 2 of the VNA. The remaining two error terms come from the isolation measurement, similar to the SOLT calibration technique. To account for the isolation measurement, the network analyzer measures the leakage between the two ports when no load is connected to the ports. Again, this leakage error can often be assumed as negligible.

The simplest two port error model is the 8-term model that assumes that the two ports are ideal and completely isolated from one another [3]. The leakage between the two ports can often be negligible for coaxial measurements while the port isolation is dependent on the isolation factor of the reflectometers within the network analyzer. Simple measurements done with precise analyzers can safely assume the errors to have little effect on the overall calibration. The 8-term error model is commonly employed by the TRL calibration procedure. As previously mentioned, the standard TRL calibration procedure accounts for 10 error terms, supplying additional equations to determine the 8 error coefficients. The extra measurements are then used to determine supplemental properties of the standards measured, specifically, the propagation constant of the line standard and the complex reflection coefficient of the reflect standard [6].

The 16-term error model is the most general two port error model and accounts for all possible error coefficients present. This calibration methodology makes no assumptions about negligible leakage errors and therefore accounts for all 16 error coefficients. Figure 7 shows the error network for the 16-term two port error model. This error model is advantageous in describing leakage prone test environments; it is suitable for coplanar test measurements with unshielded wafer probes. This test environment is susceptible to many of the errors depicted in the full 16-term model. The error network is determined by making four separate measurements on four unique loads. The four measurements consist of the reflections from each port and the forward/reverse gain of each unique load; similar to the through standard within the 12-term error model. With four unique load standards, all 16 error coefficients can be determined.

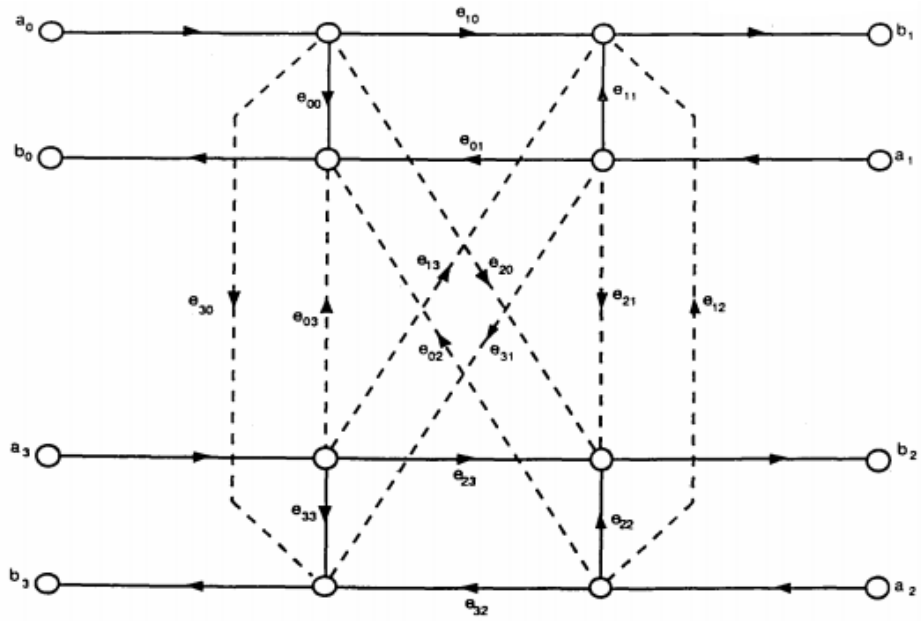

Figure 7. The two port 16-term error model. The model includes all possible sources of leakage errors between the two ports [7].

1.3 Goal of the Thesis

The goal of this research is to develop an electronic network analyzer calibration technique for submillimeter coplanar wafer measurements. The calibration methodology will exploit the voltage-dependent impedance properties of Schottky diodes to present a set of unique loads for performing standard calibrations. This research explores the measurement results for a calibration procedure conducted with quasi-vertical Schottky GaAs diodes, developed at the University of Virginia, operating within the waveguide frequency band WR2.2 (325GHz-500GHz). This work addresses shortcomings of current coplanar wafer calibration techniques by reducing the number of variables within the calibration test environment. This work employs diodes fabricated by Dr. Naser Alijabbari, Souheil Nadri and Linli Xie and builds off the calibration algorithms generated by Dr. Alexander Arsenovic. Also, this research follows coplanar wafer measurement techniques established by Dr. Matt Bauwens. This thesis is comprised of four sections:

1. Chapter 2 details the techniques of coplanar wafer measurement techniques. Additionally, Chapter 2 discusses the sources for error within the calibration procedure with an emphasis on error reducing methodology.
2. Chapter 3 discusses the procedure, application, and results of a one port electronic calibration procedure. The calibrated test results for several one port devices are compared

to the results from standard calibration procedures to validate and assess this new calibration process.

3. Chapter 4 discusses the procedure, application, and results of a two port electronic calibration procedure. The calibrated test results for several two port devices are compared to the results from standard SOLT calibration procedures to validate and assess the new two port calibration procedure.
4. Chapter 5 summarizes the research completed and discusses possible avenues for future work to build on this thesis.

2 Coplanar Wafer Measurement Techniques

Coplanar wafer measurements are used to characterize coplanar devices and circuits that have not been packaged into sealed housings with standard coaxial or waveguide interfaces. Typical coplanar wafer test pads are approximately 10 µm large, necessitating the use of microscopes and probing stations with gears to control slight movements of the microscopic probe tips [8]. Additionally, measurements within the waveguide WR2.2 frequency band are susceptible to leakage errors and repeatability inconsistencies. The systematic leakage errors arise from the design of the probing houses and scale of wafer circuits. The probe housing contains exposed metal probe tips that can radiate electromagnetic energy to nearby, conductive structures. Additionally, the size of the test structures causes the probes to be within close proximity to each other, increasing the likelihood of leakage in the test environment. The scale of the DUTs also contribute to non-systematic errors that arise from a varying reference plane. Taking multiple measurements to insure a consistent reference plane can be difficult due to the uncertainty of the location specific contact point between the test pad and probe tip. The development of standard loads within the WR2.2 frequency band is challenging due to the complexity of the manufacturing processes and available materials required to produce precise loads. This shortcoming has spurred the deployment of transmission line based calibration techniques for this frequency range. Transmission lines are easily manufactured to accurate dimensional specifications and are widely used because the impedance properties are dictated by the physical dimensions of the transmission line.

2.1 Coplanar Wafer Calibration Methods

Coplanar wafer calibration techniques have been developed to incorporate these manufacturing limitations. For one port calibration, the use of several (typically five) offset shorts or opens are deployed to realize the three unique loads required to solve the error network [8]. This is illustrated in Figure 8 and follows similar ideas proposed within the SDDL calibration technique where two offset shorts are capable of realizing a single load requirement. The use of 5 offset shorts requires that the electrical length between delay short 1, delay short 2, delay short 3, and delay short 4 all be unique. The resulting loads are derived from the original short and loads comprised of shorts with a phase offsets dictated by difference in electrical length between two delays. Lastly, the use of five delayed shorts generates four unique standards for a system of equations with only three error terms. The overdetermined system allows for the averaging of error coefficients from different combinations of standards. The averaged error terms provide more accurate information about the error network than

minimally determined systems. The overdetermined calibration process is common in coplanar wafer measurement environments to reduce measurement uncertainty and improve accuracy.

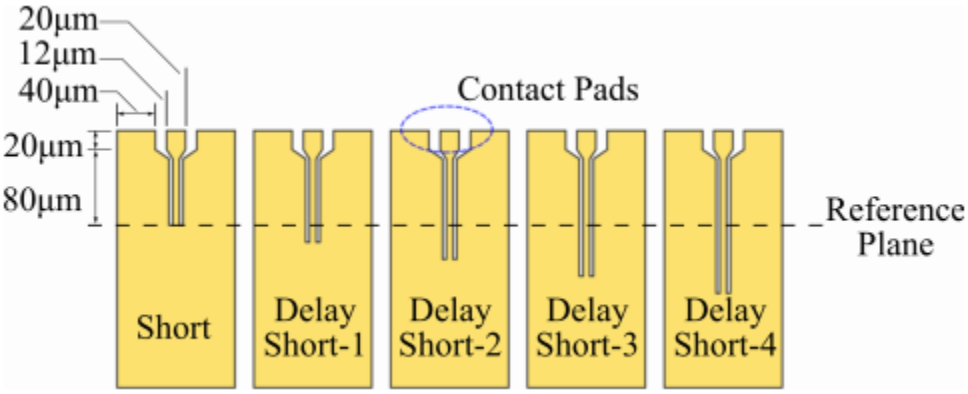

Figure 8. The use of 5 offset shorts as a one port calibration standard. This standard is realized through the development of CPW transmission lines, an easily fabricated standard for waveguide WR2.2 frequencies [8].

For two port coplanar wafer calibration, standard 12-term TRL calibration is often implemented because the load requirements can be realized through various CPW transmission line standards. This approach is useful for many measurement requirements but fails to encompass all the possible error terms. For measurements within the waveguide WR2.2 frequency band, cross port leakage can play a significant role in the calibration process. Coplanar wafer measurements contain openly exposed probes which potentially radiate directly between each other, without propagation along the transmission lines. The radiation potential increases for many two port measurements because of the scale under which these measurements are conducted. Figure 9 displays the test setup for two port coplanar wafer measurements [8].

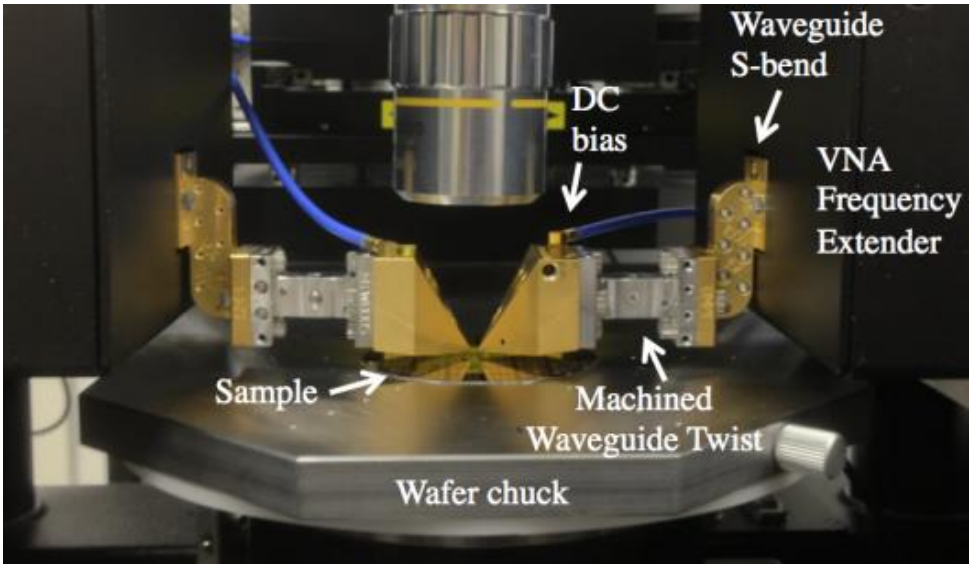

Figure 9. Coplanar wafer test environment. A two port measurement is being conducted on the wafer sample [8].

Current 16-term error models are realized through the deployment of four varying transmission line loads. A common methodology adopts a single through line and several reflect standards [7]. Technically, specifications for the standards deployed in the 16-term calibration procedure are limited, so any four unique, two port measurements will in principle calibrate the system. Most calibration procedures therefore use two port loads that are easiest to implement. Throughout this work, I will compare the electronic calibration procedure to calibration methodology that utilizes a through, a reflect, an open-short, and a short-open as the standards.

2.2 Coplanar Wafer Measurement Procedure

The process for performing coplanar wafer measurements must account for several components within the test environment. The probe tip follows the standard Ground-Signal-Ground (GSG) topology [9] shown in figure 10, with each tip point requiring contact with the DUT's test pads.

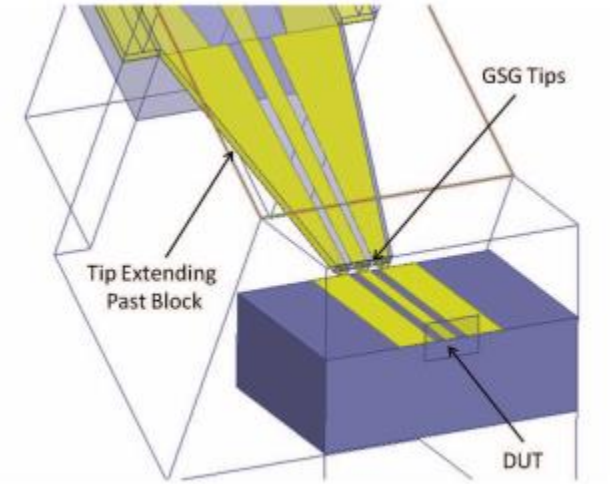

Figure 10. Model of GSG probe testing a DUT. This shows the exposure of the probe tips, leading to concerns of radiation leakage between two ports. The probe model also requires electrical contact for each probe tip.

To insure a stable electrical contact each tip of the GSG probe must be evenly pressed into the contact points. The probe tips leave slight indentations into the contact surface which can be viewed to insure the size and shape of each indentation is equivalent. If the indentations are the same then the pressure from the probe tip is applied evenly to each contact point, insuring a good electrical contact between the probe tip and the DUT. This is then verified by contacting the probe tip to a test pad and biasing the probe tip to measure the electrical conductivity of the RF transition surfaces.

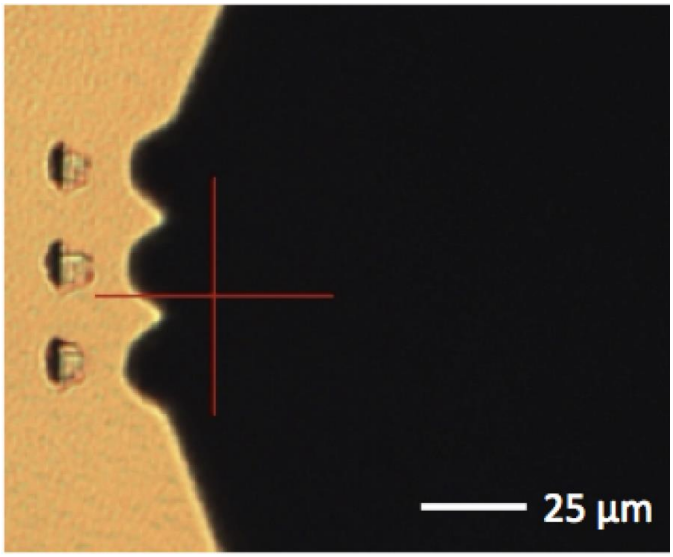

Figure 11. The indentations on the gold surface caused by the GSG probe tip (shaded object). The indentations are even in size and shape, insuring the electrical connectivity of the RF transition.

Figure 11 illustrates the "skid" marks, or indentations, created from the probe tip contacting the gold test pads [8]. These "skid" marks provide inconsistencies in contact location between the probe tip and test pad leading to the non-systematic errors described in further detail in section 2.3.2.

The remaining steps for coplanar wafer measurements involve calibrating the electronic probing station. The angle of contact and the force of contact greatly affect the coupling associated with the coplanar test pad to the probe, emphasizing the need for a calibrated electronic probing station. The probing station controls all three directional movements of the DUT and each directional movement needs to be calibrated to avoid damaging the probe tip or DUT. The probing station is calibrated by declaring reference points on the wafer test sample that enable the station to correlate directional movements of the probe tip. Additionally, the Align, Separation, and Overtravel settings must be determined to establish the contact force or degree of separation between the probe tip and wafer sample. The probing station significantly reduces the variability in wafer test measurements, however, the probing station can still generate unpredictable reference planes between multiple wafer measurements. Typically, the probe station controls the depth and length of the "skid" marks, however, these "skid" marks develop inconsistencies in the precise location of the contact point, generating the errors discussed in section 2.3.2. With the probing station calibrated, the test environment is ready to make wafer measurements for VNA calibration.

2.3 Sources of Error for Coplanar Wafer Measurements

There are several sources of error for coplanar wafer measurements in the waveguide WR2.2 frequency spectrum. The high operating frequency and small sizes of the DUTs provide an error prone test environment, subject to both systematic leakage errors arising from cross channel leakage as well as non-systematic measurement errors arising from the inconsistent reference planes.

2.3.1 Radiating Probe Tips

Due to the unshielded probe tips, on-wafer probes can radiate electromagnetic energy and this radiation leakage adds a source of error that can interfere with coplanar wafer measurements and calibration procedures. The exposed probe tip acts as an antenna and will radiate electromagnetic energy to other nearby devices. This error source can manifest itself in both one port and two port calibration. For one port calibration, the probe housing can radiate onto nearby, conductive structures on the coplanar wafer surface. The one port error model accounts for this error on the individual measurement level but if the radiating structure behaves differently for each measurement standard, non-systematic errors are introduced into the calibration. The non-systematic errors are symptoms of a changing test environment, and cannot be corrected by the error network calibration. For two port calibration, the changing test environment radiation can be caused by the probe tip for the second port. The second radiating probe, along with small dimensions of the DUT, create opportunities for cross channel leakage between the two radiating probe tips. These errors are unaccounted for in the standard 12-term TRL calibration methods but are accounted for in the full 16-term error model. Even in the 16-term error model, if the probe radiation effects each measurement standard differently, then the error network is not consistent and the calibration is no longer accurate. This leads into another source of error in network analyzer calibration for coplanar wafer measurements: calibration repeatability errors.

2.3.2 Connection Errors

The repeatability of the coplanar wafer measurements is not always consistent despite strict measurement procedures and electronic test stations. This non-systematic error occurs in the measurement procedure as a result of inconsistencies between the point of contact of the probe tip and the coplanar wafer test pad. Performing coplanar wafer measurements requires the use of a microscope and a calibrated probing station to make accurate measurements. The microscope focuses on the contact pads of the DUT causing the probe tip to be out of focus as it rests directly above the wafer sample. This introduces uncertainty in probe location, distance of separation to the wafer test

pad, and precise location of contact point between the probe tip and coplanar wafer surface. This uncertainty can introduce variations in the reference plane by as much as 10 µm [8]. For typical wafer measurements, the effects of reference plane variation is minimal but for devices operating in the waveguide WR2.2 frequency band these variations can cause phase errors as large as 10 degrees. Non-systematic measurement errors occurring during the calibration process can propagate into the characterization of the DUT, corrupting any test results. Similar errors emerge from waveguide misalignments, leading to calibration methodology aimed at reducing these errors in waveguide systems [5]. Waveguide connectors can have misalignments as large as 100 µm which can greatly affect the return loss and phase error. The variation in reference planes result in non-systematic error coefficients between measurement standards. Introducing probing stations greatly reduces the effects of this error but, as previously mentioned, the problem still persists when taking multiple wafer calibration measurements. This research proposes a solution that eliminates these error sources by implementing a single load that can be tuned to produce the necessary load impedances to solve the entire error network. The single load results in less movement and less variability in the measurement process, reducing the effects of these errors.

2.4 The Diode as a Calibration Standard

A diode can serve as the calibration standard as it can provide a set of unique impedances through electronic biasing instead of mechanically measuring unique standards. The nonlinear aspects of the diode allow for the presentation of many unique loads using a single circuit. Biasing the diode in both the forward and reverse direction allows a wide array of loads to be presented to the network analyzer. Simulated results, for a low frequency proof of concept, of the diode model presented in [10] can be seen in figure 12. Figure 12 shows the significant variability of impedances of the diode at three different bias points. The wide range of impedances enable the diode to become a calibration load standard. Several of the loads overlap each other but that is not an issue unless the overlapping loads occur at the same frequency point; under this condition there are no longer three unique loads required to solve the error network.

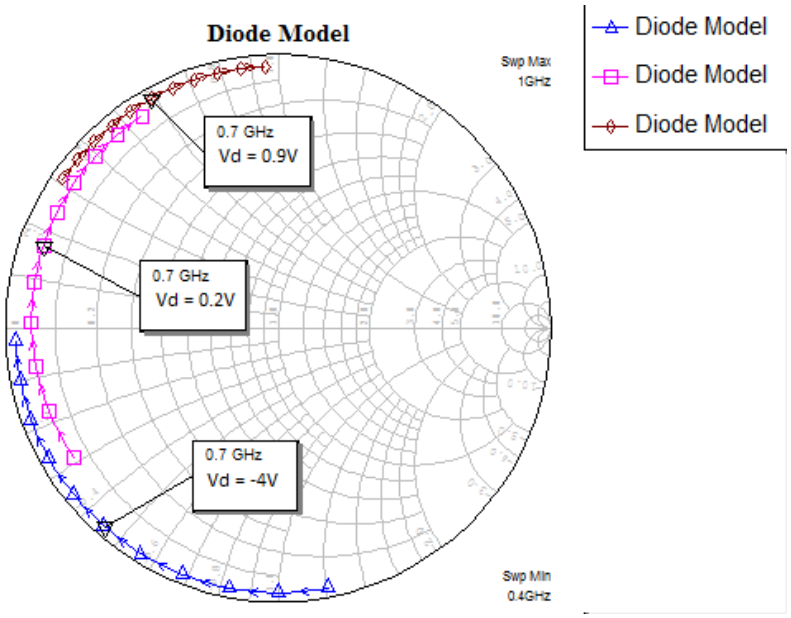

Figure 12. The impedance of a diode as characterized by the diode circuit model. The variance in impedance allows the diode to become the calibration standard.

The benefits of using a diode as a calibration standard come from the lack of mechanical movement during the calibration procedure. Measuring multiple load standards requires the movement of the test probe from one test point to another. The leakage errors associated with each measurement are not guaranteed to be equivalent nor is the contact transition guaranteed to be consistent. Reducing the need to mechanically alter the test environment allows for accurate calculations of the error coefficients. The increased accuracy is derived from the assumption that the bias voltage, and associated diode impedance, are more consistent than measurements done from mechanically varying the test environment during traditional calibration standards.

3. One-port Electronic Calibration

This chapter outlines the steps taken to verify and implement a diode as the standards for one-port network analyzer calibration. A low frequency proof of concept was tested to verify the implementation of a diode as a calibration standard. The layout of the diode calibration standard is shown in figure 13.

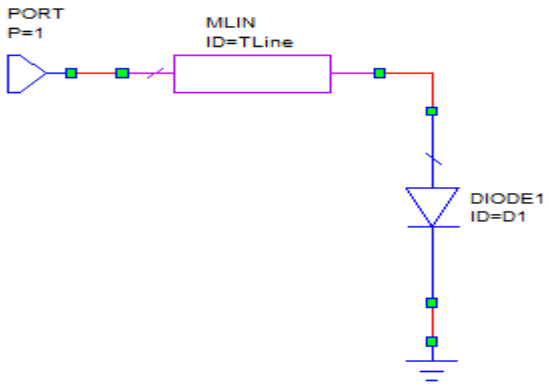

Figure 13. Circuit schematic for one port diode calibration procedure.

The diode calibration is then compared to standard, SOL calibration procedure to verify the effectiveness of deploying a diode as the load standards. This proof of concept encouraged the development of a wafer diode as the calibration standard for frequencies within the WR2.2 waveguide band. The measurement consistency of coplanar wafer diode calibration was compared to the consistency of standard, delayed shorts wafer calibration processes to determine the benefits of the error reducing effects of electronic calibration.

3.1 Low Frequency Proof of Concept

The proof of concept for implementing a diode as the load standards for one port network analyzer calibration was manufactured with surface mount components and assembled on a printed circuit board (PCB) composed of the dielectric material FR4. The proof of concept design utilized inexpensive and readily available components and manufacturing processes. The diode, part number SMTV 3002-SOT23 provided by Metelics, is connected to the VNA through SMA connectors and a microstrip transmission line [11].

3.1.1 Low Frequency Diode Characterization

The VNA test environment was first calibrated following the established SOL calibration procedure, then, the impedance of the varactor diode was measured. The diode presented a range of impedances to the VNA port based on the bias of the diode which is displayed on a Smith chart shown in figure 14. The impedances seen in figure 14 match those modelled in figure 10, verifying the diode tunability. The

impedance tunability enables the diode to be adapted as a calibration standard. The impedance for each bias point has an associated range of loads as the frequency varies. The calibration method is valid as long as the impedance of each bias point is unique for each frequency point.

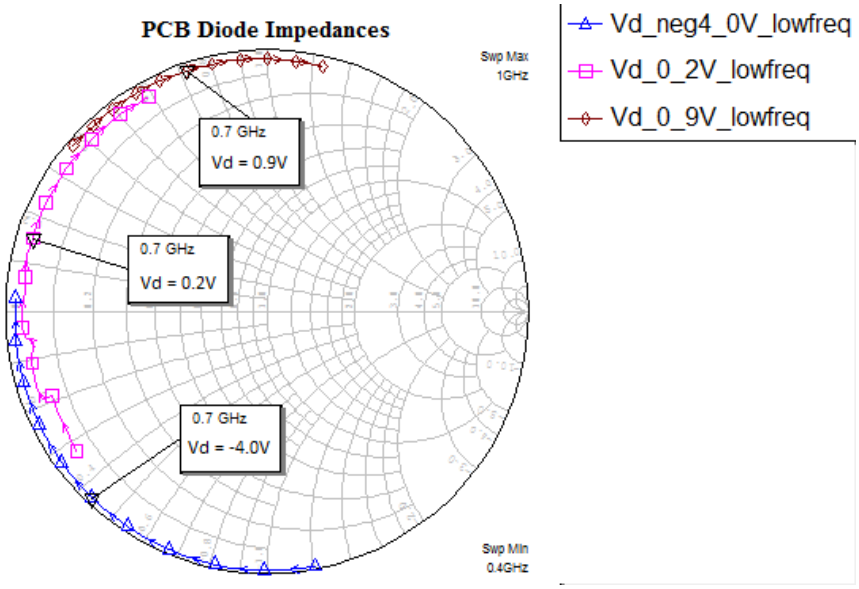

Figure 14. The impedance of a diode under the DC biases of -4V, 0.2V, 0.9V. The labels show the impedance range at a single frequency point (700 MHz) which allow for multiple standards to be derived from the single DUT.

3.1.2 Low Frequency Diode Calibration

After the diode had been characterized, it was re-measured and used to implement the standards for one port calibration. The S_{11DUT} values, from equation 1, are the known reflection coefficients of the DUT, which were determined by the calibrated reflection measurements seen in figure 14. The S_{11VNA} values, from equation 1, are the new re-measured, uncalibrated diode reflections allowing for all three error terms to be calculated. The characterized error network can then be applied to other uncalibrated devices to determine the true reflection coefficients of those devices. The uncalibrated devices are transformed by the known error matrix to produce accurate calibrated S-parameters of the DUT. The calibrated S-parameters, as determined from the diode calibration standard, were compared to the S-parameters derived from standard SOL calibration, for several different circuits. The circuits measured were a 50Ω resistor connected via a transmission line of unknown length, an open circuit connected via a transmission line of unknown length, and a diode biased to a unique bias point. The comparisons are displayed in figures 15, 16, and 17 respectively.

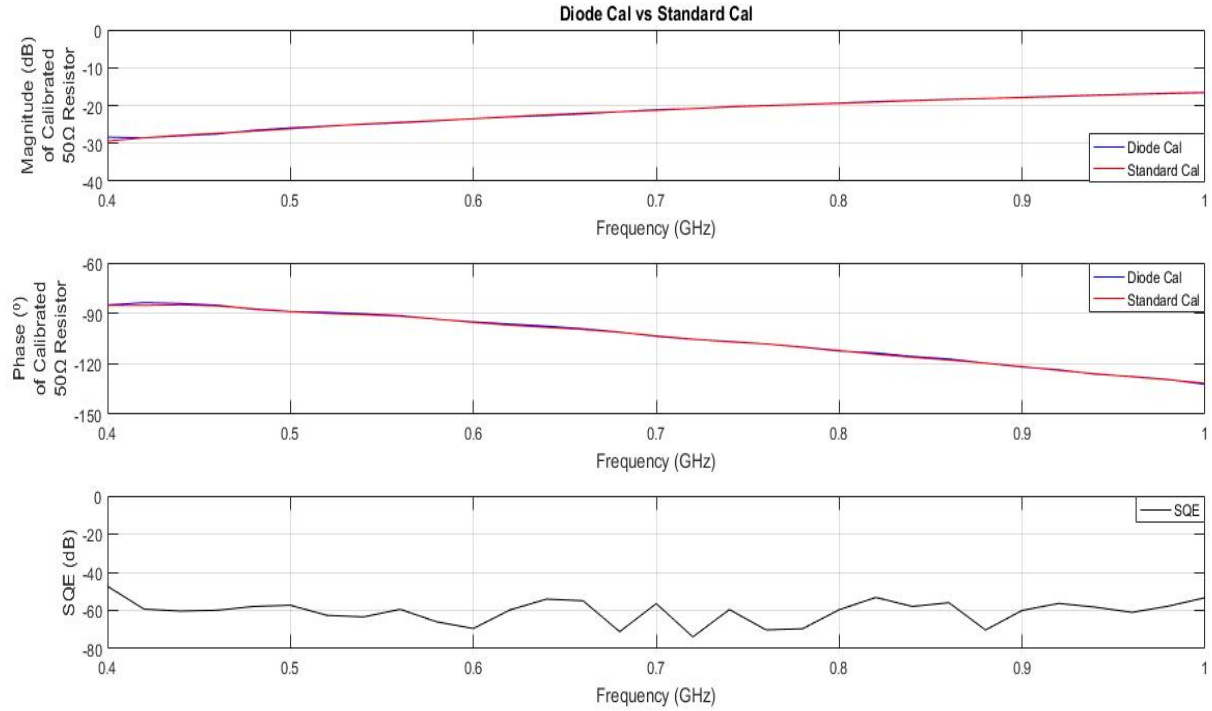

Figure 15. An offset 50 Ohm resistor is measured through two different calibration procedures. The magnitude and phase, as determined by each calibration method, of the offset 50 Ohm resistor is plotted as well as the mean square error of the calibration differences. The results show the diode calibration standard provides accurate measurements.

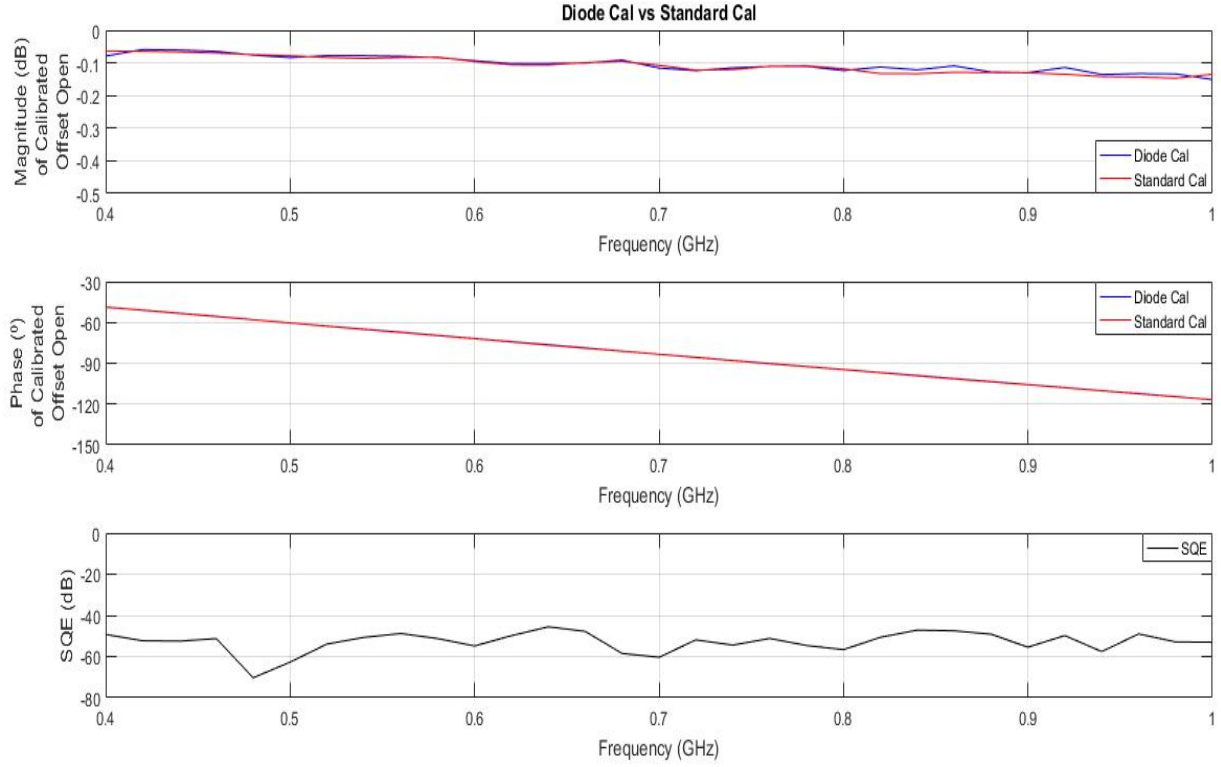

Figure 16. An offset open circuit is measured through two different calibration procedures. The magnitude and phase, as determined by each calibration method, of the offset open is plotted as well as the mean square error of the calibration differences. The results show the diode calibration standard provides accurate measurements.

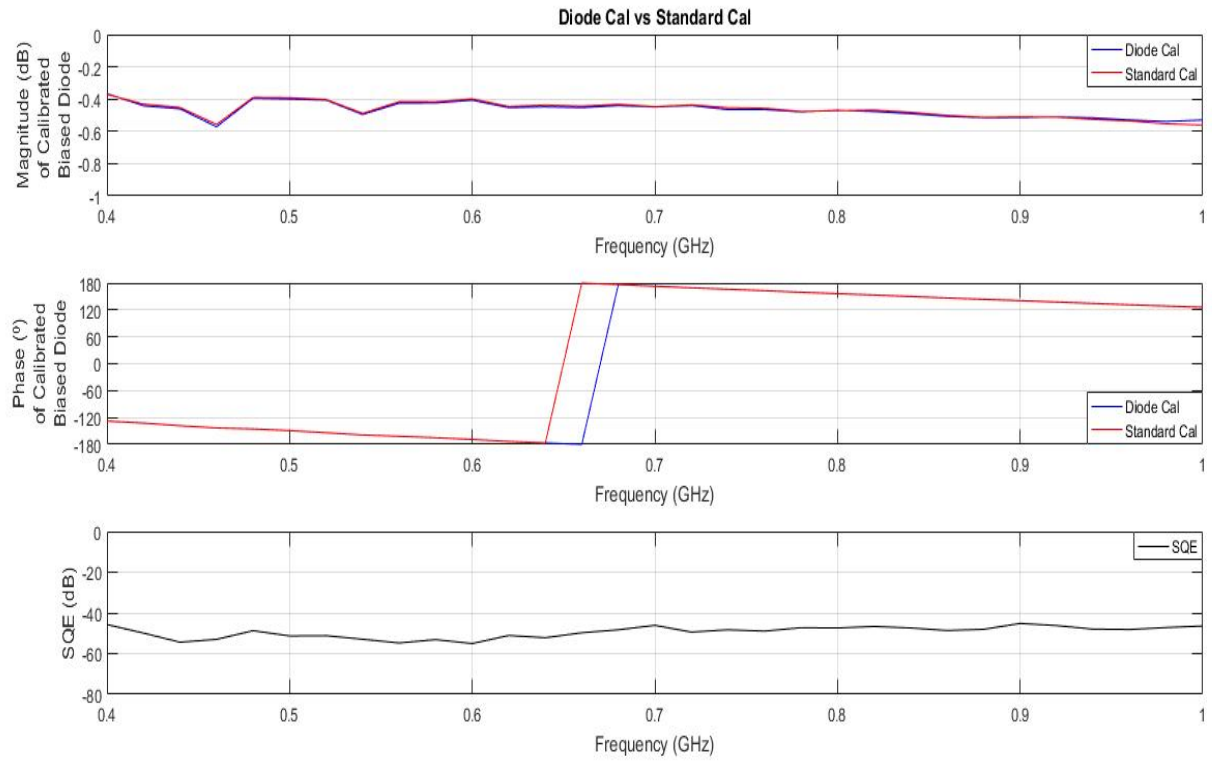

Figure 17. A uniquely biased diode is measured through two different calibration procedures. The magnitude and phase, as determined by each calibration method, of the biased diode is plotted as well as the mean square error of the calibration differences. The results show the diode calibration standard provides accurate measurements

The difference in the calibration procedures is very minimal, with squared error values ranging from -45dB to -75dB, proving the effectiveness of employing a diode as the calibration standard. The squared error values were determined from equation 2, seen below.

$$Squared\ Error\ (dB) = 10 * log_{10}(|\Gamma_{Diode} - \Gamma_{Standard}|^2) \qquad (2)$$

The diode calibration provided accurate measurements for a variety of devices allowing for the further development of a diode as the standard for one port on-wafer calibration.

3.2 Wafer Diode Calibration

Coplanar wafer diodes operating in the WR2.2 frequency band have been fabricated at the University of Virginia for a number of years. Planar diodes used in this work have been fabricated by Dr. Naser Alijabbari, Linli Xie, and Souheil Nadri and have consistently provided stable RF characteristics with minimal parasitic elements [12]. The high frequency Schottky diodes behave similarly to their low frequency counterparts; consequently, the diode calibration procedure follows the same process laid out under the low frequency proof of concept calibration.

3.2.1 Wafer Diode Impedance

First, The VNA test environment was calibrated with a set of offset shorts, standard practice for one port wafer calibration. The diode was then measured to determine the range of impedances achieved under different bias conditions. The impedance of the diode under different bias points over the entire WR2.2 frequency range is shown in figure 18.

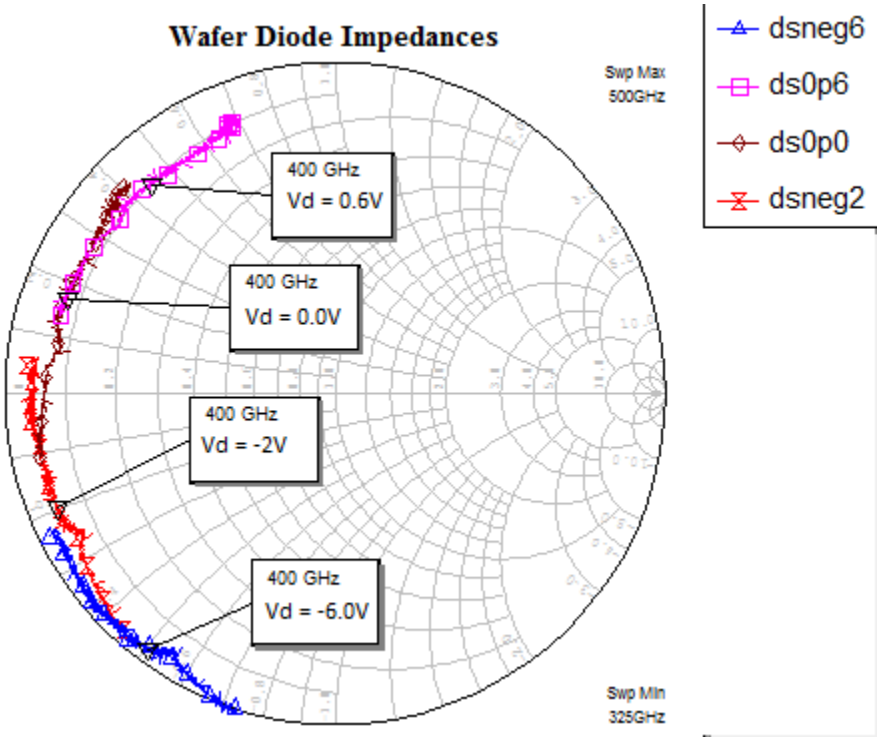

Figure 18. The impedance of a diode under the DC biases of -6V, -2V, 0.0V, 0.6V. The labels show the impedance range at a single frequency point (400 GHz) which allow for multiple standards to be derived from the single DUT.

The range of impedances shown allows for the diode to be used as a reliable standard for one port calibration procedures. Additionally, the impedances of the bias points do not overlap at any frequency within the entire bandwidth, insuring the usefulness of the diode as the calibration standards.

3.2.2 Wafer Diode Calibration

After the coplanar wafer diode is characterized, it was re-measured and used as the standards for one port calibration. Following the procedures described in section 3.1.2, the S_{11DUT} and S_{11VNA} values from equation 1 are known, allowing for the determination of the error terms. This process calculates the effects of the error network, allowing for the characterization of unknown DUTs. Uncalibrated devices are transformed by the known error matrix to produce accurate calibrated S-parameters of the DUTs. The calibrated S-parameters, as determined from the diode calibration standard, were compared

to the S-parameters derived from standard wafer calibration, for an arbitrary circuit. The circuits measured were a second biased diode whose calibration comparisons are displayed in figures 19.

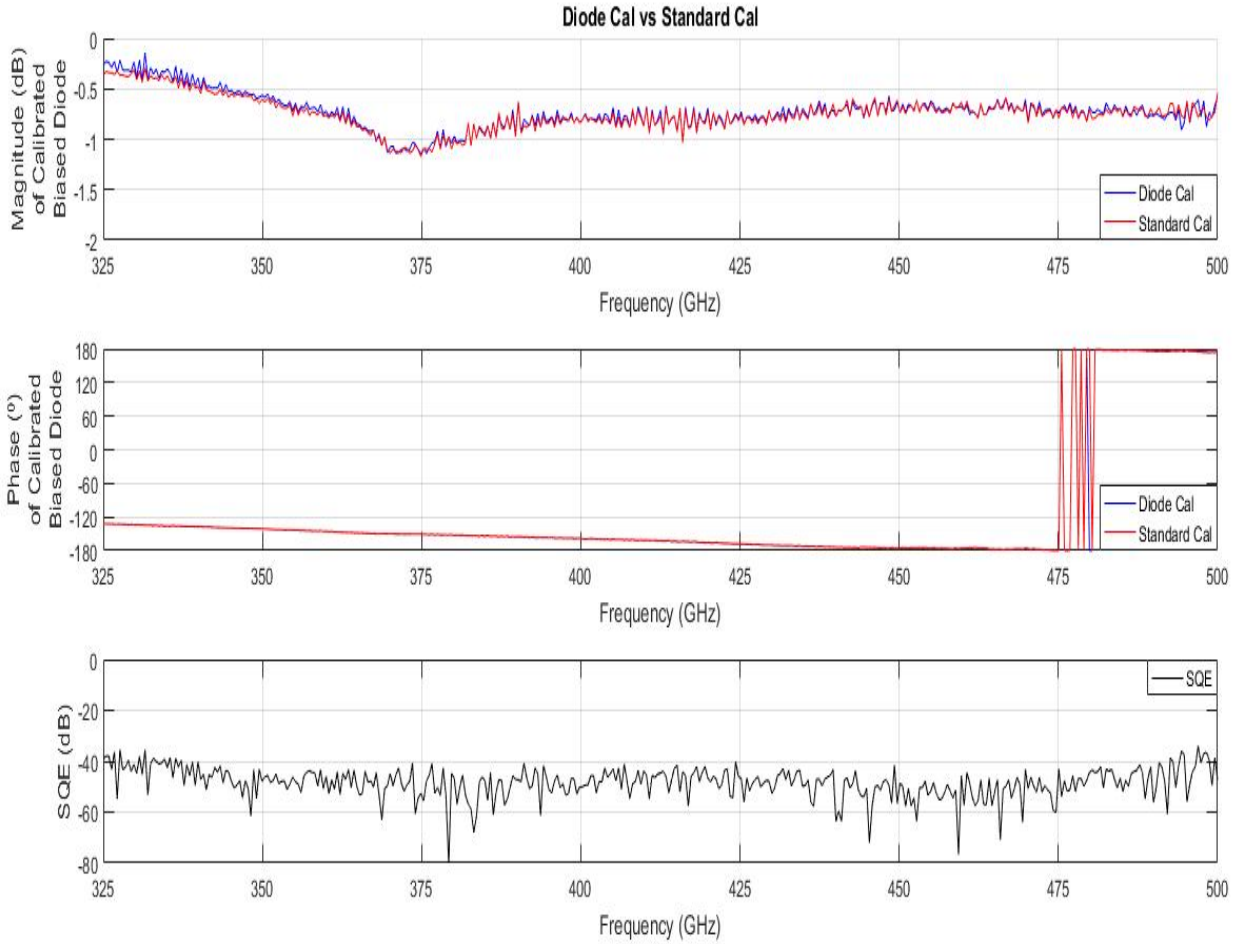

Figure 19. A uniquely biased diode is measured through two different calibration procedures. The magnitude and phase, as determined by each calibration method, of the biased diode is plotted as well as the mean square error of the calibration differences. The results show the diode calibration standard provides accurate measurements

The difference in the calibration procedures is very minimal, with squared error values ranging from -40dB to -70dB, proving the effectiveness of employing a diode as the calibration standard. These squared error values are similar to the ones seen in figures 15, 16, 17 but are slightly less correlated which can be contributed to the higher degree of uncertainty from the error prone test environment associated with high frequency, wafer measurements.

3.3 Repeatability Benefits of Diode Calibration

The previous measurements demonstrate that a diode can be a standard for one port VNA calibration but have yet to touch on the inherent benefits of a diode standard over traditional calibration standards. Those benefits arise from the lack of mechanical movement between measurements, reducing the variability and uncertainty between measurements. In traditional

calibration procedures, a series of offset shorts, opens, or a combination of the two are implemented, but for wafer measurements in the waveguide frequency WR2.2 band, extra standards are measured to reduce the effect of any non-systematic measurement errors or uncertainty in the response of standards, resulting in five or more impedance standards for typical one port calibration. The overdetermined system attempts to reduce the effects of the non-systematic measurement errors that may arise from inconsistent contact points and reference planes. The diode calibration procedure requires only one contact point to fully calibrate the test environment, eliminating any measurement variability associated with changes in the reference planes and contact points. The non-systematic measurement errors that arise from diode calibration are due to the accuracy and consistency of biasing the diode to present the exact same impedance. This possible error is dependent on the biasing power supply, which has accurate power control systems to provide consist output power. To verify the perceived benefits of employing electronic calibration, statistics about each calibration procedure were gathered. First, the usual wafer standards were measured multiple times with an emphasis of moving the probe tip between each measurement. Ideally, these measurements, and resulting error coefficients, will be identical, however, due to the non-systematic errors associated with the reference plane there will be a small variation in each measurement. Next, multiple diode measurements were conducted to determine the variance in impedance associated with any slight inconsistencies in diode biasing. The mean and variance for each error coefficient, for each calibration procedure, can be seen in figures 20, 21, and 22.

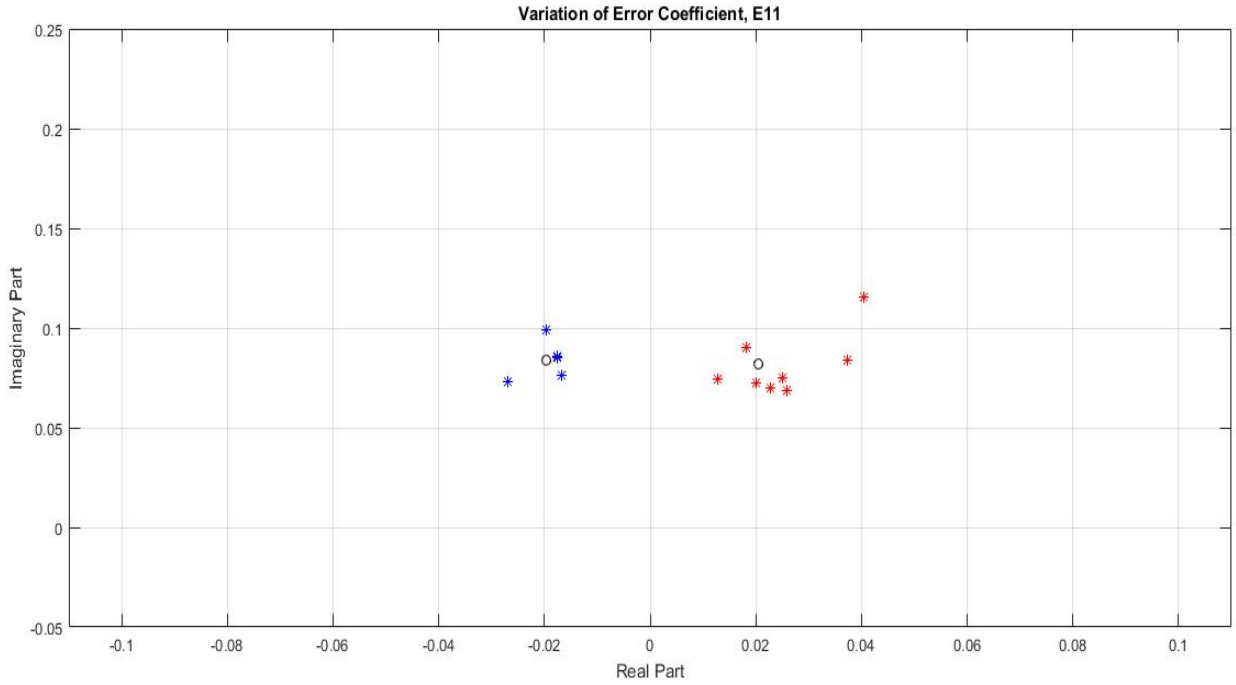

Figure 20. The variation of the complex error coefficients E11 at the 500GHz frequency point, derived from both standard calibration procedures as well as electronic calibration procedures. The E11 error coefficients of the standard calibration consists of the mean (in black) surrounded by the individual coefficients shown in red. The E11 error coefficients of the electronic diode calibration consists of the mean (in black) surrounded by the individual coefficients shown in blue.

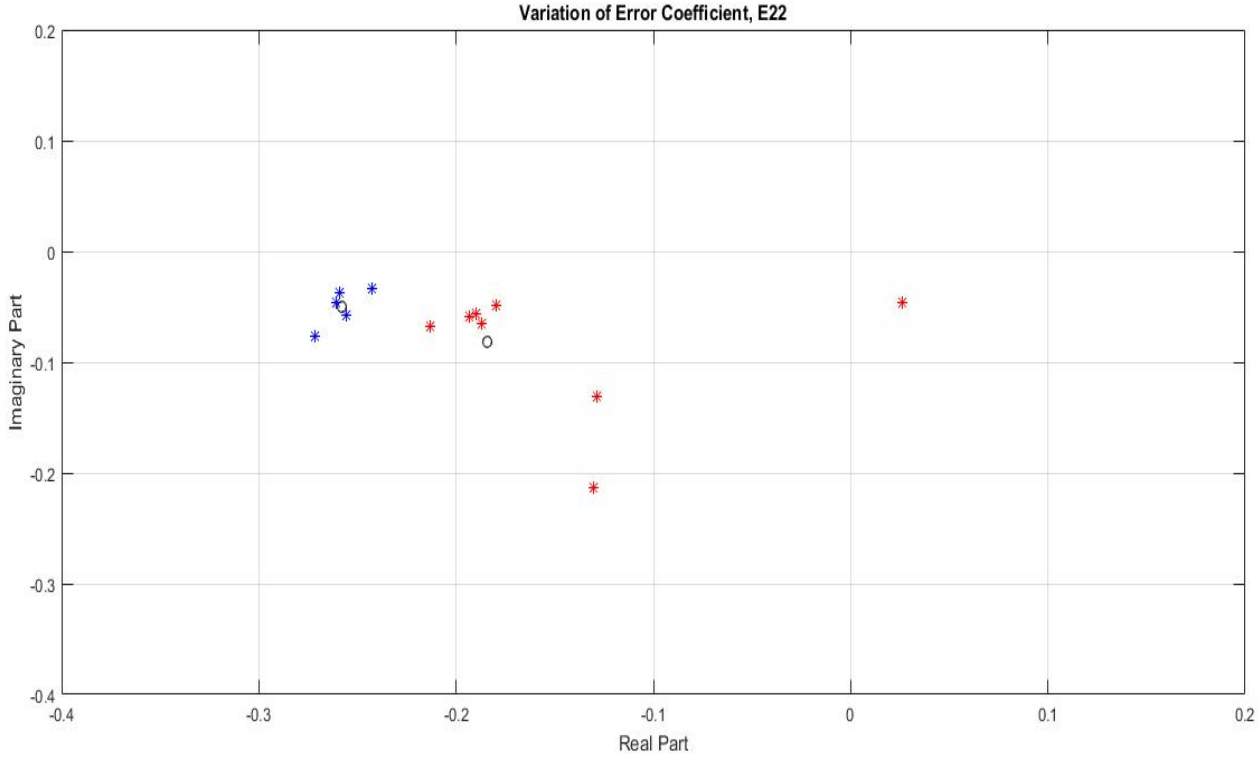

Figure 21. The variation of the complex error coefficients E22 at the 500 GHz frequency point, derived from both standard calibration procedures as well as electronic calibration procedures. The E22 error coefficients of the standard calibration consists of the mean (in black) surrounded by the individual coefficients shown in red. The E22 error coefficients of the electronic diode calibration consists of the mean (in black) surrounded by the individual coefficients shown in blue.

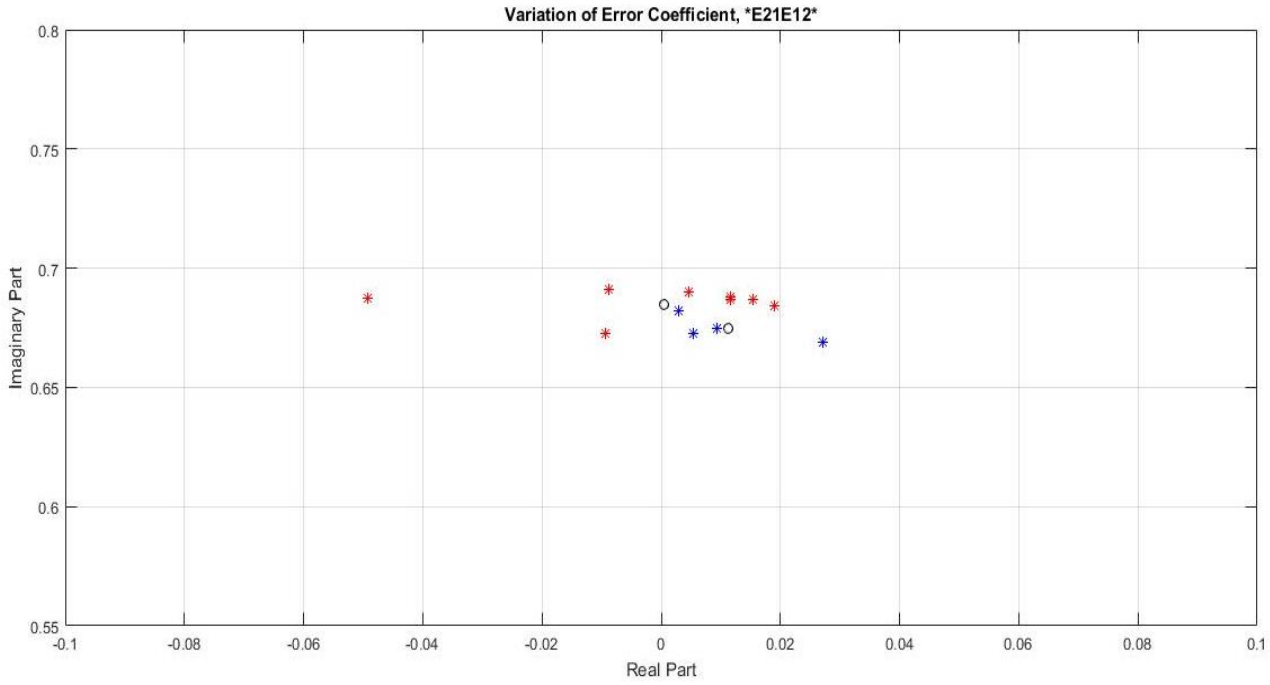

Figure 22. The variation of the complex error coefficients E21E12 at the500 GHz frequency point, derived from both standard calibration procedures as well as electronic calibration procedures. The E21E12 error coefficients of the standard calibration consists of the mean (in black) surrounded by the individual coefficients shown in red. The E21E12 error coefficients of the electronic diode calibration consists of the mean (in black) surrounded by the individual coefficients shown in blue.

The variation in error coefficients for diode calibration appear more tightly clustered than the error coefficients derived from standard calibration procedures. This perceived benefit occurs despite the effects of standard, overdetermined wafer calibration practices, which reduces the uncertainty in high frequency coplanar wafer measurements. Figures 20, 21, and 22 display the variance of the error coefficients at a single frequency point (500 GHz), however, the error coefficient variation persists over the full measurement bandwidth. The variances of each error coefficient, as calculated from equation 3, from typical calibration and diode calibration procedures are displayed in figures 23, 24, and 25.

$$Variance\ (dB) = 10 * log_{10}\left(\frac{\sum_{i=0}^{n}(|(x_i - \bar{x})|^2)}{n}\right) \quad (3)$$

These figures clearly show the reduced error coefficient variation in measurements for diode calibration, effectively reducing the effects of non-systematic errors introduced in the calibration procedure.

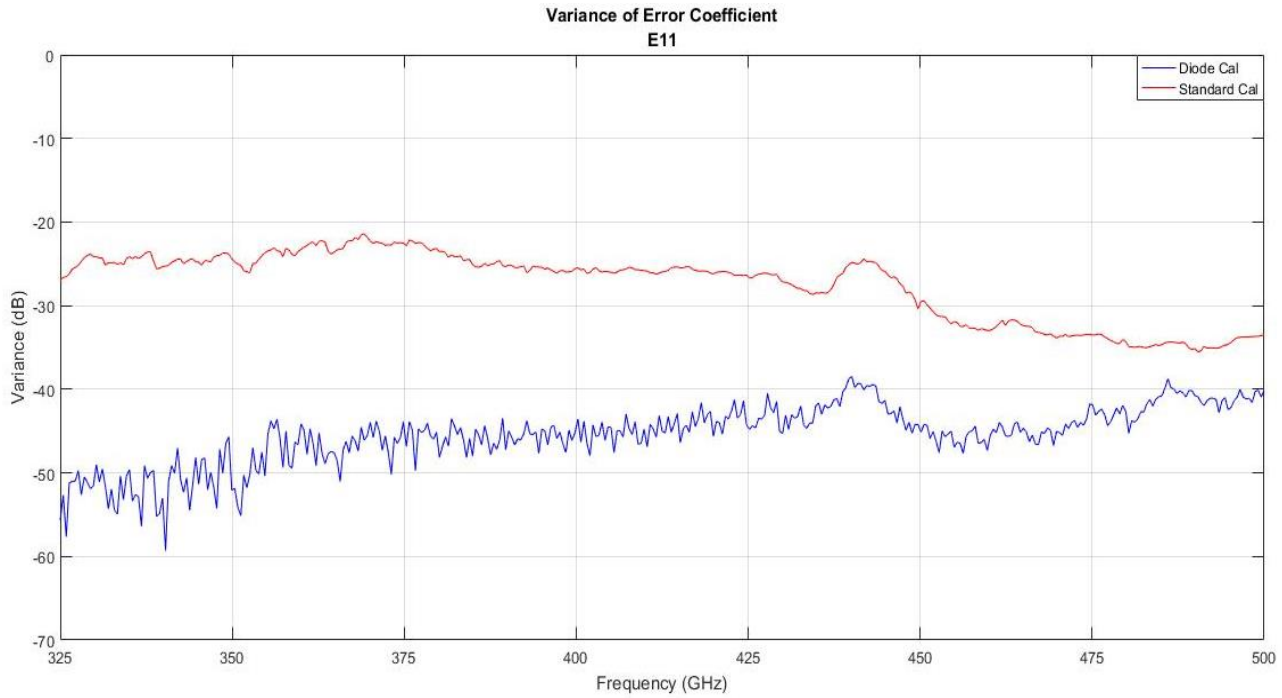

Figure 23. The variance of the error coefficient E11 between standard calibration and diode calibration procedures. The new, electronic diode calibration procedure improves consistency between coplanar wafer measurements.

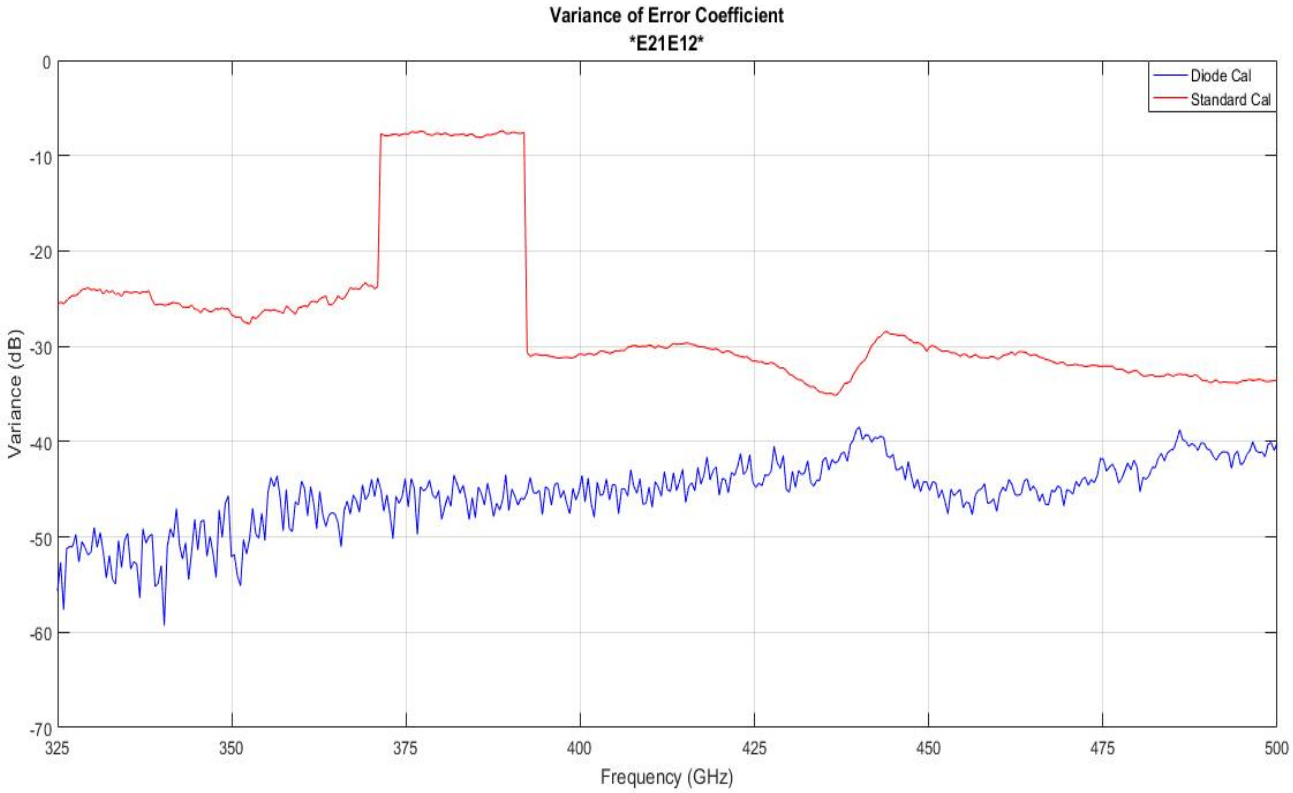

Figure 24. The variance of the error coefficient E21E12 between standard calibration and diode calibration procedures. The new, electronic diode calibration procedure improves consistency between coplanar wafer measurements.

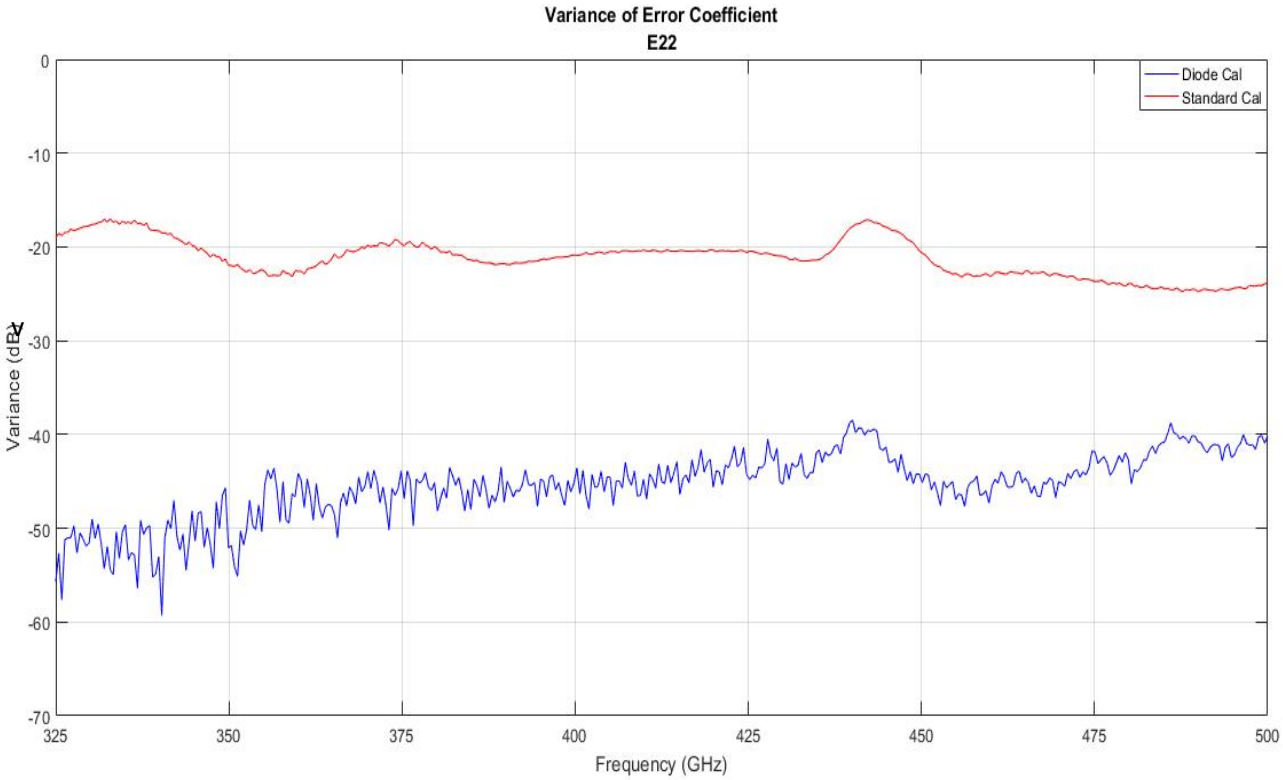

Figure 25. The variance of the error coefficient E22 between standard calibration and diode calibration procedures. The new, electronic diode calibration procedure improves consistency between coplanar wafer measurements.

The variance in error coefficients for the diode calibration range from -40dB to -60dB while the variance in error coefficients for standard calibration techniques range from -20dB to -35dB. The associated standard deviations for each calibration procedure range from 0.001 to 0.01 and 0.018 to 0.055 respectively. The measured variance in standard calibration techniques closely resemble those first explored by [13], whose standard deviation ranges from 0.02 to 0.04. The close association between standard calibration variances points to the validity of the improved consistency associated with the new electronic diode calibration technique.

4. Two Port Electronic Calibration

This chapter outlines the steps taken to verify and implement a diode as the load standards for two port network analyzer calibration. The impedance of two port diode circuits was modelled to determine the available S-parameters and a low frequency proof of concept was then tested to verify the implementation of a diode as a calibration standard. The circuit schematic for the two port diode load standard is displayed in figure 26.

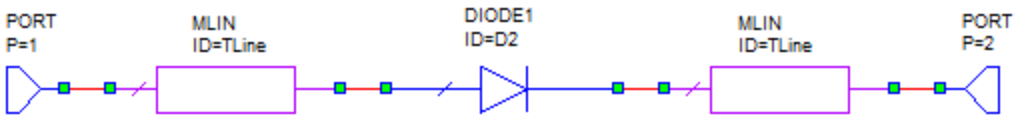

Figure 26. The circuit schematic for the diode load standard for two port calibration.

The diode calibration employed a full 16-term error model and is compared to the standard 12-term, SOLT two port calibration procedure to verify the effectiveness of deploying a diode as the load standards. The 16-term error model is satisfied through four measurements of each load standard; input reflection, output reflection, forward gain, and reverse gain. The unique load standards are generated from the four unique bias points of the diode. This low frequency diode calibration procedure scales to high frequencies, similarly to the one port calibration process.

4.1 Low Frequency Modelling

The diode has established impedance tunab3ility, from the one port calibration procedures outlined in the previous chapter, enabling the diode to be implemented as the standards for two port calibration. Following the same process described in section 3.1, a low frequency, proof of concept was developed utilizing the diode, part number SMTV 3002-SOT23 provided by Metelics [11], on a PCB with a dielectric material of FR4. The diode was connected in series to the two SMA port connectors and was characterized by measuring the calibrated s-parameters through the industry standard SOLT calibration procedure. The Smith chart in figure 27 shows the S-parameters of the diode for multiple bias points.

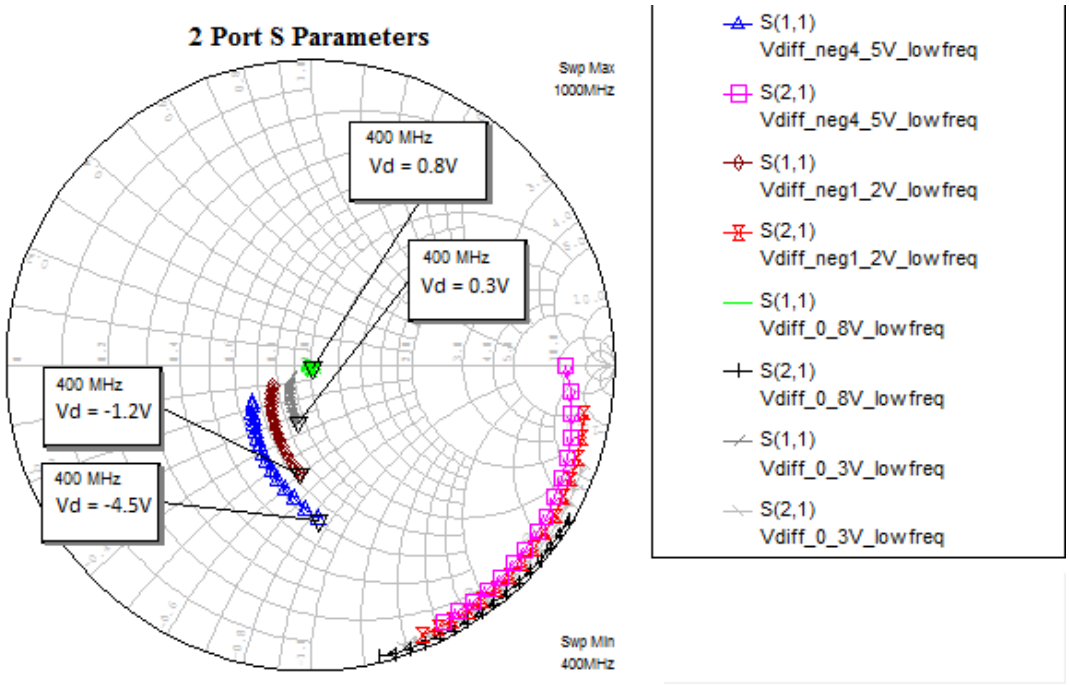

Figure 27. Two port S-parameters of a diode under different bias. The uniqueness of the impedances enable the diode to become the calibration standard.

The diode provides sufficient variability in impedances to implement as the calibration standards. The graph only shows a portion of the S-parameters under each bias point; this is due to the nature of the diode whose two port diode model is displayed in figure 28. In many practical measurements, such as low frequency test environments, the parasitic elements Cp, Ls, and Rs are often negligible in the overall characteristics of the diode. Removing these elements results in a symmetric, parallel RC circuit whose input S-parameters match those seen at the output, therefore, the S-parameters not shown in figure 27, the output S-parameters, match those displayed in the figure, the input S-parameters.

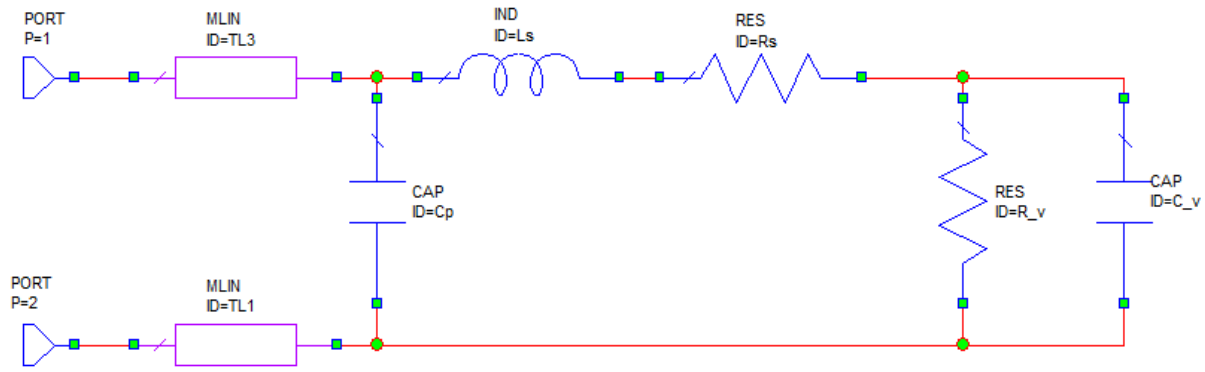

Figure 28. A two port diode model. Rj and Cj are the voltage dependent element provided by the P-N junction of the diode. The parasitic elements Cp, Ls, and Rs are derived from the packaging and connection leads of the diode. In many measurements the parasitic elements are negligible, resulting in a symmetric two port system.

The diode model, impedance variance, and the success of the one port calibration point to the success of implementing the diode as the calibration standard for two port VNA calibrations.

4.2 Low Frequency, Two Port Electronic Calibration

After the diode has been characterized, it was re-measured and used to implement the standards for two port calibration. The "ideal" values needed to solve the two port calibration algorithm are provided by the standard, SOLT, calibration measurements while the new re-measured, uncalibrated diode measurements provide the raw measured S-parameters. The combination of "ideal" and "raw" S-parameters provide enough information to solve the error coefficients within the system of equations generated from two port calibration procedures. This characterized error network is applied to other uncalibrated devices to determine the true S-parameters of those devices. The uncalibrated devices are transformed by the known error matrix to produce accurate calibrated S-parameters of the DUT. The calibrated S-parameters, as determined from the diode calibration standard, were compared to the S-parameters, derived from standard SOLT calibration. An uncalibrated, two port biased diode was measured with each characterized error network being applied to the biased diode. The difference in calibrated S-parameters, as determine by the squared error, of the two port calibration procedures are shown in figure 29.

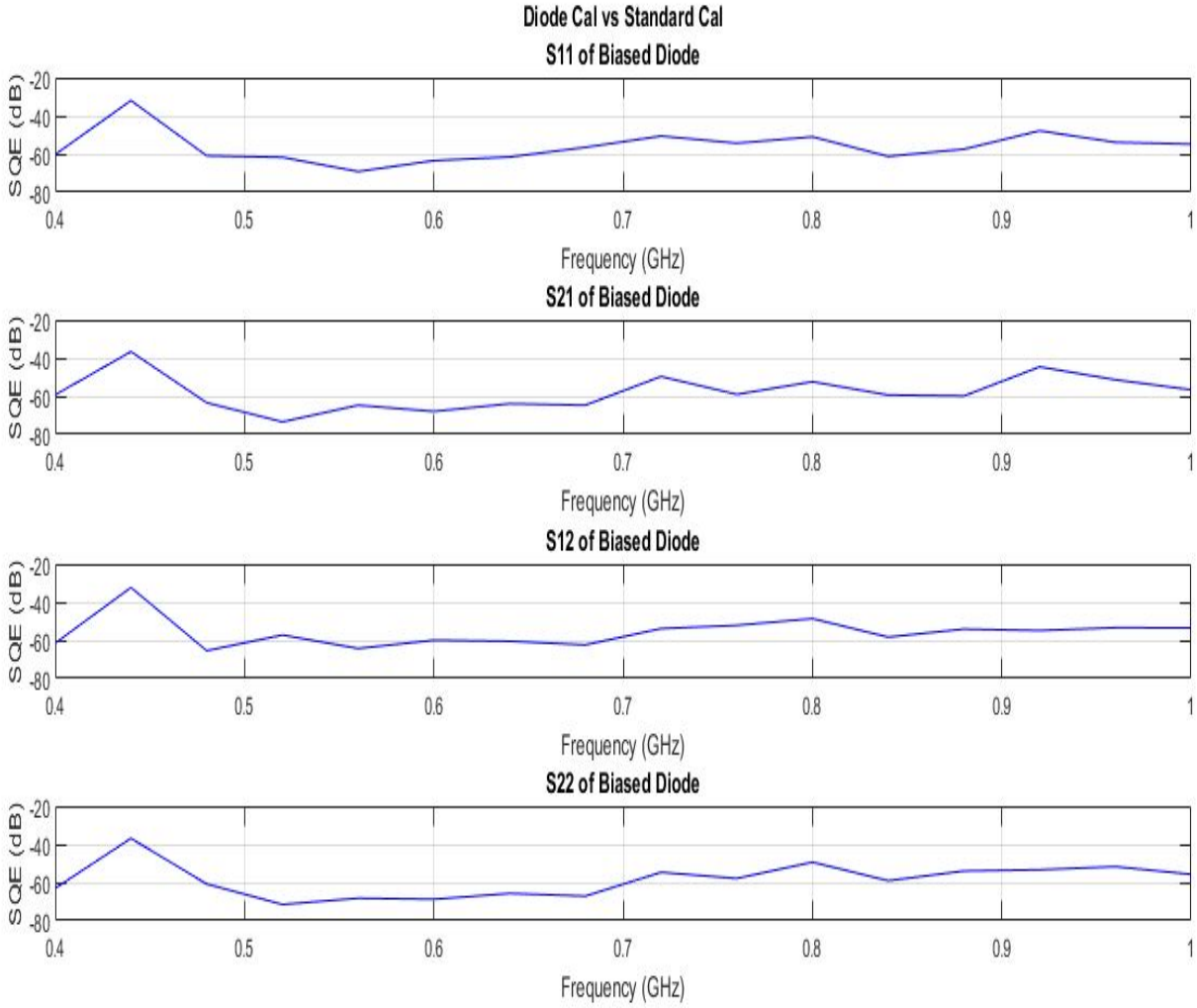

Figure 29. The squared error of the two different calibration procedures, Diode calibration and SOLT calibration. Each S-parameter is highly consistent for the two calibration procedures, enabling the success of a diode as a two port calibration standard.

The squared error for each S-parameter varies between -40 dB to -70 dB, proving the high correlation in calibration procedures. This result enables the diode to be implemented as the load standards for two port calibration. Additionally, the squared error values match those seen in one port calibration, encouraging the deployment of a diode as a two port calibration technique for coplanar wafer measurements operating within the waveguide frequency band WR 2.2.

5. Conclusion

The measurement results establish the diode impedance tunability resulting in satisfactory load standards for both one port and two port VNA calibrations. The nonlinear aspects of the diode provide sufficient loads to compute the associated error network from a single circuit. The single load circuit reduces the environmental variables, leading to more consist and accurate measurements. The error coefficients derived from the biased diode load standards are more consistent than those derived from the calibration load standards, verifying the underlying theory that electronic biasing leads to more precise impedances than physically measuring multiple load impedances. The high leakage, error prone test environment of unshielded wafer probes operating in the waveguide WR2.2 frequency range benefits most from the electronic calibration procedure. The diode calibration procedure reduces the environmental variables and uncertainty produced from high frequency VNA measurements in high leakage systems, resulting in more consist and accurate measurements.

5.1 Measurement Integrity

Throughout this thesis, there has been an emphasis on obtaining precise data and making accurate measurements to maintain integrity of the calibration methods. If the data collection was corrupted in any manner then the calibration results would yield incorrect conclusions.

5.1.1 Low Frequency Measurements

During the low frequency proof of concept for both one port and two port VNA calibration, the available VNA was not capable of providing bias to the diodes. To overcome this issue, bias tees and power supplies were incorporated into the test environment to properly tune the diode impedance. The diode biasing was implemented with a standard power supply and the bias tee PE1605, supplied by Pasternak [14]. To insure the bias tee does not leak DC power or noise into the measurement system, the S-parameters were measured and are displayed in figure 30.

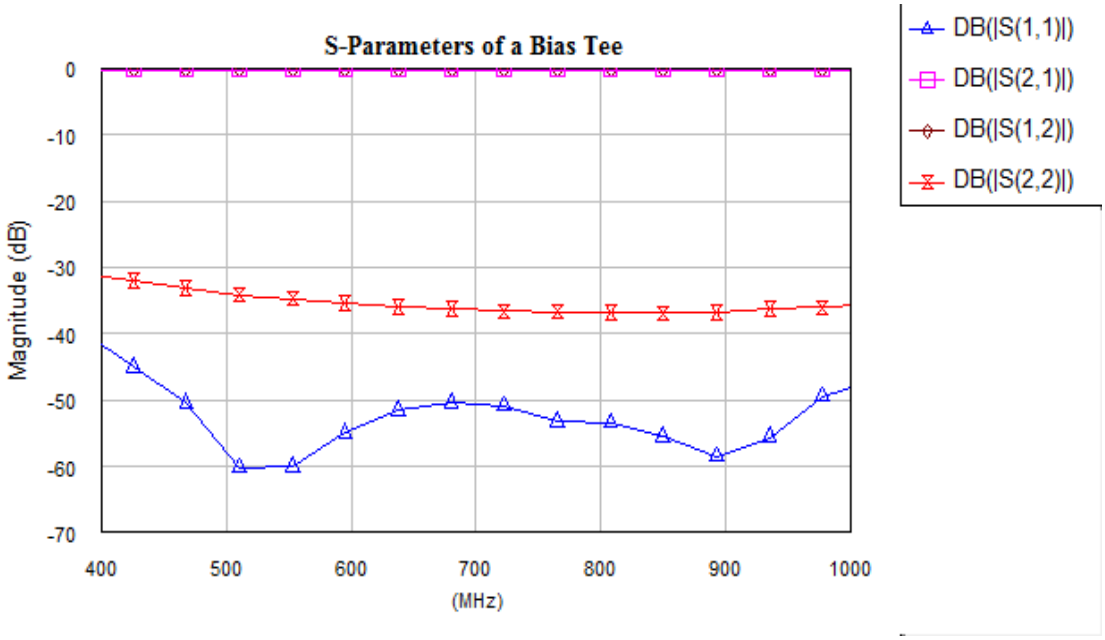

Figure 30. The S-parameters of the bias tee. The low input/output reflections and high forward/reverse throughput reflections prevents any data interference.

The low input and output reflections (S11, S22) show accurate port matching, allowing the bias tee to have minimal effect within the test system while the high gain reflections signify high isolation between the power supply and VNA. These s-parameters validate the measurement system because of the minimal influence of foreign circuits or devices in the test environment.

5.1.2 High Frequency Measurements

Data collection for coplanar wafer measurements in the waveguide WR2.2 frequency band did not contain biasing issues but generated other data integrity concerns. The coplanar wafer measurement probes contain biasing and filtering within the probe housing, preventing the biasing complications observed in low frequency measurements [8]. However, due to the high frequencies associated with WR2.2 waveguide band, frequency extenders provided by Virginia Diodes Inc. were utilized to get accurate VNA measurements [15]. The frequency extenders contain embedded circuits required to make measurements at high frequencies, however, these extenders also contain some power losses associated with these circuits that may interfere with device reflections. Additionally, the probes themselves are susceptible to power losses and, due to their fragility, are prone to other measurement errors. The RF effects of the probe and extender are incorporated into the test environment and are typically accounted for during the error network calibration procedure, however, these components contributed un-calibrated uncertainty for the one port consistency measurements shown in figures 23, 24, and 25. Upon further examination of figure 24, the through error coefficient, $E_{21}E_{12}$, has a higher

degree of variance for a specific frequency range (370-390GHz). This likely points to a systematic error within the test environment as it only affects the error coefficients within that specific frequency range. This systematic error also manifests itself in the calibrated reflections, slightly altering the expected measurement response, for several devices. Figure 31 displays the slight impedance variation the test environment implements into the calibrated measurements.

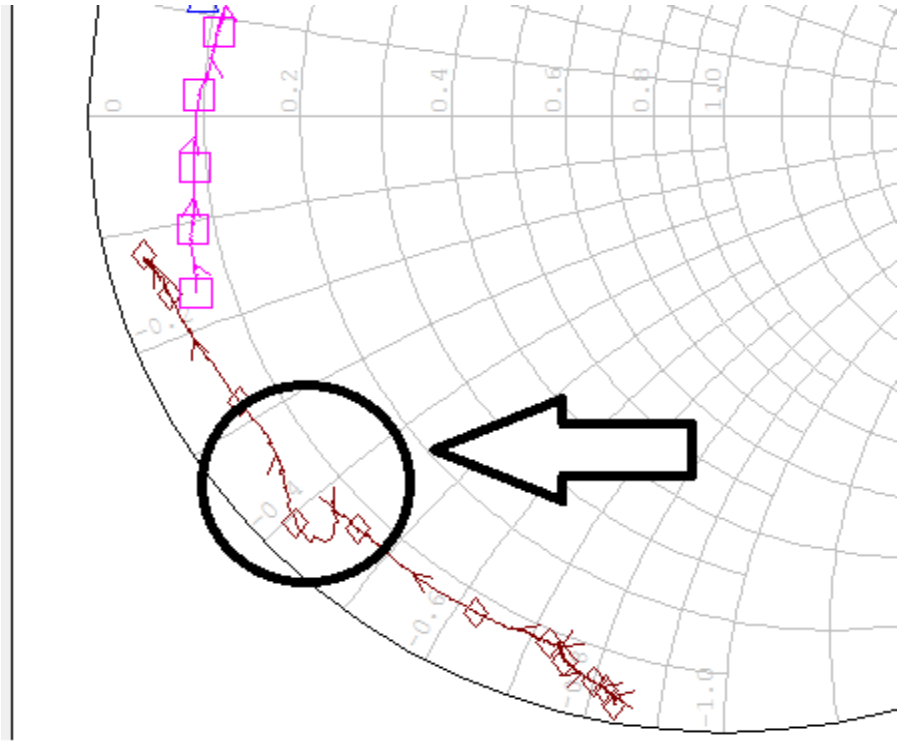

Figure 31. A portion of the Smith chart displaying the impedance of a biased diode, including the systematic error. This systematic error introduces a small bump in impedance and was only present in the variance measurements for coplanar wafer devices.

The impedance "bump" was consistent for all the variance measurements in both diode and standard calibrations. As previously mentioned, this systematic error is likely due to power issues in the test environment arising from the probe or frequency extender. The VNA is responsible for providing the incident waves while measuring the reflected waves, the combination of which allows for the calculation of S-parameter data about the DUT. The power of the incident wave must be sufficient in order to accurately measure the reflected waves. If the system is too lossy, or improperly filters the standing waves, then measurement uncertainty will occur. Despite the systematic error affecting some data, the measurement integrity was maintained due to the nature of the tests conducted. The goal of the variance analysis was to determine the variance in measurements due to non-systematic errors which provided deviation between repeated measurements. The systematic errors that influenced the test

environment provided slight deviation between the expected and actual impedances, leaving the non-systematic errors, and their effects, uninhibited.

Overall, the measurement integrity validated the data collected for both low frequency and high frequency measurements. The valid data, and conclusive results, cement the diode as the load standard for accurate one port and two port calibrations in high leakage, coplanar wafer test environments.

5.2 Future Work

This thesis built off the laborious work of many people within the RF and microwave community, therefore, it is assumed that in the future others will build on the work of this thesis. Possible avenues for future development and exploration are discussed in the final sections.

5.2.1 Two Port Wafer Measurements

This work explored one port measurement techniques for one port coplanar wafer measurements but, due to limited resource allocation, was unable to fully verify the diode consistency benefits for two port measurements. This work established a diode as a sufficient load standard for two port calibration at low frequencies, but high frequency measurements are needed to verify the benefits of diode calibration in high leakage test environments. The high leakage test environment within the waveguide WR2.2 frequency band would benefit the most from a reduction in error coefficient variance. Additionally, the diode load standard is perfectly suited for sixteen term, two port calibration procedures, by providing a stable test environment to determine all cross channel leakage errors. For this measurement, the diode test pads from each port should be as equally separated as the test pads for the DUT. The radiating probe tips from each VNA port would then be equally spaced for both calibration and measurement test environments, insuring an accurate depiction of the cross channel leakage.

5.2.2 Generating Ideal Circuit Behavior

This research utilized many sets of “ideal” S-parameters that were derived from multiple sources. Traditional coplanar wafer calibration methods model the impedance standards through electromagnetic focused software. Modelled circuit behavior is inherently different from the actual measurements but provides relatively accurate S-parameters. Ideal standards for wafer measurements within the waveguide WR2.2 frequency band are difficult to generate because of the uncertainty of the circuit behavior at these extremely high frequencies.

The issue with creating perfect “ideal” S-parameters persisted into the diode calibration procedure. As mentioned, the diodes were first calibrated and then re-measured to determine the error network.

This was required because of the lack of “ideal” diode S-parameters. A newly fabricated, or assembled, diode has unknown circuit behavior resulting in a lack of available “ideal” S-parameters. Throughout this thesis, the “ideal” S-parameters were generated from measured S-parameters calibrated through standard calibration techniques. The inconsistencies associated within those calibration techniques propagates into the diode calibration results. Therefore, it is wise to develop better methods of obtaining “ideal” S-parameter data.

A possible avenue to reduce the inconsistency or concern within the “ideal” S-parameters is to mass produce diode standards. This follows the same logical process as over-sampling load standards to create an over-determined system of equations, reducing the effect of any one outlier. A large production of diode samples results in an accurate circuit model whose parameters are statistically determined. The statistically determined “ideal” S-parameters reduce the effects of any outlier on the calibration procedure. This “wisdom of the crowd” approach does not provide perfect “ideal” S-parameters for every diode, but with consistent fabrication processes, the “ideal” diode response will be void of any non-systematic calibration errors.

6. References

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