Low Power Analog Front-Ends for Energy Efficient Physiological and Environmental Monitoring

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A

Dissertation

Presented to

the faculty of the School of Engineering and Applied Science

University of Virginia

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in partial fulfillment

of the requirements for the degree

Doctor of Philosophy

by

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May 2022

APPROVAL SHEET

This

Dissertation

is submitted in partial fulfillment of the requirements
for the degree of

Doctor of Philosophy

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ABSTRACT

The Internet-of-Things is growing at a tremendous pace with applications spanning across a wide range of sectors such as smart homes, healthcare, agriculture, smart environment etc. Specifically, IoT market for healthcare has seen an exponential growth in the recent years, and is projected to value at $54 billion dollars by 2029 [1]. Smart healthcare devices, with their real-time data collection, show great promise in improving the patient outcomes, and reducing treatment costs. Also, sensing multiple vital signs provides a well-rounded report on the user's health, and greatly improves the quality of care. Many of the smart watches like Apple watch 6, Fitbit have integrated multiple sensing modalities including electrocardiography (ECG) and photoplethysmography (PPG) to detect important physiological signs such as heart rate, blood oxygenation etc.

Studies show that breathing in high levels of air pollutants like ozone increases the risk of cardiovascular diseases like heart failure, hypertension, and causes respiratory distress such as shortness of breath, wheezing, and asthma. While some commercially available products target environmental parameters, there is a lack of single device solutions to provide both physiological and environmental sensing. Also, as most of these devices are battery-powered, they have limited lifetime and require frequent recharging, resulting in data losses. A popular solution to this challenge is enabling self-powered operation by using transducers such as photo-voltaic (PV) cells and thermoelectric generators (TEGs) to harvest energy from ambient sources. However, the readily available energy from these sources is severely limited, and does not match the high-power consumption of existing multi-modal analog front-ends. Therefore, in order to enable fully self-powered operation, it is critical to realize low-power analog front-ends (AFE) while still maintaining good performance metrics.

This dissertation aims to enable self-powered physiological and environmental monitoring by making several contributions, categorized in three research themes. The first theme involves implementation of various circuit design techniques to reduce the analog front-end power without degrading its performance. Specifically, this theme presents sub-µW AFEs for gas and respiration rate sensing. In order to support ozone sensors' large resistance range, existing analog front-ends are designed at high supply voltages, increasing their power consumption. By leveraging adaptive circuit techniques, the ozone analog front-end is able to operate at a supply voltage of just 0.6 V, bringing down its power to sub-µW levels. The presented ozone analog front-end consumes only 88.6 nW of readout power, lowering it by 300x when compared to the prior works. While doing so it is also able to maintain a high dynamic range of 152.27 dB -159.29 dB. A second generation of the gas analog front-end is designed to extend its use case towards detecting both oxidizing and reducing gases. This multi-functional gas AFE retains sub-µW operation while achieving a high dynamic range of 138dB – 144dB. The final work of this theme involves designing a sub-µW respiration rate AFE featuring on-node signal processing to compute the user's breathing rate while consuming 397 nW of end-to-end power, which is 90.7x lower than the prior respiration rate analog front-ends.

Some sensors such as PPG and gas, are either active or require UV LED illumination to maintain good sensor performance, adding tens – hundreds of µW power overhead. Therefore, once the AFE's power is optimized, these sensors start to dominate the system power. This dissertation's second research theme mitigates this issue, and implements various circuit techniques within the analog front-end to lower the PPG, and gas readout's LED power. It pushes the UV LED power below 31µW, while maintaining good sensor performance, and achieves a 4-50x reduction of PPG system power. This theme also designs a context-aware, event-driven control scheme for detecting the user's dynamically changing sensing requirements to improve the system availability, and

achieve a power reduction of >206x.

Lastly, this dissertation explores a universal analog front-end design to support low-power voltage, current, resistive, and capacitive sensing. It minimizes recurring design efforts and time by adding on-demand reconfigurability to adjust the analog front-end's performance metrics. Simulation-based verifications are carried out to verify this design's functionality, and performance metric tunability for all the four modalities.

ACKNOWLEDGMENTS

I owe my deepest gratitude to my advisor, Ben Calhoun, for taking me on as his student and advising me during my graduate school. His endless support and motivation helped me push through the tough times of my PhD. His advice has not just helped me in my academic journey, but has also been instrumental in driving my personal growth. My interactions with him over the past four years have helped me pick up valuable skills which will help me going forward. Next, I'd like to thank the members of my thesis committee: Steve Bowers, Homa Alemzadeh, Brad Campbell, and Barry Johnson, for their time and valuable feedback on this dissertation.

I would also like to thank Terry Tigner for the many times she has uplifted my spirits with her fun conversations and kind words. I am grateful for her support, both administrative and personal. I have been fortunate enough to have Peng Wang as my project partner for the entire duration of my PhD. I could not have asked for a better team mate. I will always cherish all the fun times we spent during our hikes, summer trips, and late-night measurements and tapeouts. I am grateful for her positive outlook and enthusiasm for all of our crazy ideas. I also want to thank her for her friendship and support over the past four years. I would also like to thank Henry Bishop and Anjana Dissanayake for all the times four of us spent playing badminton, eating hotpot, going for happy hours and sharing our woos. Especially, our evening steam sessions of online video gaming during the initial months of pandemic. I cannot imagine my time here at UVA Without their companionship.

I would like to acknowledge my Bengroup senior, Ningxi Liu for his mentorship and advise both, during and after his time at UVA. I am also thankful for the support from all my Bengroup colleagues who I've worked with in the past few years: Jacob Breiholz, Daniel Truesdell,

Shuo Li, Sumanth Kamineni, Shourya Gupta, Natalie Ownby, Katy Flynn, Xinjian Liu, Peter Le, Suprio Bhattacharya, Omar Faruqe, and Daehyun Lee. I greatly appreciate the help I received from Akhilesh Tanneeru, and Dr. Veena Misra while testing in their laboratory at NCSU. I would like to mention Steve-group members, Divya Divvuri, Robert Constanzo, and Pouyan Bassirian for their help and support during chip testings. I also want to thank Luis for his help and support during testing the chips. For supporting my graduate studies and projects, I'd like to thank my funders National Science Foundation and the University of Virginia.

To my mom and dad, thank you for always believing in me, and motivating me to chase my dreams. Your unrelenting love and support inspires me to succeed in life and be a better version of myself. Thank you for staying on hours long video calls during my late-night tapeout and testing sessions. Whatever I have accomplished during my short career is largely a result of your patience and teachings of perseverance. I will be eternally grateful for everything you have done to provide me with all the opportunities I desired throughout my life. I would like to thank my brother, Utsav, for being a consistent source of support and for stepping up during the many times I couldn't. For my Dadaji, thank you for providing us with the best that the world had to offer. Thank you Nanaji for always watching over me. I also like to thank my grandmas for always keeping me in their prayers and believing in me. I am grateful for the support and patience from my family members: Bikash, Sudha, Binod, Manju, Aditya, Varun, Manisha, Megha, Ravi, Rohit, Seema, Kiran, Rekha, Ridwik, and Anant. I'd specially like to thank Ashwin and Trishla for always making me laugh with their fun conversations. It truly takes a village to raise a PhD. student.

My time at UVA wouldn't have been possible without my friends. I'd like to thank Swasti, Rakshit, Meena, Sahil, and Nikhil for their friendship over the years. I'd specially like to acknowledge Charu for always being there for me. My paw-friend Gru's, and his parents Gaurav and Kratika's, friendship and warmth have been invaluable throughout the course of my PhD. I'll

always cherish all of those weekends and fun trips full with lots of laughter, amazing food, and Maal. Being away from home for such long durations of time is tough. I cannot be more thankful to Vedant and Madhav for being my family in the states, and for always looking after me. Finally, I'd specifically like to thank my fiancée Vedant for standing by me through all these years and encouraging me during this crazy journey. I am grateful to have your unconditional love and support.

Nanakorobi yaoki

To Mom, Dad, Utsav, and Dadi.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

Recent advancements in custom silicon design and sensor technology have fueled the wide spread popularity of Internet of Things (IoT). A wide range of applications including smart homes, automotive, smart energy, healthcare, smart environment etc. deploy IoT sensor nodes to retrieve real-time information for gaining knowledgeable insights and decision making (Fig. 1.1). The number of these devices is growing exponentially, and is expected to hit 1 trillion within the next decade [2]. Amongst the above-mentioned applications, IoT market for healthcare sector has seen a steady increase in the recent years, and is projected to value at $54 billion by 2029 [1]. Since, both medical diagnosis and care management is data driven, IoT with its real-time data collection, has great potential to make healthcare more accessible and efficient. Smart healthcare devices enable early detection of underlying health issues, allowing the user to seek timely medical intervention. This improves patient outcomes, and makes health care more cost-effective. Also, with the onset of the coronavirus pandemic, both physicians and patients now prefer telehealth to minimize physical contact. The IoT has been able to form a bridge between patients and healthcare professionals by allowing them to remotely monitor critical physiological signs, and provide feedback [3]. This has greatly improved the quality of care, and made at-home management of chronic diseases more efficient. Additionally, wearable healthcare devices are also being used to manage the symptoms

of long-COVID. To further improve the diagnosis and remote medical care, the wearable devices need to monitor a wider range of vital signs.

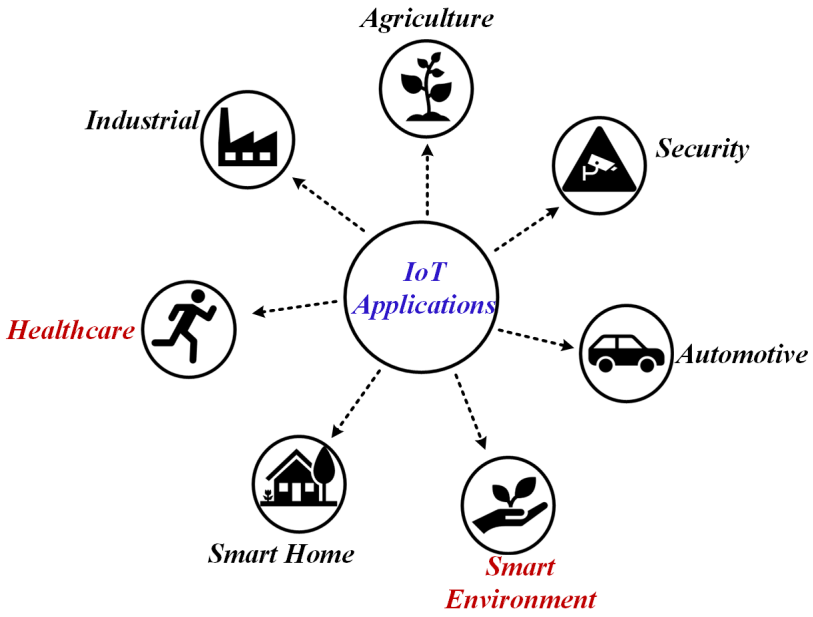

Figure 1.1: An illustration showing some of the most prevelant applications of Internet-of-Things

Many of the new-age smart watches such as Apple Watch 6, Fitbit include multiple modalities like electrocardiogram (ECG), photoplethysmography (PPG)-based heart rate and blood oxygenation, etc. [4], [5]. However, in addition to tracking the user's physiological vital signs, it is also necessary to monitor their micro-environmental parameters. One of the reasons for this is the global increase in air pollution, which is now the fourth leading cause of death [6]. We have long known that breathing in high levels of harmful air pollutants like ozone (O_3), nitrogen oxides (NOx), etc. causes both immediate and long-term physiological effects that deteriorates cardiovascular and respiratory health. Specifically, ground-level ozone, when present in harmful concentrations, is known to increase the risk of cardiovascular diseases like heart failure, stroke and hypertension, and cause respiratory distress such as shortness of breath, wheezing, and asthma

attack [7], [8]. Since, the ozone concentration varies with weather, time of the day, or local environment, a wearable device to monitor personal ozone exposure is necessary to alert the user of unsafe surroundings and take preventative measures. While, most of the smart watches are solely dedicated towards healthcare sensing, there are some commercial products like Flow 2 which target environmental monitoring [9]. However, with the present solutions, the user needs to carry/wear multiple devices in order to monitor both physiological and environmental signs. This leads to a bad user experience. Therefore, a body sensor node with multiple modalities can help solve the multi-device problem, and also provide a comprehensive study of the user's health and environment. One important challenge in realizing multi-modal body sensor nodes is caused by the high-power consumption of its components.

A wearable body sensor node's operation comprises of sensing and processing the target signals, followed by either locally storing the data or wirelessly transmitting it to the user's cellphone. A conventional body sensor node typically consists of a radio for wireless communication, a microcontroller, clocking circuits, a power management unit, and sensors and analog front-ends (AFEs) for retrieving and processing the desired signals. As mentioned before, to provide a comprehensive study of the user's health and surroundings, the sensor node needs to include multiple sensing modalities. While, a sensor node can reuse most of its hardware components, it would still require different analog front-ends to support each sensing modalities.

In order to generate a well-rounded report, it is necessary to continuously monitor important vital signs such as respiration rate (RR), heart rate (HR), blood oxygen saturation (SpO_2), blood pressure, and ambient gas concentration. These signals are retrieved by using ECG, PPG, and ambient gas sensors. Therefore, a body sensor node must include analog front-ends for each of these sensing modalities. Fig. 1.2 shows the power profile of a sensor node with the above-mentioned AFEs. It can be observed that the total sensor node power is largely dominated by its analog

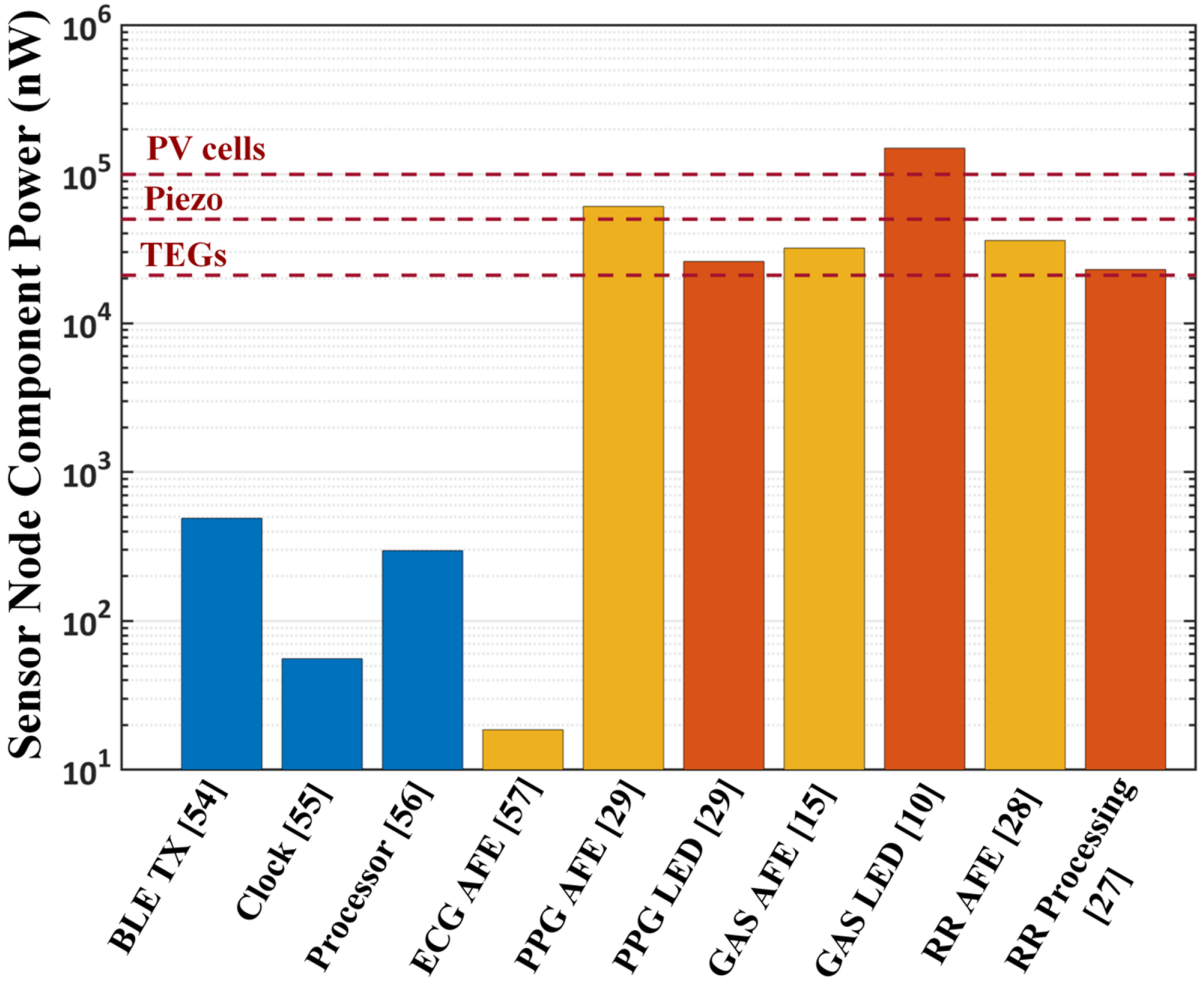

Figure 1.2: Power breakdown comparing components of a wearable sensor node.

front-ends and sensors. The lowest-power prior-reported ozone and physiological joint-monitoring system is based on off-the-shelf components, consuming 630 μW of power in just its sensors and analog front-end circuits [10]. This power level would require frequent battery recharging or replacements, resulting in data losses and bad user experience. Self-powered systems provide an alternative to eliminate similar battery recharging problems. These sensor nodes include transducers such as photo voltaic (PV) cell, thermoelectric generators (TEG), piezo to harvest energy from ambient sources (sunlight, body movements, body heat differentials), and subsequently generate

electrical signals that are later on processed by energy harvesting circuits. This makes the sensor node self-sufficient, and removes the problem of finite lifetime by allowing it to independently harvest and store the required energy. However, the energy available from these ambient sources is both spurious, and varies according to its on-body location, times of the day or ambient temperature (Table I). Specifically, on-body harvesters like TEG, even with the right conditions, have a power density of just $< 20\mu W/cm^2$ [11]. To prevent the node from dying out, it should match the power budget determined by the various energy sources. A larger harvesting transducer can be chosen to increase the available power. However, this would make the wearable sensor node bulky, and inconvenient for the user. Therefore, reducing the sensor's nodes power consumption is a better alternative for enabling system operation without overtaxing the already constrained on-body harvesters.

It has already been established that in a multi-modal sensor node, the analog front-ends significantly dominate the total system power. Therefore, by designing low-power analog front-end circuits, the power mismatch between energy source and sensor node can be reduced. Also, owing to the analog front-end's power-performance tradeoff, careful design choices need to be made in order to match the sensor specifications [12].

TABLE I

POWER DENSITY OF ENERGY HARVESTING SOURCES

Energy Harvesting Source	***Conditions***	***Power Density***
PV cell [51]	Bright	100 μW/cm^2
	Dim	500 nW/cm^2
Piezo-electric cell (Human) [52]	-	50 μW/cm^2
Thermoelectric generators (TEG) [11]	--	20 μW/cm^2

In addition to enabling multi-modal sensing, another critical challenge is to make the IoT sensor nodes more scalable and cost-effective. Existing works implement dedicated low-power multi-modal analog front-ends for each application, tailored to meet the sensor specifications. However, IoT sensor nodes with a wide range of capabilities are required to support a plethora of applications involving public safety, smart environment, smart buildings, safe hospital room conditions, monitoring radiation exposure etc. One such example involves maintaining optimal hospital room conditions to improve the patient outcomes, and prevent sudden illnesses. Environmental determinants such as ambient room temperature, humidity and room pressure, when not maintained, may cause adverse health effects [13]. In case of low room pressure, the air along with harmful particles gets trapped inside the rooms, increasing the risk of spreading airborne illnesses. Similarly, higher levels of humidity when coupled with low temperature aids in growth of black mold, causing its own set of problems in healthcare settings. With the onset of COVID-19, minimal contact between healthcare workers and patients is desired to reduce the risk of exposure. Thus, IoT sensor nodes that can enable remote monitoring of room conditions would help improve quality of medical care and patient outcomes. Most of these sensors output voltage (V), current (I), resistive (R) or capacitive (C) signals. However, majority of the existing multi-modal front-ends either support a sub-set of these signals or deliver application-specific performance metrics. Therefore, due to insufficient flexibility, these application-specific front-ends require a large design effort to account for every small change in the sensing requirements. This slows down the development time, and also increases the engineering cost. Since, many of these applications are niche and produced at a small-scale level, their budget costs are limited. Therefore, a universal V/I/R/C analog front-end that can be reconfigured to support wide range of sensors is desirable to promote accessibility and rapid development of IoT sensor nodes.

1.2 Thesis Statement

Implementing supply voltage scaling and adaptive sensor biasing can bring down the gas AFE power to sub-μW levels, resulting in 300x lower readout power compared to prior works while maintaining good dynamic range performance. Further, sub-μW respiration rate sensing can be enabled through low-power capacitive-based AFE integrated with on-node processing.

Embedding power-efficient design techniques at the AFE level enables low-power integration of sensors and their peripherals. Specifically, implementing hybrid DCOC brings down the PPG system power to sub-10μW level, resulting in 4-50x lower system power compared to prior works, without degrading its performance. By predicting sensor's saturation for decision making regarding UV LED control, its average power can be reduced to sub-31μW while still enabling gas sensor's recovery.

A context-aware, event-driven system operation of multi-modal AFE improves the quality of information by adapting to dynamic sensing requirements, and increases system availability by reducing unnecessary data generation and active power.

Lastly, using a time-based architecture, a single-channel AFE for V/I/R/C modalities can be implemented along with added performance metric tunability, without incurring high design complexity and consuming excessive power.

1.3 Research Themes

This dissertation's research goals are categorized into the following three themes which cross-cut across different chapters (Fig. 1.3).

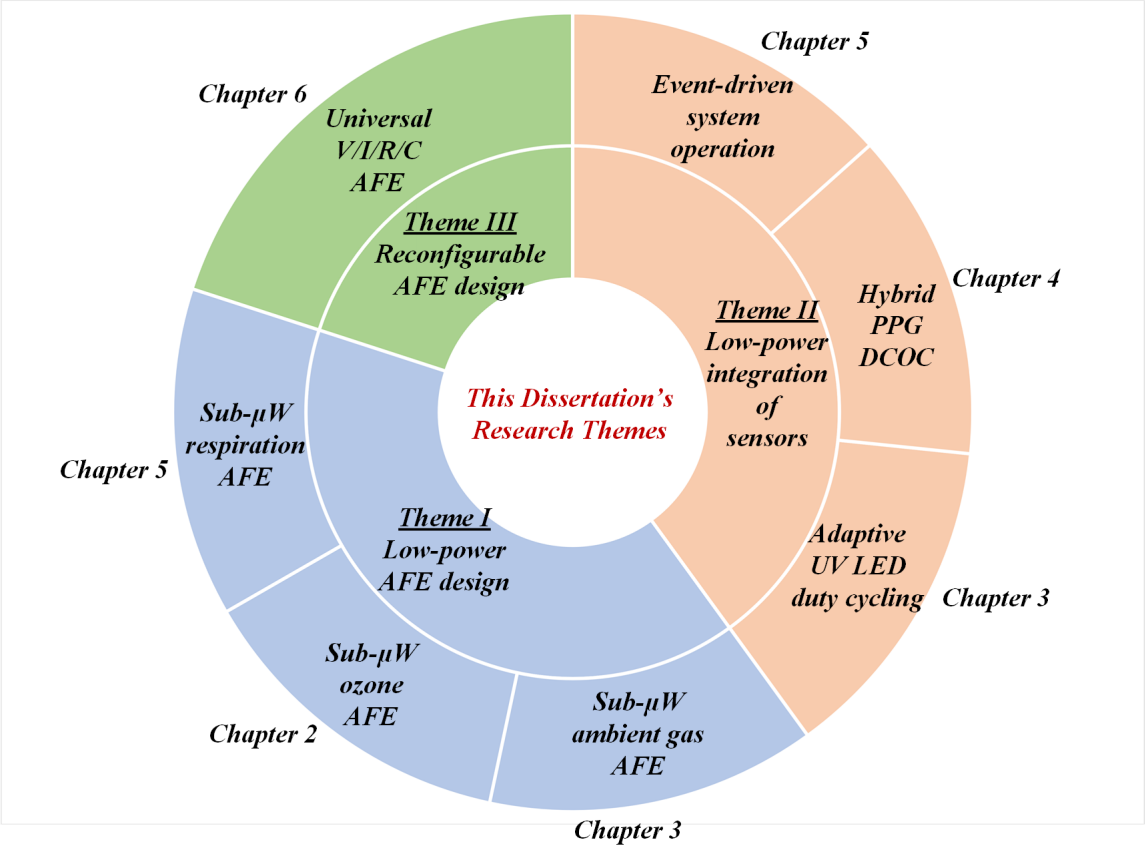

Figure 1.3: An illustration showing the mapping of this dissertation's chapter to its three research themes.

1.3.1 Low-power Analog Front-end Design

In order to support multiple sensing modalities, a sensor node must include multi-modal analog front-ends. As mentioned before, these multi-modal analog front-ends dominate system power, and overtax body-worn energy harvesters. Thus, in order to optimize the analog front-end power such that it matches the power harvested from the ambient environment, this dissertation presents low-power analog front-end designs for gas and respiration rate sensing. Due to the large resistance range of gas sensors, existing works consume power ranging from tens of μW to several mW in just the analog front-end. In this work, we introduce circuit techniques that pioneer the use of voltage

scaling (V_{AFE} =0.6 V) to bring down gas analog front-end's power to sub-μW levels while achieving high dynamic range. Prior custom silicon works extract respiration rate through ECG, PPG or Bio-Z readings, resulting in high-power readouts and accompanying complex post-processing. This dissertation proposes a sub-μW analog front-end design with local on-node processing capability to reduce both the analog front-end power and the post-processing power overhead for respiration rate monitoring.

1.3.2 Integration of Active Sensors and Peripheral Devices in an Energy Constrained System

The total system power includes power consumed by analog front-end, as well as the sensor and its accompanying peripheral devices. While low-power circuit techniques reduce the analog front-end's power overhead, integrating the required sensors in an energy-constrained system proves to be a challenging task. While some sensors are passive in nature, others including PPG and gas, are either active or require pulsed heating/UV LED illumination to maintain good sensor performance. This adds additional tens - hundreds of μW to the total system power. In self-powered multi-modal sensor nodes, this power level would drastically reduce the system availability. To mitigate this issue, this dissertation implements following control techniques within the respective analog front-ends. In contrast to the fixed duty cycle approach towards UV LED illumination of metal-oxide gas sensors, this work adaptively duty cycles the UV LED by predicting the sensor saturation point, and subsequently making a decision to turn on the UV LED. This provides a better trade-off between low-power operation and sensor performance. Secondly, in order to support both low voltage analog front-end operation, and lower PPG LED power, this work explores traditional DC current cancellation techniques, and introduces the implementation of a hybrid DC current

cancellation loop. Furthermore, sensing requirements are often dynamic, and vary according to the user's activities and surroundings. Therefore, a context-aware event-driven method is implemented at the system level to reduce the total active power by monitoring only the relevant signs, and reducing unnecessary data generation. This approach uses primary vital signs as always-on canary channels to identify critical events, and subsequently turns on all modalities for a more detailed report on the user's health and surroundings.

1.3.3 Reconfigurable Analog Front-end Design

Use of either, multiple sensor/application-specific analog front-ends or, a parallel architecture with dedicated analog front-ends (AFEs) introduces various drawbacks. In absence of reconfigurability, these application-specific analog front-ends require large design effort to account for even the smallest change in the sensing requirements. This slows down the development time, and also increases the engineering cost. Also, when these application-specific analog front-ends are used for different use cases, without enough reconfigurability, their performance metrics might be over-designed for the new application. Since, high performance typically comes at a cost of higher power consumption, this would result in poor power-performance tradeoff. In absence of a single analog front-end for V/I/R/C signals, a multi-modal sensor node needs to integrate multiple chipsets, resulting in high integration costs. These issues make the task of extending the IoT sensor nodes' to niche and small-scale applications challenging. To address this, we divulge into design and implementation of a low-power universal single-channel analog front-end for voltage, current, capacitive and resistive modalities. The design also includes on-demand reconfigurability to adjust it's performance according to application needs. This enables the AFE to support a wide range of sensors, making IoT sensor nodes more scalable and cost-effective.

1.4 Dissertation Contributions and Organization

The remaining dissertation chapters are organized as follows:

1.4.1 Sub-μW AFE for Personal Ozone Exposure

Chapter 2 gives background information on metal-oxide gas sensors' working principle, and analog front-end performance requirements (e.g., dynamic range) put forward by them. It discusses conventional gas sensing analog front-ends and the limitations that make it difficult for them to simultaneously achieve high dynamic range and low power operation. The chapter then focuses on the design of a sub-μW analog front-end for personal ozone exposure. An adaptive sensor biasing technique is implemented to enable AFE operation at a supply voltage of just 0.6 V while satisfying the ozone sensor's dynamic range requirements. A CMOS prototype consuming 88.6 nW of readout power, and a dynamic range of 153.27 dB to 159.29 dB is presented.

1.4.2 Analog Front-end for Sub-35μW Ambient Gas Sensing

Chapter 3 focuses on enabling low-power integration of power-hungry ultra-violet LEDs required for maintaining gas sensor's sensitivity. To address this problem, this chapter proposes a sensor saturation detector which is embedded within a sub-μW analog front-end. It also presents the generation II of sub-μW gas analog front-end design that can be used to detect a wider range of gases, and not just ozone. The analog front-end's CMOS prototype maintains sub-μW operation and achieves 138 dB-144 dB dynamic range. The proposed sensor saturation detector achieves $>$

5x system power reduction.

1.4.3 Hybrid DCOC for Low Power PPG Systems

Chapter 4 gives background information on PPG sensor's working principle, and discusses the importance of DC current cancellation loops. It presents a sub-μW PPG analog front-end designed to operate at a supply voltage of 0.6 V, and discusses the design requirements imposed on DCOC loop to achieve low LED power and competitive dynamic range. The chapter then lays out the challenges met by conventional DCOC methods, and implements a hybrid DCOC approach as the proposed solution. A CMOS prototype is presented and is functionally verified. It consumes 532 nW of readout power, and 8.5 μW of LED power.

1.4.4 Event-driven Multi-modal AFE for Respiratory Diseases

Chapter 5 explores the merits and drawbacks of always-on, and aggressively duty-cycled sensor nodes. It then presents a context-aware, event-driven multi-modal analog front-end to improve the quality of information and system availability by reducing unnecessary data generation, and active power. Furthermore, this section presents the design and implementation of a sub-μW respiration rate readout. Since, conventional methods extract user's respiration rate from PPG, ECG modalities, it incurs heavy computational complexity and power overhead. To mitigate this, the presented respiration readout also features low power on-node signal processing to extract the user's respiration rate. The event-driven control scheme achieves a $>$ 206x power reduction, while the respiration rate AFE achieves a 90.7x power reduction compared to state-of-the-arts.

1.4.5 Universal V/I/R/C Analog Front-end

Chapter 6 presents a low-power universal analog front-end which uses time-based architecture to support voltage, current, resistive, and capacitive modalities. It provides an initial transistor-level implementation of the proposed single-channel V/I/R/C analog front-end. The presented design also incorporates circuit techniques for easy reconfiguration of AFE's performance metrics to suit the application requirements. CADENCE simulations are presented to demonstrate the AFE's operation, and tunability.

1.4.6 Conclusion

This chapter concludes the dissertation by discussing its contributions, and provides a description of open problems which require future work.

CHAPTER 2

SUB-μW AFE FOR PERSONAL OZONE EXPOSURE

2.1 Introduction

2.1.1 Motivation

The increasing air pollution has become one of the leading causes for health degradation in the modern society. There are many sources of air pollution including but not limited to volatile organic compounds, nitrogen oxides, ozone etc. Unlike its life sustaining atmospheric counterpart which filters out the harmful ultraviolet radiations, ground-level ozone in particular is associated with many immediate and long-term adverse health effects. Some of the known adverse effects include shortness of breath, wheezing, asthma attacks, as well as increased risk of heart failure, stroke, and hypertension [7], [8]. As pointed out by the "State of the Air" study by American Lung Association more than 41.9% of Americans live in areas with unhealthy levels of ozone [6]. This issue is expected to worsen with global warming and climate change [14].

Adding to this, the ozone concentration also constantly varies depending on various factors such as the time of the day, local environment and weather, and seasonal changes. As the ozone advisories issued by the government are based on these aforementioned predictions, the actual ozone

concentrations might differ from the forecasted values. This can lead to people unknowingly being exposed to unsafe ozone levels, resulting in endangerment of one's physical wellbeing, especially younger children, elderly, and individuals with prior predispositions to respiratory or cardiovascular diseases. Thus, a wearable ozone monitoring system which can continuously track personal exposure to ozone is necessary to alert the user of caustic surroundings, and enable them to take preventive measures.

While there are some existing gas sensing analog front-ends, they do not target ozone sensing, and are designed at high supply voltage (V_{AFE}) to support gas sensor's large resistance range. This results in power consumption ranging from tens of micro-watts to several milli-watts [15], [16]. Thus, this section of the dissertation introduces low power design techniques for ozone analog front-end which can enable sub-μW operation, and simultaneously support the sensor's large resistance range.

2.1.2 Overview of Ozone Sensor

This dissertation uses custom metal-oxide gas sensors fabricated in North Carolina State University for the purposes of ozone monitoring [17]. These sensors are fabricated using atomic layer deposition (ALD) system. A typical sensor comprises of a 300 nm thick silicon dioxide (SiO_2) layer with a layer of tin oxide (SnO_2) deposited on it. The silicon dioxide layer thickness is varied between a range of 4nm to 12nm depending on the sensing requirements.

Fig. 2.1 shows the basic working principle of a metal-oxide gas sensor. The metal-oxide gas sensors are typically passive sensing elements which can be modelled as a variable resistor. The oxygen vacancies in the lattice of these metal-oxide sensors serve as absorption sites for the target gas molecules, which in our case is ozone. Before deployment, the sensor has a finite

initial resistance value which is referred as the "baseline resistance" (R_{BASE}). Once the sensor is deployed, owing to ambient ozone exposure, the target gas molecules start occupying the oxygen vacancies and getting absorbed on the sensor's surface. This leads to decrease in the number of oxygen vacancies which in turn changes the sensor's conductivity. As a result of this behavior, the sensor's resistance (R_{SEN}) increases. During exposure to higher levels of ozone concentration, the number of gas molecules present in the sensor's vicinity is also large. Due to this, higher number of ozone molecules are absorbed on the sensor's surface, which in turn results in a faster rate of increase in the sensor's resistance (R_{SEN}). Therefore, it can be concluded that the rate of increase in the sensor's resistance changes with the ambient ozone concentration.

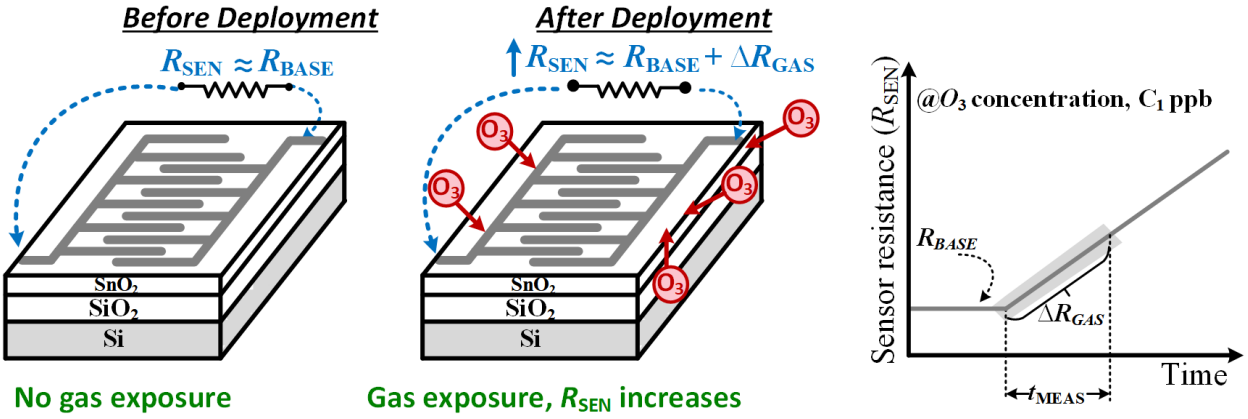

Figure 2.1: Metal-oxide ozone sensor's basic working principle

Thus, the sensor resistance, R_{SEN} , can be broken down into two components comprising of the initial baseline resistance (R_{BASE}), and the resistance variation ΔR_{GAS} due to exposure to different ozone concentration levels (2.1). Here, ΔR_{GAS} is the actual signal we care about in order to compute ambient ozone concentration.

$$R_{SEN} = R_{BASE} + \Delta R_{GAS} \tag{2.1}$$

2.2 Design Considerations and Prior Art

While reducing the AFE power consumption enables reliable self-powered operation, it is also important for the analog front-end to meet the required performance metrics. In the case of ozone sensors, this metric is the analog front-end's dynamic range, which is a function of the largest and the minimum resolvable resistance (resistive noise) measured by the AFE (2.2). However, as the metal-oxide gas sensors typically have resistance varying from tens of kilo-ohms to several mega-ohms, the resulting dynamic range is significantly large. This poses design challenges in achieving low power operation while meeting the sensor's performance requirements.

$$DR_{O_3} = 20log(\frac{R_{SEN-MAX}}{\Omega_{rms}}) \tag{2.2}$$

Traditional gas sensing analog front-ends can be mainly categorized in two architectures: 1) operational amplifier based analog front-ends which utilize resistance-to-voltage (R-V) conversion, and 2) oscillator based analog front-ends that convert resistance to frequency using resistance-to-current (R-I) conversion (Fig 2.2). The former approach biases the sensor with a fixed current source, I_{BIAS} in order to implement resistance-to-voltage conversion for generating a voltage (V_{SEN}) across the sensor (2.3). This voltage, V_{SEN}, is then processed by a signal chain comprising of an amplifier, low pass filter, and an analog-to-digital convertor. The oscillator-based design uses a fixed voltage source to generate a current which is then used for charging/discharging a capacitor to generate oscillations. These oscillations are counted for computing the sensor resistance. This dissertation adopts the operational amplifier-based architecture for ozone sensing AFE. This is done to avoid the latency caused by the oscillator-based analog front-end designs.

$$V_{SEN} = R_{SEN} * I_{BIAS} \tag{2.3}$$

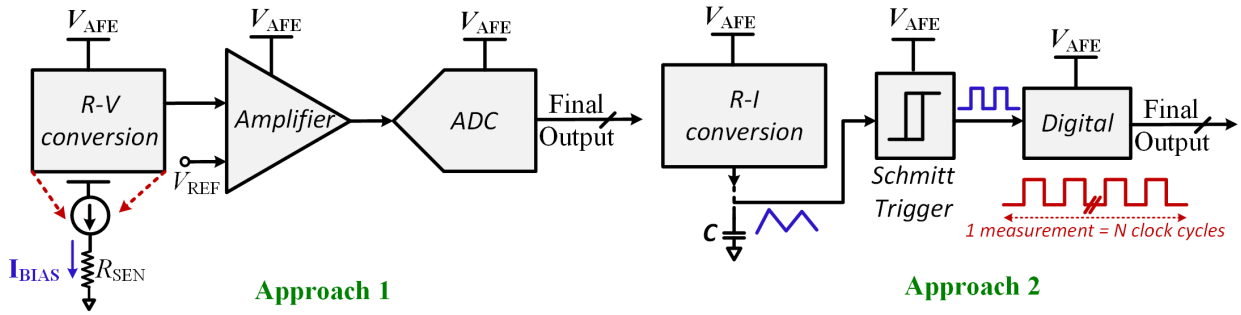

Figure 2.2: Op-amp based gas sensing AFE (left), and oscillator-based gas sensing AFE (right).

The total power consumption of any gas sensing readout can be denoted by equation (2.4). Here, P_{AFE} is the power consumed by the analog front-end, and P_{BIAS} is the power attributed to the current source used for R-V conversion. The average AFE power is a function of analog front-end's supply voltage (V_{AFE}), and the total current drawn by it (I_{AFE}). Similarly, the sensor biasing source's total power consumption is related to V_{AFE} and the instantaneous biasing current (I_{BIAS}) (2.5)

$$P_{TOTAL} = P_{AFE} + P_{BIAS} \tag{2.4}$$

$$P_{TOTAL} = V_{AFE}I_{AFE} + V_{AFE}I_{BIAS} \tag{2.5}$$

Scaling down the AFE's supply voltage (V_{AFE}), and optimizing the sensor bias current (I_{BIAS}), can significantly reduce the total power consumption. However, the design choices adopted by prior works, make it difficult to simultaneously achieve both low power operation, and high dynamic range. These design challenges are elaborated on in the following points

2.2.1 Wide common-mode range for operational amplifiers

A critical challenge of working with metal-oxide gas sensors is their large resistance range, typically ranging from tens of kilo-ohms to several mega-ohms. One of the limiting factors of an

operational amplifier is their input common-mode voltage range (ICMR) which is defined as the range of input voltages during which the amplifier retains its linear operation.

Once the sensing system gets exposed to the target gas, the sensor's resistance R_{SEN} starts increasing. Prior gas sensing analog front-ends use a fixed current source for biasing the sensor, and implementing resistance-to-voltage conversion. Therefore, the voltage generated across the sensor (V_{SEN}) also increases along with the increase in R_{SEN} (2.3). While scaling down the supply voltage (V_{AFE}) is a powerful design knob for reducing power consumption, it also limits the amplifier's range of input voltage swing. Therefore, if the AFE were to operate at a lower V_{AFE}, a large increase in resistance (R_{SEN}) would gradually push the V_{SEN} out of the AFE's input voltage range. This will ultimately saturate the amplifier's output (V_{OUT}), leading to data loss Fig. 2.3. Thus, in order to avoid this scenario, prior works are designed to operate at a higher V_{AFE}. This guarantees a large dynamic range, but at a cost of high-power consumption.

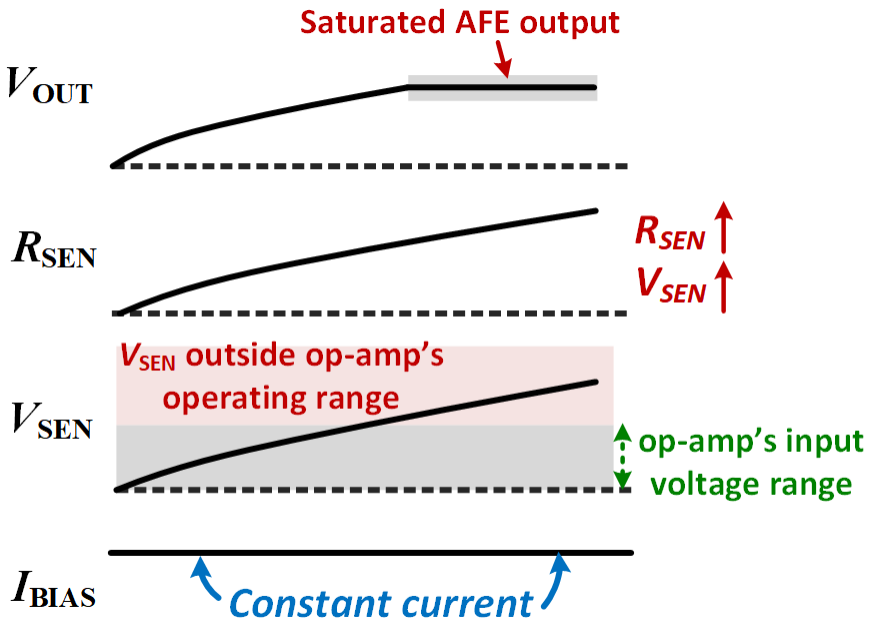

Figure 2.3: Design limitation due to constant sensor biasing current.

2.2.2 High sensor biasing current, I_{BIAS}

The sensor biasing current is used as an excitation source and is a major power contributor. The sensor's resistance range can be denoted as $\{R_{MAX},\ R_{MIN}\}$. As mentioned before, prior works utilize a fixed biasing current source for R-V conversion. The I_{BIAS} value needs to be lowered to reduce the power contributed by it. However, with a fixed biasing current, the minimum resistance of the sensor (R_{MIN}) would generate a much lower V_{SEN} for small I_{BIAS} values (2.3). Thus, in order to retain the resistance measurement resolution at R_{MIN}, one of the two choices are available: 1) include a high-resolution ADC, or 2) maximize the sensor biasing current, I_{BIAS} to generate adequate value of V_{SEN}. So, prior works fix I_{BIAS} to the maximum value ($I_{BIAS-MAX}$) needed to retain the required resolution across the entire resistance range (2.6). However, this results in large power overhead.

$$R_{MIN} = \frac{V_{SEN}}{I_{BIAS-MAX}} \tag{2.6}$$

2.3 Design Approach

As mentioned before, due to the large resistance range of metal oxide gas sensors, an analog front-end with large dynamic range is necessary. Some works have mitigated this issue by proposing to use baseline cancellation method for isolating ΔR_{GAS} [18], [19]. However, since while sensing ΔR_{GAS} these works use a constant I_{BIAS} to convert R_{SEN} into V_{SEN}, an operational amplifier with a wider input common mode range is required, making V_{AFE} scaling challenging, and thus resulting in higher power. Additionally, in order to achieve required resolution across the entire sensor resistance range, the fixed sensor biasing current (I_{BIAS}) is maximized which adds a significant power overhead. This design adopts an operational amplifier based analog front-end,

and proposes two solutions to decrease the overall power consumption of the gas analog front-end.

First, this design proposes a resistance range tracker (RRT) to dynamically vary the sensor biasing current (I_{BIAS}) to enable low V_{AFE} operation while supporting a large resistance range. In contrast to past works, the proposed resistance range tracker continues to limit V_{SEN} to a pre-determined voltage range by dynamically varying I_{BIAS} sourced to the sensor. As a result, the sensor's entire resistance range is divided into multiple sub-ranges, with each sub-range associated with a different I_{BIAS} value. The pre-determined voltage window is decided by the amplifier's input common mode range at the design's supply voltage. As, the operational amplifier in this design operates at V_{AFE} of 0.6 V, a maximum output swing 240 mV is tolerated with a folded cascode type architecture. Thus, in order to retain amplifier's linear operation and ensure reliable RRT operation, the ΔV_{IN}'s range is set such that the differential input to the op-amp ranges between 6 and 12 mV. This also sets a closed-loop gain of 26 dB is sufficient for this design.

Second, it can be seen from (2.3) - (2.5) that for reducing the power contributed by the sensor biasing current (P_{IBIAS}), I_{BIAS} can be optimized by decreasing V_{SEN}. While reducing V_{SEN} to several milli-volts is a potential solution, it is also important to ensure that the resulting I_{BIAS} is large enough to remain unaffected by the sensor and die-package parasitic. Since this design uses resistance range tracking to limit V_{SEN} to a pre-determined voltage range, the minimum I_{BIAS} depends on the largest resistance value the analog front-end has to measure. Thus, in order to determine the optimum I_{BIAS} values following design considerations are taken into account.

The ozone sensor used in this design has a resistance varying from 20 kΩ to 1.5 MΩ. We first choose the range for V_{SEN} values. In order to do so, sensor biasing current for a resistance of 1.5 MΩ is plotted across V_{SEN} ranging from 0.1 V to 1.2 V (Fig. 2.4). Taking into consideration the degradation of I_{BIAS} due to parasitic, the I_{BIAS} values below 10 nA are avoided, and an I_{BIAS}

range of 10 nA to 30 nA is taken into account. This translates to a V_{SEN} range of 15 mV to 45 mV. With this estimate available and a power budget of sub 1 μW, the I_{BIAS} power consumption is plotted across the newly available V_{SEN} range. As seen in Fig. 2.4, to allow sub-μW operation across a range of 20 kΩ – 1 MΩ and reliably source I_{BIAS}, the V_{SEN}'s minimum value can be set to 36 mV at V_{AFE} of 0.6 V. The differential input to the amplifier, ΔV_{IN}, is given as $V_{SEN} - V_{REF}$. As mentioned before, the acceptable range for ΔV_{IN} is 6 mV to 12 mV. Therefore, the V_{SEN} range is fixed to 36 mV – 42 mV. Furthermore, The V_{REF} value is fixed at 30 mV to ensure a differential input of 6–12 mV.

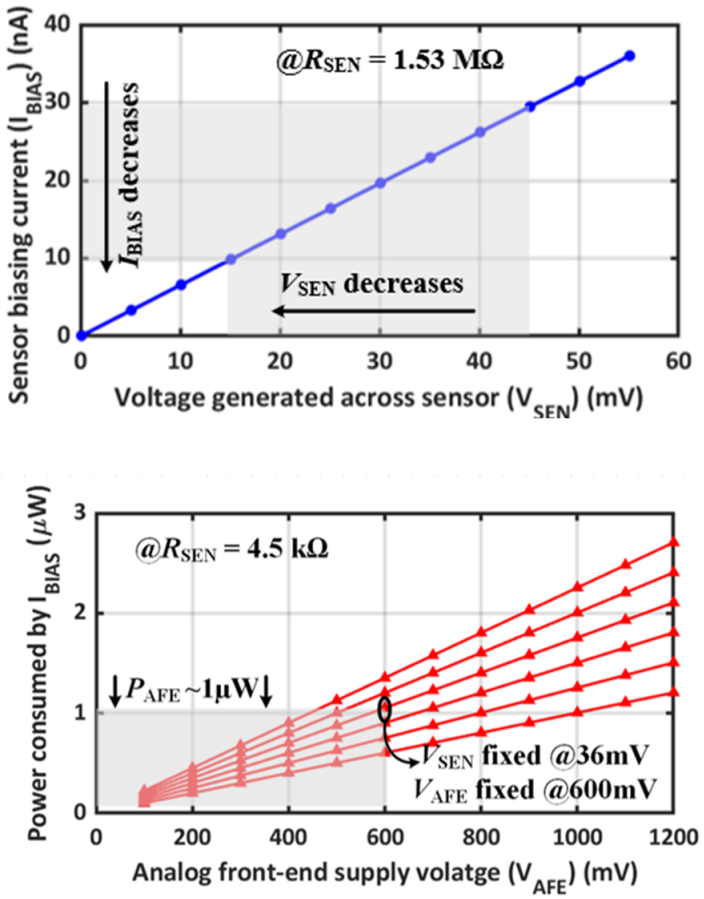

Figure 2.4: Design space exploration to optimize I_{BIAS} for sub-μW operation.

2.3.1 System Architecture

Fig. 2.5 shows the system diagram comprising of the proposed sub-μW ozone analog front-end, off-chip low-pass filter, and a custom digital readout IC with a 6-bit SAR ADC and sampling control block. The ozone analog front-end uses a variable current source (I_{BIAS}) to convert the sensor's resistance (R_{SEN}) into voltage (V_{SEN}), which feeds a differential amplifier (AMP). The proposed resistance range tracker (RRT) tunes the current (I_{BIAS}) to match the sensor's large resistance range. Since the signal from the sensor is a near dc-level signal, flicker noise *(1/f)* becomes a major concern. Therefore, chopping is implemented at a frequency of 1 kHz to remove the *1/f* noise from signal bandwidth, and also to convert the sensor's dc signal (ΔV_{IN}) into an ac signal (ΔV_{IN-AC}) for facilitating amplification. As mentioned before, with a 30 mV of fixed V_{REF}, and a V_{SEN} range of 36 mV – 43 mV, ΔV_{IN} always lies between 6 mV – 12 mV. With a closed loop amplifier gain of ~26 dB, the analog front-end outputs a differential signal (ΔV_{OUT}) within a range of 116 mV – 240 mV. Additionally, the RRT's digital backend also outputs the resistance sub-range value.

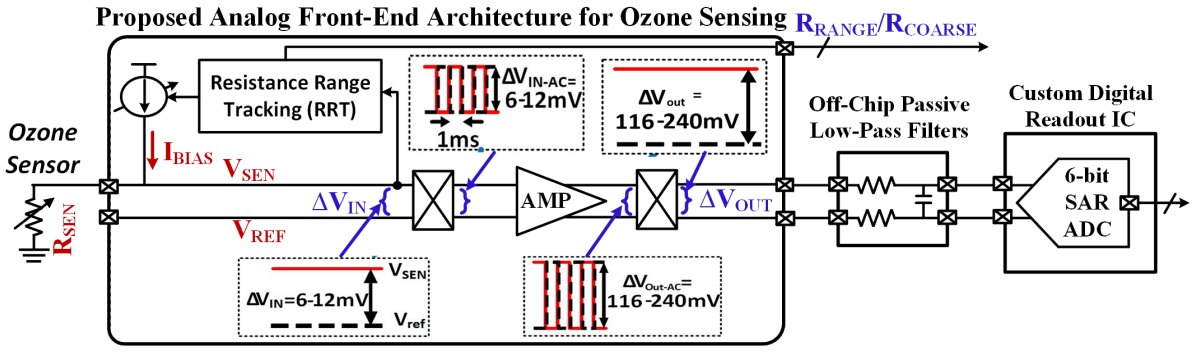

Figure 2.5: Ozone sensing system diagram and the proposed sub-μW analog front-end.

2.3.2 Chopper-stabilized Differential Amplifier

As shown in Fig. 2.6, the differential AMP in the ozone channel implements a pair of 20-pF input capacitors (C_{IN}) and a pair of 1-pF feedback (FB) capacitors (C_{FB}) as the negative capacitive FB loop. The closed-loop gain (A_{CL}) is determined by the ratio between C_{IN} and C_{FB}, which is 26 dB. A fully differential architecture is chosen to minimize the common-mode noise. A passive DC servo loop is implemented to tune the output common-mode voltage to V_{AFE}/2, and reduce the amplifier's offset.

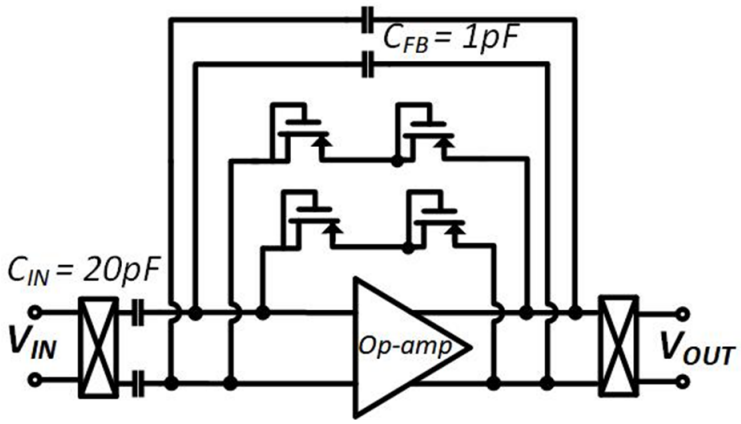

Figure 2.6: Schematic of the AMP implemented in ozone analog front-end.

The first stage of amplification (A1) within the chopper-stabilized ozone channel AMP is a folded cascode structure followed by a traditional five-transistor differential amplifier (Fig. 2.7). Compared with a conventional folded cascode AMP, three pairs of transistors are stacked to provide extra voltage headroom to ensure robust operation across process, voltage and temperature variations. Since, *1/f* noise is a major concern for ozone channel, PMOS transistors (M1, M2) are used as input devices to minimize the *1/f* noise. As both the amplification stages are differential, common-mode FB (CMFB) circuits are implemented to cancel the common-mode voltage offset in each stage. An active CMFB is implemented in the first stage of amplification (A1), tuning

the common-mode voltage of A1's outputs to V_{AFE}/2. A passive CMFB is implemented using pseudo-resistors for the second stage (A2). To further improve the noise performance, we allocate more current budget to A1 (79 nA) than the second stage (24 nA).

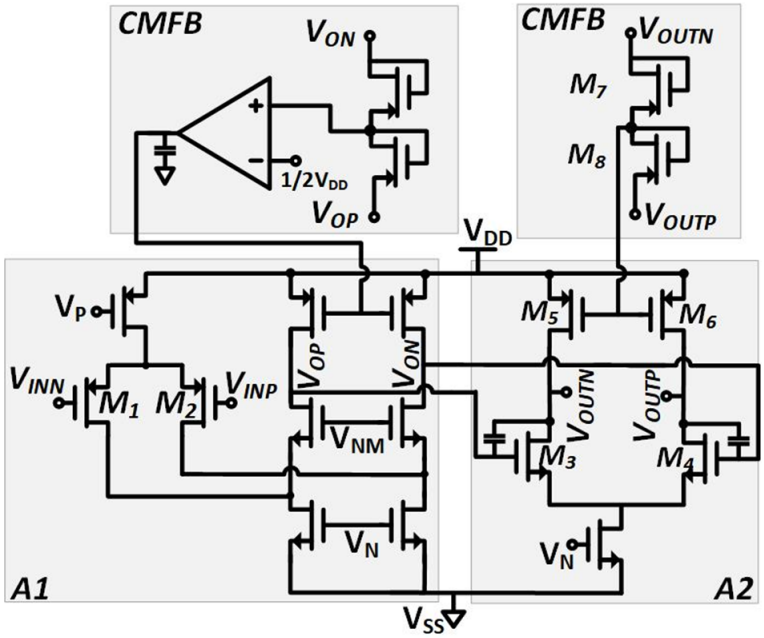

Figure 2.7: Schematic of the two-stage operational amplifier in the chopper stabilized amplifier (AMP).

2.3.3 Resistance Range Tracker

The proposed resistance range tracker is used to limit the voltage generated across the sensor (V_{SEN}) to the analog front-end's/operational amplifier's input voltage range by dynamically varying the current, I_{BIAS}. Due to this, the analog front-end is able to operate at a supply voltage of 0.6 V while achieving a high dynamic range. As shown in Fig. 2.8, the resistance range tracker comprises of an adaptive current control loop, a voltage monitor, and digital backend. The voltage monitor runs in the background to track if V_{SEN} is within the limits of V_H and V_L. Every time the

V_{SEN} increases the pre-defined value of V_H, the adaptive current biasing loop adjusts the sensor biasing current, I_{BIAS} to regulate V_{SEN}.

As shown in Fig. 2.8, the adaptive current biasing is implemented using a negative voltage-current feedback loop. Here, a PMOS transistor (M1) acts as a voltage-controlled current source to bias the sensor (R_{SEN}) for resistance-to-voltage conversion (2.3). The negative feedback first senses V_{SEN}, and then adjust M1's gate voltage to regulate the sensor biasing current I_{BIAS}. The switch, SW, is controlled using the digital backend and connects the negative feedback amplifier, FB to M1's gate. The resistance range tracker's voltage monitor consists of a window comparator, with inputs directly connected to the ozone sensor. This reduces the overall latency by directly monitoring V_{SEN}. The comparator thresholds are set to V_H (43 mV) and V_L (37 mV) to enable the voltage monitor to detect if the differential input (ΔV_{IN}) to the AMP is within the pre-determined range of 6–12 mV. When the adaptive current biasing loop is disconnected, capacitor (C_{FB}) retains the bias voltage (V_{BIAS}). As shown in Fig. 2.8, a two-stage operational amplifier with a simulated open-loop gain of 69.21 dB is used in the negative feedback loop of the resistance range tracker.

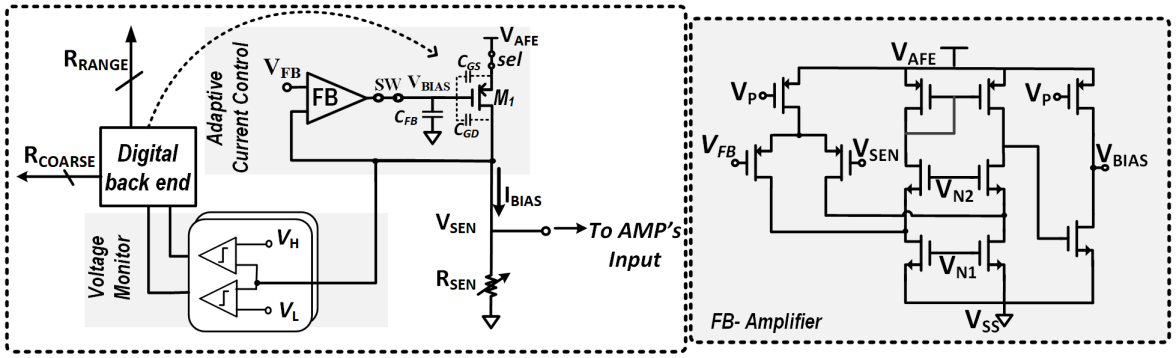

Figure 2.8: Schematic of the proposed resistance range tracker (RRT) (left), and transistor-level schematic of feedback amplifier (FB) used in adaptive current biasing loop (right).

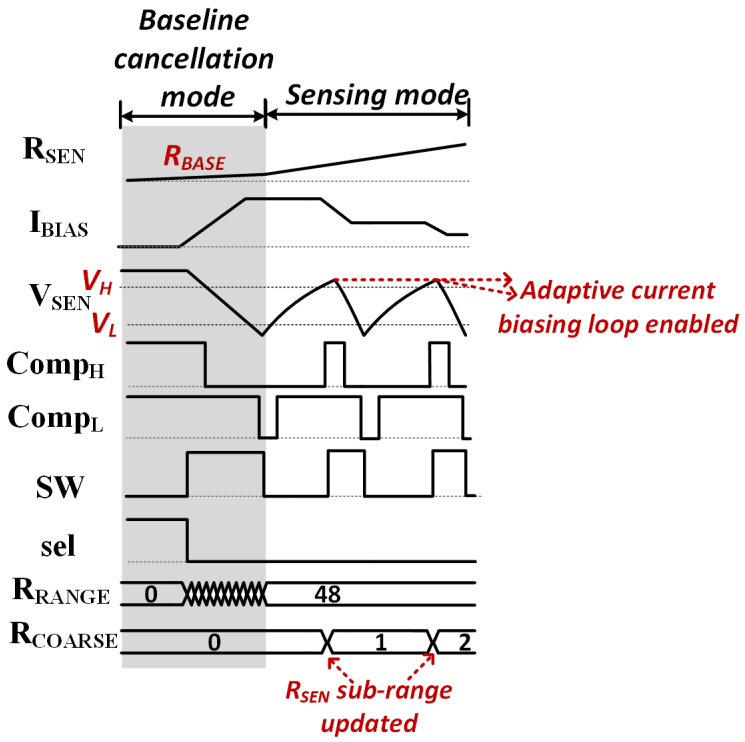

Figure 2.9: Timing diagram of the proposed resistance range tracker.

Fig. 2.9 shows a detailed timing diagram of the RRT. The RRT works in two modes. Once the sensing node is deployed, the RRT starts in the baseline cancellation mode, following which it enters and remains in the sensing mode until the system restarts. The digital backend incorporates the timing control for signaling the analog front-end to enter sensing mode. The analog front-end's operation in the two modes is described as following.

1. *Baseline Cancellation Mode:* Before deployment, that is, prior to ozone exposure, the resistance range tracker is configured in the baseline cancellation mode, and M1 is power gated, resulting in a zero-bias current (I_{BIAS}). Following this, the SW is closed, enabling the adaptive current biasing loop to regulate V_{SEN} to V_{FB} (36 mV) by tuning I_{BIAS} to an appropriate value given by (2.3). The transient response time of the adaptive current biasing

loop (t_{FB}) to perform this regulation can be calculated as shown in (2.7). Here, BW is the closed-loop bandwidth of the adaptive current biasing loop, SR_{M1} is the slew rate of M1, and ΔV_{BIAS} is the voltage at which the lumped capacitance (C_{PAR}) at the gate of M1 needs to be charged before V_{SEN} is regulated to V_{FB}. The slew rate of M1 is calculated by C_{PAR} and the current (I_{SR}) used to charge/discharge this capacitance (2.8). Equation (2.9) shows that C_{PAR} comprises parasitic gate capacitances C_{GS} and C_{GD}, and the capacitor used to store the bias voltage (C_{FB}). Here, due to the miller effect, C_{GD} is amplified by the gain of PMOS transistor M1 (A_{M1}).

$$t_{FB} = \frac{1}{BW} + \frac{\Delta V_{BIAS}}{SR_{M1}} \tag{2.7}$$

$$SR_{M1} = \frac{I_{SR}}{C_{PAR}} \tag{2.8}$$

$$C_{PAR} = C_{GS} + (1 + A_{M1})C_{GD} + C_{FB} = C_{GS} + (1 + g_{M1}R_{out})C_{GD} + C_{FB} \tag{2.9}$$

With I_{SR} being fixed, while regulating V_{SEN} to V_{FB}, a higher resistance value of R_{SEN} results in a higher t_{FB} value. This is because, $g_{M1} \propto \sqrt{I_{BIAS}}$ and $R_{OUT} \propto \frac{1}{I_{BIAS}}$, making the dominant pole proportional to $\sqrt{I_{BIAS}}$. Thus, with an increase in the value of R_{SEN}, the transient response time of the adaptive current biasing loop (t_{FB}) also increases. During the baseline cancellation mode, the voltage monitor tracks V_{SEN} while incrementing a counter (R_{RANGE}) at every positive edge of the digital clock (f_{CLK}), till the comparator output, $comp_H$ becomes low. The comparator outputs at a logic low essentially indicate that V_{SEN} is less than V_L, and is now regulated at V_{FB}. Thus, the total response time of RRT (t_{RRT}) comprises the transient response time of the adaptive current biasing loop (t_{FB}), and the propagation delay of the two comparators ($t^{pr}_{comp1}, t^{pr}_{comp2}$) (2.10). This time ($t_{RRT}$) is indicated by the R_{RANGE} value. The R_{RANGE} value is read as one of the outputs from the

SPI, and is further used to map R_{BASE} to its resistance sub-range using (2.11)

$$t_{RRT} = t_{FB} + t^{pr}_{comp1} + t^{pr}_{comp2} \tag{2.10}$$

$$t_{RRT} = \frac{R_{RANGE}}{f_{CLK}} \tag{2.11}$$

Here, f_{CLK} is chosen as 500 Hz which is large enough to provide sufficient resolution to the counter value (R_{RANGE}) to track the time across the full range of possible R_{BASE} values. The baseline cancellation is performed in a controlled environment, prior to deployment in environment with ambient ozone. This is done only once until the system is reset again. Also, the ozone sensors used here are custom metal-oxide gas sensors, which can have slightly different values of R_{BASE} depending on their thicknesses. So, if at all the ozone sensors are replaced during the lifetime of the circuit, baseline cancellation has to be performed again.

2. *Sensing Mode:* After the completion of baseline cancelation, the digital backend configures the RRT into sensing mode. Here, the switch SW is opened, and I_{BIAS} is held constant. Since the sensor is exposed to ambient ozone, its resistance R_{SEN} starts increasing which in turn increases V_{SEN}. The analog front-end leverages this behavior, and using the RRT, it tracks the increase in V_{SEN}. Once V_{SEN} exceeds the limits of V_H and V_L, SW is toggled and the value of R_{COARSE} is increased to update the resistance sub-range mapping. As SW is closed, the adaptive current biasing loop also lowers I_{BIAS} such that V_{SEN} returns to V_{FB}, ensuring that the operational amplifier does not saturate. After voltage monitor indicates that V_{SEN} is again below V_L, SW is opened. The digital backend also consists of 16-bit counters to provide digital hysteresis and filter out random spikes in comparator outputs. Overall, the resistance range (4.5 kΩ–1.53 MΩ) is divided into 37 sub-ranges.

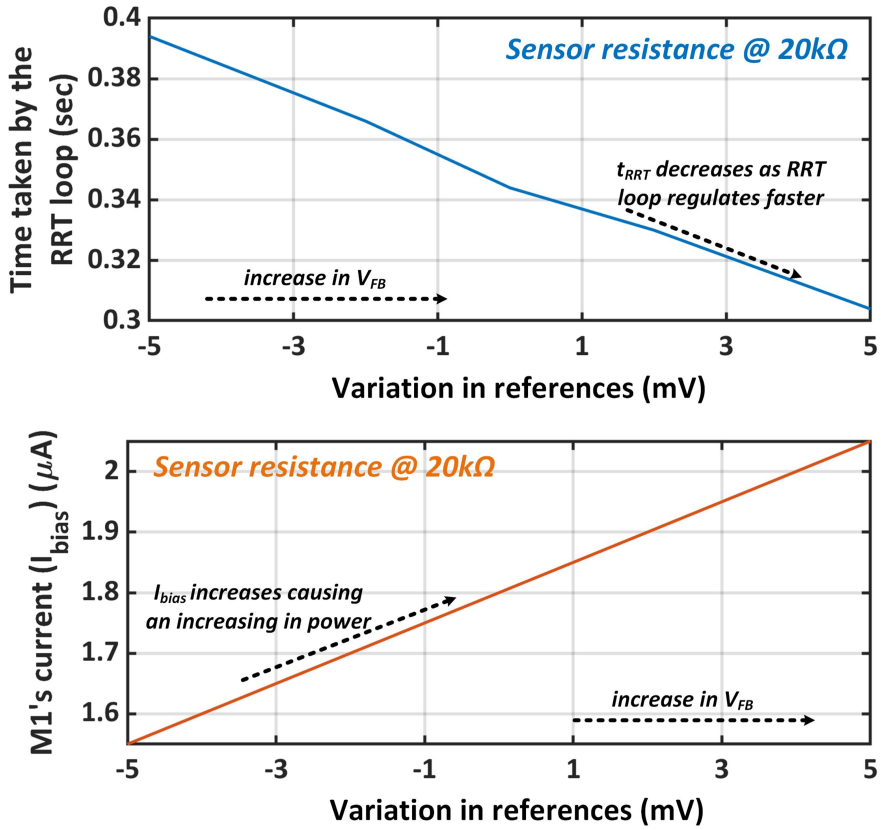

Figure 2.10: Simulated change in time taken by RRT loop during baseline cancellation (top), and change in sensor biasing current (bottom) observed for a ±5 mV of variation in AFE's voltage references.

The adaptive current biasing loop and the voltage monitor in the analog front-end's proposed RRT use three voltage references (V_{FB}, V_L, and V_H) to regulate, and track V_{SEN}. Therefore, their voltage variation across PVT is significant for the AFE's operation. A voltage variation of ±5 mV across PVT for the references (V_{FB}, V_L, and V_H) is within the tolerable limits of this design. While this variation does not hinder the channel operation, it affects two of the channel metrics. First, when there is an increase in V_{FB}, the regulation of V_{SEN} to V_{FB} happens faster, decreasing the response time of RRT (Fig. 2.10). Thus, during the

baseline cancellation mode, the counter value (R_{RANGE}) registered by the RRT loop for obtaining R_{BASE} would also change. The digital clock's frequency (f_{CLK}) can be adjusted to accommodate this change. Second, as the RRT loop works toward regulating V_{SEN} to V_{FB}, the variation in V_{FB} also results in the variation in V_{SEN}. Thus, an increase in V_{FB} also increases the sensor biasing current (I_{BIAS}) used for resistance-to-voltage conversion, causing a change in the total channel power consumption (2.5) (Fig. 2.10).

2.3.4 System Operation

Fig. 2.11 shows the flow chart of the resistance-to-ozone concentration conversion. The proposed analog front-end starts with the RRT in baseline cancellation mode. Once V_{SEN} is driven to V_{FB} (36 mV), R_{RANGE} is sampled, giving the required information to compute R_{BASE}. Following this, the analog front-end enters the sensing mode in which the operational amplifier's output (ΔV_{OUT}) and R_{COARSE} are sampled, and later used to compute R_{SEN}^{ti}. The digital backend implements a programmable timer that controls the amount of time spent in each sensing iteration. After each sensing iteration, R_{SEN}^{t1} and R_{SEN}^{t2} are obtained at the beginning and end of the iteration respectively. The difference between R_{SEN}^{t1} and R_{SEN}^{t2} gives the ΔR_{GAS}, and can be later used to calculate the ozone concentration during off-chip post-processing (2.12). The characterization of the sensor to obtain the value of α is out of the scope of this dissertation.

$$-\alpha C = \frac{\Delta R_{GAS}}{time} \tag{2.12}$$

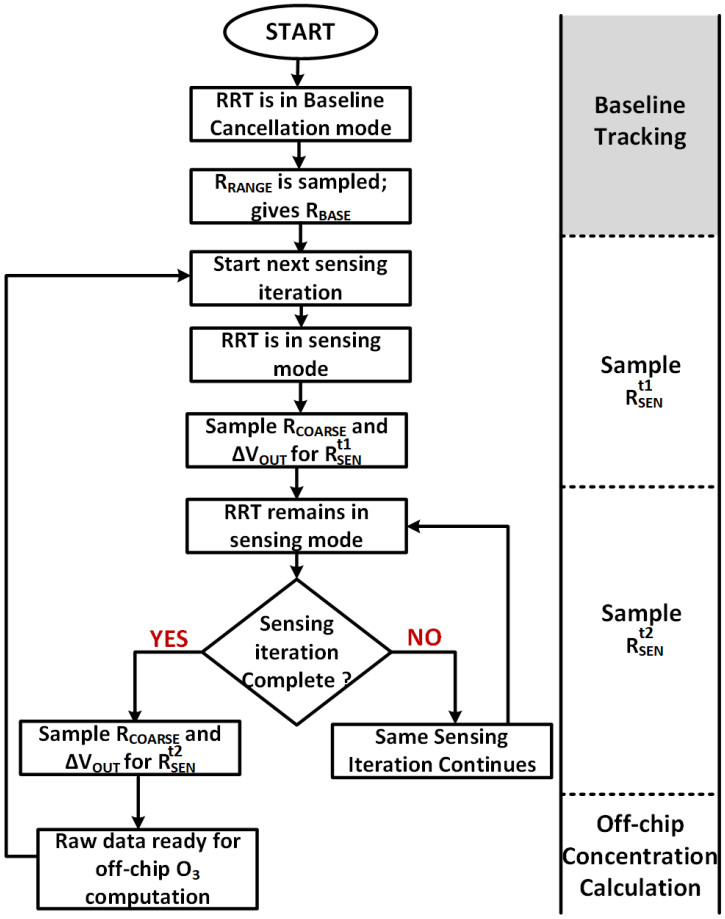

Figure 2.11: Flowchart depicting the ozone analog front-end's operation.

2.4 Measurements

To validate the design decisions and verify functionality, the sub-μW ozone analog front-end discussed in this section was taped-out and fabricated in 65-nm bulk CMOS process as a part of a multi-modal front-end design. The ozone sensing channel contributed to an active area of 1.28 mm^2. A die micro-photograph of the multi-modal analog front-end IC marked to show the presented sub-μW ozone AFE is shown in Fig. 2.12.

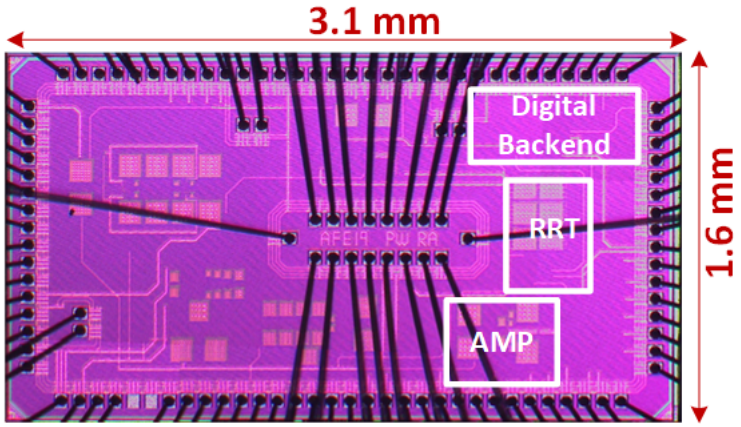

Figure 2.12: Die microphotograph of the multi-modal analog front-end.

Fig. 2.13 shows the measured transfer function of the presented analog front-end. In order to obtain the transfer function, the analog front-end's differential output voltage (left), and the associated sensor biasing current I_{BIAS} (right) sourced from M1 is measured while sweeping the resistance of a variable resistor across a range of 4.5 kΩ to 1.53 MΩ. It is also observed that using the proposed design technique, the entire resistance range is divided in 37 sub-ranges.

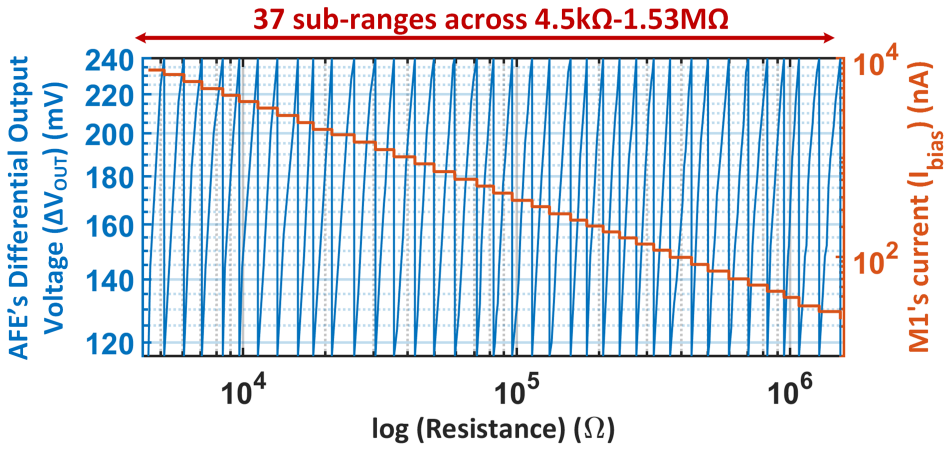

Figure 2.13: Measured transfer function of the ozone analog front-end.

The total input referred noise of the analog front-end is measured using a Keysight 35670A

dynamic signal analyzer. Since the signal from the sensor is near DC-level, a bandwidth of 0.1 Hz – 1 Hz is sufficient to measure the AFE's total input referred noise. As shown in Fig. 2.14, this sub-μW ozone sensing analog front-end has a total input voltage noise of 460 nV_{rms} across a signal bandwidth of 0.1 Hz to 1 Hz.

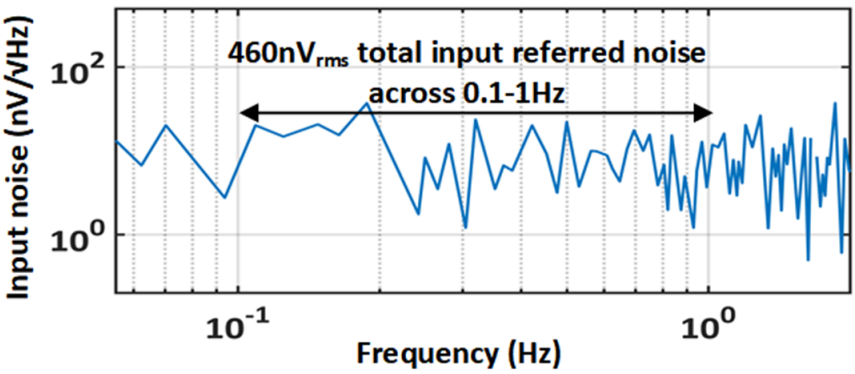

Figure 2.14: Measured input noise densities of the sub-μW ozone analog front-end.

Fig. 2.15 shows the measurements results with an atomic layer deposited (ALD) SnO_2 metal-oxide sensor previously fabricated at NCSU [17]. Ozone was generated using a "Teledyne T700U" gas calibration system, and was directed into a custom testing chamber encasing the sensor. To provide similar testing conditions at each concentration, the sensor's surface was exposed to a UV LED to desorb the ozone particles from its surface. The raw data from the analog front-end IC was post-processed off-chip to map the resistance change (ΔR_{GAS}) to ozone concentrations (C) using (2.12) and (2.13). Here, time denotes the duration for which the sensor is exposed to ozone, while α is obtained by sensor characterization which is out of the scope of this thesis.

$$\Delta R_{GAS} = \frac{\Delta V_{OUT}}{A_{CL} I_{BIAS}} \tag{2.13}$$

To calculate dynamic range for the gas channel, we consider the measurement time of 120 s

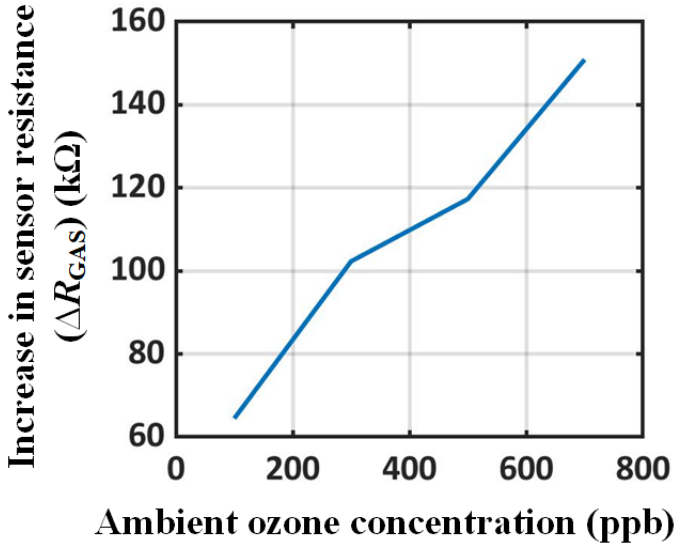

Figure 2.15: Measured resistance change at the corresponding ozone concentrations observed by the analog front-end.

which decreases the input-referred noise to 44.26 nV_{rms}. For an input signal range of 6–12 mV, the noise value of 44.26 nV_{rms} corresponds to an SNR of 102.64–108.66 dB (2.14). The ozone sensors we tested have a resistance range from 20 kΩ to 1 MΩ. Meanwhile, to support resistance variation due to surface poisoning, the readout is designed to achieve a resistance range of 4.5 kΩ –1.53 MΩ, resulting in a dynamic range of 50.63 dB (2.15). Thus, the corresponding dynamic range for the ozone channel is calculated to be 153.27–159.29 dB (2.16).

$$SNR = 20log(\frac{\text{input signal range}}{\text{input referred noise}}) \tag{2.14}$$

$$DR_{RES} = 20log(\frac{R_{MAX}}{R_{MIN}}) \tag{2.15}$$

$$DR_{AFE} = SNR + DR_{RES} \tag{2.16}$$

Table II summarizes the power and performance of the proposed chip and compares them with other state-of-the-art readouts. The power consumed by the sensor biasing current source

(M1) is within a range of 14.2 nW to 4.54 μW for sensor resistances lying between 4.5 kΩ to 1.53 MΩ. Table III provides the power breakdown of the proposed ozone sensing AFE and its system.

TABLE II

PERFORMANCE SUMMARY AND STATE-OF-THE-ART COMPARISON

	[49] This Work	[15] JSSC'09	[16] JSSC'07	[19] ISCAS'11	[50] TbioCAS'11	[51] JSSC'07	[52] JSSC'16
Technology	65 nm	180nm	350nm	500nm	180nm	350nm	350nm
Supply Voltage (V_{AFE})	0.6V	1.2V	3.3V	3.3V	1.8V	3.3V	3V
Area	1.28mm^2	0.72mm^2	3.1mm^2	4.84mm^2	3.89mm^2	0.42mm^2	12mm^2
Readout Power	76 nW	32µW	2.3mW	66µW	42.3µW-96.6µW	15mW	889µW
I_{BIAS} Power	14.2nW–4.54µW	N/R	2.8mW	N/R	N/R	3.3nW-3.3mW	N/R
Resistance Range	4.5kΩ - 1.53MΩ	10kΩ - 9MΩ	100Ω - 20MΩ	60kΩ - 10MΩ	1kΩ - 1.5MΩ	1kΩ - 5MΩ	1Ω - 10MΩ
Dynamic Range	153.27dB–159.29dB	N/R	160dB	120dB	N/R	128dB	N/R

TABLE III

MEASURED POWER BREAKDOWN OF THE SYSTEM

Analog Front-End		
Ozone readout	**Components**	**Power**
	AMP + RRT loop	73 nW
	Digital Backend	3 nW
AFE misc.		12.6 nW
Others		
Blocks		**Power**
Sensor Biasing Current Source (I_{BIAS})		14.2 nW – 4.54 µW
System Power		
Components		**Power**
AFE system power		102.8nW – 4.63µW

Fig. 2.16 highlights the contributions of this work by comparing its dynamic range, resistance range and analog front-end power with other state-of-the-art gas sensing analog front-ends and systems. This work achieves a 300x power reduction in its analog front-end while maintaining

competitive dynamic range.

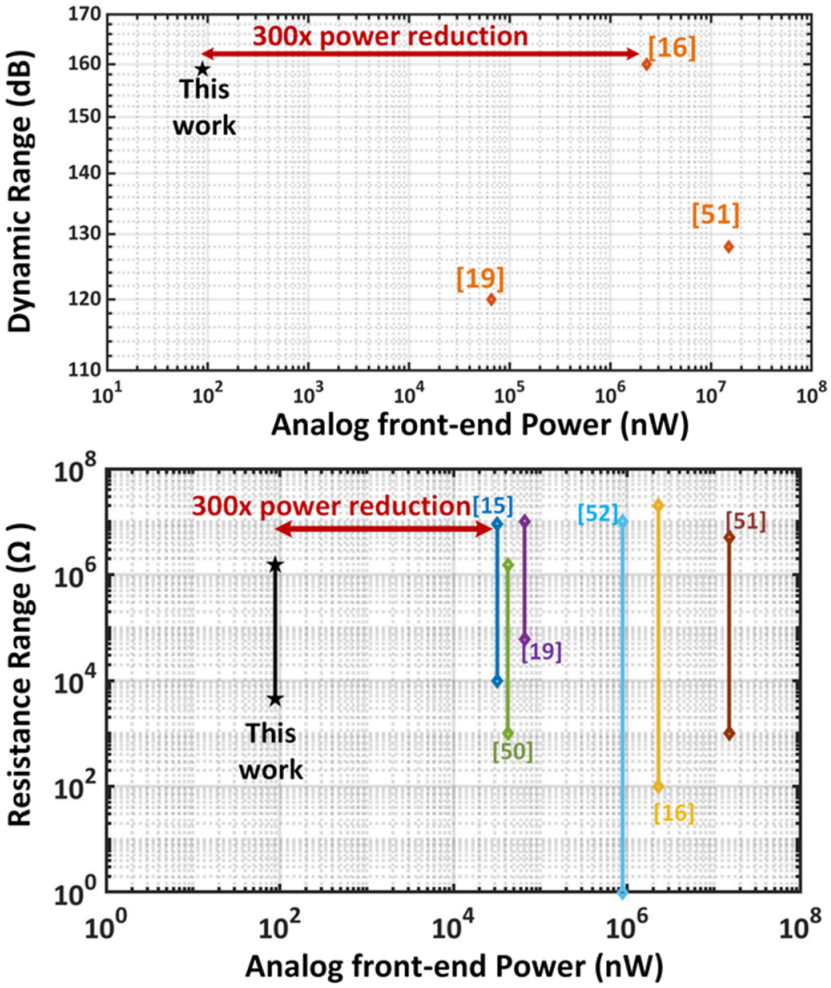

Figure 2.16: Comparison between this work's ozone analog front-end and previous gas sensing readouts for the dynamic range (top), resistance range (bottom) versus AFE power tradeoff.

2.5 Conclusion

This section presents a sub-μW, high dynamic range ozone analog front-end to enable wearable self-powered operation. It implements a resistance range tracker to dynamically vary the sen-

sor biasing current, it enables the analog front-end to operate at lower supply voltages. This allows the analog front-end to support the sensor's large resistance range, while reducing its power consumption. Additionally, by evaluating various design considerations, the sensor's biasing current is optimized to further reduce the total power consumption. A test chip is fabricated in 65-nm CMOS technology to validate the design. The presented analog front-end successfully uses the adaptive architecture for operating at a supply voltage of just 0.6 V. It improves the power-performance tradeoff by consuming 300x lower readout power measured to be 88.6 nW, while achieving a competitive dynamic range of 153.27 dB – 159.27 dB. The sensor biasing source consumes an additional power within a range of $14.2nW$–$4.54\mu W$ across sensor resistance ranging from 4.5kΩ to 1.53MΩ. Therefore, this work helps in extending the state-of-the-art multi-modal self-powered sensing nodes by enabling sub-μW ozone sensing. A list of contributions presented in this chapter are as follows:

1. Designed chopper-stabilized differential amplifier for improving the readout's signal-to-noise performance and subsequently increase its dynamic range.

2. Implemented adaptive sensor biasing technique to limit the sensor's output voltage within the analog front-end's operating range, allowing the AFE to operate at low supply voltages while supporting a large resistance range.

3. Reduced the sensor biasing current source's power consumption while achieving large resistance range by ensuring adequate biasing current values.

4. Designed the digital-backend to assist the AFE in detecting the increase in sensor's resistance.

CHAPTER 3

ANALOG FRONT-END FOR SUB-35μW AMBIENT GAS SENSING

3.1 Introduction

With the increase in global warming and carbon footprint, the air pollution across the globe is reaching alarming levels. According to the World Health Organization's recent survey, nine out of ten people are exposed to significant levels of both ambient and household air pollutions [20]. Chapter 2 of this dissertation implements a sub-μW ozone sensing AFE. However, in addition to ozone, other gases like volatile organic compounds (VOCs) emitted by pesticides, automotive products etc., nitrogen dioxide (NO_2), etc. are also a cause of great concern [21], [22]. Depending on their concentration and the length of exposure time, these gases can have minor or significant adverse effects often leading to emergency room visits. Due to the effects on a person's respiratory and cardiovascular health, there is a growing push for doctors to include screening of patients for exposure to certain air pollutants. Sensing systems like electronic nose (E-nose) dedicated towards continuous monitoring of multiple harmful gases can help mitigate this issue. In addition to environmental sensing applications, gas sensing is also being considered for monitoring certain exhaled gases that serve as important biomarkers for various diseases [23]. While chapter 2 successfully implements a sub-μW analog front-end design for ozone monitoring, there are some design gaps

and requirements that need to be satisfied in order to extend the design's use cases to all of the above-mentioned applications. These design gaps are discussed below.

1. **Low-power Integration of Sensor's Peripheral Devices:** The gas sensing analog front-ends designed in this dissertation target ALD metal-oxide (SnO_2) gas sensors. Typically, the metal-oxide gas sensors have high sensitivity. However, once these sensors are exposed to the target gas, the gas molecules start absorbing on the sensor's surface which results in variation in the sensor's resistance. For example, in case of SnO_2 sensors targeting ambient ozone, the ozone molecules get absorbed on the sensor's surface, and fill up the vacancies through ionization leading to decrease in the sensor's conductivity. However, after prolonged exposure, the number of free electrons is largely depleted, and the sensor's resistance starts to saturate. This point is referred to as the sensor's "saturation point". Beyond this point, the sensor's sensitivity starts degrading, which leads to poor sensor node performance (3.1). In order to recover the sensor's sensitivity, ultra-violet LED illumination is used. This helps in desorbing gas molecules from the sensor's surface, and retain good sensitivity throughout the sensor node's lifetime. Therefore, it is imperative to integrate UV LED illumination in a gas sensing system. However, this adds significant power overhead, requiring intervention of power-saving circuit or system level techniques.

$$S_{SEN} = \frac{\Delta R_{GAS}}{R_{BASE}} \tag{3.1}$$

2. **Multi-functional Analog Front-end:** The gas sensing analog front-ends designed in this thesis target ALD metal-oxide (SnO_2) gas sensors. When in contact with the sensor's surface, inorganic gases like ozone and nitrogen dioxide have an oxidizing effect which results in an increasing sensor's resistance in response to the target gas concentration. However, some gases like acetone produce a reducing effect on the sensor's surface resulting in a de-

crease in sensor's resistance [24]. This requires an AFE architecture which is capable of detecting both the rate of increase or decrease in the sensor's resistance while still operating in sub-μW power region.

3.2 Design Challenges and Prior Art

The analog front-end presented in Chapter 2 explores the design space for gas sensing analog front-ends, and introduces design techniques for enabling sub-μW personal ozone sensing while achieving high dynamic range performance. This is achieved by implementing the following two solutions. First, an adaptive architecture (RRT) limits the sensor voltage (V_{SEN}) to a pre-determined voltage range such that the AFE can operate at a much lower V_{AFE} of 0.6 V, and reduce the readouts power contribution. Second, the sensor biasing current I_{BIAS} is optimized to further reduce the total AFE power. Additionally, the design also implements chopping to reduce the total input referred noise, and subsequently improve the dynamic range performance. However, this architecture has certain limitations preventing it to be further used for applications involving sensing gases with reducing nature. A detailed discussion of these limitations is provided below.

Generation 1 of the AFE (Chapter 2) leverages ozone's oxidizing nature, and implements a resistance range tracker to aid in measuring the rate of increase in sensor resistance (dR_{SEN}/dt). By implementing RRT, the sensor's entire resistance range is divided into multiple sub-ranges, which are then identified by tracking the voltage generated across the sensor (V_{SEN}). The Gen I ozone AFE is designed to detect an increase in sensor resistance. Therefore, each time V_{SEN} exceeds the pre-determined voltage range (indicated by the voltage monitor's threshold, V_H) the adaptive current biasing loop adjusts I_{BIAS} to regulate V_{SEN} back to V_{FB}, while the RRT updates the resistance sub-range by incrementing the counter, R_{COARSE}.

However, in the case of reducing gases like acetone, the sensor's resistance decreases in response to the gas concentration. Due to this decrease in sensor resistance, V_{SEN} would also start decreasing. Since the Gen I AFE's RRT updates the resistance sub-range by tracking an increase in V_{SEN}, it would fail to update the resistance sub-range for the reducing gases. This renders the Gen I AFE, presented in Chapter 2, incompatible for sensing gases of the reducing nature. Fig. 3.1 shows a basic model of the Gen I approach. The voltage monitor outputs, $Comp_H$ and $Comp_L$, which are then fed as inputs to the digital backend. Thus, the Gen I AFE's RRT identifies the resistance sub-range solely on the basis of V_{SEN}. This is because the digital backend utilizes $Comp_H$ and $Comp_L$ to detect an increase in R_{SEN}, and $Comp_H$ and $Comp_L$ are both just a function of V_{SEN}. This can be avoided by identifying the resistance sub-range as a function of both V_{SEN} and I_{BIAS}. Therefore, the adaptive architecture of GEN I requires modifications to support applications involving both reducing and oxidizing gases.

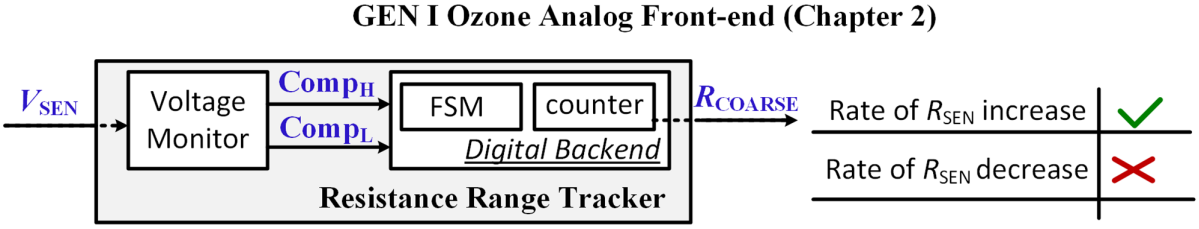

Figure 3.1: Block diagram demonstrating the basic model of GEN I ozone AFE.

The system power for a gas sensing node comprises of the power consumed by the analog front-end (P_{AFE}), and the UV LED power (P_{UV}) (3.2). Average UV LED power is a function of the UV LED's driver's supply voltage (V_{DD-UV}), the current consumed by the LED (I_{UV}), and its duty cycle rate (D_{UV}). Here, the duty cycle rate is the product of UV LED's on-time (t_{UV}), and the frequency at which it is turned on (f_{UV}) (3.3).

$$P_{SYS} = P_{AFE} + P_{UV} \tag{3.2}$$

$$P_{UV} = V_{DD-UV} I_{UV} D_{UV} = V_{DD-UV} I_{UV} t_{UV} f_{UV} \tag{3.3}$$

Since Chapter 2 has already presented the design techniques for lowering the AFE's power to sub-μW range, the UV LED now dominates the system power. Previous works that use UV LED illumination for recovering the sensor's sensitivity, have resorted to aggressively duty cycling the UV LED at a fixed rate. This results in an average power consumption of $\sim$150 μW, with the UV LED dominating the total sensor node power [10]. However, this power level is not suitable for self-powered wearable systems, and would overtax the on-body energy harvesters. Additionally, even though this approach helps in retaining the sensor's sensitivity, it is not the most power-efficient method. This is because, when the sensor is exposed to the target gas, the rate at which the resistance increases/decreases varies with different concentration levels of the target gas. Therefore, the time in which the sensor starts saturating also varies with the gas concentrations. This can be seen in Fig. 3.2, where the rate of increase in sensor resistance (R_{SEN}) is plotted for three different ozone concentration levels C_1, C_2, and C_3. Here, at the highest concentration level (C_3), the sensor saturates within time t_3 which is much faster than the time taken by the sensor at lower concentrations (C_1 and C_2). Fig. 3.2 also shows the traditional approach, wherein the UV LED is duty cycled at a fixed rate.

In this method, the sensor's saturation time at the highest gas concentration level (C_3) is chosen to quantify the length of each measurement cycle. This essentially sets the UV LED duty cycle rate as it is turned on at the end of each measurement cycle. However, in scenarios involving exposure to lower gas concentrations (C_1, C_2), the sensor would not reach saturation in time t_3. Despite this, with the traditional fixed duty cycle approach, the UV LED would still be turned on. This wastes power, as the sensor is yet to saturate for both the concentration levels (C_1 and C_2), and also adds significant power overhead. Also, an event with very high levels of harmful gases such as ozone is not very frequent in most environments, thereby again making the traditional approach

both unnecessary and power hungry. Therefore, a more intelligent approach of duty cycling the UV LED is required.

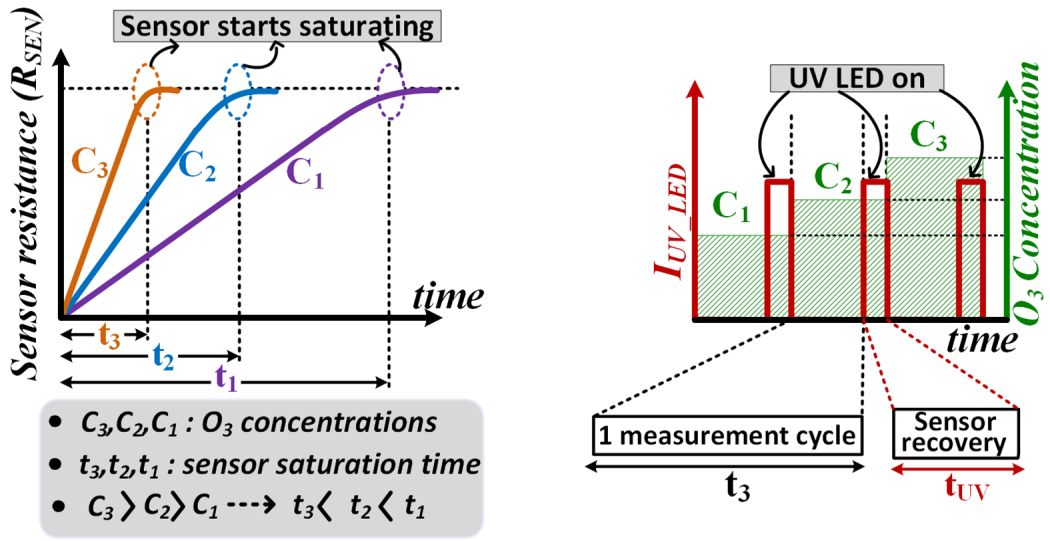

Figure 3.2: Gas sensor's resistance variation at different ambient gas concentrations (left), and traditional approach with UV LED turning on at a fixed duty cycle rate (right).

3.3 Design Approach

While keeping the fundamental design choices from GEN I of ozone analog front-end (Chapter 2), this section of the dissertation identifies and incorporates necessary design changes to implement a more modular AFE that can support both reducing and oxidizing gases. Here, the RRT from GEN I is replaced with a switched-capacitor resistor (SCR) based biasing loop to identify the resistance sub-range as a function of both V_{SEN} and I_{BIAS} (Fig. 3.3). This removes the AFE's dependency on the incrementing characteristic of the sensor's resistance, and enables the AFE to detect both an increase or decrease in sensor resistance. Thus, a multi-functional sensing node is

realized which can be used for variety of applications, including but not limited to, e-noses for medical diagnosis, indoor and outdoor air quality monitoring etc.

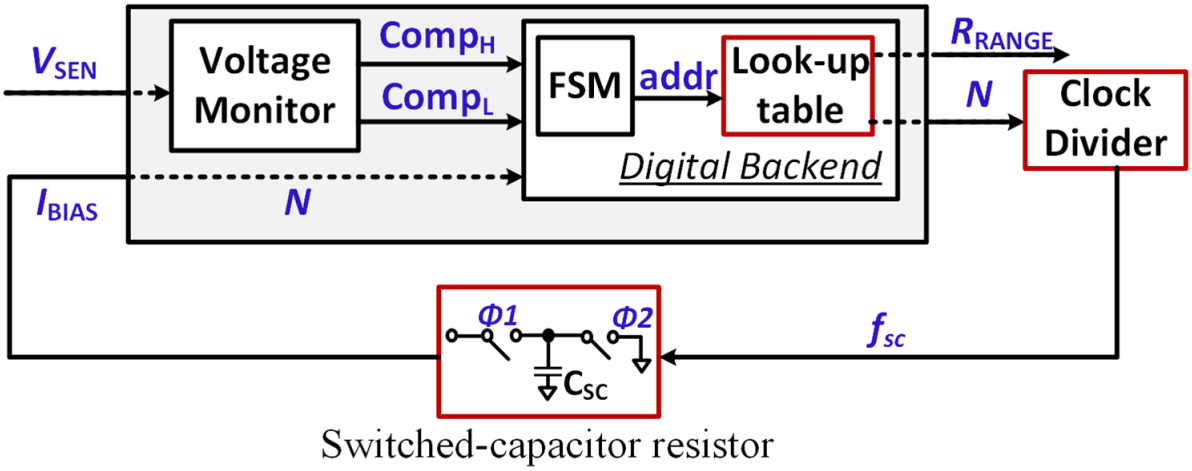

Figure 3.3: Block diagram demonstrating the basic model of the proposed GEN II AFE.

This chapter also addresses another critical issue, which is enabling low-power integration of the UV LED in an energy-constrained gas sensing node. As an intelligent alternative to the traditional fixed duty cycle method, this work implements a sensor saturation detector (SSD), which is periodically turned on to predict the sensor's saturation point, and subsequently make a decision on turning on the UV LED. Fig. 3.4 shows that by using the proposed sensor saturation detector, the AFE is able to recognize that the sensor saturates only at C_3 concentration, and as a result it does not turn on the UV LED for the remaining two cases (@ C_1 and C_2). Therefore, by adaptively duty cycling the UV LED, sensor sensitivity is maintained and the LED power consumption is also reduced.

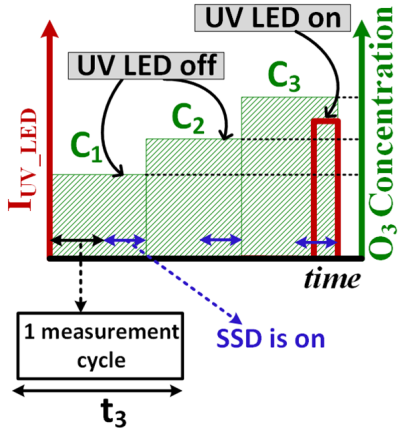

Figure 3.4: Adaptive UV LED duty cycling with proposed sensor saturation detector (SSD) block.

3.3.1 System Architecture

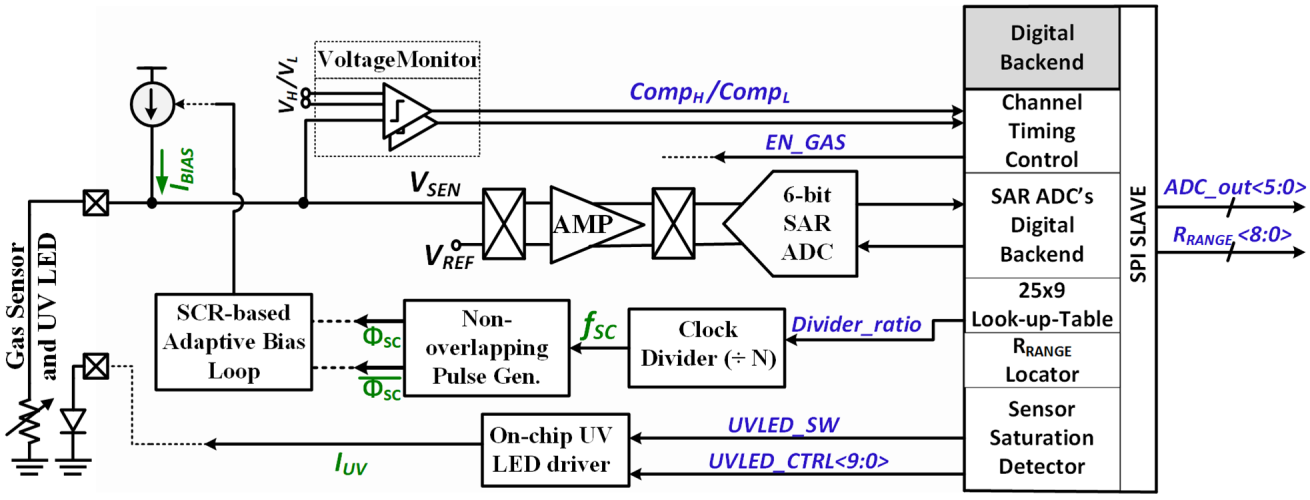

Figure 3.5: Architecture of the proposed ambient gas sensing system.

Fig. 3.5 shows the system architecture of the proposed GEN II gas sensing analog front-end. It comprises the proposed switched-capacitor resistor (SCR) based adaptive biasing loop, an integer-based programmable clock divider (on-chip), a UV LED driver, a voltage monitor, a

chopper-stabilized differential amplifier (AMP), a 6-bit SAR ADC, and associated digital back-ends. The SCR loop generates sensor biasing current (I_{BIAS}), and sources it to the gas sensor (R_{SEN}) for implementing R-V conversion. The resulting sensor voltage (V_{SEN}) is applied as an input to the chopper stabilized amplifier, AMP. Owing to the design decisions made in Chapter 2, the amplifier's other input (V_{REF}) is fixed at 30 mV. The chopper-stabilized amplifier AMP has a closed loop gain of $\sim$26dB, and follows an architecture similar to the one discussed in Chapter 2. The chopping frequency is again set to 1kHz to both remove the 1/f noise at lower frequencies, and also convert DC input to an AC differential signal for amplification. The voltage monitor tracks the sensor voltage (V_{SEN}), and sends the output ($Comp_H$ and $Comp_L$) to the digital backend. The AFE's digital backend includes a timing block, a sensor saturation detector, a programmable look-up-table (LUT) to store clock divider ratios (N) for each resistance sub-range, and a serial-to-parallel interface (SPI). The look-up-table consists of 25, 9-bit columns, one for each resistance sub-range. The SCR receives its clock pulses (ϕ_{sc}, $\overline{\phi_{sc}}$) from a non-overlapping pulse generator. An on-chip programmable clock divider is implemented to perform integer-based frequency division. The clock divider divides a 1MHz reference clock source using the 9-bit divider ratio (N) obtained from the look-up-table. Both the digital and analog components operate at a supply voltage of 0.6 V. The system also includes an on-chip LED driver, designed to operate at 3.3 V, and generate LED current ranging from 1 mA to 9 mA.

3.3.2 Switched-Capacitor Resistor Based Adaptive Bias

As mentioned before, Chapter 2's GEN I analog front-end identifies resistance sub-range solely on the basis of V_{SEN} by leveraging the ozone sensor's behavior. Thus, as a downside of this design choice, it can only detect the rate of increase in resistance. In order to extend this approach towards detecting any type of sensor resistance variation including both increase and

decrease, this section of the dissertation implements a switched-capacitor resistor based adaptive biasing technique in place of the resistance range tracker.

As shown in Fig. 3.6, the SCR-based biasing loop features a PMOS transistor (M1) acting as a current source used to bias the switched capacitor resistor (R_{SCR}). The switched-capacitor resistor comprises of a 100 pF capacitor, and two transmission gates acting as complementary switches S1 and S2. The switches are toggled using complementary clock pulses, resulting in continuous charge transfer (3.4). Therefore, the SCR is essentially a resistor with equivalent resistance given by (3.5). The SCR resistance can be modified by changing its toggling frequency (f_{SC}).

$$I_{SCR} = \Delta q f_{SC} = C_S \Delta V_{SCR} f_{SC} \tag{3.4}$$

$$R_{SCR} = \frac{\Delta V}{I_{SCR}} = \frac{1}{C_S f_{SC}} \tag{3.5}$$

Transistor M1's gate is regulated by a negative feedback amplifier (FB) such that the generated current I_{SCR} drives the switched-capacitor resistor's (R_{SCR}'s) voltage (V_{SCR}) to V_{FB}. Here, the feedback amplifier FB has a similar architecture to the one described in Chapter 2. This current I_{SCR} is copied via current mirror pair M1 and M2, and subsequently used for biasing the gas sensor (R_{SEN}) (3.6). Therefore, the voltage generated across the sensor (V_{SEN}) is also equivalent to V_{FB}. The look-up table is programmed to contain divider values needed to emulate each resistance sub-range.

$$I_{BIAS} = I_{SCR} = \frac{V_{FB} C_{SC} f_{REF}}{N} \tag{3.6}$$

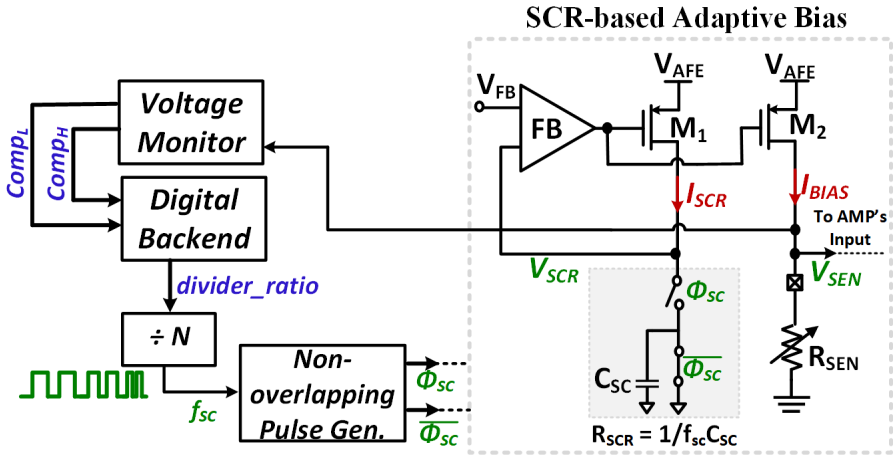

Figure 3.6: Schematic of the proposed switched-capacitor resistor-based adaptive biasing loop.

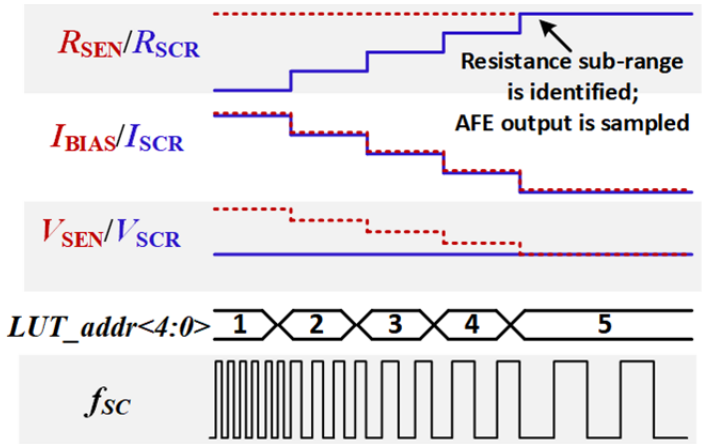

Figure 3.7: Timing diagram demonstrating SCR-based adaptive bias loop's operation.

Fig. 3.7 shows the timing diagram demonstrating the SCR based biasing loop's operation. As the biasing loop begins its operation, the divider value retrieved from the first LUT address is provided to the clock divider, which then generates the corresponding f_{SC}, and updates SCR's equivalent resistance (R_{SCR}) (3.6). Simultaneously, the biasing loop's negative feedback tunes M1's gate voltage to regulate I_{SCR} such that V_{SCR} returns to V_{FB}. This current I_{SCR} is also copied and sourced on the sensor (R_{SEN}). However, as seen in Fig. 3.7, if R_{SCR} is not yet equal to

R_{SEN}, the voltage (V_{SEN}) generated across the actual sensor would be higher than V_{FB}. The voltage monitor compares V_{SEN}, and indicates that the voltage across the sensor is not within the pre-determined voltage range. Following this, the digital backend signals the clock divider to retrieve the divider value stored in the next LUT address. With a new divider value, the on-chip clock divider updates the f_{SC} frequency which in turn changes the switched capacitor's equivalent resistor (R_{SCR}). Due to lower f_{SC}, the SCR equivalent resistance increases. This results a sudden jump in V_{SCR}, causing the adaptive biasing loop to lower I_{SCR} so that V_{SCR} is regulated back to V_{FB}. This drop in I_{SC} is also mirrored in I_{BIAS} which in turn decreases the V_{SEN}. This continues till V_{SEN} again falls within the desired voltage range. Once this state is achieved, the R_{RANGE} is updated with the most recently accessed LUT address. This LUT address gives the value of I_{BIAS}. Thus, unlike GEN I, this approach identifies the resistance sub-range on the basis of both V_{SEN} and I_{BIAS}, making it suitable for detecting rate of increase as well as decrease in resistance.

A programmable on-chip frequency divider is designed to work alongside the look-up-table, and generate the clock frequencies required by the switched capacitor resistor. The look-up-table provides the clock divider with a 9-bit input (divider_ratio$< 8 : 0 >$). This input's most significant bit (divider_ratio$< 8 >$) denotes if the divider ratio is odd or even, and the remaining 8 least significant bits (divider_ratio$< 7 : 0 >$) contain the divider ratio. Due to area concerns, the SCR's capacitor is limited to 100 pF. Thus, in order to cover a resistance range of 20kΩ to 1MΩ, a reference clock frequency of 1MHz is chosen.

The clock divider consists of two 8-bit counters, pos_count$< 7 : 0 >$ and neg_count$< 7 : 0 >$, incrementing at positive and negative edges of the reference clock. When the divider ratio is an even integer, pos_count$< 7 : 0 >$ is incremented at every positive edge of f_{REF}, while the divider's output is held at the same logic level. Once the pos_count value exceeds the value "divider_ratio – 1", the divider output is inverted, and the counter is reset. During division by an even integer, the

counter neg_count$< 7 : 0 >$ is disabled.

In case of division by an odd integer, both the 8-bit counters pos_count$< 7 : 0 >$, and neg_count$< 7 : 0 >$ are incremented at every positive and negative clock edges, respectively. Here, both the counter thresholds are set to the value obtained by applying right shift operator to divider ratio. Once either of the counter values exceeds this threshold, the divider output is raised to logic high.

3.3.3 Sensor Saturation Detector

This work implements an intelligent alternative to fixed duty cycling of the UV LED in prior gas sensing systems [10]. The sensor saturation detector (SSD) works together with the SCR adaptive bias loop to predict when the sensor is approaching saturation, and makes an informed decision on when to turn on the UV LED. Thus, the UV LED is duty cycled on the basis of degradation in the sensor's sensitivity.

For the purposes of decision making, this work predicts the sensor's saturation by tracking its $\frac{dR_{SEN}}{dt}$. To implement this, the sensor saturation detector tracks the time (*sub-range_time*) spent by the sensor in each resistance sub-range (R_{RANGE}). It can be argued that the decision of turning on the UV LED can be also made on the basis of the resistance value at which the sensor saturates. This work makes a design choice to not use this approach for the following reason. Different gas sensors do not have the same resistance range. Thus, the resistance value at which each sensor saturates is also different. If the SSD were to make a decision solely on the basis of this resistance value, the AFE would never turn on the UV LED for sensors with lower resistance ranges. Thus, in order to make the AFE more modular and sensor-agnostic, the proposed sensor saturation detector tracks the degradation in the slope of the sensor's response.

Fig. 3.8 shows a detailed timing diagram for the SSD's operation. The sensor saturation detector is synthesized along with the digital backend. It outputs the control signals *UVLED_SW* and *UVLED_CTRL*$< 9:0 >$ to turn on and program the current from the UV LED. Each time the AFE completes one measurement cycle, the sensor saturation detector block is turned on. When active, the sensor saturation detector tracks R_{RANGE}, to know the resistance sub-range at any instant. Simultaneously, the 12-bit *sub-range_time* counter is continuously incrementing to track the time spent in each resistance sub-range. During this mode, the sensor saturation detector also compares the 12-bit *sub-range_time* data to a programmable threshold. This continues till one of the following two scenarios are met. First, if at any point, the *sub-range_time* value exceeds the associated threshold, it is inferred that the sensor's response has started becoming non-linear. Thus, in response to this, the UV LED is turned on to start sensor recovery. Second, if the sensor jumps to the next resistance sub-range, the *sub-range_time* counter is reset. Following this, the *sub-range_time* counter restarts its counting process, and compares the *sub-range_time* data with the new threshold. The sensor saturation detector remains on for a fixed period of time, following which the AFE again returns to the measurement mode. As seen in Fig. 3.8, the SSD mode ensures that the UV LED is turned on only when the sensor saturates, i.e., during exposure to concentration level, C_3. Before the system is deployed, the counter thresholds associated with each resistance sub-range are programmed using SPI. These values are carefully chosen after characterizing the different sensors deployed with the AFE.

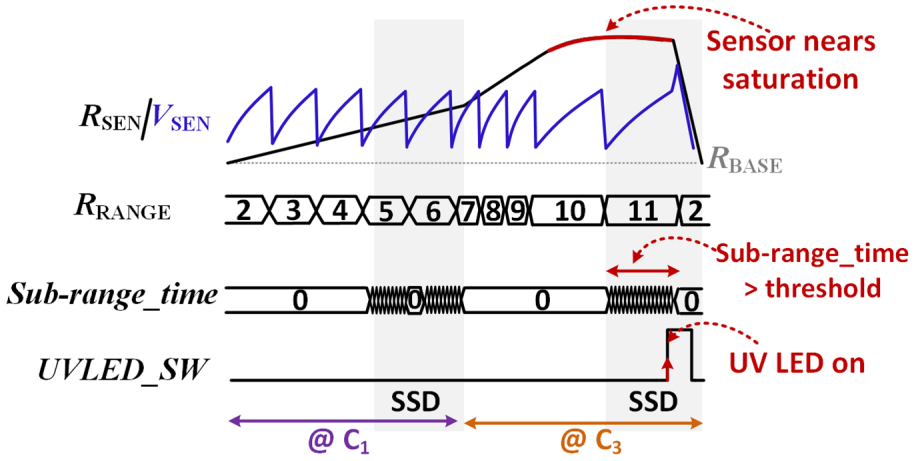

Figure 3.8: Timing diagram showing the proposed SSD mode's operation.

The UV LED adaptive duty cycle rate achieved by the SSD block can be computed as follows. The saturation time (T_{SAT}) of the sensor differs with gas concentrations, and can be denoted as a function of the resistance at which the sensor saturates (R_{SAT}), and the rate of resistance variation for different concentrations (3.7). The number of measurement cycles (M) after which sensor saturation can be observed is given by (3.8), where T_{MEAS} is the length of each measurement cycle. Therefore, the total period (T_{TOTAL}) of the new duty cycle rate, and the number of times sensor can saturate in one such period (N_{UV}), is given by (3.9) - (3.10). Since, the presence of these gases is not a continuous event, the average LED power is also a function of the probability (p) of the user coming in contact with different gas concentrations. Thus, the average UV LED power (P_{UV-LED}) achieved by the SSD block can be given by (3.11). Here, t_{UV} is the UV LED on-time, and P_{IN} is the instantaneous LED power.

$$T_{SAT} = \frac{R_{SAT}}{dR_{SEN}/dt} \tag{3.7}$$

$$M = \lceil \frac{T_{SAT}}{T_{MEAS}} \rceil \tag{3.8}$$

$$T_{TOTAL} = T_{MEAS} * M \tag{3.9}$$

$$N_{UV} = \lfloor \frac{T_{TOTAL}}{T_{SAT}} \rfloor \tag{3.10}$$

$$P_{UV-SSD} = p * (\frac{t_{UV} N_{UV}}{T_{TOTAL}} P_{IN}) \tag{3.11}$$

3.3.4 Ultra-Violet LED Driver

As mentioned before, the system consists of a UV LED to facilitate sensor recovery. This work features a programmable LED driver for powering this UV LED. Typically, LEDs demonstrate an exponential I-V characteristics. In order to turn on an LED, it is necessary to bias it with a minimum forward voltage (V_F). After the LED is on, even a small perturbation in the LEDs supply voltage leads to a large increase in LED current. If this current exceeds the LED's maximum current rating, the LED is damaged. So, in order to avoid any damage to the LED, this work adopts a current regulator architecture.

Fig. 3.9 shows the schematic of the on-chip UV LED driver. The LED driver is designed to operate at 3.3 V. It consists of a current regulation loop comprising of an operational amplifier (Op-amp) connected in negative feedback with an NMOS transistor (N_1). A resistor (R_{DR}) senses the drain current of N_1, and returns it in the form of voltage (V_{DR}) to the op-amp's input. The op-amp acts as an error amplifier and adjusts N_1's drain current such that VDR matches the voltage V_{UV-REF}. The resistor R_{DR} is implemented using a p-type diffusion resistor with a value of 12 kΩ, and the V_{UV-REF} is set to 1.2 V. Thus, once the loop is able to match V_{DR} to V_{UV-REF}, the drain current (I_{DR}) through N_1 is regulated to 0.1 mA. With careful sizing, the PMOS current mirror pair (P1 and P2) amplifies the 0.1 mA current (I_{DR}) to 1 mA. Since, the UV LED requires a current within the range of 1 mA to 10 mA, additional nine branches identical to the one formed by N_1 and R_{DR} are added. Each of these branches can source a 0.1 mA of reference current, which after copying, generate 1 mA of final current. Thus, when these branches are simultaneously switched

on, they can source up to 10 mA of LED current. For the purposes of this work, an LED current of 1mA is sufficient. These branches are selected by signals *UVLED_CTRL*$< 9:0 >$, and the LED driver is power gated through signal *UVLED_SW*. These control signals are generated by SSD.

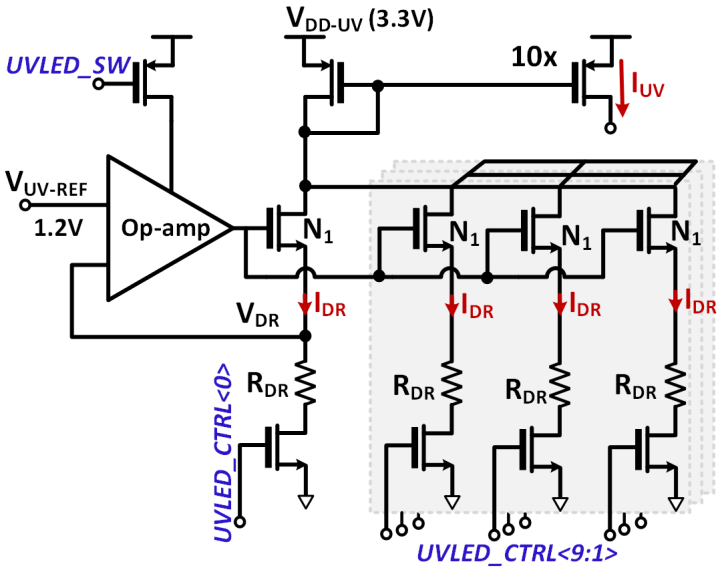

Figure 3.9: Schematic of the on-chip ultra-violet (UV) LED driver circuit.

3.3.5 System Operation

Fig. 3.10 shows the flow chart of the system operation. The proposed analog front-end operates in two modes: 1) measurement mode, and 2) sensor saturation detector (SSD) mode. After the system is deployed, the AFE waits for *EN_GAS* signal to switch to logic high. Once this occurs, the AFE enters its first measurement mode. The 5-bit address of the LUT (*LUT_ADDR*$< 4:0 >$) is read through SPI to indicate the I_{BIAS} value and the resistance sub-range at any given instant. Also, the 6-bit ADC output can be sampled to compute the instantaneous sensor resistance. A background 32-bit counter GAS#1 tracks the time spent in the measurement mode. Once the measurement mode time exceeds the length specified by the associated 32-bit threshold GAS#1,

the digital backend turns on the sensor saturation detector, programming the AFE in SSD mode. Now, another 32-bit counter GAS#2 tracks the time spent in the SSD mode. While in this mode, the analog front-end's SSD block predicts when the sensor is approaching saturation, and subsequently makes a decision on turning on of the UV LED. After GAS#2 counts one full cycle of its threshold, the AFE is re-programmed in the measurement mode. Unlike the design from Chapter 2, this AFE does not need baseline cancellation. The time spent in the measurement and SSD mode can be programmed using the SPI.

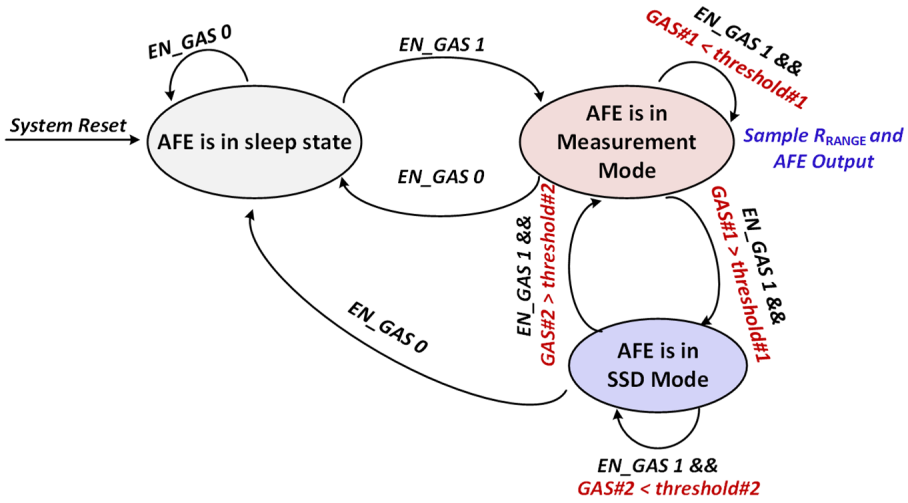

Figure 3.10: State transition diagram of system operation.

In order to program the AFE for sensing reducing gases, it is turned on only at the beginning and during the end of the measurement cycle. This is done by toggling the signal *EN_GAS* through SPI. Thus, at the end of the measurement cycle, both the extremas of the resistance value are available to the user for calculating $\frac{dR_{GAS}}{dt}$. Also, some of these reducing gases require pulsed heating for recovering sensor's sensitivity. These heating elements consume several milli-Watts of power. The SSD proposed in this dissertation is currently reserved only for the gases that utilize UV LED illumination for recovery. Therefore, the SSD mode is bypassed by setting the SSD

mode's threshold#2 to 1.

3.4 Measurement and Simulation Results

The presented multi-functional gas analog front-end was taped-out and fabricated in 65-nm bulk CMOS process. Fig. 3.11 shows the annotated die micrograph. The IC occupies a total area of 1.1435 mm^2, of which the analog components, clock divider, digital backend, 6-bit SAR ADC, and LED driver consume 0.643 mm^2, 0.0035 mm^2, 0.112 mm^2, 0.28 mm^2, and 0.105 mm^2, respectively

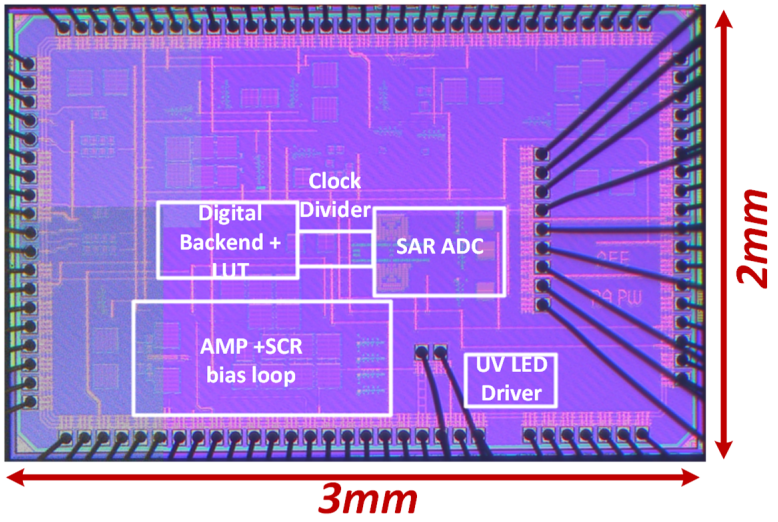

Figure 3.11: Die microphotograph of the multi-modal analog front-end.

Fig. 3.12 shows the measured transfer function of the analog front-end. In order to obtain the transfer function, the analog front-end's differential output voltage (ΔV_{OUT}) (left), and the associated sensor biasing current I_{BIAS} (right) sourced from M1 is measured while sweeping the resistance of a variable resistor across a range of 20 kΩ to 1 MΩ.

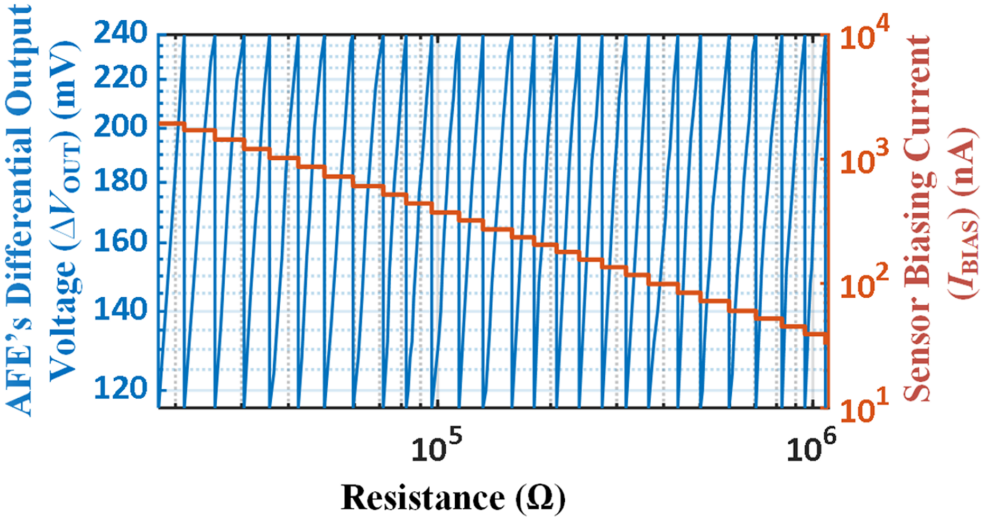

Figure 3.12: Measured transfer function of the analog front-end.

Fig. 3.13 shows the switched capacitor resistor based adaptive biasing loop's transfer function simulated with a reference clock of 1MHz. The plot follows the equation (3.6), and demonstrates that divider ratios ranging from 2 to 100 are able to generate sensor biasing current (I_{BIAS}) from 1.8μA to 36 nA.

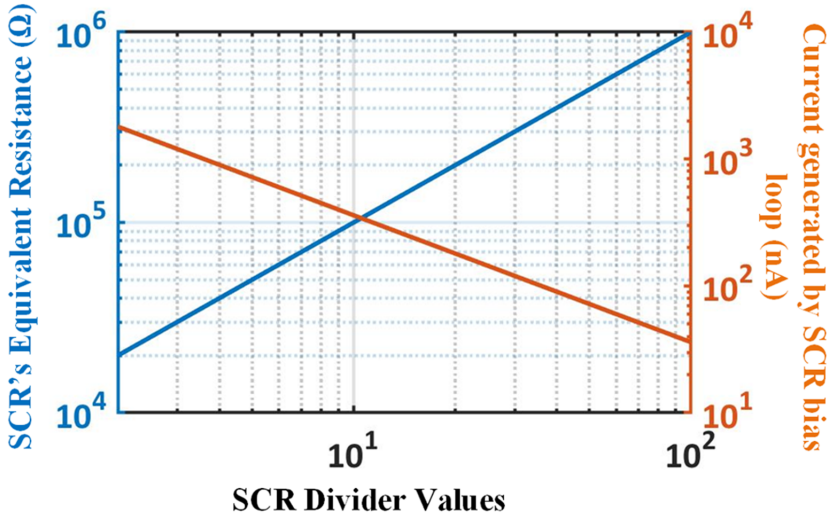

Figure 3.13: Switched-capacitor resistor based adaptive biasing loop's simulated transfer function.

An example of the adaptive UV LED duty cycling achieved by the sensor saturation detector is shown in Fig. 3.14. As observed in the figure, the UV LED only turns on in the measurement cycles wherein the sensor is approaching saturation point. Therefore, compared with prior works, the number of times the LED is turned on in this work will always be either equal or less, resulting in lower average LED power. This example measurement, results in an average power of 23.5 μW. While the AFE's measurement cycle length is of several minutes, it is difficult to capture a waveform spanning across such a long time. Therefore, this measurement is taken by programming the AFE to operate in the measurement and SSD mode for several seconds. As a result, the x-axis in Fig. 3.14 has been scaled to show the adaptive UV LED duty cycling.

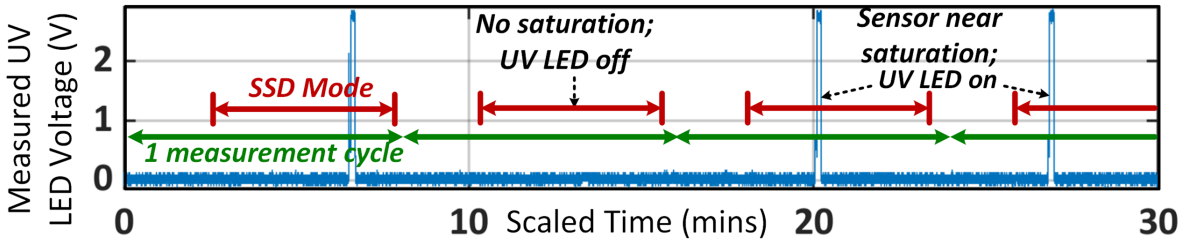

Figure 3.14: Measurement showing adaptive UV LED duty cycling using the proposed sensor saturation detector.

The total input referred noise of the analog front-end is measured using a Keysight 35670A dynamic signal analyzer. As shown in Fig. 3.15, this sub-μW ozone sensing analog front-end has a total input voltage noise of 405 nV_{rms} across a signal bandwidth of 0.1 Hz to 1 Hz.

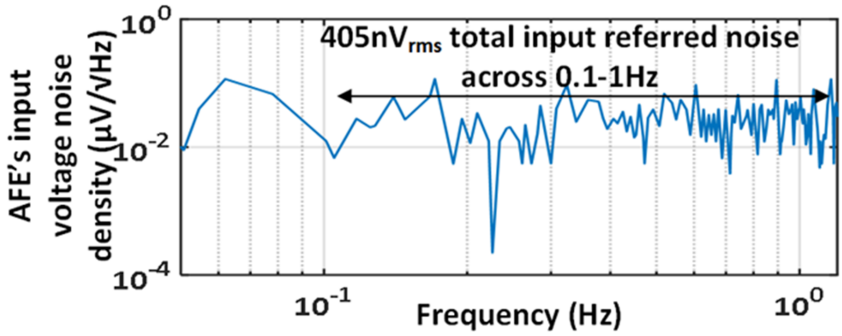

Figure 3.15: Measured input noise density of the proposed analog front-end.

Fig. 3.16 shows the measured output of the analog front-end in response to decreasing input resistance. The AFE is duty cycled using signal *EN_GAS* while detecting a decrease of 240kΩ in input resistance. Therefore, during the off-state, the AFE's measurement contains data points with a zero value. The raw data from the analog front-end IC was post processed to compute the decrease in resistance.

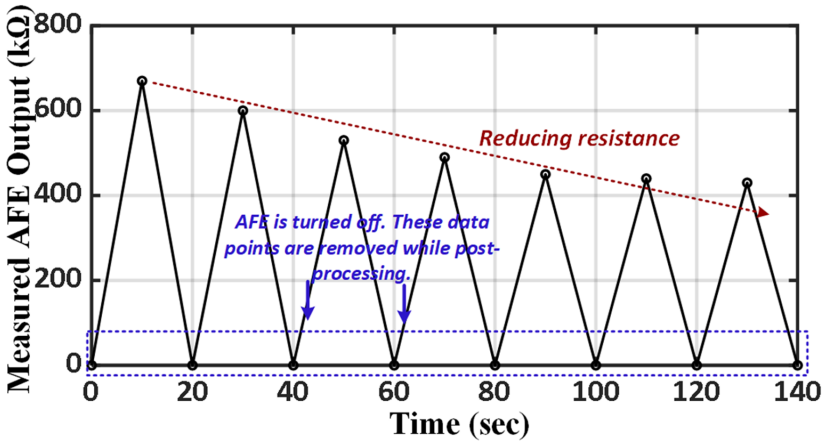

Figure 3.16: Measured AFE output for detecting rate of decrease in resistance.

TABLE IV

PERFORMANCE SUMMARY AND STATE-OF-THE-ART COMPARISON

	[53] This Work	[49] Chapter 2	[15] JSSC'09	[19] ISCAS'11	[50] TbioCAS'11	[51] JSSC'07	[52] JSSC'16
Technology	65 nm	65 nm	180nm	500nm	180nm	350nm	350nm
Supply Voltage (V_{AFE})	0.6V	0.6V	1.2V	3.3V	1.8V	3.3V	3V
Area	1.144mm^2	1.28mm^2	0.72mm^2	4.84mm^2	3.89mm^2	0.42mm^2	12mm^2
Readout Power	56 nW	76 nW	32µW	66µW	42.3µW-96.6µW	15mW	889µW
I_{BIAS} Power	28nW–2µW	14.2nW–4.54µW	N/R	N/R	N/R	3.3nW-3.3mW	N/R
Resistance Range	20kΩ - 1MΩ	4.5kΩ - 1.53MΩ	10kΩ - 9MΩ	60kΩ - 10MΩ	1kΩ - 1.5MΩ	1kΩ - 5MΩ	1Ω - 10MΩ
Dynamic Range	138dB–144dB	153.27dB–159.29dB	N/R	120dB	N/R	128dB	N/R

Table IV summarizes the power and performance of the proposed chip and compares them with other state-of-the-art readouts. The analog front-end maintains sub-μW operation and achieves 138-144dB dynamic range required by the sensor. It also mitigates the UV LED power overhead issue through the proposed sensor saturation detector, and achieves $>$5x system power reduction.

3.5 Conclusion

This section presents a sub-μW, high dynamic range analog front-end to enable ambient gas sensing in a wearable self-powered system. The metal-oxide gas sensors require UV LED illumination to maintain sensor's sensitivity throughout its course of operation. Prior works use an over-designed UV LED duty cycle rate, resulting in average power $>$150 μW. An as intelligent alternative, this work's analog front-end predicts the sensor's saturation point, and makes a decision on turning on the UV LED. With an assumption of the probability (p) of the user coming in

contact with each gas concentration being 1, the worst-case average UV LED power of the presented work lies within a range of $15\mu W$ - $31\mu W$. Therefore, the total LED power savings by the proposed SSD method is always >5x. Furthermore, this work also extends the sub-μW analog front-end design from Chapter 2, to realize a multi-functional gas AFE that can detect both oxidizing and reducing gases. A test chip is fabricated in 65-nm CMOS technology to validate the design. The presented analog front-end maintains the sub-μW operation achieved in Chapter 2, and consumes 57 nW of readout power while achieving a competitive dynamic range of 138 dB – 144 dB. The sensor biasing source consumes an additional power within a range of 28nW – $2\mu W$ across sensor resistance ranging from 20kΩ to 1MΩ. Therefore, the analog front-end design presented in this chapter extends the state-of-the-art multi-modal self-powered sensing nodes through achieving low-power integration of gas sensor's UV LED, and sub-μW analog front-end operation for ambient gas sensing. A list of contributions presented in this chapter are as follows:

1. Designed the switched-capacitor resistor (SCR) based adaptive biasing loop to enable sensor-agnostic operation of the analog front-end.

2. Designed an on-chip programmable clock divider and look-up-table to support the switched-capacitor resistor based adaptive biasing loop.

3. Implemented an intelligent alternative to traditional fixed UV LED duty cycling by designing a sensor saturation detector to predict the sensor's saturation point and subsequently make a decision on UV LED control.

4. Designed an on-chip UV LED driver for enabling the AFE's sensor saturation detector to control the UV LED.

5. Designed the digital-backend to assist the analog front-end in its operation.

CHAPTER 4

HYBRID DCOC FOR LOW POWER PPG SYSTEMS

4.1 Introduction

The last several years have seen wearable sensing platforms' growing significance and utility in our day-to-day lives. The modern-day wearable devices have enabled the users to monitor and record their vital physiological signals such as heart rate, blood oxygen saturation, blood pressure etc. These devices typically include multiple sensing modalities like electrocardiogram (ECG), photoplethysmogram (PPG), etc. Amongst these, PPG sensing has become more popular due to its ability to recover a large variety of physiological information related to both respiratory and cardiovascular systems [25]. PPG sensing is a non-invasive technique and requires an optical sensor for carrying out its operation. The PPG sensor comprises of a light emitting diode (LED) and a photodiode (PD). The LED acts as a light source which emits light, and injects it into the user's skin. The photodiode acts as an optical receiver, which senses the light reflected from the skin, and then converts into a current. The photodiode current (I_{PD}) consists of two parts namely, AC current component (I_{AC}), and DC current component (I_{DC}). The AC component registers itself due to the attenuation of LED light caused by the continuous flow of blood in our body. Whereas, the DC component within the photodiode current is present due to the more static/constant factors

like average/constant arterial blood flow, epidermal tissue, non-pulsatile veins etc. [26]. Thus, a PPG signal comprises of a pulsatile (AC) component superimposed on a DC component as shown in Fig. 4.1. Each of the peaks in the signal correspond to a pulse, and the time between two successive peaks gives the user's heart rate. Thus, while the DC component is useful for measuring parameters like blood oxygen saturation, respiration, etc., the user's heart rate can be obtained solely on the basis of AC current.

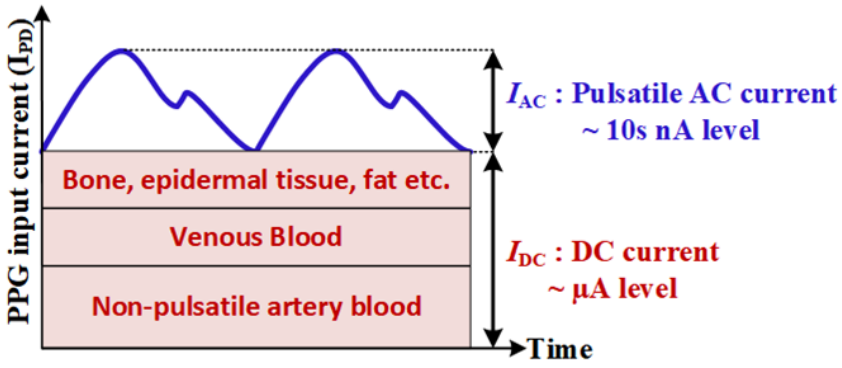

Figure 4.1: An illustration showing the AC and DC components of the PPG signal.

However, compared to other physiological sensing modalities, PPG sensing consumes higher power (tens to hundreds of μW) due to its use of LED, and AFEs operating at high supply voltages [27], [28], [29]. The readily available power from on-body energy harvesters such as TEG ($\sim 20\mu W/cm^2$) is both spurious and limited, drastically reducing the AFE power budget. Therefore, it is necessary to reduce both the analog front-end, and LED power to match the harvested power, and enable self-powered operation. While, the AFE and LED power can be reduced through voltage scaling and aggressive LED duty cycling, it affects the sensor node performance. This necessitates inclusion of design techniques that can support AFE operation at low supply voltages and shorter LED on times, while maintaining good performance.

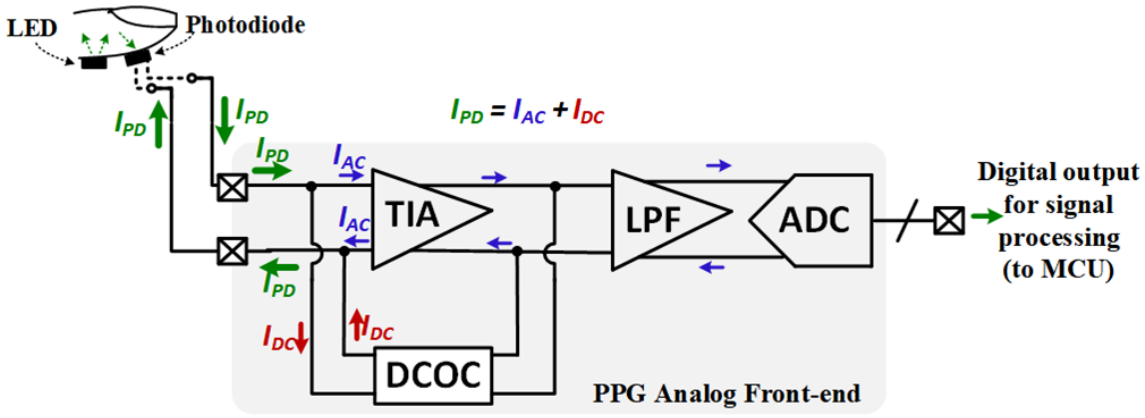

Figure 4.2: Architecture of conventional PPG sensing systems.

Fig. 4.2 shows the architecture of a conventional PPG analog front-end. Its signal chain majorly consists of a transimpedance amplifier (TIA) followed by a low pass filter (LPF), and an analog to digital convertor (ADC). An individual's heart rate (HR) is correlated to the time intervals of consecutive PPG AC signal peaks, and can be computed as the peak-to-peak interval (PPI) between two AC peaks (4.1). Thus, for the purposes of measuring heart rate, the PPG analog front-end needs to sense just the AC component of the photodiode current.

$$HR = \frac{60}{PPI} \tag{4.1}$$

As mentioned before the PPG signal has both AC and DC components, with an AC-to-DC ratio as low as 0.1% to 3% [26]. When compared with its AC counterpart, the PPG signal's DC component is significantly larger, ranging from several μA to tens of μA, thus forming almost 99% of the total photo-diode current. Due to DC components of this level, the PPG analog front-end needs to have a large dynamic range in order to avoid frequent saturation. However, since its already established that for heart rate measurement, the AC peaks are the only relevant signal, so this large DC current component can be canceled out prior to entering the signal chain. This will relax the dynamic range requirement of the analog front-end. Due to this reason, a conventional

PPG analog front-end also consists of a feedback DC current cancellation loop (DCOC loop) to cancel out the photodiode's DC component (Fig. 4.2). While the DCOC loop is important to maintain the PPG signal chain's functioning, it also affects the degree to which the system power can be reduced, especially for AFEs operating at low supply voltages. A detailed discussion of this issue is included later sections.

This chapter of the dissertation discusses design techniques that enable PPG AFE operation at low supply voltages and shorter LED on-times, while maintaining good dynamic range. Furthermore, in order to support this power-performance tradeoff, a hybrid architecture for the DCOC loop is introduced to mitigate the design challenges imposed by using a conventional DCOC architecture in similar low power systems

4.2 Design Challenges and Prior Art

A PPG system's total power consumption comprises two parts, average LED power (P_{LED}), and analog front-end power (P_{AFE}) (4.2). Here, the average LED power can be denoted as a function of LED's power supply (V_{LED}), current drawn by the LED (I_{LED}), and its duty cycle rate (D_{LED}). The LED's duty cycle rate is expressed as a product of LED on-time (t_{ON}), and sampling frequency (f_{LED}) (4.3). Similarly, the AFE power is expressed as a product of the AFE's power supply (V_{AFE}), and it's biasing current (I_{AFE}) (4.3). Thus, in order to reduce the total system power, both the LED and analog front-end power need to be optimized.

$$P_{PPG} = P_{AFE} + P_{LED} \tag{4.2}$$

$$P_{PPG} = V_{AFE}I_{AFE} + V_{LED}I_{LED}D_{LED} = V_{AFE}I_{AFE} + V_{LED}I_{LED}t_{ON}f_{LED} \tag{4.3}$$

First, we explore different design knobs to reduce the average LED power, and accompanying

design challenges. Typically, the LED power reduction is achieved by aggressive duty cyling techniques. By doing so, the LED is switched on for a short period of time (t_{ON}) at a sampling frequency of f_{LED} with an instantaneous LED current (I_{LED}). Equation (4.3) shows that with a fixed I_{LED} and f_{LED}, the LED power decreases with a shorter LED on-time (t_{ON}). However, when the signal chain is in operation, the LED needs to remain on throughout the time taken by the TIA to reach steady state (t_S), the DC current cancellation time (t_{DCOC}), and the analog-to-digital convertor's acquisition time (t_{ACQ}) (4.4). So, while reducing the LED on-time does reduce the average LED power, it also requires a faster analog front-end settling time (t_S) and DCOC compensation time (t_{DCOC}). A regulated-cascode TIA's two main poles are formed by its input (R_{IN}) and output (R_{OUT}) impedances. As both R_{IN} and R_{OUT} are a function of the TIA's biasing current, increasing the I_{AFE} would also reduce the time constants associated with R_{IN} and R_{OUT}. In other words, this improves the AFE's settling time, allowing a shorter LED on-time. While this helps in decreasing the LED power, it now requires a faster DCOC compensation time to support this shorter LED pulse. Another design knob available to the designer is the LED current (I_{LED}), which can be tuned to further reduce the average power consumption. However, this reduces both the AC and DC components of the PPG signal, requiring a high-gain TIA to retain the signal-to-noise performance. Therefore, while reducing the LED's on-time and instantaneous current can help in lowering the average power consumption, it also imposes a requirement for a high-gain TIA and a faster DCOC response time.

$$t_{ON} = t_S + t_{DCOC} + t_{ACQ} \tag{4.4}$$

Now let's consider the design challenges met while optimizing the analog front-end power consumption. As mentioned before, the LED power can be decreased by reducing the LED on-time and instantaneous current. However, in order to complement a shorter LED on-time, the TIA biasing current (I_{AFE}) is increased, resulting in higher AFE power consumption. This increase

AFE power soon starts to dominate the system power. One way to compensate for this is to design the analog front-end at a lower power supply (V_{AFE}) (4.3). However, this comes with its own set of design challenges which need to analyzed carefully. Also, to mitigate the poor SNR as a result of lower LED current, it is necessary to maintain a good front-end output swing. This requires a TIA with a considerably higher gain. In other words, in order to maintain a good tradeoff between the AFE power and performance, the PPG systems needs to feature a high-gain TIA designed at a low supply voltage. Due to the TIA's limited headroom at lower V_{AFE}, the front-end becomes more sensitive to input DC current residue. This leaves the TIA more prone to being frequently saturated or start exhibiting a non-linear operation. Thus, in order to mitigate these issues, the DC current cancellation loop needs to have a high resolution.

By considering the above analysis, it can be concluded that a good PPG system power-performance tradeoff can be achieved by designing a high-gain analog front-end at a low supply voltage while simultaneously reducing the LED on-time and current. However, to aid proper operation of such a system, a DC current cancellation loop with a high resolution and fast response time is needed.

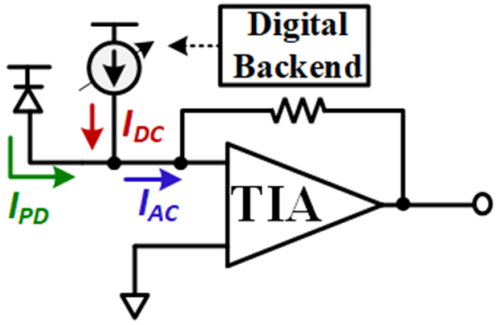

Figure 4.3: An illustration showing a generic digitally-assisted DC current cancellation loop.

Works prior to this dissertation have implemented DC current compensation using either a digital or an analog approach [30], [31], [32]. This section analyzes the impact on the resolution

and response time achieved by using these two DCOC approaches. First, we look at the digital DCOC method. Conventional digitally-assisted DCOC loops comprise linear or binary-weighted current-DACs (I-DACs), and accompanying digital backend [27], [29], [32]. These current-DACs are connected to the input of the TIA, and source a DC current close to the one present within the PPG input signal (Fig. 4.3). Some prior works source a pre-calibrated fixed I-DAC current, thus lacking the capability to compensate for any uncertain shift in the input DC current from the sensor [33]. Another frequently used approach includes blocks such as window comparators, ADC etc. to track the range of the photodiode's DC current, and subsequently tune I-DAC to match the DC current residue. Moreover, in order to reduce the DCOC response time, these methods increase the digital backend's clock frequency, translating to higher digital power. Also, the resolution achieved by the digitally-assisted DCOC loops is largely limited by the number of I-DAC branches. Typically, these loops consist of 5- to 10-bit I-DACs, limiting the DCOC compensation to an n-bit accuracy. This becomes a critical issue for low-power designs such as the one presented in this dissertation. This work's front-end is designed to operate at a supply voltage of 0.6 V, limiting the TIA's range of acceptable DC input current residue. In order to achieve high resolution while adopting a digitally-assisted DCOC, an I-DAC with a high-LSB resolution is required. This results in a large number of I-DAC branches, leading to a longer DCOC response time, and subsequently higher LED power. In addition to this, the I-DACs' branches also require good matching and very high precision comparators, which in turn increases the design complexity. Thus, the digitally-assisted DCOC loops provide a fast response time at a cost of resolution.

The fully-analog DC current cancellation loops are always in operation after the system startup, and provide a very high resolution [30], [31]. These loops typically comprise of an error amplifier connected in a negative feedback loop, such as the one shown in Fig. 4.4. The error amplifier senses the mismatch between the TIA's output and a fixed reference voltage (V_{REF}), and

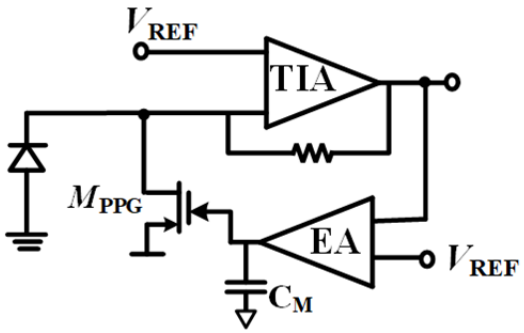

Figure 4.4: An illustration of a generic analog DC current cancellation loop.

subsequently adjusts the gate voltage of transistor (M_{PPG}) to source a current matching with the photodiode's DC current. Thus, with a high-gain error amplifier, the analog DCOC loop is able to perform DC current compensation with very high accuracy. However, in order to provide adequate phase margin across the required DCOC current range, a large compensation capacitor (C_M) is connected at the output of the error amplifier. In addition to this, the C_M is also used to set a high pass corner of $\sim$0.5 Hz. This is because the heart rate lies within the range of 30-300 bpm corresponding to a frequency range of 0.5 Hz to 5 Hz. Thus, due to the large time constant formed by C_M, the analog DCOC's response time is very large, leading to a significantly higher LED power. Therefore, an analog DCOC loop provides high resolution at a cost of slow response time. This makes the use of just an analog DCOC unsuitable for low power PPG systems.

This dissertation addresses this design gap by implementing a hybrid DCOC loop embedded within a sub-μW PPG analog front-end operating at 0.6 V. With this hybrid approach, the DCOC loop is able to achieve both, high resolution and fast response time

4.3 Design Approach

This work implements a sub-μW PPG analog front-end with readout power reduced by 37x compared to the state-of-the-art AFEs all while maintaining a dynamic range of 92 dB. The front-end is paired with a green LED to extract the user's heart rate. Overall, the average PPG system power comprising of both the analog front-end, and the LED is reduced by 4-50x when compared to the current state-of-the-art PPG systems. This improvement is brought by the following steps. First, the LED power is optimized by reducing the LED current to a range of 633 μA to 1.5 mA from 10 mA, and maintaining a short LED on-time. Also, in order to support a shorter LED on time, the AFE's biasing current is increased to an appropriate value. To avoid a large increase in AFE power, the front-end is designed at 0.6 V supply voltage. In order to maintain a front-end output swing of 200 mV, TIA's gain is carefully designed to lie between 2.4 MΩ to 5 MΩ. However, an LED current of 633 μA to 1.5 mA would result in an AC current of 35 nA to 85 nA. This coupled with a TIA gain of 2.4 MΩ to 5 MΩ, and a maximum output swing of 200 mV, imposes a requirement of a DC current cancellation loop with a minimum resolution of 5 nA (4.5). While an analog DCOC loop is able to meet this resolution, it cannot achieve a DCOC response time to support an LED pulse of $<$ 500 μs. To resolve this issue, this work features a hybrid DC current compensation circuit comprising of a fast digital DCOC loop for coarse compensation, and a background high-resolution analog DCOC loop. The hybrid DCOC loop enables low power operation by aiding the AFE to operate at 0.6 V, and helps achieve a competitive dynamic range.

$$R_{TIA} = \frac{V_{OUT}}{I_{IN}} \tag{4.5}$$

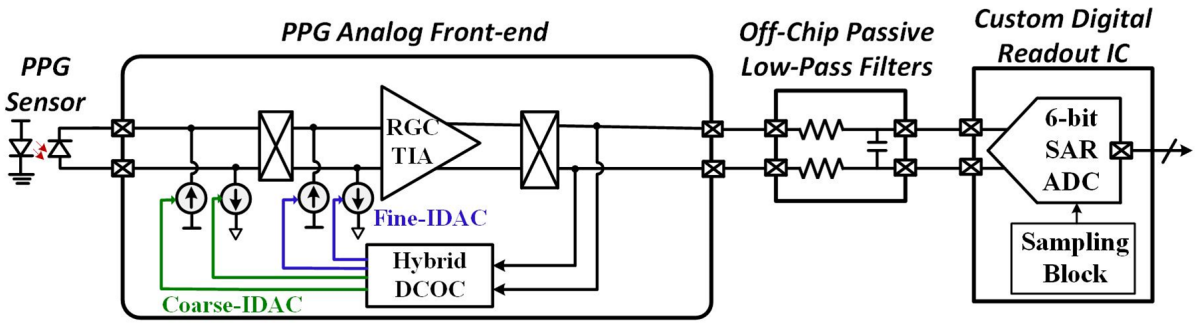

Figure 4.5: System diagram of the proposed sub-μW PPG sensing system.

Fig. 4.5 shows the system diagram of the proposed PPG system. It contains two custom ICs, the 532 nW PPG analog front-end IC, and the digital readout IC including a 6-bit custom SAR ADC and an LED sampling control block. The sub-μW PPG analog front-end IC consists of a chopper-stabilized regulated-cascode transimpedance amplifier (RGC-TIA) with a hybrid DC offset current compensation (DCOC) loop. An on-board passive low pass filter (LPF) is used to set low pass corner and reduce the chopping spikes.

4.3.1 Transimpedance Amplifier

Fig. 4.6 shows the transistor level schematic of the differential regulated-cascode TIA (RGC-TIA) along with its half circuit. As discussed before, the TIA included in this work operates at 0.6 V with a transimpedance gain of 2.4 MΩ - 5 MΩ. As mentioned before, the proposed LED current values set an input AC photodiode current of 35 nA to 85 nA. With these AC current values, and a minimum requirement of 25 dB SNR, a total input referred current noise of $< 1.97\ nA_{rms}$ is necessary to measure HR with an accuracy of ± 1 bpm [34]

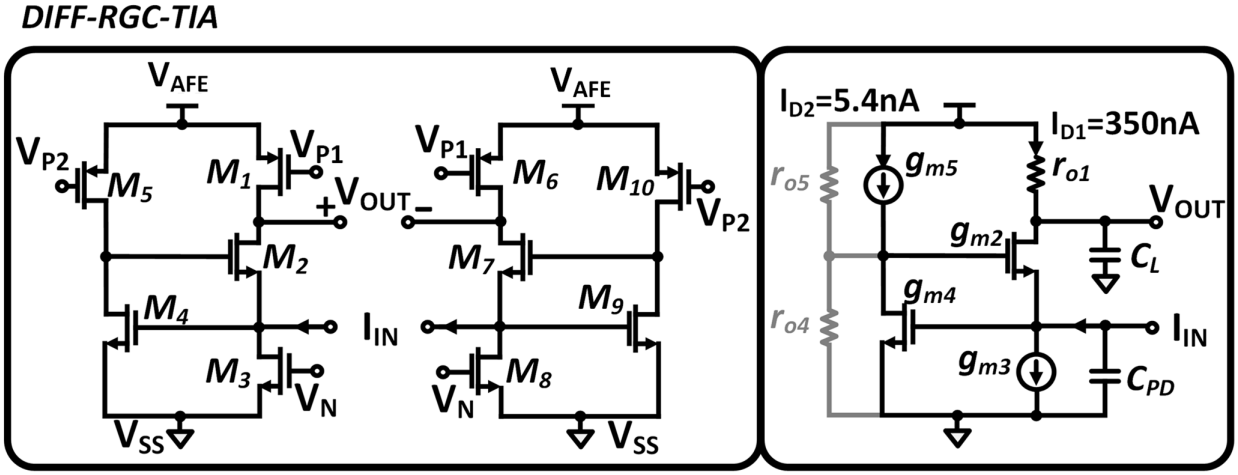

Figure 4.6: Schematic of the differential RGC-TIA (left) and the half circuit of the RGC-TIA (right).

The TIA's transimpedance gain (R_{TIA}) is given by the output impedance of transistor M_1 which is a function of M_1's drain current (I_{D1}) and the Early voltage (V_A) (4.6). As the Early voltage is neglected, R_{TIA} becomes inversely proportional to TIA's biasing current, I_{D1}. Therefore, lowering I_{D1} helps in increasing the TIA's gain

$$R_{TIA} = \frac{V_A}{I_{D1}} \tag{4.6}$$

We now evaluate the TIA's poles to help analyze the effects of I_{D1} on the TIA's settling time (t_S). An RGC-TIA typically has two poles p_1 and p_2 with time constants τ_1 and τ_2 respectively (4.7)-(4.8). Here, pole p_1's time constant (τ_1) is a function of TIA's input impedance (R_{IN}) and the parasitic capacitance of the photo diode (C_{PD}) (4.7). Whereas, pole p_2's time constant (τ_2) is a product of M_1's output impedance (r_{o1}) and TIA's load capacitance (C_L) (4.8). Owing to the sub-threshold operation, r_{o1} is significantly larger than R_{IN}, making p_2 the dominant pole. Thus, the TIA's bandwidth and settling time depend on the time constant τ_2. In other words, as r_{o1} is inversely proportional to I_{D1}, the TIA's settling time decreases with increase in the biasing current

(4.8). Also, the photodiode's parasitic capacitance (C_{PD}), and M_3's output impedance (r_{o3}) form a time constant contributing towards a left plane zero (4.9).

$$\tau_1 = R_{IN}C_{PD} \tag{4.7}$$

$$\tau_2 = r_{o1}C_L = \frac{V_A C_L}{I_{D1}} \tag{4.8}$$

$$\tau_2 = r_{o3}C_{PD} \tag{4.9}$$

For a TIA to be a good current-to-voltage amplifier, it should exhibit a small input impedance. Unlike the conventional common-gate TIA, the RGC-TIA consists of a common-source amplifier connected in feedback with the common-gate stage of the TIA. Here, the transistors M_4 and M_5 form the common-gate stage, reducing the input impedance by a factor of (1+A) when compared to a standalone common-gate stage (4.10). It is worth noting that the drain current of the cascode stage (I_{D2}) does not affect A in our case, since its effects on the transconductance of M_4 (g_{m4}) and the output impedance of M_4 (r_{o4}), M_5 (r_{o5}) cancel each other out due to subthreshold operation. Thus, I_{D2} is set to a value of 5.4 nA for a lower TIA power consumption

$$R_{IN} = \frac{1}{g_{m2}A} = \frac{1}{g_{m2}(1 + g_{m4}(r_{o4}||r_{o5}))} \tag{4.10}$$

While adding the common-source stage in feedback does increase the total input-referred noise, smaller I_{D2} value minimizes the thermal noise contributions of M_4 and M_5. The RGC-TIA's two major noise sources are the 1/f noise present at lower frequencies, and the photodiode's large parasitic capacitance at high frequency. So, this work implements chopping technique at 1kHz, in the frequency range where the thermal noise dominates

4.3.2 Hybrid DCOC Loop

Fig. 4.7 shows the proposed hybrid DCOC loop and its timing diagram. The loop is divided into a digital and an analog DCOC loop. The digital DCOC loop controls the coarse-IDACs to cancel out majority of the input DC current residue, while the analog DCOC loop regulates the fine-IDACs providing high-resolution DC current cancellation. As shown in the timing diagram, the digitally assisted coarse-loop is enabled each time a new LED pulse comes in, while the slower analog fine-loop continuously runs in background improving the DCOC's overall resolution, and also canceling out any uncertain DC residue due to environmental factors.

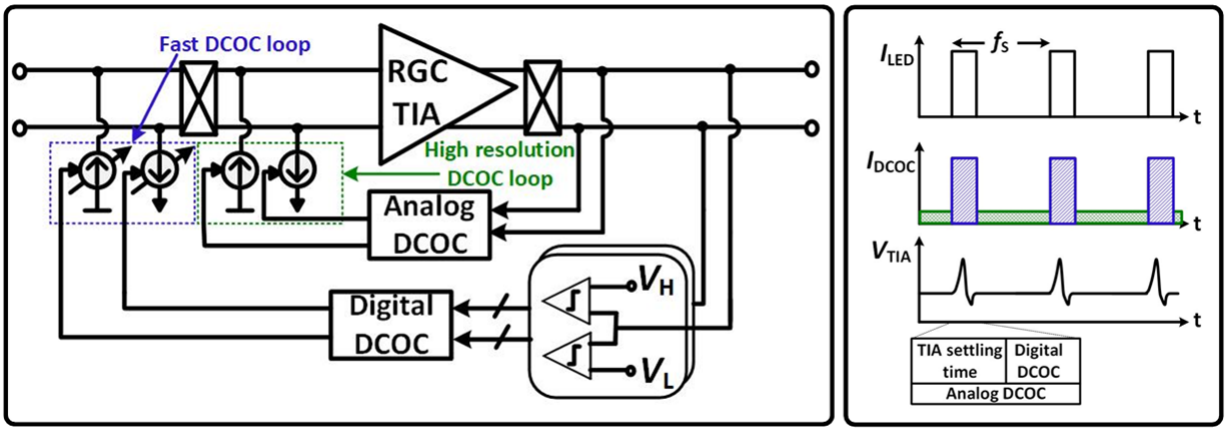

Figure 4.7: Schematic of the proposed hybrid DC current cancellation loop (left) and its timing diagram (right).

4.3.2.1 Analog Fine-DCOC Loop. As shown in Fig. 4.8, the analog DCOC loop comprises of two groups of fine-tuned current sources and sinks, directly connected at the positive and negative inputs of the RGC-TIA. These groups are implemented using two sets of PMOS and NMOS transistors acting as voltage-controlled current sources/sinks. Here, M_1 and M_3 form the first group, while M_2 and M_4 form the second group. Since, the analog DCOC loop is always on and running in the background, the current from these transistors needs to be in phase with the

TIA chopping clock. Therefore, one of the transistor groups is switched on at each of the non-overlapped chopping clock phases (ϕ1,ϕ2). Since the fine-tuned current source/sink is connected to the TIA's high-frequency input node, 1/f noise caused by M_1–M_4 is also removed from the signal bandwidth. M_1–M_4 all have 2 μm/2 μm W/L ratio, which can support up to 50-nA current residue. The analog DCOC loop also works as the common-mode feedback loop to regulate the TIA's common-mode output voltage to half of V_{AFE}.

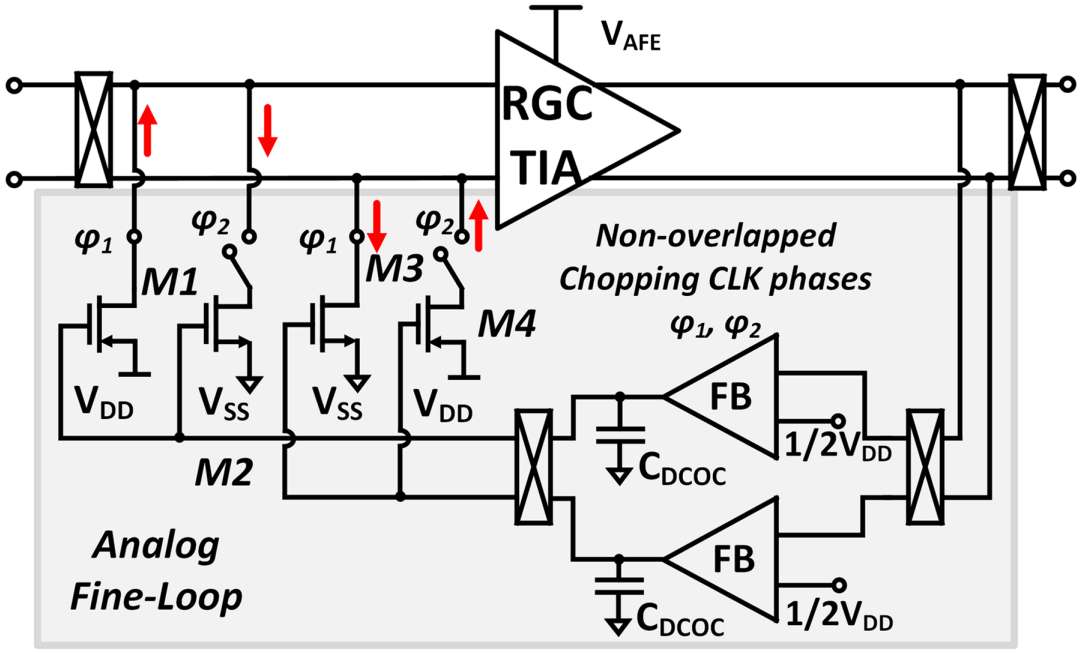

Figure 4.8: Schematic of the proposed analog DCOC loop.

Two operational amplifiers (FB) tune M_1–M_4's gate voltages and their drain current such that the TIA's output voltages are regulated as half of the supply voltage (300 mV). These amplifiers have a structure similar to the one shown in Fig. 2.8. Two off-chip capacitors (C_{DCOC}) are added at the amplifier's output nodes to reduce their bandwidth so that the analog DCOC loop sets a 0.55-Hz high-pass corner frequency for the analog front-end. The feedback amplifiers used in the analog DCOC loop each consume 5-nA of additional current. This unavoidably adds *1/f* noise

since they work in the low-frequency domain. One way to mitigate this effect is to increase the value of C_{DCOC}. Therefore, in order to set a 0.55Hz of high-pass corner and simulatneously improve the noise performance, two 100-nF off-chip capacitors were chosen as C_{DCOC} used in the design. However, choosing a large C_{DCOC} value also degrades the analog fine-DCOC loop's response time. Overall, the analog DCOC loop increases the noise density floor from 499 fA/Hz to 1.39 pA/Hz in the simulation. However, as discussed before, for sub-μW PPG analog front-ends operating at low supply voltages such as the one in this dissertation, the DCOC loop needs have both a faster response time and high-resolution. Thus, employing just an analog DCOC loop similar to the one in this section would provide high-resolution DC current cancellation but results in a long response time. So, while the analog DCOC loop here compensates for up to 50 nA of current residue, a digital loop is used for canceling out the majority of the remaining current residue

4.3.2.2 Digitally-assisted Coarse-DCOC Loop . The digitally assisted coarse-loop is synchronized and enabled each time the LED is turned on. Once on, it detects whether the TIA's outputs have an offset due to the photodiode's large DC current, subsequently cancelling it out. As shown in Fig. 4.9, the digital DCOC loop is implemented using a pair of window comparators connected to the low frequency outputs of the TIA, and a pair of PMOS- and NMOS-based 10-bit current source/sink DACs (I-DACs) controlled by digital back-end. The two I-DACs are connected at the TIA's low frequency inputs, directly cancelling out the majority of photodiode DC current.

Since the analog loop supports current residue up to 50 nA, the digital coarse-loop would require an I-DAC with at least 50-nA resolution, to match each of the LED current values. The I-DACs are thus designed to have an LSB of 50 nA, and can source/sink up to 1.8 μA of current. If a linear current-DAC is used, then a large number of I-DAC branches is required. Thus, the digital

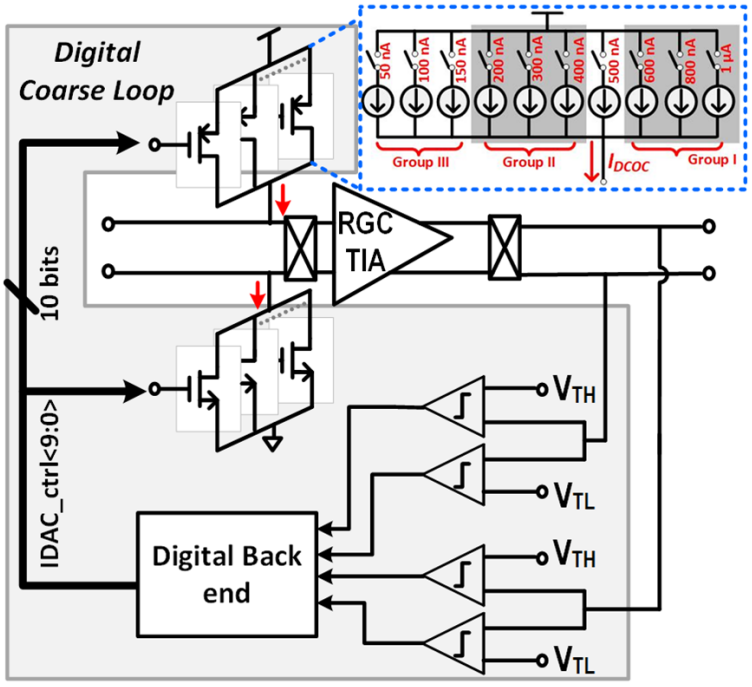

Figure 4.9: Schematic of the proposed digital coarse-DCOC loop.

back-end would have to search through a larger number of I-DAC branches to find the one required for compensation. As a result, the DCOC response time is increased, also leading to an increase in average LED current. Also, owing to the large number of I-DAC branches, the total leakage power is also high. To mitigate this, the digital DCOC loop implements a segmented I-DAC. This reduces the transistor count and hence the leakage power of the current sink/source DACs, and also achieves a shorter response time.

The two 10-bit source/sink I-DACs are implemented with ten branches segmented into three groups with 50 nA (group III), 100 nA (group II), and 200 nA (group I) step sizes (Fig. 4.9). Each of the branches consists of PMOS (source) or NMOS (sink) transistors carefully sized to support the required current values. Also, every branch has switches added as headers (source) and footers (sink) to enable digital control. The window comparators detect if TIA outputs are

within the acceptable voltage range (upper and lower threshold voltages, V_{TH} and V_{TL}). The comparator outputs thus indicate whether the TIA is in an over-saturated or under-saturated state. The digital backend tracks the comparator outputs, and traverses through the I-DAC branches till the TIA reaches an unsaturated state. Also, the chopping clock stays off while the digital DCOC is conducting the search, turning on only after the search ends. The digital backend always starts the search from a fixed I-DAC branch (note that here it is fixed at 500 nA). Depending on if the TIA is under-saturated or over-saturated, the I-DAC branches in group I or group II are turned on respectively. The *IDAC_CTRL<9:0>* is toggled such that every branch is turned on sequentially. If the TIA's outputs are pulled back within the acceptable range, the I-DAC connections are retained. However, if the matching current value is found to be missing in the group (note that this happens when the comparator outputs indicate that the TIA shifts from an over-saturated to under-saturated state, or vice-versa), the existing I-DAC connection is retained while the search moves to group III. The I-DAC branches are then sequentially turned on in group III, essentially adding current to the already connected branch from group II or group I. This continues till the correct match is found.

Fig. 4.10 shows the detailed timing diagram of the hybrid DCOC loop as an example. There are three internal signals: 1) $COMP_{PH/PL/NH/NL}$ are the comparator outputs implying whether the TIA is under-saturated or over-saturated; 2) the *EN_CHOPPER* signal turns the chopping switches on/off; and 3) the *IDAC_CTL<9:0>* signal is a 10-bit signal connected to the I-DACs, and toggles them directly. The digital back-end continuously samples the comparators' outputs. Once the window comparators detect the TIA in an over-saturated/under-saturated state, the signal *EN_CHOPPER* is set to low, and the digital back-end toggles *IDAC_CTRL<9:0>*. The I-DAC is allowed to settle after each change in *IDAC_CTRL<9:0>*, and is followed by the sampling of the comparators' outputs. All four comparators' outputs settle at logic high to indicate completion of DCOC. After this, the *EN_CHOPPER* is raised to turn on chopping. All this while, the analog

DCOC loop is working the background.

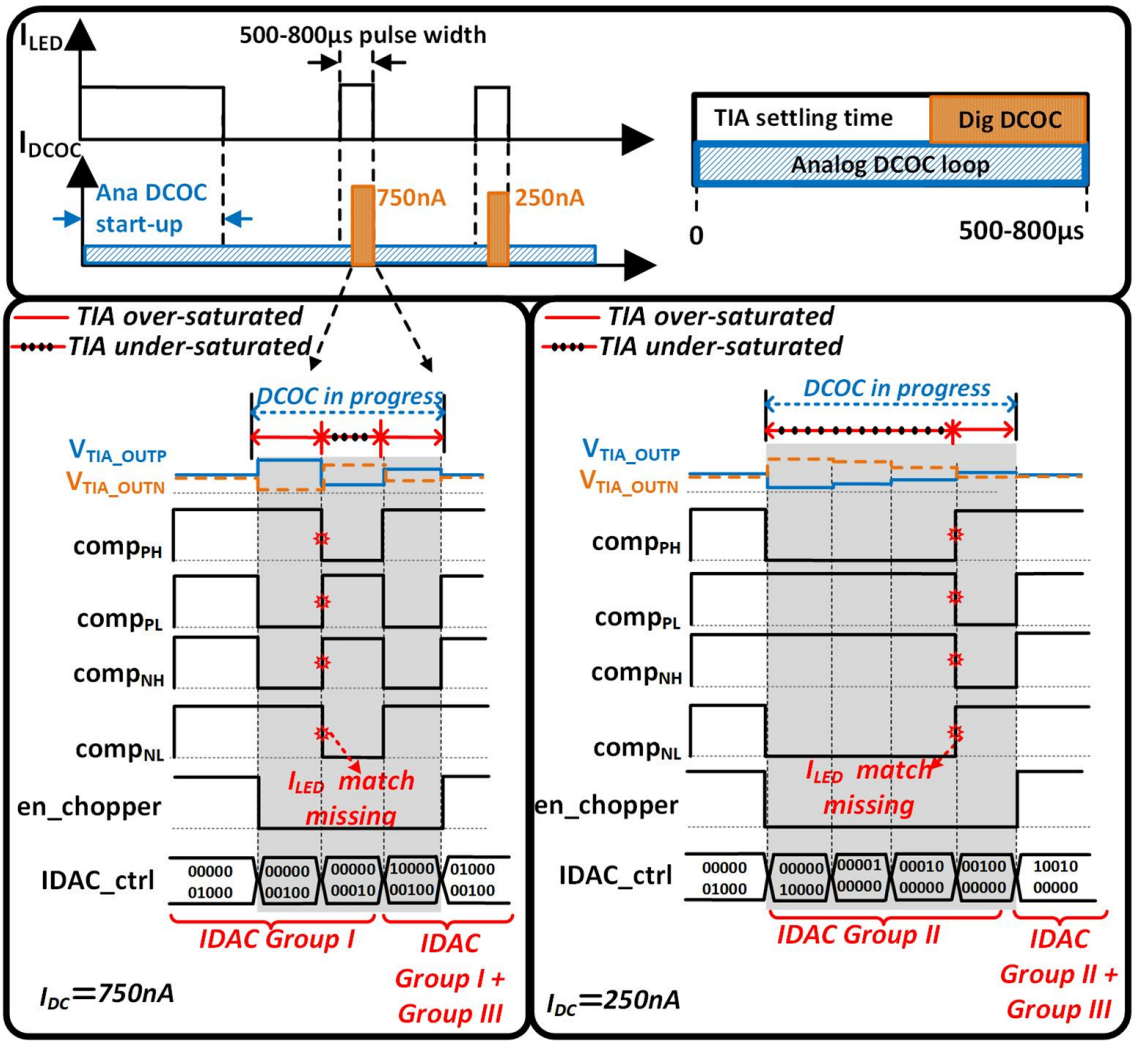

Figure 4.10: Timing diagram of the proposed hybrid DCOC loop operating for two example use cases (I_{DC}=750nA and I_{DC}=250nA).

Therefore, by adopting this hybrid DCOC architecture, a resolution of $<$ 5nA can be achieved while delivering a fast response time. This enables the RGC-TIA to retain a high-gain while operating at 0.6 V, pushing the PPG AFE power to sub-μW region.

4.4 Measurement Results

The sub-μW PPG analog front-end was taped-out as a part of a multi-modal analog front-end IC. The IC was fabricated in 65-nm bulk CMOS process with a total die area of $5mm^2$. The proposed PPG analog front-end occupies an active area of $0.47mm^2$. The die micro-photograph is shown in Fig. 4.11

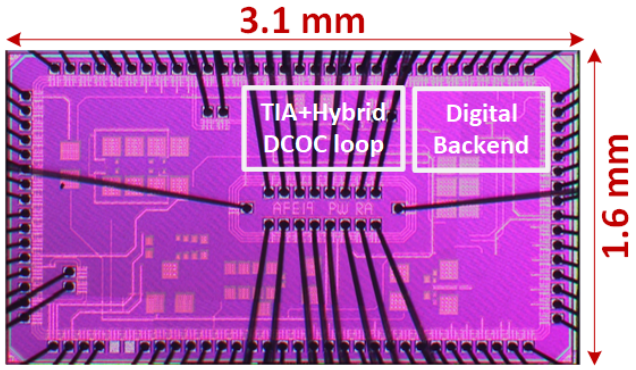

Figure 4.11: Die microphotograph of the multi-modal analog front-end.

The PPG analog front-end's transfer function is measured at the RGC-TIA's output while sweeping the frequency of the input signal. The measured transfer function shows that the PPG analog front-end has a transimpedance gain of 4 MΩ with a signal bandwidth from 0.55 Hz to 100 kHz (Fig. 4.12).

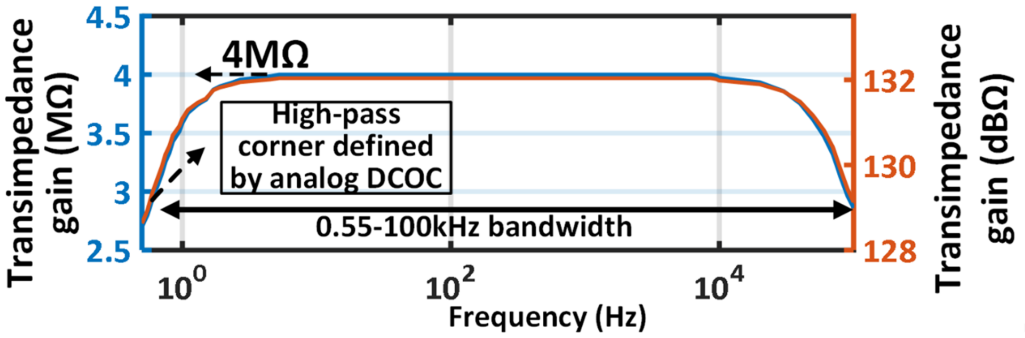

Figure 4.12: Measured transfer function of the proposed PPG analog front-end.

The bandwidth required for processing PPG signals varies for different use cases, such as clinical standard, ambulatory care, and personal wearables. Since, this dissertation targets an application of ultra-low power wearable heart rate monitoring, taking only low frequency signal components is acceptable. Previous work has stated that the PPG signal bandwidth is 0.5–5 Hz [34]. Taking this into account, this work uses a 5 Hz bandwidth for noise measurement. The total input-referred noise is measured with a Keysight 35670A dynamic signal analyzer. Fig. 4.13 shows that the PPG analog front-end in this work has a measured total input-referred noise of 45 pA_{rms} across a signal bandwidth of 0.55–5 Hz. The hybrid DCOC enables the front-end to operate without saturation at a supply voltage of 0.6 V and a gain of 4 MΩ. Since it supports a maximum input current of 1.8 μA, the front-end's dynamic range now stands at 92 dB.

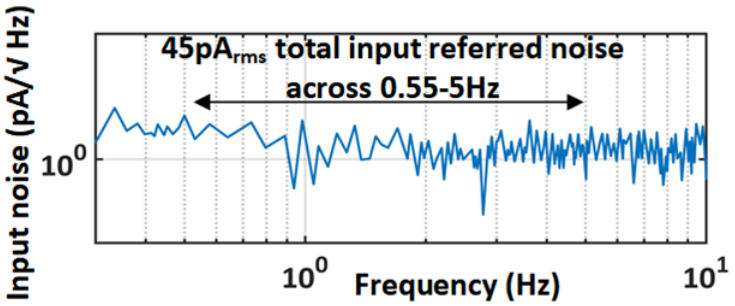

Figure 4.13: Measured input noise density of the proposed PPG analog front-end.

The analog front-end's functional verification is performed by measuring a human subject's PPG signal at the fingertip with an off-the shelf PPG sensor [35]. The sensor's green LED is pulsed at sampling frequency of 20-Hz for taking heart rate measurements. The proposed PPG AFE's signal is measured concurrently with a three-lead concurrent ECG signal. A heart rate and pulse transit time are calculated as 64 bpm and 0.64 s, respectively Fig. 4.14. The measured PPG signal shown in Fig. 4.14 is post-processed by off-chip low-pass filter.

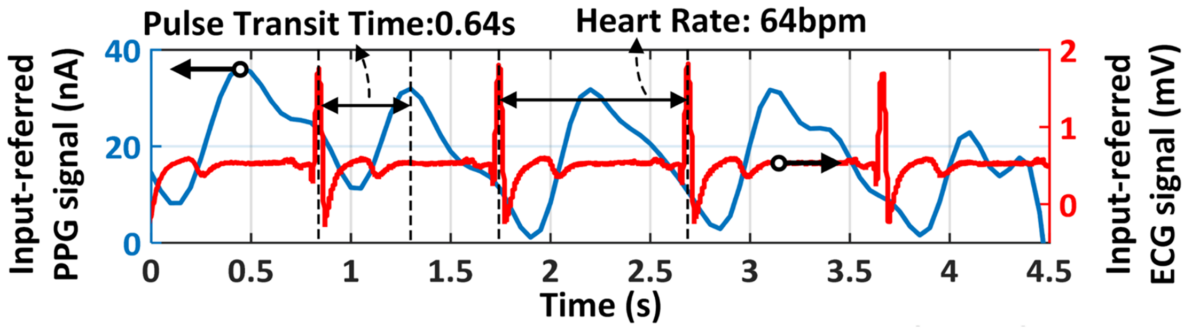

Figure 4.14: Measured transient output of the proposed PPG analog front-end.

Table V summarizes the power and performance of the proposed PPG analog front-end IC and compares it with the current state-of-the-art sensor interfaces and systems. This work's RGC-TIA and hybrid DCOC loop improve the readout power by 37x, compared to state-of-the-art PPG analog front-ends. Including the LED, the total power stands at 9.032 μW which is 4-50x lower than the other state-of-the-art PPG systems.

TABLE V

PERFORMANCE SUMMARY AND STATE-OF-THE-ART COMPARISON

	[49] This Work	[27] ISSCC'19	[28] TbioCAS'18	[29] VLSI'19	[33] ISSCC'18
Technology	65 nm	55 nm	180 nm	180 nm	180 nm
Supply Voltage (V_{AFE})	0.6V	1.2 V	1.2 V	1.2 V	3.3 V
Area	5mm^2 in total; 0.47mm^2 PPG AFE	N/R	1.1 mm^2/CH	N/R	N/R
Input noise	45 pA (0.55-5Hz)	28 pA (20Hz)	82 pA (4Hz)	224 pA (20 Hz)	N/R
Dynamic range	92 dB	111 dB	110 dB	95-119 dB	N/R
Readout power	532 nW	54 µW	20 µW	61-89 µW	29.1 µW
LED power	8.5 µW	205 µW	N/R	26-107 µW	9-480 µW
Readout and LED power	9.032 µW	259 µW	N/R	87-196 µW	38.1-509.1 µW

4.5 Conclusion

This section presents a sub-μW PPG analog front-end, which, when integrated with a PPG sensor achieves a total system power which is 4-50x lower compared to other state-of-the-art PPG systems. Various design choices such as shortening the LED on-time, and lowering the LED current are made to reduce the LED power. In order to maintain good power-performance tradeoff, the analog front-end implements a high-gain TIA designed at a low supply voltage of 0.6 V. However, due to these design decisions, the analog front-end requires a DC current cancellation loop with both high-resolution and fast response time. This is necessary in order to support the shorter LED on-time, and prevent the RGC-TIA from frequently saturating. Prior PPG AFEs implement a digitally-assisted or a fully-analog DC current cancellation loop. However, these DCOC architectures can either provide high-resolution or fast response time. A list of contributions presented in

this chapter are as follows:

1. Evaluated the design constraints imposed on DC current cancellation loops in low power PPG systems.
2. Explored the design tradeoffs of traditional DC current cancellation loop architectures.
3. Contributed to implementation of a hybrid DC current cancellation loop to provide both fast response time and high resolution. Implemented the digitally-assisted coarse DCOC loop to cancel out majority of DC current residue and improve the hybrid DCOC's overall response time.
4. Designed the digital backend to assist the AFE's operation.

CHAPTER 5

EVENT-DRIVEN MULTI-MODAL AFE FOR RESPIRATORY DISEASES

5.1 Introduction

Due to increasing popularity of both self-management and tele-monitoring of one's physical well-being, wearable healthcare devices have gained traction in the recent years. Additionally, with deteriorating air quality, monitoring of one's local micro-environmental parameters such as ozone, and their effects on the user's physiological vital signs has become necessary. However, this requires integrating multiple sensing modalities in a single on-body sensing platform. As mentioned before, breathing in high levels of ozone has both immediate and long term cardiovascular and respiratory effects. Some of these effects include rapid breathing which leads to drop in blood oxygen saturation levels, airway inflammation causing asthma flare-ups, and increased risk of cardiovascular diseases such as hypertension, stroke, heart failure etc. [7], [8]. Therefore, in order to provide a well-rounded report on the user's health, it is imperative for the wearable sensing platforms to monitor key vital signs including respiration rate (RR), blood oxygenation (SpO_2), heart rate (HR), blood pressure, and ambient ozone concentration. This also helps in providing long term management, and guaranteeing safe environment for patients of chronic diseases like chronic obstructive pulmonary disease (CPOD), congestive heart failure etc.

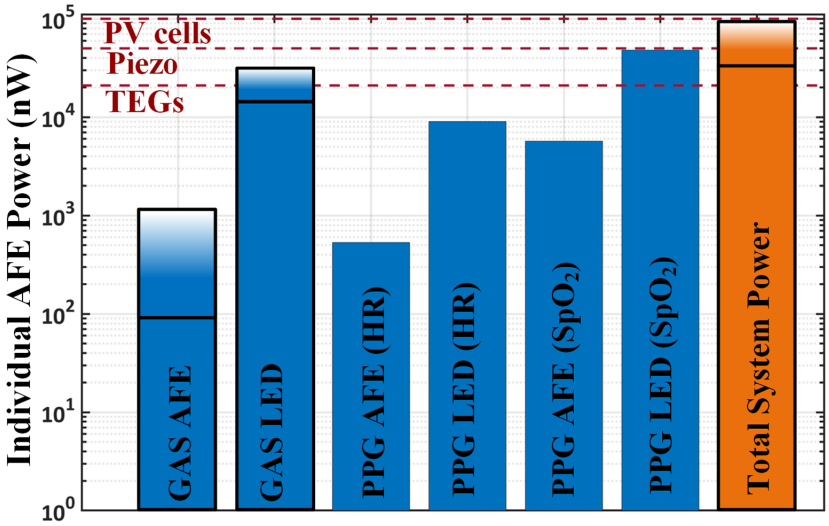

Figure 5.1: Individual readout power ranges presented so far in this dissertation, and the mismatch between the harvested power densities and resulting system power.

Most of the custom ICs have been largely focused on low-power design of cardiovascular sensing modalities including ECG and PPG [34]. However, these do not provide a multi-modal solution for monitoring key vital signs for both pulmonary and cardiovascular health. Recent works have started to integrate ECG and PPG with respiration rate monitoring [27], [36]. However, their respiration rate readouts and data processing consume power ranging from 96.96 μW – 530 μW. This type of power level attributed to a single readout would exceed a self-powered sensing node's budget. Also, these works do not integrate any type of ambient gas sensing within them. Therefore, there is a design gap for sensing nodes that provide an integrated solution for modalities including respiration rate, blood oxygenation, ozone, heart rate, ECG etc. The only prior work combining the above-mentioned modalities is designed using off-the shelf components and consumes $\sim$ 630 μW of power in just its sensors and their readouts [10]. However, this would still overtax body-worn energy harvesters like TEG. This dissertation has enabled sub-μW operation for both ozone and PPG sensing while restricting their respective system powers below 31 μW. However, on

integrating these modalities, the total resulting power would still exceed the on-body harvesters power budget Fig. 5.1.

To address these issues, this chapter of the dissertation provides two solutions. First, it introduces a context-aware event-driven system architecture to enable integration of multi-modal sensing within a self-powered system, while still maintaining information completeness. Second, it presents a sub-μW respiration rate analog front-end that can operate as an always-on channel alongside an ECG readout to enable ubiquitous monitoring of the two most critical vital signs pertaining to the user's cardiovascular and pulmonary health.

5.2 Design Challenges

A sensor node's lifetime comprises of the available energy from the harvester (E_{avail}), and the sensor node's average power consumption (P_{node}) (5.1). Therefore, the sensor node lifetime can be increased by either increasing the harvested power or by decreasing the system power consumption. However, as most of these on-body energy harvesters do not have high power densities, a larger harvesting transducer is required to increase the total harvested power. But as small form factor is desired for wearable devices, so the energy harvesting transducers sizes must be minimized. While the previous chapters in this dissertation optimize the power-performance tradeoff for the individual front-ends, this section looks into system architectures to improve the sensor node's lifetime.

$$Lifetime \propto \frac{E_{avail}}{P_{node}} \tag{5.1}$$

Typically, the sensor nodes are operated in one of the following two ways. First, applications

which require comprehensive monitoring of the highest levels and negligible data loss, need the sensor nodes to remain active throughout their lifetime. In such scenarios all of the analog front-ends in the node are always-on (Fig. 5.2). The biggest advantage of having the sensor node operate in an always-on state is that it would detect all the critical events, and subsequently alert the user. However, the downside of this approach is its high-power consumption, often rendering it unsuitable for self-powered operation. Additionally, as every analog front-end in such a system is always active, it generates a large amount of data, adding to both computation and transmission power overheads. Therefore, while this approach does provide comprehensive monitoring, it is not suitable for sensor nodes with limited power and resource allocation.

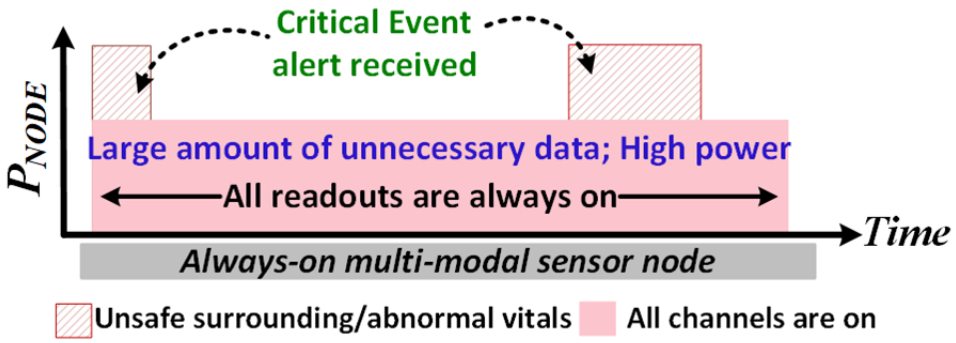

Figure 5.2: An illustration of traditional always-on sensing node operation.

Second, in order to lower the system power for multi-modal sensor nodes, prior works use a heavy system duty-cycling approach [10]. As shown in Fig. 5.3, the sensor node is periodically switched between active and sleep state, at a fixed repetition frequency. Therefore, by shortening the length of its active state (T_{active}), the sensor node's average power consumption can be significantly reduced (5.2). While this increases the sensor node's lifetime, it also results in complete data outage during the long sleep periods. As a result, the sensor node fails to notify the user regarding

any critical events that occur during sleep state.

$$Lifetime \propto \frac{E_{avail}}{P_{node}(T_{active}/T_{cycle})} \tag{5.2}$$

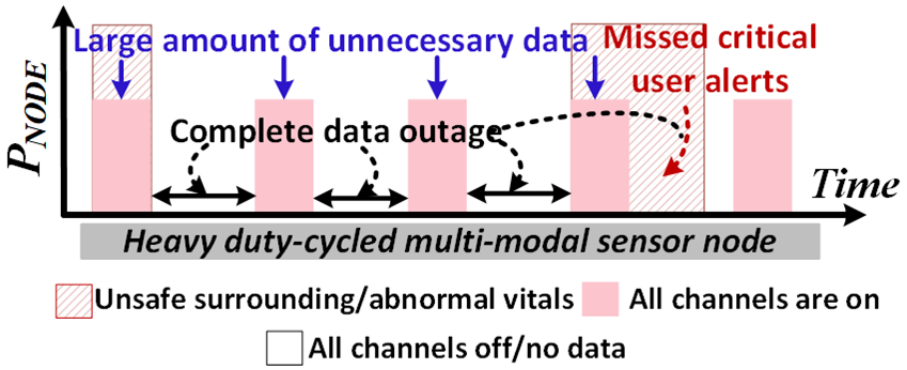

Figure 5.3: An illustration showing heavily duty-cycled multi-modal sensor node.

Furthermore, as the sensing requirements are dynamic and change with the user's environment and activities, it also affects the group of vital signs that are most relevant to the user at any given time of the day. Since, during active states, both of the above-mentioned approaches provide data from all of the analog front-ends, it reduces the overall quality of information retrieved by the sensor node. Therefore, as a body sensor node is constrained in terms of both the available power budget and computational capabilities, the above-mentioned methods are not the most efficient system architectures.

To address these issues, this section of the dissertation presents a context-aware event-driven system architecture to realize an integrated solution for heart-rate (ECG), respiration rate, blood oxygen saturation, and ozone sensing, providing comprehensive physiological and environmental co-monitoring capabilities.

Furthermore, respiration rate is the main vital sign for monitoring pulmonary health, and helps in early detection of various diseases [37]. Therefore, to provide a well-rounded report on

the user's health, it is imperative to include respiration rate sensing in wearable healthcare devices. Existing works extract the user's respiration rate from their ECG, PPG, or bio-impedance (Bio-Z) signals. However, this incurs both high readout and computational power, ranging between tens of micro-watts to hundreds of micro-watts [27], [28], [36], [38]. As an alternative, some works have explored inductive-/capacitive-based wearable respiration rate sensing, however their analog front-ends are based on off-the-shelf components, and consume several milli-watts of power [39], [40].

Therefore, in order to match the power available from an on-body harvester such as TEG, this section of the dissertation also presents a sub-μW respiration rate analog front-end designed to work with a capacitive breathing sensor. In order to reduce the computational power overhead, the analog front-end is embedded with low-power, on-node signal processing.

5.3 Design Approach

Fig. 5.4 shows the conceptual diagram of the presented event-driven system architecture for a multi-modal analog front-end. This is a context-aware closed-loop architecture that limits the always-on operation to readouts targeting the preferred primary signs. The remaining channels are turned off unless the data suggests a need for more comprehensive monitoring. Also, the always-on channels, referred as canary channels, are designed to operate in sub-μW region, significantly improving the always-on power. By opting for the proposed event-driven system architecture, the sensor node gains the following advantages. First, it reduces the amount of unnecessary data generated at any given point, which in turn reduces the computational and transmission power overhead, and also provides quality of information. Second, it eliminates the possibility of complete data outage by monitoring at least the critical primary signs at all times during the sensor node's operation. This also mitigates the issue of missing critical events during the sleep state. Lastly, the canary

channels' sub-μW operation significantly lower the average system power, enabling always-on self-powered operation.

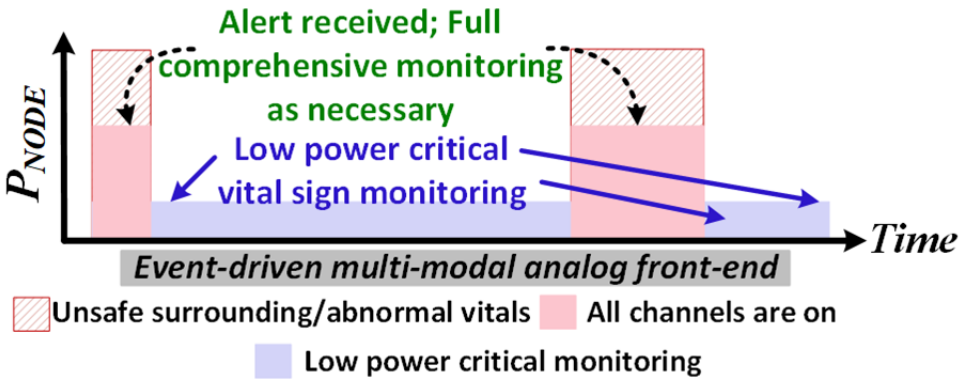

Figure 5.4: An illustration of the proposed context-aware event-driven system operation.

In order to implement the proposed event-driven system architecture, we first determine the preferred primary signals and canary channels for the given use case. Since this work is targeted towards providing physiological and environmental co-monitoring for users with or at risk of developing respiratory diseases, we choose heart rate and respiration rate as the preferred primary vital signs. Also, to promote early detection of critical events such as exposure to harmful air pollutants, asthma triggers etc., respiration rate front-end is chosen as the canary channel. The remaining PPG and ozone front-ends are categorized as secondary channels. These high-power channels remain off unless an abnormal respiration rate is detected, thereby reducing the overall system power.

5.3.1 System Architecture

Fig. 5.5 shows the event-driven multi-modal analog front-end demonstrating the example use case. It comprises of a voltage-mode ECG channel, a capacitive-mode respiration rate channel, a

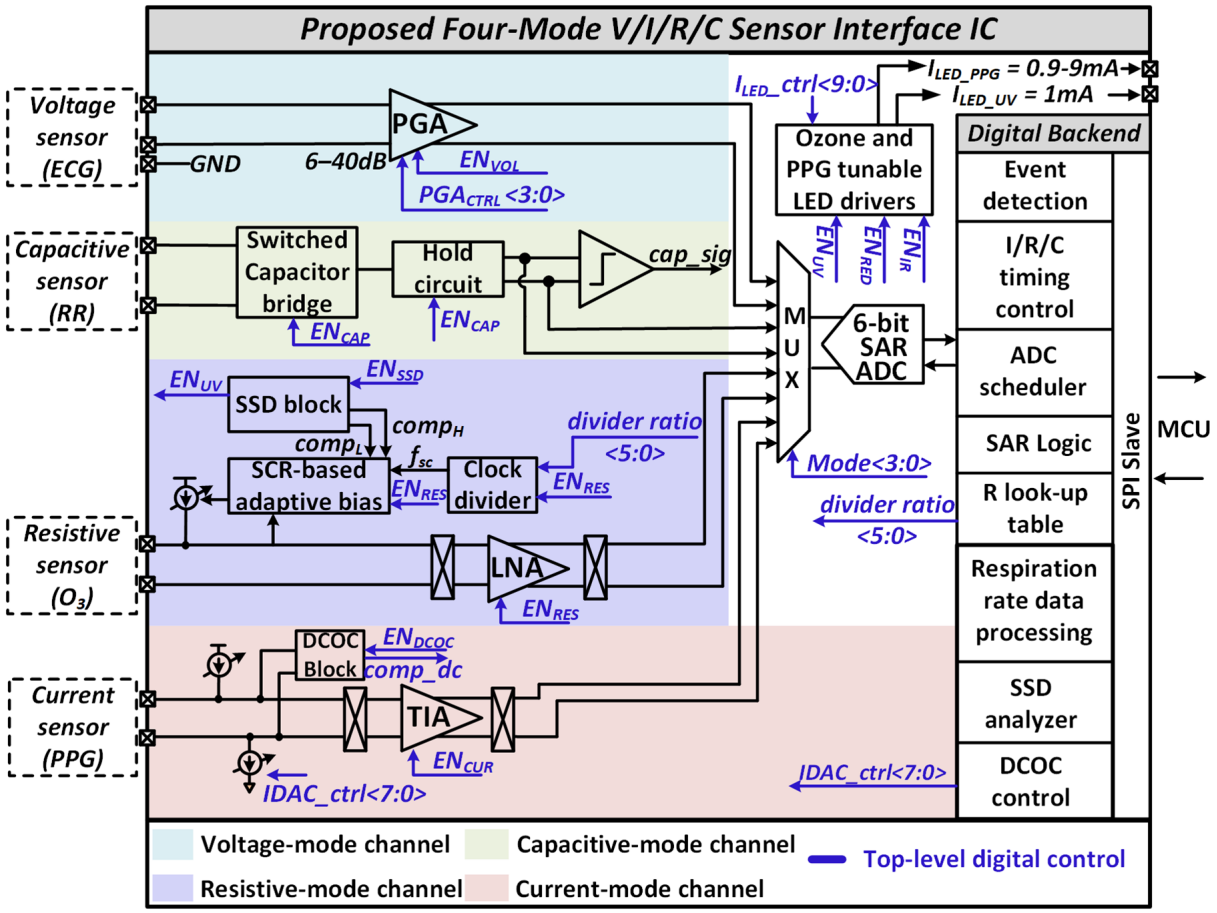

Figure 5.5: Proposed event-driven analog front-end for ECG, PPG (heart rate and SpO_2), respiration rate, and gas (ozone) sensing.

current-mode PPG channel, and a resistive-mode ozone channel, a shared digital backend, an analog multiplexer, a 6-bit SAR ADC, and on-chip LED drivers. The digital backend time-multiplexes the channels' outputs by controlling analog multiplexer's select signal, Mode$< 3 : 0 >$, and provides timing control for V/I/R/C channels. The ECG channel comprises of a programmable gain amplifier (PGA), and the respiration rate channel comprises of the front-end, and embedded data processing for low-power on-node computation. The ozone channel is similar to the one from Chapter 3, and includes a switched-capacitor resistor (SCR)-based adaptive bias for resistance-to-

voltage conversion, a chopper-stabilized amplifier (AMP), a clock divider, and associated look-up-table (LUT). It also features a sensor saturation detector (SSD) and analyzer for adaptive UV LED duty cycling. The PPG channel features a chopper-stabilized transimpedance amplifier (TIA), a DC offset compensation block (DCOC), 8-bit current DACs (IDACs), and the associated DCOC control digital logic. Three on-chip LED drivers are implemented for supporting UV (ozone channel), and red and infrared (PPG channel) LEDs. The analog blocks and digital backend operate at a power supply of 0.6 V, while the LED drivers work at 3.3 V.

5.3.2 Event-Driven System Operation

The multi-modal analog front-end's event-driven operation is divided into two modes: 1) a low-power mode for monitoring primary vital signs (respiration rate and ECG-based heart rate), and 2) a full measurement mode for comprehensive monitoring when needed (comprises of respiration rate, PPG-based heart rate and blood oxygen saturation, and ozone). Fig. 5.6 shows the state transition diagram for the event-driven system operation. Once the system is reset, the low power ECG and capacitive-based respiration rate channels are turned on. These channels provide continuous monitoring of the user's heart rate and respiration rate. The capacitive-based respiration rate channel also serves as the canary channel, and features on-node data processing. It computes the user's respiration rate, and outputs it to the digital backend which continuously tracks and compares the user's RR with two programmable thresholds. These thresholds define a safe range for the user's respiration rate, which is usually lies between 12-20 breaths/min [41]. As the monitoring progresses, depending on the physical activity and environment, the user can have unusually fast or slow breathing. Once an abnormal RR is detected, the digital backend signals the analog front-end with a flag (*event_trig*) to indicate a need for comprehensive monitoring, and subsequently alerts the user. Following this, the analog front-end enters the full-measurement mode

with PPG and ozone channels turned on along with respiration channel to simultaneously monitor the user's SpO_2, heart rate, RR, and ambient ozone concentration. The analog front-end remains in the full measurement mode, and once the respiration rate returns back to normalcy, it transits back to low-power mode.

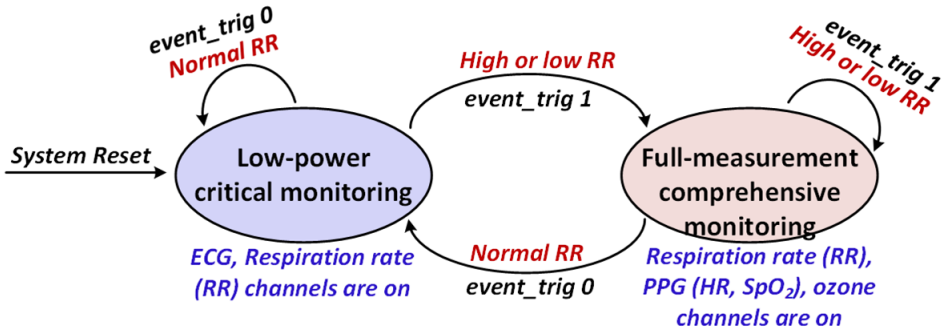

Figure 5.6: State-transition diagram of event-driven analog front-end operation.

5.3.3 Low Power Respiration Rate Analog Front-end

This work's leverages a custom passive capacitive sensor to realize a canary respiration rate channel with low-power on-node processing. Fig. 5.7 shows the capacitive sensor's working principle. To validate the channel's functionality, a model for the sensor is fabricated. This model sensor consists of two 0.05 mm thick copper films with a longitudinal gap between them. These films serve as two electrodes, and can be modelled as a capacitor with capacitance value (C_{SEN}) denoted by (5.3). Here, A is the area of the two copper films, ϵ is the permittivity of the dielectric material, and d is the distance between the two electrodes. Before the sensor is in use, it has a baseline capacitance value (C_{BASE}) ranging between 2pF – 4pF. Once deployed, the sensor tracks the user's breathing with a finite increase/decrease (± ΔC) in its capacitance from its baseline value (5.4). This is because, with each inhale/exhale action the distance between the two electrodes

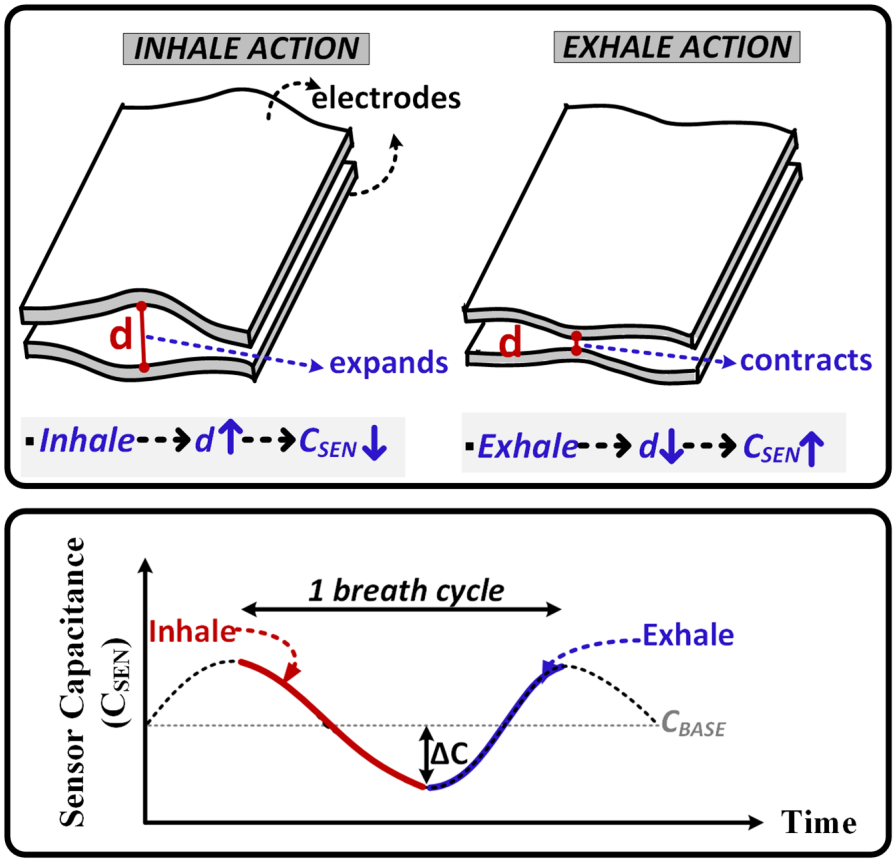

Figure 5.7: Respiration rate sensor model (top) and corresponding waveform (bottom).

increases/decreases resulting in a decrease/increase in the sensor's capacitance (5.3). Thus, each increase followed by a decrease in capacitance corresponds to one breathing cycle. Therefore, the user's respiration rate can be measured by simply detecting the high-to-low and low-to-high variations around the sensor's baseline capacitance Fig. 5.7.

$$C_{SEN} = A_{\epsilon}/d \tag{5.3}$$

$$C_{SEN} = C_{BASE} \pm \Delta C \tag{5.4}$$

The respiration rate channel extends a switched-capacitive bridge first introduced in [42], and implements on-node respiration rate processing to achieve low end-to-end power. The channel comprises of a switched-capacitor voltage divider formed by an 8-bit on-chip capacitive DAC

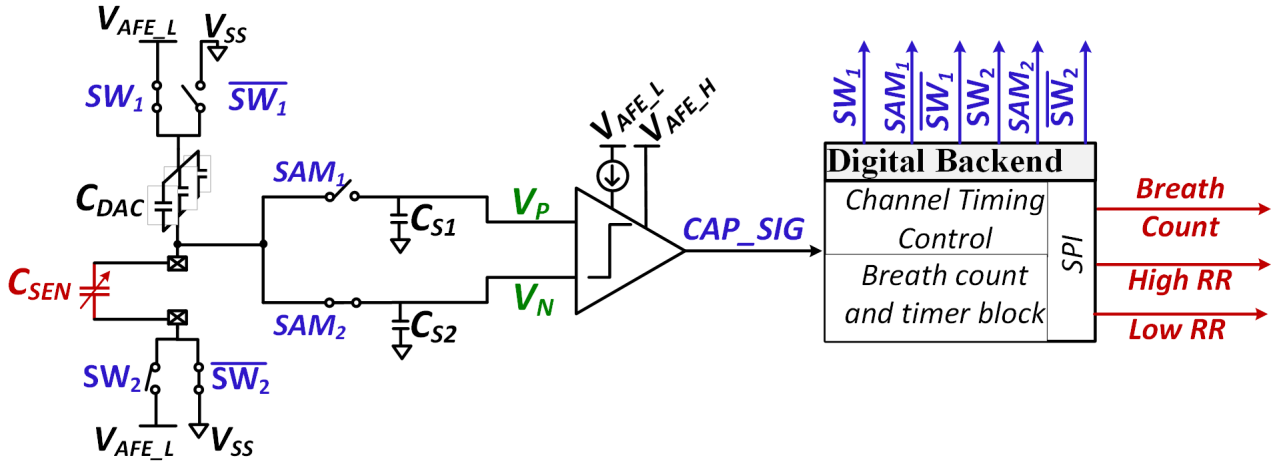

Figure 5.8: Schematic of the sub-μW respiration rate analog front-end.

(C_{DAC}) and the off-chip respiration sensor (C_{SEN}), a continuous comparator, and digital backend for on-node respiration rate processing and timing control (Fig. 5.8). During sensor characterization, its baseline capacitance value was found to typically lie within the range of 2 pF to 4 pF. Thus, the on-chip 8-bit C-DAC is implemented with eight parallel 1 pF capacitors that can be individually selected to realize an equivalent capacitance value of up to 8 pF. Since a sensor capacitance of ± 1pF to 1.5 pF is seen in response to exhale/inhale action, a capacitive DAC resolution of 1 pF is sufficient for this application. The switched capacitor bridge's top and bottom points are connected to both V_{AFE} and ground (V_{SS}) through switches SW1, ($\overline{SW1}$), SW2, ($\overline{SW2}$). When these switches are toggled, the bridge's top and bottom points are switched between V_{AFE} and V_{SS} or vice-versa. This switching action forms two voltage dividers configurations with output given by (5.5)-(5.6). The capacitors C_{S1} and C_{S2}, when connected to the capacitive bridge's output, hold the output voltages for both the voltage divider configurations. The comparator compares these stored voltages (V_P and V_N), and sends the output (*CAP_SIG*) to the digital backend for further data processing.

$$V_P = \frac{C_{DAC}V_{AFE}}{C_{SEN} + C_{DAC} + C_{S1}} \tag{5.5}$$

$$V_N = \frac{C_{SEN} V_{AFE}}{C_{SEN} + C_{DAC} + C_{S1}} \tag{5.6}$$

Fig. 5.9 shows the detailed timing diagram of the respiration rate channel's operation. Before deployment, the C_{DAC} is programmed using ***CDAC_CTRL***$< 7:0 >$ to match the sensor's C_{BASE}. Following this, in every one-minute window the channel uses repeated sample and hold cycles to measure the capacitance, and count the number of breaths taken. The sample cycle is carried out in two phases to sample the output voltage of both the divider configurations mentioned above. During the first sampling phase, the switches SW_1 and SAM_2 are high, and SW_2 and SAM_1 are set low, connecting the top and bottom of the bridge to V_{AFE} and V_{SS}, and holding the output voltage (V_N) of the bridge on C_{S2}. After this, both C_{DAC} and C_{SEN} are fully discharged and the front-end enters the next phase of the sampling cycle. Here, the switch polarities are reversed to obtain output (V_P), which is then stored using C_{S1}. Meanwhile, the comparator immediately updates its output ***CAP_SIG***. This concludes one sample and hold cycle. After this, the digital backend gets updated with the new ***CAP_SIG*** value, and the bridge is reset. In order to restrict the hold capacitors' (C_{S1}/C_{S2}) to a small area, the repetition frequency of the sample and hold cycles is set at 100 kHz. As mentioned before, in response to the user's inhale/exhale actions, the C_{SEN} value always varies around its baseline capacitance. Therefore, once the C_{DAC} value is programmed to match C_{BASE}, an inhale action translates into V_N settling to a value less than V_P. While, the inverse happens when the user lets out the air (exhale). Therefore, a transition of the signal ***CAP_SIG*** from logic high-to-low and low-to-high mimics the user's breathing, and can be used to compute the respiration rate.

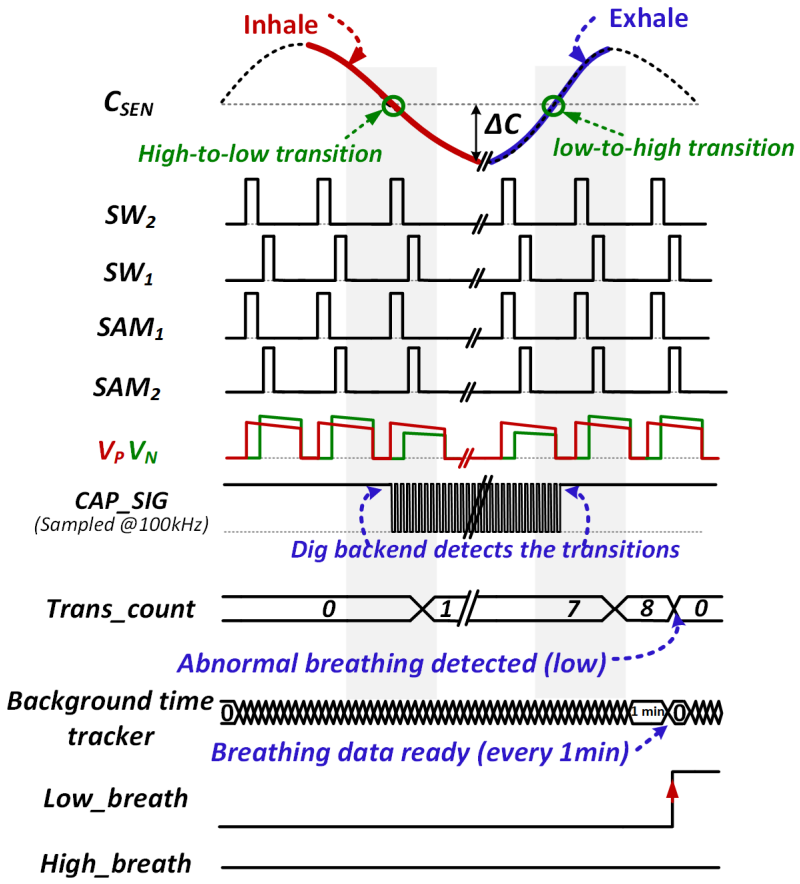

Figure 5.9: Detailed timing diagram of respiration rate analog front-end's operation.

After the end of each sample and hold cycle, the digital backend matches the comparator's new output (*CAP_SIG[n]*) with its previous value (*CAP_SIG[n-1]*) to detect the signal's high-to-low and low-to-high transitions. Each of these transitions represents one half of a breath (5.7). A 16-bit register ($TRANS\_COUNT < 15 : 0 >$) is updated at each such transition, while a 25-bit background timer keeps track of the time. Once, this background timer exceeds the threshold value set by time_threshold$< 24 : 0 >$, the number of transitions are ready to be sampled. Following this, the timer and the transition counter are reset. In order to differentiate between zero breaths-per-minute and other slower respiration rates, the background timer's threshold value is set to

correspond to one minute. Digital hysteresis is incorporated to remove the random cap variations picked up by the sensor, and subsequently the AFE. An on-chip SPI module is used to retrieve the transition count at the end of each minute, which can be then used to compute the user's respiration rate (5.7). Therefore, this approach successfully monitors the user's respiration rate without relying on high-power ADCs and complex computation.

$$Breath\,count = \frac{(\#high - to - low + \#low - to - high)}{2} \tag{5.7}$$

5.4 Measurement Results

The event-driven multi-modal sensor interface IC was designed and fabricated in a 65nm bulk CMOS process with die area of $6mm^2$. The die-microphotograph is shown in Fig. 5.10. The proposed sub-μW respiration rate channel occupies a total area of 0.205 mm^2, out of which 0.093 mm^2 is taken by its analog components, while the remaining 0.112 mm^2 is occupied by the digital backend.

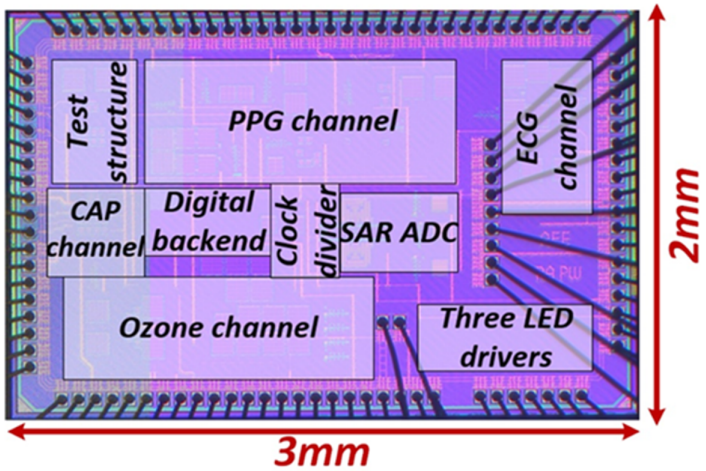

Figure 5.10: Die microphotograph of the proposed multi-modal analog front-end.

Fig. 5.11 shows the measured ECG/PPG/RR/ozone joint operation of the proposed event-driven multi-modal analog front-end IC. Here, both the ECG and PPG signals are measured by connecting respective sensors to the user's chest and fingertip. The respiration sensor prototype receives air flowing through it while a variable resistor is used to emulate the ozone sensor. The AFE is initially in low-power mode with ECG and respiration channels on. As shown in the zoomed-in measurement (topmost), at the end of 1 minute, a respiration rate of 8breaths per minute is read through the SPI. Following the detection of respiratory distress, the digital backend is able to startup the PPG and ozone channels, and give a complete report including PPG-based heart rate, respiration rate, blood oxygenation, and ozone concentration.

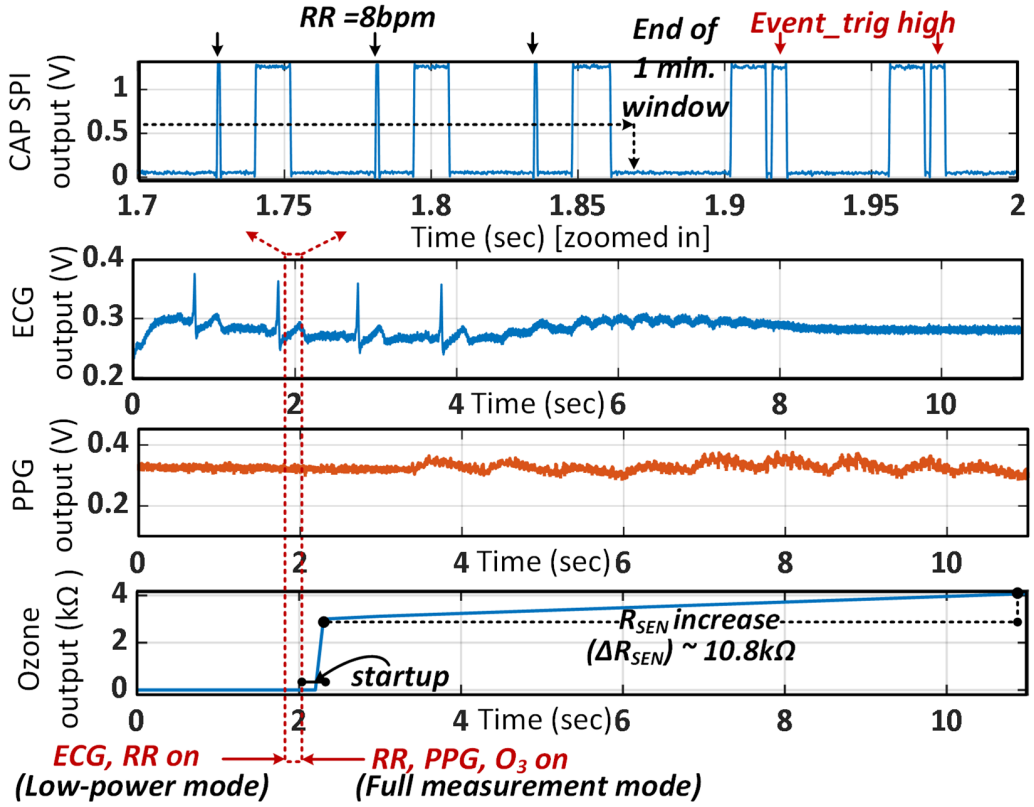

Figure 5.11: Measurement showing event-driven system operation of the proposed ECG/RR/PPG/ozone analog front-end.

The respiration channel's measurements with the sensor model are shown in Fig. 5.12. In order to mimic the user's breathing, air with varying flow rates is allowed to pass through the sensor. As mentioned before, the respiration analog front-end continuously tracks the breath count (given by number of transitions) within one minute (defined by the value of 25-bit register, time_threshold$< 24 : 0 >$) to compute the user's respiration rate. This also helps in differentiating between slower and zero respiration rate. This is because, as the respiration rate slows down, the breath count in one minute decreases and drops to zero in case of no airflow/user holding his breath. However, the available oscilloscopes cannot capture waveforms spanning across several minutes. So, for the purposes of demonstrating the analog front-end's operation, instead of tracking the number of breaths in a whole one minute, we limit the observation time to a smaller time window. Therefore, assuming the flow rate as the ground truth, we reset the time window and breath count with each flow rate, and observe the number of breath-counts within each such time window. The final breath count observed at the end of each time window is later used to compute the user's respiration rate.

The measurement plot shows the channel's comparator output annotated with the respective flow rates (L/sec) (top), and measured respiration rate (breath-per-minute) computed from the on-chip SPI's output (below). When the air flow is stopped, no high-to-low or low-to-high transitions are observed, indicating no breaths taken. The breath count in this case is observed to remain at zero till a time period of one minute is passed. Since, this happens much later than the time captured in the waveform (Fig. 5.12), the plot only contains a label showing a RR trending to zero bpm.

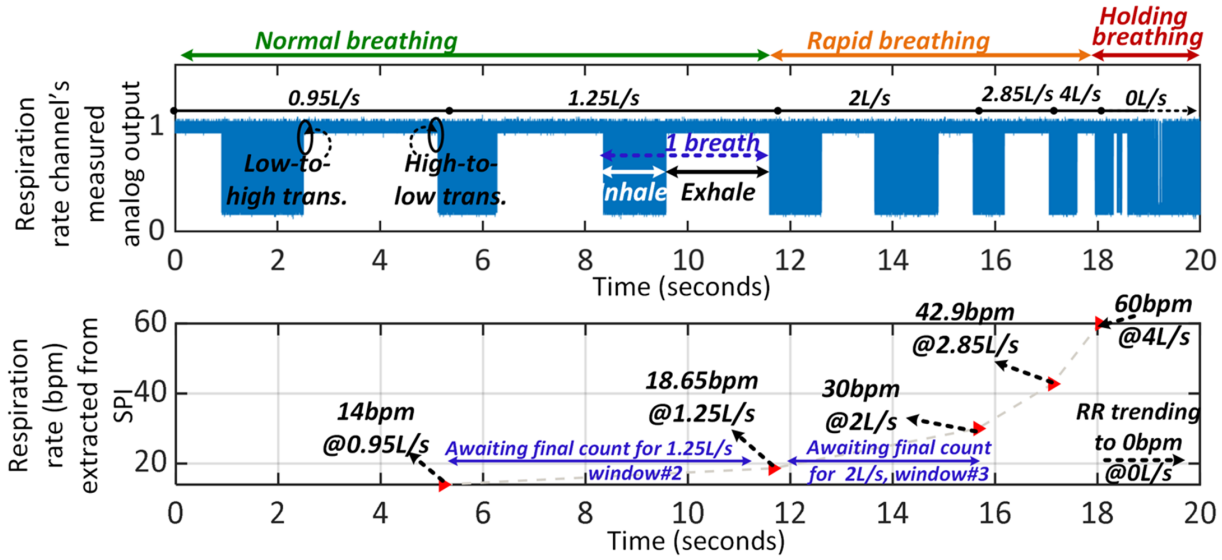

Figure 5.12: Measured respiration rate output at different breathing rates.

Table VI compares the respiration rate channel's power with other state-of-the-art custom ICs. This work's respiration channel adopts a dynamic circuit with on-node processing to achieve sub-μW operation with a 90.7x power reduction compared to prior respiration rate channels [27], [28], [36].

TABLE VI

POWER COMPARISON FOR RESPIRATION RATE ANALOG FRONT-END

		[53] This Work	[27] ISSCC'19	[28] TbioCAS'18	[36] JSSC'16
Technology		65nm	55nm	180nm	180nm
Supply Voltage		0.6/1.2V	0.6/1.2V	1.2V	1.2V
Power	***Analog Front-end***	13nW	74µW	36µW	46µW
	Data Processing	384nW	22.96µW	N.A.	458.4µW

Fig. 5.13 shows the power savings achieved through the proposed event-driven architecture. The event-driven power is estimated using equation (5.8). Here, the p denotes the worst-case probability of the user suffering from respiratory distress due to underlying health issues, daily activities or exposure to harmful air pollutants. Overall, the event-driven control scheme achieves a 206x power reduction compared to conventional always-on operation.

$$P_{EVENT} = P_{RR} + (1-p)P_{ECG} + p(P_{PPG} + P_{gas}) + P_{DIGITAL} \tag{5.8}$$

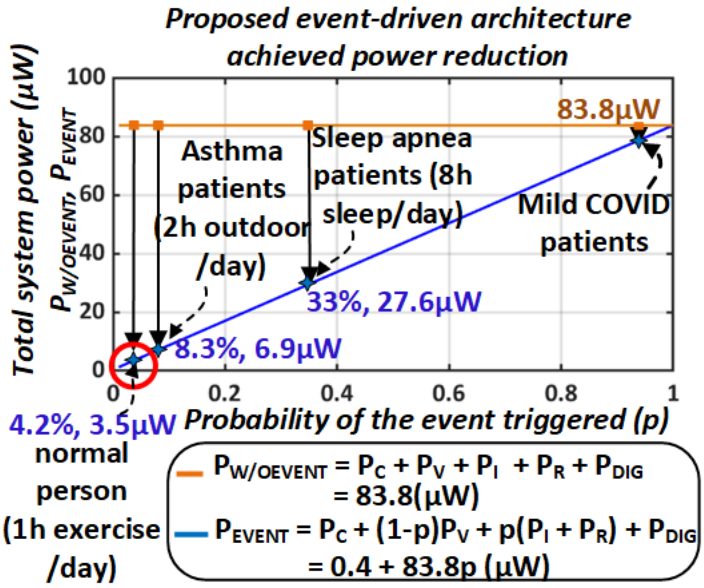

Figure 5.13: Event-driven scheme power savings achieved for different use cases.

Table VII summarizes the power and performance of the proposed chip, compared with the state-of-the-art multi-modal and dedicated PPG/ECG/ozone/respiration analog front-ends. All the four channels maintain competitive noise/dynamic range performances, and reduce the system power by ∼7-1500 times, when compared to previous physiological and environmental co-sensing.

TABLE VII

PERFORMANCE SUMMARY AND STATE-OF-THE-ART COMPARISON

Proposed Event-Driven ECG/PPG/RR/Ozone Multi-modal Analog Front-end						
Always-on low-power mode			Event-triggerd full-measurement mode			
405 nW			22.4 µW-83.4µW (w/ 3 LEDs)			
		[53] This work	**[43] ISSCC'20**	**[49] VLSI'20**	**[28] TbioCAS'18**	**[48] JSSC'14**
Modalities		V/I/R/C	V/I/R	V/I/R	V/I/R	V/I/R/C
Use case		ECG, PPG, RR, gas	ECG,PPG, GSR,BioZ	ECG, PPG, gas	ECG,PPG, GSR,BioZ	Temp,glucose, protein,pH
Event-driven		Yes	No	No	No	No
Process		65nm	55nm	65nm	180nm	350nm
V_{AFE}		0.6/1.2/3.3V	0.9/1.8/2.8V	0.6V	1.2V	1.8V
Area		6mm^2	4.5mm^2	5mm^2	1.1mm^2	11.25mm^2
C channel (RR)	***Power***	13nW	N.A.	N.A.	N.A.	2.57µW
	Input range	2pF–9pF	N.A.	N.A.	N.A.	6pF-11pF
V channel (ECG)	***Power***	3nW	192.6µW	165nW	33µW	2.57µW
	Input noise	23µV$_{rms}$(45 Hz)	0.73µV$_{rms}$(150 Hz)	20µV$_{rms}$(45 Hz)	0.8µV$_{rms}$(100 Hz)	769nV$_{rms}$/√Hz
I channel (PPG)	***Power***	2.3µW	72µW	532nW	20µW	2.57µW
	Input noise	14pA$_{rms}$ (5Hz)	63.2pA$_{rms}$ (20Hz)	45pA$_{rms}$ (5Hz)	N.R.	N.R.
	Dynamic Range	116dB	130dB	92dB	N.R.	N.R.
R channel (ozone)	***AFE power***	57 nW	N.A.	75.6nW	36µW	2.57µW
	IDAC power	0.028-2µW	N.A	N.R.	N.R.	N.A.
	Resolution	0.24 – 12Ω	N.A	0.59-65Ω	N.R.	N.R.
	Dynamic Range	138 – 144dB	N.A	N.R.	N.R.	N.R.
Digital Backend Power		384nW	N.R.	N.R.	N.R.	N.R.
AFE total power		2.5 – 4.8µW	264.6µW	785nW	28.43µW	12.83µW
PPG LED power (red/infrared)		4.9 – 48µW	N.R.	8.5µW	N.R.	N.A.
UV LED power		15µW – 31.5µW	N.A.	N.R.	N.A.	N.A.

5.5 Conclusion

This section of the dissertation presents an event-driven multi-modal analog front-end IC for heart rate, respiration rate, SpO_2, and ozone co-sensing. A context-aware event-driven con-

trol scheme is introduced to reduce the system power overhead by implementing relevant-sensing, and reducing unnecessary data generation. Measurements from a 65nm CMOS chip show 405nW always-on AFE power, 4.8μW full-measurement AFE power, and 38.4-83.8μW full-measurement system power including red/infrared/UV LEDs. Lowering the system power by 206x when compared to always-on mode, this event-driven multi-modal analog front-end increases the system availability, and achieves more reliable self-powered operation for physiological and environment co-monitoring. When compared with other environmental and physiological monitoring systems, it reduces the system power by $\sim$7-1500x [10]. This section also presents a sub-μW respiration rate channel with on-node signal processing to achieve 90.7x power reduction when compared to other state-of-the-art respiration rate front-ends. A list of contributions presented in this chapter are as follows:

1. Evaluated the various tradeoffs of traditional always-on and heavily duty-cycled sensing nodes.

2. Implemented the digital-backend for event detection and subsequent programming of analog front-end in either full-measurement or low-power monitoring mode.

3. Designed the capacitive-based respiration analog front-end along with the on-node respiration rate processing.

4. Implemented the digital backend for the respiration rate analog front-end.

5. Designed the gas analog front-end (Chapter 3), and implemented the digital backend's physical design including synthesis and placement and route for the entire multi-modal AFE.

CHAPTER 6

UNIVERSAL V/I/R/C ANALOG FRONT-END

6.1 Introduction

The recent advances in development of both the sensors and accompanying custom signal processing ICs have extended the IoT applications to a diverse group of use cases like health care, environmental monitoring, agriculture, smart homes, smart infrastructure etc. These applications utilize IoT sensor nodes for performing tasks such as sensing, predictive maintenance, continuous monitoring, and processing of critical information. The IoT sensors detect both physical and biological signals, and output them in the form of an electrical signal which can belong to any of the modalities including voltage (V), current (I), resistive (R) and capacitive (C). Also, a wide sub-set of these applications need multi-sensor data with different combinations of the above-mentioned four modalities. Thus, existing works cater to these design requirements by implementing either multiple sensor-specific single-channel analog front-ends, or an integrated multi-modal analog front-end with dedicated channels for each modality, laid out in a parallel architecture [27], [42]. While this provides high performance, it's specificity might make it unsuitable for use as a general-purpose analog front-end due to various limitations like insufficient dynamic range, over-designed resolution, large area etc. As analog front-ends are one of the major contributors in total sensor node power, design efforts towards making low-power AFEs have been quite popular. Additionally, as mentioned before, self-powered systems are also touted as a potential solution to eliminate

the battery-recharging problem. Thus, the limited power budget coupled with the requirement of multi-modal sensing platforms has made low-power multi-modal analog front-ends a much researched and looked into topic. However, majority of these efforts have been focused on designing low-power multi-modal AFEs for specific biomedical applications [27], [28], [43]. Since, these designs are highly customized to meet application-specific performance metrics, they are rendered unusable for more generic use-cases/sensors. Some of the issues faced while using these sensor-specific AFEs for other applications are described below.

Firstly, sensor/application-specific analog front-ends slow down the development time and also increase the engineering cost. With these AFEs, there is a large design effort and time involved in order to account for even the smallest changes in the sensing requirements. Additionally, the fabrication and mask costs involved with each design upgrade are significant. This especially becomes a bottleneck in niche small-scale productions, which have limited budget for engineering costs. Having a universal analog front-end that is easily reconfigurable and can support plethora of sensors would significantly reduce the development time for building new micro-nodes.

Also, in order to support the growing need for niche IoT applications, the sensor nodes need to be cost-effective. While single channel analog front-ends lead to multiple chipsets incurring high integration cost and complexity, a parallel multi-modal analog front-end would lead to larger silicon die area. The hardware cost of IoT is a significant contributor to the total development cost of an IoT node. Thus, having a universal single-channel analog front-end enables efficient hardware reuse, smaller die area, and reduced number of chipsets, all of which lead to decrease in the integration complexity, and hardware cost.

Secondly, when such application-specific analog front-ends are used for other sensors, they might deliver higher performance metrics than necessary and end up being over-designed for the

new application. Since power plays a major role in improving an AFE's performance, this would incur unnecessary power overhead. Thus, adding reconfigurability to program the analog front-end's performance helps in realizing a more flexible AFE design whose key metrics can be tailored for the target applications. Using this, one can achieve a desirable power-performance tradeoff.

Most of the analog front-ends designed for general purpose sensing, mostly support a subset of resistance, capacitance, current or voltage modalities [42], [44], [45]. Works prior to this dissertation, that combine all the four modalities consume power within the range of tens of μW to several mW [46], [47]. Therefore, a reconfigurable low-power universal analog front-end supporting all of the four modalities i.e., voltage, current, capacitive and resistive can interface with a plethora of sensors, and make more IoT sensor nodes more accessible and economical. This chapter takes a conceptual look at designing a universal, single-channel V/I/R/C analog front-end, and uses simulations to demonstrate its reconfigurability.

6.2 Design Considerations

The performance of an analog front-end and its suitability for an application can be evaluated using various key metrics such as its signal-to-noise ratio (SNR), dynamic range (DR), resolution, and signal bandwidth. Traditionally, analog front-ends comprise of components like high-gain operational amplifiers, followed by low-/band-pass filter, and an analog-to-digital converter. Typically, analog front-ends for V/I/R/C modalities are implemented using different types of amplifiers such as transimpedance amplifier, voltage amplifiers etc. Therefore, many of the multi-modal analog front-ends based off of operational amplifiers, feature dedicated parallel channels for each of the modalities, resulting in large die area. Some prior works incorporate switched-capacitor amplifiers in the signal chain to realize the different amplifier configurations needed to support all of

the four modalities [46], [47], [48]. However, adopting such amplifier-based architectures incurs heavy design complexity, and limits the amount of reconfigurability it can achieve. Some of its associated design limitations are discussed below.

Scaling down the supply voltage of any design helps in significantly reducing its power consumption. But this severely limits the headroom available for an amplifier's transistors. As a direct result of limited headroom, the amplifier's operating range reduced, which in turn lowers the AFE's dynamic range. However, in order to be used as a power-efficient universal sensor interface, the analog front-end needs to have a wide dynamic range which can be tailored to meet the application requirements. Therefore, for amplifier-based architectures, power reduction promoted by supply voltage scaling comes at a cost of reduced dynamic range. This makes these architectures a less favorable choice for reconfigurable universal analog front-ends.

Additionally, to match the application's requirements involving metrics such as dynamic range, resolution etc., the front-end's amplifier needs to provide an appropriately high gain at the signal bandwidth. In order to implement a power-efficient reconfigurable design, the amplifier needs to support a wide range of gain-bandwidth products. This significantly increases the design complexity, and again requires the front-end to operate at high supply voltages leading to increased power overhead.

Therefore, to avoid these issues, this dissertation chooses a time-based architecture to realize a low-power, single-channel analog front-end for all the four sensing modalities, and incorporate much needed reconfigurability for supporting wide range of sensors.

6.3 Design Apporach

This work implements a time-based architecture that directly gives the digital output and bypasses the use of high-resolution ADCs. This architecture utilizes the charging and discharging of a capacitor to first translate the voltage, current, resistive, and capacitive input signals to frequency, and then converts it into a digital output (D_{OUT}) corresponding to the input signal's value. The single channel AFE is adaptable, and can be dynamically programmed to operate in any of the four configurations i.e., voltage, current, resistive or capacitive.

6.3.1 System Architecture

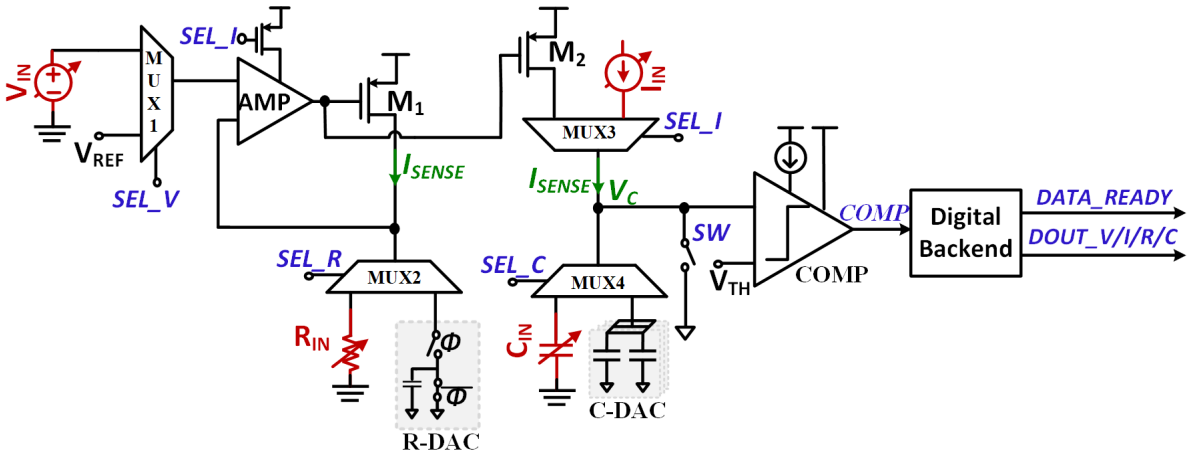

Figure 6.1: System architecture of the proposed reconfigurable universal V/I/R/C analog front-end.

Fig. 6.1 shows the schematic of the universal V/I/R/C analog front-end. Since the front-end needs to provide connections for the capacitive, current, resistive and voltage sensor inputs, analog multiplexers (MUX1-MUX4) are included to make a selection between the sensor inputs, and one of the following, C_{DAC}, R_{DAC}, V_{REF}, and I_{SENSE} components. Additionally, both V_{REF} and V_{TH} are generated using tunable resistor dividers to incorporate second order reconfigurability.

The digital backend is used to program the AFE in R, C, V, or I mode, by making appropriate selections for the analog multiplexers. The sampling frequency (f_S) is programmable, and is used to toggle the switch SW with help of the digital backend. The digital backend and R-I converter operate at V_{AFE} of 0.6 V. The comparator is designed to operate at 1.2 V.

The following sub-sections present each of the four configurations, and the design knobs used to reconfigure performance metrics like dynamic range, resolution etc.

6.3.2 Resistive Configuration

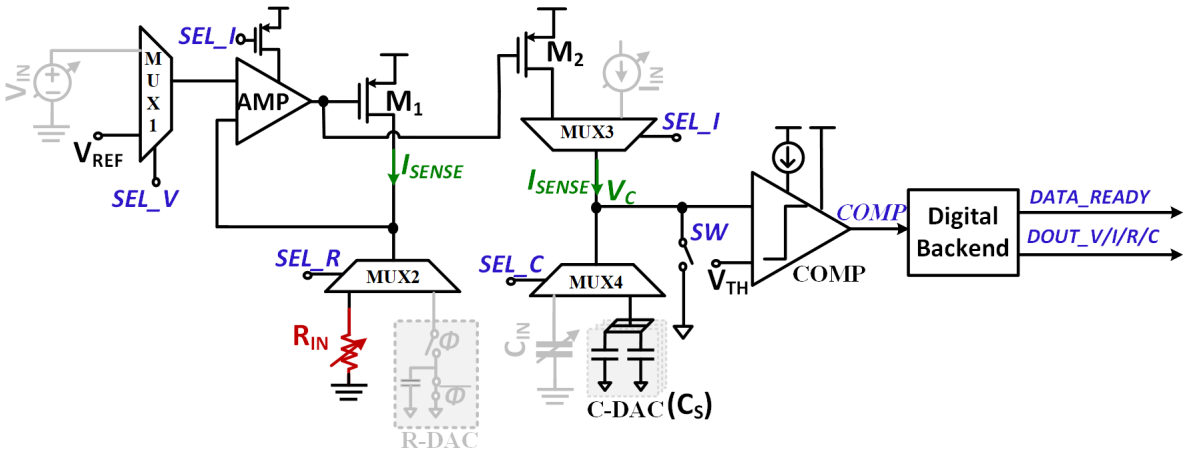

Figure 6.2: Schematic of the proposed AFE configured in R-mode.

Fig. 6.2 shows the time-based resistance-to-digital configuration (RDC) used for input signals from a resistive (R) sensor. The circuit implementation comprises of a resistance-to-current (R-I) converter, an integrating capacitor (C_S), the unknown sensor resistance (R_{IN}), a continuous comparator (COMP), and associated digital backend. The RDC's operation can be divided into two phases: 1) charge/measurement phase, and 2) reset phase. In this approach, the capacitor C_S's charging time (t_R) is measured and is used to compute the sensor resistance.

The R-I converter comprises of a high gain amplifier (AMP) connected in negative feedback with a voltage-controlled current source (M_1). This negative feedback loop converts the sensor resistance (R_{IN}) to a current (I_{SENSE}) such that the voltage generated across R_{IN} is fixed to V_{REF} (6.1). This current is further mirrored and sourced on a fixed capacitor (C_S). Now, the capacitor acts as an integrator, and its top plate starts charging up in response to I_{SENSE}. This causes the voltage across the capacitor (V_C) to start increasing from V_{SS}. Meanwhile, the comparator acts as a 1-bit slope detector and continuously tracks V_C. The digital backend includes a counter clocked at a much higher frequency of f_{CLK}, and uses it to track the time during the capacitor's charging phase. Once V_C reaches the comparator's threshold voltage (V_{TH}), the counter stops its operation, and sets signal *DATA_READY* as logic high to indicate that the measurement is complete. The digital backend output (*DOUT_R*) gives the time taken by C_S to charge from V_{SS} to V_{TH}, and is proportional to the unknown sensor resistance, R_{IN} (6.1)-(6.3). After the charge phase, the switch SW is set high to fully discharge C_S through M_2. The time duration of the charge and discharge phases is decided by the sampling frequency set by the user. The analog front-end's performance is evaluated through its resolution and dynamic range (6.4)-(6.5).

$$I_{SEN} = \frac{V_{REF}}{R_{IN}} \tag{6.1}$$

$$T_{MEAS\_R} = \frac{C_S V_{TH}}{I_{SEN}} = \frac{C_S V_{TH} R_{IN}}{V_{REF}} \tag{6.2}$$

$$D_{OUT\_R} = \frac{T_{MEAS\_R}}{T_{CLK}} \tag{6.3}$$

$$R_{LSB} = \frac{R_{IN}}{D_{OUT\_R}} \tag{6.4}$$

$$DR = 20log(\frac{R_{IN-MAX}}{R_{LSB}}) \tag{6.5}$$

The total analog front-end power in the resistive configuration comprises of static power (P_{STAT}) and dynamic power (P_{DYN}). The static power includes power consumed by the R-I

converter, the sensor biasing current (I_{SENSE}), and the continuous comparator. Whereas, the dynamic power is a function of the integrating capacitor (C_S), the sampling frequency (f_s), and the voltage generated across the capacitor (V_C) (6.6).

$$P_{R-mode} = P_{STAT} + P_{DYN} = V_{AFE}I_{SEN}\frac{t_{charge}}{t_{conv}} + V_{AFE}I_{COMP} + f_S C_S V_C^2 \tag{6.6}$$

Fig. 6.3 shows the simulated results of the analog front-end's R-mode configuration. An integrating capacitor of 400 pF and a sampling frequency of 1 kHz is chosen for this simulation. As seen from the figure, for an input resistance range of 20 kΩ to 1 MΩ, the analog front-end's total power lies between 201 nW to 3.14 μW. The resolution for the given sensor resistance range falls within 794 Ω to 2.3 kΩ.

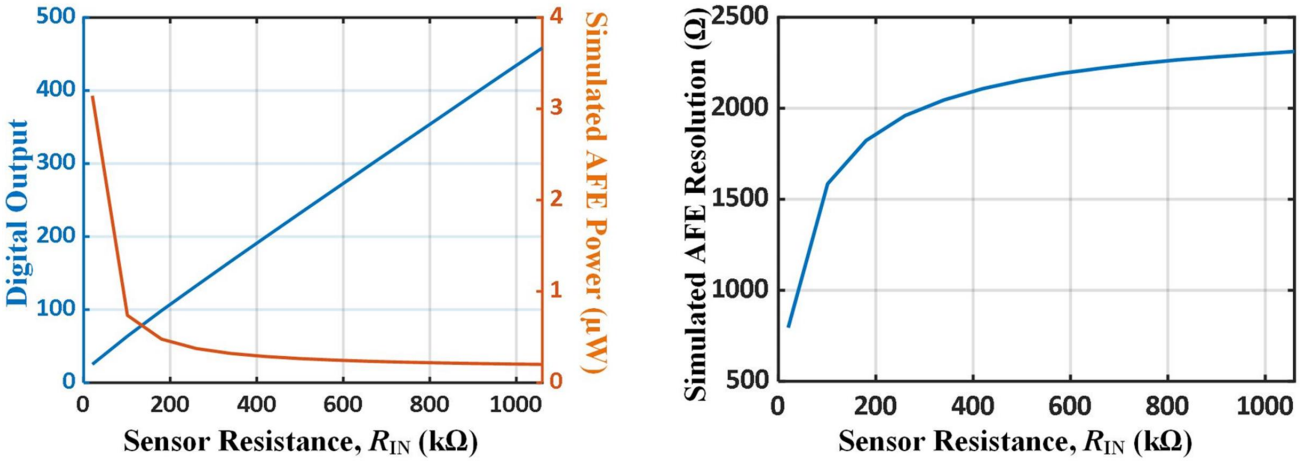

Figure 6.3: Simulated results of the R-mode configuration showing the AFE power and resolution across a resistance range of 20kΩ to 1MΩ.

6.3.2.1 Dynamic range and resolution scaling. As shown by (6.1)-(6.4), the R-mode configuration's minimum resolvable resistance is inversely proportional to its integrating capacitor, C_S. Thus, increasing the C_S will improve the AFE's resolution while simultaneously increasing its dynamic power consumption. Also, this increases the capacitor's charging time, subsequently

limiting the AFE's sampling frequency. Thus, the AFE's performance metrics such as its resolution and dynamic range can be easily reconfigured by choosing different values of C_S at the cost of higher power and slower sampling rate. This is implemented using a capacitive-DAC designed to cover the desirable range of AFE resolution and dynamic range. Since, the AFE's signal chain does not include an operational amplifier, the addition of the CAP-DAC does not contribute to any stability issues. Fig. 6.4 shows the simulated results of the AFE's resolution achieved by varying the integrating capacitor C_S. For C_S values from 50 pF to 450 pF, the AFE's resolution can be tuned from 742 Ω to 1.6 kΩ. The dynamic range tunability is computed to lie between 37.05dB to 54.08dB for a sensor resistance value of 1.06 MΩ. As shown in the figure, higher C_S values significantly improves the AFE's resolution at cost of a small increase in the power. Similarly, both V_{REF} and V_{TH} can be tuned using simple resistor-based voltage dividers to improve the AFE's resolution and dynamic range.

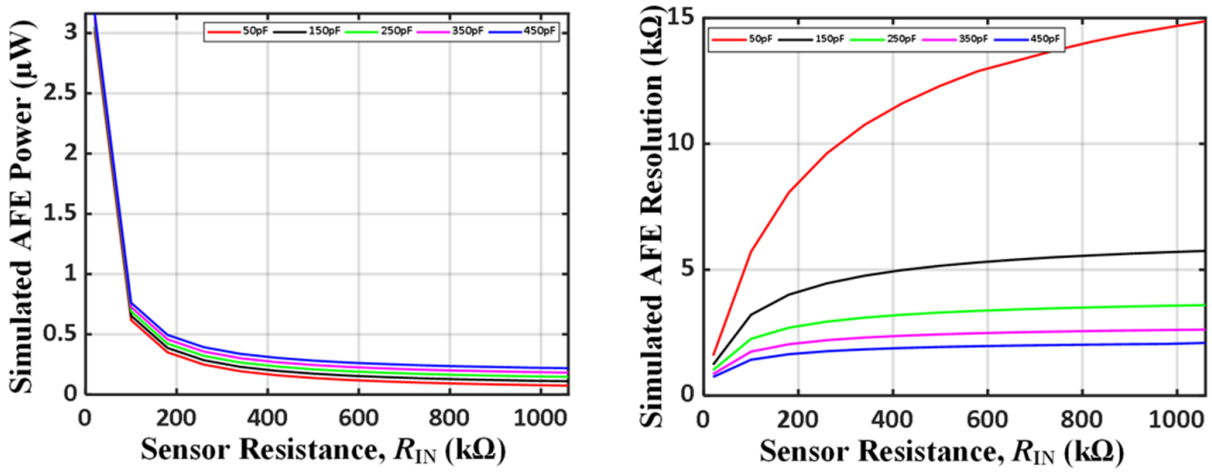

Figure 6.4: Simulated results of the R-mode configuration's tunability range for resolution (right), and resulting power consumption (left)

Another design knob that the AFE can use to improve its performance is the reference clock frequency (f_{CLK}). Since, this clock source only goes to the digital backend, it does not affect the

sampling rate or power consumed by the analog components. However, generating a higher clock frequency increases the total system power. Since, this work does not implement a custom clock source, the f_{CLK}'s effect on the AFE's performance is not simulated.

6.3.3 Current Configuration

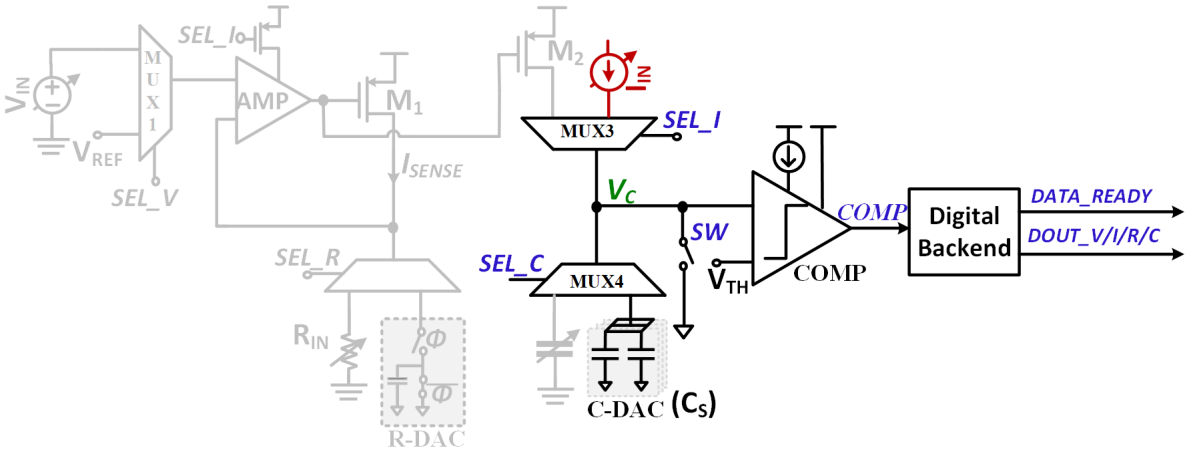

Figure 6.5: Schematic of the proposed AFE configured in I-mode.

Fig. 6.5 shows the configuration used for sensing current (I) input from a sensor. In order to facilitate the realization of a single channel universal analog front-end for all the four modalities, the current-mode is designed using a similar principle as the other configurations. Therefore, this mode is implemented using a current-to-time convertor (ITC) circuit. However, unlike the R-mode configuration, this mode comprises of only an integrating capacitor (C_S), the unknown sensor current (I_{IN}), a continuous comparator (COMP), and associated digital backend. Here, the capacitor C_S's charging time (t_R) is measured and is used to compute the sensor current. The transistor M_2 serves as a constant current sink during the discharge phase.

As the sensor's output is a current signal, the integrating capacitor is charged using the sen-

sor's signal itself, thus eliminating the need for a separate current source. The ITC's operation is also divided into charge/measurement phase followed by a reset phase. During the measurement phase, the signal SW is high, allowing sensor's current (I_{IN}) to charge the integrating capacitor. In response to this, a voltage V_C is generated across C_S. As denoted by (6.7), the capacitor's charging time is inversely proportional to the sensor current. Thus, for a higher I_{IN} value, T_{MEAS_I} would be smaller. While the capacitor's voltage is increasing, the comparator matches it with its threshold voltage (V_{TH}). Additionally, the digital backend along with the much faster reference clock, tracks the time taken by I_{IN} for charging C_S to V_{TH}. Once the capacitor voltage V_C reaches V_{TH}, the comparator's output switches to a logic high. The signal *DATA_READY* is now set to high and the digital backend's output (D_{OUT_I}) is read, and subsequently reset. D_{OUT_I} indicates the time required by I_{IN} to charge the capacitor to V_{TH}, and can be used to compute the sensor current (6.7)-(6.8). During the discharge phase, the sensor's input is cut-off from the AFE by setting SW to logic 0. At the same time, the transistor M_2 is turned on to completely discharge the integrating capacitor. The analog front-end's performance is evaluated through the resolution and dynamic range that it achieves (6.9)-(6.10).

$$T_{MEAS\_I} = \frac{C_S V_{TH}}{I_{IN}} \tag{6.7}$$

$$D_{OUT\_I} = \frac{T_{MEAS\_I}}{t_{CLK}} \tag{6.8}$$

$$I_{LSB} = \frac{I_{IN}}{D_{OUT\_I}} \tag{6.9}$$

$$DR = 20log(\frac{I_{IN-MAX}}{I_{LSB}}) \tag{6.10}$$

Unlike the R-mode configuration, the static power of the current configuration only includes the power consumed by the continuous comparator. Whereas, the dynamic power is still a function of the integrating capacitor (C_S), the sampling frequency (f_s), and the voltage generated across the

capacitor (V_C) (6.11).

$$P_{I-mode} = P_{STAT} + P_{DYN} = V_{AFE}I_{COMP} + f_S C_S V_C^2 \tag{6.11}$$

Fig. 6.6 shows the simulated results of the analog front-end's I-mode configuration. This mode consumes around 10 nW of power while achieving a resolution of 3.29 pA to 7.32 nA across an input current range of 20 nA to 1.02 μA respectively. This simulation is carried out with an integrating capacitor of 300 pF and a sampling frequency of 50 Hz. The dynamic range of the I-mode with the above-mentioned fS and CS values lies between 42.87dB-75.65dB.

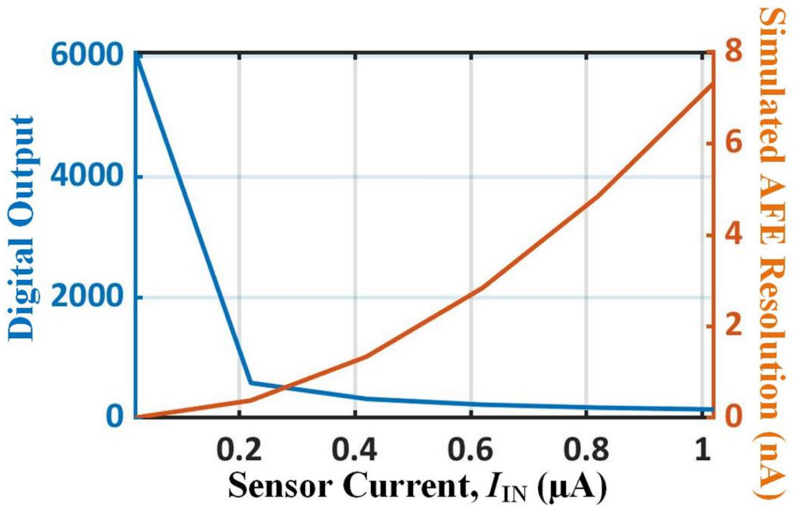

Figure 6.6: Simulated results of the I-mode configuration showing the AFE power, digital output, and resolution across a current range of 20nA to 1.02μA

6.3.3.1 Dynamic range and resolution scaling. A larger C_S would increase the time taken by the capacitor to charge to V_{TH} (6.7). This in turn increases the T_{MEAS_I}, subsequently improving the I-mode configuration's resolution (6.9). However, this comes at a cost of increased dynamic power consumption. Thus, the I-mode's performance metrics such as its resolution and dynamic range can be easily reconfigured by choosing different values of C_S at the cost of higher

power. Fig. 6.4 shows the simulated results of the AFE's resolution achieved by varying the integrating capacitor C_S across current range of 20 nA to 1.02μA. For C_S from 50 pF to 400 pF, the AFE's resolution can be tuned from 2.47 pA to 28.7 nA. A dynamic range tunability of 60.36dB to 78.13dB is achieved at sensor current value of 20 nA. As shown in the Fig. 6.7, higher C_S values significantly improves the AFE's resolution. However, in case of I-mode, the resulting increase in power is significant. Similarly, a higher f_{CLK} can be also used to improve the AFE's resolution and dynamic range.

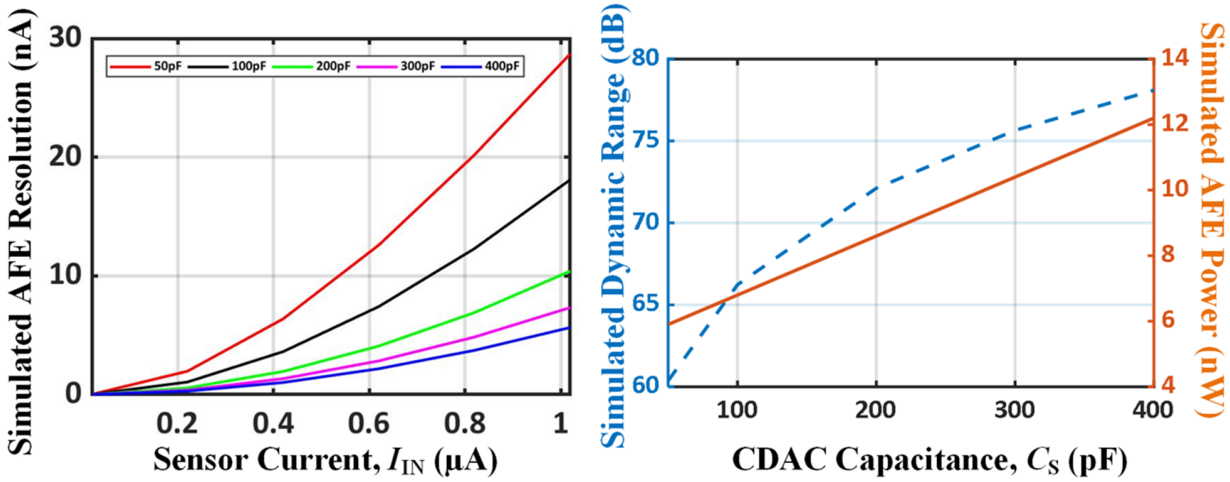

Figure 6.7: Simulated results of the I-mode configuration's tunability range for resolution (left), and resulting power consumption (right).

6.3.4 Capacitive Configuration

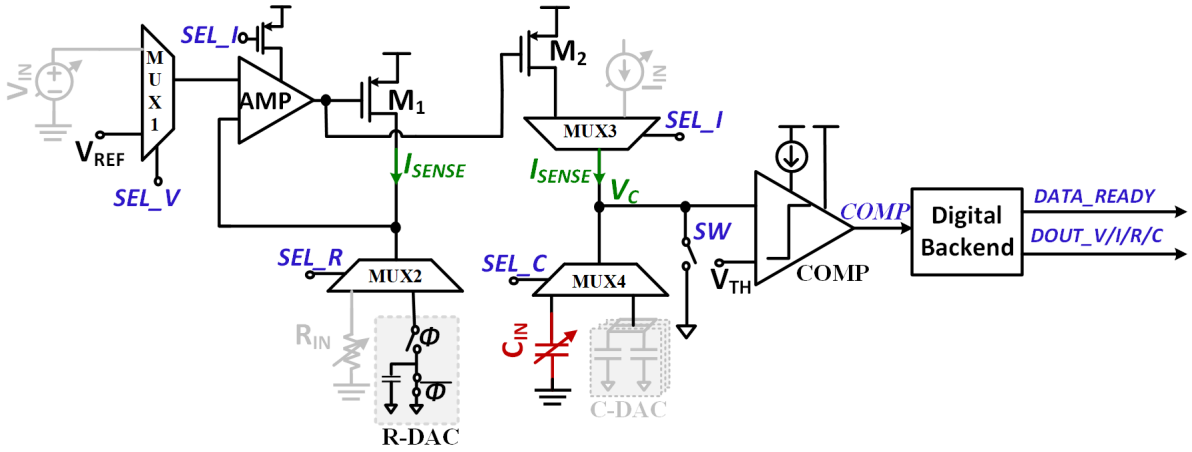

Figure 6.8: Schematic of the proposed AFE configured in C-mode.

Fig. 6.8 shows the capacitive-mode (C-mode) for the single channel universal analog front-end. The capacitive-mode realizes a capacitance-to-digital convertor (CDC), and uses a similar architecture to the R-mode configuration for ease of integration. It's circuit implementation comprises of a resistance-to-current (R-I) converter, the unknown sensor capacitance (C_{IN}), a continuous comparator (COMP), and associated digital backend. Here, the sensor itself acts as the integrating capacitor. To simplify integration with the other modalities, the capacitor C_{IN}'s charging time (t_R) is chosen as the preferred measurement to compute the sensor capacitance. Similar to the other modes, the transistor M_2 serves as a constant current sink during the discharge phase.

The R-I converter shares a similar architecture with the R-mode, and comprises of a high gain amplifier connected in negative feedback with the current source (M_1). However, unlike the R-mode, the capacitive mode's R-I converter operates differently by connecting the negative feedback loop to a fixed resistance (R-DAC) for generating a constant current (I_{SENSE}) (6.12). This current is then copied and sourced on the capacitive sensor (C_{IN}), charging its top plate, and gradu-

ally increasing the voltage across the capacitor (V_C). The comparator simultaneously keeps a track of the voltage V_C. The comparator's output is used by the digital backend to measure the time (T_{MEAS_C}) in which V_C reaches the comparator's switching threshold (V_{TH}). Once this happens, the counter stops its operation and sets *DATA_READY* as logic high to indicate that the measurement is complete. The digital backend output (D_{OUT_C}) indicates the time taken by C_{IN} to charge to V_{TH}, and is directly proportional to the sensor's capacitance, C_{IN} (6.12)-(6.14). Following this, the switch SW is set high to fully discharge C_{IN} through M_2. The analog front-end's resolution and dynamic range are given by (6.15)-(6.16). Also, the AFE's total power consumption during operation in C-mode is computed by (6.6).

$$I_{SEN} = \frac{V_{REF}}{R_{DAC}} \tag{6.12}$$

$$T_{MEAS\_C} = \frac{C_{IN}V_{TH}}{I_{SEN}} = \frac{C_{IN}V_{TH}R_{DAC}}{V_{REF}} \tag{6.13}$$

$$D_{OUT\_C} = \frac{T_{MEAS\_C}}{T_{CLK}} \tag{6.14}$$

$$C_{LSB} = \frac{C_{IN}}{D_{OUT\_C}} \tag{6.15}$$

$$DR = 20log(\frac{C_{IN-MAX}}{C_{LSB}}) \tag{6.16}$$

Fig. 6.9 shows the simulated results of the C-mode configuration. This mode consumes total power of 10 nW to 118 nW while sensing an input capacitance of 1 pF to 101 pF with a resolution of 48 fF to 187.3 fF. A constant current (I_{SEN}) of 333 nA is generated by setting the R-DAC and V_{REF} values to 600 kΩ and 200 mV respectively. This simulation is carried out with an integrating capacitor of 300 pF and a sampling frequency of 500 Hz.

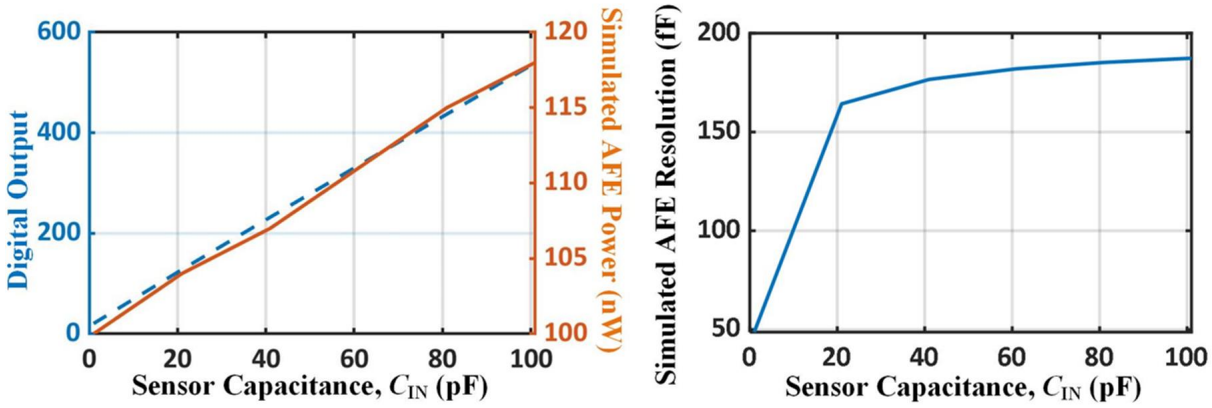

Figure 6.9: Simulated results of the C-mode configuration showing the AFE power, digital output, and resolution across a current range of 1pF to 100pF.

6.3.4.1 Dynamic range and resolution scaling. As shown by (6.12) - (6.15), the C-mode configuration's resolution can be improved by increasing the R_{DAC} value. This is because, a higher R_{DAC} value generates a lower I_{SEN}, resulting in slower charging of the sensor capacitance, C_{IN}. However, this comes at a cost of increased static power. Thus, the C-mode's performance metrics such as its resolution and dynamic range can be easily reconfigured by choosing different values of R_{DAC} at the cost of higher power. Fig. 6.10 shows the simulated results of the C-mode's resolution and dynamic range achieved by varying the $R_{DAC}$from 100 kΩ to 800 kΩ. This variation of R_{DAC} generates I_{SEN} within a range of 2 μA to 250 nA translating in a resolution tunability range of 44 fF to 873 fF for sensor capacitance values of 1pF to 100 pF. A dynamic range tunability of 41.27dB to 56.95dB is achieved for sensor capacitance of 100 pF.

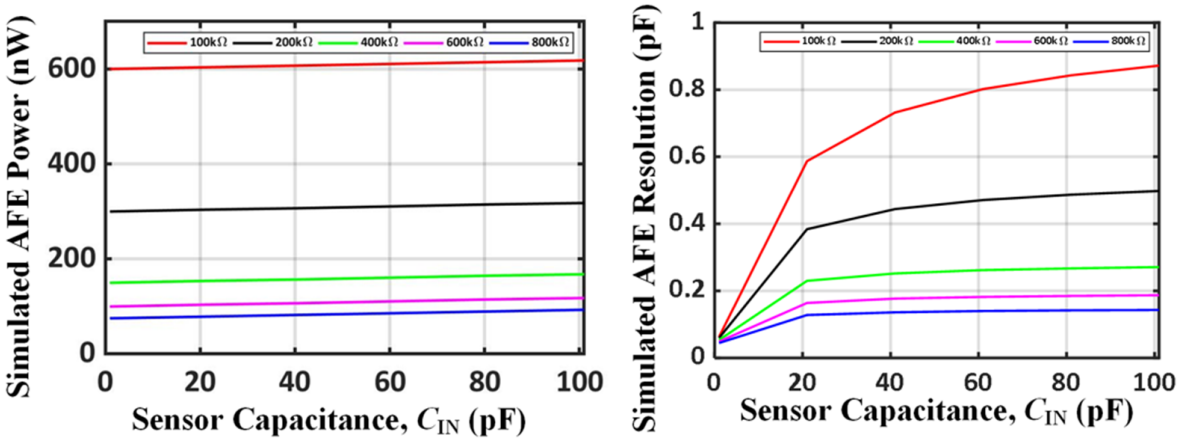

Figure 6.10: Simulated results of the C-mode configuration's tunability range for resolution (right), and resulting power consumption (left).

6.3.5 Voltage Configuration

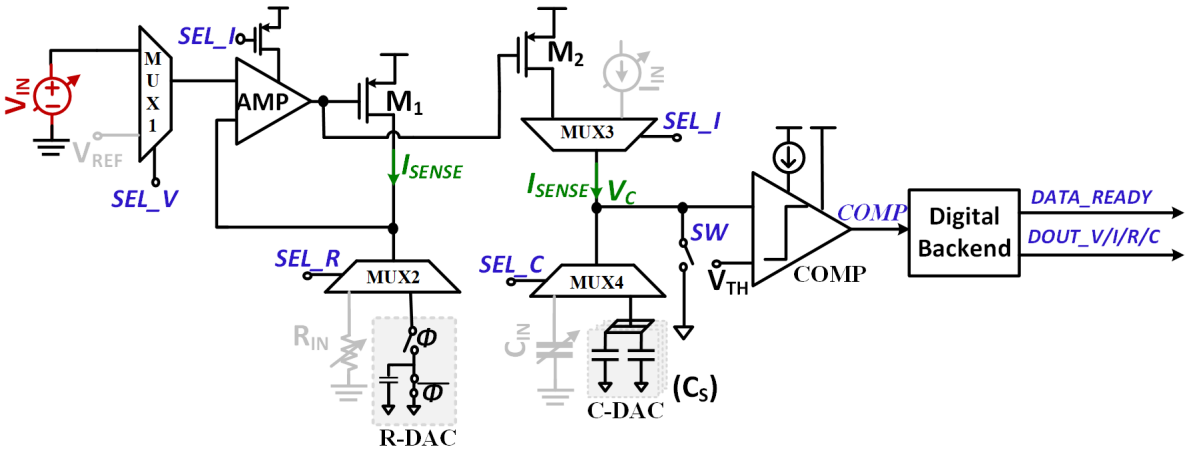

Figure 6.11: Schematic of the proposed AFE configured in V-mode.

Fig. 6.11 shows the voltage-mode (V-mode) for the single channel universal analog front-end. The voltage-to-time convertor (VTC) is implemented using voltage-to-current (V-I) converter, an integrating capacitor (C_S), the unknown sensor voltage (V_{IN}), a continuous comparator (COMP),

and associated digital backend. The AFE when in V-mode again operates in two phases namely, charge/measurement and discharge phase. The capacitor C_S's charging time (t_R) is measured to compute the sensor voltage. Similar to the other modes, the transistor M_2 serves as a constant current sink during the discharge phase.

The V-I converter comprises of a voltage controlled current source (M_1) to convert the sensor voltage (V_{IN}) into a current (I_{SENSE}) such that the voltage generated across R_{DAC} is regulated to V_{IN} (6.17). This current is further mirrored and sourced on the integrating capacitor (C_S), gradually increasing its voltage (V_C). The comparator again acts as a 1-bit slope detector and continuously tracks V_C. Meanwhile, the digital backend tracks the time during the capacitor's charging phase. Once V_C reaches the comparator's threshold voltage (V_{TH}), the digital backend stops counting, and sets *DATA_READY* as logic high to indicate the completion of measurement phase. The digital output (D_{OUT_V}) is then read through the SPI, and is proportional to the unknown sensor voltage, V_{IN} (6.17)-(6.19). Following this, the switch SW is set high to fully discharge C_S through M_2. The analog front-end's resolution and dynamic range are given by (6.20)-(6.21). The V-mode's total power consumption can be computed using (6.6).

$$I_{SEN} = \frac{V_{IN}}{R_{DAC}} \tag{6.17}$$

$$T_{MEAS\_V} = \frac{C_S V_{TH}}{I_{SEN}} = \frac{C_S V_{TH} R_{DAC}}{V_{IN}} \tag{6.18}$$

$$D_{OUT\_V} = \frac{T_{MEAS\_V}}{T_{CLK}} \tag{6.19}$$

$$V_{LSB} = \frac{V_{IN}}{D_{OUT\_V}} \tag{6.20}$$

$$DR = 20log(\frac{V_{IN-MAX}}{V_{LSB}}) \tag{6.21}$$

Fig. 6.12 shows the simulated results of the analog front-end's V-mode configuration. The simulation is setup by choosing a 400 pF integrating capacitor, and 800 kΩ R_{DAC} value. With

these values, the V-mode consumes total power of 163 nW to 332 nW, while achieving a resolution of 37.3 μV to 3.65 mV across a voltage range of 50 mV to 500 mV. A sampling frequency of 1 kHz is chosen for this simulation. The dynamic range of the V-mode with the above-mentioned C_S and R_{DAC} values is computed to be 42.72 dB-62.53 dB.

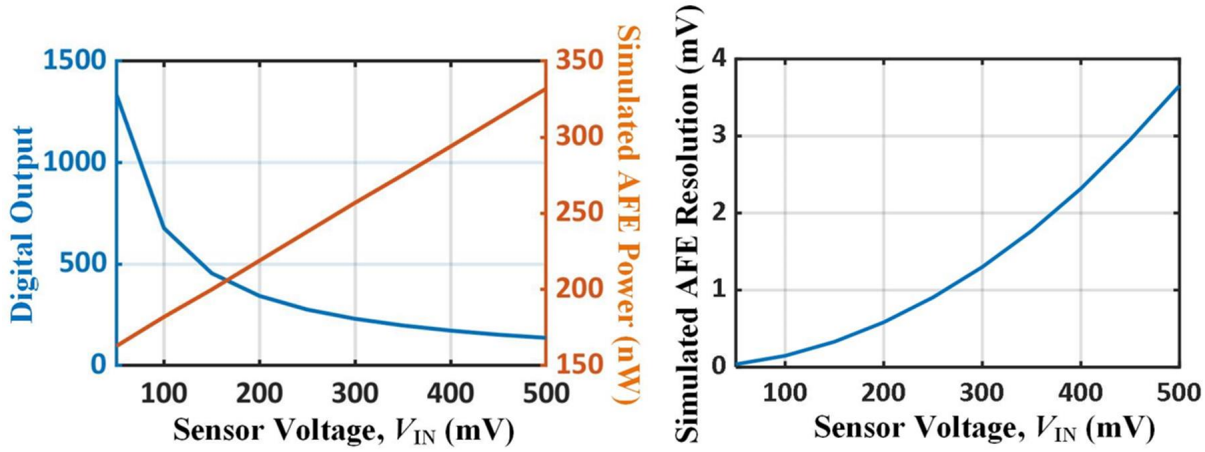

Figure 6.12: Simulated results of the V-mode configuration showing the AFE power, digital output, and resolution across a current range of 50mV to 500mV.

6.3.5.1 Dynamic range and resolution scaling. As shown by (6.17)-(6.20), the V-mode configuration's resolution can be improved by increasing either C_S or R_{DAC} values. However, this comes at a cost of increased power consumption, and might limit the maximum sampling frequency supported by the AFE. Fig. 6.13 shows the simulated results of the V-mode's resolution and dynamic range achieved by varying the C_S from 50 pF to 450 pF. This allows V-mode to tune its resolution from 33 μV to 18 mV, with total power consumption ranging from 36.8 nW to 181 nW. The dynamic range tunability of 45.43dB to 63.53dB is achieved at sensor voltage value of 50 mV.

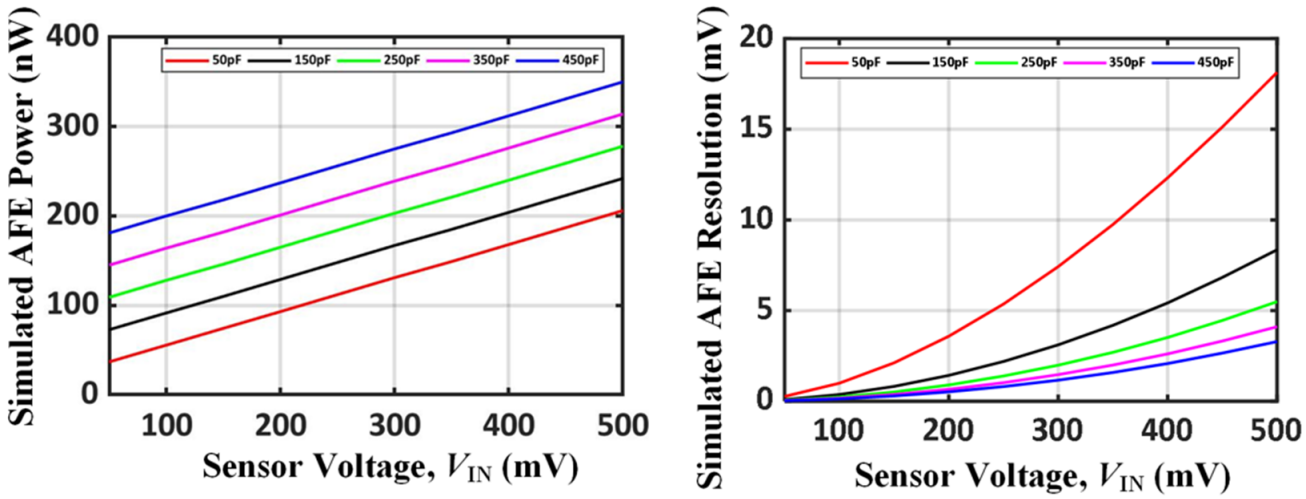

Figure 6.13: Simulated results of the V-mode configuration's tunability range for resolution (right), and resulting power consumption (left).

6.4 Conclusion and Discussion

This section presents a simulation-based design of a low-power universal analog front-end which can be configured to support voltage, current, resistive, and capacitive modalities. It adopts a time-based architecture for integration of the four modalities in a single channel. Also, by sharing a similar approach to convert V/I/R/C signals to digital outputs, it facilitates tunability of performance metrics such as resolution and dynamic range. Table VIII provides the performance summary of this work. The transistor-level design of the front-end is functionally verified using CADENCE simulations.

TABLE VIII

PERFORMANCE SUMMARY AND STATE-OF-THE-ART COMPARISON

		This work	[46] TCASI'07	[47] Sensors'19	[48] JSSC'14
Modalities		V/I/R/C	V/I/R/C	V/I/R/C	V/I/R/C
Reconfigurable Metrics		Yes	No	Yes	No
Process		65nm	500nm	250nm	350nm
Supply Voltage		0.6/1.2V	2.7/3.3V	2.5V	1.8V
C channel	***Power***	100nW–118nW	53µW	1.7mW	28.4 µW
	Input range	1pF-100pF	10fF-100pF	10pF-400pF	<41.2pF
	Resolution	48.7fF-0.18pF	1fF	N/R	N/R
V channel	***Power***	163nW-332nW	53µW	1.7mW	28.4 µW
	Input range	0.05-0.5V	0.6V-10V	0.1V-2.3V	<1.7V
	Resolution	37µV-3.6mV	60µV	N/R	N/R
I channel	***Power***	10.4nW	53µW	1.7mW	28.4 µW
	Input range	20nA-1.02µA	N/R	160nA-100µA	<7.2nA
	Resolution	3.2pA-7.3nA	N/R	N/R	N/R
R channel	***Power***	0.2 µW -3.14µW	53µW	1.7mW	28.4 µW
	Input range	20kΩ-1.06MΩ	<22kΩ	12kΩ-7.5MΩ	<18.8kΩ
	Resolution	0.79kΩ-2.31kΩ	10 Ω	N/R	N/R

Fig. 6.14 compares the proposed universal V/I/R/C analog front-end with other state-of-the-art dedicated and multi-modal sensor interfaces. As observed from the plot, most of the dedicated analog front-ends achieve high performance at the cost of higher power consumption, and sensor specificity. Also, the designs do not incorporate tunability to adjust their performance metrics. Therefore, for applications that might not require such high performance, the dedicated analog front-end's would burn unnecessary power. As shown in Fig. 6.14, the proposed work provides the much-needed performance metric tunability across all the four modalities. While this design does not provide a comprehensive range for tunability, it can be further expanded by including techniques such as baseline cancellation, digitally assisted DAC calibration etc. As observed in Fig. 6.14, the capacitive-mode's dynamic range is improved at a cost of increased latency instead

of power. This happens because in order to increase the C-mode's resolution, the capacitor's charging current needs to be decreased. As a result of this, the time taken by C_{IN} to charge increases, subsequently increasing the analog front-end's measurement latency.

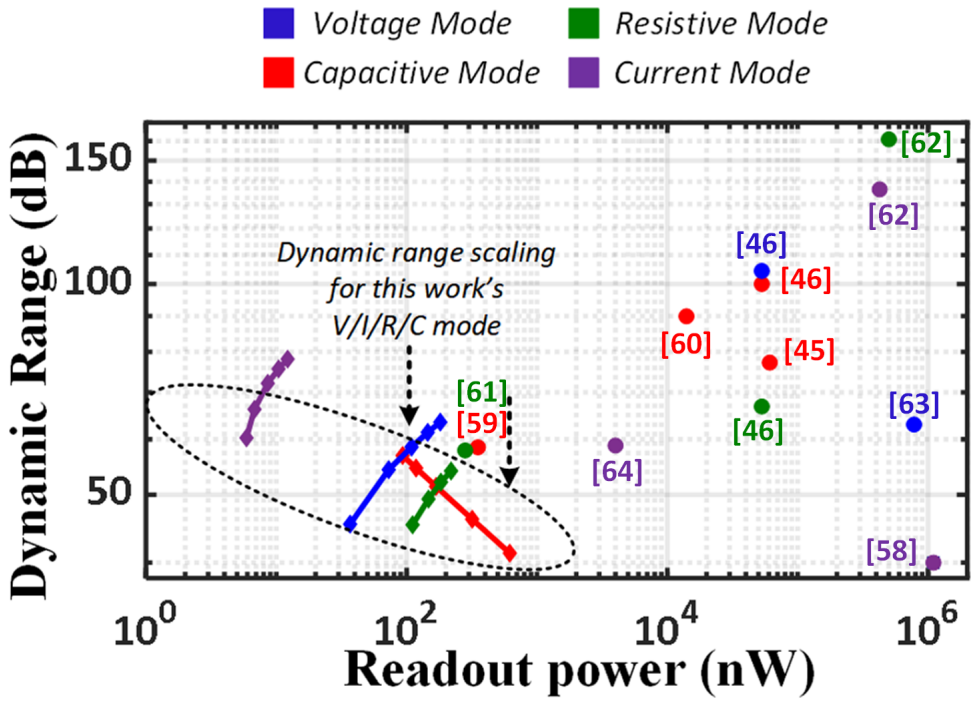

Figure 6.14: Comparison between the proposed reconfigurable V/I/R/C analog front-end with other dedicated and multimodal sensor interfaces.

A list of contributions presented in this chapter are as follows:

1. Designed the universal analog front-end and added reconfigurability to switch the single-channel AFE between V/I/R/C modes.
2. Added on-demand performance metric tunability by adding resistive- and capacitive-DACs.
3. Designed the digital-backend to providing the timing control and provide a digital output corresponding to value of the sensor's signal.

CHAPTER 7

CONCLUSION

7.1 Summary of Contributions

The contributions of this dissertation are summarized and listed according to the three research themes which cross-cut across different chapters.

7.1.1 Low Power Analog Front-end Design

This research theme aims at enabling multi-modal sensing in self-powered systems by designing low-power analog front-ends without degrading its performance.

- The first part of this research theme, presented in Chapter 2, involves the design of a sub-μW ozone analog front-end with a high dynamic range performance. By dynamically varying the sensor biasing current through the resistance range tracker, this work limits the analog front-end's input to a pre-determined voltage range. This allows the analog front-end's supply voltage to be scaled down to 0.6 V, and also optimizes the sensor biasing current power. Also, to improve the SNR performance, a chopper-stabilized differential amplifier is designed to remove the low frequency noise. This design consumes 88.6 nW of readout power, achieving a measured power reduction of 300x when compared to other state-of-the-art front-ends. The sensor biasing current adds an additional 14.2 nW to 4.54 μW of power overhead. It further

improves the power-performance tradeoff by also achieving a dynamic range of 153.27dB – 159.29dB. All of the content presented in this part is my own work.

- The second part of this research theme, presented in Chapter 3, involves the design of a multi-functional analog front-end which can detect both oxidizing and reducing gases. It uses a switched-capacitor resistor based adaptive biasing technique to make the AFE operation sensor-agnostic, and unlike GEN I, removes any dependency on the sensor's behavior. An on-chip integer-based clock divider is also designed and fabricated to aid in switched-capacitor resistor's operation. Also, digital backend is designed to aid in the AFE's working. The proposed multi-functional AFE retains sub-μW operation by consuming 57 nW of readout power while achieving a high dynamic range of 138 dB to 144 dB. Therefore, this work maintains the $>$300x readout power reduction achieved by GEN I, while delivering the required dynamic range. The sensor biasing source consumes an additional power of 28 nW to 2 μW across a sensor resistance of 20kΩ to 1MΩ. All of the content presented in this part is my own work. The 6-bit SAR ADC shown in the system figure is designed by Henry Bishop and Anjana Dissanayake.

- The final part of this research theme involves the design of a sub-μW respiration rate analog front-end, presented in Chapter 5 of this dissertation, for a custom capacitive sensor. Existing custom ICs extract respiration rate from ECG, PPG or Bio-Z leading to high readout and computational power overhead. By using a traditional switched-capacitor voltage divider to sample the sensor capacitance, and by implementing on-node respiration rate processing via a comparator and associated digital backend, the AFE is able to detect the user's inhale and exhale actions. A breath counting block is also designed and include in the digital backend to directly output the user's respiration rate. By combining the breath counting block with the readout, the proposed work is able to detect respiration rate without relying on

high-resolution ADCs. The proposed analog front-end consumes 397 nW end-to-end power, achieving 90.7x power reduction when compared to the other state-of-the-art respiration rate AFEs. All of the content presented in this part is my own work. The sensor used to validate the AFE's functionality was designed by Luis Lopez Ruiz.

7.1.2 Integration of Active Sensors and Peripheral Devices in an Energy Constrained System

Once the analog front-end power is optimized, the active sensors and their peripheral devices start dominating the system power. This research theme addresses this issue, and optimizes the system power while ensuring good performance.

- The first part of this research theme, presented in Chapter 3, involves the power-hungry UV LED illumination required by gas sensors to retain good performance. Prior works use an over-designed fixed UV LED duty cycle rate which is neither necessary nor energy efficient as the rate of sensor saturation differs with gas concentration. This work implements an intelligent alternative by designing a sensor saturation detector to predict the sensor's saturation point, and make a decision to turn on the UV LED. An on-chip driver is also designed to power the UV LED. This pushes the LED power below $31\mu W$ while maintaining good sensor performance, and achieves a power reduction of $>$5x when compared to prior works. All of the content presented in this part is my own work.

- The second part of this research theme, presented in Chapter 4, involves reducing the PPG LED power while delivering a competitive dynamic range performance. This work opts for lowering the LED current to reduce its power. Further, in order to maintain good SNR performance and low AFE power, this work implements a high-gain TIA designed at a low

supply voltage of 0.6 V. This work implements a hybrid DC current cancellation loop with both fast response time and high-resolution, to allow shorter LED on-times, and to enable TIA operation at low supply voltage by preventing it from frequent saturations. A measured readout power reduction of 37x, and system power reduction of 4-50x is achieved all while maintaining a dynamic range of 92 dB. My contributions in this part include the digitally-assisted loop of the hybrid DCOC, its accompanying components, and the associated digital backend. The TIA and analog loop of the DCOC is designed by Peng Wang.

- The final part of this research theme, presented in Chapter 5, improves the system availability of multi-modal analog front-ends while maintaining quality of information. A context-aware, event-driven control scheme is designed to detect the user's dynamically changing sensing requirements, and monitor only the relevant signs. This scheme enables indefinite operation and eliminates complete data outages through low-power always-on primary vital sign monitoring, and also provides detailed comprehensive monitoring when necessary. A measured power reduction of $>$206x is achieved for use case involving physiological and environmental co-sensing for users with respiratory distress. While, all of the content presented in this part is my own work, the ECG and PPG channels of the multi-modal analog front-end used for event-driven measurement are designed by Peng Wang.

7.1.3 Reconfigurable Analog Front-end Design

This research theme explores design of reconfigurable universal analog front-ends to make IoT sensor nodes more scalable and cost-effective for small-scale applications. This can be facilitated by minimizing the recurring design efforts and time involved in changing the sensor-specific analog front-ends to account for any changes in sensing requirements.

- This research theme's work, presented in Chapter 6, provides a conceptual look at designing low-power universal analog front-ends for voltage (V), current (I), resistive (R), and capacitive (C) modalities. Unlike the dedicated application-specific AFEs, this work adopts a time-based architecture to implement a single-channel V/I/R/C analog front-end, and adds on-demand reconfigurability to adjust the AFE's performance according to application needs. It also directly outputs the digitized V/I/R/C sensor input by using a comparator and a digital timer.A transistor-level schematic is designed and verified using CADENCE simulations. The simulation-based results are summarized in section 6.4. All of the content presented in this part is my own work.

7.2 Future Work

While the design techniques mentioned in research themes one and two are presented in respect to specific applications, they can also be used in other contexts. Furthermore, while the universal V/I/R/C AFE presented in research theme 3 is already designed to be used as a general purpose analog front-end, its architecture can be used in realizing other components as well. This section summarizes some examples of scenarios where these design techniques are applicable outside of what is covered in this dissertation.

First, the respiration rate analog front-end detects variation in the input signal around a baseline value, acting as a threshold-crossing detector. Therefore, in addition to capacitive-based respiration rate monitoring, it can also be used for monitoring available energy from a super-capacitor, as a building block for supply voltage monitors, and as low-power canary readout for coarse monitoring of capacitive sensors. Second, while the concept of limiting the sensor's output to the analog front-end's operating range is presented for gas sensing applications, it can also be used in other

applications where the analog components are designed at lower supply voltages but still need to maintain a high dynamic range. Third, since the switched-capacitor resistor (SCR) based adaptive biasing technique introduced in Chapter 3 of this dissertation makes the gas analog front-end sensor agnostic, the AFE can also be used for various other resistive sensing applications such as pressure, humidity etc. Fourth, while the SCR based adaptive biasing loop (Chapter 3) is used for sensor biasing, it can also be used as a building block for designing tunable current and voltage references. Fifth, while the hybrid DC current cancellation is currently limited to compensating the DC current residue from the photo-diode, after an increment in its current range, it can also be used for ambient light cancellation for PPG systems. Additionally, the digitally-assisted DCOC loop can be used for developing AFEs other current sensing applications involving DC inputs such as light detection, brightness control, distance measurement etc. Sixth, while this dissertation's event-driven architecture is used in context with physiological and environmental monitoring, it can also be applied towards controlling a network of sensor nodes, sensor fusion etc. Finally, the time-based universal V/I/R/C analog front-end (Chapter 6) utilizes charging/discharging of a capacitor to convert the input to digital outputs. In addition to being used towards realizing an AFE, this architecture can also be utilized for designing on-chip oscillators. However, this approach results in higher die area due to the on-chip capacitive DACs.

7.3 Open Problems

Monitoring physiological signs such as PPG-based heart rate and blood oxygenation, and respiration rate is vital to obtain critical information about user's cardiovascular and pulmonary health. However, motion artifacts generated due to the user's body movements distort these signals, and affect the heart rate, blood oxygenation and respiration rate readings. The PPG signals have always

been highly prone to body movements and might overlap with the resulting noise. Also, since the respiration rate analog front-end presented in this dissertation leverages a custom capacitive sensor, and detects the user's breathing rate on the basis of chest expansion and contraction, it also becomes very sensitive to any type of motion. Therefore, to realize a high-accuracy wearable sensing node, the analog front-ends need to incorporate motion artifact reduction techniques. Existing works have implemented various motion artifact reduction algorithms such as adaptive noise filtering, independent component analysis etc. Some designs also incorporate an accelerometer to generate a reference signal for performing motion artifact reduction. While these methods may provide higher accuracy readings, they also increase the computational power overhead. However, in absence of on-chip motion artifact reduction, these low-power sensing systems will not be able to meet consumer standards, and will remain as academic research topics. Therefore, realization of a fully deployable wearable sensing node would require further investigation into implementation of low-power motion artifact reduction techniques. Another open problem is the high-power consumption due to the pulsed heating of sensors for reducing gases like accetone. This adds several milli-watts of power overhead. Further investigation into micro- and nano-heaters is required to enable its integration in energy-constrained systems.

7.4 Publications

7.4.1 Published

1. N. Liu, R. Agarwala, A. Dissanayake, D. S. Truesdell, S. Kamineni, Xing Chen, David D. Wentzloff, and B. H. Calhoun, " A 2.5 ppm/°C 1.05 MHz Relaxation Oscillator with Dynamic Frequency-Error Compensation and 8 μs Start-up Time," ESSCIRC 2018 - IEEE

44th European Solid State Circuits Conference (ESSCIRC), Dresden, Germany, 2018, pp. 150-153 [RA1]

2. N. Liu, R. Agarwala, A. Dissanayake, D. S. Truesdell, S. Kamineni and B. H. Calhoun, "A 2.5 ppm/°C 1.05-MHz Relaxation Oscillator With Dynamic Frequency-Error Compensation and Fast Start-Up Time," in IEEE Journal of Solid-State Circuits, vol. 54, no. 7, pp. 1952-1959, July 2019 [RA2]

3. P. Wang, R. Agarwala, H. L. Bishop, A. Dissanayake and B. H. Calhoun, "A 785nW Multimodal (V/I/R) Sensor Interface IC for Ozone Pollutant Sensing and Correlated Cardiovascular Disease Monitoring," 2020 IEEE Symposium on VLSI Circuits, Honolulu, HI, USA, 2020 [RA3]

4. R. Agarwala, P. Wang, A. Tanneeru, B. Lee, V. Misra, and B. H. Calhoun, "An 88.6 nW ozone pollutant sensing interface IC with a 159 dB dynamic range," in Proc. ACM/IEEE Int. Symp. Low Power Electron. Design (ISLPED), New York, NY, USA, Aug. 2020, pp. 31–36 [RA4]

5. R. Agarwala, P. Wang, H. L. Bishop, A. Dissanayake and B. H. Calhoun, "A 0.6V 785-nW Multimodal Sensor Interface IC for Ozone Pollutant Sensing and Correlated Cardiovascular Disease Monitoring," in IEEE Journal of Solid-State Circuits [RA5]

6. R. Agarwala, P. Wang and B. H. Calhoun, "A 405nW/4.8μW Event-Driven Multi-Modal (V/I/R/C) Sensor Interface for Physiological and Environmental Co-Monitoring," 2021 IEEE Biomedical Circuits and Systems Conference (BioCAS), 2021, pp. 1-4 [RA6]

7.4.2 Submitted

1. P. Wang, R. Agarwala, Natalie B. Ownby, Xinjian Liu, and Benton H. Calhoun, “A 2.3-5.7‘W Tri-Modal Self-Adaptive Photoplethysmography Sensor Interface IC for Heart Rate, SpO2, and Pulse Transit Time Co-Monitoring”

7.4.3 Planned

1. Journal Paper on Event-driven multi-modal analog front-end

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