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Micromachined Millimeter- and Submillimeter-wave Circuits for Test and Integration

A DISSERTATION
PRESENTED TO
THE FACULTY OF THE SCHOOL OF
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Abstract

The terahertz spectrum is critical to a wide range of scientific applications, from radio astronomy to remote sensing. However, due to the cost, size and weight of terahertz systems, the terahertz frequency range remains one of the least explored and utilized regions of the electromagnetic spectrum. To reduce the size, weight and cost of terahertz components, one of the solutions is to fabricate high density integrated circuits.

Although progress has been made in the development of submillimeter-wave monolithic integrated circuits, the evaluation of these circuits still relies on test fixtures, which makes testing expensive and time consuming. A micromachined on-wafer probe covering frequencies 500-750 GHz has been demonstrated in this work to simplify submillimeter-wave integrated circuits testing.

This work also presents the design, simulation and measurement of a vertical RF interconnect with mechanical fit for three-dimensional heterogeneous integration, which is one of the major technologies for system miniaturization. The mechanical fit is a flip-chip strategy employing SU-8, an ultra-thick photoresist, to realize interlocking structures that prevent misalignment during assembly and increase the reliability of the interconnects. To determine the electromagnetic characteristics, such as insertion loss and the coupling between face-to-face chips, different test structures were fabricated and measured.

To

my parents

for

their long-term encouragement and believing in me.

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Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Submillimeter-waves Application

Submillimeter-waves, also known as terahertz radiation, refers to electromagnetic waves with wavelengths that lie between 1 mm and 100 μm or a frequency range from 300 GHz to 3 THz. Sandwiched between microwave and optical technologies, terahertz technology has some advantageous applications including imaging, material detection, astronomy *etc.*

Imaging

- Terahertz is sensitive to water concentration in tissues due to its high absorption of wafer. Cancerous tissue, which has different water concentrations compared to the healthy tissue, can be detected by submillimeter-wave imaging [7]. Submillimeter-waves have a low photon energy (0.4–40 meV) and are therefore a safe tool for hydration sensing in medical applications, including burn wound imaging and skin hydration monitoring [8].
- Submillimeter-wave radar imaging can be used to remotely uncover concealed weapons due to the ability of terahertz waves to penetrate fabrics and plastics. A personal-borne threat is unlikely to be detected by either infrared imaging, which relies on temperature differences, or lower frequency radar, which does not have sufficient resolution. [9]

Material Detection

- Intermolecular vibrations of biological materials such as crystals of amino acids and sugars result in some special peaks in terahertz spectra. These special peaks have been proposed for drugs and dangerous substances traces. [10][11]

Astronomy

- As mentioned in [12], approximately one-half of the total luminosity and 98% of the photons emitted since the Big Bang fall into the submillimeter-waves and far-IR. Terahertz astronomy provides a better understanding of the Solar System, galactic ecology and star formation through cosmic time [13].

The terahertz spectrum is critical to a wide range of applications, but due to the cost, size and weight of terahertz systems, the terahertz frequency range remains one of the least explored and utilized regions of the electromagnetic spectrum [12]. Common to the applications above and others is the critical need for greatly improved terahertz component technologies.

1.2 On-wafer Probe for Submillimeter-wave Circuits Test

To reduce the size, weight and cost of submillimeter-wave systems, one of the solutions is to fabricate high density integrated circuits. Fortunately, significant progress has recently been made in increasing the maximum frequency of operation of transistor electronics, which makes high density integrated circuits possible. For example, R. Lai *et al.* reported a sub 50nm InP high electron mobility transistor (HEMT) with f_{max} that exceeds 1.0 THz [14]. W.R. Deal *et al.* demonstrated a 480 GHz amplifier by using scaled InP transistors [15].

1.2.1 Submillimeter-wave Circuits Test

Although progress has been made in the submillimeter-wave monolithic integrated circuits (S-MMICs), the test of S-MMICs remains time-consuming and expensive because

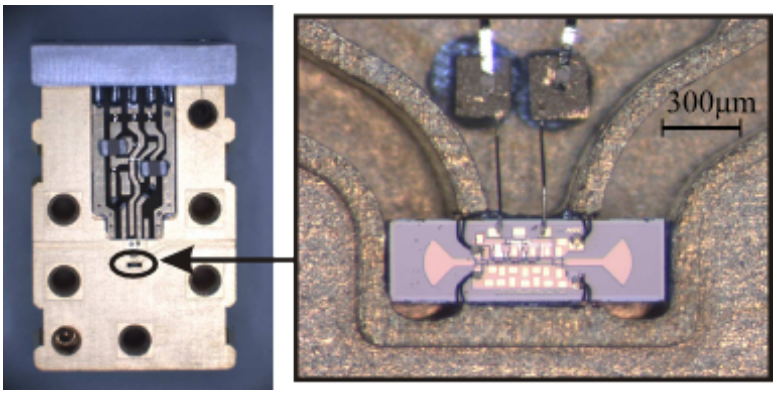


FIGURE 1.1: A typical submillimeter-wave monolithic integrated circuits test setup [1].

integrated circuits have to be assembled into a waveguide block due to the lack of on-wafer probes. A typical test setup is shown in Fig 1.1 [1]. In this setup, a submillimeter-wave amplifier with integrated waveguide transitions is mounted into a waveguide block. The integrated waveguide transitions are designed to couple the test signal between waveguide and the amplifier.

This setup can be used to estimate the gain of the device under test, but it would be difficult to obtain the scattering-parameters of the DUT. Because of the small dimensions of the waveguide at submillimeter-waves, the assembly is time-consuming (at least hours per device). The performance of the waveguide transition depends on the accuracy of the assembly, which makes it difficult to de-embed the test fixture. The testing is also destructive. Usually the S-MMICs are fixed to the block by cured epoxy. The amplifier is most likely broken when removed from the waveguide block after being mounted.

1.2.2 On-Wafer Characterization

At low frequencies (<300 GHz), on-wafer characterization is used to solve these problems. Using coplanar probes along with on-wafer calibration, on-wafer measurement can provide high-precision S-parameter measurement, better than ± 0.1 dB at 100 GHz. The advantages of on-wafer characterization at submillimeter-waves include,

- *Reducing the time and cost for terahertz circuits test*: The traditional test fixtures for terahertz circuits are complicated and expensive.

- *Creating measurement-based model*s: Modern computer-aided integrated circuit design, which significantly reduces the design time, relies on accurate models of each element. By eliminating the test fixtures, the measurement reference plane can be set right next to the devices under test (DUT). Therefore the calibrated on-wafer measurements can get accurate device measurements to create measurement-based circuit models.
- *Sorting the die by performance*: Due to the variations in materials and fabrication processes, the performance of integrated circuits varies over wafers and different corners on the same wafer. An accurate and repeatable test system can sort the individual die into performance categories.

Calibrated on-wafer characterization is critical to the development of terahertz high density integrated circuits, however coplanar on-wafer probes are absent above 325 GHz [16]. Part-I of this thesis focuses on the development of an on-wafer probe for the frequency range 500 to 750 GHz based on a microfabrication process developed at the University of Virginia.

1.3 Vertical RF Transition for Three-Dimensional Heterogeneous Integration

1.3.1 Introduction

System miniaturization technology is one primary driver of the information age. System miniaturization leads to smaller size, higher mobility, higher performance, lower cost, higher reliability, and higher functionality. In the past decades, different technologies have been developed to miniaturize systems. As listed in [17], major technologies include,

1. System on Board: Discrete components connect directly to a system board.
2. Multichip Module (MCM): Two or more integrated circuits are packaged horizontally.
3. System on Chip (SOC): A system with two or more functions is integrated on a single chip.

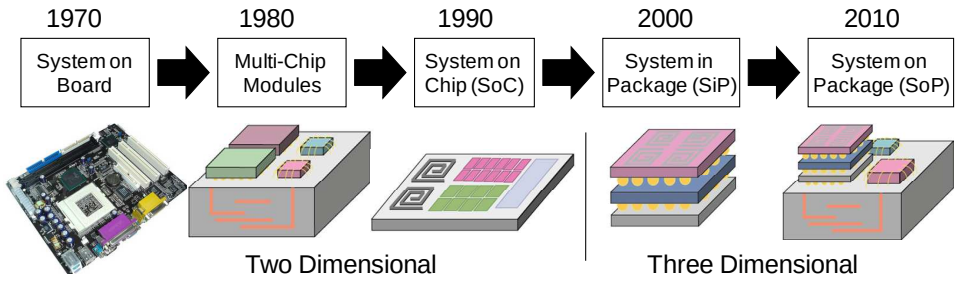


FIGURE 1.2: Evolution of system integration [2].

TABLE 1.1: A comparison of different system integration technologies.

Technologies	Pros	Cons
System-On-Board	Short market time	Low Integration Density
Multichip Module	Compatible with heterogeneous technologies	Moderate Density
System-On-Chip	Smallest size, High repeatability	Long Design/Test Time
System in Package	Compatible with heterogeneous technologies, Short vertical interconnectors	Thermal dissipation
System on Package	Compatible with heterogeneous technologies, Short vertical interconnectors, High Q passives	Thermal dissipation

4. System in Package (SIP): Two or more chips are stacked in a single package.
5. System on Package (SOP): Previous integration schemes are combined.

A summary of these technologies above is shown in Fig. 1.2 [2] and Table. 1.1. SOC leads to the most compact, light-weight systems that can be mass-produced, but since all the components are integrated within the same technology, for example, CMOS, some components may be not realized in the optimal technologies. And the long design/test-time limits SOC's applications. On the other hand, MCM, SIP, SOP are compatible with heterogeneous integration technologies. In heterogeneous integration, each component can use optimized technology and each functional block can be designed and tested separately. However, SIP and SOP are significantly different from MCM. MCM is two-dimensional; meanwhile SIP and SOP utilize the third-dimension by using short vertical interconnectors to connect vertically stacked chips.

Standard silicon technologies provide low cost components, but their performances are limited by the finite resistivity of the silicon substrate. Silicon germanium (SiGe), gallium arsenide (GaAs), and indium phosphide (InP) technologies can provide high quality factor (Q), high performance components, but their cost is relatively high. The

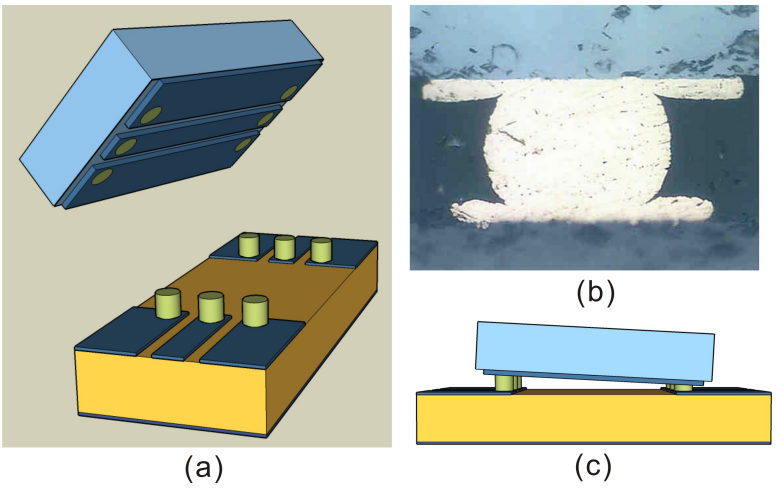


FIGURE 1.3: (a) A simple RF flip-chip integration; (b) A deformed gold bump after thermocompression bonding (cross-sectional view)[3]; (c) A flip-chip integration with one side compressed more than the other.

integration of high performance GaAs/SiGe/InP devices with low cost silicon devices would significantly improve the system performance while remaining relatively low cost.

The flip-chip based millimeter-wave interconnect is an increasingly popular technology for millimeter-wave heterogeneous integration. Due to its small dimensions, the flip-chip interconnect is attractive for high-performance, high-frequency and broadband applications [18].

1.3.2 Flip-chip Based Vertical RF Transition

The flip-chip scheme is demonstrated in Fig. 1.3(a). A MMIC die is mounted upside down on a carrier substrate by using metallic bumps as interconnects. The flip-chip technology was initially developed for low-frequency digital circuit integration. When adopting this technology to millimeter and submillimeter-wave circuit integration, we face several challenges:

- *Bump diameter and pitch have to be shrunk*: The diameter of a typical bump for digital integration is 100-200 μm. The launch pitch of a 300 GHz amplifier is 60 μm [19]. At even higher frequency, the launch pitch should be smaller to minimize the parasitic.
- *Higher placement accuracy is required*: Two major bumps, solder bumps and gold bumps, are used. The solder bumps are heated and melt to bond the die and the

substrate. The surface tension of the melted bumps can center the connections during the soldering, which provides self-alignment. For gold bumps, the die and the substrate are bonded by thermocompression. Since this process is not self centering, placement accuracy is critical. Gold bumps, which have higher thermal conductivity than solder bumps [3], are required for high power applications. When gold bumps are used in millimeter and submillimeter-wave applications, their small bump diameters and pitches require high placement accuracy.

- *The metallic bumps deform during thermocompression bonding*: Fig. 1.3(b) shows the cross-sectional view of a gold bump after thermocompression bonding [3]. If the bonding or soldering process is not well controlled, some bumps could be lower than the others, as shown in Fig. 1.3(c). For RF circuits, this may result in change in the characteristic impedance of transmission lines, which will cause high VSWR at the interconnection.
- *Characteristic impedance changes*: Due to the proximity of the substrate, the characteristic impedance, Z_0, of the CPW lines or microstrip lines changes, which changes the performance of the circuits and may cause the whole system to fail. To avoid this interaction, the minimal separation between two face-to-face chips should be no less than 0.3 times the CPW ground-to-ground spacing [20]. For the microstrip circuits, two chips need to be separated farther apart, due to the field distribution of microstrip. Therefore millimeter-wave and submillimeter-wave circuit integration requires high aspect ratio micro-bumps (>1:1). However, most solder bumps have aspect ration less than 1:2.
- *The underfill in flip-chip may change the performance of the RF circuits*: Usually an electrically-insulating adhesive, "underfill", is used to fill the under-chip space in order to provide additional mechanical strength. [21] demonstrates a twelve times mechanical strength improvement by applying underfill. However, the underfill will introduce extra loss [22] and detune RF circuits.

These factors indicate the need to develop innovative technologies.

1.4 Summary

This chapter demonstrates the urgent need to develop measurement and integration techniques for submillimeter-wave integrated circuits. Part I of this thesis focuses on the development of an on-wafer probe for the frequency range from 500 to 750 GHz. The on-wafer probe is based on a micro-fabrication process developed at the University of Virginia. This work will detail the design, simulation, and measurement of on-wafer probes at 500 to 750 GHz.

The flip-chip based millimeter-wave inter-chip interconnect is an increasingly popular transition configuration. This chapter identifies several challenges to be faced when adopting this technology to millimeter and submillimeter-wave circuit integration. Part II of this thesis presents the design, simulation and measurement of a vertical RF interconnect with mechanical fit for three-dimensional heterogeneous integration. The mechanical fit is a flip-chip strategy employing SU-8, an ultra-thick photoresist, to realize interlocking structures that prevent misalignment during assembly and increase the reliability of the interconnects.

Part I

Micromachined Submillimeter-wave On-wafer Probe

Chapter 2

Micromachined Probe Design

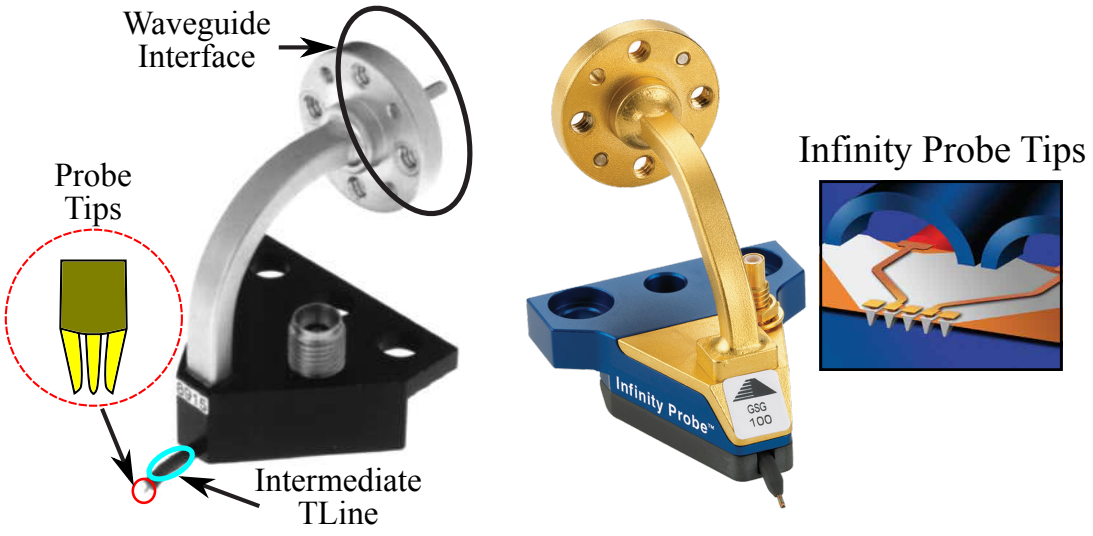
The beginning of this chapter reviews current commercially available millimeter-wave on-wafer probes. Techniques associated with these commercial probes prevent them from scaling to submillimeter-wave frequency range. This chapter then introduces a micromachined on-wafer probe for reliable probing at submillimeter-waves. The second part of this chapter details the mechanical design of the micromachined probe.

2.1 Introduction

2.1.1 Millimeter-wave Probes

Today, the primary manufacturers of millimeter-wave on-wafer probes are *Cascade Microtech* and *GGB Industries*. Probes for millimeter-wave on-wafer measurement from these two companies are similar. Fig. 2.1(a) shows a probe, Model 120, from *GGB Industries* with coplanar GSG (Ground-Signal-Ground) probe tips. This probe is designed for W-band on-wafer measurement, covering the frequency band, 75–120 GHz. Fig. 2.1(b) shows an on-wafer probe and *Infinity*® GSGSG probe tips from *Cascade Microtech*.

As shown in Fig. 2.1 (a), a millimeter-wave on-wafer probe mainly includes three



(a) (b)

FIGURE 2.1: (*a*) On-wafer probe from *GGB Industries*, Model 120 [4]; (b) *Cascade Microtech* on-wafer probe, Model i110-S-GSG-100-BT and *Infinity* probe tips (GSGSG)[5].

parts: a waveguide connection, an intermediate transmission line and coplanar waveguide probe tips. Generally, test equipment for frequencies greater than 50 GHz has rectangular waveguide interfaces, therefore on-wafer probes are required to have a flange interface for correct connection. Rectangular waveguide is used at these frequencies because of its low loss, however it is bulky. To provide good vision of the probe tips during positioning, an intermediate transmission line section is necessary. As shown in Fig. 2.1(a), a piece of coaxial line, 5 mils in diameter [4], is used to couple the signal from the waveguide to the GSG probe tips. The probe from *Cascade Microtech* uses a similar structure, as shown in Fig. 2.1(b).

The main difference between these two on-wafer probes is the coplanar probe tips, which are the most critical parts of an on-wafer probe. GGB probe tips are formed by adding ground pins to the coaxial line. This design requires hand assembly, which limits the capability to scale current designs for sub-millimeter-wave frequencies, because the dimensions of the probe tips have to be decreased as the operating frequency increases. Hand-assembled probe tips are unlikely to provide reliable on-wafer probing above 500 GHz. On the other hand, *Infinity*® probe tips made by *Cascade Microtech* are fabricated on a thin film of polyimide, as shown in Fig 2.1(b). Since this design relies on microfabrication techniques to define the probe tip dimensions, it has potential for

submillimeter-wave operation. However the probe tips are fabricated separately from other parts of the probe, which requires precise assembly to connect the probe tips to the intermediate transmission line.

Although both of these companies have recently released probes capable of operating at 330 GHz, probes above 500 GHz are generally unavailable due to the reasons stated above. A micromachined probe, based on a microfabrication process developed at the University of Virginia, was proposed for reliable on-wafer probing at frequencies from 100 GHz to 1 THz based on electromagnetic field simulation.

2.1.2 Micromachined submillimeter-wave probes

A micromachined probe mainly includes two parts: a microfabricated probe chip and a metal-machined block, as shown in Fig. 2.2. The probe chip is a passive circuit based on earlier work at the University of Virginia with ultra-thin silicon and Au beamlead fabrication processes for heterodyne detectors [23]. The metal-machined block is an *E*-plane split waveguide block, which provides a waveguide connection as well as housing for the probe chip. As shown in Fig. 2.2, recesses are milled into the waveguide block to accommodate the probe chip. When two halves of the waveguide block are brought together, the probe chip is clamped in the block.

A long waveguide section is milled into the metal block to connect the test equipment to the probe chip. The probe chip, once clamped in the block, extends beyond the metal housing to contact the device under test (DUT). This extended part also provides visual guide for probe positioning. Because probe tips are fabricated on this probe chip by microfabrication, micron accuracy can be achieved with ease, which makes this design suitable for submillimeter-wave on-wafer probing.

An important feature of this design is the simple, self-aligning mounting process of the probe chip, which does not require any adhesives. Recesses are milled into the waveguide block with a precision of ± 3 μm. The probe chip extents are defined by microfabrication, which has a better than ± 2 μm precision. The probe chip drops into these recesses and is subsequently aligned to the block to a better than ± 5 μm precision. Due to its high precision, this design has potential to work up to at least 750 GHz. How

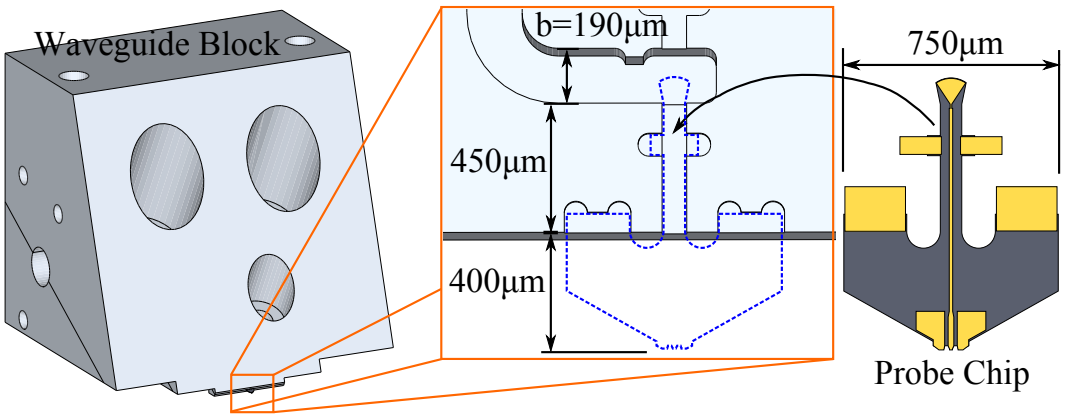


FIGURE 2.2: WR-1.5 waveguide micromachined terahertz probe. Recesses are used to align the probe chip to the waveguide block. Port-I: Waveguide connection; Port-II: CPW probe tips. b=190 μm, is half of the waveguide (WR-1.5) width a.

this tolerance affects the probe's RF performance will be discussed in Section 3.1.4 after the RF design details are introduced.

2.2 Mechanical Design

Before we get into the electromagnetic details of the micromachined probes, it is important to show how the probe is connected to the test equipment and how the probe works mechanically.

2.2.1 Probe Chip Angle

As shown in Fig. 2.3, the probe chip extends a length, l, beyond the waveguide block at an angle, θ, to contact the substrate. This probe chip must be long enough to extend beyond the block, so that the probe tips contact the substrate before the waveguide block. Also the probe chip has to be long enough to extend beyond the block to be visible in a microscope looking down from above the substrate, to provide a visual guide for positioning.

For the probe chip to contact the substrate before the waveguide block, the length, l, is influenced by the probe angle, θ, as well as the minimum required block thickness, t, as shown in Fig. 2.3. l has to be at least $t/sin\theta$.

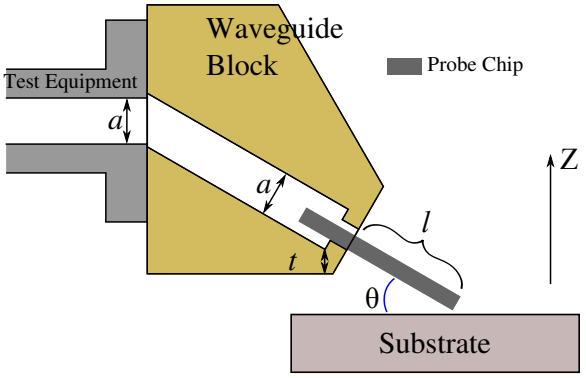


FIGURE 2.3: Side view of a micromachined probe connecting to test equipment. Dimension a is the rectangular waveguide width.

Overdrive is the additional Z-direction motion of the probe block beyond initial contact of the probe tip with the DUT. Overdrive is applied to cause the probe tips to move along the surface of the test pad and thereby break through surface contamination and roughness to ensure a low resistance contact. The maximum Z-direction motion the probe can achieve before the bottom of the probe block contacts the DUT is,

$$d_{max} = l \cdot sin\theta - t \tag{2.1}$$

assuming the probe chip will not break during the contact.

The probe angle, θ, impacts the coupling between the probe and the device under test. Simulations of the probe at different angles to the substrate show that angles greater than 30° increasingly direct energy into substrate modes rather than into the DUT [24].

The probe angle also impacts the connection between the probe and test equipment. As shown in Fig. 2.3, the rectangular waveguide inside the block is inline with the probe chip to simplify the metal machining, which results in a bend at the waveguide interface. Simulation results of this waveguide bend at different angles are shown in Fig. 2.4. Better return loss is achieved with lower angles and 30° results in a better than 25 dB return loss over WR-1.5 waveguide operating frequencies, 500–750 GHz. A 15 dB return loss is a practical goal for the on-wafer probe design. A better than 25 dB return loss can ensure the discontinuity caused by this waveguide bend does not impact other parts of the probe design. The minimum block thickness for the metal-machining technique used

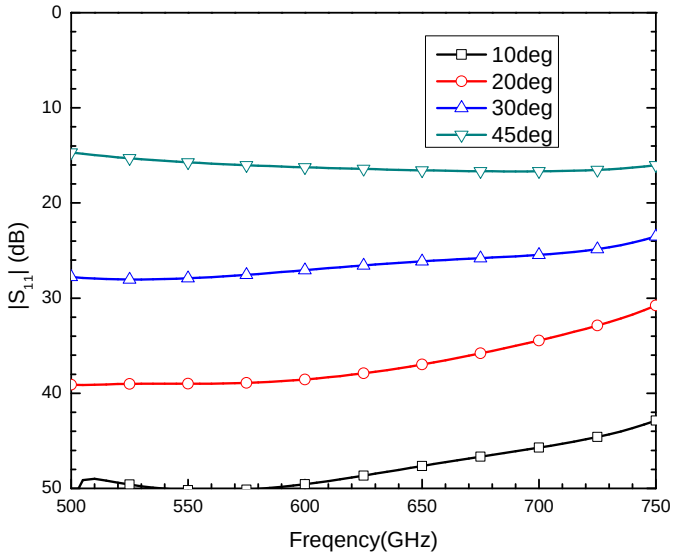


FIGURE 2.4: Return loss of the waveguide bend with different probe angle.

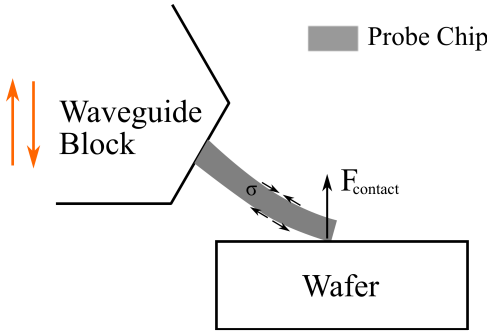


FIGURE 2.5: Side view of the wafer probe as it contacts the device substrate. As the probe is lowered onto the substrate, a stress is introduced into the probe chip as a reaction to the force, $F_{contact}$, applied to the substrate.

to make the waveguide blocks in this thesis is 50 μm. With a desired d_{max} of 150 μm, the resulting probe chip extension outside the block is 400 μm.

2.2.2 Beam Design

Fig. 2.5 illustrates the mechanics of wafer probing. As the probe makes contact, the probe chip deflects and generates a force at the contact point. The amount of force the probe chip generates depends on the material properties, the dimensions of the probe chip, as well as the probe angle.

To enable biasing and reduce insertion loss, the probe must provide enough force to create a low resistance contact with test pads on the DUT. Commercial probes are stated to have contact resistances at or below 0.1 Ω [25]. Based on microactuator

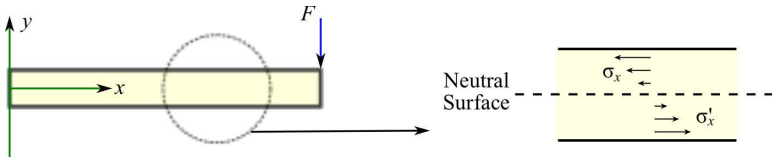


FIGURE 2.6: Side view of a cantilever beam undergoing a simply point-load F and the distribution of stress within the beam. The neutral surface is the plane of zero stress through the beam.

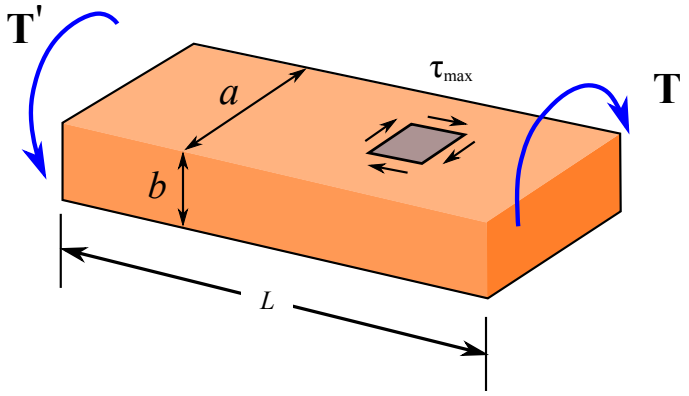


FIGURE 2.7: Model for a silicon beam under a torsional loading, $\boldsymbol{T}$.

measurements, it is expected that at least 0.2 mN of force per tip between the probe and the device are needed to achieve this contact resistance for gold to gold contact [26].

To meet the force requirements, different probe chip materials and geometry are analyzed in [24]. This section uses a simple analytic model of a cantilever beam to show the trade-offs involved in meeting the mechanical requirements.

The classical cantilever model is used in this analysis since it captures the behavior of a beam under a load with one end rigidly fixed [27]. Fig. 2.6 shows the side view of a cantilever beam undergoing a simple point-load, $\boldsymbol{F}$, and the distribution of stress within the beam.

The end of the cantilever beam deflects as the force load is applied. If the deflection is small, this mechanical behavior can be modeled using a linear spring constant, k (N/m), which can be expressed as [27],

$$k = \frac{1}{4} E a (\frac{b}{L})^3 \tag{2.2}$$

where E is the elastic modulus and L, a, b are the dimensions of the beam, as shown in Fig. 2.7. If the silicon beam remains linear until it reaches its maximum allowed

displacement, the maximum force generated can be calculated by,

$$F_{max} = k \cdot d_{max}$$

where d_{max} is the maximum allowed displacement.

Through the cross section, the stress varies linearly and can be expressed as [27],

$$\sigma_x(x) = \frac{F(L-x)b}{2I}$$

where I is the moment of inertia of the beam's cross section, and for the rectangular cross section:

$$I = \frac{1}{12}ab^3$$

When $x = 0$,

$$\sigma_x(0) = \sigma_x^{max} = \frac{6FL}{ab^2}.$$

The silicon beam will permanently deform under a stress greater than the yield strength of silicon, σ^{yeild}. By setting $\sigma_x^{max} = \sigma^{yeild}$, we can solve for the maximum force the beam can withstand at the point of failure:

$$F_{max} = \frac{ab^2}{6L}\sigma^{yeild}$$

Suppose we have beams of three different thickness: 5, 10, and 15 μm and the width of the silicon beam, a, equals to 100 μm. The maximum force that can be achieved by the probe chip is limited by either the maximum allowed displacement or the yield strength. The maximum allowed displacement is assumed to equal the maximum over-drive calculated by Eq. (2.1). The maximum force changing with the length of the silicon beam is shown in Fig. 2.8. For the 15 μm thick silicon cantilever beam, the maximum force is first limited by the yield strength and as the length of the cantilever beam increases, the maximum force is limited by the maximum over-drive. For 5 and 10 μm thick silicon beams, the maximum force is determined by the maximum over-drive. Thicker beams can generate much more force with the same beam length due to the square-dependence on beam thickness. The material properties used in the calculation

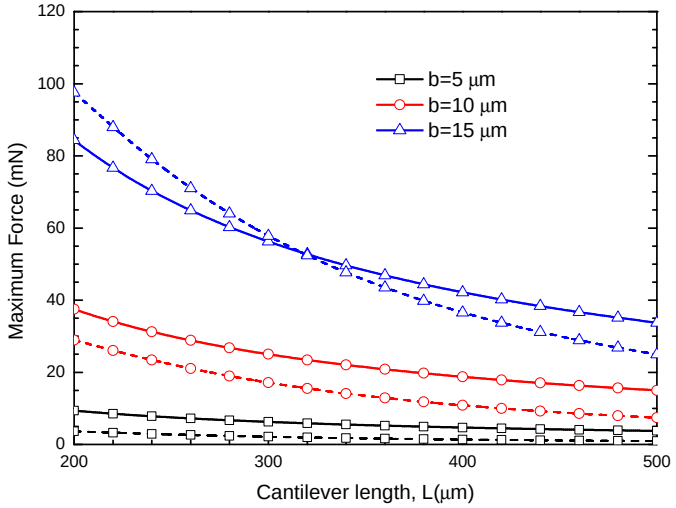


FIGURE 2.8: Maximum force the silicon cantilever can achieve with a width of $a = 100$ μm. Solid line: limited by yield strength; dash line: limited by maximum over-drive.

are listed in Table 2.1.

In reality, the probe tip may not be parallel to the substrate, which requires extra contact force to compensate this tilt. When one probe tip contacts the substrate before the other tips, the contact force at this probe tip will introduce a torque to twist the probe chip until all three probe tips (GSG) contact the substrate at the same time. A rectangular cross section bar subjected to a torsional loading, $\boldsymbol{T}$, is used to model the behavior of the probe chip under this scenario, as shown in Fig. 2.7.

The maximum shear stress occurs along the center lines of the wider face of the bar and is equal to [27]

$$\tau_{max} = \frac{\mathbf{T}}{c_1 a b^2}$$

and the angle of twist can be expressed as

$$\Phi = \frac{\mathbf{T} L}{c_2 a b^3 G} \tag{2.3}$$

where G is the shear modulus of elasticity. The coefficients c_1 and c_2 depend only upon the ration a/b. For $a/b \geqslant 5$, as is the case for the probe chip, the coefficients c_1 and c_2 are equal, and can be expressed as

$$c_1 = c_2 = \frac{1}{3}(1 - 0.630b/a)$$

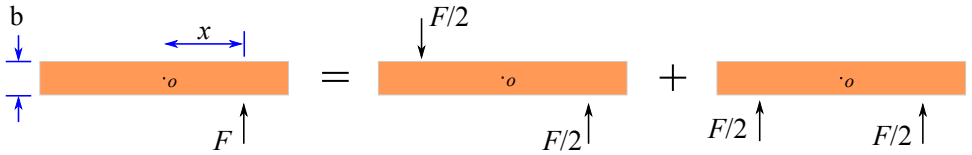


FIGURE 2.9: A cross-sectional view of a silicon beam under a point force loading and its equalized loadings.

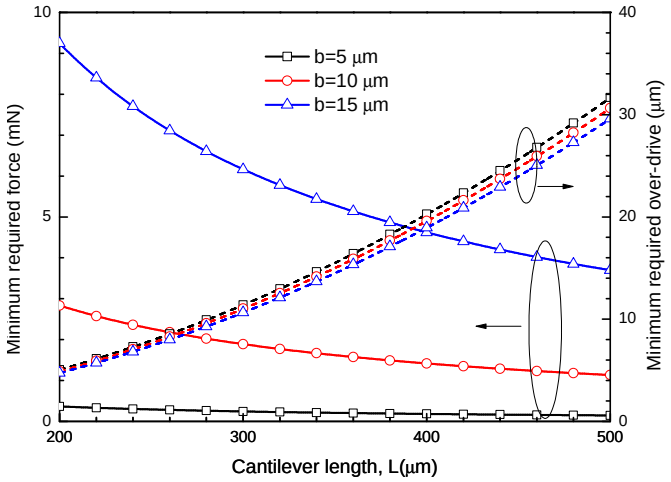


FIGURE 2.10: Minimum force and minimum over-drive required to overcome 1° tilt, for a silicon cantilever with width $a = 100$ μm.

TABLE 2.1: Material properties of Silicon. E is the elastic modulus, σ^{yeild} is the yield strength and G is the shear modulus.

Material	Si
E (GPa)	185
σ^{yield} (MPa)	4500
G (GPa)	52

When a force, $\boldsymbol{F}$, is applied to one corner of the beam, this load can equal to a torsional loading, $\boldsymbol{T}$, and two forces loading, as shown in Fig. 2.9. The torsional loading, $\boldsymbol{T}$, can be calculated by,

$$\mathbf{T} = 2 \cdot \frac{\mathbf{F}}{2} \cdot x = \mathbf{F} \cdot x$$

To overcome a 1° tilt, the minimum required force can be calculated by the reverse of Eq. (2.3) and the minimum required over-drive can be obtained using Eq. (2.2). The analysis results for three different thick silicon beams with width, a, of 100 μm are shown in Fig. 2.10. Thicker silicon beams require larger force, but the minimum required over-drive only changes slightly with beam thickness.

It should be noted that this analysis assumes the force presented is perpendicular to the beam. As shown in Fig. 2.5, this is clearly not the case since the probe approaches the probed substrate at an angle. The full model can be simulated in ANSYS. This simple model confirms our intuition that a thicker silicon beam can generate more force and a longer silicon beam has a lower spring constant. However, to overcome the same tilt, the required over-drive changes only slightly with the thickness of the silicon beam.

The final shape of the probe is guided by two goals. First, the geometry of the probe must reduce the concentration of stress induced into the probe by the contact force. The maximum stress induced under the required contact force must not exceed the yield strength of silicon, 4.5 GPa. Second, the mechanical design must allow for a transmission line to connect the waveguide to the probed substrate. Therefore the probe is designed to be 750 μm wide to support a transmission line while allowing sufficient area for the silicon to be clamped to the housing in a region that is far from the electromagnetically active portion of the probe, as shown in Fig. 2.11. Fillets are used adjacent to the clamped areas to avoid high stress concentrations in the probe. The final shape of the probe was designed by T. Reck by focusing on the maximum achievable contact force [24].

From Eq. (2.2), increasing the width of the silicon beam, a, increases the spring constant of the silicon and increases the contact force for the same displacement. However, from Eq. (2.3), increasing the width of the silicon beam, a, reduces the angle of twist for the same torsional load. Therefore, when the final shape is designed, the trade-off has to be made to ensure that the probe can generate enough contact force and that the probe requires reasonable displacement to overcome tilt.

The spring constant and the angle of twist can be calculated either by the analytic model or by simulation in ANSYS. The results are shown in Table 2.2. When the analytic model are used, $a = 750$ μm, $b = 15$ μm and $l = 400$ μm. When the probe is simulated in ANSYS, the dimensions used are shown in Fig. 2.11. The clamped areas are set to be fixed and point loads are applied to the probe tips. The analytic model is oversimplified, but the calculated results are of the same order as the simulation results.

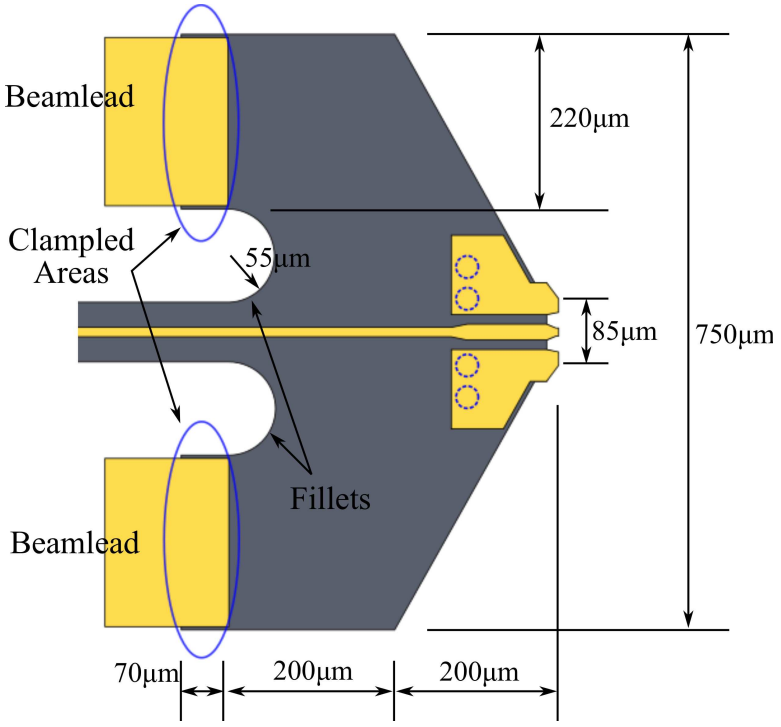


FIGURE 2.11: Top view of the probe tip indicating the clamped area and relevant dimensions.

TABLE 2.2: Mechanical properties of probe for a 15 μm thick silicon beam

	Analytical	Simulated in ANSYS
Spring constant	1.83 mN/μm	0.56 mN/μm
Angle of twist	0.53 degree/μJ	1.39 degree/μJ

2.3 Mechanical Properties Characterization

As shown in Fig. 2.5, when the probe contacts the test wafer, the silicon deflects and generates a force at the contact. The force induced by the probe with respect to the vertical distance the probe traveled can be modeled as a linear spring, with spring constant K_1.

For the WR-1.5 micromachined probe, a setup shown in Fig. 2.12 is used to measure the spring constant, K_1. A test wafer is attached to a load cell (Futek® FSH0234) that is used to monitor the contact force. A motor-driven stage is used to move the test wafer. As the stage rises, the silicon chip contacts with the wafer and generates force at the contact that is measured by the load cell. During this process, the load cell also deflects and can be modeled as another linear spring, with constant K_2. This setup is therefore a series connected two-spring system.

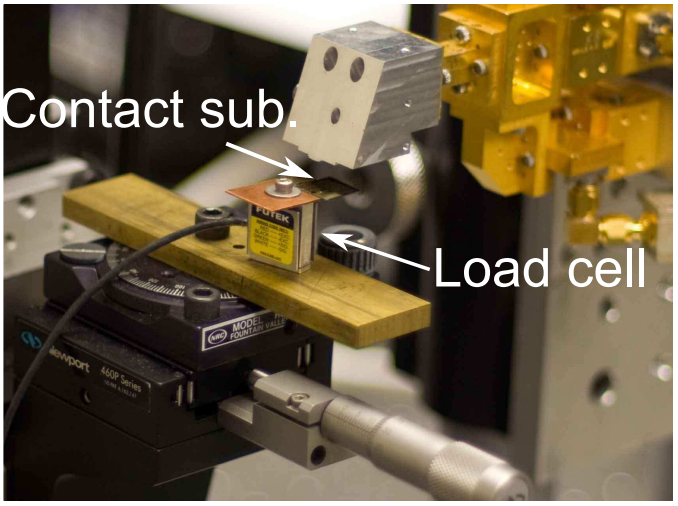


FIGURE 2.12: Measurement setup for probe spring constant.

Measuring the contact force with respect to the vertical motion of the stage gives the total spring constant, K_{total}. A linear regression of the measured results are shown in Fig. 2.13 and give $K_{total} = 0.40 \pm 0.02$ mN/μm.

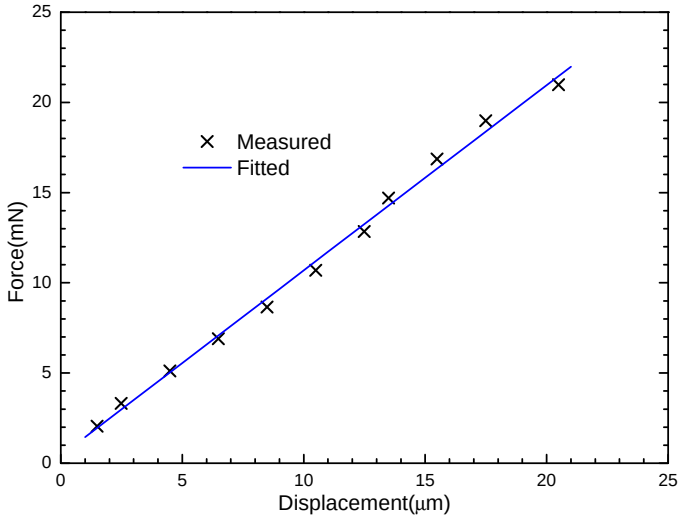
For the series connected two-spring system,

$$\frac{1}{K_{total}} = \frac{1}{K_1} + \frac{1}{K_2}.$$

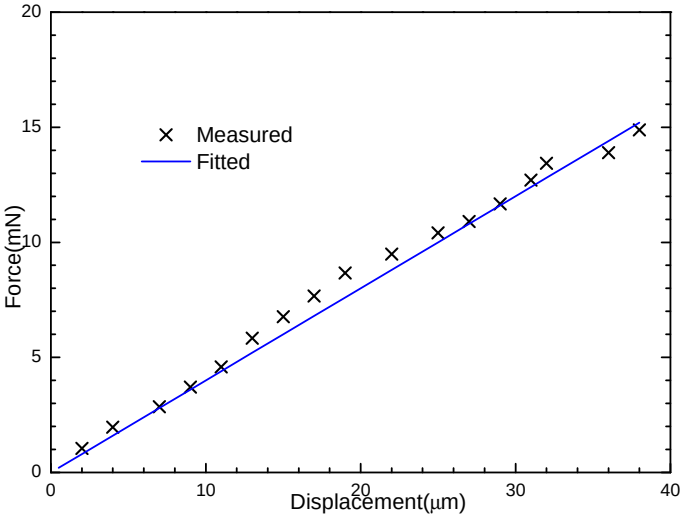
The spring constant of the load cell, K_2, is independently measured, using a similar setup, to be 1.07 ± 0.07 mN/μm. Therefore, the spring constant of the probe is determined to be, $K_1 = 0.65 \pm 0.08$ mN/μm. This measurement result is close to the ANSYS simulation result, 0.56 mN/μm.

Previous measurements have shown that a micromachined silicon chip achieves a low contact resistance of 0.07 Ω at 1 mN per tip [28]. However, compensation higher contact force (>3 mN) may be required to ensure that all three tips on the GSG probe simultaneously contact to the CPW probing pads with low resistance, given possible non-planarity of the probe with the DUT.

To measure how the tilt affect the required contact force, a DC measurement is conducted, shown in Fig. 2.13. This measurement setup is similar to Fig. 2.12. The probe is fixed to a rotary stage, Newport® Model 481-A, which is used to adjust the tilt. DC contact pads, shown in Fig. 2.14, are attached to a loadcell that is used to monitor



(a)



(b)

FIGURE 2.13: Mechanical test results of the micromachined probe using the setup shown in Fig. 3.27. Contact force vs. vertical motion of the stage. (a) The measurement of K_2; (b) The measurement of K_{total}.

the contact force. R_1 and R_2, are the resistances between the probe ground and the contact pads, G_1 and G_2 respectively. $R_1$and R_2 are measured by two independent multimeter(Keithley Model 2000 DMM). As the motor-driven stage moves toward to the probe, the contact pads are brought to contact with the probe tips. During this process, these two resistances are measured, while the contact force is monitored by the loadcell.

The measurement results are shown in Fig. 2.15. As shown in Fig. 2.15 (a), when the probe contacts with the contact pad, G_2, the resistance, R_2, changes from infinity

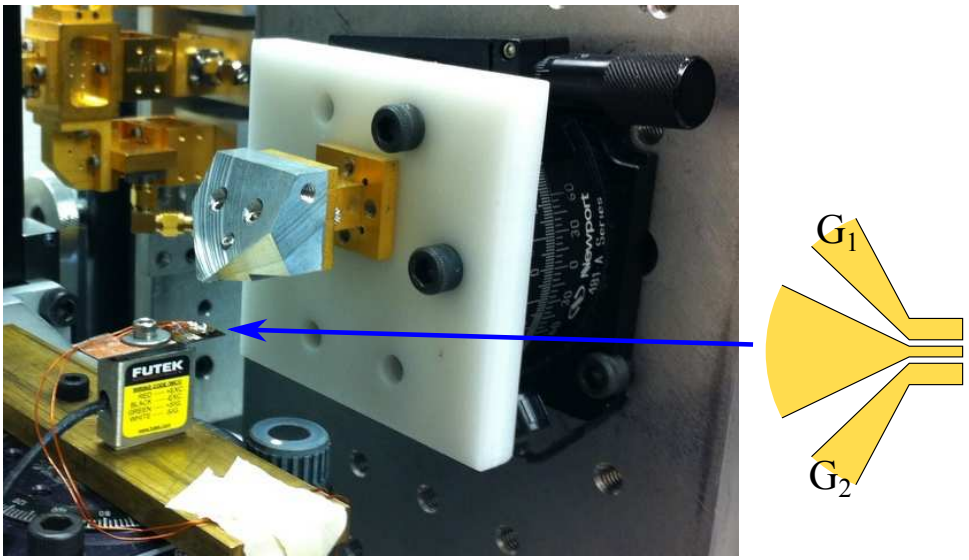


FIGURE 2.14: Measurement setup for required contact force vs. tilt.

to ∼15 Ω and as the contact force increases, R_2 remains ∼15 Ω. This resistance is due to the connections and wires used in this DC measurement. To get an accurate contact resistance measurement, Kelvin (4-wire) resistance measurement can be used. [24] shows a low contact resistance of 0.07 Ω is achieved at 1 mN contact force. Upon the initial contact with G_2, R_1 is seen to change from infinity to ∼2500 Ω. This is the resistance through the silicon substrate G_1 and G_2. As the motor-driven stage moves toward the probe further, the contact force increases. When the overdrive reaches 5 μm, R_1 is reduced to ∼15 Ω. As the motor-driven stage moves toward the probe even further, R_1 and R_2 remain unchanged.

By adjusting the rotation stage and repeating the measurement above, the minimum overdrive required vs. the tilt can be measured. As shown in Fig. 2.15 (b), G_1 is contacted with the ground of the probe first. As the tilt increases, longer overdrive is required to overcome the tilt, as shown in Fig. 2.15(c).

The contact force required for different tilt is shown in Fig. 2.16. The minimum required contact force to ensure that all three tips on the GSG probe simultaneously contact to the CPW probing pads with low resistance is ∼2.5 mN, when the probe tips are perfectly parallel to the DUT. A linear regression of the measured results is also

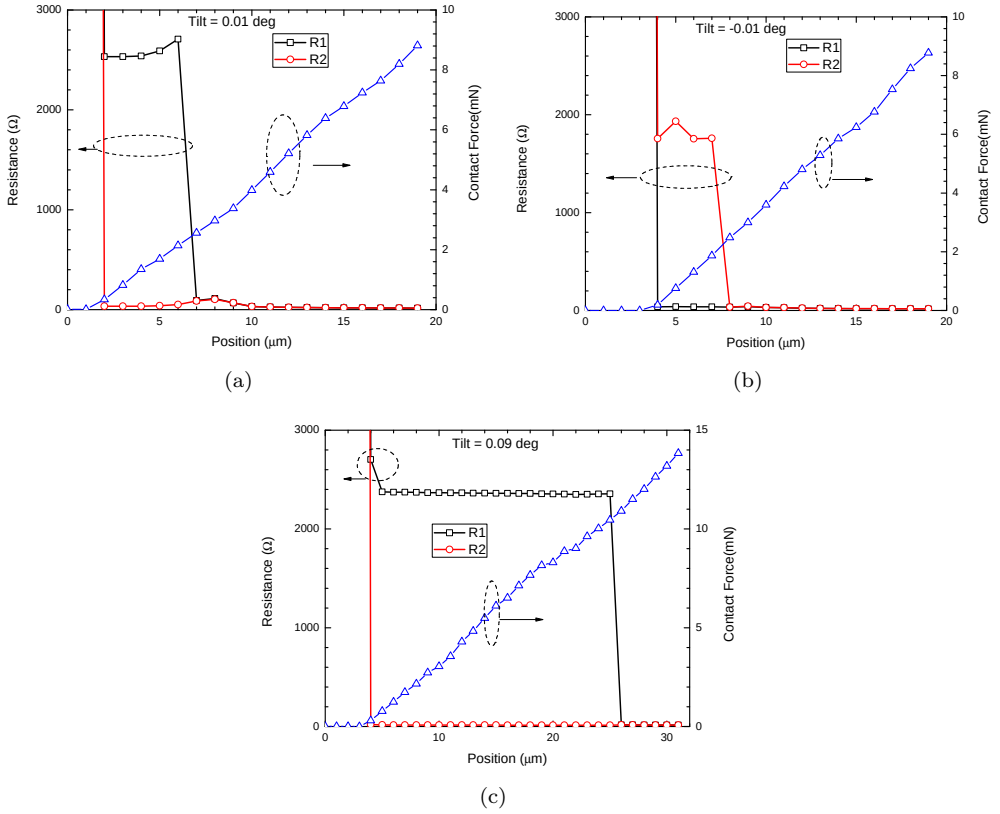


FIGURE 2.15: Tilt measurement results

shown in Fig. 2.16 (dash line). The slop of the dash line is calculated, which can be interpreted as that 1 mN rotates the probe by 0.012 degree.

During the measurement, only the total contact force is recorded. The torque generated by this contact force can be known as long as the distribution of the contact force is known. However due to the lack of test equipment, the distribution of the contact force is not able to be measured. To simplify the analysis, the contact force is assumed to distribute linearly along the probe tips, as shown in Fig. 2.17. Assuming,

$$f(x) = kx \; 0 \leq x \leq a$$

$$F = \int_0^a f(x)dx$$

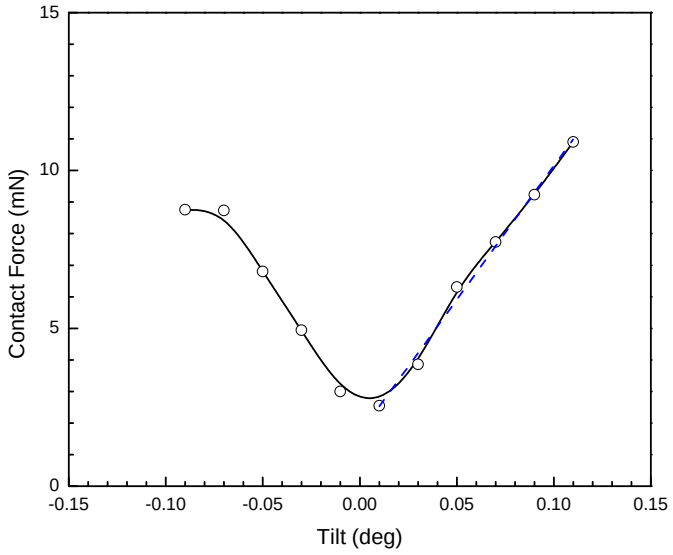


FIGURE 2.16: Overdrive required vs. tilt. The dash line shows a linear regression fit to the measured data.

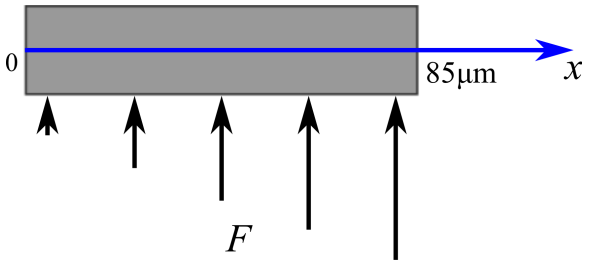


FIGURE 2.17: Contact force distributes along the probe tips.

the torque generated by contact force, F, can be calculated by,

$$\begin{aligned} T &= \int_0^a f(x)(x - \frac{a}{2})dx \\ &= \frac{1}{12}ka^3 \\ &= \frac{1}{6}F \cdot a \end{aligned}$$

where, $f(x)$ is the force distribution along the probe tips, k is an unknown constant, F is the contact force, and a is the width of the probe tips.

With $a = 85$ μm, 1 mN contact force generates 0.0142 μJ torque. Since the contact force measured is not perpendicular to the probe, only its perpendicular part contributes to the torque. 1 mN contact force generates $0.0142 \times cos30^\circ = 0.0123$ μJ. Therefore the twist of angle is calculated to be 0.98 degree/μJ, which is close to the simulation results using ANSYS, 1.39 degree/μJ. The difference between the measurement and simulation,

could be due to the over-simplified assumption of contact force distribution.

2.4 Fabrication Process

The fabrication process of the probe chip is introduced in this section. After the introduction of the fabrication process, mask design rules are detailed, which are specified to ensure high yield. These fabrication details help to understand the trade-offs made in the design. The fabrication of probes chips in this thesis was performed by fellow student Chunhu Zhang.

The fabrication starts with a silicon on insulator (SOI) wafer, a layered silicon-insulator-silicon substrate, as shown in Fig. 2.18(a). A finished probe chip, shown in Figs. 2.18(g) (top view) and (h) (cross-sectional view), features two metal layers and metalized through-silicon vias. This fabrication process was developed at the University of Virginia to produce circuits based on ultra-thin silicon substrates [23]. The fabrication process can be summarized in seven steps:

1. A beam-lead layer is deposited on the top of the device silicon layer of an SOI wafer by gold electrical plating.
2. The wafer is then mounted, beam-lead side down, on to a quartz carrier.
3. The handle silicon and insulator layers (silicon oxide) are then removed using a combination of mechanical lapping and wet etching.
4. A reactive ion etching (RIE) is used to define through-silicon via holes.
5. After the via hole etching, the bottom gold layer is patterned and aligned to the beam-lead layer.
6. Another RIE is used to define the chip extents.
7. After the chip extents are defined, the individual chips are released from the quartz carrier.

The beam-lead layer is critical to the success of the micromachined probes. First, the beam-lead is used to provide electrical and thermal contact between the chip and the waveguide block. Second, beam-leads allow for the use of thinner, more fragile substrates that might otherwise break when clamped between two block halves. As shown in

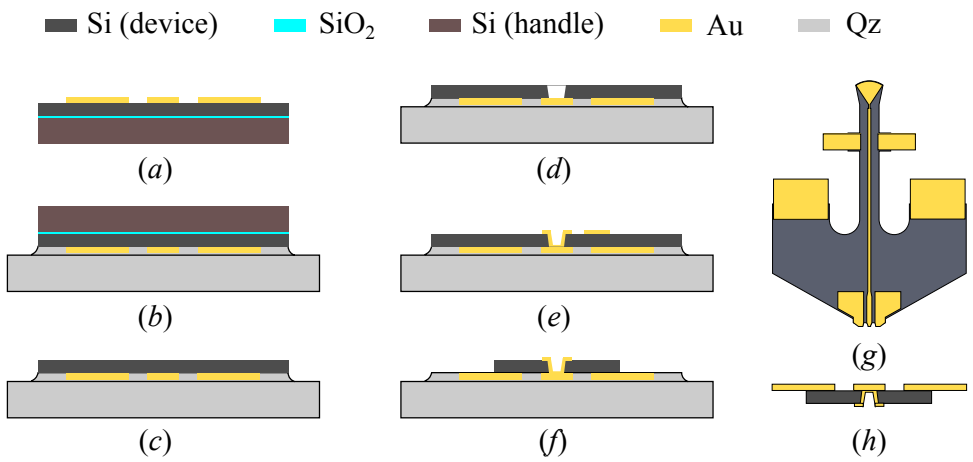


FIGURE 2.18: Process flow for the probe chip. (a) Define the beam-lead layer on SOI wafer by electroplating; (b) Mount the SOI wafer upside down to a quartz wafer; (c) Remove handle silicon and insulator layer; (d) Etch through-substrate via; (e) Metalized via holes and define bottom metal layer; (f) Define the extend of probe chips by RIE etching; (g) Top view of a finished probe chip; (h) Cross-sectional view of a finished probe chip.

Fig. 2.2, recesses are milled to accommodate the probe chip with a depth precision of +/-3 μm. When the two halves of the block are brought together, the chip are clamped between the two halves. The beam-leads, together with backside gold layer, serve as a buffer layer to prevent the probe chip from cracking given the machining tolerance.

From the mechanical analysis shown in [24], silicon is a great material in terms of mechanical properties, but if the silicon contacts directly with the DUT test pads, the probe's life time will be shortened. Beam leads at the end of probe tips prevent the ultra-thin silicon substrate from contacting directly with test pads on the DUT, as shown in Fig. 2.19.

Metalized through-silicon via holes along with the beam lead and bottom gold layers enable the realization of compact transitions from the microstrip transmission line to CPW probe tips. Metalized via holes could also be used to suppress the unwanted (even) mode in a CPW by connecting the coplanar groundplane left and right from the center conductor.

The probe chip extents are defined by photolithography followed by RIE, which gives us the flexibility to optimize the geometry of the chip extents to meet the mechanical requirements. The chip extents are also designed to provide an alignment guide when

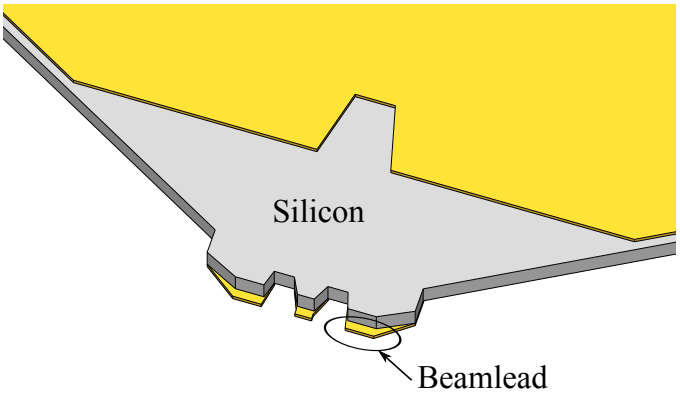


FIGURE 2.19: Micromachined GSG probe tips. Beam-lead layer, which extends beyond silicon extents, can prevent silicon substrate from contacting DUT directly to prolong probes' lifetime.

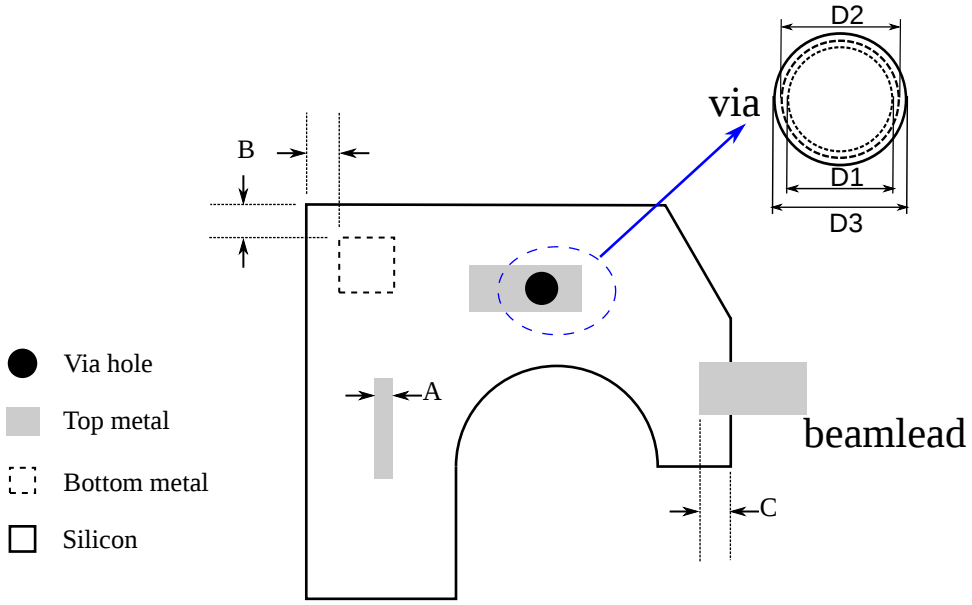


FIGURE 2.20: Mask design rules for probe chip fabrication.

the probe chip is assembled into the waveguide block.

To ensure this fabrication process achieves reasonable yield, design rules have to be followed, which are summarized in Fig. 2.20 and Table 2.3.

A in Fig. 2.20 refers to the line width on the beam-lead layer or bottom metal layer. The bottom metal layer has to be at least 4 μm away from the chip extent edges (*B* in Fig. 2.20). Otherwise, the bottom metal may change the chip extends due to misalignment during photolithography, since the RIE etching to define the probe chip extents is performed with bottom metal layer up. The beam-lead has to be at least

TABLE 2.3: Mask design rules for probe chip fabrication.

Rule	Describe	Design Rules
A	Line width	$\geq$6 μm
B	buffer	$\geq$4 μm
C	buffer	$\geq$5 μm
D_1	diameter of via hole	$\geq$20 μm for 15 μm thick silicon
D_2		$\geq D_1$+8 μm
D_3	(capture pad on bottom layer)	$\geq D_1$+8 μm

5 μm inside the chip extents to ensure beam-lead adhesion to the silicon substrate (C in Fig. 2.20). The diameter of the via hole has to be larger than 4/3 times the thickness of the silicon substrate (D_1 in Fig. 2.20). The capture pads have to be 8 μm larger in diameter than the via holes (4 μm on each side). These design rules are used to ensure microfabrication will result in a reasonable high yield.

Chapter 3

RF Design and Characterization

This chapter provides details of the RF design and characterization of the submillimeter-wave micromachined on-wafer probes. The S-parameters of the probe are measured by two-tier calibration. The last part of this chapter focus on the repeatability and reliability of the micromachined on-wafer probes.

3.1 RF Design

This section details the electromagnetic aspect of the probe design for WR-1.5 rectangular waveguide, covering the frequency band, 500 to 750 GHz. The RF design mainly includes three parts. The first part is to select the intermediate transmission line. Microstrip is selected in this thesis due to its simplicity. The other two parts are transitions for waveguide-to-microstrip and microstrip-to-CPW.

3.1.1 Intermediate Transmission Line

As shown in Fig. 2.1, an intermediate transmission line is necessary to transport the energy from rectangular waveguide to CPW probe tips. For this design, the transmission line is made of the waveguide block metal shielding and silicon substrate. Two kinds of transmission lines were considered: quasi-coax and microstrip, whose cross-sectional E-field distributions are shown in Fig. 3.1. Because of its field distribution, quasi-coax is

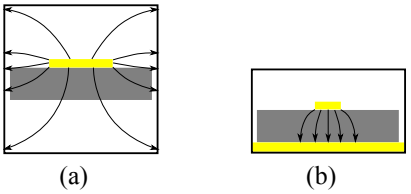


FIGURE 3.1: Transmission line mode patterns (only E-field shown). (a) Quasi-coax; (b) Microstrip.

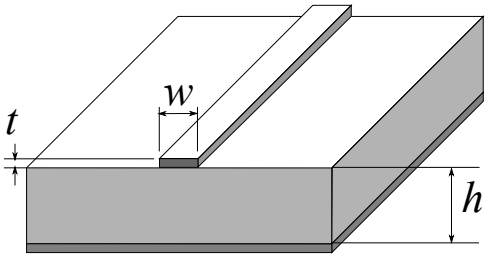


FIGURE 3.2: A cross-section of a microstrip transmission line.

less lossy, but is more sensitive to moding caused by any discontinuities in the waveguide block. The E-field distribution of microstrip is mostly confined in the substrate, therefore microstrip is selected. Designs based on the quasi-coax are detailed in [24].

Microstrip is by far the most popular microwave transmission line, especially for microwave integrated circuits and MMICs. Choosing microstrip as the intermediate transmission line could simplify the integration of circuits into the probe chip. For example, DC bias circuitry can be integrated into the probe using quarter-wave transformers. A microstrip transmission line consists of a conductive strip of width W and thickness t and a wider ground plane, separated by a dielectric substrate of thickness h, as shown in Fig. 3.2. Given the dimensions of the microstrip line, the characteristic impedance can be calculated by Hammerstad's and Jensen's formula [29],

$$Z_0 = \frac{\eta_0}{2\pi \cdot \sqrt{\epsilon_r}} \cdot ln\left(f_u \frac{h}{W} + \sqrt{1 + (\frac{2h}{W})^2}\right) \tag{3.1}$$

where,

$$f_u = 6 + (2\pi - 6) \cdot e^{-(30.666 \cdot \frac{h}{W})^{0.7528}}$$

As a rule of thumb, the thickness of the microstrip should be no more than a tenth of the wavelength in the substrate. The wavelength in silicon, which has a relative dielectric constant $\epsilon_r = 11.9$, is calculated to be 139 μm at 625 GHz (the center of

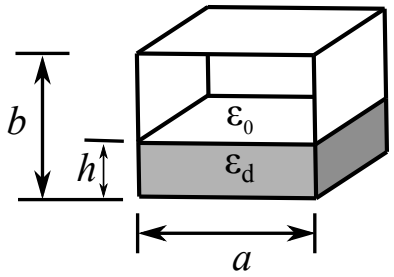


FIGURE 3.3: A partially dielectric-filled rectangular waveguide.

the WR-1.5 waveguide band). Limiting the thickness of the microstrip substrate is to prevent higher-order propagation modes. The lowest order transverse magnetic (TM) surface wave mode, TM_0, can strongly couple to the quasi-TEM microstrip mode. The cut-off frequency of the TM_0 mode can be calculated from [30],

$$f_c = \frac{c \cdot \arctan(\epsilon_r)}{\sqrt{2}\pi h\sqrt{\epsilon_r - 1}}$$

where c is the speed of light, ϵ_r is the relative dielectric constant of the substrate, and h is the thickness of the substrate.

For silicon, $\epsilon_r = 11.9$, when a 15 μm thick silicon substrate is selected, the cut-off frequency for the TM_0 mode is calculated to be 2027 GHz. The waveguide block metal shield introduces other higher-order propagation modes that can couple to the quasi-TEM microstrip mode. Microstrip in the metal shield can be modeled as a partially filled waveguide, as shown in Fig. 3.3. The TM_{10} mode in a partially filled waveguide has the lowest cut-off frequency, f_c, which can be expressed by the transcendental equation [31],

$$\frac{\epsilon_d}{\epsilon_0}\sqrt{\omega_c^2\mu_0\epsilon_0 - (\frac{\pi}{a})^2}tan\left[\sqrt{\omega_c^2\mu_0\epsilon_0 - (\frac{\pi}{a})^2}(b-h)\right] = -\sqrt{\omega_c^2\mu_d\epsilon_d - (\frac{\pi}{a})^2}tan\left[h\sqrt{\omega_c^2\mu_d\epsilon_d - (\frac{\pi}{a})^2}\right]$$

where $\omega_c = 2\pi \cdot f_c$. a, b, and h are dimensions shown in Fig. 3.3

Decreasing the channel width, a, increases the cut-off frequency. However, the width of the channel can not less than 75 μm due to machining limitations. When a 15 μm thick silicon substrate is selected, a =85 μm, and b = 45 μm, the cut-off frequency for the TM_{10} mode, f_c, is calculated to be 1223.45 GHz, which is far away from the highest

operating frequency for WR-1.5 waveguide, 750 GHz.

As shown in Fig. 2.2, the final structure is more complicated than the model shown above. Ansoft's High Frequency Structure Simulator (HFSS) is used to confirm that no higher-order propagation modes exist in the channel. Simulation results show that the lowest mode other than the quasi-TEM mode has a cut-off frequency greater than 900 GHz. The thickness of the silicon substrate is finally chosen as 15 μm, as a trade-off between being able to generate significant contact force while preventing the formation of higher-order modes in the channel.

As shown in [24], the TE_{01}^{y} mode within the transmission-line channel can couple to the quasi-coax mode. Quasi-coax is significantly less lossy than microstrip, but with an 85 μm wide channel, which is close to the minimum machining trench width of 3 mils (75 μm), the cutoff frequency of the TE_{01}^{y} mode is 800 GHz. Also, quasi-coax is more sensitive to moding caused by any discontinuities in the channel, because of its field distribution. Microstrip is selected in this thesis, because it is less sensitive to moding in the channel due to the fields being largely confined within the silicon substrate.

Microstrip attenuation consists of conductor (ohmic) losses, dielectric (substrate) losses, and losses due to radiation and propagation of surface waves and higher order modes. Generally, conductor loss is the most significant. The attenuation due to conductor loss is given approximately by [32],

$$\alpha_c = \frac{8.686 R_s}{Z_0 W}\, dB/m$$

where $R_s = \sqrt{\omega\mu_0/2\sigma}$ is the surface resistivity of the conductor and Z_0 is the characteristic impedance of the microstrip, which can be calculated by Eq. (3.1). With a 15 μm thick silicon substrate, the attenuation and characteristic impedance as a function of the width at 625 GHz is shown in Fig. 3.4. A wider strip results in lower attenuation and smaller characteristic impedance. However, the characteristic impedance of the CPW probe tips must be standardized to 50 Ω. Increasing the characteristic impedance difference between the intermediate transmission line and the CPW probe tips increases the difficulty to design the transition from microstrip to CPW. This trade-off is further considered in Sect. 3.1.3 on the microstrip-to-CPW transition.

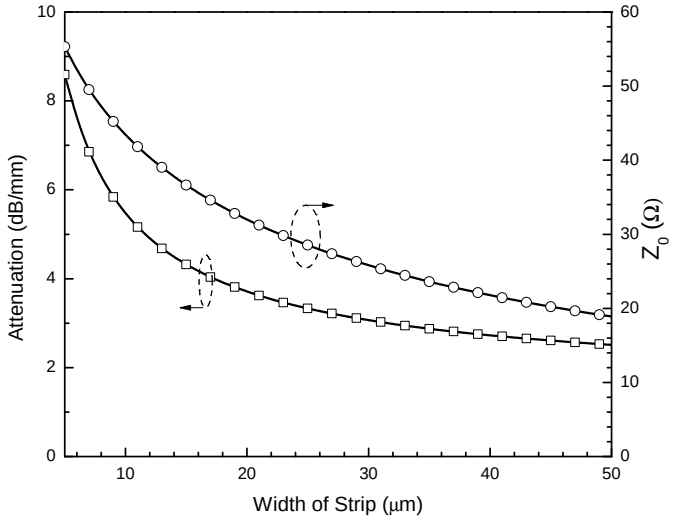


FIGURE 3.4: Calculated attenuation and characteristic impedance of microstrip for different strip width ($\sigma = 3.3 \times 10^7 S{\cdot}\mathrm{m}^{-1}$).

3.1.2 Waveguide-to-Microstrip Transition

A waveguide-to-microstrip transition is used to couple between rectangular waveguide and the intermediate microstrip transmission line on the probe chip. A waveguide-to-microstrip transition is shown in Fig. 3.5. This transition includes a thin-film E-plane probe that connects to the microstrip and penetrates into the waveguide. The input impedance from microstrip can be represented as,

$$Z_{in}(\omega) \quad = \quad R(\omega) + jX(\omega)$$

where $\omega = 2\pi f$.

A good transition has the real part of the input impedance, $R(\omega)$, close to the characteristic impedance of the microstrip, and the imaginary part of the input impedance, $X(\omega)$ close to zero over all the waveguide operating frequencies. The input impedance is a function of the thin-film probe geometry and its position relative to the waveguide back-short. Over the years, different transitions have been proposed, and the radial probe has been known for its superior broad band performance [33].

The transition is designed in Ansoft's HFSS. The model shown in Fig. 3.5 is built in HFSS, which takes into account the mechanical radii due to metal machining (37.5 μm for the WR-1.5 rectangular waveguide). To optimize the performance of the transition

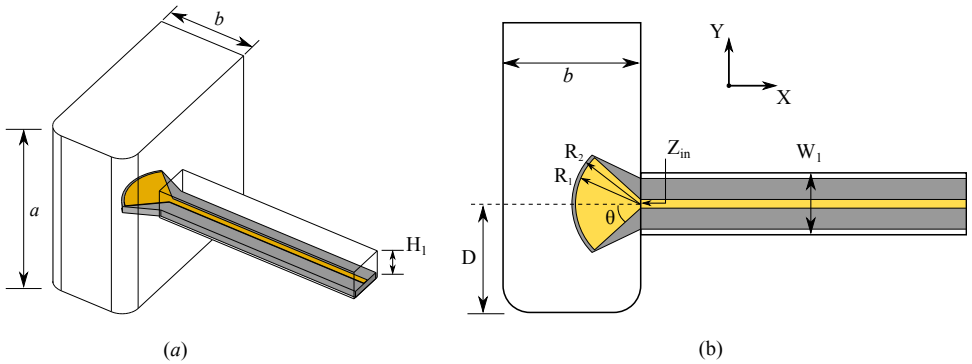


FIGURE 3.5: (a) A waveguide to microstrip transition. (b) Top view of the transition. The waveguide width, $a = 380$ μm. D is the distance between microstrip and waveguide back-short.

two different strategies can be followed. One is varying the dimensions of the transition to find an optimal dimension combination that achieves the best performance over the desired frequencies.

The other strategy is selecting a dimension combination that achieves a minimum input impedance variation over the operating frequencies, which means the input impedance confines in a small area on the Smith chart. After that, a microstrip matching network can be design to transfer the input impedance to the characteristic impedance of the microstrip transmission line. It was found that the second strategy achieved better final results in shorter time.

The input impedance over frequencies with $D = 120$ μm, $R_2 = R_1 + 4$ μm, and R_1 ranging from 75 to 95 μm, is shown in Fig. 3.6. When $R_1 = 90$ μm, the input impedance from the microstrip is confined in a relative small area in the Smith chart. To match the input impedance to the characteristic impedance of the microstrip, a short section of high impedance microstrip, serving as an inductor, is added right after the radius probe. To accelerate the design, this matching network is initially designed in Agilent® Advanced Design System (ADS) using its built-in microstrip component models. The resulting matching network dimensions from ADS are then used in the HFSS simulation and the final HFSS simulation results are shown in Fig. 3.7. The matching network is a 15 μm long and 6 μm wide high impedance microstrip and the final dimensions of the waveguide-to-microstrip transition are summarized in Table 3.1.

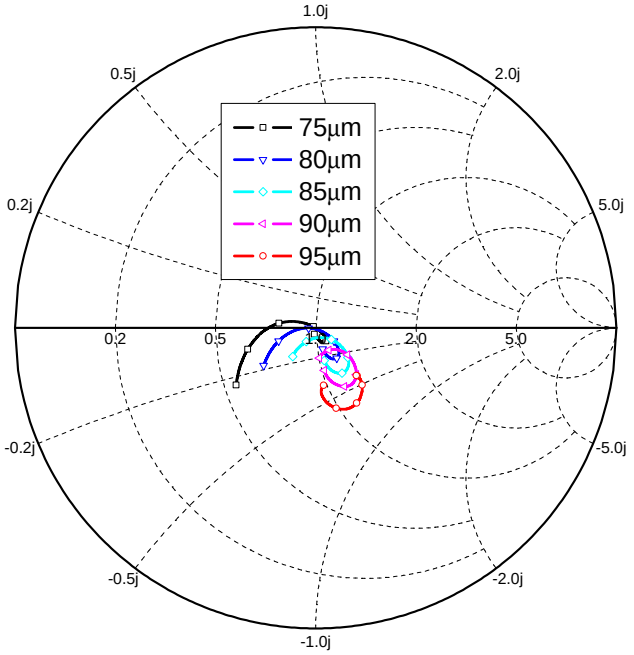


FIGURE 3.6: Simulated input impedance (Z_{in} shown in Fig. 3.5) with R_1ranging from 75 to 95 μm while R_2 is kept 2 μm larger than R_1.

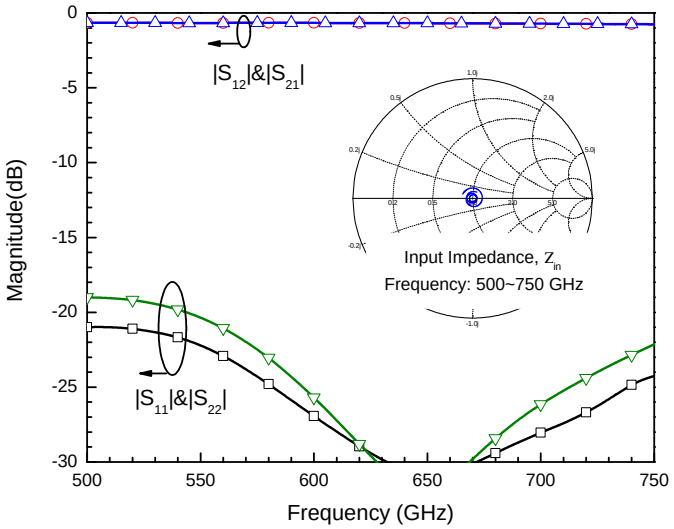


FIGURE 3.7: HFSS simulation results of the waveguide-to-microstrip transition with matching network right after radius probe.

TABLE 3.1: Final dimensions of the waveguide-to-microstrip transition.

Dimension		Dimension	
a	380 μm	D	120 μm
b	190 μm	R_1	90 μm
H_1	42.5 μm	R_2	94 μm
W_1	85 μm	θ	32.5°

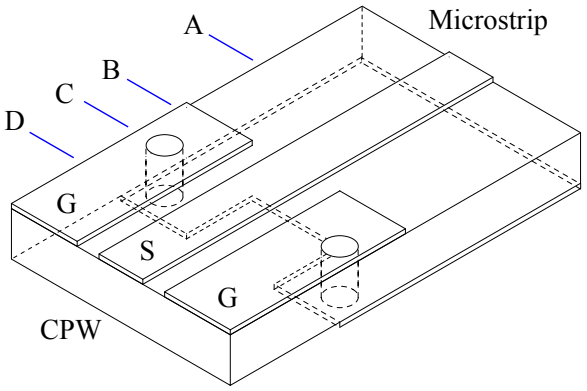


FIGURE 3.8: A "cold via" microstrip-to-CPW transition.

3.1.3 Microstrip-to-CPW Transition

On-wafer probes are terminated with GSG CPW probe tips with a standardized characteristic impedance of 50 Ω. When microstrip is selected as the intermediate transmission line, a microstrip-to-CPW transition is needed. There are two main techniques for the transitions between microstrip and CPW. One is by direct contact, and the other is by electromagnetic coupling. Transitions by electromagnetic coupling require no wire bonds or via holes, but most of them surfer from narrow bandwidth and large size[34][35]. Transitions by direct contact, on the other hand, usually call for via holes, bonding wires, or abrupt steps in the conductor[36][37], but they can achieve compact size and wide bandwidth. Since the SOI fabrication process supports metalized through substrate vias, the direct contact configuration is preferred.

Two kinds of transitions are possible between CPW and microstrip using metalized through-silicon vias. The first transition, shown in Fig. 3.8, is characterized as having vias to connect the "cold conductors" (ground) of these two transmission lines on the opposite surfaces of the dielectric substrate. It is important that the ground conductors are connected together at the same potential. With this transition, the two lines share the same "hot" (signal) conductor [36][38].

A conductor backed CPW (CB-CPW) is a part of this transition and is used as the interconnecting line between CPW and microstrip [38]. The electric field lines at cross-sections of the transition (A,B,C,D at Fig. 3.8) are shown in Fig. 3.9. In a microstrip line, the electric field lines are mostly vertical, terminating perpendicularly at the ground

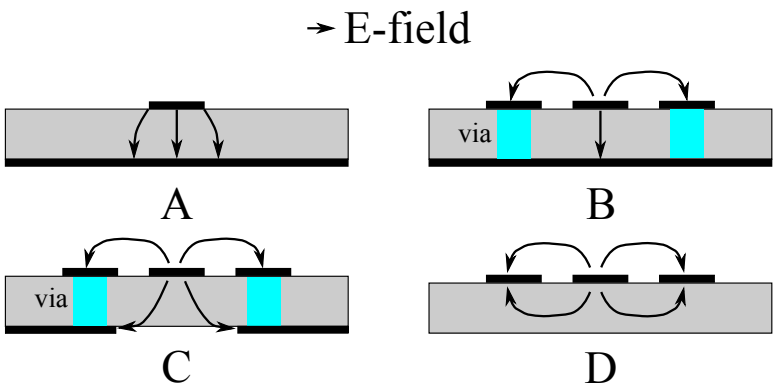


FIGURE 3.9: Electric field lines at each cross-section along the "cold via" microstrip-to-CPW transition shown in Fig. 3.8.

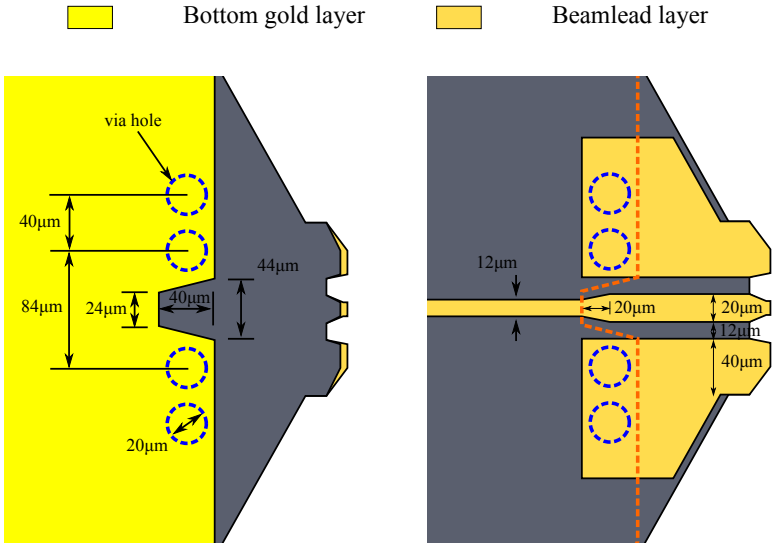


FIGURE 3.10: Dimensions of a "cold-via" microstrip-to-CPW transition.

as shown in the Fig. 3.9-A. In a CPW, the electric field lines are mostly horizontal and concentrated between the signal strip and two ground strips as shown in Fig. 3.9-D. In order to gradually match the field distributions between the microstrip line and CPW, a CB-CPW (shown in Fig. 3.9-B) is intervened, and then a ground-shaped transition structure, where the electric field lines (Fig. 3.9-C) change to those of the CPW as the signal propagates along the transition, is followed.

The field line transformation between CB-CPW to CPW is achieved by ground shaping. The transition is designed using HFSS. By adjusting the ground shape, better than 20 dB return loss is achieved. The final dimensions are shown in Fig. 3.10 and the simulation results are shown in Fig. 3.11.

The second transition, shown in Fig. 3.12, is characterized as having a via to connect

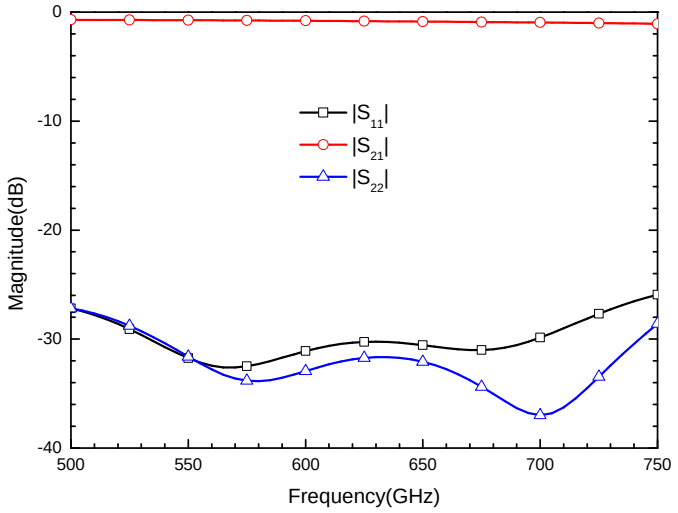


FIGURE 3.11: HFSS simulation results of a "cold-via" microstrip-to-CPW transition.

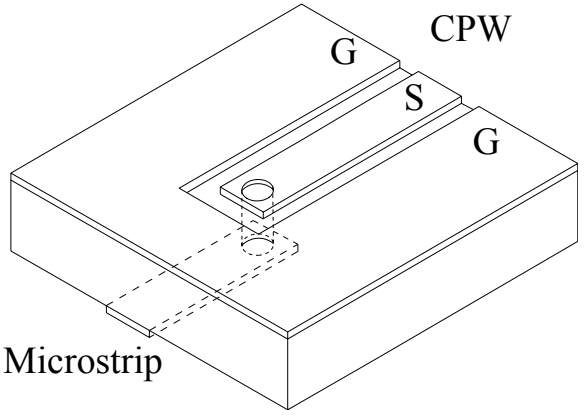


FIGURE 3.12: A "hot-via" microstrip-to-CPW transition.

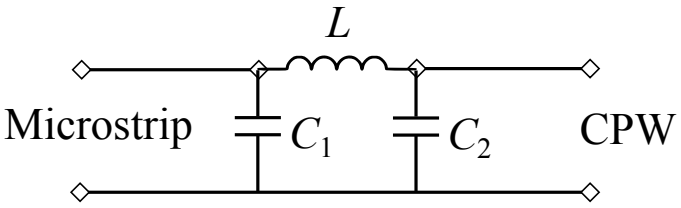


FIGURE 3.13: A equivalent circuit for the "hot via" microstrip-to-CPW transition.

the "hot conductors" (signal) of these two transmission lines on the opposite surfaces of the dielectric substrate. With this transition, the two lines share the same ground layer.

The metalized via hole connecting the signal lines of the microstrip and CPW can be modeled as an inductor, and the open ends of the microstrip and CPW add capacitance to the transition. Therefore, the transition can be considered as a low pass filter[37], as shown in Fig. 3.13.

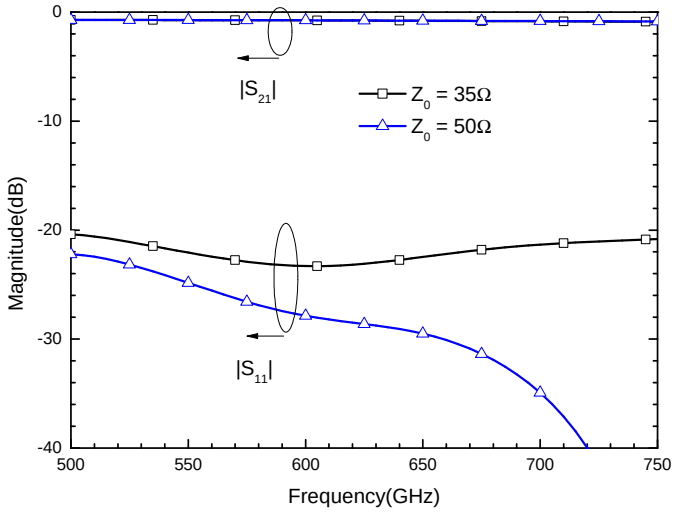
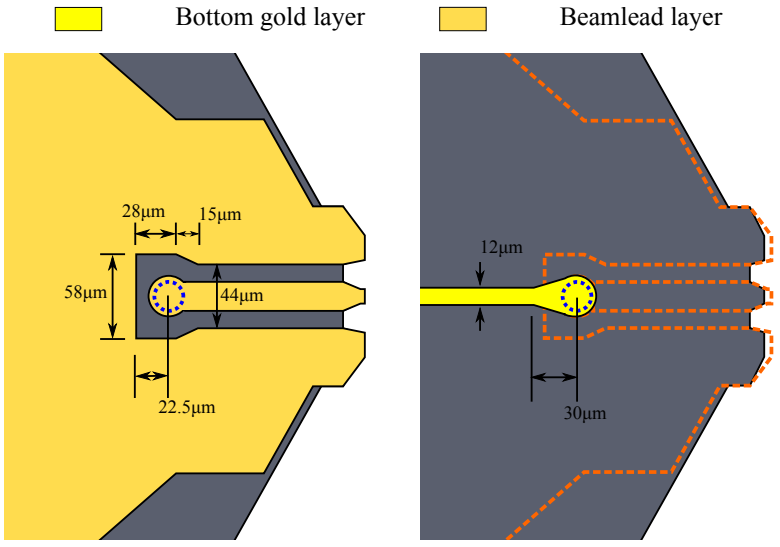


FIGURE 3.14: HFSS simulation results of "hot-via" microstrip-to-CPW transitions. Z_0 is the characteristic impedance of microstrip and the characteristic impedance of CPW is 50 Ω.

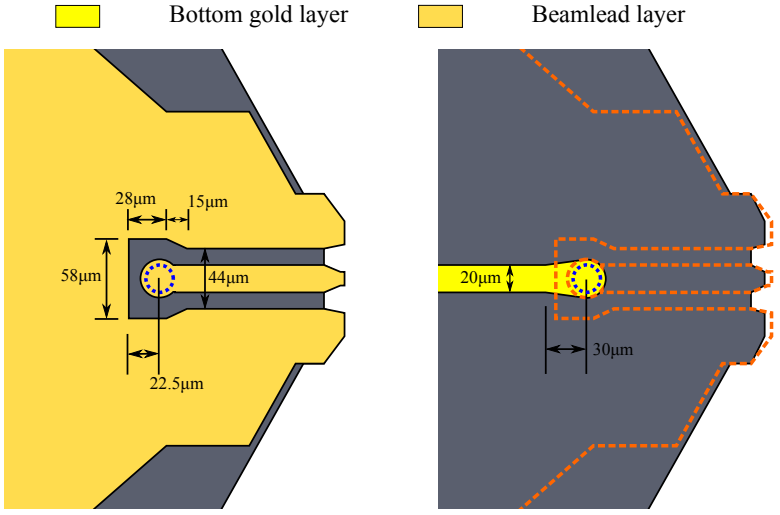
The characteristic impedance of the microstrip and CPW do not have to be the same, because the low pass filter can be designed to transfer the different characteristic impedance [39]. However, increasing the characteristic impedance difference may result in greater difficulty in the transition design. Two transitions were designed for WR-1.5: one transfer from 50 Ω microstrip to 50 Ω CPW and the other one from 35 Ω microstrip. Simulation results are shown in Fig. 3.14 with dimensions of these two transitions detailed in Fig. 3.15.

3.1.4 WR-1.5 On-wafer Probe

Insertion loss is an important characteristic for on-wafer probes. On-wafer probes, which are inserted between the test equipment and DUT, reduce the sensitivity of the test equipment. To minimize the insertion loss, the transmission lines and waveguide length that are parts of the probe are kept to a minimum. As shown in Fig. 3.16, the length of the waveguide, l_1, is limited by the size of the waveguide flange matched to the test equipment and the angle of probe to the wafer, θ. The length of shielded microstrip, l_2, is limited by the size of the waveguide. The length of the transmission line out of the metal block, l_3, and the minimum block thickness, t, determine the maximum overdrive the probe can achieve.



(a)



(b)

FIGURE 3.15: Dimensions of a "hot-via" microstrip-to-CPW transition. The dimensions of CPW is the same as the CPW in "cold-via" configuration. The diameter of the via holes is 20 μm. (a) 50 Ω microstrip to 50 Ω CPW. (b) 35 Ω microstrip to 50 Ω CPW.

TABLE 3.2: Dimensions of the probe.

Name	Describe	value
t	minimum metal thickness	50 μm
d_{max}	maximum over-drive	150 μm
l_1	the length of the waveguide	34.8 mm
l_2	the length of shielded microstrip	350 μm
l_3	the length of microstrip outside metal block	400 μm

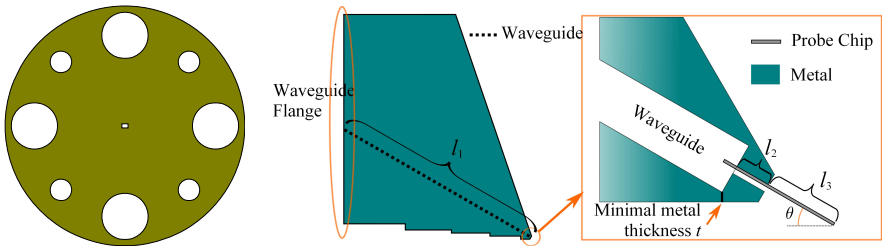


FIGURE 3.16: (a) Front view of a waveguide flange. Dowel pin holes and screw holes are consistent with waveguide interface recommendations for sub-millimeter wavelengths [6]. (b) The physical length constrains of the waveguide and transmission lines in the micromachined probe.

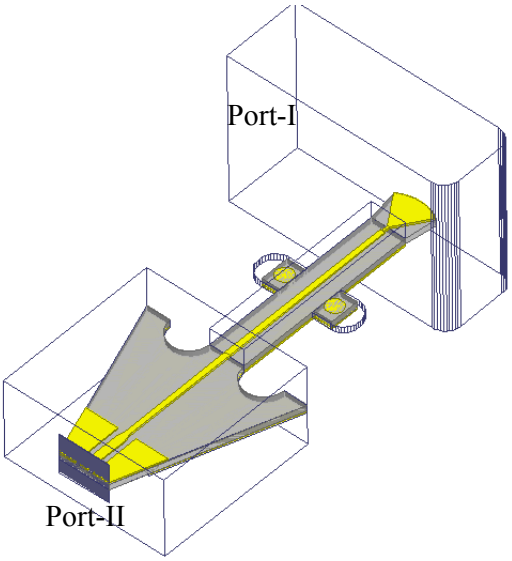


FIGURE 3.17: The HFSS simulation model of a micromachined on-wafer probe.

Given the probe angle, $\theta = 30°$, and the minimum block thickness, $t = 50$ μm, the probe chip is set to have a maximum overdrive of 150 μm, which ensures the probe tips are visible in a microscope looking down from above the DUT. Therefore, the length of the transmission line out of the metal block, l_3, is 400 μm.

The waveguide-to-microstrip transition, microstrip and microstrip-to-CPW transition are put together to form the probe. A final simulation from the waveguide to coplanar probe tips, shown in Fig. 3.17, is done in HFSS. The waveguide is Port-I and CPW is Port-II. The conductivity of the strip is set to $3.3 \times 10^7 S{\cdot}\mathrm{m}^{-1}$ and the metal block is set to lossless. Three different chip designs are simulated as summarized in Table 3.3.

1. Design-I

TABLE 3.3: Designs-summary

	$Z_0$of Microstrip	Microstrip-to-CPW transition
Design-I	50 Ω	Cold Via
Design-II	50 Ω	Hot Via
Design-III	35 Ω	Hot Via

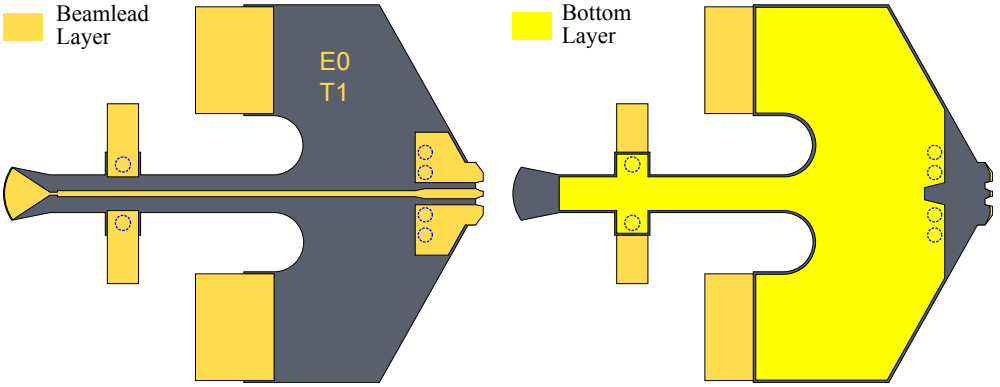


FIGURE 3.18: Images of the top and bottom of the micromachined wafer probe chip, design-I. (a) Top view; (b) bottom view.

Design-I uses 50 Ω microstrip and a "cold via" microstrip-to-CPW transition. Since the probe tip metal has to be on the beam-lead layer (as top gold layer), the signal line of the microstrip is kept on the same layer, the beam-lead layer. The microstrip ground is made of the bottom gold layer. Via holes are added to the alignment taps to prevent resonance in the intermediate transmission line. Images of the top and bottom of the micromachined probe chip are shown in Fig. 3.18. HFSS simulation results from waveguide to CPW probe tips are shown in Fig. 3.19.

2. Design-II

Design-II uses 50 Ω microstrip and a "hot via" microstrip-to-CPW transition. Since the probe tip metal has to be on the beam-lead layer, the microstrip signal line is kept on the bottom gold layer. The microstrip ground is made of the beam-lead layer. Fig. 3.20 shows images of the top and bottom of the micromachined probe chip. HFSS simulation results from waveguide to CPW probe tips are shown in Fig. 3.21.

3. Design-III

Design-III uses 35 Ω microstrip and a "hot via" microstrip-to-CPW transition. As shown in Fig. 3.4, attenuation of microstrip reduces with the increase in strip width.

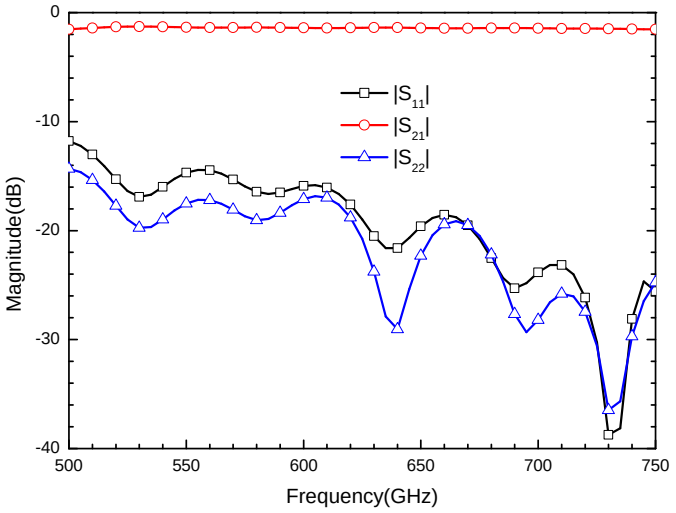


FIGURE 3.19: HFSS simulation results of probe with a Design-I probe chip. The simulation is done from waveguide to CPW probe tips.

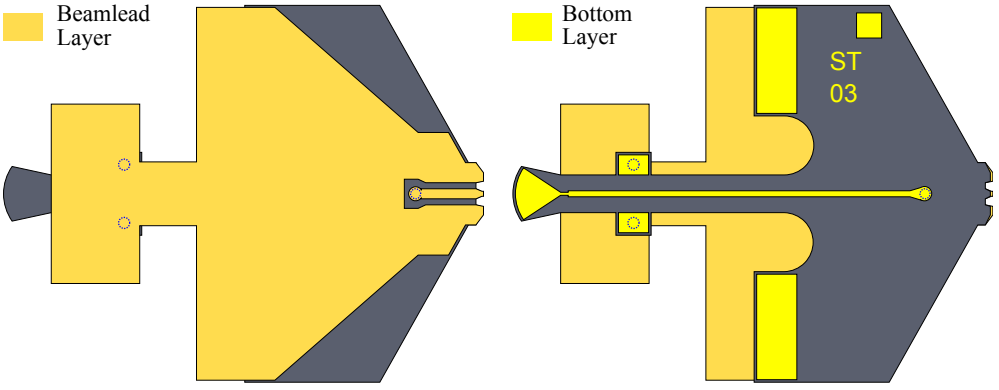


FIGURE 3.20: Images of the top and bottom of the micromachined wafer probe chip, design-II. (a) Top view; (b) bottom view.

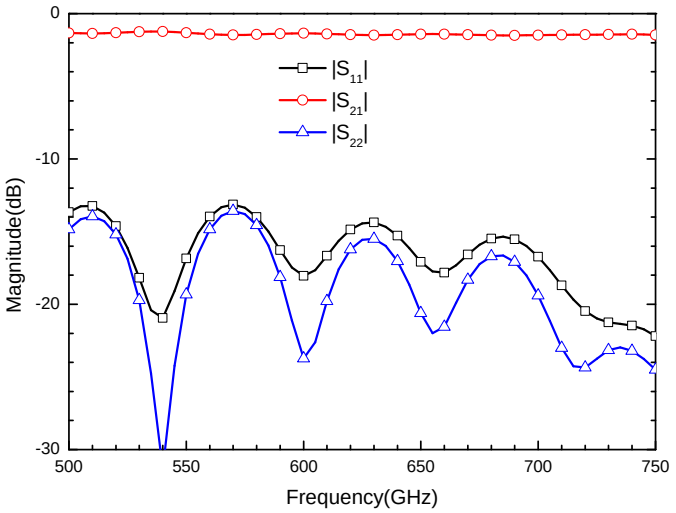


FIGURE 3.21: HFSS simulation results of probe with a Design-II probe chip. The simulation is done from waveguide to CPW probe tips.

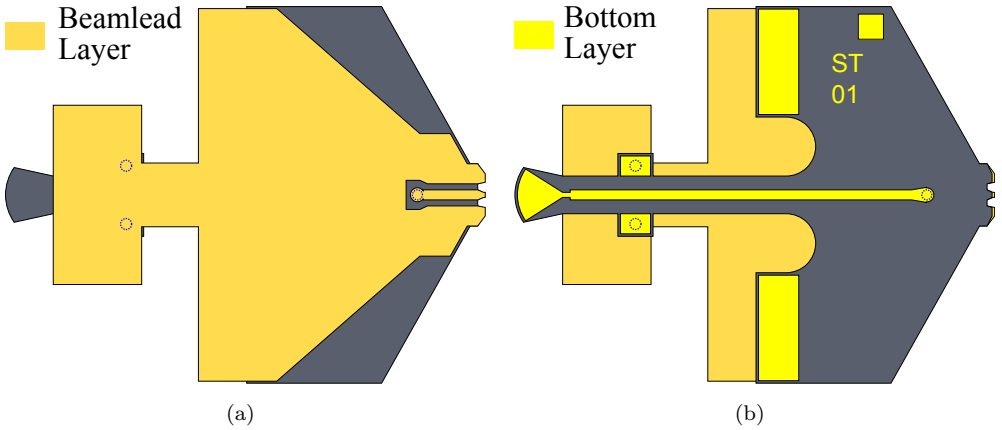


FIGURE 3.22: Images of the top and bottom of the micromachined wafer probe chip, design-III. (a) Top view; (b) bottom view.

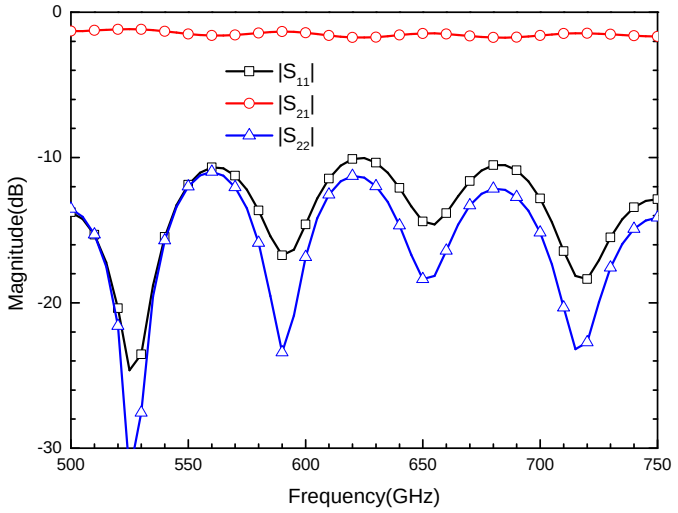


FIGURE 3.23: HFSS simulation results of probe with a Design-III probe chip. The simulation is done from waveguide to CPW probe tips.

However, the lower characteristic impedance makes the impedance transformation to 50 Ω at the microstrip-to-CPW transition more difficult to design. Therefore 35 Ω microstrip is selected in this work. Because the probe tip metal has to be on the beam-lead layer, the microstrip signal line is kept on the bottom layer. Fig. 3.22 shows images of the top and bottom of the micromachined probe chip. The width of the microstrip signal line is 20 μm, which is the same as the width of the CPW signal line to simplified the design. HFSS simulation results from waveguide to CPW probe tips are shown in Fig. 3.23. However the HFSS simulation does not shown the reduction in insertion loss because HFSS is not good at predicting the insertion loss.

As mentioned in Section 2.1.2, the probe chip is aligned to the block to a better

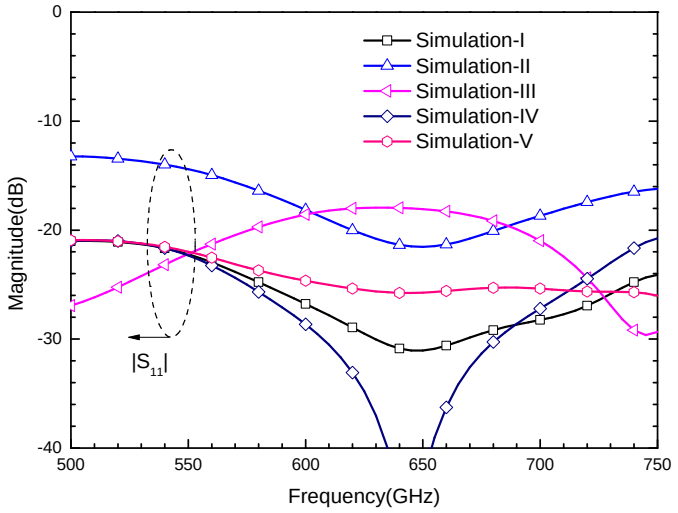


FIGURE 3.24: Simulation results of waveguide-to-microstrip transition. Simulation-I: dimensions shown in Table 3.1; Simulation-II and -III: dimensions same as Simulation-I with ± 5 μm alignment error along X-direction (shown in Fig. 3.5(b)). Simulation-IV and -V: dimensions same as Simulation-I with ± 5 μm alignment error along Y-direction (shown in Fig. 3.5(b))

than ± 5 μm precision. The waveguide-to-microstrip transition performance is most sensitive to this assembly uncertainty. The transition performance sensitivity to this assembly uncertainty is analyzed in HFSS. The simulation results show that with a ± 5 μm tolerance, the waveguide-to-microstrip transition is expected to have better then 15 dB return loss over 80% of the waveguide operating bandwidth, as shown in Fig. 3.24.

3.2 RF Characterization

A micromachined probe is a two-port electrical network. Network analyzers are commonly used to measure *s*cattering–parameters of electrical networks. Compared to other network parameters sets such as Y-parameters, S-parameters are easier to measure at high frequencies and can be converted to other network parameters. The beginning of this section shows a method using a one-port measurement system to obtain S-parameters of a two-port network.

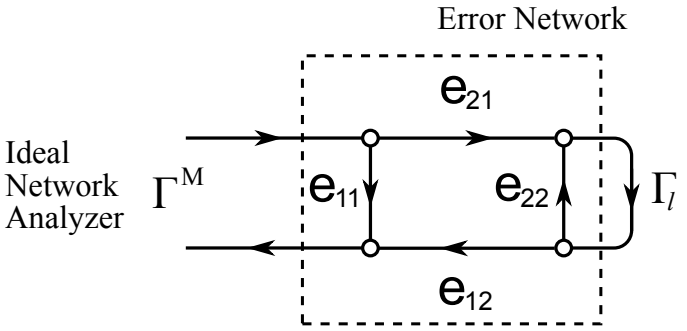


FIGURE 3.25: Error model for one-port calibration

3.2.1 Two-tier Calibration

To ensure the validity of the measurement data, network analyzers must be calibrated to correct the imperfections of the measurement system. Calibration is a process of measuring devices with known or partially known characteristics and using these measurements to estimate the error of the network analyzer.

An uncalibrated one-port network analyzer is modeled as an error-free network analyzer with an error network inserted between it and the device under test, as shown in Fig. 3.25. The reflection coefficient measured at the error-free network analyzer test port, Γ^M, is related to the S-parameters of the error network, e_{ij}, and the reflection coefficient of the device under test, Γ_l, by the bilinear transform,

$$\Gamma^M = e_{11} + \frac{e_{21}e_{12}\Gamma_l}{1 - e_{22}\Gamma_l}. \tag{3.2}$$

One-port calibration can be performed by terminating the test port with no less than three known calibration standards and measuring the corresponding reflection coefficients at the error-free network analyzer test port. Measuring known standards, we have,

$$\begin{aligned} \Gamma_1^M &= e_{11} + \frac{e_{21}e_{12}\Gamma_{l1}}{1 - e_{22}\Gamma_{l1}} \\ \Gamma_2^M &= e_{11} + \frac{e_{21}e_{12}\Gamma_{l2}}{1 - e_{22}\Gamma_{l2}} \\ &\vdots \\ \Gamma_n^M &= e_{11} + \frac{e_{21}e_{12}\Gamma_{ln}}{1 - e_{22}\Gamma_{ln}} \end{aligned} \tag{3.3}$$

where n =1, 2, 3... Let, $x_1 = e_{11}$,$x_2 = e_{22}$ and $x_3 = e_{21}e_{12} - e_{11}e_{22}$. Eq. (3.3) can be rewritten as,

$$\begin{aligned} \Gamma_1^M &= x_1 + \Gamma_1^M \Gamma_{l1} x_2 + \Gamma_{l1} x_3 \\ \Gamma_2^M &= x_1 + \Gamma_2^M \Gamma_{l2} x_2 + \Gamma_{l2} x_3 \\ &\vdots \\ \Gamma_n^M &= x_1 + \Gamma_n^M \Gamma_{ln} x_2 + \Gamma_{ln} x_3 \end{aligned} \tag{3.4}$$

By solving Eq. (3.4), we have: e_{11}, e_{22}, and $e_{21}e_{12}$. Based on these results and Eq. (3.2), the calibrated results can be obtained. When an unknown one-port network is attached to the test port, the calibrated reflection coefficient is found through the inversion of Eq. (3.2),

$$\Gamma_{DUT} = \frac{M_{DUT} - e_{11}}{e_{22}M_{DUT} - (e_{11}e_{22} - e_{12}e_{21})} \tag{3.5}$$

where, Γ_{DUT} is the calibrated reflection coefficient and M_{DUT} is the raw measured results.

A one-port two-tier calibration can be used to obtain the S-parameters of a micromachined probe, because a probe can be modeled as a two-port error network. With this method, the network analyzer is initially calibrated to a reference plane coincident with the test port to correct the imperfections of the measurement system. After the first tier in the calibration procedure, the probe is attached to the network analyzer test port. The second tier calibration is performed by terminating the CPW probe tips with on-wafer calibration standards. From the second tier calibration, the S-parameters of the probe, S_{11}, S_{22}, and $S_{12}S_{21}$, are obtained by solving Eq. (3.2). Since the probe is a reciprocal network, we have,

$$S_{12} = S_{21} = \pm\sqrt{S_{12}S_{21}}$$

The $\pm$ sign can be determined by estimating the electrical length of the probe. Therefore a two-port probe can be measured by a one-port measurement system.

To measure the WR-1.5 rectangular waveguide micromachined on-wafer probe, the

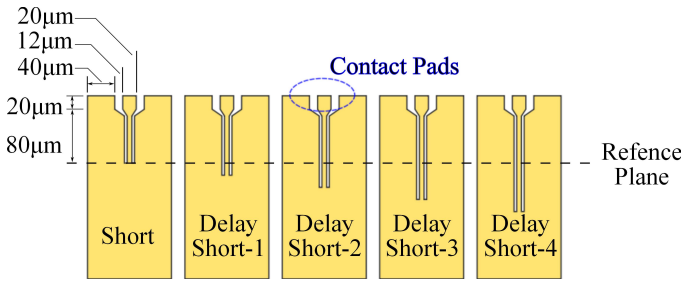


FIGURE 3.26: Dimensions of CPW calibration standards. Dimensions of CPW is 4/7/4 μm.

second-tier calibration is performed using on-wafer CPW calibration standards. Because it is difficult to make a precise on-wafer load, only CPW short and delayed shorts, which can be accurately characterized from their physical dimensions, are used as calibration standards. CPW calibration standards are fabricated on a 380 μm-thick high resistivity silicon substrate (>10 kΩ·cm). The CPW dimensions are 4/7/4 μm with other dimensions detailed in Fig. 3.26. The contact point is about 100 μm away from the reference plane to minimize the effect of the discontinuity at the contact point. The contact pads are designed to match a 30 μm probe pitch. Delay short-1 is 18 μm longer than the short, and delay short-2 is 18 μm longer than the delay short-1. This 18 μm length corresponds to 35° at 625 GHz, so that delay short-4 is 140° long at 625 GHz and 112° long at 500 GHz.

The above discussion is limited to one-port measurement systems. However, two-port calibration techniques, including Thru-Reflect-Line (TRL), Line-Reflect-Match (LRM) and Open-Short-Load-Thru (OSLT) [40], can also be used in two-tier calibration to obtain the probe S-parameters.

3.2.2 *S*-parameter Measurement Results

This section presents the S-parameter measurement results using the one-port two-tier calibration. The setup is shown in Fig. 3.27. The reflection coefficients for 500–750 GHz are measured by a one-port WR-1.5 frequency extension unit from Virginia Diodes Inc. (VDI WR1.5 VNAXTXRX) with a Rhode and Schwarz ZVA-40 network analyzer as the backend.

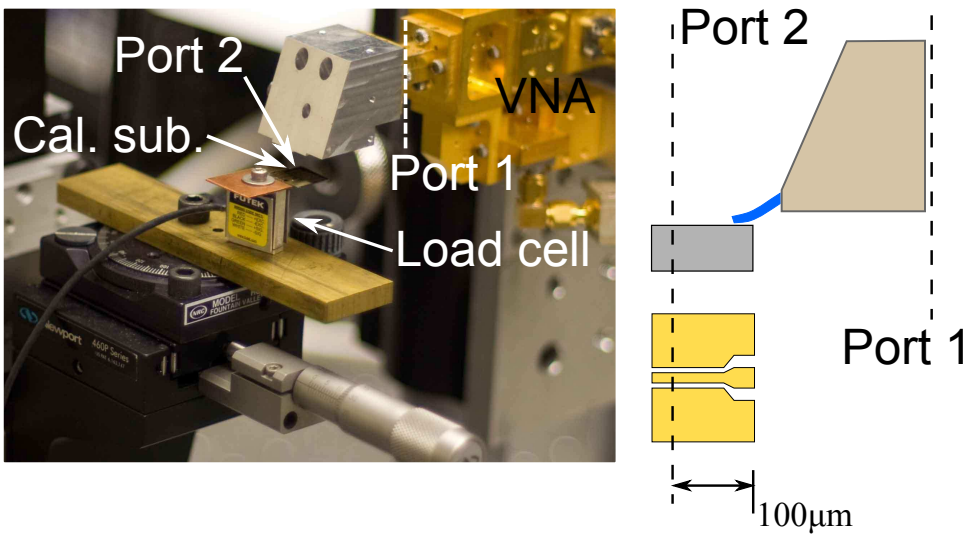


FIGURE 3.27: Measurement setup for WR-1.5 micromachined on-wafer probe.

First-tier calibration is performed using a waveguide short and delayed shorts of three different lengths. Because waveguide loads are generally unavailable in the WR-1.5 band, only a waveguide short and delayed shorts, which can be accurately characterized from their dimensions, are used as calibration standards.

During the second-tier calibration, a consistent contact force is critical for an accurate calibration and repeatable measurement. Previous measurements have shown that a micromachined silicon chip achieves a low contact resistance of 0.07 Ω at 1 mN per tip [28]. However, higher contact force (>3 mN) may be required to ensure that all three tips on the GSG probe simultaneously contact to the CPW probing pads with low resistance, given possible non-planarity of the probe with the DUT, as shown in Section 2.3. To determine the minimum force required for good RF contact, the micromachined probe is connected to the one-port network analyzer, which is used to measure the reflection coefficient at the waveguide connection, Port-I of the probe.

The gold contact pad on the test wafer shorts the CPW probe GSG tips as the stage moves up and the wafer contacts the probe. The phase of the reflection coefficient at Port-I responds to the change in probe tip contact and settles during this process. The contact force where the reflection coefficient settles is defined as the minimum contact force required for RF probing. Test results show that there is a dramatic change in the phase of the measured reflection coefficient when the contact force increases from 0 to 0.2 mN, and as the contact force increases, the reflection coefficient gradually settles.

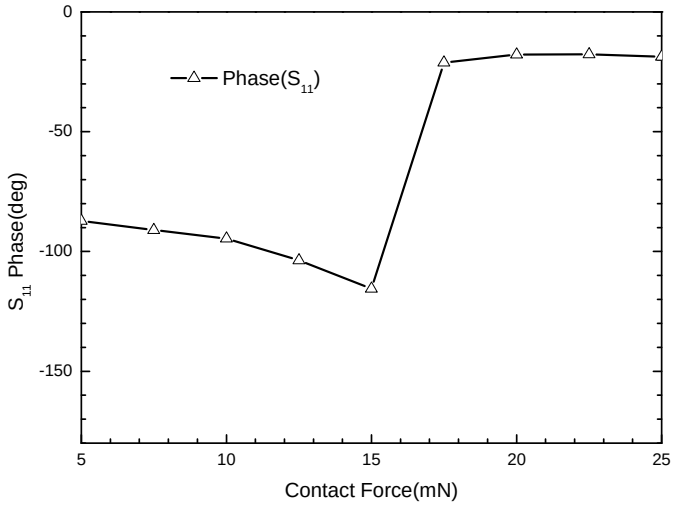


FIGURE 3.28: Phase of the reflection coefficient at Port-I vs. contact force (@625 GHz).

Above 15 mN, the phase change in reflection coefficient with respect to contact force is within the phase measurement uncertainty, as shown in Fig. 3.28.

To ensure good RF contacts, during the second tier calibration, the contact force is set to 20 mN using the loadcell as feedback. By measuring the reflection coefficient of the probe when terminated with on-wafer calibration standards shown in Fig. 3.26, and noting that the probe is a reciprocal network, the S-parameters of the probe are obtained. Three microstrip probe chip designs, as detailed in Subsection 3.1.4, are tested.

Design-I Design-I features a "cold via" microstrip-to-CPW transition. The S-parameters of this micromachined probe obtained by the one-port two-tier calibration method are shown in Fig. 3.29.

The insertion loss varies from 8 dB to 12 dB in the frequency range from 500 to 750 GHz. The measured return losses are much worse than expect based on the HFSS simulation. This discrepancy between the measurement and simulation is because the microstrip ground is floating. In design-I, the ground plane of the microstrip is fabricated on the bottom gold layer of the probe chips. According to the mask design rules, the bottom metal layer has to be kept inside the probe chip extents. The metal block used in the measurement is shared with other probe designs which use quasi-coax as the intermediate transmission line [24]. Therefore, the microstrip ground plane is not

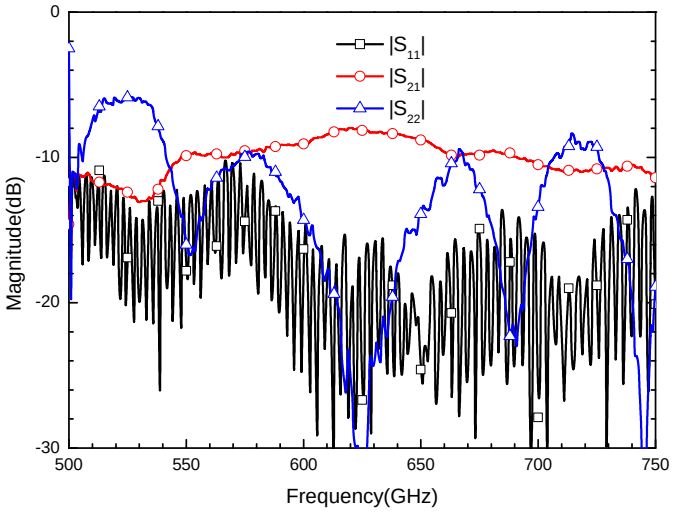


FIGURE 3.29: Measured S-parameters of a WR-1.5 micromachined on-wafer probe.

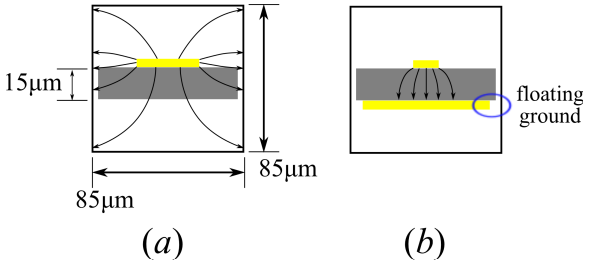


FIGURE 3.30: floating-ground

connected to the metal block along the intermediate transmission line, as shown in Fig. 3.30, until the tabs with via holes are reached (see Fig. 3.18)

An HFSS model with floating ground is simulated and the simulation results are shown in Fig. 3.31. The return losses are much worse than the simulation results with microstrip ground plane well connected to the waveguide block, as shown in Fig. 3.7.

Design-II Design-II features a "hot via" microstrip-to-CPW transition. In this design, the ground plane of the microstrip is fabricated on the beam-lead layer. Since the beam-lead layer can extend beyond the edge of the silicon probe chip, the microstrip is well grounded to the metal block. The S-parameters obtained by the same one-port two-tier calibration method are shown in Fig. 3.32. The insertion loss varies from 8 dB to 9 dB and the return losses are better than 12 dB in the frequency range from 500 to 750 GHz. The dip in the transmission coefficient near 550 GHz is a water vapor absorption line

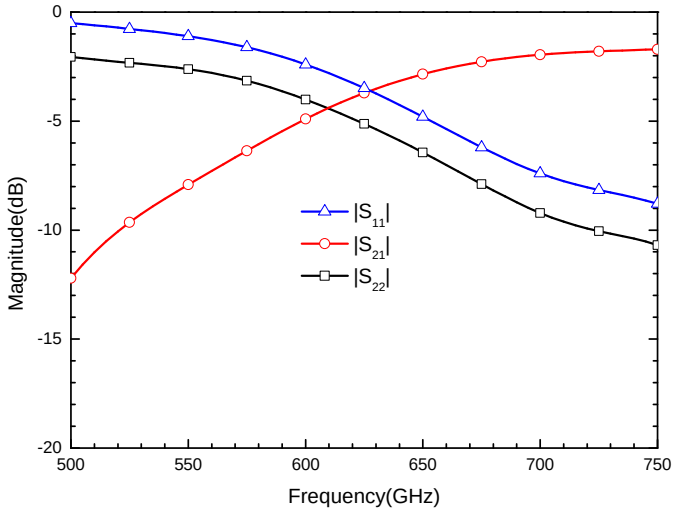


FIGURE 3.31: Simulated S-parameters of waveguide-to-microstrip transition with floating ground. The dimensions of the transition are the same as that shown in Fig. 3.5 and Table 3.1. .

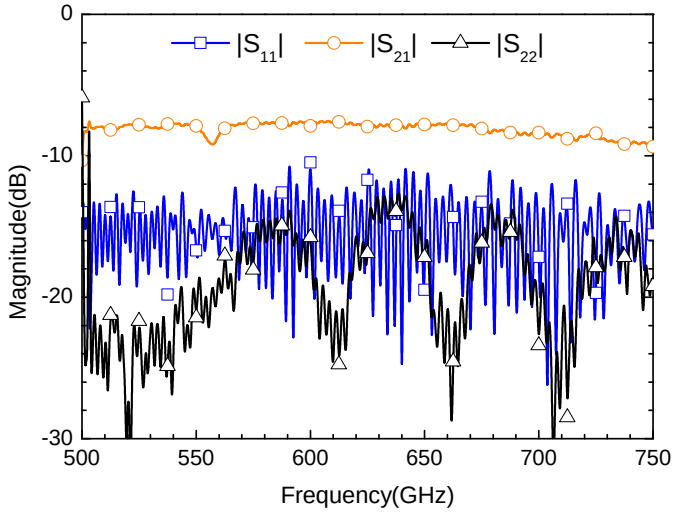


FIGURE 3.32: Measured S-parameters of a WR-1.5 micromachined on-wafer probe. The dip in the transmission coefficient near 550 GHz is a water vapor absorption line.

[41]. The ripple in the return loss, $|S_{11}|$, is due to a standing wave in the waveguide connecting the test equipment and the probe chip.

Design-III Design-III features a "hot via" microstrip-to-CPW transition and low impedance, 35 Ω, microstrip. As shown in Fig. 3.4, the low impedance microstrip results in lower loss for the same length. The measurement results are shown in Fig. 3.33. The insertion loss varies from 6 dB to 7 dB for 500 to 750 GHz, which is ∼2 dB better than Design-II. The return loss is similar to that of Design-II. The ripple in the return loss,

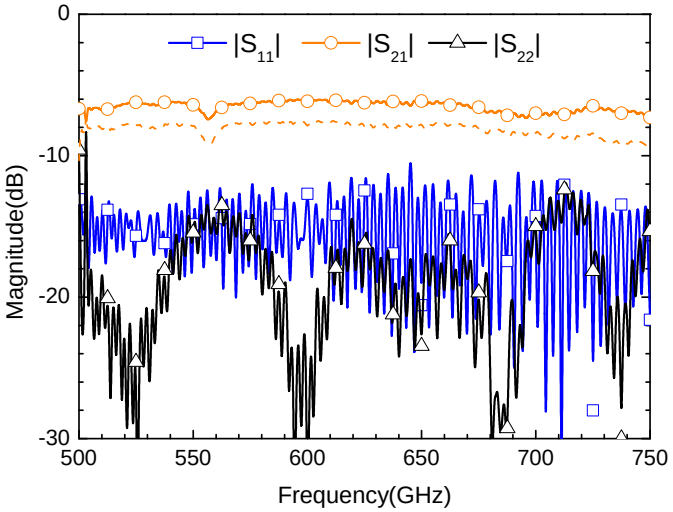


FIGURE 3.33: Measured S-parameters of a WR-1.5 micromachined on-wafer probe. The dip near 550 GHz is a water vapor absorption line. Dashed line shows the insertion loss of probe design-II.

$|S_{11}|$, is due to a standing wave in the waveguide connecting the test equipment and the probe chip. Since this ∼34 mm long waveguide section is not included in the HFSS simulation, the ripple does not appear in the simulation results, shown in Fig. 3.23.

The simulated insertion loss shown in Fig. 3.23 is about 2 dB, which only simulates the probe from waveguide to CPW probe tips and does not account the loss due to the long waveguide connecting the probe chip to the test equipment. The conductor loss of the waveguide can be calculated by [31]:

$$\alpha_c = \frac{8.686 \times R_s}{a^3 b \beta k \eta}(2b\pi^2 + a^3k^2)\, dB/m \tag{3.6}$$

where $R_s = \sqrt{\omega\mu_0/2\sigma}$ is the surface resistivity of the conductor.

However, Eq. (3.6) does not take into account the surface roughness of the machined waveguide walls, so to find the true for our waveguide block, the conductivity of aluminum is adjusted to account the surface roughness to $\sigma = 2 \times 10^7$ S/m, two thirds of the bulk value for aluminum [24]. The waveguide attenuation is calculated by Eq. (3.6) to be 0.0768 dB/mm at 625 GHz. The length of waveguide is 34.8 mm, which results in 2.67 dB. The loss due to the calibration standards is also included in the insertion loss of the probe. The attenuation of the on-wafer CPW is 5.19 dB/mm and 100 μm of CPW is modeled, corresponding to 0.52 dB. The loss of waveguide to probe tips is

TABLE 3.4: Estimated Losses in the probe with a Design-III probe chip at 625 GHz.

Structure	Loss(dB)
Waveguide	2.67
Waveguide to probe tips	1.75
On-wafer CPW	0.52
Total Estimate	4.94
Measured	6.11

simulated using HFSS. The estimated loss is summarized in Table 3.4 and the results are compared to the measured insertion loss.

Measurements exceed the calculated loss by 1.17 dB at 625 GHz. This discrepancy is due to not taking the roughness into account when simulating the CPW standards and the probe from waveguide to CPW probe tips. In additions, HFSS is not good at predicting the insertion loss. The design with 35 Ω microstrip should have lower insertion loss than the one with 50 Ω microstrip and this is confirmed by the measurement results.

As shown in this loss budget analysis, a significant source of loss is the waveguide (2.67 dB). Making the waveguide shorter would help reduce the insertion loss of the probe. The length of waveguide is largely limited by the size of the waveguide flange. Significant reductions in the length of waveguide could be made if a smaller flange is used, such as the miniature interface described by Hesler [6]. This would reduce the flange size from 0.750" to 0.500" in diameter, reducing the required length of waveguide to 12.7 mm and the resulting waveguide insertion loss would decrease to 0.98 dB(a drop of 1.69 dB).

The designs presented in this thesis have a waveguide orientation that is orthogonal to the conventional waveguide orientation used by most test equipment. To connect the micromachined probes to the test equipment, waveguide twists are needed to provide a polarization rotation. At terahertz frequencies, it is desirable to use a twist design that is compact in order to reduce loss, however these designs are difficult if not impossible to realize using standard machining. Appendix B presents a micromachined compact waveguide twist for terahertz frequencies. The Rud-Kirilenko twist geometry is ideally suited to the micromachining processes developed at the University of Virginia [42] [43].

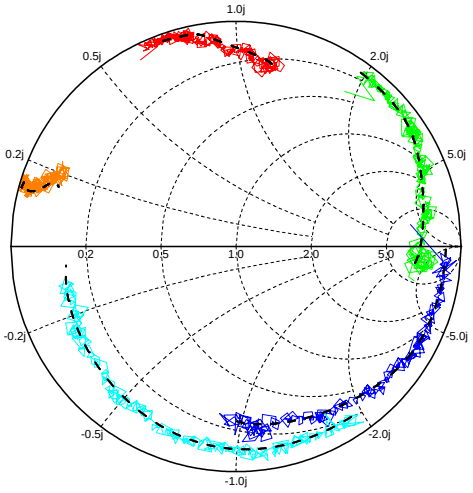


FIGURE 3.34: Remeasured S-parameters of calibration standards. The dashed lines show the simulated reflect coefficient of standards used in the calibration, and the thin solid lines show the results for a single re-measurement from 500 to 750 GHz.

Measurements of a WR-1.5 micromachined twist exhibit a return loss near 20 dB and a median insertion loss of 0.5 dB from 600 to 750 GHz.

3.3 Repeatability and Reliability

3.3.1 Repeatability

Repeatability is a measure of the agreement between repeated measurements of the same property under the same conditions. After calibration, the calibration standards are re-measured with the same contact force, 20 mN, to evaluate the repeatability of the on-wafer measurement, and these measurement results are shown in Fig. 3.34. The dashed lines show the simulated reflection coefficient of the standards used in the calibration, which are found using HFSS. The thin solid lines show the results of a single re-measurement from 500 to 750 GHz.

The calibration standards were re-measured 44 times with a 20 mN contact force and the results at 625 GHz are shown in Fig. 3.35. The spread of these data indicate the

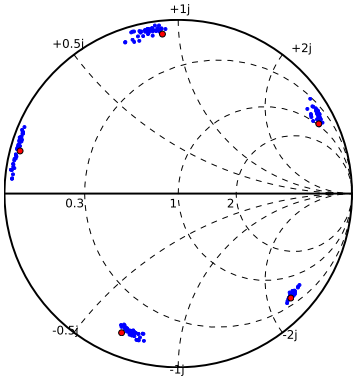


FIGURE 3.35: Red dots indicate the standards and blue dots indicate the measurement results with $\mathbf{E}_1$. (@625 GHz).

repeatability of measuring the calibration standards. As shown in the figure, different calibration standards have different measurement repeatability.

A Monte Carlo simulation was developed to identify the major error source. To simplify the discussion, the reflection coefficient measured at the network analyzer waveguide test port, Γ^M, is related to the error coefficient network, $\mathbf{E}$, and the reflection coefficient of the CPW short, Γ_l, by a measurement equation, f,

$$\Gamma^M = f(\Gamma_l, \mathbf{E}). \tag{3.7}$$

If the error coefficient network is obtained through calibration, the reflection coefficient can be calculated by inverting the measurement equation,

$$\Gamma_l = f^{-1}(\Gamma^M, \mathbf{E}). \tag{3.8}$$

Different contact positions can result in errors in the measurement, Γ^M. To simplify the Monte Carlo simulation, the launch pad is modeled as an extension of the CPW transmission line, ignoring the transition. The simplified model to calculate the measurement, Γ^M, is shown in Fig. 3.36.

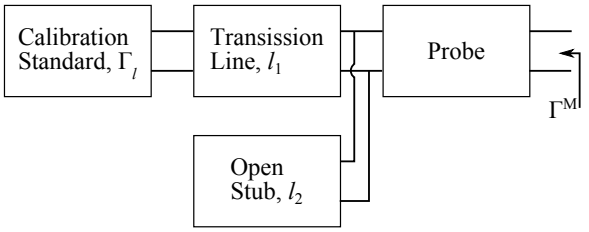


FIGURE 3.36: A simplified model to calculate the reflection coefficient measured at the network analyzer test port, Γ^M.

Changing the contact position at the contact pads changes the length of l_1 and l_2, although $l_1 + l_2$ remains constant. To investigate this positioning error, the probe is assumed to be fully calibrated out and is therefore modeled as a transmission line with zero length, to simplify the calculation. The input impedance of the CPW open is calculated by,

$$Z_{open} = -jZ_0 \cot(\beta l_2).$$

Where β is the propagation constant and Z_0 is the characteristic impedance of the CPW, 50 Ω. A sample set of error-free measurements is first generated with $l_1 = 90$ μm and $l_2 = 10$ μm (The target contact point is set to the center of the contact pad). The error coefficient network, **E**, is obtain by applying the calibration algorithm on this set of measurements. The calibration standards, short and delay shorts, are modeled using HFSS. The positioning error, δ, is assumed to be uniformly distributed between -2 μm to $+2$ μm. 50 sample measurements are generated for each calibration standard with $l_1 + \delta$ and $l_2 - \delta$ and the positioning errors are independent. These sample measurements are corrected using the error coefficient network, **E**, and Eq. (3.8). The results are shown in Fig. 3.37. Different calibration standards have different measurement repeatability due to the open stub. It is also found that increasing the length of l_2 (moving the target contact point further away from the open end) resulted in greater phase error in the calibration standards. Comparing Fig. 3.37 and Fig. 3.35, we conclude that the dominant uncertainty in these on-wafer measurements is positioning error.

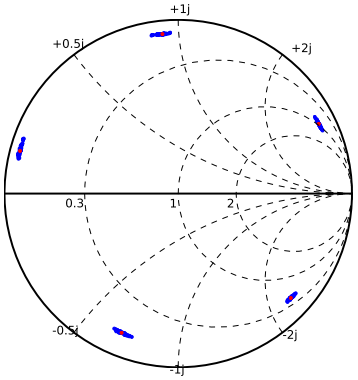


FIGURE 3.37: Reflection coefficient of calibration standards. Red dots indicate the standards without positioning error and blue dots indicate the Monte Carlo simulation results of the standards with positioning error. (@625 GHz)

3.3.2 Measurement Accuracy

From the repeatability of calibration standards, the on-wafer measurement accuracy can be estimated based on the calibration method used. Reck *et al.* use a method presented by Wong [44] to propagate the error in the calibration standards to that of a calibrated on-wafer measurement [45]. However the on-wafer measurement error is overestimated in [45]. Instead of error propagation, this section uses Monte Carlo simulation to estimate the measurement accuracy based on the measurements of calibration standards.

By doing 45 different calibrations, 45 error coefficient networks are obtained:

$$\mathbf{E}_1, \mathbf{E}_2, \mathbf{E}_3 ... \mathbf{E}_{45}$$

Assume the true error coefficient network is,

$$\mathbf{E_t} = mean(\mathbf{E}_1, \mathbf{E}_2, \mathbf{E}_3 ... \mathbf{E}_{45}).$$

When only a single calibration is performed, we could end up with any $\mathbf{E}_i$ (i = 1,2,3...45) of the 45 error coefficient networks. The difference between $\mathbf{E}_i$ and the true error coefficient network $\mathbf{E_t}$ will result in measurement error. The measurement of a fictious reflection coefficient under test, Γ^M, can be calculated using the true error coefficient network, $\mathbf{E_t}$, and Eq. (3.7). Then the calibrated measurement results can be calculated

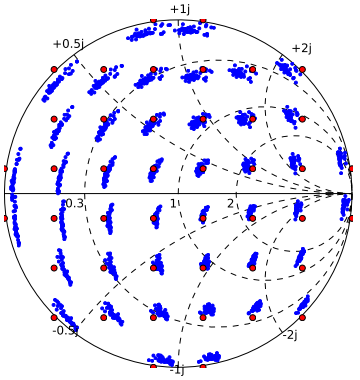


FIGURE 3.38: Red dots indicate the fictious reflection coefficient under test and blue dots indicate the "measurement" results with the error coefficient networks $\mathbf{E}_1$,$\mathbf{E}_2$, $\mathbf{E}_3$...$\mathbf{E}_{45}$. (@625 GHz).

using the error coefficient network, $\mathbf{E}_i$, and Eq. (3.8) for each of the 45 error networks. The Monte Carlo simulation results are shown in Fig. 3.38. Red dots indicate the fictious reflection coefficient under test and blue dots indicate the measurement results with $\mathbf{E}_1$,$\mathbf{E}_2$, $\mathbf{E}_3$...$\mathbf{E}_{45}$ as their error coefficient networks at 625 GHz.

This Monte Carlo simulation makes no assumption about the error distribution that requires the error to be stationary, which we found is not true due to phase drift in the network analyzer. The 45 calibrations are measurements collected over 3.5 hours. The results are presented as shown in Fig. 3.38 rather than with a standard deviation, because no assumption about the error distribution can be made and we would like to distinguish the difference between phase error and magnitude error.

3.3.3 Performance Variation

As shown in the previous section, the S-parameters of the micromachined probe are obtained by one-port two-tier calibration. The positioning error will result in uncertainty in the error coefficient network, $\mathbf{E}$, or the S-parameters of the probe that includes the launch pad and CPW up to the reference plane. The sensitivity of the probe measurement results to the positioning error is measured by attaching a probe to a network analyzer and measuring the corresponding S-parameters five times by performing five second-tier calibrations over 30 min. During the second-tier calibration, the contact force is 20 mN. The uncertainty shown in this measurement unavoidably includes the

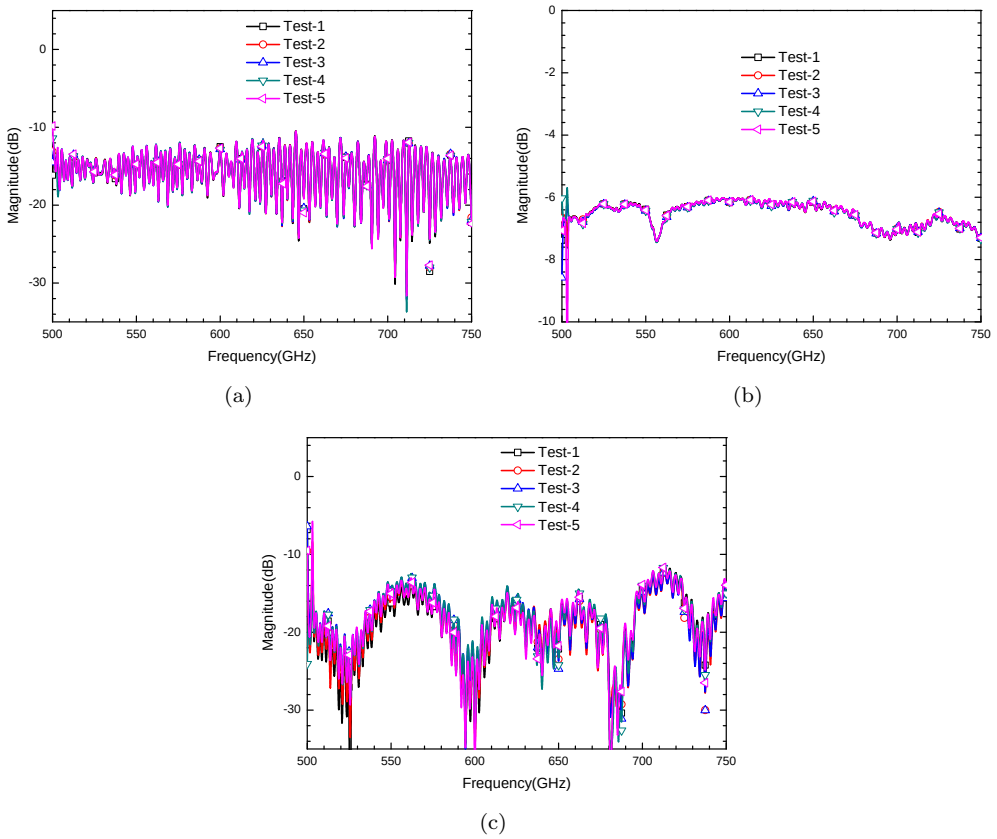


FIGURE 3.39: Five measurements of a micromachined probe's S-parameters. (a) Magnitude of S_{11} (Waveguide port); (b) Magnitude of S_{21}; (c) Magnitude of S_{22} (CPW port).

uncertainty due to the noise and phase drift of the network analyzer. However, as shown in the previous section, the dominate error source is positioning error. The probe S-parameter results are shown in Fig. 3.39. As can be seen, the uncertainty in the return loss at the CPW port is greater than that at the waveguide port. The positioning error will cause uncertainty in the return loss at both ports, but the insertion loss is about 6 dB, therefore the positioning error has much less impact in the return loss at the waveguide port. The variation in insertion loss across measurement is negligible.

As shown in Fig. 2.2, recesses are milled into the waveguide block with a precision of ± 3 μm. The probe chip extents are defined by microfabrication, which has a better than ± 2 μm precision. The probe chip drops into these recesses and is subsequently aligned to the block to better than ± 5 μm precision. The fabrication process also introduces probe chip variations across the wafer, especially from misalignment in lithography. The uncertainty both in chip fabrication and assembly will result in variations in the

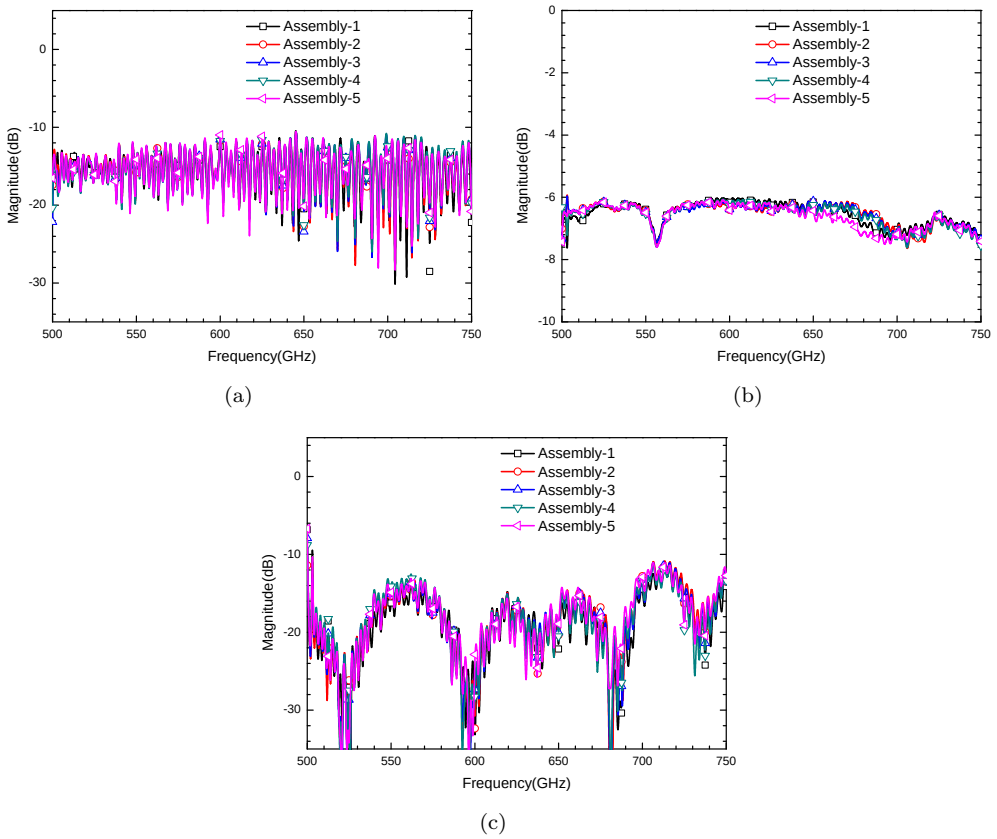


FIGURE 3.40: Measured S-parameters of the same micromachined probe chip mounted in the waveguide block five times. (a) Magnitude of S_{11} (Waveguide port); (b) Magnitude of S_{21}; (c) Magnitude of S_{22} (CPW port).

probe performance from chip to chip. The sensitivity of the probe to the alignment precision is measured by mounting the same probe chip to a waveguide block five times and measuring the corresponding scattering parameters. These measurement results are shown in Fig. 3.40. The return loss variation at the waveguide port across assembly is worse than the return loss variation across measurements due to the uncertainty in waveguide connection [46]. The probes have shown a lower than 0.6 dB variation across assembly for insertion loss.

The probe performance with five different probe chips of the same design is shown in Fig. 3.41. The performance variations are due to the uncertainty both in chip fabrication and assembly. Therefore the variations are slightly greater. The probes have shown a lower than 1 dB variation across probes for insertion loss. The return loss varies across probes, but are better than 10 dB from 500 to 750 GHz. The performance variations due to the uncertainty in chip fabrication and/or assembly will not cause measurement

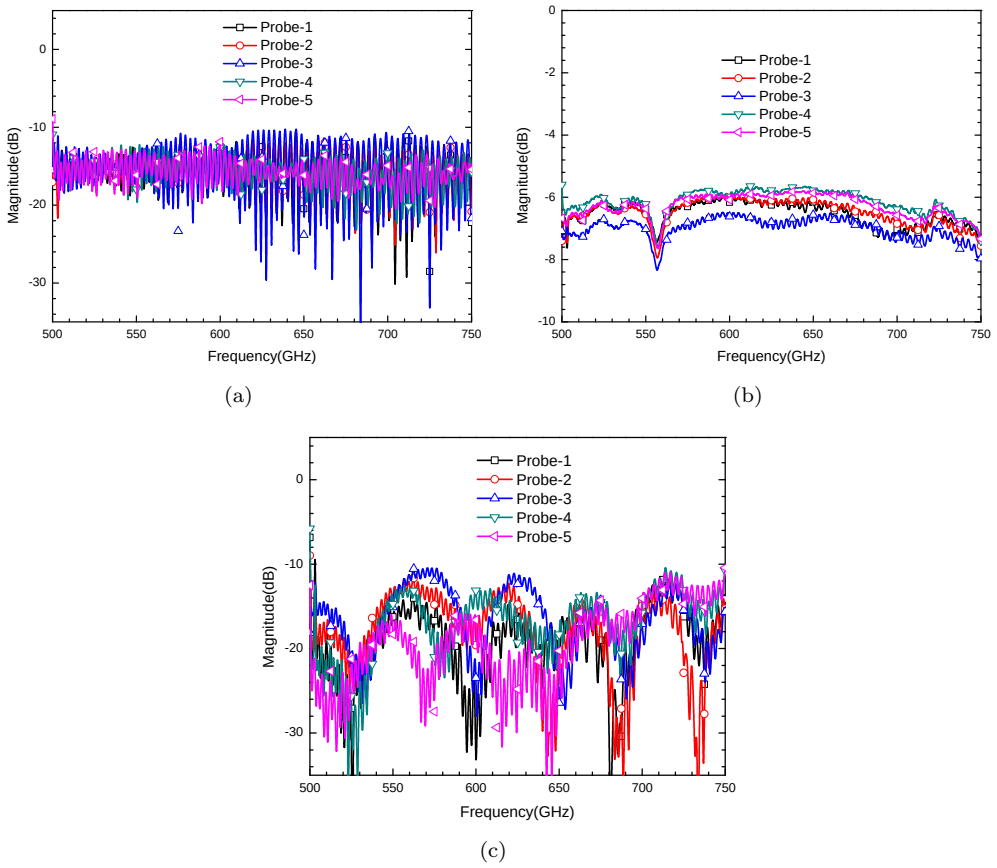


FIGURE 3.41: Measured S-parameters of three different micromachined probe chips. (a) Magnitude of S_{11} (Waveguide port); (b) Magnitude of S_{21}; (c) Magnitude of S_{22} (CPW port).

error in the final measurement results since these variations are calibrated out.

3.3.4 Reliability

The on-wafer probes are designed to skate on the contact pad to break through surface contamination and roughness to ensure a low resistance contact. However, this skating action adds to the wear of the probes. How quickly the probes wear depends on factors including contact force as well as probe tip and contact pad materials.

The setup in Fig. 3.27 is used again to test the lifetime of the micromachined probes. A motorized stage is raised up gradually until the contact force reaches 20 mN. Then the motor stage is lowered until the probe and substrate are separated. This completes one contact cycle. The scattering parameters of the micromachined probe are measured

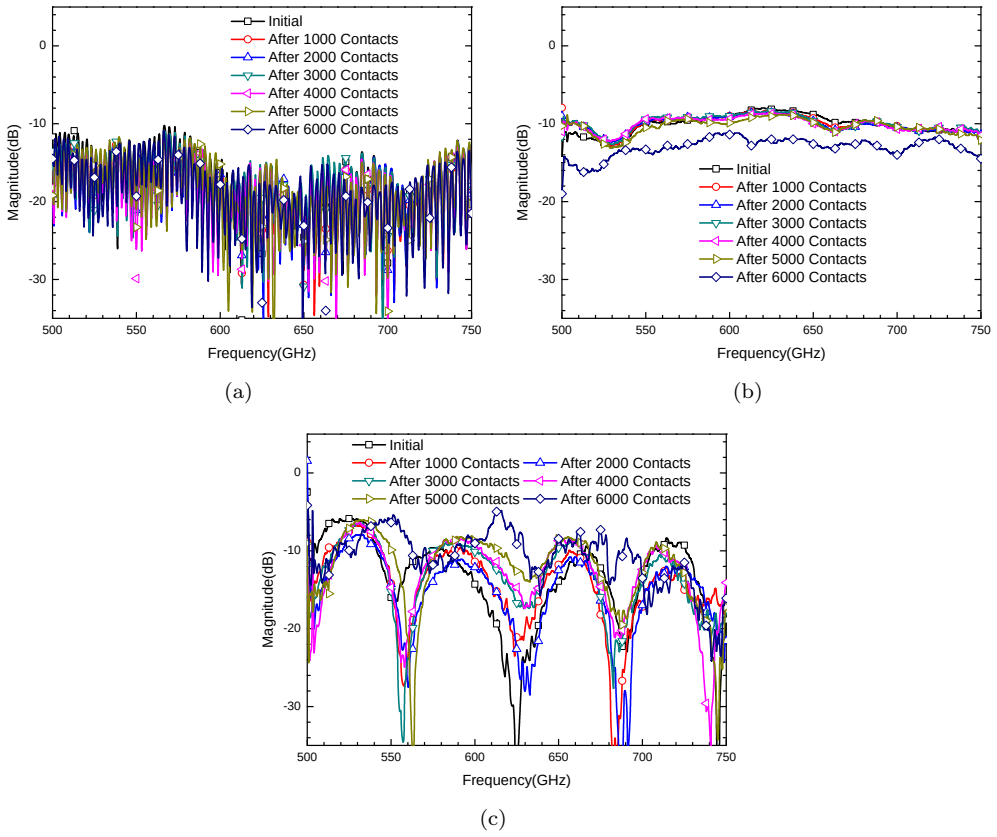
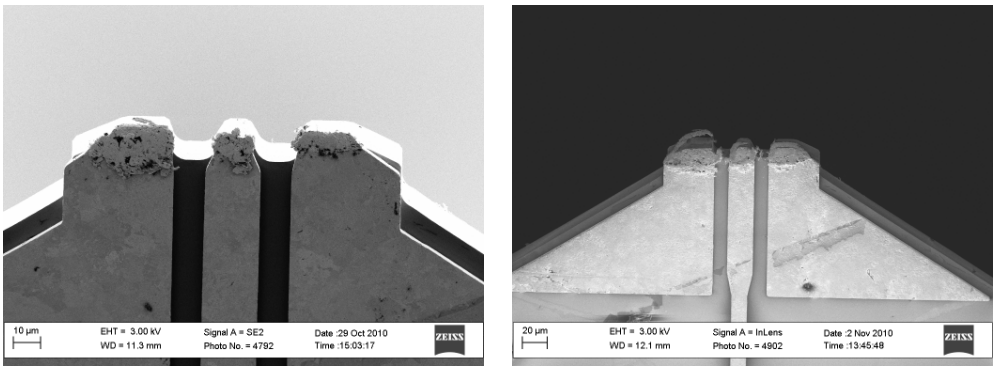


FIGURE 3.42: Measured S-parameters of the micromachined probe with soft gold doing lifetime testing. (a) Magnitude of S_{11} (Waveguide side); (b) Magnitude of S_{21}; (c) Magnitude of S_{22} (CPW side).

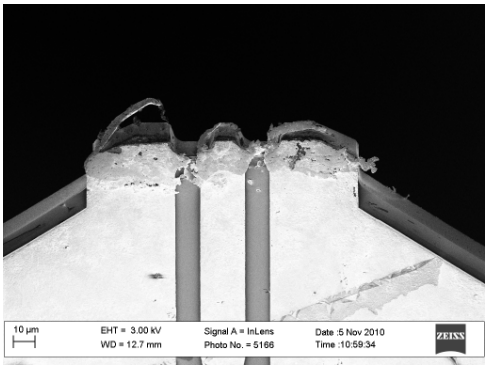
and pictures of the probe tips are taken with a scanning electron microscope (SEM) after every 1000 contact cycles.

Initially, the micromachined probe used a soft gold plating solution, Technic Gold 25ES RTU from Technic Inc. The measured results of probe Design-I are shown in Fig. 3.42. Since the three designs in this thesis share the same mechanical design, the other designs should show similar lifetime behavior. The micromachined probe maintained consistent performance through 5000 contacts and then was found to have degraded upon testing after 6000 contacts.

Scanning electron microscope images of the probe tips after 10, 3000 and 6000 contacts are shown in Fig. 3.43. The images indicate that the failure is due to a combination of displacement of the electroplated gold and wear of the silicon supporting the contact tip. The displacement of the gold is of particular concern since the material will be pushed into the area between the ground and signal contact tips. This leads to shorting



(a) (b)



(c)

FIGURE 3.43: SEM images of the micromachined probe tips with soft gold after (a) 10 contacts; (b) 3000 contacts; (c) 6000 contacts.

of the GSG probe tips before the contact metal is abrasively removed.

In order to improve the probe reliability, the probe Design-III uses a 0.5 μm thick hard gold capping layer over top of a 2 μm thick layer of soft gold. The hard gold is deposited using the Orosene 990HS cyanide based gold plating solution, which produces cobalt hardened gold films of 99.7% purity with hardness twice that of the soft gold according to plating solution manufacturer. The hard gold is designed for applications where certain sliding wear is needed.

The S-parameters results from the reliability test on the probe Design-III are shown in Fig. 3.44. The micromachined probe maintained consistent performance through 20,000 contacts. The SEM images, shown in Figs. 3.45 and 3.46, clearly show significantly less mechanical wear compared to soft gold.

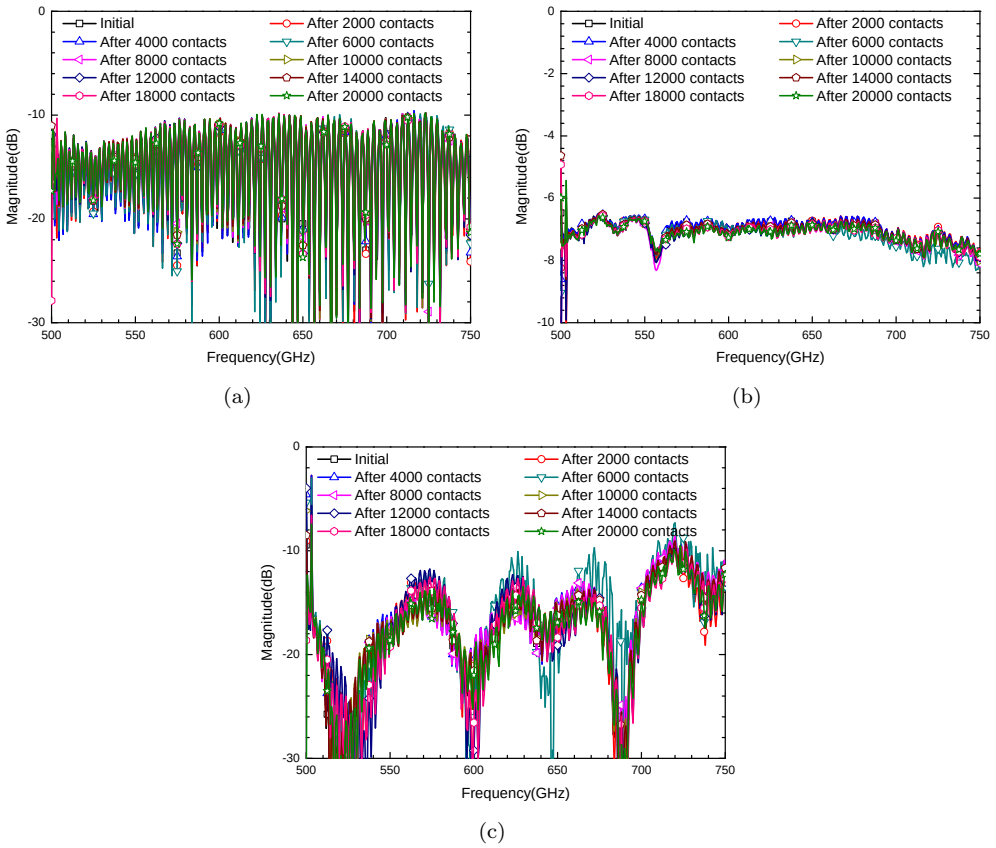
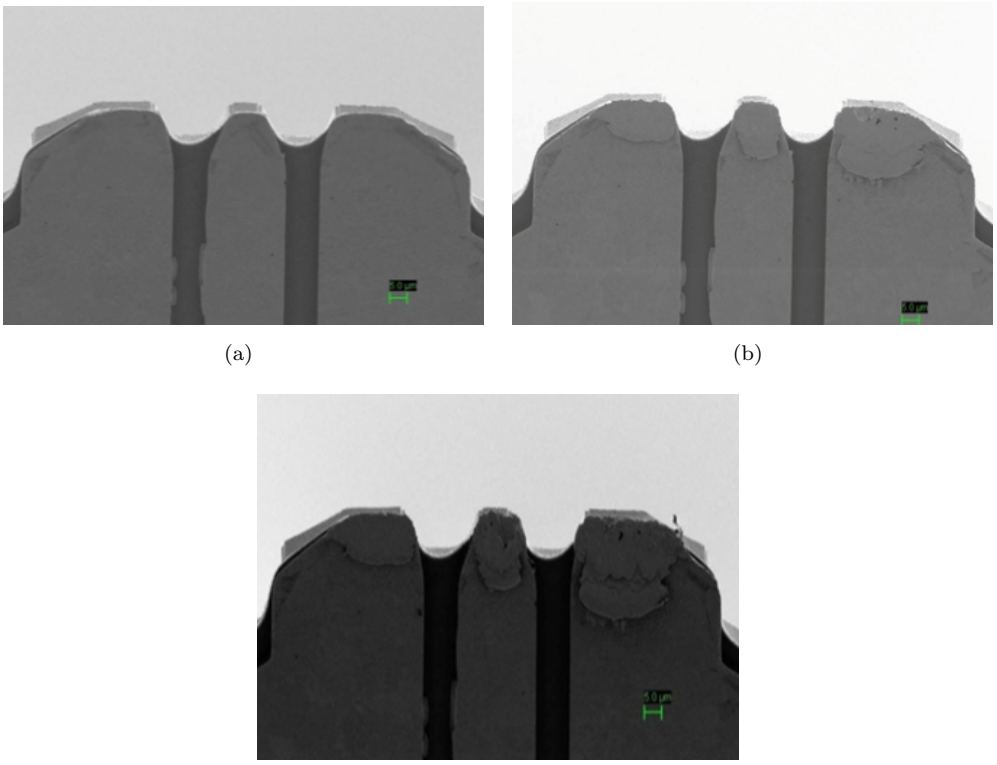


FIGURE 3.44: Measured S-parameters of the micromachined probe doing lifetime testing. The probe is fabricated with 2 μm soft gold capped with another 0.5 μm cobalt harden gold for the beamlead layer. (a) Magnitude of S_{11} (Waveguide side); (b) Magnitude of S_{21}; (c) Magnitude of S_{22} (CPW side).



(a) (b)

(c)

FIGURE 3.45: SEM images of the micromachined probe tips after (a) 10 contacts; (b) 3000 contacts; (c) 6000 contacts. The probe is fabricated with 2 μm soft gold capped with another 0.5 μm cobalt harden gold for the beam-lead layer.

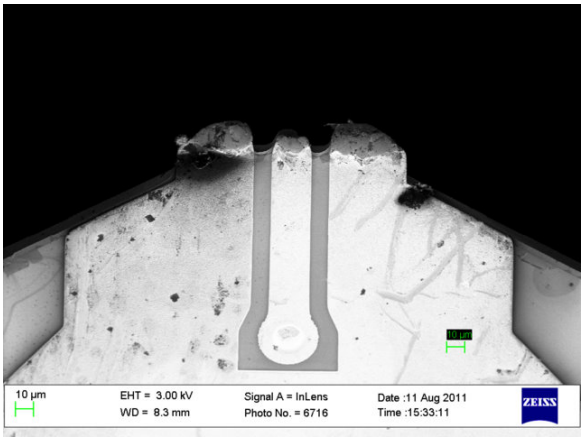


FIGURE 3.46: SEM images of the micromachined probe tips after 20,000 contacts. The probe is fabricated with 2 μm soft gold capped with another 0.5 μm cobalt harden gold for the beamlead layer.

Part II

Vertical RF Transition for 3D Heterogeneous Integration

Chapter 4

Vertical RF Transition Design

4.1 Introduction

In this chapter, a vertical RF transition with mechanical fit is introduced for heterogeneous submillimeter-wave circuit integration. The vertical RF transition consists of interlocking SU-8 structures and embedded metal micro-bumps, illustrated in Fig. 4.1. In this example, the three gold micro-bumps form the ground-signal-ground (GSG) structure, connecting two sets of CPW lines in the two face-to-face chips. This configuration is best suited for directly contacting CPW traces through vertical micro-bumps.

SU-8 is an ultra-thick photoresist designed for micromachining and other microelectronic applications. The SU-8 serves two main functions: an electroplating mold (as shown on the bottom chip in Fig. 4.1) and mating structure (as shown on the top chip

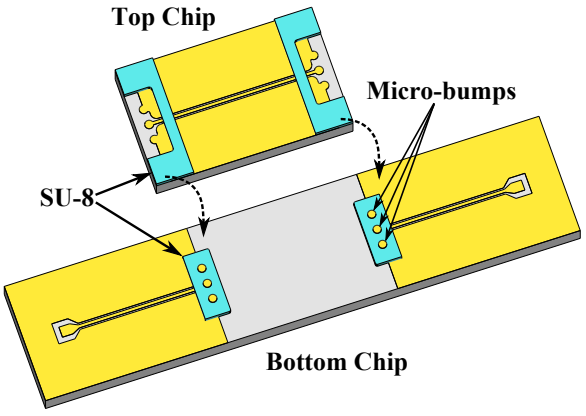


FIGURE 4.1: The structure of proposed vertical transition with mechanical fit.

in Fig. 4.1). SU-8 can achieve high aspect ratios, over 10:1, and various thicknesses from 5 μm to 1200 μm [47]. The size and pitch capabilities of the plated micro-bumps are determined by the SU-8 mold. Using SU-8 enables optimization of plated micro-bump dimensions for various applications. Because SU-8 is chemically and thermally stable after being imaged and cured, the SU-8 plating mold is left on the device as part of the interlocking structures to prevent misalignment during assembly.

The benefits of the mechanical fit include:

- *Providing an alignment guide for assembly.*
  The interlocking structures will prevent misalignment during assembly and will keep the die and the substrate in place during thermocompression bonding.
- *Improving reliability by supporting the micro-bumps with SU-8.*
  Regular micro-bumps deform under compression bonding [48]. The SU-8 structures protect the gold microbumps from excessive deformation during the bonding process. Epoxy-based underfill has been used to improve the reliability of flip-chip interconnects [21]. However, this strategy requires taking the underfill effect into account in advance for both interconnect and chip designs. For the design presented in this work, the shape of the mechanical fit structures can be specifically designed to avoid sensitive areas that could detune active RF chips while serving as an underfill in less sensitive areas.
- *Separating adjacent chips for improved RF isolation.*
  The additional space in between chips due to the height of the mechanical fit structures helps to reduce cross-coupling and also enables the integration/self-packaging of high aspect-ratio 3D and MEMS structures between assembled layers.

The following sections present designs of vertical transitions with mechanical fit for the millimeter-waves frequency range.

4.2 Millimeter-wave Vertical Transition Design

The vertical transition was first designed for *Ka*-band (up to 50 GHz) and then the design was scaled to *W*-band (up to 110 GHz).

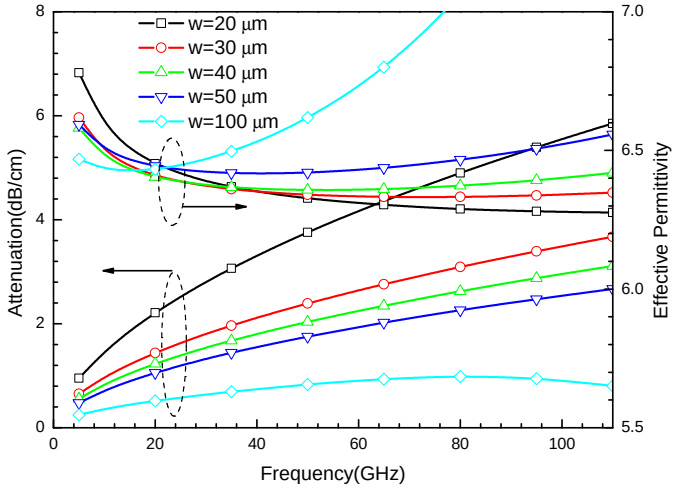


FIGURE 4.2: Full-wave electromagnetic simulation of effective permittivity and attenuation for different signal conductor widths of CPW ($Z_0 = 50\,\Omega$) on high-resistivity silicon substrate (>2000 Ω·cm).

4.2.1 CPW Dimension Selection

To design the vertical RF transition, the first step is to choose CPW dimensions that represent typical traces used in monolithic microwave integrated circuit (MMIC) design. The CPW dimensions used in this work are chosen based on full-wave electromagnetic simulation using Ansoft® HFSS. The characteristic impedance (Z_0) is mainly determined by the ratio of the center conductor width (w) to the gap (g) between the center conductor and ground planes and is not significantly affected by the width of the ground planes [49]. Fig. 4.2 shows the effective permittivity and attenuation for different center conductor widths for CPW ($Z_0 = 50\,\Omega$) on a high resistivity silicon substrate. Larger widths have lower attenuation but higher dispersion effects. Die area is also a consideration while choosing dimensions. Choosing a center conductor width of 30 μm provides a compromise between attenuation loss, dispersion, and die area.

4.2.2 *Ka*-band Design

The metal micro-bumps are embedded in the interlocking SU-8 structures with a relative dielectric constant of ∼4 [50]. The return loss of the vertical transition is determined by this material parameter as well as the radius, height, and spacing of the micro-bumps. The vertical RF transition can be represented by a pi-network circuit model consisting of

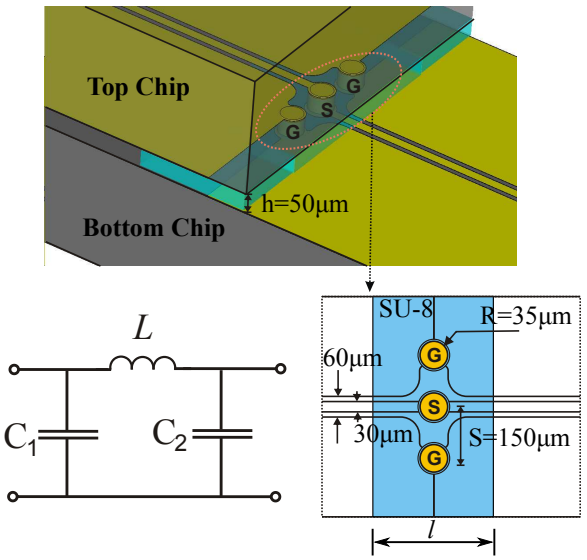


FIGURE 4.3: Dimensions of the *Ka*-band vertical transition and its Pi-network circuit model; The substrates are 380 μm thick high resistivity silicon(>2000 Ω·cm).

one series inductor, L, and two parallel capacitors, C_1 and C_2 [22], as shown in Fig. 4.3. If needed, a short section of high-impedance CPW can be used to compensate for any extra capacitance in the transition region [51].

A *Ka*-band design with CPW dimensions of w=30 μm and g=15 μm is shown in Fig. 4.3. The transition is designed by studying the influence of the transition geometrical parameters using HFSS to simulate the S-parameters of a single transition. The vertical transitions are initially simulated using HFSS with no loss (σ=∞ and tanδ=0).

The circuit model parameters are obtained from the HFSS simulation by using the admittance matrix representation of the network[52]. A pi-network circuit model can be represented by its admittance matrix as shown in Fig. 4.4. S-parameters obtained from the HFSS simulation are first converted to the admittance matrix. The series inductor, L, and the two parallel capacitors, C_1 and C_2, can be calculated by,

$$L = \frac{1}{2\pi f \cdot Im(y_{12})}$$

$$C_1 = \frac{Im(y_{11} + y_{12})}{2\pi f}$$

$$C_2 = \frac{Im(y_{22} + y_{12})}{2\pi f}$$

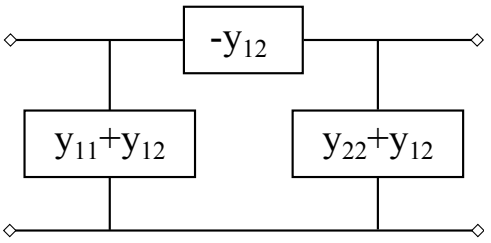


FIGURE 4.4: The admittance matrix representation of a pi-network circuit.

The influence of the spacing of the micro-bumps is simulated and the results are shown in Fig. 4.5 (a). In general, better return loss is achieved with larger spacing (S in Fig. 4.3) since the increased path length of the ground current raises the inductance, which compensates capacitance in the transition region. Increasing the spacing of the microbumps improves return loss, but it also increases parasitic coupling into the unwanted substrate mode (parallel-plate line (PPL) mode) [18]. As shown in Fig. 4.5 (a), with 500 μm spacing , the return loss quickly reduces above 40 GHz. Because a compact vertical transition is preferred, a 150 μm spacing is chosen. Also 150 μm is compatible with commonly used RF GSG launch pads of integrated circuits working under 50 GHz for on-wafer tests.

Varying the height of the micro-bumps (equivalently the thickness of the SU-8), the return loss of the transition changes slightly, as shown in Fig. 4.5 (b). In order to minimize the coupling between the top and bottom chips, the height should be at least 0.3 times the CPW ground-to-ground spacing [53]. Increasing the height between the chips improves the isolation between the chips, but also increases the fabrication difficulty. Thicker SU-8 requires a multilayer deposition and introduces additional loss. Therefore, 50 μm is chosen as the thickness of the SU-8 for the Ka-band design, which is 0.85 times the CPW ground-to-ground spacing.

The influence of the radius of the micro-bumps is also simulated. As shown in Fig. 4.5 (c), a smaller radius results in better return loss. However, for the same micro-bump height, a smaller radius results in a higher aspect-ratio for the SU-8 features, which increases the difficulty of fabrication. A radius of 35 μm is chosen for the Ka-band design, which is relatively easy to realize in a 50 μm thick SU-8 layer.

These conclusions about the influence of the transition geometrical parameters agree

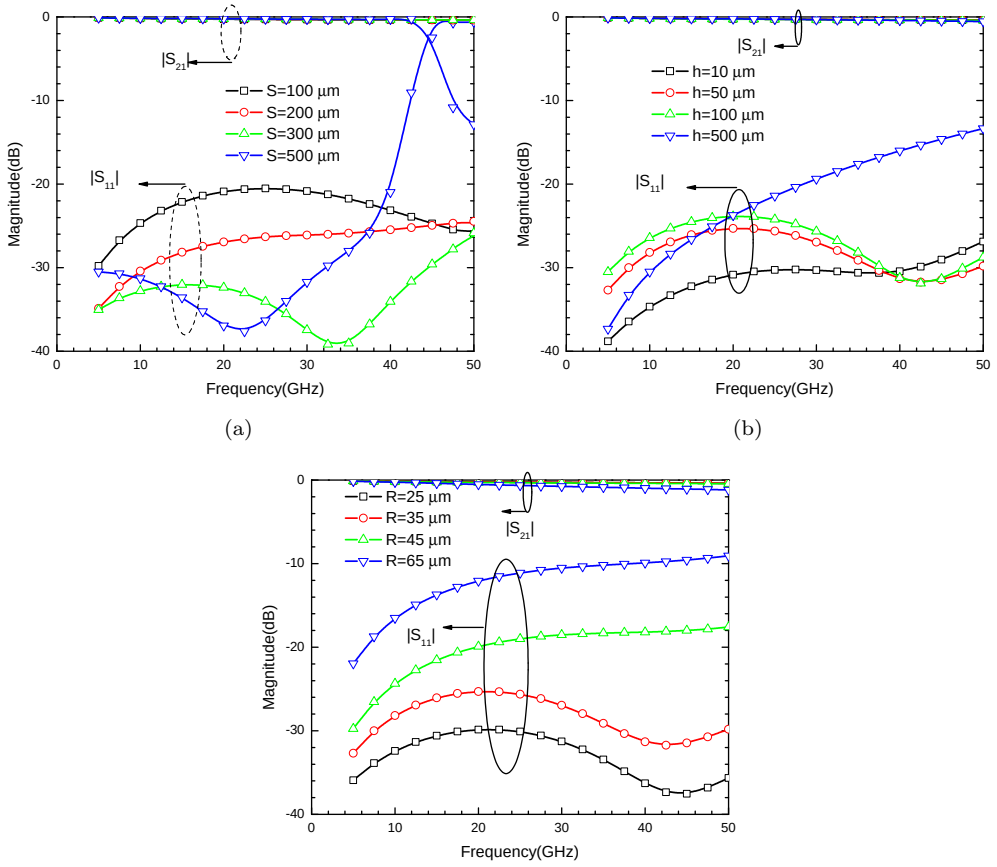


FIGURE 4.5: (a) S-parameters of the transition vs. the spacing of the micro-bumps, with h=50 μm and R=35 μm; (b) S-parameters of the transition vs. the height of the micro-bumps, with R=35 μm and S=150 μm; (c) S-parameters of the transition vs. the radius of the micro-bumps, with h=55 μm and S=150 μm.

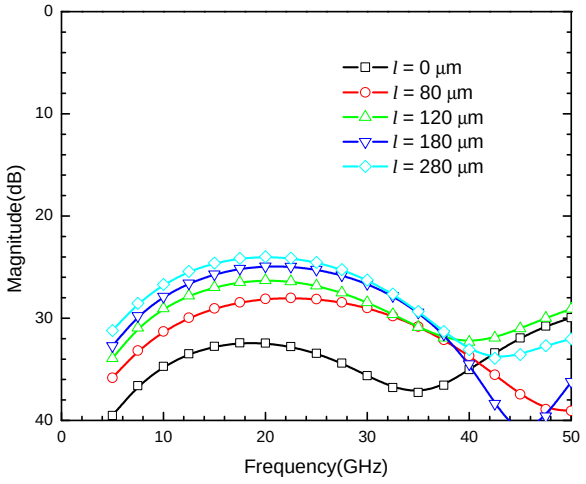


FIGURE 4.6: Return loss of the transition vs. length, l, of the SU-8 structure with h=50 μm, R=35 μm, and S=150 μm.

TABLE 4.1: Dimensions and Circuits Parameters of *Ka*-band Designs

Dimensions	h	R	S
	50 μm	35 μm	150 μm
Circuit Parameters	C_1	L	C_2
	32 fF	120 pH	32 fF

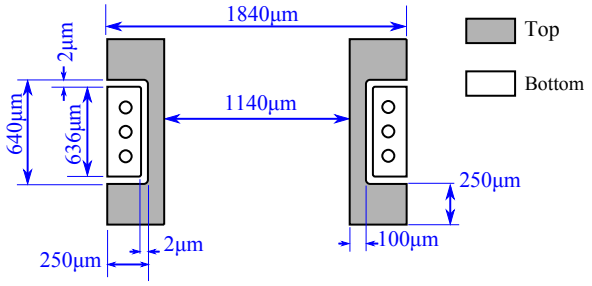


FIGURE 4.7: Dimensions of interlocking structures in *Ka*-band design.

well with the study of flip-chip interconnects without SU-8 [18]. Surrounding the interconnects with SU-8 increases the capacitance, which reduces return loss, as shown in Fig. 4.6. Return loss is reduced when a SU-8 structure (l=80 μm) is added. However, a further extension of the SU-8 structure (l>80 μm) only result in a slightly change in return loss, since only the dielectric next to the interconnect can change the capacitance. It is difficult to make l less than the diameter of the microbump.

With these optimized dimensions for the *Ka*-band design, the transition is simulated to have better than 25 dB return loss up to 50 GHz and a compensation network in the CPW transmission line is not needed. The dimensions and corresponding circuit parameters of *Ka*-band designs are detailed in the Tables 4.1.

Interlocking structures for the *Ka*-band design are shown in Fig. 4.7. The minimum size of the SU-8 plating mold is limited by the size of the microbumps and their spacing. In this case, with a microbump diameter of 70 μm, the plating mold width is set as 248 μm (greater than 3 times the microbump diameter). A simple top-chip mating structure is used in this design, however alternatively shaped mating structures are possible. Two alternative interlocking structures are shown in Fig. 4.8. The mating structures on the top chip in Fig. 4.8 (a) avoid CPW lines to reduce the impact on the top chip. The interlocking structures shown in Fig. 4.8(b) enable the self-packaging of high aspect-ratio 3D and MEMS structures between the bottom and top chips.

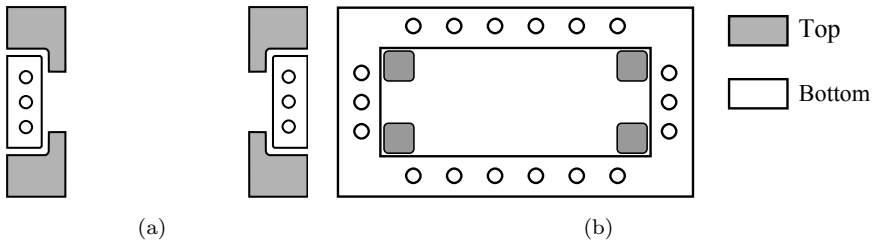


FIGURE 4.8: Alternative interlocking structures.

When the mating structures are designed, two things need to be kept in mind: aspect ratio and adhesion. The aspect ratio of the mating structure cannot exceed SU-8's capability of 10:1 and the mating structure surface area needs to be large enough to provide sufficient adhesion to the chip to withstand the assembly and bonding process with a high yield. The adhesion between SU-8 and the chip is determined by the contact area and surface material on which the SU-8 is deposited. Increasing the contact area can improve adhesion and reduce the aspect ratio, whereas reducing contact area may cause a reduction in yield. SU-8 3000 from MicroChem®, used in this work, is an improved formulation of SU-8 for better adhesion. According to shear analysis, SU-8 3000 on silicon nitride (used in this work) can withstand a shear stress up to 73 MPa whereas on gold it can only stand up to 47 MPa [54].

The clearance between the interlocking structures defines the alignment accuracy between the top chip and the bottom chip. A larger clearance makes the assembly easier, but alignment accuracy is reduced. Interlocking structures with clearances of 1 μm, 2 μm and 5 μm, were fabricated and tested. The structures with a 1 μm clearance were unable to be assembled successfully. However the 2 μm clearance structures worked well and were used for both designs presented in this work, resulting in an alignment accuracy of ± 2 μm. The 5 μm clearance structures provided too loose of a fit for these aspect ratios and were never successfully bonded using the low-cost techniques presented in this work.

4.2.3 *W*-band Design

A similar transition is designed at W-band by following the same design procedure, studying the influence of the transition geometrical parameters using HFSS to simulate the S-parameters of a single transition. The influences of the transition geometrical

TABLE 4.2: Dimensions and Circuits Parameters of W-band Designs

Dimensions	**h**	**R**	**S**
	35 μm	15 μm	70 μm
Circuit Parameters	C_1	L	C_2
	18 fF	65 pH	18 fF

parameters are summarized in Fig. 4.9. These conclusions agree well with the study of Ka-band vertical transition in Subsection 4.2.2.

It was found that varying the height (h in Fig. 4.3) of the micro-bumps (equivalently the thickness of the SU-8), has little effect on the return loss of the transition. However, a smaller radius (R in Fig. 4.3) results in better return loss. In addition, better return loss is achieved with larger spacing (S in Fig. 4.3).

Surrounding the interconnects with SU-8 increases the capacitance, which reduces return loss, as shown in Fig. 4.10. Return loss is reduced by 2 dB at 100 GHz when a SU-8 structure (l=40 μm) is added. Return loss is reduced further as the SU-8 structure is extended to l=60 μm. However, a further extension of the SU-8 structure (l>60 μm) does not result in any noticeable change in return loss. It is difficult to make l less than the diameter of the microbump.

Increasing the spacing of the microbumps improves return loss, but it also increases parasitic coupling into the unwanted substrate mode (parallel-plate line (PPL) mode) [18]. Instead, a 50 μm length of 65 Ω CPW is added to the W-bnad design to improve return loss and the simulation results are shown in Fig. 4.11. With the compensation network, the return loss of the transition is improved from 16 dB to >22 dB at frequency range 60–110 GHz. Corresponding circuit parameters of W-band design with high-impedance compensation networks are detailed in the Table 4.2.

Three different W-band test structures were designed. Those three test structures are detailed in Fig. 4.12.

- Test Structure–(a) (shown in Fig. 4.12(a)):

  In this test structure, channel-I (between ports P1 and P2) has back-to-back vertical transitions, whereas channel-II has no vertical transition and is adjacent to

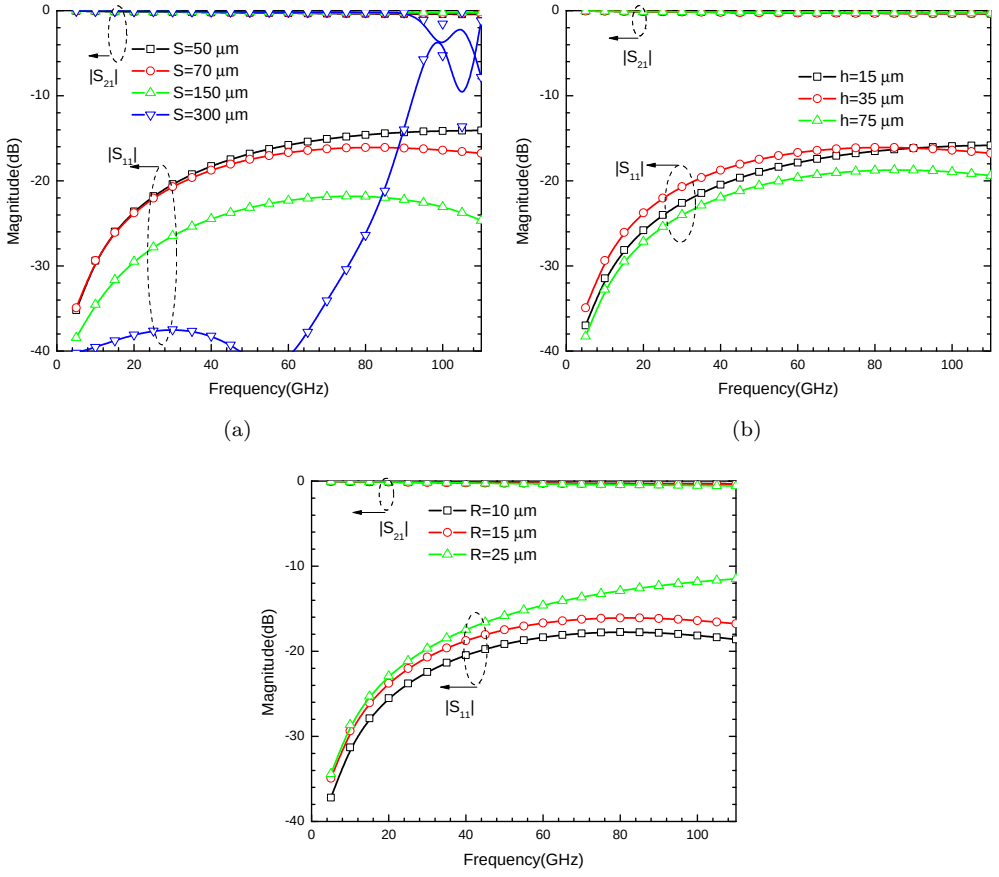


FIGURE 4.9: (a) S-parameters of the transition vs. the spacing of the micro-bumps, with h=35 μm and R=15 μm; (b) S-parameters of the transition vs. the height of the micro-bumps, with R=15 μm and S=70 μm; (c) S-parameters of the transition vs. the radius of the micro-bumps, with h=35 μm and S=70 μm.

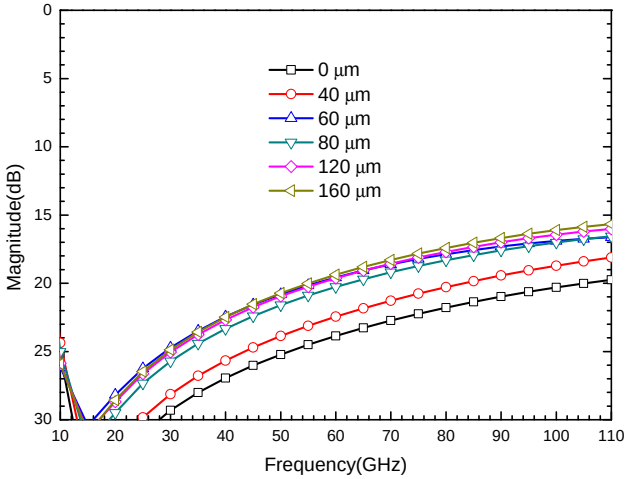


FIGURE 4.10: Return loss of the transition vs. length, l, of the SU-8 structure with h=35 μm, R=15 μm, and S=70 μm.

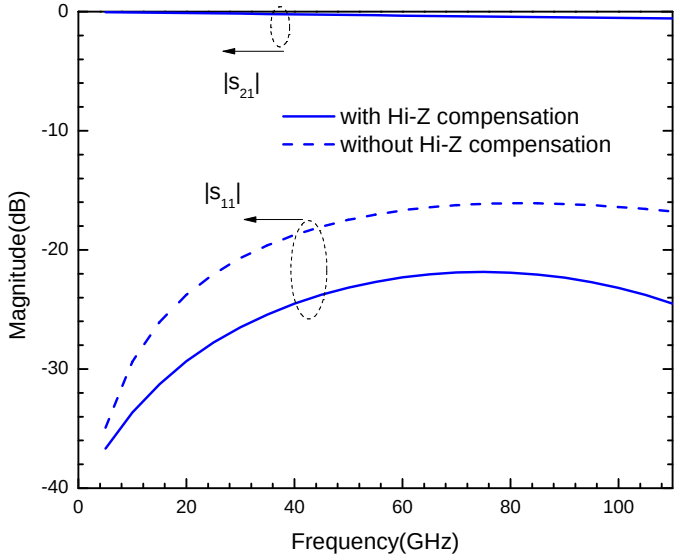


FIGURE 4.11: S-parameters of W-band vertical transition.

channel-I. The center-to-center distance between the two channels is 300 μm. This test structure can be used to de-embed the insertion loss of vertical transition.

- Test Structure–(b) (shown in Fig. Fig. 4.12(b)):

  This test structure is similar to test structure–(a), but both channels in test structure (b) include back-to-back vertical transitions.

- Test Structure –(c) (shown in Fig. Fig. 4.12(c)):

  In this test structure, channel-I (between ports P1 and P4) has back-to-back vertical transitions, while channel-II does not.

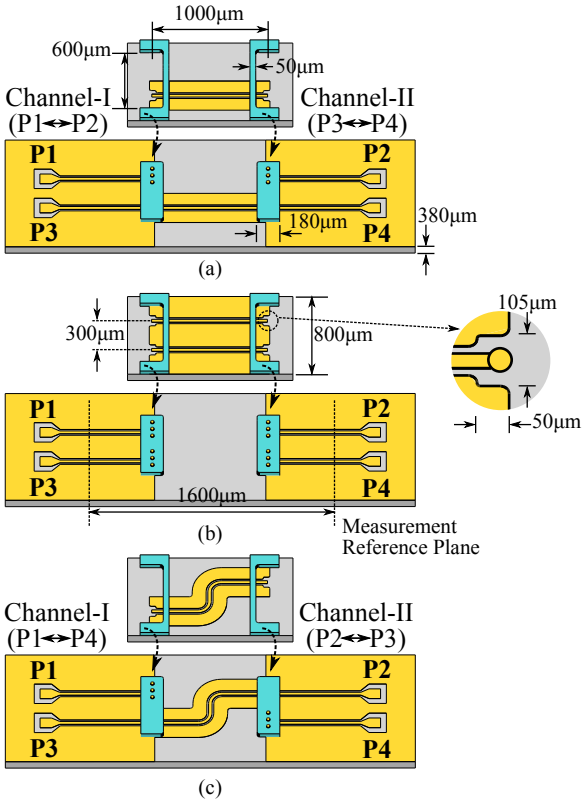


FIGURE 4.12: Three test structures of w-band vertical transition. The thickness of the SU-8 is 36 μm. The dimensions of the vertical transition are detailed in the Fig. 4.3 and Table. 4.2. CPW dimensions are 15/30/15 μm.

Chapter 5

Fabrication and Assembly

5.1 Fabrication

For the test structures presented in this work, the substrates are 380 μm thick high-resistivity silicon (>2000 Ω·cm). Only millimeter-wave vertical transitions were fabricated, but sub-millimeter-wave transitions can be fabricated using the same procedure. The fabrication mainly consists of the following three steps (as detailed in Fig. 5.1):

1. Deposit and pattern metal layers, Ti-Au-Cr(5/800/10 nm), on silicon substrate by lift-off.
2. Spin and define the SU-8 layer.
3. Form gold micro-bumps by electroplating into the SU-8 mold.

A PECVD Si_xN_y layer is deposited upon the metal layers, which serves as a plating mask to prevent Au plating outside the SU-8 mold and is etched using a CF4/O2 RIE after plating. The SU-8 layer for the Ka-band design is deposited by a multilayer SU-8 process [55]. The first spin of SU-8 3025 is 2000 RPM for 60 sec and the second is 3000 RPM for 60 sec. The combination of the two spins creates a smooth 55 μm thick layer. For the W-band design, the SU-8 layer is deposited by a single spin of SU-8 3025 at 2000 RPM for 60 sec, resulting in a 36 μm thick layer.

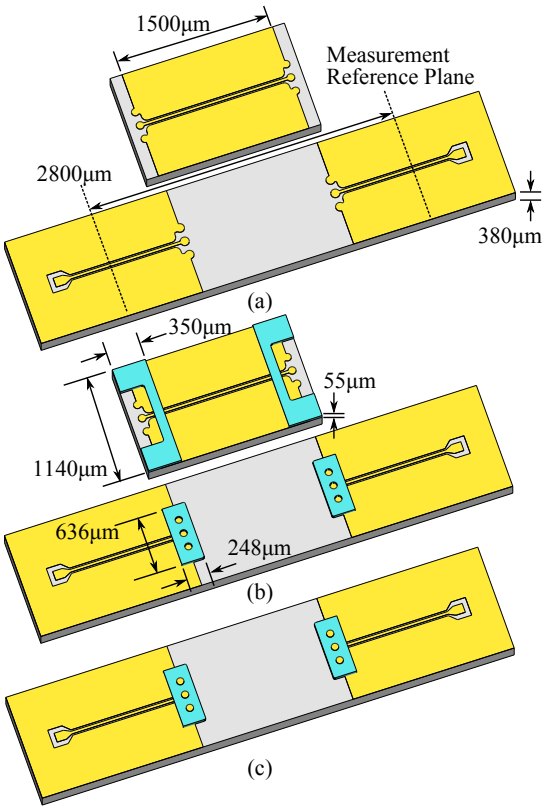
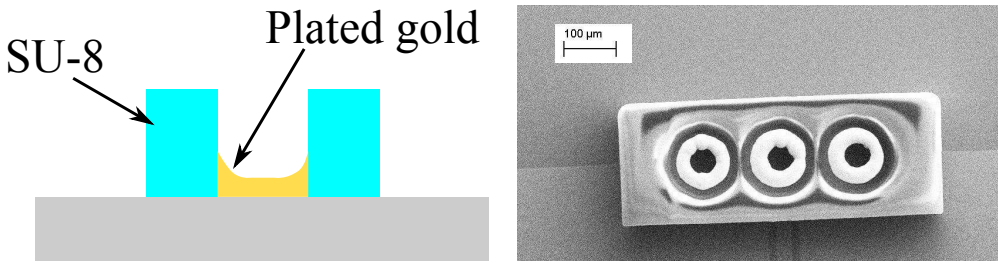


FIGURE 5.1: Process flow for the vertical transition. CPW dimensions are 15/30/15 μm. (a) Deposit and pattern metal layers by lift-off; (b) Spin and define the SU-8 layer; (c) Form gold micro-bumps by electroplating into the SU-8 mold.

The gold micro-bumps are formed by electroplating. The micro-bumps are plated to just over the thickness of the SU-8 mold ($\sim$57 μm for *Ka*-band design) to aid with bonding.

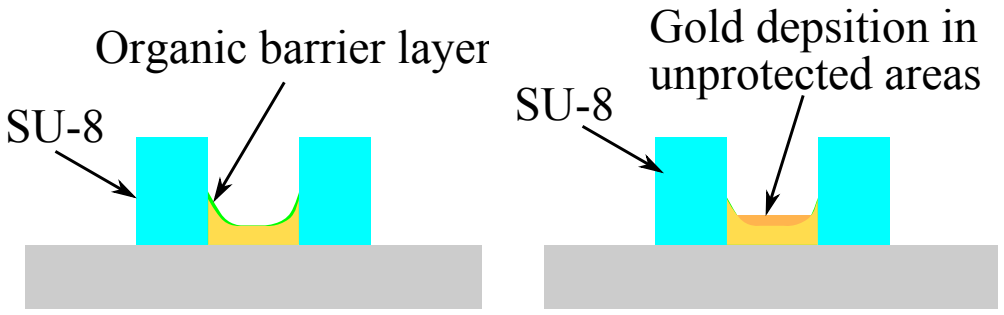
DC plating was first used, however with DC plating, the edges of the holes are more easily accessible for gold ions to be deposited (relative high current density area), as opposed to the center of the holes (relative low current density area). This results in more gold being deposited near the edges of the holes than in the center (as shown in Fig. 5.2). Plating with a lower current density can reduce this problem, but a lower current density results in longer processing time.

Reverse pulse plating is the key to achieve uniform micro-bump height while maintaining acceptable processing times. In reverse pulse plating, the current polarization is swiftly alternated [56]. During the reverse pulse, additives are adsorbed at the surface



(a) (b)

FIGURE 5.2: (a) Cross-sectional view of a DC plated microbump. The edges of the microbump are higher than the center. (b) Scanning electron micrograph of DC plated microbumps in SU-8 mold.



(a) (b)

FIGURE 5.3: The concept of pulse reverse plating. (a) Organic barrier layer is formed during reverse pulse; (b) Gold deposited in areas where organic barrier layer is broken down.

TABLE 5.1: Procedure parameters for pulse reverse plating.

	Current Density	Time
Forward	5 mA/cm^2	240 sec
Reverse	15 mA/cm^2	15 sec

of the plated gold. These adsorbed additives shield the forward current and gold deposition during the forward pulse. The thickness of the additives adsorbed is proportional to the current density, as shown in Fig. 5.3(a). High current density areas will have thicker adsorbed additives than low current density areas. During the forward pulse the organic shield is gradually broken down. More gold will be deposited on the unshielded areas, *i.e.,* the center of holes. By controlling the forward/reverse current density and time ratio, finished gold electroplated microbumps can be achieved. Fig. 5.4 shows a *Ka*-band test sample with the micro-bumps formed. The centers of the micro-bumps are slightly higher than the edges, making bonding easier. The parameters used in the pulse reverse plating are detailed in Table 5.1.

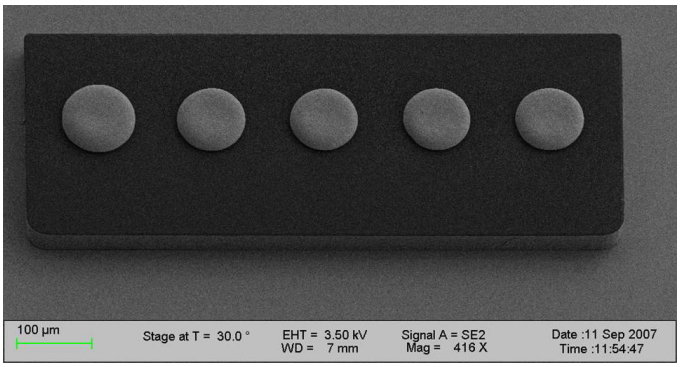


FIGURE 5.4: SEM picture of a test sample with gold micro-bump.

In the fabrication flow above, both the bottom chip with the micro-bumps and the top chip with mating structure are made at the same time. To create the mating structure on previously designed chips, SU-8 structures can be added as the final processing step in the foundry process flow before dicing the wafer. Alternatively, post processing can be performed on die by using a specially designed carrier wafer [57]. Post processing on a previously designed power amplifier[58] was performed successfully by J. Wood at the Virginia Polytechnic Institute and State University, Blacksburg.

The post processing performed on die mainly consists of the following four steps (as detailed in Fig. 5.5) :

1. Etch a cavity into a carrier wafer in order to post-process the diced top chips.
2. Spin SU-8 layer on a top chip held by carrier wafer.
3. Bake, expose, post-exposure bake, and develop SU-8 layer.
4. Remove the top chip with patterned SU-8 from carrier wafer.

A carrier wafer is necessary to planarize the surface of the top chips in order to create the SU-8 pattern for mechanical fit. The carrier wafer is fabricated by etching a cavity in the silicon surface using TMAH etching techniques. The slanted sidewalls of a TMAH-etched cavity aid in the removal of the chip after the SU-8 processing is completed. Matching the cavity depth is critical in establishing the SU-8 height on the chip. Fig. 5.6 shows a top chip held in the cavity of a carrier wafer. With the top chip inside the carrier wafer, SU-8 is spun across the surface in the same manner as previously described. To release the top chip after processing, the carrier wafer is

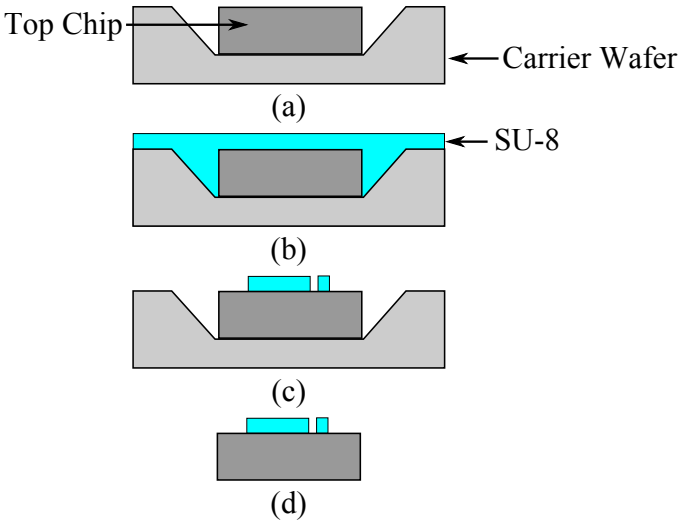


FIGURE 5.5: Process flow for creating SU-8 interlocking structures on previously designed chips.

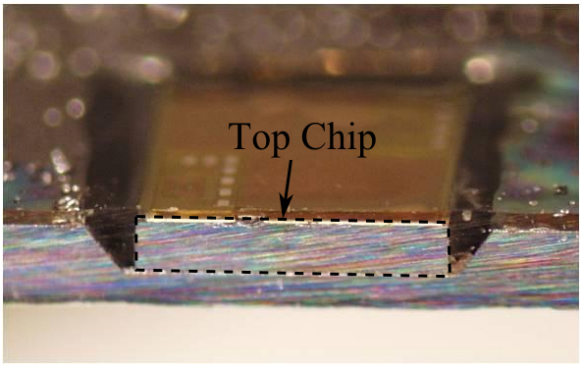


FIGURE 5.6: Cross-sectional view of a top chip in the cavity of a carrier wafer.

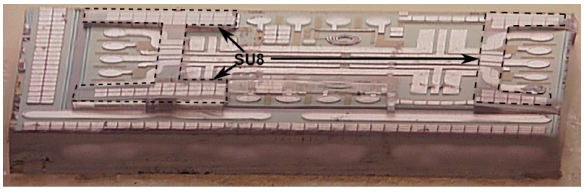


FIGURE 5.7: A previously designed chip with processed SU-8 interlocking structures.

shaken ultrasonically during the final minute of the SU-8 development. Fig. 5.7 shows a top chip with SU-8 interlocking structures.

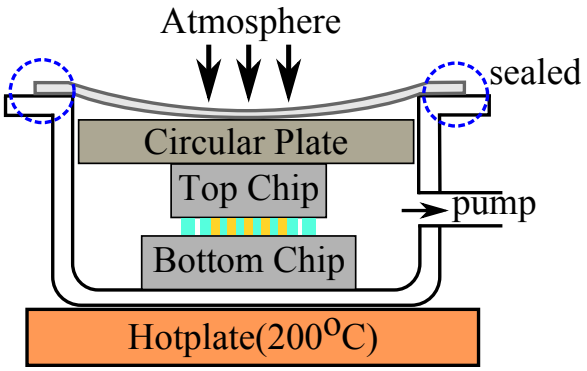


FIGURE 5.8: The structure of the thermal bonding chamber.

5.2 Assembly

During assembly, the top chip with mating structure is flipped over and attached to the bottom chip. Misalignment is avoided by checking the thickness of the assembled sample. If the interlocking structures are close but do not fit, parts of the mating structure will be on top of the SU-8 plating mold. In this scenario, the vertical distance between the top and bottom chips equals to twice the thickness of the SU-8 structures, indicating a misalignment.

A gold-to-gold thermocompression bond is used to electrically connect the two chips together. During thermocompression bonding, pressure helps to deform surface contamination by flattening the gold surface, and temperature helps to provide the energy to remove the deformed surface contamination film [59]. Therefore, the gold surfaces are brought into intimate contact such that the interatomic interaction between the two occurs.

The bonding is done in a simple thermal compression bonding chamber, which is shown in Fig. 5.8. To do the bonding in this chamber, the aligned sample is first put into the chamber and covered with a circular plate (1 inch in diameter) and a flexible rubber membrane. The chamber is then pumped down to low vacuum ($\sim$5 Torr), and put on a 200 ^{o}C hotplate for 20 min. The inner-diameter of the chamber is only slightly larger than 1 inch, so that the circular plate moves perpendicularly to the aligned chips.

The compressive load for this setup is estimated to be around 5 kg, which is about

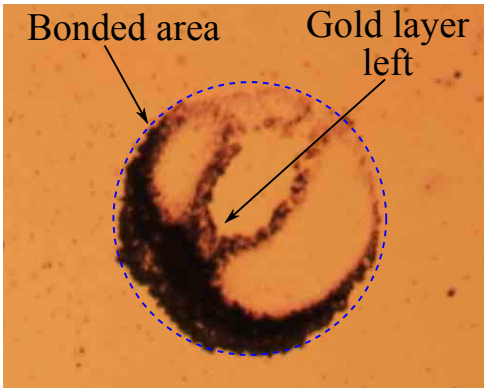


FIGURE 5.9: Gold residue left on the substrate from a successfully bonded microbump after it has been pulled apart.

800 g/bump for the single-channel devices and 400 g/pump for the double-channel devices. Ref. [59] shows that for temperatures between 150 and 200 ^{o}C, the pressure should be in the range of 300 to 500 g/bump for standalone gold bumps.

The plated micro-bumps extend just 2–3 μm over the SU-8 mold (as shown in Fig. 5.4) and are surrounded and protected by the SU-8. Therefore, this process does not require precise pressure control since the SU-8 maintains the structural dimensions of the transition. In this setup, the chips are held under pressure for 20 min to ensure the gold-gold interface reaches the critical bonding temperature of 150 ^{o}C [59]. Fig. 5.9 shows gold residue left on the substrate from a successfully bonded microbump after it has been pulled apart.

Chapter 6

Measurement

6.1 RF Performance

The vertical RF transitions are measured in a back-to-back configuration. The measurement includes return loss, insertion loss and isolation between different ports. The test setup, shown in Fig. 6.1, includes an HP 8510 network analyzer, frequency extension units (V-band and W-band), GSG probes and a probe station.

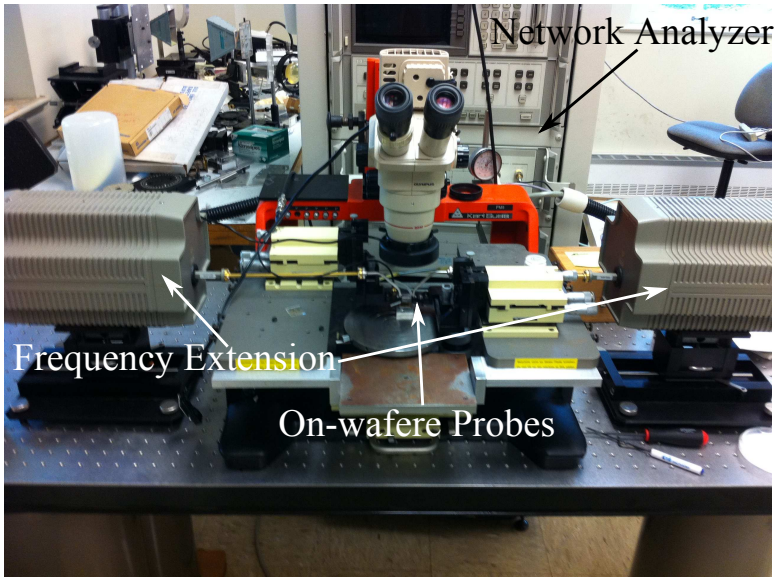


FIGURE 6.1: Test setup for millimeter-wave vertical transitions.

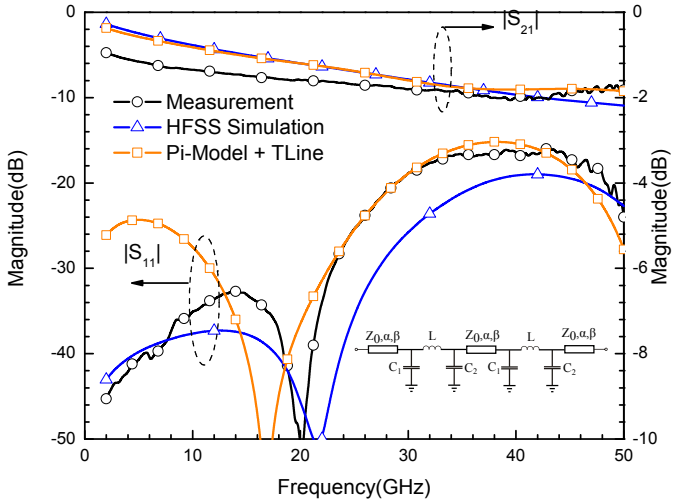


FIGURE 6.2: The measurement results of single channel back-to-back transitions with the full wave electromagnetic field simulations and the circuit simulations. The full wave simulation is done with S=150 μm, h=55 μm, R=35 μm, and other dimensions are shown in Fig. 5.1.

6.1.1 *Ka*-band Design

The fabricated structures (as shown in Fig. 5.1) were measured using the HP 8510 network analyzer and two GSG probes (Picoprobe Model 50A, DC–50 GHz) with an on-wafer Thru-Reflect-Line (TRL) calibration for 2–50 GHz. The calibration kits have multiple delay lines to cover the whole 2–50 GHz band [60] and, using MultiCal, the TRL calibration calculates the propagation constant of the CPW lines, α(dB/cm) and β(rad/cm), which is used in the circuit simulations of the vertical transitions. Fig. 6.2 shows the measured and simulated results. As seen from this figure, the measured results show return loss better than 15 dB up to 50 GHz. The circuit simulation results in Fig. 6.2 are from ADS® with the pi-model and physical transmission lines (*e.g.* α=6.25 dB/cm and β=2.128×10^{5}rad/cm at 40 GHz). The circuit values of the pi-model used in the simulation are shown in Table 4.1, and the phase constant and attenuation of the transmission lines are based on the TRL calibration data. The HFSS simulations have been changed to simulate the fabricated structures with a gold conductivity of 3.3×10^7 S·m^{-1} and a loss tangent of 0.08 for the SU-8 [61]. A reasonable agreement between the full-wave electromagnetic field simulation, the circuit model simulation and the measurements is shown in Fig. 6.2.

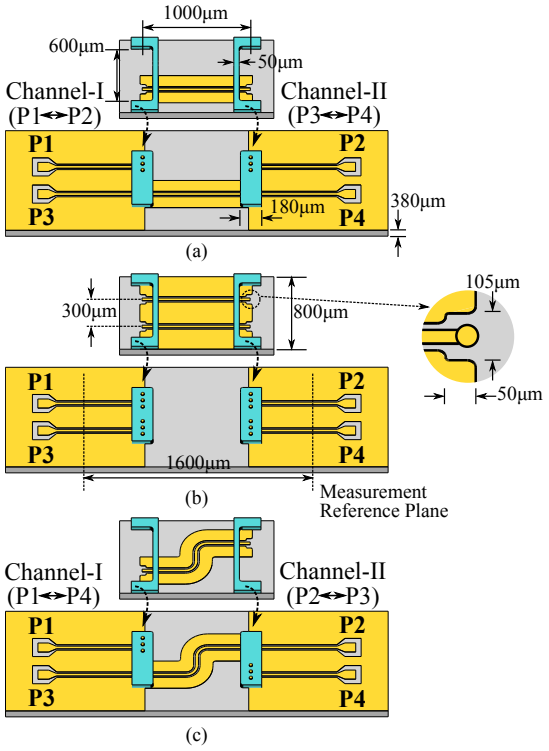


FIGURE 6.3: Three test structures of w-band vertical transition. The thickness of the SU-8 is 36 μm. The dimensions of the vertical transition are detailed in the Fig. 4.3 and Table. 4.2. CPW dimensions are 15/30/15 μm.

6.1.2 *W*-band Design

The *W*-band design is similar to the *Ka*-band design, with smaller microbumps. The measurements were done separately in three frequency bands: 2–50 GHz, 50–75 GHz (*V*-band frequency extension units) and 75–110 GHz (*W*-band frequency extension units). On-wafer TRL calibrations were performed in each band and after each calibration, the isolation between the pair of short standards was measured to give the crosstalk between adjacent transmission lines through the substrate.

Fig. 4.12 is repeated here as Fig. 6.3. In the test structure shown in Fig. 6.3(a), channel-I (between ports P1 and P2) has back-to-back vertical transitions, whereas channel-II has no vertical transition and is adjacent to channel-I. The center-to-center distance between the two channels is 300 μm. The simulation and measurement results are shown in Fig. 6.4. Both the simulation and measurement results show a return loss of better than 14 dB up to 90 GHz and better than 10 dB to 110 GHz. Channel-II has better return loss, but the insertion loss of both channels is nearly identical as can be seen in Fig. 6.5, along with the calculated loss of a CPW line with a length of

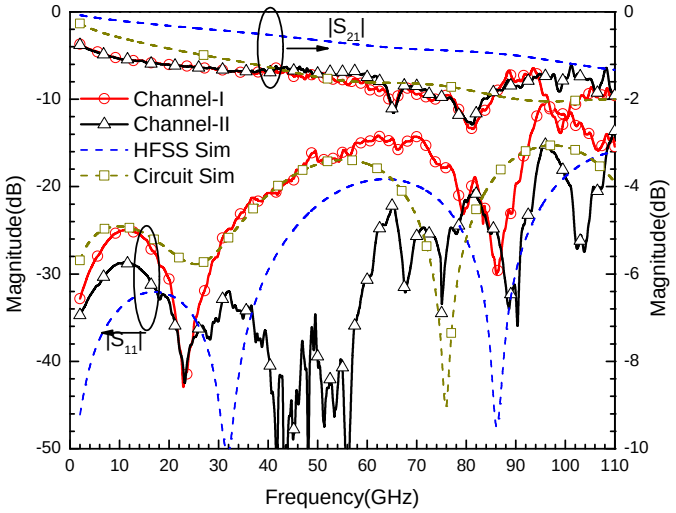


FIGURE 6.4: The simulation and measurement results of test structure shown in Fig.4.12(a). The circuit simulation was done with Pi-models and CPW transmission lines. The circuit values of Pi-model and the dimensions of the CPW are detailed in the Table. 4.2 and Fig. 4.12.

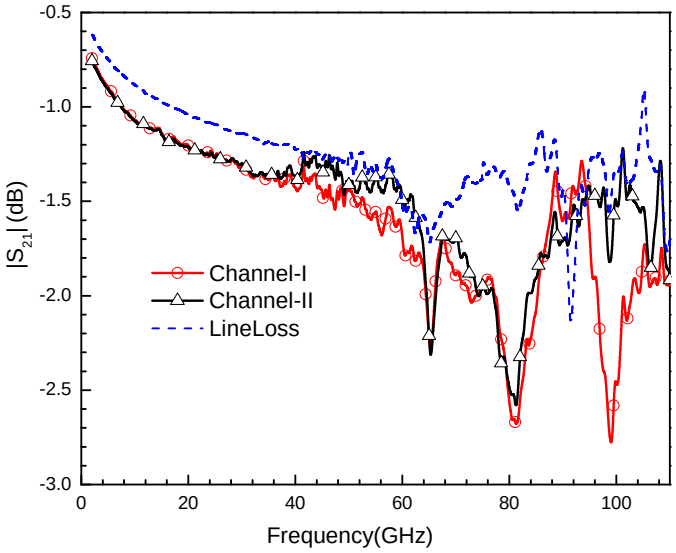


FIGURE 6.5: The loss comparison. Line loss is calculated from the TRL calibration data.

channel-I. The calculated loss is based on the attenuation data of the CPW lines from TRL calibrations. From Fig. 6.5, the insertion loss per transition is better than 0.1 dB at 40 GHz. For higher frequencies, it is difficult to measure insertion loss with high accuracy.

To measure the isolation, the insertion loss between port P1 and P4 (as shown in the Fig. 6.3(a)) was measured, leaving other ports open, and is shown in Fig. 6.6. The isolation between these two channels is better than 30 dB up to 50 GHz. At higher

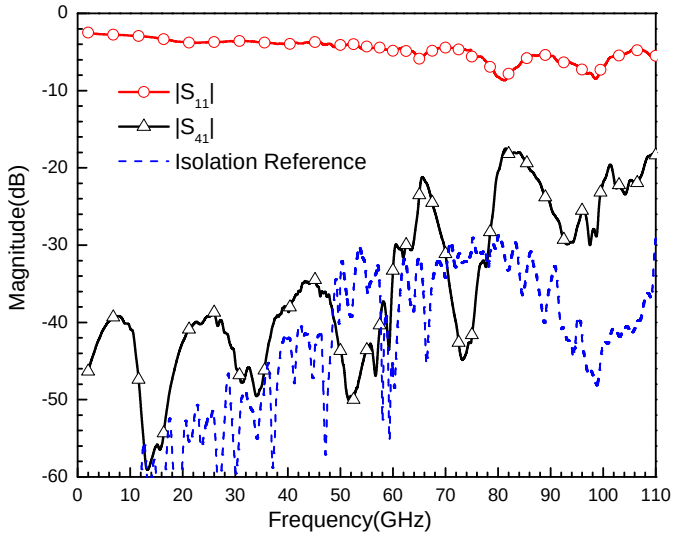


FIGURE 6.6: The isolation between channels P1 and P4 as shown in Fig.4.12(a). Ports P2 and P3 are left open during the measurement.

frequencies, the isolation decreases but remains better than 18 dB.

The test structure (b) is similar to (a), but both channels in test structure (b) include back-to-back vertical transitions. The results are similar to that of channel-I in test structure (a). The results at the measurement reference plane are plotted in Fig. 6.7 and show good agreement between the HFSS and circuit simulations. The circuit model simulation uses the phase constant and attenuation of the transmission lines calculated by TRL calibration data. The isolation between the two channels is also measured under similar conditions as test structure (a) and the results are shown in Fig. 6.8. In the frequency range 90–110 GHz, the isolation is slightly worse than test structure (a), which could be due to increased coupling between the pair of vertical transitions.

Test structure (c) has one channel crossing above the other by using the vertical transition. The measurement results of test structure (c) are shown in Figs. 6.9 and 6.10. In test structure (c), Channel-I has back-to-back vertical transitions, while Channel-II does not. The insertion loss of both channels is around 4 dB at 100 GHz, which is double the loss of channel-I in structure (a) (as shown in Fig. 6.4), but the insertion loss between these two channels in test structure (c) remains close (as shown in Fig. 6.9). The increased insertion loss is likely due to the discontinuities in the CPW lines, since air bridges are not included around the CPW corners. The isolation between the two channels (Fig. 6.10) is also worse by comparison, which points to radiation of

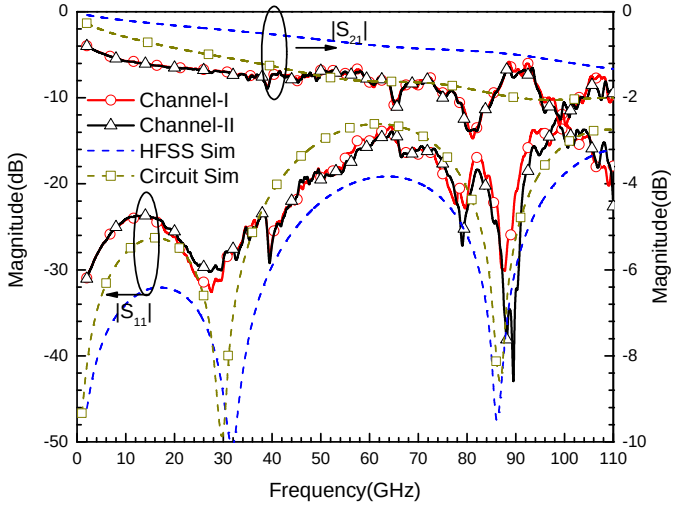


FIGURE 6.7: The simulation and measurement results of the test structure shown in Fig.4.12(b)

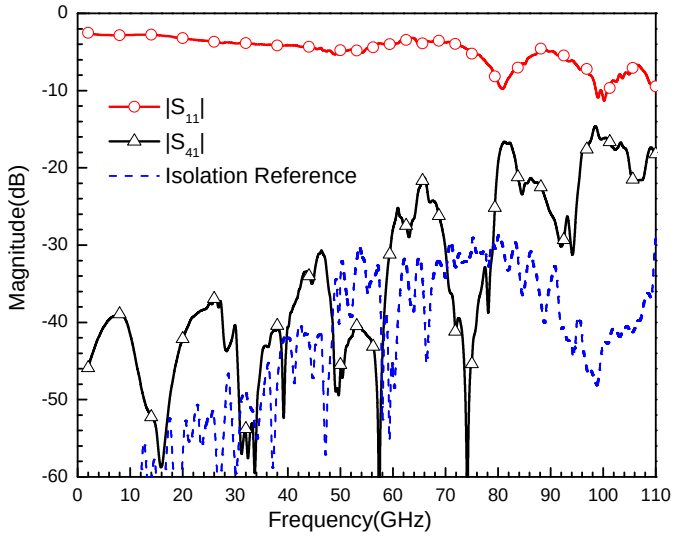


FIGURE 6.8: The isolation between channels P1 and P4 as shown in Fig.4.12(b). Ports P2 and P3 are left open during the measurement.

the discontinuities in the CPW lines.

6.2 Reliability

The integration of high performance GaAs devices with low cost silicon devices would significantly improve system performance while remaining relatively low cost. However, the Coefficient of Thermal Expansion (CTE) mismatch is a big concern for the reliability of heterogeneous integration. The CTE difference between different substrates will dominate the mismatch. Temperature cycling is a well-known method for evaluating

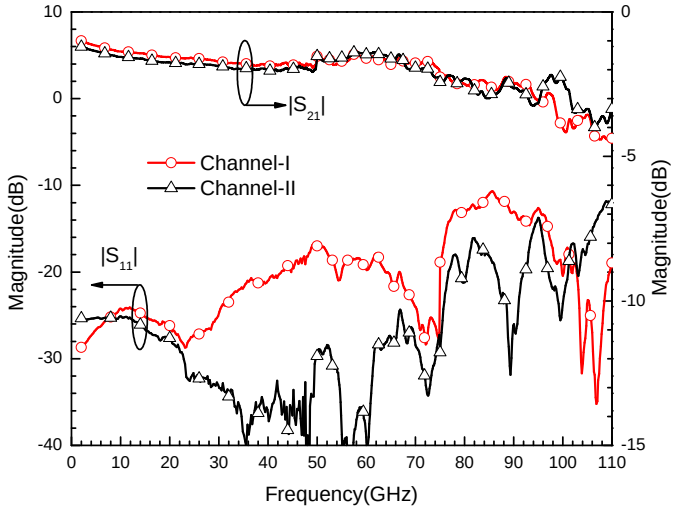


FIGURE 6.9: The measurement results of crossing channels shown in Fig.4.12(c).

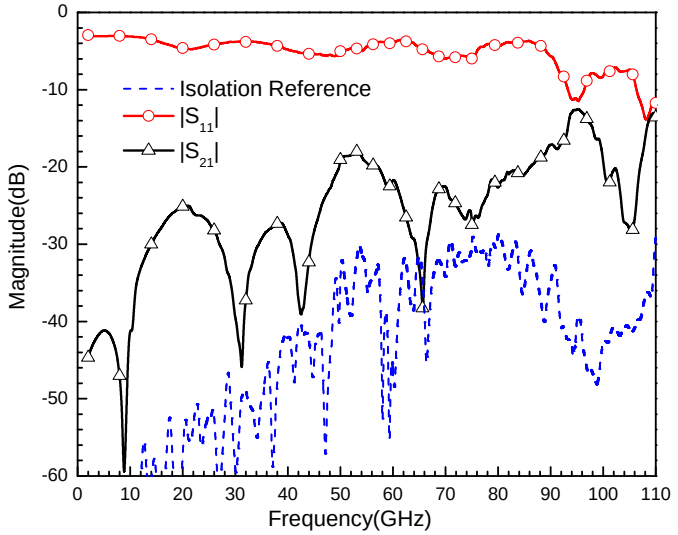


FIGURE 6.10: The isolation between channels P1 and P2 as shown in Fig.4.12(c). Ports P3 and P4 are left open during the measurement.

package reliability. The end-customer reliability requirement for the packaged device is expressed principally by a Temperature Cycle Test (TCT) excursion range and number of cycles to first failure. The most prevalent requirement for flip-chip packages is TCT (-40 to 125°C) for 1,000 cycles[62].

The CTE difference between Si and quartz is close to that between Si and GaAs, as shown in Table 6.1. Since quartz is less expensive, it was used instead of GaAs for this test. The CPW lines were re-designed for quartz by following the same design procedure shown in Fig. 4.2. CPW dimensions of w=60 μm and g=6 μm were chosen for the quartz substrate (500 μm thick). Due to limited access to the thermal cycle test equipment,

TABLE 6.1: Thermal expansion coefficients for Si, GaAs and Qz.

Material	Coefficient of Thermal Expansion (10^{-6}/K at 20^oC)
Si	3
$GaAs$	5.8
Qz(Fused)	0.59

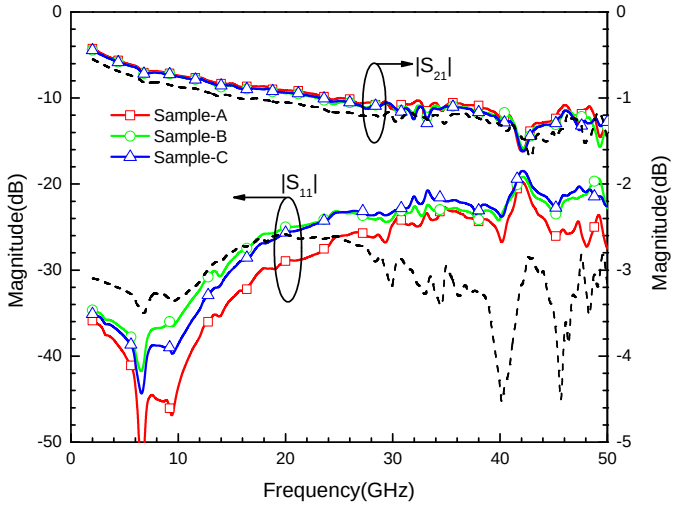


FIGURE 6.11: Thermal cycle test results: The dash lines is the RF performance before thermal cycle test; The solid line show the RF performance of three independent test samples that have back-to-back vertical transitions after 100 thermal cycles(-40 to 125˚C).

the test was stopped after 100 cycles. However, as seen in Fig. 6.11, the preliminary thermal cycle test results are promising.

6.3 Conclusions

Vertical RF transitions for heterogeneous integration with interlocking structures fabricated using SU-8 are demonstrated in this thesis. The measurement results show excellent performance up to 110 GHz with insertion loss less than 0.1 dB per transition at 40 GHz. Designs for Ka-band and W-band have been presented with excellent agreement between simulation and measurement. A submillimeter-wave vertical transition was design by following the same design procedure and simulation results show better than 15 dB return loss up to 400 GHz. The vertical RF transition with mechanical fit presented in this thesis can provide a useful alternative for millimeter/submillimeter-wave circuit packaging and vertical interconnects, since the SU-8 structure maintains the precisely defined dimensions within the vertical transition.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

7.1.1 On-wafer Probe

To advance in submillimeter-wave integrated circuit development, on-wafer probes are needed to verify the models and designs. This thesis presented the development of submillimeter-wave on-wafer probes based on a microfabrication process developed at the University of Virginia. A submillimeter-wave on-wafer probe consists of a silicon micromachined probe chip housed in a metal waveguide block. The probe chip is a passive circuit based on a 15 μm thick silicon substrate. Measurements of a WR-1.5 micromachined on-wafer probe exhibited a return loss better than 12 dB and a mean insertion loss of 6.52 dB from 500 to 750 GHz.

When the probe makes contact, the probe chip deflects and generates a force at the contact point. The probe has been designed to provide enough force to create a low resistance contact with test pads on the DUT. The probe mechanical design was analyzed using a simple analytic model of a cantilever beam and ANSYS simulation. Simulation and measurement results showed that making the probe easy to twist was more important than ensuring the probe generates enough contact force.

Probes are usually used in an automated probe station for measuring hundreds to thousands of devices per wafer to support process development and device modeling. A

practical probe requires a reasonable lifetime. Reliability of the probe is investigated using a motor driven stage and SEM imaging as detailed in Section 3.3. Tests in this thesis showed that the probe with hard gold has maintained high RF consistency up to 20,000 contact cycles at a 20 mN contact force.

Repeatability is a measure of the agreement between repeated measurements of the same property under the same condition. The repeatability of the probe is investigated in detail in Section 3.3. Monte Carlo simulations are used to identify the dominant error source of on-wafer measurement and to estimate the measurement accuracy. The dominant error source is positioning error, which results in phase uncertainty.

The loss of microstrip is greater than that of quasi-rectangular coax. However, using low impedance microstrip (35 Ω), the micromachined probe based on microstrip has achieved slightly better insertion loss than the coax probe. The advantage of the microstrip design is that it is less sensitive to the spurious modes at discontinuities in the substrate width, because the E-field in the microstrip is mostly confined in the substrate underneath the strip.

As the probe is scaled for higher frequencies, the silicon substrate thickness has to be reduced to prevent higher-order propagation modes in the intermediate transmission channel. The disadvantage of the microstrip design is that the strip width is narrower for the same characteristic impedance as the substrate thickness become thinner, leading to increased loss. However this design will not require a significant reduction in the transmission-line channel as the quasi-rectangular coax.

7.1.2 Vertical Transition with Mechanical Fit

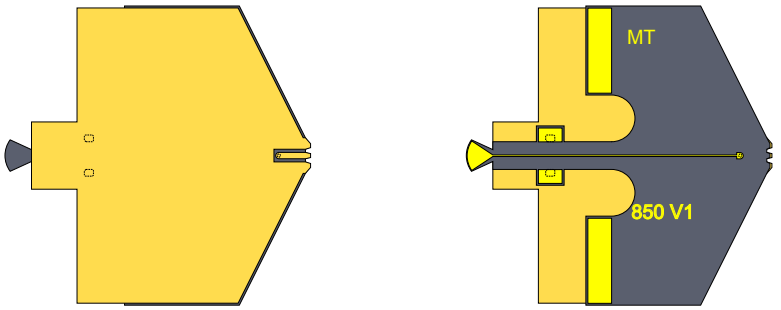
Three-dimensional integration by vertically stacking multiple die promises smaller and smarter subsystems. 3D packaging requires high-density vertical transitions that can transfer signals from the front of a chip to its back and between stacked chips. Vertical RF transitions for heterogeneous integration with interlocking structures fabricated using SU-8 are demonstrated in this thesis. The measurement results show excellent performance up to 110 GHz with insertion loss less than 0.1 dB per transition at 40 GHz.

Designs for *Ka*-band and *W*-band have been presented with excellent agreement between simulation and measurement. The vertical RF transition with mechanical fit presented in this thesis can provide a useful alternative for millimeter-wave circuits packaging and vertical interconnects, since the SU-8 structure maintains the precisely defined dimensions within the vertical transition.

7.2 Future Work

7.2.1 WR-1.2 On-wafer Probe

Based on the success of WR-1.5 on-wafer probe designs, a WR-1.2 probe is designed, which covers frequencies from 600 to 900 GHz. The wavelength in silicon ($\epsilon_r = 11.9$) is 96.7 μm at 900 GHz. Therefore a 5 μm ($<\lambda/10$) substrate is selected to prevent higher-order propagation modes. For the 5 μm silicon substrate, the width of 50 Ω microstrip is 4 μm, which results in a high insertion loss. However, the microstrip does not connect to the DUT directly. Therefore, a low impedance microstrip can be used as the intermediate transmission line to reduce the insertion loss. This subsection presents two designs, one is designed with 50 Ω microstrip and a second one with 22 Ω microstrip (width= 15 μm). Both designs use a "hot via" microstrip-to-CPW transition.



(a) (b)

FIGURE 7.1: Images of the top and bottom of the micromachined wafer probe chip, WR-1.2 design-I. (a) Top view; (b) bottom view.

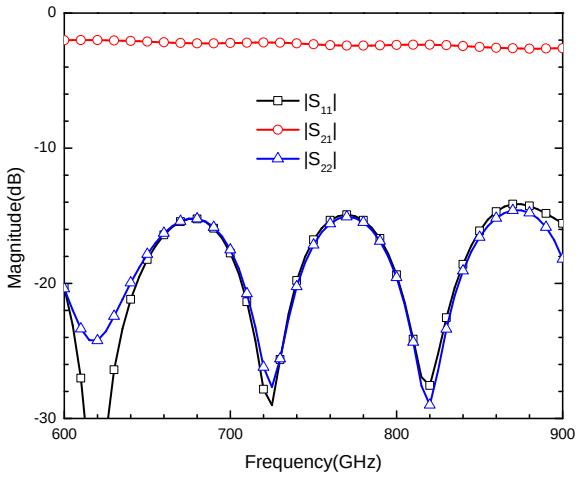
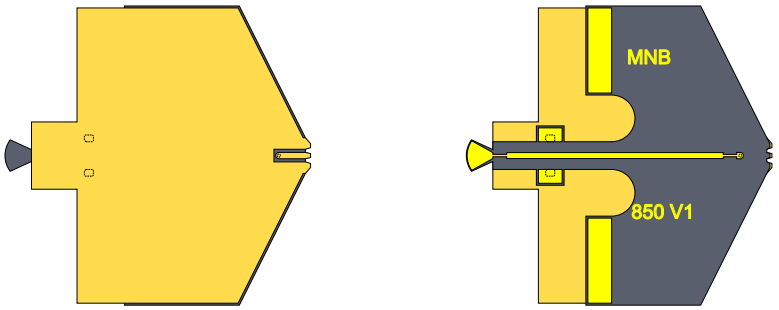


FIGURE 7.2: HFSS simulation results of probe with a WR-1.2 design-I probe chip. The simulation is done from waveguide to CPW probe tips.

The 50 Ω microstrip design is shown in Fig. 7.1 and its simulation results are shown in Fig. 7.2. The 22 Ω microstrip design is shown in Fig. 7.3 and its simulation results are shown in Fig. 7.4. While the 50 Ω design shows slight better return loss across the band, the 22 Ω design should have significantly lower insertion loss.

7.2.2 Sub-millimeter-wave Vertical Transition Design

Sub-millimeter-wave vertical transition design is based on the *Ka*- and *W*-band vertical transitions. The dimensions of CPW lines are redesigned using HFSS. The simulation



(a) (b)

FIGURE 7.3: Images of the top and bottom of the micromachined wafer probe chip, WR-1.2 design-II. (a) Top view; (b) bottom view.

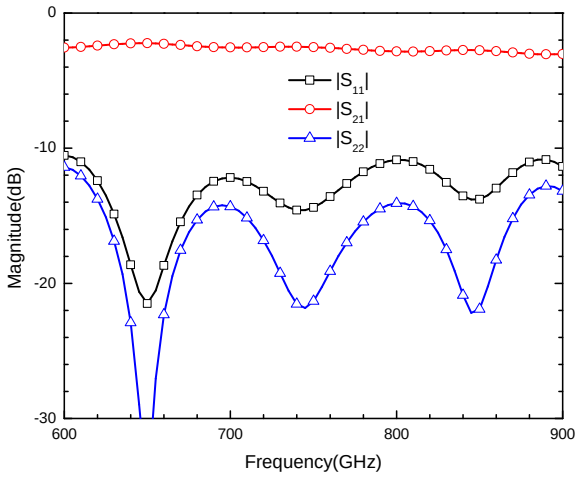


FIGURE 7.4: HFSS simulation results of probe with a WR-1.2 Design-II probe chip. The simulation is done from waveguide to CPW probe tips.

results shown in Fig. 4.2 are extended up to 400 GHz. Based on the simulation results, a center conductor width of 20 μm is chosen to provide a compromise between attenuation loss, dispersion, and die area.

The design is done by following the same procedure detailed in Section 4.2.2. The simulation results show that the transition has better than 16 dB return loss up to 400 GHz, as shown in Fig. 7.5. The dimensions of the sub-millimeter-wave vertical transition are detailed in Fig. 7.6.

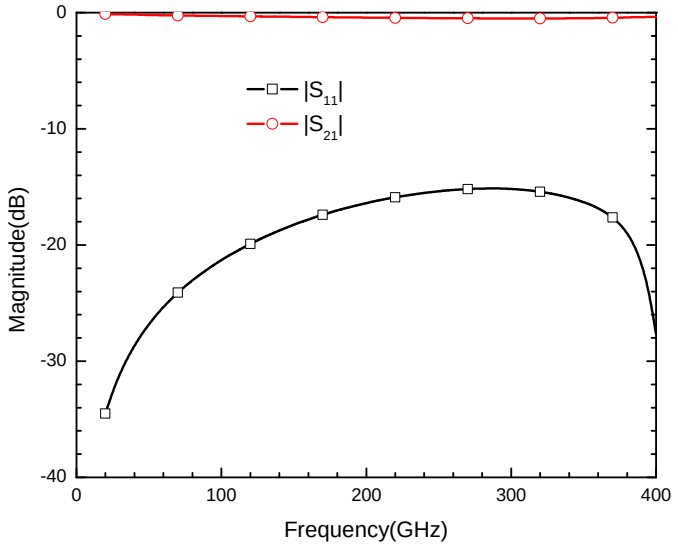


FIGURE 7.5: HFSS simulation results of a sub-millimeter-wave vertical transition.

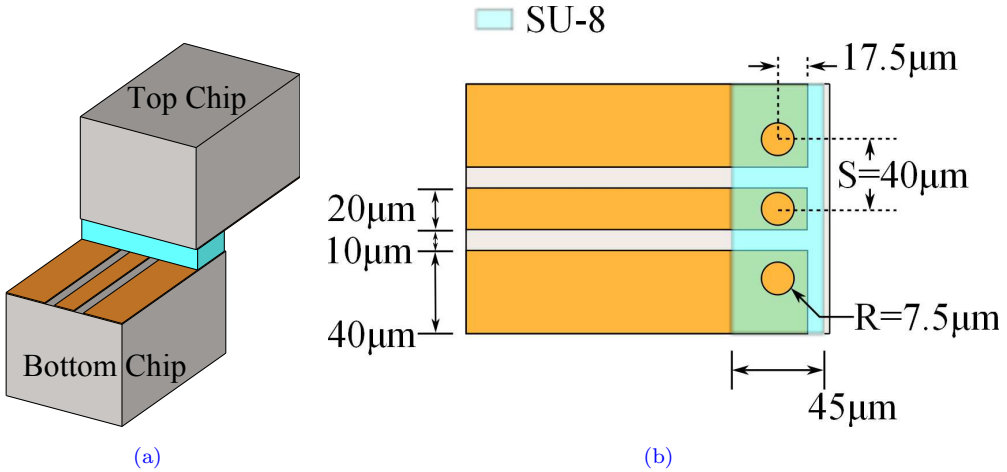


FIGURE 7.6: Dimensions of sub-millimeter-wave vertical transition.

Appendix A

Fabrication Process

This appendix gives a detailed fabrication process for vertical transition with mechanical fit. Start with high-resistivity silicon.

Conductor layer liftoff

1. Clean wafer:
   (a) ETM clean wafer.
   (b) O_2 plasma 5 min, 200W .
2. Photolithography (Mask-I):
   (a) ETM clean wafer.
   (b) O_2 plasma 5 min, 200W.
   (c) HMDS 3min.
   (d) Spin AZ 5214, 4krpm, 30sec.
   (e) Softbake 2min 100°C.
   (f) Mask expose: 18sec, L-Vac contact.
   (g) Post-exposure bake: 1min 30 sec, 100°C.
   (h) Flood expose 30 sec.
   (i) Pause 2min.
   (j) Develop AZ400K (1:4), 35sec. Ensure double line prole in microscope.
   (k) O_2 plasma, 1min, 100W.

3. Evaporate metal layers:
   (a) 100 $\mathring{A}$ Ti
   (b) 6000 $\mathring{A}$ Au
   (c) 200 $\mathring{A}$ Cr
4. Remove excess metal and clean:
   (a) Soak NMP 120°C, 30min.
   (b) DI rinse.
   (c) O_2 plasma, 5min, 120W.
5. Photolithography (Mask-II):
   (a) ETM clean wafer.
   (b) O_2 plasma 5 min, 200W.
   (c) HMDS 3min.
   (d) Spin AZ 5214, 4krpm, 30sec.
   (e) Softbake 2min 100°C.
   (f) Mask expose: 18sec, L-Vac contact.
   (g) Post-exposure bake: 1min 30 sec, 100°C.
   (h) Flood expose 30 sec.
   (i) Pause 2min.
   (j) Develop AZ400K (1:4), 35sec. Ensure double line prole in microscope.
   (k) O_2 plasma, 1min, 100W.
6. Evaporate 400 $\mathring{A}$ Ti.
7. Remove excess metal and clean:
   (a) Soak NMP 120°C, 30min.
   (b) DI rinse.
   (c) O_2 plasma, 5min, 120W.

Deposit and Pattern Silicon Nitride

1. PECVD Silicon Nitride: Plasmatron, 11” square platter:

(a) Process parameters:

SiH_4	200 sccm
NH_4	4 sccm
N_2	200 sccm
He	600 sccm
Pressure	900 mT
Temperature	$250°C$

(b) Time – 30 min.

(c) Rotate wafer 180° and deposit another 30 min.

2. Photolithography (Mask-III):

(a) HMDS 3min.

(b) Spin AZ 5214, 4krpm, 30sec.

(c) Softbake 2min $100°C$.

(d) Mask expose: 18sec, L-Vac contact.

(e) Post-exposure bake: 1min 30 sec, $100°C$.

(f) Flood expose 30 sec.

(g) Pause 2min.

(h) Develop AZ400K (1:4), 35sec.

3. RIE etch Si_xN_y:

(a) Parameters for Trion Phantom II:

P	50 mT
ICP	0
RIE	35, Keep DC<100V
CF_4	50 sccm
O_2	10 sccm

(b) Time – 3 min.

4. Clean:

(a) Remove patterning resist in Acetone.

(b) ETM clean.

(c) O_2 plasma clean, 100W, 1 min.

Deposit and Pattern SU-8 Photoresist:

1. Coat Wafer with SU-8 photoresist:

   (a) Dry the wafer on a $160°C$ hot plate for 5 minutes.

   (b) Place wafer on the photoresist spinner.

   (c) Set the spinner to 0 rpm and the time to 60 sec.

   (d) Pour SU-8 2035 directly from the bottle on the center of the wafer.

   (e) Gradually increase the speed of the spinner to 500 rpm.

   (f) Hold at 500 rpm for 10 sec.

   (g) Gradually increase the speed of the spinner to 1000 rpm.

   (h) Hold at 1000 rpm for 10 sec.

   (i) Let the wafer remain on the chuck for 12 min.

2. Edge Bead Removal:

   (a) Transfer the wafer on to Petri dish sheet.

   (b) Remove edge bead using blade.

   (c) Rest wafer on leveled chuck for 5 min before transferring the wafer to the hotplate.

3. Soft Bake:

   (a) Place a new Petri dish sheet on hotplate; Used to protect hotplate and prevent the wafer from sticking to the hotplate.

   (b) Place wafer on $65°C$ hot plate for 5 min.

   (c) Transfer wafer to $100°C$ hot plate for 1 hour.

   (d) Place wafer on $65°C$ hot plate for 5 min.

   (e) Let wafer cool to room temperature for 10 min.

4. Repeat Resist Coat and Soft Bake procedure until a thickness of 50 μm is reached.

5. Exposure (Mask-IV):

   (a) Remove bandpass filter from MJB3 Mask Aligner.

(b) Use 365 nm sensor to measure the intensity.

(c) Place the Edmund Optics' 365nm CWL Narrow Bandpass filter on top of the mask.

(d) Expose with the MJB3 Mask Aligner with a dosage of 1100mJ/cm^2.

6. Post Exposure Bake:

(a) Place wafer on 65°C hot plate for 3 min.

(b) Transfer wafer to 100°C hot plate for 20 min.

(c) Transfer wafer on 65°C hot plate for 3 min.

(d) Let wafer cool to room temperature for 10 min.

7. Develop SU-8 Photoresist:

(a) Develop with PGMEA (AZ Edge Bead Removal).

(b) Rinse with IPA for 1 min.

(c) Rinse in DI water for 1 min.

(d) Dry with N_2.

Gold Plating

1. RIE etch Cr:

(a) Parameters for Trion Phantom II:

P	50 mT
ICP	0
RIE	35, Keep DC<100V
CF_4	50 sccm
O_2	10 sccm

(b) Time – 3 min.

2. Electroplate gold into SU-8 mold via Technic Gold 25ES RTU plating solution using reverse pulse plating.

(a) The electroplating parameters are:

	Current Density	Time
Forward	5 mA/cm^2	240 sec
Reverse	15 mA/cm^2	15 sec

(b) Time – until the plated gold is slightly above SU-8 mold.

RIE Etch Silicon Nitride, Ti and Cr

1. RIE etch Si_xN_y:

   (a) Parameters for Trion Phantom II:

P	50 mT
ICP	0
RIE	35, Keep DC<100V
CF_4	50 sccm
O_2	10 sccm

   (b) Time – 3 min.

2. RIE etch Ti and Cr:

   (a) Parameters for Trion Phantom II:

P	50 mT
ICP	200
RIE	18, Keep DC<100V
CF_4	50 sccm
O_2	10 sccm

   (b) Time – 2 min.

Dice

1. Mount fabricated wafer to carrier wafer:

   (a) Apply Q-wax to 4 inch carrier wafer.

   (b) Place wafer on the carrier wafer.

   (c) Ramp temperature in $5°C$ increments to $75°C$.

   (d) Use Swabs to press wafer into wax.

   (e) Cool wafer to room temperature.

2. Protect SU-8 structure:

   (a) Coat wafer with liquid wax at 1000 rpm.

   (b) Ramp temperature in $5°C$ increments to $60°C$.

   (c) Hold at $60°C$ for 30 min.

   (d) Cool wafer to room temperature.

3. Dice wafer into chips.

4. Release and clean chips:

   (a) Submerge chips in D-limonene overnight.

   (b) Rinse in IPA for 1 min.

   (c) Rinse in DI water for 1 min.

Appendix B

A Micromachined Terahertz Waveguide 90° Twist

B.1 Introduction

Rectangular waveguide remains an important transmission medium for terahertz system development, and waveguide components such as twists are essential for assembling terahertz instruments and integrating subsystems with different polarizations. Unfortunately, the relatively small dimensions of terahertz waveguide make fabrication of waveguide components of modest complexity, such as twists, difficult or even impractical using standard milling techniques.

This appendix describes a micromachined compact 90° twist that is based on a design first investigated by Rud *et al.* [63]. The twist is designed to join a conventional WR-1.5 rectangular waveguide to a second, orthogonally-polarized waveguide, as illustrated in Fig. B.1. The micromachined twist is fabricated using a KMPR based UV LIGA process discussed in [42] and [43]. Although the twist presented here is designed for WR-1.5 waveguide (500-750 GHz), the fabrication process is readily scaled for frequencies from 200 GHz to 2 THz.

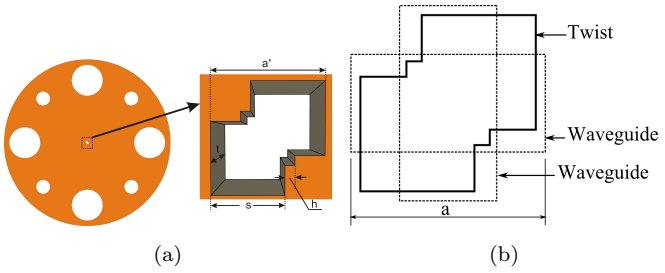


FIGURE B.1: WR-1.5 twist. (a) Principal Layout. (b) The cross-sectional view of the twist related to the waveguides. The waveguide width $a = 380\,\mu$m.

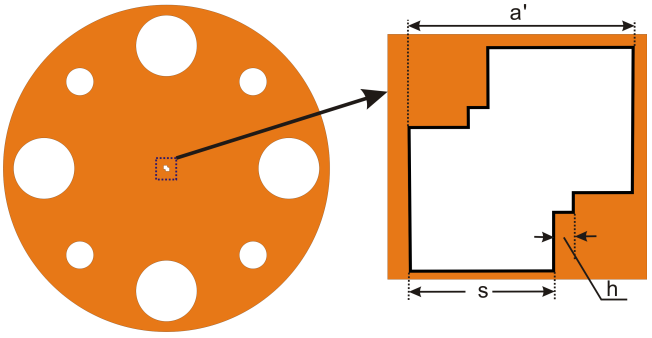


FIGURE B.2: Design of WR-1.5 waveguide twist shim with four slip fit dowel pin holes ($a' = 343\,\mu$m, $s = 223\,\mu$m, $h = 30\,\mu$m and the thickness of the shim $t = 0.71a = 270\,\mu$m).

B.2 Design and Fabrication

A variety of twist configurations are discussed in [64], but few designs have been demonstrated at submillimeter-wave frequencies. One recent example is a submillimeter-wave 90° waveguide twist reported by Ward and Chattopadhyay [65] that exhibited a return loss around 20 dB over 500-700 GHz. This design makes use of asymmetrically shaped steps with a total length much longer than the waveguide width a. For applications with size constraints, a waveguide of this length may not be practical and will have high insertion loss. The alternative design described by Rud *et al.* [63] is compact and consists of overlapping rectangular apertures, as shown in Fig. B.1. This twist design has an overall length of only $0.661a$. Although this design is geometrically simple and compact, the inner corners of the design make fabrication of a terahertz scaled version impractical with standard milling techniques.

The micromachined twist reported in this appendix is based on the prototype

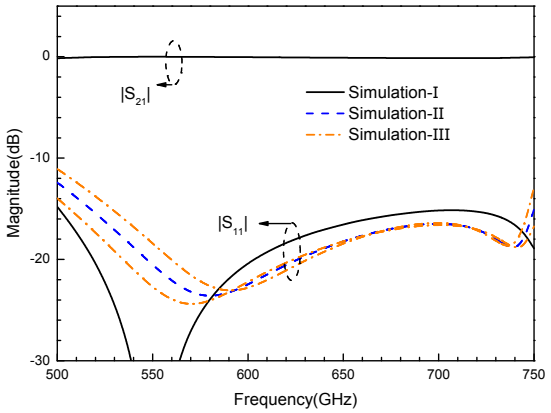
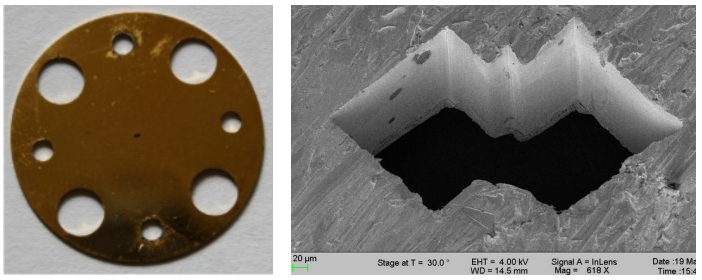


FIGURE B.3: The simulation results of twists. Simulation-I: dimensions shown in Fig. B.2; Simulation-II: taper angle $\theta = 1.5°$ and other dimensions same as Simulation-I; Simulation-III: taper angle $\theta = 1.5°$, $h = 30 \pm 3\,\mu$m and other dimensions same as Simulation-I.

demonstrated by Rud *et al.* for operation at WR-75 [63] with dimensions scaled for WR-1.5. Modeling of the twist is done using Ansoft's *High Frequency Structure Simulator* (HFSS) and the detailed dimensions used for this simulation are given in Fig. B.2. Scattering parameters obtained from modeling with HFSS are shown in Fig. B.3 (Simulation-I).

The basic process used to form the WR-1.5 twist consists of electroplating through a thick plating mask formed by KMPR 1050 photoresist. KMPR is an ultrathick photoresist, which can achieve $>500\,\mu$m with multiple coatings [43]. Although KMPR has excellent adhesion and chemical resistance, it is readily stripped from the wafer, making it ideal for electroplating-based micromachining. For the micromachined twist, a 300 to 350 μm thick film of KMPR 1050 is applied to a silicon carrier wafer and is patterned to form the twist aperture as well as the WR-1.5 waveguide flange pin and screw holes. Subsequently, the wafer is sputtered with a seed layer, Ti/Au (50/500 Å). Before nickel is electroplated to form the structure, 1 to 2 μm of gold is plated to cover the sidewalls of the KMPR, which will make the interior sidewalls of the twist covered with gold to reduce the conductor loss. A titanium sacrificial layer (1000 Å) is deposited on the silicon carrier wafer prior to lithography to facilitate releasing the shim from the mold. As a final step, the shim is lapped to planarize and obtain the final thickness. Images of the completed twist are shown in Fig. B.4.

This micromachining process is capable of fabricating the top face of the twist to



(a) (b)

FIGURE B.4: Images of the fabricated WR-1.5 twist: (a) Entire twist shim. Dowel pin holes and screw holes are consistent with waveguide interface recommendations for submillimeter wavelengths [6]. (b)Scanning electron micrograph of the WR-1.5 twist structure.

within 3 μm of the desired dimensions (a', s and h). The twist's sidewalls display a taper through the shim's thickness with an angle of 1.5° on each sidewall for the 300 to 350 μm KMPR. The accuracy of the shim thickness is determined by the lapping process. The thickness of the twist shown in this appendix is 16 μm less than the designed value due to the wax used to mount the shim to the glass substrates before lapping. By using thinner wax, the shim thickness accuracy has been improved to ± 5 μm. The twist performance sensitivity to fabrication uncertainty (including the sidewall taper) is analyzed in HFSS. The simulation results show that with the tolerance given above, the twist is expected to have better than 15 dB return loss over >60% of the waveguide operating bandwidth. Results from the analysis for variations in the twist geometry are shown in Fig. B.3.

B.3 Measurements

The twist is characterized using a one-port WR-1.5 frequency extension unit from Virginia Diodes Inc. (VDI WR1.5 VNAXTXRX) with a Rhode and Schwarz ZVA-40 network analyzer as the backend. A two-tier calibration technique was used to obtain the twist S-parameters. With this method, the network analyzer is initially calibrated to a reference plane coincident with the frequency extension unit test port using a waveguide short and four different delayed shorts. Because calibration standards are generally unavailable in the WR-1.5 band, only waveguide delayed shorts, which can be accurately characterized from their dimensions, were used as calibration standards.

After the first tier in the calibration procedure, the twist is attached to the network analyzer test port followed by a custom waveguide rotated by 90° with respect to the test port. The custom waveguide is a 0.8 inch long WR-1.5 waveguide with four dowel pin holes on one flange. This special interface is needed to allow proper mating between the standard pin layout of the network analyzer test port and the rotated waveguide. The second-tier calibration was performed by terminating the remaining waveguide port with the same waveguide short and four delayed shorts. The reflection coefficient measured at the network analyzer test port, Γ^M is related to the S-parameters of the twist cascaded with the custom waveguide, S_{ij} and the reflection coefficient of the waveguide short, Γ_l by the well-known bilinear transform,

$$\Gamma^M = S_{11} + \frac{S_{21}S_{12}\Gamma_l}{1 - S_{22}\Gamma_l}$$

By measuring the reflection coefficient of the twist with these terminations, and noting that the twist and the waveguide are reciprocal networks, the S-parameters of the twist cascaded with the custom waveguide are obtained. The waveguide S-parameters are obtained by following the same procedure. The twist's S-parameters are calculated by de-embedding the 0.8 inch waveguide. The S-parameters of the waveguide obtained by this one-port two-tier calibration method are shown in Fig. B.5. The insertion loss agrees well with the calculated waveguide loss due to conductor loss (plated gold, $\sigma = 3.3 \times 10^7\, S{\cdot}\mathrm{m}^{-1}$) [31].

The scattering parameters of the micromachined twist as determined by the above procedure are shown in Fig. B.6. The median insertion and return loss of the twist are 0.5 dB and 18.8 dB, respectively. Fig. B.6 also shows the simulated scattering parameters using HFSS with the measured dimensions of the twist, which are in good agreement with the measured S-parameters. The ripple in the measured return loss is due to a mismatch between the twist and the custom waveguide. The difference between $|S_{11}|$ and $|S_{22}|$ may be a result of one side of the shim having greater surface roughness than the other due to the lapping process. The insertion loss is slightly higher than the simulation result, but is within the measurement error range [45]. The phase of the transmission coefficient is shown in Fig. B.7 and is linear over the WR-1.5 waveguide

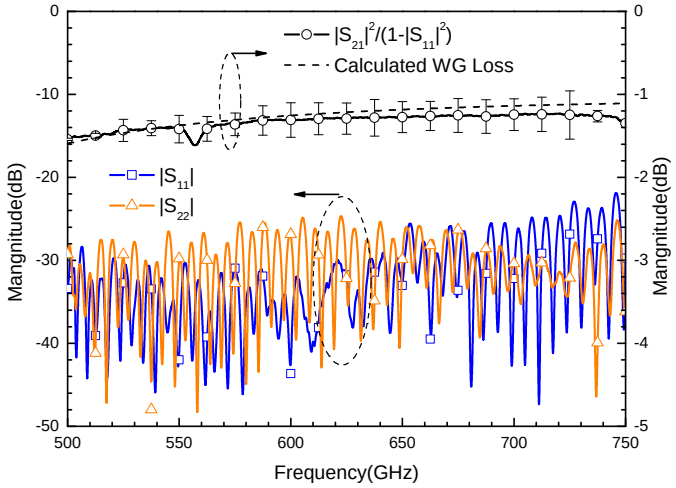


FIGURE B.5: Measured S-parameters of a 0.8 inch WR-1.5 waveguide. The dip near 550 GHz is a water vapor absorption line.

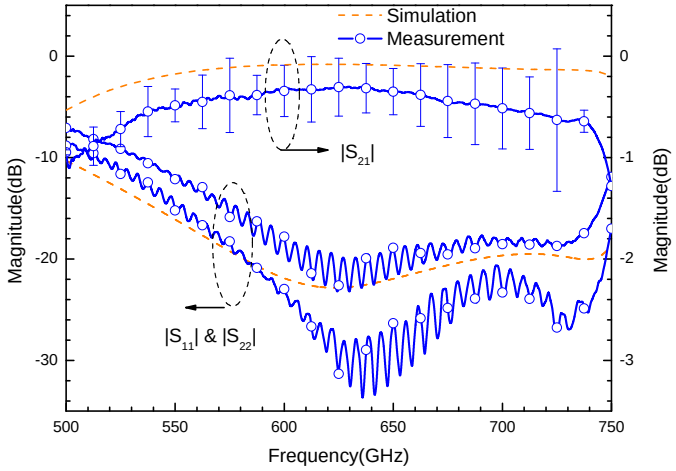


FIGURE B.6: Measured transmission and reflection of fabricated twist at WR-1.5 band shown with the solid lines. The simulation results was based on measured thickness $t = 254\,\mu$m, taper angle $\theta = 1.5°$ and other dimensions as designed (provided in Fig. B.1). Conductor loss (platted gold, $\sigma = 3.3 \times 10^7\ S{\cdot}\mathrm{m}^{-1}$) is included in the simulation.

band, which agrees with the simulation results using the measured dimensions.

B.4 Summary

A WR-1.5 waveguide twist fabricated using a KMPR based UV LIGA process has been designed and demonstrated. The twist's relatively complex geometry is difficult to realize with conventional CNC milling techniques but is relatively straightforward to fabricate with the KMPR micromachining process. The measured performance is in good agreement with that expected through numerical electromagnetic modeling and the twist

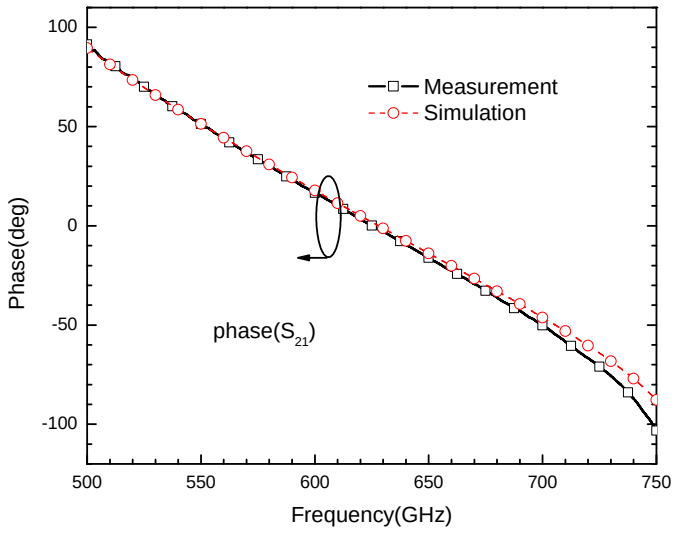


FIGURE B.7: Phase of the transmission of the twist. The simulation result is with measured dimensions.

exhibits a relatively low insertion loss over the entire waveguide band. The compact structure of the twist is a distinct advantage for many applications.

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