Energy Harvesting System Modeling

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APPROVAL SHEET

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Abstract

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DC-DC converters are electrical circuits that transfer energy from a DC voltage source to a load and regulate the output voltage. These circuits are widely used in energy harvesting applications, and should be optimized based on input power and load requirements to have maximum converter efficiency. SPICE is one of the popular tools used for this purpose which requires the user to design a circuit in the tool and perform the optimization. This requires a significant amount of time of the user at the design stage. This thesis develops a tool based on MATLAB Simulink to carry out the preliminary analysis of a power management circuits in an energy harvesting system. The tool consists of models on two inductor based DC-DC converters, linear dropout regulator (LDO) and five different non inductor based DC-DC converters. Individual models were verified in SPICE using 130 nm CMOS technology. The model is further developed to make a unified global energy harvesting model for inductor based and non inductor based DC-DC converters. The usage of a unified model for energy harvesting systems is presented in detail using three experiments. The tool can accurately model the functionality, energy and efficiency of the functional components of energy scavenging systems. This modeling can be used to make architectural design decisions in a power management unit in system-on-chip applications.

Keywords:Charge pump, thermoelectric energy harvesting, integrated inductors, SOC, Matlab, Simulink, Energy harvesting modeling, DC-DC converter modeling

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Contents

List of Figures

List of Tables

To my Wife, Parents and Brother For their unconditional support, trust and encouragement...

Chapter 1

Introduction and Motivation

1.1 Introduction to Energy Harvesting

Energy Harvesting, is a method of converting ambient energy to electrical energy, which can then be used to power electronic devices. The most well-known ambient energy sources for micro-power generation are light, heat, and vibration. Power densities for various energy sources for 1-year and 10-year lifetime are shown in Table 1.1.

According to Table 1.1, the power densities for natural energy sources stay constant over time. On the other hand typical energy sources like batteries have better performance than the energy harvesting sources for a fixed term, and degrade in performance with time. Dead batteries create environmental pollution if not recycled properly, which is another disadvantage of battery usage [2]. Due to the above reasons, there is a strong research interest in energy harvesting. A wide range of applications are targeted for the harvesters, including distributed wireless sensor nodes for structural health monitoring,

TABLE 1.1: The power densities for various energy sources [1]

Source	Conditions	Power Density 1-year lifetime	Power Density 10-year lifetime
Vibration	1 ms^{-2}	100 $\mu W/cm^3$	100 $\mu W/cm^3$
Solar	Outdoors	7500 $\mu W/cm^2$	7500 $\mu W/cm^2$
Solar	Indoors	100 $\mu W/cm^2$	100 $\mu W/cm^2$
Thermal	ΔT=5 °C	60 μW/cm2	60 $\mu W/cm^2$
Batteries (Lithium)	Non-rechargeable	89 $\mu W/cm^3$	7 $\mu W/cm^3$
Batteries (Lithium)	Rechargeable	13.7 $\mu W/cm^3$	0 $\mu W/cm^3$
Fuel Cells (methanol)	-	560 $\mu W/cm^3$	56 $\mu W/cm^3$

embedded and implanted sensor nodes for medical applications, monitoring tire pressure in automobiles, powering unmanned vehicles, mobile computing applications, and domestic security systems [3].

Photovoltaic energy harvesting is the most commonly used method, which converts solar energy into electrical energy using solar panels. This has been a very common practice used in many low power consumable electronics such as calculators, parking meters, weather stations, telephone boxes and traffic information systems [1]. Recent developments in photovoltaic technology enable extension of the application to notebooks as well [4].

Vibration energy harvesting can convert ambient mechanical energy into electrical energy. Kinetic energy can be found as a form of vibration, random displacements or forces, and can be converted to electrical energy using piezoelectric, electromagnetic, and electrostatic mechanisms [1]. Piezoelectric materials contain a dipole which can create electrical voltage when subjected to a mechanical force. Conversely, when the electric field is applied, the material can be deformed due to the rotation of the dipole. Therefore, piezoelectric materials are used in a variety of commercial sensor and kinetic energy harvesting applications. The electromagnetic transduction is based on Faradays law of electromagnetic induction. This type of system can be found in bicycle dynamos and Seiko kinetic watches. The electrostatics generators are the third most common method of kinetic energy harvesting. The system consists of charge variable capacitors and changes its capacitance due to the applied vibration. Due to the basic equation of $Q = CV$, the output voltage or charge variation is generated by keeping constant either the charge or the voltage, respectively [1, 5].

Thermoelectric (TE) based energy harvesters are the third most common method of energy harvesting. Converting thermal energy through thermoelectric devices into electricity is called thermoelectric energy harvesting, and can be found in many industrial applications like powering wireless sensors for structural buildings, sensors for engine health monitors, sensors for battlefield surveillance and reconnaissance, as well as medical sensors and implants[2].

1.2 Energy Harvesting system modeling

When the voltage generated from energy harvester is not sufficient, power management systems are needed to power loads. The block diagram in Figure 1.1 depicts basic interface circuit architecture for an energy harvesting system. The main purpose of the energy harvesting systems is to utilize the ambient energy sources to power an applicable

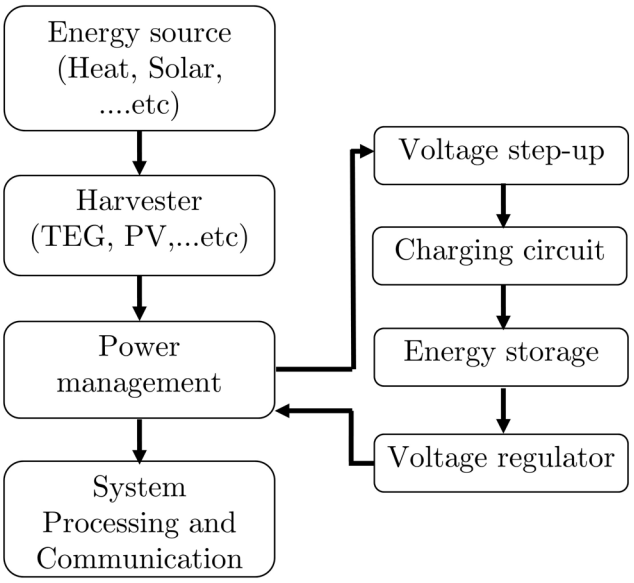

FIGURE 1.1: Energy Scavenging System Block Diagram

load. However, the voltage generated from energy harvesters is in the order of few tens of millivolts to a couple of hundreds of millivolts. This voltage has to be converted into a standard voltage which can be broadly used for other applications. On the other hand, a converter should be able to sustain with input voltage noise and load changes and provide constant voltage with less ripple (voltage droop) throughout the operation period. Voltage droop is a loss in output voltage from a device as it tries to drive load. These droops are major problems in energy harvesting battery-less ULP (Ultra Low Power) systems since they are operating in very low voltages (<0.5 V). Therefore, it is important to have high efficiency power management systems in energy harvesting systems [6].

There are many studies in literature on interface circuit architecture for energy harvesting. There are three main types of switching converters used in energy harvesting battery-less ULP systems.

1. Inductive-based DC-DC converter

This type of converters uses a modulation technique to charge an inductor and boost the DC voltage by transferring the charge on the inductor onto an output capacitor.

2. Capacitive-based converters

Capacitive-based converters use a switching scheme which can transfer the charge between the capacitors by shifting DC voltage levels at each stage. Ideally higher stages can achieve higher boost voltage. The Dickson charge pump, voltage doubler based

charge pump, and Fibonacci switched capacitor converters are widely used converters in energy harvesting system.

3. AC-DC converters

This type of converters is primarily used in piezoelectric energy harvesting systems. Full wave rectifiers and half wave rectifiers with active diodes are widely used for this purpose.

Choosing a converter topology depends on the application, input voltage and load current requirement. These circuits should be optimized based on input power and load requirement to have a maximum converter efficiency. SPICE is one popular tool used for this purpose. However, it requires the user to design a circuit in the tool and do the optimization. This takes a significant amount of time for the user at the design stage. Therefore, building a mathematical model for these converters will help the user to identify various design specification such as suitable topology, transistor sizes, operating frequency range, duty cycle etc.

Many papers in the literature can be found on power converter modeling. Analysis method, developed by Seeman et al. [7] can determine the steady-state performance of switched-capacitor (SC) DC-DC converters through evaluation of its output impedance. Efficiency model of boost DC-DC PWM (Pulsed Width Modulation) converters were developed by Aloisi et al. [8], calculate efficiency of the boost converter based on conduction losses, diode power loss, switching losses, capacitive switching loss and the gate-drive loss, for both continuous conduction mode and discontinuous conduction mode. Shrivastava et al. [9] presents a model of inductor based DC-DC buck converters that can be used to study the impact of power management techniques such as dynamic voltage and frequency scaling (DVFS). However, models proposed by Aloisi et al. [8] and Shrivastava et al. [9] cannot be used to make initial design stage parameters due to unknown parameters used in the model. A unified model, that can connect inductor based DC-DC converters, switch capacitor DC-DC converters and AC-DC converters with fewer unknowns are required to make initial design decision for power management units in system-on-chip application.

1.3 Objective of the Thesis

This thesis contributes to the development of a global energy harvesting model that can accurately model the functionality, energy, and efficiency of functional components of energy scavenging systems. The proposed model can be used to make architectural

design decisions in power management unit using MATLAB Simulink. A comprehensive list of objectives of this thesis is as follows:

1. Study and specification of the blocks required for the energy harvesting block.

2. Create MATLAB models for each converter and verify it functionality using SPICE in 130 nm CMOS technology.

3. Connect the individual converter blocks in MATLAB Simulink to create a global energy harvesting model.

4. Develop a user friendly tool flow without complicated processes so that the user can make quick and accurate architectural design decisions in power management unit in system on chip applications.

While not included in this thesis, the author also made the following contributions to the testing of the battery-less energy harvesting Body Sensor Nodes (BSN) System on Chip (SoC).

1. Power Management Unit (PMU) of the BSN SoC is investigated and the leakage current consumption of the PMU is identified. A thermal testing method was proposed to identify its cause.

2. Band gap reference inside the BSN SoC is investigated and its functionality in Si is verified.

1.4 Outline of the Thesis

The remaining part of the thesis consists of five chapters. Chapter 2 describes the previous work, proposed tool flow of the model and modeling of the low dropout regulator. Modeling of switch capacitor circuit topologies (Dickson, voltage doubler, charge pump circuit with cross connected NMOS cells (NCP4), Fibonacci, series-parallel) discussed in Chapter 3. Chapter 4 introduces the modeling technique for inductor based DC-DC converters (boost converter and buck converter).

Chapter 5 introduces the results and tool implementation of the models. The models were validated using SPICE simulation using 130 nm CMOS technology.

Chapter 6 finalizes the thesis by summarizing the achievements obtained from the models, and outlines the further study areas.

Chapter 2

Previous Work and Modeling of Low-Dropout Regulator

2.1 Previous Work

Power electronic systems are widely used in many applications, ranging from energy harvesting, medical applications, transportation and high-power transmission. The associated power levels range from nanowatts to megawatts.

Modeling and simulation are vital components of the analysis and design process for power electronic converters, which help the designer to get an understanding of the circuit. SPICE is one of the powerful tools used in industry and research fields for this purpose. Choosing a correct converter topology is very important for microwatt energy harvesting systems. The most accurate method is to use SPICE to design a system, and then choose a topology based on simulation. However, it includes many obstacles such as the need for extensive model building, excessively long simulation times, the challenges of automatically identifying and exploiting or hierarchical or modular or time-scale structure [10]. Therefore, it is very important to have a user-friendly model which can give accurate information on converters with less computing time. It helps the designer to choose the correct topology and optimize the system based on the application requirements.

Power converter modeling and, more generally, computer-aided design in power electronics, have been addressed in other journals in past years. Wei et al. [11] introduce a modeling technique of a current mode control boost converter in DCM and CCM mode using MATLAB Simulink. The model elaborated on two different work states, used the concept of digital logic, combined the variables of binary logic, setup the model of

the system, listed the differential equations and simulated the model. The two models presented for DCM and CCM were undesirable for a unified energy harvesting model as it can change the states based on the load current and frequency change. Also, the model doesn't include any parasitic effect such as V_t drop on the active or passive diode, the series resistance of switches and inductors which prevent generating accurate output voltages or efficiency values for micro-watt range power converter systems.

An Average model, together with conduction losses for the switch network of the pulse width modulated (PWM) DC-DC converters working at the boundary between discontinuous inductor current mode (DICM) and continuous conduction mode (CCM), was developed by Jingquan et al. [12]. The model was verified through PSpice and CASPOC simulation in the ampere (A) current range and at V_{in}=20 V. Therefore, the model accuracy is unknown for milliampere (mA) current range.

Christophe Batard et al. [13] proposed a method of simulating power converters using MATLAB-Simulink without using a tool dedicated to the simulation of power electronic systems, such as PSIM, SABER, PSCAD and the SimPowerSystems toolbox of Simulink. It introduced the simulation of closed loop and open loop boost, buck, DC-AC converters in DCM and CCM modes. However, it did not include any parasitic effects, thus the predicted result will deviate from the simulation.

Michael Douglas Seeman [14] developed a direct analysis method to evaluate a switched-capacitor converter's output impedance along with an optimization method to improve the performance of these converters through module sizing based on practical restrictions. Several switched-capacitor converter topologies are compared in two asymptotic limits:the fast switching region and the slow switching region. The code from reference [14] is used here in this thesis and modified in order to make a unified model of energy harvesting systems. The method can be used to derive the efficiency of a converter within a short period of time.

Chien et al. [15] proposed analytical models for voltage doublers and PMOS charge pumps using dynamic charge transfer waveforms and charge balance methods, respectively. The models were validated in Si using 0.18 μm CMOS technology. Nonlinearity of the on resistance of the switches was avoided by using dynamical analysis methods.

Hanh et al. [16] developed a design technique to maximize the efficiency and power density of a fully integrated switched-capacitor (SC) DC-DC converter. SC loss optimization was described in detail. Also, the optimum switching frequency and optimum switching widths were derived.

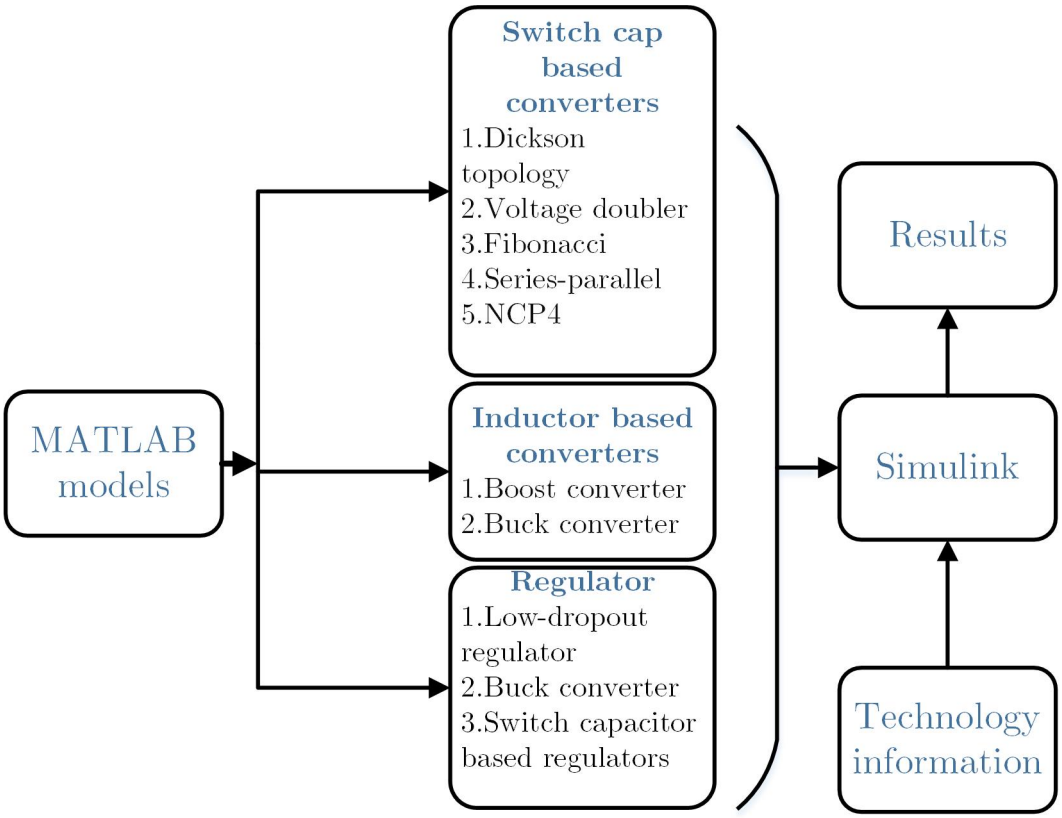

FIGURE 2.1: Tool flow of the complete energy harvesting model

2.2 Proposed Model

The tool flow of the complete energy harvesting model is given by Figure 2.1. The model consists of a boost converter, a regulator and a storage capacitor. The model of AC-DC converters is not included and it reserved for future addition to the existing model. All individual models were created in MATLAB and connected through the MATLAB Simulink interface. There is a separate file to provide technology information for models. The user can update the technology library once the information is available. Currently, technology information consists only of IBM 130 nm CMOS technology, as it uses in the current BSN SoC.

The energy flow of the proposed unified model of the energy harvesting system model designed in MATLAB Simulink is shown in Figure 2.2. External MATLAB code is used to run the parametric simulation in order to optimize the system performance and identify the required switching frequency, device sizes, ripple ratio, optimum step-up ratio, etc.

The detail description of the symbols are listed in the following Table 2.1.

TABLE 2.1: The detail description of the symbols in Figure 2.2

Symbol	Description
$V_{in}(t)$	Time varying input signal
$V_{Boost}(t)$	Time varying boosted voltage
$\eta_{Boost(t)}$	Time varying boosted converter efficiency
$P_{Loss}(t)$	Time varying converter loss
$V_{regulated}$	Regulated voltage
$\eta_{Reg}(t)$	Regulator efficiency
$I_L(t)$	Time varying Load current

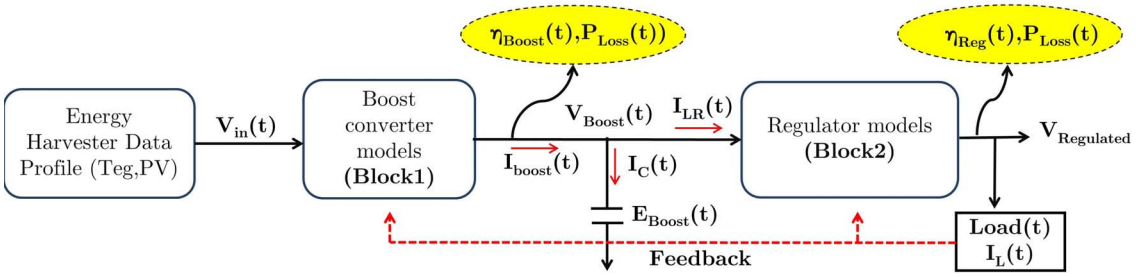

FIGURE 2.2: The block diagram of the energy flow in the system

Equation 2.1 describes the calculation of intermediate current values, except current through the capacitors. $V_{in}(t)$, $I_{in}(t)$, $f(t)$ and $I_L(t)$, which are known initial parameters.

$$I_{LR(t)} = \frac{V_{regulated} \times I_{L(t)}}{V_{Boost(t)} \times \eta_{Reg(t)}} \tag{2.1}$$

$$I_{Boost(t)} = I_{c(t)} + I_{LR(t)} \tag{2.2}$$

The current through the capacitor is calculated using following Simulink model. The basic equation for the capacitor (C) in series with a resistor (R) is shown in Equation 2.3 where V_{in} is the input voltage and V_{cap} is the voltage across a capacitor. The resistor (R) here represents the output impedance of a converter.

$$\frac{dV_{cap}}{dt} = \frac{1}{RC}(V_{in} - V_{cap}) \tag{2.3}$$

By plugging the Simulink model in to the Figure 2.2, $I_c(t)$ can be found.

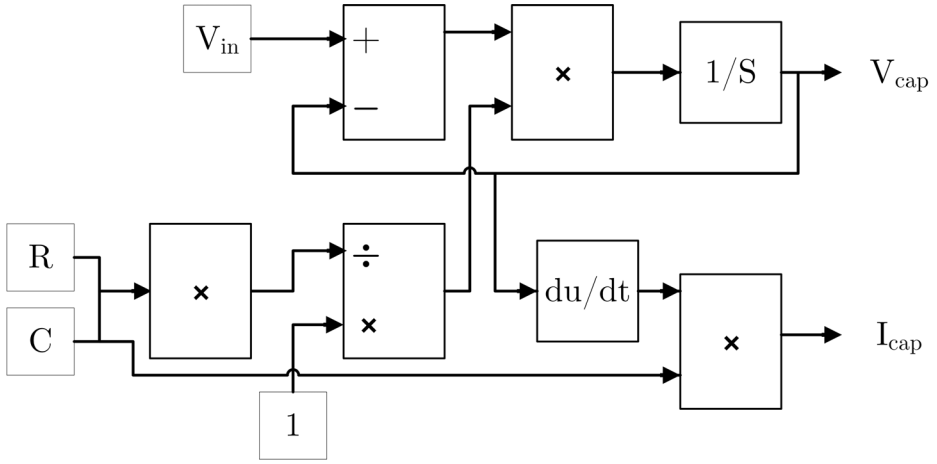

FIGURE 2.3: Simulink block diagram of the capacitor model

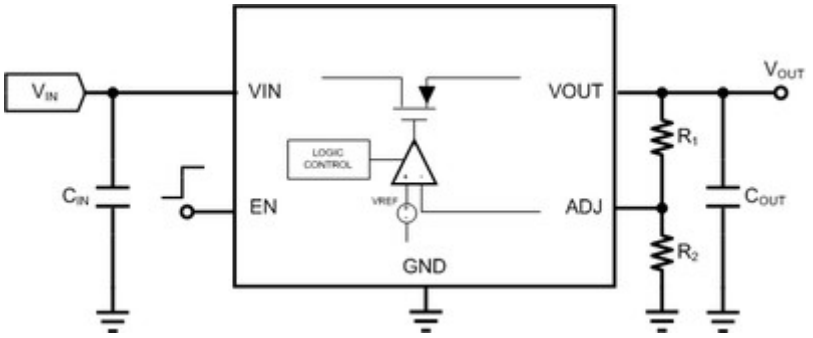

FIGURE 2.4: The schematic diagram of a LDO [17]

2.3 Modeling of Low-Dropout Regulator(LDO)

A low-dropout or LDO regulator is a DC linear voltage regulator that can regulate the output voltage even when the output voltage is very close to the input voltage. The schematic diagram of a LDO is shown in Figure 2.4.

The main advantages of LDOs over switching regulators are less noise, smaller device size and greater design simplicity. Dissipation of power across the regulation device and lower efficiency when the regulated voltage is much lower than the output voltage are disadvantages of LDO circuits. Therefore, it is important to model LDOs to identify optimum device size and efficiency [17].

The power loss and efficiency of an LDO are give in Equations 2.4 and 2.5 respectively.

$$P_{loss} = (V_{in} - V_{out}) \times I_{out} + (V_{in} \times I_Q) \tag{2.4}$$

$$\eta = \frac{P_{out} - P_{loss}}{P_{in}} \tag{2.5}$$

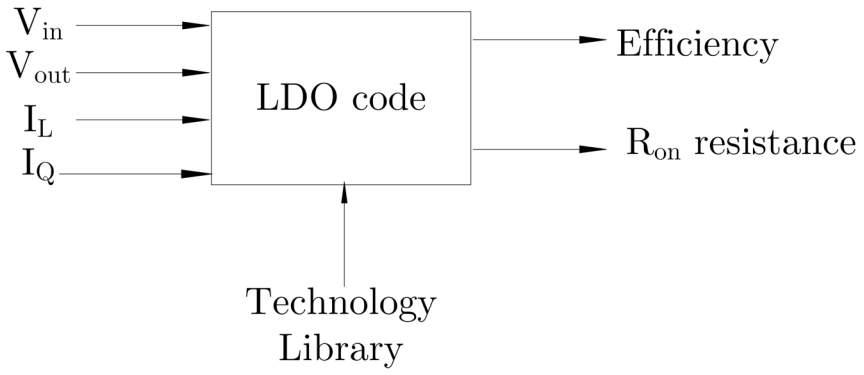

FIGURE 2.5: LDO block diagram

Where V_{in} = Input voltage, V_{out} = output voltage, P_{in} = input Power, P_{loss} = loss of the LDO, I_Q = quiescent current required by the LDO for its internal circuit.

The block diagram of the model of the LDO device is shown in Figure 2.5. The left side shows the input and the right side shows the output of the system. For a given technology library and for a given specification, the model can extract the LDO efficiency and will be useful for the unified model. The individual model is validated through SPICE simulation with 130 nm CMOS technology and the results will be discussed in chapter 5.

Chapter 3

Modeling of Switch Capacitor(SC) type DC-DC converters

3.1 Introduction

Figure 3.1 shows a capacitive DC-DC converter. It consists of two parts, the control block and the conversion block. The conversion block is the heart of the converter and the control part is a high impedance feedback path from the conversion characteristics (output voltage, output current,...) to at least one of the control parameters of the conversion block (switching frequency, duty cycle of the switching frequency,...) [18].

Figure 3.2 shows a simplified model for loss calculation. The series losses are represented by the equivalent output resistance R_0 and the shunt losses by the parallel resistor R_P, and the transformer represents the ideal voltage conversion ratio. V_0 represents the final output voltage of the converter [16].

The model will focus only on the conversion part. The impedance calculation of the switch capacitor model is carried out using the charge flow analysis method. The charge vectors can be defined by states. The charge flow through the capacitors is described by Equation 3.1 and Equation 3.2 [14].

$$a_c^{(1)} = (q_{out}^{(1)}, q_1^{(1)}, q_2^{(1)}, ..., q_n^{(1)}, q_{in}^{(1)})/q_{out} \tag{3.1}$$

$$a_c^{(2)} = (q_{out}^{(2)}, q_1^{(2)}, q_2^{(2)}, ..., q_n^{(2)}, q_{in}^{(2)})/q_{out} \tag{3.2}$$

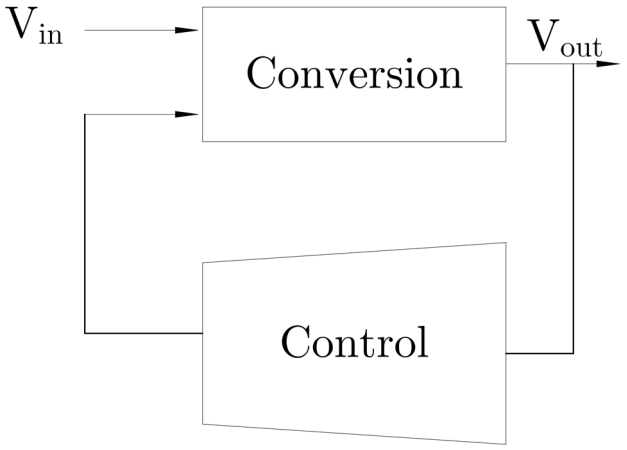

FIGURE 3.1: Graphical representation of the DC−DC converter system partitioning: the conversion block executes the DC−DC conversion and the control block controls the behavior of the conversion block [18]

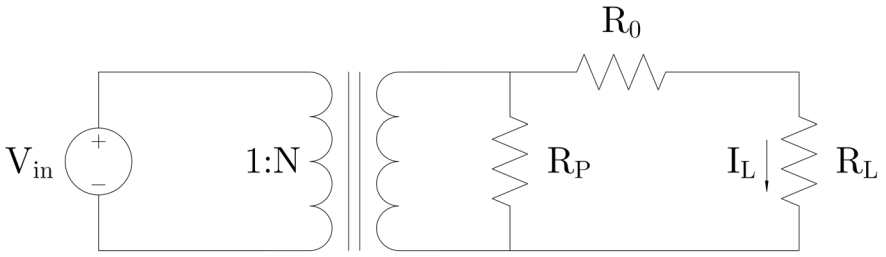

FIGURE 3.2: Simplified model for switch capacitor converter loss calculations

Charge flows through the switch resistors are described by Equation 3.3 and Equation 3.4 [14].

$$a_r^{(1)} = (q_{out}^{(1)}, q_1^{(1)}, q_2^{(1)}, ..., q_n^{(1)}, q_{in}^{(1)})/q_{out} \tag{3.3}$$

$$a_r^{(2)} = (q_{out}^{(2)}, q_1^{(2)}, q_2^{(2)}, ..., q_n^{(2)}, q_{in}^{(2)})/q_{out} \tag{3.4}$$

These charge vector elements can be determined by inspection for each states of the conversion period based on the following principles [18]:

- Kirchhoffs current law in each node.
- In steady state, for every component the sum of both states charge flow elements is equals to zero.
- Assume no voltage ripple at the output node if $C_{out}>>>C_{fly}$ where C_{out} is output capacitance and C_{fly} is the flying capacitance in SC.

3.2 Derivation of Fast and Slow switching impedances

The following equality in Equation 3.5 can be obtained by superposition of both states based on Tellegen's theorem [18].

$$v_{out}(a_{out}^{(1)} + a_{out}^{(2)}) + \sum_{i=1}^{n}(a_{c,i}^{(1)}v_{c,i}^{(1)} + a_{c,i}^{(2)}v_{c,i}^{(2)}) = 0 \tag{3.5}$$

The following simplification can be applied to the equation 3.5:

- $a_{out}^{(1)} + a_{out}^{(2)} = 1$
- $a_{c,i}^{(1)} = -a_{c,i}^{(2)} = a_{c,i}$
- $q_i = a_{c,i}q_{out}$

These simplifications reduce Equation 3.5 into 3.6.

$$v_{out}q_{out} + \sum_{i=1}^{n}(q_i\Delta v_i) = 0 \tag{3.6}$$

By assuming linear behavior and no voltage ripple at the output voltage then Δv_i is given by Equation 3.7.

$$\Delta v_i = q_i/C_i \tag{3.7}$$

If C_{out} is comparable to C_i, Δv_i can be written as in Equation 3.8. The derivation of Equation 3.8 can be found in [18].

$$\Delta v_i = \frac{q_i}{C_i}\frac{C_{out}}{C_{out} + C_i} \tag{3.8}$$

By dividing Equation 3.6 by q_{out}^2 and f_{sw} (where f_{sw} is the switching frequency) and substituting into Equation 3.7 the following equality can be obtained:

$$\frac{v_{out}}{q_{out}f_{sw}} = \frac{v_{out}}{i_{out}} = \sum_{i=1}^{n}(\frac{q_i}{q_{out}})^2\frac{1}{f_{sw}C_i} \tag{3.9}$$

Slow switching impedance (RSSL) can be obtained with no ripple approximation as in Equation 3.10 and with ripple as in 3.11, respectively. Here, n represents number of capacitors in the topology.

$$R_{SSL} = \sum_{i=1}^{n} \frac{a_{c,i}^2}{f_{sw} C_i} \tag{3.10}$$

$$R_{SSL} = \sum_{i=1}^{n} \frac{a_{c,i}^2}{f_{sw} C_i} \frac{C_{out}}{C_{out} + C_i} \tag{3.11}$$

The Fast switching impedance (R_{FSL}) is dominant for higher frequency regime since R_{SSL} is very small at a higher frequency. The power losses due to switch resistances are dominant in this regime. Each element $a_{r,i}$ of the vector corresponds to the charge flow through one of the switches S_r. Current through each switch is given by Equation 3.12, where D is the duty cycle of the clock.

$$i_{r,i} = \frac{q_{r,i} f_{sw}}{D} \tag{3.12}$$

By considering the following assumption, the $i_{r,i}$ can be written as in Equation 3.13.

- $q_{r,i} = a_{r,i} q_{out}$
- $q_{out} = \frac{i_{out}}{f_{sw}}$
- $D = 0.5$ for optimum performance

$$i_{r,i} = 2 a_{r,i} i_{out} \tag{3.13}$$

The power loss in the switches can now be formulated as in Equation 3.14. Here R_i is the on resistance of the switches in SC.

$$P_{losses,switches} = \sum_{i=1}^{n} (0.5 R_i (2 a_{r,i} i_{out})^2) \tag{3.14}$$

The Fast switching impedance (R_{FSL}) can be obtained by dividing Equation 3.14 by i_{out}^2, and it is shown in Equation 3.15. Here, n represents number of switches in the topology.

$$R_{FSL} = 2\sum_{i=1}^{n} R_i a_{r,i}^2 \tag{3.15}$$

The total output impedance and the non ideal output voltage of SC are given by Equations 3.16 and 3.17 respectively. V_t is the threshold voltage of the switching transistor and N is the number of stages of SC. However, in some topologies, V_t drop can be neglected.

$$R_{out,total} = \sqrt{R_{FSL}^2 + R_{SSL}^2} \tag{3.16}$$

$$V_{out} = (N+1)(V_{DD} - V_t) - R_{out,total} I_L \tag{3.17}$$

3.3 Loss analysis model of the switch capacitor

There are two types of losses available, resistive loss and capacitive loss. Switch resistive losses can be written as [16].

$$P_{R_{sw}} = I_{Load} \times \frac{R_{on}}{W_{sw}} \times M_{sw} \tag{3.18}$$

$$M_{sw} = N_{sw,total} \times (\frac{T_{ph1}}{T} \times N_{sw,on,ph1} + \frac{T_{ph2}}{T} \times N_{sw,on,ph2}) \tag{3.19}$$

Where, T_{ph1} is the phase 1 of the clock, $N_{sw,on,ph1}$ is the number of switches during the phase 1.

Capacitive losses are given by:

$$P_{sw,loss} = \frac{I_{Load}^2}{M_{cap} \times C_{fly} \times f_{sw}} \tag{3.20}$$

M_{cap} is a constant depend on the topology. Total switch resistance can be calculated using Equation 3.21.

$$P_{sw,loss,total} = I_{Load}^2 \times R_{out,total} = P_{R_{sw}} + P_{sw,loss} \tag{3.21}$$

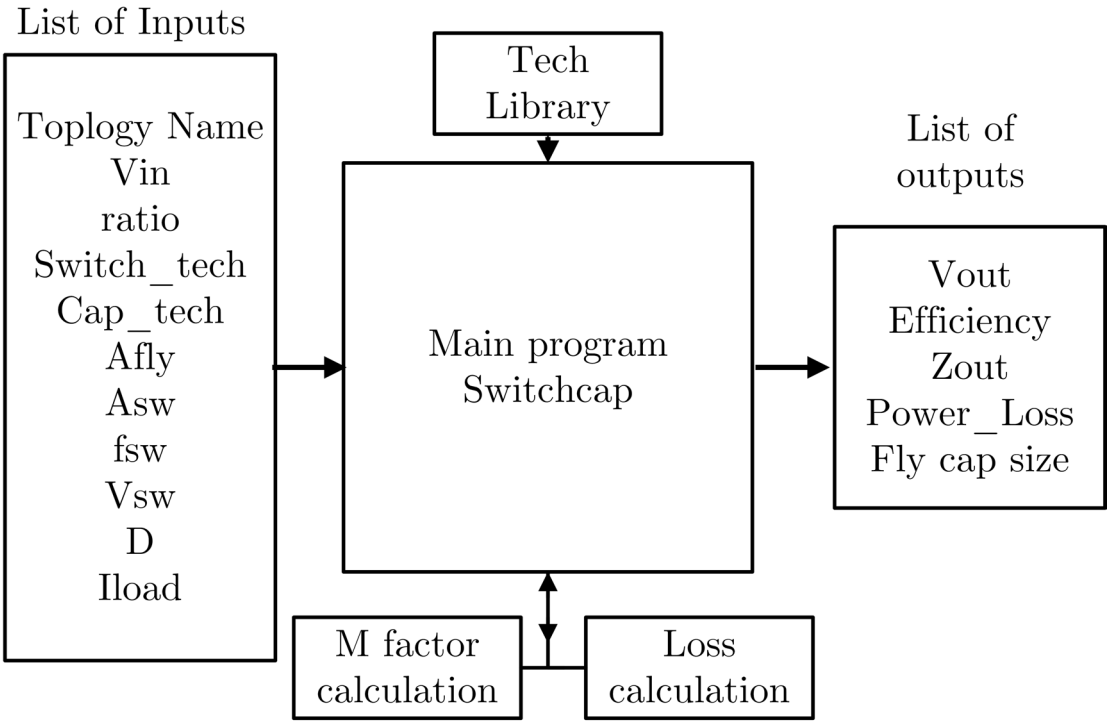

FIGURE 3.3: Block diagram of the switch cap model

The other key portion of an SC converter's losses comes from the shunt losses arising from switching the parasitic capacitance of flying capacitors and power switches. The bottom plate capacitance loss is given by:

$$P_{bott-cap} = M_{bott} \times V_{out}^2 \times C_{bot} \times f_{sw} \tag{3.22}$$

M_{bott} is a constant determined by the converter topology. The gate parasitic capacitance switching loss is given by:

$$P_{gate-cap} = V_{sw}^2 \times C_{gates} \times W_{sw} \times f_{sw} \tag{3.23}$$

Where C_{gate} is the gate capacitance density (F/m) of the switches.

The block diagram of the model is shown in Figure 3.3. The model includes basic topology architectures used in low voltage energy harvesting systems (Dickson, voltage doubler, series-parallel, Fibonacci,...etc). A_{fly} and A_{sw} represent the switch cap and switch resistance area in m^2, D-duty cycle, ratio-step up/down ratio, V_{sw}-switching amplitude, Switch-tec and Cap-tech represent the technology used for the switches and the capacitors respectively.

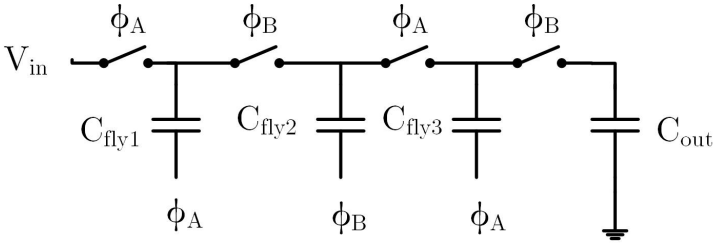

FIGURE 3.4: Three stage Dickson charge pump [2]

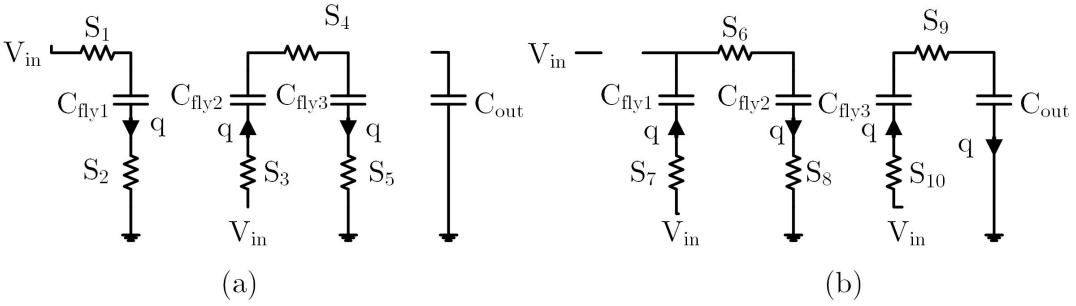

FIGURE 3.5: The charge flow analysis of the Dickson converter [18]

3.4 The Dickson charge pump

Conventional Dickson charge pump consists of capacitors interconnected by diodes and fed by two opposite phase clocks. In CMOS technology the diodes are replaced by diode-connected MOSFETs. Figure 3.4 represents the implementation of the Dickson charge pump [2].

Charge flow analysis of the Dickson converter is shown in Figure 3.5.

Based on the charge flow analysis, the charge vectors can be written by excluding the q_{out} and q_{in}. Charge vectors through capacitors are shown in Equation 3.24 and Equation 3.25. Charge vectors through the switches are shown in Equation 3.26 and Equation 3.27.

$$a_c^{(1)} = [(-1)(+1)(-1)] \tag{3.24}$$

$$a_c^{(2)} = [(+1)(-1)(+1)] \tag{3.25}$$

$$a_r^{(1)} = [1010101010] \tag{3.26}$$

$$a_r^{(2)} = [0101010101] \tag{3.27}$$

The general equation for impedance calculation can be written as follows

$$R_{SSL} = \sum_{i=1}^{n} \frac{N-1}{f_{sw} C_i} \frac{C_{out}}{C_{out} + C_i} \tag{3.28}$$

$$R_{FSL} = 2(3N-2) \sum_{i=1}^{n} R_i \tag{3.29}$$

Where N is the step up ratio and can be defined as in Equation 3.30 and it is 4 for 3-stage Dickson charge pump topology.

$$N = \frac{q_{in}}{q_{out}} \tag{3.30}$$

Switch resistive loss and switch capacitor loss of the 3-stage Dickson charge pump can be written as follows;

$$P_{R_{sw}} = I_{Load} \times \frac{R_{on}}{W_{sw}} \times 50 \tag{3.31}$$

$$P_{sw,loss} = \frac{I_{Load}^2}{\frac{1}{3} \times C_{fly} \times f_{sw}} \tag{3.32}$$

3.5 Voltage doubler (Conventional cascaded structure)

The conventional voltage doubler is a broadly used parallel-series capacitive DC-DC converter. Each voltage doubler doubles the DC input voltage. By cascading n voltage doublers the output voltage increases up to 2^n times [19]. Figure 3.6 shows a conventional cascaded voltage doubler. This results in larger voltage multiplication than a Dickson converter where the gain increases linearly instead of exponentially [18].

Charge flow analysis of a two stage voltage doubler is shown in Figure 3.7. The voltage doubler consists of three flying capacitors C_{fly1} , C_{fly2}, C_{fly3}, a single output buffer capacitor C_{out} and eight switches S_{1-8}.

Based on the charge flow analysis, the charge vectors can be written by excluding q_{out} and q_{in} for the purpose of calculating the impedance as follows. The charge vectors through capacitors are shown in 3.33 and 3.34. The charge vectors through the switches (S_1 to S_8) are showing in Equation 3.35 and Equation 3.36.

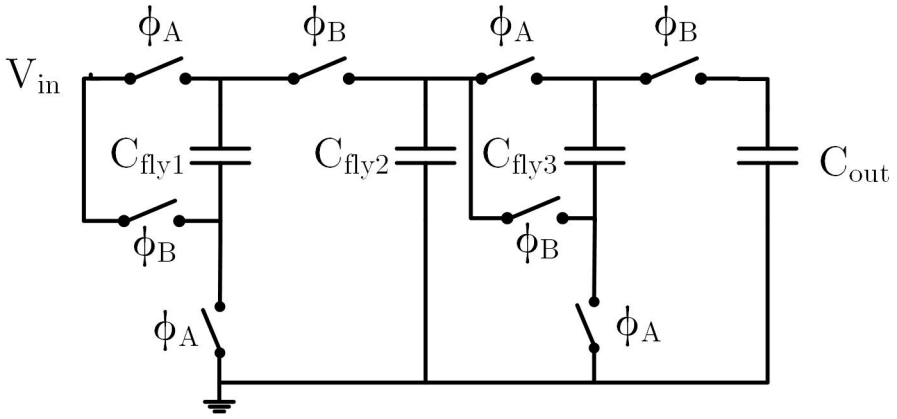

FIGURE 3.6: The conventional cascaded voltage doubler structure [14]

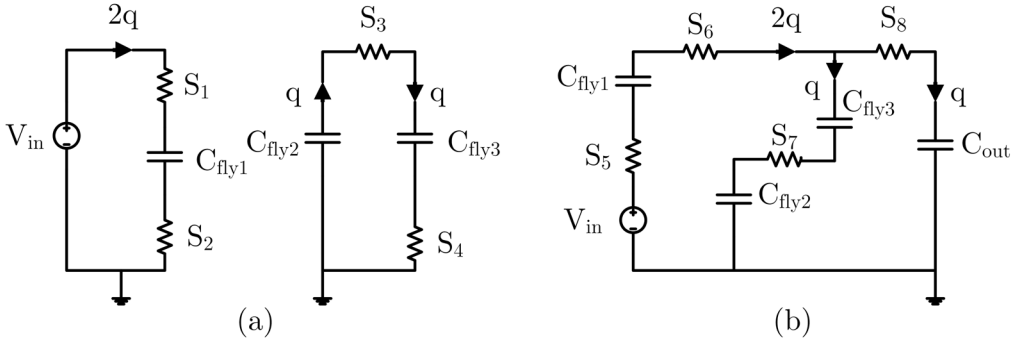

FIGURE 3.7: Charge flow analysis of two stage voltage doubler (conventional cascaded structure). (a) Phase 1 (b) Phase 2

$$a_c^{(1)} = [(-2)(+1)(-1)] \tag{3.33}$$

$$a_c^{(2)} = [(+2)(-1)(+1)] \tag{3.34}$$

$$a_r^{(1)} = [22110000] \tag{3.35}$$

$$a_r^{(2)} = [00002211] \tag{3.36}$$

The impedance calculation of two stage conventional cascaded voltage doubler structure is shown in Equation 3.37 and Equation 3.38 respectively.

$$R_{SSL} = \sum_{i=1}^{n} \frac{6}{f_{sw} C_i} \frac{C_{out}}{C_{out} + C_i} \tag{3.37}$$

$$R_{FSL} = 2(20) \sum_{i=1}^{n} R_i \tag{3.38}$$

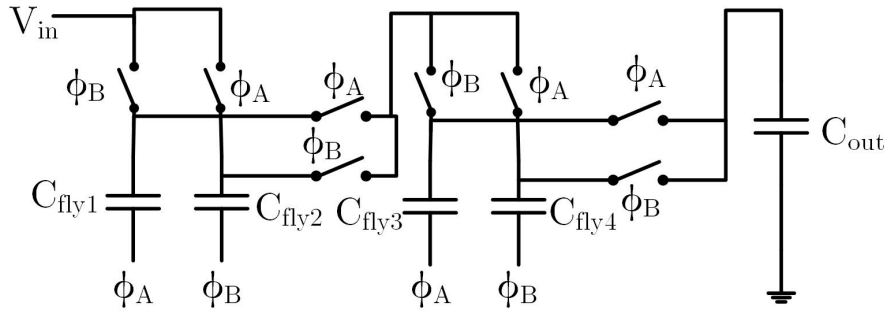

FIGURE 3.8: Two stage charge pump circuit with cross connected cells [20]

N is the step up ratio and can be defined as in Equation 3.39. N = 4 for the 2-stage conventional cascaded voltage doubler structure.

$$N = \frac{q_{in}}{q_{out}} = \frac{4}{1} \tag{3.39}$$

Switch resistive loss and switch capacitor loss of the 2-stage conventional cascaded voltage doubler structure can be written as follows;

$$P_{R_{sw}} = I_{Load} \times \frac{R_{on}}{W_{sw}} \times 32 \tag{3.40}$$

$$P_{sw,loss} = \frac{I_{Load}^2}{\frac{1}{6} \times C_{fly} \times f_{sw}} \tag{3.41}$$

3.6 Charge pump circuit with cross connected NMOS cells

Bhalerao et al. [20] proposed a circuit which can be used for low voltage application around 0.9 V to 2.1 V. This circuit is an extended version of the NCP-2 charge pump which is proposed by [21]. This version consists of cross connected NMOS cells and it pumps charge for the entire duration of the clock period. Figure 3.8 represents a two stage charge pump circuit with cross connected cells. NMOS and PMOS on the circuit are replaced by switches for simplicity. The circuit shows a remarkable improvement in efficiency compared to the previously reported charge pump circuits and can be found in energy harvesting circuits [22],[23] and [24] with starting voltages of 0.2 V or lower.

Charge flow analysis of the two stage charge pump circuit with cross connected NMOS cells is shown in Figure 3.9. The charge pump circuit consists of four flying capacitors

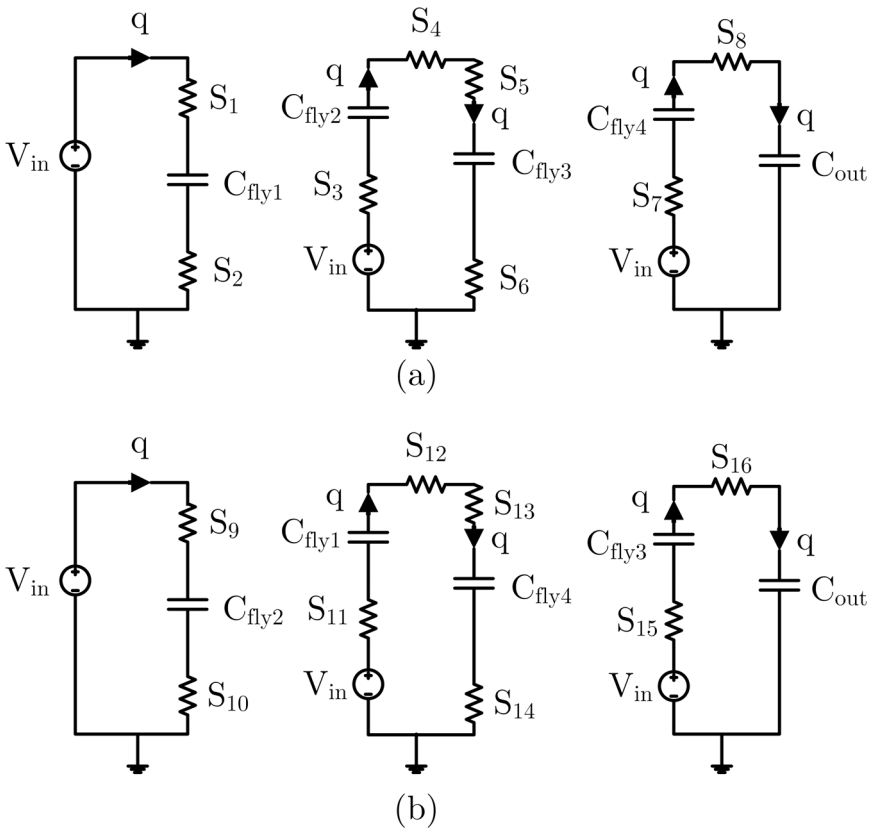

FIGURE 3.9: Charge flow analysis of two stage charge pump circuit with cross connected NMOS cells. (a) Phase 1 (b) Phase 2

C_{fly1}, C_{fly2}, C_{fly3}, C_{fly4}, a single output buffer capacitor C_{out} and sixteen switches S_{1-16}.

Based on the charge flow analysis, the charge vector can be written by excluding the q_{out} and q_{in} for the purpose of calculating the impedance as follows. The charge vectors through capacitors are shown in Equation 3.42 and Equation 3.43. The charge vectors through the switches (S_1 to S_4) are shown in Equation 3.44 and Equation 3.45.

$$a_c^{(1)} = [(-1)(+1)(-1)(+1)] \tag{3.42}$$

$$a_c^{(2)} = [(+1)(-1)(+1)(-1)] \tag{3.43}$$

$$a_r^{(1)} = [1111111100000000] \tag{3.44}$$

$$a_r^{(2)} = [0000000011111111] \tag{3.45}$$

The impedance calculation of N stage charge pump circuit with a cross connected NMOS cells converter structure is shown in Equation 3.46 and Equation 3.47 respectively.

$$R_{SSL} = \sum_{i=1}^{n} \frac{2(N-1)}{f_{sw}C_i} \frac{C_{out}}{C_{out}+C_i} \tag{3.46}$$

$$R_{FSL} = 2(8(N-1)) \sum_{i=1}^{n} R_i \tag{3.47}$$

N is the step up ratio and can be defined as in Equation 3.48 and N = 3 for two stage charge pump circuit with cross connected NMOS cells structure.

$$N = \frac{q_{in}}{q_{out}} = \frac{6}{2} = 3 \tag{3.48}$$

Switch resistive loss and switch capacitor loss of the two stage charge pump circuit with cross connected NMOS cells structure can be written as follows ;

$$P_{R_{sw}} = I_{Load} \times \frac{R_{on}}{W_{sw}} \times 128 \tag{3.49}$$

$$P_{sw,loss} = \frac{I_{Load}^2}{0.25 \times C_{fly} \times f_{sw}} \tag{3.50}$$

3.7 Series-parallel structure

Series-parallel topology implements a step-up converter by connecting all n-1 capacitors in parallel to the input source in phase one. In phase two, the capacitors are connected in series with each other and the input source to deliver charge to the output capacitor [7]. The one stage step down series-parallel converter is shown in Figure 3.10.

The charge flow analysis of the one stage step down series-parallel converter is shown in Figure 3.11. The one stage step down series-parallel converter consists of one flying capacitor C_{fly1}, a single output buffer capacitor C_{out} and four switches S_{1-4}.

Based on the charge flow analysis, the charge vector can be written by excluding the q_{out} and q_{in}. The charge vectors through capacitors are shown in Equation 3.51 and Equation 3.52. The charge vectors through the switches (S_1 to S_4) are showing Equation 3.53 and Equation 3.54

$$a_c^{(1)} = [(-\frac{1}{2})] \tag{3.51}$$

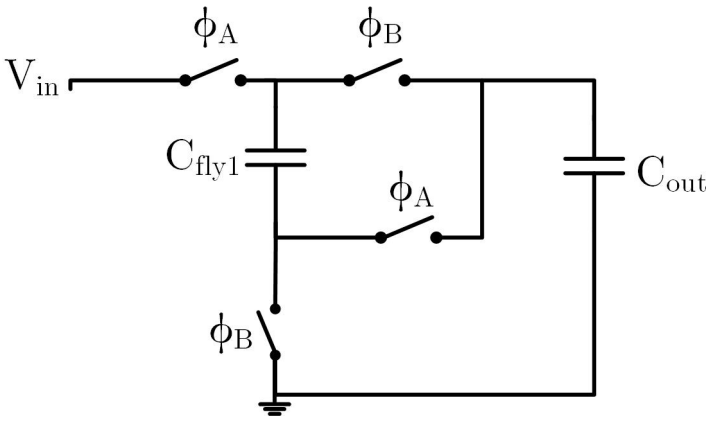

FIGURE 3.10: One stage step down series-parallel converter [25]

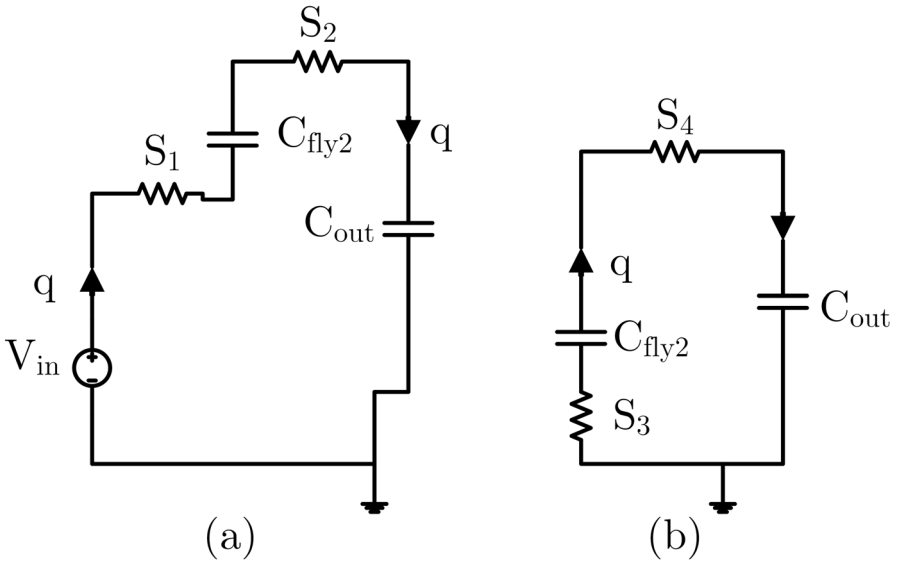

FIGURE 3.11: Charge flow analysis of the one stage step down series-parallel converter. (a) Phase 1 (b) Phase 2

$$a_c^{(2)} = [(+\frac{1}{2})] \tag{3.52}$$

$$a_r^{(1)} = [\frac{1}{2}\frac{1}{2}00] \tag{3.53}$$

$$a_r^{(2)} = [00\frac{1}{2}\frac{1}{2}] \tag{3.54}$$

The impedance calculation of the one stage step down series-parallel converter structure is shown in Equation 3.55 and Equation 3.56, respectively.

$$R_{SSL} = \sum_{i=1}^{n} \frac{0.25}{f_{sw}C_i} \frac{C_{out}}{C_{out} + C_i} \tag{3.55}$$

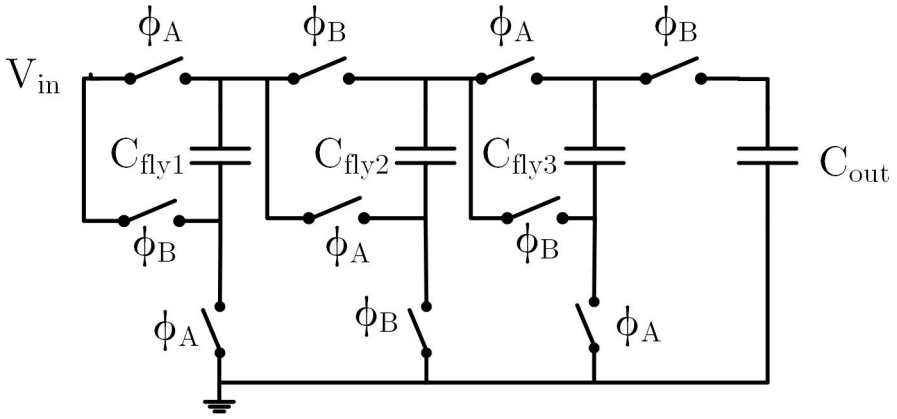

FIGURE 3.12: Schematic diagram of a 3-stage Fibonacci Charge pump [26]

$$R_{FSL} = 2(1)\sum_{i=1}^{n} R_i \tag{3.56}$$

N is the step up ratio and can be defined as in Equation 3.57 and it is 0.5 for one stage step down series-parallel converter structure.

$$N = \frac{q_{in}}{q_{out}} = \frac{1}{2} \tag{3.57}$$

Switch resistive loss and switch capacitor loss of the one stage step down series-parallel converter structure can be written as follows;

$$P_{R_{sw}} = I_{Load} \times \frac{R_{on}}{W_{sw}} \times 8 \tag{3.58}$$

$$P_{sw,loss} = \frac{I_{Load}^2}{4 \times C_{fly} \times f_{sw}} \tag{3.59}$$

3.8 Fibonacci topology

The Fibonacci topology is another viable topology that can be used in energy harvesting applications, since it can generate the largest conversion ratio for a given number of capacitors. Compare to the Dickson charge pump, Fibonacci topology can generate the same gain with fewer stages. Detailed analysis of Fibonacci topology can be found in depth in references [7, 26, 27]. The three stage Fibonacci charge pump is shown in Figure 3.12.

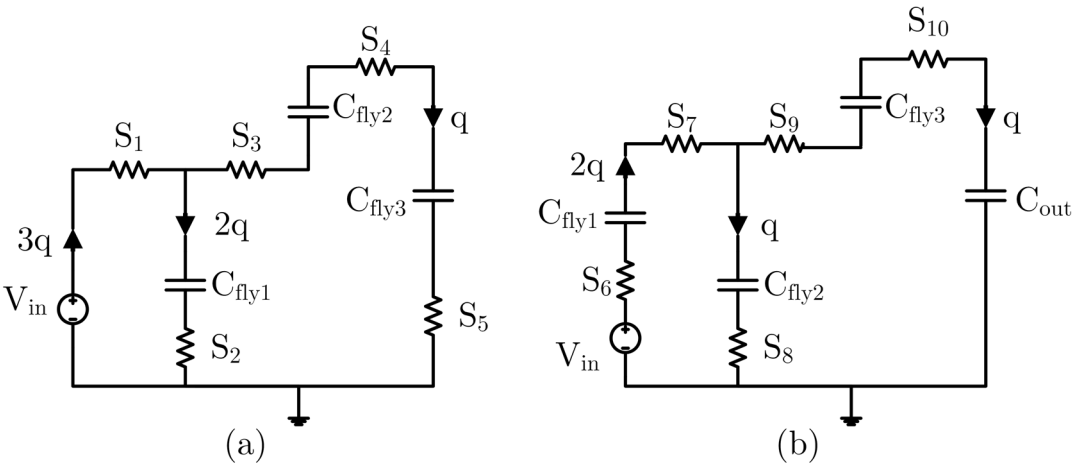

FIGURE 3.13: Charge flow analysis of the three stage Fibonacci charge pump. (a) Phase 1 (b) Phase 2

Using k capacitors (not including the input and output capacitors), a conversion ratio of n = F_{k+2} can be obtained, where k is a positive integer. For instance, with 3 capacitors, a conversion ratio of 5 can be obtained [14]. The i^{th} Fibonacci number can be obtained as shown in Equation 3.60, where $i \geq 1$.

$$F_i = \frac{\Phi^j - (1-\Phi)^j}{\sqrt{5}} = 1, 1, 2, 3, 5, ... \tag{3.60}$$

Where Φ is the golden ratio and defined as in Equation 3.61

$$\Phi = \frac{(1+\sqrt{5})}{2} = 1.618..... \tag{3.61}$$

Charge flow analysis of a three stage Fibonacci charge pump is shown in Figure 3.13. The Fibonacci charge pump consists of three flying capacitors C_{fly1}, C_{fly2}, C_{fly3}, a single output buffer capacitor C_{out} and four switches S_{1-10}.

Based on the charge flow analysis, charge vectors can be written by excluding q_{out} and q_{in}. The charge vectors through capacitors are shown in Equation 3.62 and Equation 3.63. The charge vectors through the switches (S_1 to S_{10}) are shown in Equation 3.64 and Equation 3.65.

$$a_c^{(1)} = [(-2)(+1)(-1)] \tag{3.62}$$

$$a_c^{(2)} = [(+2)(-1)(+1)] \tag{3.63}$$

$$a_r^{(1)} = [3211100000] \tag{3.64}$$

$$a_r^{(2)} = [0000022111] \tag{3.65}$$

The impedance calculation of the three stage Fibonacci charge pump is shown in Equation 3.66 and Equation 3.67 respectively.

$$R_{SSL} = \sum_{i=1}^{n} \frac{6}{f_{sw} C_i} \frac{C_{out}}{C_{out} + C_i} \tag{3.66}$$

$$R_{FSL} = 2(27) \sum_{i=1}^{n} R_i \tag{3.67}$$

Where N is the step up ratio and can be defined as in Equation 3.68 and N = 5 for the three stage Fibonacci charge pump.

$$N = \frac{q_{in}}{q_{out}} = \frac{5}{1} \tag{3.68}$$

Switch resistive loss and switch capacitor loss of the three stage Fibonacci charge pump can be written as follows;

$$P_{R_{sw}} = I_{Load} \times \frac{R_{on}}{W_{sw}} \times 50 \tag{3.69}$$

$$P_{sw,loss} = \frac{I_{Load}^2}{\frac{1}{6} \times C_{fly} \times f_{sw}} \tag{3.70}$$

Table 3.1 illustrates how the different topologies can be compared based on their output impedances. The fly capacitance size and on-resistance of each stage of the converter are assumed to be identical for simplicity. Based on the Table 3.1, the highest theoretical efficiency can be achieved by using Dickson or series-parallel topology. However, the Dickson topology suffers diode drops across the stages due to the diode connected MOSFET used in the circuit. Therefore, series-parallel topology would be suitable for low voltage applications. Series losses can be minimized by selecting a suitable frequency, fly capacitance area and switch resistance area. Even though a large fly capacitance area or switch resistance area reduces the series losses, it increases parallel losses and degrades the converter efficiency.

TABLE 3.1: Comparison of different topologies based on its output impedance

3-stage switch capacitor topology	R_{SSL}	R_{FSL}
Dickson	$\frac{3}{f_{sw}C_{fly}}$	$20 \times R_{on}$
NCP4	$\frac{6}{f_{sw}C_{fly}}$	$48 \times R_{on}$
Series-Parallel	$\frac{3}{f_{sw}C_{fly}}$	$20 \times R_{on}$
Doubler	$\frac{6}{f_{sw}C_{fly}}$	$40 \times R_{on}$
Fibonancci	$\frac{6}{f_{sw}C_{fly}}$	$54 \times R_{on}$

Chapter 4

Modeling of Inductive-based DC-DC converter

4.1 Inductive-based boost DC-DC converter

4.1.1 Introduction

Inductive-based boost DC-DC converter uses a modulation technique to charge the inductor and boost the DC voltage by transferring charge on the inductor onto an output capacitor. This type of converter is widely used in energy harvesting circuits [28], [29]. Therefore, investigating and modeling the inductive based boost DC-DC converters are essential to identifying the suitable converter based on the application.

The circuit of a PWM boost DC-DC converter is shown in Figure 4.1 (a). Its output voltage V_O is always higher than its input voltage V_I for steady-state operation. The boost converter consists of an inductor (L) , a power MOSFET (S), a diode (D), a output capacitor (C), and a load resistor (R_L). Here, ideal diode is used for simplicity. Usually in low voltage applications, diode D is replaced by a MOSFET to avoid extra losses due to the forward voltage of a diode. The switch S is turned on and off at the switching frequency $f_s = 1/T$ with the ON duty ratio $D = t_{on}/T$, where t_{on} is the ON time of the switch S. The converter can operate in either discontinuous conduction mode (DCM) or continuous conduction mode (CCM), depending on the waveform of the inductor current [30]. Figure 4.1[(b)-(c)] shows the operation principle of CCM of the boost converter.

The idealized wave form of the PWM boost converter for CCM is shown in Figure 4.2.

The operating principle of the ideal boost converter in CCM mode can be explained as follows.

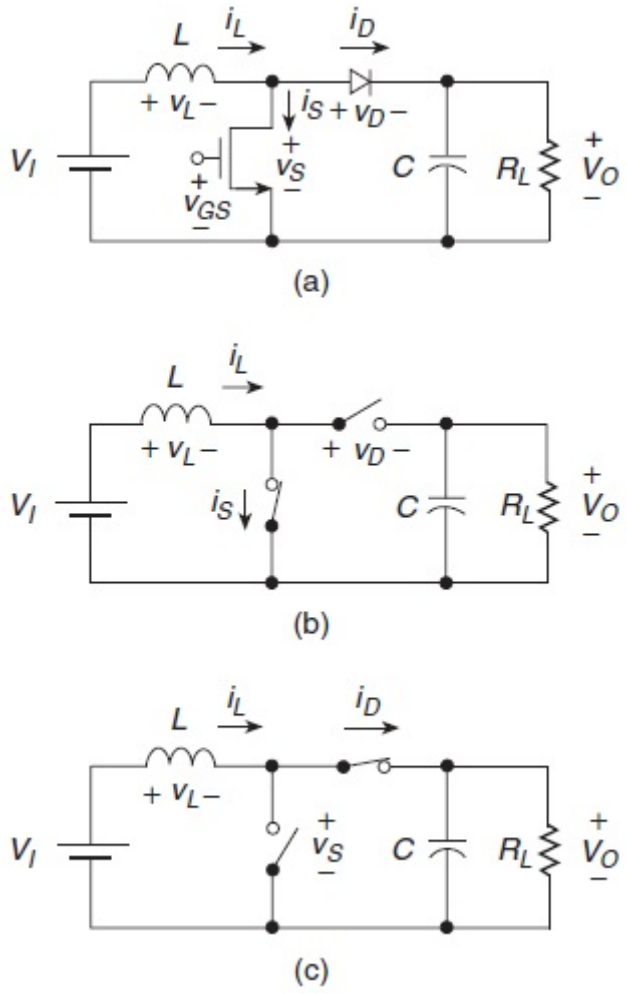

FIGURE 4.1: PWM boost converter and its ideal equivalent circuits for CCM. (a) Circuit (b) Equivalent circuit when the switch is ON and the diode is OFF. (c) Equivalent circuit when the switch is OFF and the diode is ON [30]

- In the time interval $0 < t \leq DT$, the MOSFET is ON. Therefore, the voltage across the diode is $v_D = V_O$, causing the diode to be reverse biased.
- Voltage across the inductor is $v_L = V_I$. Therefore, the inductor current linearly increases with a slope of V_I/L and $I_s = I_L$.
- At t = DT, MOSFET is turned off and the inductor acts as a current source and turns on the diode.
- Voltage across the inductor is $v_L = V_I - V_O < 0$. So, the inductor current decreases with a slope of $(V_I - V_O)/L$ and $I_D = I_L$.
- At the same time interval, the energy is transferred from the inductor (L) to the output capacitor (C) and the load resistance (R_L).
- At time $t = T$, the switch is turned on again and repeating the cycle again.

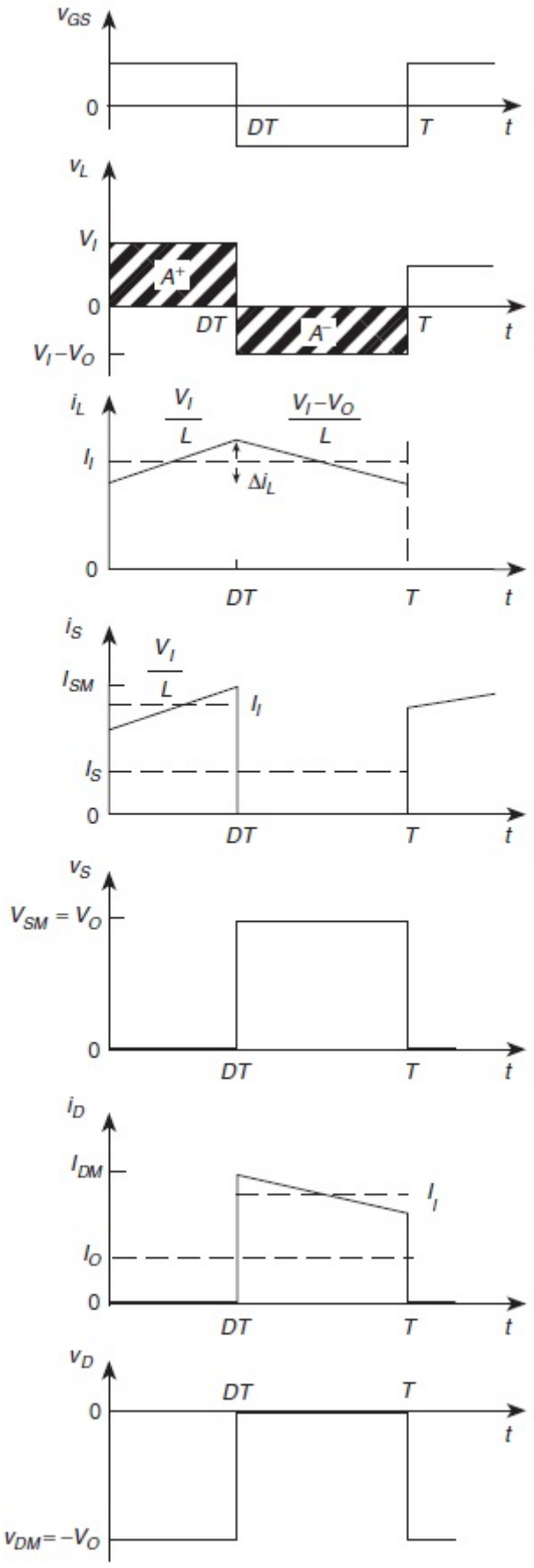

FIGURE 4.2: Idealized current and voltage waveforms in the PWM boost converter for CCM [30]

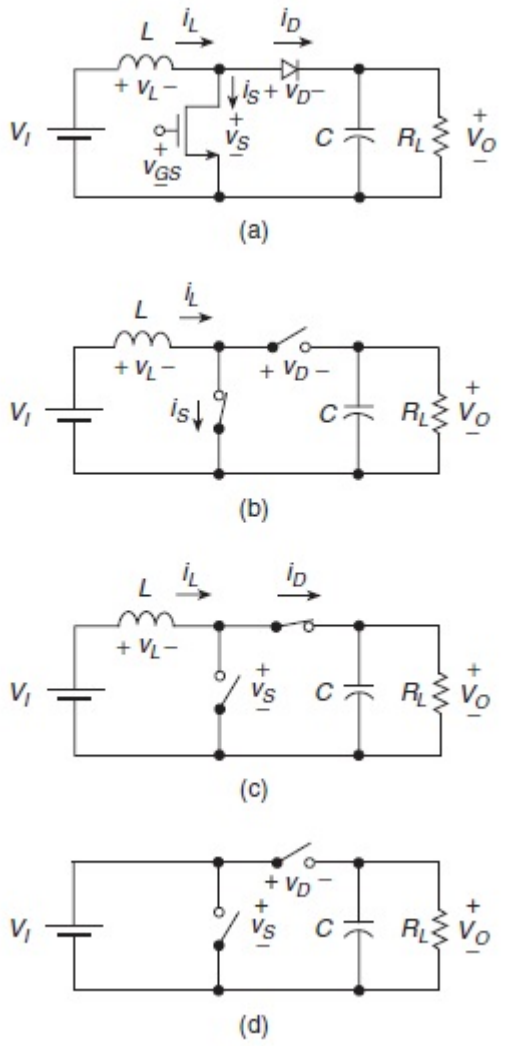

FIGURE 4.3: PWM boost converter and its ideal equivalent circuits for DCM. (a) Circuit (b) Equivalent circuit when the switch is ON and the diode is OFF (c) Equivalent circuit when the MOSFET is OFF and the diode is ON. (d) Equivalent circuit when both the MOSFET and the diode are OFF [30]

The PWM boost converter and its ideal equivalent circuits for DCM is shown in Figure 4.3. The idealized current and voltage waveforms in the PWM boost converter for DCM is shown in Figure 4.4. The operating principle of the ideal boost converter in DCM mode can be explained as follows:

- In the time interval $0 < t \leq DT$, MOSFET is ON and therefore the diode is OFF. The voltage across the inductor is $v_L = V_I$. As a result, the inductor current linearly increases with a slope of V_I/L and $I_s = I_L$.
- For the time interval $DT < t \leq (D + D1)T$,the MOSFET is turned off and the inductor acts as a current source and turns the diode on.

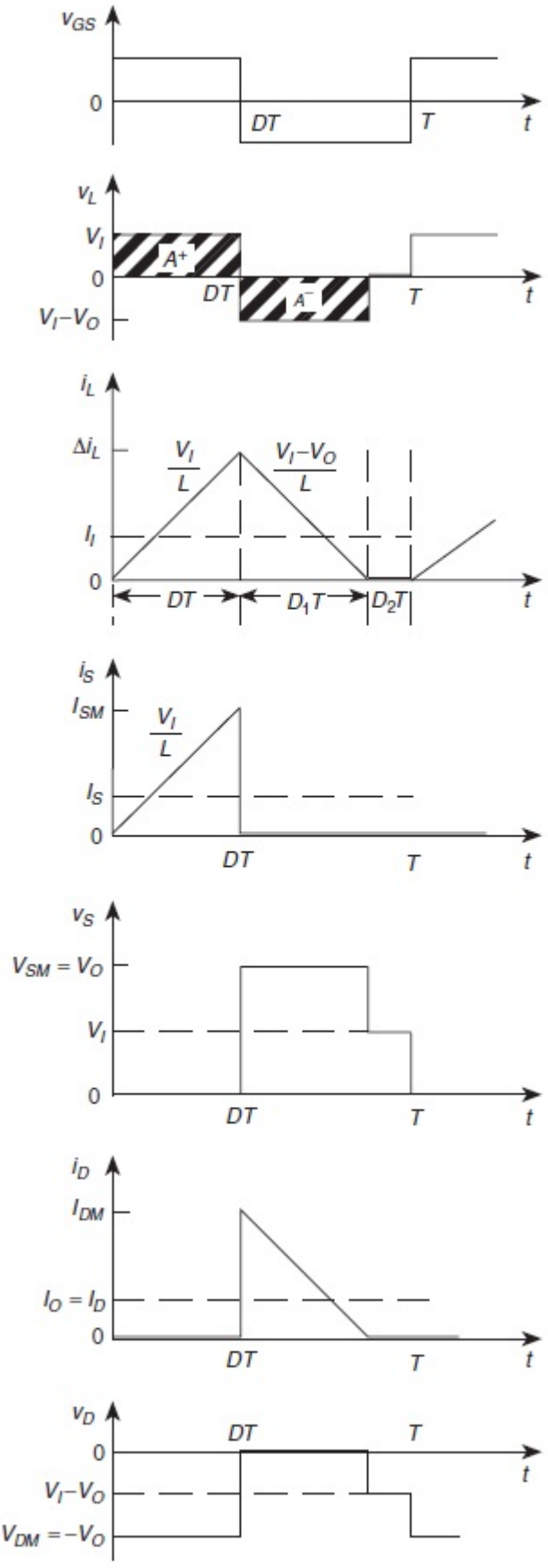

FIGURE 4.4: Idealized current and voltage waveforms in the PWM boost converter for DCM [30]

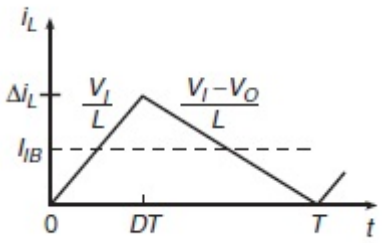

FIGURE 4.5: Waveform of the inductor current at the CCM/DCM boundary for the boost converter [30]

- At time $t = (D + D1)T$, the diode and inductor current reaches zero, turning the diode off.
- At the same time interval, energy is transferred from the inductor (L) to the output capacitor (C) and the load resistance (R_L).
- For the time interval $(D + D1)T < t \leq T$, both the MOSFET and the diode are OFF. Since the current through the inductor is constant (equal to zero), voltage across the inductor is zero.
- At time $t = T$, the switch is turned on again and the cycle repeats.

Detailed analysis of an ideal boost converter in DCM and CCM modes can be found in reference [30] and will not be discussed here. Derivation of an expression to identify the boundary between DCM and CCM mode is important. Figure 4.5 shows the waveform of the inductor current at the CCM/DCM boundary of the boost converter.

DC transfer function of lossless converter in CCM is given by Equation 4.1.

$$M_{VDC} = \frac{V_{out}}{V_{in}} = \frac{I_{in}}{I_{out}} = \frac{1}{(1-D)} \tag{4.1}$$

According to Figure 4.5, Δi_L can be written as follows,

$$\Delta i_L = \frac{V_{in}DT}{L} = \frac{V_{out}D}{f_{sw}LM_{VDC}} = \frac{V_{out}D(1-D)}{f_{sw}L} \tag{4.2}$$

For a very good approximation, the Δi_L can be rewritten as follows;

$$\Delta i_L = \frac{V_{in}}{r_{on} + r_L}(1 - \exp(\frac{-(r_{on} + r_L)D}{Lf_{sw}})) \tag{4.3}$$

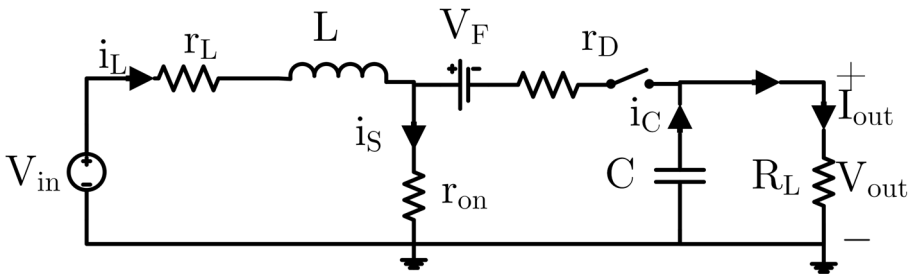

FIGURE 4.6: Equivalent circuit of the boost converter with parasitic resistances

The DC input current at the DCM/CCM boundary is given by

$$\Delta I_{in} = \frac{\Delta i_L}{2} = \frac{V_{out} D(1-D)}{2 f_{sw} L} \tag{4.4}$$

The DC output current at the DCM/CCM boundary is given by

$$I_{out} = I_{in}(1-D) = \frac{V_{out} D(1-D)^2}{2 f_{sw} L} \tag{4.5}$$

The inequality relationships of the boost converter output current at the DCM/CCM boundary condition are given by Equation 4.6 and Equation 4.7. The boost converter is working in DCM mode if Equation 4.6 satisfied. Otherwise, it works in CCM mode. In CCM mode, inequality is given by Equation 4.7.

$$\frac{I_{out}(2 f_{sw} L)}{V_{out}} < D(1-D)^2 \tag{4.6}$$

$$\frac{I_{out}(2 f_{sw} L)}{V_{out}} > D(1-D)^2 \tag{4.7}$$

4.1.2 Power loss analysis of boost converter in CCM mode

The equivalent circuit of the boost converter with parasitic resistances is shown in Figure 4.6, where r_{on} is the MOSFET on-resistance, r_D is the diode forward resistance, V_F is the diode threshold voltage, and r_L is the ESR of the inductor (L). Here, ESR of the output capacitor (C) is neglected.

Conduction losses will be evaluated assuming that the inductor current i_L is ripple-free and equal to the DC input current I_{in}. Hence, the switch current can be approximated by Equation 4.8 [30].

$$i_S = \begin{cases} I_{in} = \frac{I_{out}}{(1-D)} & \text{for} \quad 0 < t \leq DT \\ 0 & \text{for} \quad DT < t \leq T \end{cases} \tag{4.8}$$

The resulting RMS of value of I_S is given by

$$I_{Srms} = \sqrt{\frac{1}{T}\int_0^T i_S^2 dt} = \frac{I_{out}}{(1-D)}\sqrt{\frac{1}{T}\int_0^{DT} dt} = \frac{I_{out}\sqrt{D}}{(1-D)} \tag{4.9}$$

MOSFET conduction loss is then given in Equation 4.10.

$$P_{MOSFET} = r_{on} I_{Srms}^2 = \frac{D r_{on} I_{out}^2}{(1-D)^2} \tag{4.10}$$

If synchronous rectification considered, a second MOSFET is used instead of a diode. Therefore, MOSFET conduction loss of the second switch is given in Equation 4.11.

$$P_{MOSFET} = r_{on2} I_{Srms2}^2 = \frac{r_{on2} I_{out}^2}{(1-D)} \tag{4.11}$$

$$i_D = I_{S2} = \begin{cases} 0 & \text{for} \quad 0 < t \leq DT \\ I_{in} = \frac{I_{out}}{(1-D)} & \text{for} \quad DT < t \leq T \end{cases} \tag{4.12}$$

If asynchronous rectification is considered, diode losses should be evaluated instead of MOSFET loss and they are given in Equation 4.13 and Equation 4.14.

$$P_{Dioderd} = r_D I_{Drms}^2 = \frac{r_D I_{out}^2}{(1-D)} \tag{4.13}$$

$$P_{DiodeVF} = V_F I_D = V_F I_{out} \tag{4.14}$$

The average value of the diode current is given by

$$I_D = \frac{1}{T}\int_0^T i_D dt = \frac{I_{out}}{T(1-D)}\int_{DT}^T dt = I_{out} \tag{4.15}$$

The power losses due to the series resistance of the inductor is given by

$$P_{R_L} = r_L I_{Lrms2}^2 = \frac{r_L I_{out}^2}{(1-D)^2} \tag{4.16}$$

The losses due to the parasitic capacitance of drain and the gate capacitance of the switches are given by P_{switch} and P_{gate}. C_{ds} is the drain switch capacitance and W_{sw} is the width of the MOSFET.

$$P_{switch} = f_{sw}(C_{ds}W_{sw})V_{DS}^2 \tag{4.17}$$

$$P_{gate} = (W_{sw}C_{gate}f_{sw})V_{sw}^2 \tag{4.18}$$

Here V_{sw} is the gate swing voltage and it is equal to the output voltage of the converter in most cases.

4.1.3 Power loss analysis of boost converter in DCM mode

The resulting RMS value of I_S is given in Equation 4.19 and can be simplified using Equation 4.2.

$$I_{Srms} = \sqrt{\frac{1}{T}\int_0^{DT} i_S^2 dt} = \Delta i_L \sqrt{\frac{D}{3}} \tag{4.19}$$

Similarly, the RMS value of the diode current or current through the second switch is given by Equation 4.20, where D1 is given in Equation 4.21.

$$I_{Srms2} = I_{Drms} = \sqrt{\frac{1}{T}\int_{DT}^{(D+D1)T} i_D^2 dt} = \Delta i_L \sqrt{\frac{D1}{3}} \tag{4.20}$$

$$D1 = \frac{DV_{in}}{(V_{out} - V_{in} + V_F)} \tag{4.21}$$

The RMS value of the inductor current in DCM mode is given by

$$I_L = \sqrt{\frac{1}{T}\int_0^{(D+D1)T} i_L^2 dt} = \Delta i_L \sqrt{\frac{D+D1}{3}} \tag{4.22}$$

The MOSFET conduction loss is given by

$$P_{MOSFET} = r_{on} I_{Srms}^2 \tag{4.23}$$

If asynchronous rectification is considered, diode losses should be considered instead of MOSFET loss and they are given by Equation 4.24 and Equation 4.25.

$$P_{Dioderd} = r_D I_{Drms}^2 \tag{4.24}$$

$$P_{DiodeVF} = V_F I_D = V_F I_{out} \tag{4.25}$$

The losses due to the parasitic capacitance of drain and the gate capacitance of the switches are given by Equation 4.17 and Equation 4.18.

4.1.4 Proposed Simulink model for boost converter

One of the biggest limitations of existing efficiency models [9],[30] of boost converters is that we have to specify V_{out}, I_{out} and V_{in}. The models assume that, boost converter or buck converters can generate the given voltage conversion ratio and produce faulty efficiency values. The proposed approach avoids those limitations and is able to generate accurate output voltage for a given specification.

The differential equations that describe the capacitor voltage and inductor current are solved according to the boundary conditions of the switching periods. Values of current and voltages at the end of a period become initial conditions for the next switching period. This way, the model can predict the output voltage and load current it can supply based on input voltage. The proposed method assumes that the harvester can supply the required input power to the converter without any limitation.

The proposed method can be applied to both synchronous and asynchronous rectification methods. To validate the model, the asynchronous rectification method is used to avoid designing all of the control circuit. This model is the extended version of the model proposed by Batard et al. [13]. Figure 4.7 shows the states of the boost converter. Equations can be written for each state to describe the function of the state, it is shown in Equation 4.26.

$$states = \begin{cases} V_L = V_{in} - i_L(r_{on} + r_L) = L\frac{di}{dt}, i_C = I_{out} & \text{for} \quad F = 1 \\ V_L = V_{in} - V_{out} - V_F - i_L(r_D + r_L) = L\frac{di}{dt} & \text{for} \quad F = 0 \\ V_L = 0, i_C = -I_{out} & \text{for} \quad F = 0 \end{cases} \tag{4.26}$$

Equation 4.27 and Equation 4.28 can be derived by combining all three equations with state F to build the MATLAB Simulink model.

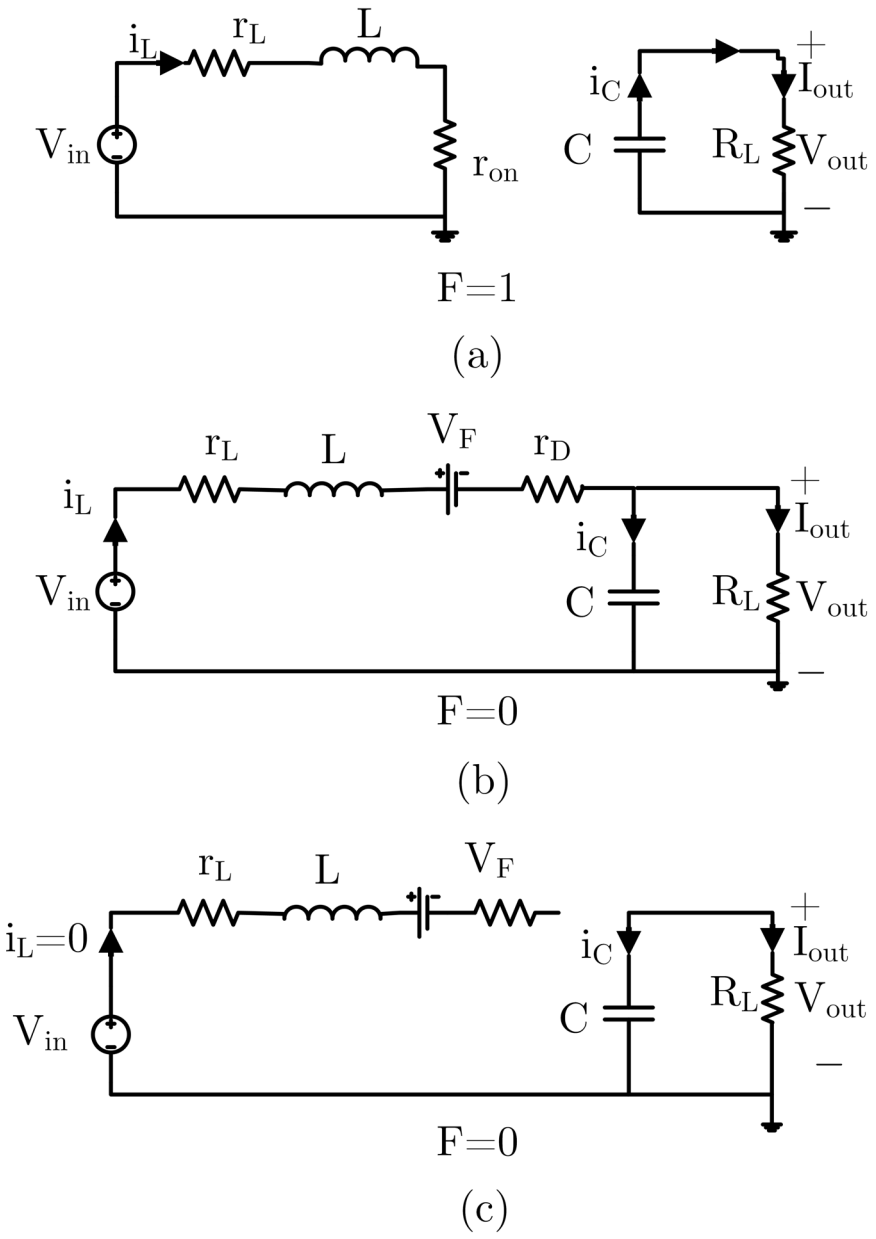

FIGURE 4.7: States of the boost converter with freewheeling diode. (a) MOSFET is on (b) MOSFET is off and diode is on (c) MOSFET is off and diode is off

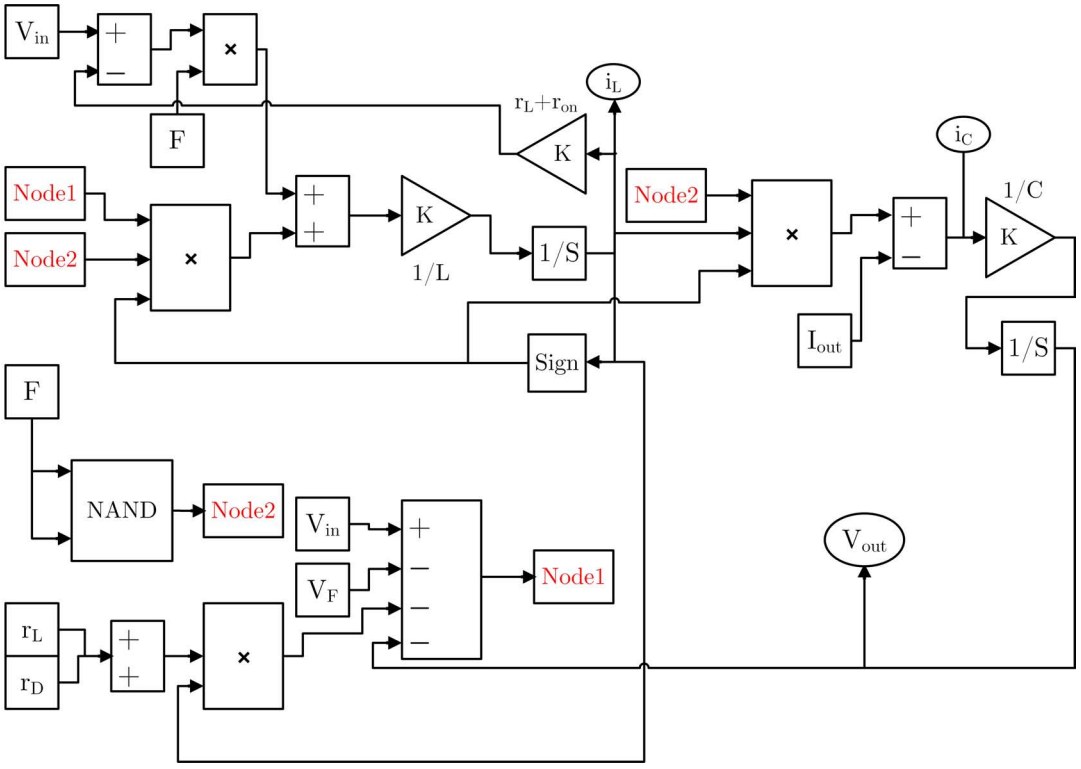

FIGURE 4.8: MATLAB Simulink model of the boost converter with freewheeling diode

$$[V_{in}(t)-i_L(t)(r_L+r_{on})]\times F+[V_{in}(t)-V_{out}(t)-V_F-I_L(t)(r_L+r_D)\times sign(i_L(t))]\times\overline{F}=L\frac{di}{dt} \tag{4.27}$$

$$i_C(t)=-I_{out}(t)\times F+\overline{F}\times I_L(t)=C\frac{dV_{out}}{dt} \tag{4.28}$$

The above two equations can be solved using Simulink. $Sign(I_L) = 1$ when I_L is positive and $Sign(I_L) = 0$ when I_L is negative. The open loop system can be generated in Simulink to calculate the V_{out} of the boost converter for a given V_{in} and it is shown in Figure 4.8.

The complete novel boost converter open loop model is shown in Figure 4.9.

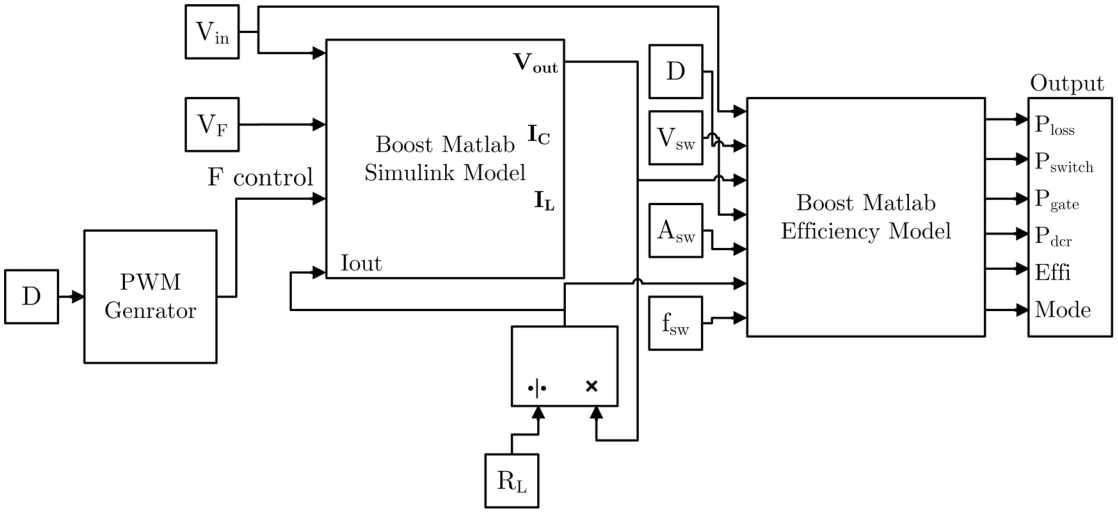

FIGURE 4.9: Complete boost converter open loop model

4.2 Inductive-based buck DC-DC converter

4.2.1 Introduction

A buck converter is a DC-DC converter, which steps down voltage (while stepping up current) from its input (supply) to its output (load). A traditional buck converter consists of an inductor, a diode and a transistor. It is shown in Figure 4.10. Here, ideal diode is used for simplicity.

The idealized wave form of the PWM buck converter for CCM is shown in Figure 4.11. The operating principle of an ideal buck converter in CCM mode can be explained as follows.

- In the time interval $0 < t \leq DT$, the MOSFET is ON. Therefore, the voltage across the diode is $v_D = V_I$, causing the diode to be reverse biased.
- The voltage across the inductor is $v_L = V_I - V_O$. As a result, the inductor current linearly increases with a slope of $(V_I - V_O)/L$ and $I_s = I_L$.
- In the time interval $DT < t \leq T$, the MOSFET is turned off and the inductor acts as a current source and turns the diode on.
- The voltage across the inductor is $v_L = -V_O$. Therefore, the inductor current decreases with a slope of $-V_O/L$ and $I_D = I_L$.
- During the same time interval, energy is transferred from the inductor L to the output capacitor C and the load resistance R_L.

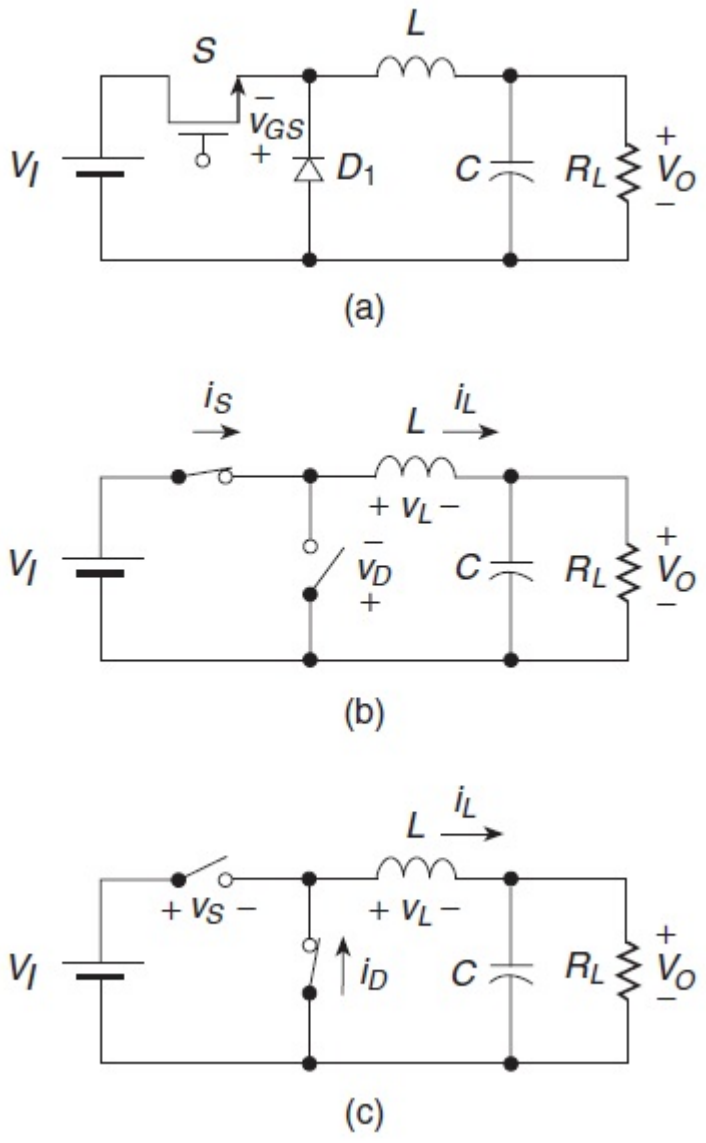

FIGURE 4.10: PWM buck converter and its ideal equivalent circuits for CCM. (a) Circuit. (b) Equivalent circuit when the MOSFET is ON and the diode is OFF. (c) Equivalent circuit when the MOSFET is OFF and the diode is ON [30]

- At time $t = T$, the MOSFET is turned on again and the cycle repeats.

The PWM buck converter and its ideal equivalent circuits for DCM are shown in Figure 4.12. The idealized current and voltage waveforms in the PWM buck converter for DCM is shown in Figure 4.13. The operating principle of an ideal buck converter in DCM mode can be explained as follows.

- In the time interval $0 < t \leq DT$, the MOSFET is ON and therefore the diode is OFF. The voltage across the inductor is $v_L = V_I - V_O$. As a result, the inductor current linearly increases with a slope of $(V_I - V_O)/L$ and $I_s = I_L$.

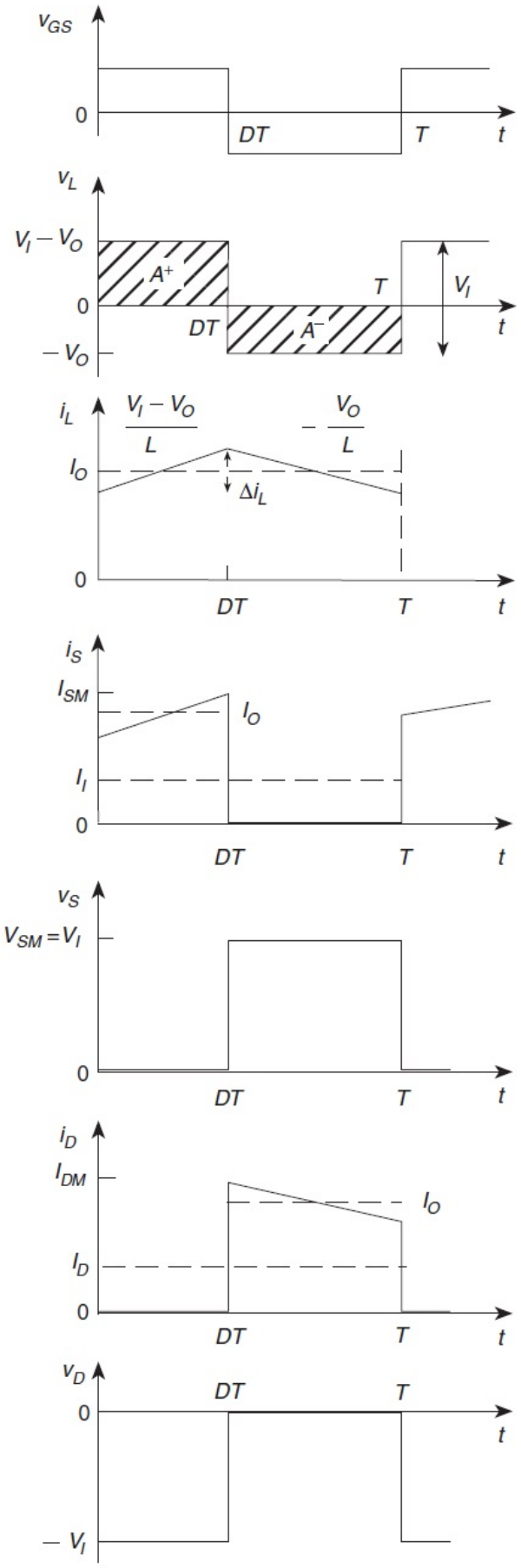

FIGURE 4.11: Idealized current and voltage waveforms in the PWM buck converter for CCM [30]

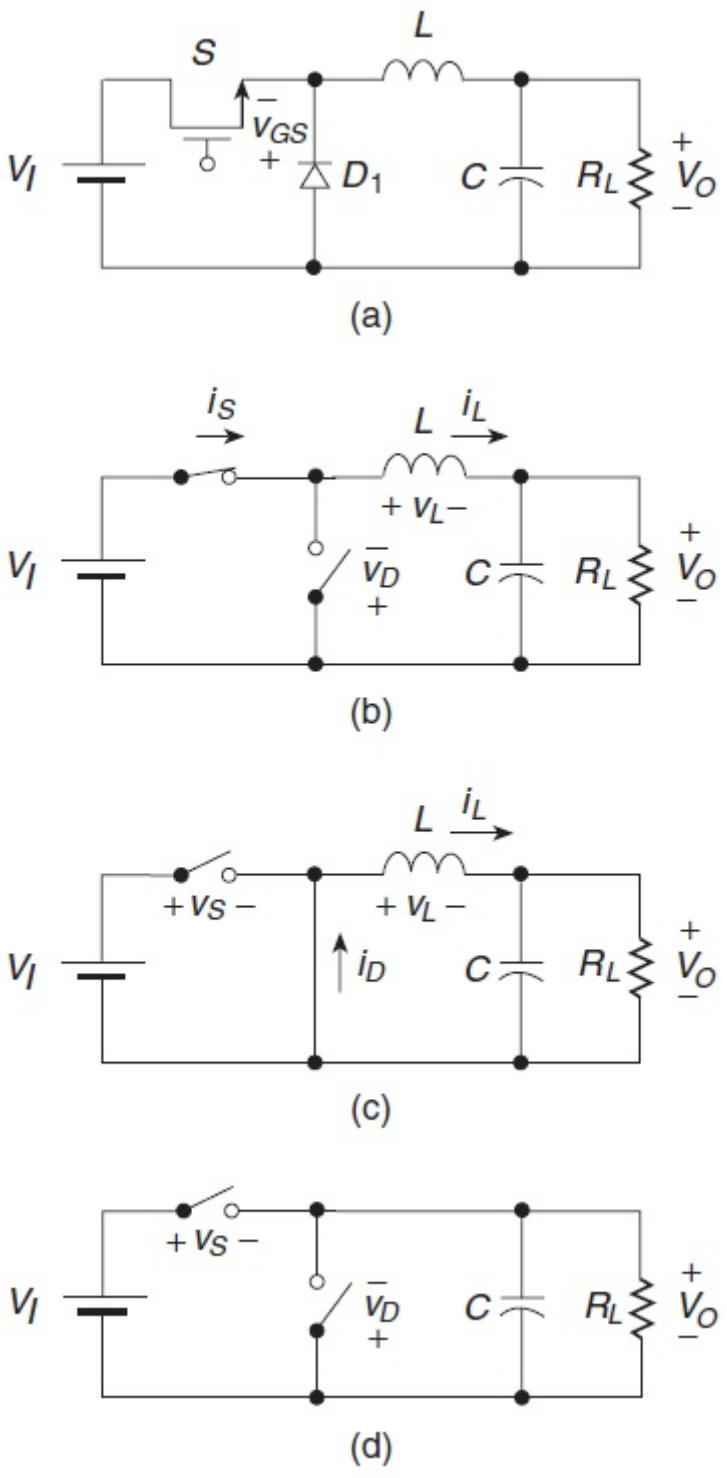

FIGURE 4.12: PWM buck converter and its ideal equivalent circuits for DCM. (a) Circuit (b) Equivalent circuit when the MOSFET is ON and the diode is OFF (c) Equivalent circuit when the MOSFET is OFF and the diode is ON. (d) Equivalent circuit when both the MOSFET and the diode are OFF [30]

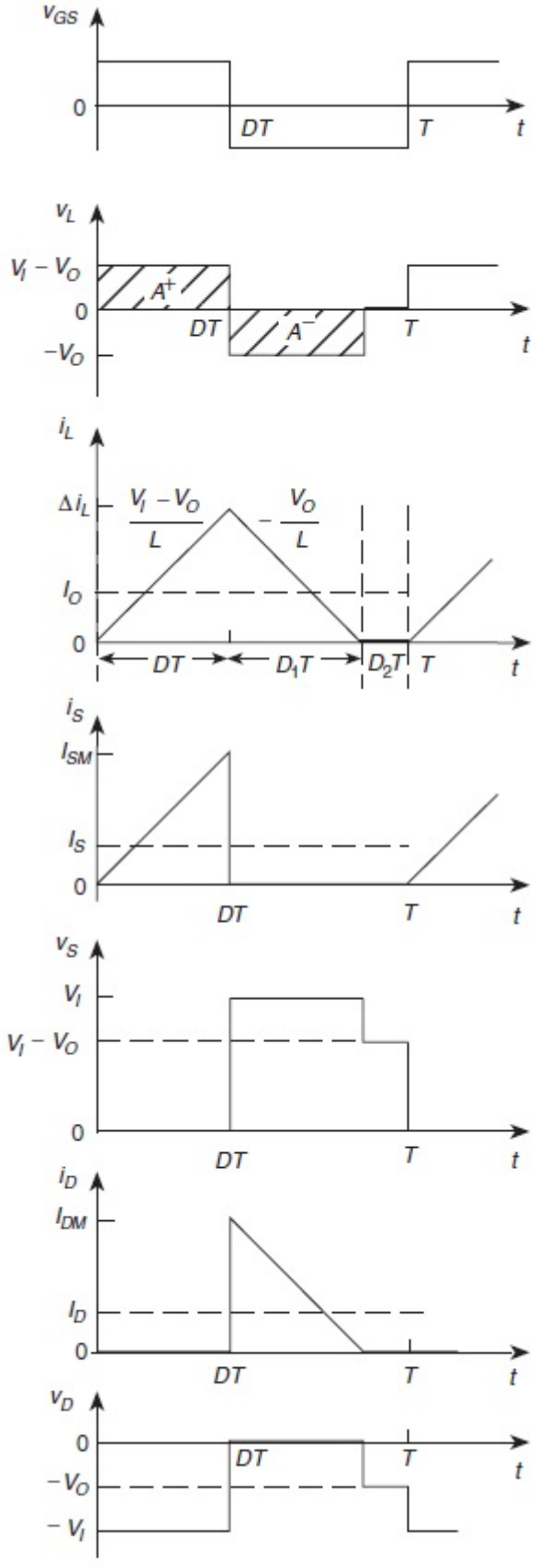

FIGURE 4.13: Idealized current and voltage waveforms in the PWM buck converter for DCM [30]

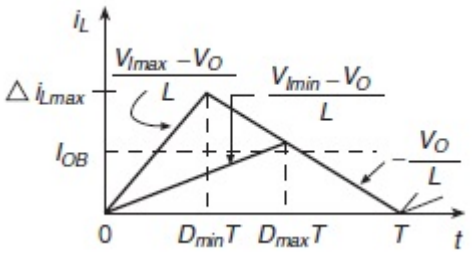

FIGURE 4.14: Waveform of the inductor current at the CCM/DCM boundary for the buck converter [30]

- For the time interval $DT < t \leq (D + D1)T$ the MOSFET is turned off and the inductor acts as a current source and turns the diode on.
- At time $t = (D + D1)T$, the inductor and diode current reaches zero, turning the diode off.
- At the same time interval, energy is transferred from the inductor L to the output capacitor C and the load resistance R_L.
- For the time interval $(D + D1)T < t \leq T$, both the MOSFET and the diode are OFF. Since the current through the inductor is constant (equal to zero), the voltage across the inductor is zero.
- At time $t = T$, the MOSFET is turned on again and the cycle repeats.

The detailed analysis of the ideal buck converter in DCM and CCM modes can be found in [30] and will not be discussed here. The derivation of expressions to identify the boundary between DCM and CCM modes of a converter is important. Waveforms of the inductor current at the CCM/DCM boundary at V_{Imin} and V_{Imax} are shown in Figure 4.14 [30].

The DC transfer function of lossless converter in CCM is given by [30],

$$M_{VDC} = \frac{V_{out}}{V_{in}} = \frac{I_{in}}{I_{out}} = D \tag{4.29}$$

The DC transfer function of a lossless converter in DCM is given by [30],

$$M_{VDC} = \frac{V_{out}}{V_{in}} = \frac{D}{(D + D1)} \tag{4.30}$$

According to Figure 4.14 and 4.29, Δi_L for CCM can be written as follows,

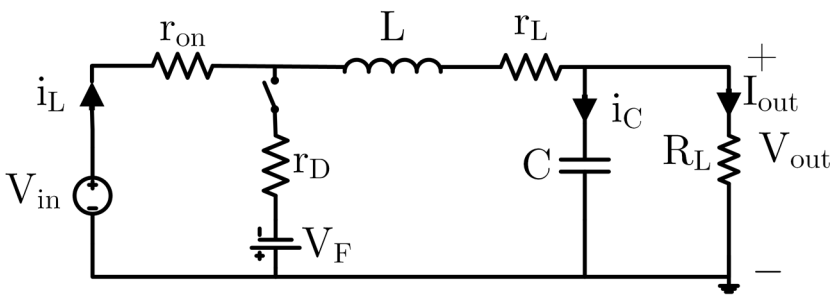

FIGURE 4.15: Equivalent circuit of the buck converter with parasitic resistances

$$\Delta i_L = i_L DT = \frac{(V_{in} - V_{out})DT}{L} = \frac{V_{out}(1-D)}{Lf_{sw}} \tag{4.31}$$

According to the Figure 4.13 and 4.30, Δi_L for DCM can be written as follows:

$$\Delta i_L = i_L DT = \frac{(V_{in} - V_{out})DT}{L} \tag{4.32}$$

The DC output current at the DCM/CCM boundary is given by

$$I_{out} = \frac{\Delta i_L}{2} = \frac{V_{out}(1-D)}{2Lf_{sw}} \tag{4.33}$$

The inequality relationship of the boost converter output current at the DCM/CCM boundry condition is given by Equation 4.34 and 4.35. The boost converter is working in DCM mode if 4.34 satisfied. Otherwise, it works in CCM mode. For CCM mode, inequality is given by 4.35.

$$\frac{I_{out}(2f_{sw}L)}{V_{out}} < (1-D) \tag{4.34}$$

$$\frac{I_{out}(2f_{sw}L)}{V_{out}} > (1-D) \tag{4.35}$$

4.2.2 Power loss analysis of buck converter in CCM mode

An equivalent circuit of a buck converter with parasitic resistances is shown in Figure 4.15, where r_{on} is the MOSFET on-resistance, r_D is the diode forward resistance, V_F is the diode threshold voltage, r_L is the ESR of the inductor (L). Here, the ESR of the output capacitor (C) is neglected.

The conduction losses will be evaluated assuming that the inductor current i_L is ripple-free and equals the DC output current I_{out}. Hence, the switch current can be approximated by [30].

$$i_S = \begin{cases} I_{out} & \text{for} \quad 0 < t \leq DT \\ 0 & \text{for} \quad DT < t \leq T \end{cases} \tag{4.36}$$

The resulting RMS of value of I_S is given by

$$I_{Srms} = \sqrt{\frac{1}{T}\int_0^T i_S^2 dt} = \sqrt{\frac{1}{T}\int_0^T i_{out}^2 dt} = I_{out}\sqrt{D} \tag{4.37}$$

MOSFET conduction loss is then given in Equation 4.38.

$$P_{MOSFET} = r_{on} I_{Srms}^2 = r_{on} D I_{out}^2 \tag{4.38}$$

If synchronous rectification is considered, a second MOSFET is used instead of a diode. Therefore, the MOSFET conduction loss of the second switch is given in Equation 4.39.

$$P_{MOSFET} = r_{on2} I_{Srms2}^2 = r_{on2} I_{out}^2 (1 - D) \tag{4.39}$$

This equation can be derived since the current through the 2^{nd} MOSFET can be approximated as in Equation 4.40.

$$i_D = I_{S2} = \begin{cases} 0 & \text{for} \quad 0 < t \leq DT \\ I_{out} & \text{for} \quad DT < t \leq T \end{cases} \tag{4.40}$$

If asynchronous rectification is considered, diode losses should be evaluated instead of MOSFET loss, and they are given in Equation 4.41 and Equation 4.42.

$$P_{Diode} = r_D I_{Drms}^2 = r_{on2} I_{out}^2 (1 - D) \tag{4.41}$$

$$P_{DiodeVF} = V_F I_D = V_F I_{out} (1 - D) \tag{4.42}$$

The average value of the diode current is given by

$$I_D = \frac{1}{T}\int_{DT}^{T} i_D dt = \frac{1}{T}\int_{DT}^{T} i_{out} dt = (1-D)I_{out} \tag{4.43}$$

Current through the inuductor (I_L) can be approximated as I_{out}. The power losses due to the series resistance of the inductor is given by

$$P_{R_L} = r_L I_{Lrms2}^2 = r_L I_{out}^2 \tag{4.44}$$

The losses due to the parasitic capacitance of drain and the gate capacitance of the switches are given by P_{switch} and P_{gate}. C_{ds} is the drain switch capacitance and W_{sw} is the width of the MOSFET.

$$P_{switch} = f_{sw}(C_{ds}W_{sw})V_{DS}^2 \tag{4.45}$$

$$P_{gate} = (W_{sw}C_{gate}f_{sw})V_{sw}^2 \tag{4.46}$$

Here V_{sw} is the gate swing voltage.

4.2.3 Power loss analysis of buck converter in DCM mode

The resulting RMS value of I_S is given in Equation 4.47 and can be simplified using Equation 4.2.

$$I_{Srms} = \sqrt{\frac{1}{T}\int_{0}^{DT} i_S^2 dt} = \Delta i_L \sqrt{\frac{D}{3}} \tag{4.47}$$

Similarly, RMS value of the diode current or the current through the second switch is given by Equation 4.48 where D1 is given in Equation 4.49. The ideal conversion ratio of the buck converter (M_{VDC}) is given in Equation 4.30.

$$I_{Srms2} = I_{Drms} = \sqrt{\frac{1}{T}\int_{DT}^{(D+D1)T} i_D^2 dt} = \Delta i_L \sqrt{\frac{D1}{3}} \tag{4.48}$$

$$D1 = \frac{D(1-M_{VDC})}{M_{VDC}} \tag{4.49}$$

The RMS value of the inductor current in DCM mode is given by

$$I_L = \sqrt{\frac{1}{T}\int_0^{(D+D1)T} i_L^2 dt} = \Delta i_L \sqrt{\frac{D+D1}{3}} \tag{4.50}$$

The MOSFET conduction loss is given by

$$P_{MOSFET} = r_{on} I_{Srms}^2 \tag{4.51}$$

If asynchronous rectification is considered, diode losses are given by Equation 4.52 and Equation 4.54.

$$P_{Dioderd} = r_D I_{Drms}^2 \tag{4.52}$$

The average value of the diode current is given in Equation 4.53, where M_{VDC} is given in Equation 4.30.

$$I_D = \frac{1}{T}\int_0^T i_D dt = (1 - M_{VDC}) I_{out} \tag{4.53}$$

$$P_{DiodeVF} = V_F I_D = V_F I_{out} \tag{4.54}$$

The losses due to the parasitic capacitance of drain and the gate capacitance of the switches can be calculated using Equation 4.45 and Equation 4.46.

4.2.4 Proposed Simulink model for buck converter

The proposed buck converter model is designed to generate V_{out} by considering the parasitic resistances of each components. This model is the extended version of the model proposed by [13]. Figure 4.16 shows the states of the buck converter. The equations can be written for each state to describe the function of every state and it is shown in Equation 4.55.

$$states = \begin{cases} \frac{dI_L}{dt} = \frac{1}{L}(V_{in} - V_{out} - I_L(r_{on} + r_L)), i_L = i_C + i_{out} & \text{for} \quad F = 1 \\ \frac{dI_L}{dt} = \frac{1}{L}(-V_F - V_{out} - I_L(r_D + r_L)) \times sign(i_L), i_L = i_C + i_{out} & \text{for} \quad F = 0 \\ V_L = 0, i_C = -I_{out} & \text{for} \quad F = 0 \end{cases} \tag{4.55}$$

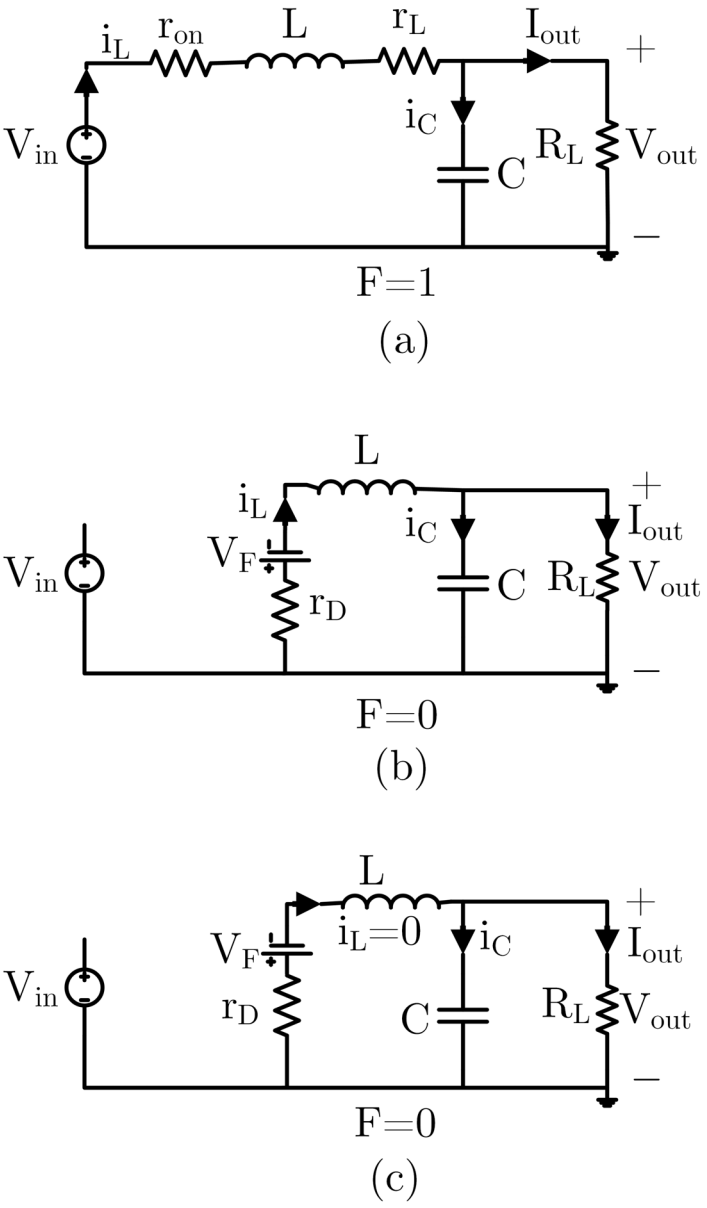

FIGURE 4.16: States of the buck converter with freewheeling diode (a) MOSFET is ON (b) MOSFET is OFF and diode is ON (c) MOSFET is OFF and diode is OFF

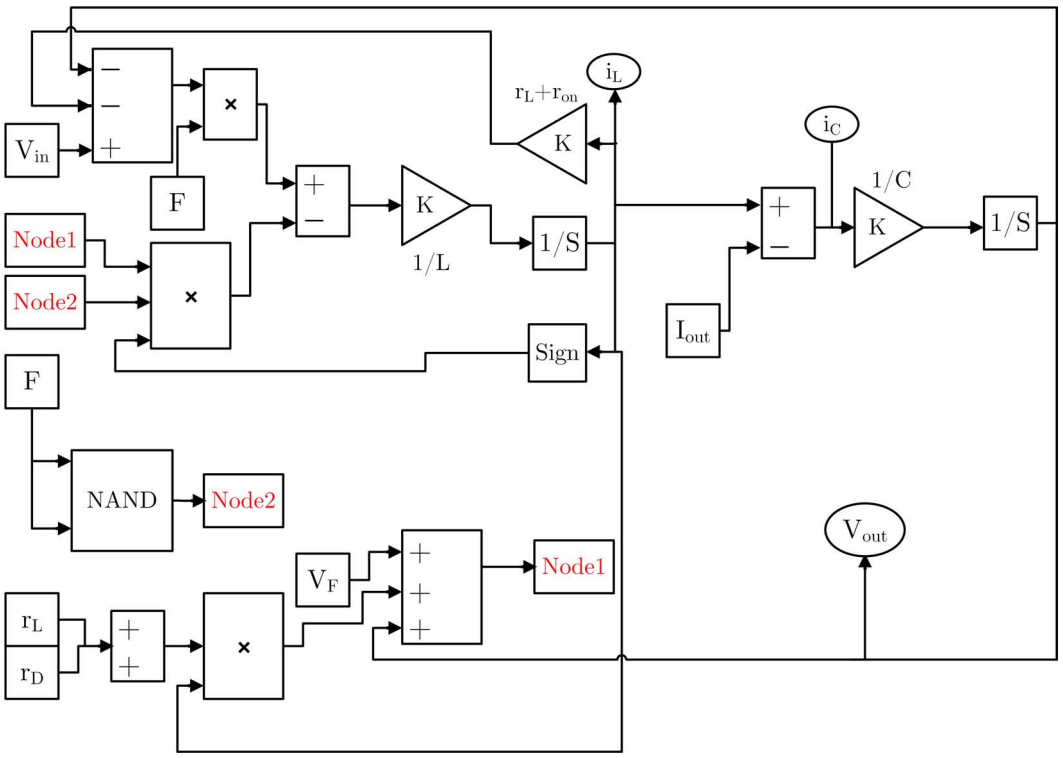

FIGURE 4.17: MATLAB Simulink model of the buck converter with freewheeling diode

By combining all three equations with state F, the following two Equations 4.56 and 4.57 can be derived to build the MATLAB Simulink model.

$$[V_{in}(t)-V_{out}(t)-I_L(t)(r_{on}+r_L)]\times F+[-V_F-V_{out}(t)-I_L(t)(r_D+r_L)\times sign(i_L(t))]\times\overline{F}=L\frac{di}{dt} \tag{4.56}$$

$$V_{out}(t)=\frac{1}{C}\int(I_L(t)-I_{out}(t))dt \tag{4.57}$$

The MATLAB model for the buck converter to obtain V_{out} is shown in Figure 4.17.

The complete novel buck converter open loop model is shown in Figure 4.9.

The models were verified for both boost and buck converters in SPICE using CMOS 130 nm technology. The verification results are listed in the next chapter.

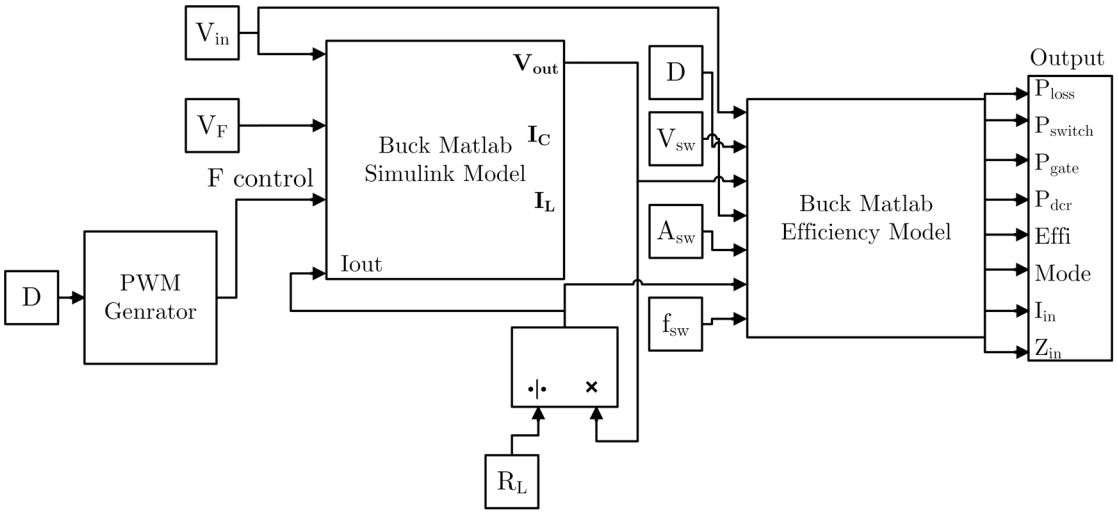

FIGURE 4.18: Complete buck converter open loop model

Chapter 5

Experiment analysis of the Models

5.1 Introduction

The validation results of the proposed model with SPICE simulation are explained in this chapter. Several experiments were designed to show the usage of the models in low power energy harvesting system designs. The proposed models were verified in SPICE using CMOS 130 nm technology and were used to get a rough estimate of efficiency values and other parameters like transistor width, fly capacitance size, operating frequency, etc.

5.2 Individual model validation

The proposed model of the linear dropout regulator (LDO) is verified using SPICE simulation. The efficiency vs Load current profile along with the model prediction error is shown in Figure 5.1. The PMOS width is set to $10\,\mu m$, $V_{in} = 1.5\,V$ and $V_{out} = 1\,V$ during the simulation.

The efficiency vs $\Delta\,(V_{out} - V_{in})$ current profile along with model prediction error is shown in 5.2.

The model can predict the LDO efficiency with less than 9 % error. Efficiency was varied as expected under ultra-low current values since the control circuit current is significant compared to that of the load current value. The predicted efficiency at higher load current ($>$ 1 mA) deviated from the simulation results with more than 10 % error. This is because the width of the PMOS is fixed during SPICE simulation. The proposed

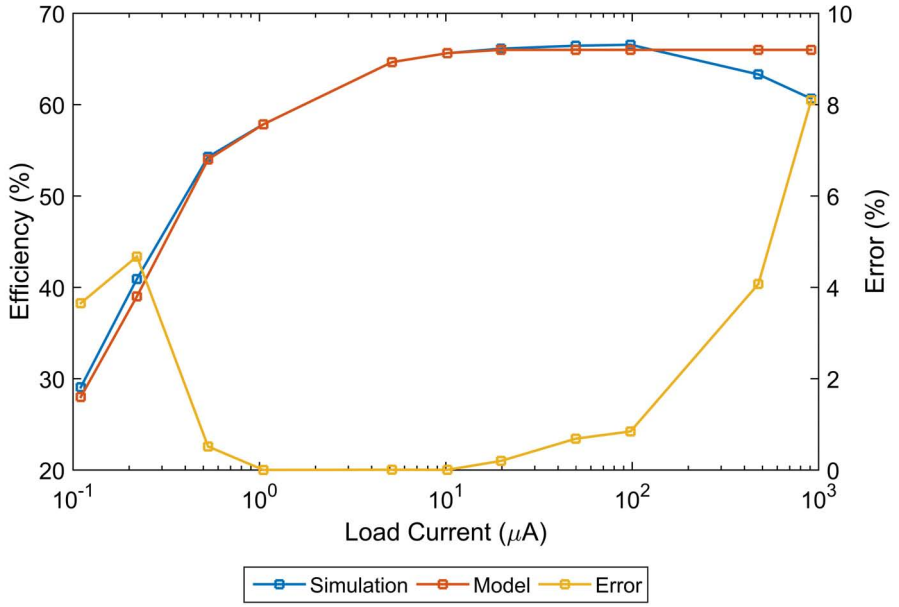

FIGURE 5.1: Efficiency vs Load current profile along with model prediction error for LDO

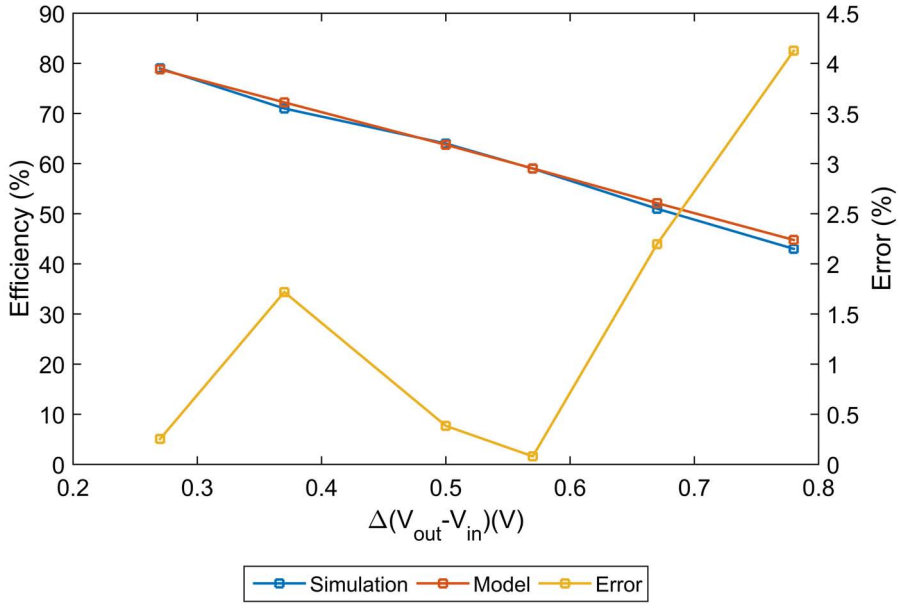

FIGURE 5.2: Efficiency vs $\Delta\left(V_{out}-V_{in}\right)$ current profile along with model prediction error for LDO

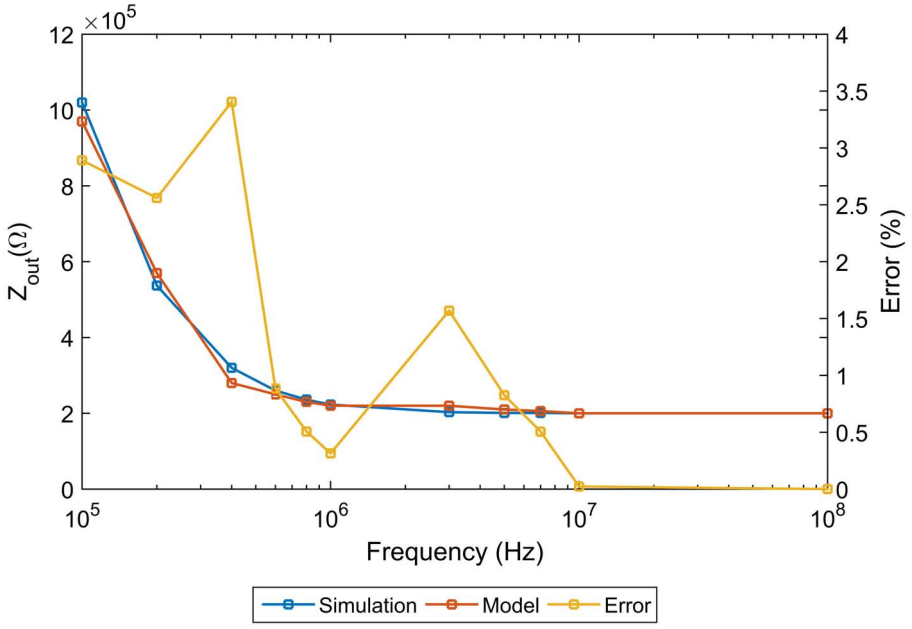

FIGURE 5.3: Output impedance vs Frequency with the prediction error for Dickson three stage charge pump topology

model assumes that the user can maintain the predicted R_{on} value by changing the width of the PMOS in SPICE simulation. To maintain a given V_{out} value for a higher load current, user needs to change the width of the PMOS to a predicted value. Therefore, if a fixed width is used during the SPICE simulation, the simulated efficiency will be less than that of the predicted value for higher load current ($>$ 1 mA) as it could not maintain V_{out} at a constant value.

To validate the switch capacitor based DC-DC converter, a Dickson charge pump is chosen with three stages. A diode connected NMOS with $10\,\mu m$ width with a length of $1\,\mu m$ is chosen in order to reduce secondary effects. A detailed description of the topology is given in Chapter 2. The output Capacitor is 2 nF and the fly capacitor is 10 pF, chosen such that $C_{out} >>> C_{fly}$. Output impedance (Z_{out}) calculation and output voltage (V_{out}) prediction are major goals in the proposed model. Therefore, it is important to compare the model prediction results with the simulation results. During the simulation, $V_{in} = 0.5\,V$ and $I_{load} = 1\,\mu A$ are kept constant. Figure 5.3 shows the output impedance vs. frequency with the prediction error for Dickson three stage charge pump topology.

Figure 5.4 shows the predicted V_{out} vs frequency with prediction error, with the same input voltage and output current values.

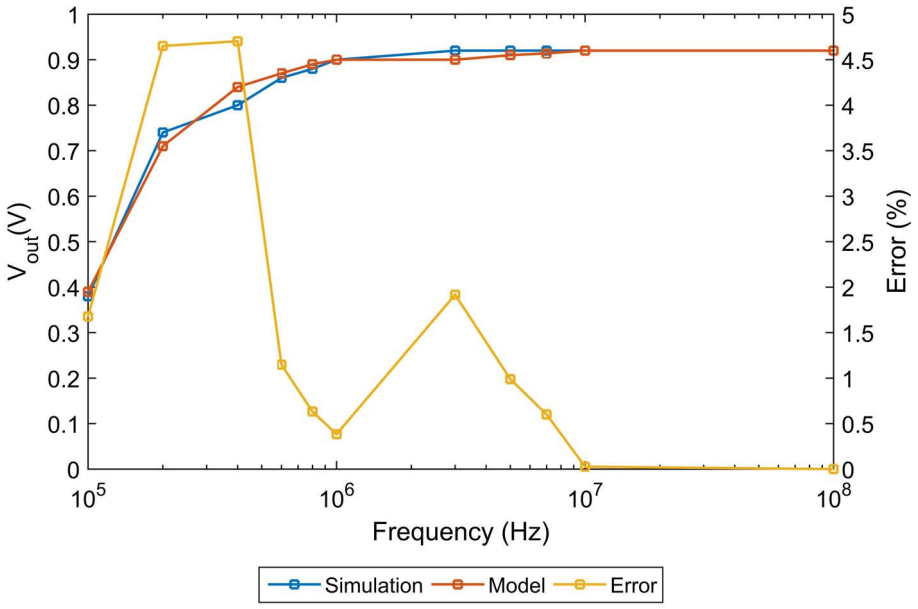

FIGURE 5.4: The predicted V_{out} vs frequency with prediction error for Dickson three stage charge pump topology

The efficiency prediction capability is verified for three stage Dickson charge pump topology with a fixed input voltage of 0.5 V for three different operating frequency ranges (0.2 MHz, 1 MHz, and 10 MHz). The Figure 5.5, 5.6 and 5.7 show the efficiency vs load current profile along with model prediction error at 0.2 MHz, 1 MHz and 10 MHz, respectively.

Figure 5.8 shows the Efficiency vs V_{in} profile along with model prediction error at 1 MHz and 1 μA load current.

The model can predict the efficiency profile of the Dickson charge pump with less than 14 % error in the frequency range of 0.2 MHz to 10 MHz at $V_{in} = 0.5\,V$. The load current range that can give maximum efficiency is considered during the model validation. The error can be varied and could be higher outside of this calculated current range, but it will not affect our model since the model is only required to calculate maximum efficiency with less prediction error. The R_{on} resistance of each switch in the model is kept at a constant value during the model validation. However, it is not constant and will vary non-linearly with different load current profiles. Also, the threshold voltage is assumed to be in the range of 0.16 V - 0.2 V during the validation process. This is another reason we could expect a prediction error closer to 14 % in some cases. However, the overall prediction error is less than 14 % for the given load current range.

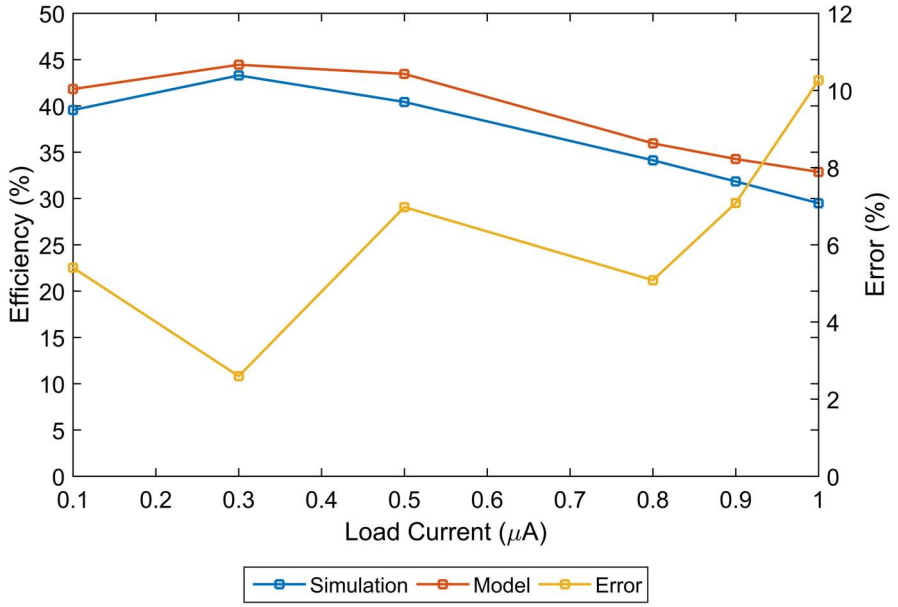

FIGURE 5.5: Efficiency vs Load current profile along with model prediction error for Dickson three stage charge pump topology at 0.2 MHz

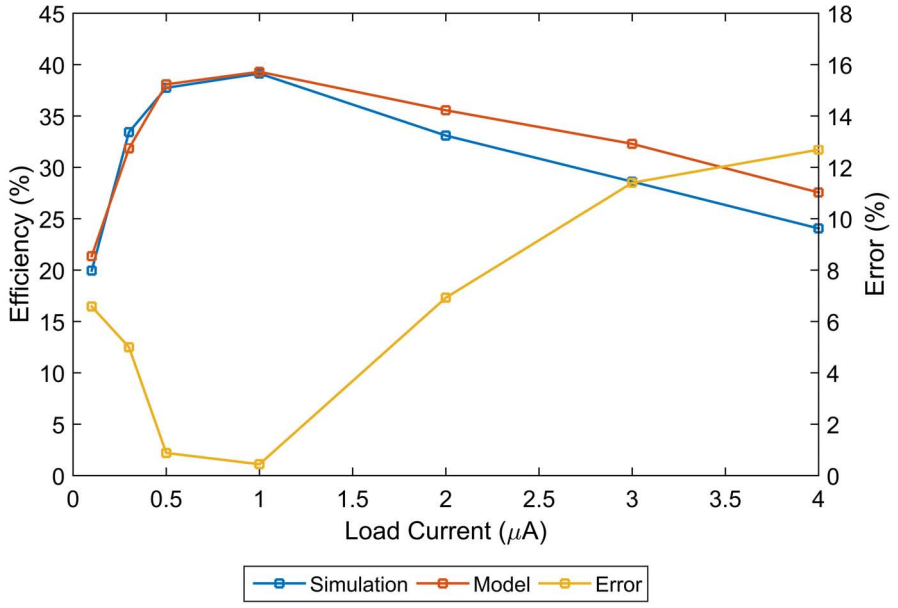

FIGURE 5.6: Efficiency vs Load current profile along with model prediction error for Dickson three stage charge pump topology at 1 MHz

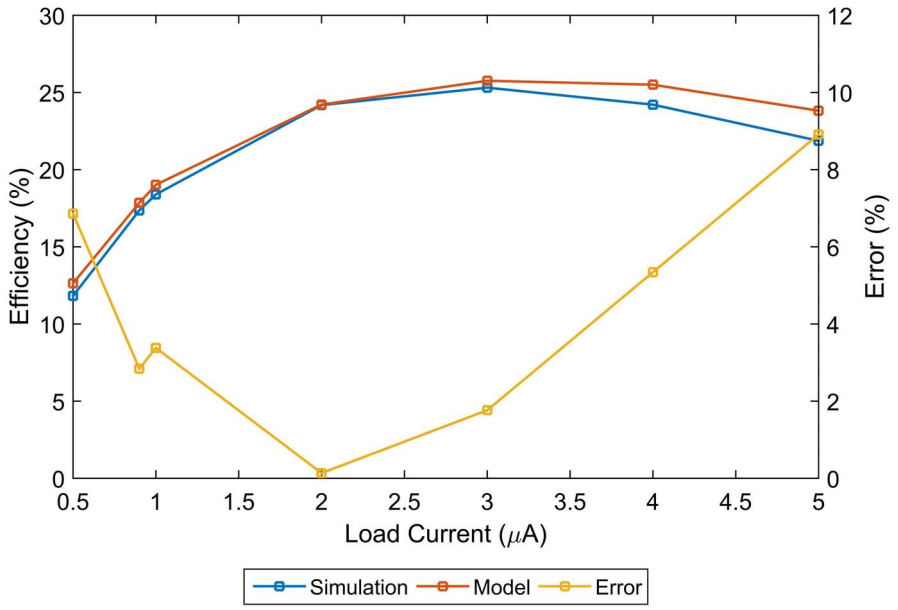

FIGURE 5.7: Efficiency vs Load current profile along with model prediction error for Dickson three stage charge pump topology at 10 MHz

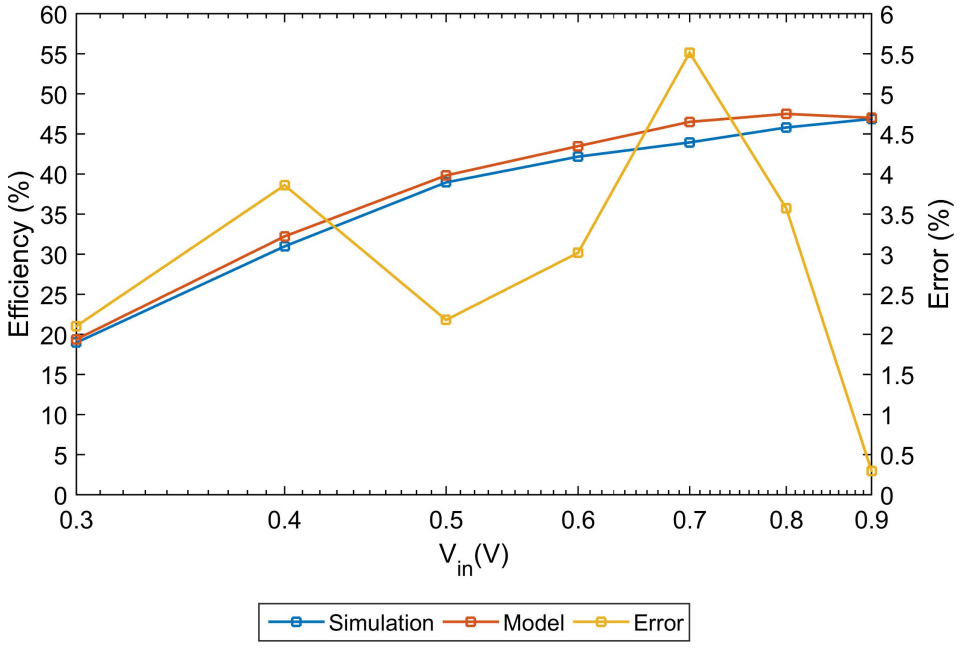

FIGURE 5.8: Efficiency vs V_{in} profile along with model prediction error at 1 MHz at $1\,\mu A$ load current for Dickson Charge pump topology

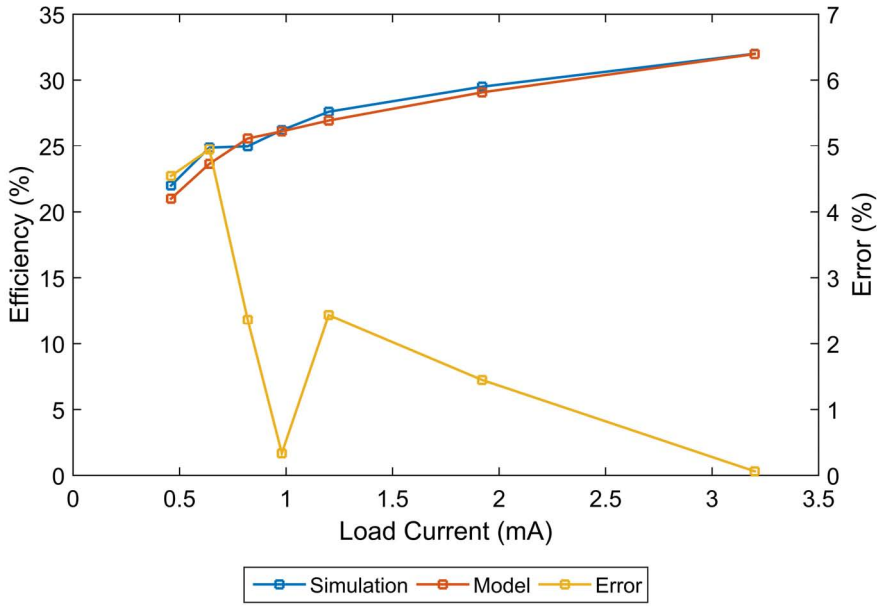

FIGURE 5.9: Efficiency vs I_{Load} profile along with model prediction error at 100 kHz at for boost converter

The boost converter validation is carried out with asynchronous rectification. A diode connected NMOS is used as a diode for this purpose. The simulation is carried out with an input voltage of 0.2 V and fixed frequency of 100 kHz. The output voltage is set to 1.7 V. Figure 5.9 shows the efficiency vs I_{Load} profile along with model prediction error at 100 kHz for the boost converter.

The validation result of the output voltage with load resistance values is shown in Figure 5.10. The input voltage is 0.2 V and the duty cycle is 0.2 with 100 kHz operating frequency, which is maintained during the validation process.

Buck converter validation is carried out with asynchronous rectification. The diode connected NMOS is used as a diode for this purpose. The simulation is carried out with an input voltage of 1.5 V and fixed frequency of 100 kHz. The output voltage is set at 1 V. Figure 5.11 shows the efficiency vs I_{Load} profile along with model prediction error at 100 kHz for the buck converter.

The output voltage generation of the buck converter is validated and it is shown in Figure 5.12. The input voltage, duty cycle and frequency are set to 1 V, 0.6 and 100 kHz respectively during the validation process.

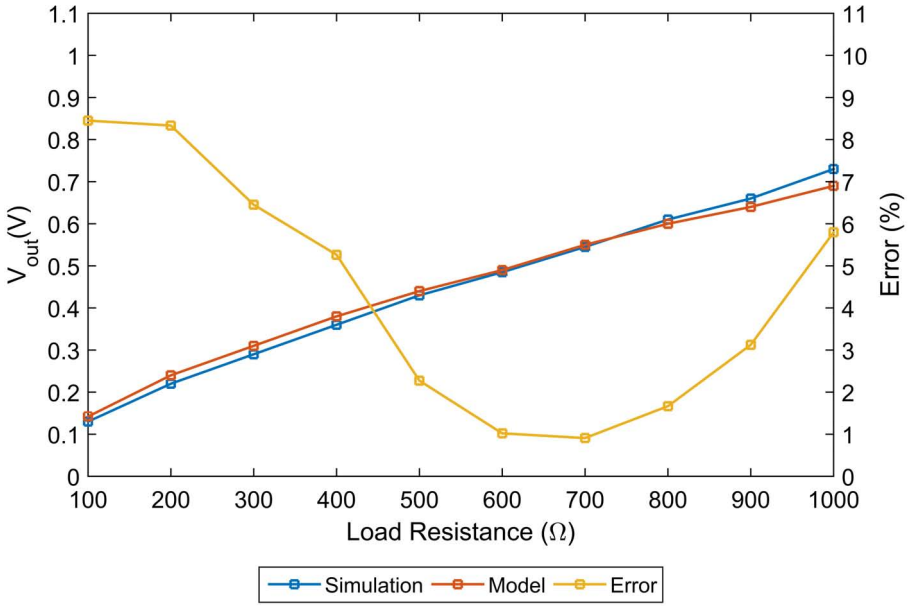

FIGURE 5.10: V_{out} vs Load resistance profile along with model prediction error for boost converter

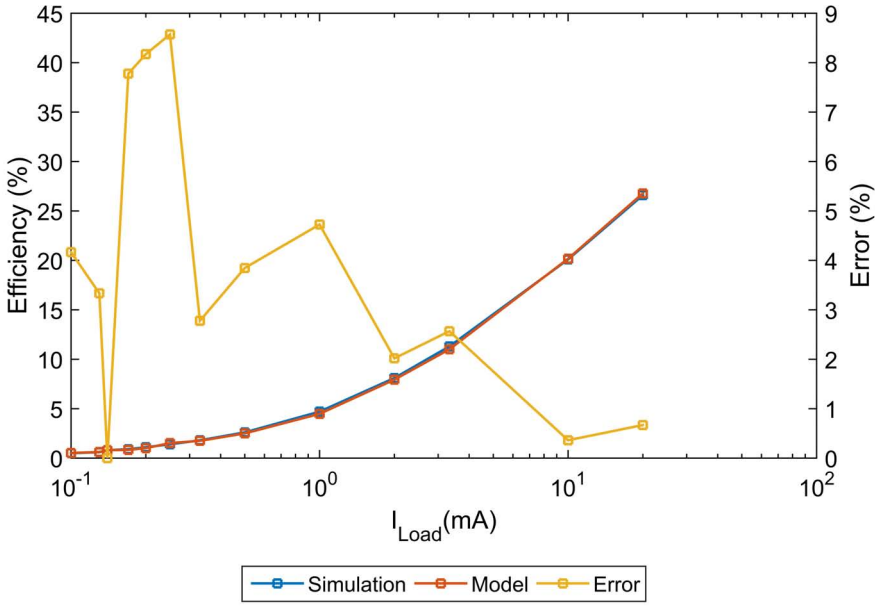

FIGURE 5.11: Efficiency vs I_{Load} profile along with model prediction error at 100 kHz for the buck converter

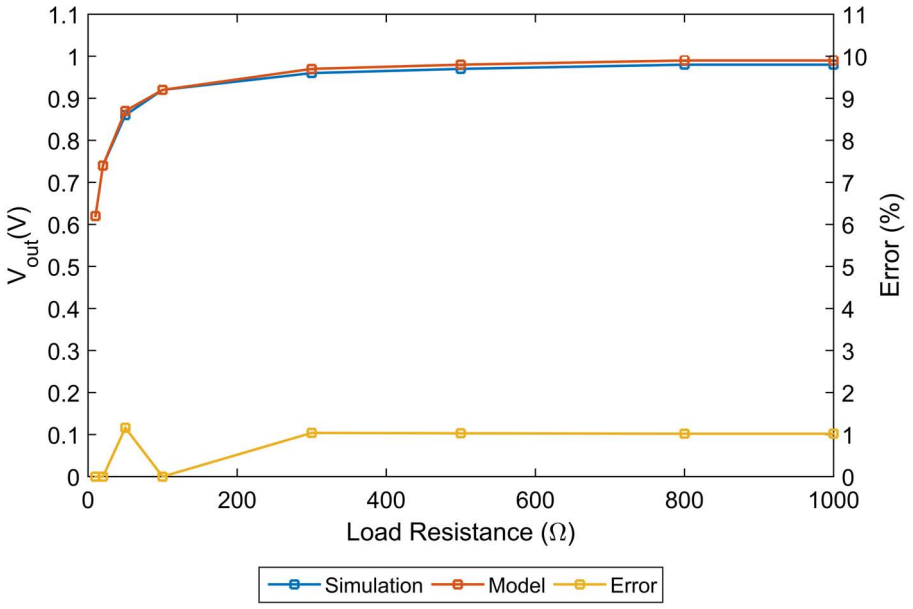

FIGURE 5.12: V_{out} vs Load resistance profile along with model prediction error for the buck converter

5.3 The usage of the unified model

5.3.1 Introduction

The energy flow of the proposed unified model is shown in Figure 2.2. The sample output generated from the switch capacitor-LDO unified model is shown in Figure 5.13. The switch capacitor is used here as a boost converter with a conversion ratio of 3 and an LDO as a regulator. The sample output of the Dickson charge pump with an LDO at $V_{in} = 0.5\,V$ and $V_{reglated} = 0.8\,V$ for a given load current profile is shown in Figure 5.13.

Experiments can be designed to optimize the overall system to obtain higher efficiency. Several experiments are designed to show the usefulness of the proposed unified model.

5.3.2 Experiment 1

The goal of this experiment is to design a regulator that can generate 0.48 V from 1.2 V. The voltage values are chosen arbitrarily for the purpose of this experiment. It assumes that only LDO and series parallel switch capacitor topology are available. There are three ways to design this system (LDO only, switch capacitor only and LDO + switch

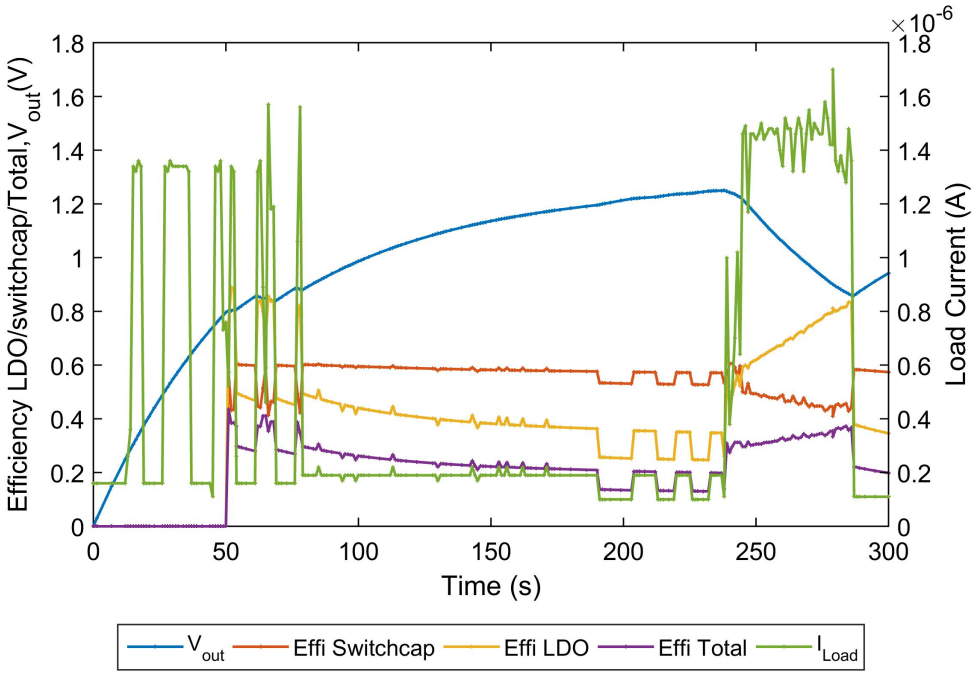

FIGURE 5.13: The sample output for the Dickson charge pump with an LDO at $V_{in} = 0.5\,V$ and $V_{reglated} = 0.8\,V$ for a given load current profile

capacitor). It is obvious from Figure 5.2 that an LDO has a very low efficiency when $\Delta\,(Vout - Vin)$ is high due to the power loss through the power switch. On the other hand, switch cap only or LDO + switch capacitor are feasible configurations to attain the above requirement.

Figure 5.14 and Figure 5.14 show the contour plot of efficiency and ripple if the switch cap (series-parallel topology) only configuration is used to regulate the voltage from 1.2 V to 0.48 V for different load current and frequencies, respectively.

Figure 5.16 and Figure 5.17 show the contour plot of efficiency and ripple if the switch capacitor (series-parallel topology) + LDO configuration is used for the same experiment. In this scenario, the switch capacitor circuit convert 1.2 V to 0.6 V and then uses an LDO to converts it further to 0.48 V, so that the LDO can have a maximum efficiency.

According to the four plots, the hybrid system with switch capacitor + LDO configuration exhibits higher efficiency with less ripple compare to that of the switch capacitor only system. However, the system has lower efficiency at frequencies higher than 1 MHz. The calculated efficiency values are true for the given fly capacitance and switch

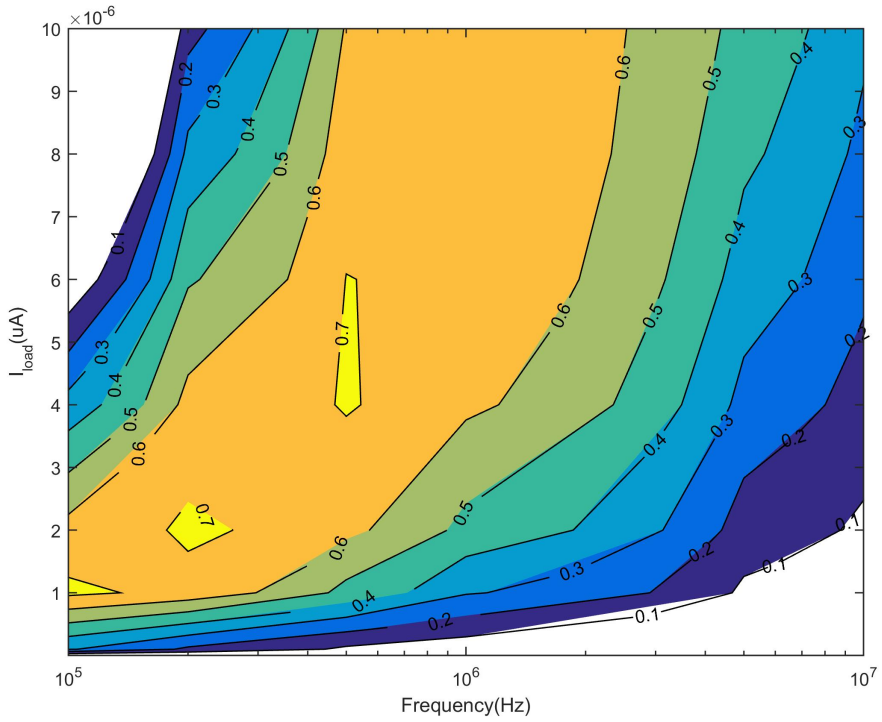

FIGURE 5.14: Contour plot of efficiency with I_{load} and frequency for series-parallel topology converting 1.2 V to 0.48 V.

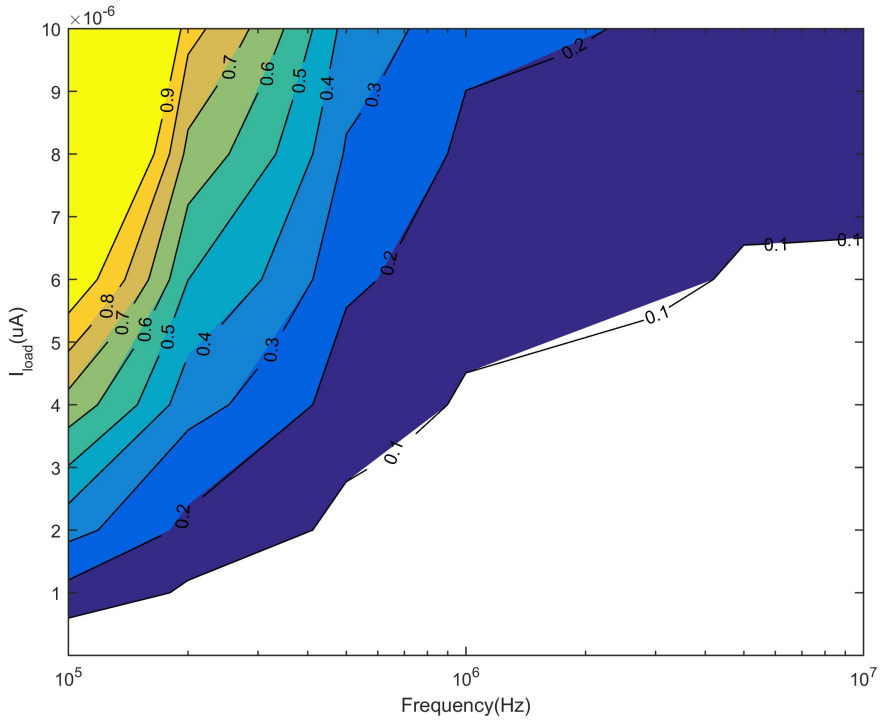

FIGURE 5.15: Contour plot of ripple ($\Delta V/Vout$) with I_{load} and frequency for series-parallel topology converting 1.2 V to 0.48 V.

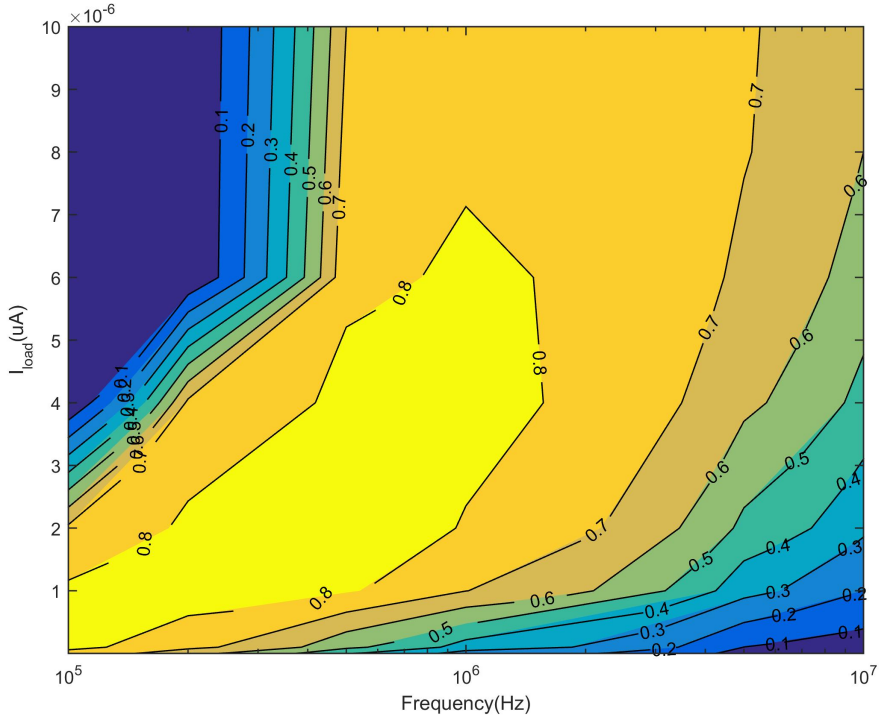

FIGURE 5.16: Contour plot of efficiency with I_{load} and frequency for series-parallel topology + LDO converting 1.2 V to 0.48 V.

resistance area. The efficiency value can vary with different switch sizes or with fly capacitance area. If the area is constrained in a proposed system, the user needs to rerun the optimization by changing fly capacitance and switch sizes.

5.3.3 Experiment 2

In order to achieve the highest overall efficiency of a converter for a given power density and area, the total loss should be minimized. The model can be used to identify the operating frequency, the load current range, and the generated output voltage that gives the converter the highest efficiency for a given input voltage, switch area, and fly capacitance area. The area optimization can be evaluated if the area is constrained for the design.

Optimization of the open loop buck converter is carried out by running the external MATLAB code listed in Appendix A. Input voltage, duty cycle and the inductor value of the buck converter are assumed to be at 1.6 V, 0.4 and 10 μH respectively. Figure 5.18 and Figure 5.19 show the contour plot of efficiency and output voltage with load resistance and frequency for a buck converter operating at 1.6 V.

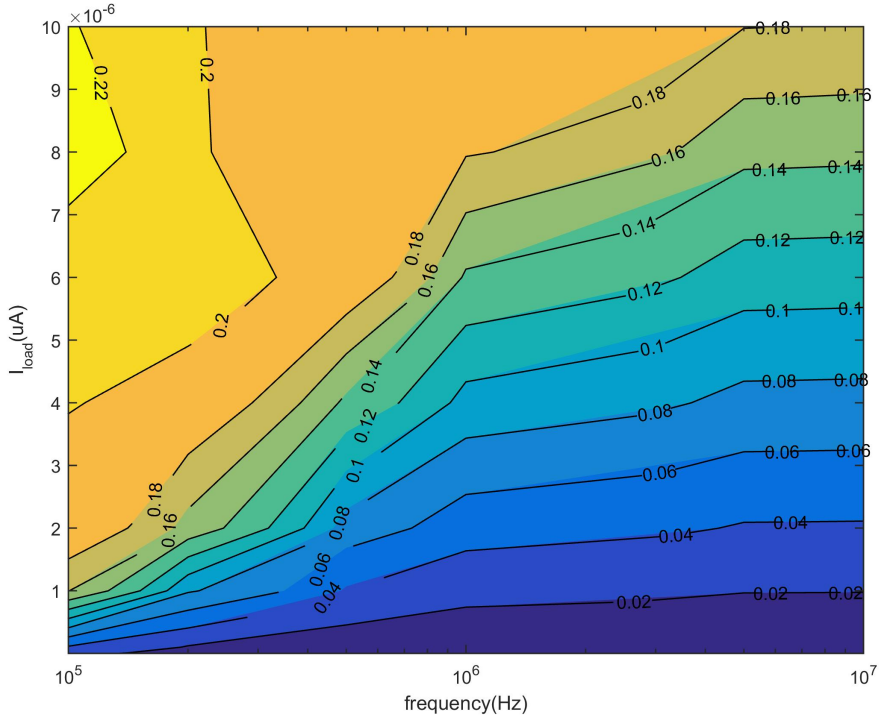

FIGURE 5.17: Contour plot of ripple ($\Delta V/Vout$) with I_{load} and frequency for series-parallel topology + LDO converting 1.2 V to 0.48 V.

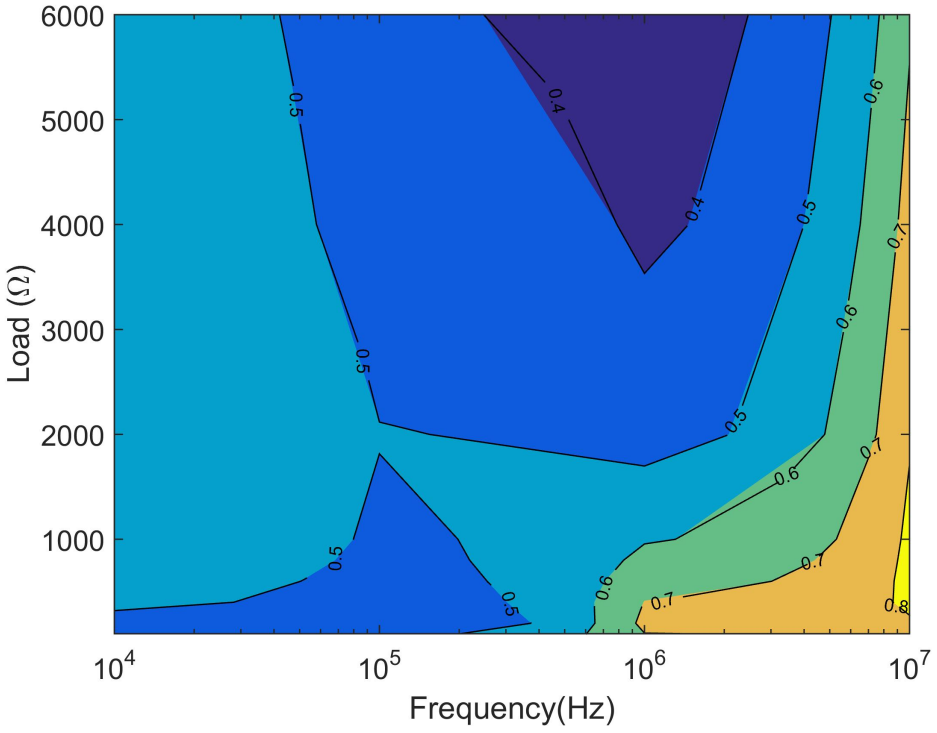

FIGURE 5.18: Contour plot of efficiency with load resistance and frequency for a buck converter operating at 1.6 V

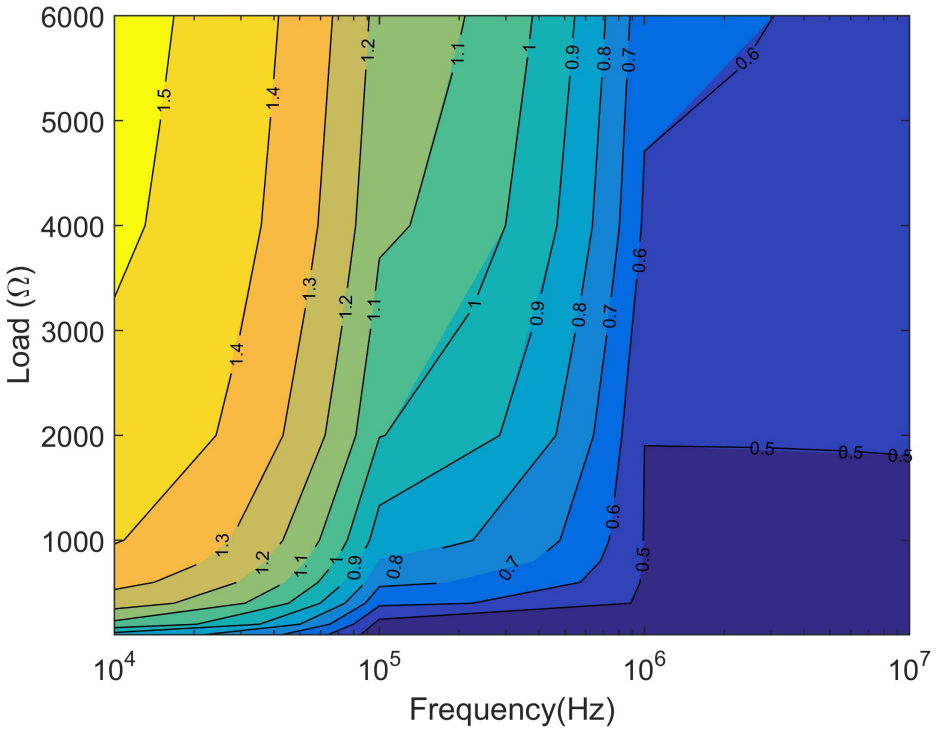

FIGURE 5.19: Contour plot of output voltage with load resistance and frequency for a buck converter operating at 1.6 V

Based on the results, it is clear that the best frequency range will be 0.5 MHz to 5 MHz if the required output voltage range is 0.5 V to 1 V. However, it is up to the designer to choose the required frequency range based on their application.

Similar to the buck converter, the boost converter can also be optimized using a similar method. In the simulation, it is assumed that the boost converter has an input voltage of 0.1 V. The duty cycle and the inductor values are fixed to 0.6 and 10 μH respectively during simulation.

The model assumes no power losses due to the control circuitry. Therefore the power loss of the control circuit can be included as a percentage into the model based on the design. According to Figure 5.20 and Figure 5.21, it is evident that the boost converters are suitable for heavy load rather than light load conditions.

Figure 5.22 and Figure 5.23 show the 4D plot of efficiency and the output voltage variation of the boost converter operating at 0.1 V with respect to the load resistance, the duty cycle and the frequency respectively. According to the results, it confirms that the traditional boost converter generates higher efficiency for heavy load conditions. Depending on the output voltage, the user can choose the range of the duty cycle and operating frequency.

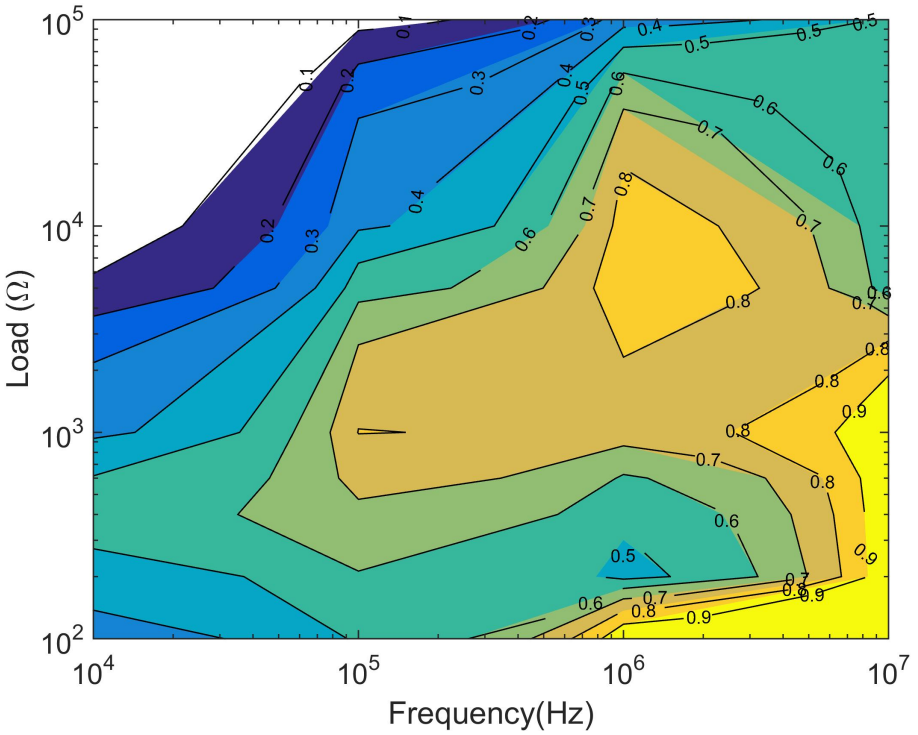

FIGURE 5.20: Contour plot of efficiency with load resistance and frequency for a boost converter operating at 0.1 V

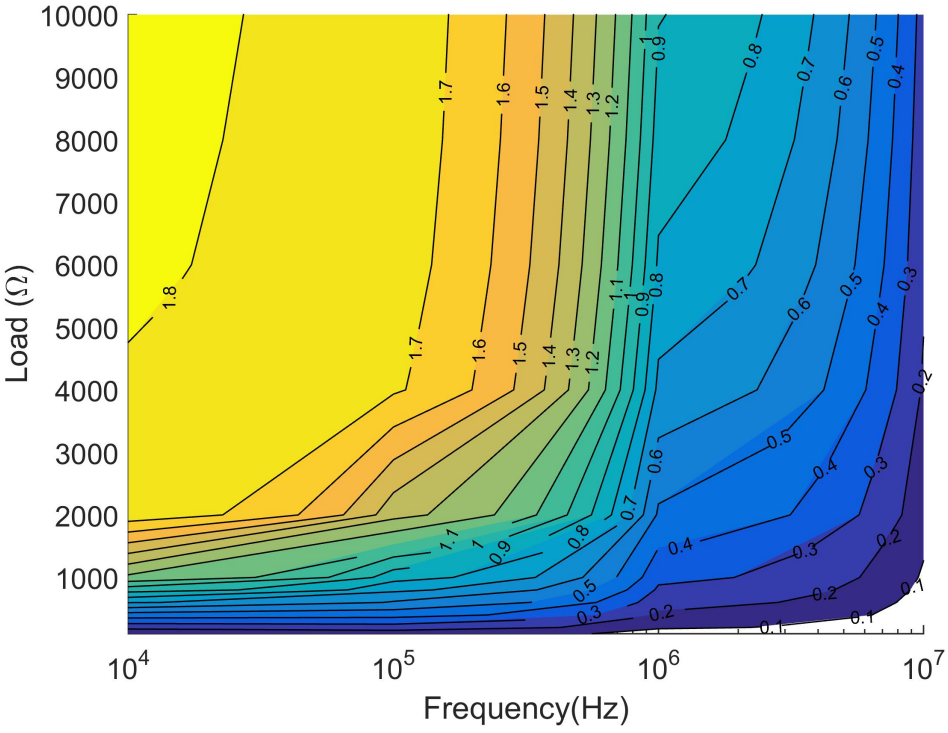

FIGURE 5.21: Contour plot of output voltage with load resistance and frequency for a boost converter operating at 0.1 V

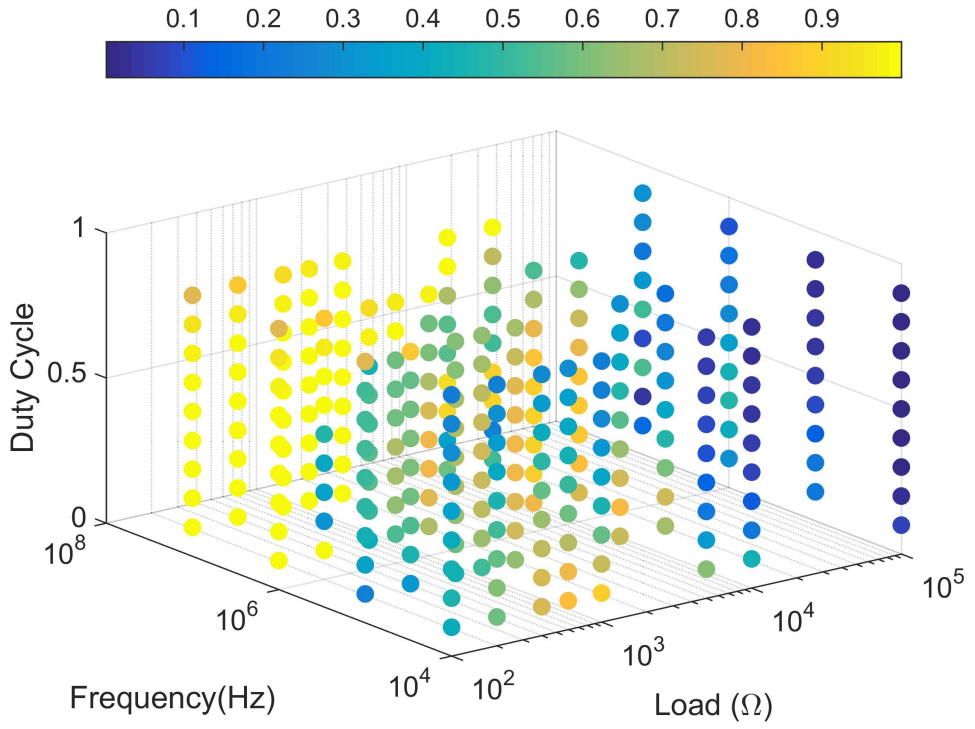

FIGURE 5.22: 4D plot of efficiency with load resistance, duty cycle and frequency for a boost converter operating at 0.1 V

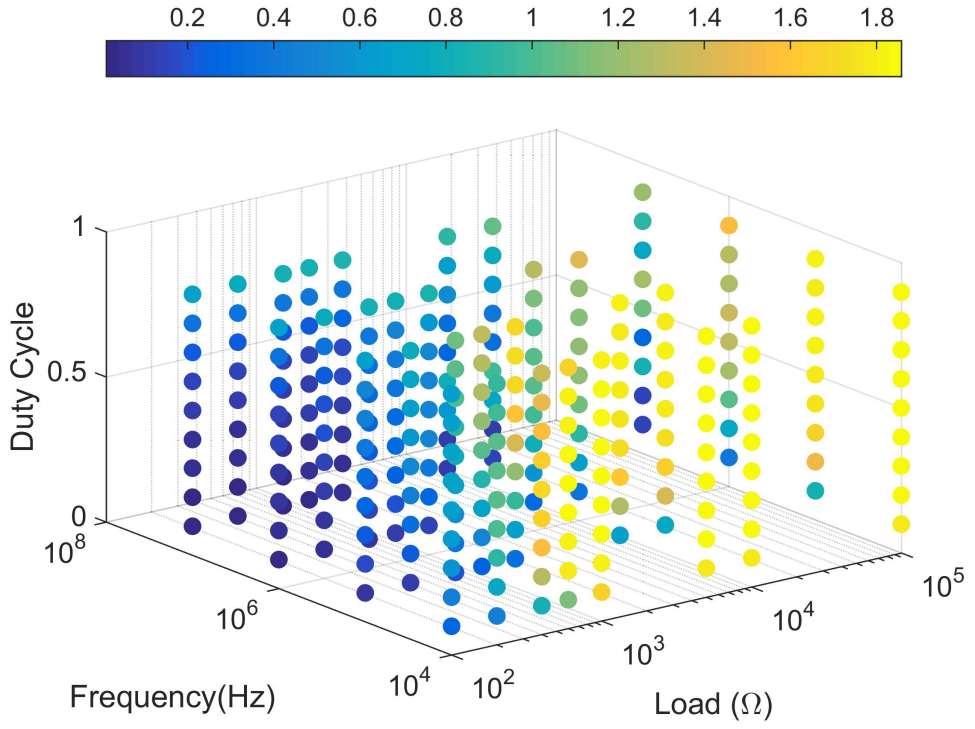

FIGURE 5.23: 4D plot of output voltage with load resistance, duty cycle and frequency for a boost converter operating at 0.1 V

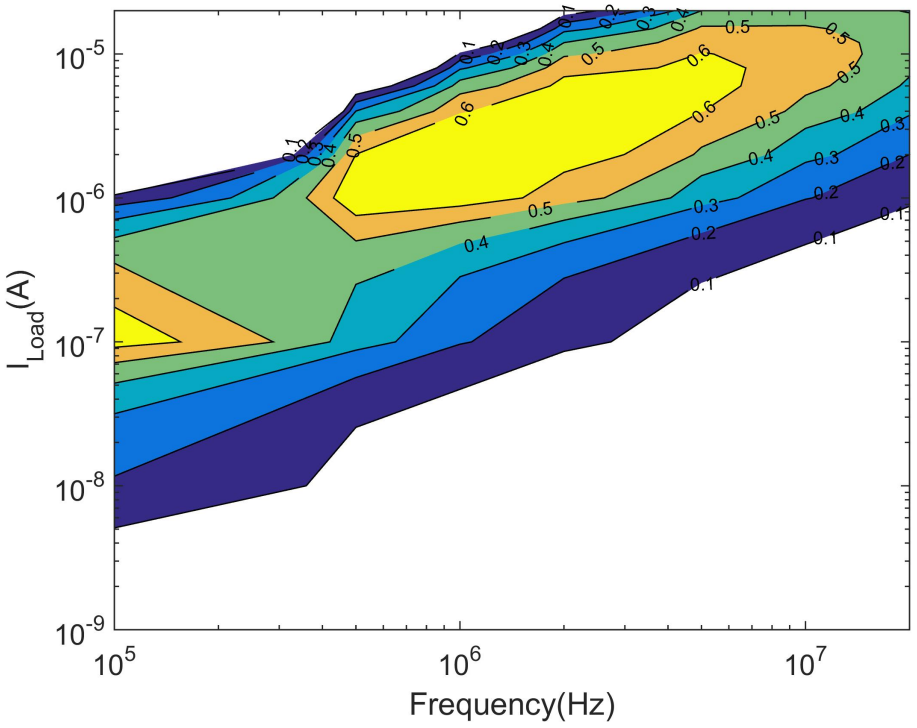

FIGURE 5.24: Contour plot of efficiency with I_{Load} and frequency for 2-stage NCP4 at 0.5 V(C_{fly}=31 pF,W=50 μm)

For an example, if a user needs 1 V or higher with more than 60 % efficiency, a 0.1 MHz to 1 MHz frequency range with a duty cycle ranging from 0.3 to 0.8 can be chosen for the design.

The optimization of the switch capacitor circuit can also be done by a similar method. Figure 5.24 and Figure 5.25 show the contour plot of efficiency and output voltage with I_{Load} and frequency for a 2-stage charge pump circuit with cross connected NMOS cells (NCP4). Fly capacitance and NMOS width are chosen to be 31 pF and 100 μm respectively. By changing the width and fly capacitance, the user can adjust maximum efficiency to shift into the required load current range. These phenomena are illustrated in Figure 5.26 and Figure 5.27. Maximum efficiency of the converter can be achieved for light loads by lowering the size of the width and fly capacitance. The general optimization script is shown in Appendix A can be used for this purpose.

5.3.4 Experiment 3

The goal of this experiment is to evaluate the performance of topologies with input voltage noise. The following assumptions are made for the system:

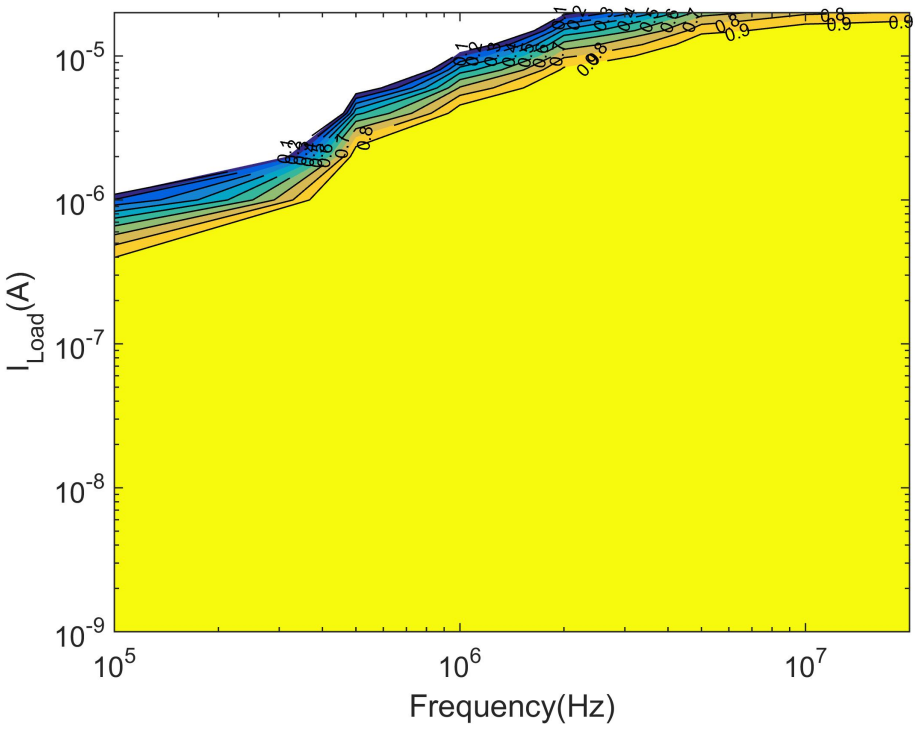

FIGURE 5.25: Contour plot of output voltage with I_{Load} and frequency for 2-stage NCP4 at 0.5 V(C_{fly}=31 pF,W=50 μm)

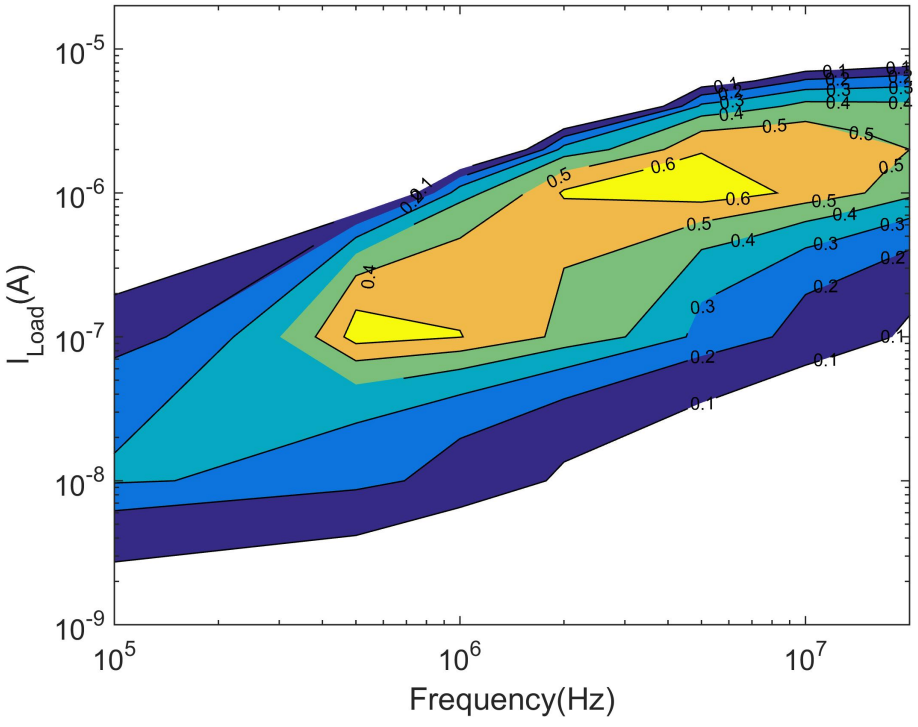

FIGURE 5.26: Contour plot of efficiency with I_{Load} and frequency for 2-stage NCP4 at 0.5 V(C_{fly}=4 pF,W=10 μm)

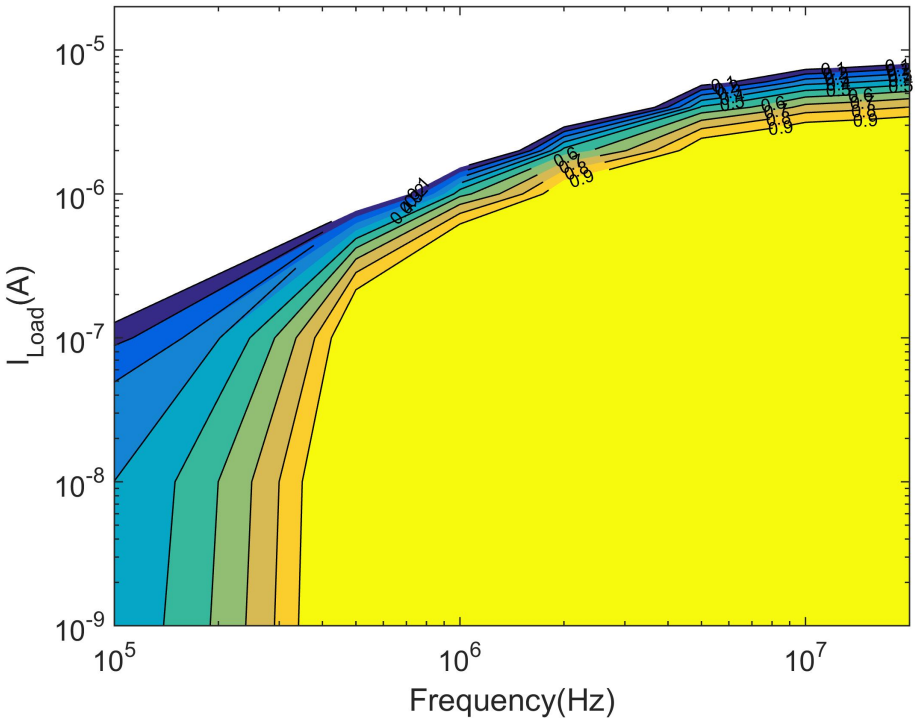

FIGURE 5.27: Contour plot of output voltage with I_{Load} and frequency for 2-stage N at 0.5 V(C_{fly}=4 pF, W=10 μm)

- The average voltage (unregulated) stored on the storage capacitor (VCAP) = 1.6 V.
- The harvester can generate the required power for both converters without interruptions.
- The clamping circuit will turn on when V_{BOOST}(harvester output) exceeds 1.8 V and clamp V_{BOOST} to 1.8 V to prevent device damage.
- The harvester is biased at the maximum power point (VMPP).
- Fixed load current range is used for a 1st order analysis.
- The fly capacitance and width of the NMOS transistors in switch capacitor circuit is fixed at 31 pF and 50 μm respectively.
- The operating frequency of the switch capacitor topology are fixed at 1 MHz.
- The control circuit current of the LDO is fixed at 0.16 μA.

The signal is applied to the input voltage of 0.5 V with 200 mV of ripple amplitude. The frequency of the ripple amplitude can be varied depending on the user requirement.

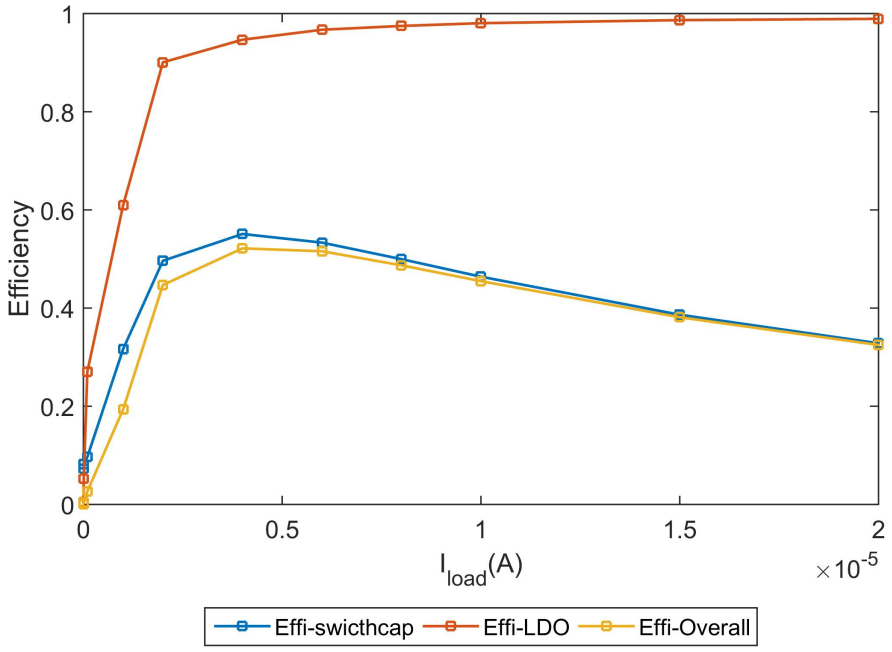

FIGURE 5.28: Efficiency vs Load current for Dickson topology (boost converter) + LDO

During this experiment, it was fixed to 1 KHz (Ultimately variation in amplitude with V_{DD} and droop frequency will be a function of system clock frequency and timing once the clocking models are available in the future developed model). The initial experiments are executed with 2 basic topologies in the MATLAB model:

- Switched capacitor (boost converter) + LDO
- Switched capacitor(boost converter) + Switched capacitor (regulator)
- Measure efficiency results for the above systems for different load currents (at fixed VDDs with droop).

Figure 5.28, Figure 5.29, Figure 5.30 and Figure 5.31 show the efficiency vs load current of the Dickson, Doubler, NCP4 and Series-parallel topologies respectively.

According to the figures, it is obvious that the series-parallel topology has the highest efficiency. The lowest efficiency is reported for Dickson topology, as expected. The diode connected NMOS connection will degrade the efficiency of the traditional Dickson charge pump topology. It is also noted that, even though the series-parallel topology can generate the highest efficiency, overall efficiency is degraded for the system as LDO

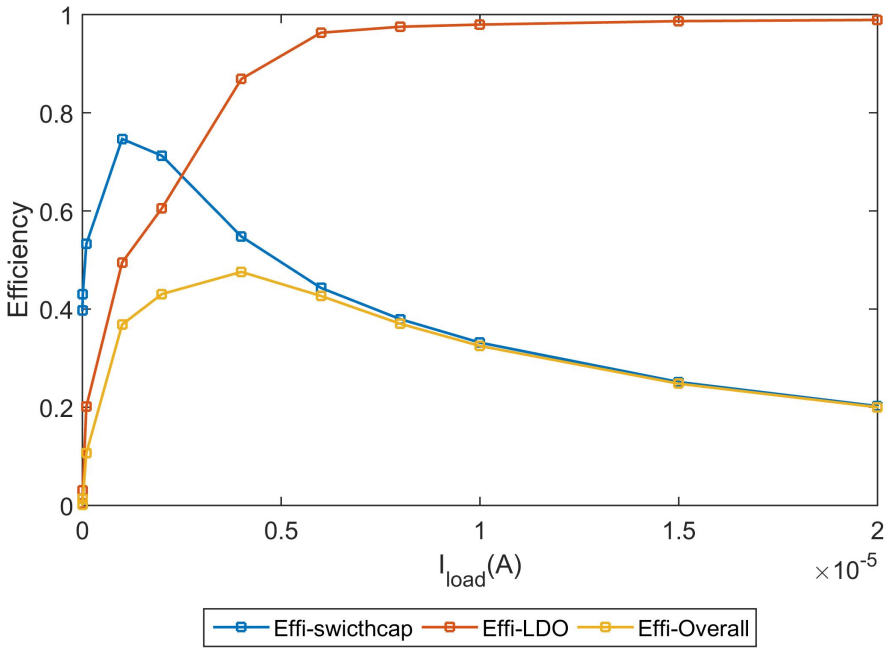

FIGURE 5.29: Efficiency vs Load current for Doubler Topology (boost converter) + LDO

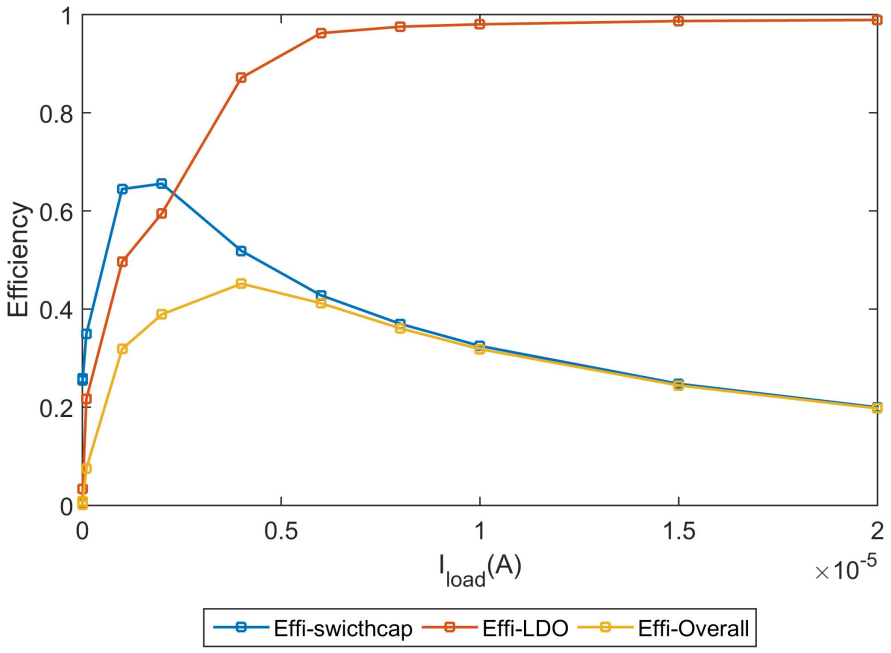

FIGURE 5.30: Efficiency vs Load current for NCP4 topology (boost converter) + LDO

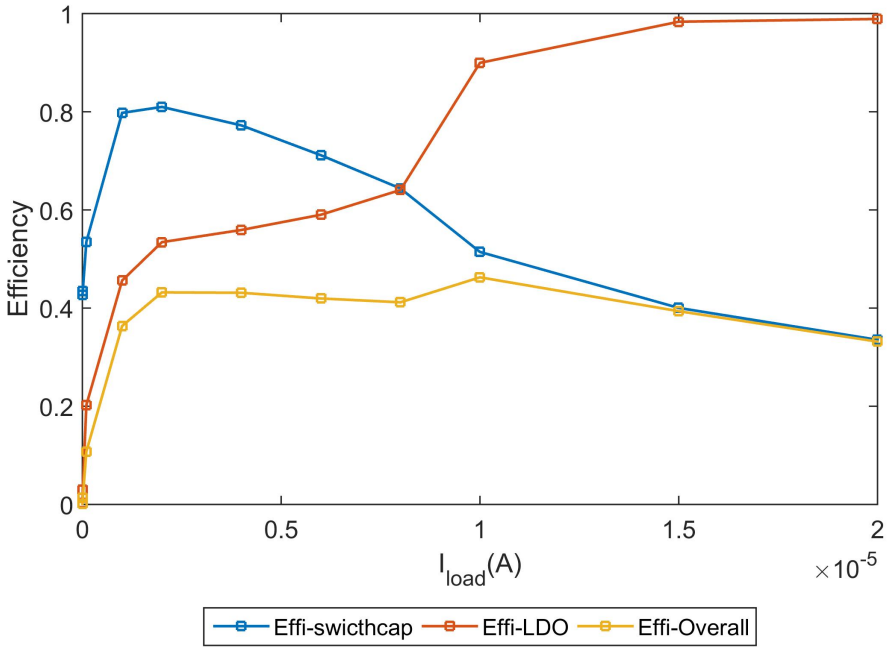

FIGURE 5.31: Efficiency vs Load current for series parallel topology (boost converter) + LDO

efficiency fluctuates. This is because LDO efficiency degrades as soon as the difference between V_{CAP} and regulated output voltage is higher. This can be avoided by using a lower step up ratio for the series-parallel converter or by setting a higher regulated output voltage limit from the LDO.

Based on the results, only the series-parallel topology is used for the configuration of switched capacitor (boost converter) + switched capacitor (regulator) since it can generate the highest efficiency as a boost converter. The fly capacitance and width of the NMOS transistors in the switch capacitor is fixed at 31 pF and 50 μm respectively. The operating frequency of the switch capacitor (boost) topology and switch capacitor (regulator) are fixed to 1 MHz and 100 kHz respectively. Figure 5.32 shows the efficiency vs load current for the configuration of series-parallel topology (boost converter) + series-parallel topology (regulator).

According to the results, configuration of the series-parallel topology (boost converter) + series-parallel topology (regulator) can generate maximum efficiency compare to the configuration of series-parallel topology (boost converter) + LDO.

The boost converter + LDO is considered next for the proposed experiment. The efficiency vs load current plots of the boost converter + LDO system with two different

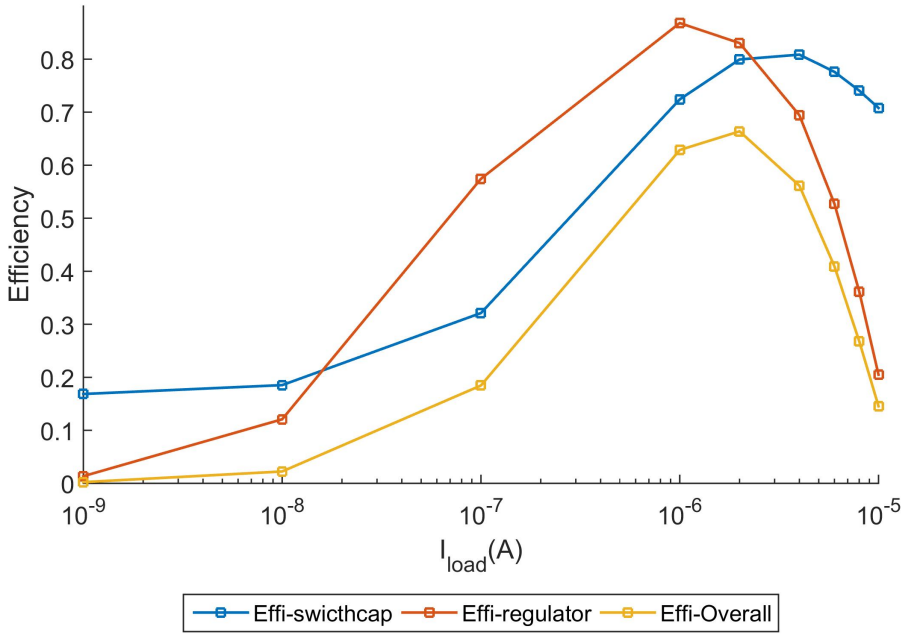

FIGURE 5.32: Efficiency vs Load current for series-parallel topology (boost converter) + series-parallel topology(regulator)

regulated output voltages are shown in Figure 5.33 and 5.34 respectively. During the simulation, following settings were used:

- Boost converter input has a ripple of 0.2 V with 1 KHz frequency at 0.3 V.
- Operating frequency and duty cycle are fixed to 1 MHz and 0.6 respectively.
- Inductor size used in the boost and buck converters is $10\,\mu H$.
- Switch resistance and inductor series resistance of both boost and buck converters are taken to be $0.3\,\Omega$ and $0.02\,\Omega$.
- LDO regulated voltages are set to 1 V and 1.6 V for the experiments and the control circuit current of the LDO is fixed to $0.16\,\mu A$.
- Buck converter operating frequency and duty cycle are fixed to 1 MHz and 0.4 respectively.

Boost converter + buck converter is considered as a next configuration. The sample output of the inductor current and capacitor current of the boost converter + buck converter configuration of the unified model is shown in Figure 5.35.

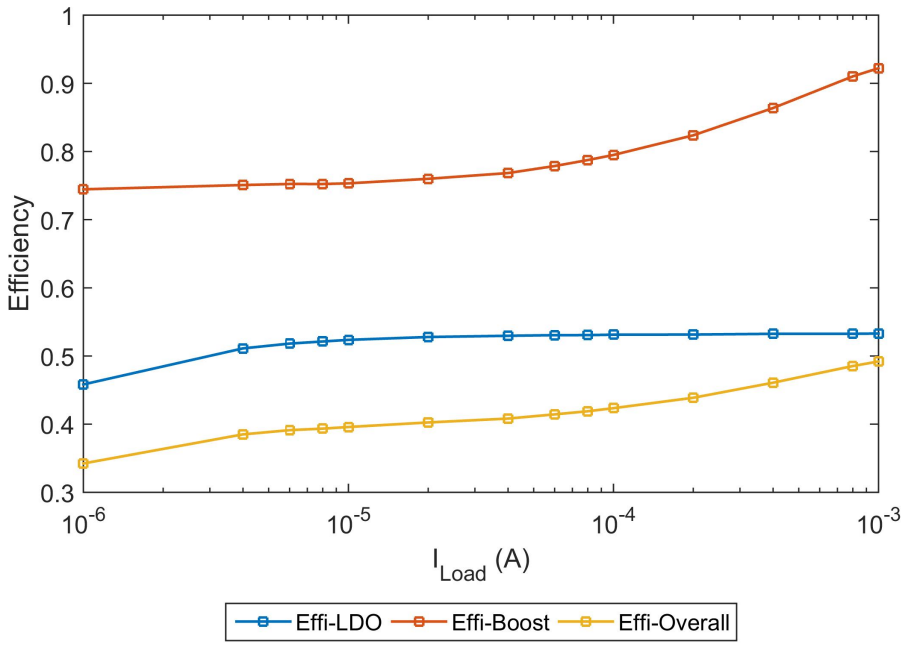

FIGURE 5.33: Efficiency vs Load current for boost converter + LDO at 1V regulated output

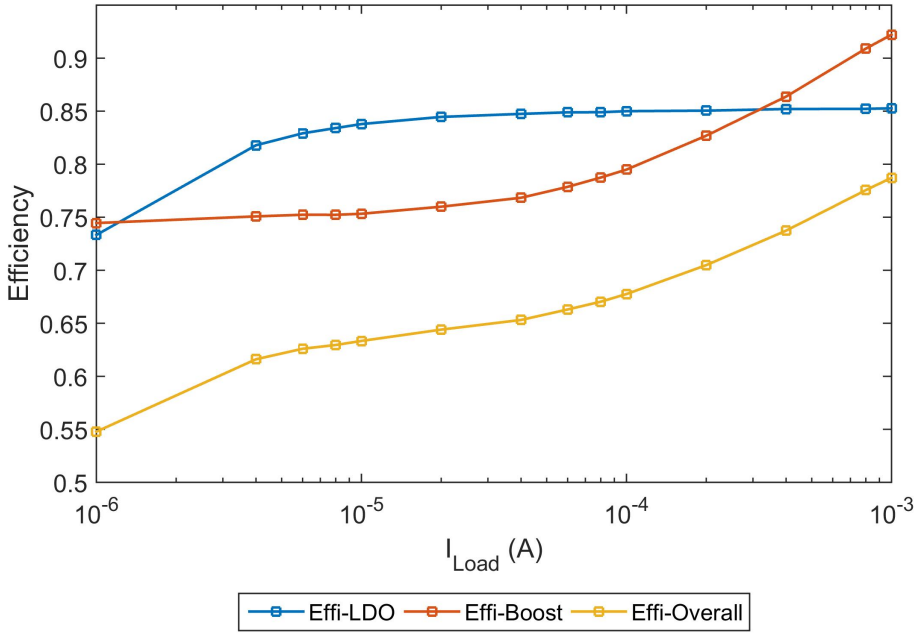

FIGURE 5.34: Efficiency vs Load current for boost converter + LDO at 1.6V regulated output

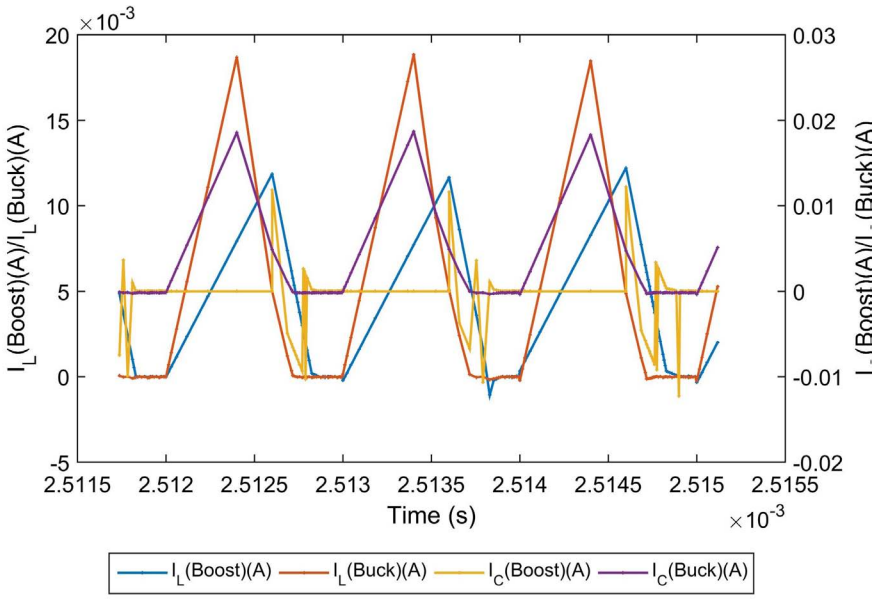

FIGURE 5.35: Inductor and capacitor current profile of the boost converter + buck converter (unregulated) with time

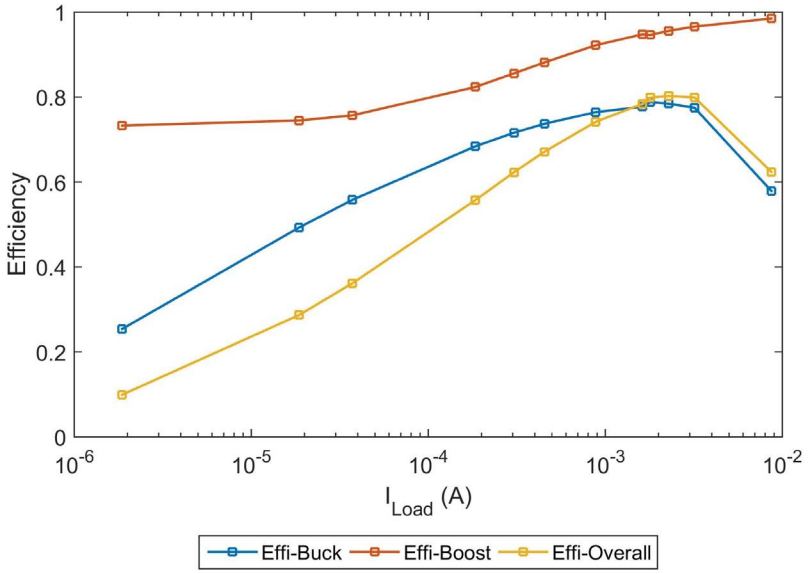

FIGURE 5.36: Efficiency vs Load current for boost converter + buck converter (unregulated)

According to the result, the configuration of the boost converter + LDO is more tolerant to the input voltage noise than the traditional boost converter + buck converter configuration for light loads. However, it is difficult to draw a conclusion as to whether the boost converter or buck converter has the lowest efficiency at light load condition considering the fact that the model doesn't have a control loop design. Also in the model, the boost converter is working continuously, resulting in a degraded efficiency at light load conditions (microampere range). The model uses traditional boost converter and buck converter design. By integrating a different control loop design, boost and buck converters can be tuned to generate higher efficiency than the predicted efficiency. Because of these reasons, simulation of boost converter + switch capacitor converter (regulator) and switch capacitor (boost converter) + buck converter (regulator) are avoided as it will generate very low efficiency for very light load conditions.

Chapter 6

Conclusion and Future work

6.1 Thesis conclusion

In this thesis, a tool based on MATLAB simulink is developed to analyze power management circuits in energy harvesting systems. The proposed tool is not designed to replace CAD tools like SPICE. Instead, it is designed to get a rough idea of the system behavior under certain conditions. The currently developed tool consists of models for inductor based DC-DC converters, inductor based buck converters, linear dropout regulators (LDO), non-inductor based DC-DC converters. The non-inductor based converters includes 5 different topologies such as Dickson, Doubler, Cross connected NMOS charge pump circuit series-parallel and Fibonacci based switch capacitor topologies. The tool is also developed further to make a unified global energy harvesting model for inductor based and non-inductor based DC-DC converters. Individual models were verified in SPICE using CMOS 130 nm technology. The model can be used to derive the characteristics of systems in other technologies by updating the technology library. Usage of the developed tools was discussed in detail using three experiments.

The first experiment is designed to identify whether the configurations of LDO, switch capacitor (regulator) + LDO (hybrid mode regulation), switch capacitor only (regulator) are suitable to generate 0.48 V from 1.2 V. The results suggested that the efficiency of the hybrid mode is 10 % higher compared to that of the switch capacitor only regulator for the load current range of 1 nA to 10 μA. Ripple can be minimized by choosing a frequency in the range of 0.6 MHz to 10 MHz.

The second experiment is designed to show how the tool can be used to optimize the individual models to identify the suitable duty cycle, frequency, load current range, flying capacitance size and sizes of the switches. According to the model prediction, the

traditional design of boost and buck converters has very low efficiency for light loads (microampere). This is because the current model does not include the control loop designs for the inductor based boost or buck converter to shut down its operation when it reaches to the required output voltage. Therefore, it generates lower efficiency for very light load.

The goal of the third experiment is to evaluate the performance of topologies with input voltage noise. The series-parallel converter (boost converter) + series-parallel converter (regulator) generate higher efficiency for a given load current range and frequency compared to that of the switch capacitor (boost converter) + LDO (regulator) configuration for non-inductor based converters. For inductor based converters, the boost converter + LDO exhibits higher efficiency for the given load current range if 1.6 V regulation is considered.

6.2 Future work

Overall the proposed unified model can be used to do a preliminary analysis of a power management system in energy harvesting systems. However, the model can be further improved to generate more accurate results. In detail:

- The current model consist of open loop DC-DC converter model. Closed loop models can be developed in order to analysis the converter's performance in Pulse-Frequency Modulation (PFM) , Pulse Width Modulation (PWM).
- The AC-DC converter model can be included in the main flow of the proposed system, so that the system performance can be predicted for piezoelectric energy harvesting systems.
- Maximum power-point tracking models can be implemented so that the boost converter model can provide an optimum input impedance to the harvester to extract the maximum energy.
- Characterize a commercial TEG or PV cell, generate a P-V curve and feedback into the proposed system.
- Generate a model for a clock generator, a clock tree and load circuits to model current draw. This may also include the power consumption of analog and digital circuits.
- Validation of proposed tool can be carried out in Si and compared with the simulation results.

Appendix A

MATLAB codes useful for running models

```
%This is code to run the optimization of the siwtch capacitor circuit to
%have maximum efficiency by varying the frequency and the load current
close all
clear all
clc
%Open the simulink model
%Here you will specify the model you want to run
open_system('SwitchcapOnly_sim_ripple_calculation')
%Define the parameter you want to change during the parametric simulation
fre=[1e5,5e5,1e6,2e6,5e6,10e6,20e6];
Iload=[0.001e-6,0.01e-6,0.1e-6,1e-6,2e-6,4e-6,6e-6,8e-6,10e-6,12e-6,15e
    -6,20e-6];
for k=1:length(Iload)
    IL=Iload(k);
    for n=1:length(fre)
    f=fre(n);
simOut=sim('SwitchcapOnly_sim_ripple_calculation','StopTime','300');
y = simOut.get('Vout');%get the generated data from simulink
y1(k,n)=y.signals.values(end);%storing the generated data
ti = y.time;
y2=simOut.get('Effi');
y3(k,n)=y2.signals.values(end);
 end
end
%Generate the required plot
set(0,'DefaultAxesFontname','CMU Serif')
 figure (1)
[C1,h1] =contourf(fre,Iload,y1,[0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9],'
    ShowText','on');
clabel(C1,h1,'FontSize',16,'Color','blue','Fontname','CMU Serif');
```

```
set(gca,'xscale','log');
set(gca,'yscale','log');
set(gca,'FontSize',16);
  xlabel('Frequency(Hz)');
  ylabel('I_{Load}(A)');
 print('NCP4ripple', '-djpeg', '-r300')

figure (2)
[C,h] =contourf(fre,Iload,y3,[0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9],'
    ShowText','on');
clabel(C,h,'FontSize',16,'Color','red','Fontname','CMU Serif')
set(gca,'xscale','log');
set(gca,'yscale','log');
set(gca,'FontSize',16)
xlabel('Frequency(Hz)');
ylabel('I_{Load}(A)');
print('NCP4effi', '-djpeg', '-r300')
```

```
%This code will generate the current Swicthcap-LDO system output voltage
%and efficiency with time.Similler codes can be used to genrate the output
%of different systems with time
close all
clear all
clc
sim('Switchcap_LDO_effiplot')
h1=figure;
[AX,H1,H2] =plotyy(sc(:,1),[sc(:,3),sc(:,4),sc(:,5),sc(:,6)],sc(:,1),sc
    (:,2))
xlabel('Time (s)')
set(AX,{'ycolor'},{'k';'k'});
set(AX,{'xcolor'},{'k'});
% set(AX(1),'yscale','log');
 set(AX(1),'YLim',[0 1.8])
set(AX(1),'YTick',[0:0.2:1.8])
 set(AX(2),'YLim',[0 1.8e-6])
 set(AX(2),'YTick',[0:0.2e-6:1.8e-6])
% set(gca,'xscale','log');
set(H1,'linewidth',1.5);
set(H1,'Marker','square','MarkerSize',1);
set(H2,'linewidth',1.5);
set(H2,'Marker','square','MarkerSize',1);
set(AX,'FontSize',14);
set(AX,'Fontname','CMU Serif');
axes(AX(1)); ylabel('Efficiency LDO/switchcap/Total,V_{out}(V)');
axes(AX(2)); ylabel('Load Current (A)');

legend([H1;H2],'V_{out}','Effi Switchcap','Effi LDO','Effi Total','I_{Load}
    ', 'Location', 'SouthOutside','Orientation','horizontal');
```

```
29 print('unfied_LDO_switchcap', '-djpeg', '-r300')
```

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