Development of Heterogeneously Integrated Photodiodes and Schottky Diodes on Silicon Platforms

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Abstract

This work presents groundbreaking research in the development of heterogeneously integrated devices on silicon platforms, focusing on radio frequency (RF) and photonic devices that are pivotal for advancements in communications, computing, and sensing. The core of this research is divided into two parts.

The first part is the design, process development, characterization, and integration of gallium arsenide (GaAs) PIN photodetectors (PDs) on a new optical waveguide platform i.e. tantala (tantalum pentoxide). GaAs is selected for its high carrier mobility and direct bandgap properties, making it efficient for light absorption and crucial for high-speed communication systems. The study explores the integration of GaAs PIN PDs onto tantala substrates for visible light detection through adhesive bonding technique, emphasizing low dark current and high quantum efficiency. The fabrication challenges are addressed to ensure the development of high-quality, reliable devices. The results show up to 17 GHz bandwidth and pA-scale dark currents. Waveguide photodetector (WGPD) quantum efficiency (QE) on the chip is measured to be 58 % for red and 56 % for 785 nm wavelengths. Open eye diagram up to 12Gbit/s was measured as well only limited by characterization setup.

The second part is heterogeneous integration of indium phosphide (InP) PDs and GaAs Schottky diodes (SDs) on silicon-on-insulator (SOI) substrate. This integration aims to harness the superior optical and electrical properties of InP and GaAs within a cost-effective and versatile silicon technology, addressing the demand for high-performance, scalable RF electronic-photonic devices in the communications industry and beyond. The research further proposes a novel method of multilayered integration of dissimilar material systems on a single platform, demonstrating a competitive alternative to the conventional heterogeneous integration methods. This technique is exemplified through the realization and characterization of an on-chip 200 MHz rectifier, showcasing the potential for enhanced performance in sensing, imaging, and RF applications.

Chapter one: Introduction

1.1 Photonic devices

Photonic devices play a crucial role in modern technology from telecommunications and computing to sensing and medical diagnostics. They leverage the principles of photonics, the science of light generation, modulation, and detection, to perform functions that were traditionally achieved using electronic components. What follows is an overview of the applicable devices that are employed in this research.

Photodetectors: devices that convert light into an electrical signal. They are essential for optical communication systems, allowing for the detection of light signals transmitted through optical fibers. Semiconductor photodetectors vary in material, design, and operating wavelength bandwidth including PIN, modified uni-traveling carrier (MUTC), and avalanche photodiodes (APDs). Integrated photodetectors utilizing group IV (such as silicon) and group III-V (such as GaAs and InP) semiconductors are discussed for their ability to generate electron–hole pairs under light exposure [1]. Other recently emerged material like perovskite materials have been shown as promising semiconductors for photodetector applications, offering excellent light absorption, charge carrier mobility, and tunable bandgap [2].

Lasers: sources of coherent light used in a wide range of applications, from optical data transmission to precision manufacturing and medical procedures. Most commons are Fabry-Perot (FP), multiple quantum well (MQW) lasers and vertical-cavity surface-emitting laser (VCSEL) [3].

Optical Amplifiers: devices that amplify an optical signal directly, without the need to convert it to an electrical signal. Erbium-doped fiber amplifiers (EDFAs) for 1550nm

wavelength and semiconductor optical amplifiers (SOAs) are extensively used in long-haul optical communication systems to boost signal strength [4].

Modulators: devices that modulate a property of light, such as its intensity, phase, or polarization, in response to an electrical signal. Electro-optic modulators such as Mach-Zehnder modulators are crucial for encoding data onto an optical carrier in communication systems [5].

Waveguides: Structures that guide light waves from one point to another, serving as the backbone of integrated photonic circuits and optical communication systems. SOI technology is widely used to fabricate telecom photonic waveguides [6].

Optical Fiber: Optical fibers transmit light over long distances with minimal loss, enabling high-speed internet and telecommunications. The technology relies on total internal reflection to confine light within the core of the fiber [7].

1.2 Importance of GaAs and InP in RF-Photonics

GaAs and InP are two semiconductor compounds that play integral roles in the field of RF photonics due to their unique electrical and optical properties.

GaAs has a direct bandgap, which makes it highly efficient for emitting light. This property is crucial for the design and operation of visible range photodetector, lasers, light-emitting diodes (LEDs), and other optoelectronic devices, the spectrum that GaAs is special for [8]. It has higher electron mobility than silicon, allowing for faster electron transport. This makes GaAs devices capable of operating at higher frequencies, which is beneficial for high-speed communication systems [9]. GaAs also serves as a substrate for the epitaxial growth of other semiconductor materials. This is essential for creating high-quality heterostructures used in advanced optoelectronic devices [10].

InP optical properties are suited for use in the near-infrared to the mid-infrared spectrum, making it ideal for long-wavelength lasers and photodetectors used in fiber-optic

communication systems [11]. InP and its lattice-matched compounds also has direct bandgap makes it suitable for a variety of applications in RF-photonics [11]. It is compatible with a wide range of III-V semiconductor materials, facilitating the integration of various optoelectronic functions within a single chip. This is crucial for developing complex PICs.

Integrating InP PDs and GaAs mm-wave SDs can leverage the application of PICs with low loss fiber and large bandwidth into RF and mm-wave systems such as in wireless communication, local oscillator (LO) distribution for large phased arrays, sub-THz spectroscopy, and mm-wave imaging.

1.3 Fabrication challenges of semiconductor devices

Integrating and bonding different epitaxial layers on the same substrate poses several technical challenges that stem from the need to achieve high-performance, reliable, and efficient devices. These challenges are critical to address the successful development of advanced optoelectronic systems. Some of the main challenges includes:

Material Compatibility

Lattice mismatch: the integration of different semiconductor materials often involves lattice mismatch issues, which can lead to strain and dislocations within the epitaxial layers. These defects can degrade the performance of photodetectors by reducing carrier mobility, increasing recombination rates, and causing bonding difficulties.

Thermal expansion coefficient difference: different materials expand at different rates when heated. This difference can cause significant stress and even cracking of the epitaxial layers during the bonding process or subsequent thermal cycling in operation.

Bonding Techniques

Interfacial quality: achieving a high-quality interface during the bonding process is crucial for device performance. Contaminants, oxides, and other surface irregularities can lead to

poor bonding strength, increased interface resistance, and defects that impair device functionality.

Thermal budget management: the bonding process often requires careful management of the thermal budget to prevent damage to the epitaxial layers and maintain the integrity of the device structure. Excessive heat applied through processes like rapid thermal annealing (RTA) can lead to diffusion and debonding problems, altering the material properties and device performance.

Process Integration

Complexity of multistep processes: integrating multiple photodetector structures on the same substrate involves complex multistep fabrication processes. Each step needs to be precisely controlled to avoid damaging previously fabricated structures, which can be challenging given the different processing conditions required for various materials.

Alignment accuracy and undercuts: for devices that are requiring precise alignment of different epitaxial layers or structures, achieving the necessary alignment accuracy is a challenge. Misalignment can lead to suboptimal optical coupling, reduced efficiency, and even device failure. Wet etching undercuts on the other hand leads to low yield.

1.4 Main concepts exploited in this research

1.4.1 Transfer length method

The transfer length method (TLM) is a widely used technique to measure the specific contact resistivity and the transfer length (the distance over which the carrier density falls to 1/e of its value at the contact edge) of metal-semiconductor interfaces [12]. This method is important for optimizing device performance, especially in devices where contact resistance significantly impacts overall functionality. I used this method to determine the total series resistance of our devices due to its impact on RC-limited bandwidth.

Fundamentals of TLM

TLM involves fabricating a series of test structures with varying spacing between metal contacts on a semiconductor substrate. By measuring the resistance between contact pads as a function of their separation, TLM allows for the extraction of the specific contact resistivity (ρ_c), the transfer length and, the sheet resistance (R_{sh}) of the semiconductor.

Measurement of contact resistivity

Contact resistivity is a critical parameter in semiconductor devices, influencing both the efficiency and speed of electronic and optoelectronic components. High contact resistivity can lead to significant power loss and heat generation. TLM provides a straightforward means to quantify ρ_c, enabling the identification and optimization of metallization and annealing processes to minimize contact resistance.

Determination of transfer length

The transfer length (L_t) is another vital parameter measured by TLM, indicating the distance over which the majority of the current transitions from the metal contact into the semiconductor. This parameter becomes of prime importance if the current enters the contact from the lateral side.

TLM's ability to provide direct measurements of contact resistivity and transfer length makes it an invaluable tool for the iterative process of device fabrication optimization. By correlating TLM measurements with changes in fabrication parameters (e.g., metal types, annealing temperatures, and doping levels), one could refine the processes to achieve the best possible device performance. Lower contact resistivities and optimized contact geometries contribute to faster device operation, lower power consumption, and improved thermal management. Figure 1-1 shows the TLM pad structure. By measuring the resistance between the two adjacent pads and plotting vs the distance I achieve to Figure 1-2 which gives us the contact and sheet resistivity parameters.

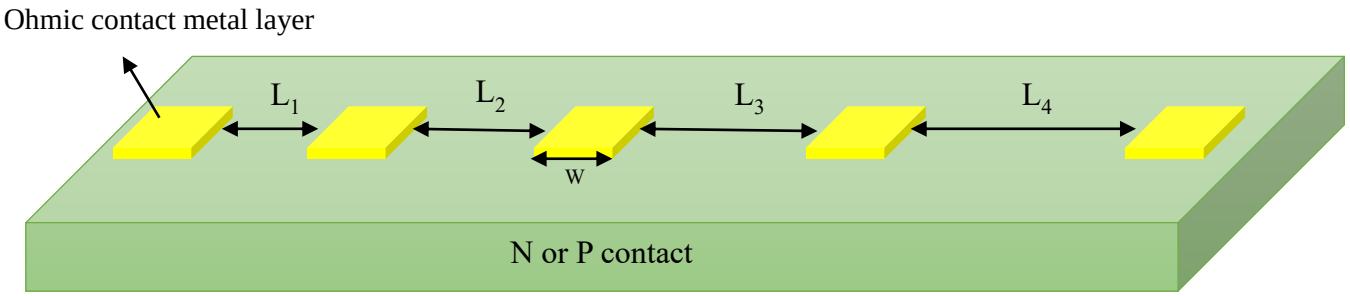


Figure 1-1. TLM structure to measure specific contact resistivity.

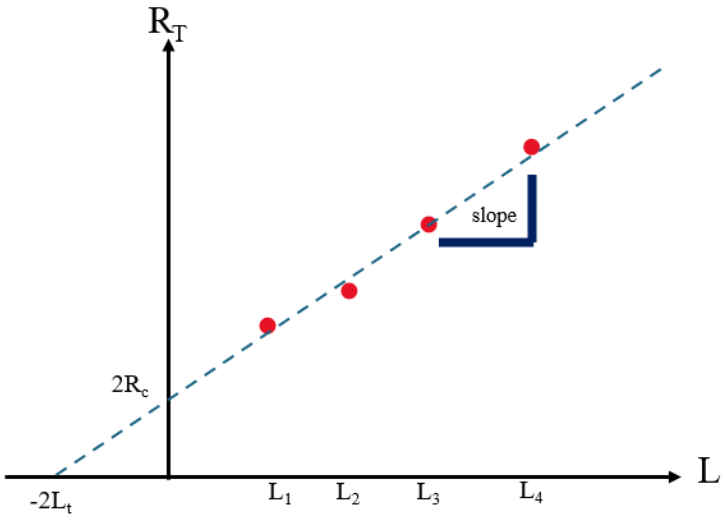


Figure 1-2. TLM plot to assign the transfer length and contact resistivity.

Depending on R_c and L_t values, I can calculate the specific contact and sheet resistivity using equation 1.1 & 1.2 [13]:

$$\rho_c = R_c \times W(\text{pad width}) \times L_t \quad (1.1)$$

$$\rho_{sheet} = \text{slope} \cdot W \quad (1.2)$$

Once I calculate the specific resistivities, I can calculate the actual ohmic and sheet resistance depending on the structure of our devices.

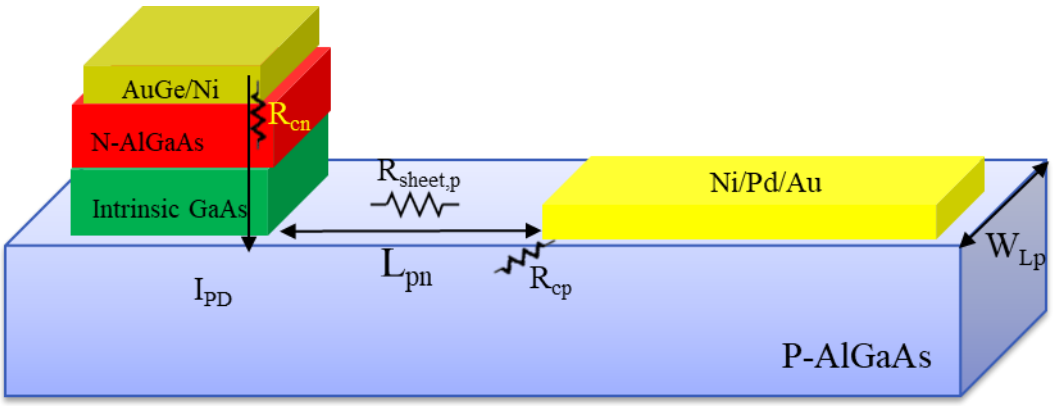


Figure 1-3. Schematic of different components of the PD series resistance.

If the current flows vertically into/from the surface of the contact, I don't need to consider the transfer length (L_t). Equations (1.3)-(1.5) give us the ohmic contact and sheet resistivity for n and p-contacts in which W_p and L_p denote the width of the p-type ohmic contact and the distance between the edge of the p-type ohmic contact and the n mesa, respectively (Figure 1-3). In our case since the p- contact is down, $A_{active,n}$ is the whole n-metal area while $A_{active\ p}$ is $L_t \times W_p$ since the p-contact is laterally oriented (Figure 1-3):

$$R_{cn}=\frac{\rho_{cn}}{A_{active\ n}} \tag{1.3}$$

$$R_{cp}=\frac{\rho_{cp}}{A_{active\ p}} \tag{1.4}$$

$$R_{sheet,p}=\rho_{sheet,p}\times(L_p/W_p) \tag{1.5}$$

Therefore, the total device resistance for RC-limited calculation is $R_{total}=R_{cn}+(R_{cp}+R_{sheet,p})/2+R_L(50\Omega)$. Using parallel plate model, I can calculate the junction capacitance of the devices of various dimensions:

$$C_j = \frac{\varepsilon_d A_{n\_contact}}{d_{abs}} \tag{1.6}$$

In which d_{abs} is the absorption layer thickness and ε_d is the dielectric constant of GaAs and $A_{n\_contact}$ is the area of the n-contact layer. The bandwidth of photodetectors can be limited by two primary factors: RC and transit-time limitations. RC limiting refers to the bandwidth limitation imposed by the PD's junction capacitance (C_j) and total series

resistance including the load resistance (R_{total}), forming an RC low-pass filter. The RC-limited bandwidth (f_{RC}) can be approximated by the inverse of the RC time constant:

$$f_{RC} = \frac{1}{2\pi R_{total} C_j} \quad (1.7)$$

Transit-time limitation, on the other hand, arises from the finite time it takes for the photo-generated carriers (electrons and holes) to travel through the PD's depletion region.

Carrier mobility is the speed at which carriers can move through the semiconductor material impacts the transit time. Higher mobility and velocity lead to shorter transit times.

The thickness of the depletion region which in PIN case is only the absorption region that is depleted and directly affects the transit time. Thinner absorption layers can reduce the transit time, potentially increasing the bandwidth. The transit-time limited bandwidth can be calculated using equation (1.8) [14]:

$$f_{\tau} = \frac{0.45v}{d_{abs}} \quad (1.8)$$

In which v is the average carrier drift velocity in the PIN junction. The total bandwidth of the device can be obtained using equation (1.9):

$$f_{total} = \sqrt{\frac{1}{f_{\tau}^2} + \frac{1}{f_{RC}^2}} \quad (1.9)$$

1.4.2 Schottky diode theory

The Schottky diode, named after German physicist Walter H. Schottky, is distinct from the standard PN diode due to its metal-semiconductor junction. This diode is also known by several other names, including Schottky barrier diode, hot carrier diode, and low voltage diode, reflecting its unique characteristics and applications.

SDs are widely used in electronic circuits and applications, including:

- Voltage clamping: to protect circuits from overvoltage conditions.

- Power rectification: in power supplies, due to their efficiency in converting alternating current (AC) to direct current (DC).
- RF applications: due to their fast-switching speed, they are suitable for use in mixers and detectors in radio frequency applications.
- Solar cells and photovoltaic panels: to prevent reverse current flow and enhance efficiency .

Current-voltage (I-V) relationship:

The I-V relationship of an SD can be described by the thermionic emission theory, given by:

$$I = \underbrace{A^* T^2 e^{-\frac{\Phi_B}{k_B T}}}_{I_S} \left(e^{\frac{qV}{nk_B T}} - 1 \right) \tag{1.10}$$

where:

I is the diode current,

I_S is the reverse saturation current,

A^* is the Richardson constant, which depends on the effective mass of the charge carriers and the area of the junction,

Φ_B is the barrier height,

q is the charge of an electron (approximately 1.6×10^{-19} C),

V is the applied voltage across the diode,

n is the ideality factor, typically close to 1 for Schottky diodes,

k_B is Boltzmann's constant (1.38×10^{-23} J/K),

T is the absolute temperature in Kelvin.

Reverse saturation current (I_S) is a very small current that flows through the diode when reverse biased. SDs typically exhibit a forward voltage drop (V_F) of about 0.2 to 0.6 volts, significantly lower than that of silicon PN-junction diodes. This is attributable to the metal-semiconductor junction, which requires less energy to allow current flow.

Ideality factor (n) accounts for the deviation from the ideal diode behavior, which is usually close to 1, indicating that how closely the I-V characteristics follow the theoretical

prediction. The diode's current is also influenced by temperature, as indicated by the T in the exponential term. Higher temperatures increase the diode current for a given voltage.

1.4.3 Responsivity

The responsivity of a waveguide PD is an essential parameter that measures the efficiency with which the device converts incident light into an electrical current. It is typically expressed in units of amperes per watt (A/W), indicating the amount of photocurrent generated per unit of incident optical power.

For waveguide-coupled PDs, the measurement of responsivity involves directing a known amount of optical power at the operational wavelength into the device and measuring the generated photocurrent. The external responsivity (R) is calculated using the formula:

$$R = \frac{I_{ph}}{P_{in}} \tag{1.11}$$

where I_{ph} is the photocurrent and P_{in} is the incident optical power. To calculate the external quantum efficiency (EQE) (η) from the responsivity (R) of a PD, we can use the relationship between quantum efficiency, responsivity, and the wavelength (λ) of the incident light. This relationship is often given by the equation (1.12):

$$\eta = R\frac{hc}{\lambda e} \tag{1.12}$$

R is the responsivity
η is the quantum efficiency
λ is the wavelength of the incident light
h is Planck's constant
c is the speed of light
e is the elementary charge

This equation expresses the quantum efficiency as a function of the PD's responsivity, the wavelength of the incident light, and fundamental constants. It shows that quantum efficiency can be derived if the responsivity of the photodetector at a specific wavelength is known.

Based on equation (1.12), the max responsivity (for 100% QE) of a PD at 635 nm and 780 nm are 0.512 A/W and 0.629 A/W respectively.

1.4.4 PIN Fundamentals

In a PIN PD, the contact layers (P and N layers) and the absorption layer (intrinsic, I layer) play critical roles in the device's functionality and performance. Each layer has distinct functions that contribute to the efficient conversion of incident light into an electrical signal. The primary function of the contact layers in a PIN PD is to collect the carriers generated by photon absorption in the intrinsic layer. In reverse bias, the p-type layer collects holes, while the n-type layer collects electrons. The contact layers, when doped and combined with the intrinsic layer, contribute to the formation of an electric field across the intrinsic layer. This electric field is crucial for the separation and drift of photogenerated electron-hole pairs towards their respective electrodes, minimizing their recombination within the device.

The contact layers also provide ohmic contacts to the external circuit, ensuring efficient charge transfer from the PD to the external load without significant resistance. The intrinsic layer is the heart of the PIN PD, where the absorption of incident photons occurs. This layer is deliberately made thick enough to absorb a significant portion of the incoming light, leading to the generation of electron-hole pairs. The intrinsic layer's undoped (or lightly doped) nature extends the depletion region formed between the P and N layers, across which an electric field is established.

The operational principle of a PIN PD can be understood through a combination of semiconductor physics and basic electronic principles as follows:

1. Photon absorption:

When photons with energy greater than or equal to the bandgap energy (E_g) of the semiconductor material hit the intrinsic region of the PIN PD, electron-hole pairs are generated.

Photon Energy(E photon)≥Eg

2. Carrier generation:

The number of electron-hole pairs generated (n_{eh}) is proportional to the incident photon flux (Φ) and the quantum efficiency (η), which represents the effectiveness of the PD in converting incident photons into electron-hole pairs:

$$n_{eh}=\eta\cdot\Phi \tag{1.13}$$

3. Charge collection:

Under the influence of an external reverse bias voltage (V_{bias}), the generated electrons and holes are quickly separated and collected at the n-type and p-type regions, respectively. This flow of charge carriers generates a current (I_{photo}) through the external circuit.

4. Photocurrent calculation:

I_{photo} can be calculated from the electron charge (e), the number of generated electron-hole pairs (n_{eh}), and the illumination time (t) or the rate of photon arrival.

$$I_{photo} = n_{eh} \cdot e/t \tag{1.14}$$

Given that the photon flux (Φ) is often given in terms of power ($P_{incident}$) and the energy of a single photon ($E_{photon}=h\cdot\nu$), where h is the Planck's constant and ν is the frequency of the light, we can express n_{eh} as:

$$n_{eh} = \frac{\eta P_{incident}}{\nu h} \tag{1.15}$$

Therefore, substituting n_{eh} into the photocurrent equation gives:

$$I_{photo} = \frac{\eta\cdot P_{incident}\cdot e}{h\cdot\nu} \tag{1.16}$$

5. Responsivity:

In surface-normal illuminated PDs there is a tradeoff between transit-time limited bandwidth and responsivity regarding the absorption thickness to design a high-speed PIN while getting a reasonable responsivity. This is also one of the reasons I use WGPD.

1.5 Characterization techniques

I used three methods for RF characterization of our PDs.

1.5.1 Heterodyne setup

The heterodyne setup, often employed in the context of optical communications, RF engineering, or signal processing to measure the opto-electrical bandwidth of devices. It is a system designed to mix two different frequencies to produce new frequencies, namely the sum and difference of the original frequencies. This technique is widely used for frequency conversion, signal detection, and modulation/demodulation processes.

In a typical optical heterodyne setup, two light sources of slightly different frequencies (f_1 and f_2) are combined, usually using a beam splitter or optical combiner. The mixed signal is then directed onto a PD, which converts the optical signals into electrical signals. Due to the nonlinear response of the PD, it generates an electrical signal at the difference frequency ($| f_1 - f_2 |$), which is easier to process and analyze compared to the original high optical frequencies. One of the drawbacks of this method is that the free running lasers usually being employed in this setup sometimes cause instability which will lead to losing the max modulation depth in the middle of measurement.

1.5.2 Electro-optical modulator setup

In this method I'm using an EO modulator to modulate the light at the desired frequency and couple it to the PD to assess the devices' high-frequency performance. The advantage of this method is that the max modulation depth is achievable easier specially at lower

frequencies compared to the heterodyne setup so the signal quality is higher while heterodyne setup can cover wider frequency range.

1.5.3 Optical pulse measurement setup

In optical communication, we use short optical pulses to assess the devices' transient time performance. In addition to the cost of an appropriate pulse source with enough power specially in visible range, the calibration process for such setup involves a high level of uncertainty as every component in the setup adding some delay (signal phase change) and loss (signal amplitude change) to the transient parameters of the device under test which needs to be taken into account to get the correct PD pulse response.

Table 1. Comparison of different RF-photonics characterization techniques.

	Advantage	Disadvantage
Heterodyne Setup	- Covers a wide range of frequency	- If lasers are free-running, amplitude response only; the detected RF signal frequency and phase will vary over time.
Modulator Setup	- Higher signal quality - Max modulation depth is easier to achieve at lower frequencies. - Both amplitude and phase responses are possible	- Limited frequency range specially at visible range - Drifting of V_π point - Modulator frequency response needs to be known for calibration.
Optical Pulse Technique	- Real time analysis of the device response is possible. - Both amplitude and phase responses are possible	- Ultra short pulse source for visible light is needed. - Calibration of amplitude and phase is challenging

Table 1 compares these three techniques and I'm going to explain each method in detail in the subsequent chapters.

1.6 The outline of the thesis

The structure of this dissertation is as follows:

In the first chapter, I discussed the basic concepts I used in this research.

In the second chapter, I will talk about the design and the fabrication process of GaAs PD on tantala platform. I will discuss the process development and the fabrication challenges and how they may affect the performance of the devices.

In the third chapter, I will present the measurement results of the fabricated PIN presented in the first chapter including DC and RF characterization results, QE measurement and eye diagrams of the devices.

In the fourth chapter, I will propose a novel method of multilayered vertical integration of two devices of dissimilar material systems on the same platform which is a competitive alternative for the existing conventional method of hybrid integration. As the proof of the of the new technique, I will realize an on-chip 200MHz rectifier, implement it using the proposed method and characterize it.

The last chapter will provide the conclusion and the future works.

Chapter Two: GaAs PIN photodetector on Tantala Waveguide

2.1 Motivation

PICs have enabled the demonstration of transformative optical microsystem concepts. Most PICs have been developed at telecom (1300 nm and 1550 nm) as of today and they've been less explored for shorter wavelengths. One reason would be SOI waveguides, as silicon materials are not transparent at visible wavelengths. Nevertheless, the material limitation of today's available technologies poses challenges in delivering all requisite optical components concurrently for diverse commercial and defense applications, thereby impeding the realization of chip-scale solutions. To surmount this limitation, imperative advancements involve the utilization of technologies based on heterogeneous integration of state-of-the-art materials. The objective is to cultivate comprehensive integrated photonics platforms that combine efficient optical gain, high-speed modulation and detection, and low-loss passive functionality onto a single substrate. The complete integration of high-performance elements such as lasers, amplifiers, modulators, waveguides, isolators, and photodetectors hold promise for compact solutions endowed with unprecedented functionality across various applications. The focus of this research pertains to the design, fabrication, and characterization of GaAs/ aluminum gallium arsenide (AlGaAs) PDs on tantala waveguide platform. The tantala waveguide presents distinctive advantages, including low optical loss comparable to silicon nitride (Si_3N_4) waveguides, CMOS compatibility, high dielectric permittivity, high refractive index (>2) facilitating robust mode confinement, negligible two-photon absorption relative to silicon, a considerably broader band transparency spanning from

ultraviolet (320 nm) to mid-infrared (IR) wavelengths, high third-order nonlinearity enabling harmonic generation through nonlinear processes such as four-wave mixing and frequency comb generation, low mechanical stress, and exceptional temperature stability attributable to a record-low thermo-optic coefficient which permits the application of high optical power without inducing excessive considerations due to thermal effects [15, 16, 17].

Only recently, initial work has been done on the integration of indium gallium arsenide (InGaAs) laser on tantala platform [18], and to expand the tantala platform's functionality, I have developed heterogeneously integrated AlGaAs/GaAs PDs through adhesive bonding technique on it. In contrast to Si PDs, which have been used for on-chip visible light detection on silicon nitride waveguides [19, 20], our heterostructure PDs can offer notable advantages detailed in the subsequent sections.

2.2 Design

2.2.1 Device design

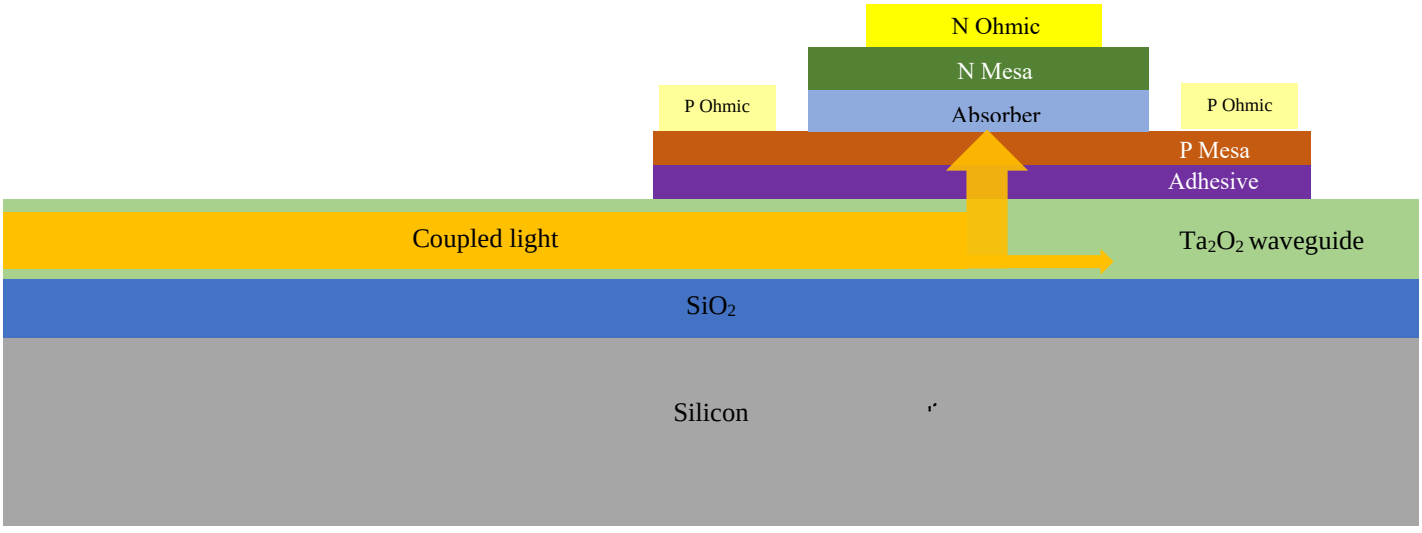


Figure 2-1. Schematic of the WGPD.

To facilitate visible light detection within the envisioned tantala platform, the goal is to develop heterogeneously integrated waveguide PIN PD characterized by low dark

current, multi-GHz bandwidth, and high quantum efficiency. In contrast to the prevalent use of Si homojunction PDs for visible light detection, a heterostructure based on GaAs was employed as an absorber due to its specific advantages aligning with the project objectives. GaAs manifests superior characteristics such as high carrier drift velocities, electron velocity overshoot, a larger absorption coefficient compared to Si [21], and notably, GaAs and its lattice-matched compounds like AlGaAs have cut-off wavelengths spanning from 879 nm to 574 nm, depending on Al compositions, allowing the necessary bandgap engineering. It is noteworthy that GaAs-based materials are frequently leveraged in PIN and Schottky PD operating within the 800—900 nm wavelength range, demonstrating previous success in discrete photodiode implementations featuring high efficiency and bandwidths up to 178 GHz [22]. In my work, the scope of GaAs-based detector technology is expanded to support an integrated heterogeneous photonics platform designed for visible light applications. Figure 2-1 depicts a schematic representation of our design, illustrating the evanescent coupling of light from the waveguide into the active PD region including the narrow-bandgap GaAs absorber sandwiched between AlGaAs contact layers with wider bandgaps.

2.2.2 Tantala waveguide design

Tantala waveguides are fabricated on Si by our collaborator, Octave Photonics, employing ion-beam sputtering (IBS) to support wavelengths ranging from 510 – 800 nm. IBS-coated tantala, whether ion-assisted or reactive, offers distinct advantages over alternative growth techniques like evaporation (Figure 2-2) such as a higher visible refractive index, approximately 2.18, enhancing mode confinement. This is further complemented by low propagation loss, attributed to a recorded extinction coefficient of less than 10^{-4} cm^{-1}, and an energy bandgap of 4.3 eV. These features position IBS-coated tantala as a favorable candidate for the goals of this project, particularly in facilitating efficient evanescent coupling from the waveguide into PDs [23, 24].

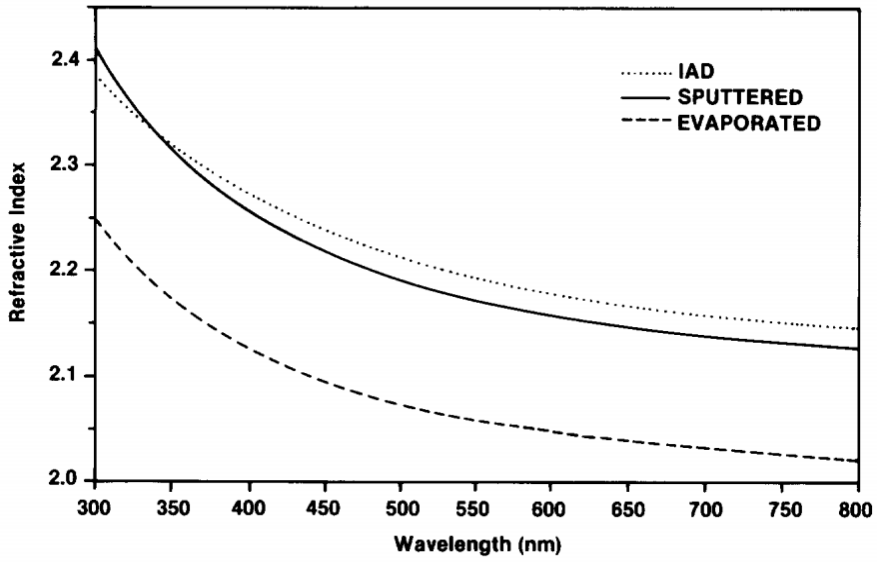


Figure 2-2. Comparison of refractive index of Ta_2O_5 using different growth methods *[23, 24]*.

The tantala waveguides feature air-cladded trench structures with a ridge thickness of 150 nm and a trench width of 2.4 µm. The substrate consists of 650 µm of silicon with an additional 3 µm SiO_2 layer on top. Two sets of waveguides (WG) chips were designed, as illustrated in Figure 2-3 and*Figure 2-4*. The first generation comprises double-ended straight waveguides with variable core widths ranging from 0.2 µm to 5 µm. The second generation is an expanded version, incorporating more PDs and encompassing a broader range of core widths from 2 µm to 30 µm. This second generation also includes "S" bend waveguides for efficient coupling through fiber-in and fiber-out tests. Additionally, there are single-facet tapered trench waveguide structures with PDs positioned on the tapered end. In these structures, the waveguide width narrows (below the fundamental mode cut-off) at the end into the PD active region. This design facilitates the 'squeezing' out of the optical mode from the waveguide. If there is field overlap with the higher index of the PD, the light will couple up into the PD, a phenomenon to be elaborated upon in the assessment of PD responsivity. This is particularly evident when comparing the low loss nature of the same waveguides (as seen in chips 1st and 2nd Gens) to the 780 nm wavelength, where most of the waveguides operate in a single-mode fashion. An interesting observation is that for 10 µm or 20 µm waveguides, PDs exhibit the least

responsivity to both wavelengths, coinciding with the wider waveguides becoming multimode. Figure 2-5 (a) shows the tantala waveguide observed through scanning electron microscopy.

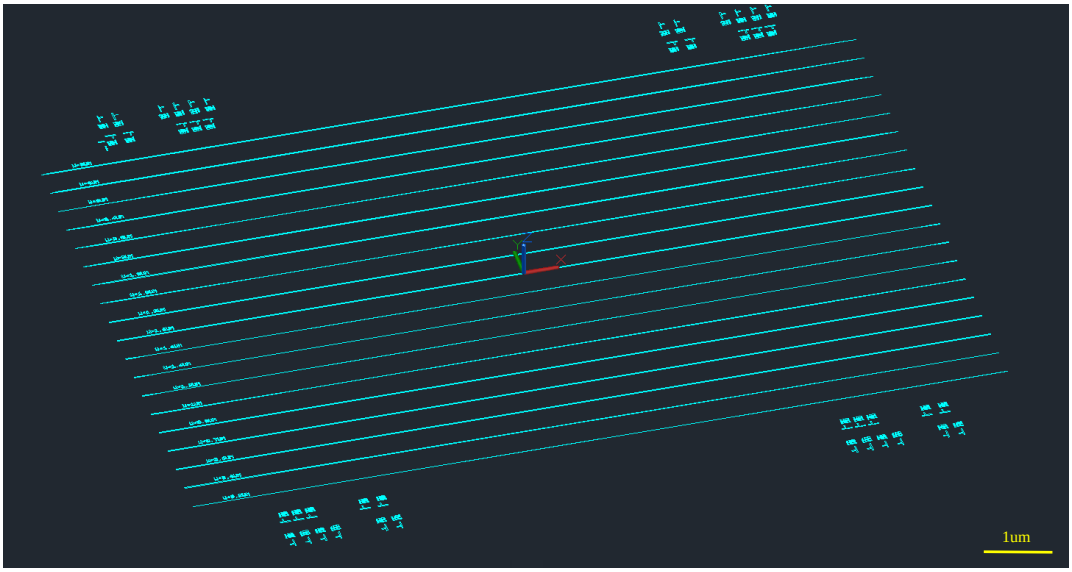


Figure 2-3. First generation of the visible PD mask.

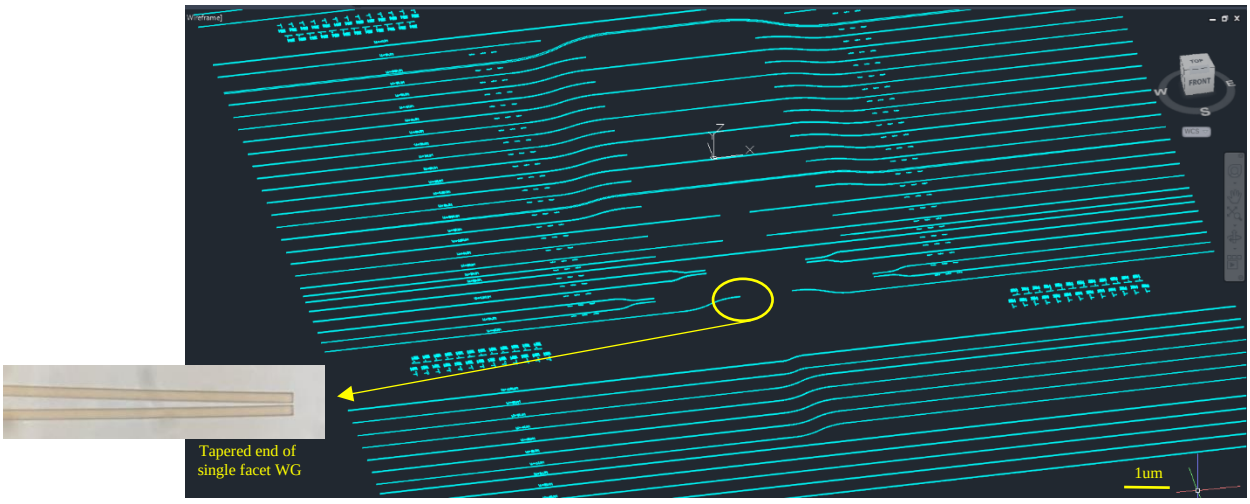
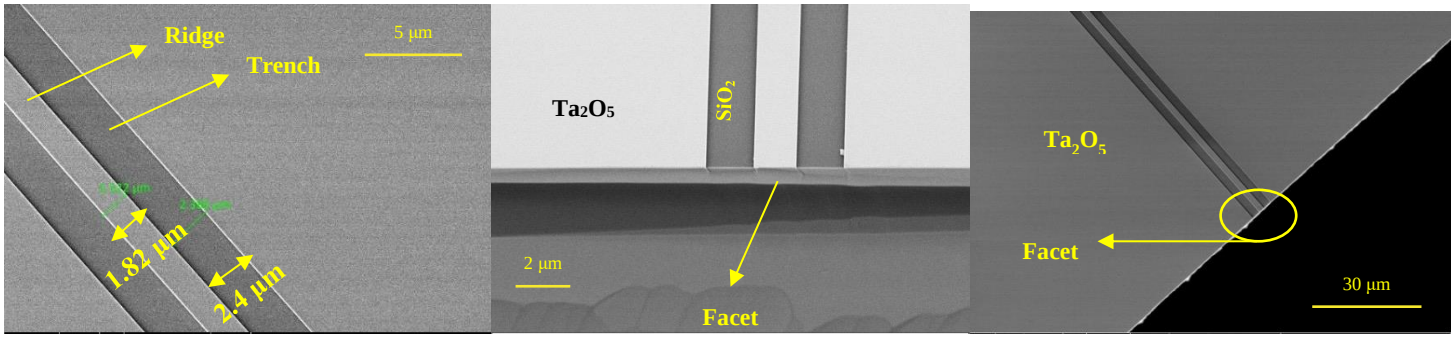
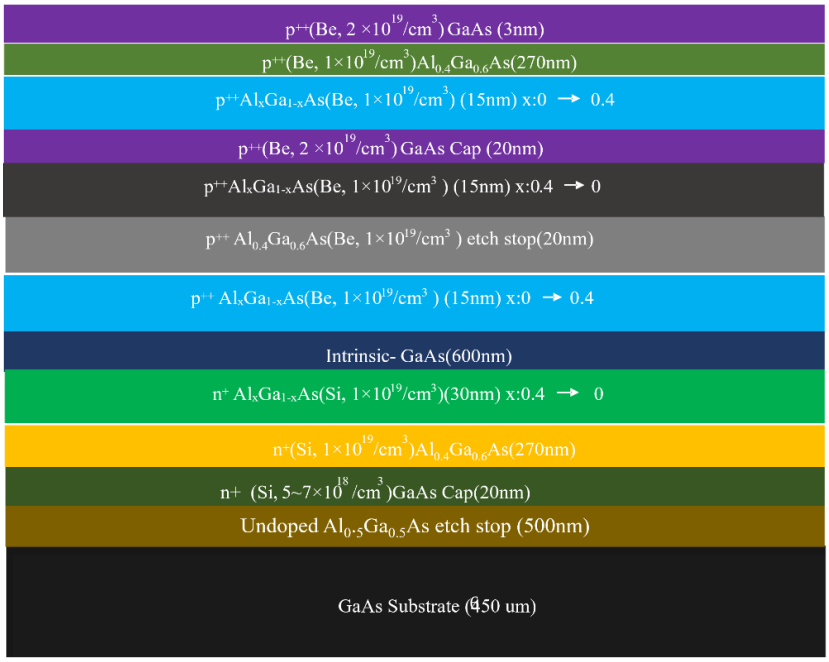


Figure 2-4. Second generation of visible PD mask.



(a)



(b)

Figure 2-5 (a) SEM images of tantala waveguides (b) Epitaxial structure of the designed photodetector.

2.2.3 Epitaxial layer design

The photodiode epitaxial layer stack, as illustrated in Figure 2-5(b), was grown through molecular beam epitaxy (MBE) by Intelliepi. The substrate possessed a thickness of 650 µm. The epitaxial stack growth initiates with the deposition of a 500 nm $Al_{0.5}Ga_{0.5}As$ etch stop layer on semi-insulating GaAs, serving the purpose of GaAs substrate removal. Subsequently, a 20 nm n_+GaAs cap is applied to minimize the ohmic contact resistivity of the 270 nm n_+ $Al_{0.4}Ga_{0.6}As$ contact layer and to prevent oxidization of Al when exposed to air. The choice of $Al_{0.4}Ga_{0.6}As$ (bandgap wavelength: 646 nm) for the highly doped

contact layers is crucial due to its lattice matching with GaAs, which is essential for minimizing the dark current. Furthermore, it exhibits low absorption at 635 nm, thereby suppressing carrier recombination and slow carrier diffusion. Leveraging the lower refractive index of AlGaAs (3.4~3.6) compared to GaAs (3.7~3.8) (Figure 2-6) these layers also function as optical claddings, aiding in the confinement of light within the GaAs absorption layer.

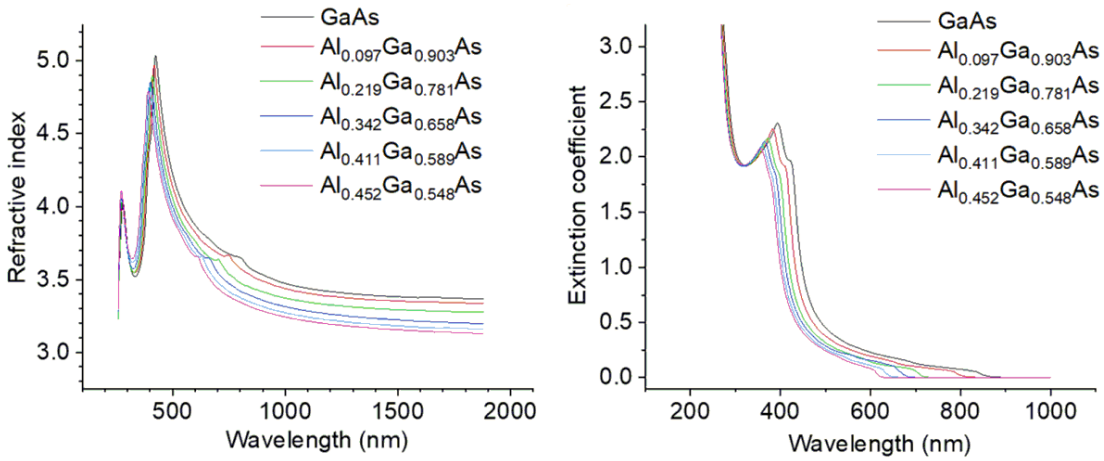
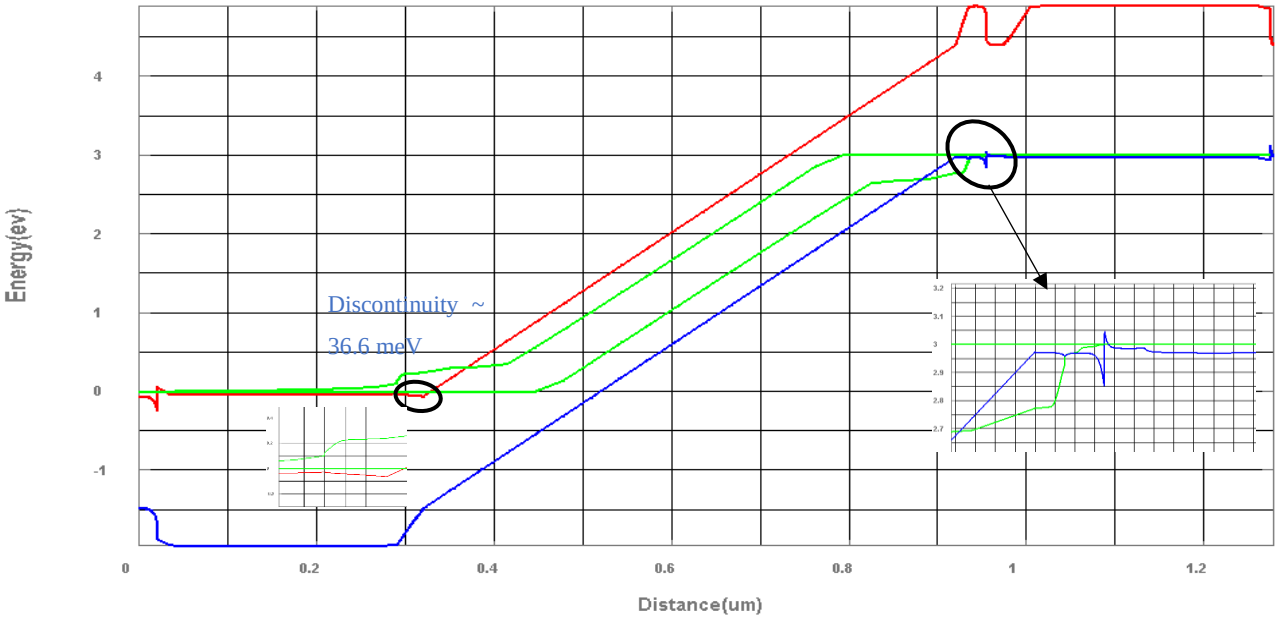


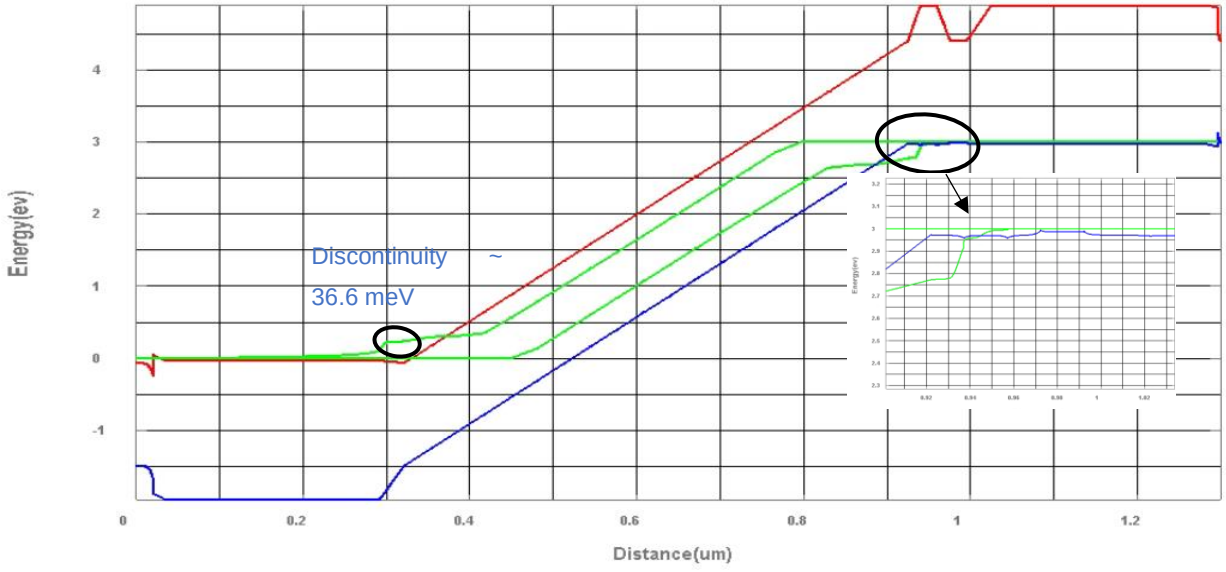
Figure 2-6. GaAs vs AlGaAs optical properties *[25, 26]*.

Compositional graded AlGaAs layers have been introduced to mitigate band offsets at interfaces and enhance carrier transport efficiency (Figure 2-5(b)). These layers are engineered to be thin enough, thereby transparent to coupling light. Notably, the inclusion of a 15 nm $p_{++}Al_xGa_{1-x}As$ layer adjacent to the p-metal contact (depicted in Figure 2-7) has demonstrated a significant reduction in energy band discontinuity from over 100 meV to less than 20 meV as evidenced by simulations conducted in this study. Further structural elements include a 20 nm $p_{++}Al_{0.4}Ga_{0.6}As$ layer, incorporated as an etch stop layer to facilitate proper wet etching. Additionally, a 20 nm $p_{++}GaAs$ cap layer has been introduced to concurrently reduce the ohmic contact resistivity of the 270 nm p_{++} $Al_{0.4}Ga_{0.6}As$ layer and serve as an etch stop for the p contact layer. The architecture is completed with a 3 nm p_{++} top GaAs layer, recommended to cut back the oxidation of the

subsequent p_{++} AlGaAs contact layer. Figure 2-8 shows the cross section of the projected designed photodetector flipped and sit on the center ridge of tantala waveguide.



(a)



(b)

Figure 2-7. Impact of adding 15nm p_{++} AlGaAs grading layer(-5V reverse bias) (a) before adding the layer(b) after adding the layer (credit: T. Fatema).

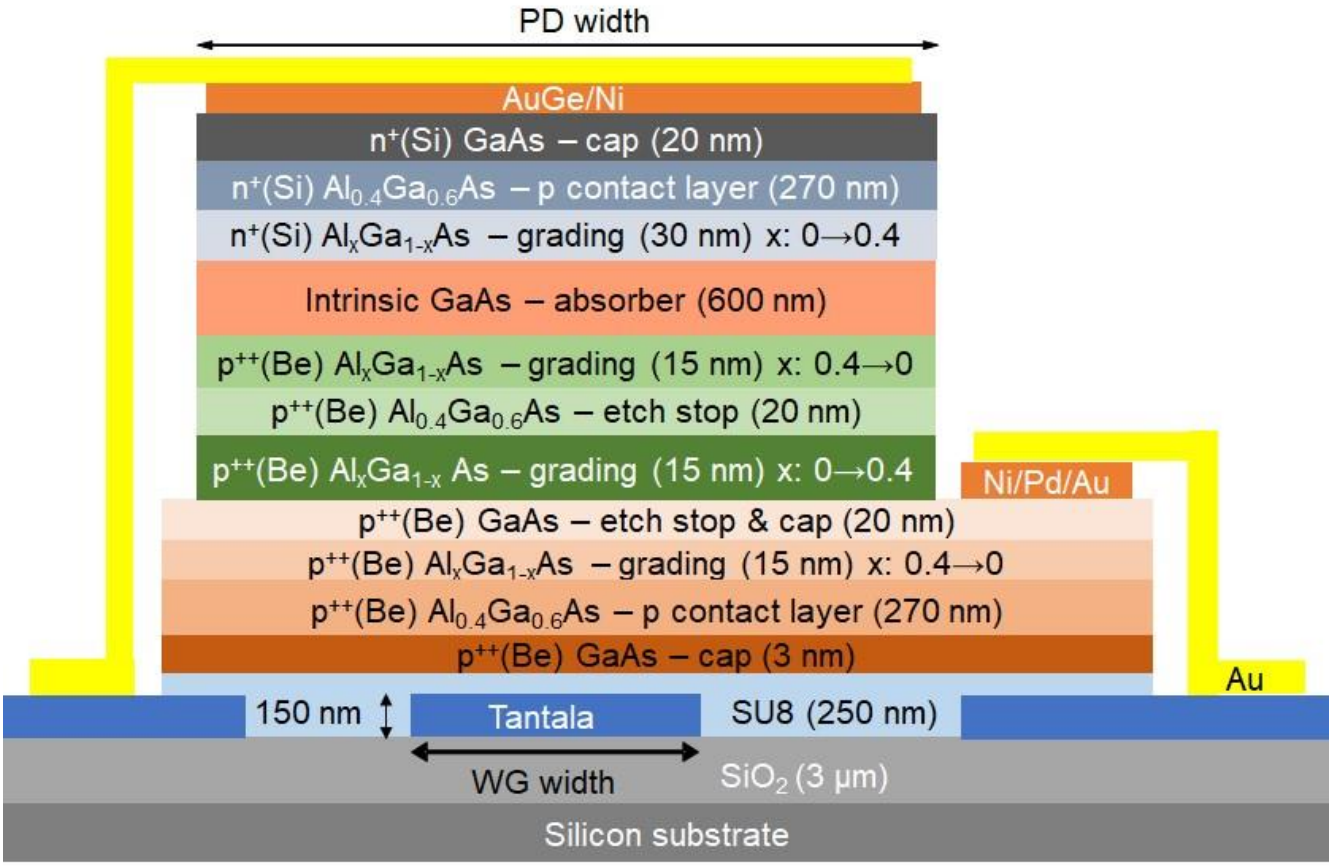


Figure 2-8. Layer stack of the designed photodetector on tantala waveguide.

Evanescent coupling, as employed in this study, stands as a versatile technique, demonstrating applicability for interfacing light transmission between a waveguide and a diverse array of optoelectronic devices, including PDs, lasers, and modulators. In the context of this research, evanescent coupling has been utilized to facilitate the coupling of light from waveguides to photodetectors. The mechanism of evanescent coupling involves the deliberate alignment of the evanescent field overlapping from the waveguide with the PD. The evanescent field, characterized by its non-propagating mode and exponential decay away from the waveguide interface with the device, assumes primary significance in this process.

Various methodologies exist to realize evanescent coupling between a waveguide and PD systems. However, there is a drawback associated with evanescent coupling—its susceptibility to fiber misalignment into the facets, a consideration critical for achieving

high performance. In the specific context of this study, the choice of SU8 as the adhesive agent for bonding the epitaxial layer to the waveguides necessitated the assessment of its optical properties within our designated wavelength range. To address this, an ellipsometry technique was employed on a 450 μm Si substrate, coated with a 400 nm layer of SU8. The results revealed exceptional transparency, exceeding 95 %, coupled with an extinction coefficient of approximately 3.95×10^{-5} over visible wavelengths. This characterization underscores the suitability of SU8 for facilitating evanescent coupling in the devised system. Figure 2-9 shows the measurement results of SU8 ellipsometry which matched the data in SU8 datasheet.

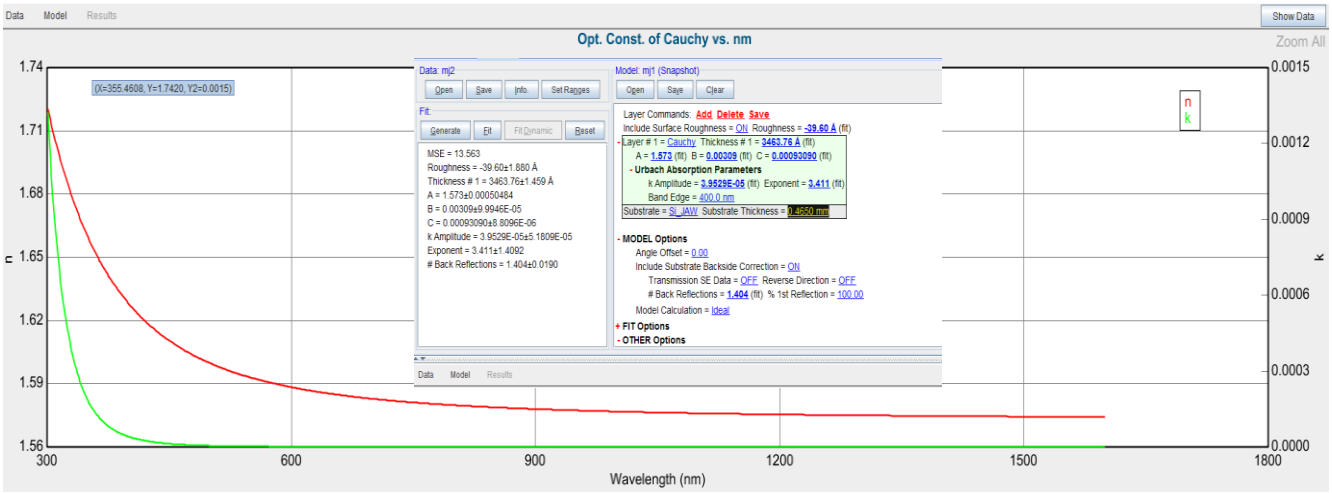


Figure 2-9. Ellipsometry measurement of SU8-6000.5 to find the optical parameters.

2.2.4 Mask Design

The mask layout comprises four principal sections, each serving distinct functionalities in the PD characterization process:

- Rectangular WGPDs (primary devices to be evaluated)
- Circular top-illuminated PDs (employed for assessing the initial DC performance)
- TLMs (designed to ascertain the ohmic contact properties)
- Alignment markers (incorporated for precision in optical lithography)

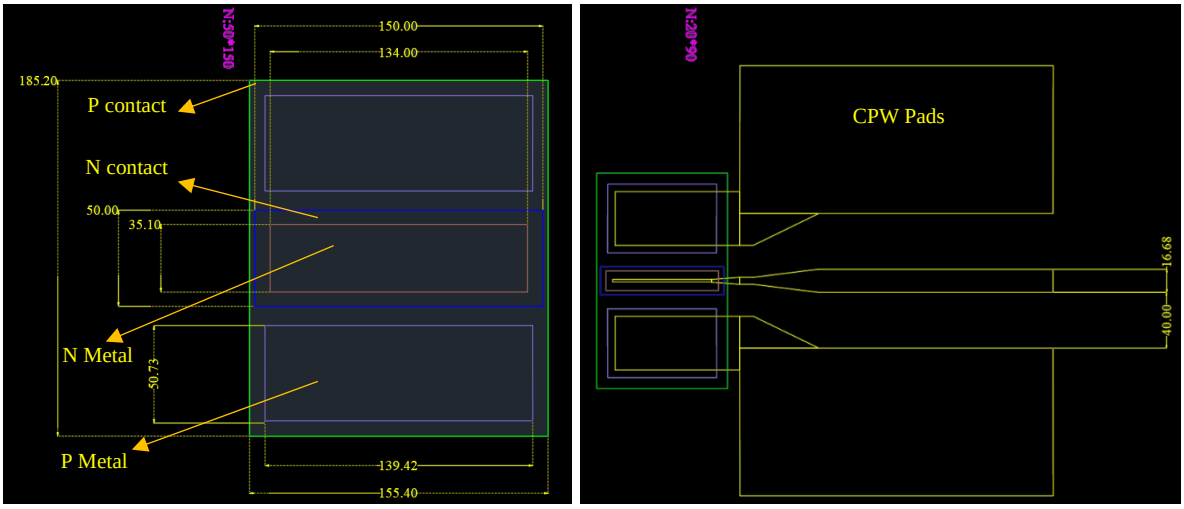
Notably, the direct laser lithography, specifically microwriter technology, was employed throughout the project due to its virtual mask capability which provides superior flexibility in modifying patterns compared to conventional photolithography techniques.

The comprehensive set of mask layers encompasses:

1. N-Mesa
2. N-Metal Contact
3. P-Mesa
4. P-Metal Contact
5. Plating Seed Layer
6. Plating

PD dimensions vary from 10×10 μm² to 50×150 μm² for n-mesa, covering a wide range of PD lengths crucial for assessing quantum efficiency and the maximum RF output frequency range. The mask layout positions two PDs on a double-facet waveguide, allowing optical coupling from either facet. The n-mesas are situated on top of the center ridge of the waveguide, adopting a rectangular shape to optimize responsivity over the n-mesa length. Circular top-illuminated PDs are included for corroborating initial IV results. Design considerations include n-metal contacts with a minimum 5 μm margin to the n-mesa edge to mitigate fabrication errors and p-mesas with a minimum 10 μm margin to the n-mesa, balancing sheet resistivity effects on BW calculations and preventing fabrication errors like undercuts and lithography misalignment.

Figure 2-10(a) details the mask structure of a 50×150 μm² PD, and Figure 2-10(b) illustrates a 20×90 μm² PD with coplanar waveguide (CPW) pads, designed for a 50 Ω characteristic impedance. Figures 2-11 and 2-12 provide top views of the overall mask layers, including tantala waveguides, alignment markers, TLMs, and etching/plating pads. The subsequent section will delve into the specifics of ohmic contact, a critical aspect in the overall fabrication process.



(a) (b)

Figure 2-10.(a) Mask design of 50×150 μm^2 PD (b) 20×90 μm^2 PD with added 50 Ω RF pads.

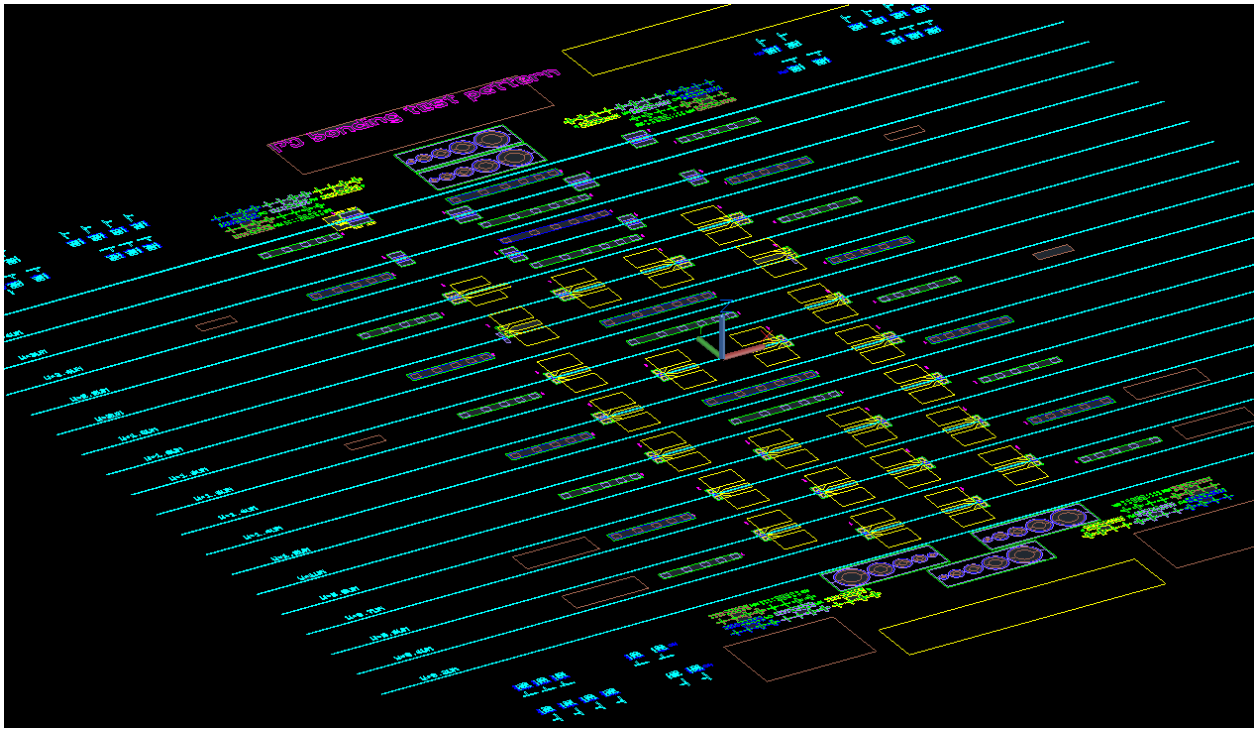


Figure 2-11. Top view of the overall 1st gen mask design including tantala waveguides in cyan.

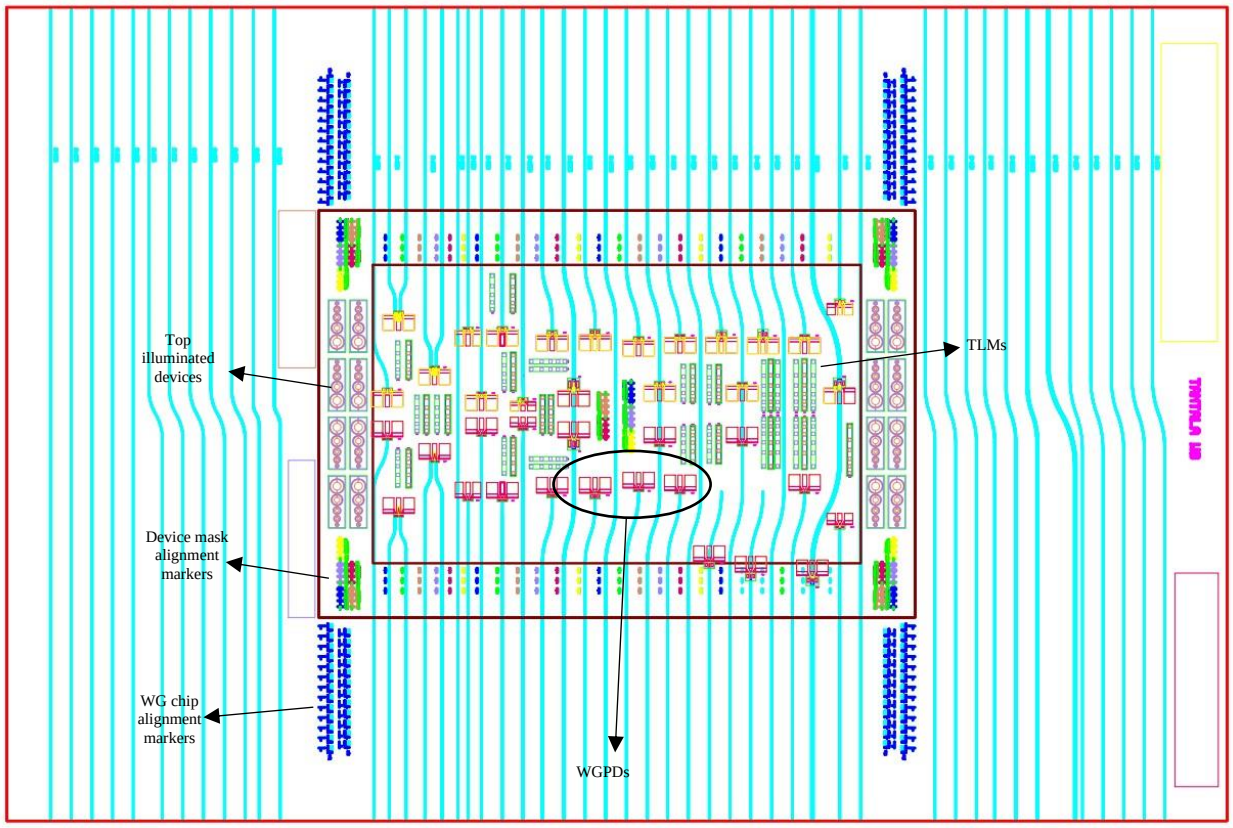


Figure 2-12. Top view of the 2nd Gen mask layout with added devices.

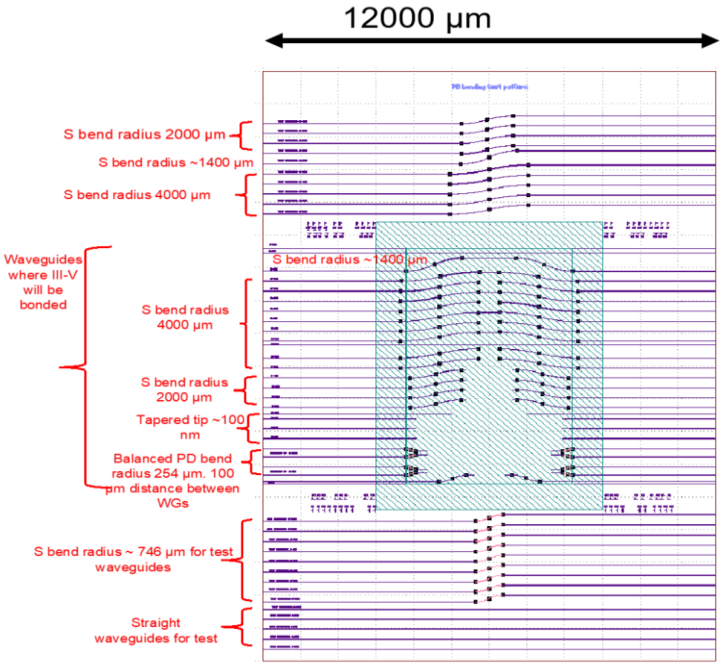


Figure 2-13. Top view of the 2nd Gen chip explaining waveguide sections.

2.3 Ohmic Contacts

In the context of semiconductor devices, establishing ohmic contacts between metal and semiconductor layers is imperative. Low resistance ohmic contacts are crucial, facilitating the carrier transport in both directions. TLM is employed for independent measurements of ohmic contact resistivity, particularly for layers featuring a metal surface. Several techniques exist for achieving robust ohmic contacts, each influencing the doping concentration and Schottky barrier height at the metal-semiconductor interface [21]. The commonly employed methods are as follows:

1. Annealing Au-based alloyed ohmic contact (high temperature): annealing at temperatures within the range of 365°C to 500°C, often accomplished through RTA [21].
2. Depositing a thin highly doped small band gap graded cap layer: particularly advantageous for non-alloyed ohmic contacts [27].
3. Solid phase regrowth-based ohmic contact formation: achieved at lower temperatures, contributing to lower contact resistance [28].
4. Non-Au or limited-au approaches: exhibiting enhanced thermal stability at the cost of higher contact resistance [29].

What's common across these methodologies lies in their impact on increasing doping concentration and/or reducing the Schottky barrier height at the metal-semiconductor interface [21]. The choice between these methods often hinges on the type of material utilized. Increasing doping concentration is a predominant approach in the state-of-the-art industry, achievable through either a direct or indirect approach. The direct approach is maximizing doping concentration to more than occurs during the 10^{19} cm^{-3} semiconductor growth process . Conversely, the indirect approach involves RTA, where annealing the metal-semiconductor system up to the alloy temperature of the metal stack induces carrier diffusion from the metal side to the semiconductor side. Consequently, the doping concentration at the interface is increased, leading to the formation of a thin, transparent barrier for carriers, in which the tunneling occurs as the primary current mechanism in an ideal ohmic contact [30]. Figure 2-14 depicts the dependency of specific contact resistivity on doping concentration for n-GaAs.

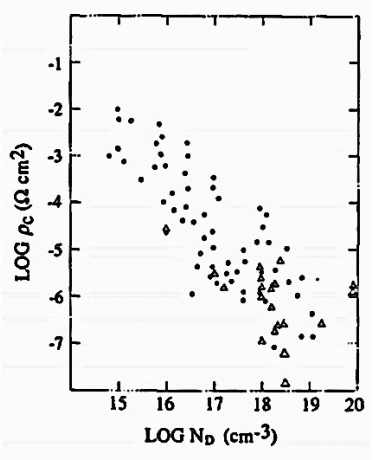


Figure 2-14. Specific ohmic contact resistivity dependency on doping concentration *[31]*.

Table 2 shows the potential candidates for the AlGaAs/GaAs configuration, sourced from existing literature [31]. From the possible configurations presented in the table, I opted for Ni (80 nm)/Pd (120 nm)/Au (200 nm) as the p-type ohmic contact and Ni (56 nm)/AuGe (200 nm) for the n-type ohmic contact. This selection was based on a comprehensive evaluation of various factors, including the need to avoid excessively high temperatures and prolonged annealing durations that could damage the SU8 adhesive layer beneath the PDs, fortunately, a 1-minute annealing at 400°C exhibited no detrimental effects on SU8. Additionally, the feasibility of utilizing the E-beam metal source configuration in the cleanroom played a pivotal role in this decision. Other reasons we chose indirect approach is on difficulties reaching to doping concentration in the range of 10^{19} cm^{-3} for both n and p-GaAs cap layers during growth process. The following sections will explain the details of the TLM parameters associated with the aforementioned ohmic contact.

Table 2. Literature review of the potential ohmic contact candidates for AlGaAs/GaAs epi system.

SemiC Compound	Contact Compound	Anneal Temp(∘C)	Yielded R_c ($\Omega.cm^2$)	SemiC Doping(cm^{-3})
N-GaAs [21]	AuGeNiAu	350-450	10^{-5}~10^{-6}	2×10^{19}(post-anneal) 1×10^{16}~5×10^{17}(Pre-anneal)

N-AlGaAs [32]	Pd/Ge Caps: n-GaAs & n+ GaAs	225–300	1.2×10^{-7}	N-AlGaAs: 2×10^{17} N-GaAs:3×10^{17} N_{+}GaAs:5×10^{17}
P-graded AlGaAs with p_{++} GaAs cap [33]	Ti/Pt/Au Pt/Ti/Pt/Au Pt/Ti/Ni/Au	350 ~400	2.8×10^{-5} $(1.4\sim2.2)\times10^{-5}$ 1.4×10^{-5}	AlGaAs:3×10^{18} P_{++} GaAs:$3\times10^{18}\sim 3\times10^{19}$
P-AlGaAs [34, 35]	Pt/Ti	300~400	$10^{-6}\sim10^{-8}$	$1\times10^{19}\sim1\times10^{20}$
N-AlGaAs [36]	Pd/Ge/Ti/Au	350~400	5.8×10^{-6}	7×10^{16}
P-AlGaAs [37]	Au-Zn	350~400	1.9×10^{-6}	2×10^{19}
N_{+}GaAs(Si-doped) [38]	Pt/Ti	NA	5×10^{-6} 1.3×10^{-6} 1.5×10^{-6}	4×10^{19} 1×10^{20} 2×10^{20}
N_{+} GaAS(Se- doped) [38]	Au/Ge (Ge cap doped with As)	NA	1×10^{-7}	Ge=1.4×10^{20} N_{+}GaAs= 1.5×10^{18}
N_{+} GaAS(Se- doped) [38]	TiPtAu/Ge (Ge cap doped with P)	NA	1×10^{-5}	Ge=1×10^{19} N_{+}GaAs= 1.5×10^{18}
N-$Al_{0.3}Ga_{0.7}As$ [39]	Pd/AuGe/Ag/Au	550	1×10^{-5}	7.3×10^{17}
N-$In_{0.53}Ga_{0.47}As$ (Si-doped) (SPR) [40]	Pd/Ti/Au	400	$2.6\times10^{-8}\pm1.7\times10^{-8}$	5×10^{17}
P_{++} graded AlGaAs with P_{++} GaAs cap [41]	Ni/Pd/Au	300	3.8×10^{-5}	1×10^{19}

To determine the annealing parameters like temperature and duration, the standard TLM structure shown in Figure 2-15 was employed. This structure includes five square pads, each with a width (W) of 50 µm, placed at varying distances from one another. The resistance between adjacent pads was measured using 4-point measurement technique, utilizing a 2400 Keithley multimeter providing 105 µA.

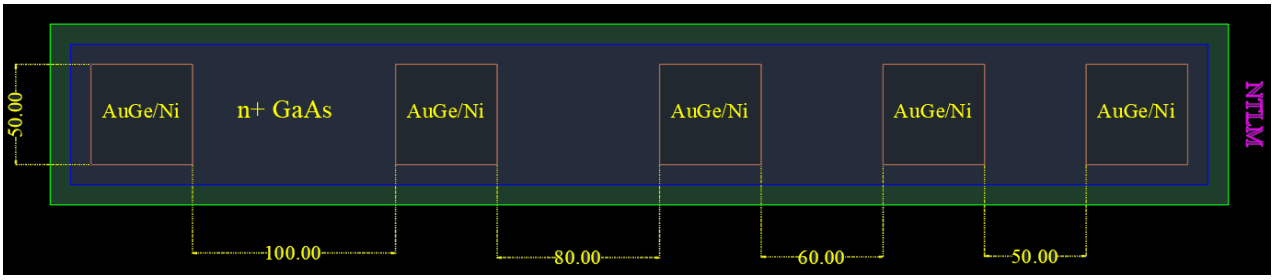


Figure 2-15. TLM structure which designed to measure the N ohmic contact resistivity.

The results of the n-type TLMs (n-TLM) are represented in Figure 2-16. The n-TLM equation featured in the plot provides comprehensive insights into the characteristics of the contact and the sheet resistance. The y-axis intersection gives $2\times R_c$ and the x-axis intersection gives us $-2\times L_t$. The slope of the equation equals to 5.9 multiplied by pad width (w= 50 μm) gives us sheet specific resistivity. Subsequently, ρ_{cn} and $\rho_{sheet,n}$ are determined through equations (1.1) and (1.2) of chapter 1 to be 7.11×10^{-5} Ω.cm^2 and 295 Ω/sq considering 4.9 μm transfer length and approximately 29 Ω contact resistance which is obtained from the line equation of Figure 2-16. The n-sheet resistance could be neglected in our design and the n-contact resistance was of primary importance.

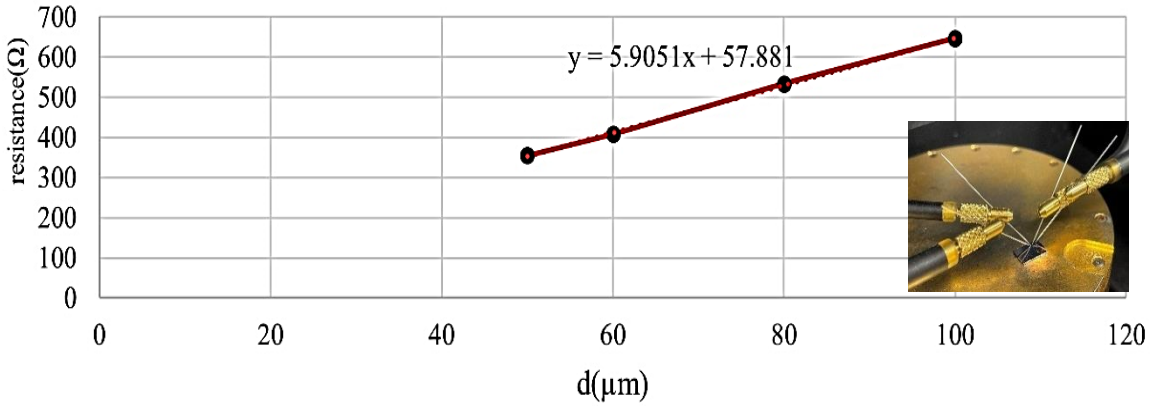


Figure 2-16. TLM measurement of AuGe/Ni n-ohmic contact on n+GaAs (1min 400C RTA).

Regarding the p-type ohmic contact, the Ni/Pd/Au metal stack was employed (Figure 2-17), showing an ohmic behavior through a similar mechanism. The inclusion of Ni in the metal stack serves to mitigate the formation of balling up, while Pd contributes to the favorable morphology of the metal stack. The utilization of Au overlayer atop the stack

has demonstrated efficacy in diminishing the resistivity of the annealed contact. The R_c and L_t that are read from the p-TLM plot (Figure 2-18) equals to 12.67 Ω and 4.4 μm respectively. Similarly, by using equations (1.1) and (1.2) of chapter one, I obtain 2.77×10^{-5} Ω.cm^2 and 144 Ω/sq for ρ_{cp} and $\rho_{sheet,p}$ respectively.

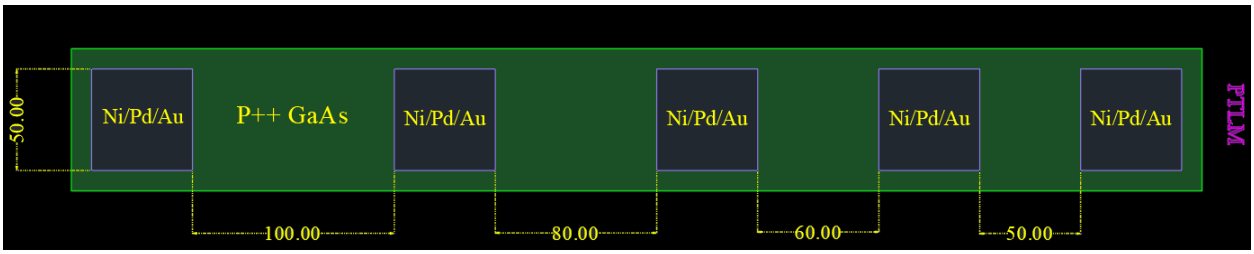


Figure 2-17. TLM structure to measure the p-ohmic contact resistivity.

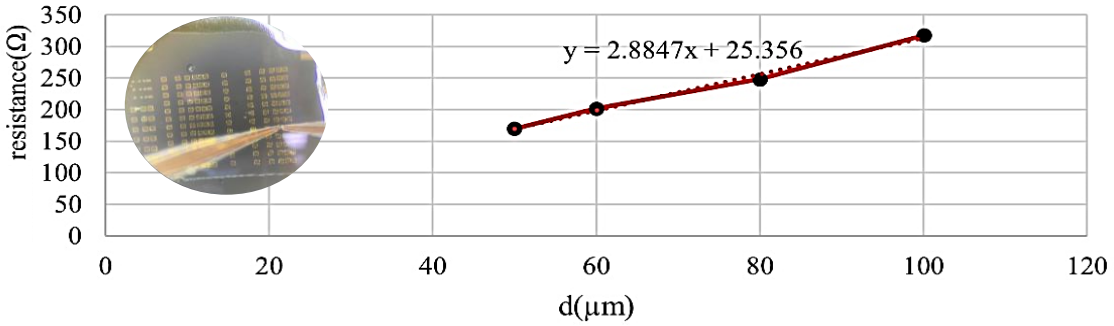


Figure 2-18. TLM measurement of Ni/Pd/Au p-ohmic contact on p_{++}GaAs (1min @ 400C, p_{++} GaAs doping was 2×10^{19} cm^{-3}).

It is worth noting that for the n-type contact, the entire n-metal area is considered as the "active area" in order to calculate the n-contact resistance, given the vertical flow of current from the surface of the n-mesa. Conversely, in the case of the p-type contact, the transfer length (L_t) is factored in to figure out the active area, considering the lateral flow of current into the p-contact. In the pursuit of optimizing temperature and annealing duration, several experiments were conducted that led to the fact that an annealing condition of 1 minute at 400 °C in an N_2 environment is optimal for both n- and p-contacts. In summary, the specific resistance for the n-type contact is established as 7.11×10^{-5} Ω.cm², accompanied by an n_+GaAs sheet resistivity of 295 Ω/sq. Simultaneously, the specific resistance for the p-type contact is shown as 2.77×10^{-5} Ω.cm², corresponding to a p_{++} GaAs sheet resistivity of 144 Ω/sq.

By obtaining the specific contact resistivity for both n- and p-contacts, along with the sheet resistivity for the bulk of p_{++}GaAs, the next step involves the calculation of the RC-limited bandwidth according to equations (1.4) And (1.7). This is achieved by applying these parameter values to photodetectors (PDs) of different dimensions to estimate the RC-limited bandwidth for each PD.

Starting with a PD featuring an n-contact area of 15 × 20 μm² and a p-contact metal area of 4.4×23.2 μm², the actual contact resistivity for both p- and n-contacts is determined by dividing the specific resistivity by the effective area of each contact metal. W_{LP} and L_{pn} (in Figure 1-3) for this specific PD are 10 μm and 38 μm respectively. By using equation (1.3) and (1.5) of chapter one and applying these parameters I obtained R_{cn}, R_{cp}, $R_{sheet,p}$ of 87.7 Ω, 27.15 Ω and 37.6 Ω respectively for this device which gives R_{tot} of 170 Ω in case of 50 Ω load. Also, by using equation (1.6) for junction capacitance for this case with GaAs absorption layer of dielectric constant of 12.9 and 600 nm thickness, we have 57 fF junction capacitance for this specific device which gives us a total RC-limited bandwidth of 16.4 GHz by applying equation (1.7). It's worth mentioning that for C_j approximation using equation (1.6) the entire n-contact area is utilized. By repeating the same calculations, I achieve table 3, delineating the RC-limited bandwidth for the three smallest PD dimensions.

The main limiting factors here in order to increase RC-limited BW are n-contact area which needs to be small in order to reduce C_j but not too small to increase the n-contact resistivity too much, absorption thickness which needs to be thin enough to reduce junction capacitance but not that thin to adversely affect responsivity and transit-time limited bandwidth and, shorter L_{pn} distance which decrease the sheet resistivity.

Table 3. RC-limited parameters included in the BW calculation of the PDs.

A_{p_metal} (μm^2)	$A_{n\_contact}$ (μm^2)	A_{n_metal} (μm^2)	W_{LP}/L_{pn}	d_{abs} (nm)	C_j (fF)	R_{cn} (Ω)	R_{cp} (Ω)	$R_{sheet,p}$ (Ω)	f_{RC} (GHz)
4.4×26.77	20×30	12.1×22	12.2/45.4	600	114	26.7	23.5	38.7	12.9
4.4×26	20×20	10×11	12.9/38	600	76	64	24.2	33.51	14.6
4.4×23.2	20×15	8.1×10	10/38	600	57	87.7	27.15	37.6	16.4

To calculate the transit time limited bandwidth, I use equation (1.8). The hole drift velocity in GaAs is 1.8×10^7 cm/s [42] which gives f_{τ} of more than 135 GHz for 600 nm GaAs absorption layer which is far above the numbers I calculated in table 3. So, considering (1.9), the limiting factor is f_{RC} .

Concluding the configuration of our mask devices, the top illumination PD pads are contributing to the preliminary assessment of the devices' DC performance prior to the incorporation of RF pads. As depicted in Figure 2-19, a subset of these top-illuminated devices is shown on the mask layout. Notably, these PDs shared p-mesa (depicted in green) and p-type ohmic contact (depicted in purple). Additionally, the ring-shaped n-type ohmic contact (in brown), enveloping the circular n-mesa (in blue) which absorbs the top illumined light.

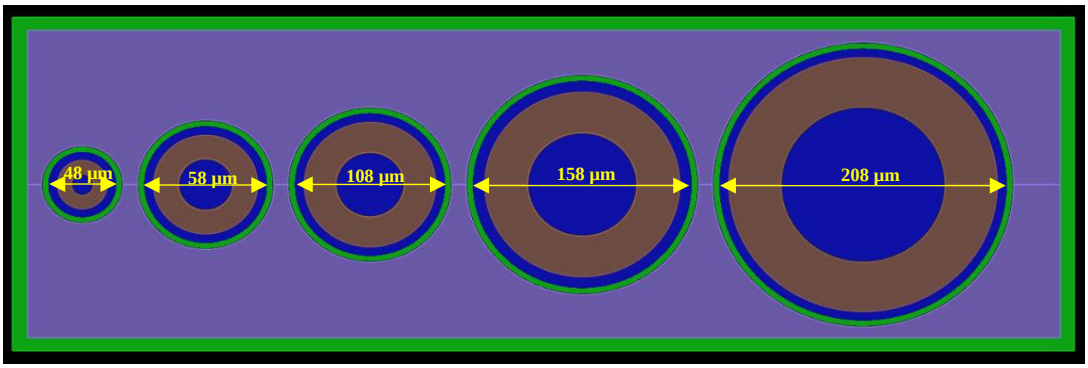


Figure 2-19. Circular top illuminated non-waveguide PDs.

2.4 Fabrication

The fabrication process of PDs encompasses four primary steps:

- Waveguide chip fabrication by our collaborator
- Adhesive bonding of GaAs epitaxial layer onto a tantala chip.
- Patterning the mesa through a series of sequential wet etching procedures.
- Deposition and subsequent lift-off of ohmic contacts.
- Integration of RF probe pads achieved via seed layer sputtering and electroplating.

2.4.1 GaAs die bonding onto SOI

The initiation of the GaAs epitaxial bonding onto the tantala chip involves the dicing of the 2-inch GaAs wafer epitaxial layer into smaller dimensions (5 x 7 mm^2). Tantala chips, received in 8×8 mm^2 pieces from our collaborator, undergo cleaning using trichloroethylene (TCE), reagent alcohol (RA), and methanol. Surface activation is facilitated through a 10-minute exposure to O_2 plasma at 300 W. Subsequently, the tantala chip is spin-coated with a 250 nm layer of SU-8 6000.5, followed by a 1-minute soft-bake at 110 °C and exposure to 280 mJ/cm^2 of MJB4. SU8 was successfully used by Prof. Weikle research group before to bond GaAs epitaxial layer on Si substrates [43].

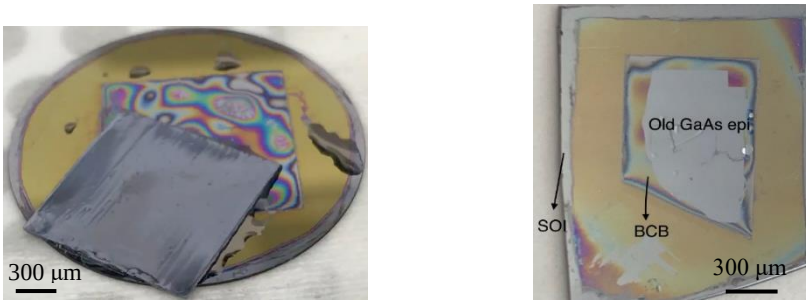
Figure 2-22(a) shows the configuration of the bonding tool employed, belonging to Prof. Weikle's research group. The tantala chip is securely fixed on a copper block, which maintains contact with a 350 W cartridge heater embedded within the heating block. The chamber interior is partitioned into upper and lower chambers using a silicone membrane sheet (depicted in Figure 2-22(b)). The bonding jig, as depicted, operates using dual-chamber pressure difference, delivering the required bonding force of approximately 10 psi. The two pieces are brought in contact at room temperature within the lower chamber after 40 min of outgassing and subsequent pumping down to base pressure (Figure 2-22(c)). Following this, the temperature is gradually elevated to 140 °C on a moderate ramp. Each chamber is evacuated through separate paths utilizing a common pump engine (Figure 2-22 (d)). Adjustment of the bonding force is achieved by injecting nitrogen (N_2)

via the green valve in Figure 2-22 (d) into the upper chamber. The two components remain in contact under a constant force for approximately 2 hours. Subsequently, demounting of the sample is facilitated by a gradual cooling process of the bonding jig. As an alternative adhesive, using benzo-cyclobutene (BCB), I explored the bonding process, and a comparative analysis with the previously employed SU8 is presented in Table 4.

Table 4. Comparison between SU8 and BCB

	BCB	SU8
Photo patternable	Yes(4000 series)	Yes
Curing	Thermal (series 3000,250 °C) UV (series 4000)	UV-thermal(140 °C)
thermal stability	Up to 350 °C	Up to 200 °C
Refractive Index	1.57 (300~1600 nm)	1.72 (300 nm) 1.57 (1600 nm)
Transparency	>90 % , λ>420 nm [44]	>90 % ,λ>420 nm [45]
Planarization	Excellent (>90 %)	Normal
Dielectric constant (ε_r)	2.65 @ 1-20 GHz [46, 47]	3.2 (< 50 GHz) [48]
Loss tangent or dissipation factor	0.0008@ 1MHz-10GHz [46] 0.01(>400 GHz) [49]	0.015 @ 1GHz [50, 48] 0.03(>400 GHz) [51]
Linear Coeff. Of Thermal expansion [ppm/°C]	42 [44]	52 [50]
Etch rate	3000 series: CF_4 dry etch [44] ~250 nm/min 100 W, 100 mT, 10 sccm CF_4, and 40 sccm O_2 [52]	CF_4 Dry etch~25 nm/min CF_4 29.2 Sccm, 25.1 mT, 100 W
Viscosity @ 25 ºC	14 [46]	2.5 [50]
Density (g/ml)	1.05 [46]	0.999 [50]

The results indicate several advantages of BCB over SU8 in adhesive bonding, including enhanced planarization and superior thermal stability. Subsequently, preliminary bonding tests were conducted using Cyclotene 3022-35, as elaborated below. As per the datasheet, a gradual temperature ramps up to 250 °C was expected to be enough for fully curing BCB. However, practical experimentation revealed insufficient bonding strength when bonding GaAs onto an SOI substrate, as depicted in Figure 2-20(a). This resulted in debonding of the two components during handle removal.



(a) (b)

Figure 2-20.(a) Debonded GaAs piece which was bonded onto SOI using BCB (b). GaAs bonded on SOI using Cyclotene 3022-35 after substrate removal using the updated recipe.

To achieve satisfactory results, it was determined that an increase in temperature up to 350 °C was necessary, a condition not consistently achievable with the existing custom-made bonder available in the cleanroom at the time. Additionally, the bonding required the application of approximately 70 psi bonding force and a base pressure of 3 mbar, both challenging to achieve with the conventional bonder at hand. In the sole bonding attempt utilizing this modified recipe, the two components showed a successful bonding, with no instances of delamination or debonding observed during handle removal. The outcomes of this experiment are illustrated in Figure 2-20(b), reflecting an approximate yield of 70 %. However, due to the inherent challenges in maintaining the prescribed bonding conditions and the knowledge that BCB necessitates an extensive dry etch for removal post hard cure—a process that could potentially damage the waveguides —it was concluded that SU8 remained a more viable option. This determination was reinforced by the observation that SU8-bonded PDs demonstrated resilience even after annealing at

temperatures as high as 400ºC. Figure 2-23(a) shows the GaAs epi bonded onto the tantala chip using SU8.

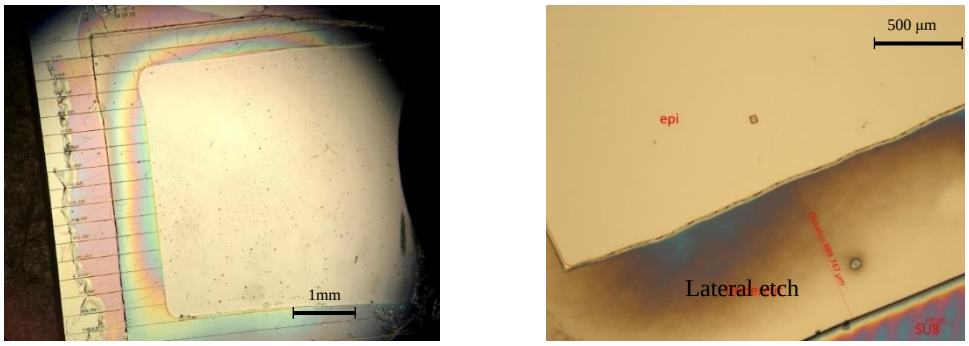
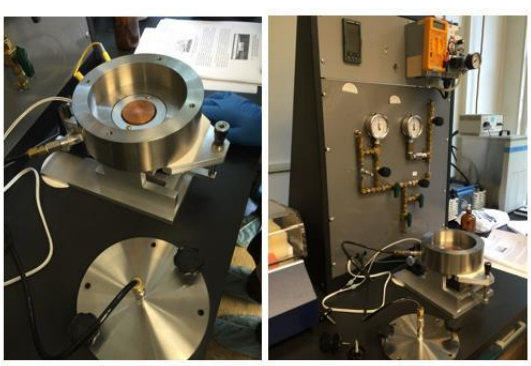
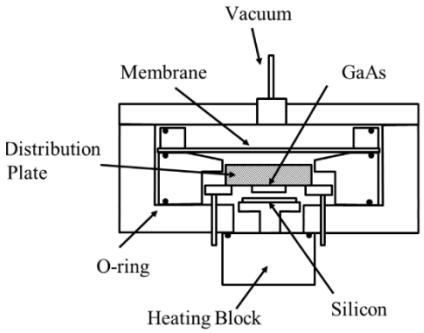


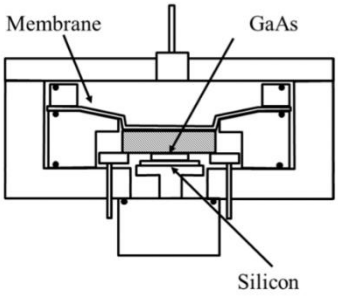
Figure 2-21. Microscope images showing undercut during GaAs substrate removal.



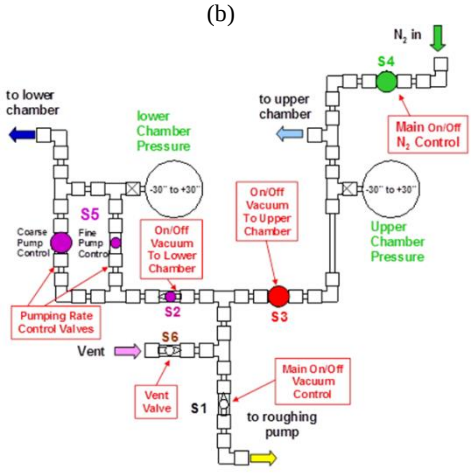
(a)



(b)



(c)



(d)

Figure 2-22. (a) The custom designed iFAB wafer bonder (b) Wafer configuration before bringing the two pieces in contact in the lower chamber (c) Piece are brought in contact manually in the lower chamber after outgassing (d) The piping/valve diagram of the bonder.

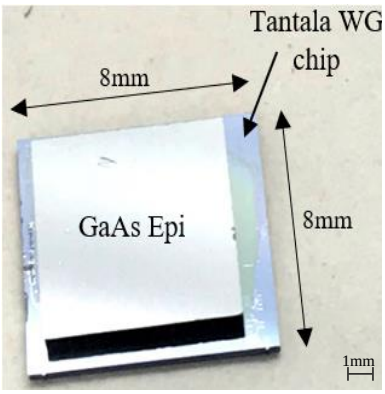


Figure 2-23. GaAs epi bonded on tantala chip.

More recently, a SUSS XB8 semi-automatic high-force commercial wafer bonder was employed too (Figure 2-24), for bonding the epitaxial layer onto the 2nd generation waveguide chips. This commercial tool comprises two plates, both top and bottom, featuring adjustable temperature and force settings. Upon loading the two components, the plates come into proximity, aligning with the stack height previously specified in the recipe. The samples are positioned at the center of the bottom plate, and for improved heat transfer, a graphite sheet can be utilized across the entire stack. The remaining steps in the recipe closely resemble those used with the conventional bonder. Despite the enhanced reliability and user-friendly features of the new tool, which provides greater flexibility in adjusting critical parameters such as temperature, vacuum pressure, applied force, and temperature ramp-up, it's noteworthy that the minimum force that can be applied to the components (200 N) is more than 10 times greater than that of the conventional bonder for the same sample dimensions which increases the risk of breaking the pieces.

Figure 2-24. SUSS commercial wafer bonder *[53]*.

2.4.2 Substrate removal

Subsequent to the bonding process, the entire stack was fixed to a carrier utilizing adhesive wax. Substrate removal involved the sequential use of nitric acid, citric acid, and hydrofluoric acid (HF). A notable challenge during the nitric acid etch phase (Figure 2-21) was the occurrence of a substantial lateral etch spanning 500~800 μm around the epitaxial (epi) die. This lateral etch exposed the waveguide section to the subsequent rigorous HF etching process.

It is imperative to highlight the necessity of preserving the integrity of the waveguides throughout all processing steps to ensure efficient optical coupling into the PDs at the end. The HF used for etching through the AlGaAs etch stop layer posed a significant threat to the waveguides, particularly in regions not protected by the epitaxial layer. Further discussion on this matter will be presented subsequently.

The GaAs substrate removal begins with a 12-minute etching in nitric acid at 50 °C, facilitating rapid removal of the GaAs substrate at a rate of 30 μm/min. This was followed by a 60-minute citric acid etching at 50 °C to achieve controlled etching of the remaining

GaAs substrate. Finally, a brief exposure of no more than 30 seconds to HF was employed to eliminate the residual 500 nm AlGaAs etch stop layer. Figure 2-25 shows the bonded piece after GaAs substrate removal.

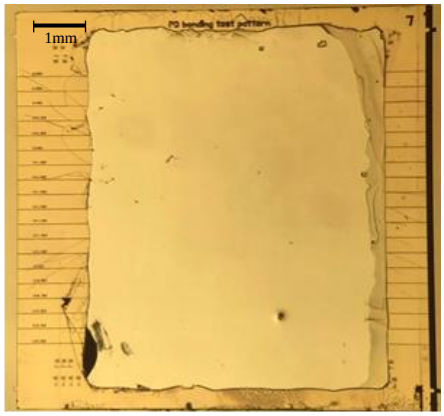


Figure 2-25. GaAs epi after substrate removal.

2.4.3 Post-processing waveguide treatment

As previously described, a major challenge encountered during the processes of substrate removal and mesa patterning was the protection of tantala waveguides located in regions initially devoid of the PD epitaxial layer. Unfortunately, certain segments of these waveguides suffered damage during the HF step of the substrate removal process (refer to Figure 2-27). It is noteworthy that this damage occurred despite the presence of a 250 nm thick SU8 layer atop the waveguides, and the HF wet etching duration did not exceed 30 seconds (see Figure 2-26). It's worth highlighting that HF infiltrates the SiO_2 lower cladding of the waveguides from the top by diffusing through trench sidewalls and by inward diffusion from the facets to the waveguides. Given the presence of the PD epitaxial layer during HF wet etching, all waveguide sections within the bonding window remained unaffected (see Figure 2-28).

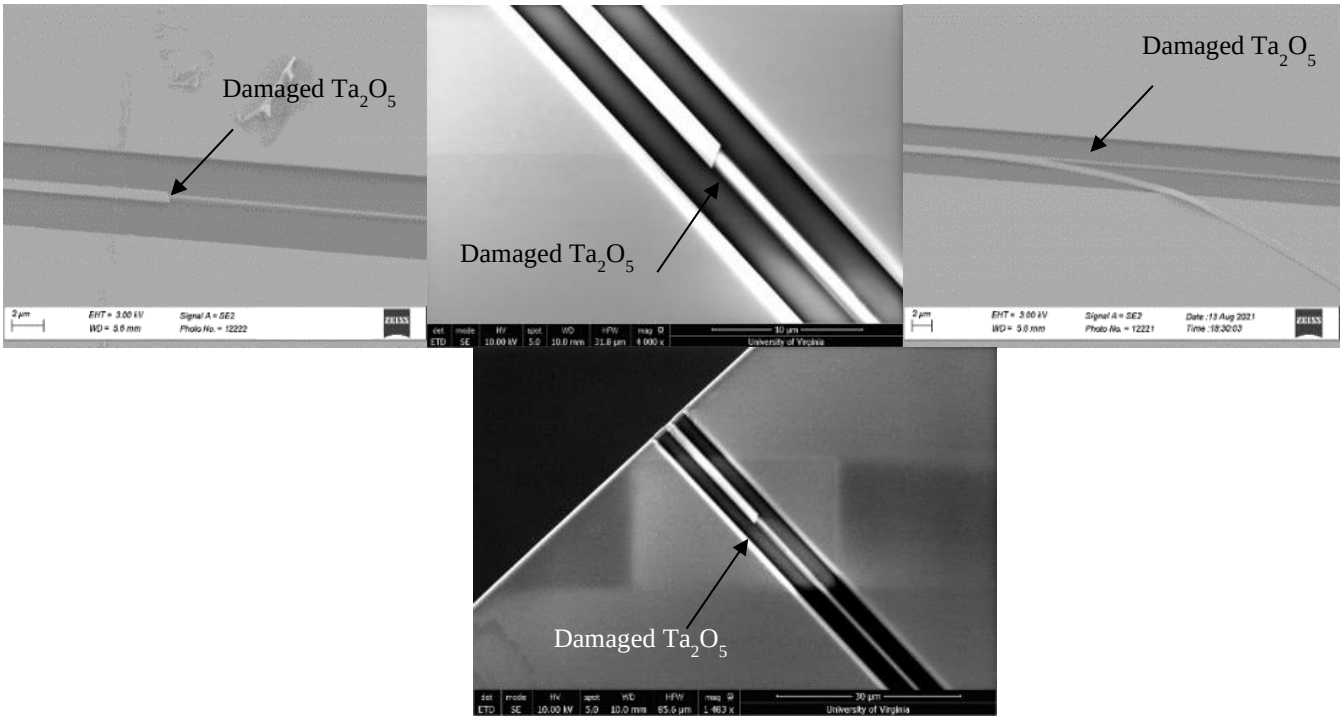


Figure 2-26. Damaged waveguides due to HF wet etching.

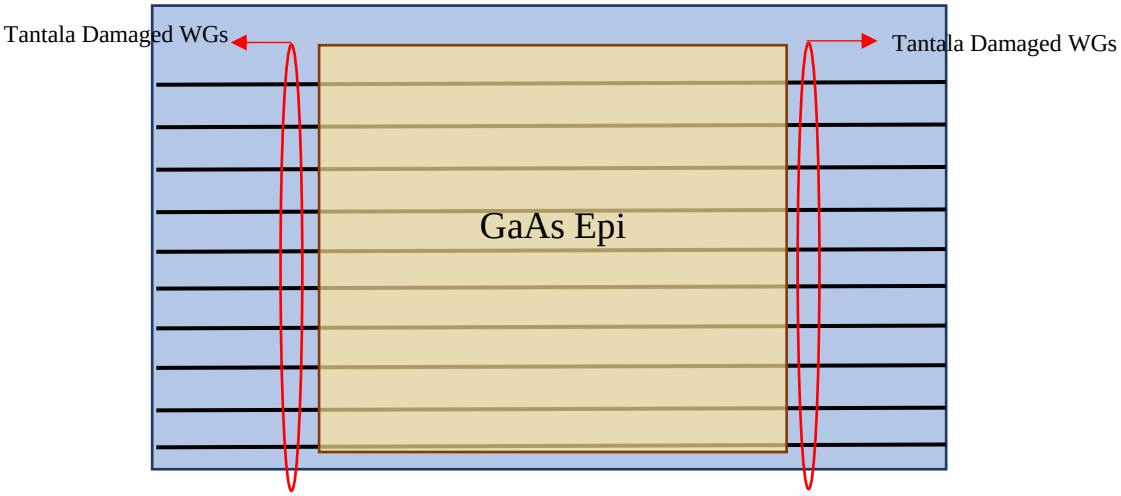


Figure 2-27. Schematic top view of the bonded GaAs on tantala showing the damaged WG areas.

To address waveguide facet damage caused by HF, I adopted the following methodologies.

1. Dicing and ion milling

To address the removal of the damaged waveguide sections and facilitate efficient light coupling into the PDs, one approach involved protecting the intact portions (refer to

Figure 2-29) using photoresist. Subsequently, the piece was diced along the edge within the bonding window using the Disco 3220 dicing machine. As shown in Figure 2-30, the waveguide facet remains rough after dicing, and the efforts were made to couple light into some of the exposed waveguides left on the piece after dicing, resulting in a substantial loss. While an anticipated loss of around 7 dB per facet was expected at 635 nm, the observed loss was significantly higher, ranging from 13~14 dB per facet for nearly all devices. Prior to the application of the resist layer, I conducted a coupling loss measurement of the unprocessed tantala to ensure the optimal functioning of the waveguide. According to this measurement, the fiber in- fiber out loss was approximately 14 dB (7 dB/facet), while the tip-to-tip loss (without any involvement of the waveguide) was measured at around 0.5 dB.

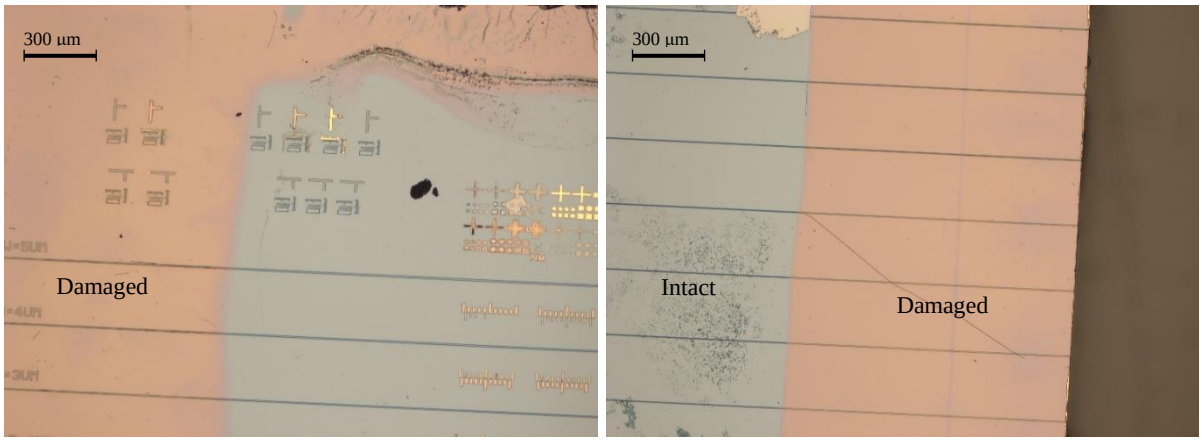


Figure 2-28. Undamaged waveguide sections inside the bonding window.

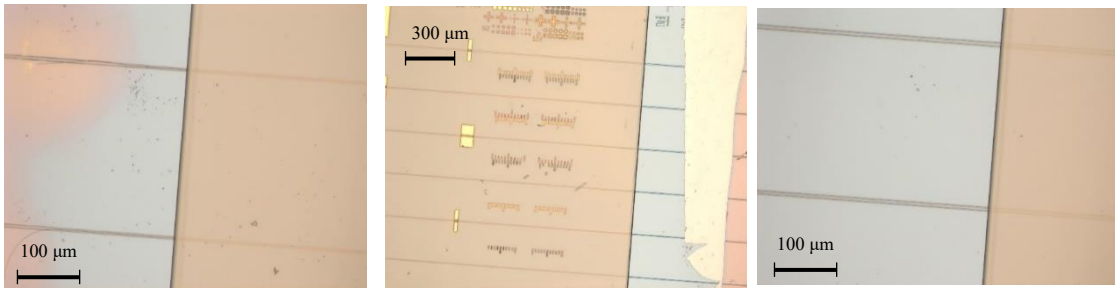


Figure 2-29. Resist protection to cover waveguide and PDs during dicing and ion milling.

This underscores the necessity of ion milling to address facet-related issues beyond dicing alone. In this regard, ion milling was employed. As I stated, the primary waveguide section was shielded with photoresist before dicing, and this protective layer was maintained during both dicing and ion milling processes to safeguard the waveguides and photodetectors (refer to Figures 2-29 and 2-31). Employing μ-writer lithography, I exposed approximately 50~70 μm of the facet edge toward the center for ion milling. After dicing, approximately 150~160 nm of the tantala chip's edge was subjected to ion milling (Figure 2-31).

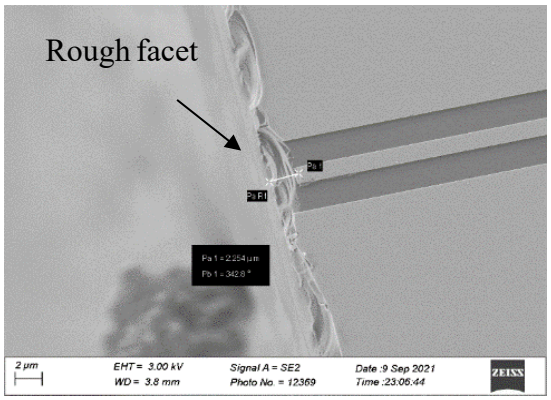


Figure 2-30. Some SEM images of the waveguide rough facets after dicing.

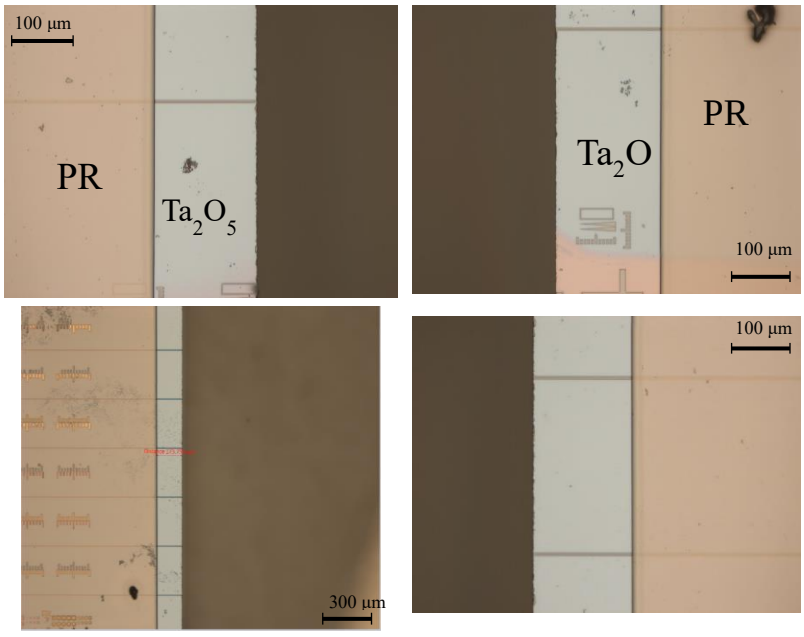


Figure 2-31. Microscope images of the diced edge of the tantala with resist protection.

a) Ga_+ ion FIB milling

In an early attempt, the endeavor to couple light into a waveguide on an unprocessed chip after utilizing the Helios gallium ion milling system, proved to be unsuccessful. Figure 2-32 shows the waveguide facets after FIB process. Consequently, I discontinued using the Helios gun. The primary reason behind this decision was to mitigate the potential damage caused by the heavy Ga_+ ions to the waveguides. Moreover, considering the aspects of time efficiency and cost-effectiveness, I opted for an alternative approach.

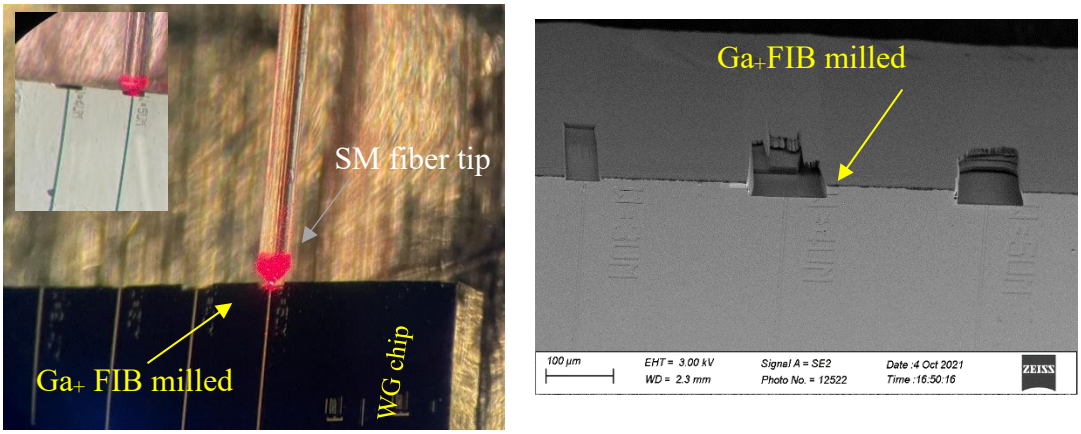


Figure 2-32. FIB polishing using Ga_+ ions to treat the waveguide facets.

b) IM4000 Ar ion milling

This time, the ion milling process was done using the cross-section mode of the IM4000 Ar ion milling machine. In addition to the top protection resist, the surface of the piece was shielded using a thick titanium piece securely fastened along with the edge of the protection resist. Figures 2-33 and 2-34 visually represent the facets after the ion milling process and subsequent removal of all protective measures.

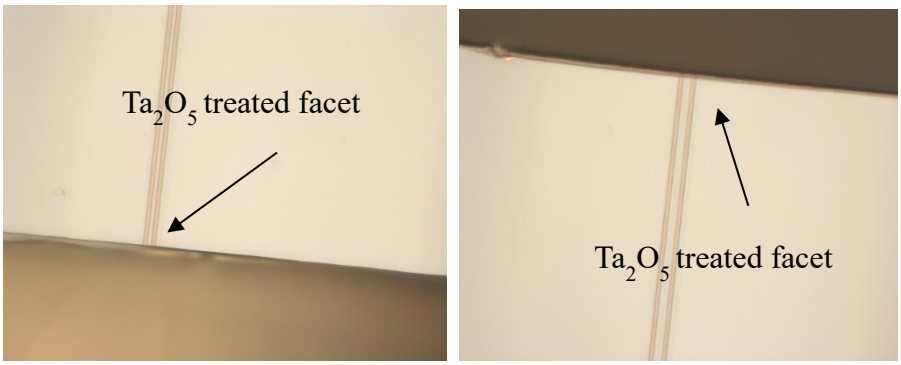


Figure 2-33. Microscope images of the tantala waveguide facet after ion milling and top resist removal.

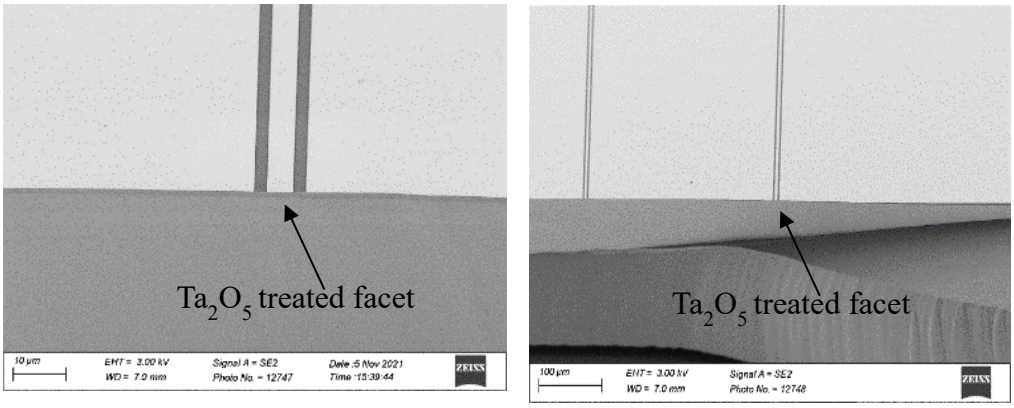


Figure 2-34. SEM images of the tantala facet after ion milling and top resist removal.

To evaluate the impact of ion milling on PD performance, I obtained current-voltage (IV) characteristics for both top-illuminated and a select number of WGPDs. These measurements were conducted utilizing the IV station, both before and after the waveguide treatment. Notably, as depicted in Figures 2-35 and 2-36, it was observed that ion milling exhibited a slight reduction in the dark current across all devices.

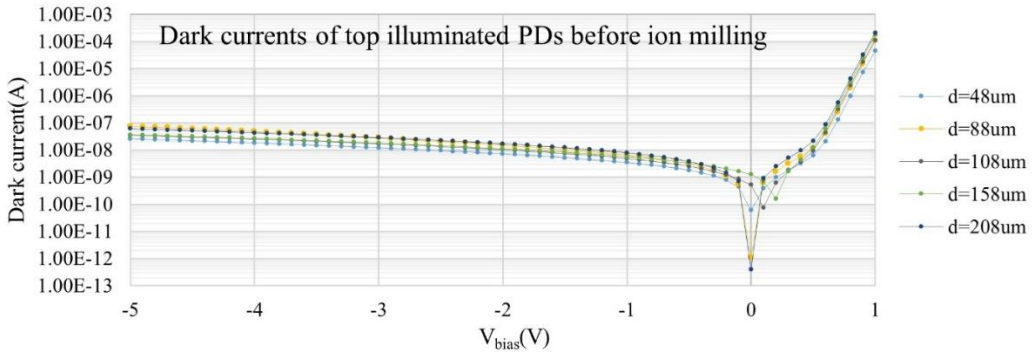


Figure 2-35. Dark current measurement of the circular PDs before ion milling.

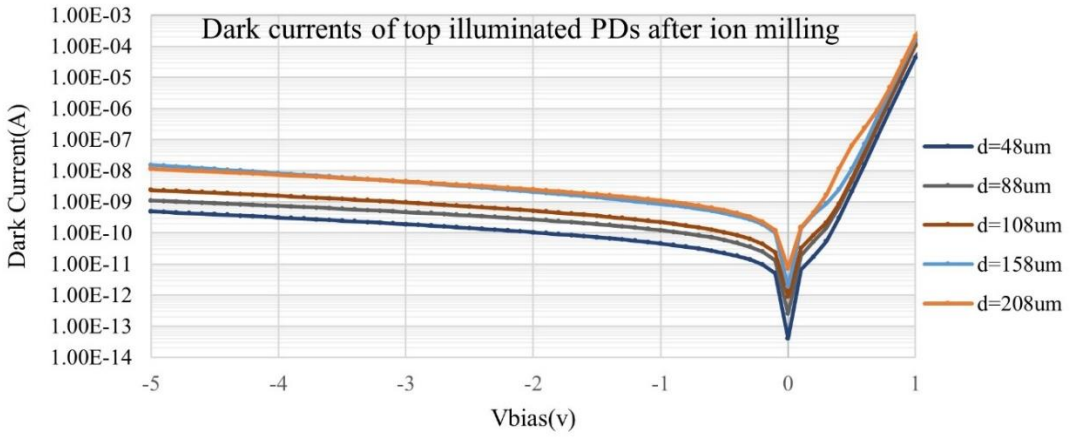


Figure 2-36. Dark current measurement of the circular PDs after ion milling.

2. Utilizing a larger epi and sidewalls protection

In conjunction with ion milling for addressing damaged waveguides, an alternative approach was considered. This involved dicing the initial epitaxial layer into larger pieces, bigger than the dimensions of the tantala chip. Consequently, the epi edges would extend approximately 1mm beyond the tantala chip on the facet side post-bonding. Subsequently, the backside and the sidewall of the tantala chip, including the facets, were protected using AZ4210. Detailed insights into this approach are illustrated in Figure 2-37.

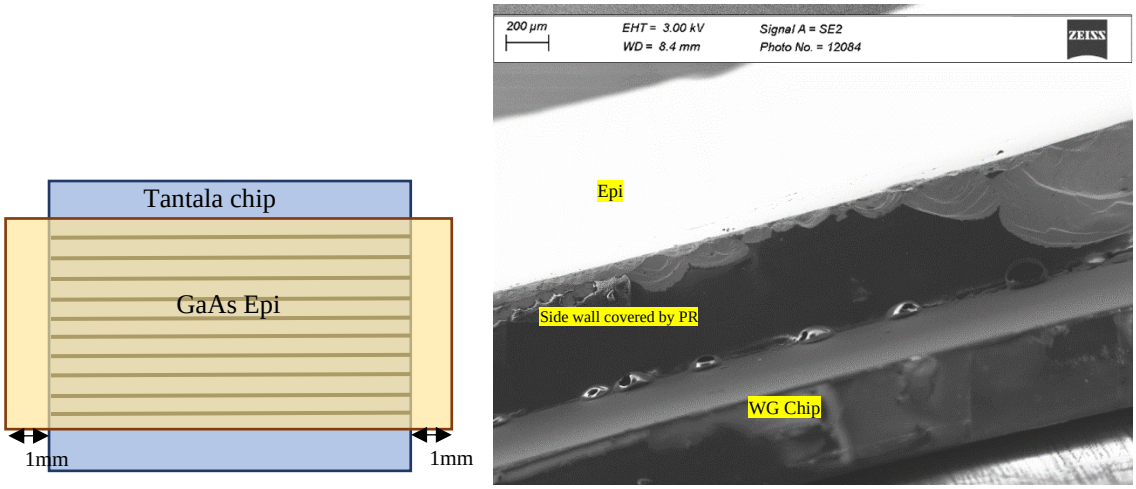
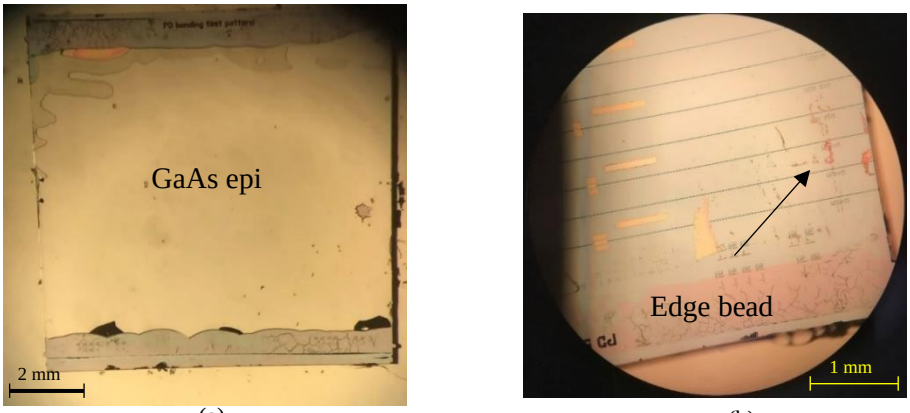


Figure 2-37. Sidewall protection approach to prevent waveguide damage.

Despite the reduction in waveguide damage inflicted by HF, as evidenced in Figures 2-38 and 2-39, additional post-processing steps, such as ion milling or polishing, are still

essential to render this chip practically viable for light coupling. Therefore, this technique proves impractical due to the following reasons:

1. The protective photoresist (PR) cannot endure prolonged nitric acid etching and tends to be partially peeled off during the process. Consequently, a small portion of the waveguides remains exposed to HF (indicated by the pink color in Figure 2-39). This necessitates additional post-processing steps, including dicing, ion milling and polishing.
2. Covering the entire waveguide chip surface with a large epitaxial layer is cost-ineffective and a waste of epitaxial material.



(a) (b)

Figure 2-38. (a) GaAs epi after substrate removal using sidewall protection method (b) Mesa formation on the same piece.

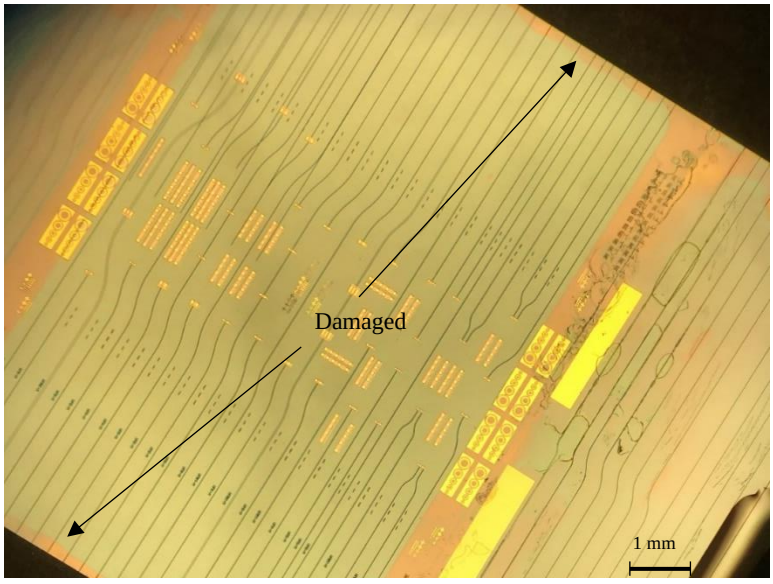
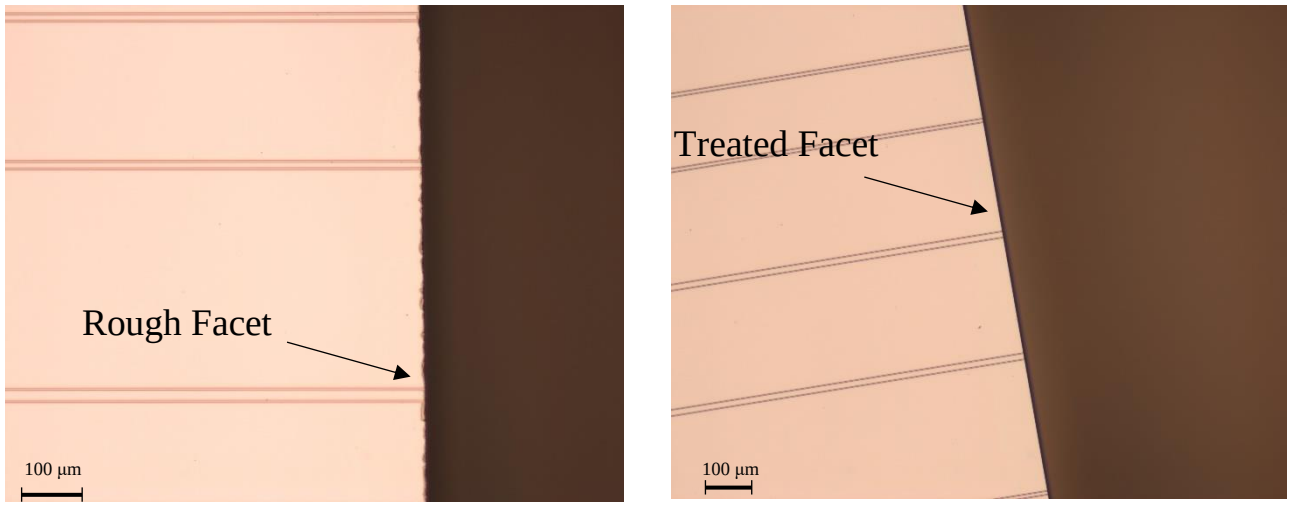


Figure 2-39. Devices fabricated on the second-generation waveguide substrate employing the sidewall protection technique.

3. Dicing and polishing

Dicing the chip along the damaged delineation and employing a high grit size abrasive paper for facet polishing is another method.



(a) (b)

Figure 2-40.(a) The waveguide chip edge after dicing (b) The waveguide chip edge after treatment using abrasive paper.

As it's evident from Figure 2-40, this method proved to be highly effective in treating damaged waveguide facets.

4. Hub-less blade dicing

The fragility of GaAs makes it susceptible to the force exerted by the hub-less blade during dicing, thereby preventing achieving a uniform substrate removal and leading to undesired stripping off a portion of the epitaxial layer, as depicted in Figure 2-41. It is noteworthy that the adoption of this method was driven by the intention to minimize reliance on wet etching procedures. Consequently, the necessity arose to eliminate more than 550 µm of the handle.

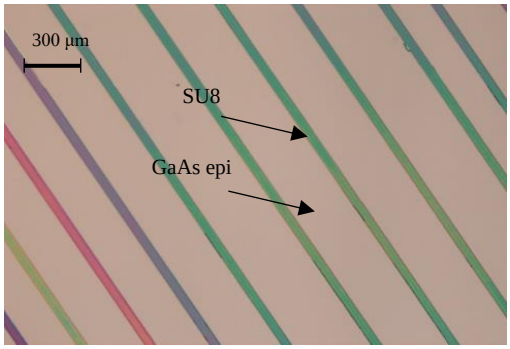


Figure 2-41. Epi peeling off caused by dicing blade force used for substrate removal.

5. Potassium iodide dilution

In addressing the previously mentioned lateral etching concern, I used diluted potassium iodide (KI) for substrate removal of the epi piece bonded on the second-generation waveguide chips. The selectivity of KI dilution over GaAs, coupled with its non-reactivity towards waveguides in contrast to the corrosive effects of HF, enabled the successful completion of the substrate removal process. This circumvented the challenges associated with subsequent post-processing treatments, including ion milling, dicing, and facet edge polishing through the application of high grit size sandpaper, as illustrated in Figures 2-42 and 2-44.

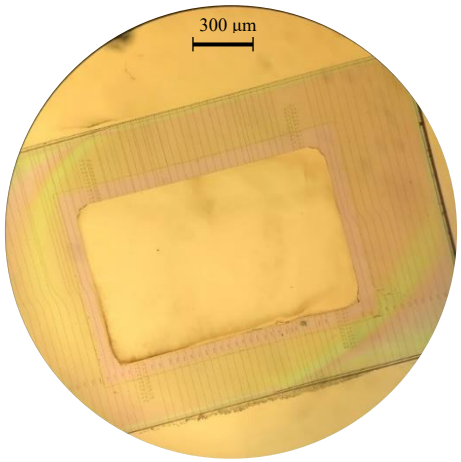


Figure 2-42. GaAs bonded on Tantala chip after substrate removal using KI dilution.

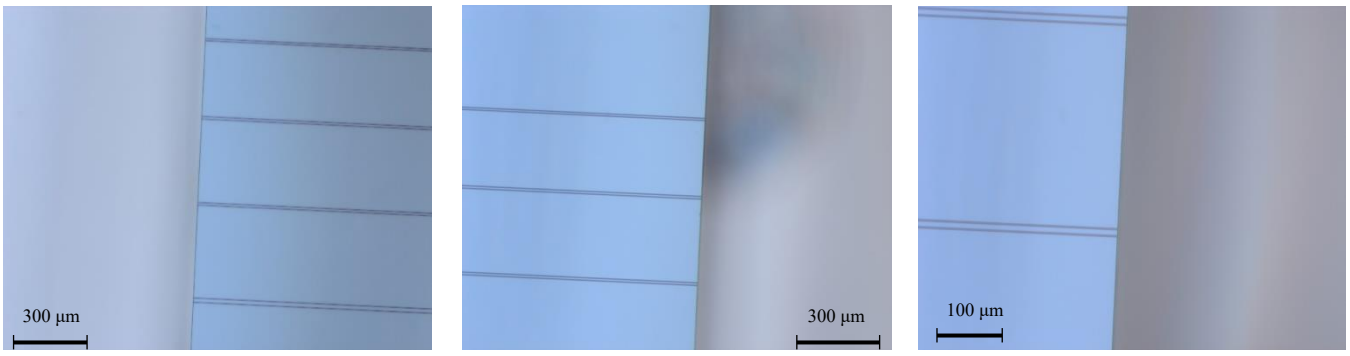


Figure 2-43. WG facet of the 2nd Gen chip after patterning mesas and ohmic contacts using KI for the purpose of substrate removal. No sign of damage was observed at the WG facets using this method.

The fiber in-fiber out measurement of the uncladded waveguides on the 2nd Gen tantala, as illustrated in Figure 2-44 subsequent to the mesa formation, confirms an approximate 7 dB per facet for red light.

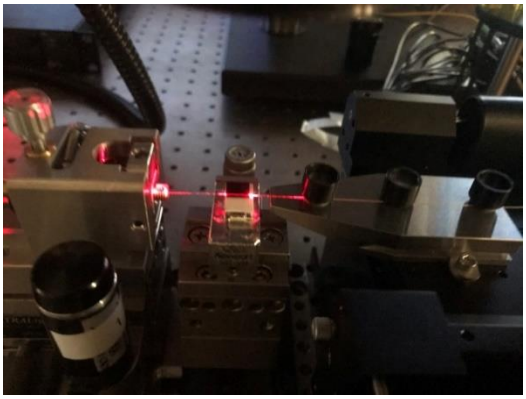


Figure 2-44. Fiber-chip-fiber measurement setup for waveguide loss measurement exploiting 635 nm optical source.

2.4.4 Mesa formation

The patterning of n mesas onto the tantala waveguides is achieved through virtual mask lithography at an incident energy of 300 $mJ.cm^{-2}$. AZ4210 serves as the photoresist, with HMDS employed as an adhesion promoter. The development process occurs in a 300MIF environment for approximately 90 seconds. For the selective wet etching of AlGaAs over GaAs, KI dilution and citric acid are utilized, demonstrating high selectivity. A comprehensive evaluation of various etchants is conducted for mesa patterning,

summarized in Table 5, illustrating the selective wet etching of GaAs over AlGaAs at different aluminum compositions. Additionally, Table 6 and Table *7* present potential etchants for selectively wet etching AlGaAs over GaAs and outline viable options for dry etching. Table 8 and Table *9* offer a comparative analysis between dry etching and wet etching techniques in the fabrication of GaAs photodetectors.

Table 5. Potential etchants to selectively wet etch GaAs over AlGaAs.

Etchant	Material	Comments
H_2O_2 with NH_4OH added to adjust pH from 7.2 to 8.6 [54]	GaAs/$Al_{0.16}Ga_{0.84}As$	Selectivity>30 at PH~8.4
$NH_4OH:H_2O_2$ (1:225) [55]	GaAs/$Al_{0.25}Ga_{0.75}As$	pH = 7:04 GaAs etch rate= 6 um/h with selectivity of 10
$NH_4OH:H_2O_2$(1:225) [56]	GaAs/AlGaAs	Selective(>10)
$NH_4OH:H_2O_2$ (1:170) [57]	GaAs/$Al_{0.42}Ga_{0.58}As$	Selective(>10)
Citric acid:H_2O_2 (4:1) [58]	GaAs/$Al_xGa_{(1-x)}As$ x=0.17 x=0.3 x=0.45 x=1	Selectivity: 1.5 155 260 1450
Citric acid:H_2O_2 (3:1) [59]	GaAs/AlAs	Selective(>10)
Citric acid:H_2O_2 [60] (m:1, with 1 < m < 9)	GaAs/AlAs or AlGaAs	Selective(>10)
Citric acid:H_2O_2 (2:1) [61]	GaAs/$Al_{0.26}Ga_{0.74}As$	Selective(>70)

H_3PO_4:H_2O_2:H_2O (4:1:90) [62]	N-GaAs/$Al_{0.4}Ga_{0.6}As$	Selective(>10) 25ºC
NH_4OH:H_2O_2:H_2O (1:3:16) [63]	GaAs/AlGaAs	Selective(>10)

Table 6. Potential etchants to selectively wet etch AlGaAs over GaAs.

Etchant	Material	Comments
Hot HCL [64]	$Al_xGa_{1-x}As$/GaAs(X>0.42)	Selectivity>10
Hot HF [65]	$Al_xGa_{1-x}As$/GaAs(X>0.38)	Selectivity>10
H_2SO_4:H_2O_2:H_2O (1:8:80) [66]	$Al_{0.1}Ga_{0.9}As$/GaAs	Selectivity>10
NH_4OH:H_2O_2:H_2O (2:0.7:100) [67]	$Al_{0.42}Ga_{0.58}As$/GaAs	Selectivity>10
NH_4OH:H_2O_2 (1:30) [68]	$Al_{0.6}Ga_{0.4}As$/GaAs	Selectivity>10
I_2:KI:H_2O (65 g:113 g:100 g) [65]	$Al_xGa_{1-x}As$/GaAs	Selectivity>10
HF:H_2O (1:10) [68]	$Al_{0.7}Ga_{0.3}As$/GaAs	Selectivity>10
HF (48%) [69]	$Al_xGa_{1-x}As$/GaAs	Selectivity>10

Table 7. Dry etch options for GaAs/AlGaAs system.

Etchant	Material	Comments
CCl_2F_2 [70]	GaAs/$Al_{0.3}Ga_{0.7}As$	$Al_{0.3}Ga_{0.7}As$(etch stop) selectivity > 4000

$SiCl_4$:SiF_4 (1:9) [71]	GaAs/AlGaAs	Selectivity>10
$SiCl_4$:CF_4:O_2:He [72]	GaAs/$Al_{0.11}Ga_{0.89}As$	Selectivity>10
BCl_3/SF_6, $SiCl_4/SF_6$ [73]	GaAs/AlGaAs	Selectivity>10
CH_4 + H_2 [74]	GaAs/AlGaAs	Selectivity>10
CCl_2F_2 + He [75]	GaAs/$Al_{0.3}Ga_{0.7}As$	Selectivity>10
BCl_3 [76]	GaAs/AlGaAs	Selectivity>10
CCl_4/He [77]	AlGaAs/GaAs	Selectivity > 1000

Table 8. GaAs PDs fabrication outline using wet etch recipe.

#	Steps	Comments
1	N mesa lithography	Direct laser (µ-writer)
2	wet etch down to p-contact	Citric acid/HF/Citric acid/HF
3	P mesa lithography	Direct laser (µ-writer)
4	P mesa wet etching	Citric acid/HF/Citric acid
5	N metal lithography	Direct laser (µ-writer)
6	N metal deposition	AuGe/Ni-Ebeam
7	N metal lift off	PG remover
8	P metal lithography	Direct laser (µ-writer)
9	P metal deposition	Ni/Pt/Au- Ebeam

10	P metal lift off	PG remover
11	Seedlayer lithography	With LOR underneath- direct laser (µ-writer)
12	Ti/Au seedlayer	Sputtering(10nm/50nm)
13	Plating lithography	Direct laser (µ-writer)
14	Plating	2 µm thick
15	Removing seedlayer & sac resist & plating resist	O_2 plasma- potassium iodide dilution- NMP in sonicator

Table 9. Fabrication outline of GaAs PDs using dry etch.

#	Steps	Comments
1	N-metal lithography	
2	N metal deposition	
3	N metal lift off	
4	Protection I lithography	µ-writer with protection margin
5	Dry etch down to p-contact to form n mesas	
6	Protection II lithography	
7	edge epi left over wet etch	Not efficient specially after patterning the n-metal!
8	P mesa lithography	

9	P mesa wet etch	Can't be done with dry etch due to the risk of potential damage to waveguides
10	P- metal lithography	
11	P metal deposition	
12	P metal lift off	
13	Seedlayer lithography	AZ5214
14	Ti/Au deposition	sputtering
15	Plating lithography	
16	Au plating	
17	Removing seedlayer & sac & plating resists	

Based on the information derived from these tables, several compelling reasons support the decision to proceed with wet etching:

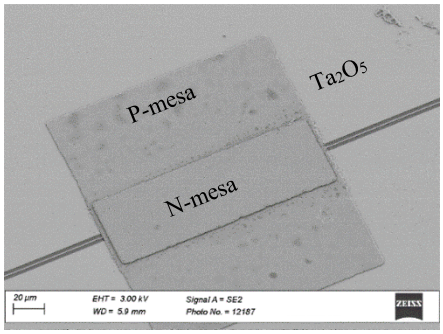
1. Reduced dark current: experimental evidence indicates that PDs produced using the wet etch recipe exhibit lower dark current compared to those fabricated using dry etch.

2. Minimized waveguide damage: dry etch recipes pose a higher risk of damaging WGs. Protecting WGs during the dry etch process is challenging, leading to potential risks for the unprotected WGs. Additionally, even with WG protection, challenges arise from the presence of residual epitaxy around the bonding window.

3. Controlled etching depth: while dry etch is more isotropic and avoids undercut issues, it lacks the selectivity of wet etch, making it difficult to control etching depth. The necessity of using a thick resist for dry etch introduces challenges in alignment due to the slower etch rate of the resist compared to the actual epitaxy. This challenge is particularly pronounced when using direct laser lithography.

4. Simplified process and yield considerations: wet etch involves fewer fabrication steps compared to dry etch, contributing to a simpler process. This reduction in fabrication steps is anticipated to have a positive impact on the overall processing yield.

Figure 2-45 (a) visually presents the outcome of the wet etching steps, showcasing the n- and p-mesas. It is noteworthy that the etch rate of AlGaAs is notably influenced by the Al composition. Specifically, at higher aluminum contents, HF (pH ~ 3) dominates as the preferred AlGaAs etchant, while at lower aluminum percentages, KI (pH ~ 7) dilution proves to be more effective.



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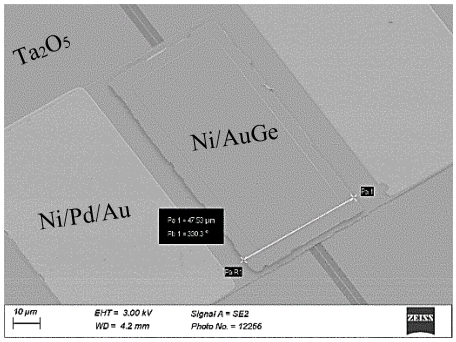

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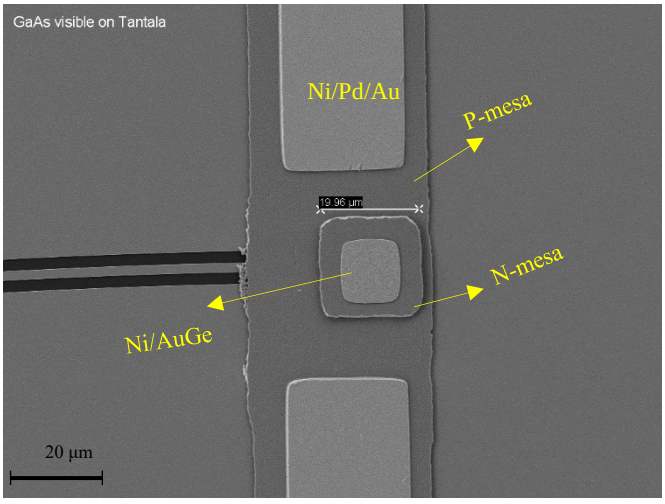

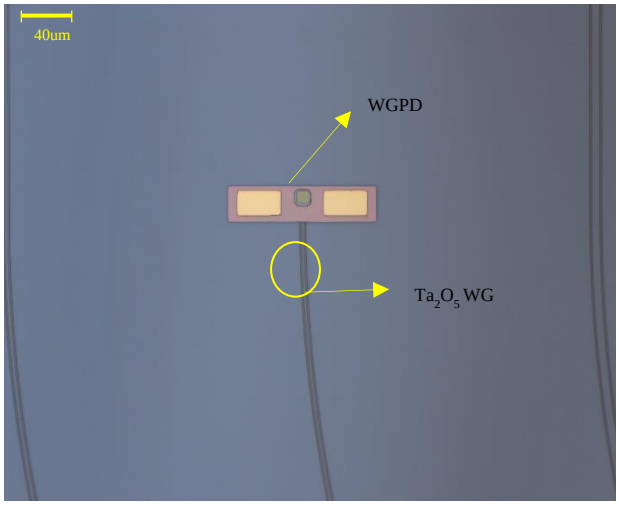

(c)

Figure 2-45.(a) n & p mesas patterned on tantala waveguide chip (b) Metal contacts added on n & p mesas (c) Mesa with metal on top patterned on a single facet waveguide.

2.4.5 Ohmic contact deposition and lift-off

To fabricate the n metal layers, a sequence of steps was undertaken. Initially, a layer of LOR was spun, followed by a soft bake at 160°C. Subsequently, AZ5214 was spin coated

on top, and a lift-off resist as a sacrificial layer was used to enhance the precision of fine patterning of small features. This sacrificial layer also facilitated the subsequent removal of the actual resist [78]. Microwriter lithography at an energy of 200 mJ.cm^{-2}, followed by a 10~20 second development in 300MIF, yielded satisfactory results for the formation of n metal features.

Moving forward, a deposition process involved Ni (56 nm) and AuGe (200 nm) layers using E-beam. The subsequent lift-off process, involving the removal of the metal with the resist underneath using PG remover, resulted in the formation of the metal stack atop the n mesa. A parallel process was conducted for the formation of p metal, with the p metal stack consisting of Ni (80 nm), Pd (120 nm), and Au (200 nm).

Figures 2-45 (b) & (c) depict the mesas adorned with the respective metal stacks. Figure 2-46 shows the top view of the chip after mesa and metal contact formations.

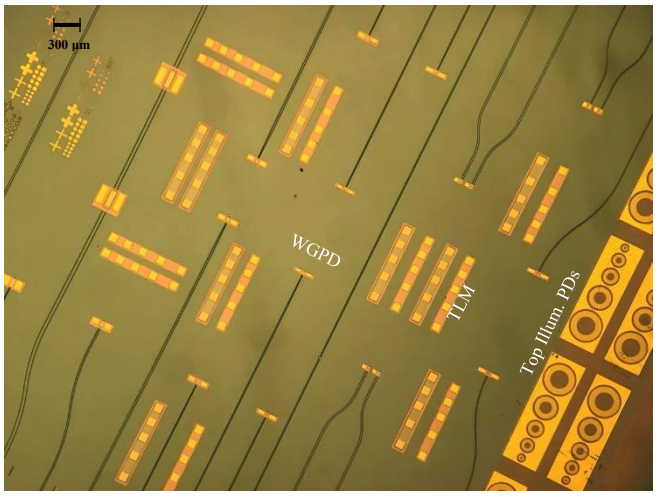

Figure 2-46. Patterned devices on 2nd Gen waveguide chip before adding the RF Pads.

2.4.6 RF pad formation using electroplating

The integration of CPW pads is imperative for assessing the RF performance of the fabricated device. The process involves the application of AZ4210 positive resist onto the chip, followed by a 2-minute soft-bake at 110 °C and exposure to a dose of 300 mJ/cm^2. Subsequently, seedlayer patterns are developed in MIF300, followed by a 1-minute hard

bake at 110 °C. A thin seedlayer consisting of Ti/Au (10 nm/50 nm) is sputtered onto the sample using the sputter3 tool. The second lithography step is then performed to define the plating areas. Actual plating is carried out in a heated container using a Technic gold solution. The subsequent steps involve a KI gold etching process to remove excess gold, followed by a lift-off process using NMP@70 °C in the sonicator. This lift-off process accomplishes the removal of the seedlayer and sacrificial resist from all regions of the chip, including underneath the air bridges. This comprehensive procedure ensures the successful integration of CPW pads for accurate RF performance measurements as shown in Figure 2-47.

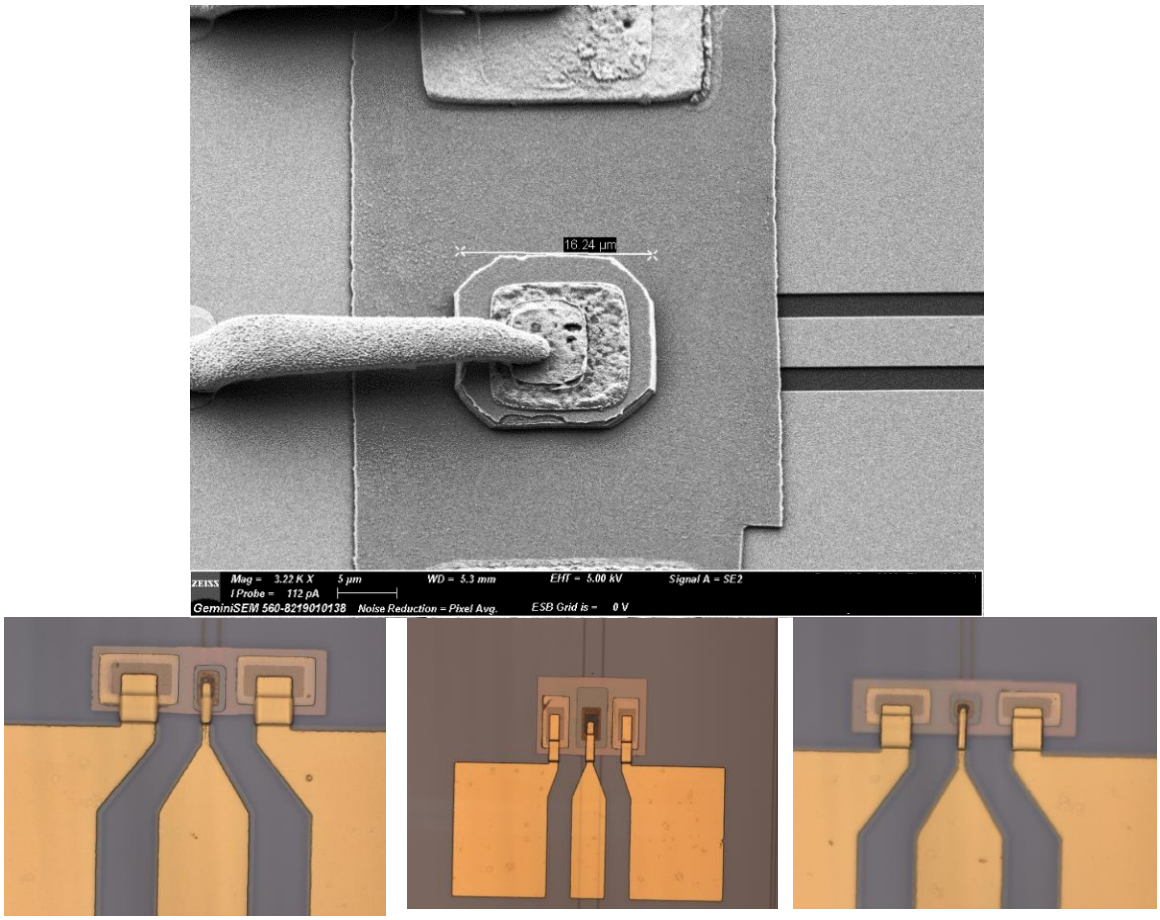

Figure 2-47. Patterned devices with added RF pads

Chapter Three: Characterization of Visible PDs on Tantala Waveguides

3.1 Introduction

In the realm of photonics, the accurate and precise measurement of PD responses stands as a critical aspect of technology development and deployment. What follows is a on the essential sections and steps I used in our PD measurement setup:

- **Light sources**: a controlled light source would be used in this regard. This can be a laser or any other light-emitting device with a known intensity and wavelength. What I've used are listed below:
  - HLS635 Thorlab handheld laser for 635 nm(red) with 2.5 mW max output power (Figure 3-1)
  -

Figure 3-1. HLS635 Thorlab handheld laser

  - Fiber coupled coherent OBIS 633 nm LX SF with 50 mW max output power (Figure 3-2).

- 

Figure 3-2. Coherent Obis 633 nm laser

- Alphalas PICOPOWER-LD-635-FCP 635 (±5) nm with 1.3 W free space max power, with 30 % efficiency fiber coupling, 4.3 mW average power, 65 ps pulse width and 80 MHz repetition rate.
- Alphalas PICOP-LD-510-free space 510 (±10) nm 0.3 W free space max, 1.1 mW average power, 55 ps pulse width and 50 MHz repetition rate (custome free space to fiber coupled dsigned with 50 % efficiency).

These two source heads shared the same driver as shown in Figure 3-3.

Figure 3-3. Alphalas driver with PICOPOWER-LD-635-FCP and PICOPOWER-LD-510-free space laser heads.

I also measured the optical spectrum of these two red lasers to compare in Figure 3-4.

(a) (b)

Figure 3-4. Optical spectrum of two red sources exploited in our characterization measured using optical spectrum analyzer (OSA) (a) Coherent laser source (b) Alphalas fiber coupled laser source.

- FPL785P 785 nm Fabry-Perot laser diode with 300 mW maximum power SM fiber (Figure 3-5).

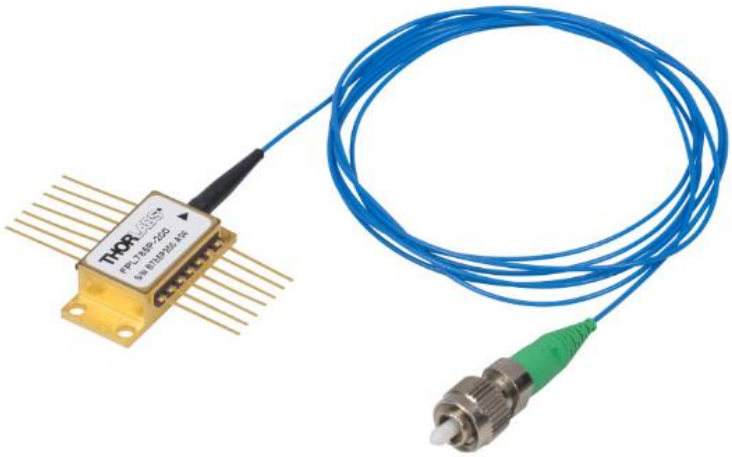

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Figure 3-5. FPL785P 785 nm Fabry-Perot fiber coupled laser diode.

- Fabry-Perot benchtop laser source, 520 nm, 15 mW (Typ.), FC/PC S4FC520 Thorlabs green laser with TEC controller.

- **Alignment system:** Align the optical components to ensure that the incident light is properly directed onto the active area of the PD. This may involve the use of positioners, optical fiber, polarization controller and fiber holder. I used a 6-axis positioner to adjust the fiber holder and manual fiber polarization controller.

- **Electrical Connections:** Connecting the PD to the appropriate electronics for signal analysis. I used 40 GHz GSG probe and bias Tee for these purposes.

- **Signal Acquisition:** This would be using a data acquisition system i.e. an oscilloscope or RF power meter to capture the electrical signal generated by the PD in response to the incident light. The response may be in the form of a photocurrent or voltage. For this purpose, I used Agilent 50 GHz sampling scope, Agilent 10 GHz real time scope, 25 GHz E4440A Agilent ESA, Anritsu ML2437A power meter, and a PM20 Thorlabs handheld power meter(400 nm-1100 nm).

3.2 DC Characterization

Characterization of the devices has been done in four steps:

1. Measuring IV and CV of the PDs.
2. Responsivity measurement in reverse bias using a 635 nm laser source, tapered lensed fiber with patch cord, and Keithley 2400 multimeter.
3. Measuring the impulse response of the PD using pulse source.
4. Measuring the output power and eye diagram of the devices using MZM electro-optical modulator

3.2.1 Measuring IV and CV of the PDs.

Figure 3-6 shows the configuration employed for DC characterization of PDs. To facilitate the FC/APC connector conversion, a patch cord was utilized given the predominance of APC connectors in single-mode (SM) tapered lensed fibers. For the purposes of biasing and monitoring the PD, a Keithley 2400 digital multimeter (DMM) was deployed. The optical sources used for these measurements comprised HLS635 FC/PC red dual-mode laser, Coherent fiber coupled laser, Thorlabs benchtop green source, and 785 nm Thorlabs laser diode.

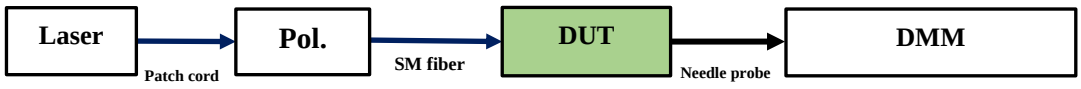


Figure 3-6. PD DC characterization setup.

Figure 3-7 presents the measured dark currents of the fabricated PDs which revealed dark currents reaching a minimum of 20 pA at a reverse bias of -2 V for PDs with an active region of 20×20 μm^2. Furthermore, a detailed analysis of the dark current, photocurrent, and responsivity parameters was conducted for a PD featuring an active area of 20×40

μm^2 at a wavelength of 635 nm on a 1 μm waveguide (Figures 3-8 and 3-9). Notably, the photocurrent measured at 16 μA exhibited a stable response independent of reverse bias less than -1 V. For the calculation of the internal responsivity of the PD at 635 nm, 7-dB loss was applied to compensate for the fiber-chip coupling loss which was obtained from fiber-in fiber-out measurement on bare waveguides of the same chip. To quantify the responsivity of the device, the laser source emitting at a wavelength of 635 nm, set to a low power mode of 1 mW and coupled via an FC/PC patch cord, was employed. For the purpose of delivering the laser power to the waveguide facets, a single mode 532 nm tapered lensed fiber with 2 μm spot diameter and working distance of 10 μm was utilized, with the output power validated using both the PM20 and Newport optical power meters. The resultant internal responsivity was determined to be 0.115 A/W, which correlates to an internal quantum efficiency of approximately 22.4 %.

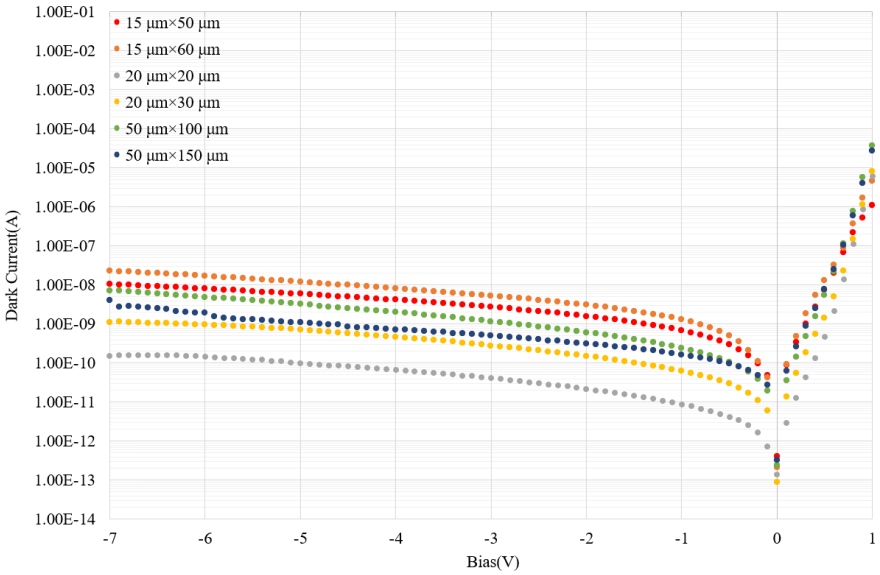


Figure 3-7. Dark current measurement of PDs with different areas.

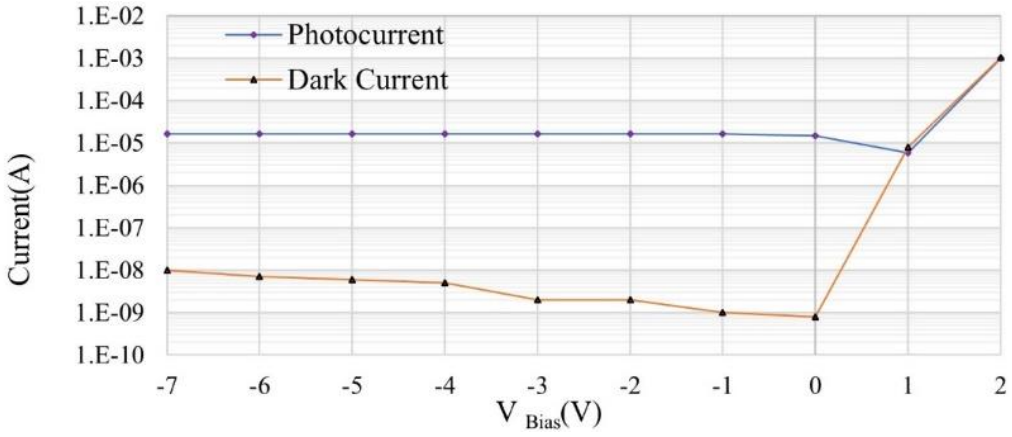


Figure 3-8. Measurement of 20×40 μm^2 PD over 1 μm waveguide with 890 μW available optical power at the fiber tip.

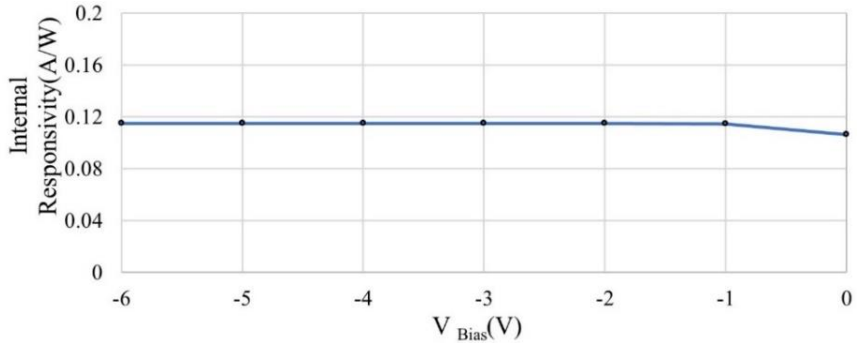


Figure 3-9. Responsivity of 20×40 μm^2 PD over 1 μm waveguide.

To evaluate the bandwidth of the devices, measurements of the PD junction capacitance were conducted using an HP 4275A multi-frequency LCR meter, set to operate at 1 MHz. Figure 3-10 illustrates that the 15×20 μm² PD achieves full depletion at -5 V bias voltage, exhibiting a junction capacitance of 45 fF. This value is close enough to the expected value of 57 fF derived from the design parameters (Table 3). Considering the contact resistance, the estimated RC-limited bandwidth for this device, when connected to a 50 Ω external load, is calculated to be 16.4 GHz using equation (1.7) with a total series resistance of 170 Ω. The stability of C_j values over reverse bias shows nearly the full depletion of the PDs even close to zero bias.

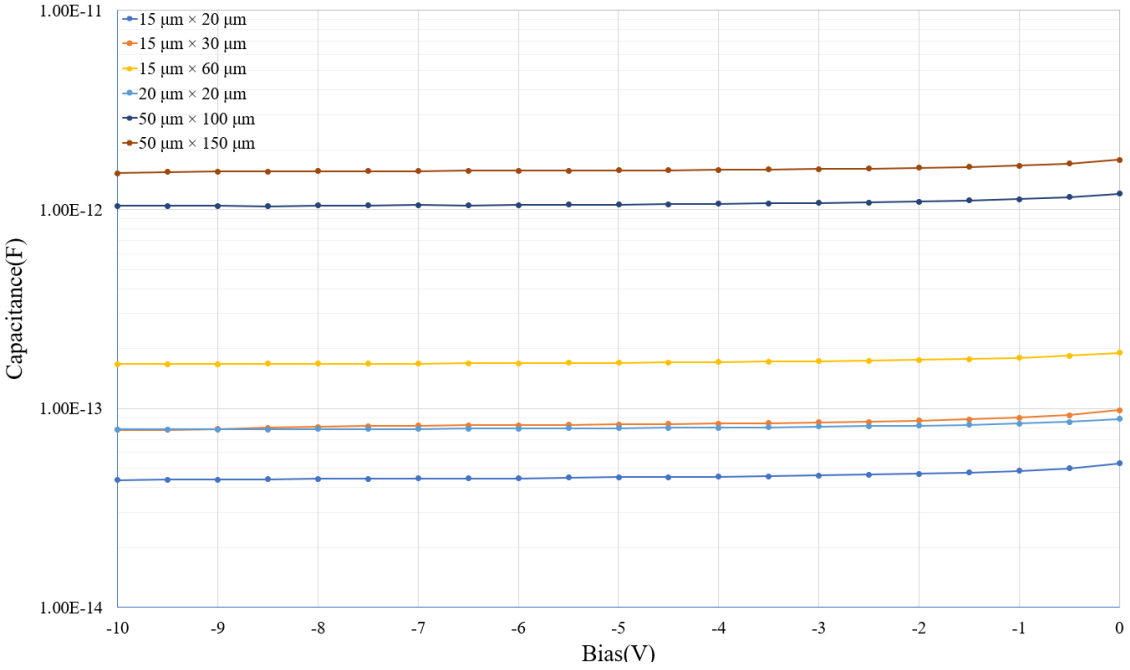
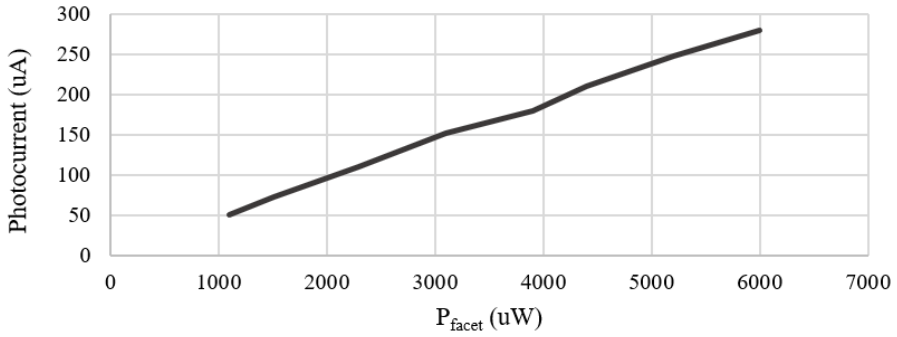
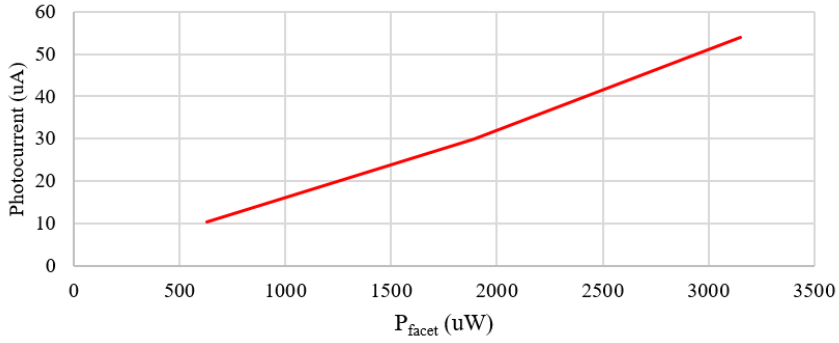


Figure 3-10. Junction capacitance measurements of PDs with different areas.



(a)



(b)

Figure 3-11. Photocurrent vs. fiber tip available power for 50×100 µm^2 device on 2.4 µm WG, V_{rev}= -5 V (a) 780 nm (b) 635 nm

Figure 3-11 illustrates the variation in PD photocurrent as a function of optical power present at the facets at 635 nm and 780 nm wavelengths confirming the linear behavior of QE over the input power. Figure 3-12 shows the relationship between the PD's responsivity and its physical length, demonstrating that an increase in the length of the n-type mesa (i.e. absorber) resulting in enhancing absorption, thereby improving the responsivity. Figure 3-13 presents the QE metrics for the 50×150 μm² PD. These values were derived by accounting for optical coupling losses including 4.5 dB for the 780 nm wavelength, 7 dB for red, and 8.5 dB for green at the facets. These losses, attributed to optical scattering, reflection, and mode mismatch, were conservatively estimated based on the fiber-to-fiber loss measurements of an uncladded waveguide situated on the identical chip. Given these considerations, the calculated power availability at the PD, is approximately 390 μW for 780 nm, 129 μW for red, and 92 μW for green wavelengths. Using red handheld source, the output power at the fiber tip was measured at approximately 650 μW, employing both PM20 and Newport power meters. This measurement signifies that the fiber insertion loss, encompassing the transmission from the laser source to the fiber tip, this time measured to be 1.87 dB.

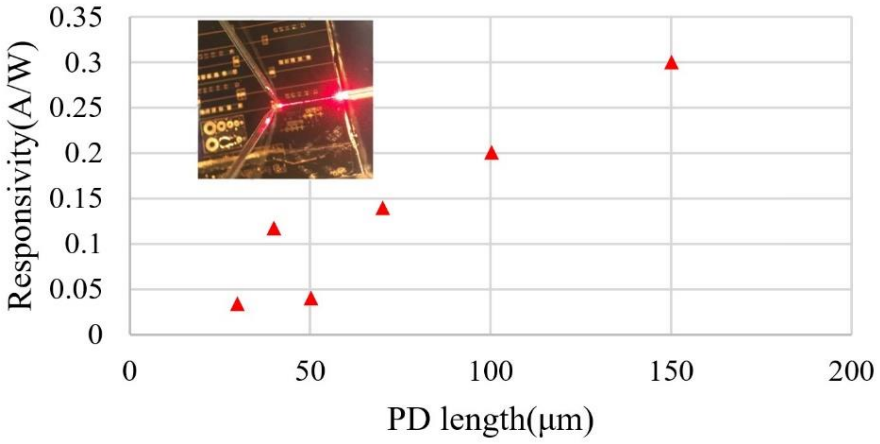


Figure 3-12. Internal responsivity vs. WGPD length @635 nm for red wavelength, PD bias=-5 V.

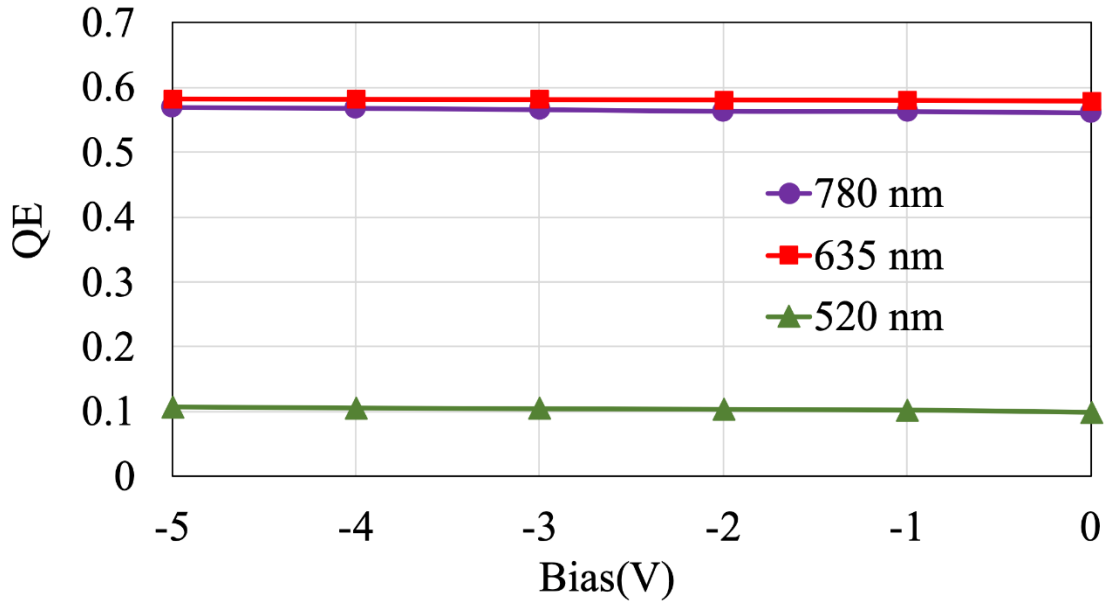


Figure 3-13. QE measurement of 50×15 μm^2 on 5 μm WG for red (635 nm), 780 nm and, green wavelengths

To elaborate more, optical fiber coupling loss refers to the loss of optical power that occurs when light is being coupled between an optical fiber and another optical device such as waveguide.

Several factors contribute to fiber-chip coupling losses:

- **Mode mismatch**: the mode field diameter represents the effective width of the light beam in the fiber. A mismatch in MFD between connecting fibers can cause a portion of the light to not overlap perfectly, resulting in coupling losses. The simulation showed that we would expect around 7 dB/facet for red and 5 dB/facet loss for 780 nm wavelengths for a beam spot diameter of 2.5 μm into a waveguide of 5 μm wide (Figure 3-14). This also depends on the vertical position of the fiber related to the facet (Figure 3-15).

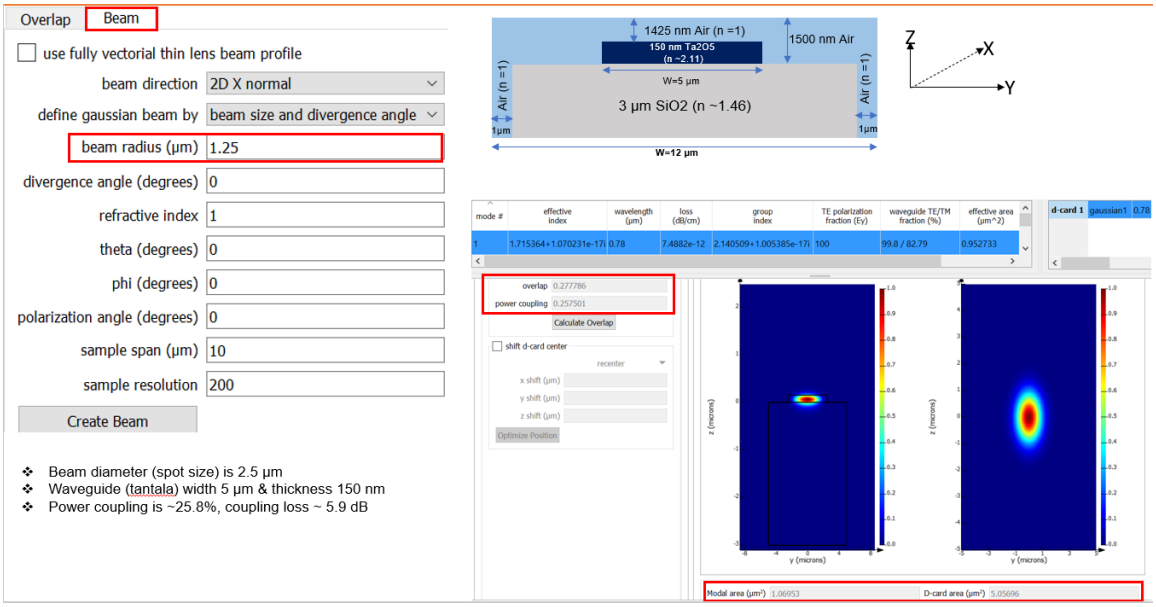


Figure 3-14. Fiber-chip coupling simulation (W= 5 µm) @780nm.(Credit: T. Fatema)

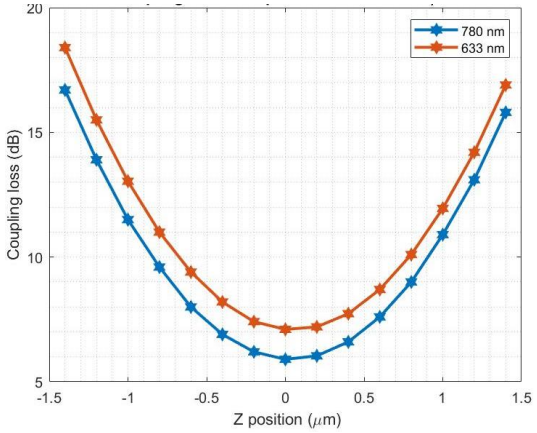


Figure 3-15. Dependency of fiber-chip coupling loss to vertical position of the beam for 2.5 µm spot diameter @ 633 nm and 780 nm. (Credit: T. Fatema)

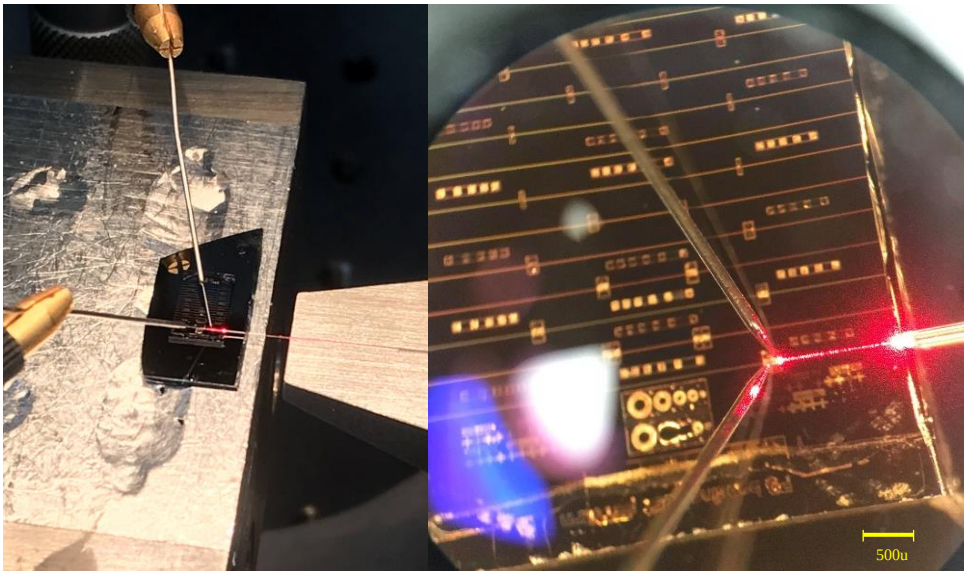
- **Reflections**: if the fibers or the fiber and the device are not perfectly parallel to each other, causing an angle between their cores, the coupling efficiency decreases. This angular misalignment can lead to a significant portion of light missing the receiving core. Assuming normal incident of the beam into the facet core, we have around 13 % of the beam power reflected using Fresnel equation (3.1):

$$R = \left|\frac{n_2 - n_1}{n_2 + n_1}\right|^2 \qquad (3.1)$$

Which is already included in the total loss of Figure 3-15.

- End-Face Separation: a physical gap or separation between the fiber ends or between a fiber end and a device can cause diffraction of the light beam, which reduces the amount of light that is coupled. That why we're willing to keep the fiber tip to facet distance close to working distance of the fiber which in case of our fiber is 10 µm.

- Facet Quality and scattering loss: as I comprehensively discussed in the first chapter, one of the challenges of the WGPD fabrication is keeping the waveguide facets undamaged. Imperfections on the fiber end faces, such as scratches, dirt, or poor polishing, can scatter and reflect light, leading to the scattering loss. Clean, well-polished fiber ends are crucial for minimizing this loss. Figure 3-16 shows the setups to characterize PDs at different wavelengths.



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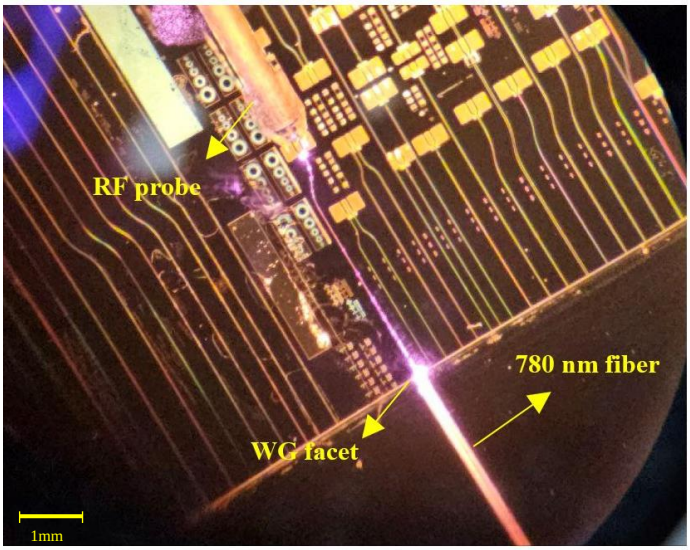

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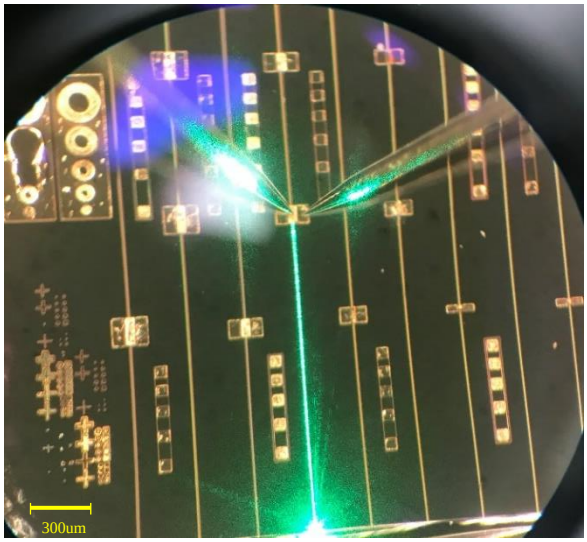


(c)

Figure 3-16. Coupling the light of different wavelengths into the WGPD chip (a) 635 nm (red light) (b) 780nm (c) 520 nm (green light)

3.2.2 Full spectral range QE measurement

Figure 3-17 presents the data on the QE of the top-illuminated PD, obtained through QE characterization setup in Prof. Campbell's laboratory. The QE values were calculated considering factors such as reflection from the device surface and absorption within the upper layers of the PD. These calculated values were derived utilizing equation (3.2) and

are plotted alongside the measured data, showing a match between the calculated and measured QEs for both 635 nm and 780 nm wavelengths [30]:

$$R_{PD} = R_{ideal}(1-R)\left(\underbrace{1-e^{-\alpha_{abs}d_{abs}}}_{absorption}\right)\left(\underbrace{e^{-\alpha_{top,n}d_{top,n}}}_{transmission\ of\ the\ n_{th}\ top\ layers}\right)\ldots \quad (3.2)$$

In this analysis, R_{PD} denotes the actual device responsivity, R_{ideal} represents the ideal responsivity, R corresponds to the surface reflection coefficient, α_{abs} is the absorption coefficient pertinent to the absorber material, d_{abs} specifies the thickness of the absorption layer, $\alpha_{top,\,n}$ defines the absorption coefficient within the n_{th} top layer, and $d_{top,\,n}$ indicates the thickness of the respective top layers. Given our device architecture incorporates three distinct upper layers, namely the $Al_{0.4}Ga_{0.6}As$ contact layer, a 20 nm GaAs n_+cap layer, and a 30 nm n-AlGaAs grading layer, hence, n=3. The transmission coefficient at a wavelength of 785 nm for these top layers exceeds 99 %, permitting the assumption of their transparency. Conversely, for the red wavelength at 635 nm, the analysis proceeds as follows:

R_{ideal}= 0.512 A/W (@635 nm)

R=0.32 (from air to $Al_{0.4}Ga_{0.6}As$)

GaAs absorption coefficient =0.9 (d_{abs}=600 nm, α_{abs}~38000 cm^{-1}) [25]

$T_{n\text{-}Grading}$=0.94 ($d_{n\text{-}Grading}$=30 nm, $\alpha_{grading}$>20000 cm^{-1})

$T_{n\text{-}Cap}$ =0.92 ($d_{n\text{-}Cap}$=20 nm, $\alpha_{n\text{-}Cap}$~38000 cm^{-1})

$T_{n\text{-}Contact}$=0.83 ($d_{n\text{-}Contact}$=270 nm, $\alpha_{n\text{-}Contact}$~6500 cm^{-1})

Derived from the above analysis, the resultant R_{PD} is quantified at 0.225 A/W, corresponding to a QE of 43.7 %, as depicted in Figure 3-17. Considering the specific case for a wavelength of 785 nm, it is assumed that the transmission coefficients across the top interfaces are unity (T=1). Thus, the analysis proceeds under this assumption:

R_{ideal}= 0.63 A/W (@785nm)

R= 0.29 (from air to $Al_{0.4}Ga_{0.6}As$)

GaAs absorption coefficient = 0.56 (d_{abs}=600 nm, α_{abs}~13800 cm^{-1}) [25]

This analysis yields an R_{PD} of 0.25 A/W, corresponding to QE of 39.3 %, as illustrated in Figure 3-17. Under the assumption of negligible reflection at the surface of the top contact layer and complete transparency across all upper layers, the resultant QE is estimated at 90 % for red (635 nm) and 56 % for 785 nm wavelengths, respectively. Furthermore, the quantum efficiency for the largest WGPD on the chip is measured at 58 % for red and 56 % for 785 nm wavelengths, surpassing the top-illuminated PD's quantum efficiency as presented in Figure 3-17. This improvement can be attributed to the evanescent coupling mechanism, which facilitates more efficient absorption in GaAs compared to surface-normal coupling. As it's shown on Figure 3-17, the QE for Green light is a little higher than 10 %, which can be attributed to the high absorption of the intermediate layers and the recombination of the generated carriers in the contact layers.

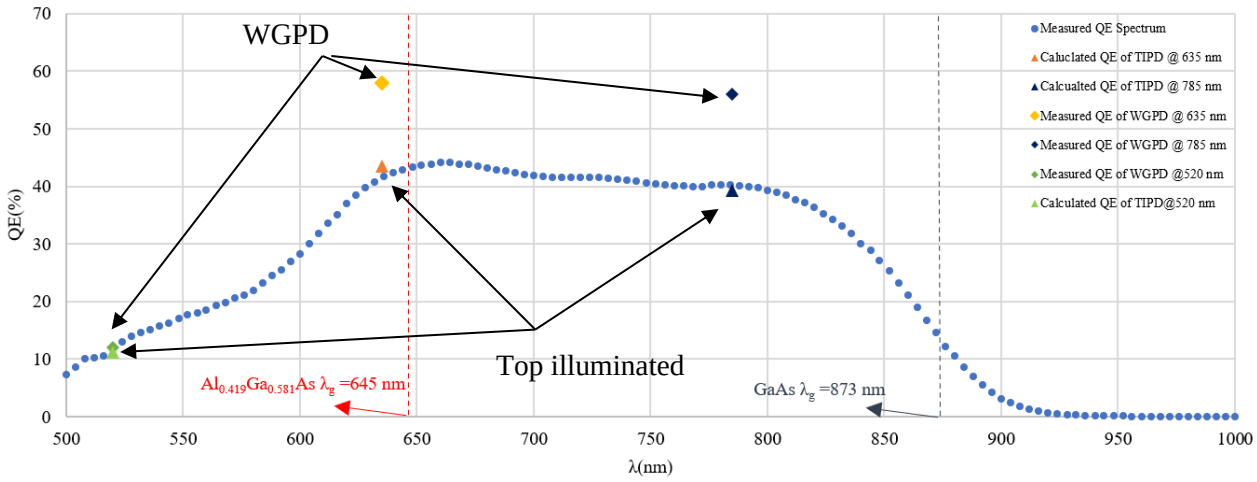


Figure 3-17. QE spectrum of 208 µm top-illuminated circular PD

Figure 3-18 shows the photocurrent spectrum of the same device. Considering the autocalibration process the tool has done to compensate for the reflection from the top surface to generate QE data (but no calibration on photocurrent data), the photocurrent at red wavelength is lower than 780 nm which means the reflection is higher in former than latter so the responsivity is slightly lower confirming our calculation above (0.25 A/W for 780 nm and 0.225 A/W for 635 nm).

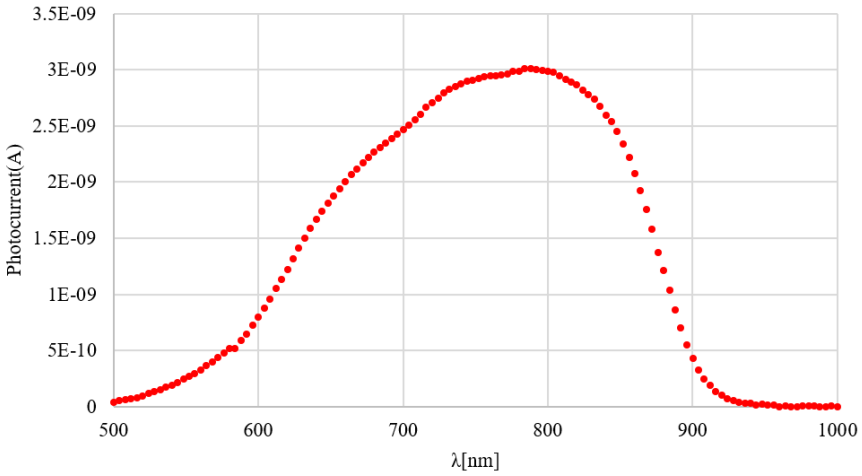


Figure 3-18. Photocurrent spectrum of 208 µm top-illuminated circular PD

3.3 Transient time analysis

Optical pulse measurement of photodetectors involves evaluating the response of a photodetector to short-duration light pulses. Figure 3-19 shows our pulse measurement setup. To generate the required pulses, I used the following sources:

- Alphalas PICOPOWER-LD-635-FCP 635 (±5) nm.

Agilent 50 GHz sampling scope and Agilent 10 GHz real time scope were used to measure the electrical signals generated by the PD. Key parameters, including rise time, fall time, and responsivity, are analyzed to evaluate the PD's high-speed performance. I also used a 25 GHz E4440A Agilent ESA to monitor the frequency spectrum of the output signal. A polarization controller ensures that the pulse's polarization matches the optical system being tested, minimizing the polarization-dependent losses.

I used a single mode (SM) 532 nm tapered fiber for red plus patch cord to minimize FC/APC loss. A 40 GHz GSG probe collects the generated electrical pulse by the PD and transfers it to the bias Tee (BT) to separate out the DC and RF components. The BT RF output is then connected to the oscilloscope or ESA. What I aim to measure here is how much delay the PD adds to the pulse response parameters which helps us to characterize the transient behavior of the device at 635 nm.

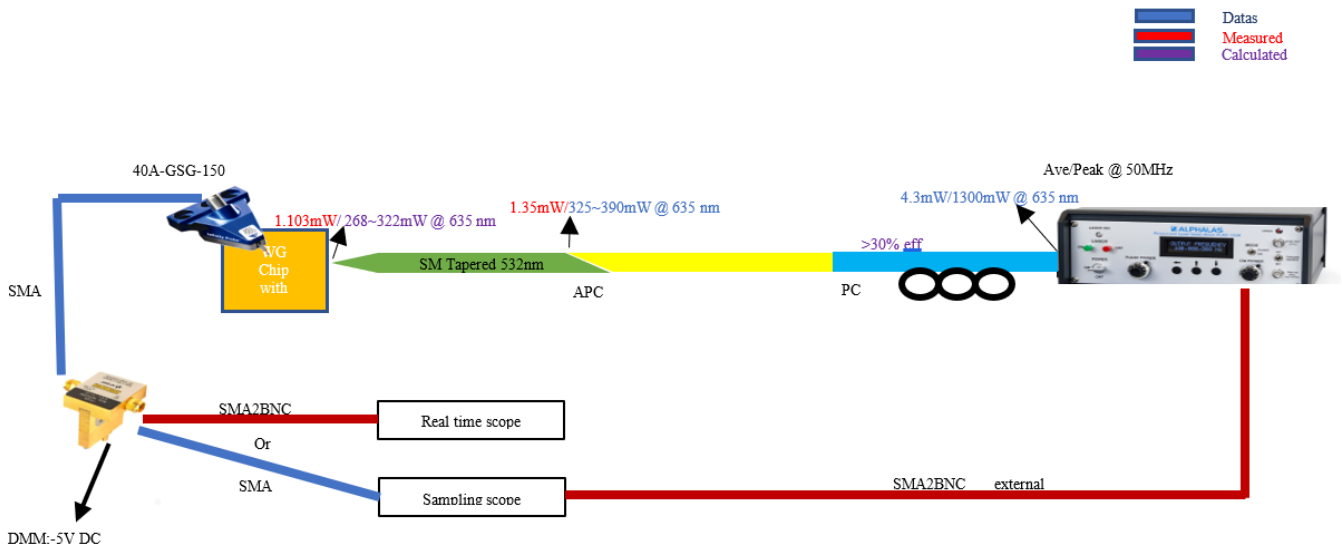


Figure 3-19. Pulse setup to measure transient time response of the visible PD at red wavelength.

The experimental setup utilized the Alphalas PICOPOWER-LD-635-FCP fiber-coupled red laser as the illumination source. This laser emits pulses with a duration as short as 50 ps with a repetition rate of 50 MHz, delivering an average power of 1.35 mW. The pulse profile provided by the manufacturer is depicted in Figure 3-20. Prior to initiating the measurements, the bandwidth of the BNC cable, both with and without BT, was evaluated using a real-time oscilloscope and a signal generator. The assessed bandwidth did not exceed 10 GHz.

Figures 3-21 and 3-22 illustrate the pulse response plots obtained from PDs of two different dimensions. The calculated parameters pertaining to each pulse are detailed within the respective plots.

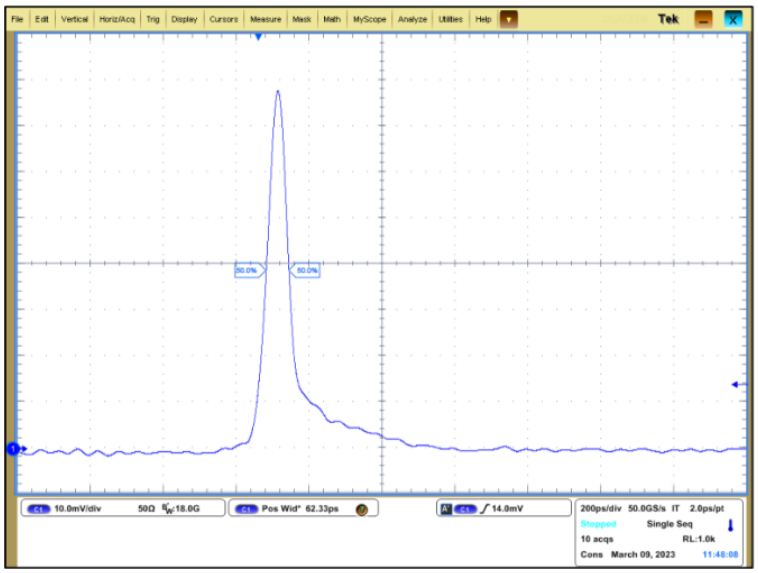


Figure 3-20. Pulse output of the source at 50 MHz repetition rate, average power = 1350 μW; pulse width (after deconvolution) = 65 ps; Peak power = 390 mW.

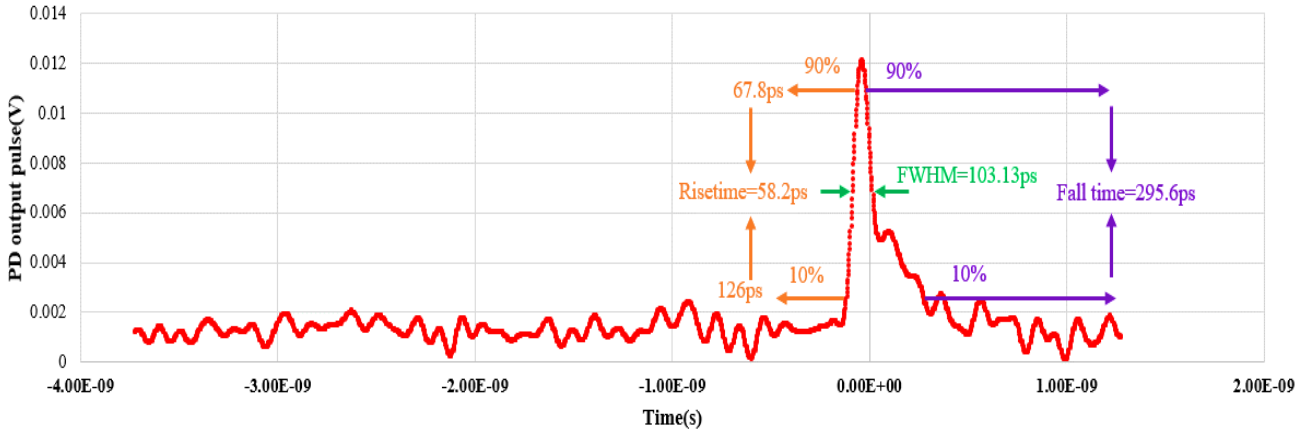


Figure 3-21. 20×40 μm^2 rectangular WGPD on 0.6 μm WG, -5 V, 2 μA, 50 MHz 635±5 nm pulse average 1.35 mW into SM532

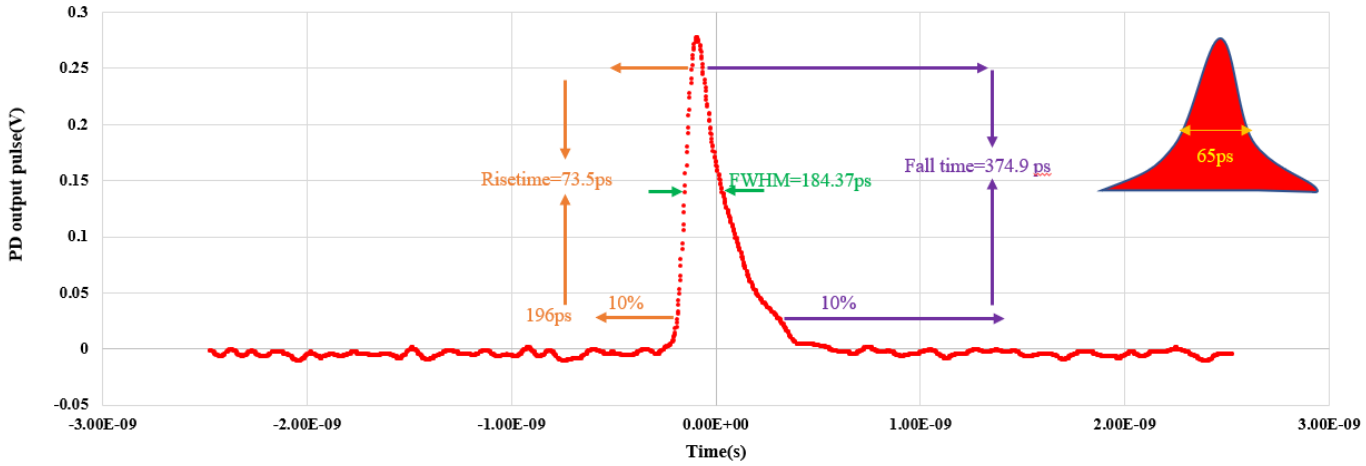


Figure 3-22. 50*100 μm^2 rectangular WGPD#5 on 3μm WG, -5V, 73μA, Gaussian optical beam, 50MH, 635±5nm, Average 1.103mW @ SM532 tip into the WG facet, Peak 325~390 mW

The analysis of the above figures reveals that the transient response parameters for the bigger devices exhibit longer durations compared to those of the smaller ones, indicating a slower response in the larger device. Additionally, Figure 3-23 demonstrates that the pulse response of the 15×20 μm² photodetector, situated on a 5 μm waveguide, remains largely unaffected by the bias voltage.

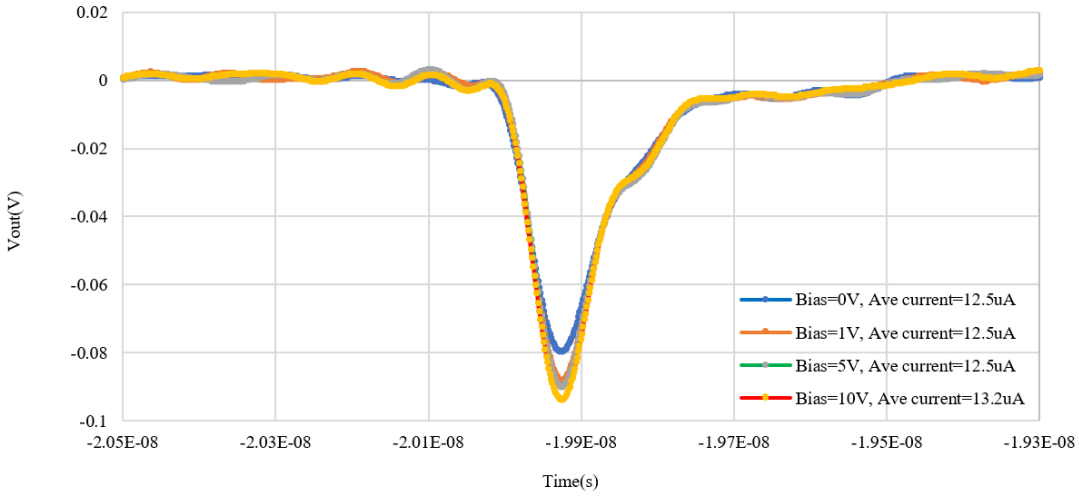


Figure 3-23. Pulse response of 15×20 μm^2 PD on 5 μm waveguide-50 MHz vs PD bias, input power set on max.

Also, Figure 3-24 shows the independent behavior of transient parameters of the pulse response over PD bias even at zero bias. To estimate the bandwidth of the devices, I employed an intensity modulator which will come in the next section.

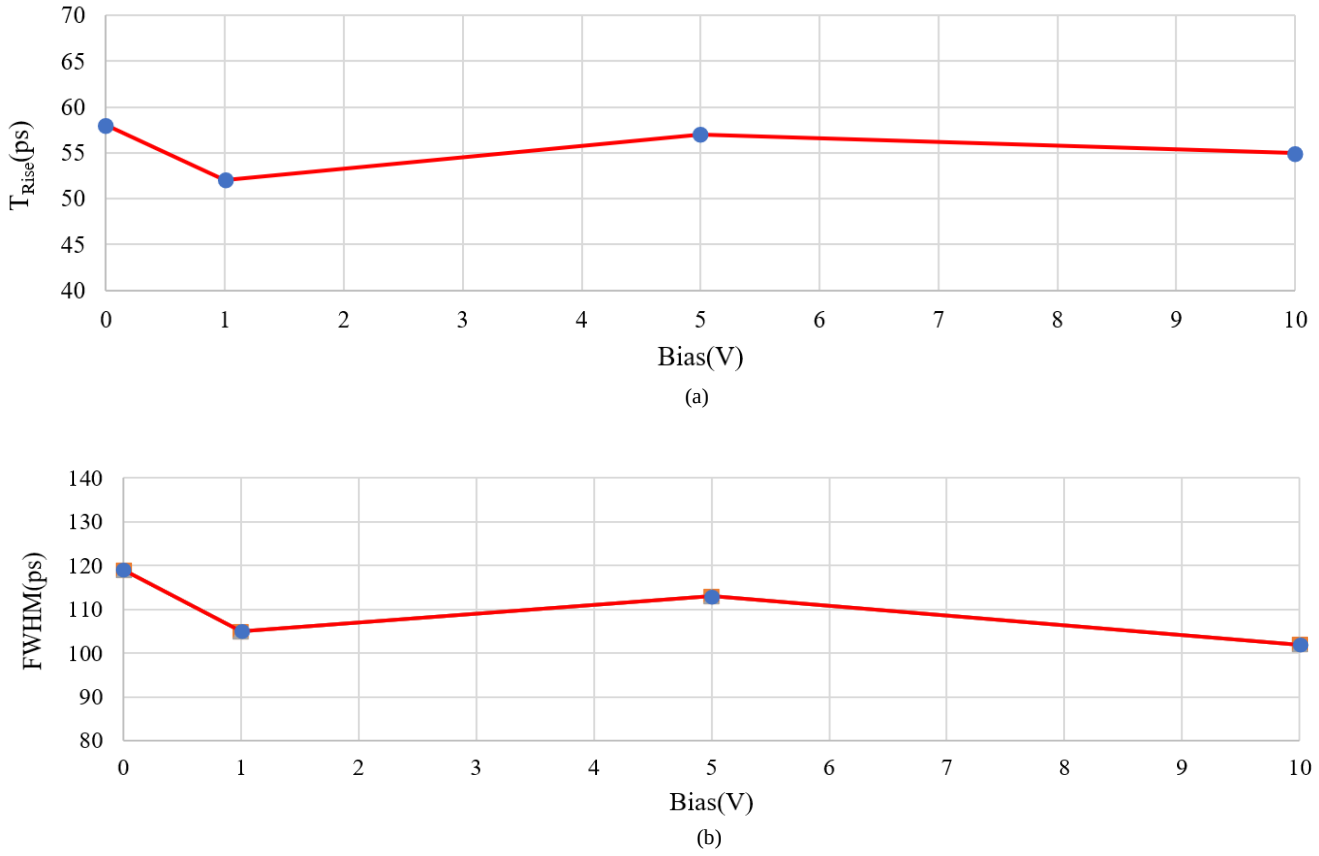


Figure 3-24. Bias dependency of the transient parameter of the impulse response of 20×20 μm^2 WGPD on 4 μm waveguide. Power Source set @ 50 MHz and, max power @ red (635 nm) wavelength (a) Rise time vs Bias.(b) FWHM vs Bias

A hurdle in accurately assessing the device's bandwidth via the pulse technique is calibration, which involves numerous uncertainties. This necessitates taking into account the latency and variations in signal amplitude and phase introduced by each component in the setup, including oscilloscopes, BNC connectors, SMAs, BT, and RF probes, to accurately determine the pulse response. In other words, to get the right amplitude response, we need to compensate for both phase and amplitude of each element in the setup. By performing a fast Fourier transform (FFT) on the input pulse, the resultant pulse bandwidth does not exceed 4.8 GHz, as depicted in Figure 3-25. This bandwidth is insufficient for capturing the high-speed response of PDs.

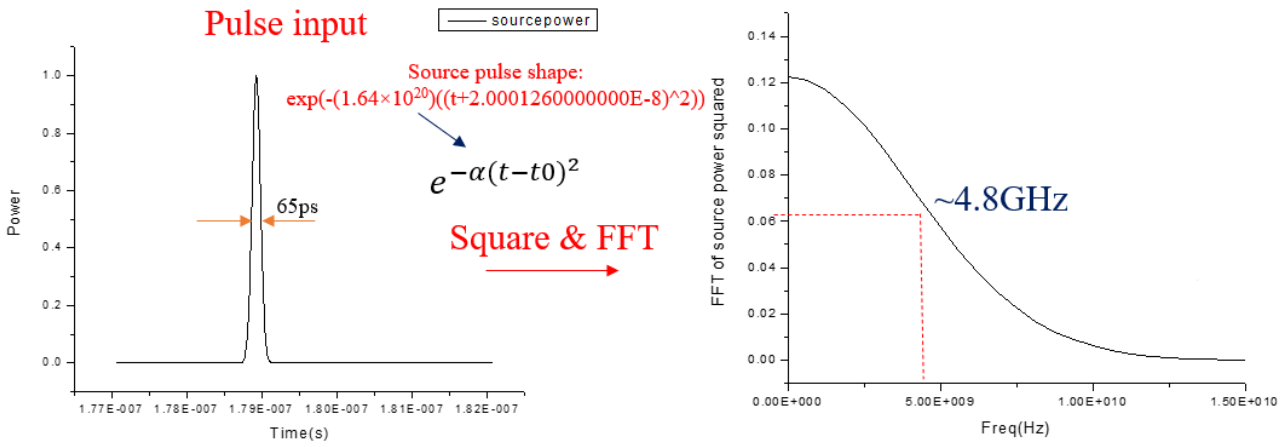


Figure 3-25. Bandwidth of the Alphalas input pulse @ 635 nm by taking FFT of the input pulse in time domain.

3.4 Bandwidth measurement

One of the most common types of optical modulators is the electro-optic modulator. Optical intensity modulation has an extensive range of applications. It is crucial in telecommunications for encoding data onto optical carriers, improving signal quality, and enabling high-speed data transmission. Here I used a common type of electro-optic modulator i.e. MZM modulator that uses the Mach-Zehnder interferometer configuration to modulate the intensity of light which was described earlier in chapter 1. The two paths later recombine, and the interference between the modulated and unmodulated light creates an output signal with intensity variations corresponding to the applied electrical signal. Figure 3-26 shows the optical modulation setup I used to measure the bandwidth of our devices.

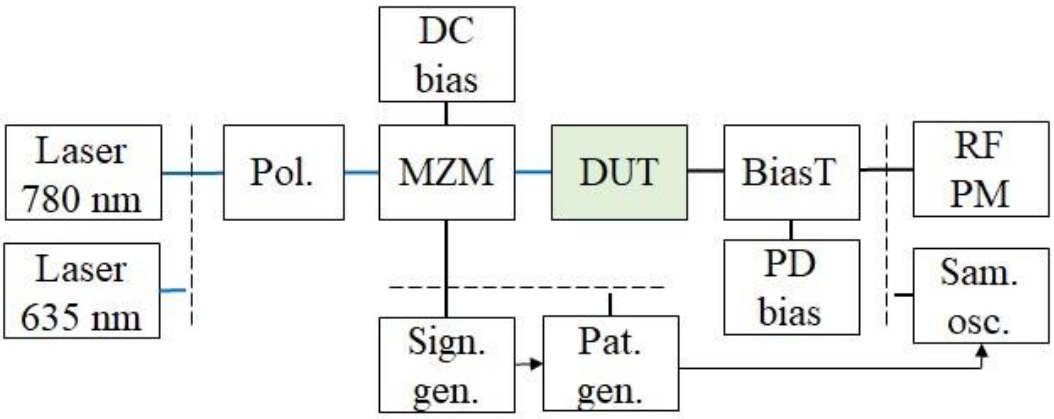


Figure 3-26. Bandwidth measurement setup of visible PD using MZM modulator.

To ensure minimal distortion in the modulated signal, it is imperative to set the operating point of the modulator to the quadrature point (half_$V_{\pi i}$) of its transfer function. The modulator in question, an NIR-MX800nm-LN-20 wide bandwidth amplitude modulator supplied by Exail, boasts an electro-optical bandwidth exceeding 20 GHz optical bandwidth (Figure 3-27) , with a $V_{\pi i}$ approximately 4 V and an operational bias point at half_$V_{\pi i}$ of 3.1 V.

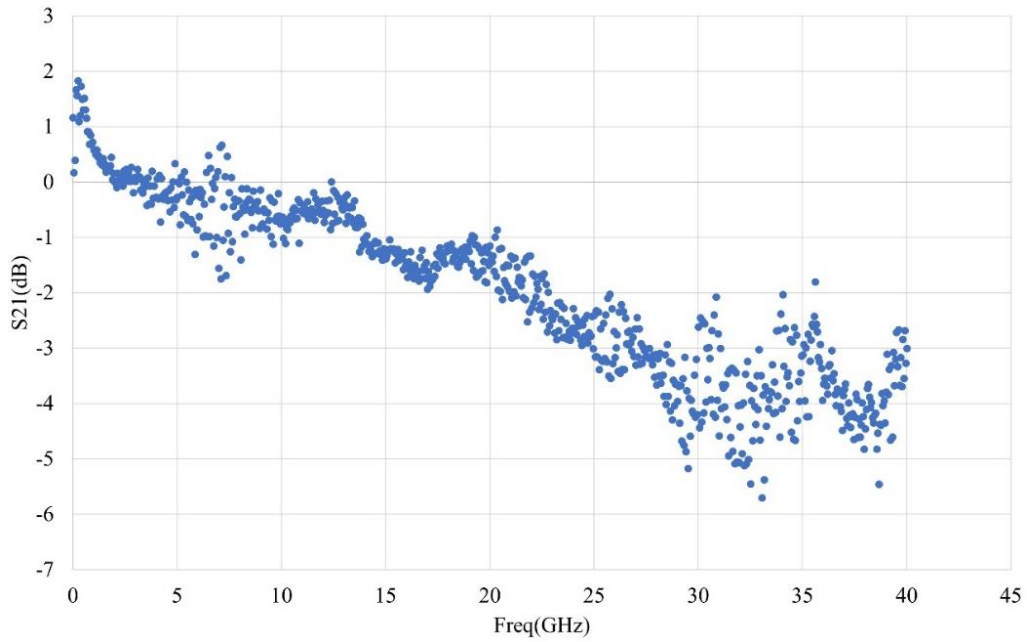


Figure 3-27. MZM(NIR-MX800nm-LN-20) EO response

The RF input power was set to around 12 dBm to avoid distortion. Additionally, adjustments were made to the Anritsu power meter calibration factor across various frequencies to ensure that the noise floor was optimized to a level below -72 dBm using the tool setting and the calibration table was embedded in. To verify the modulator maximum modulation depth across specific frequencies, preliminary measurements of the PD output signal were conducted using an 86100C Infiniium sampling oscilloscope, externally synchronized with the modulator's RF source. Figure 3-28 displays the output from 20×20 μm² PD at 10 GHz and 25 GHz.

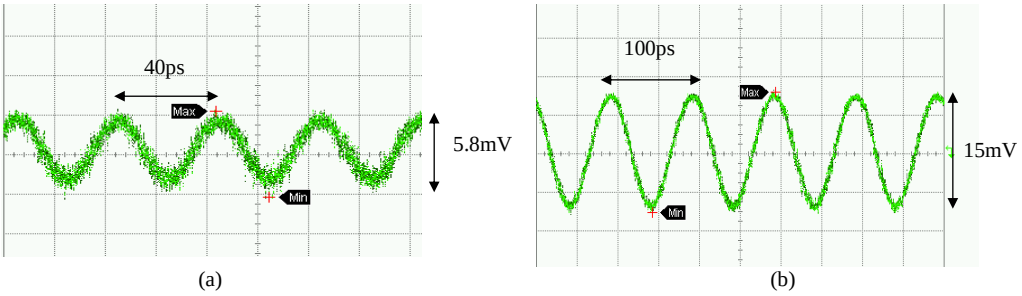


Figure 3-28. The output RF signal of the 20×20 μm² using modulator setup. PD bias=5 V, PD I_{ave}=0.5 mA, modulator RF power=12 dBm, modulator half-V_{π} bias=3.1 V (a) 25 GHz signal (b) 10 GHz signal.

Figure 3-29 plots the frequency response of a 15×20 μm² device integrated on a 5 μm waveguide, measured at two distinct average photocurrent levels. This analysis substantiates a bandwidth of approximately 17 GHz for the device independent of the PD average current. Under the premise of achieving maximal modulation depth (near 100 %), it is observed that an increase in the average photocurrent correlates with an enhanced extraction of the RF power from the device.

Figure 3-30 shows the RF output power dependency on the devices size which is an inverse relation. The 3-dB bandwidth that can be read from Figure 3-30 for each device match well with the calculated RC-limited bandwidths of the devices from the table 3 after calibrating the measured data.

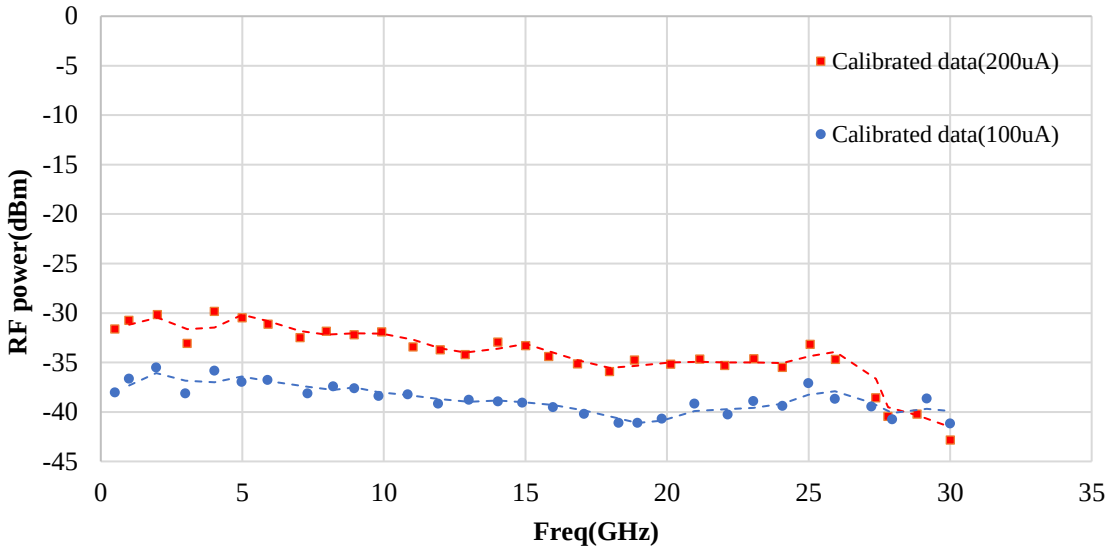


Figure 3-29. Output RF power of a 20×15 μm^2 WGPD on 5 μm WG. The measurement parameters are as follow: PD bias=5 V, Modulator RF power=12 dBm, Mod bias=3.1 V, and the laser source current of 265 mA

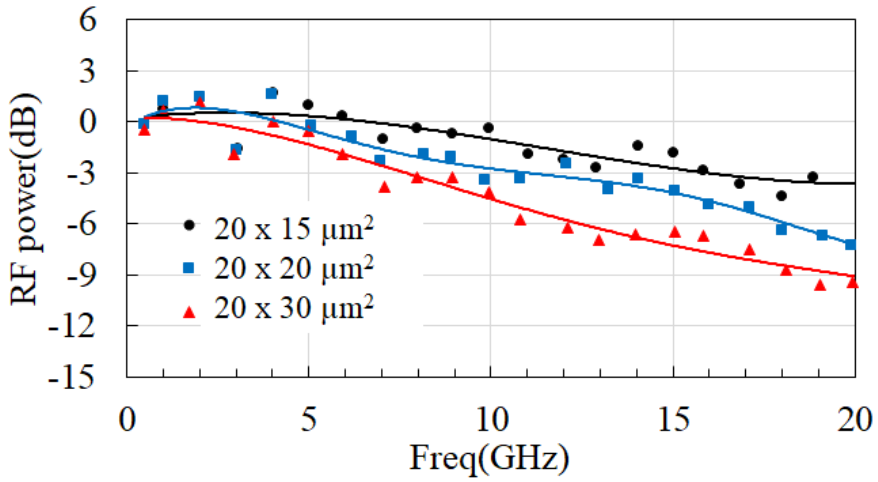


Figure 3-30. Normalized RF power vs device size. PD bias=5 V, PD average current=200 μA, Mod bias=3.1 V, Mod RF power=12 dBm, laser current=385 mA.

Figure 3-31 presents the measured RF power output from a 20×15 μm² device under illumination of a red wavelength source, post-subtraction of noise from the calibrated data points. The resultant plot indicates a bandwidth for the red wavelength that is nearly identical to what was observed at 780 nm, as depicted in Figure 3-30. This observation implies that the bandwidth characteristics of the devices exhibit no significant wavelength dependence.

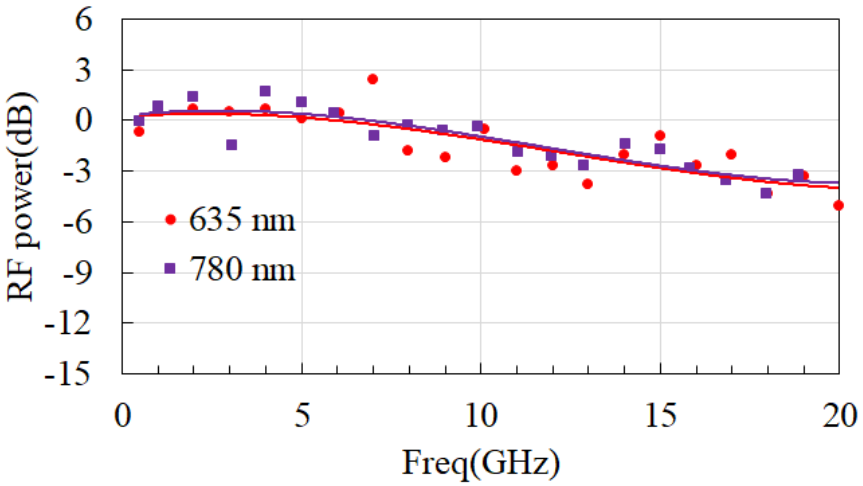


Figure 3-31. Normalized RF power of 20×15 μm^2 for red (635 nm) and 780 nm wavelengths. Coherent laser has been used as the optical source for red light and the power meter was replaced by an externally triggered E4440A Agilent spectrum analyzer to collect the data points.

3.5 Eye diagram

In optical communication, an eye diagram is a fundamental tool to visualize and analyze the quality of an optical signal modulation and its transmission characteristics. It is a graphical representation of a superimposed series of optical signal bits over multiple bit periods, allowing for the assessment of signal quality. The eye diagram typically consists of a horizontally repetitive pattern resembling the shape of an open eye, which gives the technique its name. The width of the eye opening reflects signal quality, and its closure indicates the jitter and noise.

To measure the eye diagram of our PD, I employed an Advantest D3186 pulse pattern generator (PG). A 50 GHz signal generator provides the input pulse to the "clock" input of the D3186, as illustrated in Figures 3-32 and 3-33. Subsequently, the external trigger of the instrument was connected to the standard trigger input of the oscilloscope, or alternatively, the "clock1" output was linked to the precision time base (PTB) input of the oscilloscope. Although both connections yield equivalent signals for the same input amplitude at lower frequencies, the PTB input is preferred for enhancing signal quality at higher frequency ranges. Eventually the PG data output provides the input to the RF port of the modulator.

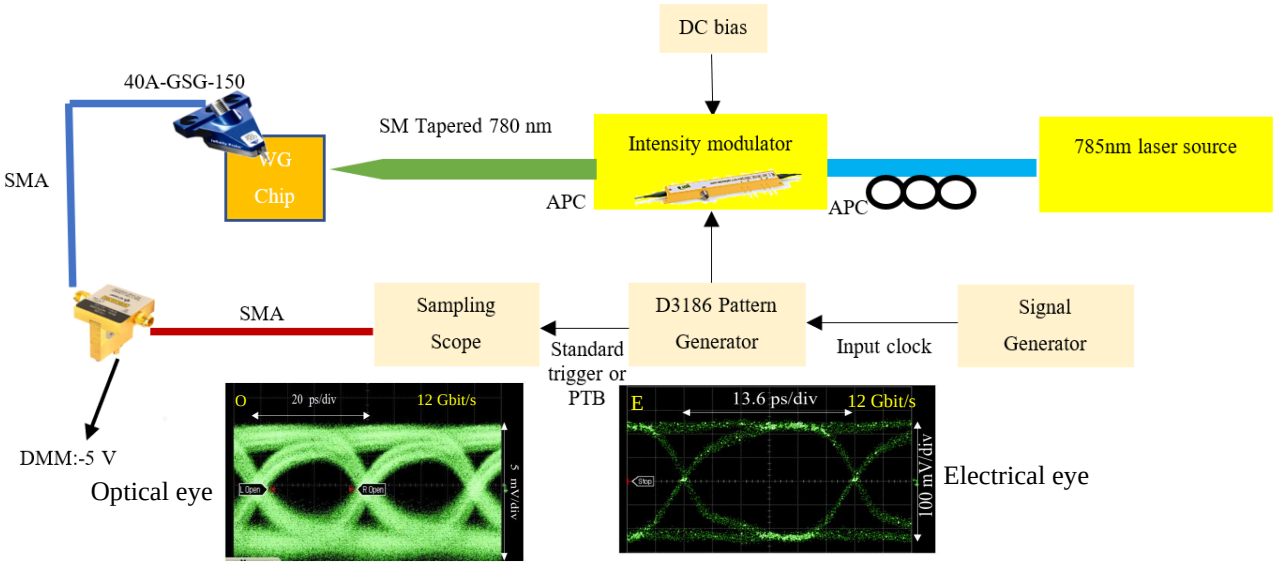


Figure 3-32. Eye diagram measurement setup using pattern generator.

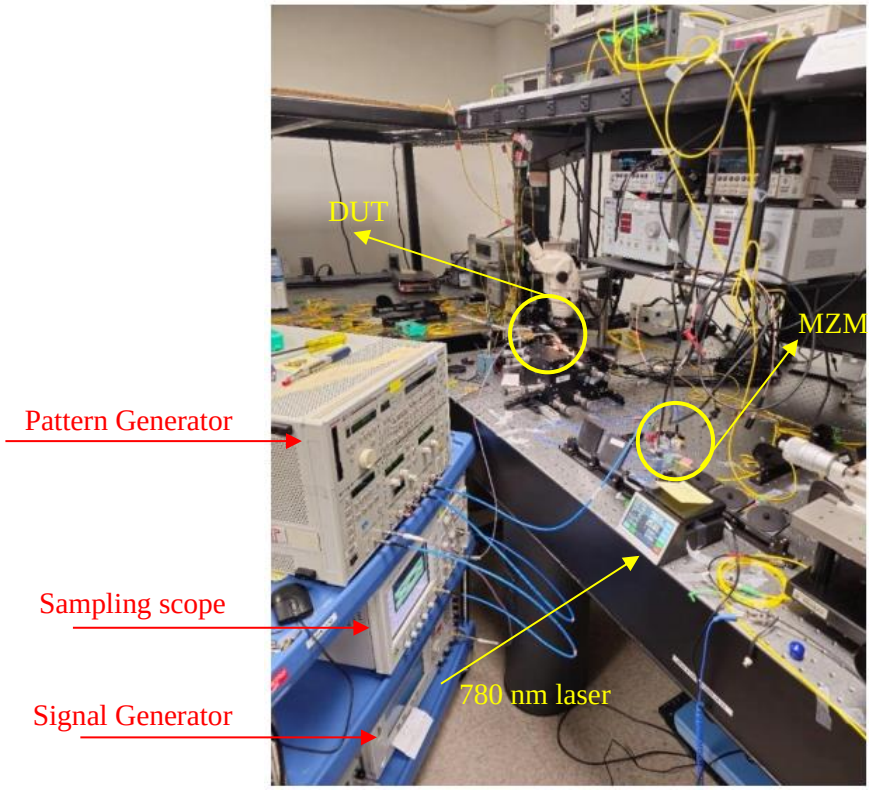


Figure 3-33. Measurement setup to evaluate the PD eye diagrams.

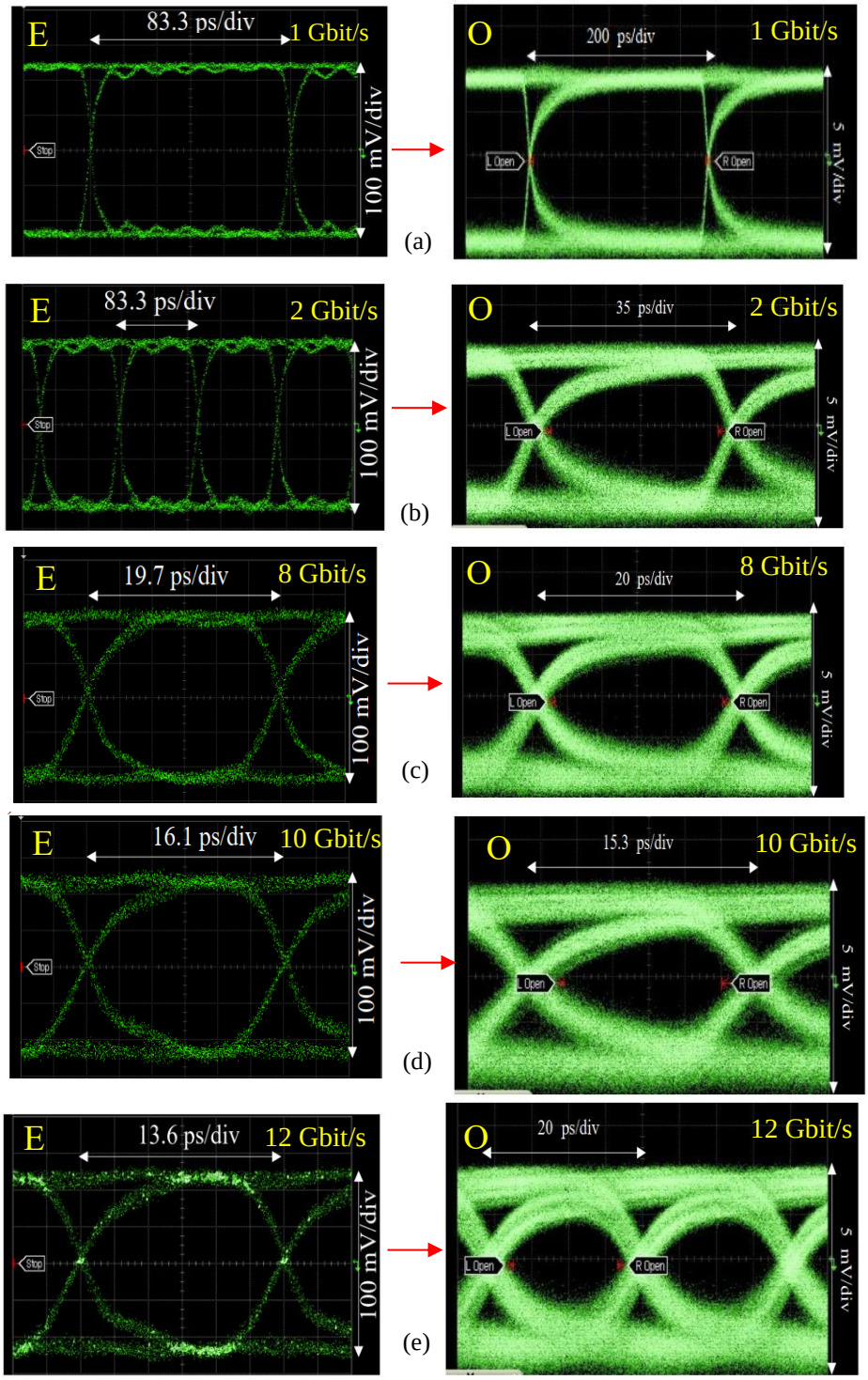


Figure 3-34. Eye diagram of 15*20 μm^2 PD on 5 μm waveguide (right side) at 780nm, electrical eyes on the sampling scope (left side, no DUT), signal and clock amplitude= 0.5 V_{p-p} (scope input limit), PD bias=5 V, PD current=0.5 mA, laser current=360 mA, mod bias=3.1 V, data p-p=2 V, clock p-p=0.5 V, RF input power to D3186~0 dBm (a) 1 GHz signal, standard trigger (b) 2 GHz signal, standard trigger (c) 8 GHz signal, PTB (d) 10 GHz signal, PTB (e) 12 GHz signal, PTB.

The left side on Figure 3-34 depicts the output from the D3186 PG (electrical eyes) as it is directly interfaced with the sampling oscilloscope over various frequencies. The

resulting plots serve as a benchmark for evaluating the eye patterns produced by the PDs. The right side on Figure 3-34 shows the eye diagram (optical eyes) of 15×20 μm^2 PD on 5 μm waveguide. Figure 3-35 presents the 12 GHz eye diagram of the device across varying bias points, substantiating that the frequency response of the PDs exhibits a notable DC bias independency. Furthermore, it demonstrates that the PD maintains a satisfactory frequency response, even at zero bias.

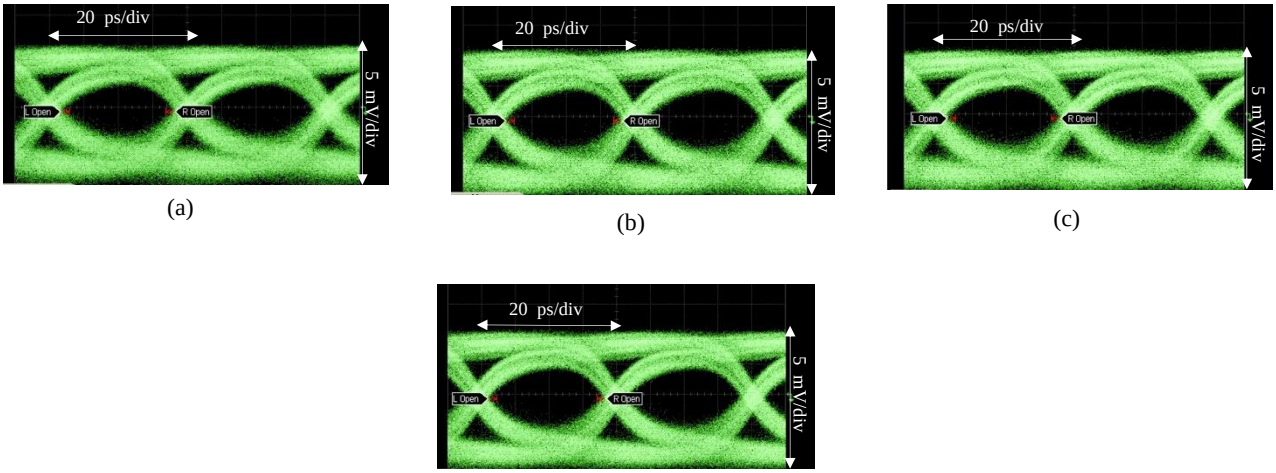


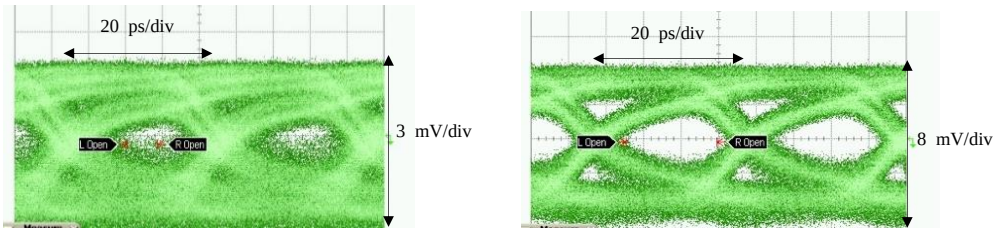
Figure 3-35. Voltage independency of eye diagrams of 15*20 μm^2 PD on 5 μm waveguide. PD bias=5 V, PD current=0.5 mA, laser current=360 mA, Mod bias=3.1 V, Data p-p=2 V, Clock p-p=0.5 V, Mod input RF=0 dBm. (a)0 V (b)1 V (c) 5 V (d) 10 V

Table 10 provides the results of the measuring such parameters for 15×20 μm^2 PD which are inversely related to the data rates for the single PD.

Table 10. Eye diagram parameters. of 15×20 μm^2 PD on 5 μm waveguide. PD bias=5 V, PD current=0.5 mA, laser current=360 mA, Mod bias=3.1 V, Data p-p=2 V,

Data rate (Gbit/s)	Bias (V)	Eye height(mV)	Eye S/N	Eye Width(ps)
1	5	15	15	962
5	5	8.8	6.26	169
8	5	7.8	5.72	97
10	5	5.2	4.53	67

Figure 3-36 shows that by operating the 20×20 μm^2 PD on 5 μm waveguide in the gain region, the eye diagram parameters are improved. This means that the noise added by operating the PD in gain region is not a hinder in improving the open eye diagram parameters.



(a) (b)

Figure 3-36. Effect of running 20*20 μm^2 PD in gain region on the eye diagrams. 12 Gbit/S, Laser current fixed @ 300 mA, mod bias fixed @ 3.1 V, 2 V data $_{p-p}$, 0.5 V clock $_{p-p}$, 0 dBm Mod RF input. (a) PD bias=-5 V, PD current= 0.184 mA, dark current= 100 pA (b) PD bias=-21 V, PD current= 0.726 mA, dark current= 0.538 mA

3.6 Conclusion

This is the first time that PDs have been successfully integrated on tantala waveguide platform. I developed a fabrication process and showed the DC and RF characterization. It's worth noting that most commercial visible Si PDs are top illuminated not on WG platforms.

Table 11. Overview of the recent works on integrated visible detectors

Type	Integration Technique/platform	Center λ (nm)	R (A/W)	QE (%)	BW	Dark current (pA)	Ref
Si APD	Mon*.Si WGPD/Si_3N_4	685	0.65 ± 0.18	max	30 GHz/ 56 Gbps	120±10	2021 [79]
InGaN/GaN PD	Mon. GaN WGPD/GaN on Si	452	*N.R***	*N.R*	250 Mbps	1-10	2018 [80]
Si PIN	Mon. Si WGPD/GaN on Si	488	0.31±0.01	78	*N.R*	178	2021 [20]
Si PIN	Mon. Si WGPD/ Al_2O_3 on Si	405	0.25	76%	*N.R*	1000	2021 [19]

Si PIN	Het**. Si WGPD/ Si_3N_4	775~800	0.195	30	6 GHz	107	2022 [81]
Our work	**Het. GaAs/AlGaAs WGPD/ Ta_2O_5**	**635-780**	**0.3~0.41**	**>58%**	**17 GHz/12Gbit/s**	**20**	**2024**

* Monolithic
** Heterogeneous
*** Not reported

In Table 11, I collected the recent works have been done in visible range PDs which are mostly monolithic not heterogenous integration. According to this table, the main competitor for GaAs to realize visible PDs is Si. Compared to indirect bandgap material (e.g., Si), GaAs absorb light more efficiently and thus may achieve equivalent photosensitivity as Si within much smaller volumes, leading to smaller devices. The highest BW in this table belongs to Si APD which has high power consumption. The other works also use Ge/Si for this purpose which leads to high dark current in the range of 100uA.

The PDs have 100 pA dark current, more than 56% QE between 635 nm and 780 nm wavelengths, and up to 17 GHz bandwidth. I also measured open eye diagrams up to 12 Gbit/s - the upper limit of our experimental setup. The PDs followed the expected behavior including extremely low dark current, high QE (responsivity) and wide bandwidth. In general, I can say these results provide a good basis for the future investigation in the area of the heterogeneous integration of optoelectronic devices in the visible range which can pave the way for a fully functionable visible light photonic integrated circuits.

One of the likely limiting factors in getting 100% QE for the larger PDs is the loss in the metals. A possible improvement could be upgrading the PIN epitaxial structure to UTC or MUTC using which we can improve both bandwidth and QE at 780nm. Regarding the green and red light, another factor comes into play to some degree which is the absorption in contact layers. This is more critical for the green light as we saw in Figure 3-17. In

order to improve QE for shorter wavelengths, one approach would be using a wider bandgap compound for contact layers like InGaP.

It's worth mentioning again that the transit time limited bandwidth or f_T that I calculated in chapter one for the holes as the limiting carriers was more than 100 GHz which means it is not the limiting factor here. On the other hand, by choosing smaller active area PDs like 5×5 μm^2 and further reducing the p sheet resistance, potential record of 100 GHz bandwidth is possible in the future design. The devices' bandwidth measurement agrees well with the calculation values of table 3. I also tried 40 Gbit/s eye diagram setup however there were not open 40 Gbit/s eye diagram due to either PDs or modulator bandwidth limitations.

Chapter Four: Heterogeneous 3D integration of GaAs- and InP-based electronic-photonic devices onto Si using multi-layer adhesive wafer die bonding

4.1 Introduction

Monolithic integration has been the common choice to implement microprocessor, memory chip and microcontroller due to its advantages like simplicity, high miniaturization, and reproducibility [82, 83, 84], however it's not flexible and imposes limited applications when it comes to integrate active devices of different technologies [85]. Therefore, heterogeneous or hybrid integration techniques were introduced.
The development of heterojunctions since then enabled the creation of more complex devices [86, 87, 88, 89]. The increasing complexity of electronic devices and the demand for higher performance, lower cost and power consumption, and smaller form factors are driving the continued development of this technology.

Hybrid integration is a broader concept though that also covers heterogenous integration. Examples are system in package (SiP), system on chip (SoC), and multi-chip module (MCM) [90, 91, 92]. All these hybrid integrations are mature techniques being used by chip manufacturers for decades but still with limited PIC compatibility. The state-of-the-art techniques of hybrid integration for both ICs and PICs are transfer printing (TP) which was introduced in 2006, selective heteroepitaxial growth and wafer bonding.

TP has been emerging in recent years and is still in the developing stage and we used this technique in our group for some of our recent projects [93, 94]. Using this technique adds

major extra processing steps of embedding a sacrificial or release layer to the host substrate and selective etching it for lifting coupons, polymer encapsulation of the devices and carefully devising tethers all around them. Adjusting the speed of lifting coupons using stamp and landing on the target substrate would be other critical steps in using this technique [95]. Other potential issues would be device density limitations and the alignment of the chiplets as it's not being done by lithography [94].

Our group also has tried selective growth process or heteroepitaxy technique as well [96, 97]. Hybrid integration based on selective growth process or heteroepitaxy comes at its own costs among them thermal expansion, lattice mismatch and antiphase boundaries (APBs) which could lead to high density of dislocation, cracks, and defects [98, 99, 100]. Costly complicated highly sensitive heteroepitaxy process keeps it away from being a versatile approach for frequent hybrid integration of III-V or other semiconductor compounds.

Efforts have been made for hybrid integration of III-V materials using wafer bonding as well. In 2010, Bowers *et al.* presented the method of selective area wafer bonding process using graphite and thin Al sheets to compensate for the thickness difference between different epis [101]. The method led to a high yield while the alignment accuracy between the devices of different epis was still around the millimeter range, so not applicable for tight integration of the devices. In fact, wafer bonding has been used for PIC for a long time but when it comes to integrating different Epi material on the same chip, it faces limitation. In this chapter, I will present how to overcome this limitation using adhesive bonding.

4.1.1 EPIC breakthrough

Electronic-photonic integrated circuits (EPICs) represent a groundbreaking technology that merges electronic and photonic components on a single IC [102]. By combining the processing power of electronic devices with the high speed and wide bandwidth

capabilities of photonic elements, EPICs offer a promising path toward overcoming the limitations of purely electronic circuits, especially in the realms of data communication, sensing, and computation.

4.1.2 The proposed EPIC

In what follows, I introduce a universal hybrid technique to integrate EPIC which offers distinct advantages over the other counterparts in terms of alignment accuracy, simplicity, and versatility. The technique is based on SU8 multi-layered bonding and to show the feasibility of the method, I proposed the idea of integrating two dissimilar devices i.e. quasi-vertical GaAs Schottky diode (SD) and InP PD both on SOI substrate. As the early application of these two distinct devices, I used them to realize an RF photonics on chip rectifier.

Even though works has been done in order to co-integration of InP photodiode and GaAs Schottky diodes circuits in separate waveguide packages [103] however as of today, no experimental demonstration of hybrid integration of these two technology on the same substrate exists due to the integration limitations of the two III-V material systems. I used this integration to realize an on-chip RF rectifier as an early application of PD/SD hybrid integration. The DC and RF parameters of the devices have been measured and the real time signal analysis of the RF rectifier will be presented.

4.1.3 Importance of the work

One of the key enabling technologies for hardware and eventual science discovery is the versatile low-parasitic THz Schottky. Its superior advantages over regular PN diodes like low turn-on voltage, faster switching speed ,and ultra-wide bandwidth, compared to PN junction make them a good candidate for a wide variety of applications like mm-wave and THz mixer/multipliers, power detectors, and solar cells [104].

The highly nonlinear behavior of these diodes can be exploited to generate higher order harmonics. One of the requirements of SD-based mixer and multipliers is that they need

to get pumped hard by LO power to get a reasonable IF or mm-wave power and this is where InP-based PDs come into the play. The amount of drive power needed for HEFT (heterojunction field effect transistor) balanced mm-wave mixer is around 5 dBm. This number for SIS (superconductor–insulator–superconductor) mixer is much lower in the range of -20 to -13 dBm [105]. Right now, PDs are exploited in the ALMA project in the front end to pump SIS mixers and they do this in antenna arrays to distribute the LO coherently to all receivers. The ALMA photonic LO system also exploited in the back end (far from the radiation field) [106]. Maintaining the phase difference stability between the antenna elements is a challenge which is complicated and expensive to realize using conventional [105].

InP and its lattice matched compound like InGaAs have been always the choice for implementing PDs in one of the main three optical windows i.e. 1550 nm for its advantages like high responsivity, large optical operational bandwidth and, high power application [107, 108].

4.2 Fabrication and DC characterization

The idea of tightly integrating a Schottky diode with a photodiode is a pioneering approach, yet to be empirically validated due to challenges associated with the heterogeneous integration of these disparate technologies. To this end, a selection was made favoring a quasi-vertical GaAs Schottky diode, a novel development at the University of Virginia, alongside an InP-based PIN PD, both situated atop SOI substrate [109]. The preliminary step involves the bonding of GaAs and InP on a single substrate, using a new multilayer bonding methodology, the details of which are shown in Figure 4-2. Figure 4-1 show the mask I designed for the purpose of this project which includes 8 layers for each step. The essential sections of the mask include the RF rectifiers, single PDs and SDs, top illuminated DC test PDs, n- and p-TLMs, alignment markers. The process started with the fabrication of PD first.

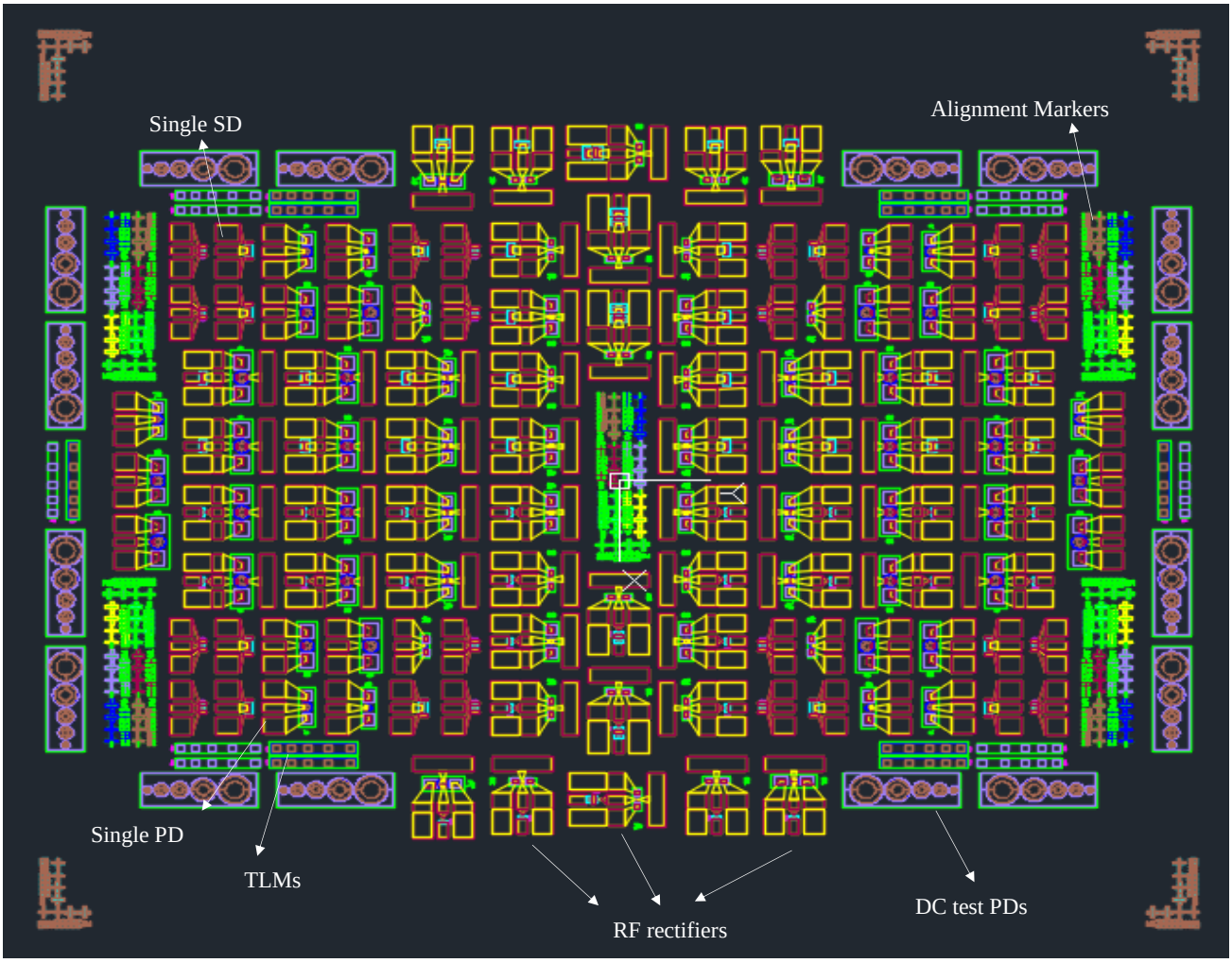


Figure 4-1. The proposed EPIC mask

4.2.1 Epitaxial structure and PD fabrication

The epitaxial structure for InP PIN to be bonded on the SOI substrate which was designed by our group, as depicted in Figure 4-2 (b) [110], wherein the 200 nm n+ InGaAs top cap layer serves as an etch stop layer for InP. This is succeeded by a 600 nm n+ InP as the n-type contact layer, a 15 nm Indium Gallium Arsenide Phosphide (InGaAsP) layer for bandgap smoothing, and a 1250 nm undoped InGaAs layer for absorption. Subsequently, a 10 nm undoped InGaAsP layer is introduced to enhance carrier transport, followed by a 200 nm p+ InP contact layer. The assembly is finalized with a 20 nm p+ InGaAs cap layer, aimed at optimizing the ohmic contact. The PD is configured for top illumination in this design.

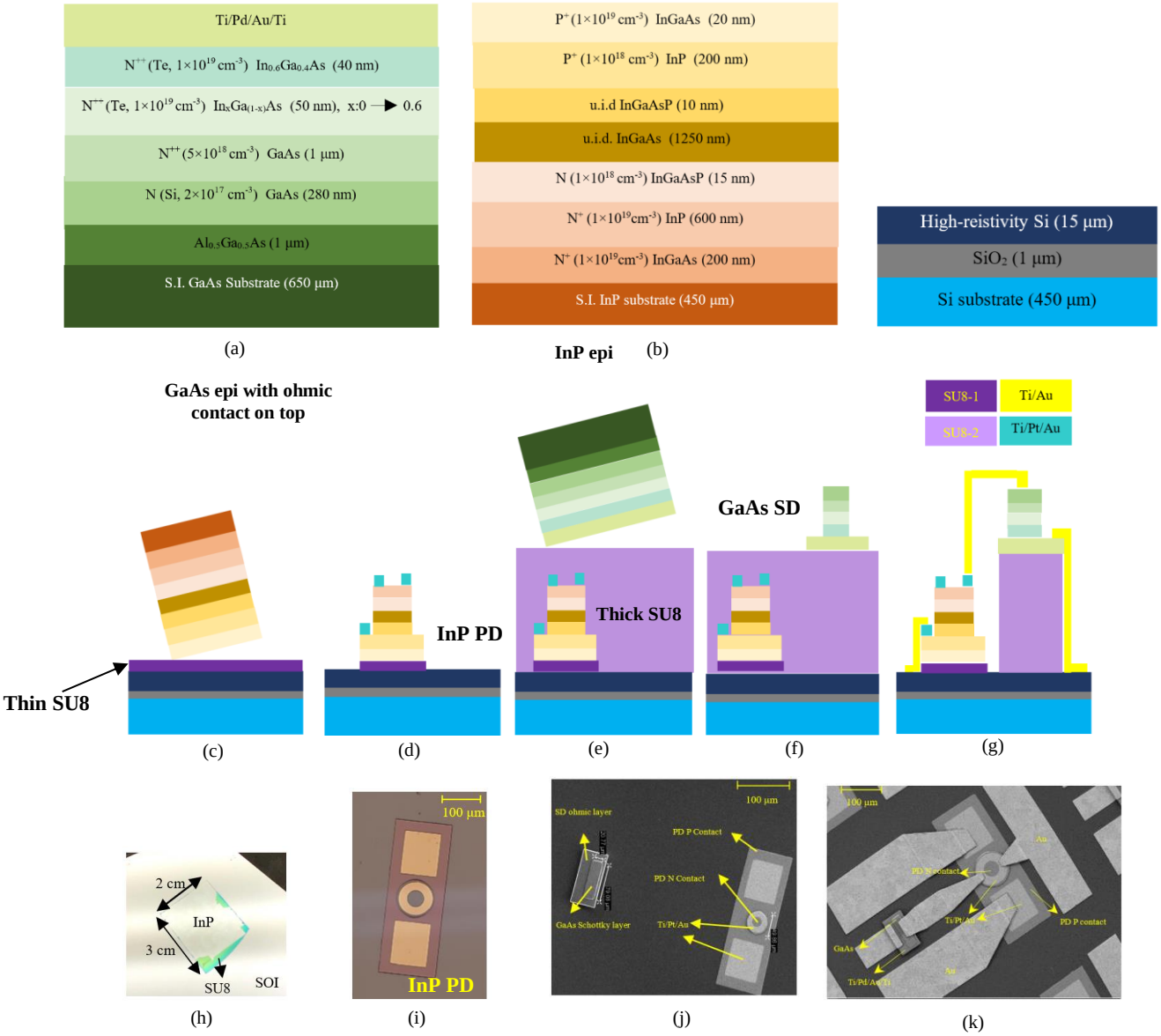


Figure 4-2. (a) Epitaxial structure of GaAs Schottky diode with metal contact *[111]* , (b) epitaxial structure of InP PIN photodetector, and SOI wafer (right), (c) Adhesive bonding of InP epi using SU8-1 on 15 µm device layer SOI with 450 µm substrate, (d) contact mesa and metal layers formed using wet etching, Ebeam deposition followed by lift-off, (e) Second adhesive bonding of GaAs layers on top of InP PDs using SU8-2, (f) GaAs substrate removal, ohmic and Schottky mesas formation using dry/wet etching and excessive adhesive removal, (g) sputtering seedlayer and electroplating to form air bridges, RF pads and metal interconnections, (h) Post-thinning state of an InP epitaxial layer bonded on SOI, (i) Microscope image of PD mesa prior to SD fabrication, (j) SEM image of the devices' mesas prior to electroplating, (k) Top view of the final fabricated square law detector.

The bonding was done in SUSS semi-auto XB8 bonder using 250 nm SU8 as adhesive, 100 N bonding force, and $5\times e^{-6}$ mbar (Figure 4-2 (c)). Figure 4-3 (a) illustrates the process of substrate removal for the InP sample, which involves immersing the sample in a

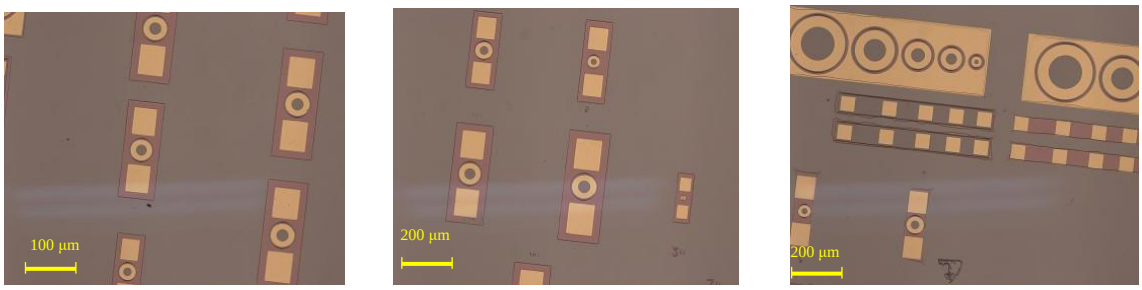
hydrochloric acid: DI (3:1) solution. This etching procedure achieves an etching rate of approximately 8 µm/min, necessitating a total duration of approximately 75 min for the complete removal of the 450 µm substrate. To ensure thorough substrate removal without having InP residue on the surface as shown in Figure 4-3(b), the etching solution requires to be refreshed upon getting saturated, typically after one hour.

(a) (b)

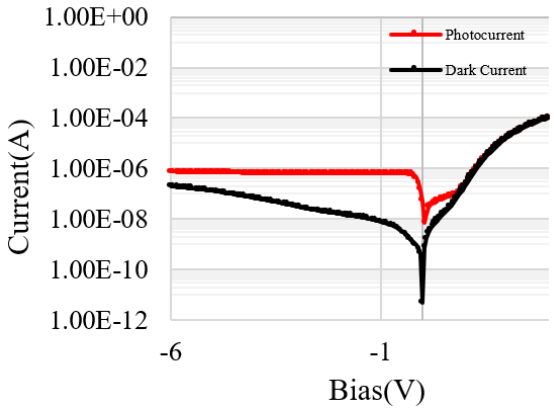
Figure 4-3. (a) Substrate removal of the InP epi bonded onto SOI in hydrochloric acid (b) Substrate residue due to saturated HCL dilution.

The point about the substrate removal process is avoiding the undercut around the epitaxial layer, as shown in Figure 4-2 (h). Subsequent to the substrate removal, it is imperative to remove the 200 nm n_+InGaAs etch stop layer too to facilitate top illumination. The fabrication process of the PD started with the spin coating of the InP diced piece with AZ4210 photoresist, underlaid by HMDS at 4 KRPM, subsequently followed by direct laser lithography using the n-mesa mask at an energy density of 300 mJ/cm². Prior to exposure, edge-bead removal was done, with the development in 300MIF developer for approximately 90 seconds. The etching process involved the use of citric acid: hydrogen peroxide (H_2O_2) (3:1) for etching through the InGaAs and InGaAsP layers, and hydrochloric acid:DI water (HCl:DI) solution, also at a 3:1 ratio, for etching through the InP layer. The initial 200 nm InGaAs layer was rapidly etched, exhibiting color pattern change within seconds. This was followed by immersion in an HCl dilution for less than

20 seconds to remove a 600 nm layer of InP. The etching of the 1275 nm InGaAs/InGaAsP layers was completed in approximately 2 minutes, stopped on the 200 nm p_+InP layer to form the n-mesa, as etching through the 20 nm p_+InGaAs layer was deemed too thin, risking complete etching. Post n-mesa formation, p-mesa lithography was done utilizing a similar recipe, with HCl dilution and citric acid employed to reach the SU8 layer. Subsequent steps involved the removal of the top resist, with SU8 removal achieved by 200 W O_2 plasma treatment. Ohmic contacts for both p and n mesas were fabricated using a metal stack of Ti (20 nm, as first layer), Pt (30 nm), and Au (50 nm). High-quality lift-off was ensured by using LOR resist, with a 150 mJ/cm² exposure dose via a u-writer, followed by a brief 10 sec development in 300MIF. Metal layer deposition was then carried out, with a final lift-off of resist facilitated by a 70 °C, 5 min PG remover. Figure 4-4 (a), Figures 4-2 (d) and (i) illustrate the outcome of the PIN mesa formation process, with the resulting IV characteristics of the PIN PDs presented in Figure 4-4 (b).



(a)



(b)

Figure 4-4. (a) PIN PD fabricated on SOI using wet etch after patterning ohmic contacts (b) IV plot of the 90 µm diameter fabricated PD.

TLM analysis reveals that exposing the devices to a brief annealing period of approximately 1 minute at a temperature of 300 °C within RTA significantly enhances the resistivity of the n-type ohmic contacts. The resultant improvement in the n-type ohmic contact post-annealing is illustrated in the subsequent Figure 4-5. This plot gives us around <1Ω n-contact resistance and 5 Ω/sq n-contact sheet resistivity.

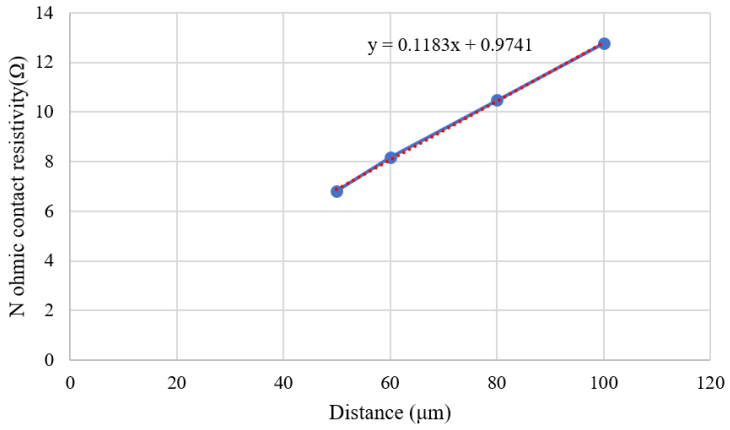


Figure 4-5. TLM plot of n-ohmic contact after annealing.

A wide range IV characterization of 100 µm single PD shows approximately 7.5 kΩ p-series resistance (both sheet and contact) at 15 V reverse bias. Figure 4-6 shows the IV characterization of PDs before and after annealing of the 200 µm diameter top illuminated device which reveals forward current improvement due to annealing. The dark current decreases after annealing at higher reverse bias and becomes independent of the bias.

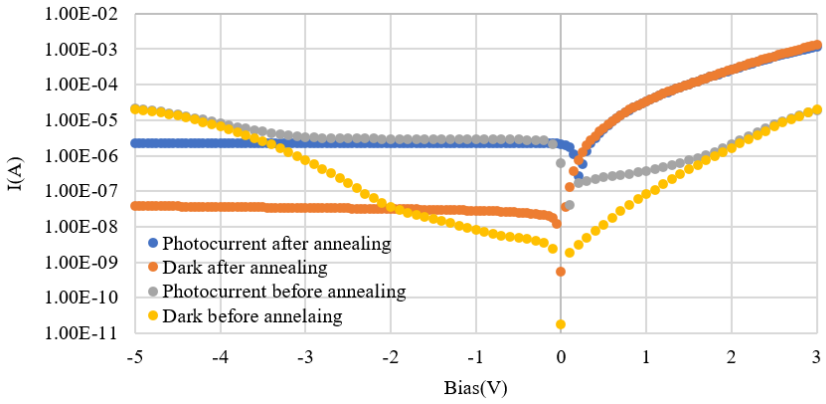


Figure 4-6. IV characteristic of 200 µm circular PD before and after annealing

4.2.2 Multilayered bonding

The primary goal of this research is to evaluate the viability of implementing a secondary layer of bonding atop the InGaAs/InP PD. The complexity of this procedure stems from a few technical challenges:

- The PIN structures introduces a non-uniform substrate surface, contrasting sharply with the conditions encountered during the first bonding effort, presenting a surface topology variation of approximately 2 µm. Consequently, a requirement emerged for an adhesive with a high planarization ratio, necessitating the development of a novel bonding technique.
- The risk of failure of substrate removal escalates due to an increased likelihood of undercut formations and debonding.
- The necessity to remove the second adhesive layer arises after SD fabrication to facilitate electrical contact with the initially fabricated PDs.

Figure 4-2 (e) shows the detailed schematic of this step. In response to the need for a more robust bonding adhesive, the transition was made to a thicker type of the SU8 6000 series. It is pertinent to mention that prior attempts had focused on the discrete integration of GaAs and InP onto the same SOI substrate, employing only one adhesive layer and placing the epitaxial dies next to one another, as illustrated in Figure 4-7.

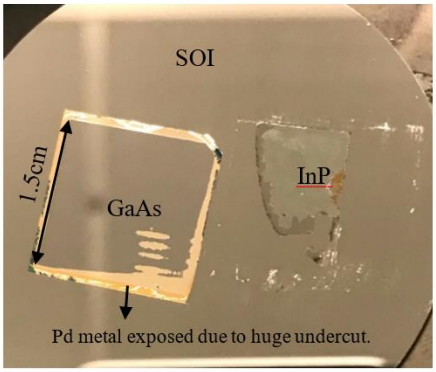


Figure 4-7. Discrete integration of GaAs and InP epi

The aforementioned methodology proves to be infeasible for practical application, primarily due to the lack of alignment capabilities and the considerable separation

between the two epitaxial segments. This spatial discrepancy significantly undermines the objective of achieving a densely integrated assembly of photonic and THz devices.

4.2.3 SD fabrication

Subsequent to the PD fabrication (Figures 4-2(c) and (d)) and preliminary DC characterization of the PIN PDs, the chip undergoes a spin coating process with a secondary thick layer of SU8 photoresist, serving both bonding and planarization purposes, Figure 4-2 (e). The specific GaAs epitaxial layer designated for this application is detailed in Figure 4-2 (a) [111]. In this epitaxial structure, which was designed and provided by Prof. Weikle's research group [111], the top InGaAs cap layer, characterized by high doping levels, is implemented to substantially reduce ohmic contact resistance. Additionally, the InGaAs compositional grading layer is engineered to smoothen the conduction band profile, thereby enhancing carrier transfer across the layers. The incorporation of a highly doped GaAs layer serves the purpose of establishing an effective ohmic contact, while a lightly doped GaAs layer is designed to fulfill the Schottky contact criteria. In this configuration, the ohmic contact metallization sequence, aimed at minimizing series resistance, is identified as Ti/Palladium (Pd)/Au/Ti [111]. Moreover, an $Al_{0.5}Ga_{0.5}As$ layer is designated as an etch stop during the substrate removal.

The next phase entails bonding of the metalized GaAs epitaxial layer atop this SU8-coated piece, as was depicted in Figure 4-2 (e). A layer of the second adhesive, 4.7 μm in thickness, was spin-coated, followed by a soft bake at 110°C and UV exposure at an intensity of 280 mJ/cm². The bonding was done in the conventional dual chamber bonder. Substrate removal was completed within a harsh acidic environment, incorporating nitric acid and HF. Notably, etching for up to 2 minutes in HF did not compromise the bonding quality, underscoring the method's reliability. Post handle removal, the fabrication trajectory advances with the processing of the Schottky diode on top the adhesive, as illustrated in Figure 4-2 (f). SD fabrication constitutes a series of dry and wet etching processes to accurately pattern both ohmic and Schottky mesas. Following mesa

formation, the subsequent step involves the removal of residual SU8 surrounding the SD mesa via Oxygen (O_2) plasma treatment. Figure 4-8 shows the two integrated devices after SD mesa formations and before electroplating.

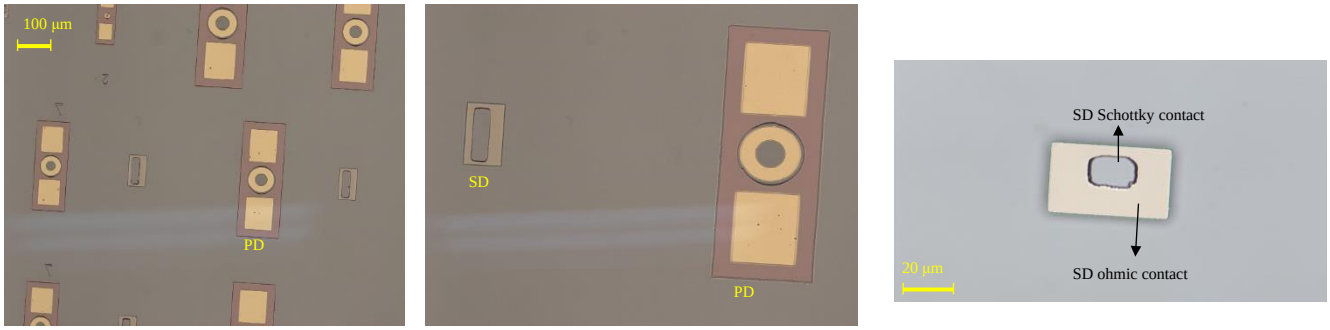


Figure 4-8. Patterning the device mesas before electroplating

Figure 4-9 shows the SEM images of some of the integrated devices before electroplating.

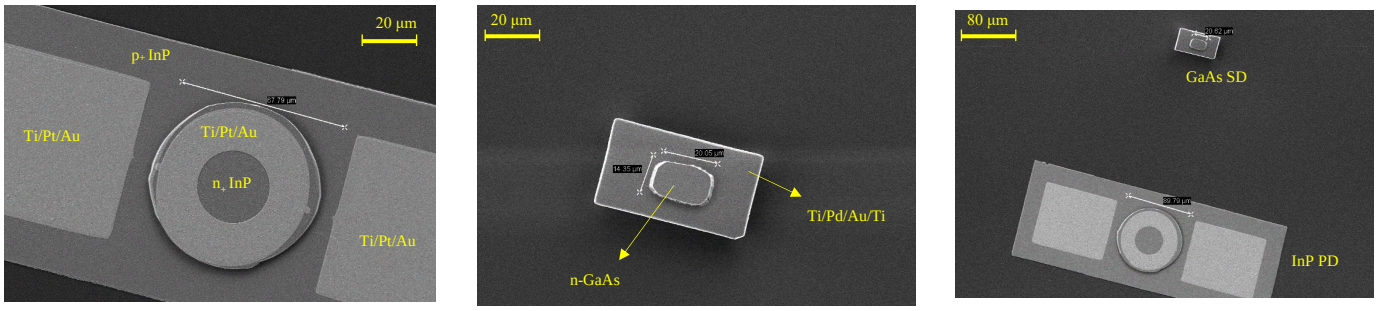


Figure 4-9. SEM images of the integrated devices before electroplating

The final fabrication steps include lithography to pattern the sacrificial resist features for air bridge, followed by sputtering Ti/Au seed layers. The last lithography step precedes electroplating for both PDs and SD together. The removal of the seed layer and sacrificial resist completes the formation of CPW pads, RF pads, anode, air bridges, and CPW interconnections between the SD and PD, as shown in Figure 4-2 (g). Also, Figures 4-2 (h)-(k) shows the microscope and SEM images associated with each step during the fabrication process. Figure 4-10 shows the dark currents of PDs of different dimensions with minimum value of 10 nA @ 1 V reverse bias. Also Figure 4-11 shows the SEM images of the devices after adding the metal interconnection and RF pads.

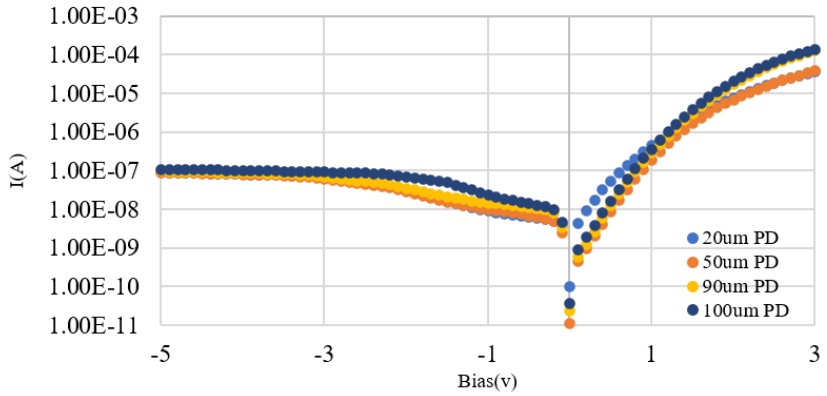


Figure 4-10. dark current of top illuminated PDs of different size.

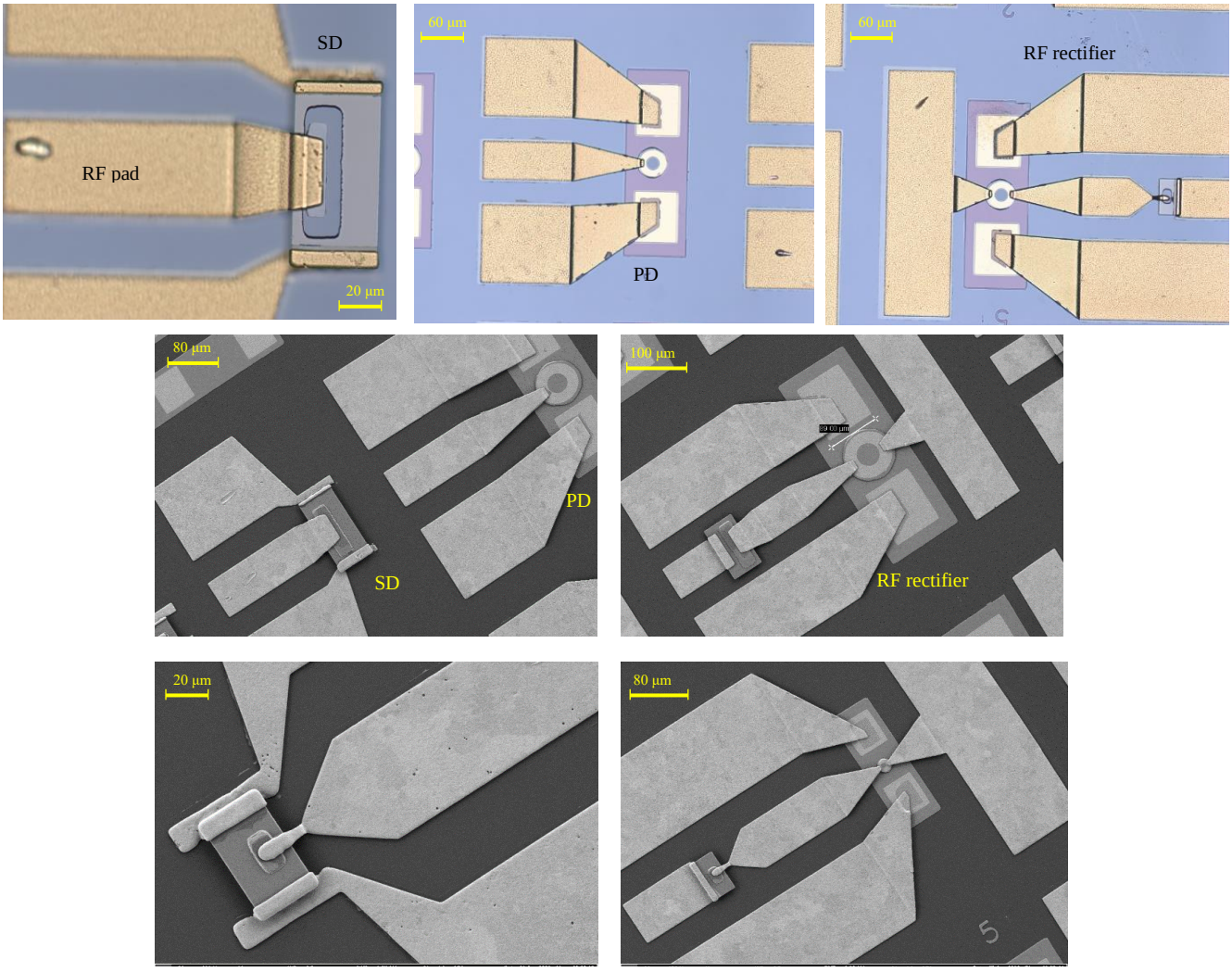
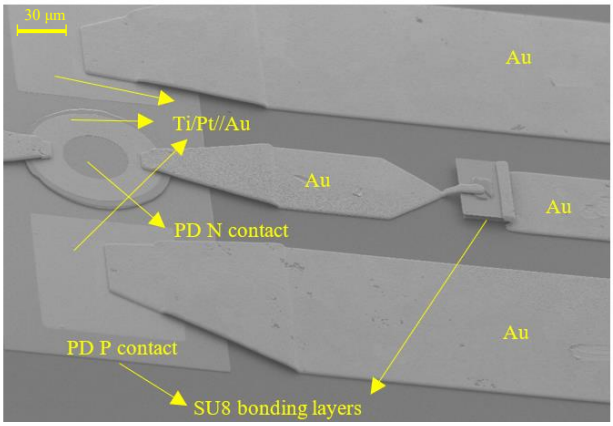
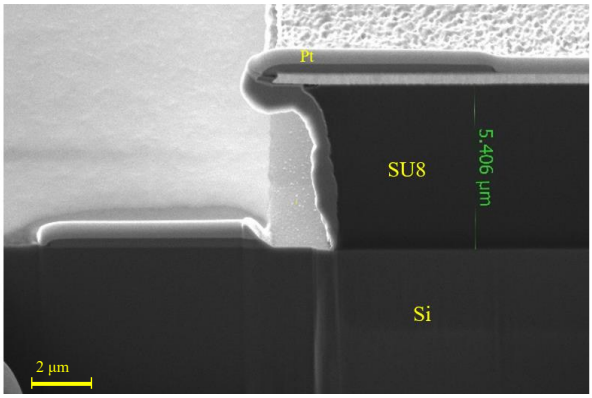


Figure 4-11. microscope and SEM images of the devices post-integration.

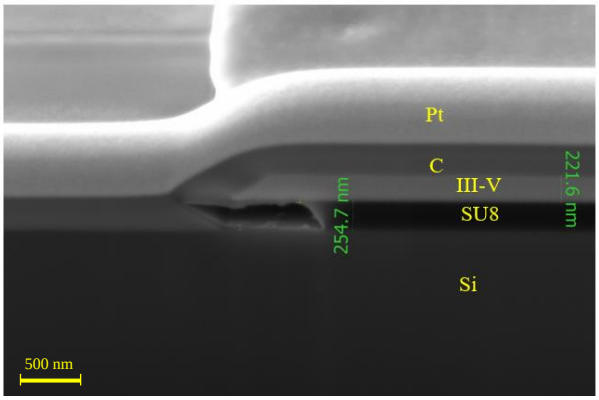
In Figure 4-12(a), the difference between the SU8 under the two fabricated devices is clear. This also confirms in Figures 4-12(b) and (c) which was taken using FIB technique. I used a Pt layer with carbon underneath to help preserve the integrity of the sample during FIB process. Without Pt, the surface would get damaged during ion milling. Carbon also improves the layers contrast.



(a)



(b)



(c)

Figure 4-12. (a) The wide lateral view of the square law detector (b) The SD bonding interface with 5.4µm thickness SU8 as bonding adhesive (c) The PD bonding interface with 300nm thickness bonding adhesive

Figure 4-13 shows the IVs of the SDs of two dimensions. Using the least-square curve fitting method, I determined a series resistance of 21 Ω, leakage current of 136 fA, and ideality factor of 1.29 for the 200 μm^2 SDs. The big SD shows a turn on voltage close to 0.45 V while the smaller one is approximately 0.6 V. The difference in turn-on voltages comes from the different contact areas. Even though the turn-on voltage of a Schottky diode is not directly related to the physical dimensions of the device in a straightforward

manner, as it primarily depends on the barrier height between the metal and the semiconductor, as well as the materials' work functions. However, the dimensions of the device can influence its electrical characteristics, which indirectly affect how the turn-on voltage might be perceived or measured in practical applications. There are a few factors play role in this regard:

Series Resistance: Larger device dimensions can reduce the series resistance within the diode because of a larger cross-sectional area for current flow. Reduced series resistance can lead to a lower voltage drop across the diode at a given current, potentially influencing the observed turn-on voltage in IV measurements, especially under high current conditions.

Junction Area: The junction area between the metal and semiconductor affects the total current flowing through the device for a given applied voltage. A larger junction area can carry more current for the same forward bias voltage, which might affect the voltage at which significant forward conduction is observed.

Edge Effects: In smaller devices, edge effects become more significant, potentially affecting the barrier height at the edges due to differences in the electric field distribution. This can modify the effective barrier height averaged over the entire junction, potentially influencing the turn-on voltage.

It’s important to note that while device dimensions can influence these parameters, the turn-on voltage is still fundamentally related to the material properties of the diode, such as the Schottky barrier height, and not directly to the device's size.

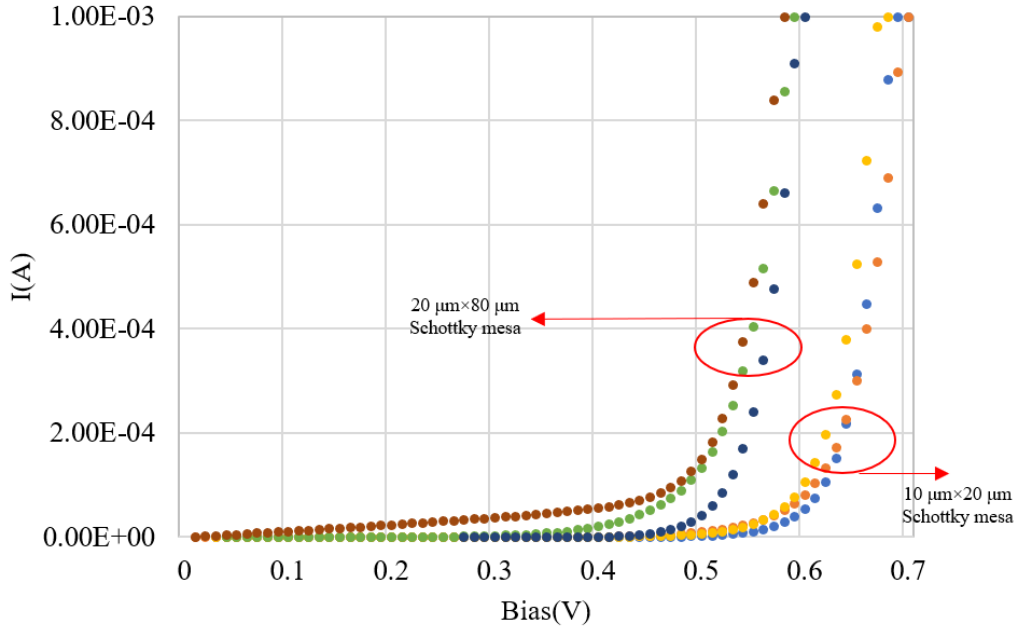


Figure 4-13. I-V characteristics of quasi vertical Schottky diodes of two different

Figure 4-14 presents the current-voltage (I-V) characteristics of photodetectors (PDs) of two dimensions at the end of fabrication. A peak quantum efficiency of 72% was obtained for a photodetector with 200 μm diameter, showing stability across a reverse bias voltage ranging from 1 to 5 V.

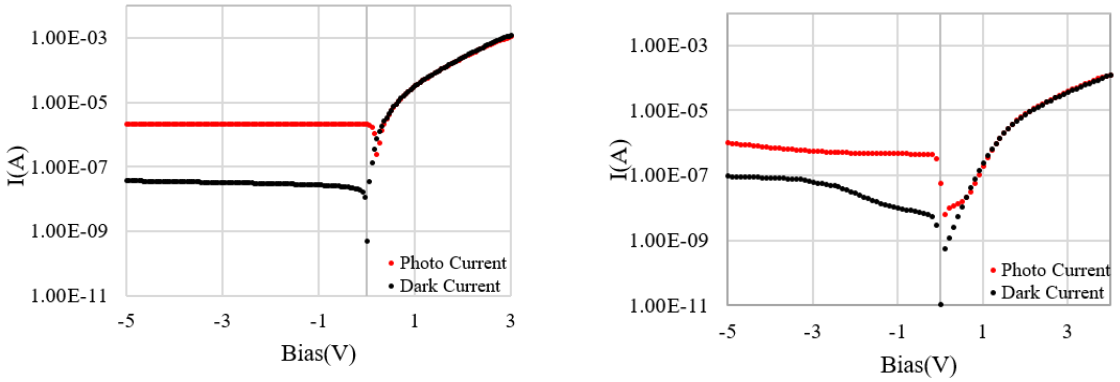


Figure 4-14. IV characteristic of top illuminated PDs. The bigger PD shows higher photocurrent while the smaller PD have lower dark current (a) 200 μm diameter PD (b) 90 μm diameter PD.

To show the feasibility of the proposed integration technique I used it to realize an on-chip rectifier which will be described further in the next section.

4.3 On-chip rectifier (square-law detector)

An on-chip rectifying square-law detector is a device that outputs a voltage proportional to the square of the input signal (i.e. power), typically used for detecting the power of an RF signal**.** Figure 4-15 shows the IV characteristic of a Schottky diode in which the square law and linear regions are designated. The latter leads to a higher sensitivity due to its non-linear nature while the former leads to a wider dynamic range. The main purpose of the proposed on-chip square law detector is rectifying the photonically generated RF signal and finding the average value which is proportional to the square of the input signal amplitude.

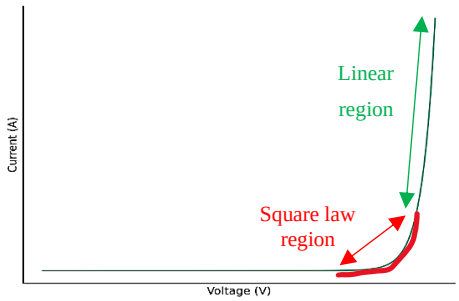


Figure 4-15. IV characteristic of a typical Schottky diode designating the two operational modes

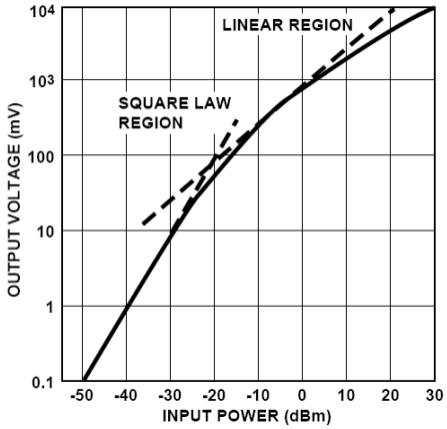


Figure 4-16.different sensitivity of the two modes of a square law detector *[114]*

Considering the items above, I designed GaAs SD/ InP PD integrated square-law detector in which the PD has the function of RF source. Figure 4-17 shows the schematic of such design in which the GaAs SD and PIN PD are connected in series.

4.3.1 Components and their functions

The DC pad represented in yellow on the left is for biasing purposes. A needle probe makes physical contact with the pad, delivering the bias necessary for the operation of the SD and PD. The RF signal, which is used to test the high-frequency response of the devices, is generated by the Keysight RF source. The PIN structure is depicted with the symbols for an N and P metals and mesas. The Schottky diode is shown with cathode (ohmic contact) and anode (Schottky contact). GSG probe is used to show the real-time signal on the oscilloscope. The RF signal generated out of the PD feeds into the SD to generate the rectified signal.

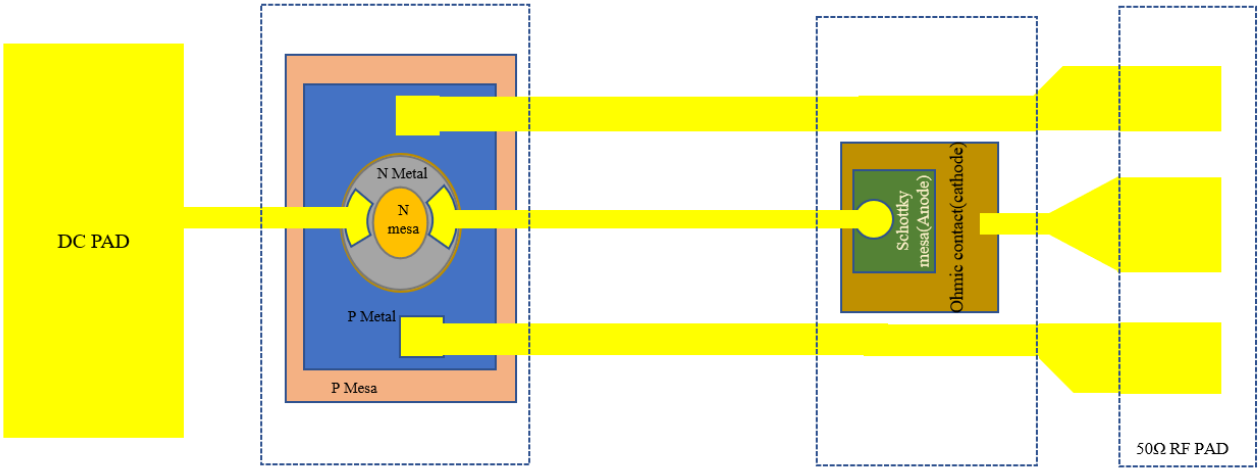


Figure 4-17. Schematic design of the SD/PD integrated rectifier.

4.4 Simulation

Figure 4-18 shows the transient time simulation of the circuit model of the implemented square law detector considering a current source model for the PD.

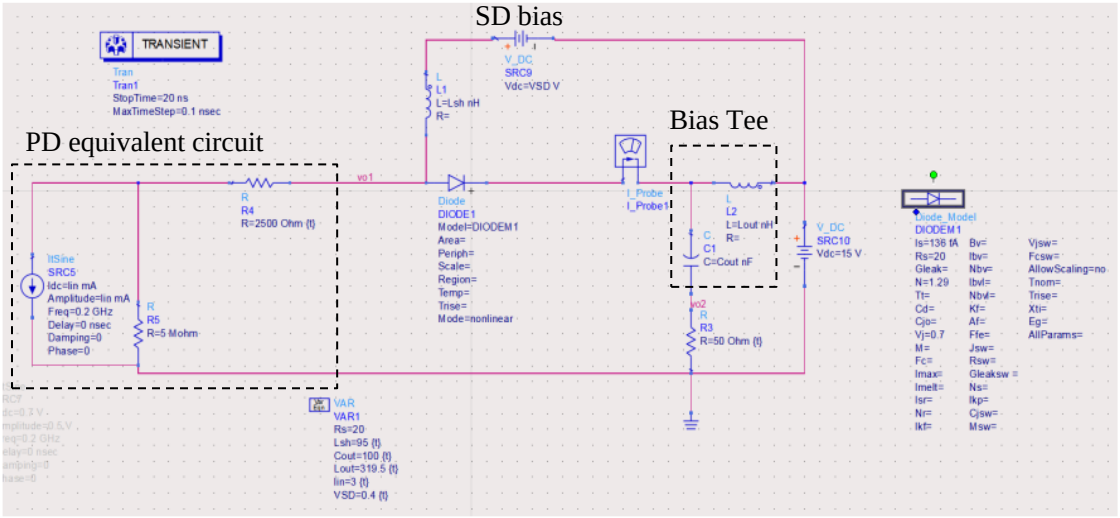


Figure 4-18. Schematic of the EPIC square law detector

In Figure 4-19 the SD is working in square law mode (SD bias=0.4 V), so the SD current and output voltage are rectified.

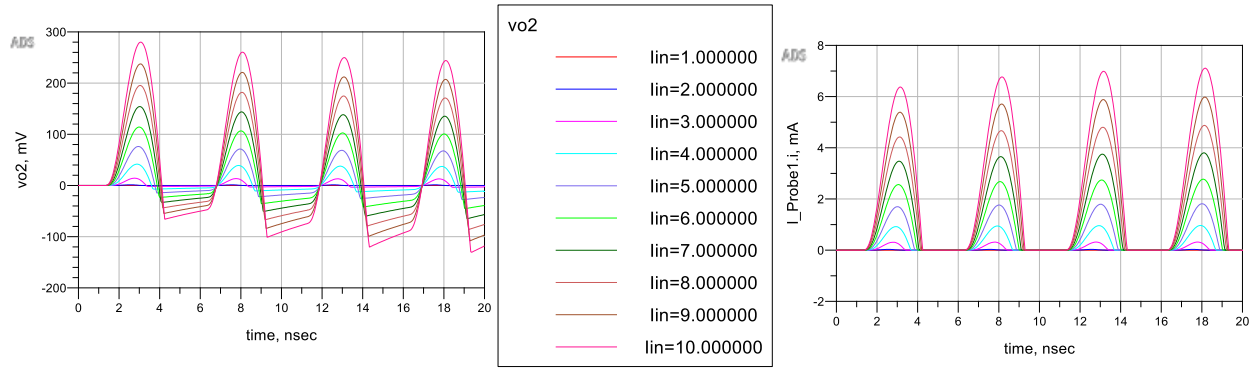


Figure 4-19. The ADS simulation results of the implemented square law detector. SD current vs optical input. (V_{SD}= 0.4 V)

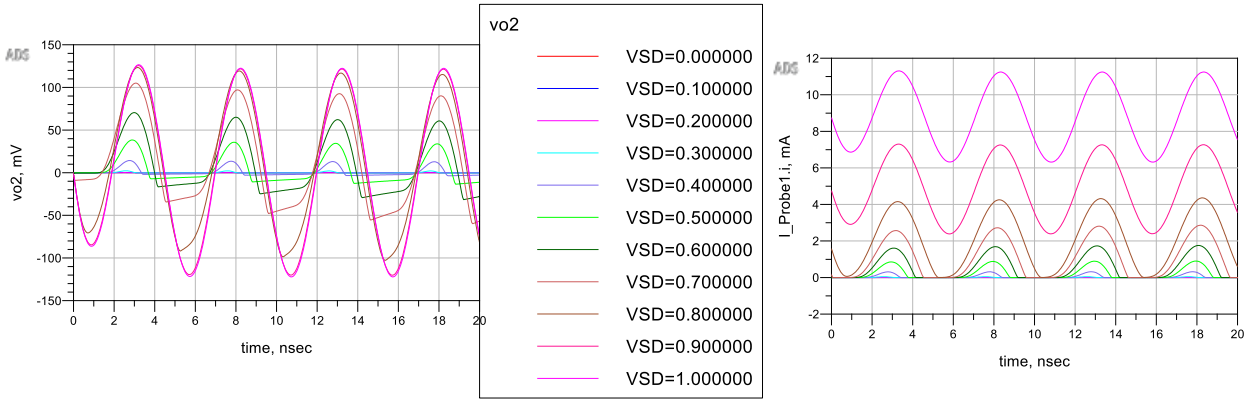


Figure 4-20. The ADS simulation results of the implemented square law detector. SD current vs SD bias. (I_{PD}= 5 mA)

Figure 4-20 shows the transition between the linear and square-law regions by sweeping over SD bias while the PD average current is fixed at 5 mA.

4.5 Single PD RF measurement setup

Figure 4-21 shows the heterodyne measurement setup for a single PD characterization. It consists of an Anritsu dual channel 1550 nm laser source followed by EDFA and attenuator. A lensed fiber goes through an optical polarizer to couple light onto the PD.

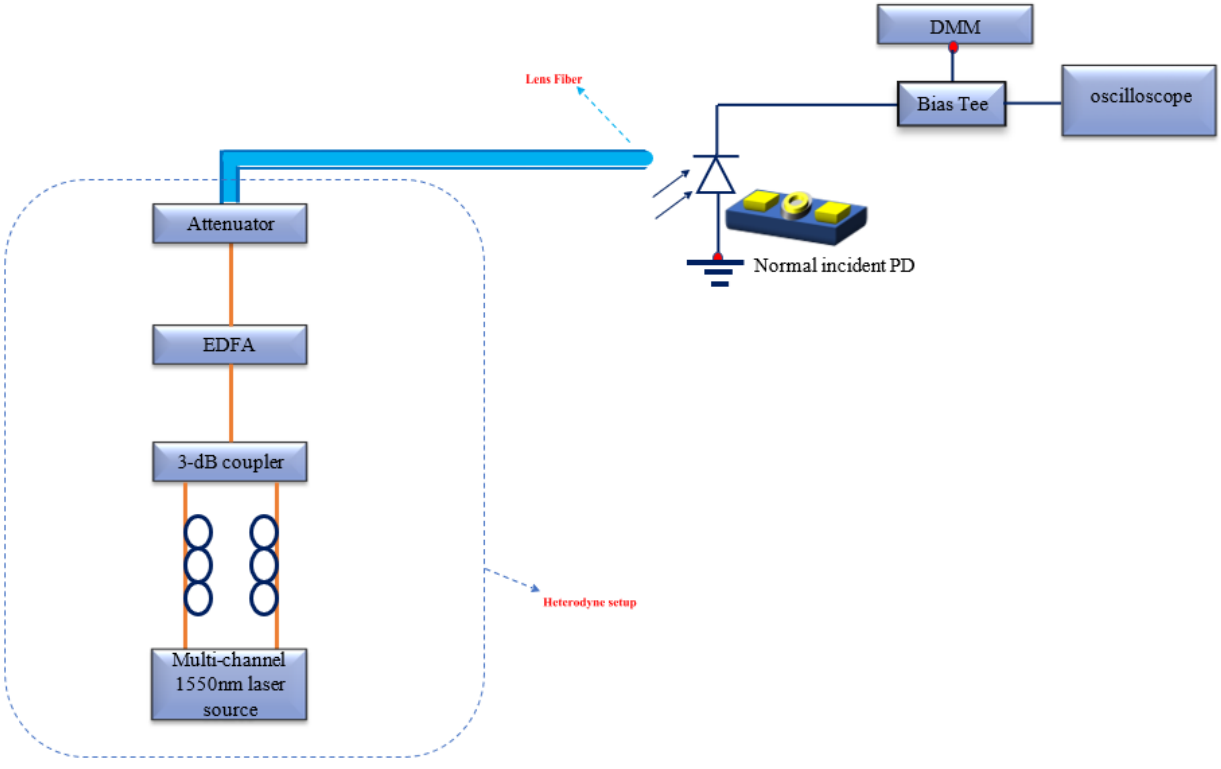


Figure 4-21. Heterodyne measurement setup for RF characterization of single PDs

Figure 4-22 shows the modulator setup to characterize the fabricated devices. The modulated light is coupled to the DUT through surface normal illumination. I utilized 10 GHz Keithley real-time oscilloscope here.

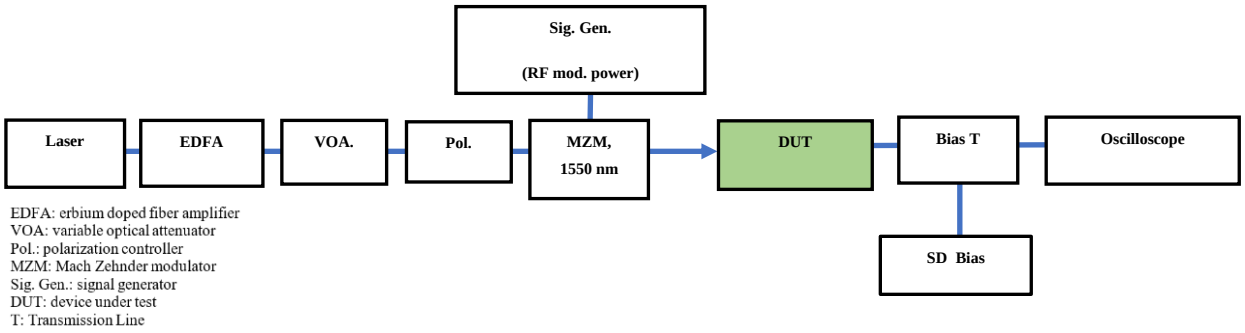


Figure 4-22. MZM modulator setup for RF measurement of single PDs

Figure 4-23 shows the time domain RF signal generated using the single PDs of different dimension using the heterodyne and MZM modulator (1550 nm EO Space) setups which confirm the higher signal quality of the latter compared to the former.

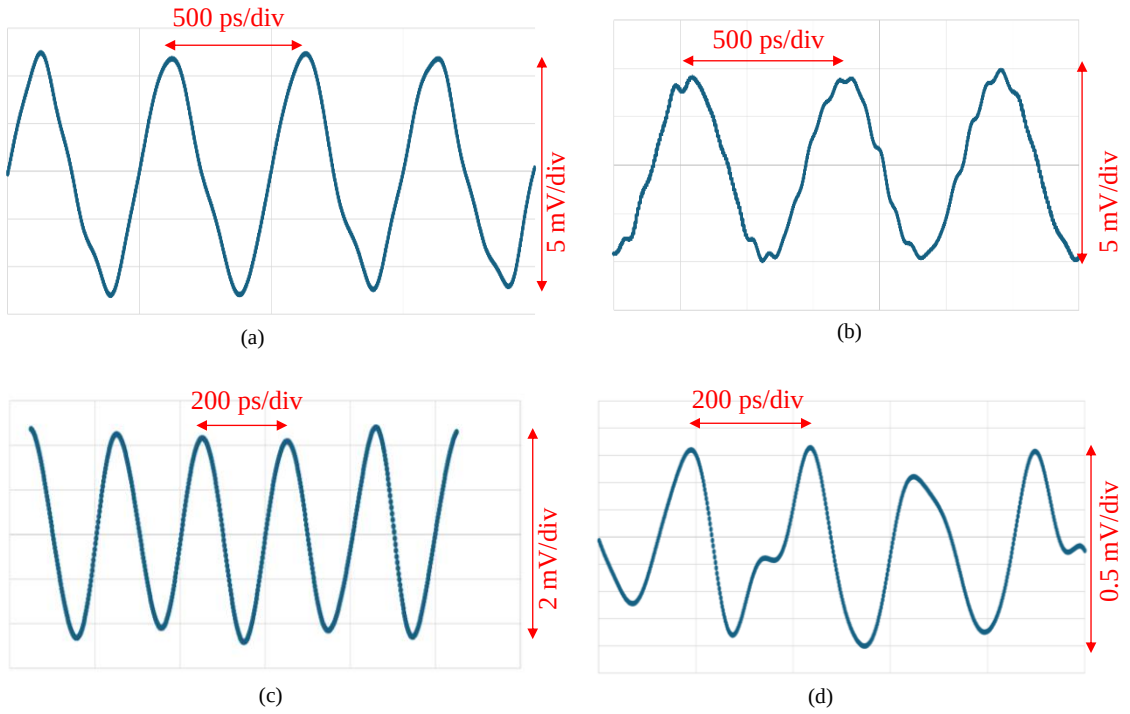


Figure 4-23.(a) Mod generated signal out of 50um diameter PD-1mA-13V-2GHz (b) Heterodyne generated 11v-4mA-1GHz-100um diameter PD (c) Mod generated signal out of 70um diameter PD-2.3mA-13.5V-5GHz RF(d) Heterodyne signal generated 13V-5mA-4GHz-100um diameter PD.

Figure 4-24 shows the single PD RF response of the 20 μm PD that was measured using heterodyne setup. The realtively low bandwidth comes from the relatively high p-ohmic

contact resistivity. Exploiting a highly selective wet etchant like sulfuric acid dilutions for InGaAsP/InGaAs over InP instead of solely citric acid would solve this issue.

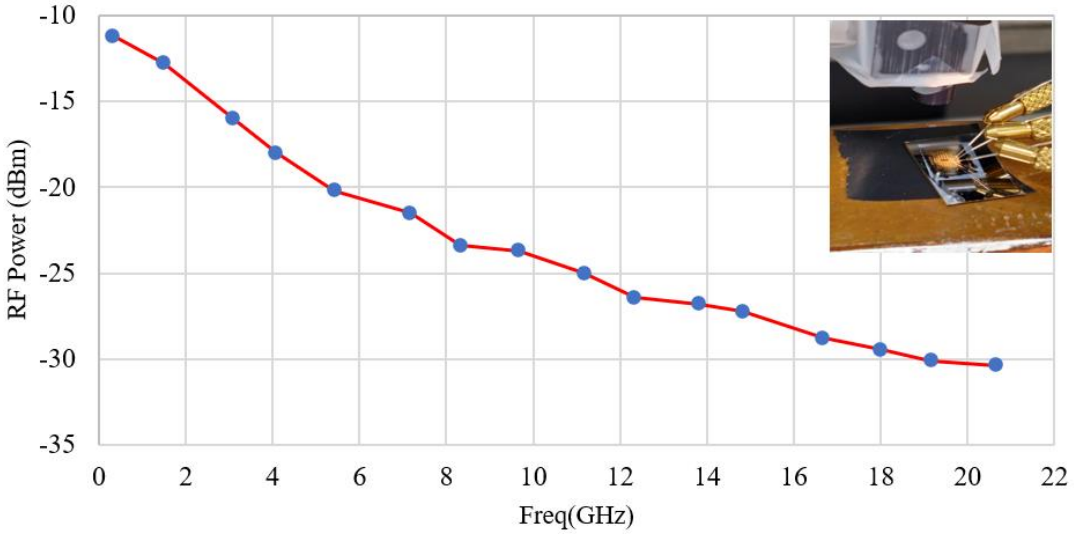


Figure 4-24. Frequency response of 20 µm circular PD, I_{ph}=2 mA, V_{bias}=-12 V.

4.6 Real time signal analysis of the square law detector

Figure 4-25 shows the biasing circuitry of the square-law rectifier. Using the RF choke and BT will make sure that the only path for the RF signal to flow in is through the SD which leads to rectification. The I_1 and I_2 DC current difference gives us the SD DC current. Since the Schottky is driven by current here and assuming 100 % modulation depth, all the RF component of the PD current going through the SD while zero portion of its DC component goes through SD as the SD DC current is prefixed by SD bias source, so any variation in SD DC current we will see in the next transient time plots coming from signal rectification. It's worth noting that the PD here acts as a current source, so this schematic is distinct from a conventional square law detector that is fed by an RF voltage and a choke being used to separate the DC and RF competent of the input signal. In other words, what is rectified here is the current, not voltage.

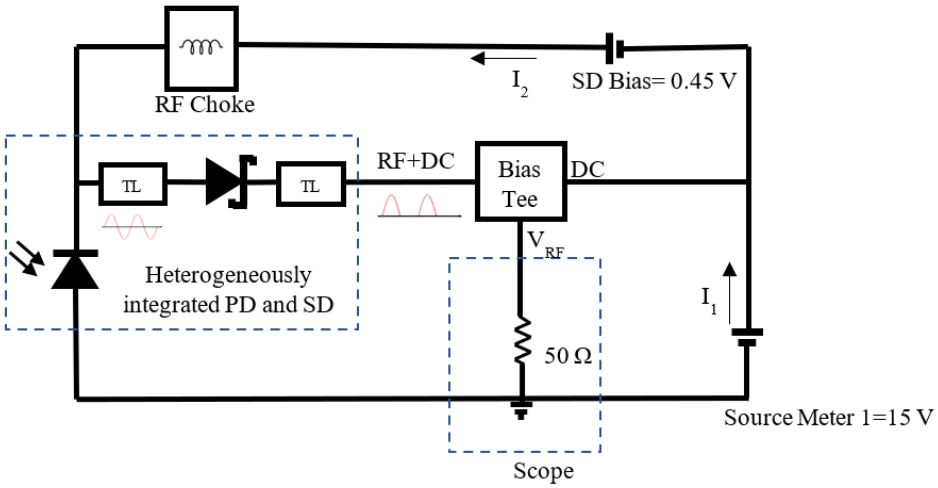


Figure 4-25. Biasing circuitry of the implemented rectifier

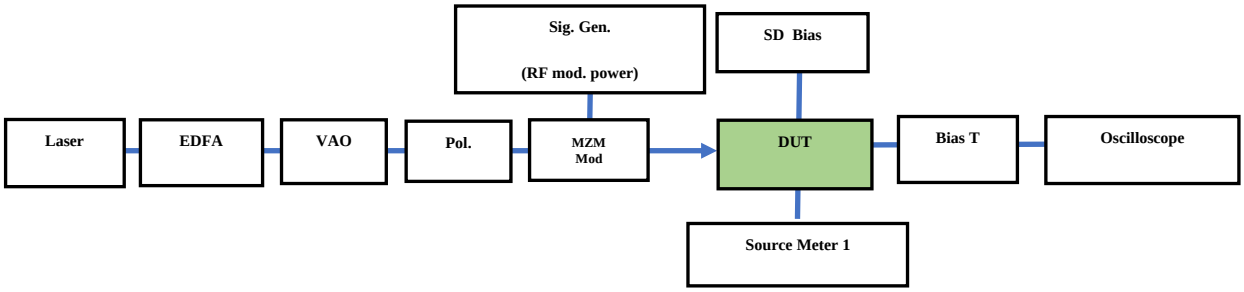


Figure 4-26. Modulator measurement setup for RF characterization of the square law detector

Figure 4-26 shows the external modulator diagram to characterize square-law detector in which the MZM modulator, driven by the RF source, is used to modulate the intensity of the optical signal from a 1550 nm source. This modulated light is directed onto the PD. BT is used to separate out the DC and RF components of the signal, allowing for simultaneous DC biasing and RF measurement of the diode without interference. The 50Ω GSG probe is used for high-frequency signal measurements.

“SD Bias” and “Source Meter 1” are digital multimeters (DMMs), that measure voltages and currents. “SD Bias” is set to supply a voltage between 0.45 and 0.65V adjusting the current across SD, while “Source Meter 1” supplies a larger voltage range, from 5 to 15V while measuring the DC current generated by PD. These voltage ranges indicate the expected operating voltages for the DUT. The 10 GHz real-time oscilloscope has been used to monitor the rectified signal. Figure 4-27 depicts the real-time output signal of a

detector which consists of 50 μm PD and 10×20 μm^2 SD with 200 MHz modulator RF input. It shows the detector output voltage vs modulator RF power. The SD bias is adjusted to 0.6 V to make sure the device is working in rectifying mode. In all the following measurements, V_{det} denotes V_{RF} (on scope)+I_{SD}×50 Ω. Figure 4-28 shows the detector output voltage over a varying range of modulator optical input. The SD is working in the same rectifying mode and the modulator RF power is set to 15 dBm to make sure that no distortion happens to signal due to PD or the modulator saturation.

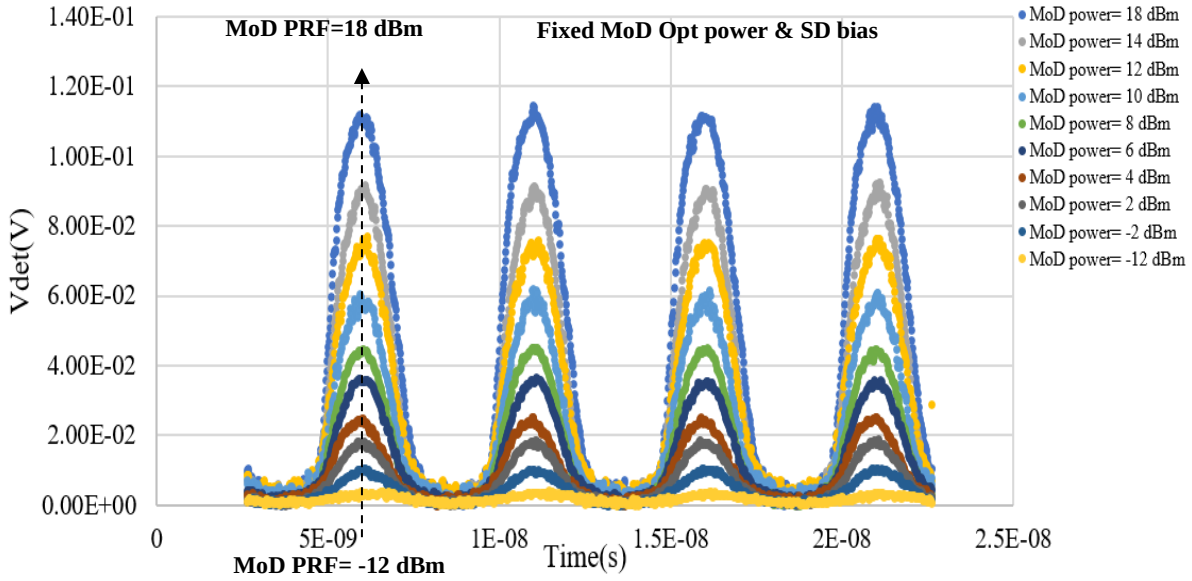


Figure 4-27. Dependency of real-time signal over Mod (modulator) RF power. 50 μm PD-10×20 μm^2 SD- 200 MHz. SD bias=0.6 V. Optical power= 17 dBm

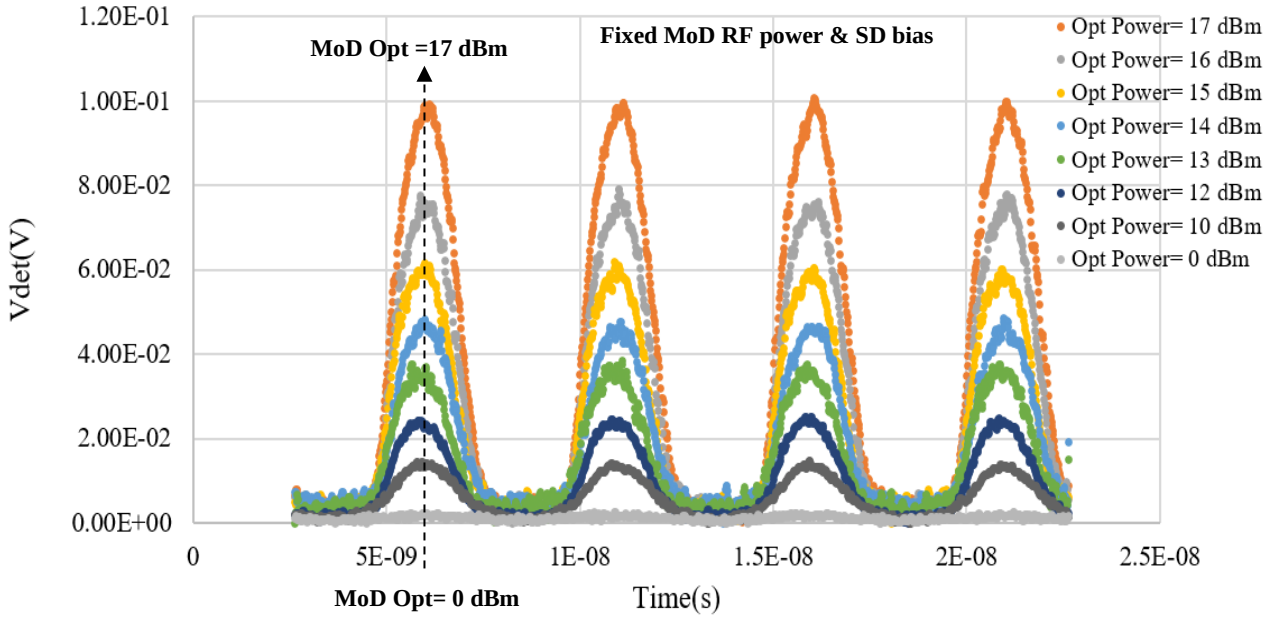


Figure 4-28. Dependency of real-time signal over optical input power. 50 µm PD-10×20 µm^2 SD- 200 MHz. MoD power=15 dBm, SD Bias=0.6 V

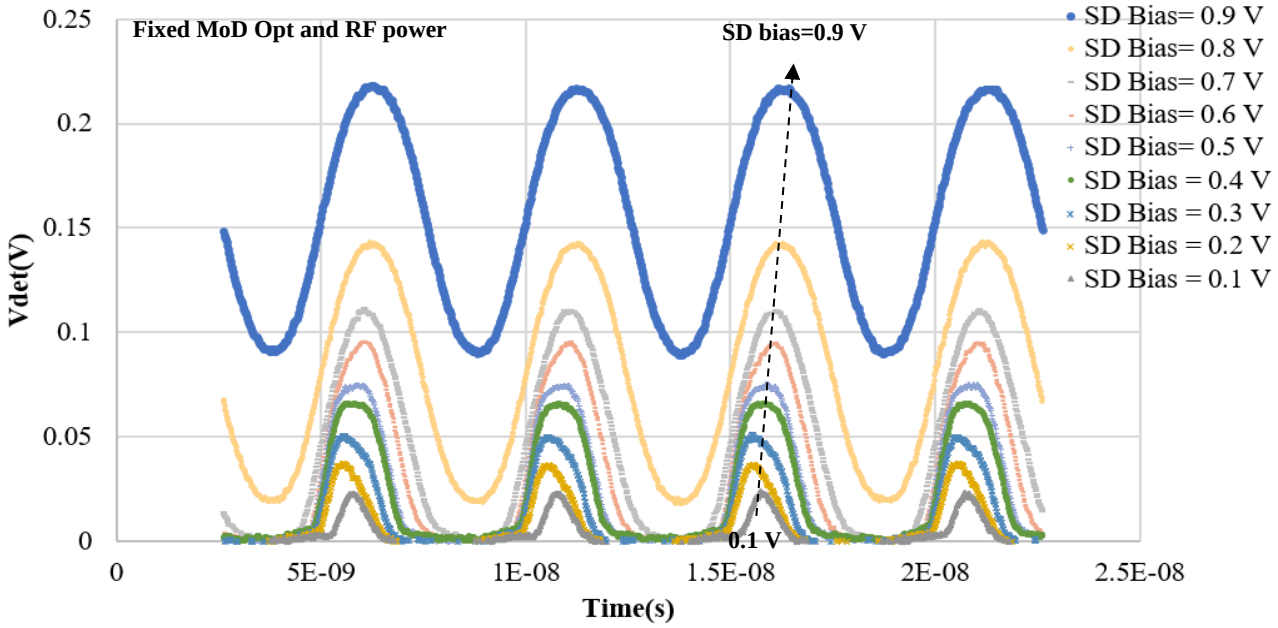


Figure 4-29. Dependency of real-time signal over SD bias. 50 µm PD-10*20 µm^2 SD- 200 MHz. Optical power= 17 dBm, MoD Power= 15 dBm

Figure 4-29 shows the detector output vs SD bias. Expectedly, by increasing the SD bias, the detector operational mode switches from the square region which rectifies the input to linear region which just scales the input signal. Figure 4-30 shows the average values of the detected output voltages which is calculated from current difference (I_1-I_2) over modulator optical input and RF power.

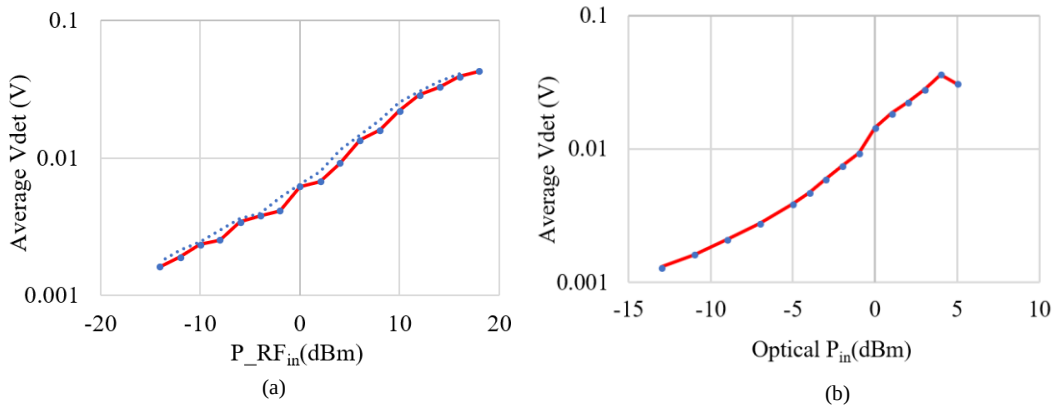


Figure 4-30. 50 µm PD-10*20 µm^2 SD- 200 MHz. Dependency of the average voltage on: (a) Modulator RF power (b) Optical power

There are upper limits for the optical input due to the PD saturation and for RF input due to modulator signal distortion and the risk of permanent damage to the device. The results show dynamic ranges of 17 dBm and 32 dBm for optical and RF input powers. As we see, there is a higher sensitivity for Figure 4-30(b) compared to Figure 4-30(a), this confirms an important fact about the modulator operation that the max modulation depth is realized from Figure 4-30(b) while the modulation depth is declining from the max value as we decrease the modulator RF power in Figure 4-30(a). Also, Figures 4-31 to 4-33 repeat the similar real-time outputs of the same detector this time for 500 MHz modulator input RF. The amplitude decline compared to 200 MHz signal is contributed to the limited PD bandwidth while still the rectification is observable.

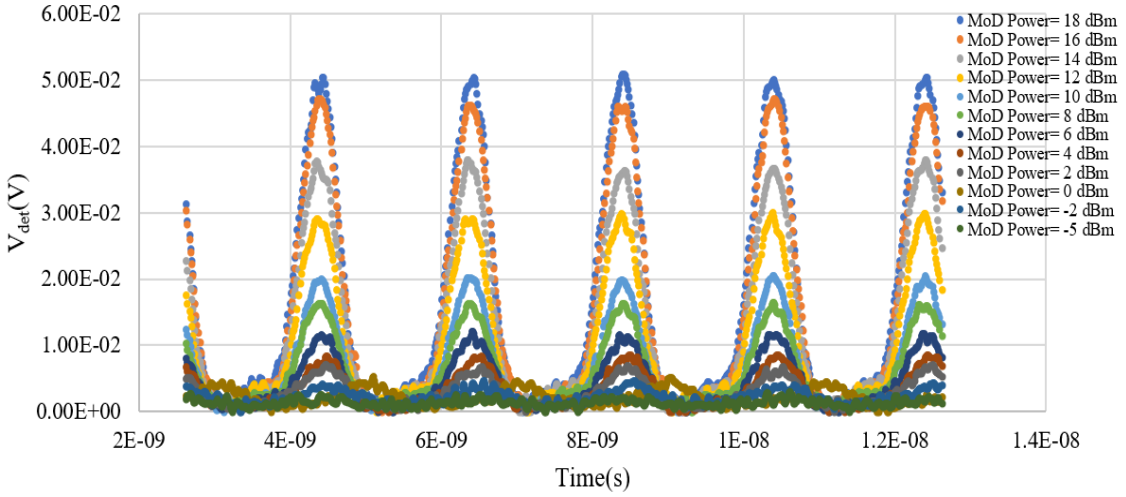


Figure 4-31. Dependency of real-time signal over Mod RF power. 50 μm PD-10*20 μm^2 SD- 500MHz. Optical power= 18 dBm, SD Bias=0.6 V

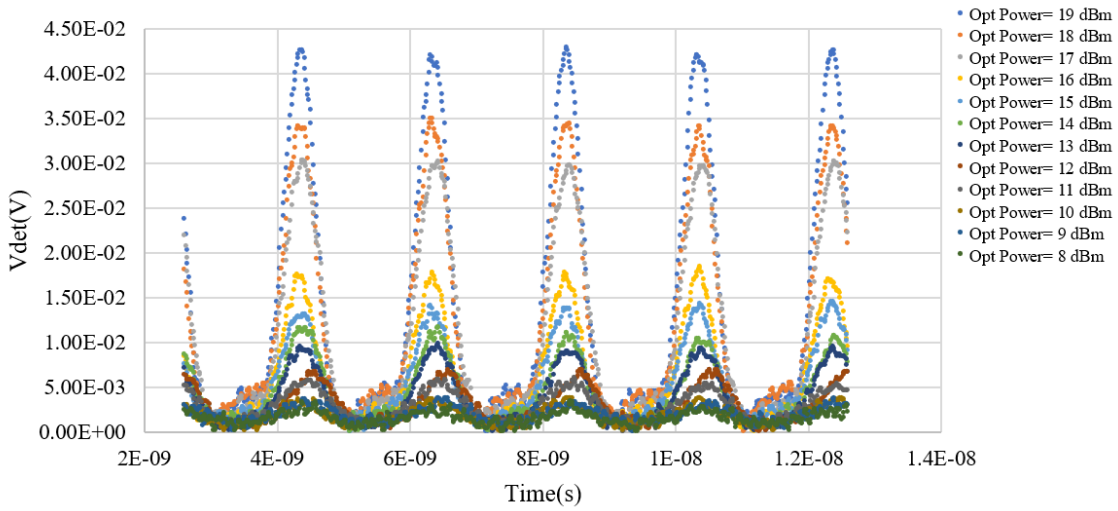


Figure 4-32. Dependency of real-time signal over optical input power. 50 μm PD-10×20 μm^2 SD- 500 MHz. MoD power= 15 dBm, SD Bias=0.6 V

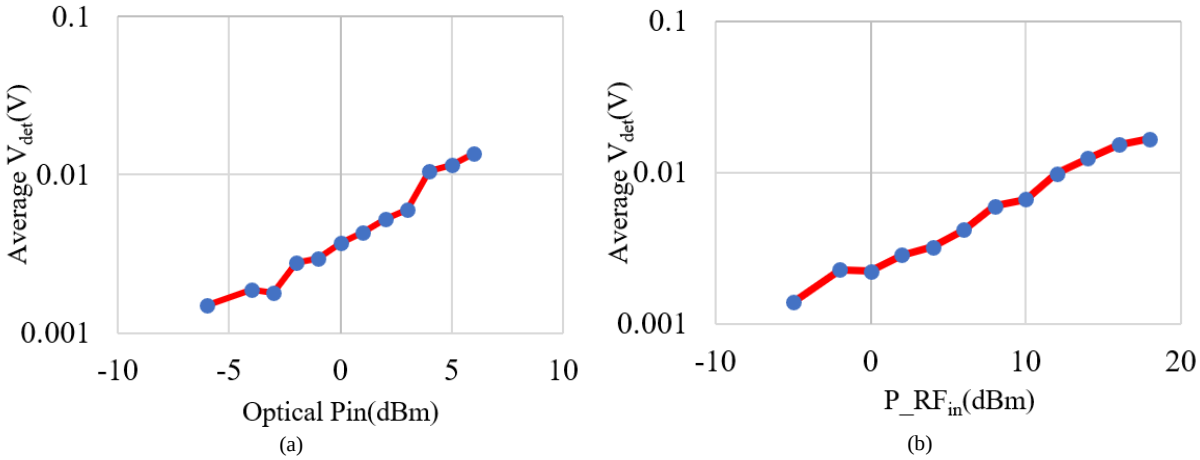


Figure 4-33. 50 μm PD-10*20 μm^2 SD- 500MHz. Dependency of the average voltage on: (a) Optical power (b) Modulator RF power

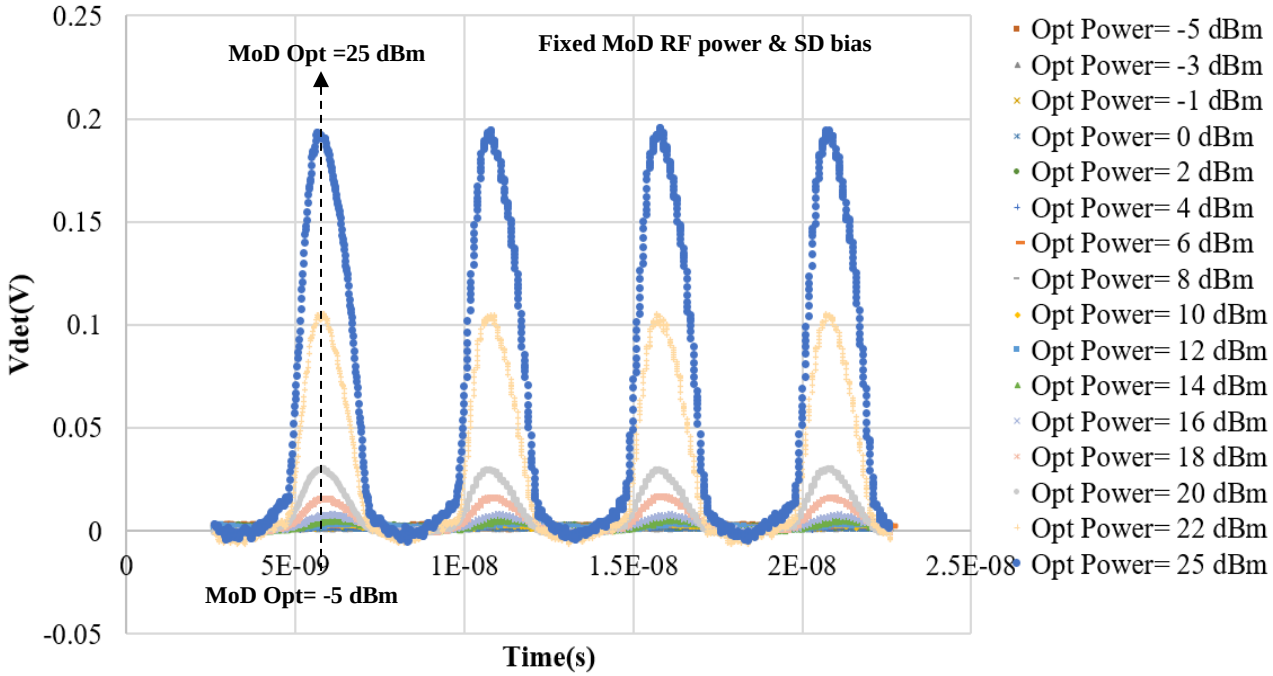


Figure 4-34. Dependency of real-time signal over optical input power. 100um PD-10*20um^2 SD- 200MHz. MoD power= 18 dBm, SD Bias=0.45 V

Figures 4-34 to 4-38 shows the similar measurement plots of the rectifier with 100 μm PD plus 10×20 μm^2 SD with 200 MHz modulator input RF. For this circuit, I also show the real time signal for the devices with SD wokring in lienar region in Figures 4-35 to 4-37 by assessing the device performance over sweeping modulator parameters,

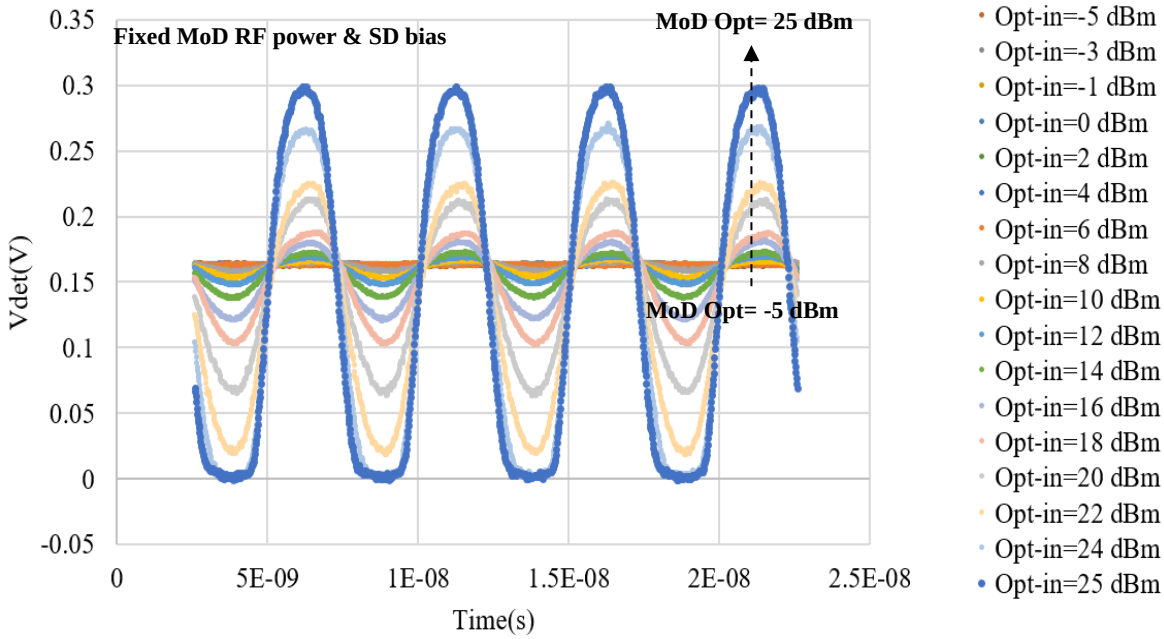


Figure 4-35. Dependency of real-time signal over optical input power. 100 µm PD-10*20 µm^2 SD- 500 MHz. Mod power= 18 dBm, SD Bias=1.15 V

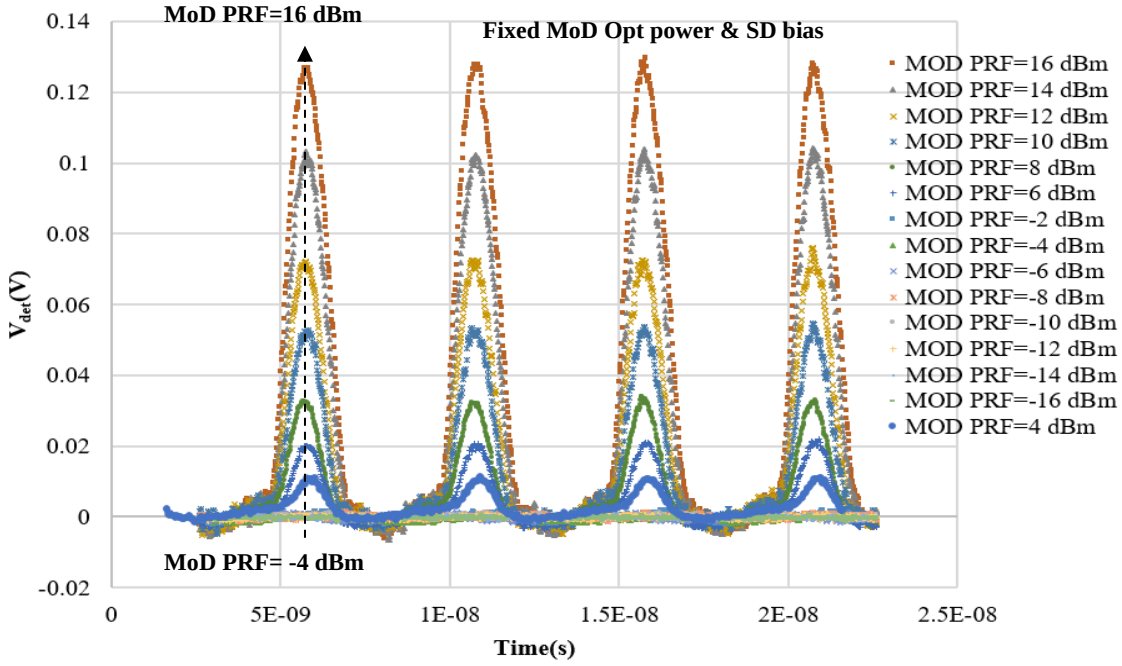


Figure 4-36. V_{det} vs P_{RF}. 100 µm PD plus 10*20 µm^2 SD-200 MHz- Vave vs Modulator PRF. SD bias=0.45 V, PD Bias=-15 V, laser input=23 dBm

As the SD current is measured from the fixed difference values of the two source meters in Figure 4-25 all the curves oscillate around ~0.08 V at the linear region, which is the fixed SD DC current multiplied by the load resistance in Figure 4-37.

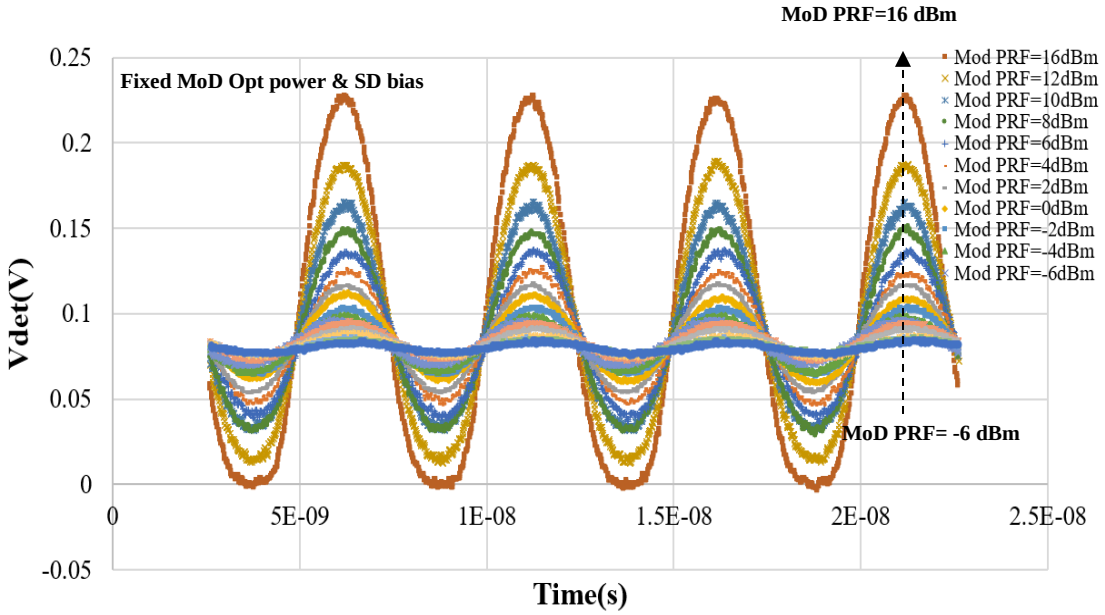


Figure 4-37. V_{ave} vs P_{RF}. 100 µm PD plus 10*20 µm^2 SD-200MHz- Vave vs Modulator PRF. SD bias=1.15 V, PD Bias=-15 V, laser input=23 dBm

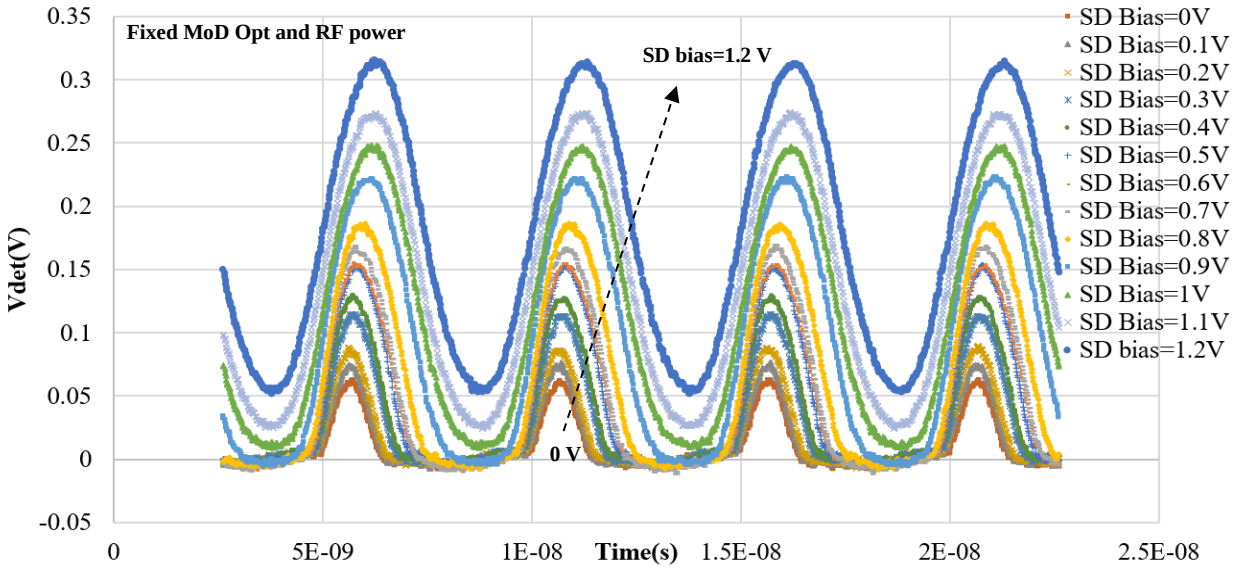


Figure 4-38. 100 µm PD plus 10*20 µm^2 SD-200 MHz- Vave vs SD bias. PD Bias=-15V, 1550 nm laser input=23 dBm, Mod PRF=16 dBm, Mod Vpi/2 bias=6.3V

Figure 4-38 shows that the maximum rectification happens at SD zero bias point with a highly limited dynamic range while there is no rectification over the input signal for higher SD bias but just scaling by SD series resistance.

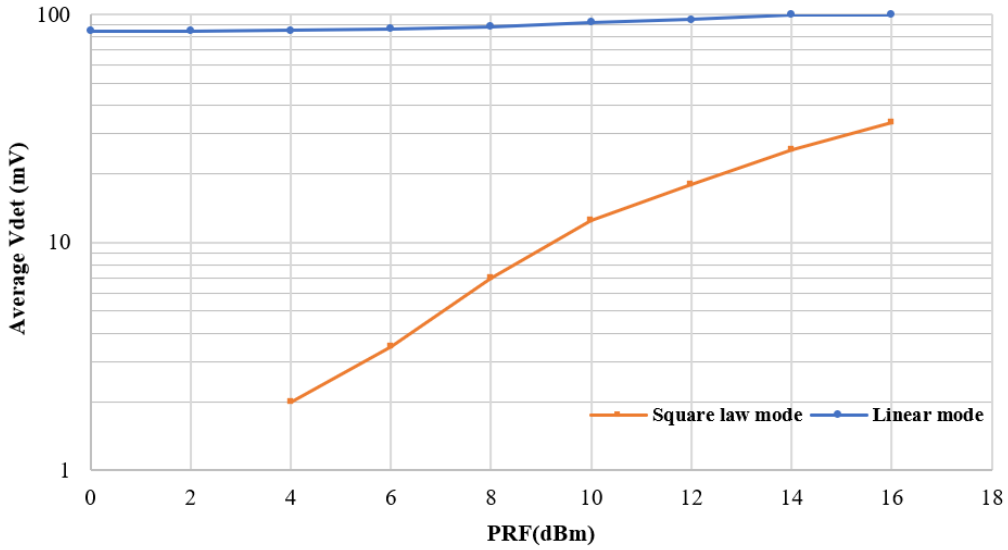


Figure 4-39. comparison of the sensitivity and dynamic range of the detector operating in two modes.

As it's shown in Figure 4-39, the sensitivity of the detector to input RF signal in square law region is higher due to the boosted average value of the rectified signal while the optical power is fixed at maximum possible required for an undistorted output. It confirms a sensitivity of 0.84 V/W over a 12 dB dynamic range of the detector working in the square law region, while the linear mode provides a wider dynamic range of 16 dBm with lower sensitivity of 0.50 V/W. Even though the schematic of our circuit is distinct from the conventional square law detector as the SD is driven by the PD current not its RF voltage, we still have a higher sensitivity in square law region compared to linear region due to the former's non-linearity. On the other hand, since the PD current is proportional to the modulator output power, it's also proportional to the modulator RF power or optical power as well and this is the reason why the plots in Figure 4-39 are quite linear similar to Figure 4-16 .

4.7 Conclusion

The described method presents a new approach for the integration of distinct III-V material systems, catering to more applications, especially in the realm of PICs. In this context, I demonstrated the integration of two applicable devices of distinct epitaxial stack—namely, a mm-wave GaAs Schottky diode and an InP photodiode—on the same substrate. As a proof of concept, I applied this integration to realize an on-chip rectifier. Despite the limited bandwidth, constrained by the PD p-contact series resistance (approximately 7.5 KΩ), the implemented circuit exhibits capabilities in spectroscopy, sensing, and RF measurement. The idea here is that I tightly(<50 μm) combine PDs with SDs and that both – potentially – can achieve high frequencies so this approach can help to make circuits with potentially small parasitic.

In terms of the process development, a new hybrid integration technique based on adhesive bonding on silicon platform was showcased in this work, and this approach can be extended to other III-V or II-IV compounds such as the wide bandgap gallium nitride (GaN) material system, lasers, RF MEMS, etc., provided the individual processing methodologies for each device are established. Moreover, the presented multi-epitaxial integration can be further extended to waveguide platforms, utilizing integrated waveguide materials like silicon nitride (Si_3N_4), tantalum pentoxide (Ta_2O_5), and lithium niobate ($LiNO_3$) for more efficient coupling into the waveguide photonic devices. This extension has the potential to enhance the integration density of wafer bonding on silicon photonic platforms beside other alternatives such as μ-transfer printing [112, 113, 94].

Chapter five:
Conclusion and future works

5.1 Conclusion

The research outlined in this dissertation spanned around heterogenous and hybrid integration of semiconductor devices on RF-photonics platforms. I contributed to the field by designing a GaAs/AlGaAs epitaxial layer for visible photodetector which was less explored in the PIC context. I explored the waveguiding capabilities of this new PIC platform at different wavelengths and characterized the coupling loss. An epitaxial layer was designed based on GaAs/AlGaAs material system considering the fab limitation and the project-specific requirements. The thickness and doping concentration of each layer carefully designed and compositional grading layer were exploited to get an efficient PIN design. Two separate masks were designed for the first- and the second-generation waveguide chips. I also developed and established a specialized fabrication process for the integration of the visible GaAs/AlGaAs PDs on the new tantala waveguide platform. Utilizing Ni/Pd/Au and Ni/AuGe for p-type and n-type ohmic contacts, respectively, and refining these through annealing processes yielded minimum ohmic contact resistance of 7.11×10^{-5} $\Omega.cm^2$ for n contact and 2.77×10^{-5} $\Omega.cm^2$ for p contact. I employed SU8 as adhesive for this integration and investigated another adhesive named BCB too. I did several trial-and-error fab runs to overcome the integration challenges, specifically how to maintain the waveguide integrity during the fab process and how to perform post processing treatment on the damaged waveguide facets. The DC and RF parameters of the visible PDs were also measured which revealed an outstanding minimum dark current of 20 pA, QE of 58 % for red and 56 % for 785 nm wavelengths. I investigated the high-speed performance of the WGPDs using three methods: optical pulse technique for

transient time analysis, electro-optical modulation setups, and pattern generation setup which led to more than 17 GHz bandwidth consistent at both 635 nm and 785 nm wavelengths and 12 Gbit/s open eye diagram for the minimum size PDs.

In the second project, I presented a new method of hybrid integration of the devices of two distinct material systems i.e. GaAs Schottky diode and InP photodiode on the same silicon substrate based on SU8 multi-layered adhesive bonding. The presented technique was important as it can be a simpler, more accurate and applicable alternative to other costly, limited application integration techniques like μ-transfer printing and selective heteroepitaxy. The devices that were implemented using this technique showed acceptable DC and RF performance. A series resistance of 21 Ω, leakage current of 136 fA, and ideality factor of 1.29 for the 200 μm^2 SDs using least square method were obtained while the minimum dark current for the smallest PD was measured to be around 10 nA at 1 V reverse bias and the photocurrent showed no bias-dependent behavior. I used this new integration to realize an on-chip RF rectifier which led to interesting results in the time-domain matches with the simulation. I explored the single PD BW using 1550 nm heterodyne setup and < 2 GHz BW was measured mainly limited by the PD p-resistivity. The square law detector measurement has been done using electro-optical modulator top surface normal setup in conjunction with an external biasing circuitry. I recorded the real-time rectification of the square-law detector for 200 MHz modular RF input in rectifying mode and observed the transition to linear mode using real-time measurement instruments. It confirms a sensitivity of 0.84 V/W over a 12 dB dynamic range of the detector working in the square law region, while the linear mode provides a wider dynamic range of 16 dBm with lower sensitivity of 0.50 V/W.

5.2 Future works

1. Upgrading the visible PD design and epitaxial stack

To improve responsivity and bandwidth, the presented work was a good basis to investigate other device structure such as UTC or MUTC which uses only electron as carrier. Reducing the PD size to 5-7 μm to improve BW using dry etch would expand RC limited bandwidth. Also, redesigning the epitaxial stack with large bandage contact layers(such as InGaP) to reduce absorption in quasi neutral regions to better cover green light and improve QE at shorter wavelengths would be another constructive modification. Using a thicker absorber to reduce C_j and reducing the distance between p-metal and n-mesa are other potential modifications to improve the RC-limited bandwidth.

2. Supercontinuum generation by tantala waveguides:

Since the visible wavelength is almost half of the telecom and 1550nm spectrum, the supercontinuum generation capability of tantala waveguides can be explored using the designed visible PD.

3. AlGaAs/GaAs PDs on other platforms:

GaAs PDs can also be adopted to other waveguide platforms including SiN, LN, and TFLN to compare with tantala.

4. Upgrading the EPIC PD epitaxial layer:

To cover higher frequency by exploiting MUTC or UTC design for PD epitaxial stack to realize a higher frequency on-chip RF rectifier in integration with THz Schottky diode which will have application in spectroscopy. Once we make sure we have enough high frequency RF power, we can consider adding the matching circuits and on chip lumped elements to realize the right applicable circuits like a hybrid photo-mixer or multiplier.

5. Photonic-based THz subharmonic generation

mm-Wave multipliers often employed a signal generator may or may not in conjunction with a frequency extender to pump the Schottky-based multiplier circuit [43]. The presented EPIC provides a basis to design another alternative for pumping an on-chip subharmonic multiplier.

6. Hybrid optically pumped THz on-chip subharmonic mixer.

Works have been done to provide optical LO for THz mixers using waveguide interconnections to connect the discrete packages [103]. Our hybrid integration technique can be employed to process all the sections of such mixer on the same chip.

5.3 Publications

[1] "Heterogeneously integrated AlGaAs/GaAs photodiodes on tantala waveguides" M Jafari, T Fatema, D R. Carlson, S B. Papp, and A Beling. Journal of Lightwave Technology, 2024 (under review).

[2] "Heterogeneous 3D Integration of GaAs- and InP-based Electronic-Photonic Devices onto Si Using Multi-Layer Adhesive Wafer Die Bonding for Photonic-Radio Frequency Applications" M Jafari, R M. Weikle, and A Beling. IEEE Transactions on Electron Devices, 2024 (under review).

[3] "Heterogeneous integration of AlGaAs/GaAs photodiodes on tantala waveguides for visible-light applications" M Jafari, DR Carlson, S B. Papp, A Beling CLEO 2022.

[4] "High-performance modified uni-traveling carrier photodiode integrated on a thin-film lithium niobate platform" Xiangwen Guo, Linbo Shao, Lingyan He, Kevin Luke, Jesse Morgan, Keye Sun, Junyi Gao, Ta-Ching Tzu, Yang Shen, Dekang Chen, Bingtian Guo, Fengxin Yu, Qianhuan Yu, Masoud Jafari, Marko Lončar, Mian Zhang, Andreas Beling, Photonics Research 10 (6), 1338-1343, 2022.

[5] "A WR-5 (140-220 GHz) Quasi-Optical Phase Shifter Array Based on GaAs Schottky Diodes Integrated on Thin Silicon Membranes" S Nadri, M Jafari, RM Weikle 45th International Conference on Infrared, Millimeter and Terahertz Waves (IRMMW-THz) 2020.

[6] "Measurement and Extraction of Parasitic Parameters of Quasi-Vertical Schottky Diodes at Submillimeter Wavelengths" S Nadri, L Xie, M Jafari, M F. Bauwens, A Arsenovic, R M. Weikle. IEEE Microwave and Wireless Components Letters, 2019.

[7] "Submillimeter-wave Schottky diodes based on heterogeneous integration of GaAs onto silicon" RM Weikle, L Xie, S Nadri, M Jafari, CM Moore, N Alijabbari, Michael E Cyberey, N Scott Barker, Arthur W Lichtenberger, Charles L Brown United States National Committee of URSI National Radio Science Meeting, 2019.

[8] “A 160GHz Frequency Quadrupler Based on Heterogeneous Integration of GaAs Schottky Diodes onto Silicon Using SU-8 for Epitaxy Transfer” Souheil Nadri, Linli Xie, Masoud Jafari, Naser Alijabbari, Michael E. Cyberey, N. Scott Barker, Arthur W. Lichtenberger, Robert M. Weikle II International Microwave Symposium, Philadelphia, 2018.

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