# Heterogeneous Silicon Photonics: Photodiodes Based on Heteroepitaxy and Adhesive Bonding, and Micro-Transfer Printed Modulators

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## Abstract

Silicon photonics has attracted considerable research interest in recent years. Leveraging complementary metal-oxide semiconductor (CMOS) infrastructure for the fabrication of photonic integrated circuits (PICs), silicon photonics has been increasingly adopted for optical data communications, microwave photonics, sensing, imaging, biomedical, and AI applications. A primary challenge for silicon photonics has been the absence of high-performance active components, which predominantly rely on group III-V materials. Given that high-speed photodetectors and modulators are fundamental to photonic circuits, my thesis focuses on the integration of high-performance III-V photodetectors and modulators onto silicon photonic platforms using different integration techniques. My dissertation is structured around several key devices: III-V waveguide photodetectors on silicon by heteroepitaxy, high-speed photodetectors integrated on silicon nitride (SiN) platform via heterogeneous integration, micro-transfer printable Mach-Zehnder modulators, and foundry-enabled silicon PICs.

In the project concerning photodetectors via III-V-on-Si heteroepitaxy, I led both fabrication and characterization efforts. We demonstrated the first high-speed III–V waveguide (WG) photodiodes (PDs) epitaxially grown on Si having high responsivity of 0.78 A/W and a 3-dB bandwidth of 28 GHz. Also, an open non-return-zero (NRZ) 40 Gbit/s eye diagram was detected by our device.

In the work on high-speed photodetectors integrated with microresonators on the SiN platform, I led the device design, fabrication, and characterization. The resulting PD exhibited a responsivity of 0.45 A/W, a 53-GHz 3 dB bandwidth, and a maximum radio frequency (RF) output power of -8.9 dBm at 50 GHz. Balanced PDs of this type achieved a record-high 3-dB bandwidth of 30 GHz and a common-mode rejection ratio (CMRR) of 26 dB. Notably, the photodetector's fabrication process that I developed had negligible impact on the microresonator's performance, demonstrating its suitability for integration into high-speed applications on the SiN platform.

A significant part of my thesis addresses high-speed transfer-printable O-band Mach-Zehnder modulators (MZMs). Here, I devised a completely new fabrication process for modulator chiplets, and developed the measurement methodology in our lab. The multi quantum well (MQW) MZM demonstrated remarkable performance metrics: a halfwave voltage-length product  $(V_{\pi} \cdot L)$  of  $3 \text{ V} \cdot \text{mm}$ , a bandwidth exceeding 67 GHz, and an extinction ratio of up to 17 dB. Moreover, our modulator chiplets were successfully transfer-printed onto a SiN waveguide chip with a promising yield.

Finally, another topic of my PhD work centered on silicon PIC design: the presented optoelectronic frequency mixer showed a 3-dB bandwidth of 30 GHz, with potential scalability for multi-channel applications.

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# Chapter 1

## Introduction and Motivation

Silicon photonics has attracted intense research efforts in recent years. With the goal to integrate high-performance active devices on silicon, my research centers around three methods to achieve heterogeneous silicon photonics: heteroepitaxy, adhesive bonding, and micro-transfer printing. My work includes both, the development of photodetectors and modulators for high-speed high-power applications, both of which are not available on silicon to date.

## 1.1 Silicon Photonics

### 1.1.1 Background

The digital revolution that shaped our modern world has been driven by the remarkable advancements in silicon (Si) microelectronics, and it continues to grow exponentially following Moore's Law. As data-intensive applications and technologies continue to evolve, traditional electronic interconnects are struggling to keep up with the exponential growth in data traffic. This is where optical interconnects step in as a promising solution due to its high bandwidth, low latency and energy efficiency. Beyond data center applications, fields such as wireless and telecommunications are increasingly adopting photonic solutions, benefited by its broadband operations, low loss and immunity to electromagnetic interference. The shift from purely electronics solutions towards photonics and photonic-electronic integrated circuits seems inevitable in these areas. At the forefront of this transition is Si photonics, a compact, scalable, and efficient technology.

Silicon photonics is the result of merging mature silicon-based fabrication techniques with optical principles, heralding a transformative era for data transmission, processing and communication. Building upon the pioneering efforts of Soref et al. [1] in the mid-1980s, the realm of silicon photonics quickly captured the attention of researchers due to its multifaceted benefits[2]–[4]. Primarily, silicon photonics leverages decades of research work and substantial investments dedicated to silicon microelectronics, facilitating cost-efficient, highyield, and robust processing capabilities. In contrast to the commonly used InP wafers for photonic circuits, the cost of silicon photonic chips is much reduced (10 times lower) and can scale up to 300-mm diameter wafer processing using standard CMOS facilities. Moreover, the inherent optical properties of silicon and silicon-compatible materials, particularly their transparency in commercially vital infrared wavelengths, contribute to the allure of this technology. Furthermore, the seamless integration of photonics into silicon's well-established infrastructure fosters a cohesive collaboration with electrical integrated circuits (EIC), amplifying its potential for future innovation and fostering a promising avenue for technological advancement.

The exploration into silicon photonic devices was initiated with an emphasis on developing high-quality waveguides [5]. This initial focus yielded the creation of low-loss, tightly bending silicon-on-insulator (SOI) waveguides [6], subsequently facilitating the realization of passive components such as splitters [7], crossings [6], and directional couplers [8]. Simultaneously, active components such as tunable ring-resonators [9] and Mach-Zehnder modulators [10], utilizing the plasma-dispersion effect, were extensively researched and integrated onto the platform. Progressing further, advancements in epitaxy enabled the wafer-level growth of high-quality germanium on silicon through molecular beam epitaxy (MBE), thereby enabling the fabrication of efficient SiGe photodetectors despite the lattice constant mismatch between Si and Ge. However, in the C- and L-bands, the absorption coefficient of germanium, which has an indirect bandgap, is influenced by growth conditions, typically around  $3000 \text{cm}^{-1}$  with a long wavelength cutoff. In contrast, photodetectors based on group III-V materials usually use InGaAs with its direct bandgap, and present a much higher absorption coefficient in the C band and consistent absorption across the L-band. Compared to Ge PDs, the InGaAs/InP PDs exhibit high absorption efficiency, lower dark current, and high power handling capability. Moreover, they offer great flexibility in band engineering for diverse design needs [11]. Another challenge of achieving comprehensive silicon PICs remains due to the absence of a laser source. This is a significant hurdle as the indirect bandgaps of silicon and germanium preclude the possibility of a monolithic silicon laser. Innovative strategies, including integrating lasers onto silicon chip through packaging like flip-chip bonding, or the heterogeneous integration of III-V materials onto silicon (discussed in more detail in Section 1.1.2), have emerged as promising avenues to address the laser challenge and also enhance the performance of other optical components like detectors and modulators, by substituting them with III-V based devices.

Integrated silicon photonics offers a promising solution for communication and interconnects using optical channels. The waveguide system enabled by silicon, silicon dioxide and silicon nitride provides the basic building block of chip-based applications. Photonic devices, including lasers, modulators and photodetectors can be monolithically or heterogeneously integrated and interconnected on the silicon photonic platform, contingent on the waveguiding systems. The progression of silicon photonics is happening in academia and industry simultaneously. Silicon photonics demonstrates exceptional utility in applications demanding cost-effective, high-bandwidth interconnect capabilities. The optical device count on a single Si PIC is attributed to robust device yields and application-driven requirements for large-scale PICs, spanning high-speed transceivers, LIDAR, optical computing and quantum photonics. Figure 1.1 (a) shows the evolution of photonic device integrated on single PICs, including monolithic InP, monolithic Si and heterogeneous III-V/Si integration. Figure 1.1 (b) illustrates the trend toward greater bandwidth and lower power consumption in the silicon photonics realm.



Figure 1.1: (a) Number of photonic components integrated in a single PIC. (b) The evolution of PIC bandwidth, power efficiency, and total power consumption. [12]

The development of next-generation photonic integrated circuits necessitates the use of wide bandgap materials that go beyond the traditional  $Si/SiO_2$  waveguides. Among the alternatives, silicon nitride ( $Si_3N_4$ ) waveguides, which are fully compatible with the SOI platform, have increasingly garnered attention over the past decades. The allure of silicon nitride waveguides can be attributed to several key features. These include remarkably low propagation losses, as low as 0.3 dB/m, an expansive transparency window that spans from visible to mid-infrared spectrum (as depicted in Fig. 1.2), and notable nonlinear properties. In contrast to silicon waveguides, which have their power handling capability significantly constrained by two-photon absorption, SiN has a much larger bandgap, enabling waveguides for much higher optical power. Such characteristics make silicon nitride waveguides particularly suitable for ultrahigh-Q resonators, highly selective tunable filters, and narrow

linewidth tunable lasers.



Figure 1.2: Transparency windows of  $Si_3N_4$ , Si and InP

### **1.1.2 Heterogenous Silicon Photonics**

Silicon photonics stands as a disruptive technology poised to revolutionize integrated photonics. However, silicon photonics based solely on the SOI platform encounters notable challenges, primarily the absence of a native light source and limitations in the performance of other active components. To address these constraints, the concept of heterogeneous silicon photonics was introduced [13], [14], integrating III-V materials with silicon. This approach harnesses the strengths of silicon photonics while capitalizing on the exceptional optical properties intrinsic to III-V materials. In contrast to traditional III-V/Si integration methods like butt-coupling or flip-chip packaging, contemporary heterogeneous silicon photonics presents a more compact and efficient process technology. It delivers low-power, cost-effective, high-capacity, high volume and high-yield solutions. Various methods achieve heterogeneous III-V/Si photonics.

The first approach involves direct heteroepitaxial growth of III-V layers on silicon or SOI using techniques like MBE or Metal-Organic Chemical Vapour Deposition (MOCVD), often utilizing intermediate buffer layers such as Ge and GaAs to mitigate the dislocations due to lattice mismatch. This method, illustrated in Figure 1.3, offers both robustness and efficiency, representing a genuine wafer-level solution. There are several devices successfully reported on silicon using heteroepitaxy including QD (quantum dot) DFB (distributed feedback) lasers[15] and photodetectors [16] [17].



Figure 1.3: (a) Schematic of the GaAs grown on the Ge/Si. (b) Cross-sectional TEM image of Ge layer grown on Si [18]

The second approach is wafer-bonding, encompassing direct, molecular, metal and polymer/adhesive bonding. As depicted in Figure 1.4, unprocessed III-V thin films are transferred onto silicon or SOI wafers and subsequently fabricated. Compared to direct epitaxial growth, wafer bonding provides a versatile and flexible means of integrating dissimilar materials [14], [19]. Years of development and mature processes have led to the realization of numerous high-performance optical devices using wafer bonding, for example grating based DFB [20] or DBR (distributed Bragg reflector) lasers [21], EAM (electroabsorption modulators) [22], MZM (Mach-Zehnder modulators) [23] and photodetectors [24].



Figure 1.4: Schematic of III–V on Silicon bonding process flow[25]

Another innovative method is micro-transfer printing ( $\mu$ TP), schematically illustrated in Figure 1.5 [26]. Devices are initially processed on the III-V wafer and protected by an encapsulation layer with local openings to access the release layer, which is then underetched. Following release, the devices or material coupons (chiplets) can be picked up and transferred to the target wafer.  $\mu$ TP proves to be a potent approach for densely integrating various optical components from one or multiple III-V source wafers, onto silicon photonics target wafers. This approach significantly enhances the efficiency of III-V wafer utilization compared to die-to-wafer bonding. Furthermore, the integration process necessitates no modifications to SiPh back-end processes, rendering it highly compatible with existing SiPh infrastructure when compared to heteroepitaxial growth.



Figure 1.5: (a) Schematic of  $\mu$ TP-based integration on Si photonic wafers in a parallel manner (b) Fabrication process of  $\mu$ TP devices [26]

## **1.2** Microwave Photonics

Microwave photonics (MWP) represents a powerful convergence of microwave engineering and optical technology, creating a field that offers great potential in diverse applications. MWP is dedicated to the generation, processing, control and distribution of microwave signals via photonic means [27]. By harnessing the inherent advantages of optical communication- such as high bandwidth, immunity to electromagnetic interference, reduced size, weight and cost, and low signal loss over extensive distances—MWP pushes the boundaries of microwave technology. Recent years have witnessed a surge in research exploring microwave photonic techniques for diverse applications, including broadband wireless access networks, radar, and satellite communications.

At its core, a typical MWP system includes a laser light source, an optical modulator, an optical signal processor, and a photodetector. Fig. 1.6 illustrates the MWP system schematic. An RF input signal is applied on the modulator or directly on the laser, translating its spectrum into the optical frequency domain, resulting in sidebands around the optical carrier frequency. The modulated optical signal undergoes processing via an optical system, which encompasses an array of photonic devices that together form the optical signal processor. At the end of optical link, a photodetector is employed to downconvert the signal, so the processed RF signal can be recovered. Functions facilitated by an MWP system span antenna remoting [28], RF photonic filtering, phase shifting, optical beamforming, arbitrary waveform generation, frequency conversion, and microwave signal generation.



Figure 1.6: Schematic of a MWP system

To date, MWP systems commonly employ discrete photonic devices, fiber-centric components, and fibers. However, with the rapid development of photonic integration technologies, there's been a transformative shift in the landscape. The adoption of photonic integration led to a substantial reduction in the MWP system's footprint size while keeping its high complexity [29]. Platforms such as InP [30], SOI [31], and silicon nitride [32] have been explored for integrated MWP circuits. Notably, the silicon platform is emerging as a frontrunner, attributed to its potential to facilitate compact, high-performance integrated MWP solutions [33].

# Chapter 2

# Photonic Device Fundamentals: Photodiodes and Modulators

## 2.1 Photodiode fundamentals

Photodetectors (PDs) are devices capable of generating electrical signals that are representative of incoming optical signals. With an increasing need for high-speed data transmission in fields such as telecommunications and data centers, there has been an exponential growth in demand for photodetectors possessing high bandwidth capabilities. In this section, I'll introduce the fundamentals of photodiodes including figures of merit and structures of PDs.

### 2.1.1 Photodiode figures of merit

### Responsivity

Responsivity is a critical parameter for evaluating the photodiode's ability to convert incoming optical signals into an electrical current. The current produced by a photodiode consists of two parts: the photo-generated photocurrent and the device's dark current. The dark current is the current that flows through a photodiode when no photons are injected into it. This dark current primarily arises from random electron and hole generation, influenced by processes such as Shockley-Read-Hall (SRH) recombination, diffusion currents, and trap-assisted tunneling [34].

To define responsivity, we focus solely on the photo-generated current or photocurrent. Quantified in amperes per Watt (A/W), the external responsivity of a photodiode signifies the photocurrent produced per unit of input optical power (typically measured at the tip of the input optical fiber), and is formally represented by the following equation:

$$R_{\rm ext} = \frac{I_{\rm photo}}{P_{\rm optical}} = \frac{I_{\rm total} - I_{\rm dark}}{P_{\rm optical}}$$
(2.1)

where  $I_{\text{photo}}$  is the photon-generated current,  $I_{\text{total}}$  is the total current,  $I_{\text{dark}}$  is the dark current of the device, and  $P_{\text{optical}}$  is the input optical power.

As the photon energy is related to the optical frequency, another parameter to quantify the efficiency of converting optical power to electrical current is the quantum efficiency. Essentially, photon energy corresponds to its optical frequency and is inversely proportional to its wavelength. Quantum efficiency is thus defined as the ratio of generated charge carrier pairs to the number of photons incident on the device. This can be mathematically represented as:

$$\eta_{\text{ext}} = \frac{N_e}{N_\nu} = \frac{I_p/q}{P_\nu/h\nu} = R_{\text{ext}} \cdot \frac{h\nu}{q} = R_{\text{ext}} \cdot \frac{1.24}{\lambda(\mu m)}$$
(2.2)

where  $\eta_{\text{ext}}$  stands for quantum efficiency,  $N_e$  represents the number of electrons generated,  $N_{\nu}$  is the count of incoming photons,  $I_p$  is the photocurrent, q is the charge of an electron,  $P_{\nu}$  is the power of the incoming optical signal, h is Plank's constant,  $\nu$  is the frequency of the light, and  $\lambda$  represents its wavelength. For photodiodes that don't have internal gain mechanisms, the quantum efficiency can reach a theoretical maximum of 100%. Consequently, the highest external responsivity these devices can achieve is 1.25 A/W at 1550 nm and 1.05 A/W at 1310 nm.

### **Bandwidth**

Bandwidth stands as a pivotal parameter of a photodiode's speed performance. The 3dB bandwidth is defined as the frequency where the RF power output from the photodiode is 3 dB below its value at near-DC. Two primary factors constrain this bandwidth: the carrier transit time and the resistance-capacitance (RC) time constant. The bandwidth can be estimated using equation 2.3

$$f_{\rm tot} = \sqrt{\frac{1}{\frac{1}{f_{\rm tr}^2} + \frac{1}{f_{\rm rc}^2}}}$$
(2.3)

For a conventional PIN photodiode, the transit time bandwidth  $(f_{tr})$  can be approximated with the equation 2.4 [35]

$$f_{tr} = \frac{3.5\nu}{2\pi d_{abs}} \tag{2.4}$$

Here,  $\nu$  represents the average carrier drift velocity, and  $d_{abs}$  is the thickness of the depletion layer in the PIN structure. The drift velocity is directly proportional to the carrier mobility, and is also related to the electric field. Typically, to maintain high drift velocity, a high electric field is required in the PD's depletion width.

The RC-limited bandwidth  $(f_{RC})$  is defined as:

$$f_{RC} = \frac{1}{2\pi R_{tot} C_{tot}} \tag{2.5}$$

Where  $R_{tot}$  and  $C_{tot}$  denote the circuit's total series resistance (including the external load resistor) and capacitance, respectively.



Figure 2.1: Equivalent circuit of photodiode

Figure 2.1 depicts a photodiode's equivalent circuit. Here,  $C_j$ ,  $R_s$ ,  $R_{sh}$ , and  $R_L$  correspond to the junction capacitance, series resistance, shunt resistance, and load resistance, respectively. The delineated frame indicates the connection between the photodiode and the load resistor, commonly a coplanar waveguide (CPW). This connection typically introduces both inductance and additional capacitance to the circuit. Within this configuration, the series resistance  $R_s$  is often minimal (around 10  $\Omega$ ) when compared to the load resistance (50  $\Omega$  in RF circuit). As a result, the junction capacitance largely determines the RC bandwidth. There are two primary methods to reduce the junction capacitance: by reducing the active device size or by increasing the depletion region thickness. However, the latter technique may lead to a reduction in the transit time-limited bandwidth. Balancing these bandwidths require careful design and novel structures to achieve the best speed performance.

#### Saturation power

The RF output power of a photodiode represents the AC power delivered to the load resistor, typically 50  $\Omega$ . For a sinusoidally modulated optical signal, the ideal photocurrent is given by equation 2.6

$$I_{\rm ph} = I_{\rm avg} + \alpha I_{\rm avg} \sin(2\pi f t) \tag{2.6}$$

Here,  $I_{\rm avg}$  is the average or DC component of the photocurrent,  $\alpha$  indicates the modu-

lation depth of the input optical signal, and f stands for modulation frequency. Given that the DC component usually gets filtered by a bias T in the external circuit, only the AC component of current reaches the load. Consequently, the RF power, as perceived by the receiver, is given by:

 $P_{\text{load}} = \frac{1}{2} (\alpha I_{\text{avg}})^2 R_{\text{load}}$ 

(2.7)



Input optical power (dBm)

Figure 2.2: Power transfer plot of photodiode showing 1-dB power compression

In a perfect scenario, the RF output power exhibits a quadratic increment with the increase of optical input power. On a logarithmic scale, this increase is linear with a slope of 2, depicted by the dashed line in Fig2.2. Nonetheless, practical photodiodes don't always match the ideal linear progression. Their RF output power will variably reach a point of saturation under large input optical power. The saturation power and saturation current of a photodiode are defined as the output power and photocurrent at which the RF power drops to 1 dB below the ideal relation. The saturation power can be influenced by many factors, among which the space-charge effect is of the upmost importance. This phenomenon is attributed to the accumulation of photo-generated charge carriers within the diode's depletion region. The electric field induced by these free carriers can work against the field originating from ionized dopants and the applied reverse bias. Consequently, a diminishing electric field slows carrier movement since the carrier drift velocities are closely related to electric field. This drop of carrier velocity leads to the saturation of RF output power. To mitigate this effect, layer engineering strategies can be employed, ensuring the sustenance of an elevated electric field within the depletion region. This topic will be discussed in detail in section 2.1.2

### Nonlinearity

The linearity of a system describes the extent to which the output mirrors linearly with the input without distortion. In photodiodes, the degree of linearity directly influences the spurious free dynamic range (SFDR), a key parameter in RF-over-fiber (RoF) analog optic links. Fig. 2.3 displays the power spectrum when the system is fed with closely-spaced fundamental frequencies,  $f_1$  and  $f_2$ . Among the various distortions present in the system output, the third-order intermodulations (IMD3) stand out as particularly problematic. Their proximity to the fundamental signals make them challenging to filter out in subsequent circuits, significantly compromising the linearity of the device.





To quantify the linearity of a photodiode, the third-order output intercept point(OIP3) is often characterized. As illustrated in Fig. 2.4, OIP3 is conceived from the hypothetical intersection of the fundamental signal and the IMD3 power. For every 1 dB rise in input power, the system's output power at the fundamental frequency increases by an equivalent 1 dB, while the IMD3 growth rate is 3 dB. The point where linear extrapolations of these two trends converge is the OIP3.



Figure 2.4: OIP3 definition

The root causes of photodiode nonlinearity are diverse. They range from the phenomena like carrier velocity modulation, carrier recombination, and nonlinear capacitance to optical effects. For instance, changes in the refractive index due to variations in the electric fields and carrier concentrations can lead to nonlinear responses.

### 2.1.2 Photodiode structures

III-V semiconductor photodetectors have distinguished themselves as superior components, excelling in speed, sensitivity and operational wavelength range. In the realm of telecommunications and data communications, Indium Gallium Arsenide/Indium Phosphide (InGaAs/InP) photodiodes are favored for their high absorption efficiency and rapid response times. The PIN photodiode is an architecture where an intrinsic InGaAs absorptive layer is flanked by wider-bandgap n- and p-type contact layers, typically InP [36]. Although this structure is simple and yields good performance, it has limitations in terms of speed and high-power performance, largely attributed to the space charge effect. Typically, holes accumulate in a PIN PD because their drift velocity is substantially lower than that of electrons. This accumulation suppresses the electric field, resulting in reduced carrier transit time, as illustrated in Fig. 2.5.



Figure 2.5: Comparison of PIN, UTC and MUTC in band diagram, carrier density, electric field

In 1997, T. Ishibashi et al. introduced the uni-traveling-carrier photodiode (UTC-PD) [37], which mitigates the space charge effect significantly by incorporating a p-doped absorber layer and an intrinsic InP drift layer. In this design, absorption occurs in the p-region and only the faster electrons drift through the depleted drift layer. However, to achieve high responsivity, a thicker absorber layer is necessary, which eventually limits bandwidth

performance if carrier transport in the absorber is based on diffusion only.

Subsequent development led to the introduction of modified uni-traveling-carrier (MUTC) photodiodes[38]–[40]. By separating p-doped and intrinsic absorber layers, the PDs exhibit enhanced responsivity while sustain high-speed performance. Additionally, an increase in the thickness of depleted region positively impacts the RC bandwidth. The space charge effect within the depleted absorber remains minimal as long as the layer is kept thin. In certain designs, a moderately doped "cliff" layer is added to compensate decreasing electric field. Given the freedom for layer engineering, an optimum balance between high responsivity, high bandwidth, and large saturation power can be achieved through comprehensive optimization of the MUTC design [41][42].

### 2.1.3 Photodiode characterization techniques

### DC: Current-Voltage (IV) and Capacitance-Voltage (CV)

A semiconductor parameter analyzer (HP4145B) was utilized to measure the currentvoltage curve of the devices. Measurements were typically conducted on the stand-alone probe station, equipped with a shield to effectively block room light. By sweeping the applied voltage and monitoring the current, a precise dark current curve can be obtained. Such IV measurements are instrumental in assessing dark current characteristics and quickly determining device functionality.

For the capacitance-voltage measurement, and similar to the IV test, the voltage is swept from 0 to reverse bias. A common choice is a frequency of 1 MHz, and the voltage usually ranges from 0 V to reverse voltages of around -5 V. After a full sweep, a CV curve is obtained that initially descends and then stabilizes at certain level of tens to hundreds of fF depending on the device design. This measured curve is consistent with the principles of pn junction physics. The CV test provides insights into the device's capacitance and rough estimation of device operating voltages, which can be identified as the voltages when the curve flattens out at minimum value. At this voltage level, the junction is fully depleted, ensuring that the bandwidth performance isn't constrained by a suboptimal junction capacitance.

### Bandwidth and saturation power

This section includes the methodology adopted for bandwidth and saturation power measurements. As elaborated in Section 2.1.1, the 3-dB bandwidth of a photodiode represents the frequency where the RF output power of the PD drops by 3dB relative to the power at near-DC frequency. As indicated by equation 2.6, the AC current or power is a function of not just the photodiode's performance, but also the modulation depth of the testing apparatus. In order to maintain a consistent 100% modulation depth across the wide frequency range, a heterodyne setup is usually employed.

Optical heterodyning involves two lasers, operating at slightly different wavelengths. When these lasers are combined, a beat RF-modulated optical signal emerges. Fig. 2.6 illustrates the configuration of the setup. In our typical experimental setup, we use two external cavity lasers (ECLs) or a combination of one ECL and a temperature-controlled diode laser. Before conducting any measurements, it's essential to calibrate the power and polarization of these lasers. We ensure both lasers have the same power level by monitoring the input power of the EDFA. To align the polarizations of the two lasers, we utilize a commercial photodetector (PD) and an RF power meter. When the wavelengths of the two lasers are closely matched, producing a near-DC beat signal, this optical output is directed to the commercial PD. The resulting RF power from the PD can then be measured using the RF power meter. By manipulating the two polarization controllers located right after each laser, we can influence the observed RF power. Ideally, when the RF power peaks (commonly around -16 dBm for a 1 mA photocurrent with a 50  $\Omega$  termination), it indicates that the lasers' power and polarization are perfectly aligned, achieving a modulation depth close to 100%.



Figure 2.6: Configuration of pd bandwidth setup

Post calibration, the beat optical signal is split into two pathways by a second 3-dB coupler: one of its outputs is fed through the Erbium-Doped Fiber Amplifier (EDFA) to the device under test, while its second output is directed to a commercial photodiode, that is connected to an ESA (for DC to 50 GHz) or a wavelength meter (for > 50 GHz) to ascertain the beat signal's frequency. Subsequent to the EDFA, a Variable Optical Attenuator (VOA) controls the input power directed to the device. Another polarization controller, situated ahead of the Device Under Test (DUT), is needed for waveguide PDs. Once the optical signal reaches the PD, the output electrical signal is captured by the RF probe. To separate DC and AC signals, a bias tee is connected to the probe. The DC outlet is linked to a Keithley souecemeter, while the RF segment interfaces with RF power meter for accurate power readings. During the measurement process, we maintained the wavelength of one laser constant while adjusting the wavelength of the other, allowing us to shift the beat signal

frequency. We recorded the RF power in relation to the signal frequency to determine the frequency response of our device.

We employed the same setup to gauge the saturation power of the device at a specific frequency. During this saturation power assessment, the beat signal frequency remained constant, while we adjusted the input optical power level by modifying the attenuation factor on the VOA. As the optical power increased, we documented both the photocurrent and the RF output power. We anticipate results akin to those presented in Fig. 2.2.

## 2.2 Mach-Zehnder Modulator (MZM) fundamentals

### 2.2.1 Working principle

The Mach-Zehnder modulator (MZM) has been widely used for broadband photonic analog links and high-speed digital optical fiber communication systems, renowned for its broadband operation, high modulation efficiency, high speed, low power consumption and capability to handle large power. As depicted in Fig. 2.7, the MZM operates as an interferometerbased optical intensity modulator. Here, incoming light is split into two separate arms, each creating a phase delay on it. The essence of its operation is hinged upon the electro-optic effect within the arms: when an electric field is applied, the refractive index of the material changes, thereby shifting the phase of the optical signal. When the light from these branches is combined, this phase difference culminates in amplitude modulation due to interference. The relation between output light intensity and phase difference between arms is demonstrated in Fig. 2.8. When the MZM is optimally biased at its quadrature point with a small signal, it can be considered as working in a linear region, ensuring an output signal that is proportional to the input signal.


Figure 2.7: Schematic of push-pull MZM



Figure 2.8: Relation between optical output and phase difference

The electro-optic (EO) effect is paramount in this mechanism. Various materials are favored for their pronounced EO effect, including Lithium Niobate (via Pockels effect), Silicon (through the Plasma dispersion effect), GeSi (employing the Franz-Keldysh effect), and the III-V multi-quantum well (MQW) primarily utilizing the Quantum Confined Stark Effect (QCSE). Our focus centers on the III-V MQW structure, which benefits from its strong EO effect and wavelength engineering capability. When applying a reverse bias across the MQW several OE effects can occur, with the QCSE being the strongest. In the QCSE, the band structure of the QW will be tilted when an electric field is applied which effectively reduces the energy difference between the two ground states [43], as visualized in Fig. 2.9. While this reduction will change the absorption coefficient (it increases for longer wavelengths), it will also change the real part of the refractive index through Kramers-Kronig relation. Mathematically, the QCSE effect can be described as a second-order EO effect, with its relation given by:

$$\Delta_{nQCSE} = n^3 \times R \times E^2 \tag{2.8}$$

where n is the refractive index of the material, R represents the empirical quadratic EO coefficient, E is the electric field.



Figure 2.9: QCSE working principle

In parallel, the Pockels effect, an anisotropic phenomenon directly proportional to the applied field, is given by:

$$\Delta_{nPockels} = n^3 \times r_{41} \times E \tag{2.9}$$

with  $r_{41}$  being the Pockels coefficient. This effect is dependent on the orientation of the applied fields and crystal plane. Additionally, carrier depletion effects, such as the plasma effect and band-filling effect, correlate with carrier concentration. The collective refractive index alteration is the net effect of these various effects, with typically QCSE being the

primary contributor.

High performance III-V MZMs have been developed based on GaAs [44] and InP [45]. In comparison with silicon ring modulators, the III-V MZM has a much wider optical bandwidth and higher speed and better power handling capability that make it very competitive in optical communication networks. In contrast to Lithium Niobate (LN) MZMs, III-V based devices have a more compact footprint, making them ideal candidates for tight integration. The comparative attributes of various modulator types are listed in table 2.1

Efficiency	Bandwidth	Optical band-	Power han-
$(V_{\pi} \cdot L)$		width	dling ability
Low	Moderate	Wide	Low
High	High	Very narrow	Low
Low	High	Wide	High
High	High	Moderate	High
High	High	Wide	High
	Efficiency $(V_{\pi} \cdot L)$ Low High Low High High	EfficiencyBandwidth $(V_{\pi} \cdot L)$ ModerateLowMighLowHighHighHighHighHighHighHighHighHigh	EfficiencyBandwidthOptical band- width $(V_{\pi} \cdot L)$ widthLowModerateWideHighHighVery narrowLowHighWideHighHighModerateHighHighModerateHighHighWide

Table 2.1: Comparison of various high-speed modulator types (RM: ring modulator, EAM: Electro-absorption modulator)

#### 2.2.2 Figures of Merit

# Modulation efficiency: $V_{\pi}L$ and Extinction Ratio

For optical modulators, efficiency and compactness are of great importance. The figure of merit  $V_{\pi}L$  stands as a central metric in characterizing the modulation efficiency of devices. The parameter  $V_{\pi}$  is defined as the voltage required to induce a phase shift of  $\pi$  in the modulator. In simpler terms, it's the voltage necessary to switch the modulator's state from 'on' to 'off' as shown in Fig 2.8 from 0 to  $\pi$ . The L in this figure of merit denotes the length of the modulator over which this voltage is applied. A smaller  $V_{\pi}L$  value indicates a more efficient modulator over a compact length. This is especially important in high-speed communication systems and dense photonic integration, e.g. trough transfer-printing.

The Extinction Ratio (ER), defined as the ratio of the power levels between the 'on' and 'off' states of a modulator, quantifies the capability of a modulator to suppress the light in its off state. A higher extinction ratio indicates that a modulator can effectively produce a clearer distinction between the modulated light states, making it essential for achieving lower bit error rates in high-speed optical communication systems. The ER is often expressed in decibels (dB).

### **Bandwidth**

Modulators intended for high-speed applications invariably emphasize bandwidth as an important metric, indicating the frequency response of the device. While ring modulators which present an inherent frequency limitation owing to their photon-lifetime-limited bandwidth, most lumped-element circuit modulators are also limited by their RC time constant, described by equation 2.5. When the EO effect is relatively small, the travelling-wave electrode (TWE) design is widely used to enhance the modulator's performance by distributing the electrical signal along the waveguide direction, reducing RC time constant limitations, and significantly decreasing RF power reflections for improved modulation performance. However, TWE MZMs tend to be large and lumped element MZMs are preferred for their small footprint.

### 2.2.3 Characterization techniques

### $V_{\pi}L$ and Extinction Ratio

In our experiments, we measured  $V_{\pi}L$  and ER at DC i.e. without applying an RF voltage to the modulator. As illustrated in Fig. 2.10, a (tunable) laser emitting a single wavelength followed by a polarization controller, an PDFA and VOA to direct light towards the device under test. The device is connected to and driven by a DC sourcemeter that supplies varying reverse bias to the modulator. Subsequently, the modulated optical output is fed to an optical power meter (or a photodetector) to monitor change in optical power levels. By plotting the optical transmission against the applied voltage, the values for  $V_{\pi}L$  and ER can be easily obtained.



Figure 2.10: Experimental setup for modulator DC characterization

#### **Bandwidth**

The setup for bandwidth measurement is depicted in Fig. 2.11. A Vector Network Analyzer (VNA) is employed for both driving the modulator under test and acquiring signals from a high-speed photodetector. The S21 measurement from the VNA includes the electrical-

to-optical (EO) transformation in the modulator, followed by the optical-to-electrical (OE) conversion in the PD. After data collection, any losses from RF components used in the setup as well as the frequency response of the commercial high-speed PD are calibrated out.



Vector Network Analyzer (VNA)

Figure 2.11: Experimental setup for modulator bandwidth characterization

The calibrated S21 reflects the EOE frequency response of the modulator. As shown by equation 2.10, the RF power is a function of the square of the RF-modulated photocurrent, whereas the photocurrent is directly proportional to the optical power. Thus the EOE response is twice that of the EO response when represented on a logarithmic scale.

$$P_{ele} = \frac{1}{2} I_{ph}^2 \times 50 = \frac{1}{2} (R \times P_{opt})^2 \times 50\Omega$$
 (2.10)

where  $P_{ele}$  is the RF power,  $I_{ph}$  is photocurrent, R represents the responsivity of photodetector,  $P_{opt}$  stands for the optical power into photodetector.

# Chapter 3

# High-speed waveguide photodiodes grown on silicon by heteroepitaxy

# 3.1 Device design

High-speed waveguide photodiodes are key components in silicon integrated photonics circuits. While Ge on Si waveguide photodiodes offer certain advantages for monolithic integration, III-V photodiodes present the prospect of superior speed, exceptionally low dark current, increased power handling capability, and operability over extended wavelengths in the L-band. This superior performance is attributed to the capability to grow complex, lattice-matched heterostructures with high crystal quality and direct bandgap, and the full availability of bandgap engineering. Within the scope of this project, we have successfully developed a MUTC waveguide photodiode grown directly on Si for the very first time.

A top-illuminated MUTC PD grown on silicon with 9-GHz bandwidth was demonstrated previously [46] by our group. In this structure, Ge and GaAs serve as the buffer layers and successfully help overcome the lattice mismatch between InP and silicon. However, as the overarching goal of silicon-based optical devices is seamless integration into silicon photonic integrated circuits, top-illuminated PDs fall as ideal candidates. In addition, top-illuminated PDs suffer from limited bandwidth-efficiency products due to the trade-off between high absorption and short carrier transit times. Therefore, and to facilitate future integration and optimize the bandwidth-efficiency product of our device, a waveguide structure is preferred. To date, only a few WG PDs based on III–V heteroepitaxy on Si have been reported. In ref. [47], a butt-coupled InGaAs WG PD grown on Si was reported; the bandwidth was 9 GHz. Side-coupled and WG-fed avalanche PDs based on III–V quantum dot material grown on Si have also been demonstrated in refs. [48] and [49]. Low dark current and a bandwidth of 15 GHz at unity gain point were demonstrated.

The designed epi-structure of our PD is shown in Fig. 3.1. To achieve high-speed and high-power performance, the MUTC structure was adopted. Describing the PD structure from the top down, it begins with a 50 nm highly doped InGaAs P-contact layer. This is followed by a 60 nm graded bandgap InAlGaAs grading layer, a 300 nm InAlAs electron-blocking layer, another 60 nm grading layer, a 150 nm undepleted alongside a 100 nm depleted hybrid InGaAs absorber, and a 15 nm InAlGaAs grading layer. Followed by a 450 nm InAlGaAs un-doped electron drift layer, which also serves as the optical waveguide core. A highly-doped InP layer on top of the buffer layers was used as the n-contact layer. The band diagram of the PD under -1 and -3 V bias is illustrated in Fig. 3.2. The epitaxial structure was grown on a silicon template using molecular beam epitaxy (MBE) in collaboration with our partners at UCSB. The details of the heteroepitaxy growth and the Si template can be found in [16].



Figure 3.1: Epitaxial layer structure of the WG PD



Figure 3.2: Band diagram of the PD under -1 and -3 V bias

In our study, we chose the InAlGaAs material system as the drift layer and optical waveguide for several reasons. First, InAlGaAs is lattice-matched to InP, as well as to our chosen absorber, InGaAs. Secondly, within the  $In_{0.52}(Al_xGa_{1-x})_{0.48}As$  material system, ensuring x > 0.2 guarantees a bandgap greater than 0.8 eV (corresponding to 1550 nm), thereby preventing undesired absorption. Furthermore, this composition ensures optimal optical confinement. We utilized InAlGaAs with diverse Al compositions to construct the waveguide. Specifically, the waveguide's core was designed with  $In_{0.52}(Al_{0.3}Ga_{0.7})_{0.48}As$ , exhibiting a large refractive index of 3.43. The layer thickness was carefully designed so that the WG was above its cut-off thickness of 350 nm at 1550 nm wavelength and at the same time the transit time-limited bandwidth remained high at 35 GHz. Fig. 3.3(a)displays the optical intensity distribution for the fundamental TE mode, illustrating that a significant portion of the optical power remains well confined within the waveguide, with a mode effective index of 3.253. 83% of the optical power is confined in the WG. Only 17%of the power resides in the highly doped lower cladding layer, which also serves as the ncontact layer in the active PD region. Our calculation showed that the free-carrier absorption resulting from this overlap was only 0.4 dB and thus could be neglected. Given that the absorber and the waveguide are separated by a mere 15 nm thick bandgap grading and 50 nm thick cliff layers, there's efficient coupling of light into the absorber. The simulated optical density along the propagation direction is depicted in Fig. 3.3(b). Our simulations indicate high absorption efficiency, where almost all the incoming light is absorbed within a device length of 30  $\mu$ m. Such a waveguide design enhances the responsivity performance, especially in shorter PDs.



Figure 3.3: Mode intensity and intensity of propagating light from simulation

## **3.2** Device fabrication

The fabrication procedure is outlined in Fig. 3.4. The process starts with a III-V on Si wafer provdided by UCSB and proceeds as follows:

1. The entire wafer (refer to Fig. 3.4) begins with a blanket deposition of the p-contact metal layers (Ti/Pt/Au in proportions 20nm/30nm/50nm) using an Ebeam evaporator. Following this, the wafer undergoes a hardmask SiO<sub>2</sub> deposition by Plasma-enhanced chemical vapor deposition (PECVD). Using a SiH<sub>4</sub> recipe at  $300^{\circ}$ C, the deposition rate averages around 60nm/min. The exact 350-nm thick SiO<sub>2</sub> layer is deposited to ensure its resilience during the following III-V etching process. Then a lithography step employing the AZ5214 photoresist (PR) and the MA6 mask aligner precisely delineates the p-mesa region.

2. A two-stage Inductively Coupled Plasma - Reactive Ion (ICP-RIE) etching using our Oxford tool is used next. Initially, after lithography, the photoresist (PR) AZ5214 serves as a mask for SiO<sub>2</sub> etching. The selected recipe for this step is CHF<sub>3</sub> at 20°C and RF power of 100 W, achieving a selective etch rate of 14 nm/min for SiO<sub>2</sub>. The etch rate is considerably slower for the photoresist and does not impact metal or III-V materials. After the complete etching of the unwanted hardmask, the overlying photoresist is removed by long-time O<sub>2</sub> plasma etch. A subsequent ICP-RIE etch is then done to remove the metal, P-contact, and absorber layers, with SiO<sub>2</sub> serving as the mask. The  $Cl_2$  and  $N_2$  recipe at 50°C is utilized here. With an ICP power of 200 W and RF power of 115 W, the etch rates are approximately 140 nm/min for InGaAs, 90 nm/min for InP, and 20 nm/min for SiO<sub>2</sub>. It's important to monitor the etching depth closely in this step, ensuring the absorber on the waveguide is completely removed without over-etching too much that might alter the waveguide's thickness, causing risk of waveguide cutoff. Utilizing a SiO<sub>2</sub>-on-Si dummy chip in this phase assists in measuring the SiO<sub>2</sub> hardmask thickness throughout the etching for enhanced control. The outcome of this process is showcased in step 2 of Fig. 3.4.

3. Another layer of  $SiO_2$  is then deposited, and the waveguide region is shaped using the dual-etching technique discussed in step 2. Dry etching is preferred over wet etch because it

prevents undercut issues that might result in undesirable waveguide structures and increased propagation losses.

4. Step 4 is to repeat the step 3 to define the N mesa.

5. After the three mesa etching stages, both, the highly doped contact layer and contact metal are buried within the thick  $SiO_2$  layer deposited as hardmask in previous steps. Another round of lithography is used to open the contact areas for metal connections. Following the photoresist development,  $SiO_2$  etching is performed, another ICP etching of  $SiO_2$  is then performed. After ICP etching, the photoresist as mask is removed by  $O_2$  plasma etch.

6. Post the N via opening window definition lithography, an N-contact metal stack of AuGe/Ni/Au (30 nm/20 nm/100 nm) is deposited. After metal deposition, the chip is soaked in acetone overnight and put into a mild ultrasonic bath to lift off metal on the photoresist.

7. A layer of SU8 are introduced, serving as an insulating layer between the coplanar waveguide (CPW) and the substrate. The SU8-2002 is employed in this step. The chip was coated with SU-8 by spinning at 3000 rpm for 40 seconds, followed by a two-minute prebake at 90°C. The mask alignment and UV exposure  $(7\text{mJ/cm}^2, 6 \text{ seconds})$  were executed using MJB4 aligner. After exposure, the chip underwent a 3-minute bake at 90°C and a 1-minute development. Then the SU-8 was hard-cured for 40 minutes on a 250 °C hot plate. The resulting thickness for the SU8 pad is around 5  $\mu$ m.

8. The seed layer is a metal film that facilitates conductivity across the entire chip surface for subsequent electro-plating. Prior to metal deposition, another round of lithography defines metal from insulation zones. A seed layer of Ti/Au (20nm/100nm) is then deposited through E-beam evaporator, establishing the contact for electro-plating.

8. Another lithography creates the plating mask. The chip is then probed and biased with a current of 100 to 150 mA, and submerged in a pre-warmed gold plating solution (50°C) for roughly an hour, allowing for an approximate 2 µm thick gold plating. Finally, the chip is soaked in acetone and put into and ultrasonic bath to remove the un-plated seed layer metal.



Figure 3.4: WG PD fabrication flow

Upon completing these processes, the chip was diced to expose the waveguide facet and then ready to be tested. It should be mentioned that no anti-reflection coating was desposited on the facets. Figure 3.5 displays both the schematic representation and the scanning electron microscope (SEM) image of the device.



Figure 3.5: (a) 3D schematic of device after fabrication. (b) SEM figure of real device

## **3.3** Device characterization

We began by characterizing the devices under DC conditions. The dark current-voltage (I-V) characteristics are presented in Fig. 3.6. With a reverse bias of 3 V, the photodiode exhibits a small dark current of 200 nA for an active area of 100  $\mu m^2$ . This translates to a low dark current density of 2 mA/ $cm^2$ . The dark current density measured from our PD is lower than that reported in other III-V on Si waveguide photodetectors [50]. The primary source of this dark current is likely bulk-dominated, originating from defects introduced during the heteroepitaxial growth process.

At 1550 nm, the fiber-coupled responsivity was measured. Fig. 3.7 (a) illustrates the correlation between the measured photocurrent and the input power, where the slope of this curve represents the responsivity of our device. For a  $10 \times 10 \ \mu m^2$  device at a -4 V bias, the external responsivity was determined to be 0.27 A/W. The SEM of the waveguide facet is shown in Fig. 3.7 (b). It's evident from the image that the facet is notably rough, which can introduce additional scattering loss beyond the mode mismatch coupling loss and reflection loss. Based on the measured value and taking the reflection loss (1.5 dB) and the simulated fiber-chip mode mismatch loss (3.1 dB) into account, the internal responsivity is 0.78 A/W,



Figure 3.6: Dark I-V characteristics

which is pretty close to our prediction from simulation.



Figure 3.7: (a) Photocurrent vs. optical power. (b) SEM of the waveguide facet.

The high-speed performance of the photodiodes was characterized utilizing an optical heterodyne setup as discussed in Chapter 2. Fig. 3.8 illustrates that upon the reverse voltage equal or exceeding 3 V, the PD becomes fully depleted, achieving its optimal bandwidth. Notably, a device with dimensions  $10 \times 10 \ \mu m^2$  had a 3 dB bandwidth of 28 GHz. The bandwidth restricted by transit time only was calculated to be 35 GHz, while the RC band-

width approached roughly 140 GHz for this particular PD. The total 3-dB bandwidth, using Eq. 2.3, was found to be 34 GHz, aligning closely with our experimental results. Evidently, the bandwidth of the photodiode is predominantly constrained by transit time.



Figure 3.8: Frequency response of a  $10 \times 10 \ \mu m^2$  device

MUTC PDs are widely utilized in integrated microwave photonic systems due to their enhanced power handling capacity compared to traditional PIN PDs. To characterize the power handling capability of our WG PDs, saturation power was measured using the optical heterodyne setup at a fixed beat frequency of 20 GHz. The results are shown in Fig. 3.9. Under a -5 V bias, the RF power achieves -0.6 dBm at -0.5 dB compression. Although this performance is inferior compared to heterogeneous PDs with a uniform light coupling design, as highlighted in [51], our PDs exhibit nearly 3 dB higher RF output power than the microwave Ge-on-Si WG PDs presented in [52], [53]. Moreover, our results are comparable to the Ge-on-Si PD array with four PDs and traveling-wave design, as cited in Ref. [54]. These observations underscore the power handling prowess of PDs derived from heteroepitaxial III–V semiconductor materials.



Figure 3.9: RF power compression at 20 GHz

We also measured the non-return-zero (NRZ) eye diagrams of these photodetectors using a 40 Gbit/s pseudo-random bit sequence (PRBS) with a pattern length of  $2^{31} - 1$  as the signal source. Given that the peak-to-peak voltage ( $V_{pp}$ ) of the PRBS source is only 500mV, we utilized an 40 GHz RF amplifier to amplify the signal to 3.5  $V_{pp}$ , matching the  $V_{\pi}$  of the EOspace lithium niobate modulator to properly modulate the signal with highest efficiency. Additionally, the modulator was biased at its quadrature point through a DC source. The modulated light was amplified by an EDFA and then attenuated to several dBm to achieve our desired photocurrent, set at 0.5 mA for this measurement. An optical filter was used to suppress the optical noise. The extinction ratio of the optical signal was measured separately with a 50 GHz photodiode and was 10 dB. Our waveguide PD detected this optical signal, and the electrical signal was captured by a sampling oscilloscope that is synchronized with the signal source using a precision timebase module to improve the jitter performance. The measurement setup is shown in Fig. 3.10.



Figure 3.10: Eye diagram measurement setup

Eye diagrams at varying bias voltages can be observed in Fig. 3.11. The eye diagrams are widely open, with an eye height of 13 mV at -3V bias and 17 mV at -4V and -5V bias, underlining the high-speed data detection capability of our waveguide PDs.



Figure 3.11: 40 Gbit/s electrical eye diagram measured before the amplifier (top left panel), and detected eye diagrams at 0.5 mA photocurrent under different voltages

# 3.4 Conclusion

This is the first III-V MUTC waveguide PD on Si with 0.78 A/W internal responsivity and high bandwidth of 28 GHz, the highest bandwidth among all III-V waveguide photodiodes grown on Si at the time.

Our PDs deliver almost 3 dB higher RF output power than the microwave Ge-on-Si WG PDs reported in Ref. [55]. Moreover, our results are comparable to the Ge-on-Si PD array with four PDs and traveling-wave design in Ref. [56]. The results show that heteroepitaxy of complex III-V heterostructures on Si is a viable path for PDs suitable for 40 Gbit/s. This work was published in Optics Letters and at CLEO.

# Chapter 4

# Heterogeneous photodetector integrated with microresonator on SiN using adhesive bonding

We have previously shown that 100 GHz microresonator solitons detected by high-speed high-power MUTC photodiodes [57] can serve as chip-based generators of stable mmWave signals. Such signals hold significant potential for high-bandwidth communications, highresolution radar, and spectroscopy applications. This pioneering work utilized discrete, chipscale components interconnected by fiber. However, the full potential of this technology will be realized when microresonator solitons are seamlessly integrated with high-speed photodiodes, and eventually, with lasers and optical amplifiers through the process of heterogeneous integration. Such a fully integrated mmWave platform promises high-power, high-coherence performance and the feasibility for large-scale deployment via mass production. Based on our recent success with high-speed heterogeneous III-V PDs on SiN waveguides [58], the proposed work aims to co-integrate a high-speed photodiode with a microresonator on the same chip for the first time.

# 4.1 Motivation

Driven by the invention of mode-locked lasers, optical frequency combs have become one of the most dynamic research areas in photonics. These combs, which consist of a series of precisely spaced, sharp spectral lines that offer a wide spectrum of frequency markers, making them invaluable in optical metrology and precision measurements. Optical frequency combs have diverse applications, from precision spectroscopy and atomic clocks to attosecond pulse generation and molecular fingerprinting. While mode-locked lasers such as Ti:sapphire and Er: fiber lasers have traditionally been the primary sources of optical frequency combs, the last few years have witnessed an improvement from bulk instrument to on-chip solutions. Advancements in high-quality factor microresonators, which offer compact, chip-scale integration and high repetition rate has drawn a lot of research interests [59]. When a continuous wave (CW) laser light is injected into a microresonator, it interacts with the nonlinear Kerr effect and the resonator's dispersion. If conditions are right, additional optical frequencies can organize themselves into a regular, equidistant comb-like spectrum called a "Kerr frequency comb." Within this comb, and above a threshold, the comb can collapse into a single, stable and circulating short optical pulse called a soliton.

The soliton microcombs have attracted increasing research efforts in recent years, with their prospective applications in optical frequency synthesis, optical clocks, metrology, and mmWave generation. Given their compact dimension, the soliton repetition rates span from a few GHz to the THz range [60]. Employing a high-speed photodiode for the direct detection of these comb lines can yield mmWaves with superior power and coherence at the soliton's repetition frequency.

Based on our previous research [57], we have successfully detected solitons generated from  $Si_3N_4$  microresonators using a discrete, back-illuminated high-speed photodiode. This yielded a mmWave power boost of 5.8 dB compared to the traditional heterodyne detection. In my work, I present a high-speed MUTC photodiode seamlessly integrated with a microresonator on a  $Si_3N_4$  platform by adhesive wafer die bonding.

# 4.2 High-speed balanced photodetectors on $Si_3N_4$

#### 4.2.1 Introduction

A heterogeneously integrated high-speed photodetector on a low-loss  $Si_3N_4$  platform is a critical component for the microring integration project. Beyond the integration with microresonators, such high-speed photodetectors can play a crucial role in various applications including telecommunications, quantum photonics, and microwave photonics. The balanced photodetector has garnered significant attention, establishing itself as a crucial element in advanced photonic systems due to its exceptional noise suppression capabilities. Balanced photodetectors are a pair of anti-paralleled photodetectors working primarily in differential mode, but they can also effectively suppress the common-mode noise introduced in the optical link, such as the laser relative intensity noise (RIN) and the amplified spontaneous emission (ASE) noise from optical amplifiers. As a result, the BPDs enhance the signal-to-noise ratio (SNR) and overall detection sensitivity.

Heterogeneous waveguide balanced photodetectors have attracted research interest due to their potential for integration with other photonic components, that promises the development of compact, efficient PIC systems. Fig. 4.1 depicts the schematic presentation of the heterogeneous balanced photodetectors on waveguides. Here, two separate waveguides serve as the optical inputs for the PD pairs, and the mesa structures of the two PDs are identical. The Coplanar Waveguide (CPW) of the BPD pair adopts traditional ground-signal-ground (GSG) RF pads design. The unique configuration of BPD electrode design is that the p contact of one PD and the n contact of the other PD are connected through metal and share the signal pad, while the alternate electrodes of both PDs are connected to the two ground pads, which in turn are connected to RF ground. This arrangement ensures that the two PDs operate in antiparallel fashion in the RF circuit.



Figure 4.1: Schematic of waveguide balanced PDs

In this section, I demonstrate heterogeneous balanced photodetectors on  $Si_3N_4$  platform with a record-high bandwidth of 30 GHz and 26 dB common mode rejection ratio (CMRR).

#### 4.2.2 Experimental Results

The epitaxial layer structure and cross-sectional view of our balanced PDs are depicted in Fig. 4.2 (a). The waveguide is composed of a Si<sub>3</sub>N<sub>4</sub> core that is 400 nm thick, 2  $\mu$ m wide, and is top-cladded with a 100-nm thick silica layer. This waveguide has been carefully designed to optimize coupling efficiency. In contrast to our previous work [24], here we adopted a modified uni-traveling carrier PD structure that results in n-contact-down structure after bonding. This design is preferred over p-down design since high n-type doping levels (> 10<sup>19</sup>cm<sup>-3</sup>) can be reached in the transparent InP contact layer which ensures low sheet resistance [61]. The PD fabrication begins with bonding of the III-V die to the pre-fabricated Si<sub>3</sub>N<sub>4</sub> wafer using SU-8 as the adhesive bonding agent [24]. Following this, the thick InP substrate is then removed by selective wet etching. The double-mesa PDs are formed by a combination of dry and and wet etching processes. Radio frequency (RF) probing pads are

subsequently deposited and linked to the contact metals through electro-plated air-bridges. As previously mentioned, the anode of one PD and the cathode of the other are interconnected, as illustrated in the simplified cross-sectional view in Fig. 4.2 (a). Concluding the fabrication procedure, Fig. 4.2 (b) shows a completed balanced photodetector, with its two  $Si_3N_4$  input waveguides.



Figure 4.2: (a)Epilayer structure and cross section of device (b)Top-view of fabricated PDs under microscope

The fabricated devices were characterized under DC conditions first. Fig. 4.3 depicts the IV measurement results for the PD pair. The dark currents for both PDs is symmetrical, of below 100 nA under a 3 V reverse bias.

For a device with a length of 40  $\mu$ m, the external responsivity was measured to be 0.63 A/W under -3 V bias. The relationship between photocurrent and input optical power can be visualized in Fig. 4.4, where the slope represents the external responsivity of 0.63 A/W. Given the mode mismatch between the fiber and the Si<sub>3</sub>N<sub>4</sub> waveguide, the internal responsivity reaches as high as 0.8 A/W. For a more compact 20  $\mu$ m-long device, the internal responsivity is around 0.72 A/W. Measurements also revealed a polarization dependence loss

of approximately 1 dB. The responsivity is slightly lower than previous work [24] since here an n-down structure is adopted and the absorption layer is positioned farther away from the waveguide.



Figure 4.3: Dark currents of balanced PDs



Figure 4.4: Photocurrent vs. input optical power

The high-speed performance of the balanced PD pairs of 10  $\mu$ m x 20 $\mu$ m each was characterized, focusing primarily on bandwidth and common mode rejection ratio (CMRR). Fig. 4.5 shows the high-speed measurement setup. Utilizing the heterodyne dual-laser approach as previously discussed, the bandwidth of BPDs was characterized. Distinct from the single PD measurement, the optical beat signal after attenuator was split into two routes. One optical branch undergoes an optical delay line, introducing a  $\pi$  RF phase difference between the two routes, ensuring that the BPDs can be operated in differential mode for each frequency point. The electrical signal from the devices under test (DUT) was extracted through a customized RF probe, that has integrated capacitors along both ground paths, serving as DC blocks. Consequently, while the two PDs are in antiparallel configuration in RF circuit, they are electrically isolated in DC circuit thus can be applied bias seperately.



Figure 4.5: Experimental setups for bandwidth and CMRR measurements (ECL: external cavity laser, PC: polarization control, PSG: RF signal generator, MZM: Mach-Zehnder modulator, EDFA: erbium doped fiber amplifier, Attn: optical attenuator, DUT: device under test, ESA: electrical spectrum analyzer)

Utilizing this setup, the BPDs' bandwidth under -3 V bias was measured to be 30 GHz, as demonstrated in Fig. 4.6. With this epitaxial design, the transit-time bandwidth was computed to be 167 GHz. The calculation is based on various parameters, including carrier drift and diffusion velocity, electric field profile, and doping concentration using similar model in Ref. [62]. Notably, since the two PDs are antiparallel in the circuit, there's twice the capacitance compared to a single PD. This suggests that BPD bandwidth performance is mainly RC limited.



Figure 4.6: Measured frequency responses of 10  $\mu$ m  $\times$  20  $\mu$ m single PD

To further investigate the circuit model of the BPDs, the S11 parameter was measured using a VNA and fitted to an equivalent circuit using commercial software ADS (advanced design circuit), as shown in Fig. 4.7 (a). By applying a particular circuit model to fit the S11, we were able to extract the BPDs' equivalent circuit, as depicted in Fig. 4.7 (b). The total junction capacitance (from both PDs) is approximately 94 fF, aligning closely with our prediction of around 50 fF for a single PD based on epilayer and device dimension design. The total resistance was 7 Ohms, and the CPW inductance is about 74 pH. The parasitic capacitance (C11 in Fig. 4.7(b)) and substrate resistance (R8) are incorporated into the circuit for precise fitting, but they do not significantly impact the bandwidth result. Utilizing this circuit model and the calculated transit-time bandwidth, I simulated again our device's frequency response using software ADS, depicted as the black trace in Fig. 4.6. The measurement results show great agreement with the simulated bandwidth, which indicates the high frequency performance is RC limited and can be improved by smaller device design.



Figure 4.7: (a) Measured and fitted S11 of BPDs (b) Equivalent circuit of BPDs

The Common-Mode Rejection Ratio (CMRR) is another crucial parameter for balanced PDs. For balanced photodetectors, the CMRR is defined as the ratio between the output RF power of the photodetectors when they operate in differential mode to when they operate in common mode. Ideally, in the case of a perfectly symmetrical PD pair operating in common mode, the signals should cancel out. It quantifies the ability of the devices to reject common-mode signals, i.e., signals that appear simultaneously and with the same phase on both inputs. CMRR is defined as:

$$CMRR = \frac{Differential Power}{Common-Mode Power}$$

CMRR is typically expressed in decibels (dB), and a larger CMRR indicates a more symmetric PD pair. Our measurement approach, as depicted in Fig. 4.5, utilizes a single laser source. The emitted laser light is fed into a high-speed modulator, which is connected to and driven by the signal source. The modulated light follows the same path as in the bandwidth measurement. The electrical signals from our devices in both differential and common mode measurements are directed to an ESA for data recording. The difference in power between these modes provides the CMRR. The measurement was done under -3 V bias and 0.5 mA photocurent. Our results indicated a CMRR of 39 dB at 20 GHz, which reduces to 26 dB at 30 GHz, as represented in Fig. 4.8.



Figure 4.8: Common and differential mode powers at (a) 20 GHz (b) 30 GHz

# 4.3 High-speed MUTC photodetector integrated with microresonator on $Si_3N_4$ platform

In this project, we propose a high-speed photodetector and microring resonators seamlessly integrated on the  $Si_3N_4$  platform for mmWave generation for the first time. This work is in collaboration with Prof. Yi's group, who provided the design for the microresonators. The chip schematic is presented in Fig. 4.9. The generation of microcavity solitons is achieved by pumping the high-Q microresonator with a CW laser. From the microresonator drop port, a waveguide leads to our on-chip high-speed photodetector which will directly detect the solitons and produce mmWave at the repetition frequency of the soliton. Compared to traditional heterodyne detection, our approach leveraging soliton mode-locking, could provide up to 6 dB gain in power [57]. Additionally, the coherence achieved through our methodology is notably superior.



Figure 4.9: Schematic of mmWave generation platform based on microresonator and PD

#### 4.3.1 Device design

In this project, the optical design for the PD was firstly addressed, focusing primarily on the waveguide optimization. In contrast to our previous work 4.2, where waveguide PDs were the only devices on the chip and the  $Si_3N_4$  waveguides were 1- $\mu$ m or 2- $\mu$ m wide, 400-nm thick with a 100-nm top cladding of SiO<sub>2</sub>, designed to optimize PD performance. In this work, since we aimed for integration with a microring resonator, the Si<sub>3</sub>N<sub>4</sub> waveguide was designed to be 800 nm thick and width of 1  $\mu$ m to better enable dispersion engineering that is needed in the microresonator. The top cladding of this 800-nm waveguide is also thinned to around 100 nm for waveguide to PD coupling.

The fundamental TE mode profiles for both waveguides can be found in Fig. 4.10 (a) for 400 nm and (b), for 800 nm thick SiN waveguide. It's evident that the 800 nm thick waveguide confines the optical mode more strongly inside the  $Si_3N_4$  waveguide core, which complicates the coupling from waveguide to the overlying III-V PD material. Subsequent simulations, illustrated in Fig. 4.10 (d), illustrate the optical intensity profile along the prop-

agation direction that reveal the coupling and absorption efficiencies of these WG designs into a PD that is located on top of 100 nm-thick top cladding. For a 20  $\mu$ m long PD, the internal quantum efficiency (QE) was 0.483. In contrast, for the 400 nm thick waveguide, as shown in Fig. 4.10 (c), the internal QE reached 0.85 for the same PD length. Clearly, to have a high responsivity with the 800-nm thick waveguide, further optical design optimization is needed.



Figure 4.10: (a) Fundamental mode of 400 nm waveguide. (b) Fundamental mode of 800 nm thick waveguide. (c) Propogation intensity profile of 400 nm thick waveguide and 20  $\mu$ m long PD. (d) Propogation intensity profile of 800 nm thick waveguide and 20  $\mu$ m long PD.

In pursuit of a higher responsivity from the 800 nm thick waveguide, I engineered a passive waveguide taper structure to improve coupling and absorption efficiency. This approach leverages evanescent coupling from the  $Si_3N_4$  waveguide to the III-V bulk of the PD. Incorporating a narrow tip in the tapered waveguide can facilitate the transfer of the optical mode from the waveguide to the absorber, thus enhancing both coupling and absorption efficiencies. The taper was designed as 1  $\mu$ m in width, tapering to 200 nm at the end, limited by the constraints of the foundry's manufacturing capabilities, and 50  $\mu$ m in length to mitigate reflection loss and scattering loss, which can be induced by a abrupt change of the waveguide's effective index. A comparison of straight and tapered waveguides, both with 800-nm thickness, is depicted in Fig. 4.11.



Figure 4.11: (a)A 3D model of the device simulated. (b) The mode profile along straight 800 nm waveguide. (c) The mode profile along the  $1\mu$ m-to-200nm tapered 800 nm waveguide. (d) The field intensity profile along the straight  $1-\mu$ m wide 800-nm thick waveguide. (e) The field intensity profile along the tapered 800 nm waveguide

Through the implementation of the taper design, the optical coupling efficiency is greatly improved that a rather short device can absorb most of the light with negligible radiation loss. To optimize the waveguide design, the quantum efficiency of PDs of varying lengths and positions was simulated. The simulated QE is illustrated in Fig. 4.12. Due to the stringent requirement for high bandwidth in this project, only devices with small dimensions were simulated. From the unsaturated QE, an even higher efficiency can be expected for longer devices. The optimized position for the device to start is 5  $\mu$ m away from the taper beginning. In comparison to the straight wide waveguide with a 20  $\mu$ m long III-V device which has an internal QE of 48%, the tapered waveguide design can achieve an internal QE of 79%.



Figure 4.12: (a) Schematic of tapered waveguide and PD. (b) Simulated quantum efficiency

Besides the optical design, I also optimized the electrical design of the CPW probe pads for optimal high-speed performance in our photodetectors targeting operations up to 100 GHz. By implementing an inductive peaking strategy [63], the power performance at high frequency can be significantly improved. Utilizing the circuit simulation software ADS, and through sweeping the width, length, and gap distance of the CPW, an optimized design emerged, as seen in Fig.4.13 (c). Fig.4.13 illustrates the comparison of RF power between the diode-only configuration, the conventional CPW for Ground-Signal-Ground (GSG) probe, and the inductive peaking design CPW. Using this strategy, I was able to enhance the bandwidth from 80 GHz to 93 GHz in the simulation.



Figure 4.13: (a) Various CPW design in the circuit. (b) Simulated frequency responses (c) CPW design for 100 GHz (d) Fabricated CPW under microscope

After the design phase was concluded, the final layout is depicted in Fig. 4.14 (a). The 10 mm x 5 mm chip is divided into two sections: the resonator part and the PD part. The resonators occupy the left half of the chip and feature a thick top cladding SiO<sub>2</sub> of 3.3  $\mu$ m. A bonding window, highlighted as the blue box in the figure, is situated on the right side of the chip. Within this window, the top cladding has been thinned to about 100 nm for efficient

waveguide-to-PD coupling. All PDs are strategically positioned within this bonding window. Each effective output port from the resonator is paired with one monitor photodetector (PD) to assist in monitoring optical power, as well as a high-speed PD designated for millimeterwave generation. Additionally, several standalone PDs are situated at the bottom of the chip, enabling the characterization of PD performance independently, without any resonator in front. The chip after fabrication is presented in Figure 4.14 (b).



Figure 4.14: (a) Final layout design of the microresonator and PD integration chip (b) Chip after fabrication

#### 4.3.2 Device Fabrication

This section provides an overview of the fabrication process for III-V on  $Si_3N_4$  PDs through adhesive bonding and subsequent steps, utilizing the  $Si_3N_4$  chip fabricated by Ligentec. Corp. The silicon nitride chip features a custom-designed bonding window of 5 mm × 4 mm dimension.

i. Bonding: Prior to fabrication on our side, the substrate of the III-V wafer was thinned to around 250  $\mu$ m to avoid severe undercut during substrate removal. The thin III-V wafer was cleaved into a small die to fit into the bonding window with about 0.5 mm margin on each side. Both, the Si<sub>3</sub>N<sub>4</sub> chip and the III-V die surfaces were carefully cleaned pre-bonding. The

cleaning process encompasses several steps: First, drip Trichloroethylene (TCE), acetone, and methanol onto the chip while it's on a spinning plate. Next, wipe the chip using ethylene glycol, and finally, rinse it with IPA and water before blow-drying it with an air gun. SU-8 6000.5 was used as the adhesive bonding layer, expecting a thickness of about 90 nm at a 9000 rpm/min spin rate. The SU-8 was then UV-exposed for 16 s (350-nm wavelength, 7 mW/cm<sup>2</sup> power density). Following manual alignment to the bonding window, the III-V die was placed on and bonded to SiN substrate using a SUSS wafer bonder XB8, undergoing one-hour outgassing and a two-hour bonding process under 500 N pressure and 140°C.

ii. In P Substrate Removal: After bonding, a fast lithography was performed to cover the edge of III-V die with thick photoresist (AZ 4620) to avoid lateral etching. Then employing a fast selective wet etch (HCl : H<sub>2</sub>O 3:1, 40 – 45°C), the 250- $\mu$ m InP substrate was removed in 10 – 15 minutes until reaching the InGaAs etch stop layer of InGaAs.

iii. P Metal Lithography: A lithography was performed, followed by the deposition and lift-off of a Ti/Pt/Au/Pd (20nm/20nm/50nm/80nm) metal stack, serving as the p-contact and hardmask for subsequent dry etch.

iv. Forming the P Mesa: Utilizing the Pd as the hardmask, the p mesa was formed using ICP RIE etching with a Cl<sub>2</sub> 50C degree recipe. It's imperative to note that, prior to any etching, all waveguide areas were safeguarded by a 7- $\mu$ m thick photoresist (AZ 4620) to shield them from RIE etching.

v. N Mesa formation: The N mesa was formed using a selective wet etch (HCl: $H_3PO_4$  1:9). Given the n mesa's large size and the solution's safety to Si/SiO<sub>2</sub>, a standard lithography and etching process suffice in this step.

vi. CPW Formation: Lastly, the CPW were shaped for high-frequency operation. A Ti/Au (20 nm/80 nm) seed layer was utilized, followed by a one-hour electrode-plating process, resulting in a 2- $\mu$ m thick gold layer.
1. Bonding and substrate removal









Chip after substrate removal under microscope



3. P mesa dry etch







Device after p mesa etch

4. N mesa wet etch & N metal deposition







Mask design for n mesa (brown) and n metal (red) Dev

Device after n mesa etch & n metal deposition

#### 5. Seed layer and plating



Figure 4.15: Fabrication process flow of heterogeneously bonding PD

#### 4.3.3 Device characterization

Prior to evaluating the combined performance of microresonators and PDs, it was worthwhile to first assess the standalone performance of the PD.

#### DC characterization

For this purpose, a stand-alone PD with dimensions of  $10 \,\mu\text{m} \times 20 \,\mu\text{m}$  from the same chip was investigated. Initially, the device was characterized under DC conditions. The dark current is depicted in Fig. 4.16(a), that at a reverse bias of 3 V, the dark current registers approximately 150 nA, which is typical for our heterogeneously integrated PDs. Additionally, the capacitance-voltage (CV) relationship is illustrated in Fig. 4.16(b). The junction capacitance experiences an initial decrease, then stabilizes at 55 fF beyond a bias of 2 V. The calculated capacitance based on depletion width and material permittivity is 49 fF. The good alignment between measured and calculated capacitance indicating that the junction has been fully depleted after 2V.

The responsivity of this device was also evaluated. An external responsivity of 0.22

A/W was measured. Through a fiber-waveguide-fiber measurement utilizing the stand-alone waveguide on the chip, a total loss of 6.5 dB was recorded for both facets combined. Taking into account the coupling loss of 3.25 dB for a single facet, the internal responsivity equates to 0.46 A/W.



Figure 4.16: (a) IV curve of the PD without light. (b) CV curve of the PD

#### **RF** characterization

The frequency response of the  $10 \,\mu\text{m} \times 20 \,\mu\text{m}$  stand-alone PD was assessed using a heterodyne setup. The 3-dB bandwidth across varying bias voltages is presented in Fig. 4.17. The results indicate that post a 2 V reverse bias, the bandwidth remains largely constant at 53 GHz. This closely aligns with our predictions based on CV measurements. An RC bandwidth calculated using the observed capacitance of 55 fF and a total resistance of 55  $\Omega$  (50- $\Omega$  external load and 5- $\Omega$  series resistance) stands at 52.6 GHz, proving our hypothesis that the device's bandwidth is limited by resistance-capacitance (RC) constant.



Figure 4.17: Frequency responses under various reverse voltages

The RF power saturation was then measured at 50 GHz under diverse bias. At lower photocurrent levels, the RF power output appears to be constrained by the junction capacitance. However, as power and photocurrent rise, due to the space charge effect, the higher density of photo-generated carriers in the junction reduces the electric field and thereby impacting power performance. The RF power measured at 50 GHz and the corresponding RF power compression measurement results are shown in Fig. 4.18. As the reverse voltage increases, the RF power's compression point rises accordingly. Specifically, at a 4 V reverse bias, the RF power at 50 GHz peaks at -8.9 dBm with a corresponding photocurrent of 5.6 mA. It should be mentioned that this device ultimately failed at 4.5 V and 5.1 mA.



Figure 4.18: Saturation power measurement at 50 GHz

#### 4.3.4 Summary

In the work, high-speed photodetectors integrated with microresonator on the SiN platform were demonstrated. The resulting single PD exhibited a responsivity of 0.45 A/W, a 53-GHz 3dB bandwidth, and an RF power of -8.9 dBm at 50 GHz. The balanced PDs achieved a record-high 3-dB bandwidth of 30 GHz and a CMRR of 26 dB at that frequency. In addition, the photodetector's fabrication had a negligible impact on the microresonator's performance, suggesting its suitability for integration into high-speed applications on the SiN platform.

## Chapter 5

# Micro-transfer printable high-speed O-band MQW Mach-Zehnder modulator

In this chapter, a high-speed O-band multi-quantumwell (MQW) Mach-Zehnder modulator (MZM) is introduced. Furthermore, we demonstrate that the devices are micro-transfer printable to a SiN platform. Section 5.1 introduces the working principles and essential design rules. Section 5.2 provides insights into the innovative fabrication processes. The characterization techniques and measurements are detailed in Section 5.3. Lastly, Section 5.4 discusses benefits of our devices and potential future work.

#### 5.1 Introduction and device design

The last several decades have witnessed the surging demand for data-intensive applications and enhanced global connectivity, which place unprecedented stress on the communication frameworks. As a result, optical communication systems, which leverage the speed and bandwidth advantages of light, have been widely adopted [64], [65]. High-speed, electrooptic modulators, as a critical component in the realm of photonics, play a pivotal role across diverse applications from optical telecommunication and microwave photonics [66] to optical computing and quantum photonics. The C-band range (1530mnm - 1570 nm) has been widely employed for long-haul communications, attributed to its minimal fiber loss, thus numerous high speed modulators have been studied from monolithic to hybrid designs[67]–[70]. Conversely, for short-range connections, the O-band (1260 nm-1360 nm) is favored due to its near-zero dispersion advantages[71], [72]. For microwave photonics applications that require high optical power, O-band InAs/GaAs quantum dot lasers and semiconductor optical amplifiers (SOAs) are readily available which offer several advantages [73]. The lower losses achievable in GaAs based waveguides compared to InP due to reduced intra-valence band absorption and the smaller confinement factors of InAs quantum dot active regions compared to quantum wells  $(10^3 - 10^4)$  both lend themselves to high power designs [74]. With regard to O-band modulators designed for datacenter or microwaves photonics applications, there's growing emphasis on high speed, compact size, dependable stability and capability to handle high optical power. The motivation of our work centered around designing a compact modulator for 1310 nm wavelength, that is not only capable of handling high power levels but is also transfer-printable, ensuring it integrates seamlessly into Silicon Nitride (SiN) PICs for application in microwave photonics systems.

There are several phenomena that can be used to realize effective electro-optic modulation, including carrier plasma dispersion [75], the Pockels effect [76] and Quantum Confined Stark Effect (QCSE) [77]. The choice of modulation technique and material often hinges on the specific demands of the application. For instance, while Lithium Niobate (LN) modulators stand out in high-speed operations and their low insertion loss, they are limited by their relatively large footprint, a side effect of their reliance on the relatively weak linear electro-optic effect [78]. Silicon microring modulators present an alternative- compact and efficient but they demand precise wavelength and/or temperature control and often falter under high optical power [79]. In this context, III-V materials with their high modulation efficiency thanks to the EO-effect induced by QCSE, and thus shorter length, and outstanding power handling capability, become compelling candidate for O-band modulators and part of photonics integrated circuits (PIC) [80]. While both the electro-absorption modulator (EAM) and MZM utilize the QCSE principle, MZMs boast a broader optical bandwidth and demonstrate greater temperature resilience than EAMs since they operate in the transparency regime. To date, the reported high speed O-band modulators are summarized in Table 5.1.

Reference	Material	Type	Bandwidth	$V_{\pi} \cdot L$	Extinction
			$(\mathrm{GHz})$	$(V \cdot mm)$	ratio (dB)
[81]	InP	EAM	76	NA	NA
[82]	InP	EAM	67	0.24	11
[83]	InP	TW-MZM	58	7	>20
[84]	Si	TW-MZM	30	24.3	3.4
[85]	Si	MZM	18	11.5	5
[78]	LN	TW-MZM	>67	27	30
This work	InP	MZM	>67	3	17

Table 5.1: Comparison of various O-band optical modulator performance metrics (NA: not available, TW: traveling wave, MRM: microring modulator)

III-V material-based MZMs, particularly those using multiple quantum well structures, have been the focus of the extensive research for years. These MQW MZMs utilize the QCSE [86]. When a reverse bias is applied to the active region of the modulator, the resulting electric field will cause a tilt in the quantum well energy band. The tilting of the band diagram effectively diminishes the energy difference between the electron and hole ground states. This results in the broadening and redshift (shifting to longer wavelengths) of the exciton absorption edge on spectrum. The QCSE introduces a concurrent change in the refractive index, as dictated by the Kramers-Kronig relation. This refractive index variation within the Mach-Zehnder structure facilitates the interferometric modulation through phase changes. Among all modulation techniques in semiconductor modulators, QCSE stands out because it can induce a significant shift in the exciton absorption edge when an electric field is applied. For our study, we opted for In<sub>0.53</sub>Al<sub>0.17</sub>Ga<sub>0.3</sub>As/In<sub>0.53</sub>Al<sub>0.35</sub>Ga<sub>0.12</sub>As QWs, attributed to their large conduction band offset which enhances QCSE, resulting in a higher modulation efficiency [87]. Figure 5.1 illustrates the design of the quantum well, along with the simulated results regarding absorption efficiency based on this design (This simulation was done by J. Khurgin at Johns Hopkins). We strategically positioned the absorption edge at 1210 nm, ensuring it's 100 nm away from the operating wavelength. This ensures minimal absorption at 1310 nm but still induces the desired refractive index change.



#### Wavelength (nm)

Figure 5.1: Simulated absorption curve (J. Khurgin) and schematic of QW

The modulator epitaxial layer structure is shown in Fig. 5.2 and was grown on InP substrate by metal-organic chemical vapour deposition. For low junction capacitance and high optical mode confinement, we chose 54 pairs of  $In_{0.53}Al_{0.17}Ga_{0.3}As/In_{0.53}Al_{0.35}Ga_{0.12}As$ 

quantum wells (total thickness 700 nm). The Al concentration and width of the QW barrier were carefully designed for exciton peak at around 1210 nm. The unintentionally doped (u.i.d.) QWs are sandwiched between n- and p-type InP layers which also serve as optical cladding layers. These relatively thick claddings are designed to prevent optical loss from free carrier absorption in the highly doped p- and n-type contact layers and in the top metal electrode which we deposited on the 50 nm-thick InGaAs contact layer. Beneath the active layers that make up our modulator, we added additional layers to enable chiplet release and micro-transfer printing . The target SiN chip has 'pockets' on it, which are etched windows where the III-V device 'coupon' will fit and butt-couples to its waveguides. To align the height of the III-V waveguide with the SiN waveguide, we added a 2309 nm spacer layer to elevate the whole MZM structure, as depicted in Fig. 5.2. Below this spacer, there are 510 nm-thick release layers. These release layers are designed specifically for the transfer printing process. During this process, the device is immersed in FeCl2 solution that etches away the release layer by lateral etching and allows the device to separate from the InP substrate, making it ready to be transferred to the target chip.



Figure 5.2: Epilayer of MQW modulator

The optical waveguides are formed by the MQW layers (core) and top and bottom cladding layers of InP. The design of the initial waveguide width was set at 4  $\mu$ m, motivated by two main concerns. Firstly, considering fabrication: the via open window, being designed smaller than the top mesa, necessitated a size not less than 2  $\mu$ m due to the limitations of our cleanroom lithography capabilities at the time. Secondly, addressing contact issues: a larger contact area was pursued to reduce contact resistance effectively. However, at the meantime a single-mode waveguide is preferred for high modulation efficiency since the EO effect QCSE shows the strongest performance with fundamental mode. In addition, the splitter and combiner in the MZ structure require singlemode input waveguides. To satisfy both large mesa on top and single-mode waveguide core, an undercut process is developed. By this step, the waveguide core width is reduced from 4  $\mu m$  to 1.2  $\mu m$  to support only the fundamental mode, as illustrated in Fig. 5.3 (a) and (b), while keeping the width of the top contact unchanged. Along the waveguides, the active segments are defined by the p contact layer and electrodes while the passive-only sections contain no  $p^{++}$ -type contact layer thus the electrical field will not be applied across the MQW. Two  $1 \times 2$  multi-mode interference (MMI) couplers are employed for splitting and combining of the optical paths.



Figure 5.3: (a) Schematic cross sectional view of active region of modulators (b) Schematic of cross sectional view of passive region

#### 5.2 Development of fabrication process

In this work, we demonstrated the first high-speed modulator fabricated in the UVA cleanroom. A novel fabrication process flow was developed for this project. In this section, I'll introduce the developed fabrication steps and challenges encountered along the way and how we effectively addressed them.

#### Fabrication process overview

Our design includes two distinct types of devices. The first category are bar-level devices which remain on the InP substrate and are immediately ready for testing without undergoing micro-transfer printing. The second category, on the other hand, comprises 'chiplets' designed for micro-transfer printing, that are isolated small coupons and necessitate additional fabrication steps compared to the bar-level ones. Fabrication process of both types of devices will be discussed in this section. The comprehensive fabrication process flow can be seen in Fig. 5.4.

1. Metal and hardmask deposition: Our starting point was a 2-inch III-V wafer. Since the EO effect, and specifically the Pockel's effect, is sensitive to the crystal orientation of the material, we precisely cleaved the 2-inch wafer along the [110] and [ $\bar{1}10$ ] orientation to 10 mm ×10 mm pieces for easy handling prior to fabrication. This ensured the active waveguides were properly aligned with the correct crystal direction. Then we initiated with a blank deposition of the P contact metal stack of Ti/Pt/Au (20nm/20nm/80nm). After this, a  $SiO_2$  layer was also blank deposited, acting as the hardmask for following lithography and dry etching.

2. Waveguide dry etch: An RIE ICP etching using  $Cl_2$  was carried out to shape the waveguide, and the etching stops at the uppermost layer of the N-contact.

3. Self-aligned dry etch: The next step is defining the P- and N- mesas. We introduced

a self-aligned etch technique, that with a single lithography step multiple etching processes happen simultaneously. As illustrated in Fig.5.4, the active region on top of the waveguide and the n mesa region on the substrate were protected against etching by photoresist. In this phase, a RIE ICP InP etching was performed for a duration of 5 to 7 minutes. This process achieved an etching depth of 600 nm, uniformly applied to both the passive region p mesa and the bottom n mesa. Consequently, for the passive regions alongside the waveguides, the p cladding thickness was reduced, leaving a 400-nm lightly-doped p cladding layer atop the waveguide core. Simultaneously, the n mesa also maintained a height of 600 nm, indicating that the redundant non-functional area of the chip experienced an etching of approximately 400 nm into the spacer. This technique ensured precision in p and n layer alignments, and avoided potential issues from lithography inaccuracies. A primary concern for this step is the identical etching duration for both top p and bottom n mesas. Thus careful design and precise execution of the etching is important.

4. N contact and heater metal deposition: Post the double mesa etching, the n-contact and heater metals, consisting of Ti/Au (20nm/80nm), were deposited using Ebeam evaporator followed by lift-off.

5. Waveguide undercut: The fifth step is a unique and critical step in our process. As stated in section 5.1, to enhance modulation efficiency, single-mode waveguides are preferred, which have a width of 1.2  $\mu$ m in our case. However, the intrinsic fragility of such a narrow and long waveguide presents challenges during processing, and the dimension was nearing the constraints of our cleanroom capabilities for future via opening step since a even smaller window has to be created within this 1.2- $\mu$ m wide waveguide.

To address this, we initially shaped a broader waveguide, with widths ranging from 4 to 6  $\mu$ m, using dry etching in previous steps. This was then narrowed down to the desired 1.2  $\mu$ m width via lateral wet etching. The etchant used was a mixture of  $H_3PO_4$ :  $H_2O_2$ :  $H_2O = 1$ : 5 : 15, chosen specifically for its selective etching properties that targets InGaAs/InAlGaAs without affecting InP.

6. Protection layer: After finalizing the mesa structures, a  $SiO_2$  layer was deposited over the chip by PECVD, protecting the devices during subsequent procedures and during micro transfer printing.

7. SU-8 coating and planarization: The chip was then coated with SU8, providing a foundation for the contact metal pads. Employing SU8-2005, after lithography and hard cure, the resultant SU8 thickness is approximately 5  $\mu$ m. This was then reduced to around 2.5  $\mu$ m using  $O_2$  plasma etch.

8. Sputter  $SiO_2$  and lithography: An additional  $SiO_2$  layer was deposited onto the chip using low-temperature RF sputter tool, that served as the hardmask for the SU8 pattering. After lithography and  $SiO_2$  etching, the via open pattern is transferred to  $SiO_2$  hardmask, as shown in Fig. 5.4 step 8.

9. Open SU-8: An SF6 + O2 ICP etching was employed to remove SU8, aiming to unveil the n contact and heater metals, that were deeply buried in the SU8 layer.

10. Blanket  $SiO_2$  etching: Upon complete removal of the SU8 from the via opening zones, the p contact, n contact, and heater metals are concealed just beneath a  $SiO_2$  layer. A blank etch using CHF3 ICP etching was undertaken to remove this  $SiO_2$  layer and finally expose the contact metal.

11. Seed layer and plating: Concluding the process, metal pads were formed on the SU8 layer and connected to the devices via seed layer deposition and plating.





#### 2. WG dry etch





#### 3. Self-aligned dry etch



#### 4. N-contact and heater metal





Passive region

	SiO <sub>2</sub> P metal		SiO <sub>2</sub> P metal					
	Р		Р					
	i		i	N				
	Ν							
Spacer								
Release layer								
Substrate								

Active region

#### 5. Waveguide undercut





Active region

#### 6. Protection layer





Passive region



Active region

#### 7. SU8 coating & Planarization







## 8. Sputter SiO<sub>2</sub> and open lithography



9. Open SU-8





Passive region



Passive region

Active region



Active region



Active region



Figure 5.4: Fabrication process of MZMs: 3D model and cross sections

After completing the above steps, the bar-level modulator that will sit on the III-V substrate were finalized. The chip was then cleaved to expose the waveguide facet and were ready to be tested.

For chiplet devices for transfer printing, several additional steps were necessary as illustrated in Fig. 5.5:

12. Spacer and Release Layer Etching: Post the formation of MZMs, it was essential to create the 'coupons' or chiplets that can be isolated from the InP substrate. This 'coupon' would later be retrieved for micro-transfer printing. This stage demanded two etching steps - one for the spacer layer and another for the release layer. For the thick 2.3  $\mu$ m InP spacer layer, a hybrid etching method was adopted. Starting with a dry etching process and subsequently a selective wet etching step ensured the prevention of lateral undercut, which is a known limitation of wet etching. The release layer then underwent a wet etch using

 $H_3PO_4: H_2O_2: H_2O = 1:1:10.$ 

13. Tether: Prior to the transfer printing, another step to cover the chiplets with an additional layer of photoresist. This layer would act as an anchor and tether the coupon to the substrate post the release layer etching. For this purpose, we utilized SPR-220 photoresist.

The chiplets were then ready for the transfer printing process. This printing process was executed by our collaborators at X-celeprint. It included picking up chiplets from our 'source' wafer with a polymer stamp and printing them into pre-fabricated pockets of the 'target' SiN/Si wafer. Chiplets were attached to the target wafer using Benzocyclobutene (BCB).





Figure 5.5: Chiplet fabrication process

As previously mentioned, our design includes two types of devices that undergo fabrication simultaneously on the same chip. The layout, depicted in Fig.5.6(a), designates the upper portion of the chip for bar-level devices and the lower section for  $\mu$ TP chiplets. Fig. 5.6(b) shows the bar-level devices post-fabrication under the microscope. The fabricated chiplets on the InP substrate are illustrated in Fig. 5.6(c), and Fig. 5.6(d) showcases the devices that have been successfully transfer printed onto the SiN chip.



Figure 5.6: (a) Layout overview. (b) Fabricated bar-level devices. (c) Fabricated chiplet devices (d) Micro-transfer printed devices on SiN chip

#### Challenges and solutions

#### i. Waveguide undercut

One of the primary challenges we confronted was the formation of the narrow, long, and robust waveguide. A narrow single-mode waveguide was preferred while spanning several millimeters in length. Our approach is to form a wider waveguide by RIE dry etching and then narrow it down by lateral wet etching. After exhaustive trials and methodical adjustments, a reliable recipe was eventually identified and validated.

For this step, we settled on a selective etching solution of  $H_3PO_4: H_2O_2: H_2O = 1:5:$ 15 with a precise etching duration of 2 minutes and 30 seconds. It's crucial to emphasize that the MMIs and waveguide facets required protection during this phase. Given the MMIs' high sensitivity to width alterations, it was important to keep them untouched during the process. Additionally, waveguide facets were also covered by photoresist to prevent lateral etching at the facet (as indicated by the red cross direction in Fig. 5.7). Otherwise, such unwanted etching could introduce large coupling losses.



Figure 5.7: 3D model of waveguide etching process: (a) Before etching (arrow: potential etching directions). (b) After etching

To improve precision in the etching depth, we employed specialized monitor structures. Owing to the inherent design of the waveguides, the etching depth couldn't be directly observed from the waveguide's top or side views. The etching rate was tightly monitored with the monitor structure using SEM throughout the process, as shown in Fig. 5.8. Precise control over the etching duration was crucial; a short etching time results in a multi-mode waveguide, while an excessively long etching time leads to waveguides that are easy to break and detach. The waveguides, successfully etched and functional after cleaving, are shown in Fig. 5.9.



Figure 5.8: The structure used to monitor etching depth



Figure 5.9: Undercut waveguide facet after cleaving under (a) microscope and (b) SEM

#### ii. Contact open

The contact opening procedure also presented a significant challenge in our fabrication process, particularly since we had to expose contacts with three different heights (p contact, n contact, and heater metal) that were covered by layers of  $SiO_2$  and thick SU8. Adding to the complexity, our smallest via opening pattern was on the scale of just 1  $\mu$ m, which is unattainable through direct (thick-)SU-8 lithography. Consequently, we developed a tripleetch opening strategy, as detailed in steps 8-10 of Fig. 5.4.

Following the deposition of a protective  $SiO_2$  layer using PECVD, we coated the chip

with a thick SU8 layer, which we then thinned to approximately the height of the p top mesa. The critical step was the opening of this thick SU8 layer. To accomplish this, we sputtered another 400-nm thick  $SiO_2$  layer atop the SU8, using a low-temperature sputter tool. This was necessary to avoid potential damage to the SU8 at temperatures above 200 C. The chip then was sealed in a sandwiched layering of  $SiO_2$  protective layer, SU8, and a  $SiO_2$  hardmask. We then did lithography, followed by an RIE  $SiO_2$  etch to imprint the via open pattern on the sputtered  $SiO_2$ . Using the patterned  $SiO_2$  as a hardmask, we carried out an  $SF_6 + O_2$  RIE ICP etching process to remove the SU8. Once all the redundant SU-8 was removed, the metals were only covered by the protection layer  $SiO_2$ . At this point, we applied a blanket  $SiO_2$  etch to simultaneously etch away the exposed protective layer and all the sputtered hardmask. Given the weak adhesion of metals to the sputtered  $SiO_2$ , this blanket etching also addressed this issue.

Fig. 5.10 shows the successful result of this approach under SEM and microscope, with a clearly distinguishable 2  $\mu m$ -wide opening achieved and perfect alignment through our strategy.



Figure 5.10: (a) SEM and (b) Microscope picture of active region after P contact opening step

#### 5.3 Device characterization

A detailed view of a fabricated modulator is shown in Fig. 5.11 (a). Fig. 5.11 (b) shows the cross-sectional model of the MZM along with a simplified schematic of the driver circuit connections and DC bias for push-pull operation.



Figure 5.11: (a) Top view of the modulator (b) Cross-sectional view of the device and driving circuit

#### DC characterization

Initially, we conducted a DC characterization of the modulators. The I-V measurement for both arms of a MZM is depicted in Fig. 5.12. Under a -10 V bias, the dark current is remarkably low of only a few nA.



Figure 5.12: IV of a 400  $\mu$ m device

To explore the absorption properties of the MQW stack, we fabricated a basic doublemesa cylindrical diode for top illumination, as depicted in Fig. 5.13 (a). This diode was top-illuminated using a tunable laser and was reversed-biased at various voltages. The resulting photocurrent spectra is shown in Fig. 5.13(b). An evident exciton peak emerges at 1.12 eV (around 1100 nm) at 0 V bias. As the applied electric field increases, the absorption edge shifts towards lower energy levels and becomes broader. By the time the bias reaches 15 V, there's only small absorption at 1310 nm. Relative to the simulated absorption curve presented in Fig. 5.1, the absorption peak deviates by approximately 900 nm smaller from the target wavelength, resulting in a higher driving voltage requirement. Nonetheless, the overall trend observed in the actual measurements aligns reasonably well with our QW design simulation. It should be mentioned that the exciton peak can be shifted to smaller photon energies by re-deisgning the MQW with smaller well width in future runs.



Figure 5.13: (a) Double mesa diode for top illumination (b) Measured photocurrent curve of the top-illuminated device

To characterize the DC  $V_{\pi}$  performance, a fiber-to-waveguide-to-fiber setup was employed. The 1310-nm wavelength light from an external cavity laser (ECL) was coupled in and out of the III-V waveguide using lensed fibers. The resultant optical power was assessed using an optical power meter connected to the output fiber's end. During these measurements, the modulator was driven on a single arm, with its twin arm set at the quadrature point. The measured and normalized transmission curves, in relation to the reverse bias for two modulator lengths, is shown in Fig. 5.14. The  $V_{\pi}$  for the 100  $\mu$ m-long modulator is 30 V, translating to a voltage-length product of a only 3 V · mm. The extinction ratio (ER) is 17 dB. The 200  $\mu$ m-long device demonstrates a measured  $V_{\pi}$  of 20 V, resulting in a  $V_{\pi} \cdot L$ of 4 V · mm and an ER of 10 dB. The discrepancy between devices might be attributed to fabrication, as the active region—subjected to most fabrication processes—may introduce some loss or defects. Therefore, devices with a shorter active region often deliver enhanced performance.



Figure 5.14: Optical transmission characteristics of modulators (single-arm drive)



Figure 5.15: Optical transmission of device at various wavelengths

To evaluate the device's functionality across the entire O-band, I measured the optical transmission for various wavelengths, as shown in Fig. 5.15. The results clearly indicate that

the device operates effectively between 1260 nm and 1360 nm, maintaining an extinction ratio of at least 5 dB. As expected, the optical performance wavelength is around 1310 nm, given the strong QCSE effect and the passive structures are designed for this specific wavelength. These findings suggest that our device is a promising candidate for applications within the entire O-band.

#### **RF** characterization

The experimental setup to measure the modulator's RF characteristics is shown in Fig. 5.16. The light emitted from the laser is managed by a polarization controller and sent into the modulator's waveguide via a lensed fiber. The output light from our modulator is coupled to another lensed fiber, initially amplified using a Praseodymium-Doped Fiber Amplifier (PDFA), and then passed through an optical filter to minimize the ASE noise. Following this, the light is directed to a high-speed commercial photodetector for the optical-electrical (OE) signal conversion.

From the electrical perspective, the DC bias voltages were applied across both arms—using the shared n-contact metal and the separated p-contact metals—via the DC port of the bias-tee. Two Keithley 2400 source meters are employed, enabling individual control and photocurrent readouts for both MZM arms, as illustrated in the circuit in Fig. 5.16. The heaters, designed to compensate phase mismatch in the two arms stemming from fabrication variances, remained biased throughout the measurements.

The RF signal from the vector network analyzer (VNA) port one, is transmitted through the bias-tee and the GS probe to the on-chip RF pads. Both pads are connected to the p-type active sections on each arm, establishing a push-pull architecture. The high-speed commercial photodetector, processing the output from our modulators, is interfaced with VNA's port two. Consequently, the VNA's S21 trace represents the electrical-optical-electrical (EOE) frequency response of our link.



Figure 5.16: Experimental setup for bandwidth measurement



Figure 5.17: EOE frequency responses of modulators

Fig. 5.17 shows the small signal electro-optic-electrical (EOE) responses of the modulators by measuring S21 from VNA using the setup illustrated in Fig. 5.16. The frequency dependent loss from the photodetector has been subtracted from the measured curves. As illustrated in Fig.5.17, the measured 3-dB EOE bandwidths of 400  $\mu m$ , 200  $\mu m$  and 100  $\mu m$  reached 25 GHz, 50 GHz and over 67 GHz, which is record-high for III-V MZMs at O-band.

To understand the modulator's RC bandwidth limitations, electrical S11 responses were measured and analyzed to extract the elements of the equivalent circuit model of the devices. As illustrated in Fig. 5.18 (a), the estimated junction capacitance of the 100  $\mu m$ , 200  $\mu m$ and 400  $\mu m$  devices are at 25 fF, 58 fF and 146 fF respectively. The corresponding 3-dB RC bandwidths calculated from the equivalent circuit model are 89 GHz, 46 GHz and 20 GHz. These values align well with the measurement results. Notably, by integrating a traveling wave electrode design, there's potential to achieve similar bandwidth performance but with lower V<sub> $\pi$ </sub> in the future.



Figure 5.18: (a) Equivalent circuit used for S11 fitting and extracted parameters.  $(C_j:$  Junction capacitance,  $R_s$ : Series resistance,  $C_pad$ : Metal pad capacitance,  $R_sub$ : Substrate resistance,  $C_sub$ : Substrate capacitance,  $R_load$ : Load resistor. Measured S11 and fitting of (b) Magnitude and (b) Phase of a 100  $\mu m$  device

In addition to small signal tesing, the MZMs are also tested with large signal modulation to determine their suitability for high-speed communication. As shown in Fig. 5.19, the setup for eye diagram measurements is similar to the bandwidth measurement. However, we utilized a  $2^{31}$ -1 pseudorandom bit sequence (PRBS) generator alongside a 40 GHz broadband amplifier here to generate a 40 Gb/s 6-V V<sub>pp</sub> NRZ signal to drive the modulator. The setup also includes an additional 50  $\Omega$  termination, probed on the MZM RF pads through a SG probe and a bias-tee as DC block, distinguishing it from the previous configuration. The 50  $\Omega$  termination substantially reduces the RF reflection, which in turn enhances the ER of the modulator. Moreover, it diminishes the RC time constant, contributing positively to the bandwidth as well. The optical input was kept consistent at 15 dBm from a 1310 nm tunable laser. The optical output signal is fed into a prasedymium-doped amplifier (PDFA) to amplify the optical signal to the level that ensures a sufficiently robust photocurrent from the photodetector. After optical-electrical conversion, the electrical signal is fed into a sampling scope to observe the eye diagram performance.



Figure 5.19: (a) Laboratory probing system for eye diagram measurement. (b) Experimental setup scheme for eye diagram measurement.

The 40 Gb/s eye diagram, measured from the MZM, exhibits a clear opening at its center, as depicted in Fig. 5.20 (b). When compared with the eye diagram derived directly

from the PRBS (Fig. 5.20(a)), the transmitted eye diagram basically retains its shape. The increase in noise observed is most likely dominated by amplified spontaneous emission noise (ASE) from the PDFA thus can be suppressed by adding a narrow FWHM optical filter with 1-nm bandwidth. Fig. 5.20 (c) demonstrates a good alignment between the electrical eye pattern diagrams from PRBS source and our device . These results prove the potential viability of our modulator in high-speed, high-capacity communication applications.



Figure 5.20: (a) Electrical eye diagram from 40 Gb/s PRBS source (b) Measured 40 Gb/s optical eye diagram from modulator (c) Electrical and OE-converted optical PRBS pattern

#### Insertion loss

The insertion loss of our  $4-\mu$ m wide device was measured to be approximately 28 dB. To investigate the passive loss from the modulator, we implemented several individual passiveonly designs on the chip. As depicted in Figure 5.21, we utilized a waveguide with two 50- $\mu$ m radius S bending structure and another waveguide featuring an MMI and two small S-bends with a 15  $\mu$ m radius to measure the passive structure loss. The waveguides,  $4-\mu$ m wide on top and with an MQW core width of about 1.4  $\mu$ m, have a total length of 2.8 mm. The measured fiber-in-fiber-out loss for this waveguide is 12 dB. According to our simulations, an estimated fiber-to-waveguide coupling loss of 5 dB per facet and an S-bending loss of 0.3 dB are accounted for, leading to a concluded waveguide propagation loss of 1 dB/mm. Subsequently, the total loss for the 1-to-2 MMI structure was measured to be roughly 20 dB. Utilizing the coupling and propagation loss measurements from the previous waveguideonly structure, the loss from a single MMI, together with the two small-radius S bends, is estimated to be 8 dB— largely attributed to the small S bends. Based on the above measurements and analysis, the total 28 dB insertion loss of our device comprises 12 dB from waveguide and coupling loss and 16 dB from two MMIs.



Figure 5.21: Passive structures to characterize insertion loss

#### 5.4 Summary and future work

The bar-level modulators were successfully fabricated and characterized. The modulator has a record-high 3-dB bandwidth of over 67 GHz, and  $V_{\pi}$ L of 3 V·mm which is comparable to other modulators for 1550 nm reported in the literature. The 300  $\mu$ m × 1000  $\mu$ m modulator chiplets have been successfully printed on the  $Si_3N_4$  target wafer. However, one remaining challenge is to address the high optical coupling loss (>60 dB) between the silicon nitride and III-V waveguides. Most likely, this is due to insufficient protection of the facets during the release layer etch and we have developed a new fabrication process to prevent the  $SiO_2$ protection layer from etching.

## Chapter 6

# Foundry-enabled microwave photonics integrated circuit

In this work, I experimentally demonstrate a fully integrated microwave optoelectronic mixer subsystem on a silicon photonic integrated circuit (PIC). The chip was fabricated by AIM Photonics foundry. Leveraging the Si MZM and high-speed Ge-PD, our mixer subsystem boasts an impressive bandwidth of 30 GHz and a spurious-free dynamic range (SFDR) of  $69 \,\mathrm{dB} \cdot \mathrm{Hz}^{\frac{2}{3}}$ . To the best of my knowledge, this architecture demonstrates the widest bandwidth reported among fully on-chip mixers on any platform.

#### 6.1 Introduction and design concept

Microwave mixers, which facilitate frequency up- and down-conversion, are widely used in transmitters and receivers for various applications ranging from radar systems to wireless communication, satellite payloads, and diverse signal processing tasks such as frequency/phase discrimination and vector signal modulation/demodulation. However, as mm-wave electronic techniques experience bottlenecks like conversion loss and electromagnetic interference, microwave photonics offers an alternative. This technology, thanks to its expansive bandwidth, reduced transmission loss, and immunity to electromagnetic interference, appears promising. As Radio-Over-Fiber emerges as a cornerstone for future mobile communication networks, the interest of integrated microwave photonic circuits is rapidly increasing. Photonic-based RF frequency converters are especially noteworthy, delivering vast bandwidth and superior isolation further facilitating efficient long-haul transport via fiber-optic links[88].

In numerous studies involving photonic frequency upconverters, the photonic component typically functions as a front-end, while the mixer generally relies on two external modulators. Commonly, a single light wave is employed, and the two external modulators can be configured in a cascaded structure[89], [90], where the modulators for LO and IF modulation are arranged in series along the optical path as shown in Fig. 6.1 (a). However, cascaded mixers often encounter substantial power loss, necessitating the use of optical amplifiers. Alternatively, another mixer architecture utilizes parallel modulators, that the input light is divided into two paths. LO and IF signals are applied to each light path by an electro-optic modulator to mix the signals in the optical domain, with the RF signal being extracted following photoelectric conversion (Fig. 6.1 (b)). This parallel-modulator structure has previously been successfully integrated onto a silicon platform[91], [92].

Nonetheless, these mixer structures, which rely on external modulators to provide both LO and IF frequencies, are substantially constrained in their operational frequency range due to the modulators' bandwidth, especially when utilizing silicon modulators on existing SOI platform for integration. In our work, we introduce and experimentally prove the concept of on-chip Optically Pumped Mixing (OPM), wherein the LO is photonically supplied to the mixer rather than through an electrically-driven modulator, significantly broadening the upconversion frequency range. The configuration of OPM frequency converter is shown in Figure 6.1(c). Although similar structures have been demonstrated on bulk separated systems in prior work[93], [94], this research represents the initial attempt to fully integrate the technology on-chip.



Figure 6.1: Configuration of photonic frequency upconverter using (a) Cascaded structure (b) Parallel structure (c) Optically pumped mixing (this work)

In the design illustrated in Fig. 6.2 (b), we employed two external lasers to generate the optical LO and the signal. One of the benefits of this design is its flexibility: for instance, a single laser could be substituted with a comb laser or a microresonator soliton when aiming for multichannel applications. The monitor photodetectors are employed for testing purposes, which assist with optical alignment. An on-chip optical ring filter with 80 GHz (0.55nm) full width half maximum (FWHM) is present, serving dual purposes: it either narrows the linewidth of the input laser or selects a specific wavelength if comb source is in use instead of single laser. Following the filter, the light traverses through a silicon traveling wave Mach-Zehnder modulator (TWMZM), where the IF signal is applied. We chose a 18 GHz bandwidth traveling wave MZM complemented by a 50-Ohm termination for impedance matching at the end of transmission line. After modulation, this light is then combined with the second input from a second laser with slightly different wavelength. This
configuration creates an optical LO signal, generated from the heterodyne beat of the two lasers, enabling a IF-to-near-LO frequency conversion. This translated RF signal is then detected by an on-chip germanium photodetector (GePD) with a 1.1 A/W responsivity and 40 GHz bandwidth.

Additionally, the heterodyne signal can be channeled to an external output port. From here, it either gets detected by an even higher-speed photodetector, broadening the bandwidth, or to a photodetector integrated with antenna emitter [95] to generate high power microwave wireless signals.



Figure 6.2: (a) Microscope picture of PIC under test (b) Schematic of the system

## 6.2 Experimental results

The experimental setup for characterizing the system is illustrated in Fig. 6.3.I utilized two narrow-linewidth fiber lasers operating around the 1550 nm wavelength. To precisely determine the LO signal's wavelength, we divert a small fraction of the output laser light to a wavelength meter, while the remaining light is coupled into the on-chip silicon waveguide via a lensed fiber and an edge coupler. The IF signal is generated from Agilent E8257D signal generator and sent to the silicon MZM through a bias tee and GSG probe. For the MZM to operate optimally at its quadrature point, the DC port of the bias tee is connected to a Keithley 2400, acting as the DC voltage source. The signal from the PD is collected by a 67-GHz GS probe. This probe is connected to a bias tee, which is also linked to a DC source meter Keithley for the PD. Simultaneously, the electrical spectrum analyzer (ESA) is connected to the RF port of the bias T to collect the RF signal.



Figure 6.3: Schematic of experimental setup for bandwidth and SFDR measurement

#### Validation of Frequency Conversion Operation

To validate the functionality of our frequency up=/down-converter design, we performed a fundamental frequency conversion assessment. Utilizing an IF signal at 2 GHz and an LO set approximately at 7.2 GHz, the PIC was able to yield an up-converted, 5.2-GHz RF. The measured spectra is depicted in Fig. 6.4. It's pertinent to highlight that this was an initial, proof-of-concept test; consequently, the input power deployed was relatively modest, resulting in a photocurrent of around 0.6 mA from the PD. The LO is determined by the beat frequency of the two lasers and can be tuned widely from sub GHz to hundreds of GHz.



Figure 6.4: Measured spectra demonstrating upconversion

### Frequency conversion bandwidth

To assess the upconverting capabilities of our design, I undertook a series of measurements. I varied the LO frequency by fine-tuning the wavelength of the second laser and set our RF signal at specific frequencies of 500 MHz and 1 GHz. With this arrangement, our ESA captured and recorded the power of the resultant RF signal.

The experimental setup is clearly illustrated in Fig. 6.3. The 3-dB bandwidths for

both the LO and the IF signals are similar, around 30 GHz. It's worth noting that only calibration along LO path was performed, including the probe and bias tee. The power difference between different RF frequencies may be caused by the uncalibrated cables along IF path.



Figure 6.5: Measured frequency response of the PIC

### Linearity measurement

I also characterized the linearity performance of our optoelectronic mixer. An equalamplitude, two-tone testing setup was employed in this measurement. The experimental setup is shown in the dashed frame in Fig.6.3, with the specifics of the testing methodology illustrated in Fig. 6.6. An RF diplexer was used to couple the RF signals of two different frequencies of  $f_1 = 5$  GHz and  $f_2 = 5.5$  GHz simultaneously onto the MZMs without mixing them prematurely. Our frequency choices were dictated by the constraints of the RF diplexer. After RF diplexer, the signal is amplified by an RF amplifier to have higher and adjustable input power. After the frequency upconversion process, the fundamental tones are located at  $f_1$  (5GHz) and  $f_2$  (5.5 GHz) distances from the LO frequency. This led the third-order intermodulation distortion (IMD3) signals to be at  $2f_1 - f_2$  (4.5 GHz) and  $2f_2 - f_1$  (6 GHz) away from the LO frequency. The fundamental signal power, together with the IMD3 signals, was recorded while increasing the input RF power. Throughout this procedure, the photocurrent was set at 1.6 mA and LO frequency maintained at around 25 GHz.



Figure 6.6: Schematic of SFDR measurement methodology

The collected and calibrated data are graphically represented in Fig. 6.7, showing the relationship between the fundamental tone, IMD3 power, and their corresponding curves with slopes of about 1 and 3. As shown in Fig. 6.7, an output third-order intercept points (OIP3) of -37 dBm is identified. The output noise figure N<sub>out</sub> was analyzed by observing and averaging the noise floor of the ESA during the measurement. An N<sub>out</sub> of approximately -140 dBm/Hz was estimated and subsequently utilized to compute the SFDR. We use the standard definition of SFDR: SFDR =  $(OIP3/N_{out})^{2/3}$ . A notable outcome from our analysis was the attainment of an SFDR of 69 dB  $\cdot$  Hz<sup> $\frac{2}{3}$ </sup>, affirming the efficacy of our optoelectronic mixer's design and performance. The SFDR measured now is reflecting the linearity performance of the entire link including the RF diplexer, RF amplifier, on-chip modulator and photodetectors. With improved measurement technique or calibration to

account the impacts from electrical signal side, the number is expected to be higher.



Figure 6.7: Measured SFDR of the PIC

## 6.3 Summary

In this work, I experimentally demonstrated a fully integrated microwave optoelectronic mixer subsystem on silicon photonic integrated circuit (PIC) with a record-high 3-dB bandwidth of 30 GHz and a spurious-free dynamic range (SFDR) of  $69 \,\mathrm{dB} \cdot \mathrm{Hz}^{\frac{2}{3}}$ .

## Chapter 7

# **Conclusion and Future work**

## 7.1 Conclusion

This dissertation focuses on high-speed photonic devices, including photodetectors and modulators, that employ hybrid III-V/Si technologies for both microwave photonics and telecommunication applications. Given the absence of high-power high-speed active devices like photodetectors and modulators in silicon photonics realm, the III-V material remains favored for its superior properties. Consequently, integrating III-V based devices with the silicon platform has garnered significant interest. To this end, I have developed waveguide photodetectors grown on silicon through heteroepitaxy, high-speed photodetectors integrated with the SiN waveguide platform via heterogeneous bonding, and micro-transfer printable, highperformance Mach-Zehnder modulators. Beyond standalone devices, I also have designed and tested a system-level PIC on silicon, that was realized through the AIM Photonics foundry fabrication service.

Regarding the waveguide photodetector directly grown on silicon, I developed both its fabrication and characterization. The photodetector exhibits a high responsivity of 0.78 A/W and a 3-dB bandwidth of 28 GHz, a record at the time we published the results. Also, an open NRZ 40 Gbit/s eye diagram was detected by our device. The outstanding per-

formance of the III-V/Si waveguide photodetector underlines its potential for III-V/silicon platform integration for diverse applications.

In collaboration with Dr. Xu Yi's group on the project involving high-speed photodetectors integrated with microresonators on the SiN platform using heterogeneous bonding, I took the lead in device design, fabrication development, and characterization. The fabricated single PD exhibited a responsivity of 0.45 A/W, a 53-GHz 3dB bandwidth, and an RF power of -8.9 dBm at 50 GHz. The balanced PDs achieved a record-high 3-dB bandwidth of 30 GHz and a CMRR of 26 dB at 30 GHz. Notably, the photodetector's fabrication had a negligible impact on the microresonator's performance, indicating its suitability for diverse high-speed applications on the SiN platform.

In the project of transfer-printable O-band MZMs, I developed a novel fabrication process and measurement methodology. The MQW MZM achieved promising performance metrics: a low  $V_{\pi}L$  of 3 Vmm, a high bandwidth exceeding 67 GHz, and extinction ratio of up to 17 dB. Designed for micro-transfer printing — an increasingly favored integration method — the successfully printed MZMs with high yield shows potential of future integration once the remaining issues have been addressed (see future work).

Another topic of my PhD work centered on silicon PIC design. Our presented optoelectronic frequency mixer shows a 3-dB IF bandwidth of 30 GHz, with potential scalability for multi-channel applications.

## 7.2 Future work

### 7.2.1 Heterogeneous photodetector integrated with microresonator

#### Soliton Measurement

The ultimate aim of this project is to realize a complete integration of the microring resonator with the high-speed photodetector for on-chip Kerr soliton detection and mmWave generation. As demonstrated in Chapter 4, The performance of the high-speed PD has been demonstrated. The next phase entails soliton generation, followed by direct detection using our integrated photodetectors.

Our chip design includes micro-ring resonators with free spectral ranges (FSR) of approximately 40 GHz, 50 GHz, and 100 GHz and an average intrinsic quality factor (Q) of  $1.1.4 \times 10^6$ . The experimental setup is depicted in Fig. 7.1. To achieve a singular soliton state, we employ a swift pump laser frequency scanning technique. The laser undergoes a frequency scan at a rate of 20 GHz/ $\mu$ s. This scan will be halted as soon as the pump laser frequency aligns with the red-detuned regime of the resonator, ideally producing a single soliton state with a pulse width of 35.4 fs.

On the detection front, the photodetector will be connected to a 100-GHz bias tee, the DC port of which links to voltage source supplying 3V reverse bias to the PD. The RF port of this bias tee is then connected to a vector network analyzer (VNA) to record the emerging mmWave signal. The VNA can measure signals up to 110 GHz and maintains a rather low noise floor of -90 dBm at this frequency.

If the experiment proceeds as planned and a single soliton is successfully generated, the detected RF power should surpass traditional heterodyne measurements by 6 dB under equivalent photocurrent conditions. Detailed analysis can be accessed in [57]. We aim for this platform to set a new benchmark in scalable, integrated photonics for high-frequency applications.Such advancements could revolutionize compact, low-noise high-frequency sources, benefiting fields like spectroscopy, ranging, and wireless communications.



Figure 7.1: Experimental setup of soliton and pd measurments

#### Future design

Inspired on previous research [96] [97], a two-stage taper was also designed for better PD performance in this project. The large refractive index difference between  $Si_3N_4$  and InP-based materials makes it challenging to make use of the adiabatic coupling schemes that were mature for heterogenous integration of III-V on Si. Here I propose a novel coupling strategy that adopts an InP layer as the intermediate matching layer. The index difference between the  $Si_3N_4$  and the III-V material is bridged by this intermediate layer of InP. Most of the light can be coupled out of the  $Si_3N_4$  waveguide into the InP layer first and then be absorbed by active region. Fig. 7.2 illustrates the new designed epi and optical simulation based on this epilayer.



Figure 7.2: (a) Epilayer structure (b) Simulation of field density along waveguide (c) Schemetic of device design from top view and the field profile of cross section

A III-V taper with 50-nm to 3- $\mu$ m width, 600-nm thickness, total length of 300- $\mu$ m was designed to reduce the effective index to match it with  $Si_3N_4$  waveguide. An improved epilayer was designed to form this bridging InP layer. This InP layer was thoroughly investigated in this work by FDTD simulation. As shown in Fig. 7.2(b), the matching InP taper layer can achieve a more than 80% coupling efficiency from  $Si_3N_4$  waveguide. Most of the light is transmitted to the InP layer, which is much closer to the InGaAs absorber layer. Thus a 10- $\mu$ m device is able to absorb most of the light. This layer will significantly improve the quantum efficiency of the PD without sacrificing bandwidth. With the recent addition of an Electron-beam lithography tool in our cleanroom, which has a resolution of 50 nm, this fabrication of this design is now achievable.

### 7.2.2 Micro-transfer printed MQW modulator

One persistent challenge in this project is the significant coupling loss (about 60 dB) between  $Si_3N_4$  and III-V waveguides. To address this, we've refined our processes, particularly focusing on the etching of spacer and release layers – a critical step in preparing for transfer printing. This step heavily influences both the printing yield and coupling efficiency. At first, we etched both spacer and release layers by selective wet etching. Severe undercut and skewed sidewall caused by lateral etching were observed in Fig. 7.3(a). We improved the process by using hybrid etching that starts with 10-min dry etching, followed by selective wet etching. The undercut issue was solved by this method, comparing 7.3(b) and 7.3(a). However, spacer layer shrinking is still noticeable. Ultimately, a photoresist masked twostep dry-etch only process was adopted. As shown in fig. 7.3(c), the spacer layer dimension stayed consistent during etching, which reduces the risk of waveguide damage in the following steps. It should be mentioned that the release layer etch and transfer printing was done by our collaborator X-Celeprint.



Figure 7.3: SEM of devices after spacer defining by (a) Wet etching only (b) Hybrid etching (c) Dry etching only

Despite improvements to the process flow, waveguide undercutting remains an issue. The latest SEM image of a printed device can be seen in Fig. 7.4. The evident gap between the two cladding layers suggests that the MQW waveguide was underetched during the release layer's wet etch process. Our next steps to rectify this involve refining the protection layer. We hypothesize that utilizing a double layer of SiO2/SiN instead of our previous single layer in addition to changes to the blanket SU8 dry etch will help protecting the waveguide facet from etching. Additionally, expanding the spacer layer further from the waveguide facet might provide improved protection, albeit at the potential cost of reduced coupling efficiency.



Figure 7.4: SEM of modulator waveguide facet after printing

For further move on this or similar project, we'll design angled waveguide on the both chiplets and the SiN waveguides to reduce loss caused by optical reflection. Also, traveling wave electrodes design will be introduced in order to overcome the RC limit in longer modulators that have much lower  $V\pi$ .

### 7.2.3 Microwave PIC on AIM tapeout

The preliminary testing of the PIC chip has been previously conducted and detailed. As depicted in Fig. 6.2, our approach involves two distinct design variations. The first design utilizes the on-chip GePD, aiming for a fully integrated microwave PIC. Conversely, the second design variation enables light coupling off-chip through a lensed fiber instead of direct detection. This off-chip approach offers enhanced flexibility of the link, enabling us to amplify optical power, leverage stand-alone high-speed PDs for superior bandwidth performance, and channel the light to a PD antenna-integrated chip for wireless transmission.

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- J. Gao, T. C. Tzu, K. Sun, P. A. Morton, J. B. Khurgin, and A. Beling, "Over 67-ghz bandwidth and 3 vmm vpil multiple quantum well mach-zehnder modulator for 1310 nm", In processing, 2023.
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