# Biomedical Circuits and Signal Analysis Systems for Measurement within Microsystems

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By

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## **APPROVAL SHEET**

This

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## Soeideh

to

for her endless love, patience and support

and Siavash & Anoush

without whom I could not carry on ...

تعديم به حمسر عربر سحيده ، م خاطرتمامی محامیت ها ، صبوری وعشق حالصاد اس و پسرایم مس<u>ا</u>دش دانومش ر مرسون این تحل این سالها برایم مکن مود ...

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### Abstract

Microsystems are especially well-suited to the study of biological tissues, cells, microbials, and molecules, due to their capability for enabling microfluidic separation towards selective enrichment, high levels of parallelization, and highly sensitive spatially and temporally resolved measurements. However, current innovations to enhance biomedical measurements are chiefly focused in the sphere of materials chemistry and device design. We seek to advance biomedical measurements within microsystems integrating key technologies from electronics and signal analysis fields.

Conventional techniques for cell separation are predominantly based on hydrodynamic methods applied to fluorescence- and magnetic-activated cell sorting. However, these techniques suffer from a lack of specificity, high cell loss, use of labels, and high capital/operating cost. Dielectrophoresis (DEP) over an insulator layer (iDEP) or contact-less DEP (cDEP) offers unique advantages for the sorting and analysis of biosystems due to its label-free ability for selective transport based on inherent dielectric properties, which can advance usability, throughput, and efficiency of cell separations. One of the main bottlenecks in iDEP-based cell separation is the physical separation of the electrodes from the sample for reducing the destruction of cells, leads to the need for a higher voltage AC signal (>  $100 V_{RMS}$ ) at MHz level. Furthermore, the microfluidic device geometry and architecture of the sample and electrode channels need to be optimized to maximize the fraction of the applied voltage available for DEP manipulation.

Despite the technological capabilities of forensic laboratories, the backlog in samples await DNA analysis has become a severe problem. This ever-growing backlog will not be reduced without new techniques that provide automation and enhanced throughput.

This dissertation is focused on the design and implementation of electronic circuits and signal analysis systems to address the current limitations in a variety of micro- or bioanalytical systems. Innovations presented here include designing a wideband high voltage AC generator that addresses the performance degradation of commercial amplifiers, an impedance analyzer for optimization of frequency-selective electrokinetic manipulation in microfluidic systems, and a compact and more efficient circuit for real-time tracking of resonance frequency for sample manipulation by acoustophoresis.

## Chapter 1 Wideband high voltage amplifier for insulated or contact-less DEP

#### **1.1 Introduction**

Dielectrophoresis enables frequency-modulated manipulation of polarized bio-particles under a spatially non-uniform electric field [1, 2] and is widely applied to selective transport, separation, and characterization of biosystems [3]. In particular, its application as electrode-less [4, 5] or insulator dielectrophoresis [6, 7] (iDEP), wherein the polarized particles are directed towards (by positive DEP or pDEP) or away (by negative DEP or nDEP) from spatially localized regions of high field caused by insulating constrictions in a microfluidic device, offers unique advantages for the sorting and analysis of biosystems. First, in comparison to electrode-based methods, problems associated with field-induced adhesion and destruction are reduced [8] since bio-particles are manipulated in an electrode-less or contact-less manner [9] across a wide spatial extent spanning the entire device depth, thereby enhancing throughput. Second, this design enables facile integration of DEP preconcentration of analytes with a variety of sensing paradigms, since the polarized particles are not trapped at the vicinity of the electrodes driving the DEP, but at insulator constriction regions where capture probes can be immobilized for enabling selectivity through biorecognition strategies [10]. However, the electrodes driving the DEP field orthogonal to the fluid flow are typically spaced considerably away from each other (~0.5-2 cm) to ensure a wide spatial extent for particle manipulation and to facilitate the absence of field distortion and bio-particle damage that can occur due to electrode edges within the channel. Hence, there is a need for higher voltages (typically ~100  $V_{RMS}$ ) than is required with electrode-based DEP (typically ~10  $V_{RMS}$ ) to ensure the necessary field for trapping particles of low polarizability, even within 3D constrictions [11] or nano-device designs that enhance localized field [12, 13]. This high voltage requirement is particularly problematic for conducting iDEP in the MHz frequency ranges due to the performance degradation of commercial amplifiers. As a result, a majority of iDEP studies are restricted to DC fields [14] or low-frequency AC fields [15] ( $< 500 \, kHz$ ), where the discrimination is based only on cell membrane conductance rather than based on membrane capacitance and electrophysiology of cellular cytoplasm (1 - 10 MHz) or nucleoplasm (> 40 *MHz*), or the unique conformation of biomolecules (> 1 *MHz*). Herein, we describe the design

principles for constructing a wideband power amplifier for performing iDEP at MHz frequencies. This instrumentation innovation has been essential towards achieving quantitative iDEP based separation of subpopulations of *C. parvum* oocysts based on sporozoite integrity in their cytoplasm (at  $1 - 10 \ MHz$ ) [16, 17] and towards coupling iDEP preconcentration to the detection of biomarkers such as neuropeptide Y at ~3 MHz [18], prostate-specific antigen (at ~5MHz) [19] and protein-DNA complexes (at  $1 \ MHz$ ) [20]. We envision its application towards enabling distinctions based on the electrophysiology of cell cytoplasm and nucleoplasm for separating stem cell subpopulations [21].

#### 1.2 The summary of the design

The literature on wideband power amplifiers is scarce. Prior work has focused on amplifying voltages (up to 1 kV) for operation at frequencies up to only a few hundred kHz [22, 23] rather than at higher frequencies. State-of-the-art commercial power amplifiers (FLC Elec. A400DI, Trek Inc. 2100HF, and Thorlab Inc. HVA200) can operate up to ~500  $V_{pp}$  until 500 kHz, after which they exhibit a steady drop in power. To address this limitation, we have designed and built a wideband high voltage amplifier, with exceptional performance in both sub-MHz and MHz frequency ranges. Additionally, the built-in signal generator has made this instrument an "All-inone" AC High Voltage AC generator. This unique feature enables researchers to control all specs of the HV signal in only one instrument, resulting in portability and less complexity in system integration. **Fig. 1-1** shows the simplified block diagram of the whole system.



Fig. 1-1 Block diagram for the wideband amplifier circuit

The system is capable of communicating with PC software (e.g., LabVIEW or Python) via a USBto-UART protocol translator. It helps to run a variety of sequential cycles in an automated way without needing user intervention. The following sub-sections briefly describe some of the most critical units inside the system.

High-speed dual-amplifier and Splitter: The speed of power Op-Amps under high voltage settings is limited by their slew rate. Slew rate is the maximum rate of change of output voltage per unit time ( $V/\mu s$ ). Limitations in slew rate capability can give rise to distortions in the signal shape of the amplifier output. For a sinusoidal signal, the slew rate (SR) capability at all points in an amplifier must satisfy:

Slew rate (SR) 
$$\geq \pi \times V_{pp} \times f$$
 (1-1)

Here, *f* is the signal frequency, and  $V_{pp}$  is the peak-peak amplitude of the signal. Hence, to obtain a sinusoidal signal output at 5 *MHz* with an amplitude of 250  $V_{pp}$ , we need an Op-Amp with a slew rate of 4000 *V*/µs. This is far beyond the capability of any ultrafast power Op-Amp in the market. PA107DP (APEX Micro, AZ), for instance, is capable of slew rates only up to 2500 *V*/µs [24]. To address this limitation, we feed two identical PA107DP Op-Amps with counter-phase (180-degree phase difference) signals of the same amplitude. In this manner, whenever the output of one Op-Amp is at its maximum, the output of the other Op-Amp is at its minimum, thereby causing a voltage difference between the two outputs, which is twice that of individual outputs. However, the Splitter unit that provides these counter-phase signals needs to be designed with super-fast low-power Op-Amps like LM7171 (Texas Instruments, TX) to prevent deviation from the 180° phase difference for eliminating distortion and nonlinearity over a wide dynamic range of input signals and frequency bandwidth.

To maximize the output amplitude in lower frequencies (< 1 *MHz*), we have employed two identical power operational amplifiers: PA98A (Apex Micro, AZ) in a counter-phase arrangement. This Op-Amp is optimized to provide larger output signals up to ~400  $V_{pp}$  in lower frequencies (LF) but has a lower slew rate (1000  $V/\mu s$ ) [25].

A network of reed relays connects/disconnects the flow of signal through either of these two Op-Amp types automatically by receiving the control commands from the controller. As a result, the high voltage amplifiers (LF) are active in frequencies below 1 MHz, while the wideband amplifiers (HF) take the wheel after 1 MHz.

Self-adjustable Power Supply: Power dissipation  $(P_D)$  inside the Op-Amps can limit the maximum output power at high frequencies. If the output current is small  $(P_{Load} \ll P_D)$ , then for two symmetrical high-voltage supplies  $(\pm V_S)$  and supply current of  $I_S$ ,  $P_D$  is given by:

$$P_D = (V_S^+ - V_S^-) \times I_S = 2V_S I_S$$
(1-2)

With increasing frequency, the power dissipation inside high-frequency OP-AMPs (PA107DP) rises due to the higher supply current ( $I_s$ ) from the lower internal parasitic impedances, approaching the maximum allowed dissipation (~60 watts).

In the megahertz frequency range, the significant drop in the output amplitude allows for lower supply voltage levels ( $\pm V_S$ ) without affecting the signal amplitude. This reduction in power dissipation gives this opportunity to increase a higher quiescent current ( $I_s$ ) by trying a larger input voltage, yielding higher output power. Hence, a self-adjustability feature is implemented for dynamic modulation of the supply voltages ( $V_S$ ) at each working frequency to ensure minimal dissipation in the 3 - 7 MHz range. In this manner, we can compensate for the drop in gain at higher frequencies by adjusting for the optimal input signal levels required to maximize output power while avoiding over-heating and reducing signal distortion over a wide frequency range.

The HV supply voltages ( $\pm 90V$  and  $\pm 180V$ ) are generated using customized linear regulator circuits following the conventional full-wave rectification and capacitor filtering. The customized power transformer (Pacific Transformer, CA) has dual center-tapped windings with the input of 120V, 60 Hz, and two output lines of 140V @ 0.8A and 250V @ 0.2A. One helpful implemented feature is on-board voltage and current monitoring of these two high voltage channels by the microcontroller to determines whether the power Op-Amps are operating within normal/safe conditions.

**Internal signal generator and preliminary amplification:** The signal generator unit includes a Direct Digital Synthesis (DDS) IC (AD9851, Analog Devices, MA), programmed by a central microcontroller (PIC16F887, Microchip, AZ) to synthesize the desired frequency (1 *kHz* to

15 *MHz*). The DDS output has a fixed amplitude of  $1V_{pp}$  fed into a wideband variable gain amplifier: VCA8245 (Texas Instruments, TX), whose gain is adjusted a Gain number (0 – 100) issued from the controller. As a result, the actual gain for this unit can vary from 0 to 2. The Gain number at each frequency point has a maximum limit to avoid excessive power dissipation and signal distortion. Next, the pre-amplifier unit elevates the amplitude to the desired level for high voltage amplifiers' input. The pre-amplifier consists of two cascaded wideband Op-Amps (LM7171), with an overall gain of 5.

**Amplitude detector:** The amplitude detection unit constantly extracts the output amplitude and delivers a DC voltage, representing the amplitude, to the controller. It eliminates the need for an external oscilloscope. This unit includes a wideband voltage divider and a precise peak detector that uses a fast comparator (AD8561, Analog devices, MA). The accuracy of measured amplitude is around  $\pm 2\%$ .

#### **1.3 Comparison of amplifiers for signal characteristics**

The performance of the wideband amplifier was compared to that of a so-called conventional amplifier (FLC A400DI) since this is the only product with an output of 300  $V_{pp}$  up to 1 *MHz*. The respective amplifiers were compared based on the frequency response of their output signal amplitude, signal distortion, and parasitic DC at the output. Output signal shapes were captured by a digital oscilloscope (Tektronix MDO3024) and then were quantified by MATLAB.

#### **1.3.1 Frequency response**

The frequency responses of the wideband amplifier's output amplifier are compared to those from the FLC A400DI amplifier in **Fig. 1-2**. It is apparent that while the conventional amplifier offers greater voltage in the low-frequency range ( $< 400 \ kHz$ ), the wideband amplifier's output is far higher, onwards from 400Hz.



Fig. 1-2 Frequency responses of the maximum voltage in wideband amplifier (blue) vs. the A400DI (Red)

### 1.3.1 Signal distortion

If the shape of a periodic signal with the frequency of  $f_1$  deviates from the pure sinusoid of that frequency, it can be called a "distorted" signal. It means that rather than the fundamental frequency  $(f_1)$ , other frequency components (harmonics) also exist in the signal that are integer multiples of  $\omega_1$ . If the n<sup>th</sup> harmonic has an amplitude of  $V_n$  (with n = 1 being the fundamental), the Total Harmonic Distortion (THD) is calculated as:

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + \dots + V_n^2}}{V_1}$$
(1-3)

An alternate problem with conventional power amplifiers is the emerging harmonic distortion at MHz frequencies. Herein, the higher-order harmonics' amplitude levels are large enough to cause a deviation of the sinusoidal wave shape from a single frequency signal to one that includes signals at several harmonic frequencies, thereby influencing the polarizability dispersion (**Fig. 1-3 a-d**). For the wideband amplifier, the sinusoidal wave-shapes are preserved in the MHz range to some extent (**Fig. 1-3 e-h**). The normalized amplitude at each harmonic with respect to the fundamental frequency ( $V_n/V_1$ ) is shown in **Fig. 1-3 j-k**, wherein significant distortions are apparent with the conventional amplifier beyond 5 *MHz*, especially at the second harmonic. In contrast, the distortions are much weaker with the wideband amplifier.



**Fig. 1-3** Output waveform of a conventional amplifier (FLC A400DI) for  $Vin = 15 V_{pp}$  (a-d) vs. wideband amplifier (e-h) in the 1 - 15 MHz range (DC offset and THD are indicated). Normalized amplitudes  $(V_2/V_1)$  and  $(V_3/V_1)$  at 1 - 10 MHz for (j) conventional amplifier and (k) the wideband amplifier.

The main implication of this harmonic distortion is the alteration in the DEP force magnitude and, in some scenarios, the force direction too. To explore the impact of signal distortion on the DEP force, we first need to relate THD to the force mathematically.

The *Clausius–Mossotti* relation describes the DEP force ( $F_{DEP}$ ) on a spherical particle of radius: *a*, in a medium of permittivity:  $\epsilon_m$ , under an RMS field:  $E_{rms}$  [2]

$$F_{DEP} = 2\pi\epsilon_m a^3 Re[K_{CM}(f)] \nabla E_{rms}^2$$
(1-4)

Here,  $K_{CM}$  is the *Classius-Mossoti* factor, which represents the frequency-dependent complex dielectric contrast of the particle versus the medium:

$$K_{CM}(f) = \frac{\epsilon_p^* - \epsilon_m^*}{\epsilon_p^* + 2\epsilon_m^*}$$
(1-5)

Here,  $\epsilon^*$  denotes the frequency-dependent complex permittivity, which includes both permittivity ( $\epsilon$ ) and conductivity ( $\sigma$ ) as  $\epsilon^* = \epsilon + (\sigma/j2\pi f)$ . Subscripts *p* and *m* denote the respective property of particle and medium, respectively.

In case the applied field is not purely sinusoidal, we can expand  $E_{rms}$  based on its orthogonal harmonics  $(E_1 \dots E_n)$  using Parseval's theorem:

$$E_{rms}^2 = E_1^2 + E_2^2 + E_3^2 + \cdots$$
(1-6)

 $K_{CM}$  may take a different value at each frequency. However, we can assume that the most significant differences occur between the first two harmonics, with all other harmonics at higher frequencies exhibiting minor differences in  $K_{CM}$  value equal to  $K_{CM}(f_2)$  denoted as  $K_{CM}(f_m)$ , then (1-4) can be shortened as:

$$F_{DEP} = 2\pi\epsilon_m a^3 \nabla \left( Re[K_{CM}(f_1)] E_1^2 + Re[K_{CM}(f_m)] \underbrace{(E_2^2 + E_3^2 + \cdots)}_{E_1^2.THD^2} \right)$$
(1-7)  
$$F_{DEP} = 2\pi\epsilon_m a^3 Re[K_{CM}(f_1)] \nabla E_1^2. (1 + \alpha THD^2)$$
(1-8)

Here,  $\alpha$  is the ratio of  $Re[K_{CM}]$  at the frequencies of higher-order harmonics versus fundamental harmonic ( $\alpha = \frac{Re[K_{CM}(f_m)]}{Re[K_{CM}(f_1)]}$ ).

The Peak-to-Peak amplitude of fundamental harmonic is not generally equal to the Peak-to-Peak amplitude of a distorted signal. To better understand the effect of distortion on DEP force, we would like to compare the DEP force with the so-called *Ideal* DEP force ( $F_{Ideal}$ ) from a sinusoidal field with the same Peak-to-Peak amplitude to the original signal:

$$F_{Ideal} = \frac{1}{8} \cdot 2\pi\epsilon_m a^3 Re[K_{CM}(f_1)] \nabla E_{pp}^2$$
(1-9)

The DEP force ( $F_{DEP}$ ) and the Ideal DEP Force ( $F_{Ideal}$ ) can be related together by comparing equations (1-8) and (1-9):

$$F_{DEP} = (1 + \alpha THD^2) \frac{\nabla E_1^2}{\nabla E_{pp}^2} F_{Ideal}$$
(1-10)

The device geometry determines the distribution of the Electric field throughout the microfluidic device. The E-field is linearly proportional to the applied voltage (*V*), though, at each point, it has different intensity. Therefore, the magnitude of  $\nabla |\mathbf{E}|^2$  (i.e.  $\nabla E^2$ ) is proportional to  $V^2$  and we can replace the ratio of gradient terms ( $\nabla E_1^2 / \nabla E_{pp}^2$ ) in **Eq. (1-10)** with their corresponding applied electric potentials:

$$F_{DEP} = (1 + \alpha THD^2) \left(\frac{V_1}{V_{pp}}\right)^2 F_{Ideal}$$
(1-11)

Here,  $V_{pp}$  and  $V_1$  are the Peak-to-Peak amplitudes of the applied electric potential and its fundamental harmonic, respectively.

In the particular case where all harmonics, including the fundamental harmonic, lie in the pDEP region and have the same polarizability dispersion ( $K_{CM}$ ), we have ( $\alpha = 1$ ), and Eq. (1-11) can be simplified to:

$$F_{DEP} = (1 + THD^2) \left(\frac{V_1}{V_{pp}}\right)^2 F_{Ideal}$$
(1-12)



Fig 1-4 Three regions of the polarizability dispersion where the main harmonics may lie.

In this scenario, as shown in **Fig. 1-4b**, the frequency-dependent term:  $(1 + THD^2)$  influences the force dispersion, due to contributions of the higher-order harmonics, whereas the term  $(V_1/V_{pp})^2$  reflects the alteration in maximum amplitude of the output signal due to deviation from the ideal sinusoidal wave shape. Hence, while the distorted quasi-triangular wave shape of the conventional amplifier causes a reduction in DEP force by just 20% at 1 *MHz* (due to 10% THD and  $V_1/V_{pp} = 0.9$ ), the respective force reductions are substantial at 5, 7, and 10 *MHz*. On the

other hand, since the THD of the wideband amplifier is less than 10% and  $V_1/V_{pp}$  remains close to unity, the DEP force alteration is less than 5% over the MHz range.

Next, considering the scenario where the fundamental frequency  $(f_1)$  is in the nDEP region close to crossover towards pDEP, whereas the next significant harmonic  $(f_m)$  is in the pDEP region, as in **Fig. 1-4a**, then:  $\alpha \ll -1$ , since  $K_{CM}$  under nDEP  $(f_1)$  is usually less than that under pDEP  $(f_m)$ . This causes greater DEP force distortions from  $F_{Ideal}$  than the scenario in **Fig. 1-4b**, according to Eq. (1-11). In fact, the DEP force direction could also be altered at high enough THD values. A similar scenario can occur at ultra-high frequencies near the second DEP crossover region (**Fig. 1-4c**).

#### **1.3.3 Parasitic DC**

The Parasitic DC levels from the conventional amplifier exhibit a steady rise as the frequency increases. While the absolute parasitic DC levels are small, they become a greater fraction of the output at higher frequencies since slew rate limitations cause a steep decline in  $V_{RMS}$  output at the fundamental frequency. For instance, while the  $V_{RMS}$  to parasitic DC ratio is 250 at 1 *MHz*, it drops steeply to just 28 at 5 *MHz* and 8 at 10 *MHz*.



Fig 1-5. Influence of DC offset on AC field-driven pDEP (a), as quantified in (b).

This steady rise of parasitic DC in proportion to the AC field causes electrophoretic ( $F_{EP}$ ) and electroosmotic ( $F_{EO}$ ) forces to influence the net force balance. As apparent from Fig. 1-5b, while

these DC-driven electrokinetic forces tilt the potential profile to enhance trapping under nDEP, they also cause the leakage of particles under pDEP trapping, thereby altering the quantitative DEP force dispersion by reducing effective pDEP trapping in the MHz range. In fact, as per **Fig. 1-5**, beyond a critical level, DC fields can cause a reduction in the DEP trapping potential. On the other hand, the parasitic DC levels are negligible for the wideband amplifier, thereby offering highly quantitative DEP force dispersions. The parasitic DC levels for wideband and conventional amplifiers are denoted inside the **Fig. 1-2 a-h**.

#### **1.4 Comparison of amplifiers for iDEP dispersion in MHz range**

**DEP force quantification:** Comparison of the positive DEP levels on 3  $\mu$ m sized *Cryptosporidium parvum* (*C. parvum*) bio-particles in the MHz range was performed by using the respective amplifiers within an electrode-less iDEP device. Neglecting inter-particle interactions, the DEP force values were calculated using frame-by-frame tracking of the trapped particles to extract their displacement vectors (*x* and *y*) over time (*t*) to compute *F*<sub>DEP</sub> using:

$$F_{DEP} = m \frac{d^2 x}{dt^2} - 6\pi \eta a \frac{dx}{dt}$$
(1-13)

Here, *m* and *a* are the particles' mass and radius, and  $\eta$  is the viscosity of the fluid.



**Fig. 1-6** (a) Set-up for observing DEP behavior of oocysts. Translation vectors for oocysts under positive DEP. (h) Center-line and sidewall vectors for the constriction device.

#### **1.4.1 Tracking dielectrophoretic particle displacement versus time**

The set-up for imaging the dielectrophoretic translation of oocysts is shown in Fig. 1-6 a [17].

Based on data from high frame per second (~30 fps) movies of oocyst translation under  $F_{DEP}$ , the displacements (x & y) are tracked as a function of time (t) for particles translated towards the constriction tip under positive DEP (PDEP) (**Fig. 1-6 c**). Since particles' motion takes place in two-dimensional space, trajectories of particles encompass both X and Y coordinates, leading us to do all computations for both directions individually.

In this manner, the experimental raw data acquired in the form of video is processed to yield a table of position versus time, i.e. (x, y, t) coordinates for the analyzed oocysts. The displacement data (x and y vectors) as a function of time is algorithmically smoothed by using a high-order polynomial fit since the faster displacements under higher  $F_{DEP}$  require higher frame rates for accurately tracking displacement over time versus the slower displacements. Furthermore, while the oocyst is several pixels large in the video images, the tracking only records one central pixel per frame, which leads to some degree of noise in the data, which can be smoothed out using the polynomial fit. Hence, having a larger number of displacements versus time points, as obtained with the field non-uniformity of the enhanced spatial extent for the constriction device, improves the computed DEP force data's accuracy. To ensure an effective smoothing, we check for the lack of jagged features on the derivatives of Eq. (1-13). As a result, we obtain  $v_x = dx/dt$ ,  $v_y = dx/dt$ dy/dt,  $a_x = d^2x/dt^2$  and  $a_y = d^2y/dt^2$  for the oocysts at a particular applied field and frequency, after each of the disinfection treatments, which can be used to compute the X and Y components of  $F_{DEP}$  frequency response in the direction of the particle trajectory ("track" direction). At each point of the trajectory, the distance from the constriction (r) can be determined based on x and y coordinates:  $r = \sqrt{x^2 + y^2}$  and the total DEP force based on the value of  $F_x$ and  $F_y$  at that point:  $F_r = \sqrt{F_x^2 + F_y^2}$ . Therefore, we can compute the force vs. distance (F(r)).

#### 1.4.2 Normalizing for field non-uniformities

Within the constriction device, the electric field profile and hence,  $F_{DEP}$  vary depending on the displacement vector of the oocysts. It can create a variation in  $F_{DEP}$  up to an order of magnitude, depending on displacement direction and distance of the oocysts to the constriction tip of a given

device. Hence, we normalized all the data for field differences from the velocity tracked direction (track) to that along the centerline direction (CL) by accounting for the field differences ( $\nabla E^2$ ) between the "track" and "centerline" directions through a normalization factor:  $K = \nabla E_{track}^2 / \nabla E_{CL}^2$ . The  $\nabla E^2$  in the "track" direction is calculated by translating the oocyst's measured trajectory to a simulation of the device to read the magnitude and gradient of the electric field along this vector direction. The electric field's magnitude and gradient along the centerline direction (**Fig. 1-6b**) are also available from this simulation. In this manner, by dividing the computed DEP force along the "track" direction by the field enhancement ratio K, we ensure that all the variations in DEP force can be solely attributed to variations in particle polarizability, rather than field non-uniformities due to the device geometry.



Fig. 1-7 (a) Measured DEP force dispersion of *C. parvum* in the 1 - 7 MHz region using the conventional vs. wideband amplifier. Monitoring the trapping performance for (b) Wideband, and (b) conventional amplifier

The DEP force data in **Fig. 1-7a** show that while the trapping under pDEP using the conventional amplifier is apparent at 1 *MHz*, it is less noticeable at 3 *MHz* and absent at 5 *MHz*. On the other hand, with the wide bandwidth amplifier, the trapping force on untreated oocysts is significant and at a constant level in the 1 - 7 *MHz* range. As a result, differences in force dispersion are easily apparent in the MHz range for probing the cytoplasm of untreated versus heat-treated oocysts. In contrast, these are not apparent using the conventional amplifier.

#### **1.5 The prototype versions of High Voltage Amplifier/Generator**

We assembled a preliminary prototype of the High voltage wideband amplifier on multiple perforated boards to investigate the feasibility of high voltage amplification in higher frequencies. Shortly after, the first PCB-based prototype with a digital controller, keypad, and LCD interface was implemented in 2015. This unit had an input port to receive a low-amplitude signal from an external signal generator and an internal frequency detector unit to rapidly detect any change in frequency for automatic gain adjustment (Fig. 1-8a). Following a research contract between CytoRecovery<sup>TM</sup> Inc. and Swami Lab, we implemented multiple instruments with a new design in Spring/Summer 2018. The main changes included adding an internal signal generator unit to eliminate the need for external signal generators, more accurate gain adjustment, USB interface, and using SMT devices instead of traditional through-hole components (Fig. 1-8b). Recently, we redesigned the system as the CytoRecovery<sup>TM</sup> commercial product, wherein the performance in higher frequency (> 5 *MHz*), amplitude measurement, thermal management, and overall system reliability have been improved. It also includes a pump controller and can interface with the Cyto Chip holder that performs microfluidic device quality control (Fig. 1-8c).



Fig. 1-8 Photos from the front panel and internal circuit for different builds of the amplifier system: (a) High voltage wideband amplifier, 2015. (b) High voltage AC generator, 2018. (c) CytoRecovery<sup>™</sup> cell recovery system (main unit), 2020

**Table 1-2** lists the main specifications of the last generation of the High voltage AC generator, designed for CytoRecovery<sup>™</sup>.

Parameter	Specification	Validation		
Board dimensions	14" × 14.5"			
Input power	120 V AC – 2 A	Cell trapping studies (Fig. 1.7)		
Interface	USB 2.0			
Frequency range	10 kHz – 15 MHz			
Frequency resolution	0.1 Hz			
Output voltage	up to 600 $V_{pp}$ ( $f < 1 MHz$ ) up to 300 $V_{pp}$ ( $f > 1 MHz$ )	Fig. 1-2		
Output current	< 50 mA @ Vmax for each frequency	Electrical measurements		
Voltage adjustment	$< \pm 2 V_{pp}$	(Tektronix MDO3024)		
DC offset	< 0.5 V			
Distortion (THD)	typical: < 5% worse case @ 5 MHz: 10%	Fig. 1-3		

Table 1-2 The specifications of Cyto HV wideband AC generator

#### **1.6 Conclusion**

To enable electrode-less or contact-less manipulation of biosystems in the MHz frequency range, we present the design principles for a wideband power amplifier to address the steep drop in amplitude and the rise of signal distortion that occurs within conventional amplifiers. Through the counter-phase coupling of two operational amplifiers by using a wideband splitter circuit, in conjunction with a self-adjustable power supply and an attenuator to deliver a constant power output for avoiding over-heating and signal distortion due to saturation, we are able to achieve the necessary power up to 15 *MHz*. This is validated by demonstrating the reduction of harmonic distortions and parasitic DC effects within the amplifier output, as well as by demonstrating a constant level of pDEP force on oocysts of *C. parvum* in the 1 - 7 *MHz* range due to dominance of cytoplasmic conductivity.

### **Chapter 2**

### **On-Chip Impedance for Quantifying Parasitic Voltages During AC Electrokinetic Trapping**

#### 2.1 Introduction

Electrical fields are widely used within microfluidic devices to selectively polarize [26] and manipulate objects using dielectrophoresis (DEP) [2], such as biomolecules [27], nano-colloids [28], bacteria [29], mammalian cells [27], multi-cell aggregates [30] and aqueous droplet suspensions in oil [31, 32]. Since electrical fields are facile to integrate within microfluidic channels for enabling localized and label-free frequency-selective deflection of polarized particles from flow streamlines, they provide an alternative to acoustic [33] and fluidic [34] actuation. To prevent electric field-induced damage to the manipulated biological object due to electrolysis, electrode fouling, and pH gradient effects, the electrodes are often placed outside the sample channel region. Device configurations to achieve this include contactless dielectrophoresis (cDEP) [35], bipolar electrode DEP [36], passivated electrode DEP [37], electrowetting on dielectric [38] and droplet manipulation systems [39, 40]. In such cases, optimal field penetration occurs above a cut-off frequency, wherein the capacitor representing the insulating barrier allows for field passage, while capacitance and resistance in the sample and electrode channels can become important at higher frequencies. The parasitic voltage drops due to these circuit elements limit fraction of the applied voltage available for particle manipulation [41]. We present an on-chip impedance method to quantify these voltage drops during AC electrokinetic particle manipulation without the need to use valuable biological samples or model particles.

The level of field penetration and its frequency response determine the fraction of the applied voltage available for electrokinetic manipulation. This is influenced by the fidelity of the microfabricated geometry, such as barrier thickness, surface area and surface charge [42], and architecture of the Electrode and sample chambers. However, these factors that ultimately determine the impedance of the microfluidic device are often not well-controlled during device fabrication, assembly, and application. For instance, barrier thickness that is determined by the rotational rate used for polymer spin coating and barrier surface area that is determined by interlayer alignment overlap during lithography can exhibit significant variations ( $\pm 15\%$ ) [43, 44].

Furthermore, merely ensuring that the respective interfaces are hydrophilic is not sufficient to control the surface charge level and its distribution since materials, such as PDMS, exhibit timedependent hydrophobic recovery [45]. Current methods to quantify the efficacy and frequency response of AC electrokinetic manipulation are based on optical microscopy or electrical measurement of the deflection of model particles [46]. However, they are unable to quantify parasitic voltage drops, and the frequency region with model particles is different from that of target cells, such as tumor [9], immune [47], or stem cells [48]. There has been some prior work on impedance measurements to monitor electrophoretic mobility [49] and gauge electrical stimulation of tumor cells [50]. However, the measurements were carried out at low frequencies (~kHz range) and using bulky impedance analyzers rather than by on-chip monitoring. This limits the feedback ability to inform on-chip manipulation decisions. Since dielectrophoresis can enable selective deflection of cells over a wide frequency range (0.1 - 10 MHz), we explore on-chip impedance measurement for monitoring and controlling microfluidic manipulation. Our circuit methodology is capable of automated determination of the impedance frequency response of the microfluidic device under the same conditions used for particle manipulation, but without needing model particles. Through fitting impedance spectra to an equivalent circuit model, the resistance and capacitance values of each layer can assess variations to the microfabricated device geometry, such as width, surface area, and surface charge distribution of the insulating barrier and architecture of the sample and electrode channels. Based on this, the device geometry and stimulation conditions can be altered to maximize fraction of the applied voltage available for DEP manipulation and to temporally alter the separation characteristics.

#### **2.2 Contactless DEP Device Layer Stackup**

A cross-section view of the microfluidic chip for particle manipulation by contactless dielectrophoresis is shown in **Fig. 2-1a(ii)**, wherein the field is applied across the conductive electrode channels that contain high salt media (10x PBS of  $\sim 15 S/m$ ), and the field lines penetrate across each insulator barrier into the sample channel for the purpose of manipulating the micro- or nanoscale objects of interest within media of high salt (10x PBS of  $\sim 15 S/m$ ) or low salt (0.1x PBS of  $\sim 0.1 S/m$ ). This generalized microfluidic design can be adapted to other situations of electric field-induced manipulation [51]. **Fig. 2-1a(iii)** shows a generalized equivalent

circuit, with resistors and capacitors for each Electrode and sample chamber, alongside capacitance for each barrier. To quantify the impedance response of a microfluidic device under the applied AC voltage ( $V_S$ ) over a wide frequency range, as per the overall circuit diagram in **Fig. 2-1a(i)**, the voltage drop across a test resistor ( $R_t$ ) needs to be measured.

An example microfluidic chip is shown in **Fig. 2-1b**, which is obtained by aligning the insulating barrier interface of a sample channel (bottom) to two electrode-containing channels (top) on the left and right side, with the sample channel additionally containing insulating posts to create spatial field non-uniformities for dielectrophoretic particle manipulation.



**Fig. 2-1.** (a) (i) Simplified measurement circuit; (ii) cross-section view of microfluidic chip with Electrode and sample channels; (iii) generalized electrical equivalent circuit of chip; (b) Example microfluidic chip obtained by aligning the insulating barrier interface of a sample chamber (bottom) to two electrode-containing chambers (top) on the left and right side, with the sample chamber additionally containing insulating posts to create spatial field non-uniformities for dielectrophoretic particle manipulation

While we seek to ensure that much of the applied voltage is dropped across the sample channel  $(R_{ch})$ , Fig. 2-2 shows the device geometry-dependent parasitic capacitances  $(C_p \text{ and } C_e)$  and resistances  $(R_e)$  can limit the fraction of applied voltage available for dielectrophoretic manipulation.



Fig. 2-2. Geometry dependent parasitic capacitances and resistances for cFEP devices that affect the voltage fraction available for particle manipulation

#### 2.3 Impedance Measurement circuit

Rather than utilizing bulky commercial impedance analyzers that are restricted to low stimulation voltage (~1  $V_{pp}$ ) and inconvenient interfacing, we develop a circuit (Fig. 2-3a) that directly interfaces to the microfluidic device to measure impedance at the AC power levels and frequency ranges used for DEP manipulation (20  $V_{pp}$  over 1 kHz to 10 MHz).

**System Overview:** The user interface (MATLAB script) directly interfaces with the High Voltage AC Generator's main controller. Upon user request for impedance measurement, the relays disconnect the device from the high voltage ports (Stim) while connecting it to the Impedance circuit (**Fig. 2-3b**). During one round of impedance measurement, the frequency is swept from  $1 \ kHz$  to  $10 \ MHz$  at a series of pre-defined frequencies, equally spaced in a logarithmic scale (12 frequencies per decade).

For each frequency, the controller programs the "Signal Generator" unit to generate a low voltage sine signal of that frequency, which is amplified through two steps: the "Pre-amplifier" and the "Power Amplifier" units to achieve  $Vs = 20 V_{pp}$ , that better provides a test condition, resemble the actual test condition, compared to that of the conventional impedance analyzers ( $Vs = 1 V_{pp}$ ). The "Current to Voltage" unit converts the AC current through the chip to an AC voltage using a network of resistors, switches, and a wideband buffer. The typical output amplitude of this unit is

in the range of hundreds of milli-volts. After amplification in the "Amplifier" unit with a variable gain controlled by the controller, the amplitude of the AC voltage (Vo) and its phase difference with respect to the original applied voltage are calculated in the "Amplitude detection" and "Phase Measurement" units, followed by digitization, verification, and storage of results inside the controller.

The results are finally sent back to the software for post-processing to extract the circuit model parameters of each element of the chip, thereby determining the voltage fraction available for dielectrophoretic manipulation. Based on the automated impedance data fitting, the main controller controls the AC stimulation for temporal control of DEP manipulation.





Fig. 2-3. A Photo (a) and the schematic (b) of the impedance measurement circuit with the signal generator, microcontroller, and amplifier.

**Current to Voltage unit:** In order to measure the AC current (Iz) through the microfluidic device (Impedance load), it needs to be converted to a voltage equivalent signal (Vz). A test resistor can

basically do this conversion; However, due to the capacitive behavior of devices in low frequencies, the dynamic range of AC current is very wide from a fraction of micro-ampere (in low frequencies) to tens of micro-amperes in the megahertz range. Therefore, a single resistor doesn't practically work over a wide frequency range; Although it may produce a perfect AC voltage in mid-range frequencies (e.g.,  $100 \ kHz$ ), in higher frequencies, the AC voltage would be too high beyond the input range of the downstream amplifier. On the other hand, the AC voltage in lower frequencies (<  $10 \ KHz$ ) might be too weak, contaminated with noise/interferences. As a result, we use a network of several resistors ranging from 100 ohms to 1 M-ohm; each has a relay in series (**Fig. 2-4**). At any time, only one of these resistors is active while other resistors are disconnected by their corresponding relay. The controller automatically manages the relays' status, ensuring Vz to be in the allowed range. A wideband buffer (OPA656, Texas Instruments, TX) delivers the converted AC voltage to the following amplifier unit in the last stage. This offers an extremely low bias current (1 *pA*) for operation over a large bandwidth up to 230 *MHz*.



Fig. 2-4. The resistor-relay network converts the AC current to a voltage equivalent. The principal parasitic capacitances are denoted with red color.

Accounting for parasitic capacitances: One key factor to avoid or suppress interferences and unwanted oscillation in high-speed circuits is minimizing the current loop area, which causes parasitic inductances [52]. Therefore, having a solid ground plane under the signal routes on the PCB and shielding of the cables are necessary. However, the proximity of ground layers/shields to the signal lines introduces a substantial parasitic capacitance (CPCB). This parasitic capacitance is basically in parallel to the internal capacitance of the buffer's inverting terminal (CIN\_opamp). Another unignorable source of error is the contact-to-contact capacitance (Co) in open relays and the capacitance between the energizing coils and the contacts (Cc). Based on the reported measured

capacitances (~2 pF) on the datasheet [53], we have driven the full impedance model resistor network that is taken into account for error compensation and improving accuracy. All mentioned parasitic capacitances are graphically shown in **Fig. 2-4**. Simply put, the Current-to-Voltage unit is not a pure resistor element, but it's a complex RC model with the total impedance of  $Z_t$ . It not only becomes prominent at higher frequencies (~  $4^o$  phase error at 10 *MHz*), it may even distort both magnitude and phase in lower frequencies as well.

**Controlling amplifier gain flatness and phase shift:** Even with selecting (enabling) the optimum test resistor within the resistor network, the output of the Current-to-Voltage unit (Vz) still needs to reach an amplitude level close to the pre-amplifier's output ( $\sim 3.2 V_{pp}$ ). It will aid the Amplitude detection unit and Phase measurement unit to work more accurately. Therefore, the gain of the subsequent amplifier unit needs to have a variable gain stage. Hence, we have used VCA824 (Texas Instrument, TX) which has a 0.1 *dB* gain flatness up to 100 *MHz* and voltage-controlled gain capability. By choosing proper Input/feedback resistors, the maximum gain of the variable amplifier was limited to 10. Another fixed gain stage (OPA656, Texas Instruments, TX) was also added to boost the overall gain to 20.

Operational amplifiers do not have an ideal flat gain response range and sometimes show considerable phase lag in the MHz frequency. Therefore, we have calculated the cumulative gain and phase profile used for data calibration in the post-processing stage.

Accurate amplitude detection: The standard approach for measuring the amplitude of a sinusoidal signal is by capturing its peak and representing it as the amplitude. Rather than using classic peak detectors [54] that include a non-negligible error (~0.5V), we use comparator-based detectors with a current booster, in which a fast comparator with a propagation time less than 7 *ns* is used to charge the storage capacitor to the level that is as close as possible to the real peak voltage, by continuously comparing these two voltage levels [55]. Fig. 2-5 shows a simplified schematic of our wideband peak detector. Here, the red-colored circuitry upgrades the classic peak detector (black-colored) to the wideband peak detector. In short, the amplifier (Gain = G) acts as an additional current source ( $I_2$ ) for the capacitor (C) in a way that the sum of  $I_1$  and  $I_2$  is relatively a constant value ( $I_c$ ), independent of the capacitor voltage ( $V_c$ )



Fig. 2-5. The simplified schematic of the wideband peak detector. The red-colored circuitry boosts the capacitor charging current

Accurate phase measurement: The purpose of this unit is to determine the phase difference between the amplified sine signal (representing the AC current) and the applied sine voltage, which is the output of the pre-amplifier unit.

One mathematical approach is to multiply the sine signals together using an analog multiplier. The result is simply the summation of two components as **Eq. (2-1)**: The DC component that includes the phase information ( $\cos \phi$ ) can be extracted by applying an averaging (low-pass) filter.

$$A_{1}\cos(\omega t) + A_{2}\cos(\omega t + \phi) = \underbrace{\frac{1}{2}A_{1}A_{2}\cos(\phi)}_{DC} + \underbrace{\frac{1}{2}A_{1}A_{2}\sin(2\omega t + \phi)}_{AC}$$
(2-1)

This approach looks simple in theory. However, it becomes problematic in practice because we cannot measure the amplitude A1 and A2 without error, thereby affecting the calculated phase. Another problem is that analog multipliers, even the fast ones like AD835 (Analog devices, MA), do not show a flat frequency response in the high-frequency ranges (> 1 *MHz*) which is another source of error after the multiplication. Meanwhile, analog multipliers have a limited input voltage level range (e.g.,  $|V_{in}| < 1$ ); As a result, this approach is impractical because sometimes the applied voltage requires passing through an attenuation stage, thereby adding another source of error for the amplitude/phase of this channel.

We use the more precise and robust approach based on comparing the signals after converting them to digital streams by using fast comparators. For this, we use the phase measurement unit of a phase-lock-loop (PLL) circuit and then apply an averaging filter to achieve more accurate results, as shown in **Fig. 2-6a**. The comparator (MAX9000, Maxim Integrated, CA) and PLL phase detector (MAX9382, Maxim Integrated, CA) are selected from the ECL logic family, which offers unique performance and accuracy within high-speed applications (> 1 *MHz*). **Fig. 2-6b** shows the Phase measurement performance for three different frequencies and phases, wherein the signals were plotted in colors similar to the color of probing points in **Fig. 2-6a**.



**Fig. 2-6.** (a) The block diagram of the Phase measurement unit that receives two sinusoid inputs: Va and Vo. (b) The resulting pulses at the output of the PLL phase detector and final DC voltage levels representing the phase difference for three different frequencies/phase shifts.

If the input AC signals have mismatched amplitudes or include parasitic DC level, the output pulses would be shifted by a phase due to the hysteresis feature implemented in the comparators. We need to estimate the amount of this error ( $\varphi_2$ -  $\varphi_1$ ) geometrically and take it into our final calculation, based on the measured amplitudes, DC levels, and pre-defined hysteresis voltage threshold (*hys* = 30 *mV*). **Fig. 2-7** shows the sources of phase errors for two in-phase input signals in two scenarios: (a) different amplitudes without parasitic DC, and (b) The amplitudes are the same, but one input has an additional DC level. Assuming that the hysteresis threshold is considerably smaller than the amplitudes (*hys*  $\ll A, B$ ), we can estimate the phase errors for these

scenarios as Eq. (2-2) and Eq. (2-3).

$$\Delta \phi_{1 \to 2} = hys \times \left(\frac{1}{B} - \frac{1}{A}\right) \ radian \qquad for \ scenario \ (a) \tag{2-2}$$

$$\Delta \phi_{1 \to 2} = \frac{DC_A - D_{CB}}{A} = \frac{D}{A} radian \qquad for scenario (b) \tag{2-3}$$



**Fig. 2-7.** The non-zero thresholding causes an error in measuring the phase between input sinusoid signals. (a) Different amplitudes, zero DC shift. (b) similar amplitudes, but one signal has a DC offset.

**Table 2-1** lists the main specifications of the Impedance measurement circuit, designed as part of CytoRecovery<sup>™</sup> product.

Parameter	Specification	Validation
Board dimensions	2.75" × 6"	
Input power	10 watts <sup>a</sup>	
Interface	USB 2.0 <sup>b</sup>	
Frequency range	1 kHz – 10 MHz	
Frequency resolution	0.1 kHz	
Test signal	10 V (7 V <sub>RMS</sub> )	
Phase resolution	0.1 °	
Freq. Sweep points	49 °	
Sweep time	90 sec. (typical)	
Z  accuracy	< 2%	walidated by HP 4192A LCR meter, using standard capacitors and resistors
Phase accuracy	$<\pm$ 0.5 °	
Capacitance under test	0.2 pF – 20 pF	
Resistance under test	$3 \text{ k}\Omega - 100 \text{ M}\Omega$	

Table 2-1 The specification of Cyto Holder (Impedance measurement circuit)

<sup>a,b</sup> Provided by Cyto main unit (HV generator); <sup>c</sup> 12 pts per decade in logarithmic scale

#### 2.4 Mathematical analysis of impedance and Voltage Fraction functions

In the next sections, the impedance measurement approach is used with the appropriate equivalent circuit model (*Section 2.4.1*) to assess the geometry and the parasitic voltages in devices with varying levels of misalignment and sample channel architecture (*Section 2.5*). Based on this, a criterion called "voltage fraction" for DEP manipulation is determined from the impedance frequency response after accounting for the parasitic voltage drops, and this is correlated to the determined levels of DEP trapping (*Section 2.6*) so that the device geometry can be optimized to maximize trapping (*Section 2.4.2*).

#### 2.4.1 Equivalent circuit simulations

The equivalent circuit of a cDEP device shown in Fig. 2-1a(iii) comprises three individual components related to the barriers, sample channel, and electrode channels that are in series with each other. Hence, we can write the total impedance ( $Z(\omega)$ ) by adding the corresponding impedances of these units.

$$\mathbf{Z}(\boldsymbol{\omega}) = -\frac{j}{C_b \boldsymbol{\omega}} + \frac{R_{ch}}{1 + j\boldsymbol{\omega} R_{ch}C_p} + \frac{R_e}{1 + j\boldsymbol{\omega} R_eC_e}$$
(2-4)

Looking at Eq. (2-4), the denominators of the terms in  $Z(\omega)$ , shows one pole at  $\omega = 0$  and two non-zero poles at the cut-off frequencies of  $\omega_1$  and  $\omega_2$ :

$$\omega_1 = 2\pi f_1 = \frac{1}{R_{ch}C_p} \tag{1-5}$$

$$\omega_2 = 2\pi f_2 = \frac{1}{R_e C_e} \tag{2-6}$$

Using Eq. (2-5) and Eq. (2-6) and knowing that  $\omega = 2\pi f$ , we can rewrite Eq. (2-4) to better show the variation of  $Z(\omega)$  as a function of  $\omega$ :

$$Z(f) = -\frac{j}{2\pi f C_b} + \frac{R_{ch}}{1 + j\frac{f}{f_1}} + \frac{R_e}{1 + j\frac{f}{f_2}}$$
(2-7)

To better explain the observed impedance responses, simulations of the possible equivalent circuits of **Fig. 2-1a(iii)** are presented under three simplifications (**Fig. 2-8a(i)-(iii)**).



**Fig. 2-8.** (a) Equivalent circuit simplifications; (i): in absence; versus (ii): in the presence of parasitic capacitance of sample channel,  $C_p$ ; and (iii): complete model including all parasitic components. The simulated frequency response of (b) impedance magnitude along with inflections at cut-off frequencies, (c) impedance phase, and (d) voltage fraction of applied voltage and its maximum value ( $\alpha$ ) that is available for electrokinetic manipulation are shown.

In circuit (i), the impedance response is chiefly determined by the net capacitance of the barriers  $(C_b)$  and resistance of the sample channel  $(R_{ch})$ , wherein dielectrophoretic manipulation occurs within media of low conductivity (~0.1x PBS), while the high conductivity media used in the electrode channels (10x PBS) ensures minimal impedance contribution due to resistance in electrode channel  $(R_e)$ . In this case, assuming  $C_b$  of ~5 pF and  $R_{ch}$  of ~500 k $\Omega$ , we expect that

the real component of the impedance will start at a stable level at low frequencies that is determined by  $R_{ch}$  and drops off at high frequencies. The response of the impedance magnitude (**Fig. 2-8b(i**)) linearly drops at a slope corresponding to the inverse of  $C_b$ , and the dispersion shows a single cutoff frequency ( $f_0 = 1/[2\pi R_{ch}C_b]$ ) corresponding to electric field penetration through  $C_b$ . The impedance phase (**Fig. 2-8c(i**)) transitions away from a capacitor response of -90° to -45° at the cut-off frequency.

To have a better sense of parasitic voltage drops, the fraction of applied voltage that is dropped across the sample channel to cause DEP at each frequency is computed as "voltage fraction" in **Fig. 2-8d(i)**.

$$Voltage \ Fraction = \frac{Voltage \ across \ the \ sample \ channel}{Voltage \ across \ the \ device}$$
(2-8)

At low frequencies, the voltage fraction is low since the high impedance due to dominance of  $C_b$  causes a majority of the applied voltage to be dropped across the barrier, with a dispersion towards the voltage fraction of 1 beyond the cut-off frequency ( $f_0$ ). However, equivalent circuit (i) fails to accurately capture the higher frequency dispersion beyond the first cut-off frequency ( $f_0$ ), which we attribute to parasitic capacitance in the sample channel ( $C_p$ ) that occurs in parallel to  $R_{ch}$  in the sample channel (**Fig. 2-2**), as per equivalent circuit (ii). This additional capacitance ( $C_p$ ) causes a second cut-off frequency ( $f_1$ ), as per the dispersion of |Z| in **Fig. 2-8b(ii)** that linearly drops at a corresponding slope, while the impedance phase exhibits another inflection towards -90° due to the capacitive behavior (**Fig. 2-8c(ii**)). In the case of the voltage fraction (**Fig. 2-8d(ii**)), rather than approaching a voltage fraction of 1, the maximum value ( $\alpha$ ) is limited to less than unity by a factor determined by: ( $C_b/[C_b + C_p]$ ). Finally, there is the case wherein input impedances in the electrode channel due to the lead-in parasitic resistance ( $R_e$ ) and capacitance ( $C_e$ ) can become important. In this case, we expect to see another high-frequency dispersion in |Z| in **Fig. 2-8b(iii)** corresponding to the cut-off frequency:  $f_2$ , which will cause a high-frequency drop-off in the voltage fraction (**Fig. 2-8d(iii**)).
# 2.4.2 "Voltage Fraction" function

To derive the "Voltage Fraction" function, we use the common voltage division rule by first calculating the ratio of sample channel impedance  $(Z_{ch}(f))$  to the total impedance (Z(f)) defined in Eq. (2-7).

$$\frac{Z_{ch}(f)}{Z(f)} = \frac{\frac{R_{ch}}{1+j\frac{f}{f_1}}}{\frac{-j}{2\pi f C_b} + \frac{R_{ch}}{1+j\frac{f}{f_1}} + \frac{R_e}{1+j\frac{f}{f_2}}} = \frac{1}{1+\frac{f_0}{f_1} - j\frac{f_0}{f} + \frac{R_e}{R_{ch}} \times \frac{1+j\frac{f}{f_1}}{1+j\frac{f}{f_2}}}$$
(2-9)

For lower frequencies ( $f \ll f_2$ ), the term  $(1 + j\frac{f}{f_2})$  in the denominator of Eq. (2-9) is close to 1. We have used this simplification in driving the "Voltage Fraction" function (*Fraction*(f)) as Eq. (2-10).

$$Fraction(f) = \left| \frac{Z_{ch}(f)}{Z(f)} \right| \approx \left| \frac{1}{1 + \frac{C_p}{C_b} - j\frac{f_0}{f} + \frac{R_e}{R_{ch}}(1 + j\frac{f}{f_1})} \right|$$

$$\approx \frac{1}{\sqrt{\left(1 + \frac{C_p}{C_b} + \frac{R_e}{R_{ch}}\right)^2 + \left(\frac{R_e}{R_{ch}}\left(\frac{f}{f_1}\right) - \frac{f_0}{f}\right)^2}} \quad for \quad f \ll f_2$$

$$(2-10)$$

In the most comprehensive model (iii), wherein  $C_p$  and  $Z_e$  are significant, the voltage fraction plot exhibits a local maximum named  $\alpha$  at the frequency  $(f_p)$ . At this frequency, the second term inside the radical sign in **Eq. (2-10)** becomes zero.

$$\frac{R_e}{R_{ch}} \left(\frac{f_p}{f_1}\right) - \frac{f_0}{f_p} = 0 \quad \rightarrow \quad f_p = \sqrt{\frac{f_0 f_1 R_{ch}}{R_e}} = \frac{1}{2\pi} \sqrt{\frac{1}{R_e R_{ch} C_b C_p}} \tag{2-11}$$

$$Fraction(\omega_p) = \alpha = \frac{1}{(1 + \frac{C_p}{C_b} + \frac{R_e}{R_{ch}})}$$
(2-12)

At frequencies beyond  $f_p$ , the "Voltage Fraction" plot declines to a finite non-zero value ( $R_1$ ) that only depends on capacitive components of the model:

$$R_1 = \frac{1}{1 + \frac{C_p}{C_b} + \frac{C_p}{C_e}}$$
(2-13)

For the simplest model (i), wherein parasitic capacitances in the sample channel  $(C_p)$  and impedances in the electrode channel  $(Z_e)$  are zero; the voltage fraction reaches a 70% value at the first cut-off frequency  $(f_0)$ . While the maximum voltage fraction reaches 100% for the simplest model (i), it shows a reduction by the amount of  $R_2 = C_p/(C_b + C_p)$  for the case of the model (ii), to yield a maximum voltage fraction:  $\alpha' = C_b/(C_b + C_p)$ ; at higher frequencies with no local maximum. Since circuit models (ii) & (iii) include parasitic impedances, the corresponding voltage fraction shows drops that are solely determined by the parameter:  $\alpha$ . Fig. 2-9b shows the variation of voltage fraction versus frequency for the circuit models (i-iii) that were shown in Fig. 2-8a.



**Fig. 2-9**. (a) Plot of voltage fraction versus frequency for each circuit model (Fig. 2-2a: (i), (ii) & (iii)). (b) Influence of varying device parameters (that alter *R* and *C* values for each device layer) on the frequency response of voltage faction available for DEP trapping ( $\alpha$ (*frequency*)). Arrow indicates an increase in respective parameters.

#### **Optimization to minimize parasitic voltage during DEP**

Next, we use the maximum voltage fraction level ( $\alpha$ ) determined from the impedance spectra to assess the critical level required for pDEP trapping. This can be utilized to optimize device geometries so that a maximum fraction of applied voltage is available for pDEP (or minimum parasitic voltage drops) over a wide frequency range. Starting with the primary plot of **Fig. 2-9b** (black curve for a standard well-aligned device), in order to create a wide frequency window for effective cDEP manipulation, devices with geometries that enable higher  $C_b$  and  $R_{ch}$  are required, as well as geometries that lower  $C_p$ ,  $R_e$ , and  $C_e$ , are preferred. This can be achieved by (1) enhancing the overlap area between the electrode and sample channels, as well as reducing the width of the insulating barrier to increase  $C_b$ ; (2) lengthening the sample channel in the direction of the electric field (or widening it based on top view) to increase  $R_{ch}$ ; and (3) widening the electrode channels and reducing their length to reduce  $R_e$ , especially in comparison to  $R_{ch}$ .

# 2.4.3 Computation of "Voltage Fraction" function based on the Circuit-model

In this section, the measured impedance responses on microfluidic devices of differing device geometry are fit using appropriate circuit models (Fig. 2-8a(ii-iii)) to obtain R and C values for each device layer. In this manner, device geometry variations can be determined, and parasitic voltage drops can be quantified based on the maximum level of voltage fraction or  $\alpha$  (Fig. 2-2d), which is then correlated to DEP levels.

The total impedance function Z(f) in Eq. (2-9) has three poles: f = 0,  $f_1$ ,  $f_2$  and two zeros at  $\omega_0$ and  $\omega_3$  as shown in Fig. 2-10. At frequencies far below  $\omega_1$  ( $f \ll f_1$ ) Eq. Error! Reference source not found. can be approximated to Eq. (2-9).

$$Z(\mathbf{f}) \cong -\frac{j}{2\pi C_b \mathbf{f}} + R_{ch} + R_e \quad for \quad \mathbf{f} \ll f_1 \tag{2}$$

The first term of Eq. (2-9) is dominant in very low frequencies ( $f \ll f_0$ ); Therefore, |Z(f)| has an oblique asymptote of  $Z(f) = 1/(2\pi C_b f)$  on a log-log scale as denoted in Error! Reference source not found. Hence, the capacitance  $C_b$  can be calculated as





Fig. 2-10 The plot of impedance magnitude:  $|Z(\omega)|$  on a log-log scale

To find other components of the equivalent circuit model, we first need to compute  $Real(Z(\omega))$  function using the impedance magnitude and phase datapoints:  $Real(Z(f)) = |Z(f)| cos(2\pi f))$ . Referring to Eq. (2-4), the real part of Z(f) is calculated as Eq. (2-16), that is the addition of channels' frequency-dependent resistances.

$$Real\left(\mathbf{Z}(\mathbf{f})\right) = Real\left(\mathbf{Z}_{ch}(\mathbf{f})\right) + Real\left(\mathbf{Z}_{e}(\boldsymbol{\omega})\right) = \frac{R_{ch}}{1 + \left(\frac{f}{f_{1}}\right)^{2}} + \frac{R_{e}}{1 + \left(\frac{f}{f_{2}}\right)^{2}}$$
(4)

If the value of  $f_1$  is known, we could find the values of  $R_{ch}$  and  $R_e$  from the Eq. (2-17) and Eq. (2-18) and finally, compute the channel impedance  $(Z_{ch})$ .

 $Real\{\mathbf{Z}(f)\}\ at\ low\ frequencies \cong R_{ch} + R_e$ (5)

$$Real\{\mathbf{Z}(f_1)\} = \frac{R_{ch}}{1 + \underbrace{\left(\frac{f_1}{f_1}\right)^2}_{=1}} + \frac{R_e}{1 + \underbrace{\left(\frac{f_1}{f_2}\right)^2}_{<0.1}} \cong \frac{R_{ch}}{2} + R_e$$
(6)

In simplification of Eq. (6), we have assumed  $f_2 > 3f_1$ , that is normally valid.

#### Accurate computation method for $\omega_1$

If  $R_{ch}$  is greater than  $R_e$ , which is usually the case, the maximum negative slope (or inflection point) in  $Real(\mathbf{Z}(f))$  plot occurs close to  $f_1$ , as shown in Fig. 2-11. Our calculation shows that if  $R_{ch} > 4R_e$ , the inflection point frequency  $(f_{ip})$  deviates from  $f_1$  by less than 10%, regardless of the value of  $f_2$ . Fig. 2-11 confirms small variations of  $f_{ip}$  with respect to  $f_1$  for a set of  $R_{ch}/R_e$ ratios over one-decade frequency span.



**Fig. 2-11** (a) the first derivative of Real(Z(f)) respect to the normalized frequency  $(f/f_1)$ . (b) the relative error in choosing  $f_{ip}$  (as the representative of  $f_1$ ), for different ratios of  $f_2/f_1$  and  $R_{ch}/R_e$ .

The impedance measurement should include a series of closely spaced frequency points (at least ~10 points/decade) to have a sufficiently smooth plot for Real(Z(f)) plot. It will enable us to efficiently employ the numerical derivation method and compute the first derivative of Real(Z(f)). The local minimum of this derivate plot would occur at  $f_{ip}$ , which is approximately equal to  $f_1$ .

To find  $f_2$ , we should first generate the real part of the electrode channel's impedance  $Real(Z_e(f))$ , by subtracting  $Real(Z_{ch}(f))$  from the total measured real impedance, as formulated in Eq. Error! Reference source not found.. Then, we can use Eq. (2-20) to find the frequency  $f_2$ .

$$Real\{\mathbf{Z}_{e}(f)\} = \underbrace{Real(\mathbf{Z}(f))}_{Measured \ data} - \underbrace{\frac{R_{ch}}{1 + \left(\frac{f}{f_{1}}\right)^{2}}}_{Generated \ Function, \\ knowing \ R_{ch} \ and \ \omega_{1}} \equiv \frac{R_{e}}{1 + \left(\frac{f}{f_{2}}\right)^{2}}$$
(2-19)

$$Real\{\mathbf{Z}_{e}(\omega_{2})\} = \frac{R_{e}}{1 + \left(\frac{f_{2}}{f_{2}}\right)^{2}} = \frac{R_{e}}{2}$$
(2-20)

Now that we determined  $R_{ch}$ ,  $R_e$ ,  $f_1$  and  $f_2$ , we can find the capacitance of both electrode and sample channels using Eq. (1-5) and Eq. (2-6).

#### Approximate estimation method for determining $\omega_1$

Another method to find the circuit model parameters is examining Real(Z(f)) plot on the log-log scale. As shown in **Fig. 2-12**, the plot would show two distinct dispersion regions; corresponding to the Sample channel and Electrode channels' R-C models. The first step here is approximating the magnitude of  $R_e$ , by searching for an inflection point between two dispersion regions. Usually, this point lies in the mid-way of the third piece in the piece-wise approximation of Real(Z(f)) plot. Next, the magnitude of  $R_{ch}$  can be calculated from **Eq. (5**). Finally, the location of  $\omega_1$  and  $\omega_2$  can be found using **Eq. (2-18)** and **Eq. (2-20)**. **Error! Reference source not found.** illustrates how this method works.



Fig. 2-12 The piece-wise approximation of  $Real\{Z(f)\}$  to find the key frequencies and resistive parameters.

While Z(f) has a significant magnitude in very low frequencies, its phase so close to  $-90^{\circ}$ , resulting in a finite magnitude for  $Real(Z(f)) = |Z|\cos(\phi)$ . The multiplier  $cos(\theta)$  is very sensitive around  $\theta = \pm 90^{\circ}$ , meaning that the computed Real(Z(f)) might be too noisy (jagged

trend) in low frequencies due to small phase measurement errors. Nevertheless, this irregularity usually diminishes as the frequency increases and more accurate estimation of  $(R_{ch} + R_e)$  is achievable in the mid-way frequencies below  $f_1$ .

#### 2.5 Impedance response on optimized micro-device

In order to ensure that the maximum fraction of applied voltage is available for electrokinetic manipulation over a wide frequency bandwidth, we need to optimize the device configuration as follows: (1) higher  $C_b$  (> 2 pF) to enable low enough  $f_0$  (tens of kHz range), since pDEP responses of cells can become significant above this frequency level; (2) lower  $C_p$  (~0.2 pF) compared to  $C_b$  to ensure minimum reduction in voltage fraction from unity beyond  $f_1$ ; (3) smaller  $R_e$  compared to  $R_{ch}$ , so that  $f_2$  is pushed to high enough frequencies wherein DEP responses cannot be initiated (> 100 *MHz*). To enable this, we microfabricated PDMS devices with the following configuration: (i) a thin insulating barrier (~10  $\mu$ m) and high depth (~50  $\mu$ m) to enable  $C_b$  of 5 pF or greater; and (ii) an electrode channel of small length (~300  $\mu$ m) and large width (50  $\mu$ m) to cause smaller  $R_e$  in comparison to  $R_{ch}$ .



Fig. 2-13. Frequency response of microfluidic device fabricated to high-fidelity at a geometry that ensures an enhanced bandwidth and voltage fraction for electrokinetic manipulation, as determined from (a) impedance magnitude; (b) impedance phase; (c) real portion of impedance, and (d) voltage fraction available for DEP

manipulation.

With the electrode channels maintained at high salt (10x PBS at 15 S/m) to reduce input impedance, Fig. 2-13 shows the impedance responses of such an optimized micro-device for two situations in the sample channel: (i) with media of low salt (0.1x PBS at 0.15 S/m) to simulate DEP conditions; (ii) with media of high salt (10x PBS at 15 S/m) to reduce the influence of  $R_{ch}$ and enhance the effect of  $C_b$  on the net impedance. It is apparent that low salt media in the sample channel is preferable since the cut-off frequency for 70% field penetration through the barrier  $(f_0)$ occurs at well below  $f_{0L} = 100 \ kHz$ , thereby providing a broader frequency window for DEP manipulation of particles, whereas  $f_0$  occurs only at  $f_{0H} = 600 \ kHz$  under high salt conditions, thereby limiting the frequency window for DEP manipulation. Similarly, the voltage fraction that determines the potential drop in the sample channel reaches a limiting value in Fig. 2-13d at an earlier frequency  $(f_{1L} \sim 1 MHz)$  for sample channel at low salt versus at higher frequencies  $(f_{1L} \sim 8.3 MHz)$  under high salt conditions. However, differences in  $C_b$  due to alterations in barrier width, interfacial charge, or channel depth can be picked out more easily under high salt conditions in the sample channel, based on the  $f_0$  value. It is also noteworthy that non-linearity in measured capacitance versus applied voltage to upshift the impedance frequency response (Fig. 2-14c) is more apparent under high salt conditions in sample and electrode channels. Similarly, variations in electrode channel and sample channel geometry would alter the respective parasitic impedances to affect the steady-state voltage fraction value.



**Fig. 2-14.** Non-linear effect of applied voltage on measured barrier capacitance (a) in the  $2 - 20 V_{pp}$  range due to non-uniform distribution of charge around the barrier (b) that shifts in the frequency response of voltage fraction in high salt and low salt media (c). Minimal shifts occur at  $V_{applied} > 20 V_{pp}$ .

## 2.6 Correlating parasitic voltage drop to DEP trapping

Next, we present how the voltage fraction determined from this impedance approach, which reflects the level and frequency response of parasitic voltage drops during electrokinetic manipulation, can predict DEP levels. For this purpose, we consider devices with common microfabrication variations, such as (1) misaligned layers; or (2) channel dimension alterations due to light exposure differences between adjacent layers across device depth.



**Fig. 2-15.** Devices with well-aligned (a) versus misaligned (c) layers of Electrode (orange) to sample channels (blue) leads to higher field intensity at well-aligned sample channels (flow from top to bottom) that enables strong DEP trapping of cells (b), whereas lower field intensity at misaligned channels causes pearl chaining of cells (d). Correlating  $\alpha$  value at each frequency to level of DEP trapping:  $\alpha > 0.5$  causes strong DEP (one cell per post),  $\alpha = 0.2$ -0.4 causes pearl chaining around post; and  $\alpha < 0.2$  causes no DEP trapping (e).

In each case, we validate the utility of the maximum voltage fraction ( $\alpha$ ) obtained from impedance measurements in predicting the level and frequency response of pDEP trapping (**Fig. 2-15e**). Considering aligned (**Fig. 2-15a**) versus misaligned devices (**Fig. 2-15c**), there is an alteration in field intensity due to the distribution of field lines in the sample channel. Hence, while the higher field intensity at well-aligned sample channels leads to strong DEP trapping, as apparent from the trapping single-cells per insulating post (**Fig. 2-15b**), the lower field intensity in devices with small angular misalignments leads to "pearl chaining" (**Fig. 2-15d**), since field interaction of cells at the posts is unable to overcome cell-cell dipole interactions.

The degree of misalignment-induced errors and its influence on parasitic voltages can be discerned based on impedance responses since the barrier capacitance on one side is altered versus the other side due to misalignment. Since capacitances added in series are dominated by the lower capacitance, the net capacitance of this device is lowered versus the well-aligned device. For the misaligned device of **Fig. 2-16a**, the  $f_0$  is shifted to higher frequencies (**Fig. 2-16 b-c**) versus that of the impedance plots for the well-aligned device in **Fig. 2-3**. In fact, the impedance response of the misaligned device filled with low salt media in the sample channel resembles that observed for well-aligned devices at high salt (**Fig. 2-16 b-c**), highlighting its inability for effective DEP manipulation in the sub-MHz range.



**Fig. 2-16.** (a) Lithography and exposure errors due to interlayer misalignment alter the barrier capacitance  $(C_b)$ . (b) The impedance frequency response of the misaligned device versus a well-aligned device with low and high salt levels. (c) determining the corresponding voltage fraction available for DEP manipulation, compared to the well-aligned device.

Considering devices with channel dimension alterations, such as narrowing of the sample channel (**Fig. 2-17a**), the lower electrical length in field direction causes  $R_{ch}$  to become comparable to  $R_e$ . Hence, even though the well-aligned device layers show a barrier capacitance of 3.5 *pF* that is conducive to DEP manipulation beyond 100 *kHz* (**Fig. 2-17b**), the voltage fraction available for DEP manipulation drops off at high frequencies (**Fig. 2-17c**), rather than reaching a steady-state level close to unity. It is noteworthy that these measured impedance responses (**Fig. 2-17 b-c**) resemble the simulated responses in **Fig. 8b(iii) and Fig. 2d(iii)**, highlighting the validity of the circuit model in **Fig. 2-8a(iii)** to this particular device geometry.



Fig. 2-17. (a) An altered cDEP device with a narrow sample channel that reduced channel resistance  $(R_{ch})$ . (b) obtaining the barrier capacitance from the impedance frequency response. (c) determining the voltage fraction (maximum at  $\alpha$ ) available for DEP manipulation, at the frequency range where  $\alpha$  exceeds 0.5

Based on such impedance analysis, we extract the relevant circuit parameters that are summarized in **Table 2-2** so that the fitted *R* and *C* values can quantify the parasitic voltages, while the frequency response can identify the particular device geometry responsible for this voltage drop. For instance, misalignment of the sample channel to electrode channels can significantly decrease the barrier capacitance ( $C_b$ ) from 5 *pF* to 0.35 *pF* so that the parasitic voltage drops reduce the voltage fraction available for DEP trapping. On the other hand, light exposure-related channel width alterations that narrow the sample channel can cause a reduction in sample channel resistance ( $R_{ch}$ ) from 470 k $\Omega$  to 250 k $\Omega$ , so that the parasitic voltage causes a high-frequency drop-off in voltage fraction available for DEP trapping (**Fig. 2-17c**).

Device Type	Aligned <sup>a</sup> (per Fig. 2-1b)		Misaligned <sup>b</sup> (per Fig. 2-6b)	Narrow <sup>c</sup> (per Fig. 2-6d)
$\sigma$ (media)	15 S/m	0.1 S/m	0.1 S/m	0.1 S/m
$f_o$	600 kHz	74 kHz	No dispersion	160 kHz
$f_1$	8.3 MHz	0.95 MHz	No dispersion	0.4 MHz
$f_2$	No dispersion		No dispersion	7.7 MHz
$C_b$	4.7 pF	5 pF	0.35 pF	3.5 pF
$R_{ch}$	63 KΩ	470 ΚΩ	450 KΩ	250 KΩ
$C_p$	0.3 pF	0.35 pF	0.5 pF	1.6 pF
$R_e$	~1 KΩ	30 KΩ	30 KΩ	33 KΩ
$\overline{C}_{e}$	0.2 pF	0.2 pF	0.25 pF	0.6 pF
Max a	90%	90%	~63%	~20%

Table 2-2 fitted circuit parameters from impedance responses of devices

<sup>a</sup> Aligned & wide sample channel; <sup>b</sup> Misaligned; <sup>c</sup> Narrow sample channel.

In Fig. 2-18, we validate the use of the parameter:  $\alpha$ , obtained from the impedance spectra to predict DEP trapping characteristics within four distinct device types: I. Wide sample channel (Fig. 2-1b), II. narrow sample channel (Fig. 2-17a), and two single-layer devices microfabricated to different depths, so that barrier capacitance ( $C_b$ ) is varied in III and IV. The frequency at which the  $\alpha$  value just exceeds 0.5 (i.e., < 50% parasitic voltage drop) is plotted on the X-axis versus the frequency for the onset of strong DEP trapping on the left Y-axis for the same device (error bars are based on three runs per device). Based on a near-unity slope (0.95) and an R<sup>2</sup> regression value of 0.96, we infer that the impedance sensor can effectively predict the DEP trapping ability based on this criterion. The plot on the right-side Y-axis in Fig. 2-18 (square symbols) shows that the frequencies used for the validation (circle symbols) were obtained at similar  $\alpha$  values (0.5 – 0.6) for each device, confirming that the comparisons across devices were performed at equivalent trapping levels.



**Fig. 2-18** The frequency at which  $\alpha$  just exceeds 0.5 (< 50% parasitic voltage drop on X-axis) can be used to predict the frequency for the onset of strong DEP trapping (Y-axis) based on the linear plot (circle symbols) for four device types: I. Wide sample channel (per Fig. 2-1b), II. narrow sample channel (per Fig. 2-6d), and two single-layer devices microfabricated to different depths, so that barrier capacitance ( $C_b$ ) is varied in III and IV.

For the standard contactless dielectrophoresis device, our specific inferences are: (1) the insulating barrier between the electrode and sample channels should be of low width (~10  $\mu$ m) and high depth ( $\geq 50 \mu$ m), which can be assessed based on a high barrier capacitance (3 – 5 *pF*) for enabling high field penetration onwards from low cut-off frequencies (~50 *kHz*); (2) the fraction of applied voltage that is available for AC electrokinetic manipulation is limited by the parasitic

capacitance  $(C_p)$  in the sample channel, and parasitic resistance in the electrode channel  $(R_e)$ , which can be lowered by increasing electrical length along sample channel (to reduce  $C_p$  and increase  $R_{ch}$ ) and widening the electrode channel (to reduce  $R_e$ ); (3) microfabrication variations, such as interlayer channel width or misalignment can be assessed by fitting impedance responses to equivalent circuit parameters to determine *R* and *C* values for each layer to quantify the altered device geometry.

#### 2.7 Conclusion

We present an on-chip impedance sensor capable of assessing the level and frequency response of parasitic voltage drops during AC electrokinetic trapping in microfluidic devices, which can be used to maximize the voltage fraction available for DEP trapping. To enable sensitive impedance measurement, the circuit includes a high-gain amplifier with 0.1 dB gain flatness up to 100 MHz, followed by a wideband peak detector that utilizes a fast comparator to accurately detect the amplitude of the measured signal. Meanwhile, phase can be detected by converting signals to digital streams and measuring the phase shift using a PLL phase detector. We show that the impedance response can be used to assess the fidelity of the device geometry and to optimize its architecture for ensuring that a maximum fraction of the applied voltage is available for electrokinetic manipulation. Finally, we validate the use of the maximum voltage fraction ( $\alpha$ ) and the critical frequency at which  $\alpha$  exceeds 0.5 (< 50% parasitic voltage drops) obtained from the impedance spectra to predict pDEP trapping characteristics using four different device types. In all cases,  $\alpha \ge 0.5$  was required for optimal pDEP trapping (single cell per field non-uniformity), with pearl chaining for  $\alpha$  in the 0.2 – 0.5 range and no pDEP trapping for  $\alpha$  < 0.2. Given the ability for on-chip impedance spectral measurements that enables rapid feedback of the measurement to the AC generator on the same circuit board, we envision the application of this method towards rapidly informing downstream decisions on DEP manipulation. While the current study is focused on the impedance-based assessment of microfluidic devices designed for contactless dielectrophoresis, we envision that this principle can be applied towards other microfluidic structures that are designed for other forms of electrokinetic manipulation, as well as for manipulation under acoustic or inertial force fields.

# **Chapter 3**

# Real-time detection and control of resonance frequency in acoustic trapping systems by monitoring of amplifier supply currents

# **3.1 Introduction**

Selective trapping and deflection of particles under acoustic force fields in a fluidic channel [56] is a versatile platform for non-destructive [57, 58] and non-contact manipulation of cells in biological samples [59-61]. It is facile to set up within a microfluidic channel and has been demonstrated for a wide variety of particle types, including vesicles [62, 63], lipoproteins[64], bacteria [65, 66], circulating tumor cells [67] and cell aggregates [68]. Acoustic trapping is achieved by selective particle transport to the acoustic standing wave node or antinode, depending on the acoustic contrast of the particle versus the medium (as determined by the mass density, compressibility, and size of particles) [69]. Given the opportunities it presents for particle separation from heterogeneous samples, acoustophoresis is poised to impact the fields of sample preparation [70], cell micropatterning [71], 3D printing [72, 73], nanomaterial synthesis [74], and cell phenotypic elucidation [75].

The most common configurations use an underlying piezoelectric transducer to set up bulk acoustic waves within a microchannel [76] so that the resulting standing wave can spatially localize particles at distinct positions along the channel width under resonance conditions [77], with orthogonal flow used to remove other particles. However, maintenance of precise and stable acoustic trapping over several minutes is often challenging [78], due to the high sensitivity of the resonance frequency on tolerances in microchannel geometry, environmental variations (e.g., media conditions due to temperature), and drift arising from variations in the system load during trapping. Additionally, most realistic biological sample preparation workflows require wash steps [79] and buffer switches [80], altering the resonance frequency for particle trapping. Hence, a method to enable real-time identification of the resonance frequency for feedback to actively modulate the trapping conditions in response to these variations would greatly simplify the workflow and versatility of acoustophoresis.

The design of microchannel widths to support an integer multiple of the wavelength of the sound

wave can be used to set the resonance frequency, but variations in actuator mounting and its coupling to the microchannel can lead to alterations in a resonance frequency that must be experimentally determined for each device geometry under relevant voltage and buffer conditions. This is usually accomplished via particle image velocimetry [81], temperature and media control [82], interferometry [83], or suspended microprobes [84], but these methods cannot automatically tune the applied frequency to resonance conditions. Since the electrical impedance of the system should reach its minimum at the resonance condition, such measurements can be applied to accurately determine and control the resonance frequency [85, 86]. However, in spite of the correlation of the electrical admittance to the resonance frequency in water-filled layered resonator devices [87], the impedance spectrum can include resonance peaks that arise from bulk resonances that overwhelm those arising from microchannel resonance [82]. In spite of this shortcoming, a number of prior studies have refined the utilization of electrical impedance measurements to identify the optimal trapping frequency [88] by coupling to a variety of theoretical simulations to decouple the channel-related resonances [77]. Most recently, differential impedance analysis using distilled water and 20% CsCl perfused in the microchannel were used to determine the peak related to the microchannel resonance frequency using the metric of the absolute value of the complex impedance difference that is normalized to the absolute value of the impedance spectrum of the water-filled channel [89]. While this metric was validated for resonance frequency determination using a variety of device materials and designs, it was applied solely to identify the initial resonance frequency, and its application on the device platform towards real-time frequency tracking to detect dynamic changes under drift or buffer swaps has not been explored.



**Fig. 3-1** (a) A simplified schematic of the circuit with a signal generator and amplifier for current-based monitoring of the resonance frequency. (b) The microfluidic chip attached to syringe pumps at each reservoir for trapping at the indicated site. (c) Schematic of particle migration and trapping under an acoustic force field (sperm cells at low-pressure nodes) for separation from smaller debris (epithelial cell lysate) under the drag force due to flow.

Samples under acoustic differential extraction (ADE) can vary dramatically in their makeup, containing anywhere from thousands to hundreds of thousands of cells. This wide range of possible samples means that the optimal acoustic trapping frequency will change on a sample-to-sample basis, which could have a devastating impact: it has been shown that a deviation of as little as 0.05 *MHz* from the ideal trapping frequency can result in a 10-fold loss of trapping efficiency [88]. As it impacts ADE, this would mean that if the applied acoustic frequency is not regulated for each sample, the majority of the target cells could be lost.

To realize this objective, we introduce a novel approach that not only performs the real-time frequency tracking during signal stimulation but it can also maximize the trapping efficiency by maintaining the stimulation power level. Rather than monitoring the stimulation amplitude across the piezo transducer, which will encounter bandwidth limitations to accurate amplitude measurement in the MHz range, our novel circuit indirectly monitor the output AC current (*Ip*) based on the averaged value of power supply currents into the amplifier ( $\overline{I_s}$ ) as shown in Fig. 3-1a. Since  $\overline{I_s}$  can be easily measured using conventional multimeters or DC circuits, with no need for a wideband peak detector, the resonance frequency can be detected as the point at which  $\overline{I_s}$ reaches its maximum level. To enable easy access for  $\overline{I_s}$  measurements, we integrate the AC stimulation, amplifier, and current measurement, all into a portable circuit that can eventually be easily scaled to enable independent measurement and control of multiple microfluidic channels, each possibly undergoing different acoustic trapping operations in parallel. The circuit design and implementation are described in Section 3.5 and validated using a microchannel design (Fig. 3-**1b**) in *Section 3.7* to confirm the maintenance of acoustic trapping of beads simultaneously with high sensitivity resonance frequency measurement during the wash and buffer switch steps (Section 3.8.1). Finally, the circuit is applied for selective trapping of sperm cells in a heterogeneous sample containing epithelial cell lysate (Fig. 3-1c) to enable male DNA quantification via quantitative polymerase chain reaction (qPCR), which amplifies male DNA (Section 3.8.2).

#### **3.2 Acoustic cell trapping theory**

Acoustic cell manipulation techniques employ standing acoustic waves generated within a resonant cavity to move or capture particles and/or cells as they pass through the channel. The primary axial radiation force ( $F_r$ ) dictates particle movement, causing them to aggregate at low-pressure nodes due to their acoustic contrast with the surrounding medium, with larger particles experiencing a stronger primary acoustic radiation force[90], as described in Eq. (3-1).

$$F_r = \left(\frac{\pi \,\rho_0^2 \, V_c \,\beta_w}{2\lambda}\right) \cdot \phi(\beta,\rho) \sin\left(2kx\right) \tag{3-1}$$

Where  $\rho_0$  is the applied acoustic pressure amplitude,  $V_c$  is the volume of the particle (i.e., size),  $\lambda$  is the wavelength of applied sound, k is the wavenumber defined by  $2\pi/\lambda$ , x is the distance from a pressure node,  $\rho_c$  and  $\beta_c$  are the density and compressibility of a particle, respectively, in a fluid with density  $\rho_w$  and compressibility  $\beta_w$ , and  $\phi$  is the acoustic contrast factor and is given by:

$$\phi = \frac{5\rho_c - 2\rho_w}{2\rho_c + \rho_w} - \frac{\beta_c}{\beta_w}$$
(3-2)

This axial force acts in the direction of propagation of the acoustic wave field and is responsible for the movement of the particles and/or cells to the nodes or anti-nodes of the wave (see Fig. 3-1c). As evident from the equations above, the axial radiation force is highly dependent on the size and shape of the particle as well, where a decrease in size results in a decrease of the acoustic force. On the other hand, the flow of fluid causes a drag force ( $F_d$ ) which linearly depends on the radius of particles, according to Stokes' law [91]:

$$F_d = 6\pi\mu R v \tag{3-3}$$

Where  $\mu$  is the dynamic viscosity, *R* is the radius of the spherical particle, and *v* is the flow velocity relative to the particle. For example, if radius decreases by half, radiation force decreases by factor of 8 while drag force decreases by factor of 2. Therefore, larger particles (target cells, e.g., sperm cells) aggregates on nodes ( $F_r > F_d$ ), while smaller particles (non-target cells or debris) pass

through the channel without getting trapped ( $F_r < F_d$ ).

In addition to the  $F_r$ , there is also the scattering of acoustic waves by other particles, causing particles to be attracted to or repulsed from one another. Although these inter-particle forces are much weaker than the  $F_r$ , they are significant when attempting to aggregate and sediment cells [92, 93]. Moreover, the dependence of the acoustic factor on the density ( $\rho_w$ ) and compressibility ( $\beta_w$ ) of the fluid surrounding the cells. This indicates that strict attention be paid to the solutions/buffers used during a trapping event.

#### 3.3 Voltage-mode approach

In order to accurately monitor resonance frequency variations in real-time for feedback to control stimulation conditions, the state-of-the-art solution utilizes a standard peak detector circuit to continuously monitor variations in the amplitude of the stimulation voltage signal across the piezoelectric transducer [88, 94]. The frequency corresponds to the minimum amplitude is the resonance frequency of the system. This approach, referred to as the Voltage-mode approach, exploits the non-zero internal resistances ( $Ro \approx 50 \Omega$ ) at the commercial amplifiers' output that is comparable to the piezo impedance at the resonance frequency.

While these voltage-based detection approaches are able to accurately determine the resonance frequency under relevant sample conditions, they suffer from two major drawbacks:

#### 3.3.1 Peak detector: errors and complexity

Most piezoelectric transducers operate over a wide range (1 - 10 MHz), but the design and implementation of a wideband peak detector for operation over the ~MHz range can be challenging [95]. The classic peak detector is a relatively simple circuit with a few components. However, its performance degrades at higher frequencies [96], especially for larger input amplitudes required for strong trapping. Adding a wideband voltage divider at the input to scale down the signal would improve the accuracy of measurement. However, it degrades the ability to detect the minimum voltage since the peak detector error is considerably high (~0.3 to 0.4V) and varies with input amplitude. Another novel circuit for peak detection is based on a super-fast comparator IC and charger current booster [55] (see Section 2.3). However, while its output error (DC output – actual

peak) is sufficiently low (<  $\sim 40 \text{ mV}$ ) over a wide range of frequencies (up to 10 *MHz*) and input amplitudes ( $\sim 0.1 V_{pp}$  to 6  $V_{pp}$ ), it continues to require a wideband voltage divider. Fig. 3-2 shows the variation of absolute error (mV) over the megahertz range at the output of both peak detector designs range for several input amplitudes.



**Fig. 3-2** The absolute error (mV) over 1 to 10 MHz frequency range for several input amplitudes (Peak-to-Peak), for (a) Improved Classic Peak detector, and (b) Wideband Comparator-based Peak detector with Current booster

#### **3.3.2 Sensitivity against Acoustic Power**

Consider a non-ideal amplifier as a combination of an ideal one  $(V_{out} = V_s)$  with an output resistance  $(R_o)$  as shown in **Fig. 3-3** Using the voltage division between  $R_o$  and  $Z_{Piezo}$ , the amplitude of AC signal across piezo  $(V_p)$  is:

$$V_p = V_s \left( \frac{|Z_{Piezo}|}{|Z_{Piezo} + R_o|} \right)$$
(3-4)

Eq. (3-4) shows that the voltage across the piezo transducer  $(V_p)$  is always smaller than Vs. As the frequency approaches the resonance frequency, the impedance becomes mostly resistive in its minimum magnitude  $(Z_p)$ . Therefore, the amplitude  $V_p$  will reach a minimum as well, according

to Eq. (3-4).



Fig. 3-3 A non-ideal amplifier (Ro  $\neq 0$ ) that stimulate a piezoelectric transducer with Ac signal  $V_p$ 

By taking the differential from both sides of Eq. (3-4),

$$dV_p = V_s \left(\frac{R_o}{\left(Z_p + R_o\right)^2}\right) dZ_p$$
(3-5)

By dividing both sides of Eq. (3-5) by the corresponding sides in Eq. (3-4) and simplification:

$$\frac{dV_p}{V_p} = \frac{dZ_p}{Z_p} \left( \frac{R_o}{Z_p + R_o} \right) = \frac{dZ_p}{Z_p} \left( 1 - \frac{V_p}{V_s} \right)$$
(3-6)

$$\frac{\% \,\Delta V_p}{\% \,\Delta Z_p} = \left(1 - \frac{V_p}{V_s}\right) = \alpha \tag{3-7}$$

The measurement sensitivity for the resonance frequency is determined by the ratio of the change in Vp to the change in impedance magnitude around the resonance frequency (Zp), as given by Eq. (3-7). Hence, higher measurement sensitivity (high  $\alpha$ ) to enable improved detection of changes in Zp based on measurement of Vp, requires larger voltage drop across  $R_o$  so that less voltage is available for stimulation of the piezo transducer. Since the delivered energy depends sharply on this stimulation voltage ( $\propto V_p^2$ ), the trapping force will be significantly diminished, which becomes particularly apparent under conditions of flow or drift.

#### **3.4 Current-mode Approach**

To address this issue, let's consider monitoring the current drawn from the amplifier stimulating the piezo transducer rather than on the voltage drop across the load resistor.

According to Fig. 3-3, we can express the amplifier's output current as Eq. (3-8).

$$I_p = V_s \left(\frac{1}{Z_P + R_o}\right) \tag{3-8}$$

Similar to Eq. (3-5) and Eq. (3-6), we can compute the measurement sensitivity ( $\beta$ ) based on current ( $I_p$ ) to the change in impedance magnitude around the resonance frequency ( $Z_p$ ):

$$\frac{dI_p}{I_p} = \frac{-dZ_p}{Z_p} \left( \frac{Z_p}{Z_p + R_o} \right) = \frac{dZ_p}{Z_p} \left( \frac{-V_p}{V_s} \right)$$
(3-9)

$$\frac{\% \,\Delta I_p}{\% \,\Delta Z_p} = \left(-\frac{V_p}{V_s}\right) = \beta \tag{3-10}$$

According to Eq. (3-10), the sensitivity ( $\beta$ ) can be maximized by making  $R_0$  as small as possible, to lead to the condition of:  $V_p \approx V_s$ . Hence, both sensitivity and magnitude of  $V_p$  can be maintained independent of each other, thereby ensuring that the need for high measurement sensitivity does not lower the voltage delivered to the piezo transducer. Nevertheless, Measuring the amplifier's output AC current is not a straightforward task, particularly in the Megahertz frequencies. The conventional method uses a trans-impedance amplifier with a test resistor in the feedback to convert the current signal to voltage signal, followed by a post-amplifier and finally a peak detector (**Fig. 3-7**). Apart from the complexity of implementation, the nonlinearities in the post-amplifiers and the peak detector would degrade measurement accuracy.



Fig. 3-4 An example for the implementation of AC current measurement unit

To bypass this complexity, one alternative way to measure the output AC current  $(I_p)$  is to monitor the variation of power supply currents into the amplifier. The input terminals of the amplifiers practically draw near-zero current from the input source. Hence, according to Kirchhoff's Current Law (KCL),  $I_p$  can be expressed as the summation of two supply currents (Is + and Is -) entering into the respective amplifier supply pins. **Fig. 3-8** shows these currents on an amplifier symbol and plots them versus time. If no load is connected to the amplifier (*Iout* = 0), the magnitude of both supply currents is the steady value of  $I_{s0}$ . This value, by itself, is dependent on output amplitude (*Vs*) and the working frequency. If a load is connected (*Iout*  $\neq$  0), the supply currents are no longer DC values, but they take the shape of a half-wave rectified AC signal that includes either positive or negative cycles. An outward current (*Iout* > 0) is fully provided through the positive supply current (*Is* +). Therefore *Is* + strictly follows the positive cycles of *Iout* with a DC offset of + $I_{s0}$  while the negative supply current will supply an inward output current in the same way. In other words, the active cycles in positive (*IS* +) and Negative (*Is* -) supply currents alternate with each other.



Fig. 3-5 The variation of supply currents (IS + and IS –), Output amplitude (Vs), and current (Iout) of an amplifier versus time

Unlike the output AC current, which is oscillating around zero, the supply currents are bounded between  $I_{s0}$  and  $(I_{s0} + I_p)$ . Hence, the supply currents have non-zero averages that can be obtained by calculating the integral of its waveform over one period as **Eq. (3-11)**. It shows that the averaged value of supply currents  $(\overline{I_s})$  can represent the amplitude of output AC current  $(I_p)$ . Therefore, by monitoring the averaged supply current  $(\overline{I_s})$  and finding its maximum value, the resonance frequency can be determined at any time point, based on the conditions in each microchannel.

$$\overline{I_S} = \frac{1}{T} \int_0^T I_S \, dt = I_{S0} + \frac{1}{T} \int_0^{\frac{1}{2}} I_P \sin\left(\frac{2\pi}{T}t\right) dt = I_{S0} + \frac{I_P}{\pi}$$
(3-11)

#### **3.5 Circuit Implementation**

The "Current-mode" approach requires direct access to the supply pins of the amplifier that is not possible for most commercial/enclosed amplifiers. Additionally, their output impedance is comparable with the resonance impedance of typical piezo transducers used for acoustic trapping (tens of ohm range). Hence, we custom designed the amplifier for direct access to the supply pins and for providing sufficient current to a piezo load (at least 0.2A) while having a relatively low output resistance (~4 ohms) to minimize voltage waste.

#### 3.5.1 Custom Amplifier design

Several criteria should be taken into account when it comes to selecting the right components for the implementation of a custom amplifier.

1) The amplifier needs to be able to generate an output swing as large as 20  $V_{pp}$ . It requires a dual power supply with symmetrical voltage levels of at least  $\pm 12V$  or preferably  $\pm 15V$ .

2) At the resonance frequency of a piezoelectric transducer, the impedance magnitude reaches a minimum value while becoming more resistive than reactive. A smaller impedance value leads to a higher AC current drawn from the amplifier. For the specific Piezo type used in our acoustic trapping system, the piezo impedance is around 70  $\Omega$ . Therefore, for a stimulation voltage of 20  $V_{pp}$  ( $V_p = 10V$ ), the AC current has a peak amplitude of approximately 140 mA that should be handled easily by the amplifier system.

3) The amplifier's large-signal bandwidth needs to be high enough to provide a flat frequency response up to 9 - 10 MHz for high voltage output.

4) The high output current capability would also necessitate a precise control on the power dissipation inside the amplifier. The total power dissipation (PD) can be expressed as the difference between the amount of power from the power supply (through Vcc and Vee terminals) into the amplifier and the delivered power to the impedance load ( $P_{Load}$ ) as Eq. (3-12).

$$P_D = P_{supply} - P_{Load} = 2V_{cc} \left( I_{S0} + \frac{I_P}{\pi} \right) - \frac{1}{2} V_p I_p \cos\theta$$
(3-12)

Where  $I_{S0}$  is the DC component of supply current known as quiescent current and  $I_p$  is the amplitude of output AC current. In the second term, the parameter  $\theta$  is the phase shift between the AC voltage and AC current at the output. For a capacitive load,  $\theta$  is around 90 degrees in frequencies away from the resonance point. However, this angle for a resistive load (at resonance) is close to 0. By substituting the working parameters of our experiments (Vcc = 15V,  $I_p = 140 \text{ mA}$ ,  $V_p = 10V$  and  $\theta = 0$ ) into Eq. (3-13), a simplified expression for calculation of dissipated power is obtained:

$$P_D = 2V_{cc} \left( I_{S0} + \frac{I_P}{\pi} - \frac{V_p I_p}{4 \, V cc} \, \widetilde{cos0} \right) \cong 30^V (I_{S0} + 21^{mA})$$
(3-13)

Eq. (3-13) reveals that the DC quiescent current is also a critical factor in minimizing the power dissipation. However, apart from the Dc dissipation, the small impedance of load would dissipate more than  $\sim 600 mW$  (= 30 × 21) heat inside the amplifier that only a few single amplifiers could tolerate.

If one is interested in implementing the custom amplifier with a single amplifier module (i.e., Operational Amplifier or Op-Amp), Apex's amplifier products could be a promising candidate. PA107DP is undoubtedly the best when it comes to providing all criteria mentioned above. It can operate with high supply voltage levels (up to  $\pm 100V$ ), 1.5A output current capability, and maximum dissipated heat of 62W with Heatsink. However, the minimum gain by which this amplifier can work properly (with stability) is 20. Knowing that its gain Bandwidth (GBW) product is 180 *MHz*, the amplifier bandwidth becomes 9 *MHz*. It means we would lose 50% of power at this frequency (equal to 70% of output voltage) that is close to the working frequency in our experiment (~ 7.5 to 8 *MHz*). Therefore, the selected amplifier needs to be stable in low gain values so that a more generous portion of its bandwidth is suitable for large signal amplification. Among thousands of commercially available Op-Amps in the market, we nominated three Op-Amps: LM7171, LM7372, and THS4631, all from Texas Instrument, TX. **Table 3-1** summarizes the relevant features of these amplifiers.

Parameter	THS4631	LM7171	LM7372
Minimum Gain (Av)	2	2	2
Slew rate (V/µS)	1000	4100	3000
Gain Bandwidth Product (MHz)	210	200	120
Supply Current (mA)	11.5	6.5	13
Iout max (mA)	98	118	150
Package	8-SO	8-DIP	16-SOIC
PD max at 25C (W)	2.3*	1.1	2.6*
#Circuits in a package	1	1	2

 Table 3-1 Comparison of three wideband operational amplifiers as candidates for the output stage of the custom amplifier

<sup>\*</sup> If soldered to PCB with copper planes

Despite having a good power rating, the other features of THS4631 Op-Amp are the worst among this group, including the highest supply current, lowest output current, and lowest slew rate. The other amplifier ICs (LM7171 and LM7372) are comparable in several features. LM7372 offers a higher output current, but LM7171 has more power bandwidth. Based on **Eq. (3-13)**, the maximum power dissipation will be around 850 mW (assuming  $I_{s0} = 6.5mA$ ). Both Op-Amp candidates promise to tolerate this dissipation power. Nevertheless, this is not the whole story. According to the LM7171 datasheet, for the load impedance as low as 100  $\Omega$ , the maximum achievable output amplitude is around 14  $V_{pp}$  in lower frequencies that ends up to 10  $V_{pp}$  at 10 MHz, yielding only ~50mA output current (**Fig. 3-6a**). Therefore, a single amplifier cannot practically provide the nominal output current stated in the datasheet (118mA), while the amplifier's power bandwidth will be reduced too. Nevertheless, if the load has higher resistance, such as 700  $\Omega$ , the output voltage amplitude of 20  $V_{pp}$  with little distortion (< 1%) at 8 MHz is possible [97] (**Fig. 3-6b**).



Fig. 3-6 Undistorted output swing for (a)  $RL = 100 \Omega$ , and (b)  $RL = 700 \Omega$  in LM7171 operational amplifier

Hence, as a solution, an array of parallelized amplifiers (**Fig. 3-7b**) is needed so that each amplifier IC (called: sub-amplifier module) contributes by providing a fraction of the overall output current. For this application, eight identical Op-Amps (LM7171) were selected with the package type of DIP-8 (Dual in-line Package, eight pins) because they have better thermal resistance compared to smaller surface-mount counterparts (e.g., SOIC-8). Moreover, to have better thermal management, these eight ICs are directly attached to the corners of two low-profile rectangular heatsinks. The inputs and outputs of all sub-amplifiers are tied together in this parallel arrangement.

Nevertheless, the output signals are not identical due to the intrinsic tolerances in the fabrication

of ICs and resistors. Therefore, a small resistor (33  $\Omega$ ) at each amplifier's output provides isolation and prevents the over-current issue. These small protection resistors make an effective resistance of 4  $\Omega$  (= 33/8) at the whole amplifier system's output.

The non-inverting feedback in each sub-amplifier is Av = 2.5, preserving the excellent power bandwidth of the LM7171 amplifiers. All sub-amplifiers' outputs have the same phase and amplitude with high accuracy, thanks to the high precision feedback resistors (0.1%). Each subamplifier is responsible for providing ~18 mA (= 140/8) of output current around the resonance frequency. Following Eq. (3-13), this AC current results in a dissipated power of ~275mW inside each IC that does not raise their body temperature significantly. It is worth mentioning that using the heatsinks was not strictly necessary, but they prevent the ICs from becoming hot.



Fig. 3-7 The details of circuits for the custom amplifier and current-meter units

#### 3.5.2 Current-meter unit

A custom amplifier allows full access to all internal terminals/nodes of the system, including the supply pins. The maximum averaged current ( $\overline{I_s} max$ ) into our custom amplifier is around 100 mA, according to Eq. (3-14).

$$\overline{I_S} \max = 8 \times I_{S0} + \frac{I_P}{\pi} \cong 8 \times 6.5^{mA} + \frac{140^{mA}}{\pi} \cong 100^{mA}$$
(3-14)

To measure the averaged current  $(\overline{I_s})$  into the amplifier, a small test resistor  $(RT = 0.25 \Omega)$  was

added in series within the positive supply line to produce a voltage equivalent ( $V_{RT}$ ) of supply current (**Fig. 3-7b**). Hence, the maximum of this voltage drop would be around ~25mV that is negligible compared to Vcc (+15V), thereby not affecting the amplifier's performance. Here, the easiest and more accurate way to measure  $V_{RT}$  is using a high precision current-sense amplifier like MAX44284F (Maxim Integrated, CA). This IC amplifies the input differential voltage with a fixed gain of 50. Very low input bias current (max: 80 nA) ensures no wasted/leaked current during current to voltage conversion. Moreover, this IC can reject the common-mode DC voltage on its input terminals (+15V) operating with only a lower voltage (+5V) single supply. The Megahertz ripple on the supply current is far beyond this amplifier's sensible bandwidth (~ 3 kHz). Nevertheless, a low-pass filter ( $f_{3db} \sim 1 kHz$ ) has been added at the input terminals, mainly to suppress the transient noise/interferences. The current-meter unit output is a DC voltage that varies from ~0.65V to 1.2V, representing the amplifier's momentary averaged supply current.



# 3.5.3 Single-board Acoustic Trapping circuit

Fig. 3-8 (a) The block diagram and (b) a photo of the whole Acoustic trapping controller circuit

The custom amplifier and current-meter are two of the main units of the Acoustic trapping circuit, designed and built on a single PCB to accomplish automated signal stimulation and frequency tracking (**Fig. 3-8**). **The microcontroller** (PIC16F887, Microchip) is the circuit commander, which constantly reads the analog DC voltage from the Current-meter unit and tunning the **signal generator unit.** It comprises a Direct Digital Synthesis IC (AD9851, Analog Device) that

generates frequencies from 7 *MHz* to 10 *MHz* with an amplitude of 1  $V_{pp}$ . This signal is scaled up to eight-fold by the **Pre-Amplifier unit** that is fed into the custom high current amplifier. A variable gain amplifier (VCA824, Texas Instrument) inside the pre-amplifier unit allows the user to control the stimulation voltage from 0 to 20  $V_{pp}$  based on the amount of acoustic force that is needed in a variety of sample types, piezo sensors, and chip designs. The **Peak Detector** is an optional unit that can measure the stimulation voltage amplitude, but it does not contribute to the detection of the resonance frequency or to automated frequency tracking.

 Table 3-1 lists the main specifications of the Acoustic trapping circuit for the Impedance

 measurement circuit, designed to replace the earlier electronics inside the SONIC system

Parameter	Specification	Validation	
Board dimensions	5" × 6"		
Input power	10 watts <sup>a</sup>		
Input voltage (DC)	10 – 36 volts		
Interface	USB 2.0		
Frequency range	$7 \text{ MHz} - 10 \text{ MHz} {}^{\text{b}}$		
Frequency resolution	1 kHz		
Stimulation amplitude	10 V (7 V <sub>RMS</sub> )		
Current measurement resolution	0.2 mA		
Frequency tracking cycle			
Iteration time step	Min: 0.1 sec.		
Cycle time	Min: 0.5 sec.		
Output current	Max: 400 mA (AC peak)	validated by electrical	
Piezo capacitance	Max: 500 pF @ 10 MHz	measurement (Tektronix	
Minimum piezo impedance	Min: ~ 50 ohm	MDO3024), using selected	
_	@ resonance frequency	standard RLC impedance models	

Table 3-1 The specification of the Acoustic trapping controller circuit

<sup>a</sup> Stand-by power consumption; <sup>b</sup> Internally limited in the firmware

# 3.6 Real-time detection of resonance frequency to control stimulation:

Finding the resonance frequency of the piezoelectric transducer mainly includes a single preliminary frequency sweep throughout a wide frequency range ( $f_1$  to  $f_2$ ) and a sequence of continuous local (narrow range) sweeps around the latest found resonance frequency. Fig. 3-9 Illustrates the basics flowchart of this procedure. The left box inside this figure shows sweep parameters that the user can change during the frequency tracking operations. The dashed arrows indicate the relationships among the sweep parameters and the instructions.



Fig. 3-9 The simplified flowchart of the instruction for real-time tracking of the resonance frequency

Fig. 3-10 illustrates the sequence of steps toward real-time tracking of the resonance frequency, implemented as part of the Microcontroller software. The procedure starts with finding the initial resonance frequency of the system by sweeping the frequency between two pre-defined values of  $f_1$  (default: 7.7 *MHz*) and  $f_2$  (default: 8.2 *MHz*), with the frequency step of  $\Delta f$  (default: 20 *kHz* for the resonance frequency of the current transducer chip at ~8 *MHz*). Sweep Speed is another parameter, controlled by the time interval (*Tp*, default: 0.2 sec) for which the circuit pauses at each frequency point.

For each frequency point, the averaged supply current  $(\overline{I_S})$  is monitored by the microcontroller. At the end of the preliminary sweep, the initial resonance frequency  $(f_R)$  is detected based on the maximum value among all  $\overline{I_S}$  values. Following this, a series of consecutive local sweeps are executed to track and update the momentary resonance frequency. The local sweeps include only three frequency points of  $f_R - \Delta f$ ,  $f_R$  and  $f_R + \Delta f$ .

Since the stimulation frequency is always locked to the momentary resonance frequency of the system, any drift in resonance frequency over the course of acoustic trapping can be detected and controlled to maintain trapping.



Fig. 3-10 The sequence of steps toward real-time tracking of the resonance frequency

**Fig. 3-11** shows the variation of output current and voltage amplitude during one course Preliminary Sweep (Zoomed View) for both Voltage-mode (a) and Current-mode approaches (b). In the Voltage-mode, output amplitude drops significantly (below  $10 V_{pp}$ ) around the resonance frequency, causing less effective Acoustic trapping. On the other hand, the amount of amplitude drop in the Current-mode approach is substantially low ( $18 V_{pp}$ ), and the maximum current determines the resonance frequency.



**Fig. 3-11** The zoomed view of detailed preliminary sweeps around the resonance frequency for two approaches: (a) Voltage-mode and (b) Current-mode. The frequency step was 2 kHz with a stay time of 0.1 sec at each frequency point. The blue plots are Output amplitudes (*Vs*) against the left y-axis and, the red plots are Supply currents (*Is*) against the right y-axis. The Up-Down dotted lines indicate when the frequency hopped to the next frequency point.

#### **3.7 Experimental Methods**

Device fabrication is achieved by laser cutting the channel design into a thin (~280  $\mu$ m) sheet of polydimethylsiloxane (PDMS) (Stockwell Elastomeric Inc, PA) sandwiched between two pieces of microscope cover glass (Thermo Fischer Scientific, MA) bonded using solvent bonding and plasma oxidation. The bead, sample, and washing buffer reservoirs are created by laser cutting 3 mm (poly)methyl methacrylate (PMMA) (McMaster-Carr, IL) and attached to the glass chip using pressure-sensitive adhesive (Adhesives Research Inc, PA). The piezo transducer (PZT) has the characteristic frequency of 7 *MHz* is ~2mm (w) x 4 mm (L) x 1 mm (d) in size. This small size allowed it to be shifted from being part of the instrument and bonded to the chip (**Fig. 3-12a**). With this PZT, ultrasonic standing waves are established around 8.1 *MHz* with three nodal planes.

**Fig. 3-12b** shows the printed chip interface manifold; this is the area where the chips are loaded for each run. After loading, the clamping manifold is closed (hinged movement) and locked in place, positioning the camera lens right above the trapping site to visualize the acoustically trapped cluster. The camera is connected to a Raspberry Pi single-board computer that directly transfers video data to PC. **Fig. 3-12c** schematically presents this setup for particle flow from the right side (arrow) to set off particle trapping under acoustic stimulation from the underlying piezo transducer.

Per **Fig. 3-12d**, three syringe pumps attached to different reservoirs move fluid through the chip at flow rates of 45  $\mu$ L and 100  $\mu$ L for sample trapping and elution, respectively. The first reservoir (R1) is used to transport 6  $\mu$ m yellow beads (Fluoresbrite) to the trapping site as a marker for the initial local frequency sweep to determine the resonance frequency based on chip geometry. The second reservoir (R2) contains the sample of sperm cells mixed with epithelial cell lysate, both from anonymous donors. The third reservoir (R3) contains a buffer to wash the trapped sperm cells to remove any extraneous epithelial cellular material. Initially, a local frequency sweep is done to determine the approximate resonance frequency. Yellow beads are routed via pneumatic valving to the waste reservoir (R6). The local frequency sweep is then used to inform another local sweep, and the feedback mechanism of the circuit board is activated as the sample is traversing the trapping site. Sperm cells are trapped and held together in the trapping site so that the female epithelial debris can be routed into another reservoir (R5) for quantifying the female fraction. The buffer is then passed over the sperm cluster for washing, and sperm cells are released into reservoir R4 for downstream processing by nucleic acid analysis.



**Fig. 3-12** (a) The miniaturized piezo transducer, bonded below the trapping site (b) SONIC instrument: the manifold is open before loading a microfluidic chip. Chip mounted beneath rubber o-ring, which provides the connection to syringe pumps and valving (c) PDMS Channel geometry and trapping site with respect to the piezo transducer (d) The microfluidic chip attached to syringe pumps at each reservoir for trapping at the indicated site.

This mechanical structure with the pneumatic fluid controller is part of the SONIC instrument system, designed by Prof. Landers' group, Department of Chemistry, University of Virginia.

# 3.8 Results

# **3.8.1** Real-time control of acoustic trapping under wash and buffer switch conditions

Utilizing the setup in **Fig. 3-12c**, we compare the ability of this novel current monitoring mode (**Fig. 3-8**) to the previously reported voltage monitoring methods to enable the maintenance and control of acoustic trapping in real-time under wash and buffer switch conditions. To maintain the experimental conditions for both methods as close as possible, we have implemented a feature in the board to quickly convert the board to a voltage-monitoring circuit to imitate the behavior of Voltage-approach systems. Herein, an external resistance (50 ohms) is temporarily added to the

output of our custom amplifier, and the frequency tracking process relies on the measured voltage by a wideband peak detector. In both scenarios, we stimulate the piezo transducer with a nominal 13  $V_{pp}$  signal (measured far from the resonance frequency).

While resonance frequency tracking under current mode is able to continuously grow the trapped site to a larger cluster size over the measured 70 s period (**Fig. 3-13a**), the growth in cluster size plateaus under the voltage mode, after reaching a balance between the weaker acoustic radiation force and drag force (**Fig. 3-13b**). To quantitatively compare the size of trapped clusters in both methods, we calculated the area of clusters using ImageJ software (developed by NIH) for one frame per second, as plotted in **Fig. 3-13c**. This figure shows that while the trapped cluster areas for both methods are comparable until  $t \sim 40 s$ , the current mode method finally yields roughly twice as much as that of the voltage mode.



**Fig. 3-13** The trapping of beads (6  $\mu$ m) over ~70 seconds under a stimulation voltage of 13 V in (a) current mode versus (b) voltage mode. (c) Cluster growth over time, quantified by calculating cluster areas. (d) The corresponding resonance frequency shift over time for both methods

Under real-time control to correct for drift of the resonance frequency due to the increasing size of

the trapped cluster, both methods initially show a downward trend in the resonance frequency. However, the current mode smoothly continues this downward trend until the end of trapping time (**Fig. 3-13d - Red**), whereas the resonance frequency reaches a saturation level (**Fig. 3-13d - Blue**).

It is also apparent that disruptions to the resonance frequency for particle trapping under a simulated wash step, by doubling of the flow rate after 20 seconds of trapping, can be accounted in real-time to maintain trapping using the current mode (Fig. 3-14b); but the same causes dissipation of the trapping under voltage mode (Fig. 3-14a). The trends of resonance frequency shift for both methods are also shown in Fig 14c., confirming the robustness of the current mode compared to the voltage mode method. Furthermore, this figure shows that the current mode method, even with less stimulation level (10  $V_{pp}$ ), is still more efficient than the voltage mode with the stimulation of 13  $V_{pp}$ .



**Fig. 3-14** Simulation of flow conditions in microchannel by doubling of flow rate (30  $\mu$ L/min to 60  $\mu$ L/min) after 60 s of trapping shows the maintenance of trapping under current mode (a) and its dissipation under voltage mode (b). The corresponding resonance frequency shift over time for both methods (c)

Finally, disruptions to the resonance frequency for particle trapping under a buffer switch by using 10% glycerol can be accounted real-time to maintain trapping using the current mode (**Fig. 3-15a**); but the same causes disruption of the trapped cluster into smaller clusters under voltage mode (**Fig. 3-15b**). The impact of buffer change on the resonance frequency plots is interesting as well. As expected, the current mode method that maintains the trapped cluster continues the downward drift in resonance frequency (**Fig. 3-15c - red**). In contrast, dispersing the trapped cluster after buffer change ( $t \sim 40s$ ) causes an upward turn in the plot for voltage mode (**Fig. 3-15c - blue**).



**Fig. 3-15** Simulation of a buffer switch after 40 s of bead trapping by introducing 10% glycerol leads to no disruption of trapping under real-time control by the current mode (a), while the analogous procedure under the voltage mode causes the trapped cluster to be dislodged and broken into multiple smaller clusters (b). The corresponding resonance frequency shift over time for both methods (c)

# **3.8.2** Selective trapping and quantification of sperm cells from a heterogeneous sample

Using the previously described setup, the separation of sperm cells from a heterogeneous mixture of epithelial cell lysate was evaluated in current and voltage modes. Samples were prepared to contain 300,000 epithelial cells and 3,000 sperm cells, creating a ratio of 1:100 (M:F). Samples were separated at low (10  $V_{pp}$ ) and high amplitude (16  $V_{pp}$ ) stimulation in current mode, as well as low amplitude stimulation (10  $V_{pp}$ ) in voltage mode. As seen in Fig. 3-16, samples separated in current mode, at both low and high stimulation, resulted in large and medium-sized trapped clusters, respectively. After acoustic isolation of sperm cells from these samples, these 'sperm fractions' went on for downstream analysis, including a DNase I treatment to remove any remaining female DNA in solution, followed by Acrosolv extraction (ZyGEM). Samples were then analyzed using the Quantifiler Trio kit, which detects two human DNA markers, the large human autosomal target and the small autosomal target, and the male target, the Y chromosome. Analysis using this kit can provide information on the total amount of human DNA present and the total amount of human male DNA present in a sample. By analyzing the nucleic acid composition of the sample prior to acoustic separation and the 'sperm fraction' after acoustic separation, the level of enrichment of male DNA can be assessed. It was hypothesized that due to the more inefficient trapping seen in voltage mode, fewer sperm cells would be trapped, and thus less enrichment would
be observed.



Fig. 3-16 A larger cluster is seen at the higher amplitude stimulation  $(16 V_{pp})$  compared to lower amplitude stimulation  $(10 V_{pp})$ , and no significant trapping is observed in Voltage mode. The DNA quantities listed are not experimentally validated, just projections and placeholders. The standard curve is also not from experimental data, just a placeholder.

#### **3.9** Conclusion

We have developed a system for automated monitoring and control of the resonant frequency during acoustic particle trapping and buffer changes. We applied it to selectively trap sperm cells from a heterogeneous sample containing epithelial lysate for validation based on STR analysis.

### Conclusion

This dissertation demonstrates the design, implementation, and performance of some electronic instrumentations to address some current limitations in manipulating biological samples within microfluidic chips. In the first instrument, we described the design overview of a wideband high voltage AC generator that enables Dielectrophoretic cell separation and characterization in the frequency range of  $1 - 10 \, MHz$  up to  $600 \, V_{pp}$  within insulated or contact-less DEP devices. This HV AC generator provides the highest voltage in the MHz range among all commercially available HV amplifiers. We have utilized this instrument to separate live *C parvum* cells in a mixture containing live and heat-treated cells, thanks to their different dielectrophoretic response in the megahertz frequency range. Three generations of this instrument have been built so far for the University of Virginia, Virginia Tech, and our research collaborator in Taipei, Taiwan. We expect to assess this instrument's performance to manipulate other biological samples, such as tumor-initiating cells. CytoRecovery<sup>TM,</sup> as a new startup company, uses this generator inside its future all-in-one DEP-based biological sample analyzer.

In the second chapter, we introduced a compact and specialized on-chip impedance analyzer for quantifying the field penetration within the contactless DEP devices. Using this instrument, we can assess the quality of a microfluidic chip, particularly contact-less DEP devices, prior to the experiment to verify the manufacturing process and detect any failure that may degrade the separation efficiency. With this approach, we can prevent wasting our valuable biological samples in a non-functional chip. The impedance measurement is performed over a wide frequency range  $(1 \ kHz - 10 \ MHz)$  with the stimulation voltage close to the actual experiments. It enables us to extract all the chip's critical parameters that finally lead to the computation of the maximum fraction of voltage available across the sample channel for cell manipulation, thereby determining the chip manufacturing quality. This data could also help us revise our design to alter those parameters, including the barrier capacitance, sample channel's resistance, and parasitic capacitance, to improve our microfluidic devices' DEP performance.

The last chapter explained a novel methodology for easy but accurate detection and real-time control of resonance frequency in acoustic-based trapping of micrometer-sized particles within bulk microfluidic chips. Instead of a state-of-art approach where the peak amplitude of the voltage across the piezo transducer is monitored to find the resonance frequency, we monitor the piezo AC

current indirectly by measuring the DC supply current of the power amplifier. With this method, the AC voltage doesn't need to reach a minimum level during the frequency sweep that causes less stimulation power. Our experimental results confirmed that the current-based approach preserves the voltage level, increasing the trapping efficiency compared to the voltage-based approach. It is also robust against unavoidable disturbance in fluid flow due to wash steps and a buffer change. Additionally, our compact system integrates almost all necessary electronics needed for acoustic-based separation such as signal generation, amplification, and onboard measurement into a single compact board, making it an ideal tool for portable forensic applications. Our circuit has also demonstrated superior performance in separating sperm cells in a mixture of lysate epithelial cells that provide sufficient samples for genetic profile extraction through the qPCR technique.

### **Future work**

#### 1. Electrical isolation system to enhance output power

The current build of this instrument gives the maximum possible performance in the MHz frequency range by employing the best candidates among commercially available state-of-the-art power operational amplifiers. Within the strategy based on the counter-phase interconnection of Op-Amps, we cannot enhance power simply by additional stacking of the sub-amplifiers. For instance, to connect these two sub-amplifiers in series, we need to wire the negative channel of the upper sub-amplifier to the positive channel of the lower sub-amplifier, as per **Fig. 5-1**. However, it is not possible to connect the nodes with two different voltage levels and expect to preserve their respective voltages, since they will share the same common ground (GND), which then becomes the voltage level of all the nodal points. Hence, we propose to utilize a design based on the stacking of multiple signal generators, each with its own AC generator unit and power supply that are synchronized to the same frequency and phase, thereby enabling them to be fully isolated electrically.



Fig. 5-1 Stacking of sub-amplifiers to enhance gain is not possible without electrical isolation.

To explain the strategy, we draw an analogy to the stacking of multiple batteries in series combination to obtain higher voltage, which is feasible only because each battery is an isolated power unit that does not share any common voltage (the ground point) with any others. While this problem could be addressed by using two isolated signal sources for each amplifier, there is the issue of matching the frequency and phase of these input signals. Hence, our strategy is based on

using a Master DDS (inside the mainboard) and two slave DDS ICs (each inside one slave unit). All slave modules receive their inputs via a set of their own Digital Isolators, thereby keeping them galvanically isolated from outside. Moreover, each module has its Battery-operated power supply to preserve isolation.

The Master DDS will generate a square wave signal with a fixed frequency of 30 *MHz* and acts as the reference clock for the Slave DDS ICs. Therefore, the frequencies of all Slave DDS ICs are synchronized, while the phase of generated signals in all units reset to zero simultaneously upon receiving a reset command, assuming the cumulative delay in all units are similar due to identical digital isolators and relatively similar signal paths.

#### 2. Multiplex Acoustic Trapping system

After a sexual assault, victims undergo a thorough forensic examination of their bodies. During this examination, four evidentiary swabs are collected from the victim, a vaginal swab, a vaginalcervical swab, a perianal swab, and an external genitalia swab. All of these swabs have to undergo the time-consuming process of differential extraction. Differential extraction (DE) is the process by which forensic scientists separate sperm cells (from the perpetrator) and epithelial cells (from the victim) in order to produce a genetic profile of the perpetrator. This process requires a trained technician to first selectively lyse the female epithelial cells before a series of centrifugation and washing steps are conducted to obtain a purified sperm pellet that can then go on for downstream extraction, nucleic acid amplification, and capillary electrophoretic separation to produce a genetic profile that can be used to identify the perpetrator. The development of the SONIC-DE system allows for the elimination of the time-consuming steps of centrifuging and washing, and when tested by real forensic scientists, was considered a promising replacement for their current workflow. However, as the current system is only able to process one swab at a time, it was brought to our attention how valuable it would be to process multiple samples simultaneously. Having an instrument that is capable of processing four samples simultaneously would work effortlessly with the current workflow, as analysts are commonly working on a single case at a time to prevent any contamination.



Fig. 5-2 The schematic of quad-channel acoustic trapping chip

We plan to design a multi-channel acoustofluidic chip (Fig. 5-2) and instrument that is capable of video monitoring the acoustic trapping in each channel. Additionally, the currently implemented system will be expanded to include four independent modules, each includes a signal stimulation unit and current measurement unit, that will independently control each trapping site, applying the resonant frequency based on real-time current measurements. It is our aim to develop this system, validate it for a wide variety of mock sexual assault swabs before testing the prototype instrument in a real forensic lab.

## **List of Publications**

#### ✤ Journal papers

- Real-time detection and control of resonance frequency in acoustic trapping systems by monitoring of amplifier supply currents
   V. Farmehini, S. Kiendzior, J.P. Landers, N.S. Swami ACS sensors (submitted)
- A wide-bandwidth power amplifier for frequency-selective insulator-based dielectrophoresis
  V. Farmehini, A. Rohani, Y.H. Su, N.S. Swami Lab on a Chip (2014) (21), 4183-4187
- Microbial analysis in dielectrophoretic microfluidic systems R.E Fernandez, A. Rohani, V. Farmehini, N.S. Swami Analytica chimica acta 966 (2017), 11-33
- Aptamer-functionalized graphene-gold nanocomposites for label-free detection of dielectrophoretic-enriched neuropeptide Y
  R.E. Fernandez, B.J. Sanghavi, V. Farmehini, J.L. Chávez, J. Hagen, N. Kelley-Loughnane, C.F Chou, N.S. Swami
  Electrochemistry Communications 72 (2016), 144-147
- On-chip impedance for quantifying parasitic voltages during AC electrokinetic trapping V. Farmehini, W. Varhue, A. Salahi, A.R. Hyler, J. Čemažar, R.V. Davalos, N.S. Swami IEEE Transactions on Biomedical Engineering (2019) 67 (6), 1664-1671
- Real Time Electronic Feedback for Improved Acoustic Trapping of Micron-Scale Particles
   C.P. Clark, V. Farmehini, L. Spiers, M.S. Woolf, N.S. Swami, J.P. Landers Micromachines (2019), 10 (7), 489
- Self-aligned microfluidic contactless dielectrophoresis device fabricated by single-layer imprinting on cyclic olefin copolymer
  Salahi, W.B. Varhue, V. Farmehini, A.R. Hyler, E.M. Schmelz, R.V. Davalos, N.S. Swami
  Analytical and bioanalytical chemistry (2020) 412 (16), 3881-3889

- Electrophysiology-based stratification of pancreatic tumorigenicity by label-free singlecell impedance cytometry
   J.S. McGrath, C. Honrado, J.H. Moore, S.J. Adair, W.B. Varhue, A. Salahi, V. Farmehini, B.J. Goudreau, S. Nagdas, E.M. Blais, T.W. Bauer, N.S. Swami Analytica chimica acta 1101 (2020), 90-98
- Conductance-based biophysical distinction and microfluidic enrichment of nanovesicles derived from pancreatic tumor cells of varying invasiveness
  J.H. Moore, W.B. Varhue, Y.H. Su, S.S. Linton, V. Farmehini, T.E. Fox, G.L. Matters, M. Kester, N.S. Swami
  Analytical chemistry 91 (16) (2019) 91 (16), 10424-10431
- High-throughput dynamical analysis of dielectrophoretic frequency dispersion of single cells based on deflected flow streamlines
  K. Torres-Castro, C. Honrado, W.B. Varhue, V. Farmehini, N.S. Swami Analytical and bioanalytical chemistry (2020) 412 (16), 3847-3857
- Sensing of diseased mitochondria proportion by DEP at the organelle level of intact cells P.Y. Chi, T.W. Chuang, T.T. Chu, C.T. Kuo, Y.T. Wu, V. Farmehini, D.B. Shieh, F.G. Tseng, Y.H. Wei, N.S. Swami, C.F. Chou Microfluidics, BioMEMS, and Medical Microsystems XVIII (2020) 11235, 112350N

### **\*** Conference proceedings

- Separation of mitochondrial diseased cells based on organelle-level difference using a dep microfluidic system
  P.Y. Chi, T.W. Chuang, T.T. Chu, C.T. Kuo, Y.T. Wu, V. Farmehini, D.B. Shieh, F.G. Tseng, Y.H. Wei, N.S. Swami, C.F. Chou
  23rd International Conference on Miniaturized Systems for Chemistry and Life Sciences, MicroTAS 2019
- A Novel Approach to Artifact-Free EMG Recording During Electrical Stimulation-Induced Muscle Activation
   V. Farmehini, N.S. Swami, P. Faghri, M. Vromans Archives of Physical Medicine and Rehabilitation (2017) 98 (10), e26

### ✤ Patents

- Identification and monitoring of cells by dielectrophoretic tracking of electrophysiology and phenotype
   N.S. Swami, Y.H. Su, C.A. Warren, A. Rohani, V. Farmehini
   US Patent App. 15/515,528
- Method and system for impedance-based quantification and microfluidic control N.S. Swami, V. Farmehini, W. Varhue, International Application No. PCT/US2020/014899
- Multiplexed on-chip impedance cytometry system and method N.S. Swami, J. McGrath, W. Varhue, C. Honrado, V. Farmehini, Y. Liu International Application No. PCT/US2019/053242

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# Appendix

#### **Board schematics and PCB Layouts**

In the following pages, the design schematics of all circuits and the corresponding PCB layouts (signal routes) are included. All board were designed using Altium Designer software. The list of presented designs/PCBs is as below:

- HV AC Generator Power Supply Board
- HV AC Generator Main Board
- HV AC Generator Panel Board
- Impedance Measurement circuit with Chip holder
- Acoustic Trapping Controller











![](_page_93_Figure_0.jpeg)

![](_page_94_Figure_0.jpeg)

# HV AC Generator (Main Board)

![](_page_95_Figure_1.jpeg)

![](_page_96_Figure_0.jpeg)

![](_page_96_Figure_1.jpeg)

![](_page_96_Figure_2.jpeg)

![](_page_96_Figure_3.jpeg)

![](_page_96_Figure_4.jpeg)

![](_page_97_Figure_0.jpeg)

![](_page_98_Figure_0.jpeg)

![](_page_99_Figure_0.jpeg)

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CSD AND 33uF GND  $\overset{+12V}{\underset{i=1}{\overset{-1}{\underset{i=1}{\overset{-1}{\underset{i=1}{\overset{-1}{\underset{i=1}{\overset{-1}{\underset{i=1}{\underset{i=1}{\overset{-1}{\underset{i=1}{\underset{i=1}{\overset{-1}{\underset{i=1}{\underset{i=1}{\underset{i=1}{\overset{-1}{\underset{i=1}$ H +85V +15V GND +16V +16V +160V +160V +160V Hsader +12V H2 GND 23 H4 +15 Header

# HV AC Generator (Panel Board)

![](_page_100_Figure_1.jpeg)

![](_page_101_Figure_0.jpeg)

![](_page_101_Figure_1.jpeg)

![](_page_101_Figure_2.jpeg)

![](_page_101_Figure_3.jpeg)

![](_page_101_Figure_4.jpeg)

![](_page_101_Figure_5.jpeg)

![](_page_101_Figure_6.jpeg)

# Impedance Analyzer and Chip Holder Board

![](_page_102_Figure_1.jpeg)

![](_page_103_Figure_0.jpeg)

![](_page_104_Figure_0.jpeg)

![](_page_105_Figure_0.jpeg)

![](_page_106_Figure_0.jpeg)

![](_page_107_Figure_0.jpeg)




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Acoustic Trapping Controller Board







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