Near-zero power wake-up receivers for the Internet of Things

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ABSTRACT

The Internet of Things (IoT) envisions the networking of a massive amount of interconnected devices. These devices enable us to monitor and control our world in a way never possible before. A significant aspect of this technology is the deployment of massive wireless sensor networks (WSN). A critical consideration in large-scale WSN is the sensor node power consumption. In massive WSN, regular battery replacement is infeasible, and node power consumption limits the sensor node lifetime [1]. Event-driven sensor networks are large-scale WSN that spend most of their lifetime in an asleep yet aware state. These sensors obtain low power consumption and long lifetimes through aggressive node-level duty cycling. One method of performing node-level duty cycling is to use a wake-up receiver circuit. Wake-up receivers are ultra-low-power radio frequency receiver circuits used to duty cycle the sensor node, based on an external wireless wake-up event. Ideally, the standby power consumption is kept at near-zero power levels ($< 1\mu W$).

This dissertation investigates how to overcome sensitivity limitations in near-zero power level wake-up receivers. While previous work has presented wake-up receiver circuits operating at very low power levels ($< \ 100nW$), these receivers suffered from severely limited operating ranges due to their reduced sensitivities [2], [3]. The initial intended application for these sub-100nW sensors was ultra-short-range body area networks operating over a few meters. This limited operating range restricts the application space available to sensor nodes using these wake-up receivers. It is desirable to decrease wake-up receiver power consumption further, while obtaining significantly higher receiver sensitivities, enabling longer-range applications.

This work first examines the "detector first" receiver architecture, which has obtained the lowest power consumption to date. A particular emphasis is placed on the envelope detector circuit, which is a critical component in the detector first architecture. Further, this document explores the advantages associated with highly tunable bit-level, duty-cycled, tuned radio frequency (TRF) front ends and presents a receiver that demonstrates a 1000-fold improvement in sensitivity over

the envelope detector (ED) first receivers.

Chapter 2 discusses ED analysis and design techniques that led to the development of the wake-up receiver presented in Chapter 3. The detector first receiver, presented in Chapter 3, demonstrated a better sensitivity of $-76\ dBm$ while obtaining a power consumption of $7.4\ nW$. Using an automatic offset compensation algorithm and careful baseband design, this receiver was shown to be resilient to external radio frequency (RF) interference. This work has extended state-of-the-art in sub-W wake-up receivers in both sensitivity and robustness. A new ED topology is introduced in Chapter 4, which addresses many robustness issues and shortcomings of the conventional Dickson ED.

The analysis presented in Chapter 2 indicates that state-of-the-art detector first receivers are rapidly approaching their fundamental limitations regarding sensitivity. To extend the operating range further, Chapter 5 proposes a bit-level duty-cycled TRF receiver to overcome the sensitivity bottlenecks encountered in ED first receivers. Chapter 6 presents techniques to enable low-power good sensitivity TRF receivers. The combination of improvements in TRF design with the architecture proposed in Chapter 5 has enabled a higher than 1000 increase in sensitivity over the system presented in Chapter 3.

The developments presented in this work will drive higher wake-up receiver sensitivities and lower power operation. Higher sensitivity has enabled a communication range improvement in smart sensor nodes. Receivers operating with the old sensitivities were limited to short-range applications, such as across the body. With the advances proposed here, operating ranges can be extended to several kilometers, or potentially to satellites in near-earth orbit.

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Table of Contents

List of Tables

List of Figures

LIST OF ABBREVIATIONS

IoT Internet-of-things

RF Radio Frequency

Rx Receiver

WuRx Wake-up Receiver

ULP Ultra-low power

CMOS Complementary Metal Oxide Semiconductor

LPWAN Low-power wide area network

RFIC Radio frequency integrated circuit

ED Envelope detector

RFID Radio frequency identification

LNA Low noise amplifier

TRF Tuned RF

IF Intermediate Frequency

BB Baseband

LO Local Oscillator

WiFi Wireless Fidelity

SNR Signal to noise ratio

CW Continuous wave

AGOC Automatic gain and offset compensation

MEMS Micro-electro-mechanical systems

OCVS Open circuit voltage sensitivity

NEP Noise equivalent power

MOSFET Metal-oxide-semiconductor field effect transistor

IV Current voltage relationship

W Transistor gate width

L Transistor gate length

RC Resistor capacitor

Q-factor Quality factor of impedance

PCB Printed circuit board

DTMOS Dynamic threshold voltage MOSFET

NFET N-type CMOS transistor

PFET P-type CMOS transistor

LVTRF Low-threshold voltage RF transistor

ZVT Zero threshold voltage transistor

ZVTDG Zero threshold voltage thick oxide transistor

VNA Vector network analyzer

FET Field-effect transistor

VDD Power supply input

OP-Amp Operational Amplifier

OOK On-off-keyed

MURS Multi-use radio service

ISM Industrial, Scientific and Medical band

BER Bit-error-rate

PRBS Pseudo-random-bit sequence

TMD Triode mode Dickson envelope detector

GFUS Global foundries US

LC Inductor-capacitor

PVT Process voltage and temperature

SAR Successive approximation

ADC Analog-to-digital converter

RFFE RF-Frontend

FOM Figure of merit

CIR Carrier to interferer ratio

ENOB Effective number of bits

LSB Least significant bit

LPHS Low power high sensitivity

LLHS Low latency high sensitivity

LPLL Low power low latency

SEM Scanning electron microscope

IC Inversion coefficient

LP Low power

DIBL Drain induced barrier lowering

B1dB Blocker 1dB compression point

B3dB Blocker 3dB compression point

BSIM6 Berkeley MOSFET model V6

EIRP Effective iso-tropic radiated power

MUTC Modified uni-traveling carrier photodetector

AlN Aluminum Nitride

PD Photodetector

PL Path-loss

EDFA Erbium-doped fiber amplifier

VOA Variable optical attenuator

EM Electromagnetic

MDS Minimum detectable signal

PSD Power spectral density

NEB Noise equivalent bandwidth

LIST OF SYMBOLS

P_{Lossy} Power received by a lossy antenna

P_{Ideal} Power received by an ideal antenna

η_{Ant} Antenna efficiency

A_{Ant} Antenna effective area

f_0 RF carrier frequency

V_O Output DC voltage of envelope detector

V_{RF} RF voltage at detector interface

t independent time variable

T Sampling period

F Dependent variable of frequency

f independent frequency variable

ω independent frequency variable in radians

ϕ Arbitrary phase angle

$OCVS$ Detector Open Circuit voltage sensitivity, defined as output voltage over input RF power

P_{RF} Power available from RF source

NEP Noise equivalent power of envelope detector

$\overline{v_n^2}$ Noise power spectral density

I_D Drain bias current for transistor

V_G Applied gate voltage of transistor

V_S Applied source voltage of transistor

V_D Applied drain voltage of transistor

n Subthreshold slope

V_t Thermal voltage (kTq)

I_{D0} Normalization current for MOSFET IV curve

W Transistor gate width

L Transistor gate length

V_{TH} Transistor threshold voltage

G_D Transistor small signal output conductance

V_{op} Operating point voltage

R_O Transistor small signal output resistance

C_O Transistor small signal output capacitance

α Detector open circuit voltage sensitivity

σ_D Constant linking bias current to output impedance for device

γ_D excess noise factor of device

k_f Flicker noise constant

A Transistor gate area

T Temperature

k Boltzmanns constant

N Number of diodes in multistage envelope detector

Z_D Diode impedance

Z_C Capacitor impedance

K_i Voltage division ratio

μ_D Device open circuit voltage sensitivity

Z_{oi} Z-parameter associated with input network

Y_{in} Terminal admittance

Y_{SS} Single stage input admittance

C_{Par} Parasitic capacitance

C_D Diode capacitance

I_i I'th input current N-port network

s Independent complex frequency

b_i Dominant time constant

τ_i Time constant

R_s Source resistance at resonance

B Bandwidth

SNR Signal to noise ratio

R_o Output impedance

Λ Normalized voltage sensitivity

P_{MDS} Minimum detectable signal power

δ Trans-conductance efficiency g_m/I_D

A_V Voltage gain

L Latency

S Sensitivity

DF Duty factor

R Bit rate

FOM Figure of Merit

CIR Carrier to interferer ratio

$ENOB$ Effective number of bits

V_{Sig} Signal voltage

V_{Int} Interferer voltage

Δ_f Frequency offset

$H(f)$ Bandpass filter transfer function

Rej Interference rejection

V_{Int} Interferer voltage

$S(f)$ Frequency response of power spectral density

V_i RF voltage into system

F Noise factor of amplifier

IC Inversion Coefficient

G_{spec} subthreshold gm/Id ratio

η amplifier efficiency

B Feedback factor

Q Quality factor

C_P Parasitic capacitance

R_L Load resistance

L Inductance

V_{th} Thevinin voltage

ϵ_r Dielectric contant of medium

λ_0 Free-space wavelength

d Thickness

G Antenna gain

$\mathcal{R}$ Autocorrelation function of time domain signal

VN Noise voltage

$E[]$ Expected value operator

σ_N Variance of noise voltage

$Rect$ Rectangular function aka gate function

$sinc$ sinc function

CHAPTER 1

INTRODUCTION

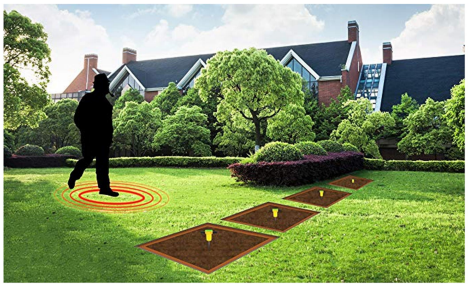
1.1 Motivation for event driven wake-up receivers

Event-driven smart sensor node's [5] are an emerging technology that promises to be useful in a wide range of applications. Event-driven sensors are small form factor wireless sensor node's that monitor some environmental variable over a long timescale. This data was collected from a large number of node's and processed by an end-user to make informed decisions. Event-driven sensing is applied (Figure 1.1) across a wide array of economic sectors including agricultural [6], industrial, civil infrastructure [7], and unattended ground sensor networks.

Event-driven sensors spend the majority of their lives in an "asleep yet aware state," drawing a minimal amount of DC power yet remaining aware of the ambient environment. These sensors minimize power consumption through a combination of ultra-low-power sensing units and node-level duty cycling through the use of a wake-up receiver circuit. The real power of such a sensing system comes from combining the data collected across a large number of sensors operating in parallel. Utilizing a near-zero power wake-up receiver allows the sensor node power consumption to be dominated by the active sensing circuitry, maximizing node lifetime.

Smart sensor node's (Figure 1.2) will form the heart for the IoT. The scale of the IoT is predicted to be massive when compared to contemporary networks. Some predictions for the size of the IoT surpass 1 trillion interconnected devices before 2035 [8]. This new network in many ways will be fundamentally different from current wireless networks in both breadth and technical requirements.

Agriculture Monitoring [6]



Unattended ground sensors [10]

Industrial Monitoring [7]

Infrastructural Monitoring [8]

Figure 1.1: Applications for Internet of Things (IoT) technologies are widely varied and found wherever remote or ubiquitous monitoring is desirable.

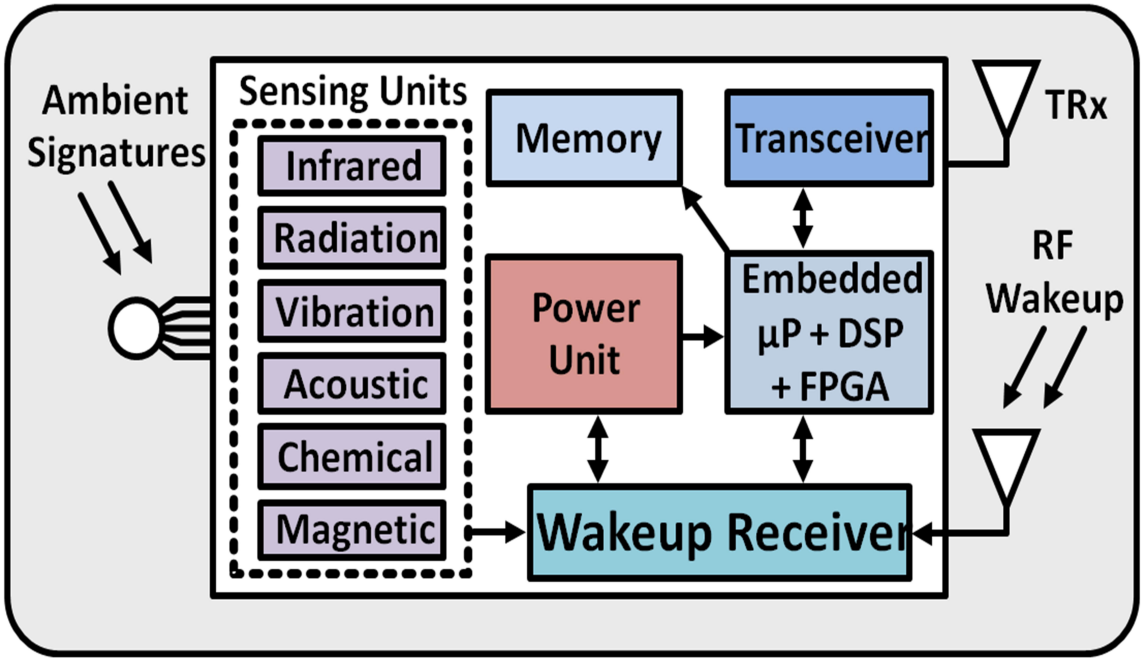


Figure 1.2: Block Diagram of a smart sensor node, showing major system components and inter-dependencies between major system blocks.

Many emerging applications move radio requirements from extremely low latency, ultra-high-speed communication towards ultra-low power low throughput networks. While the amount of data transmitted might be much smaller, the nature of the information can be quite critical.

The potential size of the network places two basic requirements on the hardware used to implement it: ultra-low power (ULP) consumption, and low-cost implementation. Utilization of subthreshold design techniques and aggressive duty cycling enables low power-efficient operation, which enables an improvement in its lifetime from months to years. Low system cost allows economically for networks to be scaled to the size envisioned for the IoT. Advanced complementary metalox-idesemiconductor (CMOS) technologies can meet both of these needs simultaneously.

Sensor node's consume most of their energy in the standby state; this is due to the frequent nature of the events of interest. Ideally, standby power consumption should be limited to levels comparable to that of the battery leakage. For small button cell batteries the leakage can be as low as 10 nW, which enables continuous operation over many years. Modern radio front-ends consume

very high levels of power, typically in the milliwatts. If radio monitoring or control is needed, the radio front-end easily dominates standby power consumption. These sensor nodes will include processing [9–11, 11], analog front-ends and sensors [12, 13], frequency references [14, 15], energy harvesting [16, 17], wireless transceivers [18, 19] and power management [20–23] and will include both SIP solutions and fully integrated solutions [24–26].

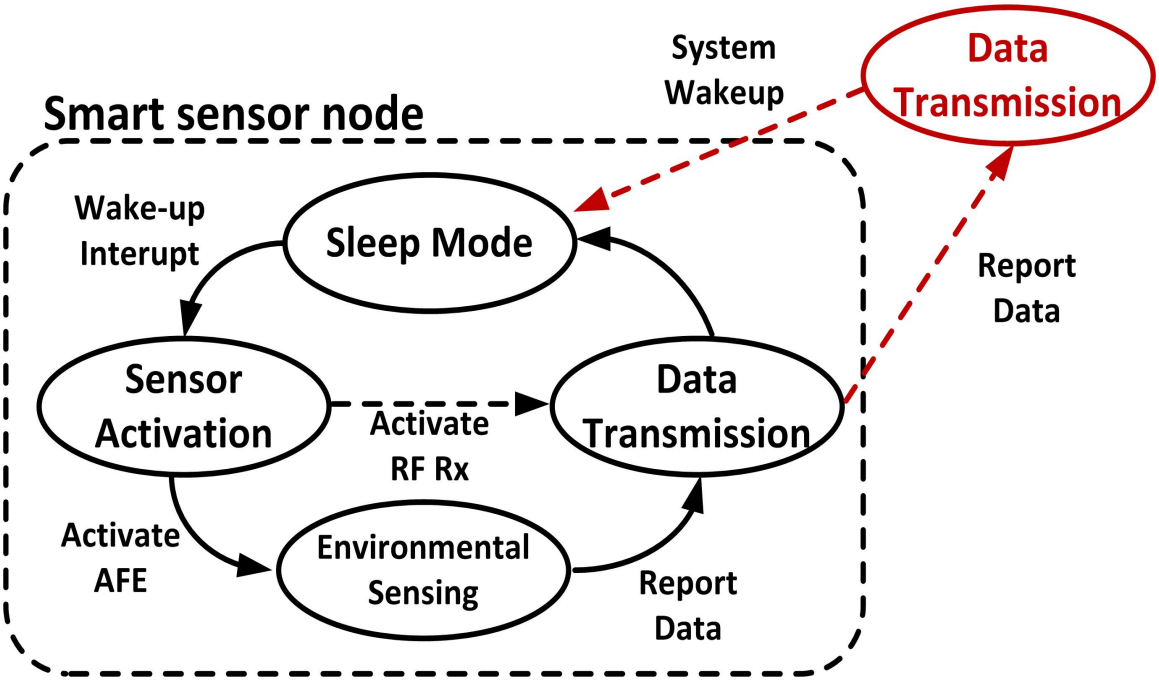


Figure 1.3: A flow-chart depicting wake-up receiver operation, this diagram shows the response of an "asleep yet aware" sensor to an external RF trigger, which is detected by the wake-up receiver.

Duty cycling the primary radio receiver using a wake-up receiver circuit offers an attractive solution to this issue. Wake-up receivers sense a predefined radio frequency (RF) wake-up pattern and then activate high power analog sensing units or the main radio. A flow-chart depicting this operation is shown in Figure 1.3. Typically, the wake-up receiver and the system leakage current dominate the node's standby power consumption. By reducing wake-up receiver power consumption from 100's of μW to less than 1 μW, the lifetime of the sensor node can be extended by a factor of 100 or more.

1.2 Wake-up receiver sensitivity requirements

Figure 1.4 (a) and (b) compares node lifetime given a fixed battery supply, and details the sensitivities of several commercial standards. Previously demonstrated sub-μW receivers obtained sensitivities of less than -60 dBm [27]. Obtaining sensitivities similar to those of Wi-Fi receivers ($-80\ dBm$) enables many short-range and indoor IoT applications. Applications such as outdoor and industrial low power wide area networks (LPWAN) require sensitivities similar to cellular technologies ($< -100dBm$). The lowest power receivers demonstrated to date demonstrating $< -100dBm$ sensitivity have power consumption in the hundreds of μW [28]. A solution is needed to bridge this power consumption-sensitivity gap and enable many near-zero sensing applications.

In applications where operating range is not a predominant concern, the system area can be a crucial design consideration. At low RF, ($<\ 1\ GHz$), the antenna area becomes a significant contributor to the node area. Electrically-small antennas are well known to be inefficient radiators [29]. This leads to a decreased operational range for systems with an electrically-small antenna. Limited antenna size leads to reduce efficiency, as seen in Figure 1.5. The effective sensitivity of an RF receiver including antenna loss is

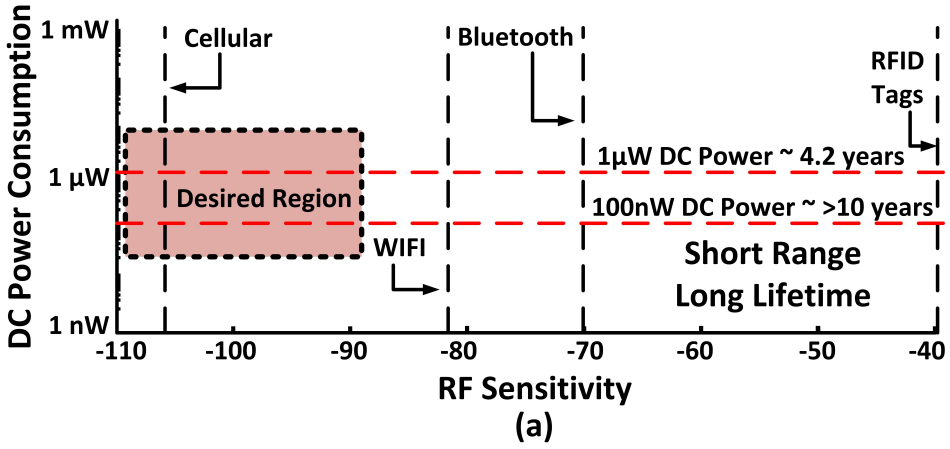
$$P_{Lossy} = P_{Ideal} - log10(\eta_{Ant}), \tag{1.1}$$

where P_{Lossy} and P_{Ideal} are the signal strength in dBm for the lossy and ideal 0 dB gain antennas, respectively, and η_{Ant} is the efficiency of the antenna under consideration.

A popular antenna type in smart sensor node applications is the electrically-small loop antenna [30], and [31]. The small loop antenna can be shown to have an antenna efficiency relative to its footprint by

$$\eta_{Ant} \propto A_{ant}^2 f_0^4. \tag{1.2}$$

where A_{ant}^2 is the antenna aperture, and f_0 is the RF carrier frequency. Comparing receivers operating at different frequencies responding to the same input power flux at a constant receiver antenna



(a)

Technology	Sensitivity (dBm)	Typical Range (m)
Passive RFID	> -40	< 10
Bluetooth	-70	~ 10
WIFI 802.11.ac	-82	~ 50
Cellular: GSM	-102	> 10k
Cellular: WCDMA	-106	> 10k
GPS Receivers	<-125	Satellite

(b)

Figure 1.4: (a) Receiver sensitivity of various commercial wireless technologies compared with node power consumption and lifetime considering a typical CR1220 coin-cell battery, (b) Receiver sensitivity and typical operating ranges across various wireless technologies

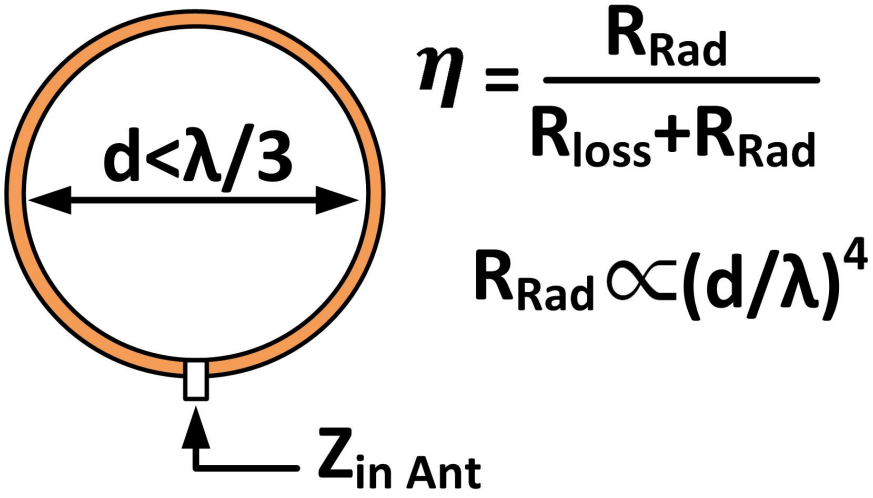


Figure 1.5: Diagram showing small loop antenna including efficiency equations

aperture enables a comparison between the performance gained when scaling frequency. Comparing two systems operating a the 433MHz ISM band and the 2.4GHz ISM band we find that we find the effective sensitivity of the 433 MHz system is 15 dB lower than an equivalent system operating at 2.4 GHz for a given antenna area noting that free-space path loss is proportional to F_{RF}^2.

These results indicate that for some applications that do not require good sensitivity, there still exists a substantial motivation for pushing wake-up receiver sensitivity beyond $-100dBm$. Pushing state-of-the-art in sensitivity can enable both new applications as well as reduced sensor node footprint in current applications.

1.3 Prior art

State-of-the-art in wake-up receiver design [32] has deviated substantially from the traditional heterodyne architecture [28], [33], [34], and [35]. A resurgence of several radio techniques that were superseded by the modern heterodyne architecture has occurred, and these developments make this an exciting space for the RFIC designer.

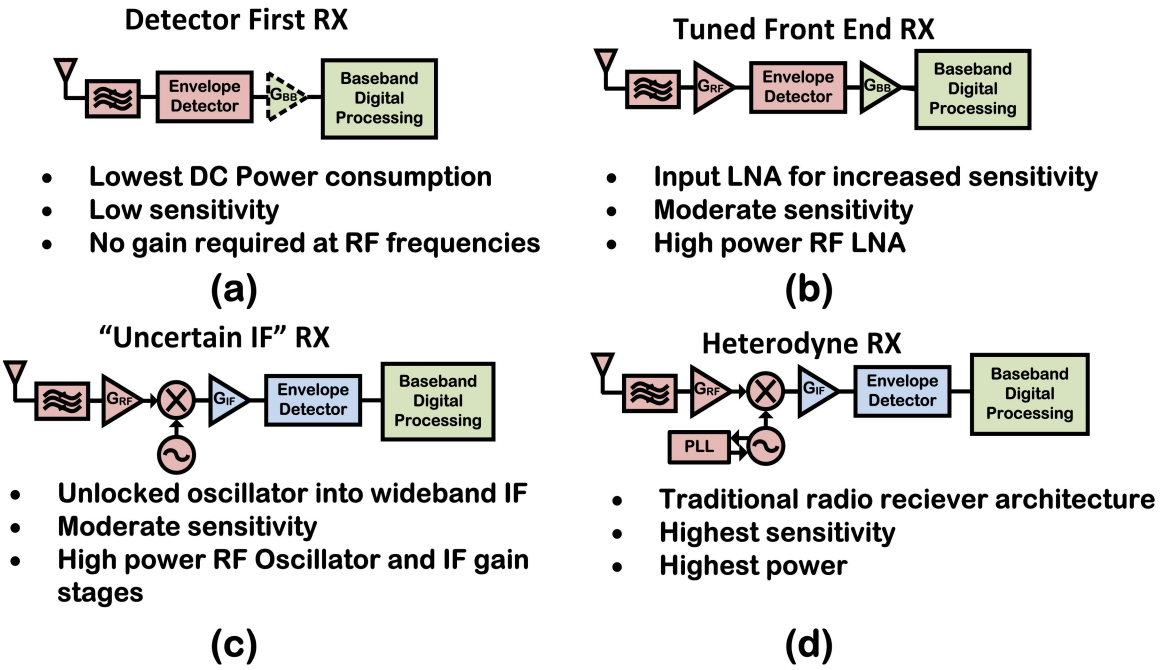


Figure 1.6: Popular radio receiver architectures utilized at ultra-low power levels consisting of (a) detector-first receiver utilizing no RF power gain, (b) Tuned RF or "TRF" receiver utilizing RF LNA with active RF power gain, (c) Uncertain IF receiver with RF mixer/LO, and (d) full Hetrodyne receiver.

detector-first receivers (Figure 1.6 (a)), which forego the use of any circuits providing active RF power gain have achieved the lowest power consumption. The only class of receivers to achieve lower power consumption are fully passive radio frequency identification (RFID) systems, which are limited in sensitivity to worse than $-32dBm$ [36]. These circuits obtain all their voltage gains passively through impedance matching networks. The RF signal is then down-converted through a "square-law" ED before detection by the baseband circuits. A notable example of a receiver existing before this work began [27] demonstrated $-56\ dBm$ sensitivity at $2.4\ GHz$ with a data rate of $8kbps$. Due to the lack of front-end RF gain, these receivers struggle to overcome the sensitivity limitations imposed on them by noise generated by the ED. Because of this limitation, optimal detector design offers a path towards obtaining superior performance.

Adding a relatively high-power RF low noise amplified (LNA) to the detector-first receiver can

boost front-end sensitivity substantially. This architecture (known as a TRF) receiver is shown in Figure 1.6 (b). The RF LNA offers power gain, unlike the passive impedance matching network. Unfortunately, this power gain comes at a significant power overhead, associated with biasing the amplifier into a region where RF gain is available. To obtain high sensitivities, high levels of RF gain are required, typically exceeding 50 dB. The high gain required reduces the robustness of the receiver to interference, typically requiring external filtering for robustness. Recent examples [37], [38] of this receiver have shown better than -80 dBm sensitivity but at a high power consumption of greater than 10 μW.

An alternative technique to provide better sensitivity than the detector-first receivers, while reducing power consumption compared to the full heterodyne receiver is the "Uncertain IF" architecture (Figure 1.6 (c)) [39]. This receiver uses a free-running local oscillator (LO) to convert the input RF signal to a wide-band intermediate frequency (IF). As the frequency uncertainty of the oscillator increases, the IF bandwidth required to detect the input signal also increases. The primary advantage of this architecture over the TRF architecture is that most of the gain can occur at IF frequencies where power gain is more readily available. Unfortunately, the wide IF bandwidth required for detection implies a wide noise equivalent bandwidth in the IF-ED. This wide noise bandwidth reduces the receiver sensitivity and increases susceptibility to interference. These receivers have shown very similar performance to the TRF receivers, obtaining around -85 dBm in sensitivity at 10s of μW in power consumption [39].

1.4 Problem Statement

Increasing standby power consumption degrades battery lifetime or lowers the obtainable functionality of energy harvesting solutions. Event-driven wake-up receivers enable the reduction of standby power consumption using aggressive node-level duty cycling. While previously demonstrated sub-μW wake-up receivers can operate with very low power consumption, they do so with poor RF sensitivities $> -60\ dBm$. Many consumer and indoor IoT applications will require sensi-

tivities at least as good as those of commercial Wi-Fi receivers (roughly $-80\,dBm$). The sensitivity gap between the previously demonstrated sub-μW receivers and the sensitivity of standard Wi-Fi receivers is more significant than a factor of 100. In symmetric networks where the transmitter power is constrained, the receiver sensitivity requirements will become harder.

Applications such as outdoor and industrial IoT require much better sensitivities than those present in Wi-Fi receivers. These networks will operate over kilometers, where sensitivities surpassing -100 dBm are desirable. Improving receiver sensitivity to better than -100 dBm, while maintaining sub-μW power consumption requires an improvement of over 1 million-fold compared to previous work. Compounding the issue, as receiver sensitivity is increased, the requirements in interference robustness must also increase. This sensitivity and power consumption gap presents a significant hurdle in the development of wireless sensor networks operating over long ranges.

1.5 Thesis Statement

A direct path to addressing the sensitivity gap in sub-μW receivers is to push the detector-first receiver towards its technological limitations. However, analysis reveals that directly scaling this architecture to the sensitivities required in outdoor and industrial IoT applications ($<$ -90 dBm) is not feasible. While duty cycling can reduce the power consumption of higher power receivers ($P_{DC} < \ 100\mu W$), even at higher power levels, sensitivities surpassing -90 dBm are challenging to obtain.

This work reveals the technological limitations of the detector-first receiver sensitivity given certain technological constraints based on detector device limitations and impedance matching limitations. Practical and robust receivers can be designed that approach these technological limitations. A combination of bit-level duty cycling and the adoption of the TRF front-end can overcome the limitations of the ED first receiver and obtain superior sensitivity.

A practical and robust detector-first receiver approaching technological sensitivity limitations is shown to obtain -76 dBm with a low 7.4 nW power consumption. A careful study of noise in the

TRF receiver, combined with innovations in better ultra-low power amplifier design has enabled TRF sensitivities surpassing -103 dBm, while maintaining an active power consumption of less than $45\mu W$. Through a combination of aggressive bit-level duty cycling and the better sensitivity TRF receiver, a highly tunable duty cycled receiver has been demonstrated which surpasses -100 dBm in sensitivity at 33 nW.

1.6 Research Tasks

The main topics addressed in this dissertation are:

1. Development and optimization of near-zero power level ED circuits,
   (a) Analysis of square-law ED which develops accurate and scalable models for detector design,
   (b) Identification of metrics of importance, relating these to design variables,
   (c) Explorations of fundamental trade-offs between detector architectures finding the optimum design for a given set of performance goals,
   (d) Both topological investigations and investigations into limits imposed by the technology,
   (e) Development of a design methodology to reach an optimal detector design with regards to receiver sensitivity.
2. Interference robust nanowatt power level detector-first receiver design
   (a) Developing a robust near-zero power wake-up receiver, which approached the technological signal to noise ratio (SNR) limitations for detector-first receivers,
   (b) Designing the baseband for rejection of continuous wave (CW) interference,
   (c) Developed offset control and automatic calibration methods suitable for an event driven receiver system (AGOC design)

3. Developed highly scalable bit-level duty cycled wake-up receivers,
    (a) Demonstrated a wide tunable trade-space enabled through the system level architecture,
    (b) Designed fast-start up circuits to ensure the receiver has superior power consumption,
    (c) Demonstrated the first radio operating at $< 1\ \mu W$ achieving a sensitivity of $<$ -100 dBm,
    (d) Helped to develop automatic gain and offset control algorithms that operate with the samplifier type of receiver.
4. Tuned RF front-end design exploring amplifier optimization, and integration with high Q filter components,
    (a) Performed system level sensitivity optimization finding and overcoming key bottlenecks in the RF architecture,
    (b) Designed interface between MEMS filter and CMOS RF amplifiers,
    (c) Developed efficient RF gain stages through both novel amplifier topologies and design methodologies.

The current state-of-the-art with regards to sensitivity and power consumption is shown in Figure 1.7, where our proposed receivers are highlighted, obtaining a $>$30dB sensitivity improvement over the state of the art sub-microwatt receivers.

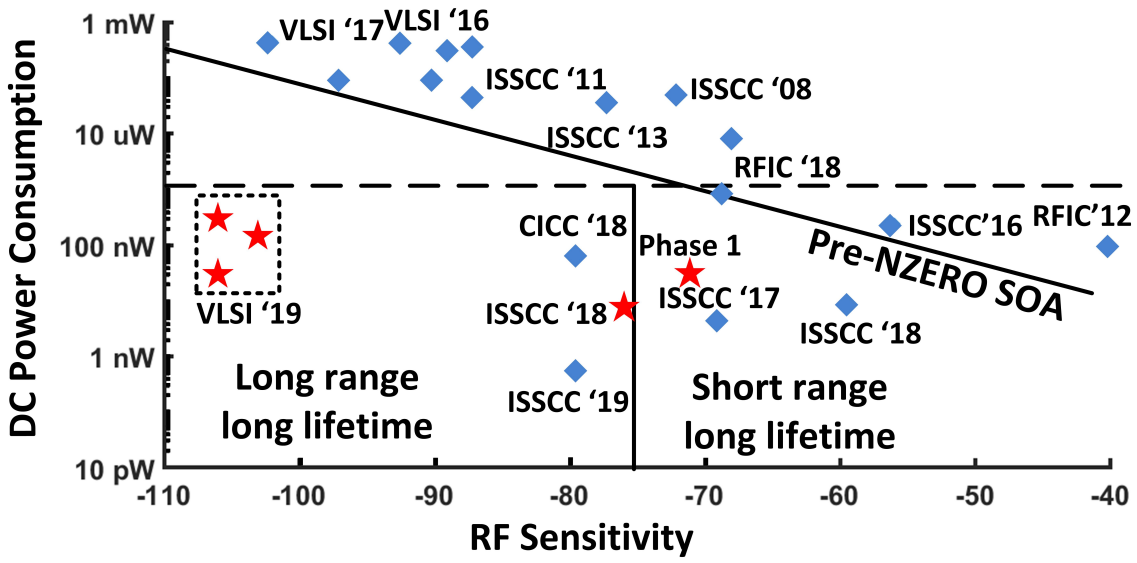


Figure 1.7: Scatter plot of the state-of-the-art in ultra-low power receivers highlighting the contributions obtained in this Thesis, where the stars represent receivers developed in this thesis.

CHAPTER 2

SQUARE LAW ENVELOPE DETECTOR ANALYSIS AND DESIGN

2.1 Motivation

Envelope detector (ED) circuits operating under the square law regime find application in the majority of sub-milliwatt RF receivers. The various ultra-low-power receiver architectures use square-law ED circuits in different parts of the signal processing chain, as seen in Figure 2.1. The detector has varying levels of significance to the overall receiver performance depending on the receiver architecture, ranging from a crucial design choice in the ED first receiver to secondary importance in the heterodyne receiver. Depending on the system-level requirements, the ideal ED design ranges from a zero power and rather slow passive ED to high-speed and high-power active EDs. This chapter develops accurate and scalable models for ED circuits which show < 1 percent deviation from full transient simulation, enabling a comparison between different detector topologies, and a codesign methodology for passive EDs. This work lead to the publications [40], [41] and [42].

2.2 Envelope detectors in ultra-low-power wake-up receivers

The critical issue in detector-first receivers is the design of the ED, which has a significant impact on the sensitivity, DC power consumption, and robustness of the receiver. Optimal detector design and optimization can significantly improve receiver sensitivity and reduce power when compared

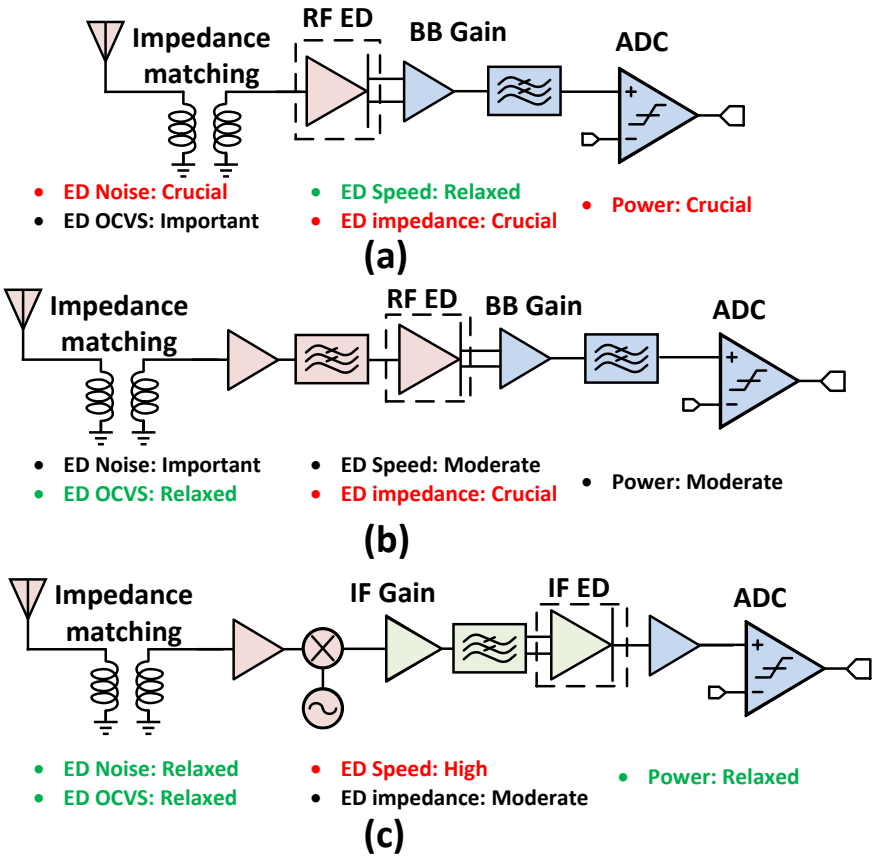


Figure 2.1: (a) Detector-first receiver places the detector immediately after impedance matching, (b) Tuned RF front-end places the detector after RF gain and noise filtering, and (c) Hetrodyne receivers place the detector after IF gain and filtering.

to less efficient designs. Detector architecture choice is a critical design decision that moves the front-end towards a particular set of performance metrics.

The ”Tuned RF Front-end” architecture utilizes active RF gain in order to boost the sensitivity of the receiver. The detector noise and sensitivity determine the required level of RF gain for front-end noise to dominate over detector noise. Further, the RF gain stages need to drive the ED; therefore, front-end power consumption can be lowered utilizing a high impedance detector interface so as to not load the RF gain stages.

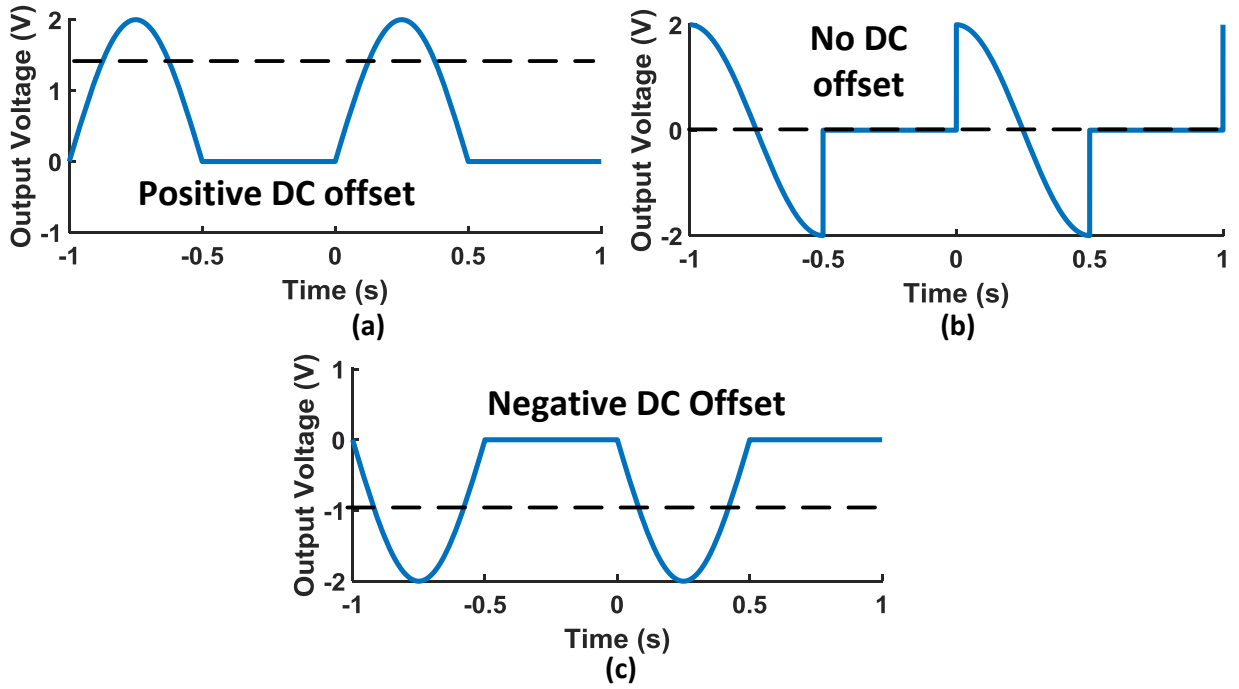


Figure 2.2: Differing phase relations between the RF input signal and LO pump for a single balanced mixing (a) 0-degree phase shift between RX and LO, (b) 90-degree phase shift between RX and LO, and (c) -90-degree phase shift between RX and LO, where the DC component of this waveform is detected.

Event-driven wake-up receivers fundamentally lack phase synchronization with the wake-up signal due to the asynchronous nature of the receiver. Heterodyne and homodyne receivers typically require LO synchronization with the transmitted signal in order to avoid the dependence upon the baseband signal amplitude on RX and LO phase alignment during the signal conversion to baseband. Considering the down-conversion of a single tone from either an RF frequency (Direct conversion receivers) or IF frequency (Heterodyne receivers), we can express the down-converted signal as

$$V_O = V_{RF} cos(2\pi f_0 t + \phi) square(2\pi f_0 t), \tag{2.1}$$

where $square(2\pi f_0 t)$ is a square-wave varying from -1 to 1 representing a single balanced mixing,

and ϕ is the phase offset between the RX signal and the LO which, after low-pass filtering, presents an output DC voltage which varies as

$$V_O \propto cos(\phi), \tag{2.2}$$

indicating that the output baseband signal amplitude is uncertain as the phase difference between the transmitted signal and local oscillator change.

Plotting 2.2 across various signal phases leads to the output signals shown in Figure 2.2. After the down-conversion, the signal is typically low-pass filtered, leading to a varying DC level (and therefore output signal) depending on the phase or amplitude of the transmitted signal. A reliable alternative to baseband down-conversion that works without the requirement of phase synchronization between transmitter and receiver is ED, which is typically done under the square law regime in ULP receivers due to RF and IF power and linearity requirements.

Due to these phase ambiguity concerns, even ULP mixer-based receivers have widely employed ED circuits to provide conversions to baseband [43], [28].

2.3 Square-law detector modeling

ED circuits are inherently nonlinear, and, when driven by a sufficiently weak excitation, they operate under a square law regime [29], where the output voltage level is proportional to the input RF power level. Square law operation is necessary in situations where RF gain is limited and input signals are not sufficiently strong to excite higher order linear effects. Important merit considerations for detectors include output noise, rise time (defined here as 10% to 90% of the final value), and detector open circuit voltage sensitivity (OCVS) [44]. OCVS is defined by:

$$OCVS = V_O/P_{RF}, \tag{2.3}$$

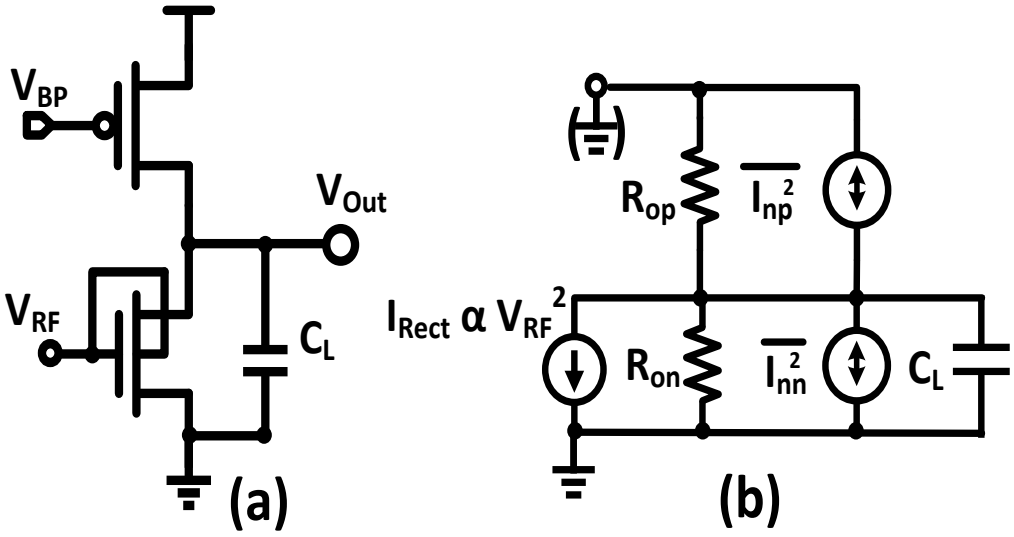


Figure 2.3: Schematic diagram of a: (a) common source active detector, (b) baseband equivalent network for a common source active detector.

which relates input RF power (P_{RF}) to output baseband voltage V_{Out} for square-law detectors. Detector Noise Equivalent Power (NEP) [45] is defined as

$$NEP = \sqrt{\overline{v_n^2}}/OCVS \quad W, \tag{2.4}$$

where $\overline{v_n^2}$ is the power spectral density at the output of the detector. This NEP is equal to the input RF power level required to obtain a 0 dB SNR in a 1 Hz output bandwidth. The NEP is a useful quantity for calculating the sensitivity of a detector whose noise is dominated by thermal noise. Furthermore, when multiplied by the square root of the output bandwidth, the NEP calculates the minimum detectable signal (rms voltage). The NEP has a similar function to input-referred noise for linear receivers in that it determines the sensitivity limits of the receiver but is not equivalent to an input-referred noise.

There are two broad classes of ED circuits, i.e., passive and active ED circuits. Active detectors (Figure 2.3) are ultra-low-power amplifiers biased for very high second-order nonlinearity, and the second-order current produces a voltage sensed by the subsequent stages.

Passive detectors are variations of cascaded single-stage diode detectors, in which the output signal of several single-stage diode detectors is combined and sensed at the output. One commonly used detector architecture (Figure 2.4 (a)) is based on the Dickson charge pump [46], [36]. In the CMOS implementation, the detector diodes are replaced with diode-connected MOSFETS. A useful way to understand this topology is to consider the detector as an array of N diode detectors in parallel with the RF source at RF frequencies where the coupling capacitors present a low impedance relative to the device impedance R_D. At lower baseband frequencies, it can be considered as an array of diode detectors connected in series for which the coupling capacitors present high impedances.

For both active and passive detector architectures, a pair of decoupled linear networks can accurately model the sensitivity, input impedance, transient response, and noise of the network [40]. One network is utilized to analyze the circuit at the RF frequencies, and the other network is used to analyze the network at the baseband frequencies. The first linearized network consists of the detector circuit with the nonlinear device impedances replaced by their small-signal equivalent impedances and driven by the RF source. The outputs of this network are the RF voltages found across the terminals of all rectifying devices in the circuit. Figure 2.4 (b) illustrates the single-stage RF equivalent network of a Dickson ED. For the second network, the rectifying devices are replaced with a current source placed in parallel with the devices channel impedance. This current source drives the network, including the small-signal impedance of the rectifying devices. The current source amplitude is quadratically related to the RF voltages across the device and controlled via a unit step function corresponding to the time at which the RF signal is applied to the detector (Figure 2.4 (c)). Figure 2.3 details the RF and baseband equivalent circuits for the common-source active detector.

When comparing full transient simulations of active and passive EDs to the decoupled linear network models, a strong agreement is found, as seen in Figure 2.5 (a,b,c). The output noise spectral density can be found through calculating the output noise of the linear baseband networks when assuming that the signal source is removed. The voltage sensitivity of the structure is found by calculating the steady-state solution of the baseband equivalent networks.

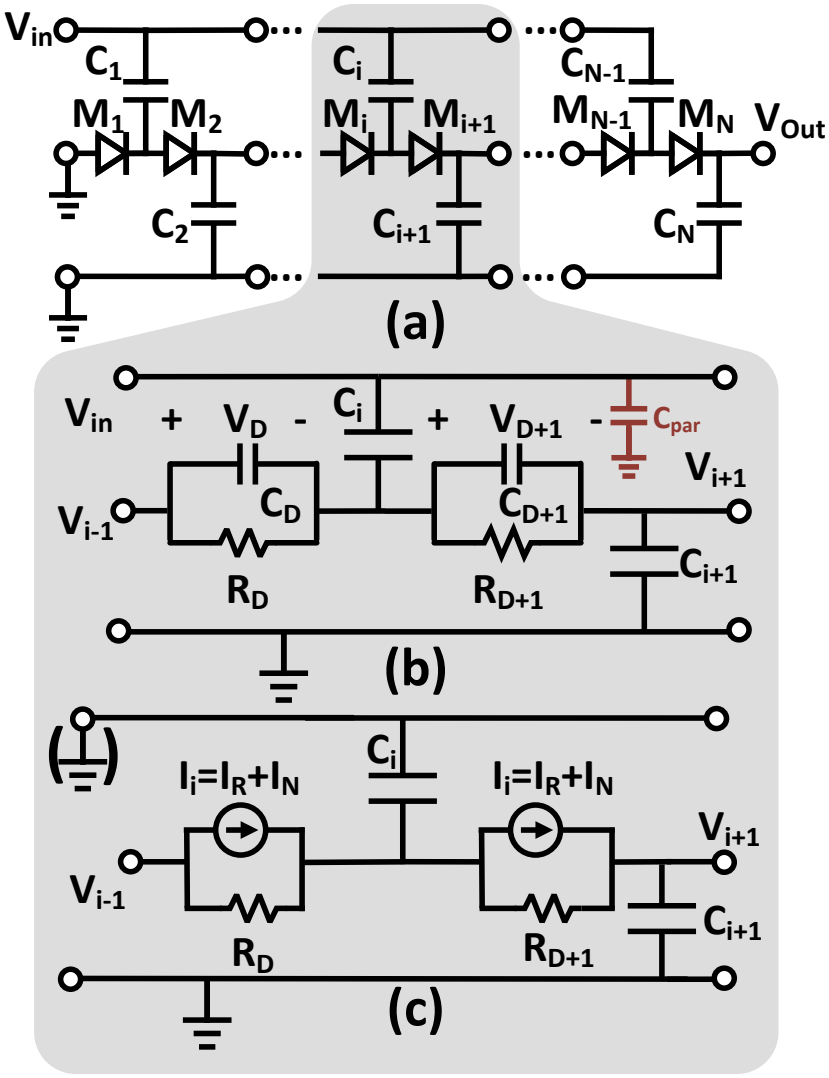


Figure 2.4: (a) Schematic diagram of a Dickson envelope detector with its two decoupled linear network models for a single stage: (b) the RF linear equivalent network and (c) baseband linear equivalent. I_i is defined as the baseband equivalent current through the diode and is composed of the rectified current I_R and the noise current I_N

2.4 Nonlinear device modeling

Frequency conversion is obtained through the use of nonlinear MOSFET devices, which operate in the sub-threshold regime and employ self-mixing of the carrier for down-conversion. The IV

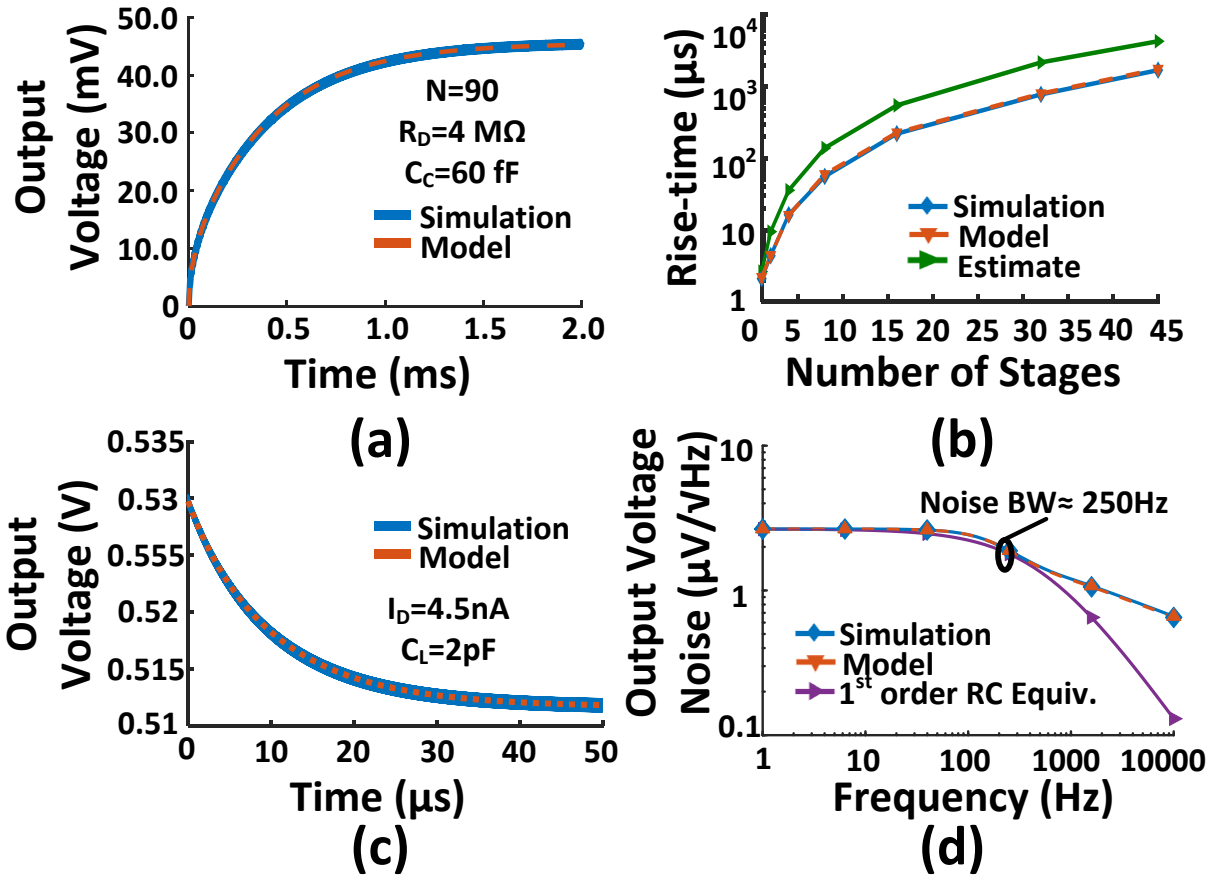


Figure 2.5: Detector performance comparing simulations to models and estimates for the (a) transient of the Dickson detector output, (b) Dickson detector rise time as a function of detector stages, (c) transient of the common-source active detector output where the output signal is the drop in the output voltage, and (d) noise performance of the Dickson detector that show the model accurately predicting the slower roll-off vs frequency compared with a fitted first-order RC equivalent circuit.

characteristics of a sub-threshold MOSFET can be expressed by [47]

$$I_D = I_{D0} e^{V_G/nV_t} (e^{-V_S/V_t} - e^{-V_D/V_t}), \tag{2.5}$$

where n is the sub-threshold slope, $1 < n < 2$, and V_t is the device thermal voltage $I_{D0} \propto \frac{W}{L} e^{-V_{TH}/nV_t}$ for which V_{TH} is the device threshold voltage, and W and L are the device width and length, respectively.

Utilizing the technique outlined in [29], a small RF signal of $V_{in}cos(\omega_{RF}t)$ and $V_{in} << V_t$ are applied to one of the device terminals, and approximating the exponential functions as quadratic functions through application of Taylor series allows for analytical expressions to be developed for the rectifying devices in the structure.

For diode- connected MOSFET devices utilized in the Dickson detector architecture, an important device parameter is the zero-bias device channel impedance R_D. Examining (2.5) for the case of a zero-bias diode connected device, the channel conductance can be found with

$$G_D = \frac{\partial I_D}{\partial V_D}\Big|_{V_D=0} = \frac{V_t}{I_{D0}} = \frac{V_t}{\frac{W}{L} e^{-V_{TH}/nV_t}}. \tag{2.6}$$

2.5 Active detector modeling

Application of the decoupled linear networks allows for the analysis of the sub-threshold regime-active detector circuits. Applying the baseband quadratic voltage-controlled current source across the rectifier device enables the calculation of the output signal. This rectified current drives the output impedance of the rectifying device, where the resultant voltage is superimposed upon the DC bias point of the detector at the output node. For the circuit shown in Figure 2.3b, the transient response can be found with

$$V_O(t) = V_{op} - \frac{I_D}{2(nV_t)^2} V_{RF}^2 R_O(1 - exp(-t/R_O C_O))\ t \geq 0, \tag{2.7}$$

where R_o is the output resistance of the detector which is inversely proportional to the bias current (I_D) of the detector, C_O is the output capacitance at the detector output noise, V_{op} is the output voltage when no RF input (V_{RF}) is applied, and nV_t is the sub-threshold slope times the thermal voltage.

Extracting the OCVS from this expression leads to

$$\alpha = \frac{I_D}{2(nV_t)^2} R_O, \tag{2.8}$$

which, for common source detectors, can be reduced to

$$\alpha = \frac{\sigma_D}{4(nV_t)^2}, \tag{2.9}$$

where σ_D is the constant linking the bias current to the output impedance in the sub-threshold, and the additional factor of two in the denominator is from the reduced output impedance from the biasing current mirror.

The output noise level can be calculated from the baseband equivalent circuit as

$$\overline{v_{n,act}^2} = R_o^2(4kT\gamma_D \frac{I_D}{nV_t}) + \frac{k_f}{Af} \ \frac{V^2}{Hz}, \tag{2.10}$$

where γ_D is the excess noise factor of the device, k_f is the empirical flicker noise coefficient, and A is the area of the input device.

Applying the same procedure for transforming (2.8) to (2.9) to (2.10), we can arrive at

$$\overline{v_{n,act}^2} = \frac{\gamma_D \sigma_D^2 4kT}{I_D n V_t} + \frac{k_f}{Af} \ \frac{V^2}{Hz}, . \tag{2.11}$$

Examining (2.9) and (2.11), it can be seen that the output signal voltage is independent of the bias current, while the output thermal voltage noise level drops with the square root of the bias current. This relationship indicates that the output signal-to-noise ratio is a function of the applied bias when it is dominated by detector thermal noise. Increasing the detector bias current lowers the thermal noise at the detector output while the flicker noise voltage remains constant. Once the flicker noise dominates the detector output noise, increased device sizing is needed to reduce output noise levels further. Unfortunately, increasing the detector devices area increases the input capacitance of the active detector. This increase in input capacitance indicates a trade-off between the output noise level and the voltage boost obtainable for the detector.

2.6 Passive detector modeling

Important relationships for the Dickson detector can be derived from the RF equivalent network shown in Figure 2.4 (b), such as the single stage input admittance,

$$Y_{SS} \approx j2\pi f(C_{par} + 2C_D) + 2/R_D = Y_{in}/N, \tag{2.12}$$

where Y_{in} is the admittance of the detector, C_{par} is the parasitic capacitance associated with each stage, C_D is the device capacitance, R_D is the device channel impedance of the detector, and N is the number of diodes utilized in the detector. The device voltage swing can be found with

$$V_D = V_{RF}\frac{Z_D}{2Z_{Ci} + Z_D} \approx V_{RF}\frac{C_i}{C_i + 2C_D} = K_i V_{RF}, \tag{2.13}$$

where k_i is defined as $C_i/(Ci + 2C_D)$, Z_D is the impedance of a detector diode, and C_i is the coupling capacitor associated with the i^{th} stage.

Equation (2.13) is linked to the baseband equivalent circuit through

$$I_D = \mu_D G_D V_D^2, \tag{2.14}$$

where μ_D is the device open-circuit voltage sensitivity relating the square of the applied voltage to the rectified current, and G_D is the inverse of the device channel impedance. It should be noted that μ_D is primarily a function of device sub-threshold slope which is independent of G_D and can be calculated from

$$\mu_D = \frac{1}{4V_t} \tag{2.15}$$

for a diode-connected MOSFET where the RF input signal has been applied to the source terminal of the device.

These expressions can be used to find the detector output voltage

$$V_O/V_{RF}^2 = \mu_D \sum_{i=1}^{N}(\frac{Z_D}{2Z_{C_i} + Z_D})^2 \approx \mu_D \sum_{i=1}^{N} k_i^2, \tag{2.16}$$

which is equal to $\mu_D N k_i$ assuming that identical stages are cascaded. The output noise power density can be calculated from

$$\overline{v_{n,out}^2} = \gamma 4kT \int_0^\infty \sum_{i=1}^{2n} \frac{|Z_{oi}(\omega)|^2}{R_{D_i}} d\omega, \tag{2.17}$$

where $Z_{oi}(\omega)$ is the Z-parameter associated with the i^{th} diode and the output. The low-frequency spot noise can be found by

$$\overline{v_n^2} = \gamma_D 4kTR_D N \quad \frac{V^2}{Hz}. \tag{2.18}$$

These equations allow for straightforward, accurate calculation of the voltage sensitivity and noise level of the Dickson detector. Note that the single-stage voltage sensitivity is only a function of the sub-threshold slope or ideality factor of the diode and is not related to the channel impedance of the device (R_D). A comparison between the baseband equivalent noise model and the simulation shows strong agreement, and an interesting comparison can be made between the model shown in Figure 2.4 (c) and a single-stage RC equivalent low-pass circuit (with the same noise bandwidth as the Dickson detector). From Figure 2.5 (d), it is apparent that the output noise of the Dickson detector rolls off much slower than that of an equivalent first-order low-pass network. This slow noise roll-off is an important observation, as the Dickson detectors output noise extends to much higher frequencies when compared to a first-order filter response with equivalent 3dB bandwidth. Additional low-pass filtering in the baseband can reduce this effect. The noise extending to high frequencies is due to the distributed noise sources in the Dickson detector, where each noise source requires a different transfer function to the output node, resulting in the gradual roll-off.

The full transient response for the Dickson detector can be found through the application of the lumped linear network theory on the cascaded baseband equivalent circuits

$$V_O(s) = \sum_{i=1}^{N} \frac{I_i Z_{oi}(s)}{s}, \tag{2.19}$$

where $Z_{oi}(s)$ is the Z-parameter associated with the i^{th} diode and the output, and I_i is the rectified current associated with the i^{th} stage.

A useful bound on the rise time of the Dickson detector can be found by examining the dominant

time constant of the baseband network [48] via

$$b_1 = \sum \tau_i^0 = \sum C_i R_i^0 \tag{2.20}$$

$$= [C_1(R_D) + C_1(2R_D)] + ... \tag{2.21}$$

$$+ [C_N(2N-1)R_D + C_n(2NR_D)]$$

$$= (4N-1)R_D C_N + (4N-5)R_D C_{N-1} + \cdots + 3R_D C_1\,. \tag{2.22}$$

Assuming that identical coupling capacitors are used, this expression simplifies to (2.23), which is equivalent to the Elmore delay of the network driven by the first device in the chain. This bound on the dominiant time constant can be used to bound the detector rise time.

Under the assumption that all stages are identical, this expression can be simplified to

$$b_1 = (2N^2+N)R_D C \Rightarrow t_r \approx 2.2(2N^2+N)R_D C_C, \tag{2.23}$$

where C_C is the size of the coupling capacitors, and t_r is the 10% to 90% rise time of the detector. The rise time estimation for (2.23) provides a useful conservative bound that can be used for the estimation of the rise time of the full network. As can be seen from Figure 2.5d, this conservative estimate captures the general trend with respect to rise time and the number of stages and is more compact than the general form.

2.7 A holistic design methodology for passive envelope detectors

In applications targeting a receiver power consumption of fewer than 100 nanowatts, the Dickson detector presents better noise performance than the active detector based on the derivations shown in the next section. A holistic design approach dictated by the impedance boundary conditions imposed on the detector by the system allows for an optimization of both DC power consumption and sensitivity. The boundary conditions presented to the detector are the input source admittance G_S,

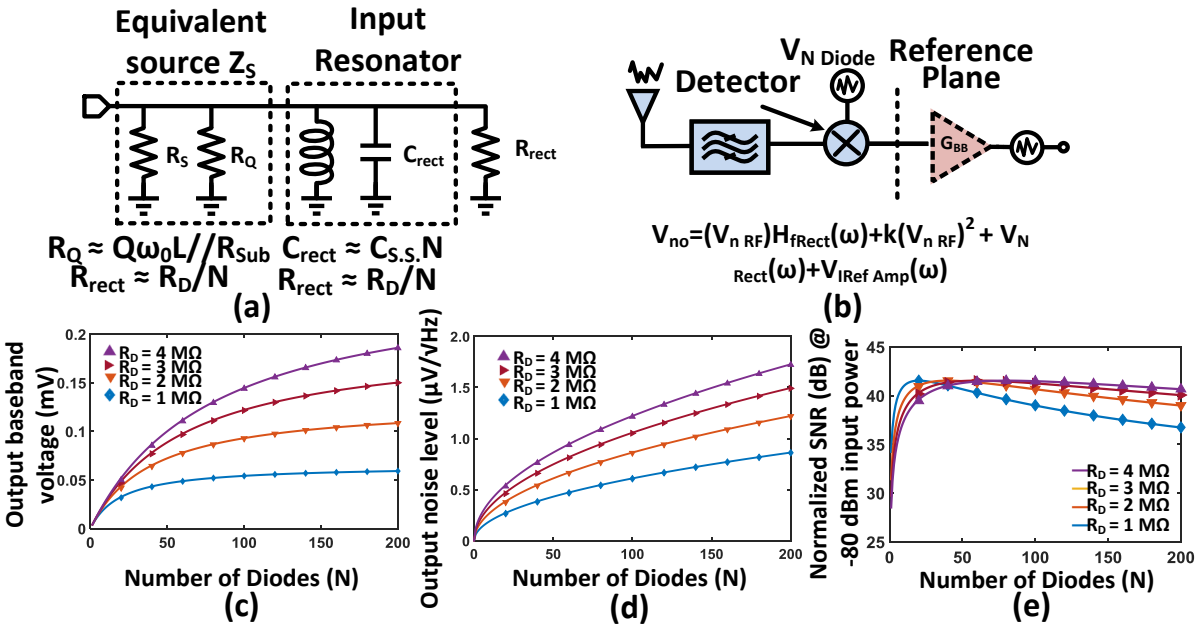


Figure 2.6: (a) Model of a source impedance driving detector at the input RF frequency, (b) noise contributions referred to the output of the envelope detector, (c) detector OCVS across a variety of device channel impedances (R_D) when assuming a constant source impedance of $R_S = 50k\Omega$, (d) output voltage noise level across device channel impedance (R_D), and (e) output signal-to-noise ratio across device impedance (R_D) when assuming a constant source impedance of $R_S = 50k\Omega$ and input RF power level of -80 dBm.

presented by the input impedance matching network, and the input-referred noise of the subsequent baseband circuit.

A co-design between the input source impedance and the detector RF equivalent circuit allows for NEP optimization. Furthermore, this co-design can simultaneously obtain minimal power consumption. Equating amplifier input-referred noise to an equivalent noise resistance allows for the co-design to be considered as a boundary impedance optimization, where the total output noise is the sum of the detector thermal noise (2.18) and the baseband amplifier output noise. The contribution of the RF input noise can typically be neglected for detector-first receivers, as it is heavily attenuated by the conversion loss of the detector [49].

The decoupled linear network models illustrated in Section 2.3 greatly facilitate this holistic design methodology, allowing the RF interface to be treated semi-independently from the baseband interface. The two primary design decisions for the Dickson detector are device channel impedance (R_D) and the number of diodes used in the detector (N). Optimization of detector NEP for N and R_D under the assumption of a finite real admittance $G_S = 1/R_S$ that is independent of detector design allows for sensitivity optimization. The source conductance can be related to the equivalent conductance presented by a matching network and antenna, including losses of the inductor and PCB, or to the source conductance presented by an antenna [30] when considering antenna-matched systems. The constant source impedance assumption requires that the inductor size be independent of the number of diodes in the detector, which occurs when interface parasitics dominate input capacitance.

The output voltage from a detector driven by a constant source resistance (Figure 2.6 (c)) is by found by

$$V_O = \frac{\mu_D N R_D R_s P_{RF}}{R_D + N R_s}, \tag{2.24}$$

where P_{in} is the RF power available from the source and the output signal-to-noise ratio (SNR) normalized to bandwidth can be found by

$$SNR_{out} = \frac{N \mu_D P_{RF} R_D R_s}{(R_D + N R_s)\sqrt{(4kTBNR_D)}} \tag{2.25}$$

or, in the power domain,

$$SNR_{out} = \frac{(N\mu_D P_{RF} R_D R_s)^2}{(R_D + NR_s)^2(4kTBNR_D)}. \tag{2.26}$$

where μ_D is the device open-circuit voltage sensitivity with units of $1/V$. Figure 2.6 (c) shows the output detector voltage as a function of device channel impedance and N, where larger N and R_D lead to higher voltage levels. From Figure 2.6 (e), it can be seen that the optimum detector SNR is invariant to the channel impedance.

Finding the optimum number of diodes with respect to output SNR leads to

$$N_{opt} = \frac{R_D}{R_s}\,. \tag{2.27}$$

Under this optimum condition, the detector's impedance is matched to the equivalent source impedance presented to the detector by the matching network, indicating that a power match is achieved at optimum sensitivity. The SNR for an optimum detector

$$SNR_{opt} = \frac{\mu_D P_{RF}\sqrt{R_s}}{2\sqrt{4kTB}} \propto \sqrt{R_s}\,, \tag{2.28}$$

is a monotonically increasing function of the source impedance, indicating that higher impedance interfaces provide superior sensitivity. It should be noted from (2.29) that the optimum SNR is independent of both the number of detector diodes (N) used and the device channel impedance selected (R_D). In the case of a passive impedance matching network, it should be noted that the source impedance presented to the detector is the impedance of the matching network and the RF power source. This analysis indicates that optimum performance is obtained when both a power match is obtained and the detector and source impedances have been maximized.

$$SNR_{opt} = \frac{(\mu_D P_{RF})^2 R_s}{16kTB} \propto R_s. \tag{2.29}$$

Using (2.27) and (2.29), optimum output SNR is achieved under a power-matched condition but is also strongly dependent upon the source impedance presented to the detector. This dependency indicates that not only is power matching a chief consideration, but presenting the highest voltage

from a given power source is also critical to optimum sensitivity. This optimum output SNR represents under the assumptions the limitation in the achievable sensitivity for ED first receivers.

Choosing $R_D = 1/G_S$ in (2.27) is a valid design choice, as it degenerates the Dickson detector into a single-stage diode detector. Therefore, the utility of the Dickson architecture is not found in improving output SNR when compared to a single-stage diode detector. When considering the performance of the Dickson in a system context, equations (2.24) and (2.29) show that the Dickson detector provides a higher output voltage for a given output SNR. This voltage boosting facilitates the design of a low-power baseband circuit, allowing the full receiver to be scaled towards nanowatt power levels.

Figure 2.6 (b) demonstrates noise sources contributing to the output noise of the detector, where the dominant noise factors for ED-first receivers are the detector thermal noise and input-referred noise of the baseband amplification. Assuming a sub-threshold baseband amplifier follows the detector, the total output noise can be written as

$$\overline{v_{out}{}^2} = \overline{v_{Amp}{}^2} + \overline{v_{Det}{}^2} \approx \frac{\alpha}{I_{DAmp}} + 4kT\gamma_D R_D N, \tag{2.30}$$

where α is a multiplicative constant related to the design of the baseband amplifier, and I_D is the bias current of the baseband amplifier. As increasing R_D and N is equivalent to modifying the output impedance of the detector without modifying the output SNR, a detector output impedance can be chosen to minimize the total noise contribution of the baseband amplifier. This technique is equivalent to modifying the source impedance presented to the baseband amplifier to achieve a better baseband noise figure for a given bias current.

Combining this insight with the preceding result from (2.26), the indication is that low-power operation can be achieved by utilizing a detector with high R_D and N without sacrificing receiver sensitivity. Designing for a fixed baseband noise contribution $\overline{v_{Amp}{}^2}$ and fixed baseband amplifier SNR noise figure is equivalent to designing for a given detector output impedance $R_O = R_D N$, which, when combined with (2.27), gives

$$N_{Opt.Codes.} = \sqrt{R_o/R_s} \tag{2.31}$$

and

$$R_{DOpt.} = \sqrt{R_o R_s}, \tag{2.32}$$

where $N_{Opt.Codes.}$ is the optimum number of detector diodes found via the co-design method, and $R_{DOpt.}$ is the optimum device channel impedance. This set of equations defines both the number of detector diodes to use as well as the device impedance to utilize if the detector designed by these equations has a sufficiently fast rise time, as given by (2.19) or estimated from (2.23).

Examining equation 2.29 and rearranging it into

$$P_{MDS} = \sqrt{\frac{16 SNR_{min} kTB}{\mu_D R_s}}, \tag{2.33}$$

Where P_{MDS} is the minimum detectable signal (sensitivity) and SNR_{min} is the minimum SNR required for detection. SNR_{min} and B are set through the required latency and correlator design, while k and T are physical constants. This leaves two technological parameters μ_D and R_s which can be used to scale sensitivity. Choosing an SNR of 3 (roughly 10dB) and a BW of 50Hz a device OCVS of 10 (for CMOS/silicon devices) and an R_s of $50k\Omega$ leads to a sensitivity of roughly -83 dBm. For both the technology dependent parameters μ_D and R_s there is a 5dB per decade slope in the sensitivity from equation 2.33 and is plotted against RF source impedance in Figure **??**. The obtainable sensitivity should be to first order independent of the power consumption of the subsequent baseband processing.

2.8 Noise comparison between active and passive envelope detector circuits

The choice between active and passive detectors for ED-first receivers and TRF receivers is primarily contingent on two factors, i.e., DC power consumption and RF sensitivity. Both detector types have limited sensitivity due to finite device output impedances, which limits their functionality. A

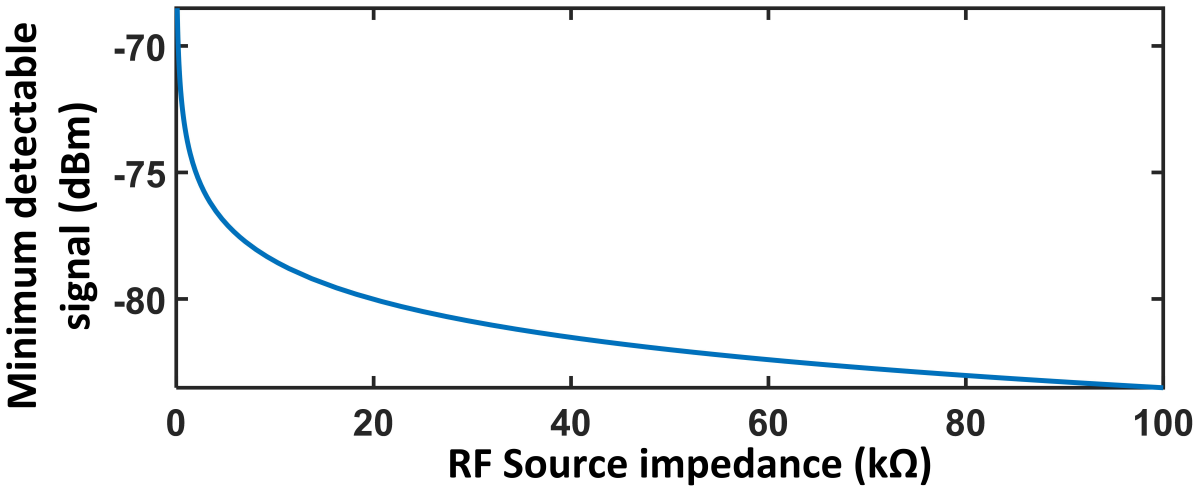


Figure 2.7: Variation on estimated minimum detectable signal of ED first receiver assuming $\mu_D = 10\ V/V^2$ B=100 Hz and $SNR_{min} = 10dB$,

useful metric for comparing detector sensitivity is detector voltage sensitivity normalized to output voltage noise level.

$$\Lambda = \frac{\alpha}{v_{nrms}}. \tag{2.34}$$

This figure of merit is similar to the detector NEP but does not capture the effects of the input impedance matching network; instead, it is purely a function of the detector architecture. One disadvantage of this figure of merit is that it does not take into account the detector input impedance.

Comparing the implemented detector from Chapter 3 (Standard Dickson ED) to an ideal common-source detector with a DTMOS body connection to self-biased leads to Figure 2.8, which shows the passive detector over the active detector biased at less than 100nA.

In order to derive analytically the inflection current when the noise performance of the active detector is superior to the passive detector, we can compare the normalized detector sensitivity between the two detectors and solve for current. Then an application of the results derived in the previous section enables the derivation of the inflection current based on fundamental device parameters. Generally, the voltage loss of the coupling capacitance (k_i's from (2.16)) should be

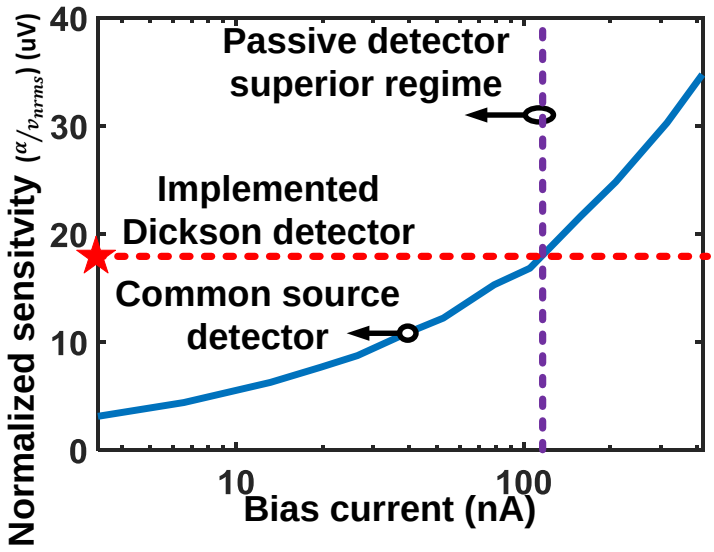


Figure 2.8: Comparison between detector OCVS normalized to output thermal noise for the implemented 45-stage Dickson passive detector and an ideal common-source detector biased in the deep sub-threshold regime.

considered in 2.34 for an exact result. An illustrative example comparing the self-biased common source active detector to the triode-mode Dickson architecture (Chapter 4), we can derive a simple, yet elegant, result.

From equations (2.11) and (2.18), we can see that the thermal noise of the active detector is inversely proportional to the bias current, where the passive detector noise is independent of the bias current since it is a passive device. Equating $A^2_{passive}$ to A^2_{Active} (for analytic simplicity), we can find

$$R_{DOpt.} = \sqrt{R_o R_s}, \tag{2.35}$$

where $N_{Opt.Codes.}$ is the optimum number of detector diodes found via the co-design method, and $R_{DOpt.}$ is the optimum device channel impedance. This equation defines both the number of de-

tector diodes to use as well as the device impedance to utilize if the detector designed by these equations has a sufficiently fast rise time, as given by (2.19) or estimated from (2.23).

$$\frac{N^2}{(4V_t)^2\gamma_D 4kTR_D N} = \frac{\sigma_D^2}{(4(nV_t)^2)^2} / \frac{\gamma_D \sigma_D^2 4kT}{I_D n V_t}, \tag{2.36}$$

which, after simplifying, leads to

$$\frac{N}{R_D} = \frac{I_D}{n^3 V_t}. \tag{2.37}$$

Solving for the I_D when the two detectors are equivalent yields

$$I_D = \frac{n^3 V_t N}{R_D}. \tag{2.38}$$

Assuming that the passive detector has been optimized with respect to its terminal impedances (2.35) and (2.31), equation (2.38) can be reduced to

$$I_D = \frac{n^3 V_t}{R_s}, \tag{2.39}$$

where R_s is the source impedance presented by the impedance-matching network to the detector. The dependence on R_D makes sense intuitively, as the output SNR for the Dickson detector grows with respect to the square root of R_s, while the output SNR for the active detector grows linearly with this parameter. Comparing inflection points calculated from (2.39) of 1.49μA and simulated values using the extracted sub-threshold slope of 1.4 with a source impedance of $50k\Omega$ and an inflection bias current of 1.59μA shows an agreement of $<10\%$ between the simulation and calculation. An identical method applies to the comparison of other active and passive detector topologies.

Equation (2.39) assumes both detectors are driven by a real impedance (where any reactance has been resonated out) equal to R_s. The inclusion of 1/f noise degrades the performance of the active detector relative to the passive detector, but this analysis does indicate a lower bound on the performance of the passive ED relative to the active ED. Further complicating this analysis, the active detector typically presents much higher capacitive loading than the passive detector when sized for 1/f noise.

A graphical plot of this inflection point is found in Figure **??** which assumes a subthreshold slope of 1.3 and a temperature of 300k. The wide range of source impedances reflects the wide range of possible applications for these detectors where the obtainable source impedance drops with frequency, and is dependent upon receiver architecture.

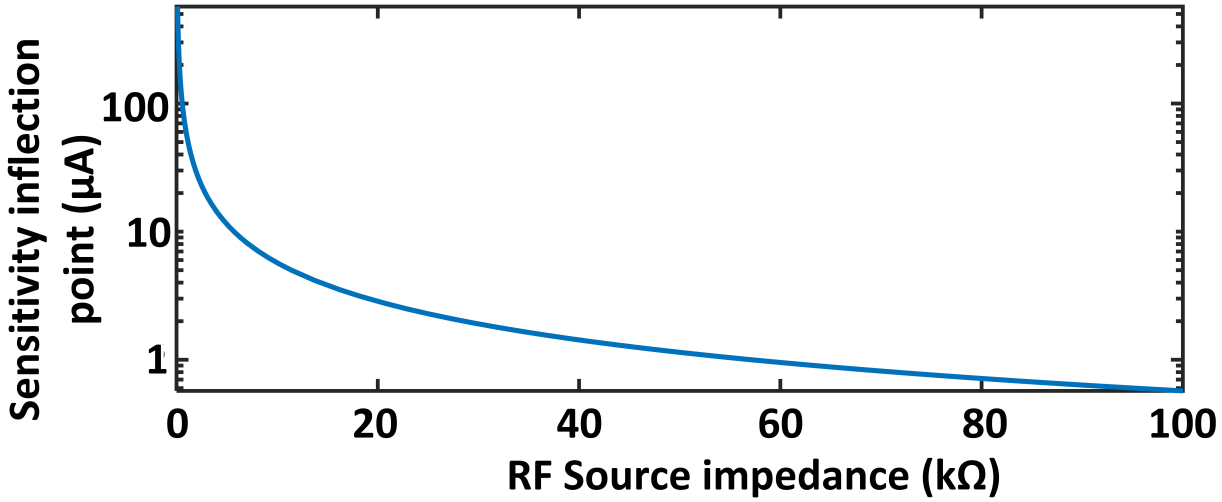


Figure 2.9: Bias current at which active detector sensitivity normalized to thermal noise flood is equal to that of an ideal passive detector across varying source impedance.

2.9 Detector test structure measurement results

A passive ED test structure chip (Figure 3.9)) was fabricated using the Global Foundries US (GFUS) 130nm RF CMOS process to verify the modeling techniques presented in this chapter. The measurement results generally corroborated the modeling techniques but showed their limitations in modeling the passive detector associated with process variation. The techniques for ED optimization shown in equations (2.27), (2.31), and (2.35) as well as the models presented in equations (2.12), (2.18), and (2.23) assume a fixed and known R_D. Unfortunately, the very high sensitivity of the device channel impedance (4.2) makes accurate modeling of these detectors difficult due to the highly variable nature of this term for process and temperature variation. Fortunately, a modified topology to be presented in Chapter 4 overcomes many of these limitations.

The test structures utilize primarily three different devices types: Low-Threshold Voltage RF NFETs (LVTRF), Zero-Threshold Voltage NFET (ZVT), and Zero-Threshold Thick Oxide NFET devices (ZVTDG). The primary characterization of the ED includes input impedance, rise-time, and OCVS. The EDs were characterized by the measurement set-up detailed in Figure 2.11.

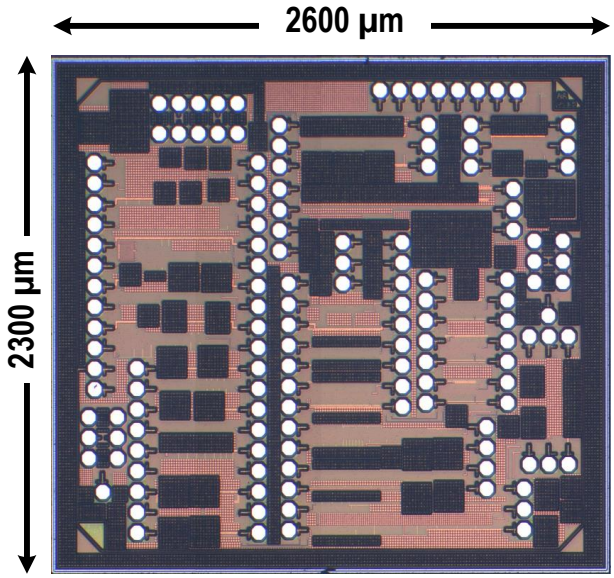


Figure 2.10: Die photo of envelope detector test structure chip, where each row of pads has detector inputs and outputs on every other pad.

The input impedance characterization, as shown in Fig. 2.12, is accomplished with a Keysight PNA-X vector network analyzer and MPI titan wafer probes. This measurement is challenging due to both the very high impedance nature of the ED input and nonlinear nature of the device, i.e., strong excitation drives the detector into a more nonlinear regime. The non-linearity restriction means that the input RF voltage for probed input impedance measurements limits the available power of the 50Ω source to less than -30 dBm, which introduces significant noise into the measurement. Wide variation in channel impedance with process and temperature also introduces some deviation between simulation and measurement, but an overall agreement is observed between measurements and simulation.

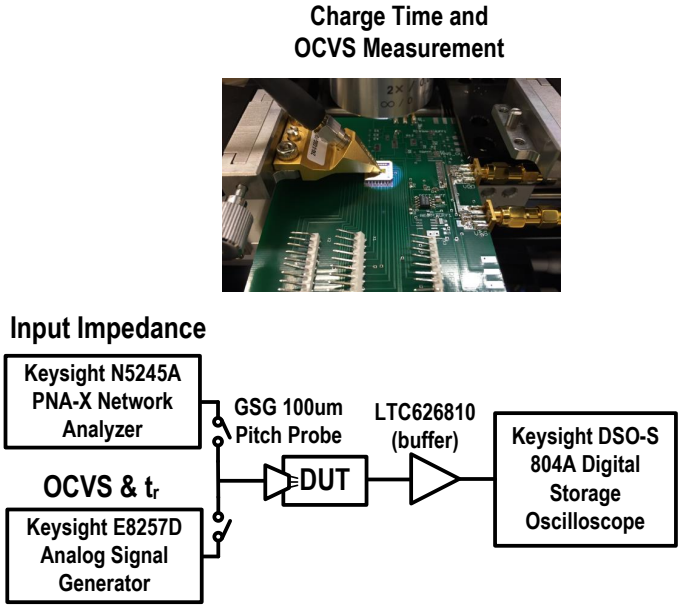


Figure 2.11: Measurement set-up used to characterize detector OCVS, input impedance, and rise time.

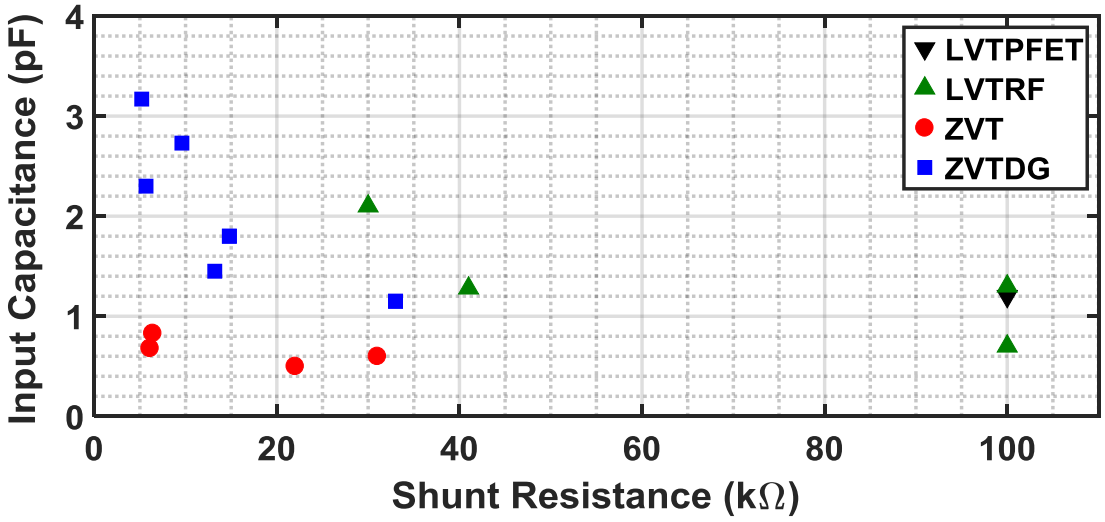


Figure 2.12: Input impedance across various device types, number of stages, and coupling capacitor designs.

OCVS measurements require a very high input resistance buffer, necessitating the use of an FET input OP-amp to observe the output such as the LTC6268 utilized. A Keysight (MXG N5183B) signal generator forces the input RF signal and a Keysight 804ADSO is used to record the rectified DC voltages. Fig. 2.13a shows the detector OCVS normalized to a 1Ω source impedance, showing strong agreement between simulation, modeling, and measurement. The strong agreement between simulation, modeling, and measurement indicates that the uncertain diode R_D has degraded the accuracy of the charge time and input impedance measurements.

Rise-time measurements are accomplished with the same setup that was used for the OCVS measurements, as shown in Fig. 2.13b. The accuracy of the rise-time measurements can be improved with the addition of an on-chip buffer circuit, which avoids the significant additional capacitive loading associated with an onboard OP-Amp, chip carrier, and PCB traces. Fig. 2.14 indicates the inherent trade-off between OCVS and rise time, where the coupling capacitor size and number of stages were varied and characterized versus OCVS and rise time.

2.10 Conclusions

The proposed detector models are accurate, compact, and robust in predicting the performance of square-law EDs. These models show excellent agreement with simulated results; this accuracy allows a complete co-design methodology based upon the terminal impedances presented to the system. The development of a simple analytical technique to compare detector architectures has enabled better trade studies between various topologies. Exploring the limitations and behavior of these architectures allows for the invention of more effective detector architecture. This work also contributes to the development of receivers approaching fundamental sensitivity limitations.

This work has both enabled near-zero-power high-sensitivity receivers, as well as provided a design framework from which the design of detector-first receivers can be accomplished. Further, the fundamental sensitivity limitations presented in (2.26), (2.9), and (2.11) enable an analysis of the fundamental sensitivity limits of detector-first receivers based on technological and application-

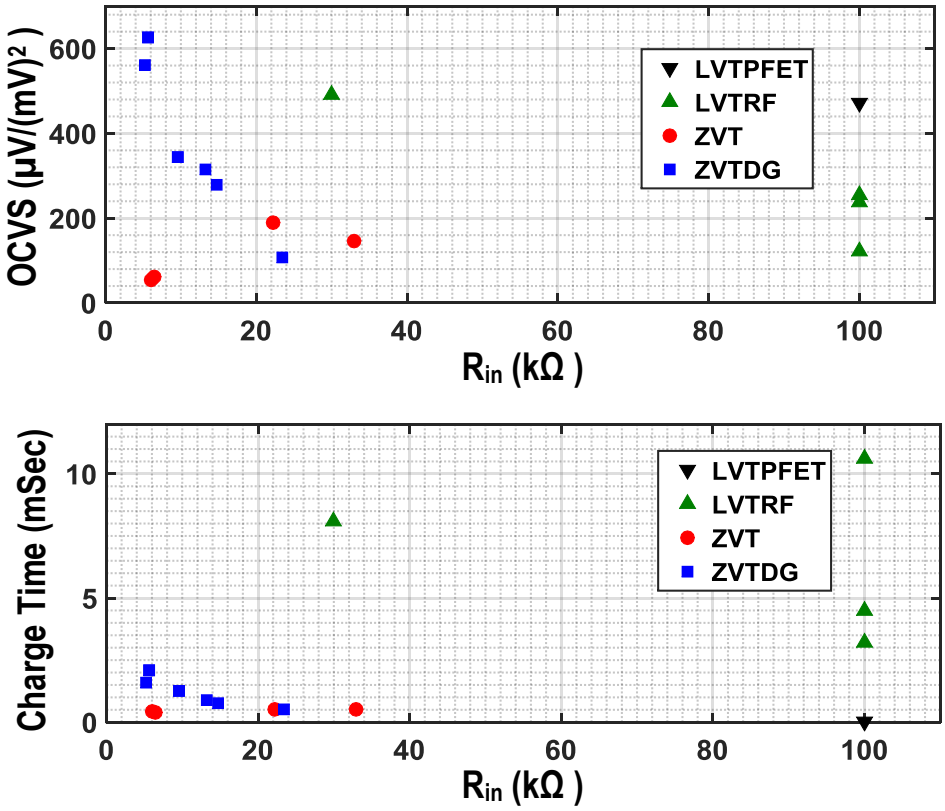


Figure 2.13: OCVS and rise-time versus envelope detector input shunt resistance, where lower resistance corresponds to higher N, demonstrating that a higher n leads to increased rise time and higher OCVS.

specific constraints.

2.11 Contributions

1. Developed decoupled linear network models for modeling behavior of ED circuits.
2. Applied decoupled linear network analysis to accurately model the detector sensitivity, output noise, input impedance, and transient response.

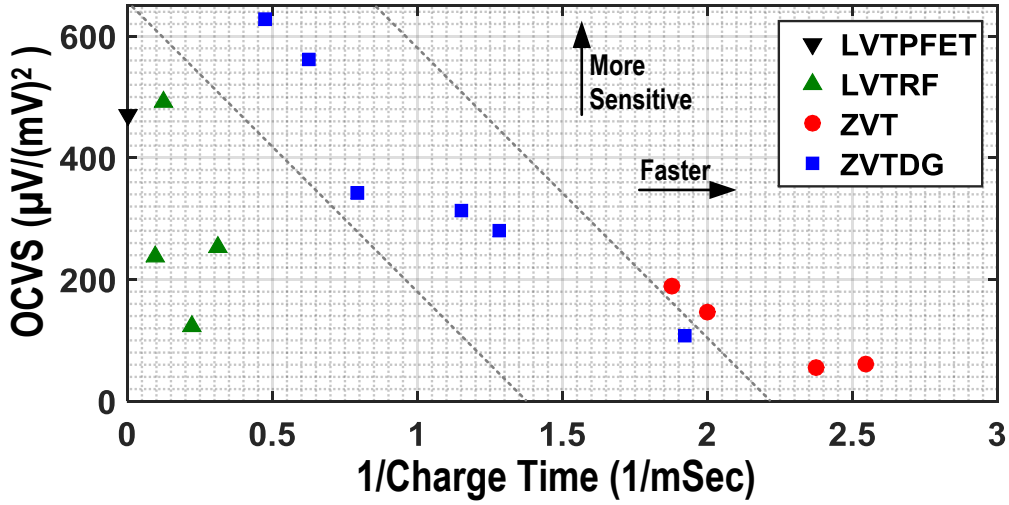


Figure 2.14: Measured rise time versus OCVS illustrating that large N and coupling capacitors improve OCVS and degrade rise time performance.

3. Developed co-design methodology between matching network, ED, and baseband circuitry.
4. Developed theory comparing active and passive detectors, thus enabling robust comparisons between architectures.
5. Taped out test structures verifying the modeling of the detectors.

This work was done in collaboration with Pouyan Bassirian.

CHAPTER 3

INTERFERENCE ROBUST DETECTOR FIRST NEAR-ZERO POWER LEVEL WAKE-UP RECEIVERS

Our work on the detector-first architecture has achieved performance comparable to the of the sub-10nW design space and at the time of publishing pushed the state of the art further in sensitivity and robustness. The receiver demonstrated a state-of-the-art sensitivity of -76 dBm with a DC power consumption of 7.6 nW (Figure 3.1). The high sensitivity and low power consumption is enabled by the co-design methodology outlined in the previous chapter. This performance will enable operation from single battery supply and allow wake-up nodes to be separated by hundreds of meters. This work lead to the publications [50], [51], [52], and [53].

One crucial development has been the combination of the ED with an ultra-low-power baseband low- noise amplifier. These blocks were co-designed for optimum power and noise performance. This work is contrasted with recent developments utilizing an active ED whose design was explored but found to be fundamentally noisier when compared to the passive detector at extremely low bias current. The optimization of this passive detector has allowed it to achieve lower input capacitance when compared to the active detectors. Finally, this front end demonstrated a novel offset compensation algorithm which allowed for in-band interference rejection in the presence of non-constant envelope interferers.

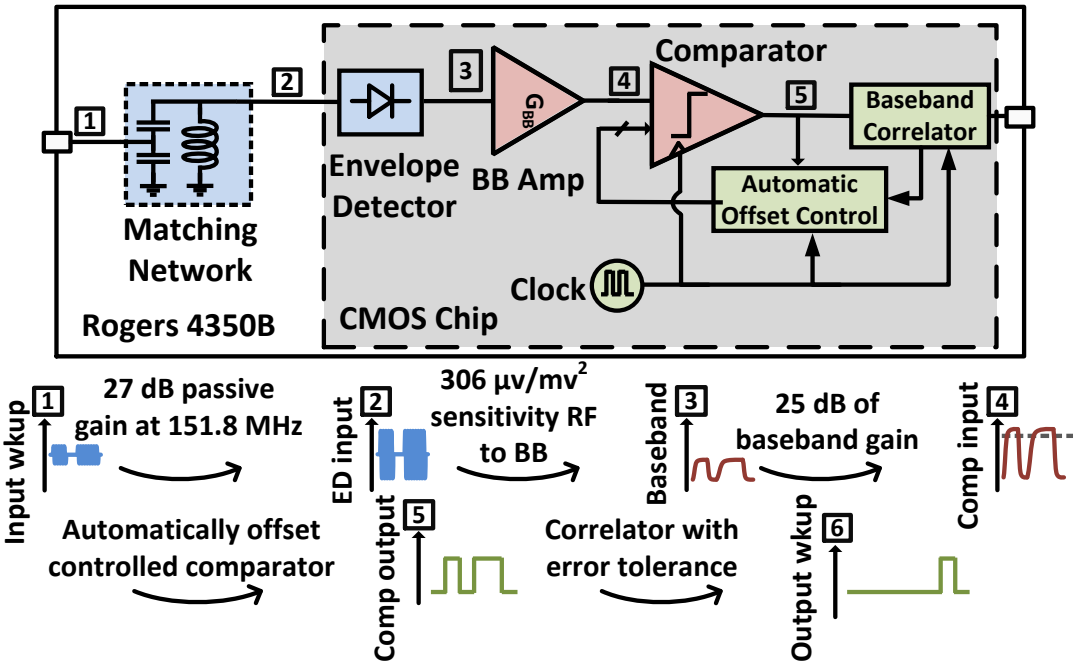


Figure 3.1: Block diagram of the wake-up receiver showing waveforms from the RF input through the digital wake-up output.

3.1 RF front end

The CMOS RF front end is co-designed with a discrete tapped capacitor transformer to maximize the SNR at the output of the ED. The matching network inductors shunt conductance limits the achievable passive voltage gain of the transformer. Minimizing the input capacitance of the ED by reducing the number of detector stages enables the use of larger and higher quality factor inductor's with smaller shunt conductances, which optimizes the voltage gain.

Comparing the performance of the passive Dickson detector and the active detectors shows that the noise performance of passive (Dickson) detectors becomes superior when currents are restricted to less than several hundred nA. This degradation is due to the output thermal noise levels of active EDs, such as common-source and common-gate architectures, degrade considerably at extremely low bias currents. Additionally, passive detectors with zero-bias, diode-connected transistors have no flicker noise, erasing the trade-off between flicker noise corner frequency and input impedance.

The ED is optimized for operation in the 151.8 MHz band, where a 45-stage, low-threshold voltage device ED provided a minimum NEP of 170 fW/Hz in simulation, with an overall measured voltage sensitivity ranging from the 50 Ω input to the 15 mV/nW output of the detector. A second transformer was designed and implemented for the 433 MHz band which achieves a voltage sensitivity of 7 mV/nW.

3.2 Envelope detector implementation

Aiming to achieve high sensitivity and a DC power consumption of less than ten nW system power, the detector is designed using the boundary-condition-based optimization presented in the previous chapter. A bit-rate of 200 bps, which corresponds to a $5ms$ integration time and wake-up latency of under $100ms$, is used.

A bond-pad capacitance 270 fF, estimated PCB interconnect capacitance of 1 pF, and estimated inductor Q-factor of 120 provide an approximate model for the source impedance presented by

the matching network, which is estimated to present approximately $40k\Omega$ at resonance. A BB amplifier noise figure of 1 dB is chosen as the second design parameter. Based upon the required rise time, BB amplifier noise figure, and required rise time, the output impedance is set by (2.31) and (2.35), which corresponds to an output impedance of greater than 300 MΩ being required from the detector.

A 45-stage Dickson detector is implemented with low-threshold voltage devices (W/L equals 300nm/300nm) which exploit the reverse short-channel effect. As the transistor length increases [54], the transistor threshold voltage decreases, lowering channel impedance through the (4.2). This technique lowers the device channel impedance to $\approx 4M\Omega$ and presents an output impedance of greater than 300 $M\Omega$. The rise time is estimated from (2.23) to be faster than 5 ms and is simulated to be $\approx 2ms$. The coupling capacitors utilized were $60fF$, which corresponded to the smallest metal insulator metal (MIM) capacitors in the design kit. Body bias tuning is implemented through the use of triple-well devices, allowing for dynamically setting the channel impedance to account for process and temperature drift.

3.3 Baseband analog amplifier and filter design

The baseband analog amplifier and filter consists of a self-biased modified cascode amplifier, followed by a common drain impedance buffer and an ultra-low-power ground reference comparator with wide dynamic range. The design goals of the analog baseband circuitry are minimal DC power consumption, wide decision voltage range, and maximum sensitivity.

The baseband amplifier shown in Figure 3.2 is primarily designed with conservation of DC power in mind. A single-ended architecture is utilized to save DC power at the expense of supply noise rejection. Due to the ground referenced nature of the rectifier, a ground-referenced baseband amplifier is implemented as a modified cascode amplifier with the input device replaced with a PFET, allowing for a fully ground-referenced operation. The dynamic range improves due to the ground-referenced nature, as the polarity of the input RF signal is always positive, meaning that the ampli-

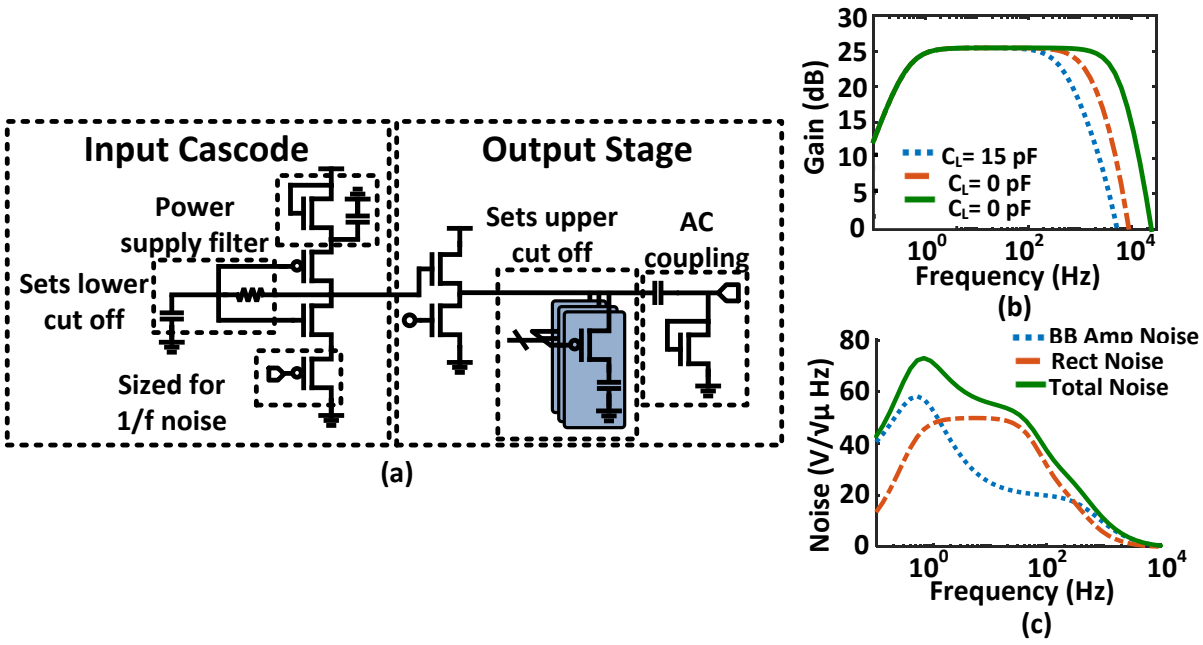


Figure 3.2: (a) Implementation of a band-pass baseband amplifier circuit, (b) simulated gain for various bandwidth settings, and (c) simulated noise contributions referred to comparator input where the noise powers are added at the output to calculate the total noise.

fier swing can be improved by optimizing the voltage bias for a purely positive swing. A zero-pole pair is inserted into the transfer function through the self-biasing circuitry to reduce the susceptibility of the receiver to constant envelope interference, improving the robustness of the design. The limitation for constant envelope interference occurs when a sufficiently strong signal drives the baseband amplifier into compression. As the supply voltage is set by the digital requirements, additional headroom is available for the baseband amplifier, allowing for a series low-pass filter to be inserted in the series with the bias path to reject supply noise, increasing the robustness of the design. A tunable first-order low-pass buffer and filter stage following the input amplifier sets the baseband bandwidth of the system and provides impedance buffering to reduce comparator kickback. Comparator kick-back is charge injection from the switching comparator into the high

impedance analog amplifier. The DC power is primarily set by the noise requirements imposed by the output noise of the rectifier. Both amplifiers combined draw 2.0 nW from a 0.6 V supply and only degrade the SNR by $\sim$1 dB for detector output noise while adding a mere simulated $45fF$ of capacitive loading on the detector.

3.4 Automatic offset control loop

Automatic Gain Control (AGC) is typically employed by receivers to account for environmental drift and varying interference levels in receivers. In a data receiver, the input signal is about 50% ones and 50% zeros, and the costs of a false positive and a false negative are roughly equal. In this case, the threshold should be set halfway between the ones level and the zeros level, which requires an RF input training sequence to find the ones level. In contrast, in the context of wake-up receivers designed for a very low activity factor, externally generated RF input training sequences are not available, which means that calibration must be functional in an all-RF quiet environment. An example of an offset compensation algorithm for wake-up receivers is seen in [3], where it is found to reject continuous wave interference. Additionally, the ideal comparator error rates may not correspond to equiprobable false ones and zeros, as the distribution of the incoming RF ones and zeros is heavily skewed towards more zeros. Furthermore, the cost associated with a false wake-up is very application-specific, meaning that no individual false ones rate exists for a given receiver across all applications.

An ideal gain/offset compensation algorithm in the event-driven WuRx context requires the ability to deal with time-varying aperiodic interferers that could be either a constant envelope or pulsed. Furthermore, this algorithm should accommodate a varying environment with respect towards process and temperature variation. This algorithm needs to achieve optimum performance for a desired false wake-up rate, all without external RF calibration signals.

Exploiting the event-driven nature of wake-up receivers, an algorithm is devised to determine the optimal threshold voltage by setting a fixed probability of a false alarm from the wake-up receiver

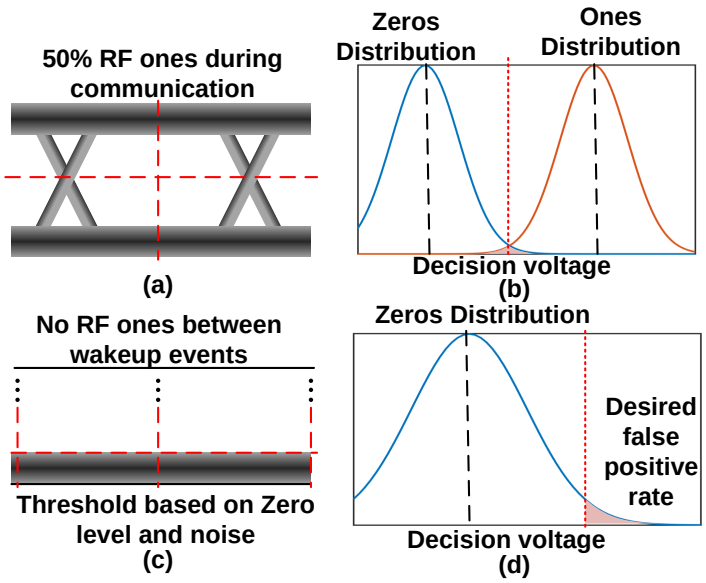


Figure 3.3: (a) Eye diagram showing the decision voltage obtained by a classic AGC algorithm; (b) classic binary decision problem optimization, where the optimum decision voltage is based on the minimum bit error rate, including both false positives and false negatives; (c) WuRx all-zeros 'eye' diagram during the quiet time between the wake-up signals that the algorithm must operate in that lacks a received ones level; and (d) decision voltage set to maximize sensitivity while maintaining an optimum false positive rate when the RF input is quiet.

without any external calibration and is shown in Figure 3.3. The system-level specifications define the acceptable false alarm rate and, in the context of an 8-bit code and 200 Hz clock rate, corresponds to a 2 $\%$ rate of false positives, leading to one false alarm per hour. When operating in the state that gives the set false alarm rate, the radio operates in its maximum sensitivity state with regards to input signals. The algorithm based on the flow chart shown in Figure 3.4 manages the offset state. A time delay in adjusting the threshold is built to account for real wake-up events. After waiting for the predetermined period without comparator positives, the offset is then decremented. Ideally, the comparator offset will continually fluctuate between three adjacent offset

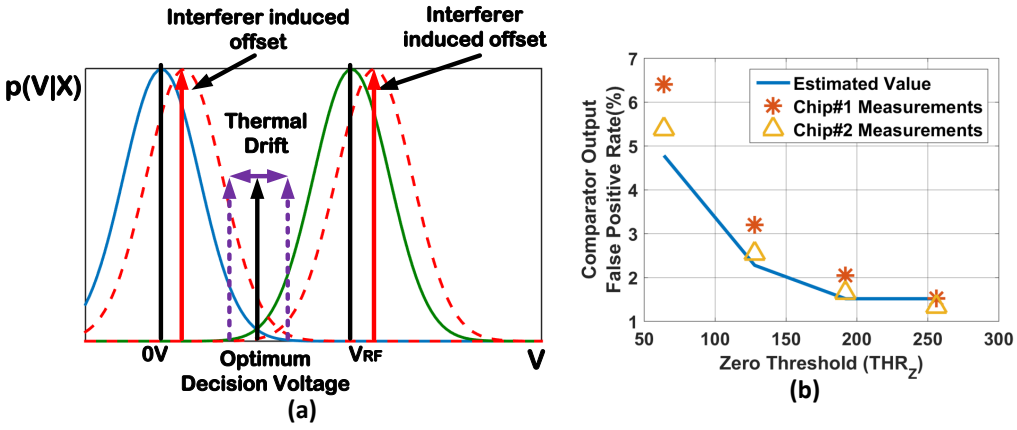


Figure 3.4: (a) Flow chart of the automatic offset control algorithm that can operate without any input from RF ones and optimizes the comparator decision voltage to maximize sensitivity while maintaining a digitally controllable optimum false positive rate. (b) Comparison between the estimated convergence and measured convergence of the offset compensation algorithm.

states for which the error statistics are close to ideal.

This algorithm allows the system to self-calibrate out interference, including in-band On-Off Keyed (OOK) modulated interference, which presents the most challenging type of interference in ED-first receivers. When interference first activates, it causes a large number of comparator false positives, which are rejected as the comparator threshold increases. After the offset is increased, the total sensitivity of the receiver is reduced, as only RF signals stronger than the interferer can trip the comparator. Overall, this algorithm enables functionality even in the presence of an in-band pulsed interference which is strong relative to the signal strength. The convergence speed of this algorithm is a linear function of both the sample clock rate used in the system as well as the number of offset steps required for the desired false positive rate. For a single offset state change, a total time of 50ms (10 sample clock cycles) is required to account for the possibility of a wake-up code being sent. The dynamic range of the comparator presents the primary limitation on the

Table 3.1: Summary of performance and comparison to the state-of-the-art

	This Work	SSCL '18	JSSC '18	ISSCC '16	RFIC '17	CICC '12
Technology	130 nm	180 nm	180 nm	65 nm	65 nm	130 nm
Carrier Frequency	151 MHz || 433 MHz	109 MHz	113.5 MHz	2.4 GHz	2.4 GHz	433 MHz
Band	MURS || ISM LPD433	N/A	N/A	ISM	ISM	ISM
Wake-up Sensitivity[1] (dBm)	$-76 \|\| -71$	-80.5	-69	N/A	N/A	$-45 \|\| -43 \|\| -41$
Sensitivity BER[2] (dBm)	-75 || N/A	N/A	-65^{1}	-56.5^{2}	-61.5^{2}	N/A
Normalized Sensitivity[3] (dBm)	-81.5 || -76.4	-84.2	-68.5	-68	N/A	-58
Power Consumption (nW)	7.4 || 7.4	6.1	4.5	236	365	116
Voltage (V)	0.6/1.0	0.4	0.4	0.5/1.0	0.8	1.2/0.5
Latency (s)	82.5m	180m	53.3m	4m	1.28m	2.48m
Data Rate	200 bps || 200 bps	33 bps	300 bps	8.192 kbps	2.5 kbps	12.5/31 kbps
Energy per bit (pJ)	37 || 37	184	15	28.8	146	0.98
Non-constant Envelope Interferer rejection	Automatic Offset Control Loop	N/A	N/A	N/A	N/A	Threshold Control
Out-of-band Interferer Rejection Method	High-Q FE Transformer	High-Q FE Transformer	High-Q FE Transformer	Matching Network	High-Q Antenna codesign	Matching Network
SIR (CW) (dB)	-30 (MURS) || -28 (ISM)	N/A	-15	N/A	-19.1	-3.3
Detector Arch.	Passive	Passive	Active	Passive	Passive	Passive
Die Area	$1.95mm^2$	$6mm^2$	$6mm^2$	$2.25mm^{2*}$	$1.1mm^{2*}$	$0.35mm^{2*}$

1. Measured at 0.1% missed detection rate at $<$ 1 False alarm an Hr
2. Measured at BER = 10^{-3}
3. Sensitivity normalized to 1/Latency accounting for square law behavior
4. Full wake-up functionality at -30 dB CIR, tone at 3 MHz Offset
5. BER = 10^{-3} with -10 dB CIR at 2 MHz offset
6. BER = 10^{-3} with -19 dB CIR at 3 MHz offset
*Active Area

dynamic range over which this algorithm operates.

The implemented algorithm consumes one nanowatt of DC power from a 0.6 V supply. The algorithm was designed in a sub-threshold digital design flow, and the Verilog implementation only consisted of low-power components such as counters and digital comparators. The total state machine consisted of 16 registers, which allowed for the near zero-power implementation.

3.5 Measurement results and characterization

The WuRx was fabricated in a 130-nm RF CMOS process. A summary of measurements and a comparison to the state- of-the-art is shown in Table 1. The chip is mounted on a Rogers 4350 PCB as a chip-on-board package to reduce parasitic capacitance. A lumped off-chip network is utilized to provide a passive voltage boost.

The envelope detector input capacitance is measured as a 650 fF input capacitance at 150MHz using on-wafer probed S(1,1) measurements taken with a Keysight PNA-X VNA. Due to the high Q-factor and high impedance presented by the detector, accurate measurements on the real part of the input impedance are challenging to accomplish with a standard VNA-based measurement. The

front-end voltage sensitivity is shown in Figure 3.5a, where the detectors OCVS is measured across the frequency with a low impedance of 50 Ω and a reference RF input voltage. Power sensitivity measurements are accomplished by adding one of two matching networks at the 151.8 MHz MURS (Multi-Use Radio Service) band and the 433 MHz ISM (Industrial, Scientific, and Medical) band. Front- end Q factors are measured as 55 and 40 for these matching networks, respectively. The degradation at the 433 MHz frequency is due to the reduction in the shunt rectifier resistance at the higher frequency, resulting in additional losses on-chip, as well as the lower Q factor of inductors available at this frequency. The reflection coefficient was measured to be less than 10dB for both devices, and the matching network gains were measured as 27dB and 25 dB for the MURS and ISM matching networks, respectively.

The measured transient response of the front-end output is depicted in Figure 3.5b. The effect of forward body biasing on the detector charge time is shown in Figure 3.5c. By changing the body biasing, the charge time can increase from 5 ms to 970 μs across a 0.35 V body bias range with a maximum leakage current of $<$ 1nA. The measured charge time of 4.96 ms is slower than the simulated value of 3 ms, likely due to a process fluctuation in the detectors zero-biased diodes.

The receiver sensitivity is measured at an RF false wake-up rate of $<$1 /hr, and a probability of the missed detection at 10^{-3} to an input of -76 dBm at 151.8 MHz is obtained. This detection rate is measured out of the 8-bit correlator with 3 bits of error tolerance, as shown in Figure 3.6. A half-clock cycle phase-shifted RF transmission is sent after the initial transmission to protect against asynchronization (TX and RX clock phase misalignments degrade sensitivity) between the transmitter and receiver. In the worst case, doing so correlates to an approximately 1.3 dB degradation in baseband signal level or a 0.65 dB degradation when referred to the RF input. The detector BER was measured using a PRBS 5 pattern at 200 bps to de-embed the sensitivity of the front end from that of the system including the correlator and is measured to be -75 dBm at 10^{-3}. The bit interval for the PRBS test was equal to the rise time, which degraded the sensitivity of this bit interval by $< 0.3dB$.

Further tests are performed with both constant envelope interference and non-constant envelope

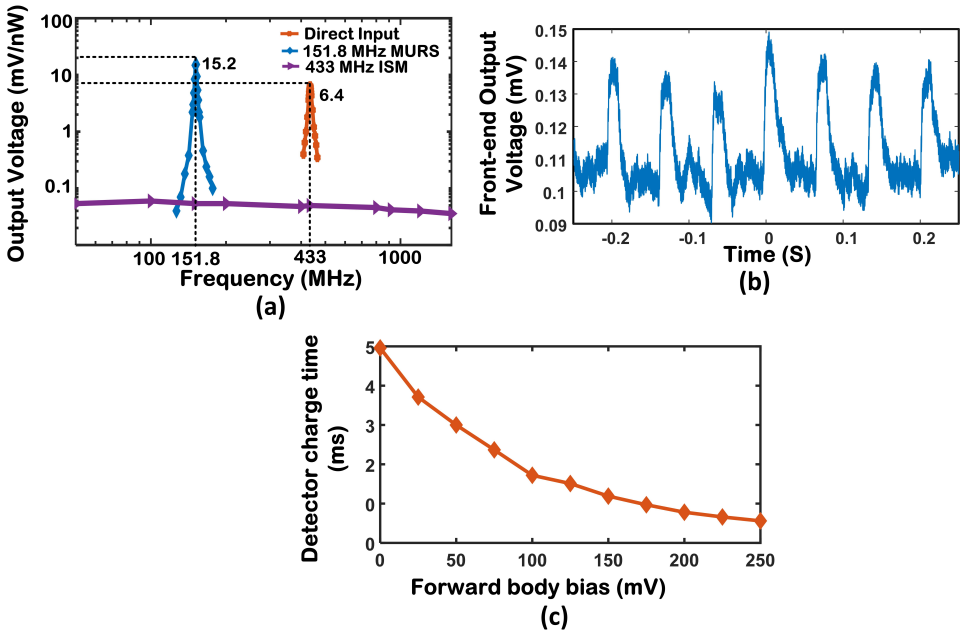


Figure 3.5: (a) Measured output signal from a baseband amplifier with an -77dBm input signal when directly connected without a matching network, with a 151.8 MHz MURS band matching network, and with a 433 MHz ISM band matching network; (b) measured transient output voltage of the front end, including a baseband amplifier at 433MHz and -66 dBm input signal at 200bps; (c) measured tunability of detector charge time as a function of forward body bias voltage.

interference utilizing a tone at a frequency offset of 3MHz from the center RF frequency. Due to the band-pass baseband response and the wide dynamic range on the comparator, the receiver is able to operate at the -76 dBm sensitivity with a -46 dBm interferer present. The rejection is eventually limited by linearity on the baseband amplifier and ED. The interferer performance across the offset frequency is measured at the 433 MHz ISM band and is shown in Figure 3.7. This measurement demonstrates a robustness to 27 dB CIR interferers at a small frequency offset of 20kHz under nominal wake-up sensitivity. A comparison to the existing state-of-the-art wake-up receivers shown in Table 1 shows state-of-the-art sensitivity for sub-microwatt receivers operating in commercial bands with a DC power consumption of fewer than ten nanowatts.

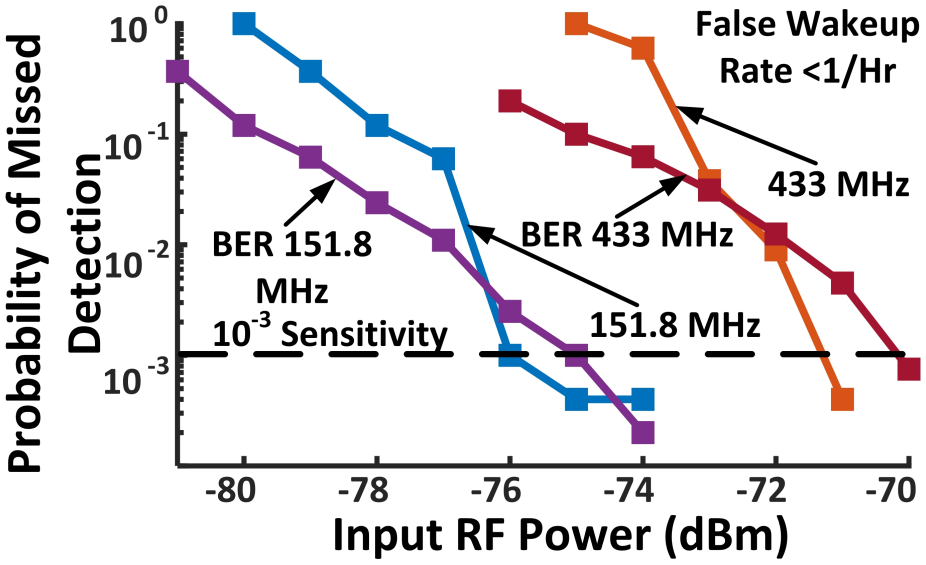


Figure 3.6: Measured receiver operating curves demonstrating a $10^{-}3$ probability of missed wake-up detection sensitivity of -76 dBm at 151 MHz and -71 dBm at 433 MHz with a false wake-up rate of less than one per hour. The measured bit error rate (BER) for the MURS matching network and 200bps PRBS- generated signal showing -75dBm sensitivity for the BER measurement.

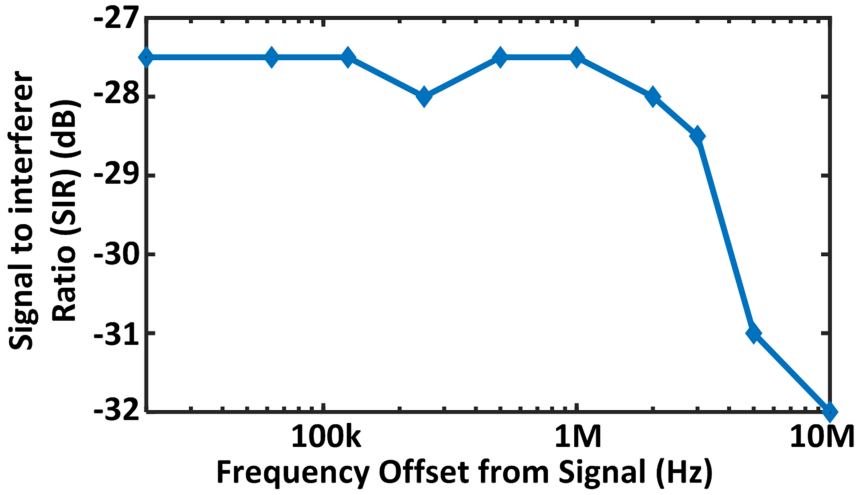


Figure 3.7: Measurement of wake-up mode interference robustness for a narrow-band CW blocker versus the frequency offset of the 433MHz band at nominal sensitivity.

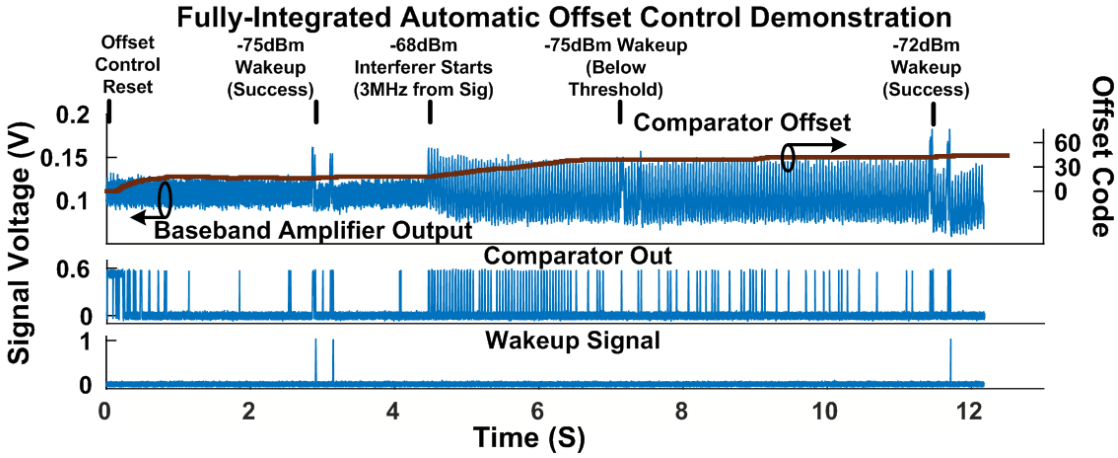


Figure 3.8: Measurement of the automatic offset control algorithm initialization and offset settling allowing for the detection of a -75 dBm signal, followed by the rejection of a -68 dBm OOK interferer and successful detection of a -72 dBm signal in the presence of the interferer signal.

A demonstration of the automatic offset control algorithm is shown in Figure 3.8. The operation in the presence of time-varying interference, as well as the start-up self-calibration of the receiver, is shown. Initially, the receiver is activated at the minimum offset point at which the probability of comparator false positives is very high; therefore, the compensation algorithm automatically adjusts the threshold to a value which obtains the set false-one rate required for optimal performance. A wake-up signal is then sent at a -75 dBm power level and detected. A pulsed -68 dBm signal is modulated at the sampling clock frequency and then sent into the receiver at a 3 MHz offset from the RF center frequency. The output signal of the interferer is stronger than the -75 dBm wake-up signal, meaning that it blocks the receiver, as it is in-band and at a baseband frequency similar to the wake-up signal sent at -75 dBm. This pulse rate is set to be the same as the comparator clock rate, which is a worst-case scenario, as the analog baseband does not filter it. As the pulsing interferer creates a high number of comparator false positives, the offset control algorithm raises the comparator threshold to suppress the interference. Afterwards, a wake-up signal at -72 dBm is sent and detected, demonstrating that while the sensitivity of the WuRx is reduced, the receiver maintains functionality. PCB and die photos are shown in Figure 3.9.

3.6 Conclusions

Initially, the sensitivity bottleneck in nanowatt-power-level receivers was related to process limitations in both the minimum trip voltage of the comparator [55] and the detector OCVS. Through the co-design of an ED and an ultra-low-power low-noise amplifier as well as an integrated offset compensation algorithm, the bottleneck is moved to a combination of the detector noise limitations and the comparator kickback noise.

(2.29) shows an expression relating to the obtainable sensitivity of the passive detector front ends. The detector-first architecture is rapidly approaching fundamental sensitivity limits set by the output thermal noise of the detector and the obtainable matching network Q which is defined by the optimal output SNR of the detector defined in the last chapter. Improving this architecture beyond

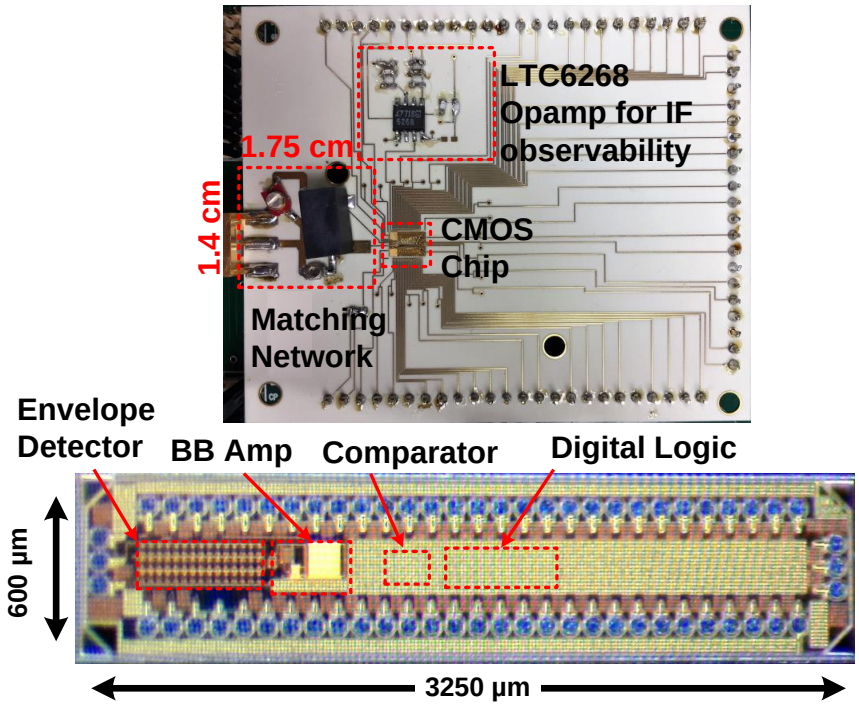


Figure 3.9: Die photo of CMOS WuRX and Rogers PCB with matching network.

the current limit will require the development of higher Q resonators to optimize the input voltage boost or utilizing higher sub-threshold slope devices. A co-design of the RF matching network and the ED is a critical design practice that allows for the development of optimum sensitivity. The passive front-end architecture has provided sensitivities $<$ -80 dBm but is likely to saturate soon due to fundamental noise limitations **??** [**?**] [56].

3.7 Contributions

1. Led system-level design identifying critical components and requirements for system operation.

2. Led baseband design and interfacing between the detector and baseband amplifier.

3. Designed the PCB and high impedance interfacing with the ED and worked with the ED designer to utilize the theory on optimal sensitivity and power consumption for the ED-first receiver.

4. Developed the high-level idea and flow chart of the automatic offset compensation used in this design.

5. Preformed top-cell integration and floor planning for system-level integration.

6. Led the measurement and characterization of the receiver.

This work was done in collaboration with Pouyan Bassirian, Abhishek Roy, Ningxi Liu.

CHAPTER 4

DETECTOR ARCHITECTURE EXPLORATION - THE TRIODE MODE DICKSON

The passive ED circuit has many attractive features compared to the active EDs, of which the most notable are: zero power consumption, zero flicker noise, and high input impedance. These attributes make passive EDs very attractive for high-sensitivity, ultra-low-power receiver designs. Unfortunately, due to the zero-bias nature of the detector devices, these detectors are very dependent upon process and temperature variations, substantially degrading their applicability in IoT networks.

This chapter presents an ED topology based upon triode mode transistors operating as a chain of charge pumps, as shown in Figure 4.1. Both single-ended and pseudo-differential detectors have been demonstrated in this architecture. This detector offers superior tunability, performance, and robustness over the Dickson topology and utilizes a direct-gate bias applied to complementary devices to form a single detector stage. Application of the RF signal directly onto the transistor source node allows for an independent gate bias. The source-only injection reduces the total input capacitance of the detector device, thereby reducing total input capacitance. This direct gate bias allows strong control over the device channel impedance (R_D), which directly modulates the detector input impedance, output noise level, and charge time. This work lead to the publication [57].

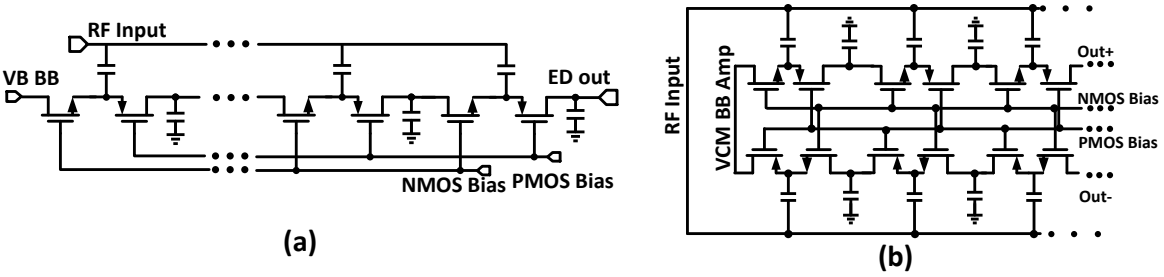


Figure 4.1: (a) Single-ended triode mode envelope detector, and (b) pseudo-differential triode mode envelope detector.

4.1 Motivation

There are several issues with the Dickson ED architecture previously used in near-zero-power-level front-ends limiting its applicability. One primary difficulty with the architecture is that the device options in the design kit define performance. Unless the design kit has the desired device channel impedance, the design is compromised, and cannot obtain optimal performance. Typically, this limitation results in much larger device sizes increasing input capacitance. The Dickson ED has significant degradation across the temperate and process corners, meaning that robust design is challenging. This lack of tunability means that it is difficult to make the detector design stable across process and temperature corners. Often in a given design kit, there is only one device with which it is feasible to build a detector from the limited design choices, forcing the designer to adopt a sub-optimal design.

4.2 Fundamental insight

A novel ED structure has been developed by not relying on diode-connected devices to produce the output signal. Examining the complete sub-threshold conduction equation

$$I_D = I_{D0} exp(\frac{V_G - V_{TH}}{nV_t})(exp\frac{-V_S}{nV_t} - exp\frac{-V_D}{nV_t}) \tag{4.1}$$

where V_{TH} is the device threshold voltage and applying an RF excitation shows that the rectified current for a device is invariant to the signal applied to the gate under sufficiently weak excitation. This insight allows for a modification of the Dickson detector to a new topology where the signal is injected directly into the MOSFET source node. In this modified topology, every other NMOS device in the chain is replaced with a PMOS device, and the gates are AC short-circuited to a reference. This modified Dickson architecture or Triode Mode Dickson (TMD) architecture can overcome the robustness limitations of the Dickson detector while obtaining the performance of an ideal Dickson ED. Utilizing non-diode connected devices and AC grounding, the gate and drain terminals of zero-biased MOSFETs allows one to develop a gate bias reducing (or increasing) the shunt resistance of the diode as well as allowing for a substantial reduction in the device size. This modified topology exhibits less input capacitance than the Dickson detector due to the source-only injection. This structure based on the Dickson architecture combines tunability and superior performance, allowing for a versatile passive detector.

4.3 Device channel impedance

Chapter 2 demonstrated the significance of device channel impedance analytically and utilized this parameter in optimization. A summary of the significance of R_D in passive ED design follows.

ED figures of merit are OCVS, output noise, input impedance, and rise time. For the Dickson detector, these metrics are all dependent upon the device channel G_D impedance.

$$G_D = \frac{\partial I_D}{\partial V_D}\Big|_{V_D=0}. \tag{4.2}$$

As seen in Figure 4.2a, increasing channel impedance linearly increases the charge time and monotonically increases output noise voltage. Furthermore, channel impedance (R_D) modulates detector input impedance as well, limiting the maximum obtainable voltage gain of the matching network. Finding the detector output SNR with respect to the N and R_D ($R_D = 1/G_D$) leads to

$$SNR_{out} = \frac{N\mu_D P_{RF} R_D R_s}{(R_D + NR_s)\sqrt{(4kTNR_D)}} \tag{4.3}$$

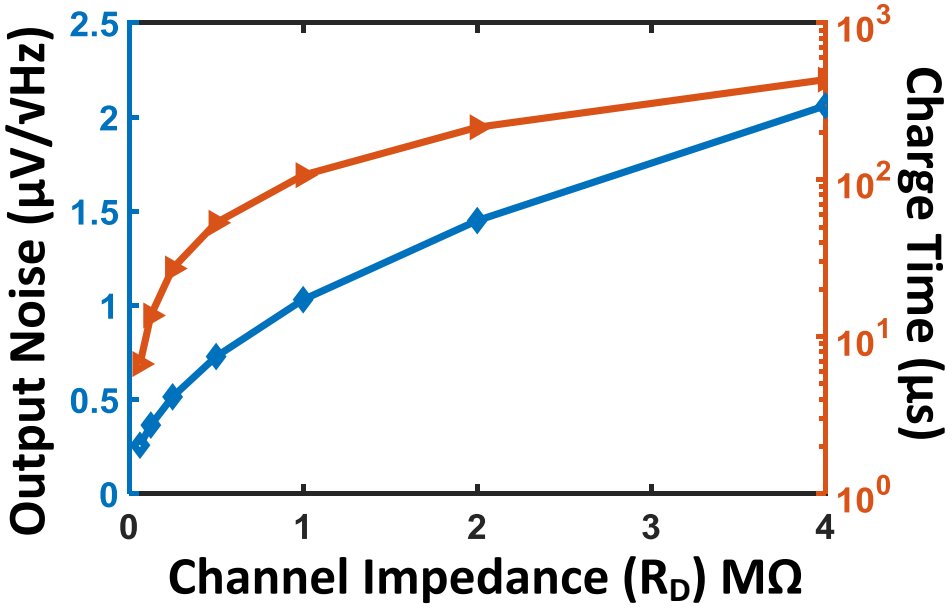


Figure 4.2: Demonstration of the dependency of charge time and output detector voltage noise on channel impedance for a 16-stage Dickson detector with minimum-sized coupling caps in a standard 130nm RF CMOS process.

for a detector driven by a finite, real-source impedance R_S. Optimizing this expression for sensitivity with respect to the number of stages N leads to

$$N_{opt} = \frac{R_D}{R_s}\,. \tag{4.4}$$

The results of the preceding analysis show that sensitivity is optimized when the ratio of the channel impedance to the number of stages is equal to the source impedance. For a detector design satisfying this optimum SNR condition, the output SNR cannot be a direct function of the channel impedance. Limited control of the impedance means that the detector performance is challenging to optimize and an under-constrained design problem.

These results indicate that excellent control of detector channel impedance is beneficial for optimal detector performance. The range of R_D available in modern CMOS kits is restricted, limiting practical implementations of the detector in many design kits. Channel impedance varies widely across devices of varying threshold voltages. In the GFUS 130nm RF CMOS process, a minimum-

sized zero-threshold-voltage device has a channel impedance of 130 $k\Omega$, while a minimum-sized low-threshold- voltage device has a channel impedance of 1 $G\Omega$. In the GFUS 130nm CMOS kit, a channel impedance variation of four orders of magnitude exists between the two lowest impedance devices in the kit. The channel impedance varies appreciably across the process corners as well. In the GFUS 130nm kit, channel impedance varies from 5.5 $M\Omega$ in the fast corner to 5 $G\Omega$ in the slow corner for the low-threshold-voltage NMOS device.

4.4 Triode mode envelope detector design

4.4.1 Diode connection versus source-only injection

Utilizing gate bias on the detector diodes allows for the tunability of R_D and thereby the optimization of detector performance. Examining the sub-threshold conduction equation

$$I_D = I_{D0} e^{V_G/nV_t} (e^{-V_S/V_t} - e^{-V_D/V_t}), \tag{4.5}$$

where n is the sub-threshold slope, and V_t is the device thermal voltage $I_{D0} \propto \frac{W}{L} e^{-V_{TH}/nV_t}$, where V_{TH} is the device threshold voltage and W and L are the device width and length, respectively.

The device channel impedance under zero bias for a diode-connected device can be calculated using (4.5) and (4.2) in

$$R_D = \frac{V_t}{I_{D0}}\,. \tag{4.6}$$

The application of the analysis techniques presented in [29], [40] allows an analysis of device output voltage level referenced to the input RF voltage.

Applying an input RF signal of $V_{RF} cos(\omega_{RF} t)$ to a diode-connected device (Figure 4.3a,b) with

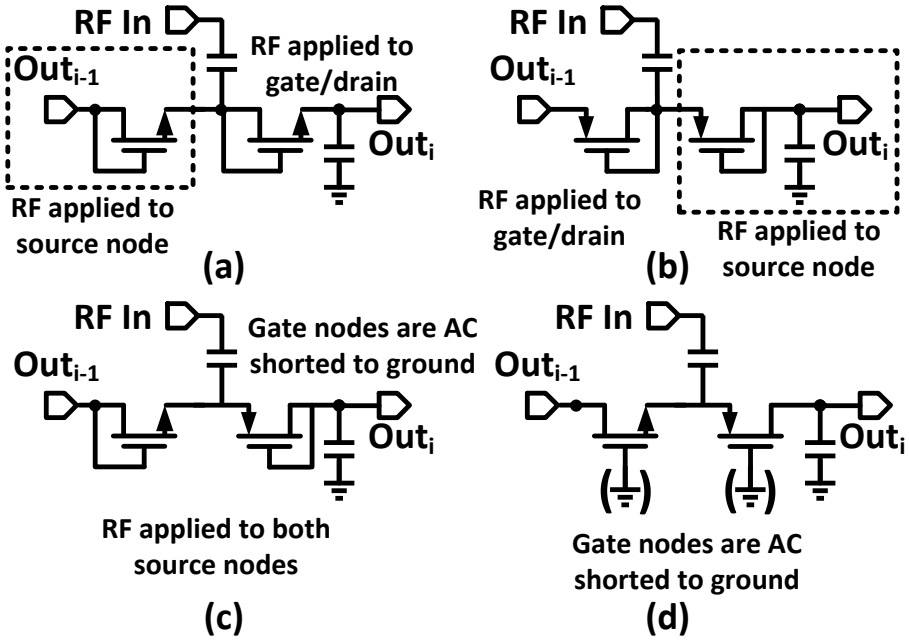


Figure 4.3: Schematic diagram of a single-stage: (a) NMOS-based Dickson envelope detector, (b) PMOS- based Dickson envelope detector, (c) complimentary Dickson envelope detector utilizing only source node injection, and (d) proposed triode mode envelope detector with the disconnected gate connection.

AC grounding the source terminal leads to

$$I_D = I_{D0}\frac{V_{RF}^2}{2V_t^2}(\frac{1}{n} - \frac{1}{2})\,. \tag{4.7}$$

This equation assumes all terms of order higher than two are negligible due to the supposed weak injection levels. The quadratic terms produce a self-mixing between the carrier and itself, producing a signal at baseband, and all odd-ordered terms produce signals at the odd harmonics which can be suppressed by baseband filtering.

When this current is flowing through the device output impedance, ($R_D = \frac{V_t}{I_{D0}}$) produces a voltage of

$$V_D = \frac{V_{RF}^2}{2V_t}(\frac{1}{n} - \frac{1}{2}) \tag{4.8}$$

under the assumption that $V_{RF} < V_t$.

Comparing this result to the case where the gate-drain nodes are AC grounded and a signal is directly injected into the source node (Figure 4.3c)) leads to

$$I_D = I_{D0}\frac{V_{RF}^2}{4V_t^2} \tag{4.9}$$

and

$$V_D = \frac{V_{RF}^2}{4V_t}\,. \tag{4.10}$$

This analysis indicates that the source-only injection provides superior sensitivity when compared to a diode-connected device. If the device sub-threshold slope approaches unity, both configurations can provide identical rectification. For low-threshold voltage devices in the GFUS 130nm RF CMOS process, the source-injected device provides $\approx 40\%$ more rectification than when the signal is applied at the gate-drain nodes.

Utilizing complementary devices, as shown in Figure 4.3d, allows for source injection on every device in the structure. This structure enables a direct-gate bias to be applied to each device independently, thus modifying the device channel impedance from (4.6) to

$$R_D = \frac{V_t}{I_{D0}}e^{(V_G - nV_s)/nV_t}, \tag{4.11}$$

which enables tunability through the modulation of the applied gate voltage.

4.4.2 Advantages of triode mode detector design

The topology in Figure 4.3d provides several advantages over the Dickson envelope detector. Most notably it offers: improved sensitivity, lower parasitic capacitances, and a wide range of tunability in the device channel impedance.

The lower parasitic capacitances arise from the signal driving only the source node as opposed to both the gate and drain nodes. The direct-gate bias enables a drastic ($> 100X$) reduction in device size for a given channel impedance.

Perhaps the most considerable advantage of this structure is the vast degree of tunability enabled. Through varying the bias voltages process and temperature can be compensated. Furthermore, this tunability means that the detector design space is not limited by the choice in threshold voltages. This trait is crucial for detector designs that require channel impedances that are not easily provided by the process.

Additionally, the analysis of this structure is identical to that of the Dickson envelope detector with an additional degree of freedom in the choice of device channel impedance. The analysis and design procedure presented in Chapter 2 applies equally well to triode mode envelope detectors as it does to the conventional Dickson topology.

4.5 Measurements results and conclusions

This detector topology has been taped out in a standard 130nm RF CMOS process (Figure 5.9). The detector input impedance is measured through on-chip probing with a Keysight PNA-X vector network analyzer. The detector charge time and OCVS are measured with a pulsed signal generated from an RF signal generator and recorded with an oscilloscope. Due to the wide variety in the tunability of this detector, it has been characterized across several modes, as detailed in 4.5, where the modes are labeled 1 through 7 in order of increasing channel impedance, and biased with external DC voltage supplies.

The measured detector input impedance agreed well with the simulation, as shown in Figure 4.4, at frequencies of less than 2 GHz but diverged considerably from simulated values at higher frequencies due to substrate coupling. Furthermore, the detector input capacitance is measured to be $\approx 143\ fF$, as opposed to a simulated input capacitance of $\approx 153\ fF$, indicating strong agreement between the simulated and measured impedance values.

Direct measurement of the detector OCVS referenced to a constant input voltage is measured across bias points and detailed in 4.5. The detector OCVS across all bias points is higher than the simulated value and decreases with increasing bias. The decrease in OCVS at higher bias is likely

Table 4.1: Comparison of operating modes

Mode	VBP (V)	VBN (V)	R_D (kΩ)	R_{In} (kΩ)	Charge Time (µs)	Meas. OCVS	Sim. OCVS	OCVS (mV/nW)
1	0.15	0.78	77	2.4	38	0.13*	0.07*	0.9
2	0.21	0.75	125	4	72	0.16*	0.11*	1.7
3	0.25	0.73	200	6.3	115	0.18*	0.14*	2.4
4	0.29	0.7	330	10.3	237	0.21*	0.16*	3.3
5	0.31	0.67	500	16	450	0.23*	0.18*	3.9
6	0.35	0.65	1100	31	952	0.26*	0.20*	4.5
7	0.38	0.63	2100	65	2000	0.30*	0.21*	5.8

***Output voltage in µV Referenced to 1 mV RF input voltage**

attributable to an increased gate leakage current lowering the output impedance of the detector diodes. Utilizing an external LC-matching network detector, the OCVS is measured referenced to a one nanowatt input power across 3 RF center frequencies, as shown in Figure 4.5. The detector OCVS across frequencies is measured in bias modes 3 ($R_{in} = 6\ k\Omega$) and 5 ($R_{in} = 16\ k\Omega$). The OCVS of the detector and matching network at 433 MHz is characterized across all the modes listed in 4.5. The OCVS can be seen to vary from 5.8 mV/nW at the highest impedance to 0.98 mV/nW at the lowest impedance.

Detector charge time is characterized across the various operating modes and shown in 4.5, where, for the lowest impedance, the mode charge time is measured to be $38\ \mu s$, and, for the highest impedance, the mode is measured to be $2\ ms$. This wide dynamic range shows a wide tunability in performance, enabling either multi-mode operation or robustness across the variation required for IoT sensor nodes.

This structure was also verified in a 65nm TSMC tape-out and was utilized in a full wake-up receiver chain.

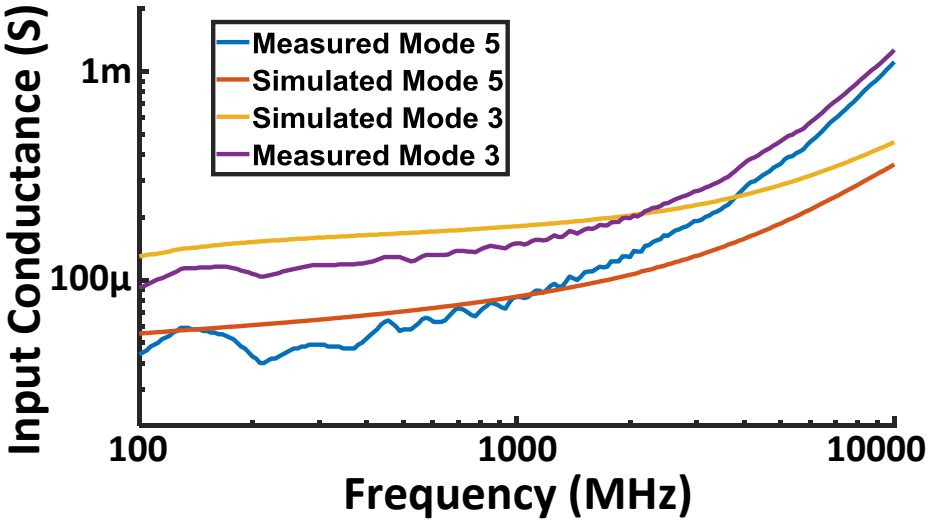


Figure 4.4: Detector input conductance, measured across modes 3 and 5, showing strong agreement between measured and simulated values for frequencies of less than 2GHz.

4.6 Conclusions

This work presents a new passive envelope detector topology, the triode mode envelope detector, offering superior performance and tunability over the convention Dickson topology. Furthermore, the new topology shows superior tunability, lower capacitance, and higher sensitivity when compared to the standard Dickson envelope detector. Detector-first receivers, as well as other receiver architectures, can benefit from adopting this detector topology.

4.7 Contributions

1. Discovered weaknesses inherent in the Dickson architecture and related these to the device impedance.

2. Developed the TMD ("Triode-mode Dickson") topology and verified the operating principle through simulation.

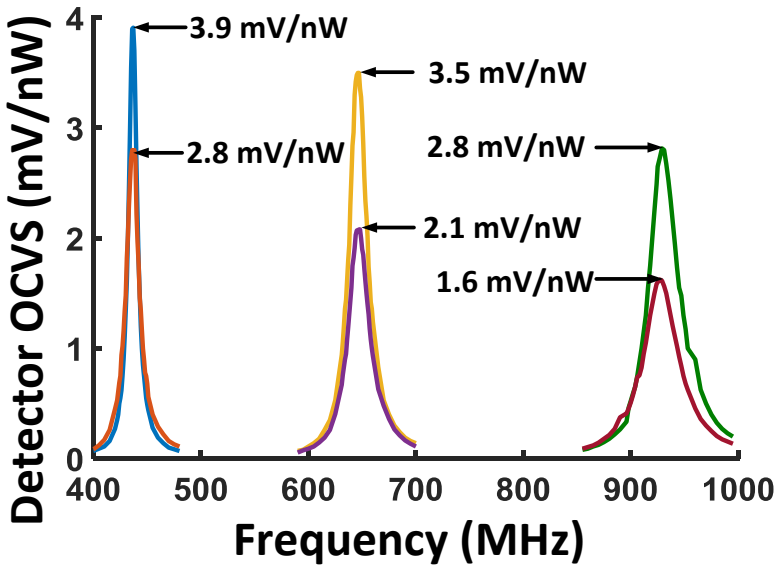


Figure 4.5: Open Circuit Voltage Sensitivity (OCVS) of the detector and matching network across frequency in modes 3 ($6k\Omega$) and 5 ($16k\Omega$).

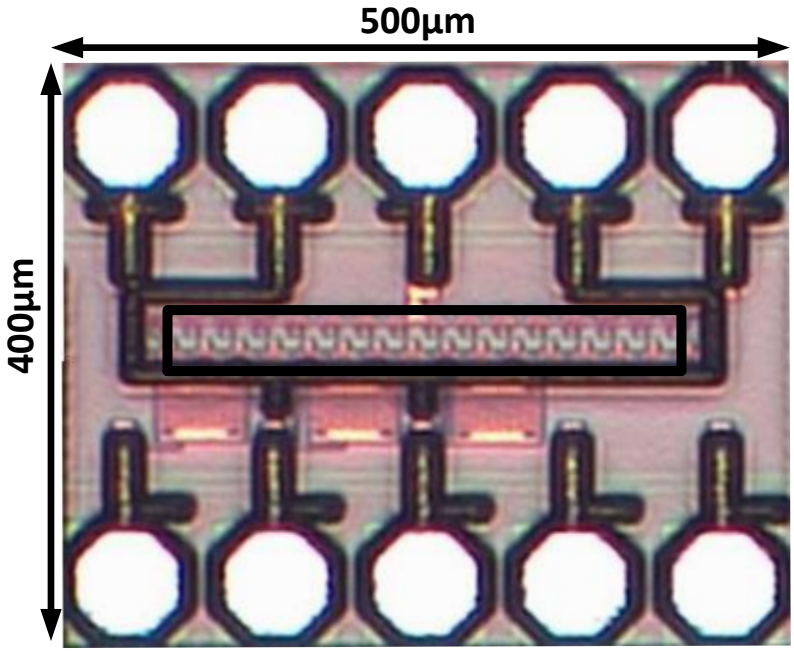


Figure 4.6: Die photo of a fabricated 130nm CMOS 16-stage triode mode envelope detector with an active area of 350μm by 50 μm

3. Developed the theory behind the operation and verified it analytically through simulation and measurement.

4. Compared the TMD to the Dickson and other passive envelope detector architectures to discover the detectors merits.

5. Taped out test structures and measured results, verifying the theory developed for the TMD detector.

CHAPTER 5

BIT-LEVEL DUTY-CYCLED TRF RECEIVER DESIGN (SAMPLIFIER)

The detector-first RF front end sensitivity limitations (roughly $-80\ dBm$) necessitate the examination of other receiver architectures. One obvious way to reduce DC power consumption while using high-power RF amplifying blocks is to duty cycle to the receiver. Typically, WuRx duty cycling schemes adopt either packet-level or bit-level duty cycling to reduce power consumption. Bit-level duty cycling enables WuRx performance scaling across a constant wake-up receiver FOM; this technique enables a direct three-dimensional trade-off between sensitivity, power consumption, and latency. To explore this design space, we have developed the first sub -100 dBm wake-up receiver that operates at less than one micro-watt power consumption. A bit-level duty-cycled TRF receiver was utilized in this design and has been dubbed the "Samplifier" wake-up receiver. This lead to publication [58] and pending journal and conference submissions.

5.1 Motivation

Many IoT applications require links operating at ranges similar to those of cellular technology, such as outdoor and industrial low-power wide area networks (LPWAN). Furthermore, many applications benefit from very long sensor lifetimes, ideally enabling a sensor to function for years on end without battery replacement. The lowest-power receivers demonstrated to date with $<$ -100 dBm sensitivity have power consumptions in the hundreds of micro-watts [28], [59], [60]. Recently demonstrated receivers [4], [41], and [50] have achieved extremely low power consump-

tions of less than ten nano-watts but are typically limited to sensitivities of around -80 dBm. A solution is needed to bridge this power-sensitivity gap and enable many near-zero power sensing applications.

This chapter proposes the "Samplifier" or highly scalable bit-level duty-cycled tuned RF front end (TRF) receiver shown in Figure 5.1 to achieve the combination of better than -100 dBm sensitivity and power levels below 100 nW. This receiver utilizes high impedance off-chip impedance matching at the input followed by bit-level duty-cycled RF gain cells, which drive an external MEMS filter to reduce noise self-mixing before the RF ED. The output of the ED circuit drives the baseband gain and filtering before detection by the correlator. Finally, a fully integrated "Automatic Gain and Offset Control" algorithm senses the presence of interfering signals and adjusts the baseband circuits to reject the offset induced by the jamming signals.

A digitally programmable baseband bandwidth and digital timing controller enable dynamic digitally controllable performance trade-offs. Through modulating both the bit-duration (integration time) as well as the sampling window duration, a single receiver can operate in a wide range of data rates, power levels, and sensitivities. This programmable tunability enables one device to be used for a wide variety of applications and needs. The initial receiver demonstrated a wide dynamic range in power consumption and latency ranging from 33nW power consumption to 350nW power consumption across a latency range of $250ms$ to $5ms$ while operating at bit integration times of between $50us$ and $100us$. Furthermore, the initial receiver improved the state- of-the-art in sub-microwatt receivers by 26dB and the power consumption of sub-100-microwatt receivers by a factor of greater than ten thousand.

This receiver was limited in its integration time dynamic range by a limited baseband tuning range. Furthermore, RF linearity and stability issues limited its robustness to PVT as well as interference into the RF front end. Front-end instability was resolved by decreasing the Q-factor on the input matching network to ensure robust operation; this technique led to a decrease in sensitivity and weaker out-of- channel rejection. Finally, comparator non-linearity and the slow nature of the offset compensation algorithm limited its ability to respond robustly and quickly in a rapidly

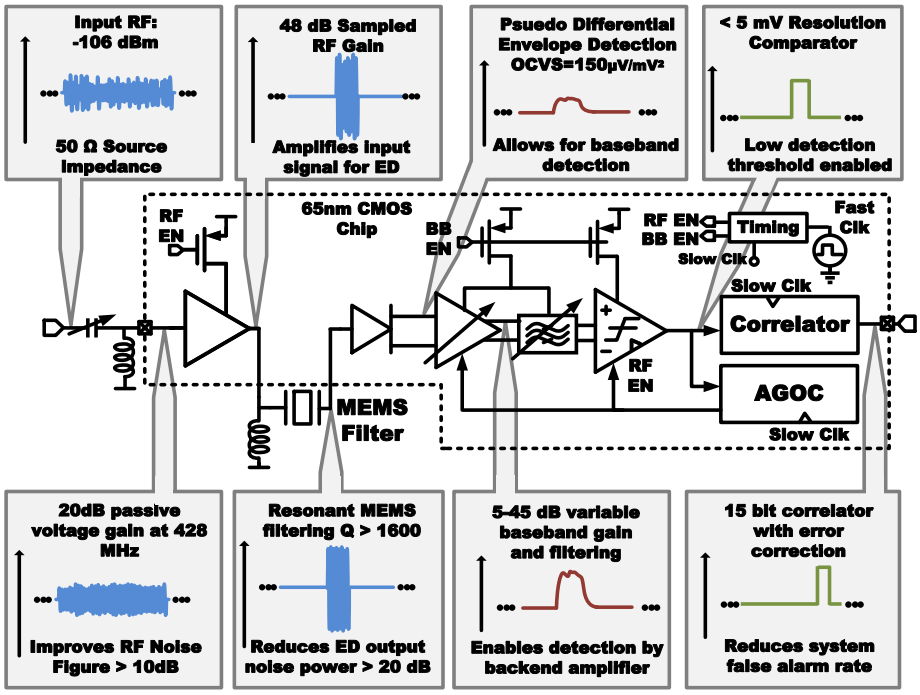


Figure 5.1: Initial Samplifier system design showing major system components and functionality of each block.

fluctuating interference environment.

A second Samplifier wake-up receiver was developed based on the first-generation design and focusing on improving performance as well as robustness. It is shown in Figure 5.2. The second Samplifier demonstrated a high sensitivity of -108dBm at a power consumption of less than 100nW. This receiver further overcomes many limitations regarding stability, PVT robustness, and interference rejection present in the initial Samplifier receiver. This performance improvement is accomplished through the use of a dynamic RF bias and an improved high-impedance interface design. Furthermore, this receiver obtained a superior interference rejection of 30dB through many block-level and architectural innovations. Most notably, this receiver has two operating modes, a two-tone down-conversion mode to shift the wake-up signal to an IF frequency, reducing the effect of the interference which folds down to baseband frequencies as well as a single-tone

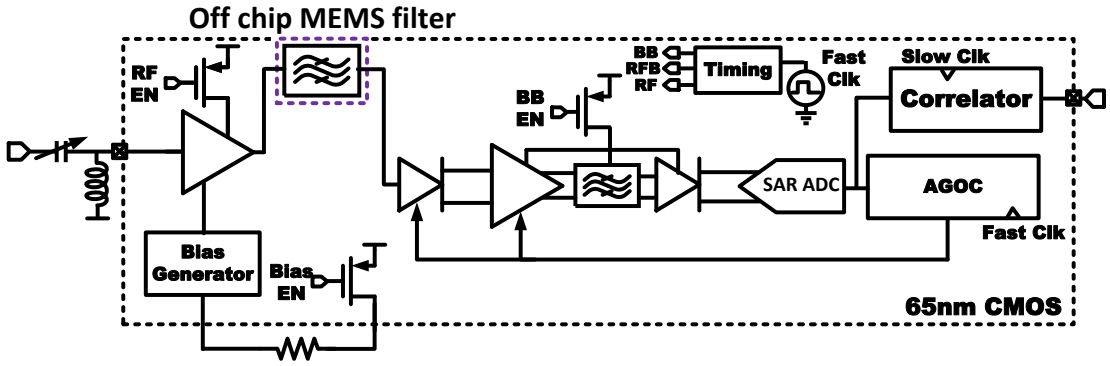


Figure 5.2: Second Samplifier system diagram showing additional blocks added, including a temperature- robust fast-start-up RF bias generator, a 6-bit SAR ADC, and two tone-down conversion paths.

high-sensitivity mode. This receiver also employed an "Automatic Gain and Offset Correction circuit employing a 6-bit SAR ADC, which enables extremely fast convergence in the presence of high-powered interference. The two-tone down-conversion reception and the ADC can enable co-channel existence between receivers operating in the same band though the use of different IF frequencies for the reception and higher-dimensional correlator matched filters. These system-level innovations in the second-generation receiver enable a much more robust and scalable receiver.

5.2 Detector-first receiver limitations

Detector-first receivers are the most popular architecture in the literature for achieving sub-microwatt power consumption. These receivers have been demonstrated to obtain around a -80 dBm sensitivity while consuming less than ten nano-watts of power. A calculation of the minimum detectable signal obtainable for a given detector-first receiver can be found in equation 2.26 in Chapter 2, which, in the power domain, is equal to

$$SNR_{Ideal} = \frac{\mu_D P_{RF}^2 R_S}{16kTB}. \tag{5.1}$$

Choosing a source impedance of $R_S = 10\ k\Omega$ and device voltage sensitivity of $\mu_D = 5\ V/V^2$ leads to a sensitivity of about -80 dBm (assuming $SNR \approx 9\ dB$) assuming that a $B = 100\ Hz$ baseband bandwidth has been utilized. Recently, several receivers have approached this sensitivity [50], [56], indicating that further work towards optimizing the ED- first sensitivity will either require device-level innovations (μ_D or R_S) or longer integration times to improve sensitivity further.

When considering scaling this architecture from -80 dBm to -100 dBm or beyond, it is apparent that either significant technological improvements are required, integration times exceeding 1b/s, or more is required. Due to the nonlinear nature of the square-law of ED circuits, the receiver sensitivity and latency trade-off are related in a quadratic manner. This quadratic relationship implies that doubling sensitivity requires a four-fold increase in latency to maintain performance. The latter option is the most straightforward approach; unfortunately, in order to scale these systems past a -100 dBm wake-up, the latency will have to become prohibitively long. For example, the receiver in Chapter 3 obtained -76 dBm in sensitivity with a 200mS wake-up latency; hence, scaling this sensitivity to -100 dBm would entail a wake-up latency of just under 3 hours.

A further complication of the detector- first receiver is a limited ability to scale the receiver data rate. Due to the long integration times required to provide high sensitivity (typically $> 5ms$), this architecture has many drawbacks when operated as a data receiver. The data rate limitation on ED-first receivers can necessitate the integration of a separate high-power data receiver in many applications, increasing cost and complexity.

5.2.1 Tuned RF receiver limitations

The TRF receiver has yet to obtain better than -100dBm sensitivity at less than $1\mu W$ as shown by [38], [61], [62], [63], [64], and [65] but has the potential to be scaled to these sensitivities. The TRF receiver cannot be directly scaled to nanowatt power levels, as the bias current required

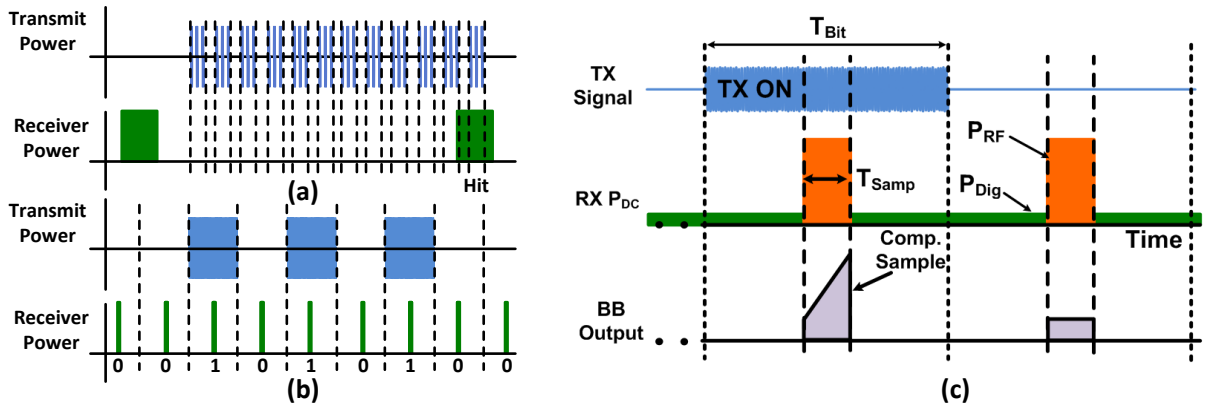


Figure 5.3: (a) Packet-level duty cycling with multiple transmission events required for detection, (b) bit-level duty cycling for which only a single transmission event is required for detection, (c) Illustration of bit-level duty-cycled receiver operation highlighting the transmitted and sample window durations.

to provide active gain is prohibitively high. A back-of-the- envelope calculation for the current required to provide a capacitively loaded common source amplifier with a given gain can be found from

$$I_D = \frac{A_v 2\pi f_c C_L}{\delta}, \tag{5.2}$$

where ω_c is the frequency of operation, C_L is the load capacitance seen when looking into the drain of the device, and α is the transistor current efficiency (gm/I_{DS}). For example, in order to obtain a gain of 0dB at 433MHz, assuming a load capacitance of $10\ fF$ and a current efficiency of 20, a bias current of about $1.5\ \mu A$ is required. Operating the device at higher gains and bias currents increases this current even further, indicating that a TRF-based circuit will require duty cycling to obtain sub-microwatt operation.

5.2.2 Duty cycling method comparison

In order to overcome the sensitivity limitations of the ED-first architecture while obtaining a power consumption of less than one microwatt, an asynchronous duty cycling approach can be adopted [66]. Asynchronous duty cycling is a duty cycling technique in which the transmitter does not know the specific instance in time at which the wake-up receiver is active. The two types of asynchronous duty cycling used in the wake-up receiver context are conventional packet-level duty cycling (Figure 5.3a) and bit-level duty cycling (Figure 5.3b,c)). Conventional packet-level duty cycling activates the receiver for a duration long enough to detect the transmission of the full wake-up packet. The bit-level duty cycling technique activates the receiver for a fraction of each wake-up bit before deactivating for the rest of the bit period. The latency (L_{packet}), power consumption, and sensitivity (S_{packet}) associated with packet-level duty cycling are

$$L_{Packet} = \frac{1}{2}(NT_{bit} + NT_{bit}/DF_{Packet}) \approx \frac{1}{2}NT_{bit}/DF_{Packet}, \tag{5.3a}$$

$$P_{DC} = P_{Leakage} + P_{Digital} + P_{RF}DF_{Packet}, \tag{5.3b}$$

$$S_{Packet} \propto T_{Bit}. \tag{5.3c}$$

For bit-level duty cycling these terms are

$$L_{bit} = T_{bit}N, \tag{5.4a}$$

$$P_{DC} = P_{Leakage} + P_{Dig} + P_{RF}DF_{bit}, \tag{5.4b}$$

$$S_{bit} \propto T_{Samp}, \tag{5.4c}$$

$$DF_{bit} = T_{Samp}/T_{bit}, \tag{5.4d}$$

where DF is the duty factor of the RF front end, which is expressed as $DF = \frac{T_{On}}{T_{Off}}$; N is the number of bits in the wake-up code; and T_{bit} is the transmitter on time per bit in both sets of equations. In a packet-level duty cycled receiver, the front end must be activated for enough time to ensure that the entire wake-up packet is detected. If the receiver, due to asynchronization,

samples only part of the wake-up packet and deactivates in the middle of the wake-up packet, the receiver will miss the detection. If the receiver in the packet-level duty-cycling case is on for at least the duration of two wake-up packets, a reliable detection can be made, as every bit in the packet will be captured.

Both techniques enable a power savings over continuous reception. However, in the wake-up receiver and IoT context, there are several prominent advantages to the bit-level detection technique: direct wake-up receiver FOM scaling, reduced current draw during the sampling window, and lower RF- occupied bandwidth.

Bit-level duty cycling enables a receiver to change its performance dynamically across a constant wake-up receiver figure of merit. A useful figure of merit for wake-up receiver circuits can be found by [30]

$$FOM_{WuRx_dB} = -Sensitivity + P_{DC} + Latency, \tag{5.5}$$

where all quantities are in logarithmic format. The bit-level duty cycling technique enables FOM scaling through trading RF sensitivity and scaling the wake-up latency (bit rate) for power consumption. For packet-level duty-cycled receivers, a direct trade-off between duty factor (power) and latency is possible, but a direct trade-off between sensitivity and power consumption cannot be accomplished without changing the transmitted bit duration. An illustration of the operation of a bit-level duty cycled receiver is shown in Figure 5.3, where $T_{bit} = 1/R_{bit}$ is the duration of a single transmitted bit and defines the bit rate into in the correlator. T_{Samp} defines the sampling window over which a decision is made in the presence of the input RF signal. Changing the sampling window or the integration time of the bit-level duty cycled receiver allows for a scalable and straightforward trade-off between sensitivity and power consumption.

Previous work [67] has exploited the bit-level duty cycling technique on a full transceiver to mitigate the supply ripple for an energy-harvesting-based sensor node. The short duration of the RF activation, followed by a more extended period of inactivity, reduces the instantaneous droop in supply voltage when compared to a packet-level duty cycling approach. This behavior makes the

bit-level duty cycling technique appealing in the context of systems relying on energy harvesting.

For receivers operating at lower RF frequencies for which the available RF bandwidth for the wake-up signal is limited, the bit-level duty cycling technique requires far less bandwidth than that needed for a packet-levelly duty cycled receiver with an equivalent duty factor. Examining the expected bit-rate of a bit-level duty cycled receiver leads to

$$R_{bit\ BL} = \frac{N_{bit}}{L_{Avg}}, \tag{5.6a}$$

which can be compared to a packet-levelly duty cycled bit rate of

$$R_{bit\ PL} = \frac{N_{bit}}{2DFL_{Avg}}, \tag{5.6b}$$

where R_{bit} is the bit rate of the wake-up signal, L_{Avg} is the desired wake-up latency, and N_{bit} is the number of bits in a wake-up signal. As an example of the channel bit rate required for a system wake-up at a 100ms wake-up latency, a duty factor of 0.1% along with a 64-bit correlator length leads to a bit rate of 640 bits per second in the bit-level duty-cycled system and 320k bits per second for the packet-level duty-cycled system. For RF-bandwidth-restricted applications, the bit-level technique offers advantages over the packet-level duty cycling method.

5.3 Synchronization and timing generation

Due to the nature of the bit-level duty cycling technique, no synchronization is required between the transmitter and receiver, forgoing the use of the correlated oversampling [4] technique. The probability of the sample window corresponding with an edge of the transmitted bit period is equal to the duty factor of the receiver; hence, when the receiver is duty cycled at high factors, the probability of this event occurring is very low, as shown in Figure 5.3a.

A set of 16-bit digital counters and digital comparators generate the timing and control pulses to control the bit-level duty cycling. The counter is incremented at the rate of the systems fast clock and generates RF control pulses based on simple digital comparators. This technique generates all

of the control pulses needed with minimal logical overhead and enables a wide range of reconfigurability in the receiver through modifying the various timing and control pulses.

Bit-level duty cycling is employed throughout the receiver chain in order to reduce power consumption on both the RF gain stages and baseband signal processing. Due to the widely varying start-up times and power consumptions associated with different signa-processing blocks, multiple start-up pulses are utilized to minimize the system start-up time and energy. The RF LNA is the highest instantaneous power-consuming block, but it has a swift transient start-up response on the order of 10s to 100s of nanoseconds. The baseband gain, noise-limiting filter, and the comparator operate at much lower bias currents; correspondingly, these blocks have much greater start-up times. From the flexible and straightforward timing scheme, five timing pulses are propagated through the system: the RF enable, baseband start-up, baseband enable, comparator enable, and correlator clock pulses. The enable signals the power gate in each block, while the baseband start-up is a control pulse used to enhance the start-up time of the baseband.

5.4 Interference limitations in bit-level duty cycled receivers

One distinct drawback of the bit-level duty cycling technique is that the sampling affects not only the signal but also any interference into the system. Ideally, in a TRF receiver, a tone at the input creates a DC offset at the baseband frequencies. When the receiver samples the input RF signal, the baseband signal is spread across a wide bandwidth due to the sampling. Appendix (Section A.3) analyzes this effect for the case of a single tone and noise sent into a square-law ED and sampled by an ideal rectangular pulse. The impact of interference on the baseband output noise is analyzed in a later section.

Utilizing the results arrived at in the Appendix, for a single tone input signal, we can write

$$V_{O\ BB}(f) = [V_{Int} + V_{Sig}]Tsinc(f/T), \tag{5.7}$$

where V_{Int} is the DC voltage produced by the interference without the presence of sampling, V_{Sig} is the DC voltage produced by the interference without the presence of sampling, and T is the duration of the sampling window. As the energy of both the signal and interference is spread spectrally across a wide bandwidth, continuous-wave interference does not introduce a DC offset but instead overlaps with the signal of interest. Detector-first receivers which do not present sampling to the CW interference can reduce the impact of CW interferers at the baseband drastically through simple AC coupling in the signal path. As the power spectral density of the sampled CW interference and the signal are identical, direct filtering cannot reduce the impact of CW interference on the receiver.

As filtering cannot be used to resolve a single-tone input signal and interference, stringent requirements are needed on the baseband receiver. For example, for a minimum comparator decision voltage increment of $1mV$, an interferer at $20dBc$ into the ED creates a $100mV$ offset. In order to detect the input RF signal riding on top of this interference, the comparator needs to be able to resolve $1mV$ riding on top of a $100mV$ DC offset. Designing a comparator or ADC that can perform this detection is complicated and requires a gain and offset control loop to set the optimum decision threshold. A calculation of the maximum CIR (in dB) at the detector interface that the ADC can resolve given a set ENOB is done using

$$CIR_{Max} = 10log10(2^{-ENOB}), \tag{5.8}$$

where the ENOB is the effective number of bits in the ADC, while an ideal case of the signal being equal to 1 LSB is assumed. The factor of 5 accounts for the square-law nature of the ED. Out-of-band interference is assumed, which implies that the interferer down-converted noise does not degrade the baseband SNR.

A calculation for the ADC ENOB required for a 30dB CIR shows that an ENOB of 10 bits is needed. A comparison to the ED- first receiver presented in Chapter 3 which obtains a 30dB rejection through simple high-pass filtering highlights the problem. This harsh requirement on the ADC ENOB, coupled with the difficulties in designing a baseband which can support such high

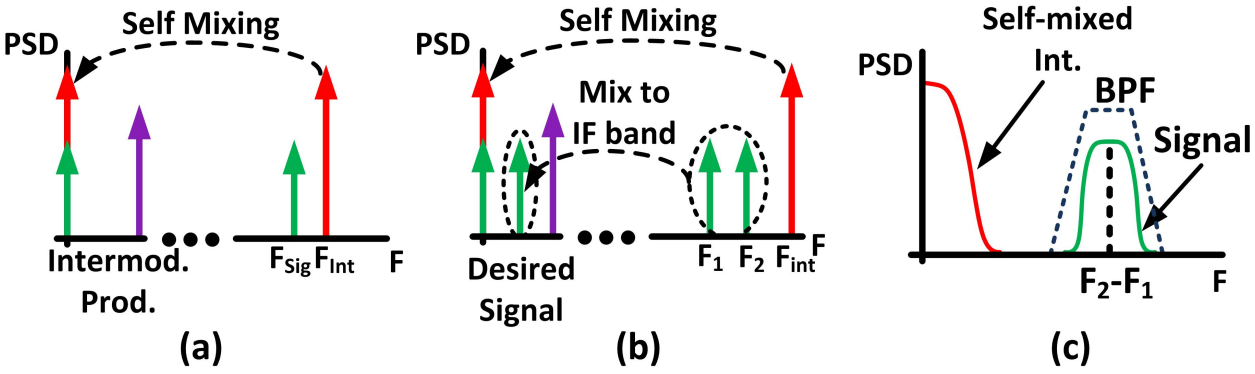


Figure 5.4: (a) Conventional OOK receiver, where both the interference and signal fall to DC; (b) a two- tone demodulation, where the desired IF signal is extracted; and (c) a bit-level duty cycled two-tone receiver, where the filter is positioned at $F_1 - F_2$ to reject interference folding down to DC.

dynamic range signals at low power and low noise, makes interference-robust design challenging.

5.5 Two-tone down conversion

The second Samplifier receiver shown in Figure 5.2 overcomes many of the interference down-conversion problems through the use of a two-tone down conversion [68]. The two-tone down-conversion technique splits the input power into two signals at a frequency offset of Δf (Figure 5.4b) and OOKs this signal into the receiver. This two-tone modulation produces an intermixed product (Figure 5.4c) at a frequency of Δf, which is then detected by another down-conversion stage before detection by the ADC. This frequency offset allows high-pass filtering of the interfering signal from the signal of interest.

The excitation into the receiver can be expressed as

$$V_{In\ ED} = \frac{V_{RF}}{\sqrt{2}} cos(2\pi f_0 t) + \frac{V_{RF}}{\sqrt{2}} cos(2\pi f_0 t + \Delta f), \tag{5.9}$$

where Δf is the frequency offset between the two tones, and V_0 is the peak voltage of a single-tone

signal whose power is equal to the power in each of the two tones. This signal going through a square-law detector produces an IF output of

$$V_{O\ ED} = \frac{\alpha V_{RF}^2}{2} cos(2\pi \Delta f t), \tag{5.10}$$

which can be compared to the voltage produced by a single tone into an ED detector of

$$V_{O\ ED} = \frac{\alpha V_0^2}{2}. \tag{5.11}$$

Doing so shows that the output power of the two-tone output is 3dB lower, as (5.10) is an AC quantity. This initial result implies that the SNR hit associated with this technique is 1.5 dB, but, as the bandwidth needed for the signal in equation (5.10) is twice as high as the bandwidth in (5.11), the actual degradation is 3dB when referred to the ED input.

While this technique does reduce the impact of interference in the baseband, it does not remove the problem. Considering equation (5.7), the power spectral density of the DC down-converted signals extends out and falls off with a sinc envelope. Figure 5.5 compares several sampling window durations of $50\mu s$, $150\mu s$, and $250\mu s$ and compares these with the extinction a 60kHz offset. Comparing the extinctions for the $50\mu s$ and $250\mu s$ sampling periods shows extinctions of 14dB and 28dB, respectively. The square-law nature of the ED implies 7dB and 14dB extinctions, respectively, when referred to the input of the ED.

Figure 5.6 details the issues with energy leaking from the DC down-converted interference into the AC two-tone filter. Unfortunately, matched filtering for a square pulse cannot be reliably implemented in an ULP analog design, so a second-order bandpass filter centered at Δf is used instead. The rejection ratio obtained through this technique is found through

$$Rej = 5log10(\frac{\int_0^\infty |H_{BPF}(f) sinc((f-\Delta f)/T)|^2 df}{\int_0^\infty |H_{BPF}(f) sinc(f/T)|^2 df}), \tag{5.12}$$

where $H_{BPF}(f)$ is the transfer function of the band-pass filter used to reject the interference. A second-order band-pass filter with a Q-factor set at $\Delta f/T$ captures half of the power in the two-tone down-converted pulse. Using the filter, as mentioned earlier, and a $\Delta f = 60kHz$ and $T = 100\mu s$

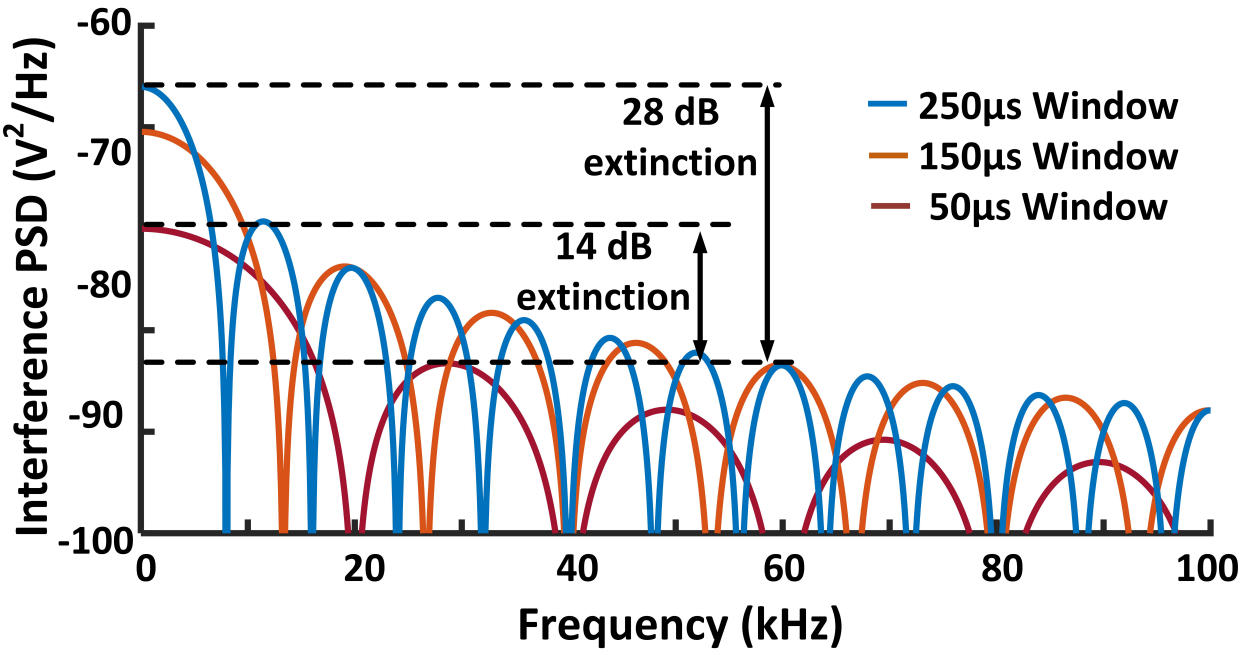


Figure 5.5: Comparison of the roll-off of interferer power spectral density versus the frequencies for several sampling intervals, showing a 28dB extinction at 60kHz offset for a $250\mu s$ sampling duration and a 14dB extinction at 60kHz offset for a $50\mu s$ sampling duration.

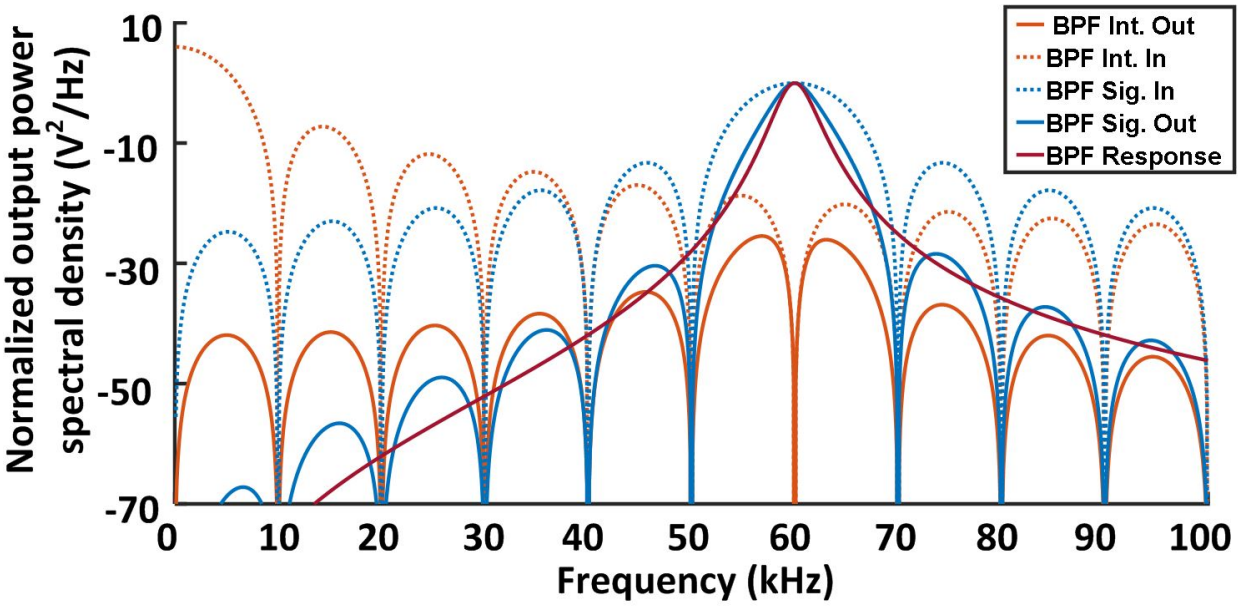


Figure 5.6: This figure shows the power spectral densities of the interfering signal and noise passing into the IF bandpass filter. The output PSD of the interference is significantly attenuated as it peaks near the DC, whereas the output power spectral density of the signal peaks in the filter bandwidth. The integration time used is $100\mu s$, and a filter center frequency of $60kHz$ is utilized.

shows a rejection of 12.6dB of the interfering pulse. Increasing either the frequency offset or the integration time further improves this rejection. The placement of the center frequency of the filter in a null of the interfering signal side lobes improves rejection by approximately 1 dB compared to setting the filter at the maxima.

These results imply that for an ideal two-tone down-conversion receiver, additional interference rejection of greater than 10dB can be realized compared to single-tone down-conversion. Furthermore, this analysis both highlights a potential issue with the bit-level duty cycling technique and presents a potential workaround. The development of an ideal system to perform the two-tone down-conversion will enable the receiver to achieve carrier-to-interference ratios similar to that of the ED-first receiver when combined with an efficient automatic gain and offset compensation algorithm.

5.6 Measurement results

Both Samplifier receivers were characterized at block and systems levels to capture their performances and compare them to state-of-the-art. Both receivers were designed and fabricated using a TSMC 65nm low-power process. The low-power process was used over the general-purpose process due to lower gate leakage in the core devices. This reduced gate leakage reduced the digital power consumption considerably. The MEMS resonator used in this design was fabricated at UIUC and utilized an AlN (Aluminum Nitride) device.

Operating curves, bit error rates, and interference rejection are characterized for the initial Samplifier receiver. Given the ample trade space that the system architecture provides, three operating modes are chosen to showcase the extent of these trade-offs: Low Power, High Sensitivity (LPHS) using a 10s; Low Latency, High Sensitivity (LLHS); and Low Power, Low Latency (LPLL). In addition, a high-sensitivity measurement with a mid-range 1s latency was used. The LPHS (5s latency) mode obtained a -106 dBm sensitivity at 32.7nW power consumption from a 0.75V VDD. In the high-sensitivity mode, a bit error rate measurement was made showing the receiver operating

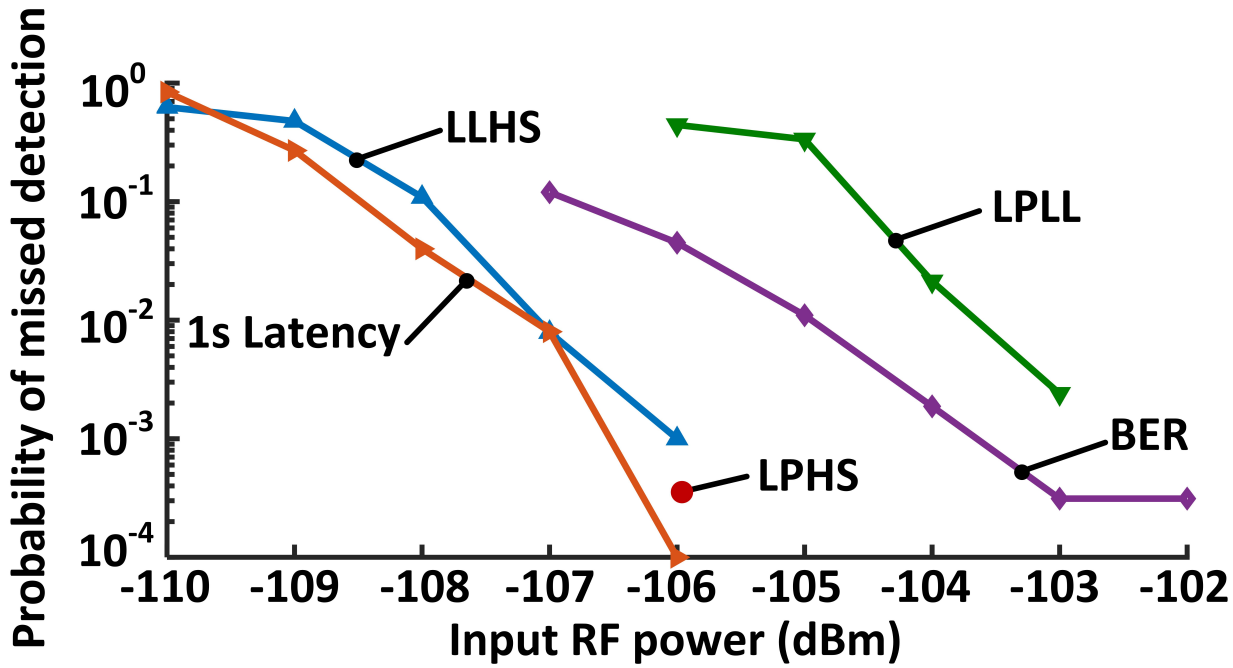


Figure 5.7: Demonstration of wake-up receiver sensitivity through multiple Receiver Operating Curves across multiple operating conditions showing trade-offs between latency, DC power consumption, and RF sensitivity.

at -103dBm with a bit-error rate of less than 0.1%. Increasing the baseband bandwidth and clock rate enabled the LPLL (240ms latency) at the cost of reduced sensitivity.

Figure 5.7 shows the sensitivity of the receiver across all the operating modes, including a measurement of the receiver bit-error rate. A wide range in power consumption (9X), latency (20X), and sensitivity (3dB) are shown with this architecture. Through exploiting these various operating modes, the receiver can be optimized for a variety of applications. The carrier-to- interference ratio is measured across varying frequency offsets in Fig. 5.8, which shows a 22dB rejection at a 3MHz offset and 16dB rejection at a 500KHz offset. Figure 5.9 shows an SEM image of the MEMS resonator and a die photo of the CMOS chip.

A comparison of the first Samplifier receiver with the state-of-the-art in ultra-low-power wake-up receivers is shown in Figure 5.11 and Table 5.6.

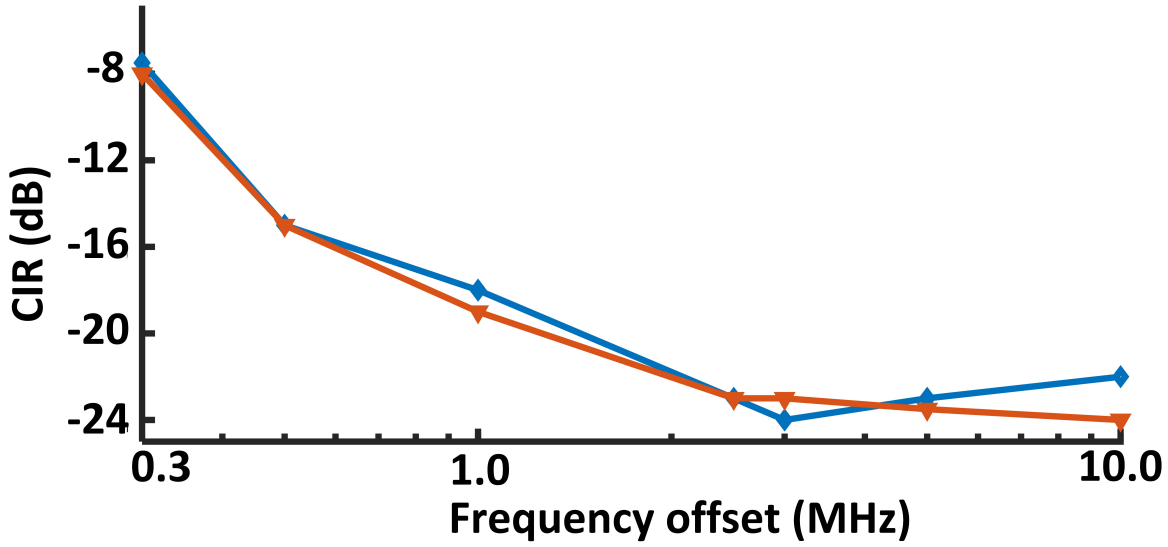


Figure 5.8: Carrier-to-interferer ratio across different frequency offsets above and below the center frequency measured at -102dBm 1% BER. This measurement shows a 16dB rejection at a frequency offset of 500kHz and a 22dB rejection at a 3MHz offset.

System-level measurements of the second Samplifier system are ongoing, but the preliminary results show promise of better than -108 dBm sensitivity at sub-100nW power consumption and an interference rejection better than 28dB.

5.7 Comparison with other ULP RX

Figure 5.7 shows this work compared to the receiver presented in chapter 3 as well as several recent ED first receivers. The estimate sensitivity limitations of the ED first receiver shown in that work is shown showing that work approachs within 5dB of the thermal noise limitations. Results from both Samplifier receivers are shown as well and compared with a previous work scaled to this latency. Comparing to the closest work in the SOA ([60]) in terms of RF frequency and sensitivity -102dBm with a 31 bit code and consuming 370μW at a data rate of 1kbps. Assuming a synthesizer startup time of 600μs for a desired 1s latency this translates into a 12μW power consumption at 1s latency

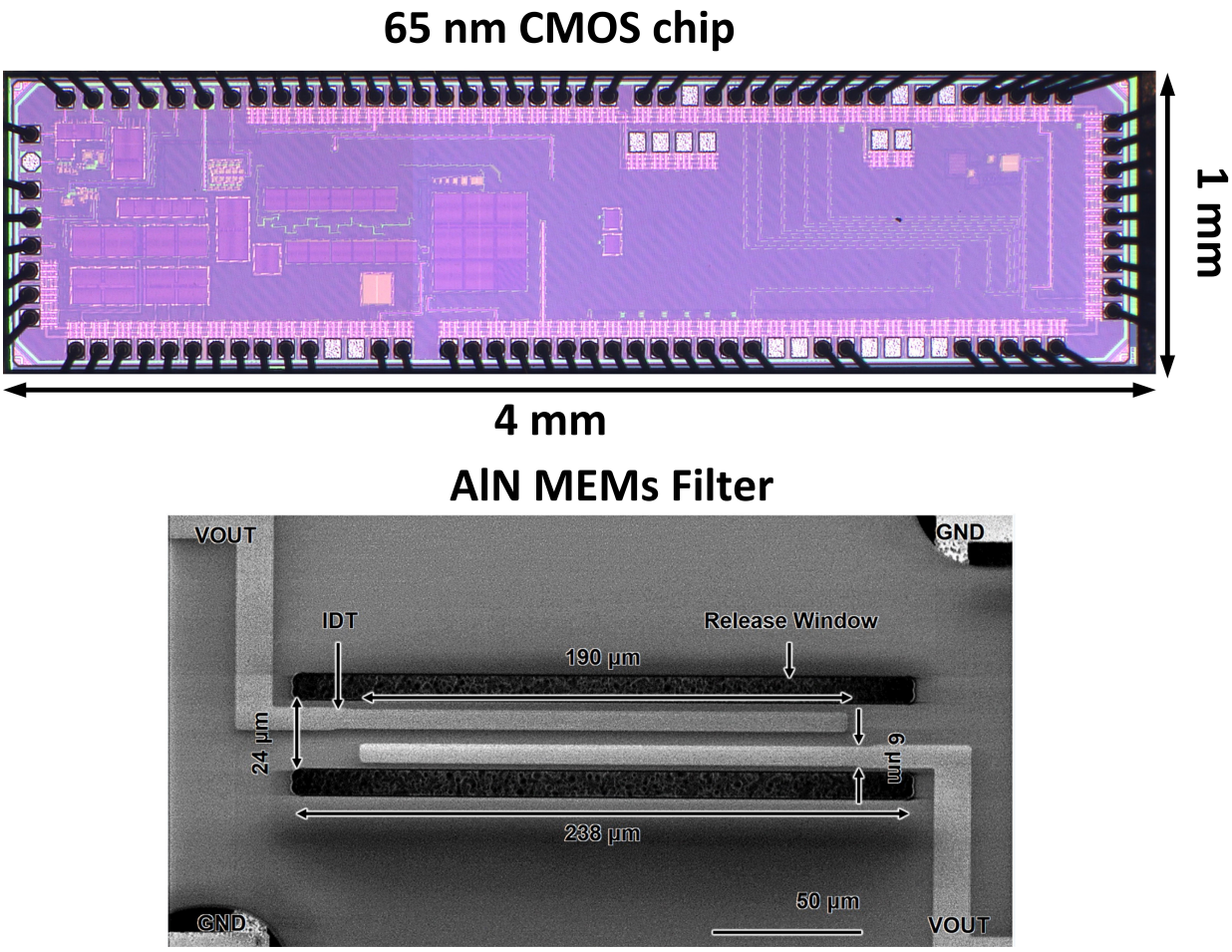


Figure 5.9: Carrier- to-interferer ratio across different frequency offsets above and below the center frequency measured at -102dBm 1% BER. This measurement shows a 16dB rejection at a frequency offset of 500kHz and a 22dB rejection at a 3MHz offset.

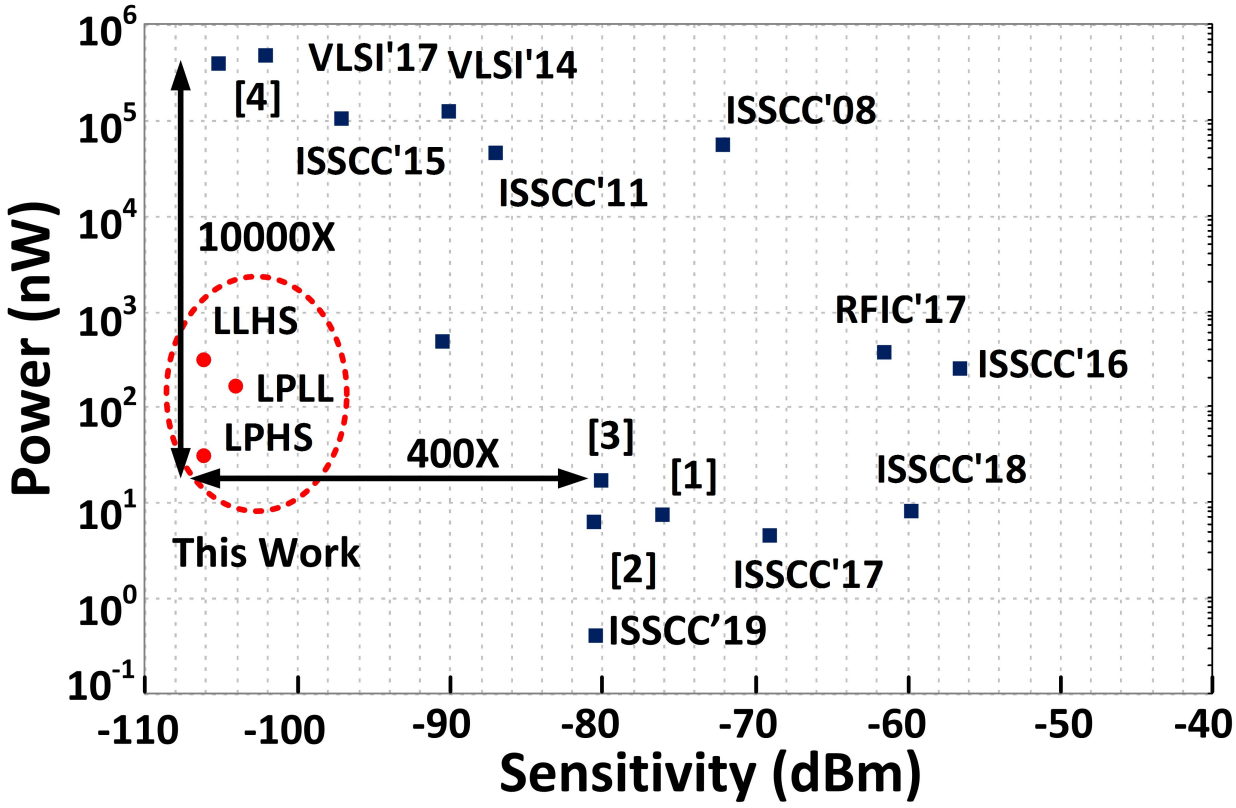


Figure 5.10: Scatter plot of sensitivity and power consumption of state-of-the-art wake-up receivers. This work shows a 26dB improvement over existing sub-microwatt receivers and a 10,000X improvement in power consumption over existing -100dBm receivers.

Table 5.1: Summary of performance and comparison to the state-of-the-art

	This Work			[1]	[2]	[3]	[4]	ISSCC'16
	LPHS	LLHS	LPLL					
Technology	65 nm			130 nm	65 nm	65 nm	65 nm	65 nm
Carrier Frequency	428.3 MHz			151.8 MHz	113 MHz	2.4 GHz	433 MHz	2.4 GHz
Sensitivity	-106 dBm	-106 dBm	-103 dBm*	-76 dBm	-80.5 dBm	-80 dBm	-102.5 dBm	N/A
Power Consumption	33 nW	288 nW	161 nW	7.4 nW	6.1 nW	17 nW	378 µW	236 nW
Latency/Data Rate	5 s	240 ms	240 ms	92.5 ms	180 ms	5 s	1kbps	12.8 ms
Interferer Rejection	AGOC/MEMS			Offset Comp	N/A	N/A	N/A	N/A
CIR @ 0.1% Offset	-16 dB			-27 dB	N/A	N/A	N/A	N/A
Sensitivity BER	-103			-75	N/A	N/A	N/A	-56.5
Die Area	3.95 mm^2			1.95 mm^2	6 mm^2	4 mm^2 *	2.25 mm^2 *	1.1 mm^2 *

* Measured at 99.7% Probability of detection

and -102 dBm sensitivity. This comparison to the work shown in [60] shows that the proposed bit-level duty cycled architecture obtains over 100X less power consumption when compared to a directly scaled design.

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5.8 Conclusions

The initial demonstration of the Samplifier architecture has improved the state-of-the-art sub-microwatt wake-up receiver sensitivity by three orders of magnitude. This advancement has enabled many exciting new applications since smart-sensor node technologies were previously limited by operating range.

The Samplifier architecture has shown considerable tunability, allowing a single receiver design to facilitate many applications. This flexibility reduces the overhead associated with approaching new smart-sensor node applications from the wake-up receiver perspective. Furthermore, the adoption of more complex signaling schemes promises to enable increased robustness-to- interference for operation in the chaotic RF environment.

The second Samplifier system, while still in testing, is showing promising results for potentially increasing the sensitivity of state-of- the-art wake-up receivers another 5-10dB while improving the interference robustness of the first design another 10dB.

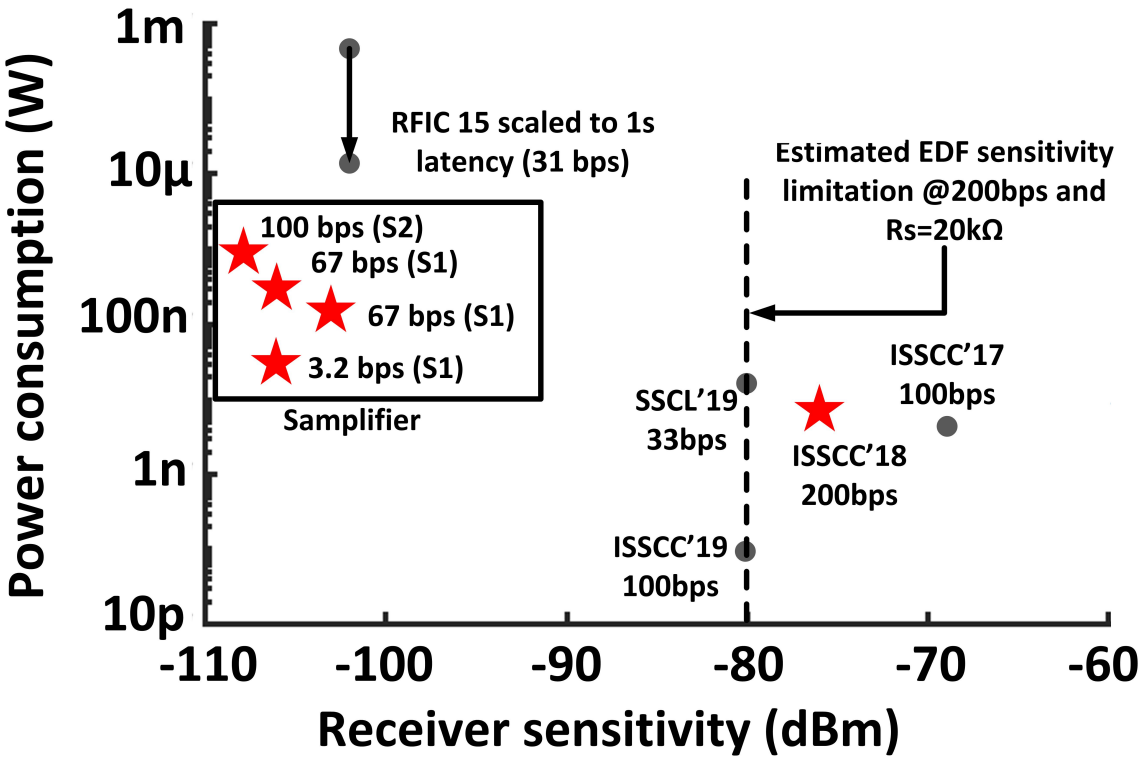

Figure 5.11: Comparisons with work presented in chapter two highlighting estimated sensitivity limitations, and showing other recently published ED first receivers. Also shown in a higher power SOA receiver directly scaled to a 1s latency.

5.9 List of contributions

1. Co-developed a high-level conceptual idea behind the Samplifier architecture and proposed it as a solution to the SNR limitations found in the current state-of-the-art.

2. Developed modeling techniques and designs enabling the TRF architecture to make a greater than 20 dB jump in sensitivity over the current state-of-the-art designs.

3. Developed system-level architecture, including the principal components needed for successful demonstration.

4. Developed the theory behind the interference-related limitations associated with bit-level duty cycling and proposed a two-tone modulation to reduce these effects.

5. Contributed to the development of the AGOC architectures, explicitly helping to develop the analog block requirements and architecture for the system.

6. Led a team of students working on sub-system design and oversaw overall system architecture.

7. Developed the system architecture and performed top-level integration for both generations of wake-up receiver.

8. PCB design and testing lead for the first Samplifier, as well as PCB design and testing assistant on the second.

This work was done in collaboration with Anjana Dissanayake, Henry Bishop, Ningxi Liu, Divya Duuvri, and Ruochen Luo.

CHAPTER 6

TUNED FRONT END RECEIVER ANALYSIS AND DESIGN FOR SAMPLIFIER WAKE-UP RECEIVERS

6.1 Motivation

Careful RF front-end (RFFE) design is critical for obtaining high sensitivity and low power operation. A reduction in active power consumption leads to improved RF sensitivity in bit-level duty cycled receivers at a constant system average power consumption, while lowering the front-end power enables a longer integration time. Active RFFE power consumption is typically dominant over the rest of the systems power consumption. This high-power consumption occurs due to the very high bias currents required to bias the active devices into a regime where active RF gain is available, as seen in equation (5.2).

Several techniques are utilized in this work to improve the sensitivity and minimize the power consumption of the TRF receiver. These techniques consist primarily of: a high-Q-factor impedance matching for low LNA noise design, a power-efficient RF gain design for the reduction of noise self-mixing though high-Q post-gain filtering, and an all-passive ED design. A diagram of the front end highlighting these innovations from the 50-ohm RF input to the ED output is detailed in Figure 6.1. Both Samplifier receivers taped out following the same underlying RFFE architecture, with changes made to individual components to optimize performance further.

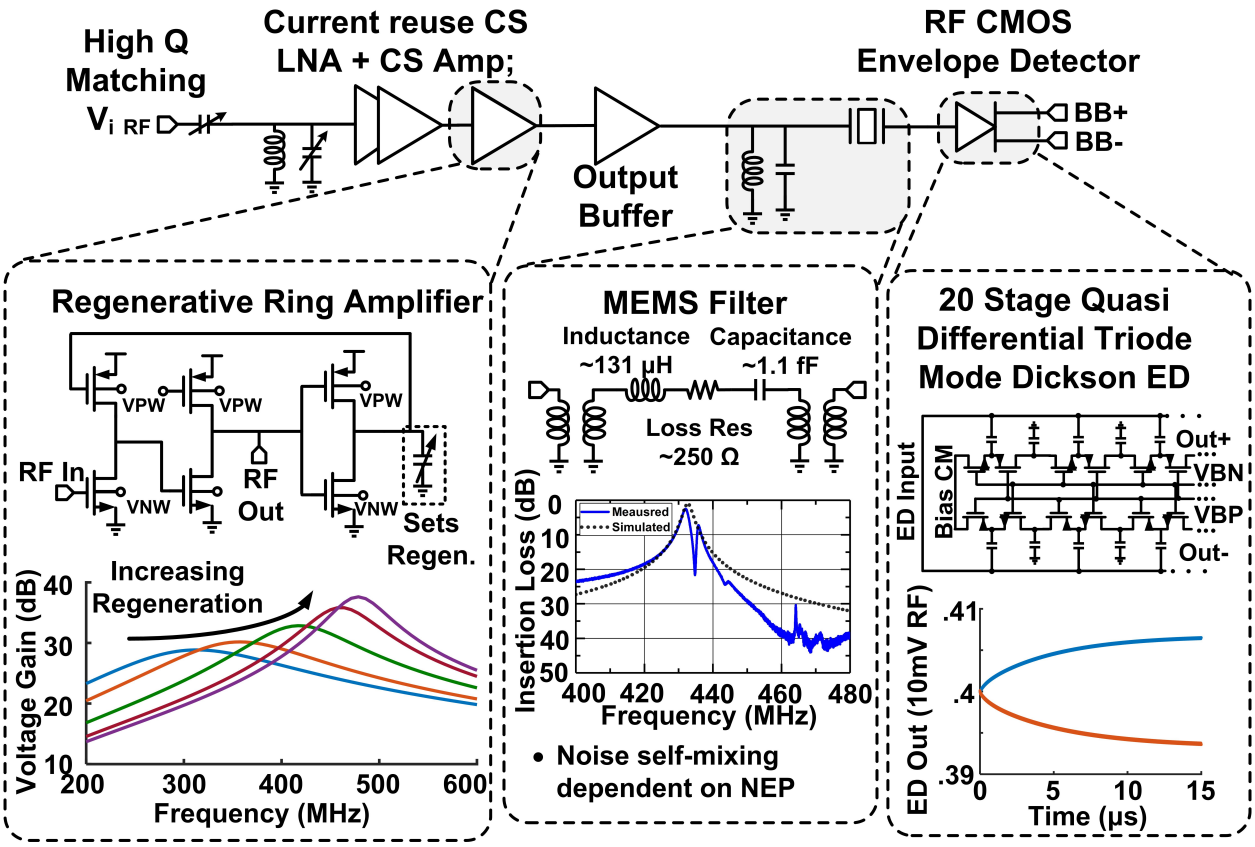

Figure 6.1: RF front-end architecture for the first-generation Samplifier receivers detailing the critical components utilized, including the regenerative ring amplifier, MEMS filter, and TMD envelope detector

6.2 Summary of TRF noise analysis

A general solution for the ED output signal and noise levels is provided in the Appendix. The Appendix has utilized a time-domain approach, allowing for the analysis of the general input RF noise spectrum and input RF signals. For the particular case of a brick wall filter, this analysis reduces to the results found in [69]. These findings show that TRF receivers require special design considerations in the RF gain stages in order to maximize front-end sensitivity. There exist three principal noise sources to consider in TRF design: self-mixing noise, noise signal mixing, and noise generated in the ED detector and baseband circuits. The noise interactions in the tuned RF

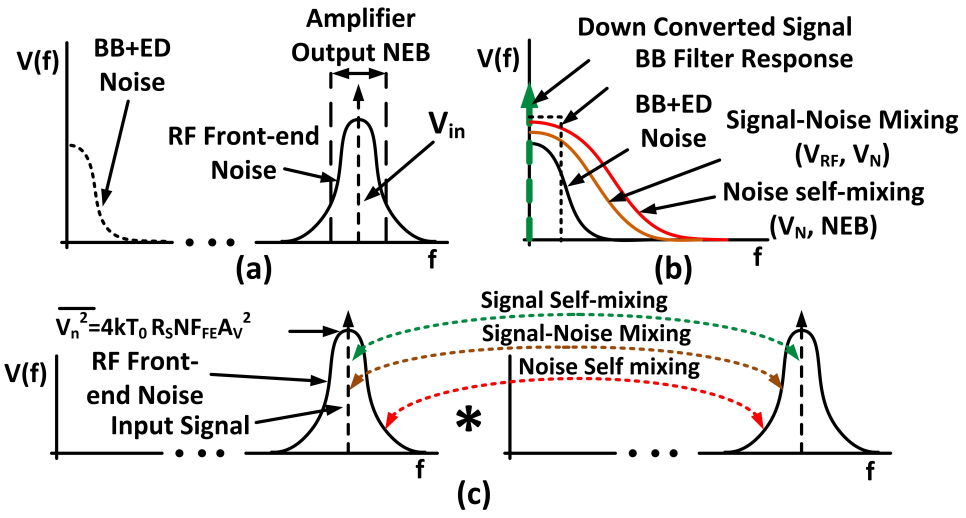

Figure 6.2: Detailed noise interactions and down-conversion in TRF receivers through square-law envelope detectors showing: (a) noise and signal power spectral densities before the square law operation; (b) output down-converted signal from the RFFE, along with noise components present at the output of the baseband, including BB/ED noise, noise signal mixing effects, and noise self-mixing effects; and (c) graphic depicting various mixing effects on the square-law ED.

receiver are visualized in Figure 6.2, where the various mixing effects are detailed. Examining equation (6.1) and adding a term $S_{BB}(f)$ to account for the detector noise as well as the input-referred noise of the baseband we can write

$$\overline{v_n^2(f)} = \alpha^2((\underbrace{8V_{RF}^2 kT_{Sys}R_s}_{\textbf{Noise-Signal Mixed}} + \underbrace{4(T_{Sys}kR_s)^2 B_{RF}}_{\textbf{Noise-self Mixed}} + \underbrace{S_{BB}(f)}_{\textbf{ED and BB Noise}}). \quad (6.1)$$

Equation (6.6) is the general form of the output noise power spectral density out of the ED. Note that only the noise term related to the ED and baseband noise are frequency dependent, as, when assuming $B_{RF} << B_{BB}$, the noise generated from the RFFE can be assumed to be white.

6.2.1 Noise self-mixing and detector noise bandwidth

The detector output noise resulting from self-mixing noise is a direct function of the total integrated noise power passed into the ED. This relationship necessitates the use of high-Q-factor noise filtering prior to the ED. Utilizing high-Q-factor filtering at the RF input of the receiver fails to filter any noise injected by the RF amplifier stages. The noise injection after the RF gain stages means that the optimal position for an external high-Q-factor filter is after the RF gain stages and before the ED.

From a communication systems design perspective, the narrowest bandwidth filtering typically occurs before the decision circuit to optimize the SNR into the ADC. Noise filtering before the RF ED does not necessarily limit the equivalent noise bandwidth at the ADC. The RF noise filtering instead changes the noise power spectral density out of the ED and does not directly change the noise bandwidth out of the detector. For this reason, additional filtering in the baseband receiver is needed to reduce the noise- equivalent bandwidth out of the ED in order to optimize the SNR. Many radio receivers utilize high-Q-factor filtering before the RFFE in order to reduce the impact of out-of-band interfering signals, followed by a down-converter stage to increase selectivity further and then a matched filtering stage to optimize the SNR. The use of high-Q-factor RF filtering before the RF gain stages improves out-of-band front-end linearity but does not significantly reduce the noise self-squaring, which significantly reduces the receiver sensitivity.

Noise injected after the input RF amplifiers has degraded the sensitivity of many state-of-the-art TRF- based receivers [49]. Post-amplification filtering is required to suppress the noise self-mixing effect and enable high RF sensitivity (Fig. 6.2). Rearranging the TRF receiver, as shown in Figure 6.3b, enables a sensitivity increase in the front end.

The RF-noise-equivalent bandwidth at which the down-converted noise dominates is found through examining the noise-signal mixing and the noise self-mixing terms in the Appendix (A.53), equating these terms, and solving for the RF-noise-equivalent bandwidth where they are equal leads

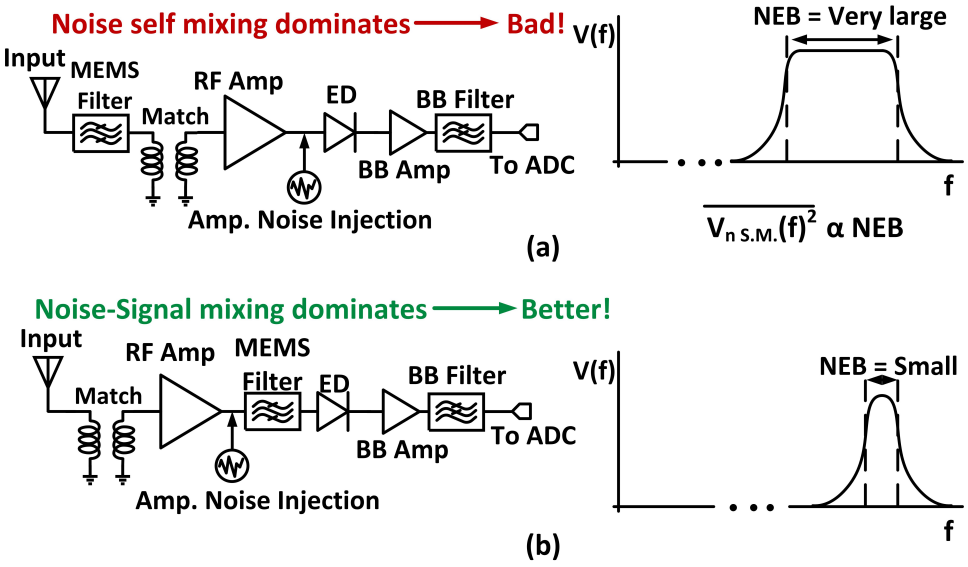

Figure 6.3: Comparisons between the location of high-Q-factor MEMS filtering rearranging the filter from: (a) the RF input, which is typically used to improve the linearity of the RF receiver, and (b) positioning the MEMS filter before the ED to optimize sensitivity through reducing the noise self-mixing effect, which increases the ED output noise power spectral density.

to

$$B_{RF} < \frac{2V_{RF}^2}{T_{Sys}kR_s} = \frac{2V_i^2}{T_0F_{FE}kR_s} = \frac{4P_{RF}}{T_0F_{FE}k}, \tag{6.2}$$

T_{Sys} is the noise temperate at the ED, V_i and T_0 are the input RF voltage and temperature, respectively, referred to the input, R_s is the source impedance presented by the matching network at resonance, F_{FE} is the noise factor of the input RF amplifier, and P_{inRF} is the input RF signal power. The second and third equalities relate to the signal and noise terms referred to the RF amplifier input. Equation (6.2) represents an SNR at the ED, for which greater SNRs lead to signal noise mixing dominating over noise self-mixing. Equation (6.2) makes sense intuitively; when the noise fluctuations at the ED are more significant than the signal level, self-mixing noise should dominate. This result also indicates that as sensitivity is improved, the RF NEB at which noise self-mixing dominates decreases further.

When the noise self-mixing dominates the detector output noise level, the minimum detectable signal is inversely proportional to the square root of the baseband bandwidth, entailing a square-law sensitivity trade-off with bandwidth similar to that for the ED-first receiver.

6.2.2 Noise down-conversion through interference

Sufficiently strong interference degrades the sensitivity of every RF receiver, and interference rejection is an important consideration in any receiver design. For a square-law TRF, both the interference power and frequency offset determine the impact of the interference. For the case of interference at a frequency offset Δf, equation (A.47) is modified as

$$S_{vo}(f) = \alpha^2((\frac{V_{Int}^4}{4} + V_{Int}^2 4kT_{Sys}B_{RF}R_s + (4kT_{Sys}B_{RF}R_s)^2)\delta(f) + 8V_{Int}^2 kT_{Sys}R_s S_{LP}(f+\Delta f) + 4(T_{Sys}kR_s)^2)S_{LP}(f) * S_{LP}(f)), \quad (6.3)$$

assuming no RF input and an interfering signal of amplitude V_{Int}. The most prominent effects in the case of a strong interfering signal are the down-converted RF noise and the DC offset produced by the interference. Techniques presented in Chapter 5 attempt to address the DC offsets making detection more difficult. A more fundamental issue than the baseband offset is noise down-converted by the interference, which in (6.4) is represented by the term

$$S_{vo}(f) = \alpha^2 8V_{Int}^2 kT_{Sys}R_s S_{LP}(f+\Delta f). \quad (6.4)$$

This noise down-conversion is visualized in Figure 6.4, which shows how the RF down-converted noise changes based on interference frequency offset. When the interfering signal is at a large frequency offset from the center frequency of the output filter, the output filter attenuates the interference, weakening the down-converted noise power. Furthermore, at large frequency offsets, the input RF noise mixes with the interfering signal and down-converts the noise to an IF frequency. For interference outside of the RF filter, the bandwidth mixes with RF noise at a frequency offset

from the center frequency of the RF filter, down-converting the noise to some IF frequency. Assuming a small baseband bandwidth $B_{BB} << B_{RF}$, this down-converted noise can be represented as

$$S_{vo}(0) \propto P_{Int} S_{LP}^2(\Delta f) \tag{6.5}$$

for the bandwidth of the baseband filter.

Equation (6.5) implies that the RF filter reduces the down-converted noise by twice the rejection of the output filter. This doubled rejection arises due to the filtering of the interference at RF frequencies as well as the frequency offset from the DC of the down-converted noise. In a configuration similar to the one shown in Figure 6.3a, a wide-band RF noise injected after the input filter will mix with the interfering signal and down-convert at an IF frequency similar to the configuration shown in Figure 6.3b. The major drawback of Figure 6.3a is that the down-converted noise now has a much higher bandwidth, meaning that only the signal is rejected by the filter. These results imply that the configuration shown in Figure 6.3b not only offers better sensitivity but, in the case of close-in interference, can offer superior interference robustness.

6.2.3 TRF front-end gain requirements

In TRF receivers, increasing the RF gain enables a higher sensitivity level until the down-converted RF noise dominates over baseband and ED noise. Increasing the RF gain beyond this limit has two detrimental effects on the receiver, where the first is increased power consumption, and the second is decreased front-end linearity. Examining the equation (6.1)

$$S_{vn}(f) = \alpha^2[16V_{RF}^2 T_{Sys} k R_s + 8B_{RF}(T_{Sys} k R_s)^2] + S_{BB}(f), \tag{6.6}$$

and equating the RF down-converted noise terms and the ED/baseband noise leads to

$$S_{BB} = 8\alpha^2 A_{vAmp}^4[2V_i^2 T_0 F_{FE} k R_s + B_{RF}(T_0 F_{FE} k R_s)^2]. \tag{6.7}$$

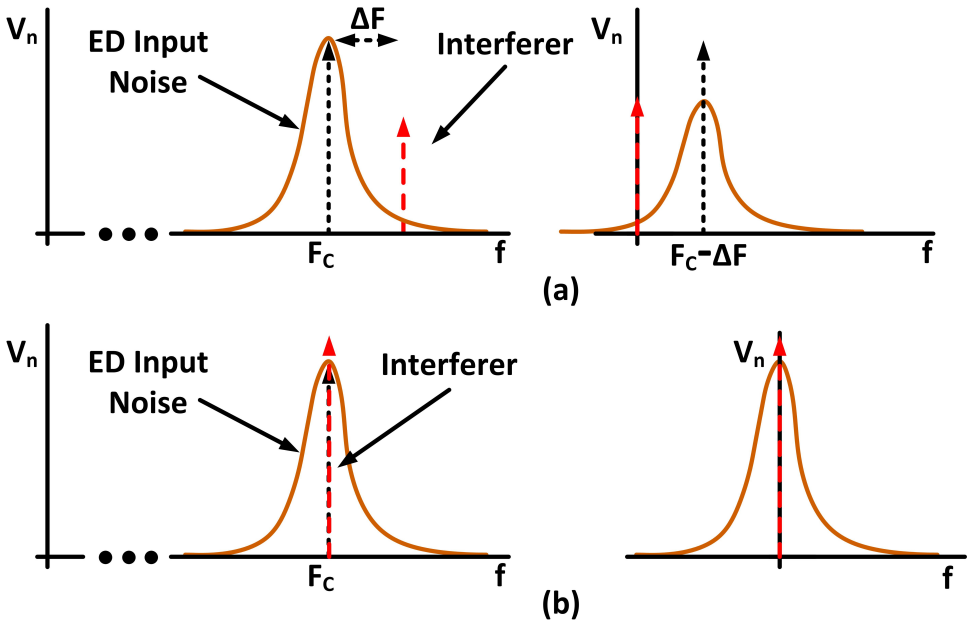

Figure 6.4: This figure shows the down-conversion of RF noise through an interfering signal. If the interferer is centered in the bandwidth of the filter, the detector output noise floor increases with the interferers power. If the interferer is out-of-band, the filter attenuates the interferer, weakening the noise down-conversion directly. Furthermore, the maximum noise down-conversion occurs at some IF frequency which can be filtered out, reducing the impact of the down-converted noise from the out-of-band interference.

Solving this last equation for the minimum RF gain required for the noise power spectral density of the down-converted RF noise to equal the noise power spectral density of the baseband noise without any RF input leads to

$$A_{vAmp} > \sqrt[4]{\frac{8\alpha^2[2V_i^2 T_0 F_{FE} k R_s + B_{RF}(T_0 F_{FE} k R_s)^2]}{S_{BB}}}, \tag{6.8}$$

and

$$A_{vAmp_M in} \propto \frac{\sqrt{\alpha}}{\sqrt{v_{N.BB}}} = \sqrt{NEP_{ED}}, \tag{6.9}$$

where $V_{N.B.B}$ is the noise voltage spectral density referred to the output of the ED. Equations (6.8) and (6.9) have several implications in the design of TRF receivers. Equation (6.8) implies that

RF noise dominates at lower gain levels for front-end amplifiers with high noise figures. Equation (6.9) relates the minimum RF front-end gain A_{vAmp_Min} to the noise equivalent power of the RF envelope detector, indicating that EDs with better NEP require less RF gain to obtain optimum sensitivity.

6.3 Introduction to ULP RF amplifier design

RF design in the ULP regime does not fundamentally differ from design at higher power levels. While there are different design considerations, the basic intuition behind circuit performance does not change significantly between traditional RFIC design and design in the ultra-low-power regime. The most significant difference between RF design at ultra-low-power levels and traditional design is the relative impedance level in the circuit. Biasing devices at ultra-low bias currents means that the transconductance of each device is very small. The low transconductance makes these devices struggle to drive capacitive loads at high frequencies. The small transconductances and high self-gain found at ULP bias points indicate that the active devices have very high output impedances.

Inductively-loaded amplifier stages are impractical in the ULP regime when considering both on-chip and off-chip inductors due to limited Q-factors and inductor size. The low-Q low-value inductors require a relatively large amount of bias current to drive due to their low impedances. Several works have implemented ULP amplifiers utilizing active inductors, but these approaches require higher voltage headroom, thus increasing power and reducing linearity [38], [70].

At ultra-low bias current levels, conventional RF amplifier design becomes difficult due to the increased impact of parasitic capacitances. Components, such as polysilicon and diffusion resistors, present high levels of bulk capacitance, which degrades the amplifier bandwidth and necessitates higher bias currents in the RF amplifiers. Coupling capacitors in the signal path also degrade bandwidth due to bulk capacitance, which necessitates an increase in bias current.

Recently, three articles published in the SSCS magazine [71], [72] and [72] develop general design equations for ULP amplifiers (and deeply scaled submicron CMOS amplifiers, in general) which

are derived from the EKV transistor model [72]. The EKV model is a robust technique used to model the operation of MOSFET devices in deeply scaled silicon processes ($L < 100nm$) and predict operation from the weak to the strong inversion regime. The unified current equation from the EKV model in its simplified form is

$$e^{\sqrt{(IC)}} = e^{v} + 1, \tag{6.10}$$

where IC is known as the "inversion current" and defined as

$$IC = \frac{I_D}{I_{D0}W/L}, \tag{6.11}$$

where $v = \frac{V_{VGS}-V_{th}}{2nV_t}$ and $I_{Spec} = K(2nV_t)^2$. IC represent normalized device currents for which a given technology is only dependent on the transistor type used in the design and not on other design variables. An inversion coefficient of unity for a minimum-length device in the 65nm LP process corresponds to roughly $1.5\mu A/\mu m$; this current density corresponds to operation in the moderate inversion region.

For the strong inversion regime or $v >> 1$ and current $IC = v^2$ and weak inversion regime with $v << 1$, the current varies exponentially with the applied voltage or $IC = e^{2v}$. When the applied voltage is near threshold, neither sub-threshold modeling nor strong-inversion modeling is accurate. [72] has proposed classifying the operating regions based on the inversion coefficient and not the applied voltages. This definition better captures the change in transconductance between these two regions and explicitly models a third operation region known as the "moderate inversion" region. Many works have proposed the moderate inversion region [73], [74], [71] and [75] due to the optimum performance metrics being found in this region. Typically, most ULP RF amplifier design is performed in the moderate inversion region, meaning that accurate models of this region are crucial. The regions classified by the inversion coefficient are typically defined as

$$IC \leq 0.1 \sim WI, \tag{6.12a}$$

$$0.1 < IC \leq 10 \sim MI, \tag{6.12b}$$

$$10 < IC \sim SI. \tag{6.12c}$$

From the more complicated form of the EKV model shown in [72] taking into account velocity saturation (σ_d), expressions for the device transconductance (6.13), output impedance (6.16), and transconductance efficiency are defined for the normalized device current.

$$g_m = G_{spec}\frac{\sqrt{(\lambda_c IC+1)^2+4IC}-1}{\lambda_c^2 IC+\lambda_c+1}, \tag{6.13}$$

where $G_{spec} = I_{spec}/V_t$. Assuming that $\lambda_c \approx 0.32$ from [71] and $IC < 3$, we can reduce (6.13) to

$$g_m = G_{spec}\frac{\sqrt{4IC+1}-1}{2}, \tag{6.14}$$

which, for $IC = 3$, has an error of approximately 15% compared to the full expression. For ICs of 0.5 and 1, the errors between these expressions reduce to 4.5% and 7%, respectively. This reduced form for gm allows rapid calculations for gm in the moderate inversion regime, assuming the bias point remains less than $IC < 3$. Dividing this expression by IC leads to the trans-conductor efficiency, which, with a similar approximation, leads to

$$\frac{gm}{IC} = G_{spec}\frac{\sqrt{4IC+1}-1}{2IC}. \tag{6.15}$$

Comparing the transconductance efficiency presented in (6.13) and (6.14) to the ideal sub-threshold transconductance shows that the sub-threshold model underestimates the current efficiency significantly. Comparing a device biased at $IC = 0.1$ with the efficiency predicted in sub-threshold modeling leads to an error of about 10%, while comparing devices biased at $IC = 1$ and $IC = 3$ leads to errors of approximately 50% and 65%, respectively, indicating that significant errors are obtained in the middle of the moderate inversion region when using sub-threshold modeling.

The device output impedance g_{ds} is needed to calculate amplifier gain levels and the device self-gains $g_m g_{ds}$. This parameter can be found with

$$g_d = \sigma_d gm, \tag{6.16}$$

where $\sigma_d = \delta V_t / \delta V_{DS}$ and accounts for DIBL (Drain Induced Barrier Lowering) in the device. DIBL, rather than channel length modulation, is the dominant factor in output impedance for devices biased into weak or moderate inversion in deeply scaled CMOS ($< 100nm$). This simple dependency allows for the transistor self-gain to be written as $A_{self} = 1/\sigma_d$.

6.4 High-impedance interface LNA noise figure optimization

Previous work in the near-zero- power level detector-first receivers has exploited off-chip high-impedance matching between the detector and RF source to maximize sensitivity [56], [4], [50]. While the noise considerations may be different between the two architectures (TRF and ED-first), both benefit from having a high-impedance high-voltage interface between the RF source and the CMOS input.

The input LNA utilizes a self-biased current-reuse common-source amplifier ([76]) cascaded with a self-biased common-source amplifier with a pseudo-resistor bias, as shown in Figure 6.5a. The amplifiers were biased for optimum amplifier efficiency [37], as defined by (6.17) ,which entailed biasing into the moderate inversion regime.

$$\eta = \frac{A_{vdB}}{P_{DC}} \tag{6.17}$$

Utilizing high-Q-factor passive gain enables a substantial impedance transformation and narrow input RF bandwidth. This high- impedance transformation leads to a sizeable passive RF voltage gain, which drives the high- impedance CMOS and optimizes amplifier efficiency (Figure 6.5b). A simple way to understand the high-Q-factor LNA input matching is to consider that the source impedance has been power matched to the loss resistance of the matching network inductor at resonance. Power matching the RF input to the loss resistance enables maximization of the voltage at the CMOS input. This technique is similar to matching to a fixed-loss resistance in parallel with the LNA input, which typically entails a 3 dB noise figure degradation [77] while enabling an

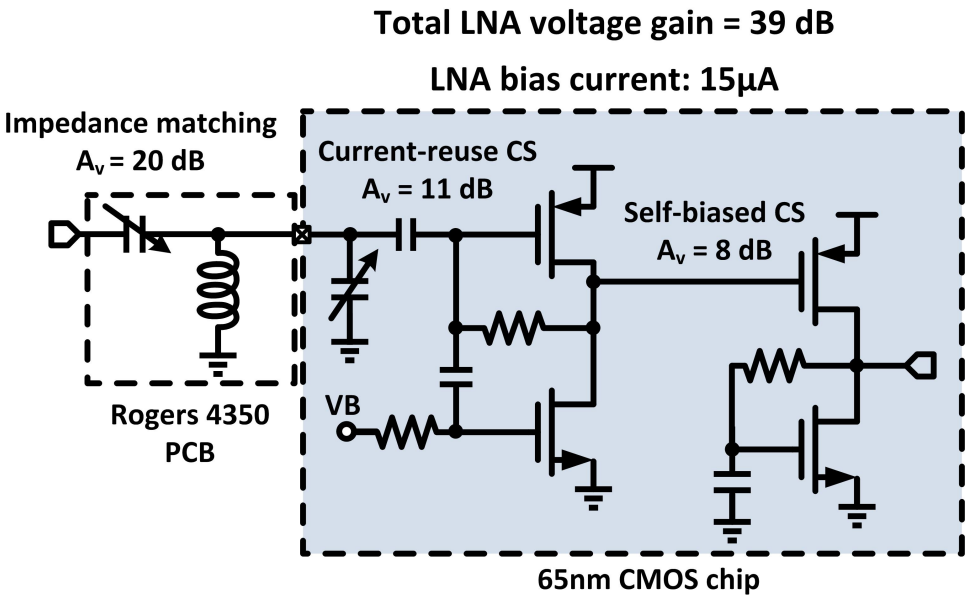

Figure 6.5: Schematic diagram of the two-stage input LNA used in the first Samplifier, including off-chip high-Q-factor lumped-element impedance matching to optimize front-end noise figure and gain.

input power match. Under this power matched condition, the LNA noise figure versus transformer Q-factor is shown in Figure 6.6b, where it can be seen that higher matching network Q-factors lead to better LNA noise figures and passive voltage gains. The combination of a high passive voltage gain from the impedance transform and the active power gain of the CMOS LNA lead to a high amplifier efficiency of 2.6M, with a voltage gain of 39 dB and power consumption of $15\mu W$.

One difficulty in estimating the overall receiver sensitivity utilizing the high-Q-factor input matching technique is the uncertain inductor Q-factor. Measured and modeled Q-factors deviate significantly, likely due to PCB parasitics as well as difficulties in characterizing the high-impedance inductors. A comparison of simulated passive voltage gain and LNA noise figures across varying matching network Q-factors is shown in Figure 6.6. A significant performance hit occurs when the resonator Q-factor drops from the 140 shown on the inductor datasheet to the measured Q-factor of between 30 and 40. This degradation entails a noise figure increase from 3.7 dB to 6.5 dB as well as a 6 dB decrease in the passive voltage gain obtainable. Furthermore, this degradation also

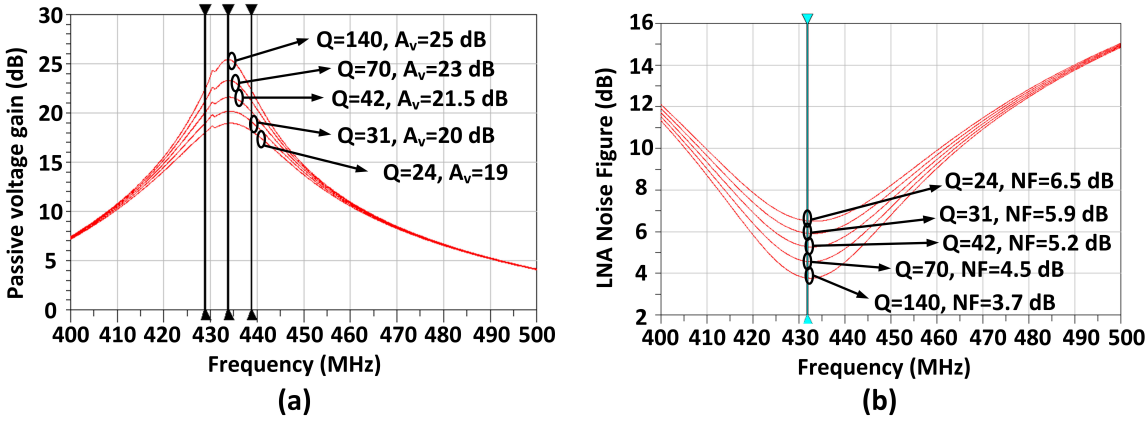

Figure 6.6: The comparison of (a) an LNA passive voltage boost, and (b) a noise figure across varying inductor Q-factors showing a 6dB drop in voltage gain as well as a 3dB noise figure hit when the inductor Q-factor drops from the modeled 140 to the measured 24.

increases the 3dB bandwidth of the input match, which decreases receiver interference rejection.

The RFFEs for both Samplifier designs utilized the same input current-reuse common-source LNA, while the second front end did not use the self-bias common-source stage but instead utilized a secondary neutralized ring amplifier to provide additional gain.

6.5 Power-efficient RF gain design

A reduction in RF front-end power consumption leads to superior sensitivity in the bit-level duty cycling scheme. For constant system-level DC power consumption, operating at a reduced power allows the RF front end to remain active for longer, which increases sensitivity. In order to maximize sensitivity, the design of power-efficient RF gain stages is crucial to system-level optimization.

Utilizing a high-gain LNA before the main RF gain stage enables relaxation in the noise figure of the RF gain stage. This relaxed noise figure allows the design to focus on optimizing the amplifier

efficiency metric shown in equation (6.17). Aside from amplifier efficiency, other design considerations for the RF gain stage are a fast-startup time required for bit-level duty cycling, robustness to PVT variation, and low voltage operation to reduce power consumption and increase headroom. One final attribute needed is a band-pass gain in the RF gain stage. Band-pass gain suppresses DC offsets in the gain stages, increasing the robustness to PVT. Band-pass gain also reduces the RF noise levels out of the amplifier, which can appreciably impact the DC operating point of the buffer amplifier.

There are a wide variety of ultra-low-power amplifiers which can provide the high levels of RF gain required in the TRF receiver. A few common amplifier topologies are shown in Figure 6.7 a,b,c,d. Figure 6.7b shows an attractive ULP amplifier topology, which is called a self-biased common source amplifier. The PMOS device and bias tee compose a simple gyrator circuit which rejects low-frequency noise and provides a band-pass response. Pseudo-resistors can be used to implement the biasing resistor used in this design in order to reduce the parasitic capacitance and improve efficiency. Unfortunately, the pseudo-resistors are very PVT sensitive, and it is challenging to synthesize relatively small value resistors. These devices typically present resistances in the tens of giga-ohms, which either significantly reduces front-end start-up time or necessitates a very large device which degrades amplifier efficiency. The amplifiers shown in Figure 6.7c,d are common current reuse amplifiers used in ultra-low-power design. The amplifier in Figure 6.7c has very high efficiency but has offset issues when cascaded in large chains, and the circuit in Figure 6.7d has degraded efficiency due to the coupling capacitor appearing in the signal path.

An exciting class of amplifiers for consideration are the regenerative amplifiers [31], [78]. These amplifiers can exhibit very high gains at low bias currents, leading to very power-efficient designs. The high efficiency arises from a slight amount of controlled positive feedback, enabling the closed-loop gain to exceed the open-loop gain of the amplifier. Typically, regenerative amplifier topologies can be mapped to conventional oscillator topologies. In these amplifiers, the loop gain is controlled digitally to set the gain and Q-factor. The amplifier employed in [31], [79] and [79] is based on a cross-coupled oscillator backed off from the oscillation point. The negative impedance of the amplifier cancels the positive resistance of the source and creates positive gain at the port

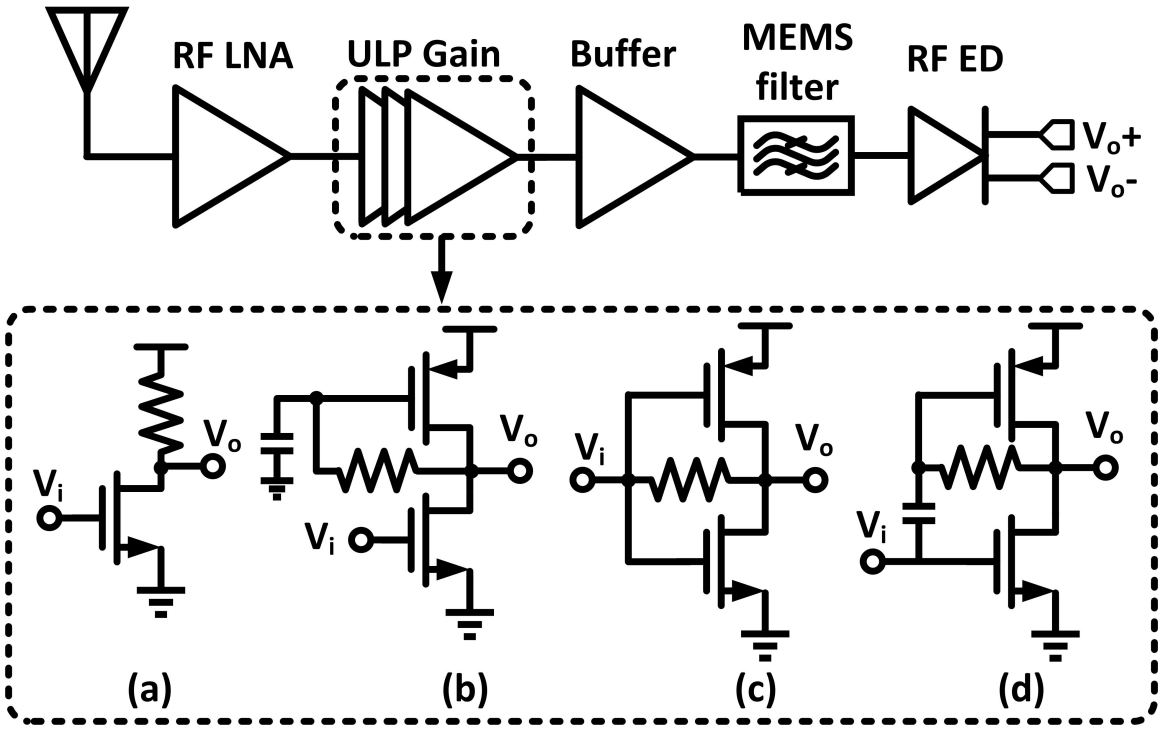

Figure 6.7: Sample RF gain cells for consideration, including: (a) a restively loaded common-source amplifier, (b) a self-based active-load common-source amplifier, (c) a current-reuse common-source amplifier, and (d) a self-biased current-reuse common-source amplifier.

of the antenna. The amplifier employed in [78] utilized a Colpitts-oscillator-based amplifier which has been backed off from the point of oscillation to operate in a regenerative gain mode. Both of these designs employ an LC resonator to form a regenerative amplifier. Resonator-based regenerative amplifiers consume large currents due to the relatively low inductor Q-factor, so a more power-efficient resonator-free amplifier is desirable.

Modifying the conventional ring oscillator into a regenerative amplifier can be accomplished through the configuration shown in 6.8a. This topology enables regenerative operation by modifying the pole associated with the third stage through the capacitor C_N. This technique enables a compact, tunable, and power-efficient regenerative amplifier design. The third stage does not require high bias currents as in the previous two stages, as it does not support high gains at the RF frequency, so

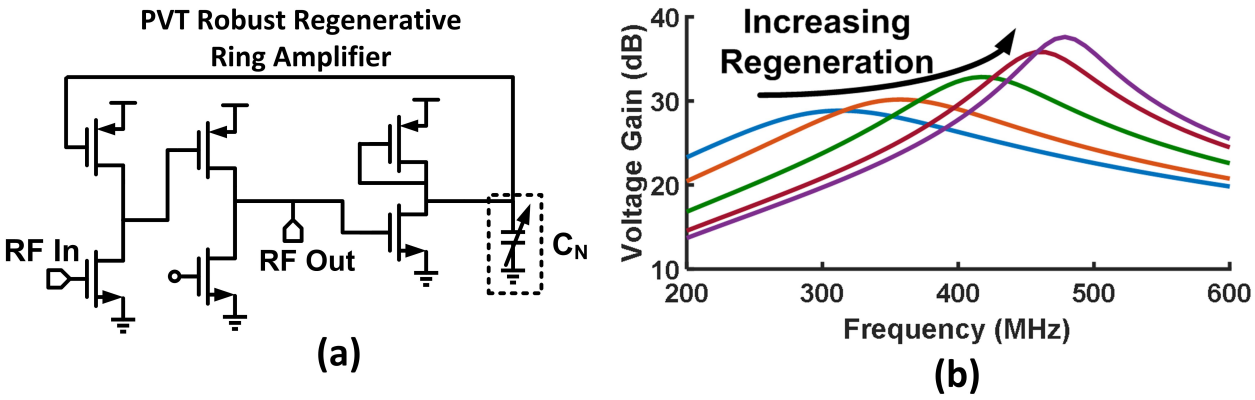

Figure 6.8: (a) Regenerative ring amplifier configured for optimum PVT robustness, where the second and third stages can be modified depending on requirements (gain, linearity, stability, and so forth). (b) Demonstration of the regenerative effect through the modification of the output capacitance on the third amplifier stage, with a constant bias current showing increasing levels of gain as regeneration is increased.

it can be current-starved to reduce power and further improve amplifier efficiency. As this design requires no pseudo-resistors, the circuit start-up can be made very fast compared to the speeds found in the more conventional ULP amplifier designs shown in Figure 6.7a,b,c,d. Through trimming both the amplifier bias current and the capacitor C_N, the phase margin can be lowered to provide higher levels of regeneration, which increases gain and the Q-factor at the cost of stability and robustness, as shown in Figure 6.8b.

A powerful method for analyzing the regenerative ring amplifier is through feedback analysis. Considering the amplifier as a transimpedance amplifier, where the input device is replaced with its small-signal equivalent, simplifies the analysis greatly, as shown in Figure 6.10a. Shunt-shunt feedback modeling, while neglecting C_{GD}, leads to an accurate model of the amplifier which captures the behavior of the ring amplifier. Examining the simplified model shown in Figure 6.10b,c, equation (6.18) defines the transimpedance from the current output of the first NMOS device to the voltage output of the second stage. The feedback path from the voltage input of the

third stage to the current fed back to the input stage defines the transconductance feedback path defined by equation (6.19).

The loop gain defined as the product of (6.18) and (6.19) is used to find the amplifier phase margin. Plotting closed-loop gain times for the transconductance of the input NMOS device (6.20) gives the closed-loop voltage gain; allows for the optimization of the amplifier phase margin, Q-factor, and gain levels; and gives considerable design insight into the amplifier. This analysis is especially useful in determining the sensitivity of the gain and phase margin for a particular parameter and in optimizing across a wide range of bias currents, device sizes, and transistor-size ratios.

$$A_{OL}(\omega) = \frac{-g_{m2}R_{o1}R_{o2}}{(1+j\omega R_{o1}C_{o1})(1+j\omega R_{o2}C_{o2})} \tag{6.18}$$

$$A_{FB}(\omega) = \frac{g_{mp}g_{m3}R_{o3}}{(1+j\omega R_{o3}C_{o3})} \tag{6.19}$$

$$A_{CL}(\omega) = \frac{g_{m1}g_{m2}R_{o1}R_{o2}(1+j\omega R_{o3}C_{o3})}{(1+j\omega R_{o3}C_{o3})(1+j\omega R_{o1}C_{o1})(1+j\omega R_{o2}C_{o2}) + g_{mp}g_{m3}R_{o3}g_{m2}R_{o1}R_{o2}} \tag{6.20}$$

which can be modified through $g_{m1}R_{oi} = A_{si}$ where A_{si} is the self-gain of the i^{th} amplifier stage and $R_{oi}Coi = \tau_i$ where τ_i is the time constant related to the capacitor on the i'th stage into

$$A_{CL}(\omega) = \frac{A_{s1}A_{s2}(1+j\omega\tau_3)}{(1+j\omega\tau_1)(1+j\omega\tau_2)(1+j\omega\tau_3) + A_{s1}A_{s3}A_{s2}} \tag{6.21}$$

assuming $g_{mp} = g_{m1}$.

The demonstrated regenerative ring amplifier in the first-generation Samplifier achieved a roughly 26 dB voltage gain at a DC power of $7.5\mu A$, while the second design had a simulated power consumption of $7\mu A$ and 32 dB due to operating at a lower phase margin than the initial design. Varying the second design across process and temperature corners saw a sub-2 degree phase margin degradation and a 1 dB gain degradation. These results indicate that this amplifier topology

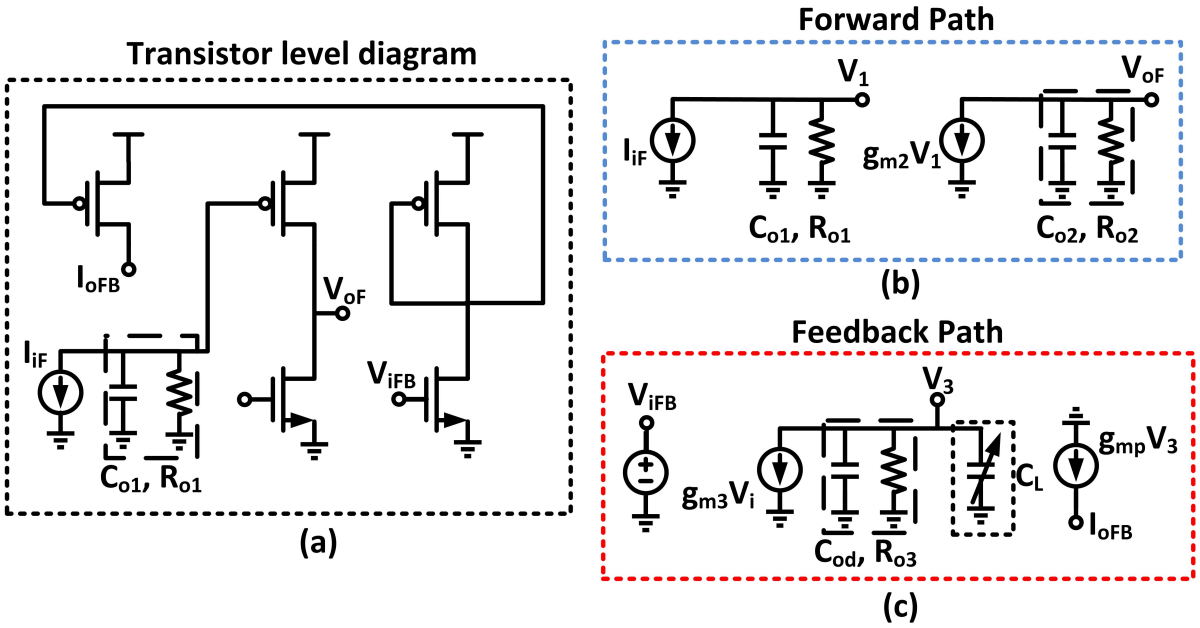

Figure 6.9: (a) Feedback amplifier model of the regenerative ring amplifier, where the forward TIA path and reverse TCA paths are shown. (b) Forward TIA path from input device to the output of the second stage. (c) Feedback TCA controlling regeneration through the output capacitance C_L

potentially offers a very- high-efficiency low-power RF amplifier suitable for use in the Samplifier design.

6.6 RF buffer and MEMS interface design

One distinct drawback of the filter configuration shown in Figure 6.3 is that the RF amplifiers must drive the off-chip filter and then return to the chip to drive the ED. This interface is very susceptible to parasitic capacitance and can require very high bias current levels in the RF buffer design. For reference, in the first Samplifier design, the RF buffer consumed roughly 40% of the RF power, while, in the second Samplifier, the RF buffer consumed roughly 35% of the RF bias current. This interface also presents very high levels of insertion loss and requires careful co-design between the RF buffer stage, PCB interface, MEMS filter, and ED circuit.

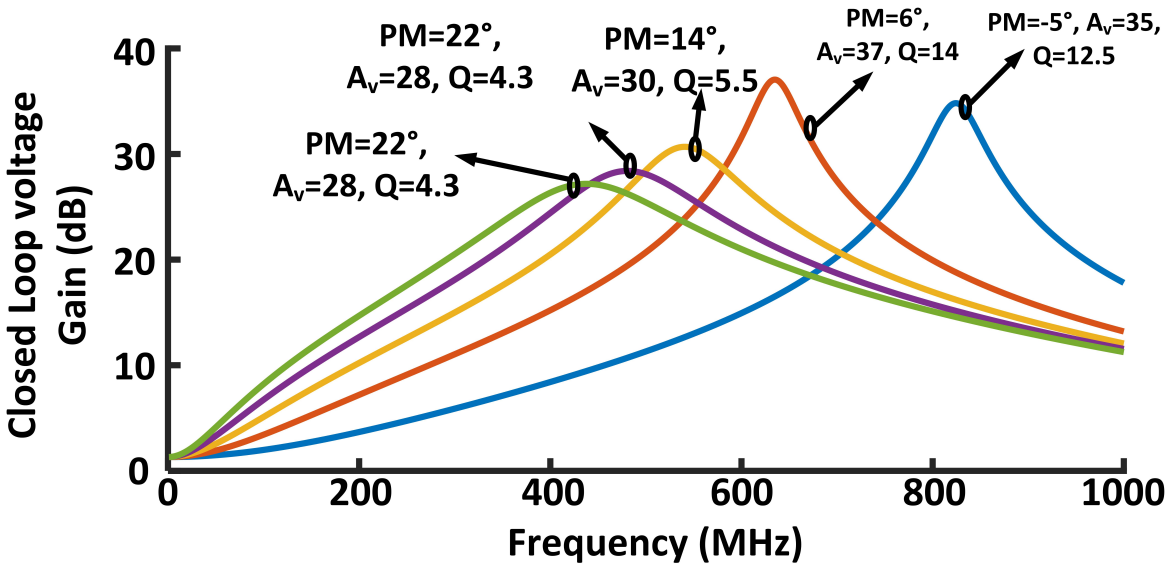

Figure 6.10: Variation in load capacitance and the variation between Q-factor, gain, and phase margin is well predicted by the simplified model of a ring amplifier.

The high sensitivity of this high-impedance interface to parasitic capacitances complicates the design. When high capacitance levels are present, the insertion loss of the MEMS filter increases, as the circuit is more susceptible to the finite Q-factor in the MEMS resonator. Two output designs have been simulated and verified in the first- and second-generation Samplifier designs. The first design was a common drain buffer amplifier presenting a low source impedance to the MEMS resonator and utilizing an external inductor to resonate out the capacitance at the interface and serve as a DC return path. The second design utilized a current-reuse common-source output stage and no external inductor.

6.6.1 Inductor-based output driver

A model of the interface used in the first design is shown in Figure 6.11a and utilizes a CMOS driver amplifier coupled onto a Rogers 4350 PCB, which houses the resonating inductor and MEMS filter. Afterwards, this filter is bonded to the PCB and back into the CMOS chip. Due to the high impedance interface and relatively low operating frequency, the impact of the wire

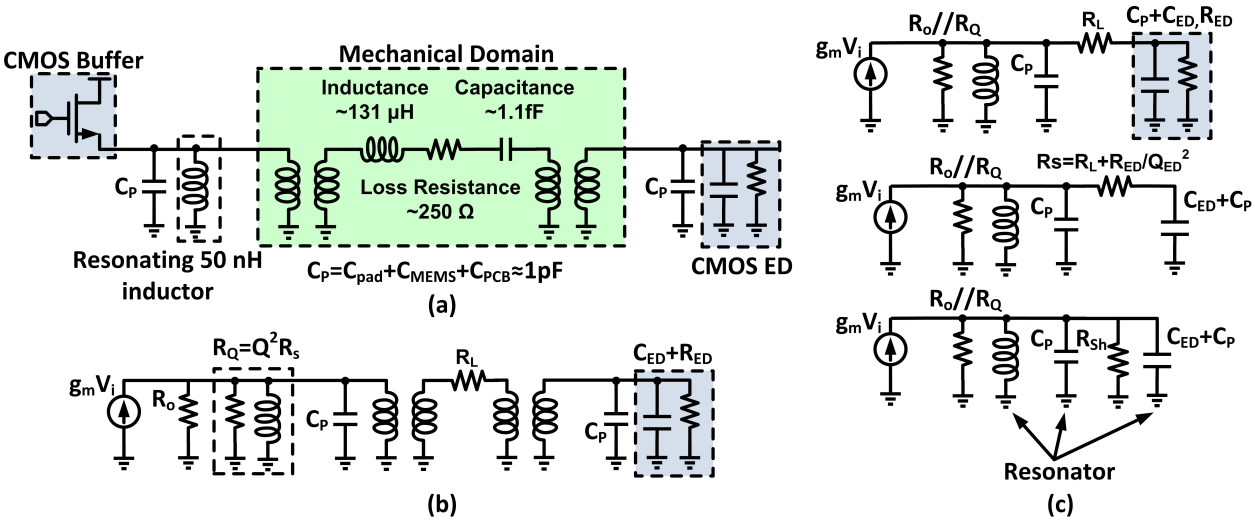

Figure 6.11: (a) Model of the MEMS filter-RF CMOS interface, including the output inductor and Rogers PCB. (b) A circuit-level model of the output interface at the resonant frequency of the MEMS filter. The ED is modeled as a shunt RC circuit, and the driving amplifier is modeled with a voltage-controlled current source. (c) Finally, the analysis method used to estimate the response of (b), where series-to-parallel transforms are used to simplify the circuit.

bonds is seen to be negligible. Figure 6.11b models this circuit at the resonant frequency of the MEMS filter, allowing a simple model to be formed. The RF buffer stage can be replaced by its Norton equivalent generator, which is defined by its transconductance and output impedance. The motional resistance of the MEMS filter is modeled as R_L and is directly related to the Q-factor of the MEMS filter. The finite Q-factor of the output resonating inductor is lumped into a shunt resistance R_Q, and the MEMS series resonator has been canceled out, presenting a low impedance at resonance. To simplify this network, series-parallel transformations (Figure 6.11c) can be used. Assuming that the Q-factor of the output capacitance from the ED capacitance C_{ED} and C_{PO} is of a sufficiently high Q-factor ($Q > 5$) leads to the model shown in Figure 6.11c. This is a good assumption for reasonable values of detector input impedance ($R_{ED} > 10k\Omega$) and parasitic capacitance ($C_{ED} + C_{PO} < 1pF$). Analyzing this model under the assumptions above leads to a voltage

at the output of the amplifier of

$$V_{o\ Amp} = g_{m\ CD}(R_o//R_Q//R_{SH}), \tag{6.22}$$

with

$$R_{Sh} = \frac{R_L + R_{ED}/Q_{ED}^2}{(R_L + R_{ED}/Q_{ED}^2)(\omega C_{ED} + C_{PO})^2}, \tag{6.23}$$

where $Q_{ED} = \omega R_{ED}(C_P C_{ED})$, omega is the operating frequency, and the other parameters are the same as those in Figure 6.11. Once this voltage is known, the voltage delivered to the load can be found through AC voltage division (equation (6.24)) between the loss resistance of the MEMS R_L and the load presented by R_{ED}, C_{ED}, and C_P.

$$V_{ED} = V_{o\ Amp}\frac{\sqrt{(R_{ED}/Q_{ED}^2)^2 + (1/(\omega C_{ED} + C_{PO}))^2}}{\sqrt{(R_L + R_{ED}/Q_{ED}^2)^2 + (1/(\omega C_{ED} + C_{PO})}}. \tag{6.24}$$

For reasonable values of R_S, R_{ED}, C_{ED}, and C_{PO}, the AC voltage division in (6.24) approaches unity, indicating that (6.22) is sufficient for estimating the interface loss. This analysis provides design intuition behind the impacts of the decreased MEMS filter Q-factor (increased R_L) and parasitic capacitance at the output node. A comparison between the simulated and modeled (equations (6.22) and (6.24)) insertion loss across varying C_P and R_L is shown in Figure 6.12. For small R_L, the parasitic capacitance has a negligible impact on the filter insertion loss. For low parasitic capacitance levels, the filter loss resistance R_L also has a very weak impact on the overall insertion loss on the filter, as it is in series with the high impedance of the ED. Unfortunately, when both C_P and R_L are relatively high, both factor into the insertion loss of the filter. An important conclusion from this analysis is that while the MEMS filter Q-factor (R_L) is critical in reducing interface loss, the parasitic capacitance at the output of the MEMS filter also plays a significant role.

A primary limitation of this output design is inductive coupling from the input matching network to the output interface. The simulation shows that low levels of inductive coupling between the output and input can lead to front-end instability. The initial output buffer design presents an impedance match between the amplifier and detector. A better design methodology is maximizing power (voltage) delivered to the load for a given buffer bias current. The difference between the

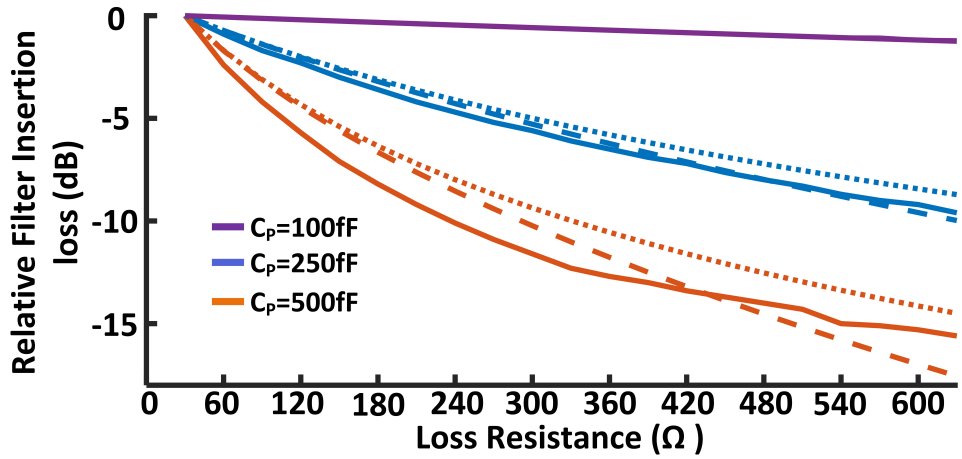

Figure 6.12: Comparison between the model shown in equation (6.22) (dotted line), the model shown in 6.24, and the simulation of the output interface of CMOS chip. Strong agreement is seen between the models ($< 2dB$), demonstrating the significance of both the parasitic capacitance at the interface as well as the Q-factor of the MEMS filter (R_L). A major conclusion from this modeling is that parasitic capacitance is as major of a contributor to insertion loss as the MEMS Q-factor is, indicating that both need to be considered in the design. The parameters used in the models are extracted from the DC operating point and are as follows: $g_{m\ Amp} = 117\mu S$, $R_o = R_Q = 7k\Omega$, $R_{ED} = 10k\Omega$, and $C_{ED} = 100fF$, with the unloaded insertion loss of the buffer found to be $-5.6dB$.

classical power- matching technique and the proposed technique lies in the assumption about the signal source (buffer amplifier). Different buffer topologies present different source impedances as well as different powers available from the source.

To create an impedance matched output, a common drain output buffer was chosen for use in the initial design. Switching to a high output impedance common-source stage provides higher signal levels to the ED despite a degraded power match. While the common-source amplifier requires prohibitively high bias currents to present a power match, the unmatched common-source stage can provide higher signal levels to the ED than the impedance-matched common drain stage.

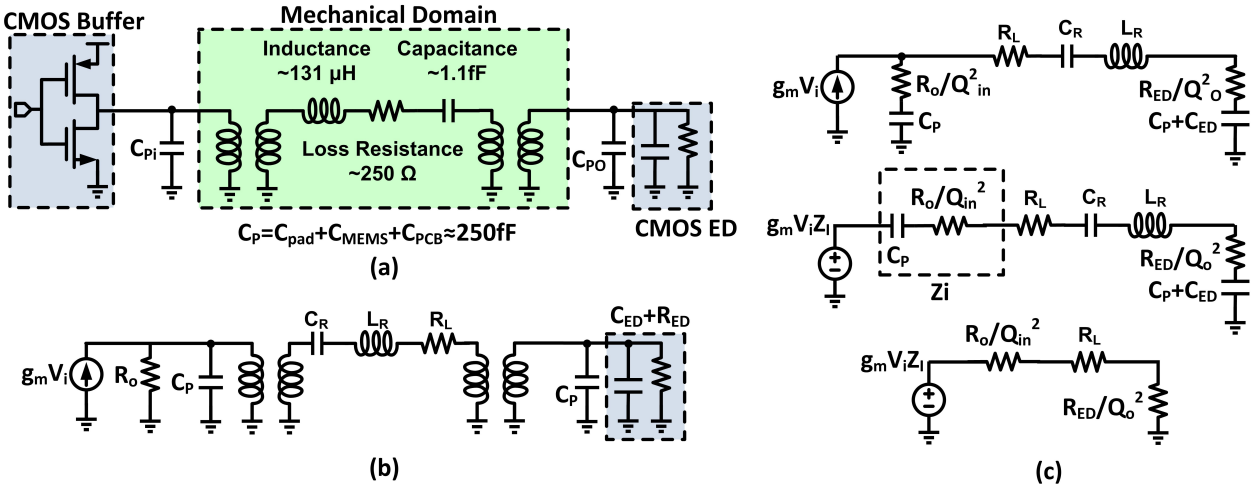

Figure 6.13: (a) Model of the MEMS filter-RF CMOS interface. (b) A circuit-level model of the output interface at the resonant frequency of the filter modeling the ED as a shunt RC circuit and the driving amplifier with a voltage-controlled current source. (c) Finally, the analysis method used to estimate the response of (b), where series-to-parallel transforms and a Thevenin transform are used to simplify the circuit.

6.6.2 Inductor-free output stage design

The second-generation Samplifier used an inductor-free output buffer design. This design choice removed to the inductive coupling issues and required fewer external components. In the previous design, the inductor was utilized to form the DC return path for the common drain output stage. Replacing the common drain output stage with a current-reuse common-source amplifier not only improves power efficiency but also naturally includes a current-return path through the second amplifying device. While it would seem that forgoing the use of an inductor to resonate out the parasitic capacitance would degrade the front-end gain, the inductance of the MEMS filter absorbs the parasitic capacitance. Furthermore, as there is no need for additional external components directly die to die, bonding can be used in the output stage.

Direct modeling of this interface is shown in Figure 6.13a. A similar analysis method to the one

used in 6.11 exists for this output configuration. Utilizing series-to-parallel transformations on the source impedance presented by the amplifier output impedances R_o and C_P as well as the load impedance presented by R_{ED} and $C_P + C_{ED}$, along with a Thevenin transformation on the source, leads to the second network in 6.13c. The inductance absorbs the series capacitances C_P and $C_P + C_{ED}$ and shifts the resonant frequency of the MEMS resonator by

$$f_c = \frac{1}{2\pi\sqrt{L_R C_{eq}}}, \tag{6.25}$$

where

$$C_{eq} = \frac{C_P C_R (C_P + C_{ED})}{C_P C_R + C_R(C_P + C_{ED}) + C_P(C_P + C_{ED})}. \tag{6.26}$$

An estimate of the resonant frequency shift can be found from the motional capacitance of $1.05fF$, which is measured from the filter samples and the motional inductance of $130nH$, along with the estimated parasitic capacitance of $250fF$ in parallel with the ED input capacitance of $100fF$. An estimate of the unloaded resonator frequency is $429.9MHz$, whereas, under the loading shown in Figure 6.13c,) this frequency shifts to $430.35MHz$ or roughly 0.3%. If this small shift in center frequency is accounted for in the filter and circuit design, this shift does not present a significant issue in performance.

Estimating the voltage delivered to the load can be performed using the third model in Figure 6.13 with

$$V_{Rect} = V_{th} \frac{R_{ED}/Q_{ED}^2}{R_{ED}/Q_{ED}^2 + R_L + R_o/Q_{in}^2}, \tag{6.27}$$

and

$$V_{th} = V_i g_m \sqrt{(R_o/Q_{in}^2)^2 + (1/\omega C_P)^2}, \tag{6.28}$$

where Q_{in} is the Q-factor of the RC parallel circuit formed from the amplifier output resistance, C_P, Q_{ED} is the Q-factor of the ED impedance, and V_{th} is the Thevenin equivalent voltage of the RF amplifier loaded by its output impedance and the capacitor C_P.

These results confirm that the inductor-free design combined with a high-power-gain current-reuse common-source amplifier produces an efficient interface. A comparison between the two interface design techniques illustrates the superior performance of the inductor- free current-reuse common-source amplifier in terms of insertion loss and bandwidth. In the first Samplifier, the output interface showed an 6.5 dB insertion loss and a 3dB bandwidth of 1.2 MHz, while the second Samplifier interface showed a power gain of 1.3 dB and a 3dB bandwidth of 1.1 MHz when assuming a fixed parasitic capacitance of 250fF. Comparing current-reuse buffers with and without an external inductor showed a 1 dB improvement in gain when using the inductor. Given that the performance improvement gained from using the output inductor is small, and the potential instability issues which arise from inductive coupling, a direct interface was chosen.

6.7 RF envelope detector design

The final design decision in the RF front-end design is the choice of RF ED. The RF ED is used to convert the RF signal to baseband/IF frequencies. Due to the high sensitivity targeted as well as the limited availability of RF gain, the RF ED is designed to work within the square-law regime. A back-of-the envelope calculation for the gain required to drive the ED into the linear regime shows that over 90 dB of RF gain is needed for a -110dB input signal. Not only is this gain challenging to realize in CMOS, but it would severely limit the linearity of the front end and does not present a practical option for ultra-low- power applications.

Chapter 2 presented a detailed analysis of ED circuits, including accurate and scalable models for the responsivity, input impedance, and output noise levels. The same metrics that were involved in the design of the ED-first receivers apply to the TRF front-end receivers and include primarily response speed, OCVS, detector NEP, and input impedance. The Samplifier requires much faster response speeds due to the bit-level, duty-cycled nature of the front end. For this reason, a high-impedance detector with many stages, such as the detector used in Chapter 3, is impractical. Similar to the case for the ED- first receiver, a significant design decision is the choice of which

ED architecture is appropriate.

The two types of detectors, as mentioned in Chapter 2, are the passive and active detectors shown in Figure 6.15. Equation 2.39 from Chapter 2 allows for a direct comparison between the two topologies. In particular, this equation compares the sensitivity of a passive ED with that of an active ED. It also reveals the bias current of the active ED at which the two detectors output noise levels normalize to their OCVS are equivalent. Choosing a value for the source impedance presented by the RF buffer and MEMS filter of roughly $5k\Omega$ from the simulations in the previous section and a sub-threshold slope of 1.45 extracted from the process equation (2.39) leads to an expected active ED bias current of about $20\mu A$. This inflection bias point at which the noise performance of the two detectors is similar is confirmed through simulation of both a passive TMD ED and a common-source active detector.

While a required active detector bias current of $20\mu A$ would increase the system RFFE bias current considerably (25%), it would not dominate front-end power. Considering the 1/f noise contribution reveals the primary issues with adopting this architecture, namely, input capacitance and flicker noise. For a low-threshold NFET detector with an input device sized at $10\mu m\ X\ 100\mu m$ biased at $20\mu A$, a 1/f corner of 1kHz is observed. The impedance loading for an active device of this size would be considerable, presenting roughly seven pF of input capacitance as well as a $2k\Omega$ shunt resistance. A similar design with the input device sized at $5\mu m\ X\ 50\mu m$ shows 1.2pF and $5k\Omega$ with a 3kHz corner frequency. Further shrinking the design to a $2\mu m\ X\ 20\mu m$ device produces a 1/f corner frequency of 21kHz with an input capacitance of 400 fF and a shunt resistance of roughly $10k\Omega$.

Utilizing a two-tone down-conversion mitigates the issues with input impedance and flicker noise [49], as the second frequency is higher than the 1/f noise corner. Unfortunately, this method has a fundamental 3dB SNR hit over single-tone modulation and requires a more complicated transmitter. For both the power savings as well as the flicker noise and input impedance performance, a ten-stage pseudo-differential triode mode Dickson detector is used in both Samplifier designs. The envelope detector exhibits a voltage domain OCVS of $100V/V$ and a tunable input impedance

from $5k\Omega$ to $50k\Omega$ at a very low input capacitance of 100fF.

6.8 Simulation and measurement results

Both systems have been extensively simulated to characterize their expected performances regarding power consumption, sensitivity, and interference rejection. Due to the very high impedance nature of the RF signal path, direct measurements for many sub-systems are challenging. The systems have been characterized, where possible, with direct measurements, which have been supplemented by simulation results. For brevity, the performance of the second Samplifier front end is shown via both simulation and measurement results. The second front-end design utilizes the experience and intuition gained from the first design in order to obtain a better performance in terms of the primary performance metrics.

6.8.1 Front-end sensitivity and gain

The significance of the front-end RF gain highlighted in Sections 6.1 and 6.2 helps determine the overall sensitivity of the receiver. Due to the very high impedance nature of the output interface, accurate measurement is difficult. Direct measurement of the RF gain is possible through measuring the ED output voltage. Figure 6.16 shows the simulated RF gain from the input to the CMOS chip to the input of the MEMS filter across varying amplifier stages. At 430MHz, the RF chain amplifier efficiency (6.17) is found to be roughly $1.2M$. This performance is achieved thanks to the combination of moderate inversion biasing and the ultra-low-power RF regenerative ring amplifiers. The band-pass nature of the ring amplifier shows rejection at lower frequencies presenting a Q-factor of roughly 5. Simulating an amplifier gain at 430MHz shows roughly a 3.3dB gain variation across a -30 to 30 degree Celsius range, indicating robustness to temperature variation in terms of the front-end performance. The phase margin is simulated across this same temperature range and is shown to be less than 1 degree.

Figure 6.17 shows the gain from the RF input, which includes the effects of input impedance matching showing a total efficiency of roughly $1.8M$. The efficiency is boosted by the passive voltage gain obtained via the input impedance matching. This input match demonstrates an input Q-factor of roughly 40 and a bandwidth of 10 MHz. Including the full RF amplifier chain into the ED is shown in Figure 6.18, where the RF gain is shown to be 68dB and an improved front-end bandwidth is reduced from 10MHz to 550kHz. This tight RF output bandwidth reduces the impact of out-of-band interference and RF noise self-mixing effect. Overall the Q-factor increases from 5, which only considers the CMOS circuit, to 40 when combining the passive impedance matching and then increases to roughly 650 when taking into account the output MEMS filter.

Measurement of RF gain using an assumed detector OCVS of $100V/V$ is accomplished by viewing the output signal from the ED. The RFFE gain was measured at nominal bias currents and recorded as: 43 dB for the standalone CMOS, 63dB for the CMOS and input matching, and 64.5dB for the complete RF front-end gain. The characterization of RF gain across frequency is shown in Figure 6.19, which shows a narrower input RF bandwidth than the simulated 550kHz, likely due to the increased resonator Q-factor.

6.8.2 Front-end linearity

Front-end linearity is simulated through B1dB and B3dB are measures of front-end compression points for a given blocker power. The interference rejection of any receiver does not depend solely on the RF front end but also depends on the digital and baseband circuits. The blocker compression points indicate the failure point of the RF front-end, after which point the system is desensitized, even for an ideal baseband. The simulation of blocker 1dB compression is shown in Figure 6.20 across varying blocker offset frequencies, indicating the linearity of the front end in the presence of blocking signals. These results suggest the front end can tolerate an in-band interfering signal of -75dBm, which, for an ideal baseband, corresponds to an interference rejection of 33dBm. The measured B1dB and B3dB corresponded to -79dBm and -74dBm, respectively, showing strong agreement with the simulation.

6.8.3 Active power consumption and startup time

The RF front-end startup time is characterized through both direct measurements and simulation, resulting in a simulated startup time of roughly $10\mu s$ produced via measurement and of less than $3\mu s$ produced via simulation. This discrepancy is likely due to additional capacitance in the bias lines as well as the slow slew rate of the observation buffers at the ED output. A measured power consumption of $34\mu W$ is similar to the simulated power consumption of $38\mu W$ but reduced compared to simulation for a given RF gain and ring amplifier center frequency. This discrepancy is likely due to reduced model accuracy in the moderate inversion region, which is difficult to model without EKV-based models (BSIM6) [72].

6.9 Conclusions

Careful design is required for optimizing the TRF front end beyond -100 dBm, but it is possible at bias currents of less than $100\mu A$. Optimization of both gain and power is possible through utilizing power-efficient RF gain cells and is necessary for obtaining the desired sensitivities and power levels. Finally, optimization of the output interface, as well as the noise bandwidth into the detector, is critical for obtaining the desired sensitivities.

This work opens the door for sub-microwatt RF front ends, which can run for years without battery power while obtaining similar sensitives to designs in the 100's of micro-watts regime.

6.10 Contributions

1. Noise analysis of TRF front ends showing optimization strategies for the design.
2. Design of the major blocks in the RF front end, including the LNA, gain stage buffer, output stage, and ED.

3. Developed high- impedance LNA design techniques and applied these to the Samplifier front end.

4. Developed a ring amplifier architecture and theory of operation for use in the Samplifier.

5. Explored the output buffer and MEMS interface design and optimized them in terms of power consumption.

6. Designed an ED for integration into the system.

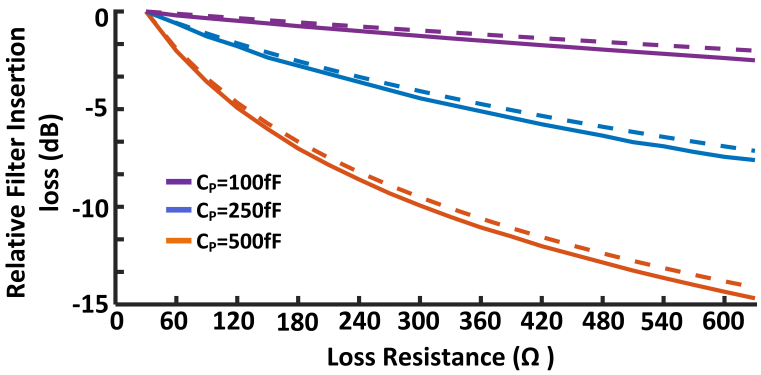

Figure 6.14: Comparison between the model shown in equation (6.27) (dotted line) and the simulation of the output interface of the CMOS chip shown in Figure 6.13. There is strong agreement between the model and simulation ($< 1dB$). This plot demonstrates the significance of both parasitic capacitance at the interface and the Q-factor of the MEMS filter (R_L). Similar to the interface presented in the previous section, both resistance and capacitance are significant in the overall insertion loss. These results show that the MEMS resonator can successfully absorb the parasitic capacitance, which, combined with a superior buffer design, enables lower insertion loss at iso-power compared to the design presented in the previous section. The parameters used in the models are extracted from the DC operating point and are as follows: $g_{m\ Amp} = 360\mu S$, $R_o = 10k\Omega$, $R_{ED} = 10k\Omega$, and $C_{ED} = 100fF$, with the unloaded insertion loss of the buffer found to be $-5.6dB$.

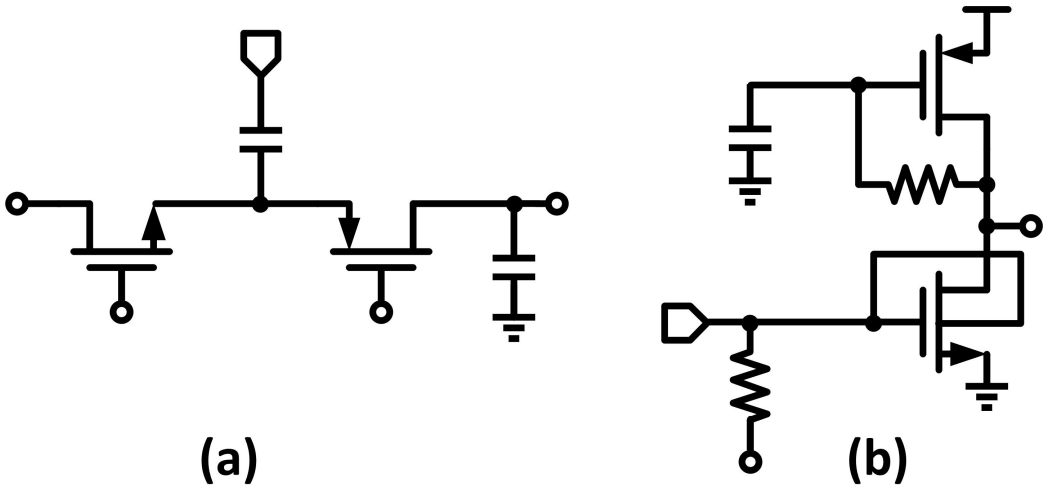

Figure 6.15: Two ULP ED design choices: (a) a passive ED exemplified by the Triode Mode Dickson detector, and (b) active detectors such as the self-biased common-source detector using a DTMOS connection for boosting OCVS, as shown in [4].

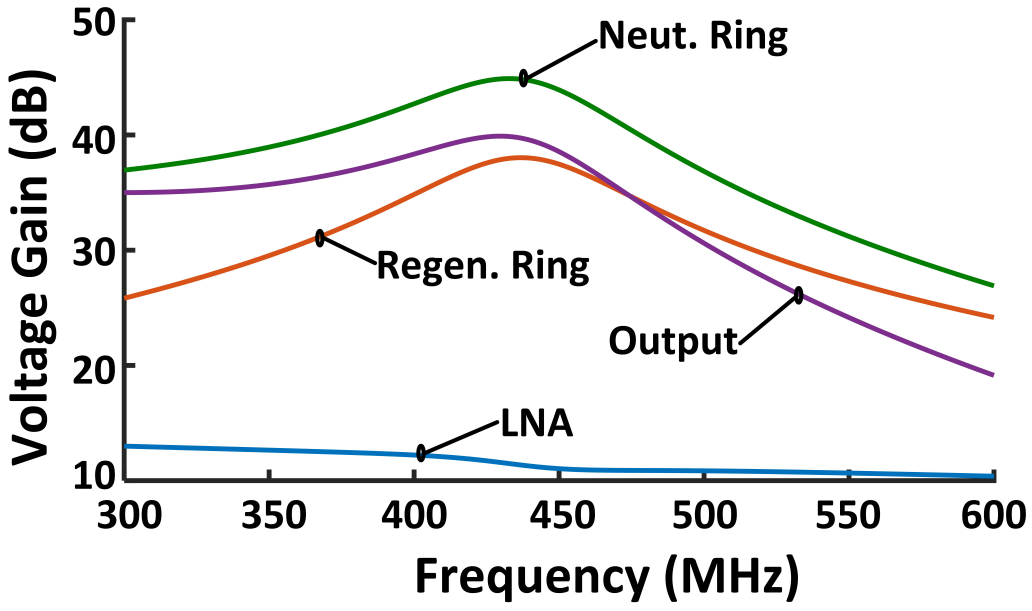

Figure 6.16: RF front-end gain, not including the MEMS filter or input impedance matching showing a 40dB gain at the center frequency of the ring amplifier.

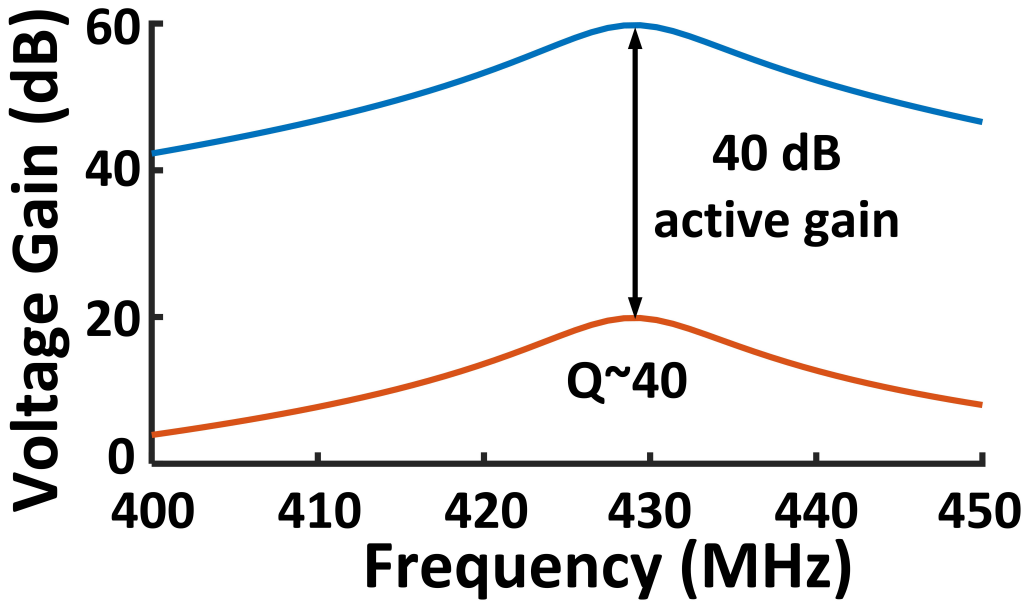

Figure 6.17: Simulated RFFE gain, including the effects of input matching boosting the gain from 40dB to 60dB and the Q-factor from 5 to 40.

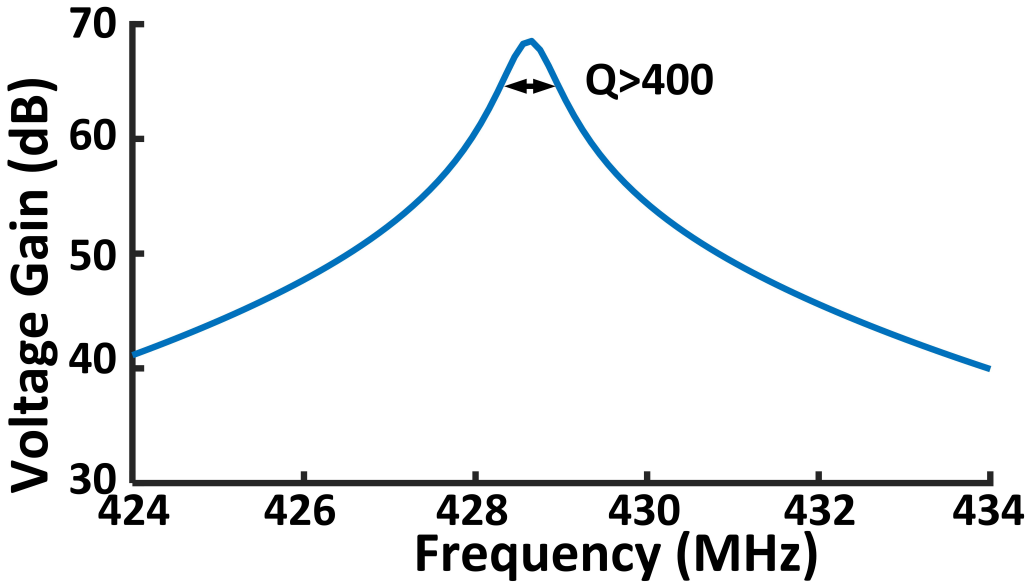

Figure 6.18: Simulated gain with the MEMS filter, showing a Q-factor of 650 and a gain of 68 dB.

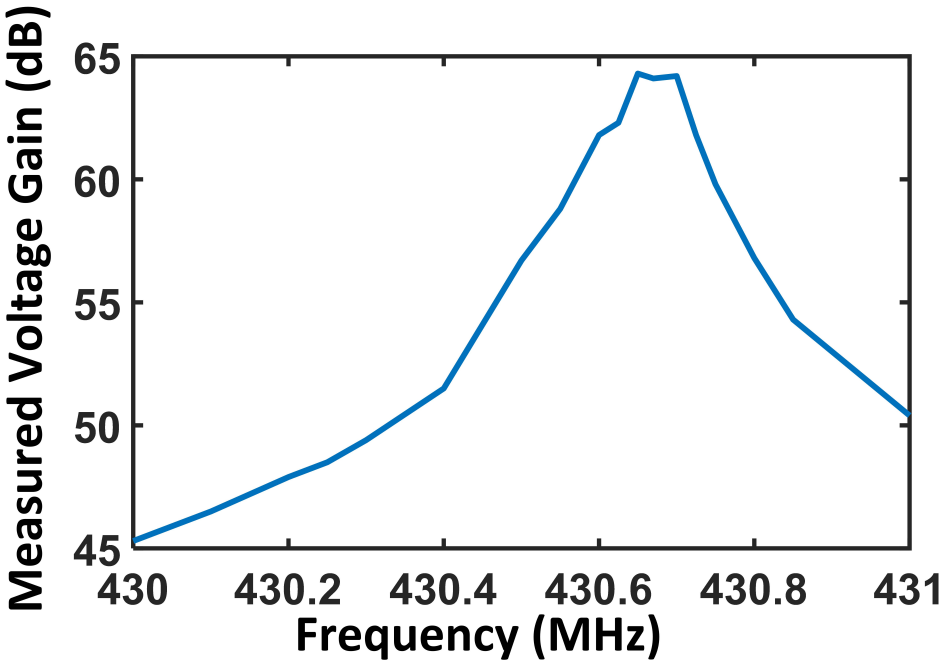

Figure 6.19: Measurement of RF front-end gain out of the envelope detector circuit showing a high Q-factor and very high RF gain of 64.5 dB.

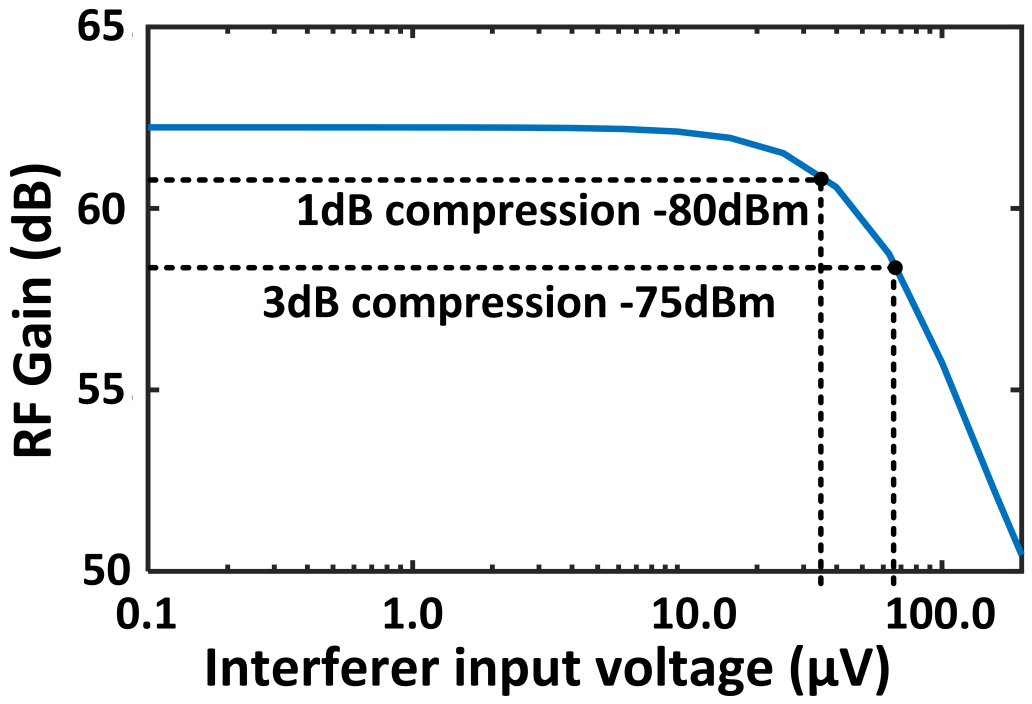

Figure 6.20: Simulation of a blocker 1dB compression point which indicates limitations in obtainable receiver CIR for in-band interference. The receiver can tolerate a -75dBm in-band interferer at 3dB degradation before the RFFE fails.

CHAPTER 7

OTHER WORK: PHOTONICALLY-DRIVEN RADIATORS

Optically-driven electromagnetic radiators combine mm-wave antennas with broadband and high-power photodetectors to produce high-power free-space RF signals. There is an increasing need for robust, high-RF-power mm-wave sources for applications, including high-throughput communications, medical imaging, and defense applications. In these applications, photodiode-driven radiators offer several attractive advantages over purely electronic sources such as inherently wide-band operation, high-output power levels, and decreased losses associated with feed networks in large-scale phased arrays.

Microwave photonic radiators employ two lasers offset in a wavelength in such a manner that the lasers are coupled into a photodetector, producing a beat frequency proportional to the difference in wavelengths and then coupled into free space through an antenna [80], as shown in Figure 7.1. Optimization of the coupling between the antenna and photodetector is critical for efficient radiation; additionally, thermal and mechanical considerations are essential design factors.

Presenting a strong impedance match between the photodiode and antenna is essential for high-powered operation. Parasitic substrate modes can distort the radiation pattern and reduce the efficiency of the antenna and must be suppressed through careful design. The coupling between the antenna and photodetector was optimized while pursuing a robust and inexpensive mm-wave radiator design without the use of an external silicon lens or complicated antenna fabrication techniques.

This chapter presents an integrated photonically-driven radiator operating between 95 and 110 GHz

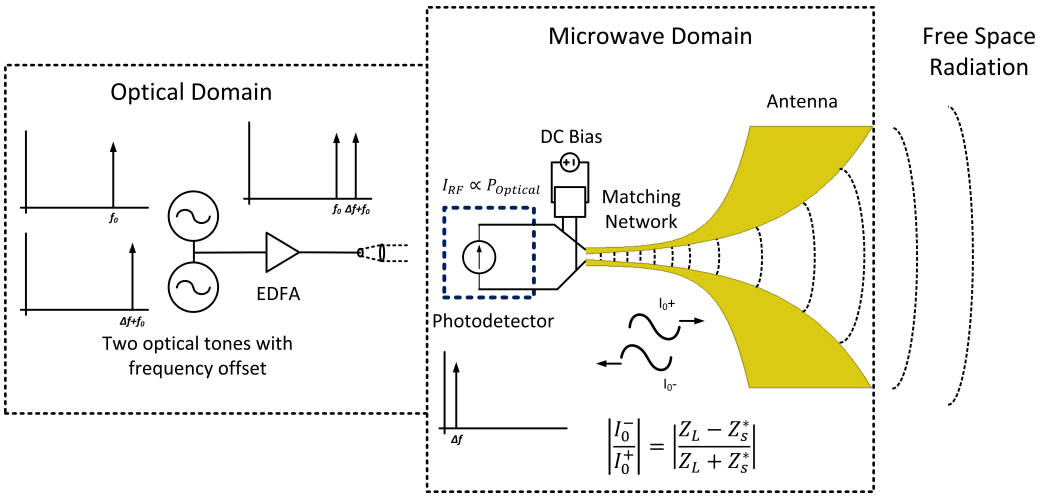

Figure 7.1: A schematic diagram demonstrating a system used for the generation of mm-wave radiation via optical heterodyning. Two laser signals are coupled in the photodetector, which extracts the output signal in the current domain and drives the mm-wave antenna.

and demonstrating an -1.5dBm EIRP (effective isotropic radiated power) and wide-band operation, whose photodiode operation was shown in [81]. A sandwiched Vivaldi was integrated with a high-power flip-chip bonded MUTC photodetector to create a robust compact and integrated mm-wave radiator (Figure 7.2). Previously demonstrated works produced EIRP levels of up to -2.4dBm though the use of silicon lenses or 3D horn antennas [82]. This work lead to the publications [**?**], [83], and [84]

7.0.1 Antenna design

A Vivaldi antenna was chosen due to its high gain, wide bandwidth, and end-fire beam, which is amendable to the implementation of compact large antenna arrays. The Vivaldi antenna is an exponentially tapered slot-line, in which the opening width typically determines the lowest operating frequency of the antenna. The antenna is fabricated on top of a 10mil thick AIN substrate to enhance its thermal conductivity, thus enabling optimal output power from the photodetector by

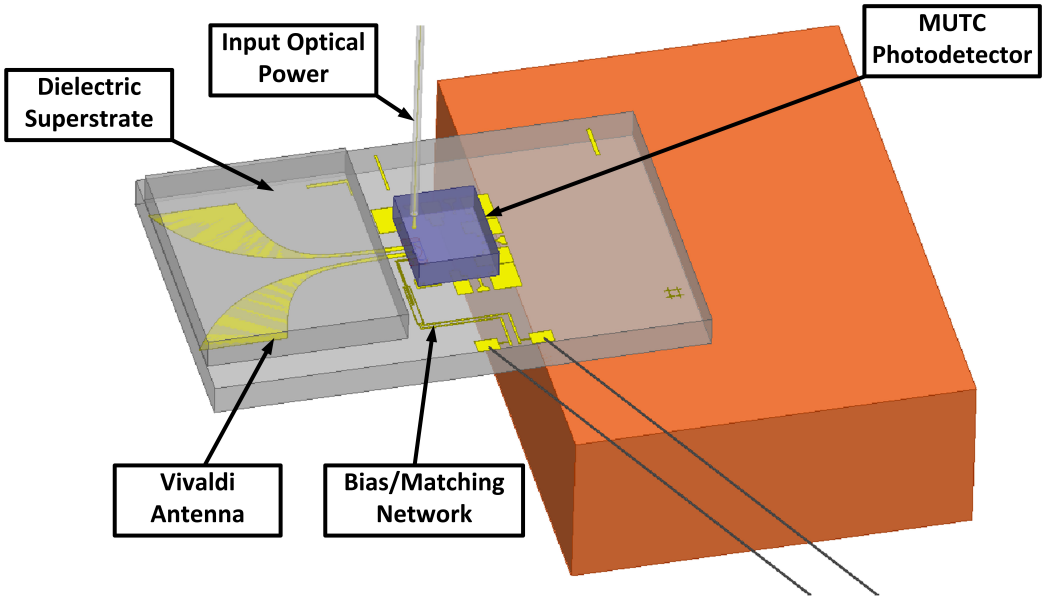

Figure 7.2: Diagram detailing the proposed antenna system showing the major components, including the photodiode, antenna, and dielectric superstrate.

mitigating thermal effects. The low conductivity of undoped AIN also provides small dielectric losses associated with coupling-to-substrate modes.

Tapered slot-line antennas on dielectric substrates can couple power into dielectric substrate modes, reducing their effective efficiency. For a low-loss substrate such as undoped AlN, this loss is generated from stray beams formed when the dielectric thickness is larger than

$$(\sqrt{\epsilon_r} - 1)d/\lambda_0 < .03, \tag{7.1}$$

where epsilon is the dielectric constant of the medium, d is the dielectric thickness, and lambda is the free-space wavelength [85].

Various methods are employed in the literature for reducing the coupling of power into the substrate modes at these frequencies, such as the use of a dielectric lens, which is a bulky and expensive option [86]. Another method particular to tapered slot antennas is fabricating the antennas on thin dielectric membranes. However, designs on such thin substrates may present mechanical

stability issues as well as complicated manufacturing requirements. Another substrate mode suppression technique involves removing the dielectric in the slot region, which requires an etch into the dielectric of $> 50\mu m$ for operation at 110 GHz [86].

A cheaper and simpler solution in the form of a dielectric superstrate cut from the same wafer that the antennas were fabricated from was placed on top of the radiator, creating a sandwiched design [87]. The dielectric sandwiching technique creates a more symmetric environment for the antenna and thus improves the radiation pattern through the suppression of substrate modes, as shown in Fig. 2. This dielectric superstrate technique resulted in a limited bandwidth compared with a free- space Vivaldi but enabled efficient operation in the pass-band in the desired radiation direction. A detailed diagram showing the significant design variables for the Vivaldi antenna with dielectric superstrate is shown in Figure 7.3.

7.0.2 Antenna PD integration and simulation results

Optimum radiator design requires careful co-design between the antenna and the photodiode, with a particular focus on the interface impedances. The DC bias of the PDs must be considered during the design of the antenna to ensure that proper impedance matching is maintained at mm-wave frequencies. Two approaches were investigated: the first approach applied the bias along the edge of the antenna arms where most of the power had already radiated from the antenna, minimizing the effect of any impedance placed by the bias network at that node. The second approach utilized a quarter-wave open circuit, followed by a length of transmission line, whose inductance resonates the parasitic capacitance of the PD. The second biasing approach had the advantage of simultaneously producing isolation from unknown impedances at the DC biasing points as well as improving the match between the photodetector and antenna. Due to the improved match when utilizing smaller devices, the quarter wavelength transmission line biasing method was used in the final design.

The PD is modeled as a current source in parallel with a capacitance C_j and a series resistance Rs and inductance Ls that determine the optimal impedance match for the antenna [88]. The Vivaldi

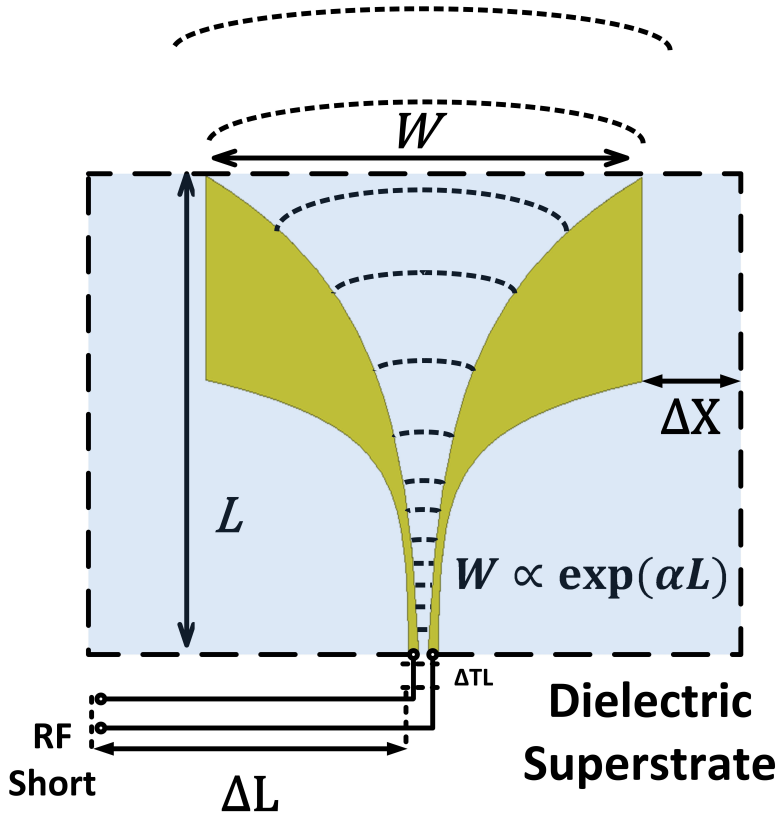

Figure 7.3: Vivaldi antenna design showing major design parameters and relative locations of the bias network and superstrate.

antenna is designed for maximum EIRP, which requires good matching between the PD and the antenna as well as high antenna efficiency. The antenna was initially designed for integration with a 5um- diameter PD with a predicted input capacitance of $10fF$. Designing for the small capacitance of the $5\mu m$ PD resulted in a real input impedance of the antenna of around 80 in the band of interest. A shunt inductor matching network integrated into the DC feed network was designed to resonate out C_j, as shown in Figure 7.4.

The effect of this matching network rotates the load impedance seen by the PD along a constant real admittance contour of the Smith chart closer to a conjugate match. However, 14um diameter PDs with input capacitances of $70fF$ have been used in these preliminary measurements due to

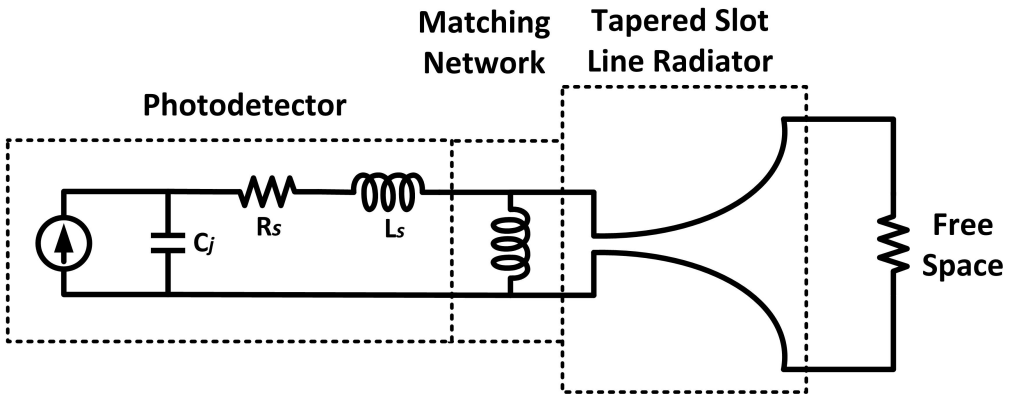

Figure 7.4: A lumped-element model of the Vivaldi antenna photodiode interfaces, where the DC bias path is used as an inductor to partially resonate out the parasitic capacitance of the photodiode.

availability, reducing the achievable EIRP, as expected. Figure 7.5 shows the simulated frequency performance of the PD-antenna system for various PD dimension capacitances.

The simulated antenna input impedance is fit to a 80Ω resistance in parallel with a 130pH inductance, which is in agreement with the theoretical model and antenna test structure measurement results and shown in Figure 7.6.

The simulated radiation pattern of the designed antenna is plotted in Figure 7.7, showing that the radiation bandwidth was around 10 GHz with a simulated gain of $7dBi$, where the parasitic coupling into substrate modes from the antenna is the primary limitation on the bandwidth. With a photocurrent of $20mA$, the simulated delivered power to the antenna was -3dBm, which, combined with a simulated gain of the antenna, yields a simulated EIRP of 4 dBm.

7.0.3 Measurement results

The photodetector and antenna are characterized independently to predict the performance theoretically. The integrated system is measured directly to compared with the estimation from the block-level measurement. The integrated system is shown in the substrate and board-level photos

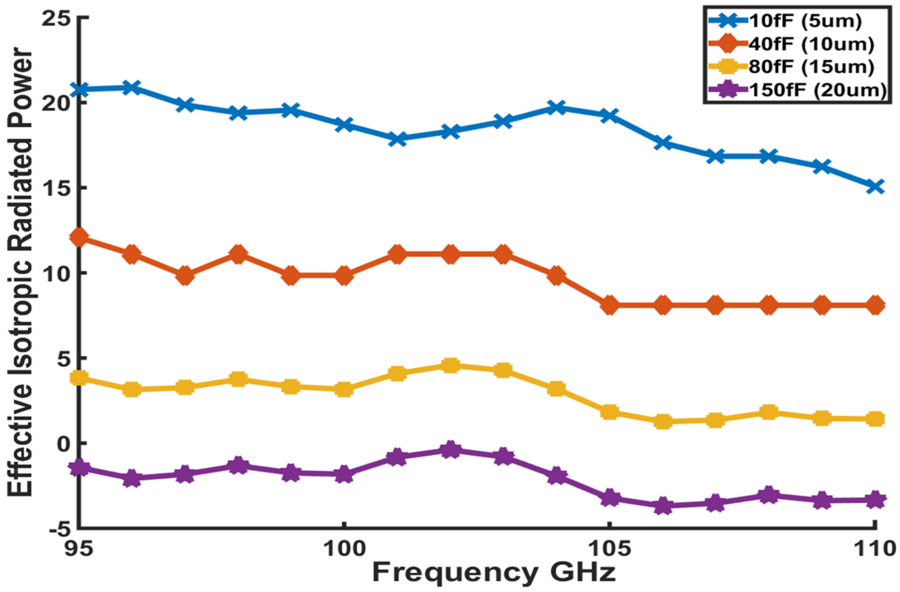

Figure 7.5: Simulation results of the EIRP of the integrated photodiode antenna combination showing dependence upon photodiode size. Increasing the diode dimensions leads to reduced radiated power.

in Figure 7.8. Similar PDs have been shown to provide 9.6 dBm of output power at 100 GHz with 49 mA photocurrent utilizing inductive peaking into a 50 termination [88].

The antenna and biasing network test structures are measured independently with a Keysight PNA Network Analyzer and OML frequency extenders operating up to 110 GHz. The antenna is measured through direct-wafer probing with MPI Titan RF probes and a 23dB gain horn antenna, and a down-conversion mixer was placed in the far-field of the radiator, as shown in Fig. 9. The equivalent models of the matching network and antenna are verified through measurements of the probed measurements from Figure 7.6.

The radiation pattern of the antenna is measured in the far-field using a horn antenna with a W-band mixer to down-convert the received signal from RF to a 2 GHz IF frequency. After down-conversion, the signal is measured with a Keysight PXA 9030A spectrum analyzer. The end-fire gain of the antenna was measured to be 7dBi and calculated from the received power, the

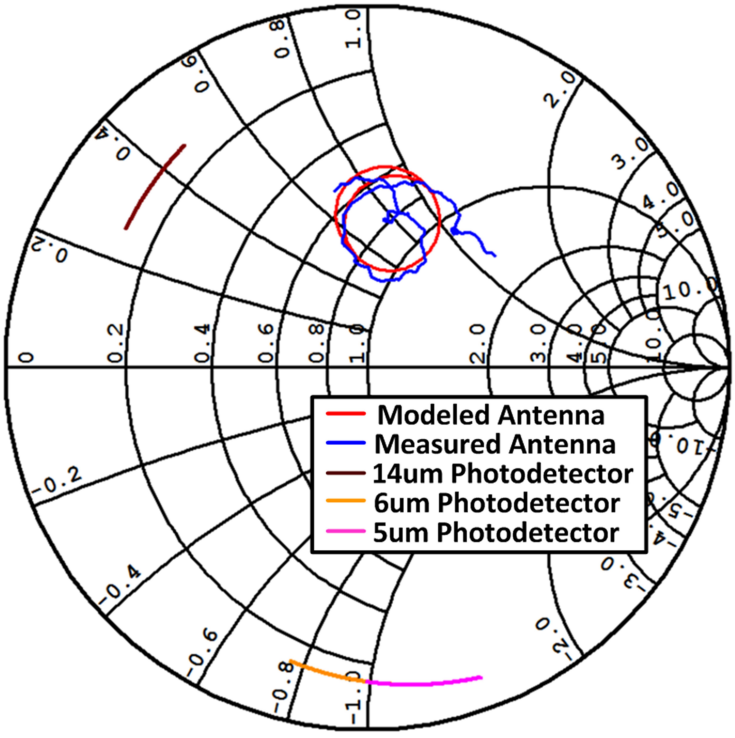

Figure 7.6: This figure presents a comparison between the measured and modeled antenna next to the estimated impedance of the photodiodes from various areas. This result indicates that the impedance match is optimized for smaller diode areas.

conversion loss of the mixer, and the Friss free-space propagation loss equation.

$$G_{T(dBi)} = P_{Meas.} - P_{Trans.} + PL_{(dB)} - G_{R(dBi)} + C.L._{(dB)}, \tag{7.2}$$

where P_{Meas} is the measured power of the spectrum analyzer, PL is the free-space path loss, G_T is the gain on the receive antenna, and CL is the conversion loss on the harmonic mixer.

The E-plane radiation pattern was measured by sweeping the angle of the receiving antenna with respect to the transmitting antenna while maintaining a constant distance (Figure 7.9).

Light from two distributed feedback lasers with constant frequency offset is combined into a single-mode fiber and amplified with an Erbium-doped fiber amplifier (EDFA) and attenuated with a vari-

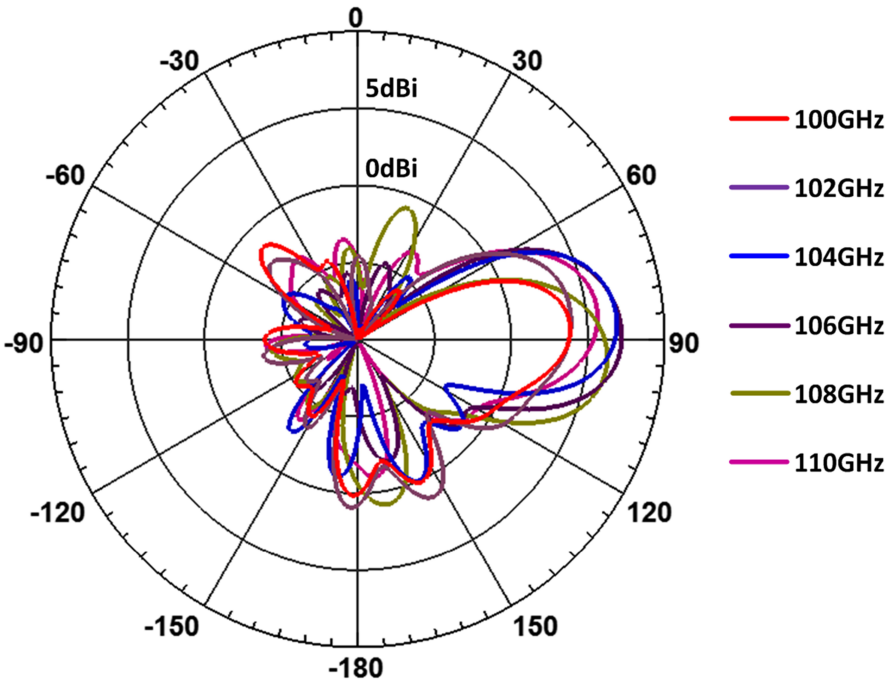

Figure 7.7: Simulation of antenna gain versus frequency when using the dielectric superstrate technique. Results show the beam radiating in the end-fire direction across 10GHz of bandwidth.

able optical attenuator (VOA) to illuminate the PD and is depicted in Figure 7.10. The radiated EM field is measured using the same receiver as the antenna characterization. The 6dB frequency bandwidth is measured as 14 GHz by sweeping the beat frequency between the two lasers and thus the frequency of the radiated RF signal, as shown in Figure 7.11. The measured maximum EIRP is -1.5dBm, where this output power is measured under a DC bias of -3V and an unsaturated photocurrent of 20mA. It is expected that higher output power can be achieved by driving the photodetector further into saturation. Between 100 and 110 GHz, the measured and simulated system performances differ by about 7dB. This discrepancy between measurement and simulation can be attributed to various non-idealities, including increased losses on the antenna, process variation in the photodetector, and increased parasitic capacitance in the interface between the photodetector and the antenna

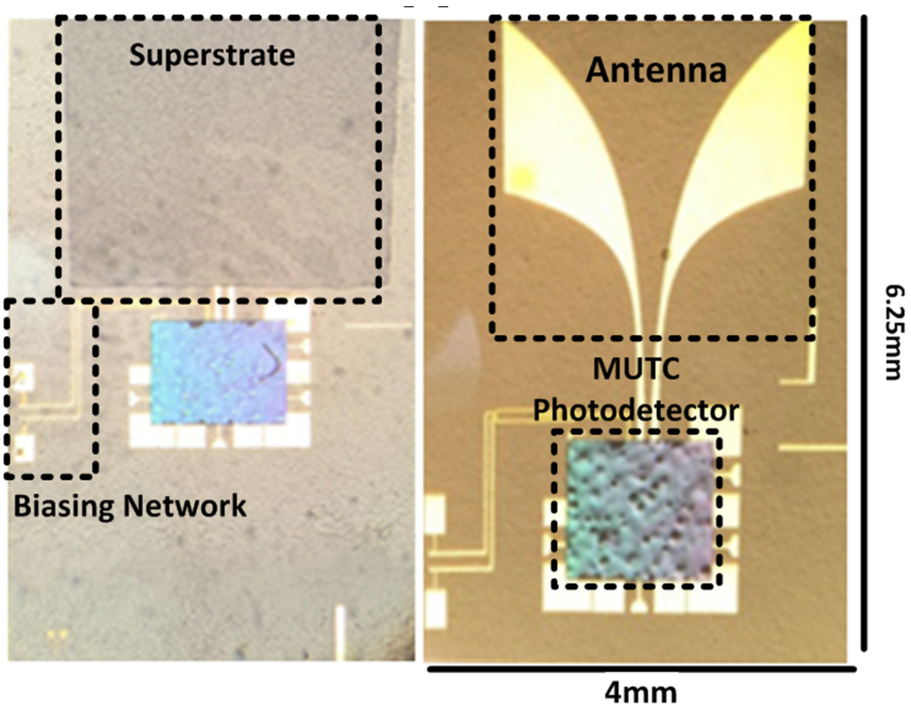

Figure 7.8: Die photo of the implemented antenna system showing it both with and without the dielectric superstrate on top of the Vivaldi antenna.

7.0.4 Conclusions

This work shows a mm-wave antenna integrated with a high-power MUTC photodiode for operation in the W-band, where parasitic substrate modes require careful antenna integration design without the use of complicated post-processing on the antenna. An EIRP of -1.5dBm unsaturated output power with 20mA of current is observed at 100 GHz. Higher output powers are anticipated through integration with a smaller PD with lower capacitance.

7.0.5 Contributions

- Led the development of the antenna design.
- Developed the techniques for substrate mode suppression in the antenna.

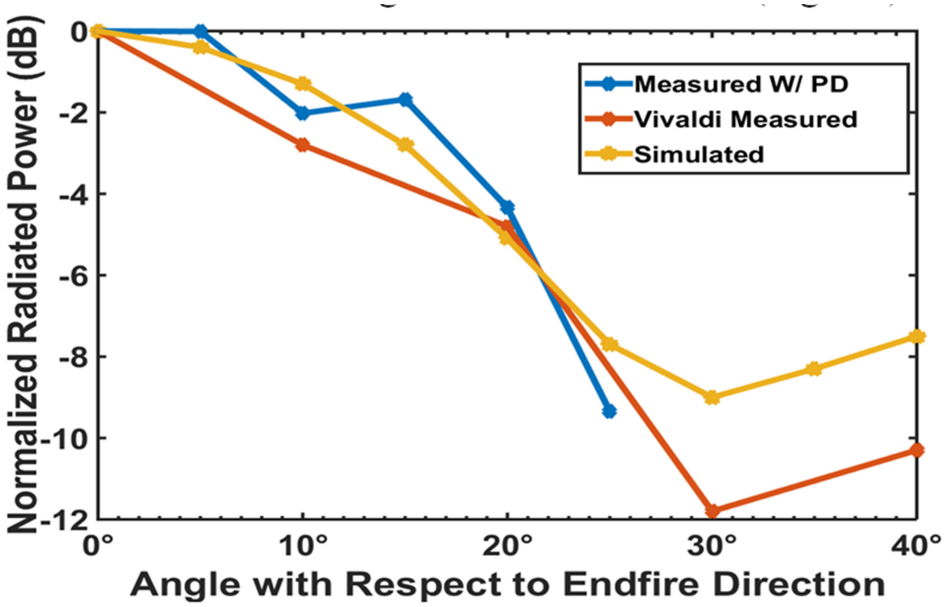

Figure 7.9: Measured antenna gain in the E-cut of the antenna plane showing strong agreement with the simulation.

- Co-led the integration between the photodiode and antenna.
- Co-led the measurement and characterization of the emitter.

This work was done in collaboration with Keye Sun and Qinglong Li.

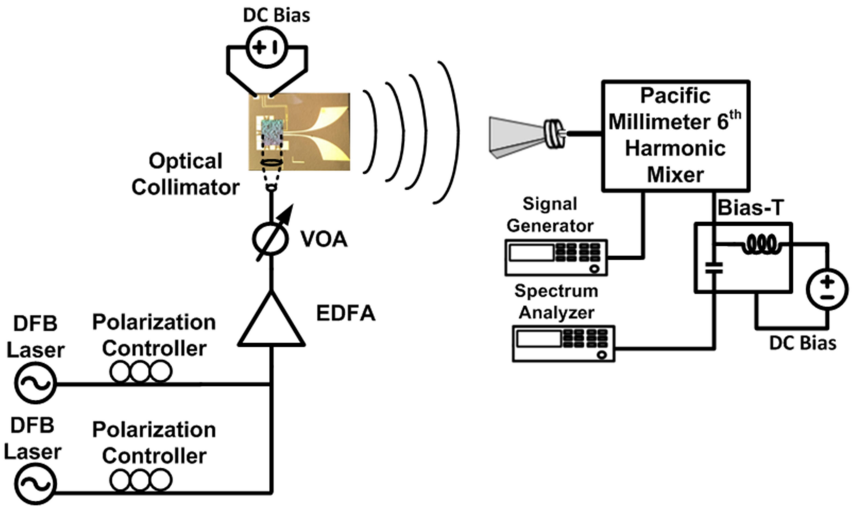

Figure 7.10: Measurement set-up for the RF photonic radiator using two DFB lasers coupled in an ED to drive the PD. The receiver is composed of a Pacific mm 6th harmonic mixer and spectrum analyzer signal generator combination.

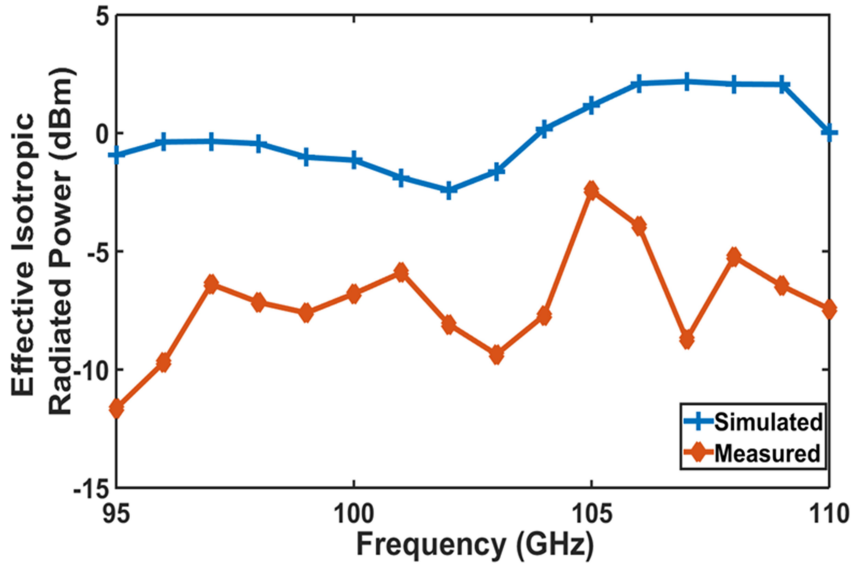

Figure 7.11: Measurement of the antenna photodiode EIRP across a wide frequency range. The discrepancy between simulation and measurement is likely due to additional interface capacitance between the antenna and photodiode.

CHAPTER 8

CONCLUSIONS AND FUTURE DIRECTIONS

This work has contributed to the development of near-zero power level wake-up receivers by helping to extend the state-of-the-art in sensitivity over 50dB. This massive sensitivity improvement required contributions from many aspects of the system design, ranging from ultra-low-power digital design and algorithms to nanowatt-power-level baseband and reference design and including the RF designs presented in this work. This work helps to bridge the application versus performance divide in sub-microwatt receivers. The development of accurate and scalable models for both the RF EDs and the noise mechanisms at play in the TRF receivers has laid a foundation for the design of more sensitive receivers. The insights developed with these analyses have both directly led to design improvements and new component topologies as well as helped reveal fundamental limitations of these receiver architectures. Through the adoption of the TRF receiver and the bit-level duty cycling technique, this work has contributed to the development of the Samplifier receiver. This highly adaptable architecture has demonstrated state-of-the=art performance combined with a high degree of flexibility.

While this work has dramatically extended the sensitivity of sub-microwatt receivers, more work is required to increase the interference robustness of these systems. As sub microwatt receivers are now more sensitive, their relative interference robustness must improve in order to take full advantage of these high sensitivities. This goal can be pursued through adaptions in the signaling techniques used, improving gain and offset correction algorithms, and developing more interference-robust designs.

8.1 Summary of contributions

8.1.1 Square-law envelope detector analysis and design.

1. Developed decoupled linear network models for modeling behavior of envelope detector circuits.

2. Applied decoupled linear network analysis to accurately model the detector sensitivity, output noise, input impedance, and transient response.

3. Developed the co-design methodology for the matching network, envelope detector, and baseband circuitry.

4. Developed the theory of comparing active and passive detectors, enabling robust comparisons between architectures.

5. Taped out test structures, verifying the modeling of the detectors.

8.1.2 Interference-robust detector in the first near-zero-power-level wake-up receivers.

1. Led system-level design identifying critical components and requirements for system operation.

2. Led baseband design and interfacing between the detector and baseband amplifier.

3. Designed the PCB and high- impedance interfacing to the envelope detector and worked with the ED designer to utilize the theory on optimal sensitivity and power consumption for an ED-first receiver.

4. Developed the high-level idea and flow chart for the automatic offset compensation used in this design.

5. Performed top-cell integration and floor planning for system-level integration.

6. Led the measurement and characterization of the receiver.

8.1.3 Detector architecture exploration - the triode mode Dickson

1. Discovered weaknesses inherent in the Dickson architecture and related these to the device impedance.

2. Developed the TMD ("Triode Mode Dickson") topology and verified the operating principle through simulation.

3. Developed the theory behind the operation and verified it analytically through simulation and measurement.

4. Compared the TMD to the Dickson and other passive envelope detector architectures to discover the detectors merits.

5. Taped out test structures and measured results, verifying the theory developed for the TMD detector.

8.1.4 Bit-level duty cycled TRF receiver design (Samplifier)

1. Co-developed the high-level conceptual idea behind the Samplifier architecture and proposed it as a solution to the SNR limitations found in the current state-of-the-art.

2. Developed the modeling techniques and designs which enabled the TRF architecture to make a greater than 20 dB jump in sensitivity over the current state-of-the-art designs.

3. Developed a system-level architecture including the use of principal components needed for successful demonstration.

4. Developed the theory behind the interference-related limitations associated with bit-level duty cycling and proposed a two-tone modulation to reduce these effects.

5. Contributed to the development of the AGOC architectures, explicitly helping to develop the analog block requirements and architecture for the system.

6. Led team of students working on sub-system design and oversaw the overall system architecture.

7. Developed the system architect and top-level integration for both generations of wake-up receivers.

8. PCB design and testing lead for the first Samplifier, as well as PCB design and testing assistant on the second.

8.1.5 Tuned front end receiver analysis and design for Samplifier wake-up receivers

1. Conducted the noise analysis of TRF front ends showing optimization strategies for the design.

2. Designed the major blocks in the RF front end, including the LNA, gain stage buffer, output stage, and envelope detector.

3. Developed high impedance LNA design techniques and applied these to the Samplifier front end.

4. Developed the ring amplifier architecture and its theory of operation for use in the Samplifier.

5. Explored output buffer and MEMS interface design and optimized them for power consumption.

6. Designed the envelope detector for integration into the system.

8.1.6 Other work: Photonically-driven radiators

- Led the development of the antenna design.
- Developed the techniques for substrate mode suppression in the antenna.
- Co-led the integration between the photodiode and antenna.
- Co-led the measurement and characterization of the emitter.

8.2 Future directions

Significant work not captured in this thesis is currently underway towards improvement in the robustness of sub-microwatt wake-up receivers. A third-generation Samplifier receiver has been taped out at UVa which promises to improve both interference robustness as well as temperature stability substantially. This work employs entirely integrated bias generation and should present very robust performance across temperature and process drift. Furthermore, this work employs more robust signaling techniques which promise to overcome the shortcomings of the two-tone demodulation. Finally, a substantial improvement in interference robustness is expected from a nanowatt-power-level detector-first "canary path" which detects the presence of RF interference and adjusts the gain to ensure linearity in the front end and baseband.

Further architectural explorations promise to reveal a path towards greater robustness but will require careful considerations in the frequency synthesizer. Overall, this work has opened a path to better designs in this space and can be used as a stepping stone for further exploration.

8.3 Publications

8.3.1 Accepted and Submitted Conference Publications

1. J. Moody, K. Sun, Q. Li, A. Beling, S. M. Bowers, “A Vivaldi antenna based W-band MUTC photodiode driven radiator, 2016 IEEE International Topical Meeting on Microwave Photonics (MWP), Long Beach, CA, 2016, pp. 217-220. [JM1]

2. K. Sun, J. Moody, Q. Li, S. M. Bowers, A. Beling, “High-power integrated photodiode-antenna emitter for 100GHz applications, OSA Integrated Photonics Research (IPR) Conference, July 2016. [JM2]

3. P. Bassirian, J. Moody, S. M. Bowers, “Analysis of quadratic Dickson based envelope detectors for IoE sensor node applications, 2017 IEEE MTT-S International Microwave Symposium (IMS), Honolulu, HI, 2017, pp. 1-4. [JM3]

4. P. Bassirian, J. Moody, S. M. Bowers, “Event-driven wake-up receivers: Applications and design challenges, 2017 IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS), Boston, MA, 2017, pp. 1-4. [JM4]

5. J. Moody, P. Bassirian, A. Roy, Y. Feng, S. Li, R. Costanzo, N. S. Barker, B. H. Calhoun, S. M. Bowers, “An 8.3 nW -72 dBm event driven IoE wake-up receiver, 2017 European Microwave Integrated Circuits Conference (EuMIC), Nuremberg, Germany, 2017, pp. 1-4. [JM5]

6. P. Bassirian, J. Moody, A. Gao, T. Manzaneque, B. H. Calhoun, N. S. Barker, S. Gong, S. M. Bowers, “A passive 461 MHz AlN-CMOS RF front-end for event-driven wake-up receivers, 2017 IEEE SENSORS, Glasgow, Scotland, 2017, pp.1-3. [JM6]

7. J. Moody, P. Bassirian, A. Roy, N. Liu, S. Pancrazio, N. S. Barker, B. H. Calhoun, S. M. Bowers, “A -76dBm 7.4nW wake-up receiver with automatic offset compensation, accepted

to 2018 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2018, pp. 1-2. [JM7]

8. J. Moody, A. Dissanayake, H. Bishop, R. Lu, N. Liu, D. Duvvuri, A. Gao, N. S. t Barker, S. Gong, B. H. Calhoun, S. M. Bowers "A -106 dBm 33 nW 428 MHz Samplifier wake-up receiver," Accepted for the Very Large Scale Integrated Systems - Circuits (VLSI), Kyoto, Japan, 2019 [JM8]

9. J. Moody, S. M. Bowers, "Triode-mode envelope detectors for IoE wake-up receivers, Accepted for the 2019 IEEE MTT-S International Microwave Symposium (IMS), Boston, MA, 2019, pp. 1-4. [JM10]

8.3.2 Accepted and submitted journal publications

1. K. Sun, J. Moody, Q. Li, S. M. Bowers, A. Beling, "High power integrated photonic W-band emitter, in IEEE Transactions on Microwave Theory and Techniques (TMTT), vol. PP, no. 99, pp. 1-10. [JM11]

2. P. Bassirian, J. Moody, R. Lu, A. Gao, A. Roy, N. S. Barker, B. H. Calhoun, S. Gong, S. M. Bowers, "Nanowatt-level wake-up receiver front-ends using MEMS resonators for impedance transformation," Submitted to IEEE Transactions on Microwave Theory and Techniques (TMTT). [JM12]

3. J. Moody, P. Bassirian, A. Roy, N. Liu, N. S. Barker, B. H. Calhoun, S. M. Bowers, "Interference robust detector-first near-zero power wake-up receiver," in IEEE Journal of Solid-State Circuits, pp. 1-14, 2019. [JM13]

4. J. Moody, A. Dissanayake, H. Bishop, R. Lu, N. i Liu, D. Duvvuri, A. Gao, N. S. Barker, S. Gong, B. H. Calhoun, S. M. Bowers, "A highly re-configurable bit-level duty cycled TRF receiver achieving -106 dBm sensitivity and 33 nW power consumption" Invited to SSCL special issue on VLSI 2019. [JM14]

8.3.3 Planned publications

1. Samplifier 2 journal submission (JSSC) [JM15]

2. Samplifier 2 conference paper (ISSCC) [JM16]

3. Samplifier 3 conference submission (VLSI-C or RFIC) [JM17]

4. MEMS amplifier publication (MWCL-IMS) [JM18]

APPENDIX A

ANALYSIS OF SQUARE-LAW TRF RECEIVERS

A.1 Motivation

Accurate modeling of a system under consideration is necessary in order to establish performance boundaries, preform design optimization, and to identify weaknesses in the architecture which can be resolved with topological and architectural changes. For the samplifier system this analysis allows us to answer such questions as:

1. What are the fundamental sensitivity limitations of this architecture?
   (a) How much RF gain is needed to optimize sensitivity?
   (b) How does RF input bandwidth affect our minimum detectable signal (MDS)?
   (c) How does front-end noise figure affect sensitivity?
2. What are the fundamental trade-offs between power consumption, sensitivity and latency?
   (a) What is the trade space like regarding sensitivity and power?
3. What are the key components to focus design efforts on?

A.2 Samplifier system noise analysis

A system diagram for the Samplifier is shown in figure A.1 (a), where the following assumptions have been made:

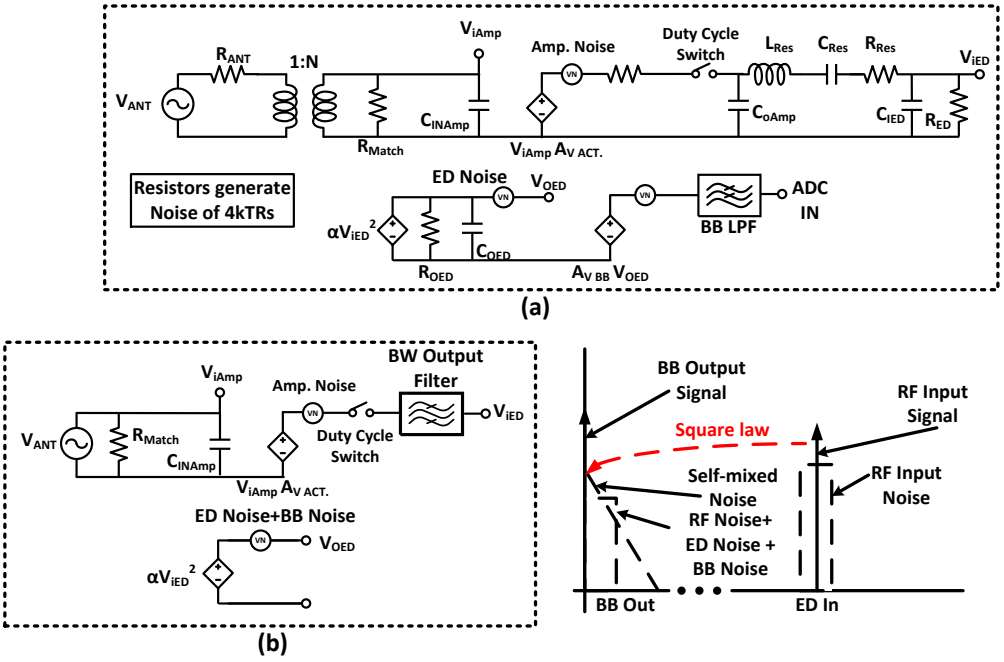

Figure A.1: System block diagram for noise analysis, (a) shows functional diagram of the system including major amplifier and signal processing blocks, (b) shows simplified model of (a) for noise and signal analysis, and (c) single tone TRF block diagram not including sampling.

1. Ideal square-law envelope detector
2. Detector RF input noise is narrow-band Gaussian
3. Single tone is present at input with an amplitude of A_0

The RF amplifier output voltage noise spectral density can be written as

$$\overline{v_{n,in}^2} = 4kT_{sys}R_{Match}|H_{RF}(f)|^2 \quad \frac{V^2}{Hz}, \tag{A.1}$$

where k is Boltzmann's constant, T_{Sys} is the input noise temperature into the envelope detector post filtering which includes the effect of gain, R_{Match} is the source impedance presented to the

system by the antenna and matching network, $|H_{RF}(f)|^2$ is the shape of the output noise spectrum normalized to unity.

Therefore the RF amplifier output integrated voltage power is

$$\overline{v_{n,in}^2} = 4kT_{sys}R_{Match}\int_0^\infty |H_{RF}(f)|^2 df = 4kT_{Sys}R_{Match}B_{RF} \quad V^2 \tag{A.2}$$

where B_{RF} is the noise equivalent bandwidth presented to the envelope detector, where

$$T_{sys} = T_0 F_{FE} A_{vAmp}^2 \quad Kelvins \tag{A.3}$$

where T_0 is the physical input noise temperature, F_{FE} is the RF amplifier noise factor and A_{vAmp} is the RF amplifier active voltage gain.

The noise voltage dropping entirely across the amplifier does not imply a reflection at the antenna interface, as noise and signal power is dissipated in the antenna source impedance and the finite Q-factor of the resonating inductor.

In order to find the output noise power spectral density, it is useful to work with the time domain expressions for both signal and noise at the RF input. As noise is a random signal, examining the auto-correlation function of the ED input noise can be useful for analysis. The autocorrelation function can be shown as

$$\mathcal{R}_{vi}(\tau) = 4kT_{Sys}R_s\mathcal{R}_{LP}(\tau)cos(2\pi f_0\tau) \quad V^2, \tag{A.4}$$

the corresponding power spectral density is

$$S_{vi} = 2kT_{Sys}R_s[S_{LP}(f-f_0) + S_{LP}^*(f+f_0)] \quad V^2/Hz. \tag{A.5}$$

where S_{LP} is the normalized low pass equivalent spectrum shape of the shaped RF input noise, and $\mathcal{R}_{LP}$ is the low pass equivalent noise autocorrelation function. This frequency response is not necessarily equivalent to the transfer function of the RF filter as in general noise figure is a function of frequency. For a ideal rectangular band-pass filter the autocorrelation can be written as

$$\mathcal{R}_{vi}(\tau) = 4T_{Sys}kB_{RF}R_s\frac{sin(\pi B_{RF}\tau)}{\pi B_{RF}\tau}cos(2\pi f_0\tau) \sim V^2, \tag{A.6}$$

where f_0 is the RF carrier frequency, and the power spectral density is

$$S_{vi} = 2T_{Sys}kR_s[rect(\frac{f-f_0}{B_{RF}}) + rect(\frac{f+f_0}{B_{RF}})] \sim V^2/Hz. \tag{A.7}$$

Equation (A.7) provides a good approximation of the PSD of the output noise assuming a high Q-factor output filtering is utilize. The envelope detector can be treated as an ideal square-law detector for the noise analysis:

$$V_O = \alpha V_{iED}^2 \tag{A.8}$$

where V_O is the output voltage from the ED, V_{iED} is the ED input voltage and α is the detector OCVS.

The input voltage V_{iED} can be expressed as

$$V_{iED} = V_{Sig}(t) + V_N(t) \tag{A.9}$$

where V_{Sig} is the signal voltage and $V_N(t)$ is the input noise voltage with auto-correlation (A.4 and integrated voltage spectral density (A.3).$V_{Sig}(t)$ can be expressed as:

$$V_{Sig}(t) = V_{RF}cos(2\pi f_0 t + \phi) \tag{A.10}$$

where ϕ is a random phase offset for mathematical convenience, V_{RF} is the amplitude of the RF carrier at the ED input.

The auto-correlation of the output signal from the detector

$$R_{Vo}(\tau) = E[V_O(t)V_O(t+\tau)] = \alpha^2 E[V_i(t)^2 V_i(t+\tau)^2] \tag{A.11}$$

$$= \alpha^2 E[(V_{sig}(t) + V_N(t))^2 (V_{sig}(t+\tau) + V_N(t+\tau))^2] \tag{A.12}$$

$$= \alpha^2 E[(V_{sig}(t)^2 + 2V_{sig}(t)V_N(t) + V_N(t)^2)(V_{sig}(t+\tau)^2 + 2V_{sig}(t+\tau)V_N(t+\tau) + V_N(t+\tau)^2)]. \tag{A.13}$$

This expression generates nine cross terms inside the expected value operator.

$$R_{Vo}(\tau) = \alpha^2 E[\sum_{i=1}^{9} X_i] \tag{A.14}$$

The first cross term represents the signal mixing with itself

$$E[X_1] = E[(V_{sig}(t)^2(V_{sig}(t+\tau)^2] = V_{RF}^4 E[cos(2\pi f_0 t + \phi)^2 cos(2\pi f_0(t+\tau) + \phi)^2] \tag{A.15}$$

$$= \frac{V_{RF}^4}{4} E[(1 + cos(4\pi f_0 t + 2\phi))(1 + cos(4\pi f_0 t_c(t+\tau) + 2\phi))] \tag{A.16}$$

$$= \frac{V_{RF}^4}{4} E[1 + cos(4\pi f_0 t + 2\phi) + cos(4\pi f_0(t+\tau) + 2\phi)) + cos(4\pi f_0 t + 2\phi) cos(4\pi f_0(t+\tau) + 2\phi))] \tag{A.17}$$

from the identities any $cos(x + \phi)$ where ϕ is a random variable $E[cos(x + \phi)] = 0$, $E[C] = C$, and $E[X(\tau)] = X(\tau)$ if $X(\tau)$ is deterministic.

$$= \frac{V_{RF}^4}{4} + \frac{V_{RF}^4}{4} E[cos(4\pi f_0 t + 2\phi) cos(4\pi f_0(t+\tau) + 2\phi))] = \frac{V_{RF}^4}{4} + \frac{V_{RF}^4}{8} cos(4\pi f_0 \tau) \tag{A.18}$$

.

The second cross term is a mixing between the signal and noise producing

$$E[X_2] = E[V_{Sig}^2 V_N(t+\tau) V_{Sig}(t+\tau)] = 2V_{RF}^3 E[V_{Sig}^2 V_{Sig}(t+\tau)] E[V_N(t+\tau)] = 0 \tag{A.19}$$

from $E[V_N(\tau)] = 0$ (zero mean Gaussian noise).

The third cross term generates represents noise mixing with the signal

$$E[X_3] = E[V_{Sig}^2 V_N(t+\tau)^2] = V_{RF}^2 E[cos(\pi f_0 t + \phi)^2 V_N(t+\tau)^2] \tag{A.20}$$

$$= \frac{V_{RF}^2}{2} E[(1 + \cos 4\pi f_0 t + 2\phi) V_N(t+\tau)^2] = \frac{V_{RF}^2}{2} E[V_N(t+\tau)^2] = \frac{V_{RF}^2 \sigma_N^2}{2}. \tag{A.21}$$

where σ_N^2 is the variance of the input RF noise. This term is very interesting in that it implies that at very low signal levels the envelope detector operates in a "linear regime" where input and output signal amplitudes are proportional. A physical explanationc for this effect is found by considering when there is constructive interference between the noise and the RF signal, the output signal is slightly stronger, whereas when they are out of phase the output signal is slightly weaker. Due to the quadratic nonlinearity, the rectified output signal when signal and noise add is in-phase is larger than the drop in the output signal when they are out of phase producing a DC offset.

Cross term 4 is symmetric with cross term 2 so $E[X_2] = E[X_4] = 0$

Cross term 5 represents the signal down-converting the input noise spectrum, and leads to baseband noise as seen by

$$E[X_5] = 4E[V_{Sig}(t) V_N(t) V_{Sig}(t+\tau) V_N(t+\tau)] \tag{A.22}$$

$$= 4V_{RF}^2 E[V_N(t) V_N(t+\tau)] E[cos(2\pi f_0 t + \phi) cos(2\pi f_0 (t+\tau) + \phi)] \tag{A.23}$$

$$= 4V_{RF}^2 R_{vi}(\tau) E[cos(2\pi f_0 t + \phi) cos(2\pi f_0 (t+\tau) + \phi)] = 4V_{RF}^2 \mathcal{R}_{vi} cos(2\pi f_0 \tau). \tag{A.24}$$

where $\mathcal{R}_{vi}$ is the auto-correlation function of the input RF noise to the envelope detector. Cross term 6 is found by:

$$E[X_6] = E[2V_N(t) V_{Sig}(t) V_N(t+\tau)] = E[2V_N(t) V_N(t+\tau)] E[V_{Sig}(t)] = 0. \tag{A.25}$$

Cross term 7 is equivalent with 3 so it is equal to $\frac{V_{RF}^2 \sigma_N^2}{2}$ Cross term 8 is equivalent with 6 so it is equal to 0. Finally cross term 9 which represents a self-mixing between the RF noise and itself

$$E[X_9] = E[V_N(t)^2 V_N(t+\tau)^2] = E[V_N(t)^2] E[V_N(t+\tau)^2] + 2E[V_N(t) V_N(t+\tau)]^2, \tag{A.26}$$

from $E[WXYZ] = E[WX]E[YZ] + E[WY]E[XZ] + E[WZ]E[XY]$ for zero mean Gaussian processes. Therefore

$$E[X_9] = \mathcal{R}_{vi}(0)^2 + 2\mathcal{R}_{vi}(\tau)^2, \tag{A.27}$$

where $\mathcal{R}_{vi}(0)^2$ represents a DC offset caused by the noise self mixing, and $2\mathcal{R}_{vi}(\tau)$ represents time varying noise at the detector output.

Summarizing the analysis, each cross term generates either zero or a term in the output of the detector as follows:

- X_1 represents the signal mixing with itself at the output of the envelope detector.
- $X_{3,7}$ is generated due to interaction between the RF noise and the signal producing a DC components proportional to the signal and noise amplitudes.
- X_5 represents noise down-converted by the input RF signal appearing at the output of the detector, this is equivalent to the down-converted output noise of an ideal product mixer. This noise is the most fundamental noise in our receiver system.
- X_9 represents the self-mixing of the RF noise with itself, which produces a DC term and an AC term at the output of the envelope detector. It is important to note that the DC offset when the signal amplitude is less than the rms noise amplitude is larger than the signal generated by the self-mixing of the signal.

Combining these terms leads to

$$\mathcal{R}_{no}(\tau) = \alpha^2(\frac{V_{RF}^4}{4} + V_{RF}^2\sigma_N^2 + 4V_{RF}^2\mathcal{R}_{vi}(\tau)cos(2\pi f_0\tau) + \mathcal{R}_{vi}(0)^2 + 2\mathcal{R}_{vi}(\tau)^2) \tag{A.28}$$

Taking the Fourier transform of this expression leads to our desired result, which is the power spectral density at the output of the envelope detector (A.43).

$$S_{vo}(f) = F\{\mathcal{R}_{vo}(\tau)\} \tag{A.29}$$

Evaluating this expression term by term at f=0 leads to:

$$F\{\frac{V_{RF}^4}{4} + V_{RF}^2\sigma_N^2 + \mathcal{R}_{vi}(0)^2\} = \delta(f)(\frac{V_{RF}^4}{4} + V_{RF}^2 4kT_{Sys}B_{RF}R_s + (4kT_{Sys}B_{RF}R_s)^2), \tag{A.30}$$

for the DC components is found through evaluating $\mathcal{R}_{vi}(0)^2$ which leads to

$$\mathcal{R}_{vi}(0)^2 = (4kT_{Sys}B_{RF}R_s)^2, \tag{A.31}$$

where we can see a dependence of the DC offset voltage on the noise equivalent bandwidth of the front-end, this dependency comes from the identity $R(0) = \sigma_N^2$. Note that this offset voltage is independent on the shape of the filter response.

For the signal mixing with noise components we find:

$$F\{4V_{RF}^2\mathcal{R}_{vi}cos(2\pi f_0\tau)\} = 2V_{RF}^2(S_{vi}(2\pi(f-f_0)) + S_{vi}(2\pi(f+f_0))), \tag{A.32}$$

where S_{vi} is the voltage spectral density of the input noise. Utilizing (A.5) we find

$$2V_{RF}^2(S_{vi}(2\pi f-2\pi f_0)+S_{vi}(2\pi f+2\pi f_0)) = 4V_{RF}^2kT_{Sys}R_s[S_{LP}(f-2f_0)+S_{LP}(f)+S_{LP}^*(f)+S_{LP}^*(f+2f_0)]. \tag{A.33}$$

Removing the sum and difference frequency terms due to post ED low pass filtering leads to

$$2V_{RF}^2(S_{vi}(2\pi f - 2\pi f_0) + S_{vi}(2\pi f + 2\pi f_0)) = 4V_{RF}^2kT_{Sys}R_s[S_{LP}(f) + S_{LP}^*(f)], \tag{A.34}$$

which from $S(f)^* = S(-f)$ and the fact that the Fourier transform of a real-valued even function is a real even function gives us

$$2V_{RF}^2(S_{vi}(2\pi f - 2\pi f_0) + S_{vi}(2\pi f + 2\pi f_0)) = 8V_{RF}^2kT_{Sys}R_sS_{LP}(f). \tag{A.35}$$

This expression for the case of the ideal band-pass filter becomes

$$2V_{RF}^2(S_{vi}(f - f_0) + S_{vi}(f + f_0)) = 8V_{RF}^2T_{Sys}kR_srect(\frac{f}{B_{RF}}). \tag{A.36}$$

Finally transforming the noise self-mixing term of (A.28) we find

$$S_{SelfMix}(f) = F\{\mathcal{R}_{vi}(\tau)^2\}) = (4T_{Sys}kR_s)^2F\{(\mathcal{R}_{LP}(\tau)cos(2\pi f_0\tau))^2\}, \tag{A.37}$$

$$S_{SelfMix}(f) = 8(T_{Sys}kR_s)^2F\{(\mathcal{R}_{LP}(\tau)^2(1+cos(4\pi f_0\tau))). \tag{A.38}$$

Filtering out double frequency components leads to

$$S_{SelfMix}(f) = 8(T_{Sys}kR_s)^2F\{(\mathcal{R}_{LP}(\tau)^2)\} \tag{A.39}$$

which is equal to

$$S_{SelfMix}(f) = 8(T_{Sys}kR_s)^2S_{LP}(f) * S_{LP}(f) \tag{A.40}$$

as $S_{LP}(f)$ is symmetric about the $f = 0$ axis and has a value of 1 at frequencies close to zero due to the assumed normalization in the definition of $S_{LP}(f)$. We can express (A.41) as

$$S_{SelfMix}(f) = 8(T_{Sys}kR_s)^2\int_{-\infty}^{\infty} S_{LP}(\lambda)^2d\lambda \tag{A.41}$$

for frequencies close to zero relative to the RF carrier bandwidth. From the definition of the noise equivalent bandwidth we can express this as

$$S_{SelfMix}(f) = 8(T_{Sys}kR_s)^2B_{RF} \tag{A.42}$$

for $f << B_{RF}$. This result again shows the importance of the input noise equivalent bandwidth on the output noise of the receiver, as the downconverted noise power spectral density grows linearly with the NEB.

For the example of an ideal BPF

$$F\{\mathcal{R}_{vi}(\tau)^2\}) = (4T_{Sys}kB_{RF}R_s)^2F\{(\frac{sin(\pi B_{RF}\tau)}{\pi B_{RF}\tau}cos(2\pi f_0\tau))^2\} \tag{A.43}$$

$$= \frac{(4T_{Sys}kB_{RF}R_s)^2}{2} F\{(\frac{sin(\pi B_{RF}\tau)}{\pi B_{RF}\tau})^2(1 + cos(4\pi f_0\tau))\} \quad \text{(A.44)}$$

Setting $K = \frac{(4T_{Sys}kB_{RF}R_s)^2}{2}$ we can expand (A.44) into

$$= KF\{(\frac{sin(\pi B_{RF}\tau)}{\pi B_{RF}\tau})^2 + (\frac{sin(\pi B_{RF}\tau)}{\pi B_{RF}\tau})^2(cos(4\pi f_0\tau))\} \quad \text{(A.45)}$$

The second half of this expression is up-converted by the sinusoidal modulation, this term is removed through low pass filtering, reducing (A.46) to

$$F\{\mathcal{R}_{vi}(\tau)^2\}) = KF\{(\frac{sin(\pi B_{RF}\tau)}{\pi B_{RF}\tau})^2\} = \frac{K}{2B_{RF}} tri(\frac{f}{2B_{RF}}) \quad \text{(A.46)}$$

Combining (A.30), (A.35) and(A.46) we finally arrive at

$$S_{vo}(f) = \alpha^2((\underbrace{\frac{V_{RF}^4}{4} + V_{RF}^2 4kT_{Sys}B_{RF}R_s + (4kT_{Sys}B_{RF}R_s)^2)\delta(f)}_{\textbf{DC Components}} + \underbrace{8V_{RF}^2 kT_{Sys}R_s S_{LP}(f)}_{\textbf{Noise-Signal Mixed}}$$
$$+ \underbrace{4(T_{Sys}kR_s)^2)S_{LP}(f) * S_{LP}(f))}_{\textbf{Noise-self Mixed}}. \quad \text{(A.47)}$$

As an example the special case of a ideal rectangular filter on the input leads to

$$S_{vo}(f) = \alpha^2((\underbrace{\frac{V_{RF}^4}{4} + V_{RF}^2 4kT_{Sys}B_{RF}R_s + (4kT_{Sys}B_{RF}R_s)^2)\delta(f)}_{\textbf{DC Components}} + \underbrace{8V_{RF}^2 T_{Sys}kR_s rect(\frac{f}{B_{RF}})}_{\textbf{Noise-Signal Mixed}}$$
$$+ \underbrace{4B_{RF}(T_{Sys}kR_s)^2 tri(\frac{f}{2B_{RF}})}_{\textbf{Noise-self Mixed}} \quad \text{(A.48)}$$

For the special case where $B_{BB} << B_{RF}$ we can write the downconverted noise as

$$S_{vo}(f) = V_{RF}^2 kT_{Sys}R_s + 4(T_{Sys}kR_s)^2 B_{RF} \quad \text{(A.49)}$$

for $f < B_{BB}$. Note that this expression does not depend on the shape of the input noise, but only on its noise equivalent bandwidth.

The output signal terms (here defined as output signals which are related to the transmitted RF signal) can be expressed as

$$V_{Sig}^2 = \alpha^2(\frac{V_{RF}^4}{4} + V_{RF}^2\sigma_N^2) \tag{A.50}$$

or in voltage domain

$$V_{Sig} = \alpha\sqrt{\frac{V_{RF}^4}{4} + V_{RF}^2\sigma_N^2} \tag{A.51}$$

with DC voltage offset of

$$V_{Offset} = \alpha\mathcal{R}_{vi}(0) = \alpha 4kT_{Sys}B_{RF}R_s. \tag{A.52}$$

The total integrated noise from integrated from 0 to B_{BB} gives an output noise of

$$\overline{v_{n,Out}^2} = B_{BB}\alpha^2[8V_{RF}^2T_{Sys}kR_s + 4B_{RF}(T_{Sys}kR_s)^2] \quad \frac{V^2}{Hz} \tag{A.53}$$

which leads to an output SNR of

$$SNR_{Out} = \frac{\frac{V_{RF}^4}{4} + V_{RF}^2 4kT_{Sys}B_{RF}R_s}{B_{BB}[8V_{RF}^2T_{Sys}kR_s + 4B_{RF}(T_{Sys}kR_s)^2]} = \frac{V_{RF}^2}{16B_{BB}}\frac{V_{RF}^2 + kT_{Sys}B_{RF}R_s}{[2V_{RF}^2T_{Sys}kR_s + B_{RF}(T_{Sys}kR_s)^2]}. \tag{A.54}$$

This expression enables us to calculate the output SNR of a TRF receiver, which enables optimization of the RF blocks from a system perspective. Through this analysis the significance of both the RF noise figure, output bandwidth, ED noise and ED conversion gain are shown.

A.3 Effect of sampling on output signal and noise in bit-level duty cycled receivers

The sampling of a bit-level duty cycled receiver has the effect of spreading the energy of the input signal and interference across a wide frequency span. The effect of this sampling on the input signal and noise at the detector interface can be expressed as

$$V_{IED}(t) = (V_{S/I}(t) + V_N(t))Rect(t/\tau), \tag{A.55}$$

where $V_{S/I}$ is the voltage produced by the signal and any interference, V_N is the bandpass filtered RF noise into the detector, $Rect(t/\tau)$ represents a single sampling event which is described by a single square pulse and T is the sampling duration of the bit-level duty cycle, where the Rect function has been shifted so that the beginning of sampling occurs at t=0.

Applying a procedure similar to that found in Equation (A.18) in the appendix reveals

$$R_{Vo}(\tau) = E[V_{OED}(t)V_{OED}(t+\tau)] = \alpha^2 E[V_i(t)^2 V_i(t+\tau)^2] = \\ \alpha^2 E[(V_{S/I}(t) + V_N(t))^2 (V_{S/I}(t+\tau) + V_N(t+\tau))^2] Rect(\tau/T), \tag{A.56}$$

where the properties of the rect function of $Rect(X)^2 = Rect(X)$ and $Rect(X + A)Rect(X) = Rect(A)$ have been applied. The term $\alpha^2 E[(V_{S/I}(t) + V_N(t))^2 (V_{S/I}(t+\tau) + V_N(t+\tau))^2]$ is equal to the second term in Equation (A.18) and is solved in this appendix as equation (A.47). Taking the Fourier transform of (A.56) leads to

$$S_{VoSamp}(f) = 2Tsinc(Tf) * S_{Vo}, \tag{A.57}$$

where S_{Vo} is the found from Equation (A.47), and $*$ is a convolution operator and the factor of two accounts for negative frequency in the voltage domain signal. As the effective bandwidth of the sampling pulse is assumed to be very narrow compared with the noise equivalent bandwidth

at the RF input this convolution has a very weak impact on the power spectral density of the down-converted RF noise. This is due to the sampling window typically being several hundred microseconds long, which corresponds to 10's of kHz in bandwidth for this signal, and an assumed several MHz of bandwidth assumed on the RF input noise. This can lead to a simple modification of (A.47) which leads to

$$S_{vo}(f) = 2\alpha^2((\frac{V_{S/I}^4}{4}+V_{S/I}^2 4kT_{Sys}B_{RF}R_s+(4kT_{Sys}B_{RF}R_s)^2)Tsinc(Tf)+8V_{Int}^2 kT_{Sys}R_s S_{LP}(f+\Delta f) + 4(T_{Sys}kR_s)^2)S_{LP}(f) * S_{LP}(f)). \quad \text{(A.58)}$$

This simplification of (A.57) arises from the fact that the sinc function is very narrow spectrally with respect to the down-converted noise, and the convolution property of the delta function. In the case of strong interference ($V_{S/I}^2 >> 4kT_{Sys}B_{RF}R_s$) the signal terms in (A.58) can be expressed as

$$S_{vo}(f) = 2\alpha^2 T\frac{V_{S/I}^4}{4}sinc(Tf). \quad \text{(A.59)}$$

This result has many implications in the design of the receiver. Principally it determines the ideal baseband filter frequency response (matched filter) to maximize output SNR, it also shows that because of the sampling the use of simple low frequency DC blocking filters does not reject the presence of CW interference as it does in the non-bit-level duty cycled receivers. Another way to consider this result is that all CW interference into the receiver becomes spread spectrally following in a sinc envelope which requires additional filtering to reject.

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