Investigation of Ti-line and E-beam Fabrication Processes for Superconducting, Phonon Cooled Hot Electron Bolometers

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Abstract

Two processes were devised utilizing electron beam as well as optical lithography for fabricating niobium nitride (NbN) hot electron bolometers (HEB). This process was developed due to issues with an HEB fabrication method known as the "Ti-line" method. The Ti-line process utilized only optical lithographic means for making HEB devices. This was revolutionary in that HEB's need nano-scale features which usually necessitate the use of electron beam lithography. By being able to use optical lithographic mean to obtain nano-scale dimensions allows for faster throughput among other things. In all, the Ti-line method was an excellent means for fabricating Nb HEB devices. Unfortunately, when trying to make NbN HEBs the NbN material would have higher than normal resistances as well as resistances that would rise over time. After much work investigating the reason for the heightened resistance, it was determined that an oxygen plasma step was a major factor. Unfortunately there did not appear to be a way to process the HEBs using the Ti-line method without using the O_2 plasma.

Electron beam lithography (ebl) is the current state of the art for fabricating HEB devices. In this work two mask designs were devised with the same basic end design as the Ti-line device design except that the new mask sets incorporate an ebl step. Along with this, the two processes have different ebl techniques for obtaining nano-scale dimensions. The reason for having two methods was the ebl system at the University of Virginia is an older system and was not always able to resolve small enough features. Thus two variations were devised in the event the e-beam resolution was not optimal.

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List of Symbols

A - Ampere
Å - Angstrom
C – Celsius
dB – Decibel
DI – deionized
f – Frequency
f_{IF} – Intermediate frequency where $f_{IF} = f_{sig} - f_{LO}$
f_{LO} – Local Oscillator frequency
f_{sig} – Incident RF signal
HEB – Hot Electron Bolometer
Hz – Hertz
I_{beam} – Beam Current
IF – Intermediate Frequency
LO – Local Oscillator
$L_{e\text{-}ph}$ - Electron to phonon scattering length
RF – Radio frequency
R_{HEB} – HEB resistance
R_S – Sheet Resistance
rpm – revolutions per minute
S – Step size
sccm – standard cubic centimeter per minute
T – Torr
T_B – Bath temperature
T_c – Critical temperature
T_{dwell} – Dwell Time
τ_{ep} - Electron-phonon energy transfer time
τ_{es} – Phonon escape time
τ_{ep} - Phonon-electron energy transfer time
UV – Ultra Violet
V – volt
W – Watt
w – width
Ω - Ohm

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Finally, the Blue Ridge Mountain Rescue Group, for the friendships formed and the experiences gained. I probably could have finished my thesis sooner had I not been as involved. But to give up those experiences just to finish earlier is not a choice I would make.

Chapter 1: Introduction

This master thesis encompasses the investigation of the fabrication processes for hot-electron bolometer (HEB) devices, ultimately for application to THz heterodyne detectors. Superconducting HEBs have been used for a variety of submillimeter detector applications. One such application is in the field of radio astronomy where HEB devices have been used beyond one-terahertz with lower noise compared to Schottky or superconducting insulator superconducting (SIS) devices [1] [2] [3] [4] [5].

The basic structure of an HEB is a superconducting thin-film bridge spanning thicker metal contact pads. An HEB operates by absorbing energy in the superconducting film, which in turn heats the film and increases its resistance [1] [6] [7] [8]. The HEB is typically cooled by one of two mechanisms: diffusion or phonon cooling. Diffusion cooling occurs when the hot electrons diffuses out of the superconductor to the adjacent contact pads where they are absorbed/dissipated. Phonon cooling occurs when the absorbed energy is dissipated through phonons into the substrate itself [1] [5]. The basic operation of these HEB devices and basic mixer theory, will be described further in chapter 2.

In the past decade a novel HEB fabrication method, called the Ti-Line process, was developed at the University of Virginia [7]. This fabrication method was radically different from other approaches in the literature since it did not require electron beam (e-beam) lithography to create the nanometer wide dimensions necessary for submillimeter HEBs. All of the fabrication is accomplished using optical lithography methods. This increases the speed of fabrication since it is not a direct write technique and even more importantly permits groups without e-beam lithography capabilities to engage in HEB research. The Ti-line process worked well for Niobium (Nb) d-HEB devices. Unfortunately, when using the same process to develop niobium nitride (NbN) phonon cooled p-HEBs, significant technical obstacles were encountered in this work, including higher than expected device resistance and HEBs

that increased in resistance over time. Chapter 3 of this thesis describes the basic Ti-line process and also describes the initial evidence and measurements of resistance problems with our Ti-line fabricated HEB devices.

Chapter 4 details this thesis's investigation of the Ti-line resistance phenomena, as well as our attempts to solve this issue. After exhausting reasonable avenues of Ti-line fabrication, a different fabrication scheme using e-beam lithography was sought to avoid the resistance rise issue. Given the limitations of our e-beam lithography tool, a process that uses a minimal amount of e-beam and mostly optical lithography was devised and developed. This e-beam HEB fabrication design will be discussed in chapter 5. Finally, a conclusion and recommendations for future work is given in chapter 6.

Chapter 2: P-HEB Operation

In this chapter we will go over the basic operation of phonon cooled (p-HEB) devices. Diffusion cooled (d-HEB) HEBs will also be discussed, though less so since the primary emphasis of this work is on p-HEBs. The material structure of an HEB and how it affects the device's operation is another important point that will be delved into. Initially though, we will go over basic mixer theory for heterodyne receivers and how HEBs are implemented as mixers.

There are a variety of devices that are used as mixers for mm and sub-mm applications such as the SIS (Superconductor-Insulator-Superconductor) device and Schottky diode. The SIS device acts as an excellent mixer below the THz range while the Schottky diode can operate in the THz spectrum offering larger IF bandwidth, but suffers from a higher noise temperature than a HEB at the same frequency [8] [9]. In its simplest form, an HEB is a device for detecting incident electromagnetic power [6] [7]. Operationally, the HEB material has a resistance that is temperature sensitive [10]. Another important benefit is that HEBs do not require as high a LO (Local Oscillator) power as a Schottky diode [8][11].

The operation of a heterodyne receiver starts with an incident RF signal (f_{sig}). This signal is sent to the mixing element that is also receiving a local oscillator frequency (f_{LO}). When the two signals are mixed, an intermediate frequency (IF) is produced. The IF can then be amplified and measured. Fig. 2.0 shows a basic block diagram of a heterodyne receiver.

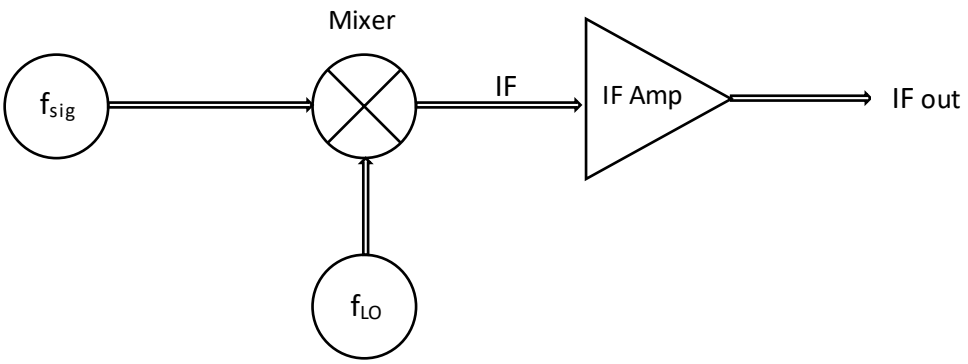

Fig. 2.0 Block diagram of a heterodyne receiver.

Since the incident RF is a high frequency signal, it can be more readily amplified and analyzed after the frequency is reduced. The mixer accomplishes this by generating the difference of the signal frequency and LO frequency and creating an intermediate frequency f_{IF}.

$$f_{IF} = f_{sig} - f_{LO}$$

With the mixing, many other harmonics are created in the process but those can be filtered out leaving the IF only [5]. Also, although the IF is at a different lower frequency than the original signal frequency, it still retains the same information as the signal frequency including phase and spectral information [5].

The structure of both the d-HEB and p-HEBs contain similarities. They are both superconducting, nanoscale devices between two normal metal contact pads. The core of the HEB device is a nanoscale superconducting thin film and this part of the device will be referred to as the "kernel". Fig 2.1 shows the basic structure of a HEB. Incident radiation is absorbed by electrons in the superconducting kernel to create 'hot electrons' and these electrons can lose their energy primarily by diffusion into the contact pads or interact through phonons with the substrate [8] [12].

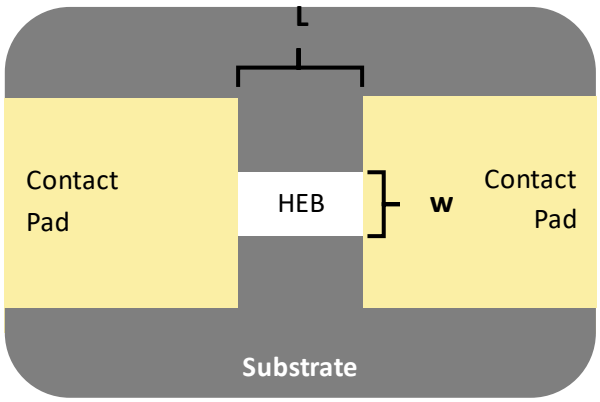

Fig 2.1 Top view of the general structure (not to scale) for a Hot Electron Bolometer consisting of a substrate in gray, two normal metal contact pads (with the superconducting thin-film directly underneath) in yellow, and the superconducting HEB 'kernel' in white. L and w denote the HEB length and width respectively.

We will begin our discussion with the diffusion cooled d-HEB. The most important factor of a d-HEB is that it has a kernel with a relatively short length 'L'. This length is the distance between the two contact pads. The length is important since one cooling mechanism of the hot electrons is accomplished through diffusion of the hot electrons from the HEB kernel to the contact pads that serve as heat sinks. However, if the length of the kernel is too long, then electron-phonon cooling through the substrate will start to dominate the cooling process. To prevent this from happening, the d-HEB length must be smaller than $L_{e\text{-}ph}$ - the electron to phonon scattering length [12].

$$L < L_{e\text{-}ph}$$

In contrast, for the p-HEB case, the length shouldn't be too short or else diffusion cooling will start to dominate. To realize phonon cooling, the thickness of the superconducting kernel also plays an important role. In a p-HEB, the superconducting kernel layer needs to be very thin, on the order of a few

nanometers. With a thin superconducting layer the phonon energy can quickly be absorbed into the substrate and not revert back to the electron 'bath' which is an increasing possibility with a thicker film. With the thinner film, the substrate can act as the heat sink for the energy absorbed by the HEB thus cooling the HEB back to equilibrium [13] [14]. For p-HEBs, there are three main reactions in time that can take place. The electron-phonon energy transfer time τ_{ep}, the phonon escape time τ_{es}, and the phonon-electron energy transfer time τ_{pe} [8] [14] [15]. τ_{ep} is the time it takes within the HEB kernel for the energy in an electron to be transferred to a phonon. From here the phonon energy can escape into the substrate provided the HEB film is thin enough, this is the τ_{es}. For this to happen τ_{es} must be shorter than τ_{pe} . If this is not the case and the film is too thick, the τ_{pe} may occur, reverting the phonon energy back to the electron. So, for a properly working HEB we want: $\tau_{es} << \tau_{pe}$ [8] [15].With all that said, keeping the length short for a p-HEB is still important for the gain bandwidth. With a short HEB length the gain bandwidth increases which allows for a larger range of frequencies for signal amplification. In a paper by S.A. Ryabchun EtAl, NbN p-HEB devices with a length of 0.35µm on Si normally has a 3dB gain bandwidth roll-off of 3.5GHz. With a shorter length of 0.12µm the gain bandwidth increased to 6.5GHz [19]. Also, scaling down the mixer dimensions holding the L x w ratio constant decrease the Absorbed LO power by a factor of two [19].

Another facet that has not yet been mentioned for the operation of an HEB is that they typically currently operate at super-cold, single digit, kelvin temperatures (Though there are some more exotic materials that can operate in the high double digits [16]). This is not the case for Schottky diodes that do not require cooling (though cooling can improve their performance) but can operate at room temperature. Depending on the application, this can be a benefit to that technology over HEBs. Cooling is necessary for HEB operation since the superconducting HEB material needs to be operated near its critical temperature T_c. Given the requirement for thin superconducting films, especially for p-HEBs, the T_c of the kernel is often significantly below the T_c of the bulk superconductor. For most HEBs, including

NbN p-HEBs, this is often achieved by the use of liquid He (of bath temperature T_B) or with closed cycle refrigeration systems [7] [17]. In an HEB, as the material is heated by RF energy, the kernel, or portions of the kernel, temperature can rise above T_c and revert back to a normal metal (i.e. resistive) state. This heated, and resistive, area of the HEB is known as a hotspot and can fluctuate in area with a fluctuation in the input RF [5] [14] [17] [18]. In the case where the HEB acts as a mixer, the heating is caused by both the incident RF and the LO energy [5] [14] [17] where diffusion or phonon cooling acts to bring it back to the bath temperature.

Chapter 3: The Ti-Line Process for HEB Fabrication

In this chapter we will examine the Ti-line process as originally developed at the University of Virginia by Dr. Jonathan Schultz [7]. A significant benefit for using this process is that no electron beam or ion beam techniques are needed to fabricate the HEB. So for research groups that do not have access to a high end E-beam tool, the Ti-line process is an option for realizing feature sizes on the order of 100nm. The process is done completely through UV lithographic means that lithographically defines the features in parallel, as opposed to serial single write methods such as e-beam. We will also delve into the HEB resistance rise and the higher than expected resistance issues that was initially observed by Delbert Herald when he was trying to fabricate NbN HEBs using the Ti-line process. When I began my research Mr. Herald was in the midst of trying to work out the two increased resistance phenomenon. Upon joining the effort my time was initially divided between investigating an existing but old Raith50 (Recently upgraded to a Raith Quantum) electron beam lithography system which was in disrepair with multiple and continuously changing problems, and working with Mr. Herald on the Ti-line project.

(See appendix A) for the full Ti-line fabrication process as developed by Dr. Schultz. The Ti-line process I started with was virtually the same as the original process Dr. Schultz had created with only minor changes. And only a portion of the fabrication process, the actual HEB fabricating part, is of interest. This Ti-line processing portion begins with a wafer composed of a 20nm “thin Au” overlayer on a thin (on order 4nm) NbN layer that was deposited onto a SOI (Silicon On Insulator) substrate. This Ti-line process starts with the application of a spun on bilayer of lift-off resist,(LOR 5B) at 6krpm for a thickness of 500nm and polyimide (Durimide 284) spun at 6krpm for a thickness of 1.2um. According to Dr. Schultz, the LOR was not necessary, though it does allow for a better liftoff and is removed more cleanly in an O2 ash [6]. If no LOR is used then the spin speed was changed to 5krpm for a polyimide thickness of 1.3um. This is followed by a 60nm magnetron sputtered Ti deposition, NFR resist

patterning, and finally reactive ion etching of the Ti. The Polyimide is also etched to a depth of 600nm creating a step in the organic layers with the LOR below and polyimide partly etched in areas not covered by the Ti patterns. The remaining Ti is etched and a second layer of Ti is deposited via magnetron sputter. Since there is a 600nm step in the organic layer from the previous etch, it is necessary to use a deposition tool that is able to cover that sidewall of the step as well as the planar surfaces. This was accomplished by using a Ti target, in the sputter deposition tool, at a 45^{o} angle to the sample. From this point a photoresist layer is spin coated over the newly deposited Ti and the circuit layer pattern is exposed and developed onto the sample. The remaining Ti line processing is shown and described in the following image Fig. 3.0.n

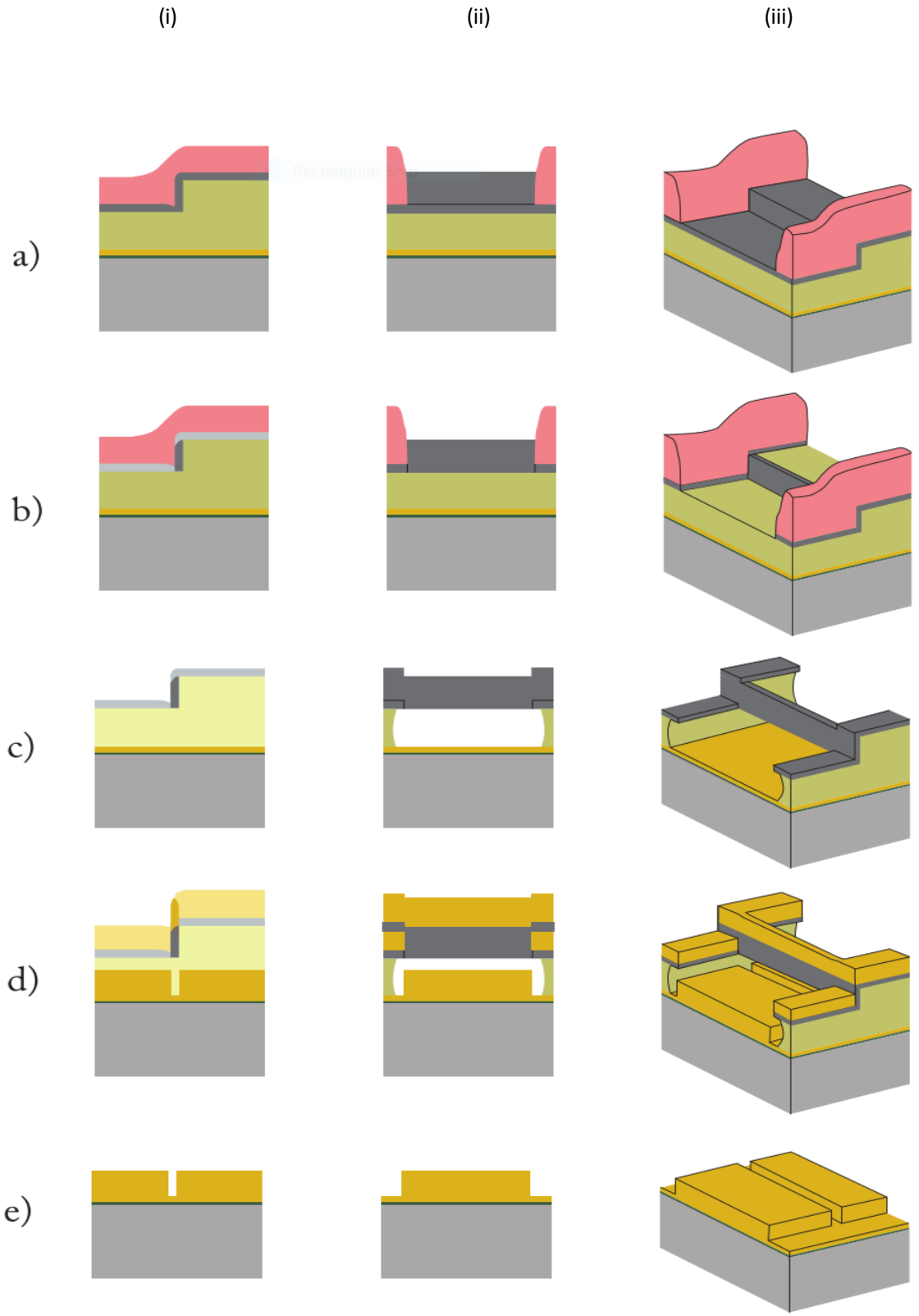

Fig. 3.0 Ti-Line Process Flow [7]

Fig 3.0 row a

The Ti film (thin grey line on top of the pea-green polyimide, is patterned with photoresist (pink). Column (i) shows a cross section where the photo resist is covering the step. Column (ii) is a front view of the step where there are two banks of photoresist, one on the left side and one on the right side, bracketing the Ti covered polyimide step. Column (iii) is a 3D view

Fig 3.0 row b

An anisotropic (in the vertical direction) RIE of the Ti film has been performed. Since the thickness of the Ti film on the planar surfaces is thinner than the thickness of the Ti film on the step (as measured vertically), the Ti film on the planar surfaces will be removed well before a significant amount of Ti has been removed from the sidewall of the step. Column (iii) shows Ti etched away from the planar surfaces, but remaining under the photoresist *and* as a thin (width) line of Ti on the sidewall of the step. This thin strip of Ti is the "Ti-line". The width of this Ti-line (as viewed from above) is controlled by the duration of the Ti deposition. Since thin film deposition is typically on order of 100's of nm, this technique is suitable for the realization of sub-micron sized Ti-line features.

Fig 3.0 row c

An isotropic oxygen plasma has been used to etch away all of the photoresist and much (but not all) of the nLOF/polyimide where it can be seen that the majority of the LOR/polyimide remains under the larger Ti patterns. This 'ash' step typically takes on the order of 5 hours in a tabletop oxygen plasma stripper. Given the thin width of the Ti-line, all of the LOR/polyimide has been removed from underneath what is now a suspended Ti-line element. The left and right banks of LOR/polyimide/Ti support the Ti-line and hence 'anchor' the structure.

Fig 3.0 row d

... At this point the circuit layer Au "thick Au" (on the order of 200nm) is deposited via electron beam evaporation and the suspended Ti-line shadow-masks the area below it from the deposition leaving it free of Au. The HEB will eventually be formed along this shadowed area.

Fig 3.0 row e

Finally, the LOR/polyimide holding up the Ti-line structure is lifted-off in an NMP soak which was heated at 120^{o}C for 30 minutes. This removes the Ti-line stencil and the anchor regions. Finally a 5 minute O_2 plasma ash is done to clean up any residue on the sample surface.

At this point two banks of the thick Au, separated by the Ti line width, have been formed on top of the original NbN/thin Au films. This gap will define the length of the eventual HEB. What remains to be accomplished in principal is the definition of the HEB width. This can be accomplished with the

lithographic definition of the HEB width perpendicular to the previously defined gap, an etch of the thick Au, an etch of the unmasked NbN superconducting film, and finally an etch of the thin Au over the HEB.

While NbN HEB devices can be realized with the Ti-line process, problems have been encountered, the most significant of which stem from changes in the resistivity of the NbN material due to the processing involved. In addition to device resistance increases measured after certain processing steps, often the resistance would continue to rise over time. A relatively simple case is that of the NbN samples provided by an external vendor which had sheet resistances (R_S) ranging from the expected 400Ω/square to over 800Ω/square. Since the existing, original mask set had HEB dimensions of L=0.2µm x w=2µm, any resistance values much over 400Ω/square would not give the designed for room temperature HEB resistance (R_{HEB}) value of 40Ω/square. The equation used to find the resistance of an HEB ($R_{HEB)}$ is:

$$R_{HEB}=R_s*L/w$$

where R_s is the sheet resistance in Ω/square, L and w are the HEB length and width respectively.

A seemingly simple problem could be, and was, accommodated in a new mask set by changing the dimensions to account for the higher starting resistance (This is one of the "fixes" in the new mask set developed which will be described in a subsequent chapter). Unfortunately, the main issue is the resistance increases over time and the increases after various processing steps. It appears that NbN p-HEBs do not react well to some of the Ti-line fabrication process steps. A method for resolving the issue with Nb based d-HEBs was devised by capping the Nb HEB with 100nm of electron beam evaporated germanium [5]. Germanium capping was considered to be a promising solution for resolving the resistance rise over time issue for our NbN p-HEBs such that a mask was added so that the HEB can be capped with Ge. Though one of the major problems dealing with the resistance rise was that the rise is

tied to the use of an oxygen plasma. When NbN is exposed to an O_2 plasma the sheet resistance of the NbN can increase [7]. To see the dramatic increase possible when the NbN HEB is exposed to an oxygen plasma, fig. 3.1 shows the resistance over time of a set of five separate large area NbN HEB devices (no Ge capping layer) where the devices were defined with resist and without the Ti-line process. This large area chip set was developed to allow for rapid testing without having to resort to the Ti-line process or other time consuming methods such as e-beam lithography (and in this case because the e-beam system at our disposal was non-functional). The large area HEBs fabricated using this method were on the order of a micron rather than hundreds of nanometers. We will delve into the large area HEB processing details later. The chips from Fig. 3.1 have a very minimal rise over time up until they are exposed to a 2 hour oxygen plasma. The rise is very sharp with a range of around 200 to 500Ω increase. The small jump before the large spikes was due to heating (The chips were baked on a hotplate at 190°C).

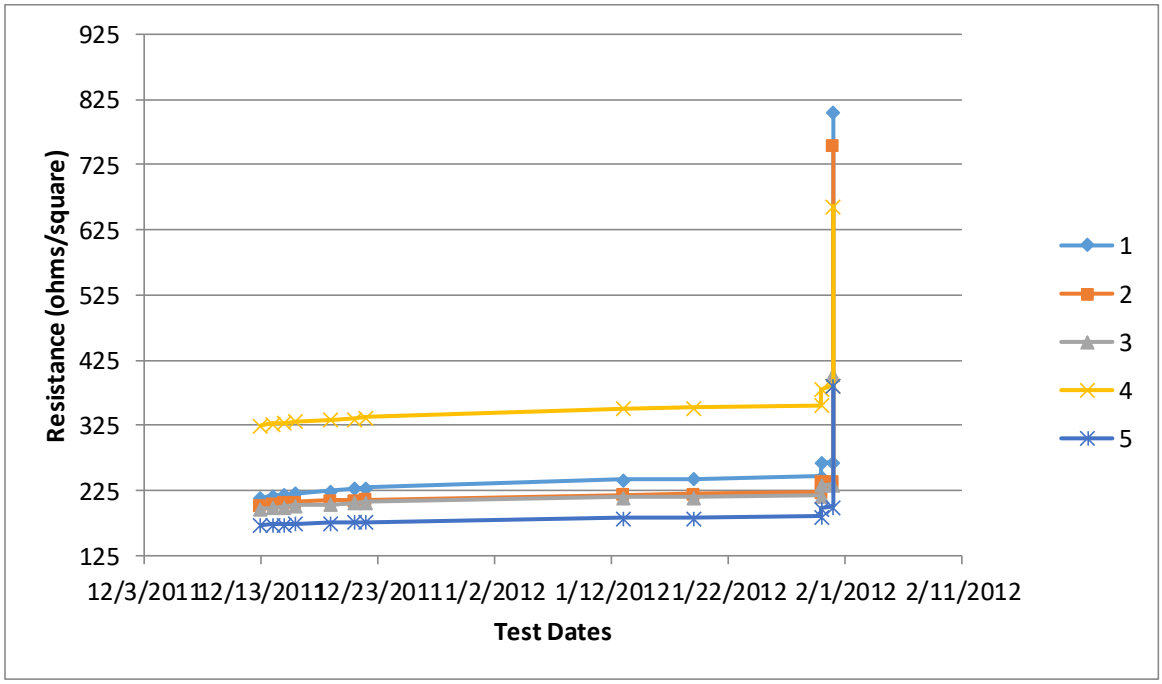

Fig. 3.1 Resistance rise of large area HEB chips over time exposed to O2 plasma

Interestingly, such resistance rise was not only seen to increase when the bare NbN HEB was exposed to an O_2 plasma but it was also seen to increase even when the NbN was protected by a Au capping layer. Though, in some cases, Au capped NbN did not rise as much as bare NbN as shown in Fig. 3.2. Chip 6 had a bare NbN HEB kernel (a Au wet etch was used to remove the Au) whereas Chip 10 had the ~ 20nm Au protection layer still present (again, no Ge capping layer). Both chips were placed in a MARCH oxygen plasma system, on a cooled grounded electrode for four hours at 100W. Chip #10 in this experiment, even while covered with a Au film, demonstrated a modest though non-negligible rate of rise.,

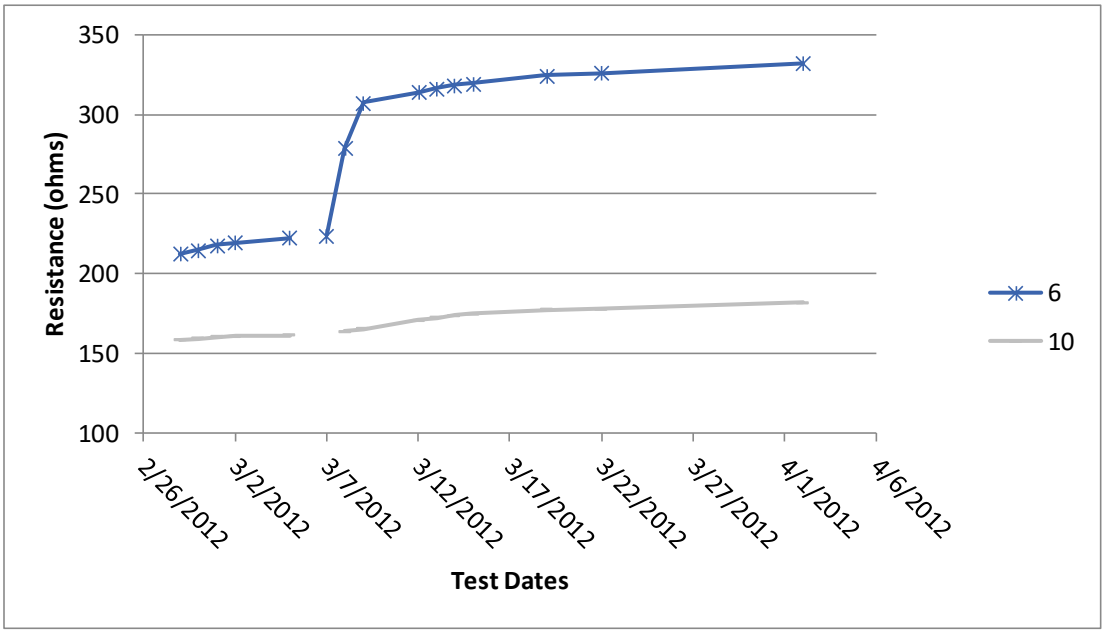

Fig. 3.2 Au vs. No Au Resistance Rise after 4 hour O_2 plasma. #6 had a bare HEB kernel while #10 had a Au protection layer over the NbN HEB kernel.

However we did observe Au protected HEB's with a significant resistance rise. Fig. 3.3 shows three test chips. Chip 8 was a bare HEB chip exposed to an O_2 plasma for 5minutes at 100W. This HEB did not have

a significant resistance rise and very little rise over time. This may be due to the very short O_2 plasma exposure. Chip 6 was a HEB with a 20nm Au protection layer. This chip was exposed to a 4 hour O_2 plasma followed by a Au wet etch. The chip had a significant rise over time starting at 143Ω and ended up at 329Ω after six days. #3 only had a Au wet etch done to remove the Au protection over the HEB. Chip 3 was acting as a control to see if the Au wet etch was affecting the resistance rise. Measurements of sample 3 were taken before and right after the wet etch and the resistance did not change. Only after testing it again four days later was the increase seen. This rise could be due to oxidation of the now exposed NbN. As can be seen in the graph, the rate of rise between chips 6 and 3 are different with 6 having a rise rate twice as fast as chip 3.

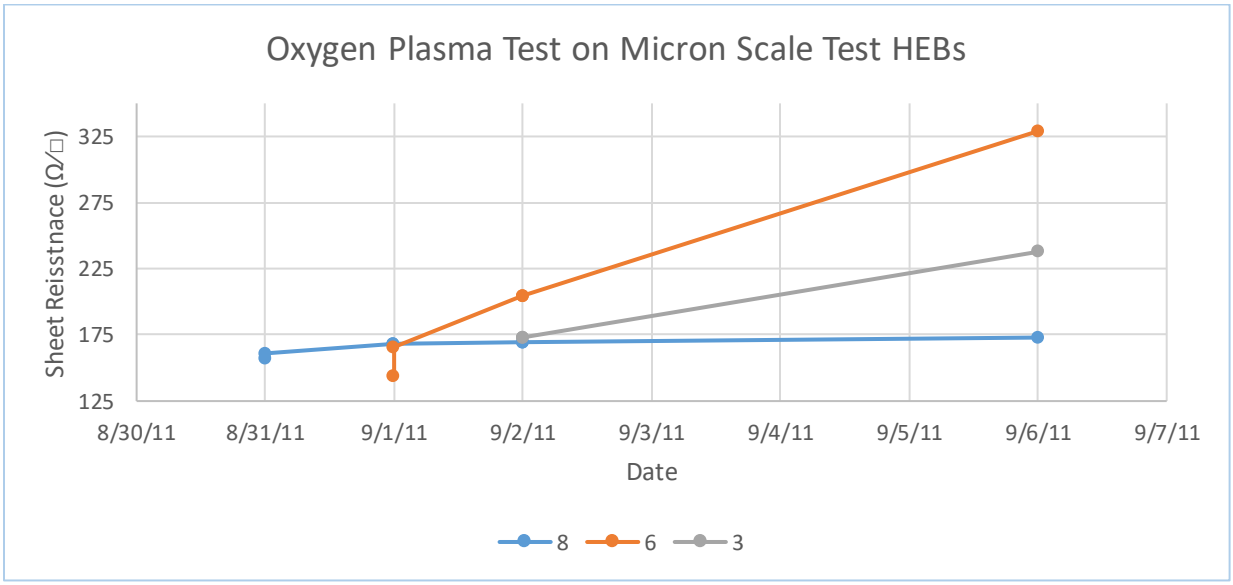

Fig. 3.3 Resistance of three NbN test chips. #8 was a bare HEB exposed to an O2 plasma for 5minutes at 100W, #6 was a HEB with a Au protection layer that was exposed to a 4 hour O2 plasma at 100W followed by a Au wet etch. #3 only had a Au wet etch.

It would seem after this experiment that the Au wet etch may also be causing the resistance rise over time phenomenon. However, other Au wet etches were done which did not show a correlation with the resistance rise and the wet etch. As just one example, in Fig. 3.2 chip 6 had a Au wet etch preformed on the date of the initial point on the chart and the increase in resistance was relatively small with only about a 2Ω gain per day for the next several days until subjected to the O_2 plasma.

With plasma being a known issue with regard to resistance rise [7] [20], several steps were changed in the process so as to minimize or eliminate the amount of plasma that the samples would encounter. However, it seems impossible to remove all of the required plasma etch steps. In particular the Ti-line process requires the hours long oxygen plasma etch during the step shown in Fig. 3.0c.

Chapter 4: Investigation Into the Resistance Rise Phenomenon

In the previous chapter, we went over the Ti-line HEB fabrication process and also touched on the resistance rise issue that was plaguing the HEB devices. In this chapter we will look at our investigations into determining the possible cause or causes of the rise and also some ideas for resolving the issue. During the investigation of the resistance rise phenomenon, "large area" HEB chips (where HEB sizes were on the order of microns rather than nanometers) were used in order to quickly test various HEB fabrication steps to help find the cause of the resistance rise. The HEB dimensions for these large-area chips have lengths of 4μm and widths being between 10 to 20μm. In contrast, the actual 1.6THz HEB devices have a length of 0.2μm and widths between 4 to 8μm.

With completed Ti-line device chips having much higher than expected resistance and with the resistance rising over time, it was necessary to figure out how to stop this problem. Since it was not known which processing step or steps was causing the resistance rise, several hypotheses were tested while taking into account previous work by others who saw similar phenomenon [5] [7] and work by groups who successfully made NbN HEBs [10] [14] [21]. Numerous changes in the Ti-line process were tried such as using different resists and changing etch times. Unfortunately no solution was found by just altering Ti-line steps. There were two main obstacles with using the Ti-line process for finding the cause of the resistance rise. One was that the process was delicate and time intensive. The entire process would have to be finished and complete chips realized before a resistance test could be done.

The second problem was that there were many different steps involved in the Ti-line process, hindering our capacity to test individual processing steps. While most of these steps could be altered, many could not be removed entirely from the process such as the long O_2 plasma etch step used to suspend the Ti-line. Fortunately, the large area HEB chips allowed us to more quickly fabricate HEBs and also allowed more flexibility in testing various fabrication techniques to prove or disprove the various processing steps.

During the investigation of the resistance rise, the large area test chips (see fig. 4.0 for an example of that layout and fig. 4.1 for a close up image of the HEB test device) were often fabricated using liftoff methods, instead of the customary plasma etching processes. These chips will be referred to as liftoff-chips in subsequent discussions.

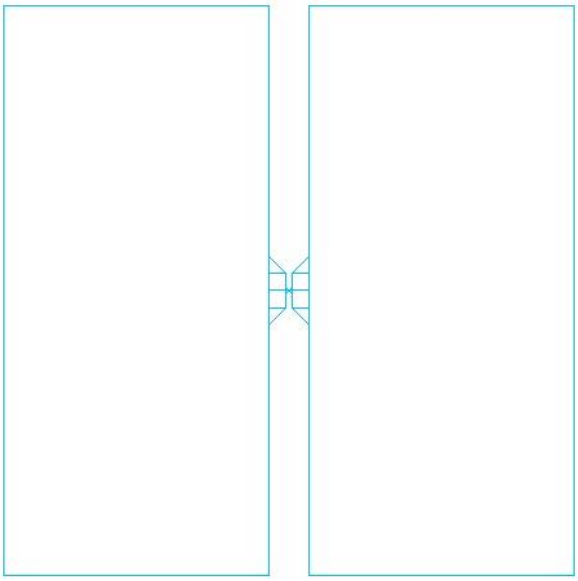

Fig. 4.0 Large Area Test Device. The two large rectangles are contact pads with the center area having the HEB.

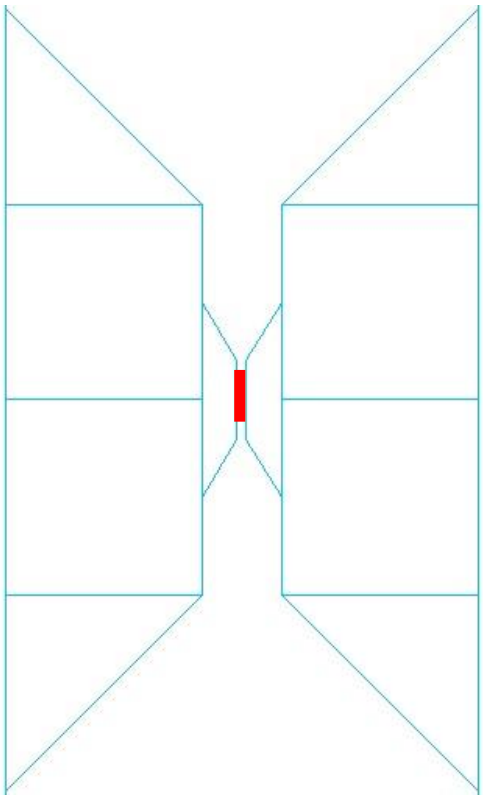

Fig. 4.1 Close up of the center of the large area test device. The red rectangle denotes the actual HEB device.

This lift-off method for one allowed us to fabricate HEB devices and test various aspects of the Ti-line process such as bake temperatures, wet chemical etches, dry etches, etc. while avoiding many other process steps that are intrinsic to the Ti-line process.

The basic outline of the liftoff process for fabricating the large area test chips are as follows: The process usually begins with a bare NbN on SOI wafer (the process also works with a little variation if a thin Au layer is already on the wafer. This is explained later). The sample is baked on a hot plate for 5

minutes at 130^{o}C. nLOF 2035 resist is then spin-coated over the sample at 3krpm for 30 seconds. The resist is then UV exposed with the proper mask. The exposed resist is baked on a hot plate at 110^{o}C for 1 minute and developed in 300MIF developer solution for about 2.5 minutes. The sample is again baked on a hot plate at 90^{o}C for 1 minute and loaded into a sputter deposition tool to deposit 200nm of Au perpendicularly onto the sample surface. It was necessary to do a 2 minute, 150V beam voltage, ion clean just prior to Au deposition to insure a good electrical contact to the NbN film [24]. Without the ion clean the sheet resistances would be in the kilo-ohms-cm range. The resist is lifted off in 300T stripper heated to 80^{o}C for 1hour. E-beam evaporation of Au was originally tried instead of the sputter deposition, since evaporation generally gives superior lift-off results compared to sputtering. Unfortunately the adhesion of the Au to the NbN was not good in the evaporator compared to sputter deposition as the Au would peel during the lift-off (the only time evaporated Au should be done is when the evaporation is done over another Au layer such as the thin Au layer). In the few tests that were done, Au evaporated on a sample (without an ion clean) gave resistance values of between 3k – 7kΩ while a sputter deposition run without using an ion gun clean gave resistances between 1.8k – 2.2kΩ. The rise in resistance over time was about 2% over a 24 hour period for both. When the ion gun clean was used prior to sputtering the Au onto the sample, the resistances started out much lower. Back to the processing steps, after the lift-off a resist such as AZ4110 is used to define the HEB width. A NbN RIE is used to etch the sample defining the HEB. The tool used is an Oxford PlasmaLab System 100. The etch recipe uses gas flows of SF_6=25sccm, CHF_3=20sccm, RF Power=20W. The temperature is set to 10^{o}C, and

a chamber pressure of 10mT, the etch time is about 1minute 40seconds. After the RIE etch, the width defining resist is removed in a liquid stripper such as acetone or NMP. The first successful sample done with this basic method rendered a resistance of 164Ω and after seven days increased by only 1Ω. Since this lift-off method was a successful test process it was dubbed the "Landmark process". Subsequent tests confirmed the Landmark results and allowed us to test various processing steps "beyond" the Landmark process.

With this Landmark lift-off method, many variations can be done to run different tests or work with different parameters. As alluded to previously, if the initial sample had the thin in-situ Au already on the NbN surface, or if deposition of thin Au was desired, the process could be altered to accommodate. In this case the thin Au would be deposited onto the NbN surface followed by the LOR lithography. The 200nm thick Au would then be deposited followed by the LOR lift-off. From here the thin Au could be wet etched away and the width lithography can proceed in the usual manner. Another option is to do the width lithography on the thin and thick Au covered surface. After this lithography the wet etch of the thin Au would be done followed by the NbN RIE etch. The resist would be removed followed by another Au wet etch to remove the thin Au which was masked by the width defining resist.

Before moving on, there are two points to note about this process. The first is that an Ar ion clean was used to pre-treat the Au surface before any Au wet etch. This is done instead of using an O_2 plasma. Normally, without the O_2 plasma pre-treatment of the Au surface, the Au does not clear off the wafer well and can leave residual Au on the surface. Using the ion clean showed to be an effective

substitute to the O_2 plasma pre-treatment. Also since in other research ion milling is used to fabricate HEB devices with negligible changes to the material parameters it was seen as a viable alternative to try [19] [20]. The other variation was to soak the sample in 300T stripper at 80^{o}C for 1 hour for the liftoff step. This was used instead of NMP for a cleaner liftoff result. Along with the 300T, sonicating the sample in a beaker of Ethylene glycol for 10 seconds and placing back into 300T aided the lift-off and cleaning of the surface in comparison to using 300T alone. The reason for using 300T and trying to find a robust wet cleaning solution was to remove the need to do an O_2 plasma cleaning.

With the Landmark low resistance process in hand, various tests on these devices were run. Since there were multiple chips per wafer, some of the samples were split in two by using a diamond scribing tool so that different tests could be done with chips of similar characteristics. One such wafer that had the Landmark process, M4466 (this wafer half was described a bit in chapter 3 and shown as fig. 3.1), was a half wafer SOI/NbN/Au (the wafer was ordered to have in situ deposited Au deposited on the NbN). The other half, M4474, had the in-situ Au capping layer removed with a wet etch and was placed in a sputter deposition system to ex situ re-sputter the Au. This was to test whether the in situ deposited Au is necessary for low resistances. With the Au removed from M4474 and after it was cleaned, the sample was placed in a sputter deposition system and given an ion gun pretreatment clean for a duration of two minutes at 150V. This was followed by a 200nm Au deposition. From this point, the regular Landmark process was performed on both samples. In comparing the two samples, they both had low resistances with an average around 200Ω. The percent increase in resistance was also low at

about 1% or less per day. After 36 days the resistance for M4466 (in situ Au) increased by an average of 25Ω per chip. M4474 (ex-situ Au) that saw no treatments post fabrication also rose over time slowly. After 67 days the resistance only rose an average of 37Ω.

It was theorized that the oxygen plasma was the critical process causing high resistance, and resistance rise. As a preliminary test, sample M4466 was baked on a hot plate at 190^{o}C for 5 minutes to check the effect of temperature. This bake increased the resistance by about 15 – 20Ω. The next day the rise leveled off only increasing 1-2Ω. Seeing that the bake did not dramatically increase the resistance or cause a continual significant resistance rise. The wafer was next subjected to a 100W O_2 plasma for a duration of 2 hours. This plasma treatment significantly increased the resistance by 200-500Ω, depending on the chip. Another sample was fabricated where 10nm of Au was sputter deposited onto a NbN on SOI sample. An NFR + nLOF2020 bilayer structure was used for the circuit patterning layer. This was followed by a 200nm Au evaporation (this evaporation was depositing onto the thin Au layer. The issue of peeling Au is when the Au is evaporated directly onto the NbN). The bilayer was lifted off in NMP. Next the wafer was cleaned for 15minutes in an O_2 plasma at 100W. Width patterning was done in the usual manner followed by another 5minute O_2 plasma clean. The resist was stripped in acetone and the sample's NbN was etched in an RIE with a final 10second Au wet etch. The resistances were over 1kohm with a rise of 4-8% over 24hours. After 3 days the rise was up at around 10% overall. This experiment was significant since the areas where the HEBs are had Au covering them during the entire processing time.

Since the O_2 plasma is a major player causing the resistance, experiments were performed to see if the Ti-line process could still be realized with modifications that would eliminate the use of the O_2 plasma in the processing steps. The first thought was to find a wet etch that would selectively clear away the polymer under the Ti-line in the same way that the plasma does. A photo-sensitive lift-off resist, LOR 10A, was used instead of the bilayer of LOR 5B and polyimide. Aside from this organic layer difference, the only other major change to this revised Ti-line process was that a wet etch would take the place of the O_2 plasma etch or to significantly reduce the amount of O_2 plasma that the wafer will see. This wet etch, however, proved to be a very delicate process due to the fact that the Ti-lines are very thin- being on the order of 200nm in thickness and having a length of around 6µm. Fig 4.2 is an example of a fully formed Ti-line fabricated using the normal Ti-line process.

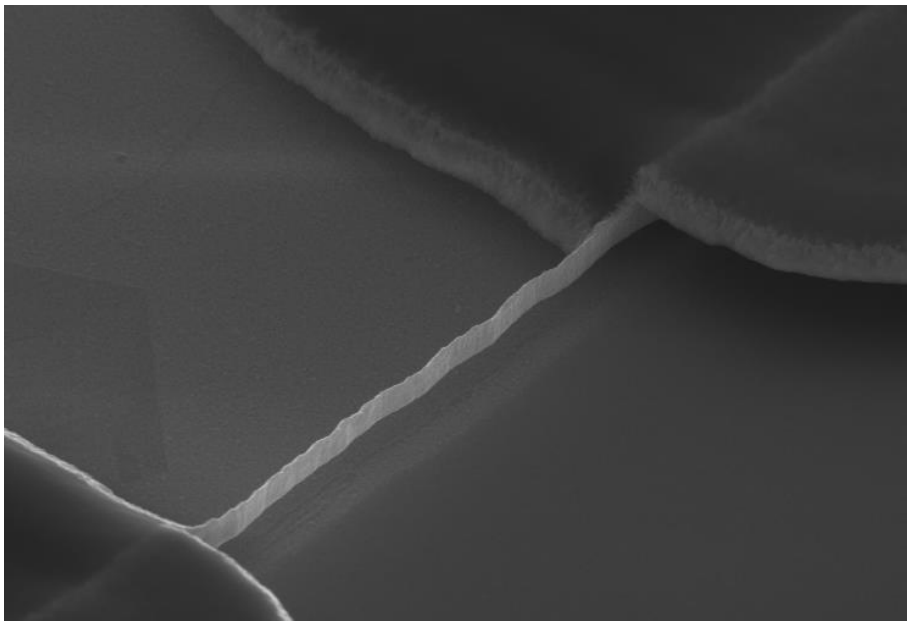

Fig. 4.2 Fully formed "Ti-line"

The LOR 10A etch consisted of a careful soak in a beaker with an AZ 400K:DI water solution. It was imperative to move the sample slowly when removing it from the solution after the allotted etch time to prevent the Ti-lines from breaking. Also, drying the sample was done by basically letting the solvent evaporate with a very light "breeze" of nitrogen blowing adjacent to, but removed from the sample. This process was repeated if the area under the Ti-line was not cleared of LOR. Once the sample is satisfactorily clean, it is placed in a vacuum chamber for ion-cleaning since there was always some amount of residue found on the surface after the above LOR etch process. This consisted of a low energy 150V ion clean for a duration of 20 minutes. After this point the sample is basically back to the normal Ti-line processing scheme. Unfortunately, this approach was abandoned as most of the Ti-lines would break or buckle as the "anchor" areas would move and dissolve (fig. 4.3).

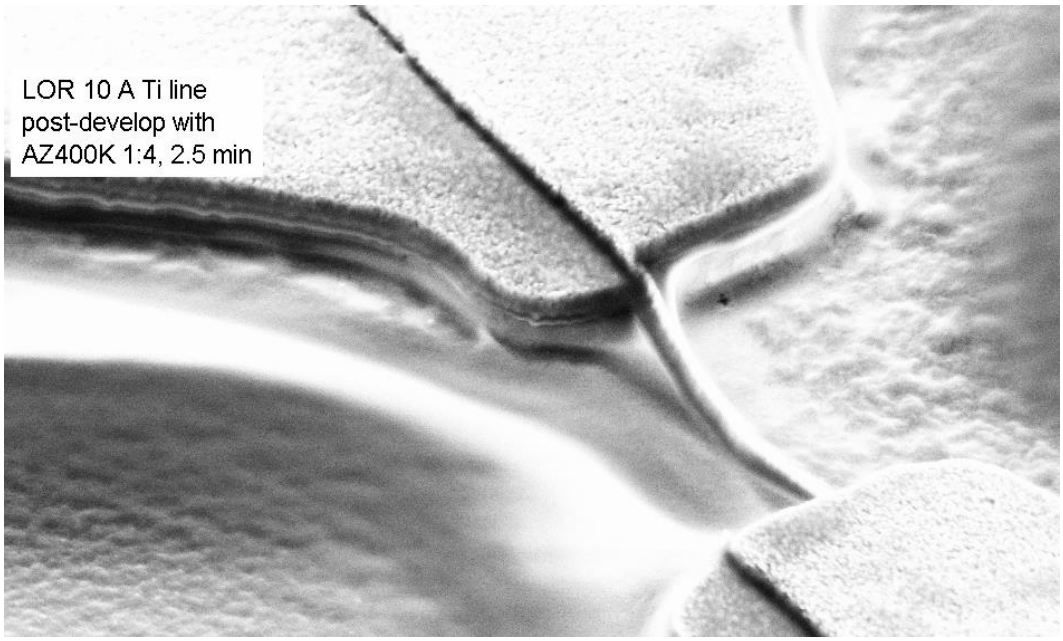

Fig. 4.3 Ti line damaged after AZ400K etch. Note the sample is not cleared of LOR yet.

The only way to prevent the anchors from moving was to bake the LOR at a higher temperature, 190^{o}C, instead of the lower 160^{o}C bake. The resulting issue that arose, however, is twofold. The first is that we have already established that such a high temperature back will cause the NbN sheet resistance to rise. The other and more significant problem is that the LOR becomes much more difficult to remove with the higher temperature bake. 300T resist stripper was tried as well as ion cleaning. Unfortunately, a fully and properly cleaned surface was not obtainable (fig. 4.4). And many of the Au pads that were evaporated on the sample were torn from the sample. Of the devices that were successfully built, the resistance was still too high with values 5-10 times higher than predicted.

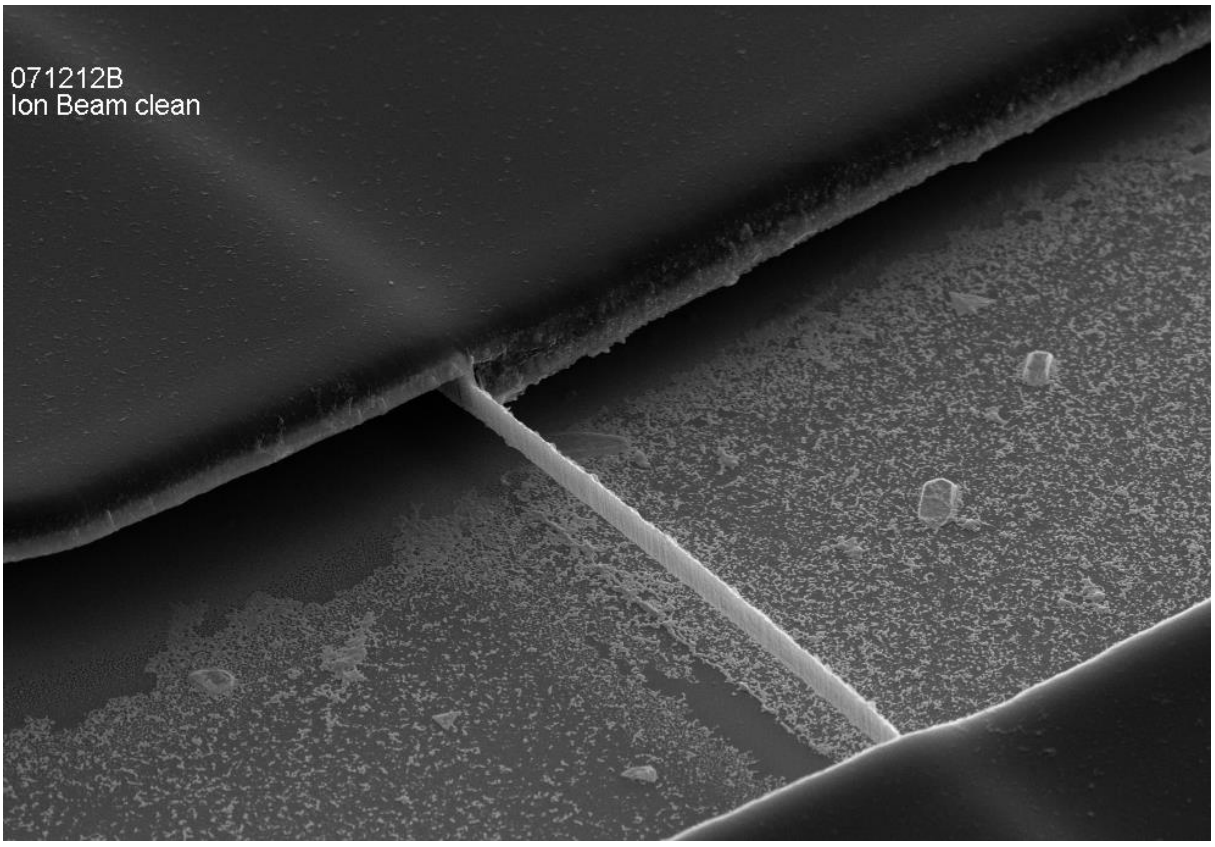

Fig. 4.4 Residue after LOR Ti-line processing and Ion gun clean of surface.

At this point the old RAITH 50 e-beam lithography system was considered for fabricating HEBs, though considerable work was needed to get the system up and running (it had never been used regularly and was inoperable at the time). With no apparent solution to be found to resolve the resistance rise issue while still using the Ti-line process, it was determined that all efforts should be diverted from the Ti-line process to finding an e-beam solution. This would also entail altering the current HEB mask set to accommodate e-beam steps and vice versa.

Chapter 5: Electron Beam Lithography HEB Fabrication Process

Electron beam lithography is currently the standard method used for fabricating nanometer size HEB devices. With that said, Dr. Jonathan Schultz was able to devise a method, called the Ti-line process, for making Nb HEBs at the University of Virginia using only optical lithographic means. Unfortunately, as described in chapters 3 and 4 of this dissertation, NbN is sensitive to some of the Ti-Line processing steps and we have been unable to realize working, stable HEBs using the Ti-Line process. This problem compelled us to use e-beam to attempt the NbN HEB fabrication. Since e-beam is a direct-write process, it is inherently slower than optical lithography. With this in mind, a hybrid e-beam/optical lithography process was developed, using optical lithography where practical. This combined use of e-beam and optical patterning is not a novel concept and is used by other groups as well [10] [19] [22].

Two fabrication schemes requiring two mask sets, were devised to explore this hybrid e-beam/optical lithography approach. It should be pointed out that the current e-beam lithography tool at UVa is an old system and does not have the precision, speed or reliability that a newer or better kept system would possess. The E-beam system at the University of Virginia is a Raith Quantum which was an upgrade on the Raith 50 electron beam lithography tool. Even before this, the e-beam tool was originally an FEI/Philips scanning electron microscope that was converted by Raith into the Raith50. The software and motor controllers were the main points upgraded with the Quantum package. This was to allow the system to have a faster writing speed along with other various tools and upgrades to the software to enhance accuracy and reliability. Despite the major software upgrade, the tool has seen several minor and major repairs over the years. With that said, the system does not have a high resolution beam. Most e-beam systems are able to easily resolve 20nm feature sizes and in newer tools, depending on the resist used, 5-10nm. This system was originally supposed to be able to resolve features down to 50nm (best case scenario). However, the system currently has difficulty obtaining 200nm wide features.

300nm line widths seem to be the smallest linewidth that the system can regularly resolve using the standard PMMA process.

In regards to the two processing methods, in most respects they are very similar to each other in that most of the masks are the same and can be utilized for either method. However, there are some major distinctions that are described below. One of the main differences is in the amount of e-beam writing between the two. Though both are conceived to use a minimal amount of e-beam processing, they have much different write times due to the difference in the amount of writing area. The first method which will be called the ("Trench") technique requires only sets of thin 200nm wide by 6um to 12um long lines. The second ("Liftoff") technique has a much larger pattern to write as will be described later. The other major difference is with one of the optical mask layers where the two distinct e-beam designs require two variations of the Microstrip mask. With that said, the rest of the optical lithography masks are the same for both methods. In this chapter we will go over some of the basics regarding e-beam lithography. We will also delve into the two different approaches devised for accomplishing the same goal of fabricating HEB chips.

Electron beam lithography (EBL) is a lithographic method which uses electrons instead of photons to expose resist since the wavelength of an electron is much smaller than that of a photon. EBL will be used to fabricate the critical nanometer HEB feature while optical lithography will be used for the remainder of the device. The standard method for creating a thin trench in e-beam resist is to use a positive, electro-sensitive resist such as PMMA (Polymethyl methacrylate) and expose it with a calibrated beam of electrons. In order for the beam to be as small as possible, the system needs to be calibrated for several factors else the beam may be too large in diameter or misshapen when it strikes the resist. The Raith EBL at the University of Virginia is a relatively old system where most of the

alignments and calibrations need to be done manually. Fortunately, those calibrations only need to be done periodically.

In the first "Trench" fabrication method, a thin open "trench" is exposed in resist and developed. This trench is in the region of the device of the intended HEB. The length of the trench is not of too much consequence. However, the width is the critical factor and necessitates the 200nm feature size for the HEB. This basic approach is one of the two e-beam HEB methods devised for this thesis. The second method, which will be referred to as the "Lift-off" was conceived since the Raith e-beam system is an old model which doesn't reliably resolve thin line features. In this second method, two adjacent but separated regions are exposed and developed so as to leave a thin line of resist between the opened areas. This raised nanometer wide resist feature would act as a lift-off mask for subsequent processing steps and would be the region where the HEB would be located.

The two fabrication processes for creating HEB devices will next be described in detail. Both methods begin with a NbN sample wafer consisting of a SOI (Silicon On Insulator) handle layer with a 3nm NbN layer deposited on the SOI through magnetron sputtering. On top of the NbN 20nm of Au "thin Au" is present to cap and protect the NbN from oxidation and ESD (electro static discharge). This layer will also serve as a seed layer for Au plating. This capping "thin Au" could be deposited in situ of the NbN run, or it could be deposited after the NbN deposition in a separate vacuum step. The majority of the wafers processed were obtained from the Moscow State Pedagogical University in Russia and had Au in situ deposited on the NbN surface. We also acquired SOI/NbN test samples from Nanjing University, China

TRENCH APPROACH

The first method we will go over is the "Trench" method. This starts with the above mentioned wafer of NbN/Au. A negative lift-off resist (nlof 2035) is spun on and the "microstrip" optical lithography

mask (fig. 5.0) is used to define the main device bodies (cad shown in fig. 5.1 where a dark pattern mask was used) along with several other features and devices such as alignment markers (both optical and EBL) and larger test devices. After the resist is patterned and developed, the wafer is placed in an e-beam evaporation tool to deposit 200nm of "device-layer" Au. After the deposition, the resist is lifted-off and the device-layer Au patterns are left on top of the "thin Au" layer.

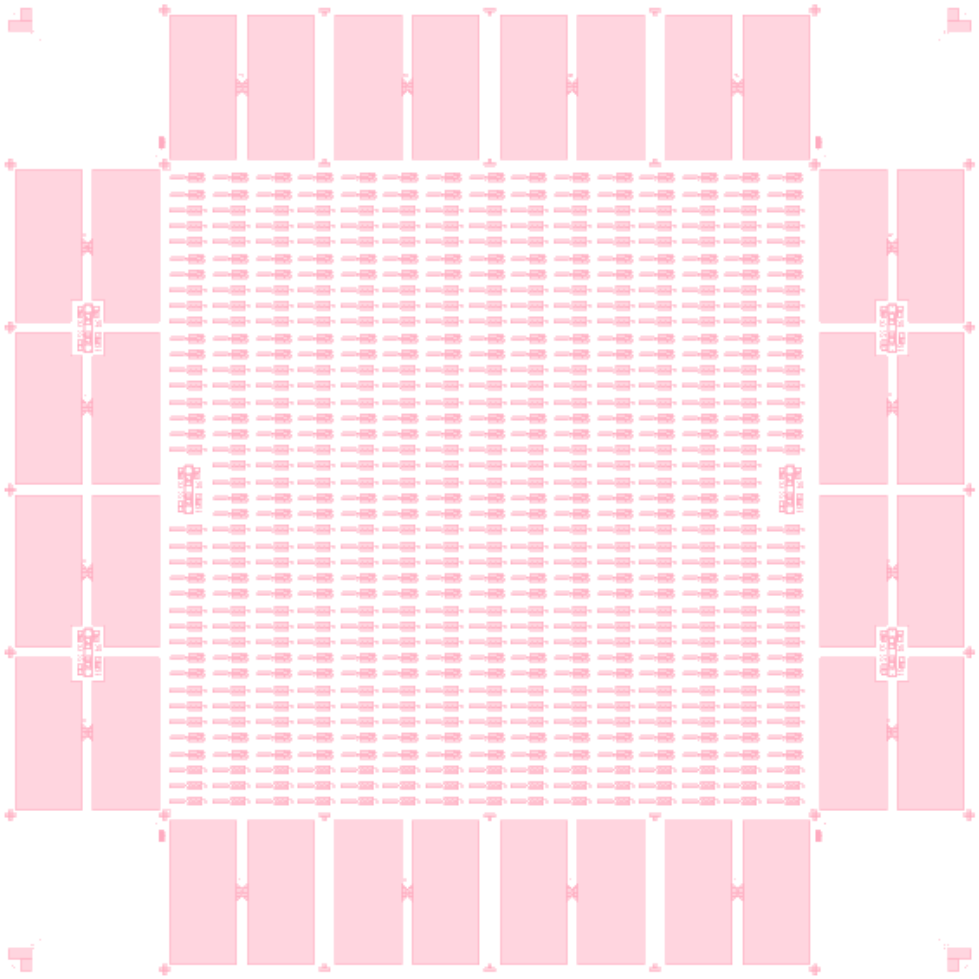

Fig. 5.0 Optical lithography microstrip layer mask, overall view. The pink areas are where the resist is developed away and where the device-layer Au remains after the evaporation and liftoff.

Fig. 5.1 Two device design variants. The small crosses are EBL alignment markers.

The next step is to build up the beam leads using electroplating (fig. 5.2a & b). This is another reason for having the in situ thin Au layer where the thin Au acts as the plating seed layer. A positive resist (AZ4330) is spun on to approximately 3.5um thickness and optically exposed with the beam-lead mask (cad shown in fig. 5.3 where a clear pattern mask was used). After development the Au is plated up to about 2.5um followed by a resist strip.

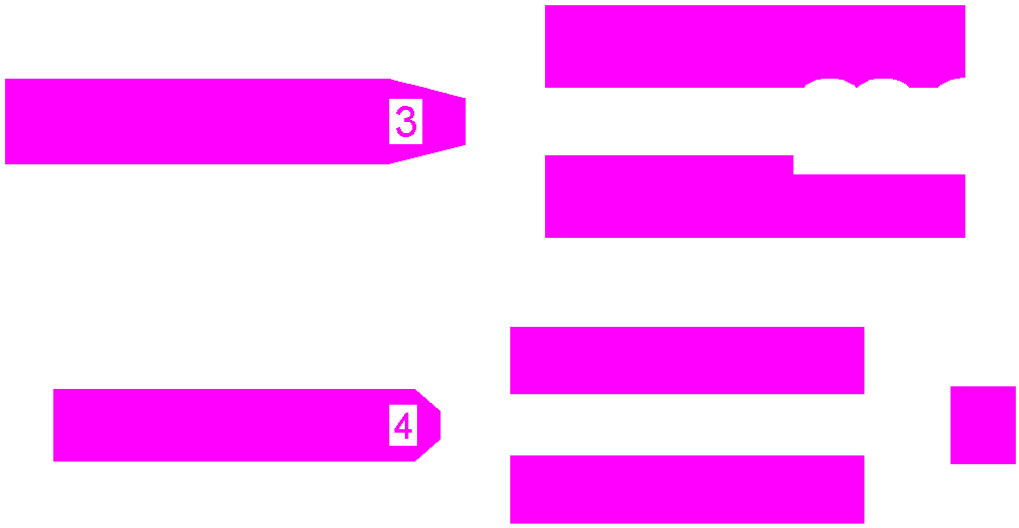

Fig. 5.2a Device beam lead layer.

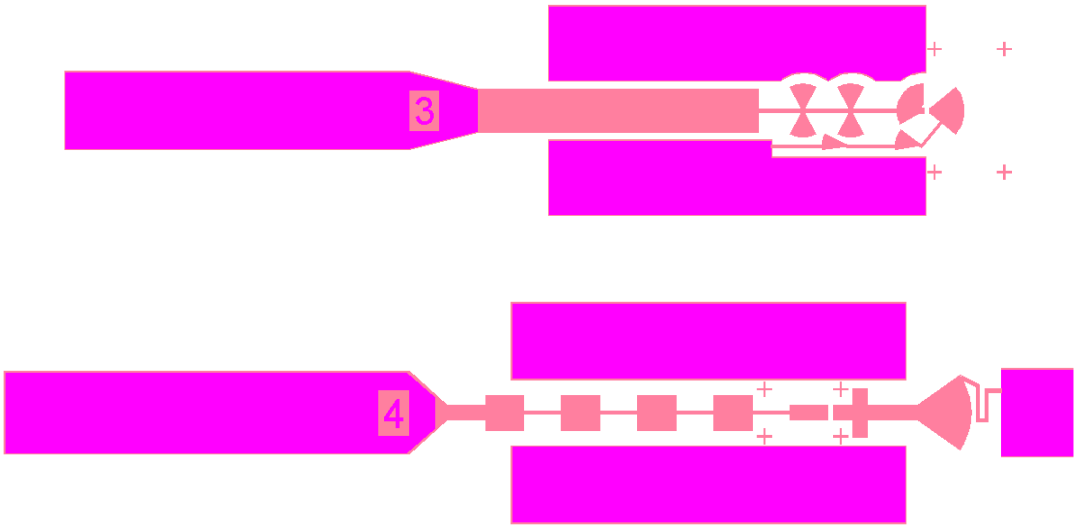

Fig. 5.2b Beam lead layer over the microstrip layer.

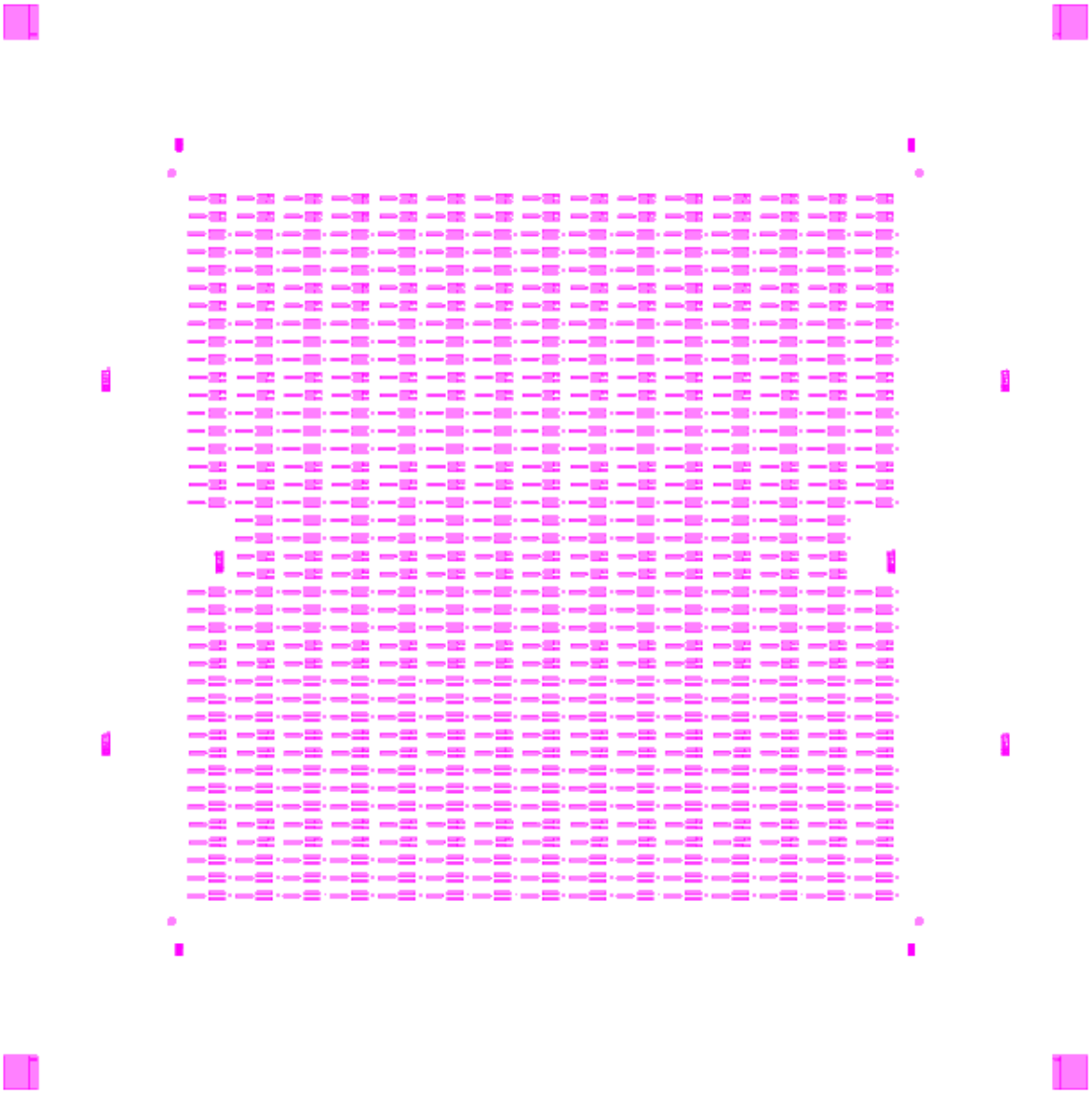

Fig. 5.3 Overall beam lead mask design.

With the beam leads complete, e-beam PMMA (polymethyl methacrylate) resist is spun on for the subsequent electron beam lithography process. With the layer of PMMA resist applied, the sample is loaded into the EBL vacuum chamber. Using the digital GDS2 mask, the e-beam layer pattern is written into the PMMA and developed to form a trench with dimensions of 200nm x 6µm or 12µm (depending on the device) Fig. 5.4. This is where the HEB device will eventually be formed. An iodine based wet

etch, HG-800, is performed on the sample removing a thin strip of Au (trench area). At this point the PMMA resist is stripped and the wafer is ready for the HEB kernel width patterning.

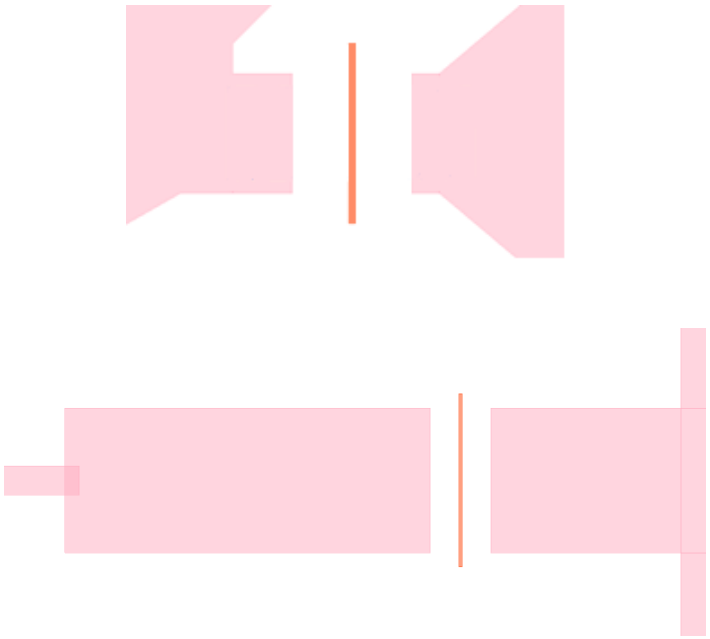

Fig. 5.4 E-beam exposed "Trench" area (Red lines).

The HEB kernel width is defined by spinning on a positive (non e-beam) resist, AZ 4330, and developing with the Kernel mask which covers over a portion of the previously defined trench in the thin Au (uncovered NbN), and a portion of the two separated pads of microstrip Au (Fig. 5.5). In the previous step, the e-beam wrote a ~200nm wide trench that defines the *length* of the HEB. The width of the HEB is nominally determined by the length of the trench. After the Trench step, the length of this 200nm wide trench is several microns longer than the device's actual size. The reason is that the following kernel step is optically aligned and would be very hard, if not impossible, to be in perfect alignment with the previously defined e-beam line if the length of the e-beam line was of the exact desired size. With the length of the e-beam defined trench being purposefully large, the kernel mask will be much easier to align with the sample since an acceptable amount of alignment error has been built-in.

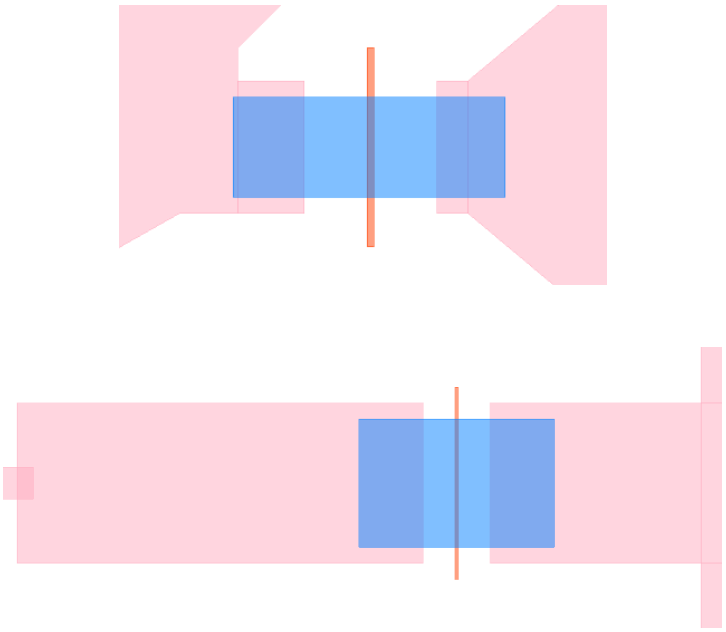

Fig. 5.5 Kernel mask layer (blue) across the microstrip (pink) and e-beam trench (red) layers. The HEB is the area overlapped by the kernel and trench layers.

After the kernel lithography, the uncovered thin Au is removed in another HG-800 wet etch revealing NbN not under the thicker device-layer (microstrip) Au or the kernel resist pattern. The uncovered NbN across the wafer can now be dry etched in a reactive ion etch (RIE) tool. We used the PlasmaLab System 100 by Oxford Industries. The etch chemistry consists of a flow of SF6 and CHF3 at 25 and 20sccm respectively. RF power is set at 40W, pressure at 10mT, and platter temperature at 10°C. The etch usually takes about 1minute with a minimal 10second over etch to ensure that the area is clear of NbN. Using the reflectometer on the RIE it is relatively easy to know when the NbN is etched and the Si is exposed. When observing the real-time graph of the surface reflectance the line shape will change to a sinusoid when the top layer of Si of the SOI wafer is being etched. Following this, the resist is stripped leaving a properly sized HEB Fig. 5.6 where the pink area is the thick Au, the yellow represents

the thin Au, and the blue strip between the yellow area is the NbN HEB kernel. The outer white area would be the first Si layer of the SOI wafer.

Fig. 5.6 A close-up diagram of the HEB device before the addition of a capping layer. Pink: Thick Au, Yellow: thin Au, Blue: NbN.

Earlier in this thesis, it was stated that previously fabricated Nb HEBs were capped with Ge to help prevent the Nb material from increasing in resistance over time [5]. Given that concern, a Ge capping mask was developed to allow for a protective Ge cap over the HEB device if necessary Fig. 5.7.

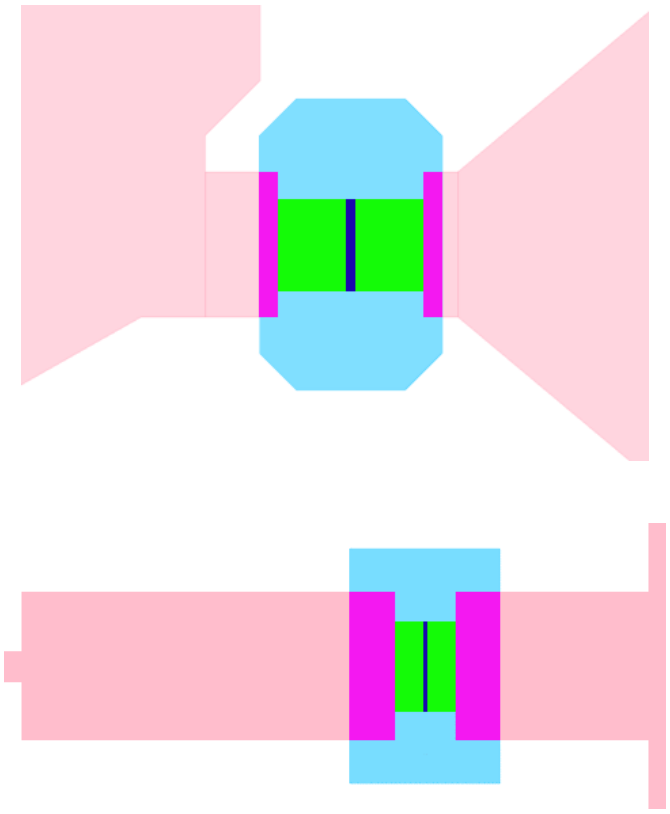

Fig. 5.7 Area of Ge (translucent blue) for capping over the HEB.

Finally, an Extents mask layer is used, in a backside process, to define the geometry of the thin Si chip (as outlined in Appendix B. The backside process is a method of thinning the chips by etching away the thick Si handle layer and the oxide layer of the SOI wafer. After which the Extents layer mask allows for the creation of a protective resist layer over the main device circuit elements Fig. 5.8 and 5.9. With this protection the rest of the thin Si can be etched away using reactive ion etching. This etch also reveals the Au beam leads that are anchored to the Si chip but also extend beyond

Fig. 5.8 Extents pattern for backside processing. Note, extents patterns are not limited to rectangular geometries

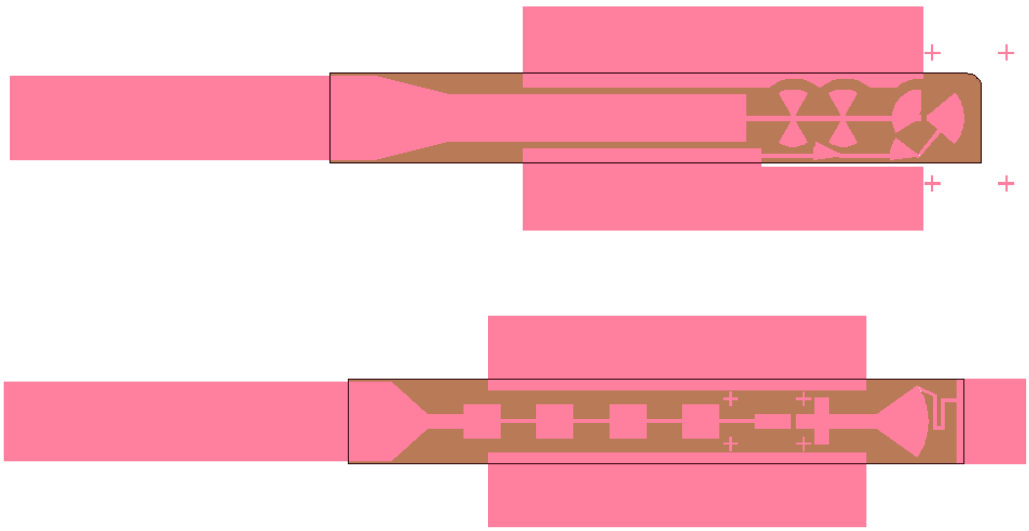

Fig. 5.9 Extents pattern (brown) shown below the microstrip layer (pink). The black outline shows the borders of the extents pattern and is not actually a design element.

LIFTOFF APPROACH

The next mask set, referred to as "Liftoff", differs from the previously described "Trench" mask set by one Optical mask and the e-beam pattern. This mask set and process was made primarily in case the "Trench" method, described above, failed i.e. the e-beam was not able to resolve a small enough open line. Since most of the process is the same for both masks, only the differing portions will be detailed.

To begin, the geometry of the devices in the microstrip layer are different between the two methods. In the Liftoff process, there is a larger portion of the final circuit "missing" in the microstrip mask compared to the "Trench" process (Fig. 5.10). This missing circuit portion will be created during the e-beam stage of the process. Aside from the physical difference between the two microstrip patterns, all of the basic processing steps are the same as the "Trench" microstrip process.

Fig. 5.10 The top two devices are the Lift-off version while the bottom two are of the Trench version (Copy of Fig. 5.1 for comparison).

The next difference is in the e-beam step (the beamlead step previous to this e-beam step is the same for both processes). A resist layer is spun on which needs to be thick enough to work as a lift-off mask. The usual method for doing this with e-beam is to use PMMA along with a copolymer layer of MMA to bulk up the resist thickness as well as creating a "T-shaped" resist structure. This structure can be made by spin-coating MMA followed by PMMA and since the MMA dissolves faster than the PMMA

A resist structure with a PMMA overhang can be realized. This type of structure will also allow for an easier lift-off.

Once the resist is applied to the sample it is exposed with two closely spaced features by the e-beam and developed. The anticipated result is a solid 200nm wide line of resist between the now open (developed) areas. Next, approximately 200nm of Au is deposited via evaporation followed by a resist lift-off. This Au is the same thickness as the microstrip layer Au since we are creating microstrip device structures. (The microstrip layer in the "Liftoff" approach had large areas removed from the mask design, when compared with the "Trench" approach, to be created during the e-beam lift-off portion) The resulting geometry (ignoring the beamleads) is shown in Fig. 5.11. A close up of the e-beam portion is shown in Fig. 5.12 that reveals a thin gap created by the two separate regions developed by the e-beam lithography. This line will become the area where the HEB will be formed. After resist development, the thin unexposed area becomes a thin section of raised resist which separates the Au that is deposited, creating the short NbN HEB length needed between the Au contacts. Underneath this resist is the in situ thin Au. After the lift off, the thin Au between the thicker, 200nm, Liftoff Au is wet etched leaving the NbN exposed between the Liftoff Au pads.

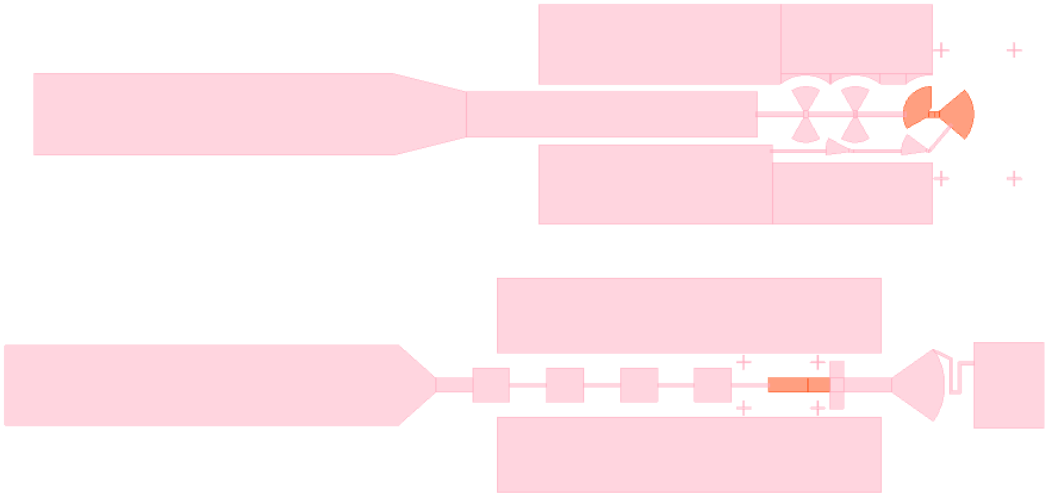

Fig. 5.11 E-beam area in red along with the device mask area in pink.

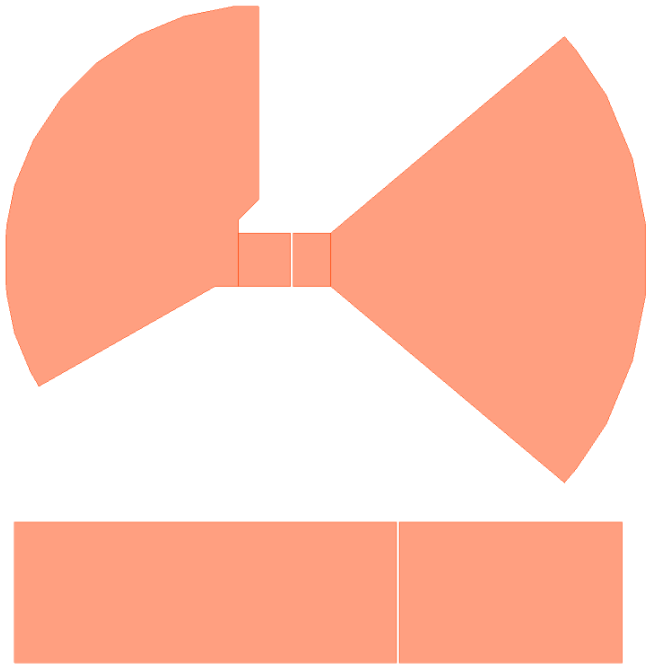

Fig. 5.12 Close up of the E-beam lithography portion.

At this point the next steps i.e. the kernel width, kernel protection, and extents are processed in exactly the same way as is done in the Trench processes.

Chapter 6: E-beam Process Verification and Future Work.

In this chapter we will go over some of the processing experiments that were conducted to verify if it was possible for the process to actually work at the University of Virginia with the tools at hand and in particular the e-beam tool. Many of the steps in this process have been ported over from previously known and common fabrication methods used at the University of Virginia. Most of the steps and processes that will be detailed in this chapter will be those which are particular to this process. Some of the processing test samples were NbTiN and not NbN. This was done since NbTiN is more cost effective for testing purposes and has similar characteristics as NbN in that it can be processed using similar methods [26].

Microstrip Thick Au Evaporation Step.

As stated in the last chapter, the device begins life as a SOI wafer with 3nm of NbN and 20nm of a thin Au protection layer over the NbN. For the thick Au or microstrip layer processing, the wafer is spray/spin cleaned with ethanol followed by TCE (trichloroethylene) and finally methanol. The wafer is then baked on a hot plate at 110^{o}C for 3 minutes. AZ2035, a negative lift-off resist, is applied and spun on. The spinning was manually ramped up from 3krpm to 7krpm with a total spin time of 60sec. The sample was again baked on a hot plate this time at 100^{o}C for 2 minutes. From there the sample was UV exposed in an optical aligner for 35sec. with the device layer (microstrip) mask. A post exposure bake was done at 100^{o}C for 1 minute. Finally the sample was developed in 300MIF for 1min 45sec.

After the development of the resist, the sample is placed in an electron beam evaporation unit to deposit 200nm of thick Au. The target deposition rate was 2Å/sec. After the deposition the resist is lifted off in NMP (N-methyl-2-pyrrolidone) resist stripper. The NMP is at room temperature in a beaker with a stir bar spinning at 200rpm. The sample is suspended upside down on a Teflon basket in the NMP.

After the lift-off there appeared to be some residue on the sample surface around the edges of the evaporated Au. This residue appears to be an organic substance and probably the AZ2035 photoresist. Subsequent hours-long NMP soaks did not appear to remove the residue and a better lift-off recipe should be developed. However, since it is removable with a nominal O_2 plasma clean and that a very short plasma clean does not adversely affect the resistance rise of the HEB. A two minute O_2 plasma clean can be done if residue is observed on the surface. Au evaporation is a common enough process however the processing parameters for it were discussed since the mask has the e-beam alignment patterns which are important for the e-beam lithography step.

E-Beam Lithography

With the e-beam lithography layer. The sample is first given an ETM clean and can be followed by a 1 minute O_2 ash at 100W. This is then followed by a 110^{o}C hot plate bake for 2 minutes.

With regard to the PMMA application, normally PMMA is spun on a sample either by itself or above/below a copolymer such as MMA (methyl methacrylate). The MMA is useful for lift-off or creating T shaped structures being that MMA undercuts during development more than PMMA. MMA can also be used to simply increase the thickness of the resist stack. One of the issues with the e-beam process we encountered was that the resist was either not being fully exposed by the electron beam or that it appeared to be over exposed and the width of the line would be too wide, greater than 200nm though usually in the 300-400nm range. This would happen whether PMMA was used separately or in tandem with MMA. Interestingly, there were occurrences where 200nm and in some cases sub-200nm lines were developed using the Raith EBL. These tended to happen when the PMMA resist was spun on more than once. For example a double PMMA spin on was tried which yielded near 200nm width lines Fig. 6.1a & b and a triple PMMA spin on also resulted in the 200nm line width sizes Fig. 6.1c. The basic

processing for this resist layering was to have the resist spun on and baked, then have another layer spun and again baked, etc…

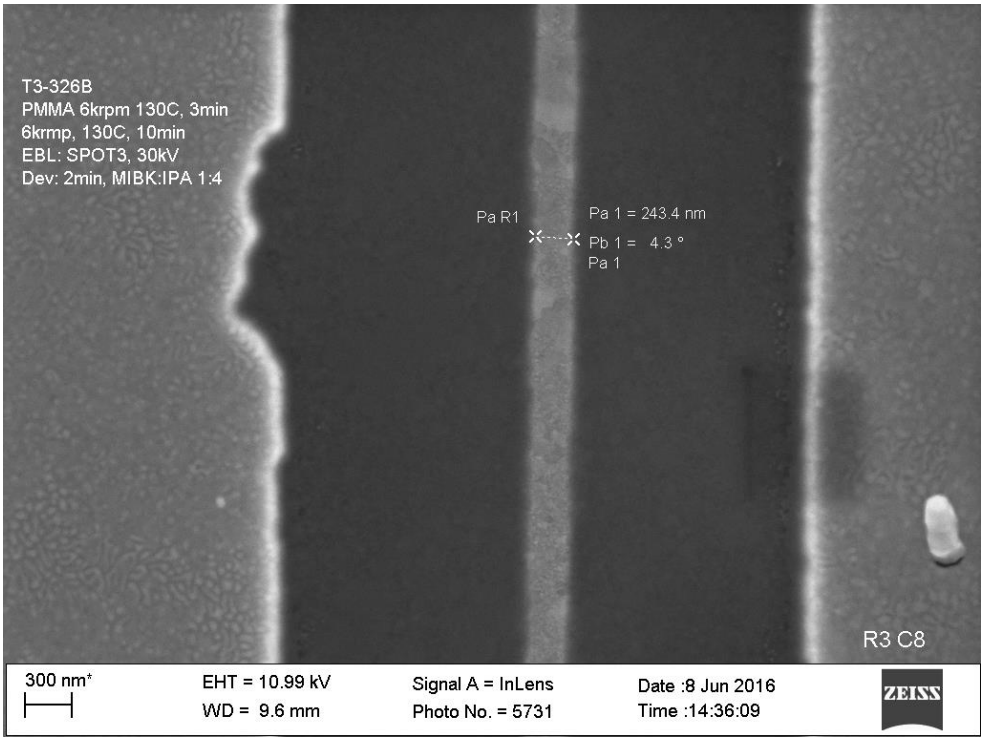

Fig. 6.1a Double PMMA Spin on resulting in a near but larger than 200nm width.

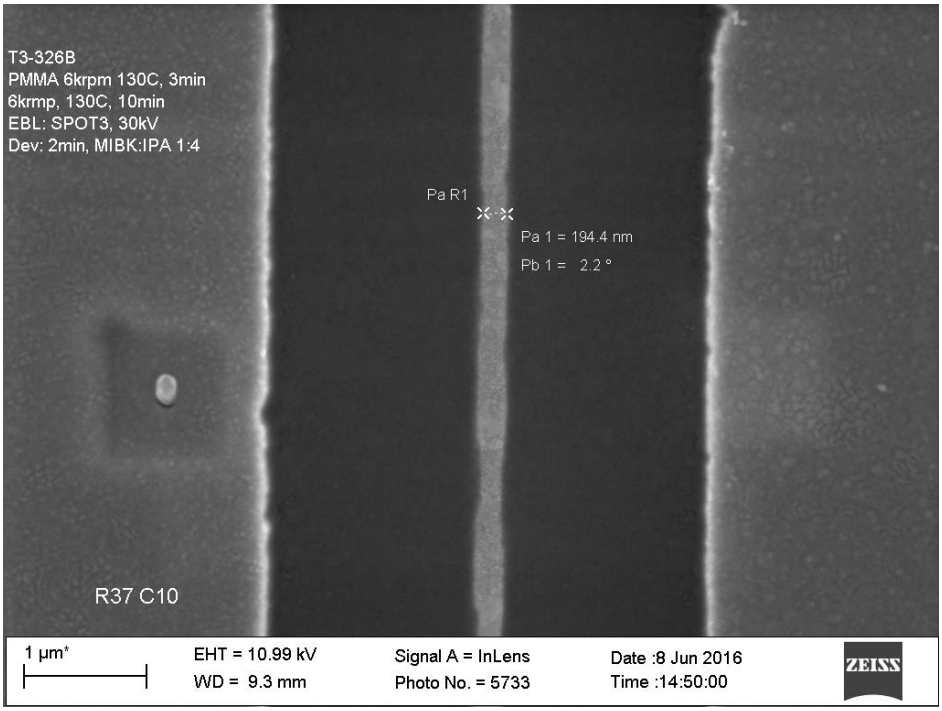

Fig. 6.1b Double PMMA Spin on resulting in a slightly smaller than 200nm width.

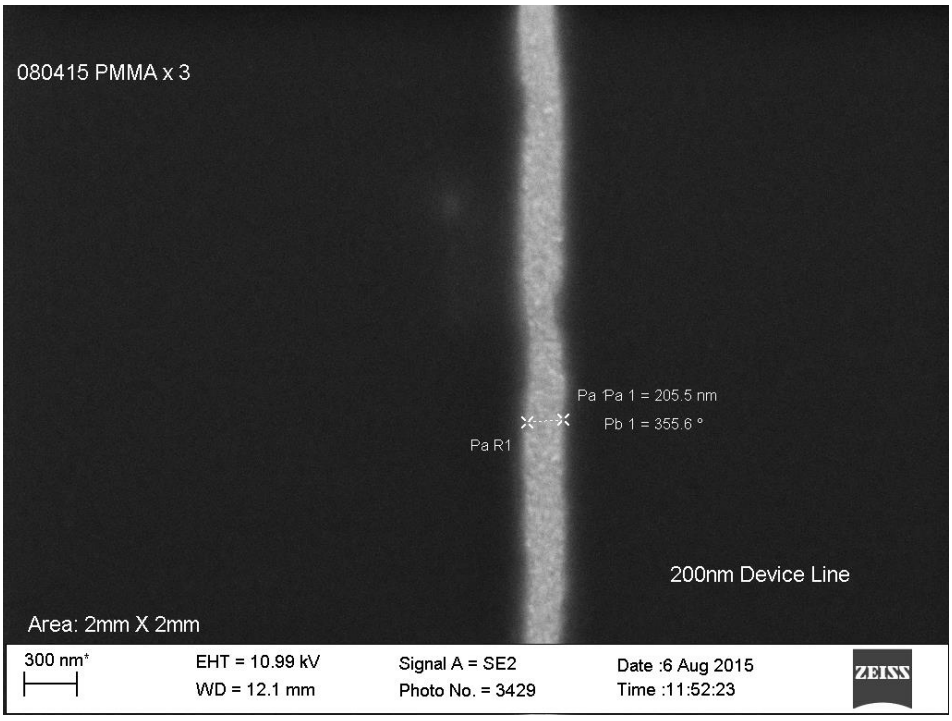

Fig. 6.1c Triple PMMA Spin on resulting in a near 200nm width.

With better test results obtained from the multi-spin process. A double spin-on was used for the actual sample.

The PMMA used for this process is PMMA 950 A2. This was spin coated at 6krpm for 40 seconds and then baked at 130^{o}C for 3 minutes. Another coating of PMMA was then applied with the same parameters except for the final bake which was done for 10 minutes. The wafer was then loaded into the electron beam lithography system.

Another issue with the e-beam tool which was encountered late in the research and after the Quantum software install was that the system was not able to write the entire GDS2 mask. The program generally freezes once it gets to the sixth device. A workaround was found through some trial and error. The fix, though not optimal nor time efficient, was to set the system so as to write up to twenty devices at a time. Writing anymore devices would cause the system to crash. In any event, the parameters used for the e-beam are: EHT=30kV, Spot size=3, and a filament current between 1.65-1.79A. These parameters lead to a beam current of around 330pA±30. Exact values are not necessary as long as they are in the ballpark. In the Raith's software the beam current (along with a step size value which the user selects) will be used in the calculations for the various parameters such as: dwell time, dose, and beam speed. Fig. 6.2 illustrates the step size, S, parameter which is the center distance between beam points.

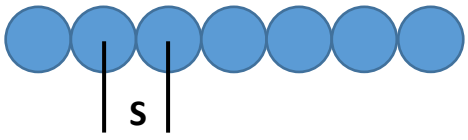

Fig. 6.2 Step Size: Distance between the center of adjacent beam points.

Dwell time is the amount of time the beam is exposing a given point. The dose is a calculation between the dwell time (T_{dwell}) multiplied by the beam current (I_{beam}).

$$Dose = T_{dwell} \times I_{beam}$$

After the electron beam exposure, the sample is developed for 2 minutes in MIBK:IPA (1:4) solution. A 10min ion clean is done prior to the Au wet etch. Again the wet etch is HG-800 for 5-10 seconds. Finally, the PMMA is removed via acetone spray and soak.

Preliminary test runs with the Raith e-beam system shows that thin trenches can be formed. With a better working and more precise lithography tool the possibility of fabricating the devices should not be an issue. In the future, using a different more stable e-beam lithography system should be looked into.

Future Work

Since no devices have been fabricated with this e-beam process there is the possibility of problems arising during processing. The points were issues could occur will be discussed beginning with the trench process. In this processing scheme, the trench is formed by a Au wet etch to remove the thin Au. This leaves the NbN exposed to atmosphere. Although this shouldn't be a problem since further processing steps such as the kernel width step covers the HEB area, incase this does pose an issue the workaround would be to do the kernel width step right after the beamlead plating layer step and before the e-beam step. The process would go as follows:

After completing the beamleads, do the kernel process as usual ending with a Au wet-etch of the thin Au across the wafer (the thin Au under the kernel mask being protected). Follow this with the NbN RIE etch. This will clear away the NbN uncovered by the thin Au. At this point the HEB width has been defined. Strip the kernel resist and apply PMMA. Proceed to run the e-beam process as normal and

wet etch the thin Au under the trench. Finally, remove the PMMA resist. In the future it may be best to run the process using this change rather than the original idea.

Conclusion

The work in this thesis was twofold. To find the culprit for the high sheet resistance as well as the resistance over time problem and to find a method for fabricating NbN p-HEB devices at the University of Virginia. With regard to the O_2 plasma, though there may be more factors, it appears the main factor was that the O_2 plasma was damaging the NbN. Exactly how and why the damage was occurring has not been determined. In any event, knowing that the O_2 plasma was the primary issue allowed us to find a different method to fabricate p-HEB devices. Also, the same basic device design was kept.

Another added benefit with using e-beam is that the HEB dimensions, and the dimensions for any of the layers, can be altered. All of the physical mask layers have a CAD and GDS2 counterpart. This gives the ability to change and test various dimension in any layer which is cost effective and efficient since physical masks do not need to be made.

Appendix A: Ti-line NbN p-HEB Process

Starting material: 19mm SOI wafer square, 300-500µm handle layer, 1µm BOX layer, 3µm device layer, 1-20 Ohm cm device Si, precoated with 40Å NbN

ETM spin clean

Multi-target sputter system (grease mounting optional)

30sec ion clean, 150V (as system normally runs at 300V one may have to finely adjust pressure to stabilize power supply)

Deposit 100Å Au, 150W, 2.70mTorr

Ti-line 1 (Circuit layer patterning)

Spin LOR 5B: 6krpm, bake 160C 5min (LOR is optional, but has been found to improve liftoff and ashes in O2 more cleanly than polyimide alone)

Spin Durimide 284 (polyimide): 6krpm (5krpm if there is no LOR), bake 100C 1min, 120C 1min, 130C 1min, 160C 5min

Multi-target sputter system: deposit 8min Ti 2.70mTorr (approx. 600Å)

Lithography 1: Ti-line 1 pattern

Spin NFR:thinner 1:1: 6krpm (2000Å), bake 90C 2min

Expose on EVG Aligner: 5" mask holder, 2" metal wafer chuck, Ti-line 1 Mask, with mesh filter, hard

contact 5psi, 20sec

Develop: 300MIF, 30sec, rinse DI

Post exposure bake: 120C 5min

Ti/Poly RIE in Semigroup RIE

Condition: F12 11sccm, O2 2sccm, CF4 10%, 8mTorr, 120W, 5min

Vent, insert quartz platter, place wafer in plastic dish near front edge of platter

Etch Ti: F12 11sccm, O2 2sccm, CF4 10%, 8mTorr, 120W, 5min (flash usually around 2.5min)

Etch Poly/Remove NFR: (no vent or recondition necessary) O2 15%, CHF3 30%, 10mTorr, 120W,

12min (very consistently 500Å per min, usually there is no need to do a measurement at this stage unless there has been a change to the RIE system, Ti-line width is not greatly sensitive to the poly etch depth in any case)

Remove Ti: F12 11sccm, O2 2sccm, CF4 10%, 8mTorr, 120W, 2-3min for flash plus 30sec overetch

Vent and remove wafer, measure poly etch depth_____Å

Ti-line Deposition

Multi-target sputter system

Deposit Ti thickness according to Ti-line fitting function: 14*(Desired width in nm)-500Å=Film thickness in Å (works in range of approx. 100-250nm, function may require re-calibration from time to time), 300W, 2.70mTorr, (can increase pressure to 2.90µm for narrow lines for increased tensile stress), 30rpm rotation

Deposit Nb such that Nb+Ti thickness > 1200Å at least (used to bulk up horizontal surface film

thickness to improve capability as evaporation stencil), 500W, (low stress pressure)

Lithography 2: Circuit layer pattern

Spin NFR undiluted: 6krpm, bake 90C 2min

Expose on EVG Aligner: 5" mask holder, 2" metal wafer chuck, Circuit layer (microstrip) Mask, align, use mesh filter, hard contact 5psi, 25sec

Develop: 300MIF, 35sec, rinse DI

Post exposure bake: 120C 10min, in vacuum baking jig (removes water and solvent that can interact with polyimide in following etch)

Ti-line RIE in Semigroup RIE

Condition: F12 11sccm, O2 2sccm, CF4 10%, 8mTorr, 120W, 5min

Vent, insert quartz platter, place wafer in plastic dish near front edge of platter

Etch Ti: F12 11sccm, O2 2sccm, CF4 10%, 8mTorr, 120W, approx. 200Å/min etch rate, overetch 1min after flash

Poly pre-etch: (no vent or recondition necessary) O2 50%, 100mTorr, 120W, 30sec, after initial 30sec leave power on and increase pressure by slowly closing VO over the course of ~2min to reach 1Torr (this process removes the top layer of polyimide hardened by the F12 while preventing further hardening by high energy O2 ions)

March polyimide ash: 5 hour O2 plasma ash, 100W, cooled electrode (undercuts Ti-mask by 1-2µm and usually removes NFR layer above Ti, though NFR presence has no impact on process)

Circuit layer evaporation

Grease wafer onto evaporator wafer holder and clip

Insert in system and pump down

Low power (low temperature) evaporation is critical, as heating of the wafer can cause thermal expansion and Ti-line deformation

Evaporate Au, 5-10Å/sec, 2000-2500Å total (any amount above 2000Å is used as sacrificial Au that will be unintentionally removed in the bridge etch process, the max Au limit is set by the distance between the Ti-line and wafer surface and is approximately 1µm for an LOR/Poly sacrificial layer)

Liftoff sacrificial polymers

NMP 120C, approx. 30min (entire wafer is placed in solvent along with grease from evaporation)

After 30min NMP soack, cycle between DI beaker rinse, high-pressure DI faucet rinse, and NMP soak until surface is clean

DO NOT USE SWABS TO RUB WAFER (can damage the contact pads structure)

Final DI rinse

Methanol spin clean

March O2 plasma clean: 150W, 5min, cooled electrode

Beamlead Fabrication

Lithography 3: Beamlead pattern

Spin AZ4330: 3krpm (4µm), bake 100C 2min

Expose on EVG Aligner: 5" mask holder, 2" metal wafer chuck, Beamlead Mask, NO mesh filter, hard contact 5psi, 200sec

Develop: AZ400K, 2-4min, rinse DI, blow dry

Measure resist height:_____µm

March O2 clean: 5min, 100W, cooled electrode

Electroplating

Place wafer on 1" wide glass slide, in "mouse trap" plating jig (no wax or adhesive necessary)

Tighten contact tip on plating pad with wafer center facing away from mouse trap

Heat Technic 25E plating solution to 50C

Electroplate with 4mA plating current, gently stirring wafer in plating solution, 6min (approx. 2.5µm, thickness from 2-3µm is acceptable)

Remove wafer from solution and mouse trap, measure resist-Au step:_____µm

Continue plating if necessary

Remove wafer, thoroughly rinse all components under DI faucet, disassemble

Spray wafer with acetone to remove photoresist

ETM spin clean

March O2 clean: 5min, 100W, cooled electrode

Bridge Patterning

Lithography 4: Bridge pattern

Spin AZ4110: 6krpm (1µm), bake 100C 2min

Expose on EVG Aligner: 5" mask holder, 2" metal wafer chuck, Bridge Mask, NO mesh filter, hard contact 5psi, 45sec

Develop: AZ400K, 1-2min, rinse DI, blow dry

Post exposure bake: 120C 5min

March O2 clean: 5min, 100W, cooled electrode

Wet Etch Pattern Transfer

(use non-conductive tweezers for all wet etching)

Au wet etch: HG1200, 30sec or until open-field capping Au is gone, DI rinse

Spray wafer with acetone to remove photoresist

ETM spin clean

NbN wet etch: 4 parts DI, 2 parts nitric acid, 1 part BOE (made freshly each time, ready to use immediately after mixing), approx. 10min or until Si surface becomes hydrophobic (dip in DI periodically to test) and is slightly darkened with small 'star' shaped features (don't excessively overetch as etchant will aggressively attack Si), the special DC test pads without bridge masking features should measure 200+ Ohms

Bridge Au removal: HG1200, 20sec or until normal DC test pads with bridge masking features measure Close to target room temperature resistance (will be only a few Ohms if Au is not removed, transition to target resistance is usually fairly abrupt), DI rinse

(Avoid excessive heating, O2 plasma cleaning, or other plasma exposure to front side of wafer once Au and NbN have been etched)

Bridge Protection

Lithography 5: Protection pattern

Spin AZ4110: 6krpm (1µm), bake 100C 2min (safe for exposed NbN)

Expose on EVG Aligner: 5" mask holder, 2" metal wafer chuck, Protect Mask, NO mesh filter, hard contact 5psi, 45sec

Develop: AZ400K, 1-2min, rinse DI, blow dry

Appendix B: SOI Backside Process

SOI BACKSIDE MASTER SHEET

MAKE SURE ALL FRONT-SIDE PROCESSING IS DONE!!!

□ **Does the Wafer need a backside stress compensation layer?** _____

□ **SOI device Si thickness 3um?** _____

Backside Process

□ Mount epoxy/Waferbond

□ March Clean

□ Dice thin

□ Oxford RIE thin

□ BOE remove BOX SiO_2

□ Stress Compensation later?

□ Yes □ No

□ Alignment Marker Opening

□ Alignment Marker Lithography

□ Alignment Marker Etches

□ Extents Lithography

□ Extents Etches

□ Chip Removal

SOI Chip Definition Process 07-14-09

1. Wafer Bonding

We initially keep the hotplate at room temperature and place the teflon ring directly on the hotplate. This is done to first hold a vacuum for 10 minutes in order to remove any bubbles before we start to cure the waferbond. The hotplate is then set to 150C to cure the waferbond.

a. Spin Wafer Bond (WB) onto the Device Wafer
   i. Spin clean device wafer and back at 120C for 10 minutes.
   ii. Spin Wafer Bond at 3.5k for 40 sec (start at 0 rpm to spread W and increase to 3.5krpm over ~10 seconds).
   iii. Take 3-4 large textwipes, spray a ~3" center region thoroughly with ETH or METH, then place Device Wafer ontop and push back and forth to help clean off the backside of the wafer.
   iv. Place Teflon ring assembly on cold variable hotplate.
   v. Put the bell jar adapter on top of the Teflon ring and pull a vacuum, hold vacuum for 10 minutes with the hotplate turned off.
   vi. Turn on hotplate and bake under vacuum for 25min at 150C, start timing from the moment the hotplate is turned on. Proceed to mix epoxy during this time.

b. Mix Epotek epoxy

i. Either take a small metal dish or create one with Al foil and a small plastic dish. You want to make the dish sit with a tilt (so the epoxy will pool to one side) either by folding the Al foil over onto one side of the backside, or to crimp/bend the Al foil dish so that it does the same).
ii. Put the dish on a small wipe in the Pan Scale. Measure out 10 parts mass of A. Then rezero scale and add 1 part B by mass. Something around 1.0 and 0.1 grams should be enough.
iii. Thoroughly mix epoxy with the stick end of a swab.
iv. Place in the vacuum desiccator (under vacuum) in photolith for >30min

c. Bonding in Jig

One should note that the epoxy can be dissolved in methanol before it is cured. If for some reason the device wafer falls into the epoxy prematurely, you must vent the bonding jig and remove the wafer immediately. You can use methanol to remove the epoxy and then TCE to remove the waferbond. The bonding process will have to start over, but there will be no damage to the wafer.

i. TCE spin clean 3" carrier wafer and bake at 160C for 5 minutes
ii. Heat lapping jig to 100C
iii. Make sure hotplate used in bonding is at room temperature!
iv. Place Teflon ring onto hotplate
v. Place 4" wafer on cold mounting plate to prevent epoxy runoff from curing to hotplate
vi. Place 3" carrier onto 4" wafer
vii. Make sure bonding jig is in the highest position (screw fully backed out) and attach SOI to bell jar swivel chuck using L-grease (Wafer Bond side down, facing away from the grease) Make sure L-grease is applied in lines radially outward from center of chuck. The radially outward grease application is critical because trapped air pockets that may result from other grease patterns may cause wafer to fall off when a vacuum is applied.
viii. Using micropipette, dispense ~500uL of epoxy on carrier
ix. Make sure epoxy mound is centered on carrier.
(You can use filter papers to shim the legs of the hotplate to make it level in the case that the mount starts flowing in one direction.)

x. Place bell jar Jig on Teflon ring, slowly apply vacuum making sure Si carrier wafers don't shift and pump vacuum for 10 min, DO NOT lower wafer yet.
xi. Visually inspect for any remaining bubbles
xii. Lower the SOI wafer slowly into epoxy/Si carrier by carefully depressing plunger and gently push device wafer into the epoxy.
xiii. Set hotplate to 100C and cure Epoxy for 5min, start timing from when hotplate is turned on.
xiv. Turn off hotplate, release vacuum
xv. Remove wafers from hotplate, wafer will slide off of chuck since L-grease is hot
xvi. Clean excess epoxy using meth/swabs
xvii. Put in lapping press with for >=30min at 100C
    1. Place silicone sheet over SOI wafer to prevent epoxy from curing to cylinder
    2. Use 2" OD X 1.25" high cylinder
xviii. Remove from lapping jig

2. Handle Lap-Dice in Dicing Saw
    a. Measure and record height of carrier+wafer in several locations, we choose the thickest point to be safe and refer to this as the 'stack height'
    b. Start Dicing Saw
    c. Load hubless blade
    d. Setup
        i. Cutspeed - 1.2mm/s
        ii. Y-IND – 0.40mm
        iii. Cutstroke – 65mm
    e. Reduce cut height to leave ~30um of Si handle

    Cut height = (stack height + 30 microns – handle thickness)

    f. Dice entire wafer from back to front

3. Epoxy removal
    a. Using Exacto knife/scalpel, carefully scrap off any excess epoxy that remains after dicing
    b. Place Wafer in March O2 plasma overnight to remove any remaining exposed epoxy
    c. At 150W, the epoxy etches at roughly 2um/hr

4. Handle Etch in Oxford
    a. For all backside etches we use a Si/SiO2 wafer for maximum heat transfer. First the wafer is mounted to the carrier via L-grease on a hotplate at 100 C.
    b. Place Carrier wafer on 100 C hotplate. Apply a pea-size drop of L-grease to center
    c. Place Carrier wafer on 100 C hotplate. Apply a pea-size drop of L-grease to center
    d. For the Etch, we begin with applied RF power to generate a DC bias, but only for the beginning of the etch as the DC biased etch is believed to be aggressive toward the SiO2 stop layer. After 5 minutes it is then removed and the plasma is maintained by the ICP.

    The conditions are:

    SF6: 20

    O2: 2

    Pressure: 20 um

    Temperature: 20C

    He: 5

    ICP: 500

    First 5 minutes:

    RF: 100W (resulting DC bias is around 300V)

    For 30 secs: (to maintain plasma with sudden drop in applied power)

    RF: 50W

    For the rest of the etch:

    RF = 0W

Stop after 10 minutes and inspect the wafer. Proceed to etch in 5-10 minute intervals if silicon is still present. This can take up to 40 minutes total etching time depending on the thickness of the handle

e. The Si appears as very dark spots on the wafer and will be noticeable when it is fully removed. After the dark Si areas are removed, there will be artifacts of the dicing that appear under the microscope as lines in the BOX layer, note this is not left over silicon.
f. Carefully remove wafer from carrier by sliding it off while heated on a 100 C hotplate.
g. Carefully remove grease from backside by spraying with TCE. Do not apply TCE to frontside as it will cause the waferbond to dissolve.

5. BOX strip
    a. 30 min in BOE
    b. Dip is beaker of DI and remove slowly. The wafer should be hydrophobic and come out almost perfectly dry on the Si surface. If not, etch for 5 minutes. Repeat until wafer is hydrophobic.
    c. 3X DI rinse

Alignment Marker Opening Lithography

Note, we now open the alignment markers before applying the backside compensation layer.

The goal is to use the microscope as an exposure tool to open holes in the resist to provide an etch mask for the thin silicon. Using the differential interference contrast (DIC) on the microscope, it is possible to see alignment features through the thin silicon. Once the features are located, the microscope light is placed over an alignment marker and the size is adjusted through the focal shutter. The UV filter is then removed and UV light from the incandescent spectrum of the microscope light will provide the energy to expose the illuminated resist so it may be developed. 5214 is used because the resist can be hardened by performing a flood exposure and HPB after development. This hardened resist can withstand the BOE and RIE etches.

□ **Spin Coat Photoresist**

- □ Spin clean Ethanol, TCE, Methanol
- □ 110C bake for 5 minutes
- □ HMDS 5 min
- □ Spin AZ5124 4 krpm 30 sec
- □ Bake 100C for 1 min

□ **Exposure**

- □ Use Microscope to expose areas above alignment markers.
- □ Expose for 5 minutes at full intensity with filter removed
- □ Repeat for at least 4 alignment markers.
- □ After all desired alignment markers are exposed, expose an addition area in the center of the wafer to use as an endpoint in the Oxford.
- □ Develop in AZ 400K 1:4

  Actual time = _____

- □ Flood Expose MJB4 60s (Needed to cause cross-linking and harden resist)

□ HPB 110C 2 minutes (Needed to cause cross-linking and harden resist)

Alignment Marker Etches

□ **BOE Etch (Only if Stress Compensation Layer is present)**

□ BOE etch for 3 minutes (for ~2500A sputtered SiO2)

□ Dip is beaker of DI and remove slowly. The wafer should be hydrophobic around the marker openings.

□ 3x DI rinse

□ **Si Etch in Oxford:**

The etch is timed by monitoring the camera for the endpoint. The silicon will flash between bright and dark as it is etching. When the flashing stops, the etch is completed. The etch is VERY FAST (~15 seconds), so watch carefully.

□ Grease carrier to 5" Si/SiO2 carrier.

□ Place wafer on center of the carrier and check, by looking through the underside of the carrier, that the Fomblim oil is spread between the carrier and device wafers.

□ Etch in Oxford: (RF is used for first 10 seconds only in order to start the plasma)

SF6: 20

O2: 2

Pressure: 20 um

Temperature: 20C

He: 5

ICP: 500

First 5 seconds:

RF: 100W

For 5 seconds:

RF: 50W

For the rest of the etch:

RF = 0W

Actual time = _____ (~15 seconds here + preview two etches = ~25s total)

□ Strip Resist in March ~90W (takes around 3 hours)

Backside compensation layer (fill in system conditions if used)

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