A Fully Integrated 0.4 mm^2 Soft-Charging Switched-Capacitor DC-DC step-down Converter with 85% Peak Efficiency Minimizing the Circuit Footprint for Sub-mA-Load E-Textile Applications

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A

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Abstract

This work proposes a design approach for a fixed/narrowed-voltage-conversion-ratio (VCR) in a soft-charging switched-capacitor (SC) DC-DC step-down converter, utilizing a continuous-scalable-conversion-ratio (CSCR) architecture, specifically designed for sub-mA-load smart e-textile applications where minimizing size is critical. By narrowing the VCR range, the proposed approach reduces area consumption by constraining design parameters such as capacitor size and operating frequency, sacrificing wide VCR flexibility to enhance power density (PD). This makes it particularly suitable for fixed-VCR mA-load smart e-textile applications, where seamless system integration and compact size are essential. Designed for a 1.8V to 1.2V conversion, the system achieves peak efficiencies of 85.4% and 87.8 % in compact footprints of 0.4mm² and 0.6mm², using 65nm CMOS technology. It operates efficiently across a load range of 0.15mA to 2 mA. These simulation-validated results demonstrate the efficiency and PD advantages of the proposed design method over wide-VCR designs in sub-mA-load scenarios. The approach optimizes capacitor sizing and operating frequency, balancing efficiency and area, making it well-suited for space-constrained fixed-VCR-sub-mA smart e-textile applications where maximizing PD in small form factors is crucial.

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Chapter 1

Introduction

1.1 Overview of Smart E-Textiles and Power Requirements

The integration of electronics into textiles is reshaping the landscape of wearable technology, offering transformative potential across diverse fields such as healthcare, fitness, sports, and military applications [30]. This shift is driven by the demand for electronic systems that are compact, robust, and flexible, seamlessly embedded within textile structures [31] to deliver advanced functionality without compromising the comfort, flexibility, and durability [32] inherent to fabrics. These characteristics are critical for wearables, which must maintain the tactile [33] and aesthetic qualities expected from traditional textiles while enhancing them with innovative technological capabilities.

The miniaturization of components has become a cornerstone of this evolution, allowing complex electronic systems to enhance fabric functionalities in a nonintrusive manner. Recent breakthroughs, including lithium-ion ribbon batteries with widths below 500 micrometers [1], exemplify how miniaturized power sources can be integrated into wearables without adding bulk. Similarly, embedding audio, imaging, and monitoring systems within fibers creates possibilities for new applications in both everyday clothing and specialized textile applications. Such advancements are paving the way for "system-on-textile" designs shown in Figure 1.1, where entire electronic subsystems are distributed throughout fabrics, providing a unique combination of convenience and

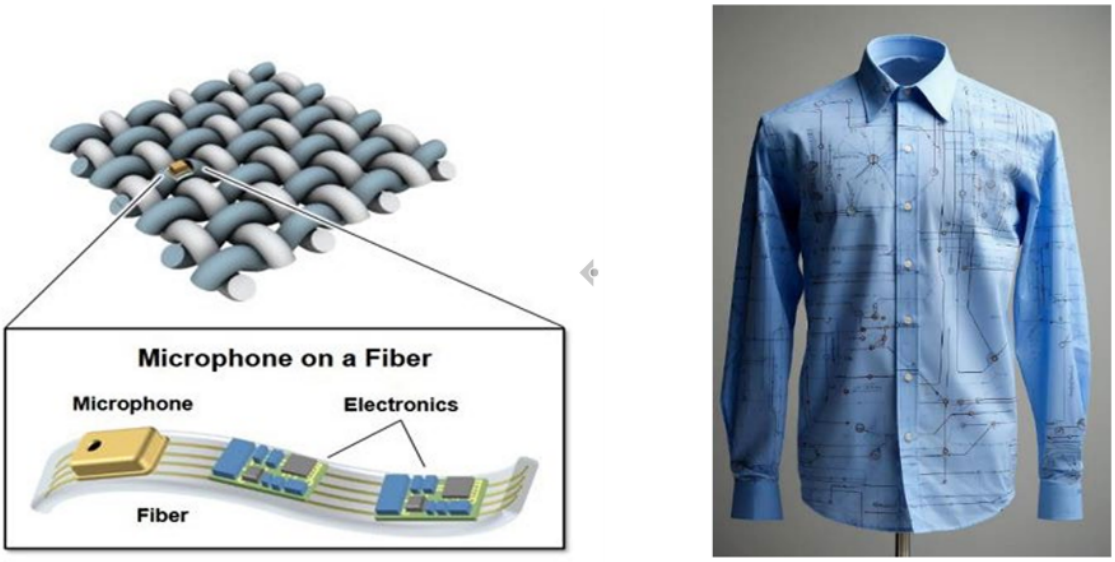


Figure 1.1: System-on-Textile [1]

functionality that redefines traditional textiles.

Efficient power management is crucial in wearable technology, particularly for textile-based applications, where ensuring user safety, comfort, and extended battery life is essential. Power management systems must not only extend battery life but also prevent risks like overheating and skin burns. To be viable, these systems need to be highly efficient, mechanically resilient, and compatible with large-scale textile production. Miniature, lightweight, and flexible power management solutions are key to operating within the constraints of textile materials [34]. Since many wearable textiles operate in low-power modes with minimal load demands, there is an increasing need for compact, low-current power converters that can efficiently step-down voltages, minimize their physical footprint, and maintain high efficiency. For example, healthcare monitors embedded within textiles that consume only 1.1 mW highlight the need for low-power components [35]. These applications require converters optimized for low-load conditions, ensuring extended battery life, reduced power dissipation, and overall efficiency. This convergence of textiles and electronics motivates the development of miniature, highly efficient, and compact on-chip power management solutions that are essential for the future of smart wearable technology.

1.2 Challenges in Existing DC-DC Conversion for Wearable Applications

Wearable applications, especially in e-textiles, require DC-DC switched-capacitor (SC) converters that are not only scalable and compact but also fully integrated on-chip. This integration is crucial to eliminate bulky external components, such as off-chip inductors, capacitors, wiring, pins, and pads, which can compromise the flexibility and aesthetics of wearable textiles. Fully integrated solutions enable a streamlined and scalable approach, aligning with the miniature and lightweight demands of e-textile applications. Although SC architectures are increasingly favored for their on-chip potential [36], they still face significant challenges in maintaining high efficiency across varying loads.

Figure 1.2 illustrates a range of state-of-the-art SC converters, highlighting both fully integrated designs and those utilizing off-chip capacitor & open-loop configurations. This comparison emphasizes high-efficiency/low-area converters to capture the current design landscape. Among soft-charging architectures, designs such as [2–10] have demonstrated high efficiency; Notably, converters in [3] and [7] achieve the smallest areas at 4nm and 28nm nodes, respectively, showcasing the benefits of advanced miniaturization. Additional examples include designs with ferroelectric capacitors [14], deep trench capacitors [25], [26]-combine off-chip capacitance (0.5 nF) and integrated capacitance (3.7 nF) within a 45nm node and high-density MIM capacitors [28] on a 22nm tri-gate CMOS in the targeted design space. Figure 1.2 (b) further illustrates efficiency improvements across recent soft-charging techniques, underscoring the impact of various technological nodes on performance.

Soft-charging techniques, especially multiphase designs [2–10], have notably improved efficiency by minimizing charge-sharing losses through multiple charge transfer stages. These innovations reduce voltage swings across capacitors per transfer, ensuring optimal performance across a broad range of voltage conversion ratios (VCRs). While these designs reach high efficiency at higher power outputs, they often suffer at low-load conditions, where efficiency decreases due to their optimization for heavier loads. Notable designs, such as the multiphase CSCR, provide flex-

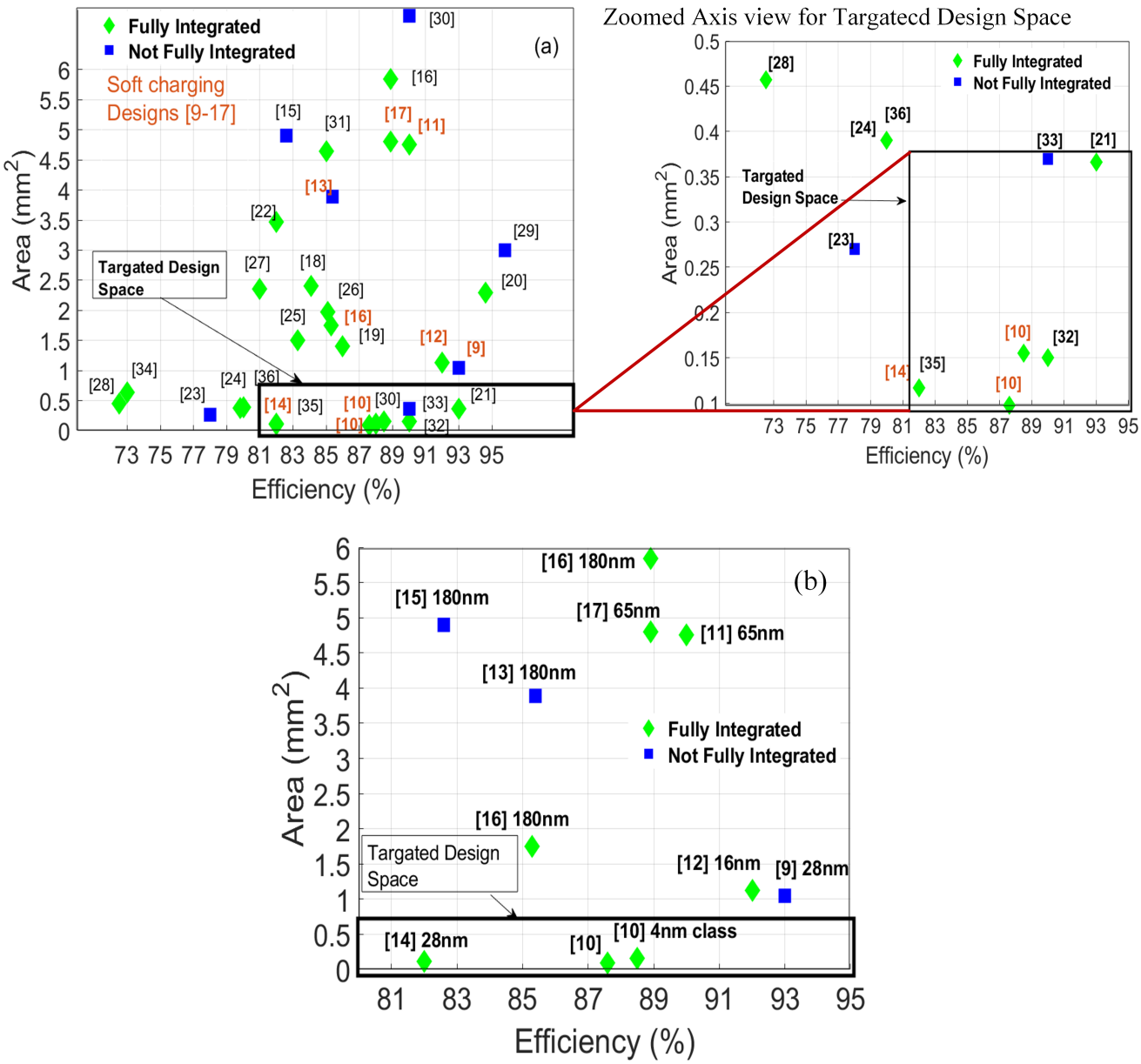


Figure 1.2: Area vs. Efficiency Scatter Plot: A comparison of state-of-the-art SC converters focusing on high (a) efficiency/miniature footprints mostly fully integrated (b) for soft-charging SC converters with different technology [2–29].

ibility over a wide VCR range [3–6], while the Dickson SC topology, optimized for high power delivery, operates at a fixed VCR [7]. Although these converters leverage advanced technology

nodes to enable miniaturization, their power density often declines at loads below 5 mA [2] [8–10]. This limitation underscores the need for converters with high efficiency, compact footprints, and specific optimization for low-load conditions, which are critical for e-textile applications.

1.3 Motivation for a Fixed/Narrowed VCR Approach

Soft-charging switched-capacitor (SC) converters are particularly effective for low-power e-textile applications, achieving high efficiency through capacitive power transfer. As illustrated in Figure 1.2(b), the miniature footprints seen in advanced technology nodes, such as 4nm and 28nm, underscore this efficiency. The goal of this work is to design in the 65nm node, focusing on a fixed voltage conversion ratio (VCR) to achieve a miniature footprint. By focusing on fixed/narrowed VCR implementation within a continuously scalable conversion ratio (CSCR) architecture and optimizing parameters such as capacitor size and operating frequency, this optimization aims to reduce overall dimensions while increasing power density (PD), resulting in a miniature footprint that enables easier integration into space-constrained textiles.

1.4 Design Goals and Objectives

The goal is to design a compact, fully on-chip DC-DC SC step-down converter optimized for a fixed voltage conversion ratio (VCR) of 1.8V to 1.2V, ensuring efficient operation across a load range of 0.15mA to 2mA. By narrowing the focus to a fixed VCR, the design targets moderately high peak efficiency while maintaining a miniature footprint of 0.4mm². The design process and implementation are validated using simulated data.

1.5 Thesis Statement

i) A design approach for a soft-charging switched-capacitor (SC) DC-DC step-down converter optimized for sub-mA load applications in smart e-textiles, emphasizing reduced area and en-

hanced power density (PD) at the expense of a wide voltage conversion range.

ii) A converter design, implemented using proposed design approach, incorporates a continuous-scalable-conversion-ratio (CSCR) architecture with a fixed/narrowed voltage conversion ratio (VCR) approach, enabling a universal and adaptable topology suitable for various VCR requirements. The fully integrated compact on-chip design utilizes an advanced multiphase out-phasing technique within the CSCR architecture, delivering moderately high efficiency in a miniature footprint with 0.4mm² and 0.6mm² for e-textile applications.

Chapter 2

Soft-Charging Advance-Multiphase Operation in Switched-Capacitor (SC) step-down Converters

Soft charging is a technique in switched-capacitor circuits that minimizes the voltage difference across capacitors during charging and discharging phases to reduce energy losses and enhance efficiency. This section will introduce the Soft-Charging-based Advanced-Multiphase SC Buck Converter, starting with background information on charge-sharing losses in switched-capacitor circuits, then an overview of soft charging in terms of loss reduction, followed by a discussion of the converter topology and the advanced multiphase operation.

2.1 Background: Charge-Sharing Loss in Switched-Capacitor (SC) Converters

Charge-sharing loss is a fundamental efficiency constraint in switched-capacitor (SC) converters. It occurs when capacitors are hard-switched between nodes at different voltage levels, leading to energy dissipation from the redistribution of charge. The energy dissipation due to charge-

sharing loss, denoted as E_{cs}, is proportional to the square of the voltage difference, such that $E_{\text{cs}} \propto \Delta V^2$. On the other hand, the charge transfer q, is linearly proportional to ΔV, and can be expressed as $q \propto \Delta V$.

$$\frac{q}{E_{cs}} \alpha \frac{1}{\Delta V} \tag{2.1}$$

In a SC converter with approximately fixed capacitor voltages, efficient operation is typically limited to specific rational voltage conversion ratios (VCR). When a lower output voltage is required, the capacitor's voltage swing increases, reducing efficiency.

2.2 Overview of Soft-Charging in DC-DC Converters

Soft-charging facilitates charge transfer through multiple steps or phases, effectively minimizing the voltage swing in each transfer. This approach removes dependence on the final voltage swing across capacitors, effectively eliminating VCR dependency. With soft-charging, efficiency can be controlled by adjusting the number of phases, denoted by S, which determines the step size or phase increment. Increasing the number of phases decreases charge-sharing losses, leading to higher efficiency. Consequently, Equation 2.1 can be rewritten for soft-charging as follows: Equation 2.1 can be rewritten for soft-charging as follows:

$$\frac{q}{E_{cs}} \alpha \frac{S}{\Delta V} \tag{2.2}$$

Figure 2.1 illustrates the basic idea of soft-charging flying capacitor voltage swing between Vin to 0 and back in the multiple steps, regardless of Vout voltage, that helps to break the VCR connection to efficiency, these steps introduce intermediate nodes, increasing intermediate nodes/steps/phases helps to achieve the high efficiency by reducing the charge-sharing-loss.

2.3 Topology

Single capacitor architecture has been chosen for simplicity, and the polarity of the capacitor stays the same over the full cycle of charge transfer also the capacitor must connected to one of the

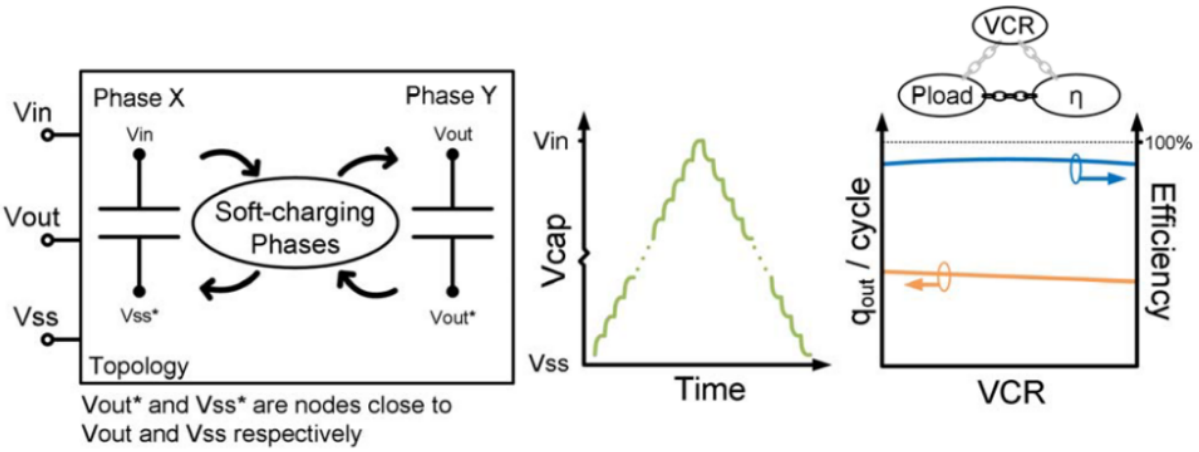


Figure 2.1: Fundamental of Soft-charging conversion Fig 3 from [2]

converter terminals (Vin, Vss, Vout) during the soft charging transfers; and the goal is to discuss step-down conversion topology. Topology can be explained with the help of phases that are not soft-charging denoted as cornerstones, as shown in Figure 2.2 regular phases (cornerstone phases) can be denoted as D1 (Vout-Vss) and D2 (Vin-Vout), and during the cornerstone phase each cap terminal must be connected one of the converter terminal, to satisfy that condition capacitor stays connected to the same terminal during a set of soft charging transfers, basically two consecutive cornerstone phases always share capacitor terminal connection. The capacitor terminal goes through a separate charging /discharging cycle, the top plate alternates between Vin to Vout and the bottom plate between Vout to Vss, soft-charging can be employed by adding intermediate nodes M from T1 to TM (top intermediate nodes) and N from B1 to BN (bottom intermediate nodes) shown in Figure 2.2 phases per cycle of each capacitor. The cell count needed 2N+2M+1 to complete S=2N+2M+2 phases, and single Cfly cap architecture, each cell has a Cfly cap with N+M+4 switches shown in Figure 2.3.

Bottom nodes boundary condition from equation (7.3) from [37]

$$
\begin{aligned}
V_{B,1} &= V_{B,2} - V_{B,1}, \\
V_{B,i+1} - V_{B,i} &= V_{B,i} - V_{B,i-1} \quad \forall i \in \{2, \ldots, N-1\}, \\
V_{\text{out}} - V_{B,N} &= V_{B,N} - V_{B,N-1}.
\end{aligned}
$$

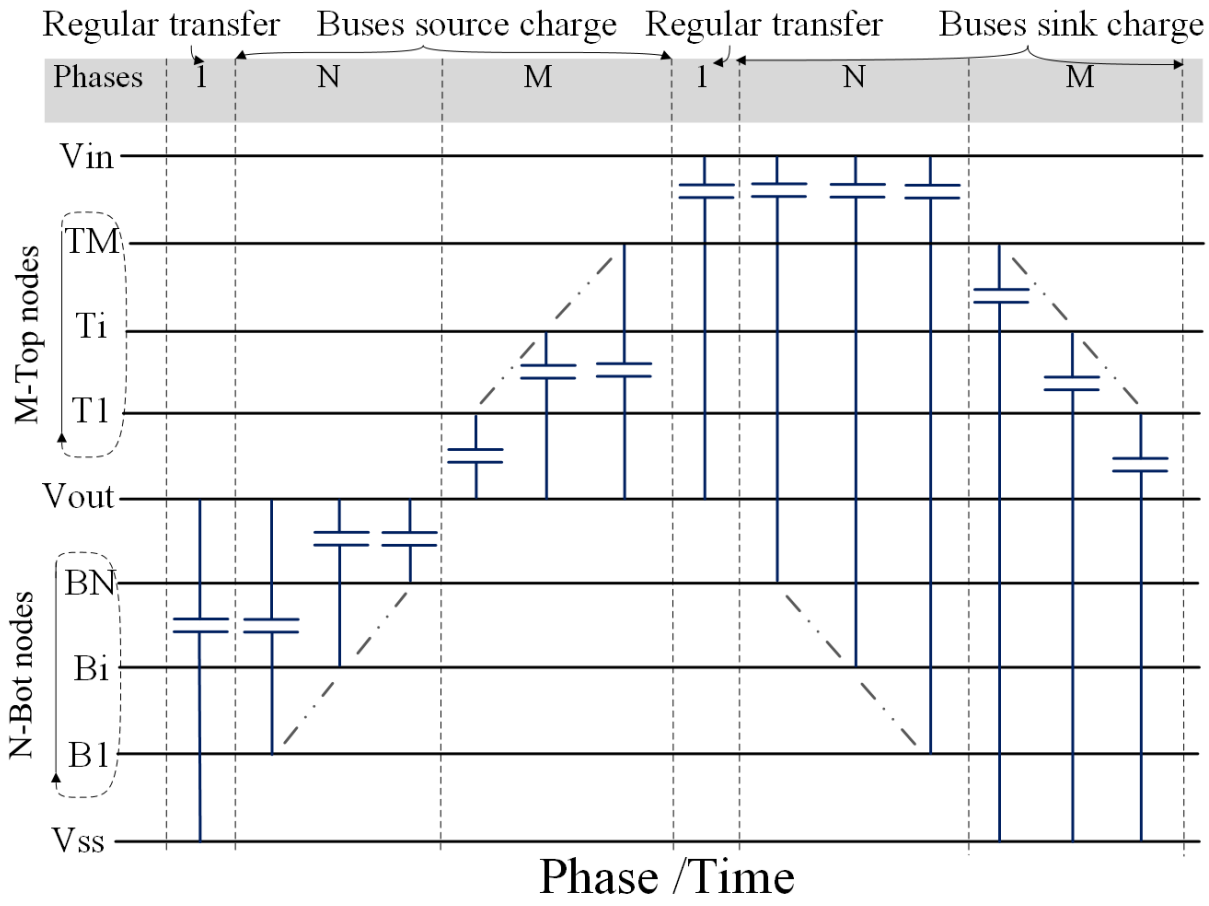


Figure 2.2: Phases/cycle for each cell in Continuous Scalable Conversion Ratio (CSCR) converter.

The top nodes boundary condition from equation (7.4) in [37] is given by:

$$
\begin{aligned}
V_{T,1} - 2V_{\text{out}} + V_{B,N} &= V_{T,2} - V_{T,1}, \\
V_{T,j+1} - V_{T,j} &= V_{T,j} - V_{T,j-1} \quad \forall j \in \{2, \ldots, M-1\}, \\
V_{\text{in}} - V_{T,M} - V_{B,1} &= V_{T,M} - V_{T,M-1}.
\end{aligned}
$$

The voltages at the bottom-side nodes are linearly distributed. The difference between consecutive nodes is constant. Based on these boundary conditions the output- and input charge per cycle, qout and qin, are determined in equations (3) and (4) in [2] or (7.7) and (7.8) in [37].

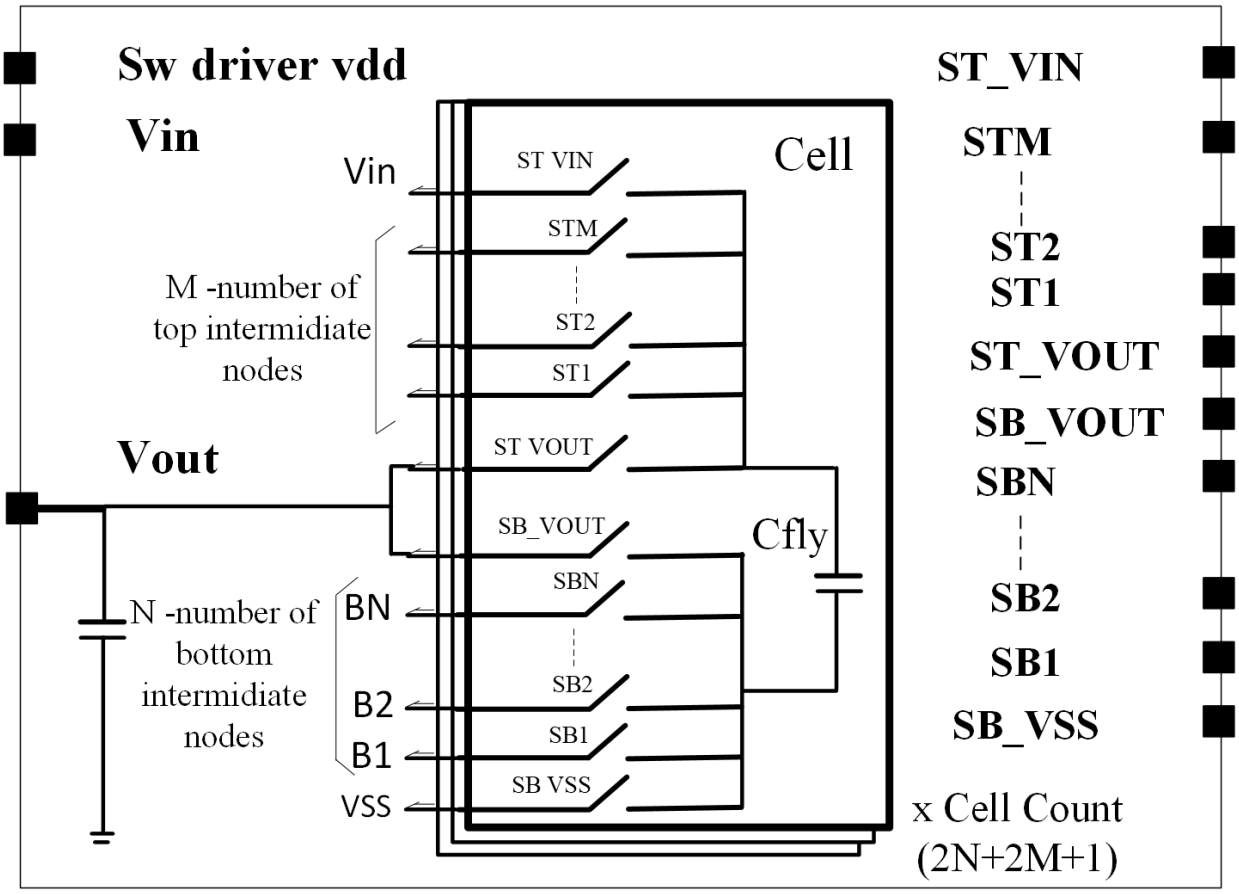


Figure 2.3: Cell structure with switch requirements, and cell count.

The equation (7.5) from [37] is given by:

$$\frac{q_{\text{in}}}{C_{\text{tot}}} = (V_{\text{in}} - V_{T,M}) + (V_{\text{out}} - V_{B,1}).$$

The equation (7.6) from [37] is given by:

$$\frac{q_{\text{out}}}{C_{\text{tot}}} = (V_{T,1} - V_{\text{out}}) + V_{B,N} + (V_{\text{in}} - V_{T,1}) + (V_{T,1} - 2V_{\text{out}} + V_{B,N}).$$

(3) and (4) from [2] /(7.7) and (7.8) from [37]

$$\frac{q_{\text{out}}}{C_{\text{tot}}} = \left(\frac{M+2}{M+1}\right) V_{\text{in}} - \left(\frac{M+N+4}{(M+1)(N+1)}\right) V_{\text{out}}.$$

$$\frac{q_{\text{in}}}{C_{\text{tot}}} = \frac{V_{\text{in}}}{M+1} - \frac{MN+M-2}{(M+1)(N+1)} V_{\text{out}}.$$

Efficiency can be expressed as follows, where N, M can be any integer number.

$$\eta = \frac{q_{\text{out}}}{q_{\text{in}}} \times 100\,\%$$

$$\eta = \frac{\frac{M+2}{M+1}V_{\text{in}} - \frac{M+N+4}{(M+1)(N+1)}V_{\text{out}}}{\frac{1}{M+1}V_{\text{in}} - \frac{MN+M-2}{(M+1)(N+1)}V_{\text{out}}} \times 100\,(\%) \tag{2.3}$$

Since the architecture relies on intermediate top and bottom nodes, the switch size must be carefully designed to ensure complete charge transfer.

2.4 Advance-Multiphase: Out-phasing Working Principle

In a CSCR (Continuously Scalable Conversion Ratio) architecture, the out-phasing technique effectively doubles the soft charging phases by putting the bus-sourcing phases in out-phase relative to the bus-sinking phases. This approach effectively doubles the operation of intermediate nodes, enhancing efficiency by reducing charge-sharing losses while requiring the same number of switches and cells as a regular CSCR implementation with M and N intermediate nodes. This minimizes area requirements and maintains performance, making it well-suited for our goal of a minimized footprint design. For example, in the case of M, N= 1,1 Figure 2.4 illustrates the cell count and phase timing across all five cores (C1-C5). In this implementation, each capacitor discharges and charges over a cycle consisting of 2(2N+2M+1) phases which is 10 phases, with a total cell count of 2N+2M+1 which is 5 cells. This configuration achieves efficiency with double effective soft changing phases, reduce losses, and a compact design—perfectly aligning with our objectives. The input and output charge per cycle for the out-phase operation can be expressed as follows:

$$\frac{q_{\text{in}}}{C_{\text{tot}}} = \frac{V_{\text{in}}}{2M+1} - \frac{(4MN+2M-2)}{(2M+1)(2N+1)}V_{\text{out}} \tag{2.4}$$

$$\frac{q_{\text{out}}}{C_{\text{tot}}} = \left(\frac{2M+2}{2M+1}\right)V_{\text{in}} - \frac{2M+2N+4}{(2M+1)(2N+1)}V_{\text{out}} \tag{2.5}$$

Figure 2.5 also illustrates the connections of each phase capacitor plate throughout a full cycle for $M, N = 1, 1$, with cells denoted as C_1 to C_5. In the first phase, the V_{out} voltage is applied across C_1.

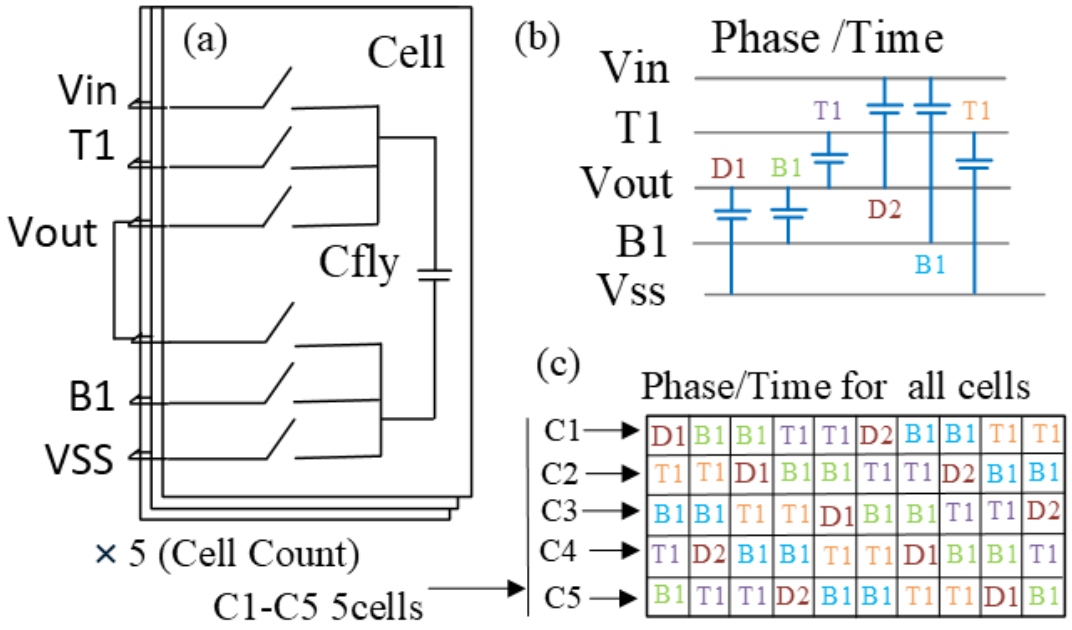


Figure 2.4: Cell structure, Out phase operation-phases per cycle for each core

In the second phase, C_1 discharges as it is connected to C_3 in an out-of-phase setup. During this phase, C_3 charges while C_1 discharges, settling the voltage at the midpoint between $V_{B,1}$ and V_{ss} of both capacitors' bottom plates. Then, in the third phase, C_1 discharges and C_4 charges, with both capacitors' bottom plates settling at the midpoint voltage between V_{out} and $V_{B,1}$. This introduces an additional bottom intermediate node into the operation: the first bottom node $V_{B,1_{\text{effective}}}$, which is the midpoint between $V_{B,1}$ and V_{ss}, and the second bottom node $V_{B,2}$ between V_{out} and $V_{B,1}$. This is how the cycle of discharging and then charging continues, utilizing the out-of-phase technique, completing the cycle with double the effective intermediate nodes.

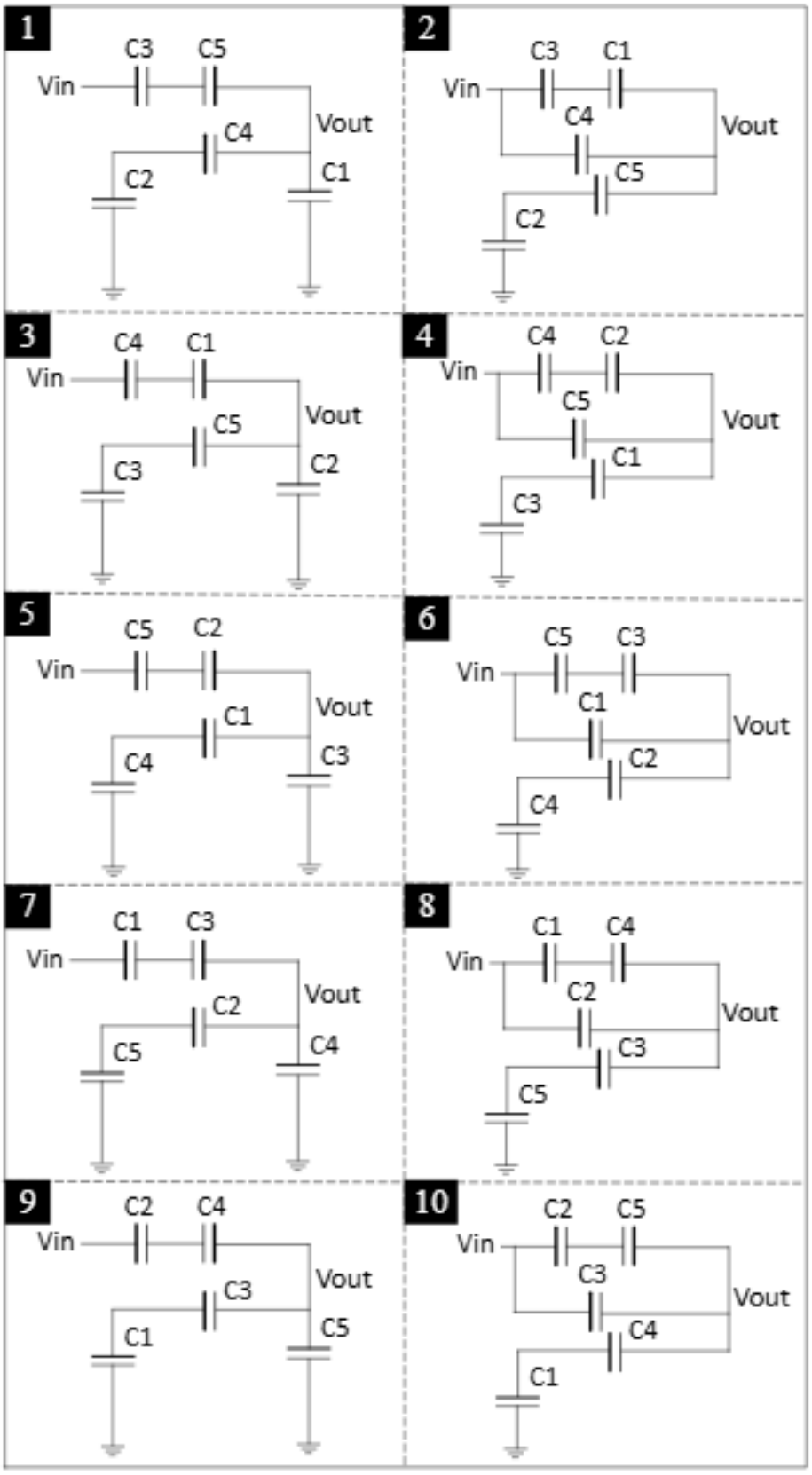


Figure 2.5: Phase diagram of out-phase operation in CSRC step-down converter with M, N=1,1

Chapter 3

Proposed Design Approach

This section outlines the proposed design approach for identifying operating design parameters (ODPs) within a fixed area. A performance analysis follows, supported by simulations, to assess potential deviations both within and beyond these parameters.

The current project in the RLP VLSI group, SMART E-PANTS, focuses on developing stretchable, bendable, and washable Active Smart Textiles (AST) fully integrated into clothing. The components and threads should ideally have a diameter of 0.6 mm based on (Board Agent Announcement) BAA, although slightly larger diameters may be acceptable if they maintain comfort and durability. Based on these criteria, the final target area is approximately 0.6 mm × 0.6 mm, with a rounded-up value slightly higher, around 0.4 mm² (w/ pad 0.6mm² approximately).

3.1 Step1: Capacitor Size within Area Requirement of 0.4 mm²

An estimated total capacitance of 1.149 nF can be achieved within 80% of the area constraint of 0.4 mm² (approximately 0.32 mm²), as shown in Figure 3.1, using a simulated capacitor density of $5.78\,\mathrm{fF}/\mu\mathrm{m}^2$. This density is attained through stacking MOS capacitors [38] (using 3.3V IO devices in 65nm technology), MIM, and MOM capacitors.

Figure 3.1: The estimated total capacitor can be placed in 80% of 0.4 mm², 1.149nF placed in 853um x 344.54um

3.2 Step 2: Maximum Efficiency within 0.4 mm² with OPDs

As discussed in Chapter 2, advanced out-phasing operation, the efficiency can be expressed as follows:

$$\eta = \frac{\frac{2M+2}{2M+1}V_{\text{in}} - \frac{2M+2N+4}{(2M+1)(2N+1)}V_{\text{out}}}{\frac{1}{2M+1}V_{\text{in}} - \frac{4MN+2M-2}{(2M+1)(2N+1)}V_{\text{out}}} \times 100\,(\%) \tag{3.1}$$

Since only the intermediate nodes of the equation play a role in efficiency, a contour plot calculated from Section 3.1 with varying M and N values for Vin=1.8V and Vout=1.2V shown in Figure 3.2. This figure highlights all points with efficiencies of 90% or higher, and identifies the minimum M, N values required to achieve 90% efficiency. However, this plot does not directly relate to or provide results based on area or capacitor size relationships. To proceed, the next step involves correlating the area (capacitor value) to identify operating design parameters. This includes determining the cell count and corresponding M, and N values, and operating minimum frequency to achieve maximum efficiency within the targeted area.

$$f_{\text{sw}} = \frac{I_{\text{out}}}{q_{\text{out}}} \tag{3.2}$$

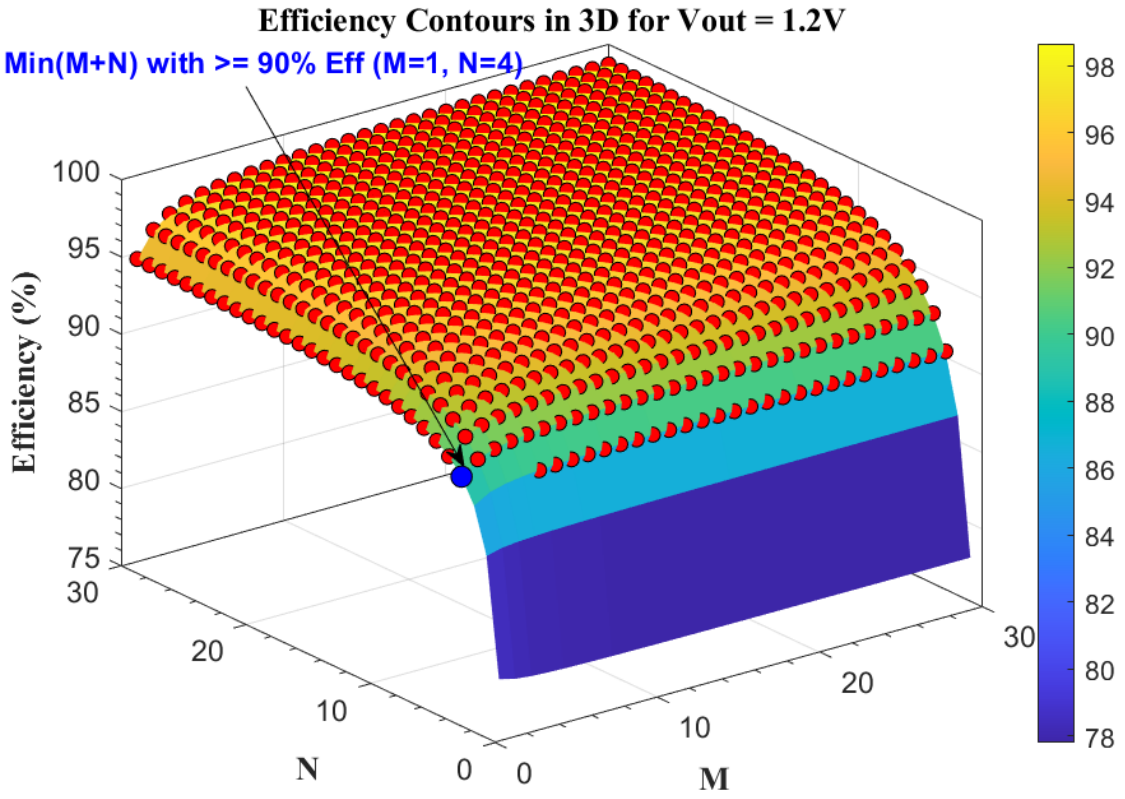


Figure 3.2: Efficiency contour based on different N, M values for Vin=1.8, Vout=1.2V, 90% or above efficiency marked (red circle), and also leveled the min N, M =1,4 for 90% efficiency.

The minimum phase frequency is given by the equation:

$$f_{\text{min\_phase}} = 2 \times \text{Cell Counts} \times f_{\text{sw}} \tag{3.3}$$

Figure 3.4 illustrates the operating design parameters (ODPs) determined from simulated data, showing the cell count and frequency that yield maximum efficiency for an output current of 2mA within the targeted area. Maximum efficiency is calculated using equation 3.1 for each unique $M + N$ configuration, where the cell count follows the expression $2N + 2M + 1$, based on the respective M and N values. The plot presents maximum efficiency as a function of cell count. This analysis has not yet incorporated considerations for C_{tot} (total capacitance) or area constraints.

The minimum frequency is determined using equation 3.3, with phase duration calculated as

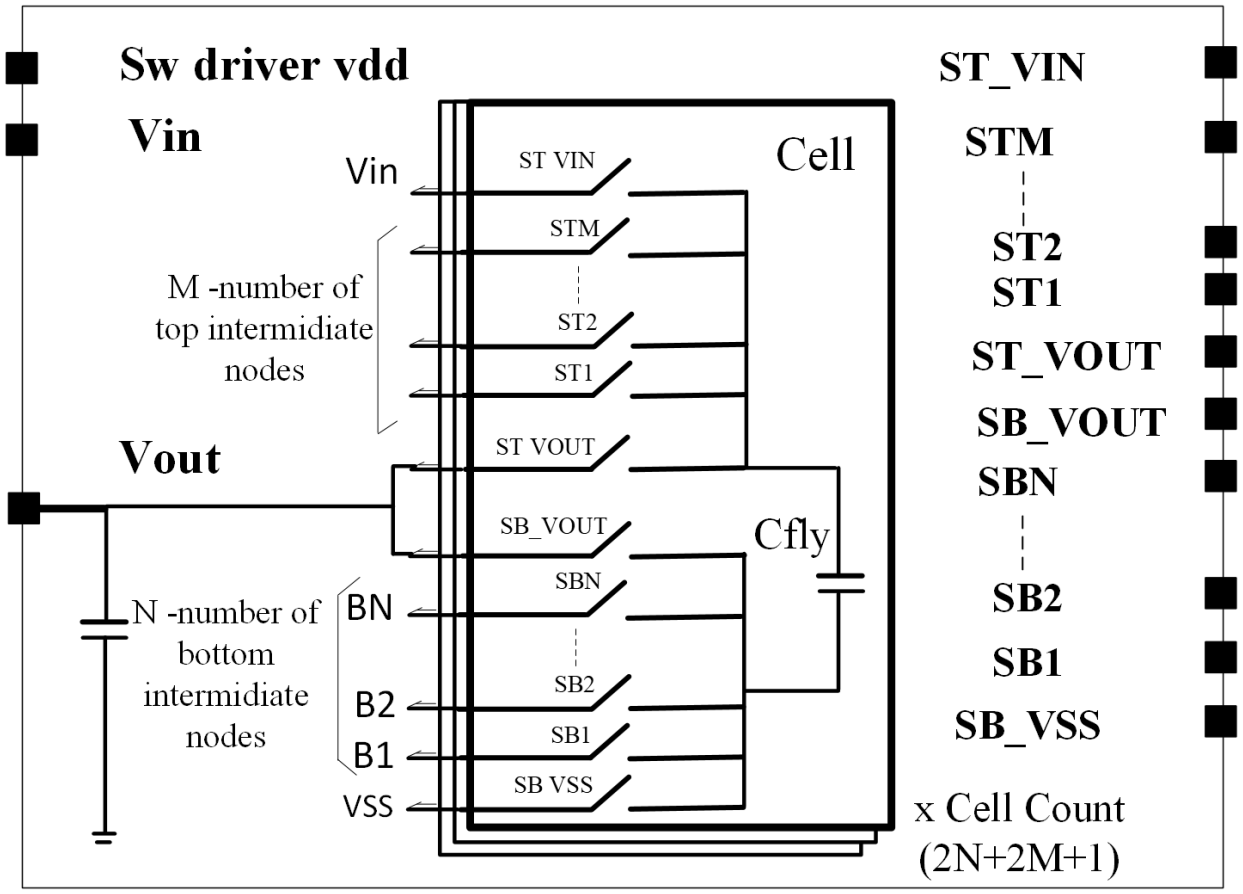


Figure 3.3: Switch-capacitor Core circuit, simulation set up of ODPs

$\frac{1}{f_{\text{min\_phase}}}$. For the targeted area, the maximum allowable capacitance is $C_{\text{tot}} = 1.049\,\text{nF}$ with $C_{\text{out}} = 100\,\text{pF}$. The flying capacitance C_{fly} is calculated as $C_{\text{tot}}/\text{Cell Count}$. As $M + N$ values increase, efficiency is expected to improve while C_{fly} decreases.

Complete charge transfer is influenced by the size of C_{fly}, available charging/discharging time, and switch dimensions. Switches contribute to both the charging and discharging current, and their size impacts transistor driving losses, estimated approximately by $C_{\text{gs}} V_{\text{in}}^2 f_\alpha$. Here, α represents the total number of transitions, approximated as $(N + M + 4) \times 2(2N + 2M + 1)$. Switch sizing and frequency limitations are key considerations for achieving full charge transfer; as frequency increases, the time for charge transfer is reduced, adding complexity to the design.

Simulations are performed across multiple parameter sets to validate the theoretical calcula-

tions. Figure 3.3 shows the simulation setup, where all control signals are ideally sourced. The switched-capacitor core is implemented with transistors, and the stacked capacitor, featuring a density of $5.78\,\text{fF}/\mu\text{m}^2$, is designed using MOS [38], MOM, and MIM capacitors in 65nm technology. An open-loop simulation is performed, and the results are compared with theoretical calculations. Simulated maximum efficiency is achieved with a cell count of 9 at a minimum frequency of 19.2 MHz.

The simulation results closely matched theoretical values up to a cell count of 7, but deviations appeared beyond that. The observed deviation as cell count (N, M) increases is primarily due to two factors. First, as N and M grow, C_{fly} decreases because the total capacitance remains fixed, while the rise in frequency equation 3.3 leads to incomplete charge transfer. Second, non-overlapping signals in the control signals introduce a loss percentage, with the rate of increase accelerating as cell count rises, as expected.

Attempts to mitigate the first factor by increasing switch size are only beneficial up to a certain point. Further increases in switch size raise C_{gs}, resulting in additional losses. Each simulation configuration displayed simulated efficiency at a particular switch size, with efficiency decreasing beyond this operating design point. In this design, the V_{dd} of the driving buffers was varied from 1.8V to 3.2V for configurations with 5, 7, 9, 11, 13, 17, and 25 cells, as shown in Figure 3.5. The operating best performance was achieved with 9 cells at a driver V_{dd} (sw_driver_vdd) of 2V. This demonstrates that further improvement in charge transfer cannot be achieved by adjusting the switch driving parameters without increasing the capacitor size and corresponding frequency that is necessary to achieve the target output current.

However, this design point with maximum efficiency requires an additional voltage source or an additional voltage generation to provide the necessary bias voltage for this operation. The difference in efficiency with sw_driver_vdd values of 1.8V and 2V is less than 1%, meaning that adding a separate bias voltage does not provide significant benefit due to the impact of transistor driving losses.

To determine the design point with fewer simulation data points, we can plot Figure 3.4 showing the maximum efficiency versus C_{fly} (C_{tot}/cell count) and the minimum frequency versus C_{fly}.

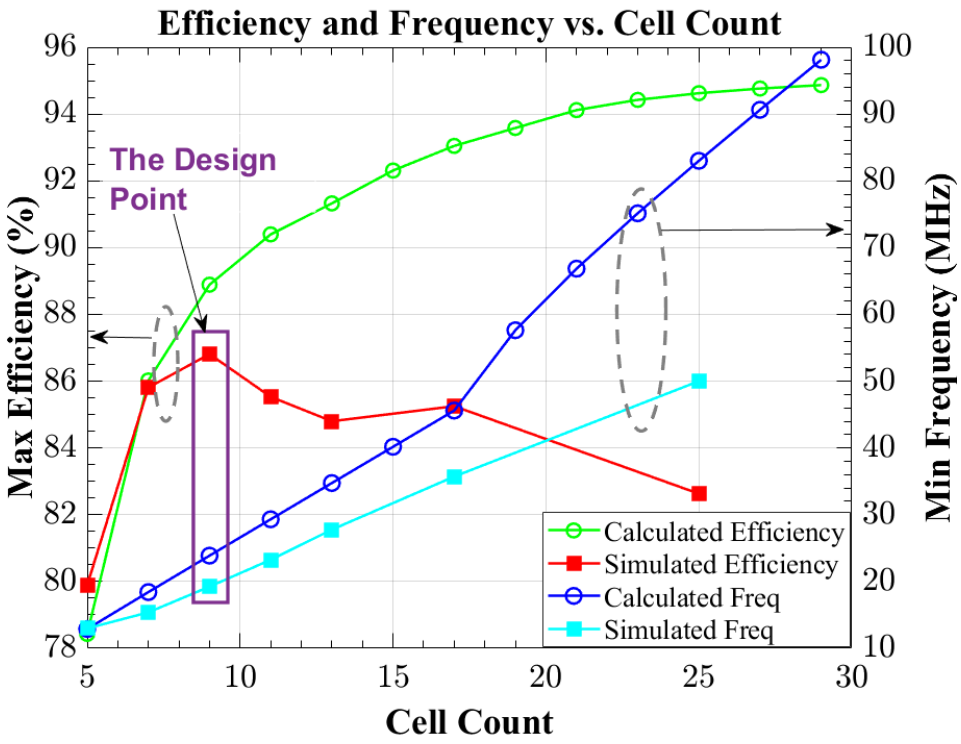


Figure 3.4: Comparison between calculated and simulated Max efficiency, Minimum Frequency vs. Cell count for Vin=1.8, Vout=1.2V at Iout=2mA

As frequency increases with a decrease in C_{fly}, the rate of change in efficiency lags behind the change in minimum frequency, creating a quasi-design point. By simulating the behavior at three key points—below the quasi-design, at the quasi-design, and above the quasi-design—the operating design point can be identified quickly, eliminating the need for simulating multiple sets of parameters.

While this approach simplifies the path to the design point, it may not always be fully sufficient. In some cases, more detailed simulations with varying parameter sets might still be needed to capture the full complexity of the system and ensure robustness under different operating conditions. Nevertheless, this method provides a good starting point for identifying the best operating design before conducting more point simulations.

Leveraging the efficiency and frequency equations, we can determine the maximum efficiency and minimum frequency for a given area, with simulated verification, alongside other design pa-

rameters such as cell count, C_{fly}, and M, N. The design point parameters, with a 0.4mm² area, $C_{\text{fly}} = 116.55\,\text{pF}$, frequency = 19.2 MHz, and Cell Count = 9 (M, $N = 1, 3$), achieve an efficiency of 88.9% as calculated and 86% in simulation (with non-overlapping signals in an open-loop setup). The fully integrated system will be discussed in Chapter 4 as follows by Operating Design Parameters (ODPs). A modest efficiency improvement and a better match with calculated efficiency are anticipated in the system-level implementation with non-overlapping controls.

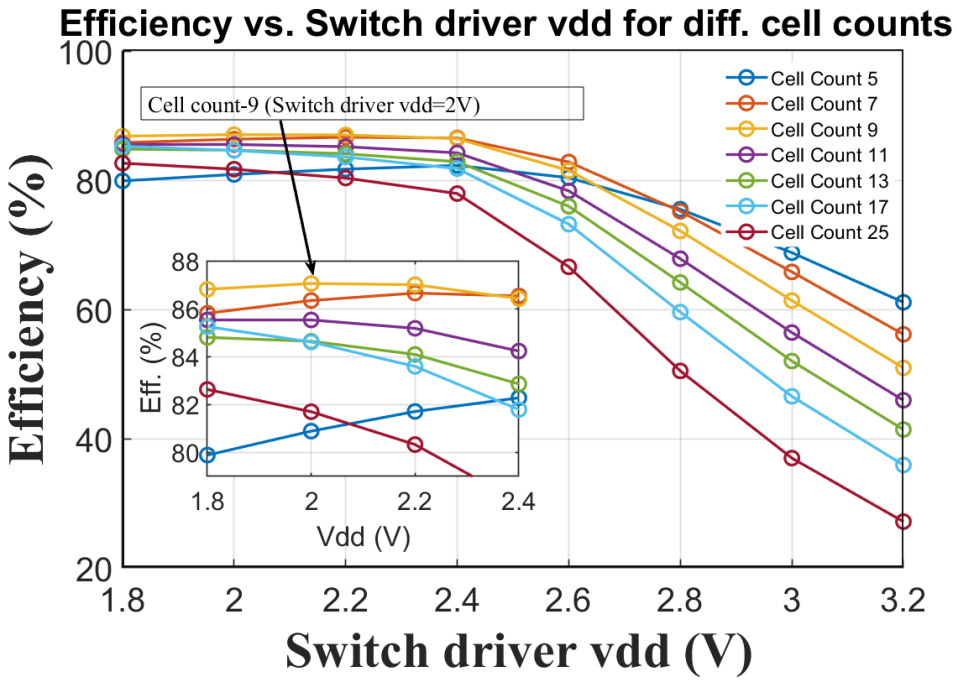


Figure 3.5: Efficiency vs Switch Driver vdd for different Cell count; with Vin=1.8, Vout=1.2V and Iout =2mA

3.3 Summary of Design Approach Steps

Step 1: Total Capacitor Size Estimation Based on Area Requirement

Determine the total capacitance C_{tot} based on the area target or requirement: allocate 75–80% of the area for capacitors.

Step 2: Operating Design Parameters (ODPs)

Max Efficiency and Min Frequency vs Cell Count

Calculate the maximum efficiency and minimum operating frequency, which define the phase duration across cell counts for each unique $N + M$ value using the given equation 3.1 and equation 3.3.

Perform simulations using the switched-capacitor core design, including transistors and capacitors from the 65nm CMOS technology PDK with ideal signal sources as control for simplicity and comparison. While non-overlapping signals are used for simulations to reduce simulation design work.

Simulation Strategy

Begin with simulations at three key points (discussed in Section 3.2); if these are insufficient to locate the maximum efficiency point, simulate additional points as needed. In brief, the quasi-design point can be chosen from calculated maximum efficiency and minimum frequency vs C_{fly}, where C_{fly} is calculated from $C_{\text{tot}}/\text{cell count}$, at the point where the efficiency change rate lags enough compared to the frequency change rate as C_{fly} decreases or N, M increases (or cell count increases).

Identify the design point-operating parameters by selecting parameters based on simulation results of these three quasi-design points that achieve the best performance.

Design Parameter Documentation

Record all ODPs at the design point, including cell count, operating frequency, flying capacitance (C_{fly}), and N and M values.

Implementation Phase

With the operating parameters defined, proceed to the system implementation.

Chapter 4

Fully On-Chip System Design Implementation with 0.4 mm² area

This section outlines the fully integrated system implementation, using the operating design parameters (ODPs) for design point established in Chapter 3. The primary objective of this work is to design a fully on-chip soft-charging switched-capacitor (SC) step-down converter that efficiently converts voltage from 1.8V to 1.2V with a 2mA load.

4.1 Soft-Charging Switch-Capacitor Core Implementation

Based on the design approach detailed in Chapter 3, the proposed implementation leverages Operating Design Parameters (ODPs) within a 0.4 mm² area. A soft-charging switched-capacitor (SC) core is implemented with top intermediate nodes $M = 1$, bottom intermediate nodes $N = 3$, and $M+N = 4$, corresponding to a cell count of 9 (calculated as $2N+2M+1$). This phase-shifted core is designed using 3.3V I/O devices in a 65nm CMOS technology, with the design parameters listed in Table 4.1. Charge transfer is achieved over 18 phases (2 × cell count), targeting a fixed Voltage Conversion Ratio (VCR) in a Continuous Switched-Capacitor Ratio (CSCR) topology. The system is designed to operate with $V_{\text{in}} = 1.8\,\text{V}$ and $V_{\text{out}} = 1.2\,\text{V}$, supporting a 2 mA load. Figure 4.1 illustrates the block diagram of the fully on-chip integrated system, designed to meet

these specifications.

Table 4.1: Implemented design Parameters for 9 cell with M=1, N=3 top/bottom intermediate nodes

Design Parameters	Value
Cfly	114.91pF
Cout (on-chip)	105.5pF
Frequency (f_phase_min)	13MHz
CLK frequency from VCO (Vctrl=1.5V)	44MHz
Vin	1.8V
Vref (Vout)	1.2V
Delay (dead time)	1ns

The outphasing operation is discussed in detail in Chapter 2. Fundamentally, the cornerstone phases, D_1 ($V_{\text{out}} - V_{\text{ss}}$) and D_2 ($V_{\text{in}} - V_{\text{out}}$), have phase durations that are half of the phase durations of the soft-charging top and bottom nodes; such that the durations of B_1, B_2, B_3, and T_1 are double those of D_1 and D_2. Each core will be 2-phase shifted. Figure 4.2 shows the phases per cycle for a single core.

4.2 Closed-loop control Implementation for soft-charging SC fully integrated on-chip converter

A closed-loop control system is designed for a fully integrated soft-charging switched-capacitor (SC) converter to efficiently regulate V_{out}. The system includes a latch-comparator and a voltage-controlled oscillator (VCO) that generates the clock signal serving as the latch-comparator's clock input. When V_{out} is zero initially, the comparator output exhibits the highest available frequency

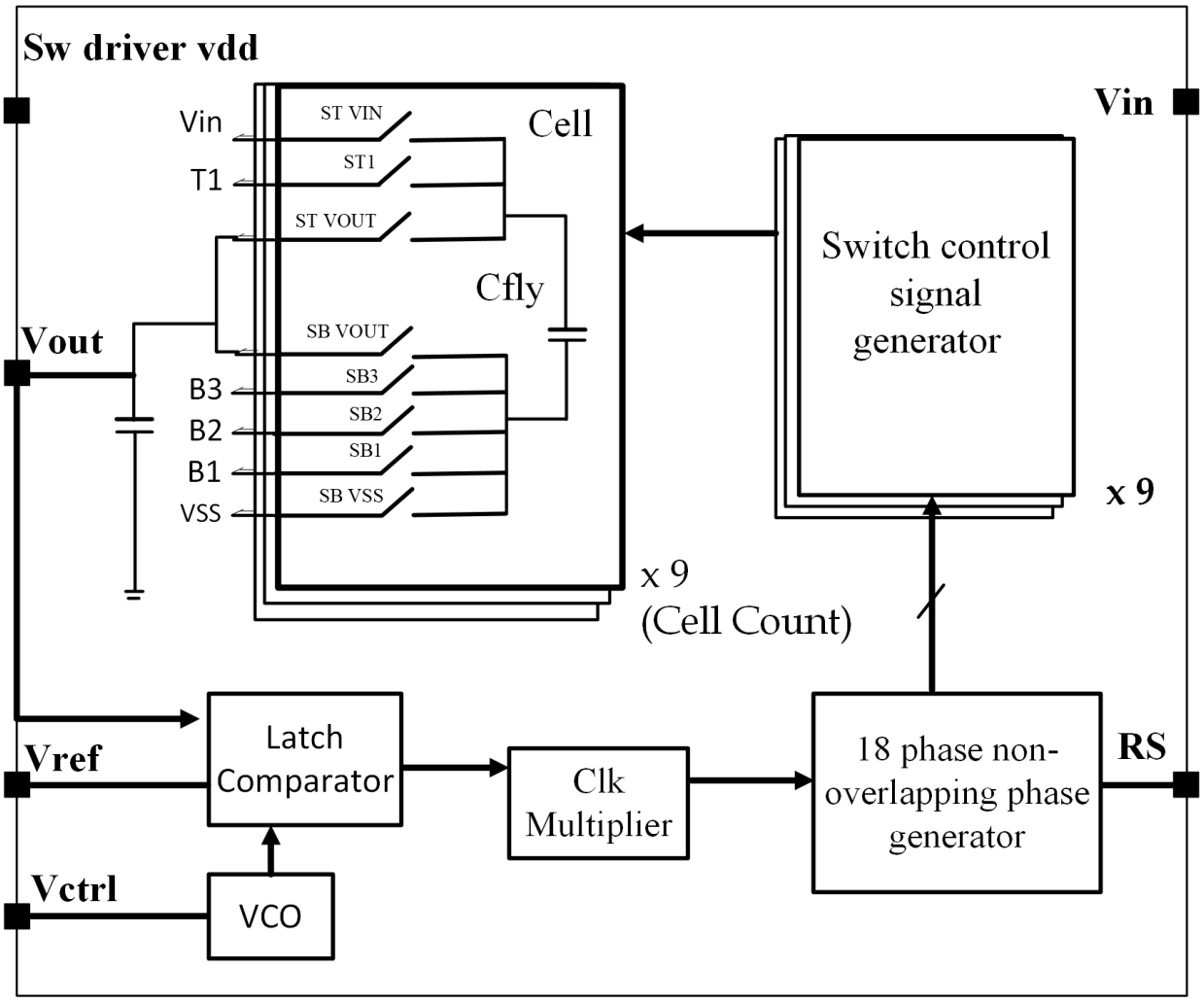


Figure 4.1: Overview of the fully integrated on-chip system

provided by the VCO, ensuring fast recovery. Conversely, when V_{out} exceeds V_{ref}, the comparator output initiates pulse-skipping, thereby reducing switching frequency and improving efficiency.

The comparator output and its delayed signal go to the inputs of an XOR gate, which functions as a clock multiplier. This setup effectively generates the necessary dead time for the non-overlapping phase generator. Figure 4.3 illustrates the output of the clock multiplier, CLK_{mult}, signal generated based on the input signals, where signal A corresponds to Comp_{out} and signal B represents the delayed version of Comp_{out}. The output from the clock multiplier, CLK_{mult}, serves as the clock input to the non-overlapping phase generator, as shown in the circuit diagram in Fig-

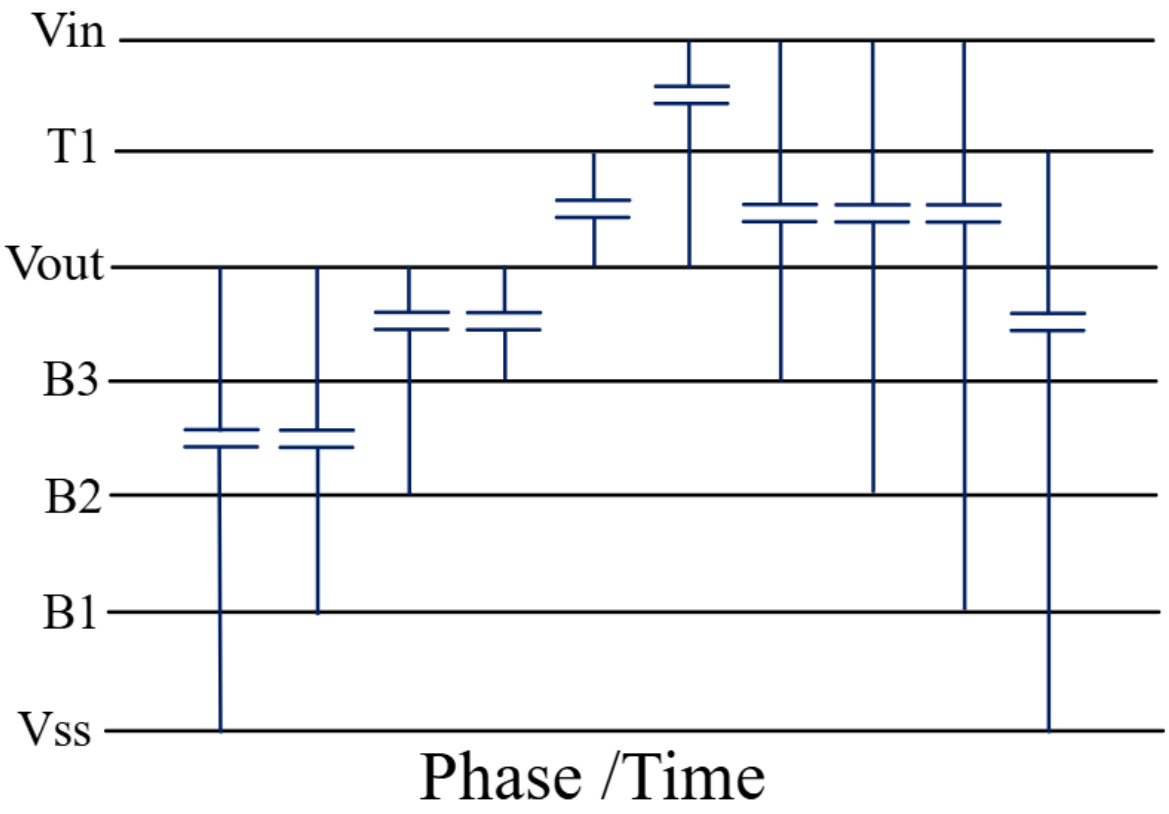


Figure 4.2: Phase diagram per cycle for a each Cell (Cfly) with N=3, M=1 Cell count 9 as per ODPs

ure 4.4. The generator consists of D flip-flops connected sequentially, with the final stage output fed back to the first stage input. A preset at the first stage ensures proper initialization, while the subsequent stages use a clear signal for the same purpose. The RS signal, which is active low, facilitates initialization when RS $= 0$. The circuit begins by initializing and, once RS $= 1$, introduces delays through each stage. Any variations in CLK_{mul} directly influence the phase duration, enabling the generation of the required phase signals based on comparator decisions.

These phases serve as inputs to generate control signals for the soft-switching outphasing operation. Figure 4.5 depicts the circuit used to generate each switch signal, where the primary purpose of the SR latch is to eliminate unnecessary transitions and ensure effective switching. All switch signals ($N + M + 4$) are shown in Figure 4.6. Additionally, Figure 4.7 illustrates the capacitor's

top and bottom plate voltages, indicating six intermediate bottom nodes and two intermediate top nodes. This aligns with expectations, as outphasing doubles the number of intermediate nodes without adding extra switches or core components, confirming the effective operation of the outphasing mechanism.

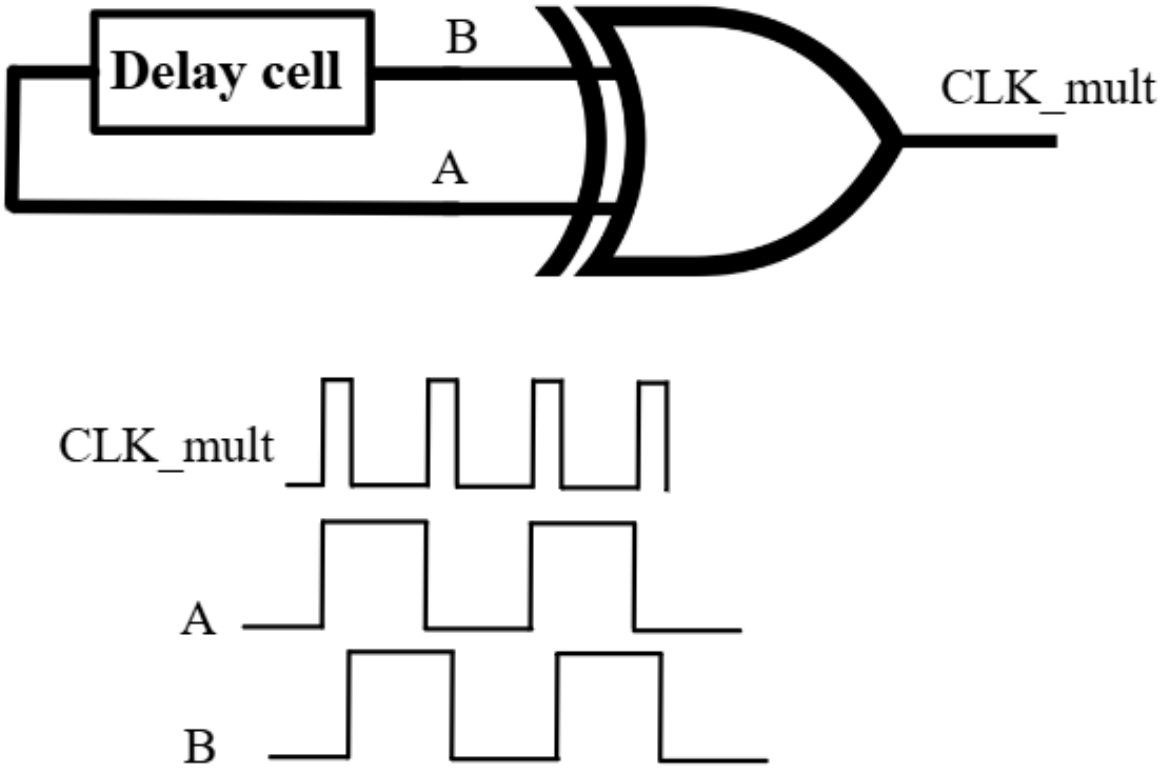


Figure 4.3: Clock multiplier circuit, generating deadtime for non-overlapping phase generator

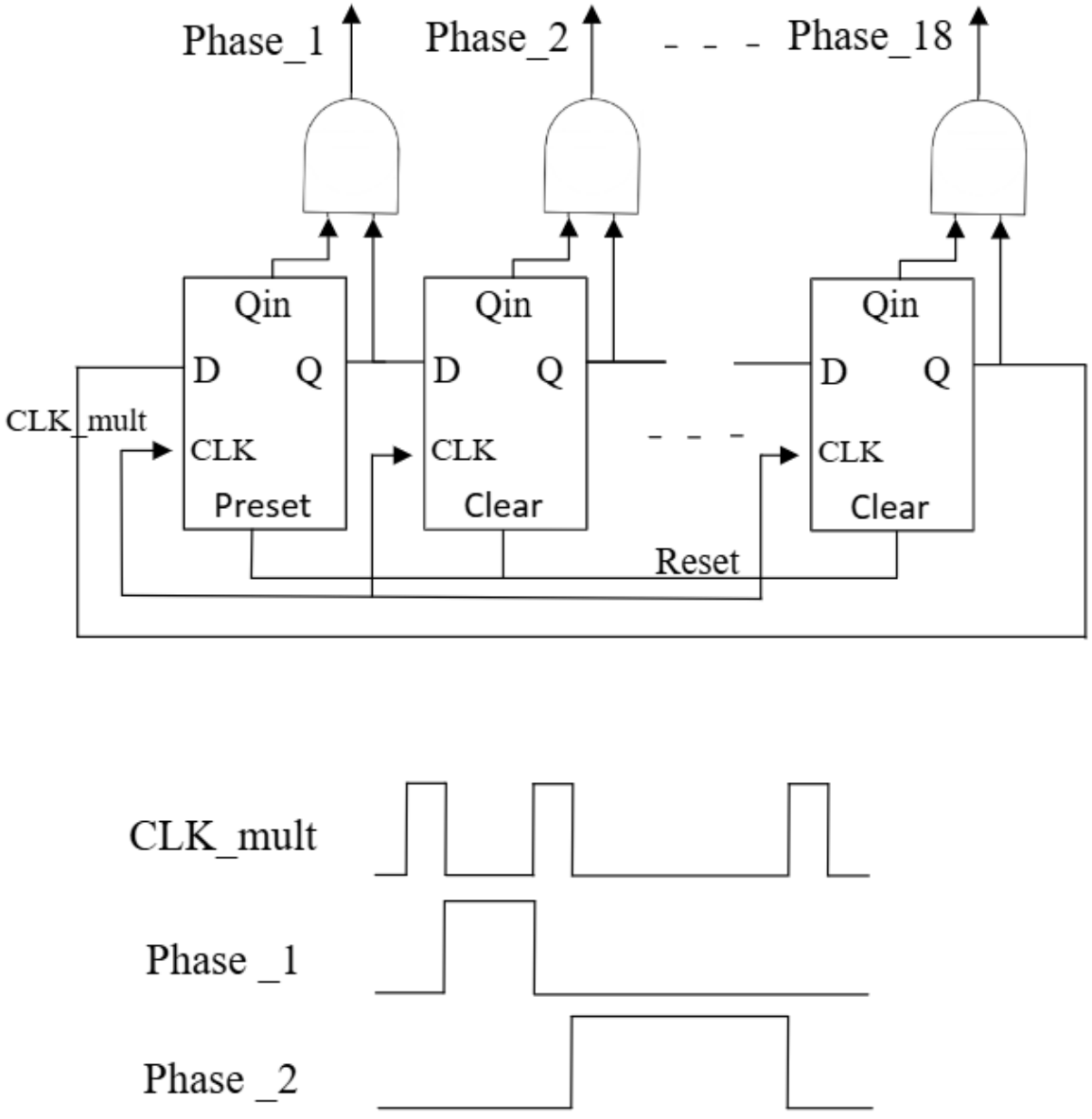
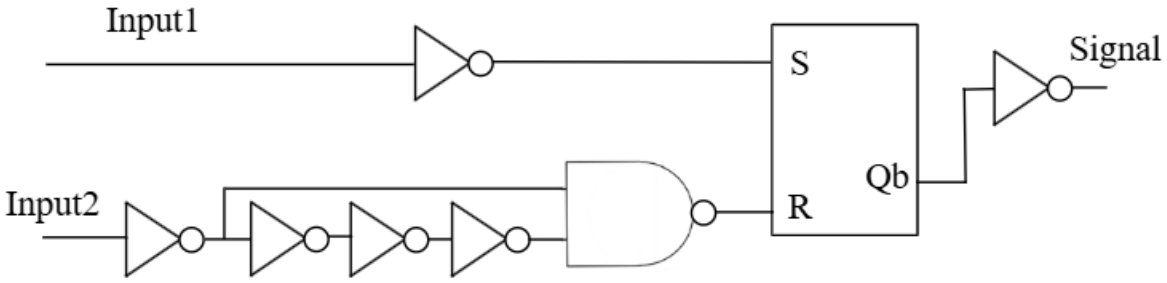


Figure 4.4: Non-overlapping phase generation circuit.



Number of switch -> (N+M+4)
Control Signal->Inputs
ST_Vout -> P1,P(2N+1)
SB_Vout-> P (2N+2),P(2N+2M+2)
ST_Vin->P(2N+2M+2),P(4N+2M+2)
SB_VSS-> P(4N+2M+3), P1
ST_a-> P(2N+2) & P(4N+2M+3) ,P(2N+2M+1)&P(4N+4M+2)
SB_b->P(b+2) & P(2N+2M+b+3) , P(b+3)&P(2N+2M+b+4)
a=1, 2 ,3 ...M
b=1, 2, 3....N

Figure 4.5: Control signal generator for soft-charging outphase SC core operation across all switches.

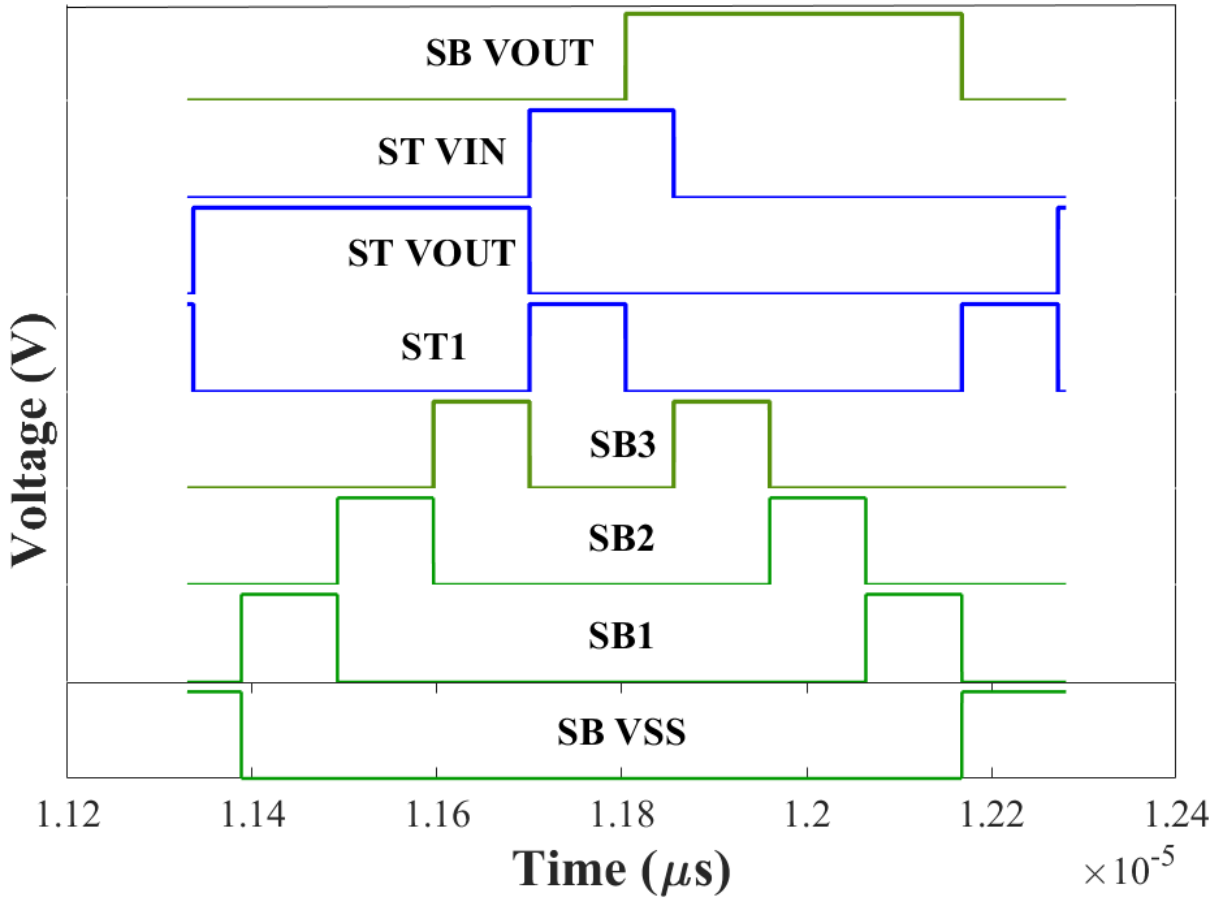


Figure 4.6: All switch signals for a 9-core implementation with M=1 and N=3.

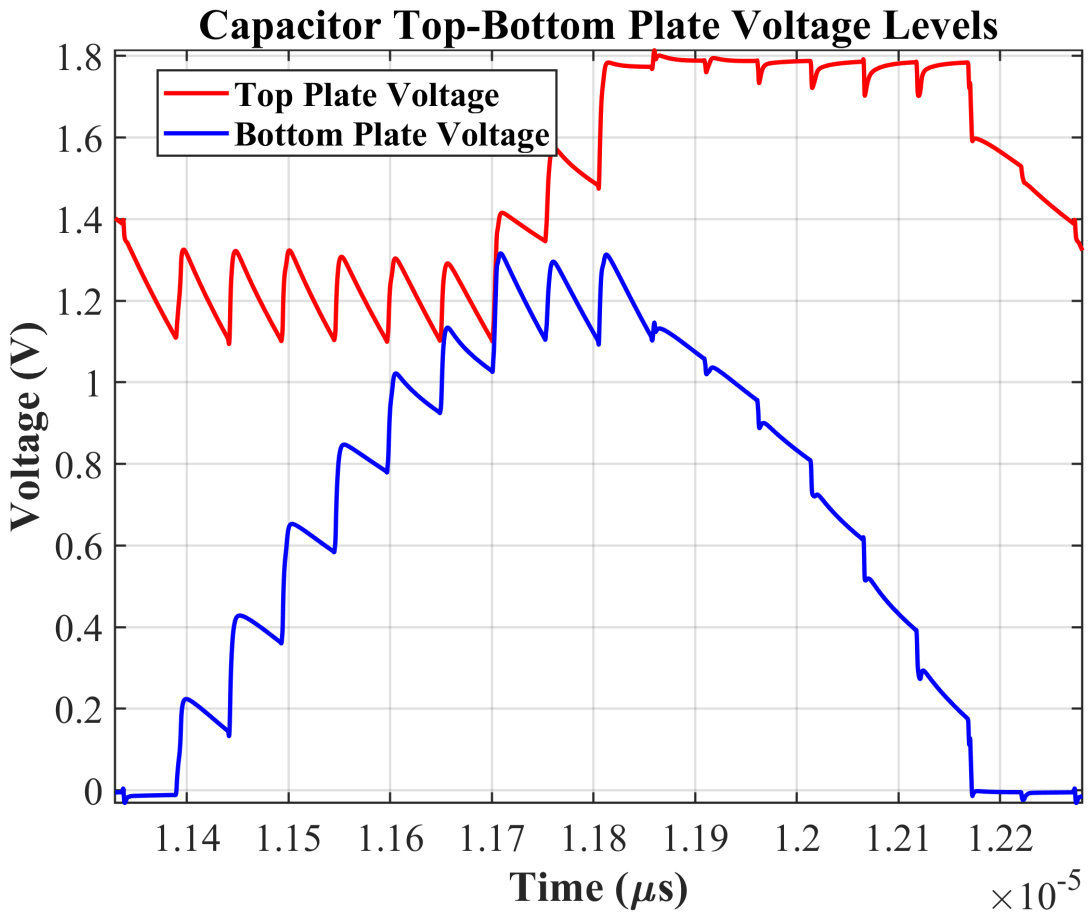


Figure 4.7: Capacitor top and bottom voltage levels for each core per cycle with M=1, N=3.

Chapter 5

Simulation Results and Evaluations

This section presents the results of the fully integrated on-chip soft-charging SC step-down converter with outphasing operation, developed using operating design parameters (ODPs) for design-point outlined in Chapter 3 and design implementation. The system block diagram is shown in Figure 4.1.

The results focus on evaluating the proposed design approach for determining design-point ODPs and assessing the effectiveness of its implementation. Key aspects analyzed include the transient response of the integrated system, efficiency performance across load current, the narrowed Voltage Conversion Ratio (VCR) range, and their associated trade-offs. These evaluations validate the system's ability to meet its design objectives and specifications, demonstrating its contribution to advancing the standards of soft-charging SC converters, particularly in terms of power density (PD) for compact and seamless e-textile sub-mA-load-fixed-VCR applications.

5.1 Transient Analysis : fully on-chip integrated

The transient analysis includes the output voltage V_{out}, reset signal (RS), and comparator output signal. The system requires a V_{ctrl} bias of 1.5V for the VCO circuit. The load varies from 1 µA to 2 mA within nanoseconds. The ripple, measured with $C_{\text{out}} = 105$pF, is 240 mV. The fully integrated on-chip implementation meets the required specifications without adding any off-chip

components. While the ripple is slightly higher, increasing the on-chip C_{out} can help to reduce it.

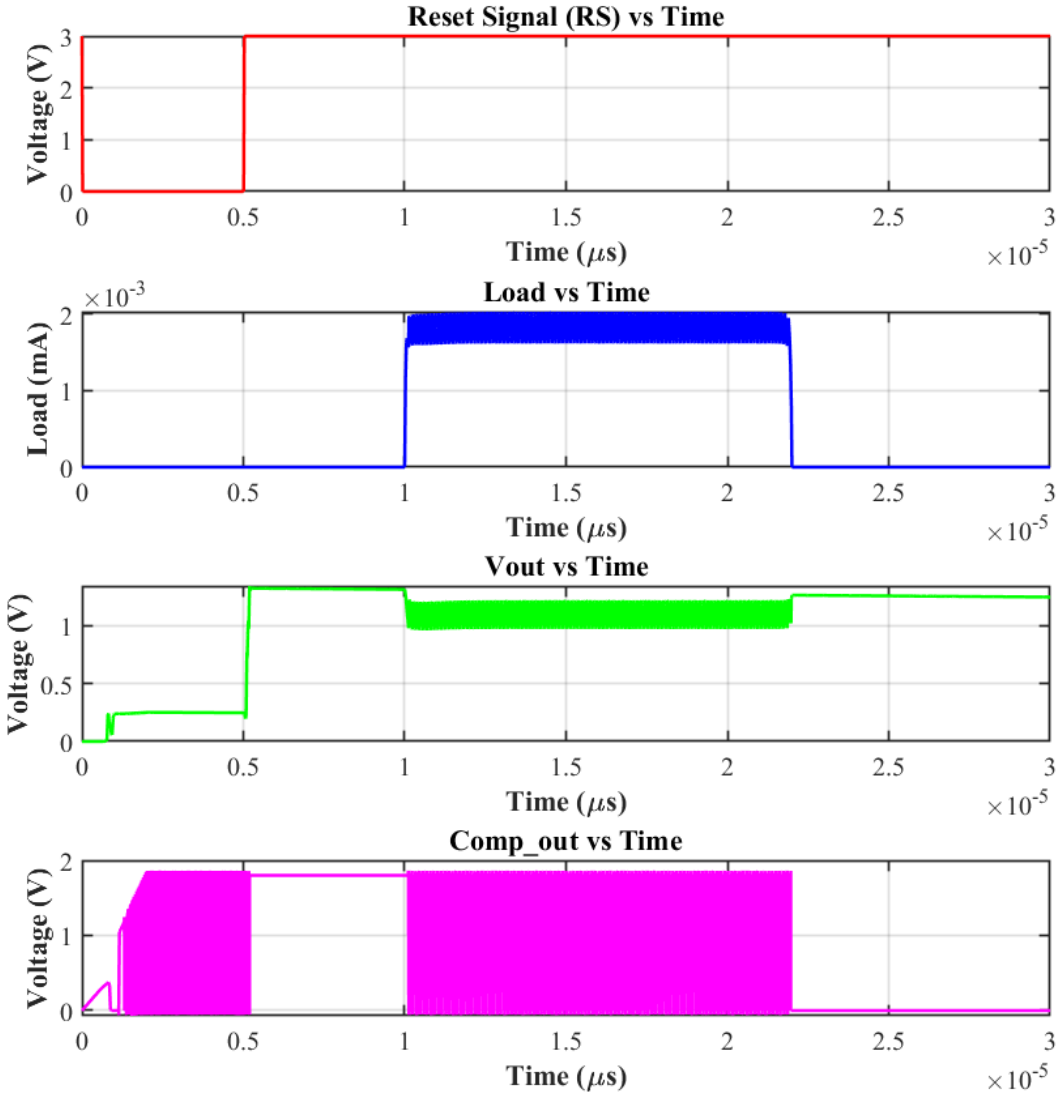


Figure 5.1: Transient analysis : Reset signals (RS), Load, Vout and Comp out.

5.2 Efficiency across load

The efficiency is evaluated across a load current range of 0.15 mA to 2 mA. Simulations show a peak efficiency (η_B) of 85.4%, achieved at a load current of 0.8 mA using 0.4 mm² design-point ODPs. Figure 5.3 highlights the performance of the 0.4 mm² ODPs, achieving an efficiency (η_A) consistent with the calculated results for a maximum load of 1 mA. While the ODPs may not fully align with the calculated performance for a 2 mA load, they provide a solid foundation for future optimization. This figure also compares η_A and η_B efficiencies across load currents for switch driver V_{dd} of 1.8 V and 2 V. Although efficiency is slightly higher at $V_{dd} = 2\,V$, the difference is minimal compared to 1.8 V. However, implementing a 2 V V_{dd} would require an additional bias circuit, increasing the required area. To achieve the calculated efficiency at 2 mA, it requires higher phase durations increasing C_{fly} size or reducing the load current. Within the fixed area constraints for a 2 mA load current, this design demonstrates best performance. In earlier chapters, it was assumed that the overall system implementation, including non-overlapping signals, would enhance efficiency (η_A) a bit, as the earlier analysis was done with non-overlapping signals. However, losses due to incomplete charge transfer, larger switch sizes, and driving losses contribute to reduced efficiency compared to the calculation. Despite these challenges, this design achieves the maximum efficiency for a 2 mA load with a compact 0.4 mm² area.

5.3 Narrow VCR

Scalability is the primary goal of this implementation, necessitating a compact design footprint. The application targets a fixed VCR-based textile system operating under sub-mA load conditions. To achieve this, the design constrains capacitor sizes and related parameters, which inherently limits the VCR operating range. Figure 5.3 presents the simulated VCR range for switch driver supply voltages (V_{dd}) of 1.8V and 2.0V, compared to the calculated range. Despite a narrower simulated VCR range, efficiencies of 80% or higher are maintained. The simulated VCR range is from 0.55 to 0.72 for $V_{in} = 1.8\,V$ with a 2 mA load. While efficiency slightly improves with $V_{dd} = 2.0\,V$, the VCR range remains consistent with that at $V_{dd} = 1.8\,V$. Figure 5.4 depicts the

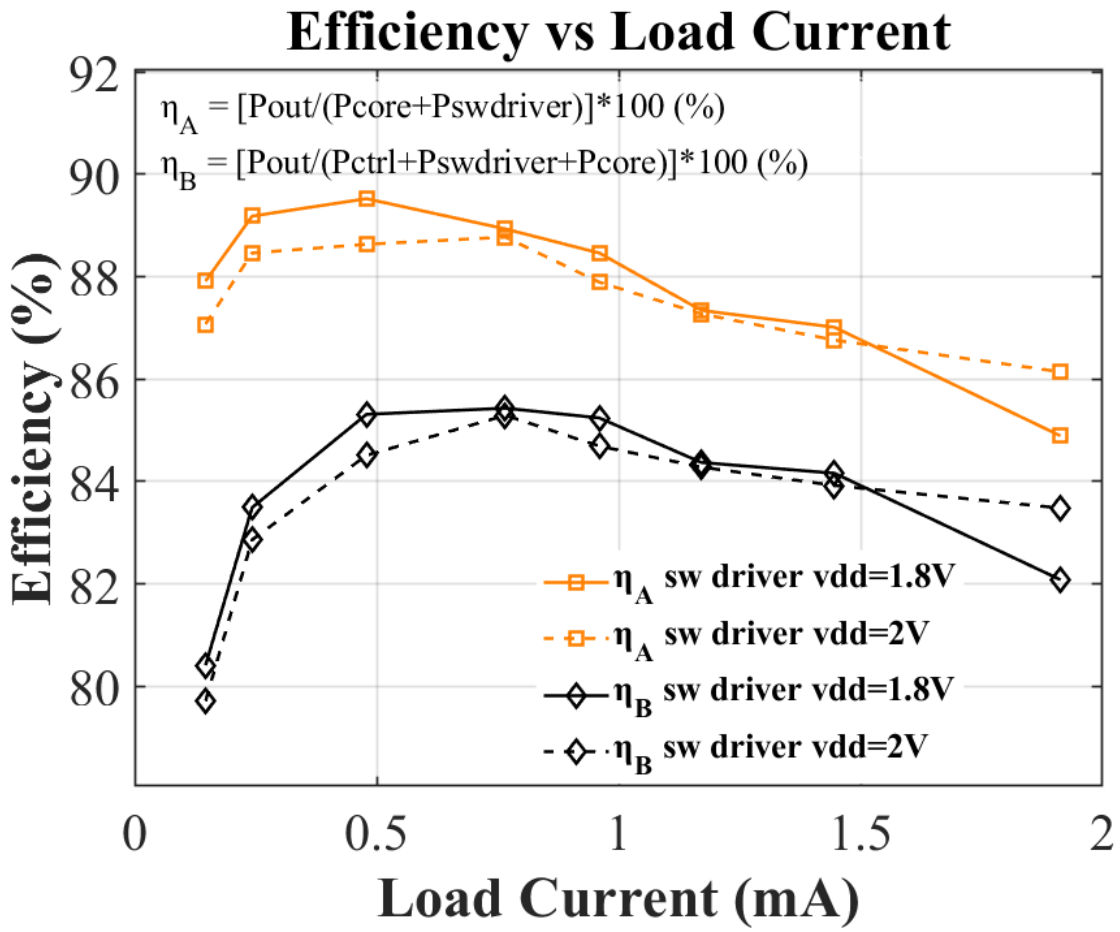


Figure 5.2: Simulated efficiency across load 0.15mA -2mA at ODPs with 0.4mm2 for Vdd (switch driver vdd) 1.8 and 2V.

output voltage (V_{out}) varying from 0.7V to 1.3V across load currents ranging from 0.15 mA to 2 mA. These results confirm the achieved efficiency under the specified conditions.

5.4 Design Implementation with design-point ODPs for 0.6mm²

In this section, the proposed method outlined in Section 3 for ODPs has been applied for a 0.6 mm² area. This is followed by the system implementation, with the design-point ODPs illustrated in Figure 5.5 and the simulated system results shown in Figure 5.6. These results validate the proposed method for identifying ODPs, their implementation, and the overall system performance.

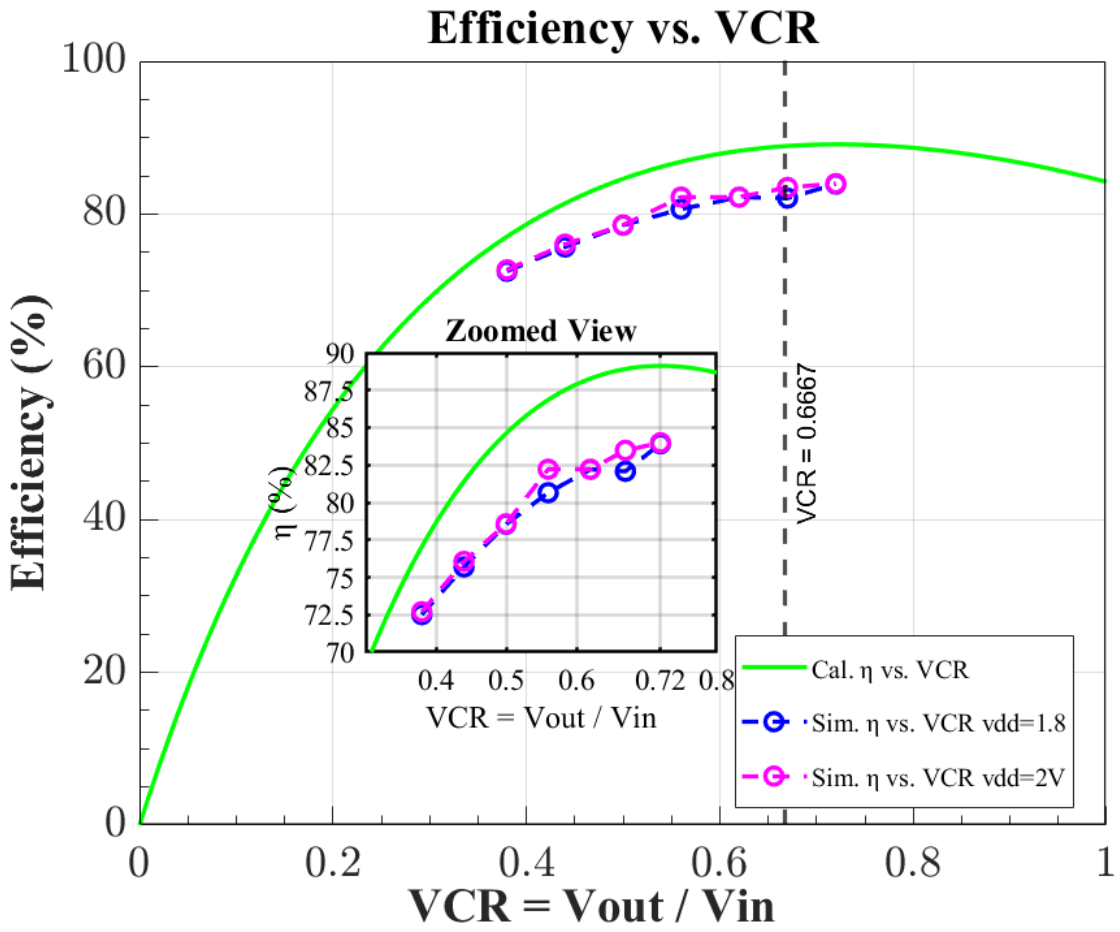


Figure 5.3: Comparison between calculated and simulated VCR range with fully integrated converter, simulated VCR range for switch driver Vdd 1.8 and 2V at Iout=2mA with Vin=1.8.

While the detailed analysis focuses on a 0.4 mm² area compared to 0.6 mm², the intended purpose has been successfully achieved.

5.5 Comparison with state-of-art designs

A comparison table is provided to benchmark the proposed design against state-of-the-art implementations. Key performance metrics, peak efficiency, VCR range, load current range, power density (PD), and footprint, are highlighted to demonstrate the advantages of the proposed approach, particularly in low-load, space-constrained textile applications. Figure 5.7 illustrates that

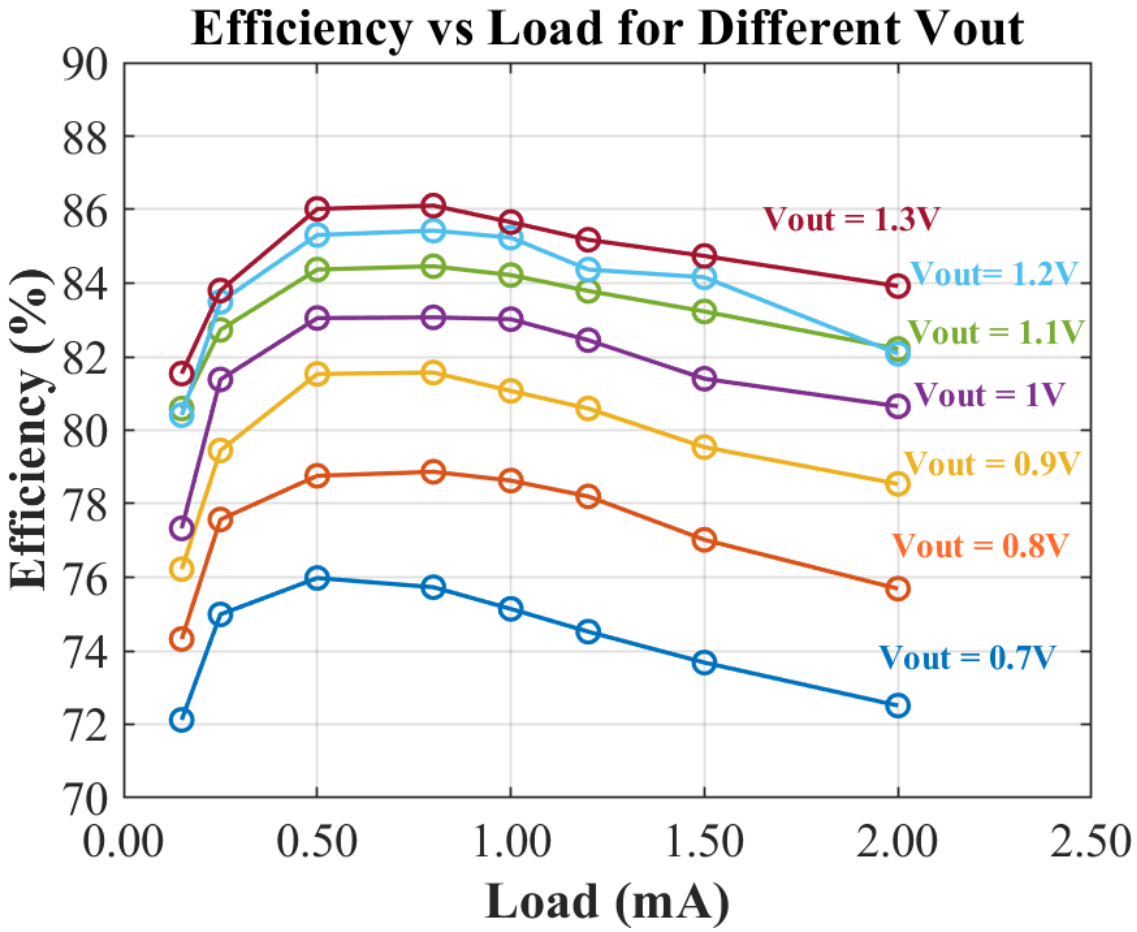


Figure 5.4: Efficiency vs load current with different Vout, 0.7V to 1.3V with Vin=1.8V at Iout=2mA

the proposed design achieves a higher PD at operating design parameters (ODPs) compared to state-of-the-art designs with loads under 5 mA. It also emphasizes enhanced efficiency and PD within a fully integrated comparison for certain low load conditions. By improving PD in low-load conditions, this design addresses a critical gap, achieving the goal of a miniature implementation tailored for textile applications. Overall, the proposed method optimizes the design process for targeted applications, ensuring better performance and successfully meeting the objectives while setting a new standard for efficiency concerning power density (PD) for miniature seamless e-textile applications. Figure 5.8 also illustrates the visualized design space achieved by the proposed approach in comparison with state-of-the-art designs, focusing on efficiency versus area. It high-

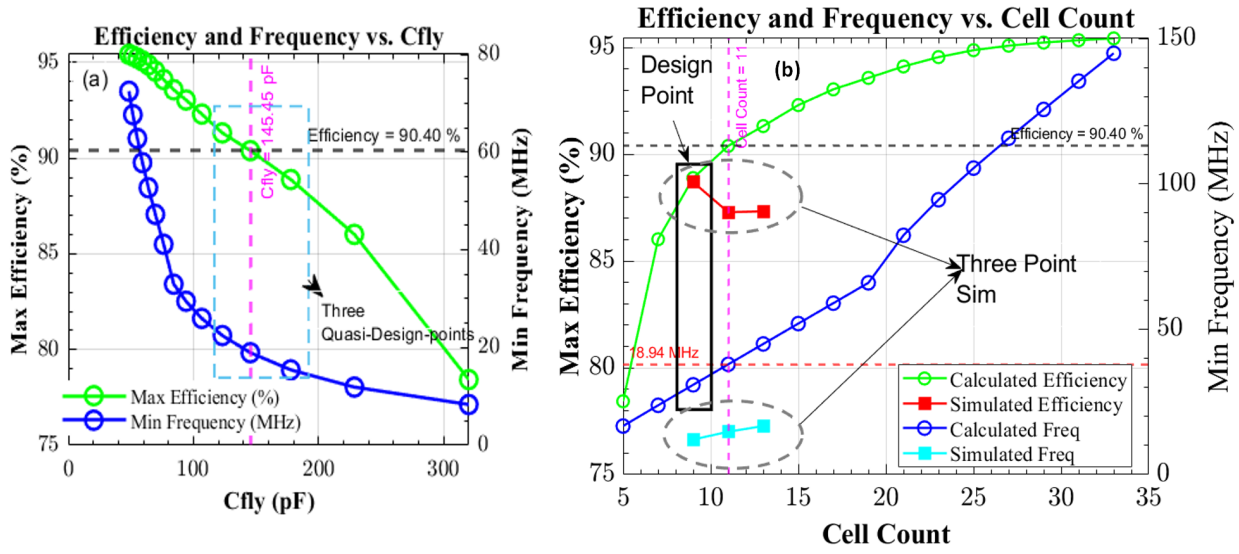


Figure 5.5: (a) Quasi-design Three Points (b) Comparison Between Calculated and Simulated Efficiency and Frequency, with the operating design parameters for design point point (ODPs).

Table 5.1: Implemented design Parameters for 9 cell with M=1, N=3 top/bottom intermediate nodes with 0.6mm²

Design Parameters	Value
Cfly	177.7 pF
Cout (on-chip)	105.5pF
Frequency (f_phase_min)	13 MHz
CLK frequency from VCO (Vctrl=1.5V)	44MHz
Vin	1.8V
Vref (Vout)	1.2V
Delay (dead time)	1ns

lights the targeted design space successfully attained by this work, showcasing its optimization for compactness and efficiency in space-constrained applications.

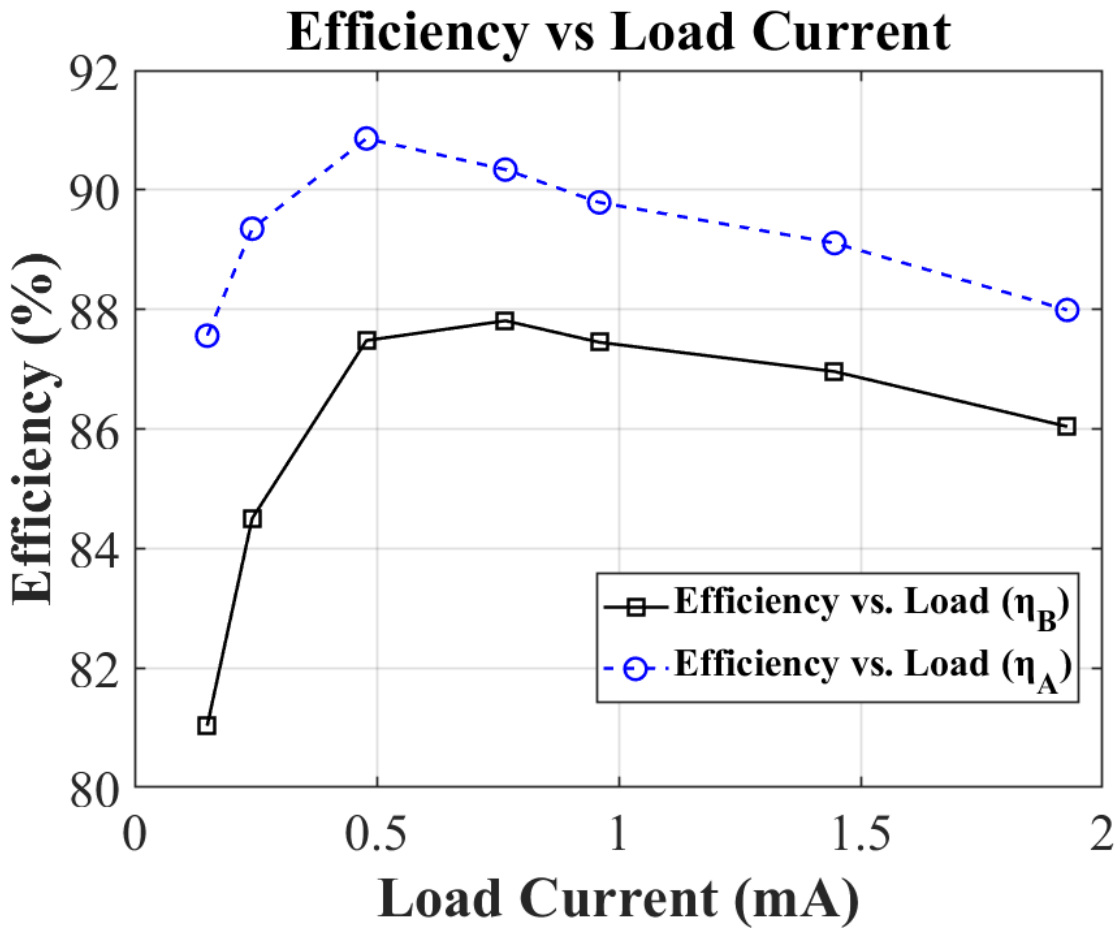


Figure 5.6: Efficiency vs. load current for both $\eta_A = \left(\frac{P_{\text{out}}}{P_{\text{core}}+P_{\text{swdriver}}}\right)$ and $\eta_B = \left(\frac{P_{\text{out}}}{P_{\text{core}}+P_{\text{swdriver}}+P_{\text{ctrl}}}\right)$

5.6 Discussion & Summary

This design balances a trade-off between capacitor size, which reduces the overall area (the primary objective), and both the VCR range and efficiency. Despite these compromises, the design achieves moderately high operational efficiency and a narrowed VCR range, making it suitable for space-constrained applications where maintaining reasonable efficiency is crucial.

The proposed design approach effectively identifies the operating design parameters (ODPs) that maximize efficiency for specific areas. Simulated results confirm that the design objectives are met with footprints of 0.4 mm² and 0.6 mm², Peak efficiencies of 85.4% and 87.8% respectively.

Table 5.2: Comparison with State-of-Art Designs

	JSSCC'2019 [9]	ISSCC'23 [11]	JSSCC'21[13]	JSSCC'17[14]	Electronics'22 [15]	TCAS-I'20 [16]	TCAS-I'2022 [17]	ISSCC'21[20]	**This Work**
Tech.(nm)	28	65	180	28	180	180	28 -FDSOI	40	65
Topology	Soft charging -outphasing	Reconfigurable VCR step CSC(RCSC)	Dual mode CSCR SC	Dickson with multiphase	Phase reduced Soft charging	Soft charging based boost SC	CSCR w/ sw matrix	SPCR	Soft charging -outphasing-Fixed-VCR in CSCR
Area (mm^2)	1.05	4.76*	3.89	0.117	4.9	1.75/5.84	4.82*	2.43*	**0.4**
Peak η (%)	**93**	83.9 @fixed **90 @reconfig.**	85.4	**82**	82.6 @54uW	85.3/83.6	88.9	**94.6**	**85.47**
Fully on-chip	No	**Yes**	No	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**	**Yes**
PD (mW/mm2)	4.6 (@ 93%) 4.95*	**6.3 @ fixed 6.93@ reconfig.**	5.34*	1100	0.011*	0.668/0.359	0.58*	1.3@Peak 1.6*	**5.781**
Vin (V)	2	0.4-2.5	0.1-.5	3.2	0.5-1.2	0.95-1.8	0.65-1.5	1.855-2.07	1.8
Vout (V)	0-2.22	0.5-2	0.75	0.95	1.2-1.8	1.8 /3-4.2	<2	0.7	0.7-1.3
VCR Range	0.25-1.1* @ >80%	.5-1/1.25-1.33 * @ >80 %	2.4-5.33* @ >80%	0.33	1.5-2.4	1-1.89 /2.14-6.56	.35-.55/.66-2.3 * @ >80 %	0.43-0.49* >@88%	0.55-0.72>80%
Frequency (MHz)	20 (Max)	20 (Max)	0.015-0.067	1600	0.3- 2	09-2.7	0.054-3.4	50	13
Load current (mA)	3	19.8	20*	126	0.0364	0.650/0.700*	1.5*	34*	150uA-2mA
Output power (uW)	5.4*	31mW/39.7mW	20.8mW	119.7mW	54 @ 82.6%	<1.17/<2.1mW	2794	3.83mW*	2400
Ripple (mV)	NR	NR	<20 @10uW/1mW	NR	50mV@36.4uA	50 @ 200uA & 1nA	NR	18	240 @ 2mA
Cfly(Total)	9.5nF	19.8nF	7.8nF	1.5nF	4.6nF	5.5nF/19.8nF	15nF	10nF	**1.034nF**
Additional cap	780pF	N/A	0.47uF /2.2uF	N/A	N/A	N/A	N/A	N/A	Cout- 100.4pF
N,M (Int. Nodes)	N+M=32	N+M= 16	N=4,M=10	N/A (6 phase)	N=9,M=13	N=39,M=11	N,M -NR cell-48	N=16	**N+M= 4**

Notes - NR- Not Reported * -calculated from Figures

The fixed/narrow VCR approach helps improve Power Density (PD) by reducing the area required for low-load applications (under 5mA), as demonstrated in comparison with state-of-the-art designs. From the literature, existing low-current switching designs generally exhibit low power density (PD), while high-load designs achieve higher PD but often suffer from lower efficiency when operating at low loads, as they are optimized for high-power delivery. By improving PD in low-load conditions, this design addresses a critical gap, achieving the goal of a miniature implementation tailored for textile applications.

The idea of achieving a smaller area by compromising efficiency and VCR range proved effective. The out-of-phase operation complements the compact area target, enabling a significant improvement over state-of-the-art designs implemented in 65nm technology.

In summary, this design method focuses on optimizing key parameters, such as capacitor size with out-of-phase operation, to achieve compact and efficient system designs for fixed/narrow VCR sub-mA-load textile application. It is particularly well-suited for applications with stringent space constraints, such as wearable devices, IoT nodes, and biomedical implants, where minimizing the design footprint is critical. However, the soft-charging mechanism itself is not area-efficient, as

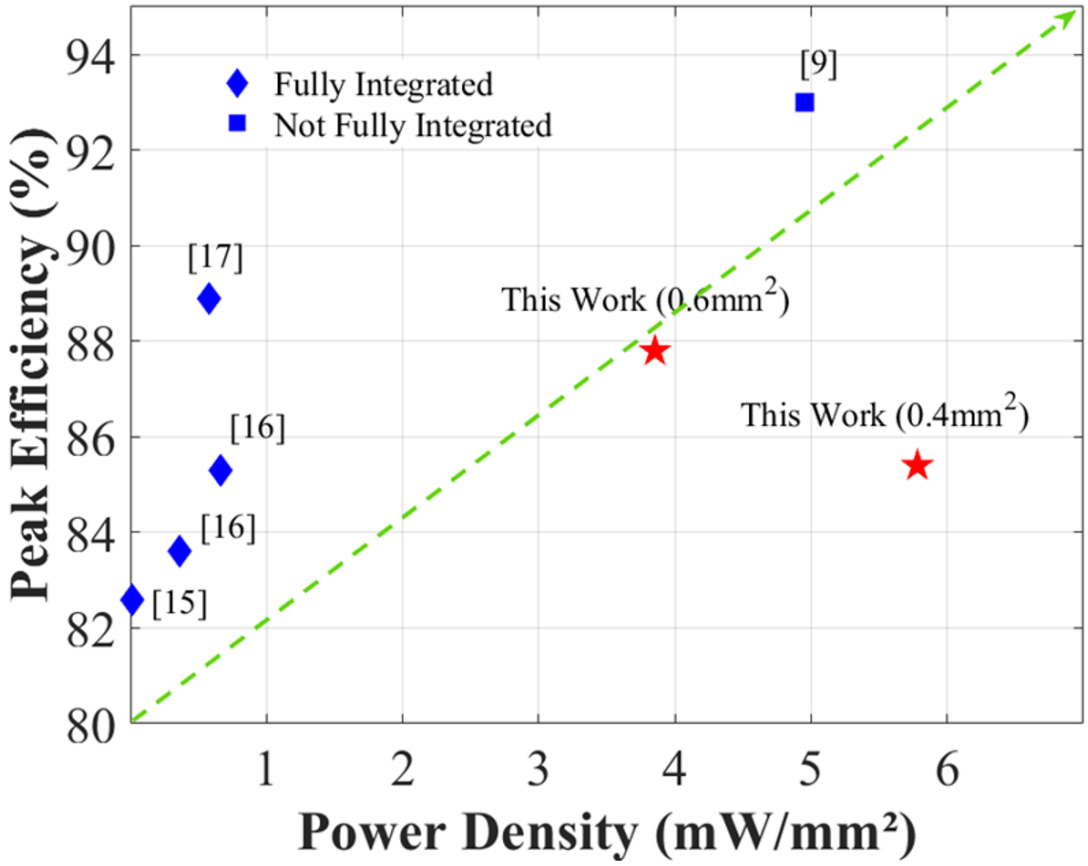


Figure 5.7: Comparison of the proposed design with state-of-art with <5mA load

maintaining the required frequency necessitates larger capacitors to store smaller voltages. While space-constrained designs often compromise on efficiency, this design approach strikes a balance, leveraging techniques like soft-charging advance-multiphasing [9] in CSCR to maintain moderately high efficiency even within a small area. This approach is highly scalable, allowing adjustments to voltage conversion ratios (VCRs) and load current ranges to adapt for various system requirements. Beyond textile-based and low-power IoT applications, this design approach can be extended to other systems that require a trade-off between size and efficiency, such as biomedical implants and compact robotics. By laying a foundation for future innovation in ultra-compact electronics, this design method provides a versatile framework for achieving the best design point performance in applications with stringent constraints on areas with moderate efficiency.

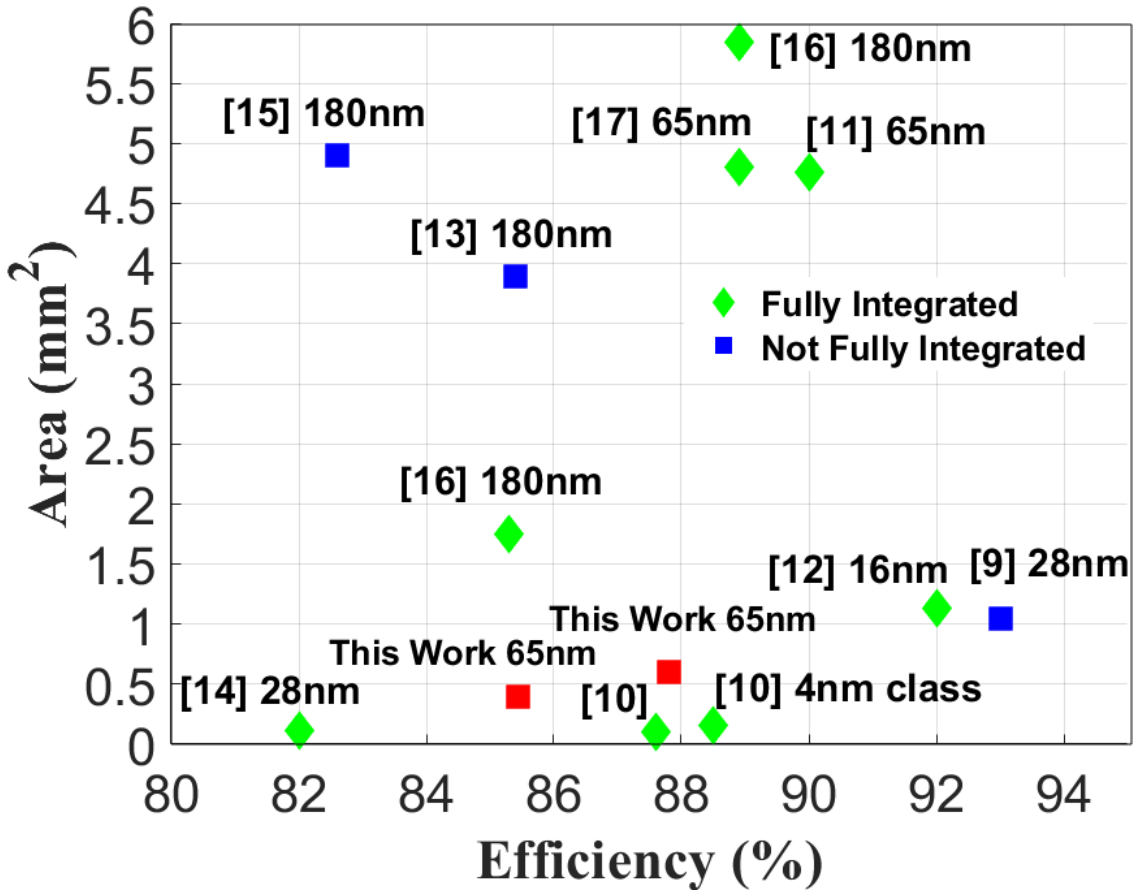


Figure 5.8: Area vs. Efficiency comparison of the proposed design with state-of-art

5.7 Future Work

This work demonstrates the potential for achieving higher efficiency in distributed systems that operate with lower load current ranges, thereby expanding its range of applications. The ample surface area available in such systems can be effectively utilized. However, further analysis of system parameters is required, including fault analysis. For example, potential issues such as broken wires or non-functioning components disrupt communication between chips, ensuring the system can reroute communication and maintain reliable operation.

Acronyms and Abbreviations

Acronyms and Abbreviations	
SC	Switched Capacitor
CSCR	COntinuous Scalable Conversion Ratio
VCR	Voltage Conversion Ratio
SoT	System-on-Texile
IoT	Internet of Things
I/O	Input/Output
Ecs	Charge Sharing Loss
MHz	Mega Hertz
M	Number of Top Nodes
N	Number of Bottom Nodes
D1	Cornerstone Phase
D2	Cornerstone Phase
T1 to TM	Top Intermediate Nodes
B1 to BN	Bottom Intermediate Nodes
S	Total Phases
Cell Count	Number of Cfly 2N+2M+1
qin	Input Charge per cycle
qout	Output Charge per cycle
Ctot	Toltal Cfly

η	Effciency (%)
AST	Active Smart Textiles
MOS	Metal Oxide Semiconductor
MIM	Metal Insulator Metal
MOM	Metal Oxide Metal
BAA	Board Agent Announcement
UVA	University of Virginia
RLP	Robust Low Power

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