Submillimeter-Wave Quasi-Vertical GaAs Schottky Diodes Integrated on Silicon Membranes

A Dissertation

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Doctor of Philosophy of Electrical Engineering

by

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Abstract

GaAs Schottky diodes are the central component of Terahertz (THz) metrology instrumentation. The frequency translating property of the Schottky diode is used in ground and space based observatories and for characterization of other THz devices. As detectors, GaAs Schottky diodes are used for measuring signal power levels, as mixers they are used in heterodyne receivers, and as variable capacitors they are used in frequency multipliers.

The focus of this dissertation is the integration of GaAs Schottky diodes on silicon-on-insulator (SOI) substrate carriers to better control the device parasitics and to accommodate assembly of fully integrated diode-based circuits. During research into this process, a unique quasi-vertical diode geometry was developed in which the ohmic contact lies directly below the Schottky anode. While similar in concept to the first whisker contacted Schottky diodes, the quasi-vertical diode is nevertheless a planar device that is readily integrated with other components supported by the SOI substrate, including beamleads for electrical connection. To illustrate the advantages of this technology, 40-to-80 GHz doublers and a new 40-to-160 GHz quadrupler were designed and implemented using the quasi-vertical diodes and heterogeneous integration methods developed in this research. These multipliers are the first demonstrated fully-integrated GaAs varactor circuits fabricated on SOI, yielding record performance in multiplication efficiency, and demonstrating the benefits of the novel diode architecture and substrate replacement technology.

Acknowledgements

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Chapter 1

Schottky Diode Technology for Terahertz Application

The terahertz spectral range refers to the frequency band between 300 GHz and 3000 GHz [1], or vacuum wavelengths of 1 millimeter to 100 micrometers (Figure 1.1). This chapter introduces the primary applications that take advantage of this frequency range, reviews the development of GaAs Schottky diode technology, which is crucial to THz metrology, and provides a statement of current issues in diode technology that are addressed in subsequent chapters.

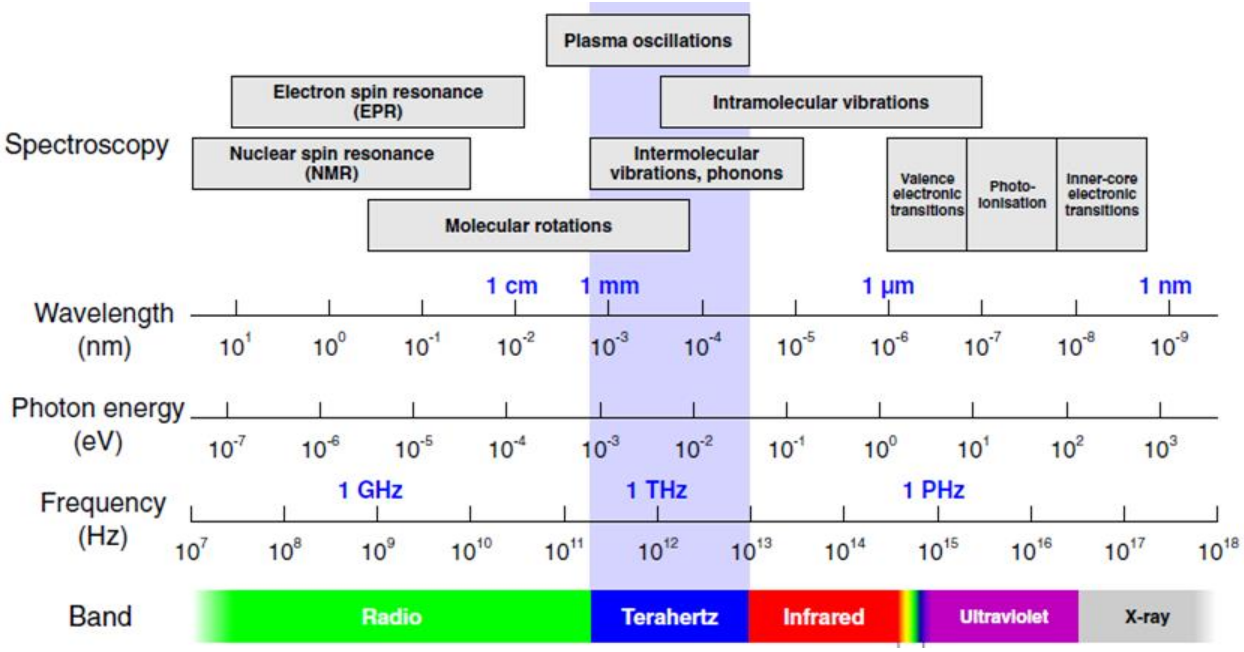


Figure 1.1: Terahertz regime within the electromagnetic spectrum.

1.1 Overview of Applications of the Terahertz Spectrum

Terahertz (THz) radiation is non-ionizing (energies corresponding to 1.24 – 12.4 meV) and interacts with materials by stimulating rotational and vibrational modes of molecules, resulting in absorption peaks in the spectral response [2]. Molecules with non-zero dipole moments exhibit characteristic rotational transitions with distinct observable frequencies within the millimeter and submillimeter wave region. The frequency of the rotational transition is based on the molecule's angular momentum quantum number and its moment of inertia about its rotational axis [3]. The spectra obtained from these molecular transitions can be used for identifying a given species [4], [5] (Figure 1.2). Spectroscopy in this band is currently used for investigating the chemical composition of interstellar media and planetary atmospheres by radio astronomers. Both ground-based radio telescopes, such as the Atacama Large Millimeter/submillimeter Array (ALMA) [6], [7] (Figure 1.3), and space based observatories, such as the Herschel Space Observatory [8], take advantage of this spectral range for radio astronomy. The use of GaAs Schottky diodes in an ALMA receiver is highlighted in Figure 1.3, and an example of an image generated by ALMA in the submillimeter range is shown in Figure 1.4 [9].

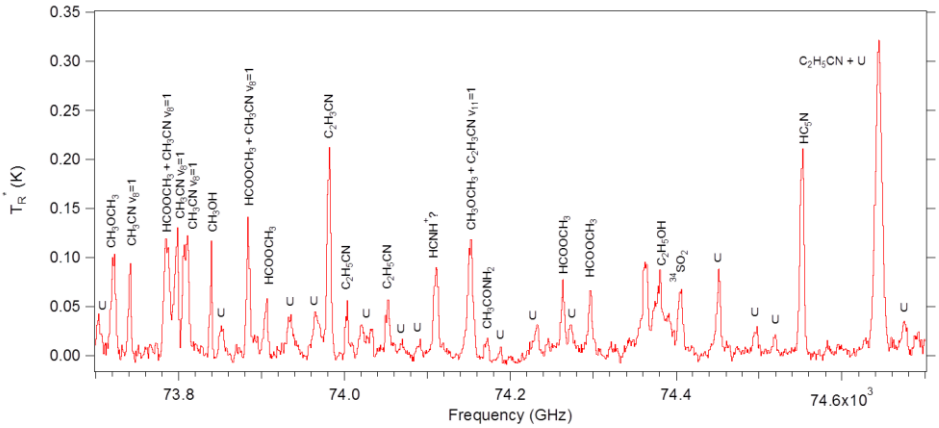


Figure 1.2: Single-sideband spectrum identifying the rotational transition of known species; measured towards Sagittarius B2 (SgrB2(N)) star forming region at 74 GHz, using the ARO 12 m telescope, with 1 GHz of bandwidth.

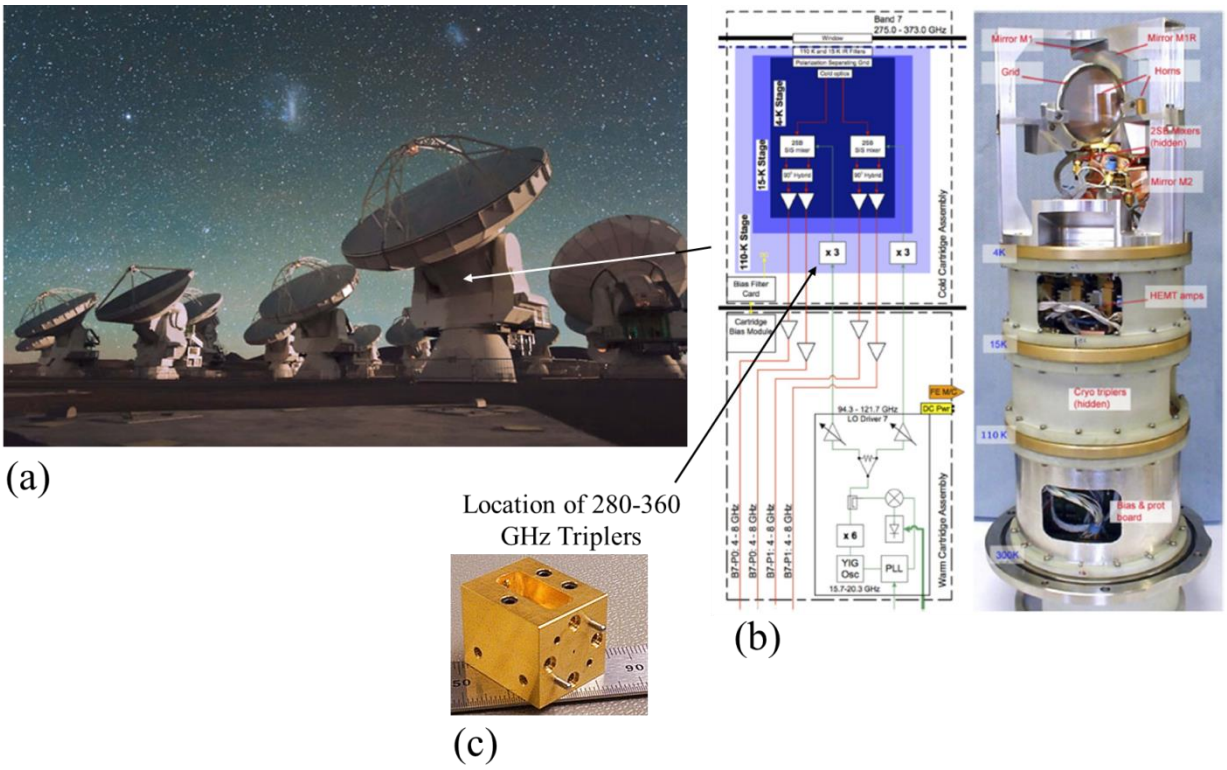


Figure 1.3: (a) ALMA telescope array, (b) ALMA receiver front end (c) GaAs Schottky diode triplers employed in the ALMA receiver.

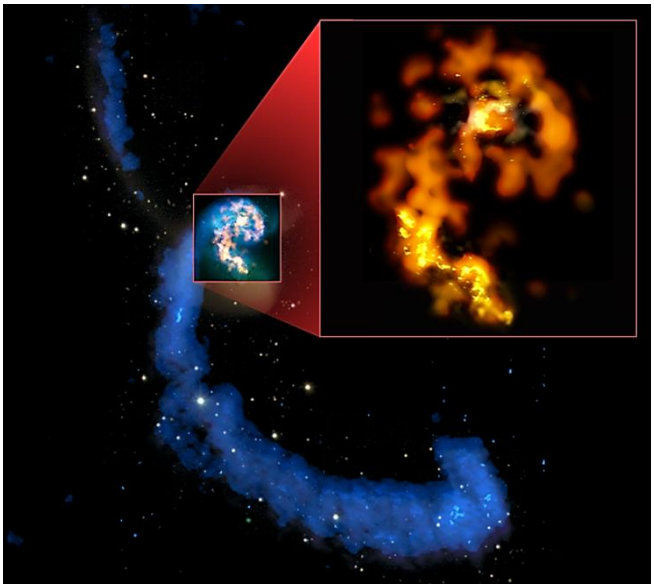


Figure 1.4: ALMA image of a merging pair of galaxies (Antennae Galaxies) using wavelengths between 3.5 mm to 810 μm (84 to 370 GHz), with visible-light observations from the NASA/ESA Hubble Space Telescope. Oranges and yellows reveal carbon monoxide molecules.

The remote sensing capability used by radio astronomers to determine the chemical composition of extraterrestrial atmospheres is likewise used by satellites such as the Microwave Limb Sounder (MLS)

[10], to observe the earth's atmosphere. The spectral range between 118 GHz to 2.5 THz [11] is currently used aboard the MLS to determine the impact of manmade emissions on the global climate. The MLS provides a daily global map of the following chemical species: O_3, H_2O, OH, HO_2, CO, HCN, N_2O, HNO_3, HCl, HOCl, ClO, BrO, SO_2, and CH_3Cl. These plots can be used for monitoring the ozone layer, the global chlorine load, the effects of biomass burning, and also for improving global chemical transport models. Figure 1.5 illustrates stratospheric polar projection plots for some of the atmospheric gases that affect climate change [12].

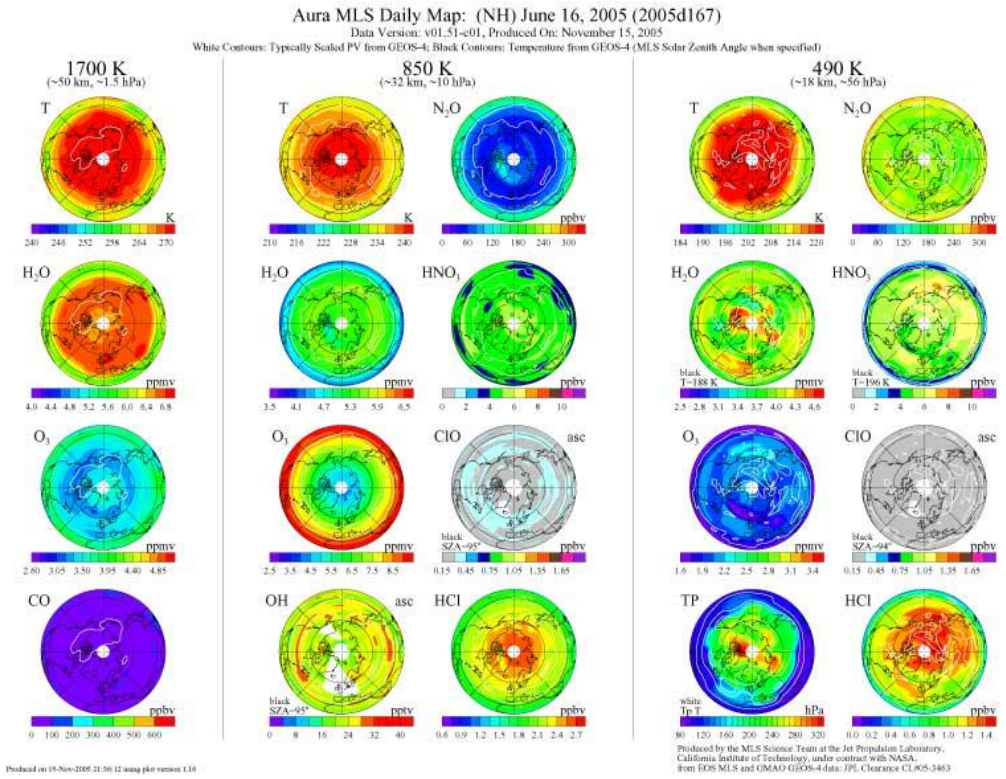


Figure 1.5: Stratospheric polar projection plots for N_2O, CO, H_2O, HNO_3, O_3, ClO, and HCl atmospheric chemical species temperature and pressure as obtained by MLS

An additional application of the terahertz spectrum is the characterization of components employed for space exploration, compact radar, and submillimeter-wave imaging. Vector network analyzer frequency extension modules have enabled scattering parameter measurements to 1 THz and on-wafer measurements of diode and transistors at these frequencies, which augment the design and fabrication process for these components [13], (Figure 1.6 and Figure 1.7). As shown in Figure 1.6, GaAs

Schottky diode mixers and multipliers within the Virginia Diodes, Inc. frequency extension module enable frequency translation from 50 GHz to the submillimeter bands. Moreover, submillimeter-wave GaAs and InP amplifiers are currently under development to drive local-oscillator chains for terahertz mixers used in the receivers of various space observatories. An example of a 650 GHz amplifier is shown in Figure 1.8 [14]. This nine stage indium-phosphide double-heterojunction bipolar transistor amplifier was fabricated by Teledyne Scientific Company for heterodyne receivers that could have wide-ranging metrology applications. A proposed use for a G-band (140-220 GHz) power amplifier is in the transmit/receive module for a planetary entry radar [15]. Such a radars would provide velocimetry and altimetry measurements with a smaller antenna footprint.

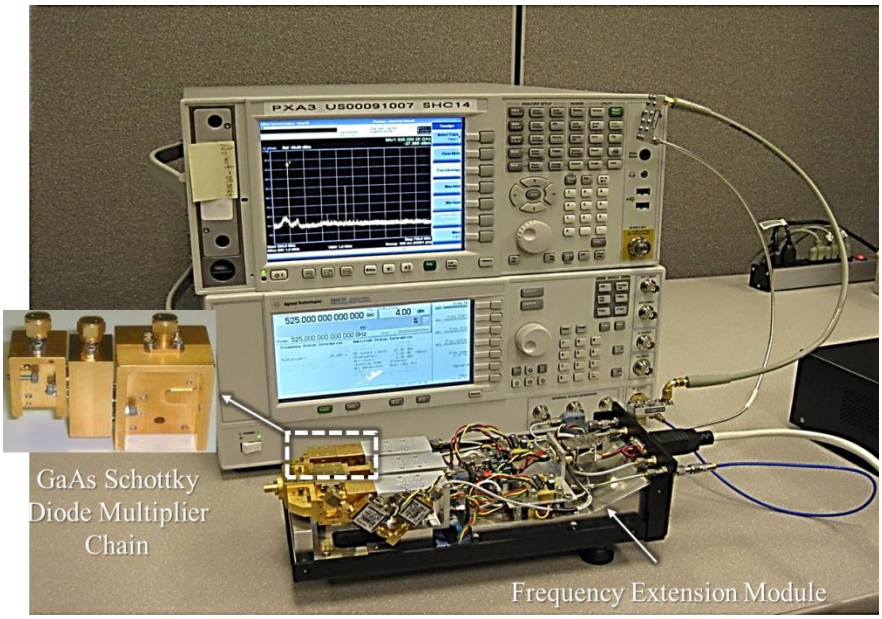


Figure 1.6: Vector network analyzer frequency extension module with highlighted GaAs Schottky multiplier chain.

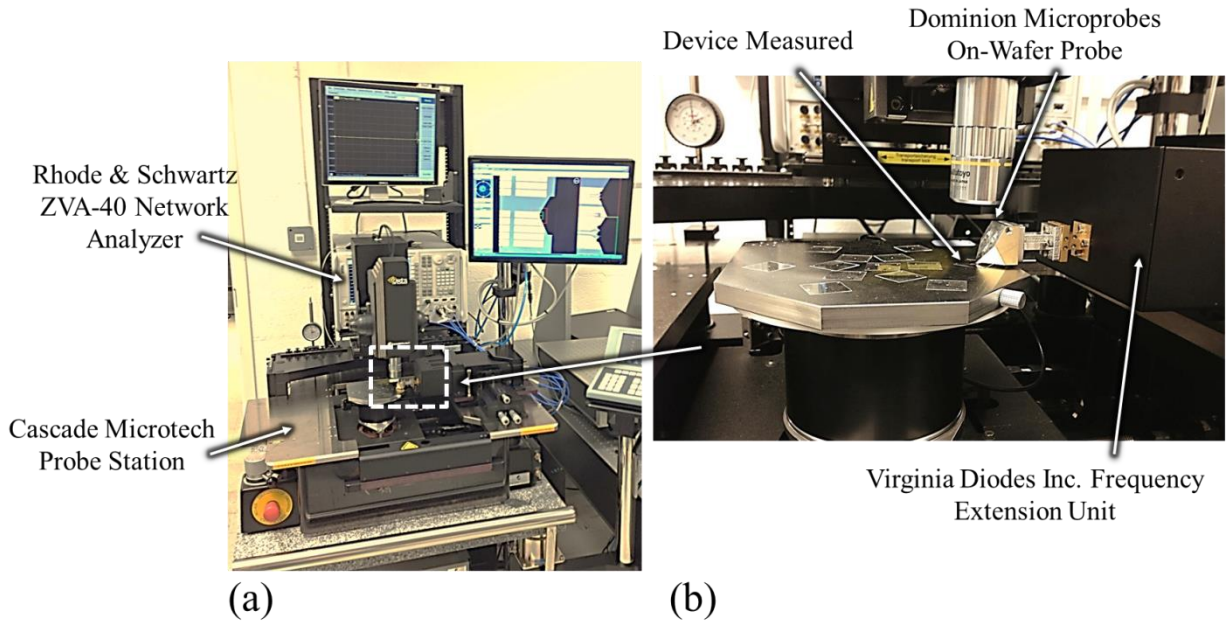


Figure 1.7: (a) Overview of the measurement setup with Cascade Microtech probe station, vector network analyzer frequency extension module and Dominion Probe Inc. on-wafer probe used to measure a coplanar waveguide circuits, (b) close-up view of the on-wafer probe

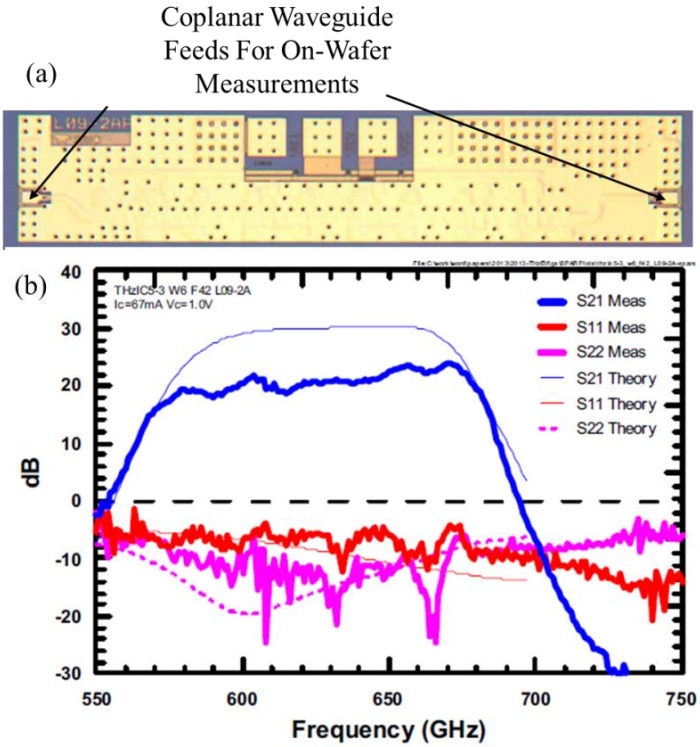


Figure 1.8: (a) Photomicrograph of the InP amplifier, (b) measured insertion gain (s_{21}) and input (s_{11}) and output (s_{22}) return loss of the 9-stage amplifier design

Other applications of THz spectroscopy include surface imaging for medical purposes and inspection of dielectrics with low water contents [16], [17], [18]. Medical surface imaging is currently being developed for the detection of skin cancer, tooth decay or for laboratory tests of thin tissue samples [19].

1.2 Submillimeter Wave GaAs Schottky Diodes

GaAs Schottky diodes are the central component of the terahertz metrology instrumentation described in the previous section. The frequency translating property of Schottky diodes is employed in instrumentation for ground and space based observatories and for the characterization of other THz devices. As detectors GaAs Schottky diodes are used for measuring signal power levels, and as mixers they are used in heterodyne receivers. The nonlinear capacitance-voltage dependence of the reverse-biased Schottky diode is used for frequency multiplication and Schottky multipliers are in turn utilized as local oscillator sources for receivers.

The submillimeter diode geometry has evolved over time to allow for a more robust and integrated device. The exact placement of the ohmic contact and the Schottky anode affect the device parasitics and series resistance which directly influences the Schottky diode's frequency translating efficiency. The first diodes operating in the THz region consisted of a metal whisker pressed against a Schottky anode contact (Figure 1.9). The vertically-oriented whisker diodes could be unreliable due to the fragility of the contact and were difficult to integrate with other components due to their contact geometry [20].

Nonetheless, this type of diode exhibited low series resistance and low shunt parasitic capacitance due to proximity of the ohmic contact and geometry of the whisker connection to the Schottky anode. In the mid-1980's, laterally-oriented planar diodes [21], [22], as shown in Figure 1.10 and Figure 1.11 [13], began to replace whisker contacted devices as their planar geometry is compatible with modern IC circuit design and processing, allows for integration of multiple diodes in a single circuit, and permits the geometry of the device to be defined lithographically.

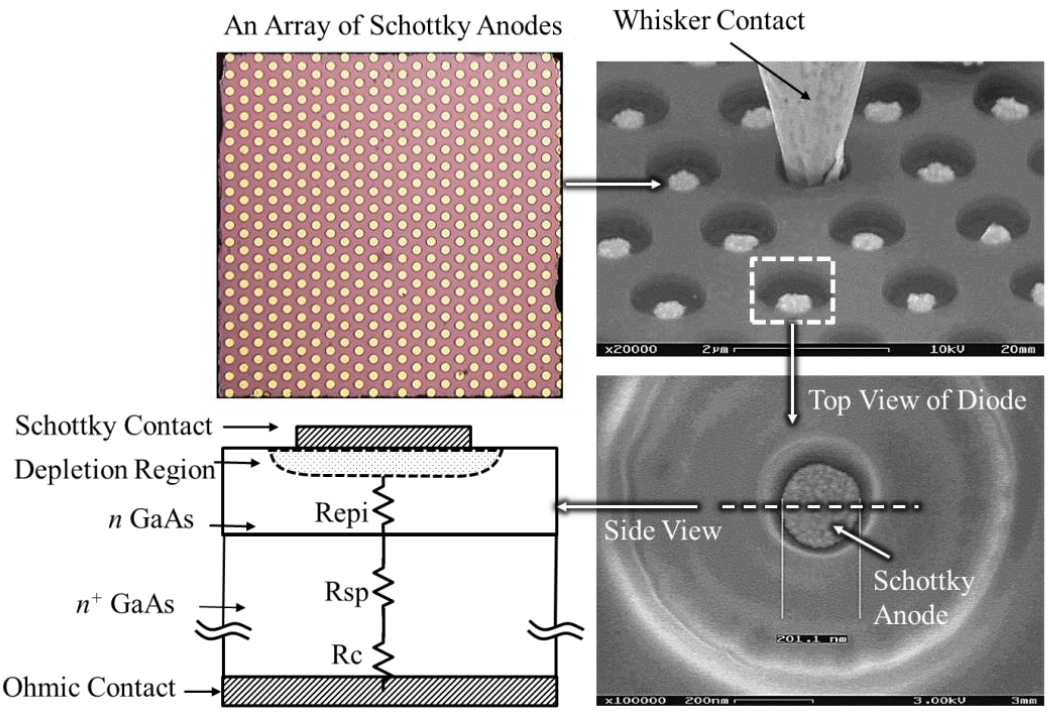


Figure 1.9: Whisker contacted Schottky diode

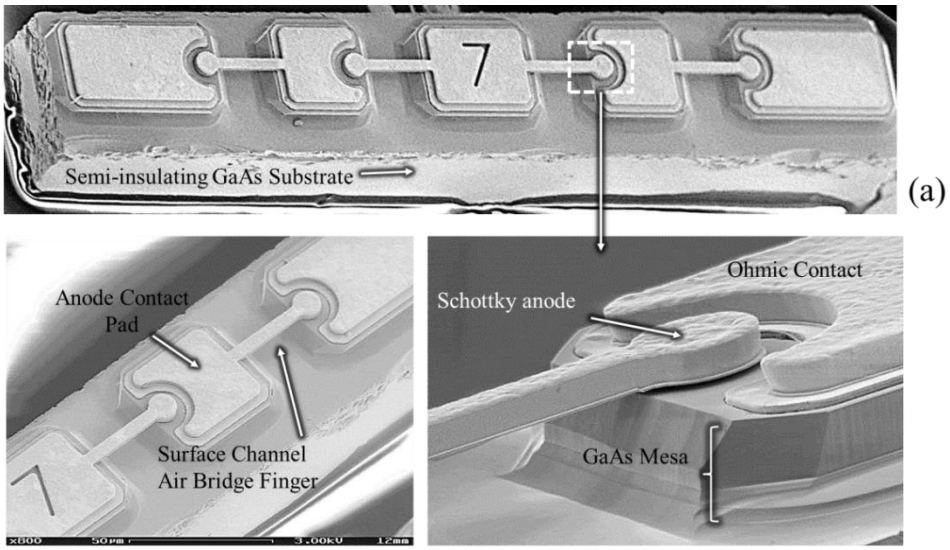


Figure 1.10: (a) Flip-chip planar varactor doubler with array of 4 anodes, (b) details of the surface channel air bridge finger used to reduce the device parasitics, (c) close-up of the ohmic contact and Schottky anode

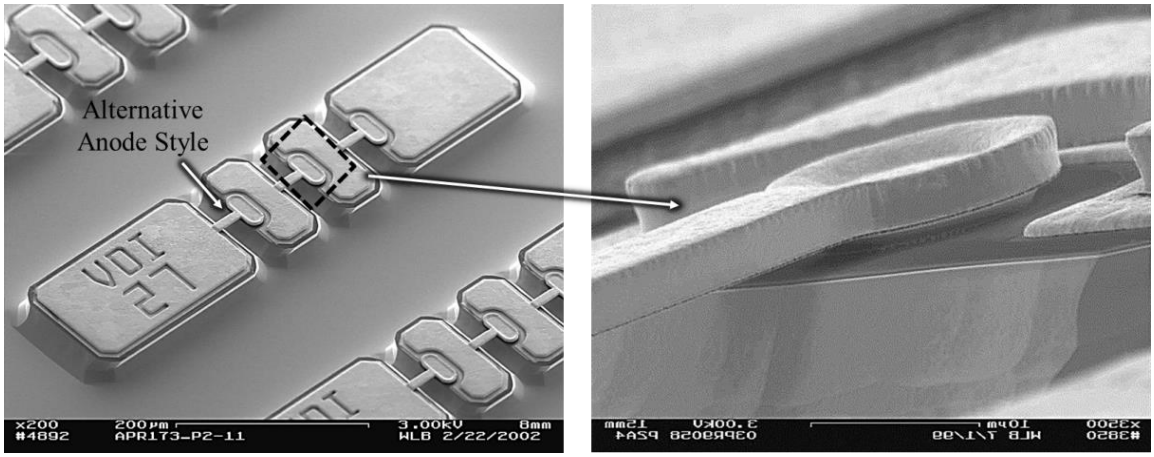


Figure 1.11: Planar varactor multiplier with array of 3 anodes

The planar diodes shown in Figure 1.10 and Figure 1.11 are designed to be flip-chip bonded to a substrate containing the necessary biasing and matching circuitry.

1.3 Quartz Substrate Replacement

Fabricating diodes with their impedance matching network allows for the creation of sophisticated circuit architectures that yielded improved performance. Figure 1.12, shows an example of a pair of GaAs Schottky diodes wafer-bonded to a quartz substrate with the necessary embedding network [23]. Integrating diodes on a quartz substrate eliminates the flip-chip manual assembly, allows for the use of a handle with a lower dielectric constant and superior mechanical strength, and permits backside inspection of the diode during processing. This technique is currently used when diode placement within the embedding network is critical to the circuit performance.

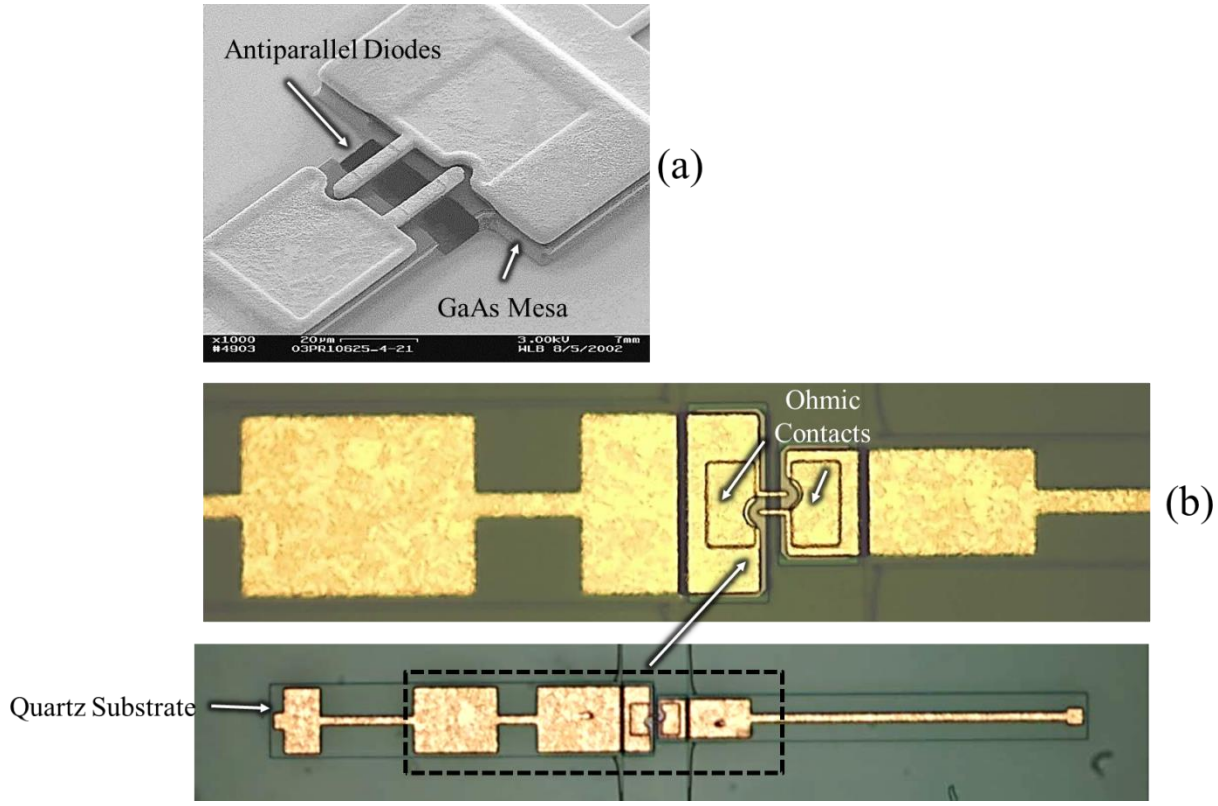


Figure 1.12: Integrated 640 GHz GaAs mixer circuit integrated with its matching circuitry on a quartz substrate, (a) detail view showing the GaAs mesa bonded to the quartz substrate and the antiparallel diodes, (b) photomicrograph of the quartz circuit

Building on previous work, this thesis focuses on the integration of GaAs Schottky diodes on a silicon-on-insulator (SOI) substrate to better control the device parasitics and to facilitate the device and circuit assembly. During the development of this process, a new quasi-vertical diode geometry was implemented in which the ohmic contact lies directly below the Schottky anode. While similar in concept to the first whisker contacted Schottky diodes (Figure 1.9), the quasi-vertical diode is nevertheless a planar integrated device on a 15 μm high resistivity silicon substrate with gold beams for electrical connections and assembly. An example of this diode geometry is shown in Figure 1.13. The GaAs mesa is attached directly to the ohmic contact which in turn is bonded to the silicon substrate using an adhesive and an air bridge finger is used for connection to the Schottky anode. These quasi-vertical diodes exhibit 3-7 Ω of series resistance at DC for 3-1.8 μm anode diameters, and a 35°C working temperature when operating in multiplier circuits.

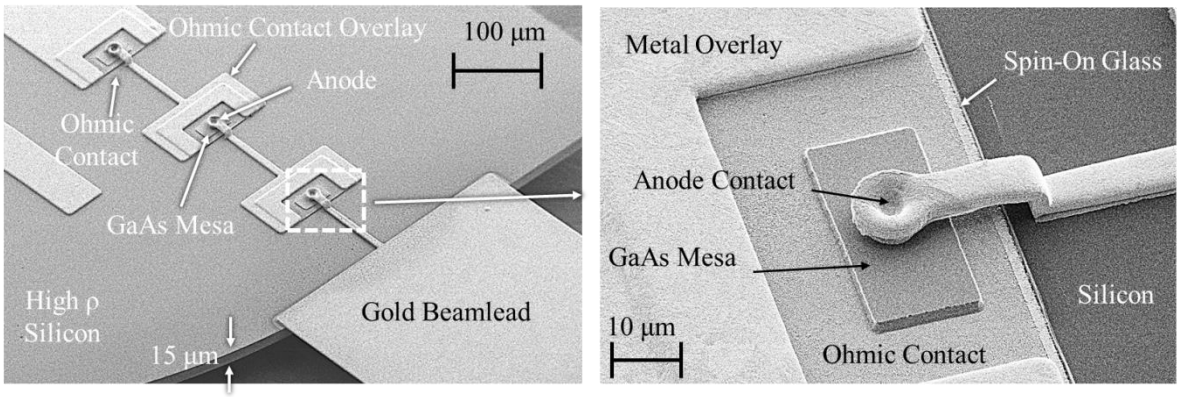


Figure 1.13: SEM of quasi-vertical diode array fabricated on a 15 µm thick high-resistivity silicon carrier with beamleads

In this work, 40 to 80 GHz doubler and 40 to 160 GHz quadrupler multiplier circuits are designed and fabricated to demonstrate the advantages of the novel diode architecture and substrate replacement technology. Schottky diode multipliers are also one of the most important solid-state components for generating high-frequency millimeter and submillimeter-wave signals, and hence are critical for a variety of metrology instrumentation. This research is supported in large part by the National Ground Intelligence Center and addresses their need for higher order multipliers for scaled radar range applications.

1.4 Organization of Thesis

This thesis is organized to describe the processes that led to the development of the quasi-vertical diodes on integrated silicon membranes. Chapter 2 presents a 200 GHz proof-of-concept GaAs varactor Schottky phase-shifter on a 15 µm SOI substrate. Issues arising from this design were used to develop the quasi-vertical diode. Chapter 3 describes the metrology equipment used to characterize the quasi-vertical diodes. Chapter 4 presents the quasi-vertical diode design and fabrication process as well as a device characterization based on measurements in the 350-1100 GHz range. Chapter 5 examines the fabrication and measurement of doubler and quadrupler multiplier circuits and demonstrates the potential of the new diode geometry on SOI process. Lastly, conclusions and contributions are discussed in Chapter 6.

In this work, a robust process was developed for transferring GaAs epitaxial layers to silicon. This substrate transfer procedure was then used to invent a new quasi-vertical diode geometry with lower

device parasitics and more favorable thermal characteristics compared to other integrated membrane diodes. At the same time, the first on-wafer measurements of this quasi-vertical diode geometry were made above 1 THz, and a new integrated quadrupler architecture was invented to further demonstrate the performance of the new diode geometry. This 40 to 160 GHz quadrupler, is the most integrated multiplier to date, has the highest efficiency for a high order multiplier in this range, permits the cascading of multiple stages without loading effects, and demonstrates repeatable and consistent performance for multiple quadrupler chip assemblies.

Chapter 2

Heterogeneous Integration of GaAs Schottky Diodes On Thin Silicon Membranes

As described in Chapter 1, the first terahertz GaAs Schottky diodes were created by pressing a metal whisker against a predefined GaAs Schottky area [24]. Whisker contacted diodes produced the some of the lowest device parasitics, and as a result the highest operational frequencies at that time [25]. However, difficulties associated with the mechanical robustness of the whisker contact, as well as complications associated device integration led to the development of a "planar" or lateral diode. In the planar diode geometry, the Schottky contact is defined lithographically, contacted with an integrated finger, and the anode and the ohmic areas are oriented parallel to the semiconductor substrate.

The loss, fragility, and poor thermal properties of the semi-insulating GaAs substrate employed for planar diodes led to the development of substrate replacement methods in which the GaAs epitaxial layers were bonded to a host substrate with more desirable physical properties. Table 2.1, lists the common substrates currently used by researchers for Schottky diode fabrication. The ideal substrate should have high thermal conductivity, be mechanically strong, and be amenable to lithographic processing and etching for creation of interconnects and beamleads to eliminate manual assembly. This chapter presents the current state of the art and initial research with silicon-on-insulator substrate replacement technology.

Substrate	εr	tan δ	R	k	α
GaAs	12.9	.006	50	50	6.8
Silicon	11.9	.004	130	157	2.3
Quartz	3.78	.0001	2	6.2-12	0.5

Table 2.1: Substrate properties.
ε_r = Dielectric constant [26], tan δ = Loss tangent (10 GHz) [26], R = Modulus of resilience (MPa) [26], k = Thermal conductivity ($W \cdot m^{-1} \cdot K^{-1}$) [27], α = Coefficient of thermal expansion (10^{-6}/C) [27].

2.1 Overview of State of the Art

2.1.1 Quartz Supported Diodes

Quartz has long been the substrate of choice for heterogeneous integration of Schottky diodes at the University of Virginia, Virginia Diodes, Inc. and other institutes [28], [29], [30], [31]. The initial work on transferring GaAs epitaxial layers to quartz was performed by Bishop [32], and further developed by Marazita [33], Schoenthal [34], and Midkiff [35]. The GaAs-on-quartz fabrication process begins by first removing the GaAs substrate's semi-insulating (SI) layer. This is accomplished by attaching the GaAs wafer to a silicon carrier using Apiezon W wax, and lapping and wet etching the SI layer to reach an AlGaAs etch stop etch layer. The AlGaAs epitaxy is then wet etched in an iodine solution to expose the epilayers needed for device fabrication. These epilayers, still attached to the silicon handle, are then bonded to the 250 μm quartz substrate using Filmtronic's *methyl-phenyl silsesquioxane* spin-on-glass (SOG) in a bonding press. The silicon handle is then detached from the epilayers by heating and liquefying the Apiezon W wax, leaving the GaAs epitaxial layers attached to the quartz substrate. The Schottky diode fabrication process would then proceed as described in [35]. Upon completion of the diode process, the quartz substrate is then bonded to a silicon handle and lapped to thickness designed for the operating frequency. Finally, the quartz substrate is diced to release individual chips.

Figure 2.1, displays an assembled 1.6 THz integrated varactor side band generator circuit based on UVA's quartz process, in its waveguide housing, with the top half of the E-plane split block removed to show the circuit. The quartz substrate allows for integration of the diode with its matching network; however the quartz process does not readily permit the creation of beamleads. Quartz etching experiments by Lichtenberger at UVA have typically resulted in beamleads with poor mechanical properties. This is partly due to the high power reactive ion etching recipe utilized for etching quartz. Therefore, indium or silver epoxy must be used for bonding independently created beamleads to the matching network on the quartz substrate, and the positioning and attachment of these beamleads requires considerable dexterity and skill. Furthermore, the quartz substrate is not a good thermal conductor, and indium has a melting

temperature point of 150°C, which limits the maximum circuit operating temperature. The quartz substrate must also be attached to the waveguide housing using an adhesive, which complicates circuit replacement and repair.

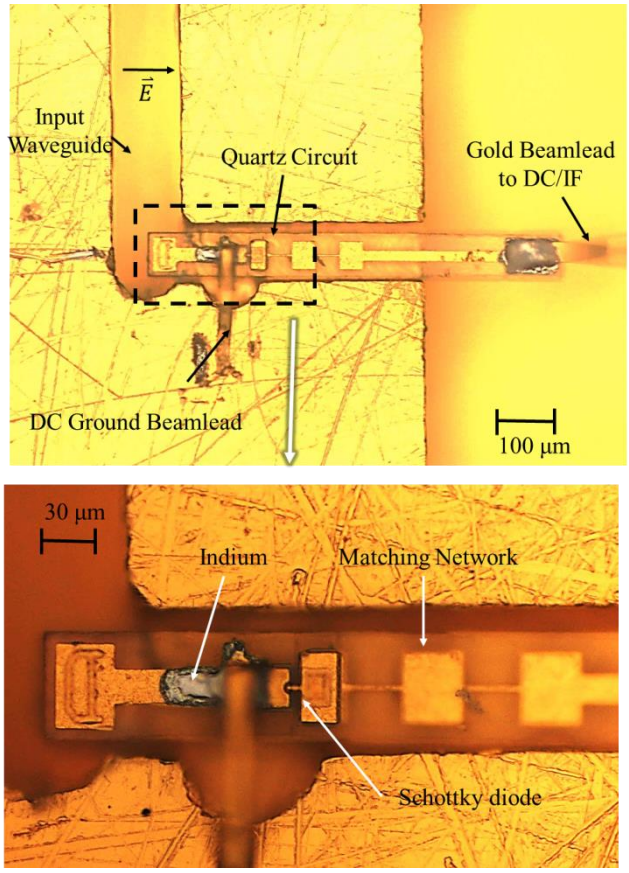


Figure 2.1: 1.6 THz integrated varactor side band generator circuit fabricated by Virginia Diodes, Inc. and assembled by the author

2.1.2 GaAs Membrane Diodes

The Jet Propulsion Laboratory has developed a diode fabrication process that does not utilize substrate replacement techniques, but instead employs a GaAs membrane with thickness of 3-50 µm [36]. As shown in Figure 2.2, this approach allows for the creation of beamleads and arbitrary chips geometries. For the 200-800 GHz band, the JPL process uses a 50-12 µm GaAs membrane and for frequencies above 800 GHz a 3 µm substrate is employed. As shown in Figure 2.2, designs in the 200-800 GHz band

require the GaAs substrate to be removed from sections of the matching network leaving only a supporting frame. This is done to reduce substrate losses and to prevent waveguide loading.

The diode fabrication process for the 12-50 μm and 3 μm membrane GaAs Schottky diodes is identical, with the main difference being the membrane formation methodology. For the 200-800 GHz devices the GaAs wafer is first waxed to a carrier. The semi-insulating (SI) GaAs substrate is then lapped to 12-50 μm, and reactive ion etching (RIE) is used to create the beamleads and separate devices. For the higher frequency designs, an additional AlGaAs etch stop layer is grown below a 3 μm GaAs device layer, which allows for the precise control of the substrate thickness. For designs above 800 GHz, lapping is used to thin the SI substrate. This is followed by a wet etch to reach the secondary AlGaAs etch stop layer. This layer is then removed to reveal the 3 μm device layer supporting the Schottky diode. To create the beamleads and to separate the devices, photoresist is patterned and RIE is used to define the extents of the 3 μm device layer.

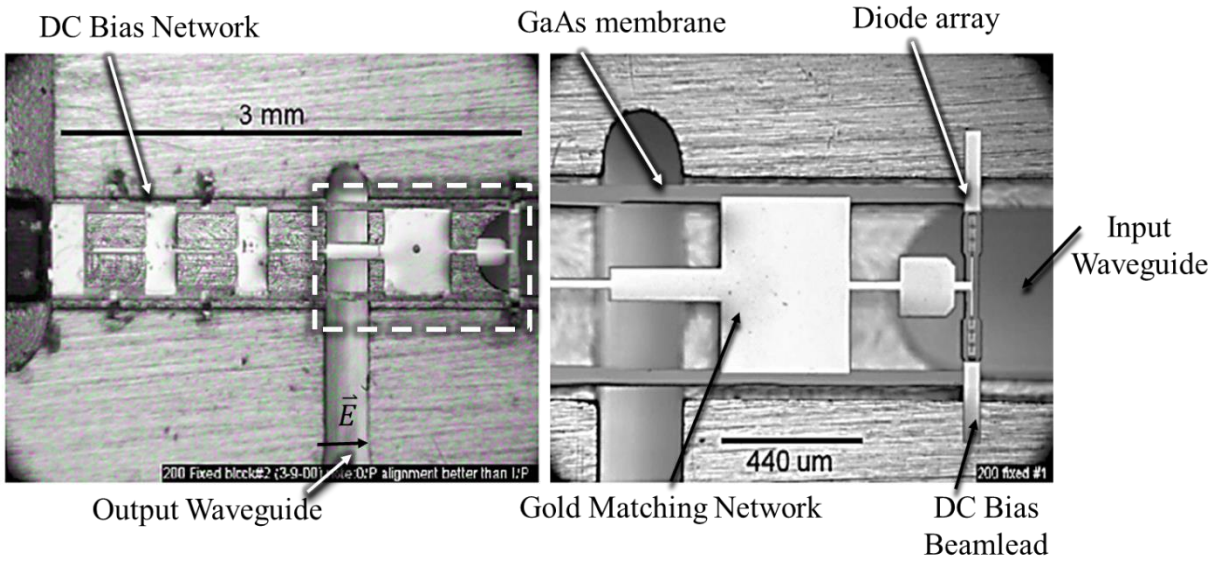


Figure 2.2: 200 GHz varactor multiplier with 15% efficiency at 369 GHz with a 9% bandwidth.

Although the thin GaAs membrane is advantageous electrically, it is not robust or very thermally conductive. Nevertheless, it is advantageous to have a substrate with a predetermined thickness that is amenable to beamlead formation for biasing and circuit assembly. This is not the case with a quartz substrate and the additional processing steps needed to precisely define the substrate thickness further

complicates the fabrication process. An alternative approach was sought that would permit the use of a mechanically robust and thermally conductive substrate, that had had a well-defined thickness and could easily etched.

2.1.3 GaAs Diodes on Thin Silicon Membranes

To address the issues associated with thin GaAs membranes, the focus of this work is on GaAs epitaxy bonded to 15 μm silicon-on-insulator (SOI) substrate to create an integrated circuit, with improved thermal conductance and mechanical robustness. A proof-of-concept demonstration to illustrate this fabrication methodology was a 200 GHz phase shifter, shown in Figure 2.3. Beamleads were used to bias the varactor diode and to clamp the substrate in place to the waveguide housing, making the assembly free of adhesives and solder. While this is the first GaAs Schottky diode fabricated on SOI, it is not the first example of substrate replacement for a III-V semiconductor. Previous work by the optoelectronical industry has resulted in heteroexpitaxies of GaAs and InP with silicon for the purpose of leveraging the processing infrastructure already available for silicon. An in-plane optical link, composed of an edge-emitting laser diode, a silicon waveguide and a photodiode, has been fabricated using this process [37]. Other applications have realized lasers and light emitting diodes [38] on a SOI substrate.

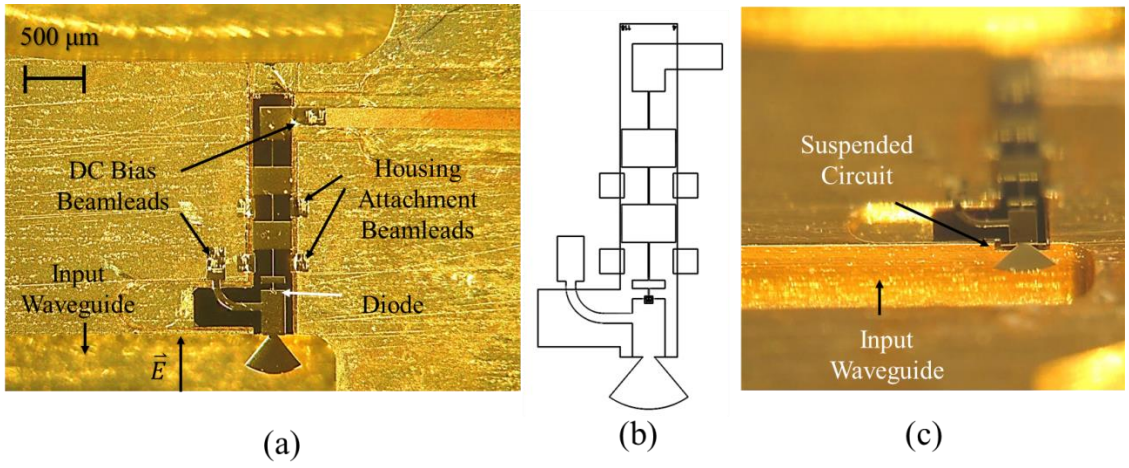


Figure 2.3: 200 GHz varactor phase shifter (a) circuit in its waveguide housing, with the top half of the *E*-plane split block removed, (b) an outline of the fabricated circuit, (c) front view of circuit in the waveguide.

The use of SOI in this work stems from past research at UVA on integrated hot-electron bolometers [39] and co-planar waveguide (CPW) micromachined probes for on-wafer measurements [40], [41]. In the case of the integrated bolometer, shown in Figure 2.4, SOI was used to simplify the fabrication and assembly by creating beamleads to allow a 3 μm silicon support substrate to be utilized as a carrier. Similarly, an on-wafer probe, shown in Figure 2.5, exploits silicon's mechanical robustness to generate the contact force needed for low-resistance contacts to CPW circuits. For the probe chips, SOI also allows for a photolithographically defined chip with gold beamleads for circuit positioning, clamping, and assembly.

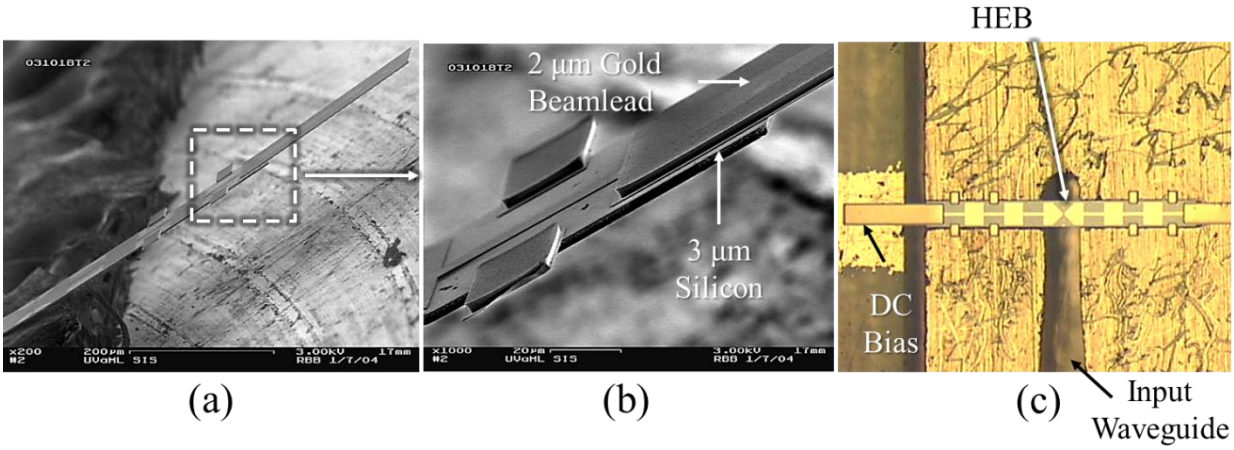


Figure 2.4: (a) 585 GHz hot electron bolometer (HEB), (b) a view of the 3 μm substrate and 2 μm beamleads, (c) the device in an E-plane split waveguide housing with beamleads used for assembly and electrical connections.

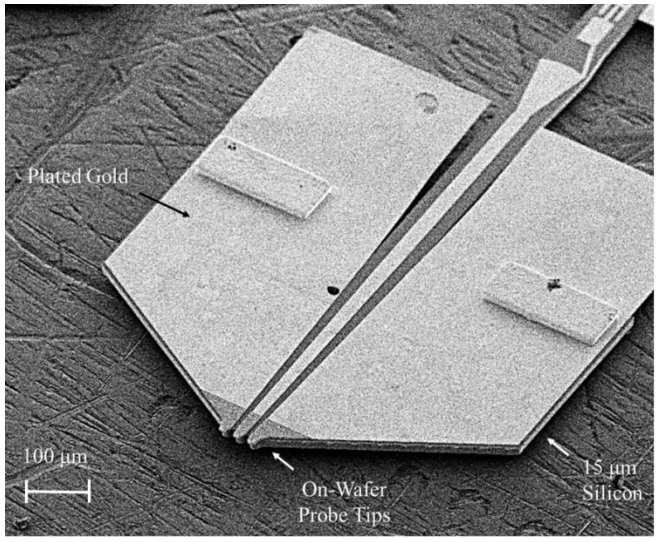


Figure 2.5: 500-750 GHz (WR1.5) micromachined probe

2.2 200 GHz Phase-Shifter Design

The 200 GHz varactor phase-shifter is used as a proof-of-concept demonstration and a vehicle to develop, refine and evaluate techniques for transferring GaAs epitaxy to SOI. There were concerns that transferring the GaAs epitaxy to silicon might damage the device epitaxial layers. DC and RF characterization of the 200 GHz phase-shifter on SOI would quantify the possible damage or lack thereof. The phase-shifter was design to provide 180° phase shift at 200 GHz with a 20% bandwidth. The 180° phase shift specification for this device is based on the criterion for minimum conversion loss when a phase modulator operates as a lossless double sideband mixer or a sideband generator [42]. Consequently, this device could also be used as an efficient sideband generator. In a phase-shifter, the varactor diode's capacitance change as a function of bias is used to modulate the phase of a reflected millimeter-wave signal [43]. To achieve a 180° phase shift, two transmission line tuning elements (ℓ_1 and ℓ_2) are integrated with the Schottky diode, as shown in Figure 2.6. The length of first tuning element (ℓ_1), in cascade with the diode, is intended to resonate with the varactor's capacitance at a bias of 0.5 V, producing a short circuit to an incident signal. The length of the second element (ℓ_2), in shunt with the diode, is designed to resonate with the varactor's capacitance at -4 V, effectively producing an open circuit.

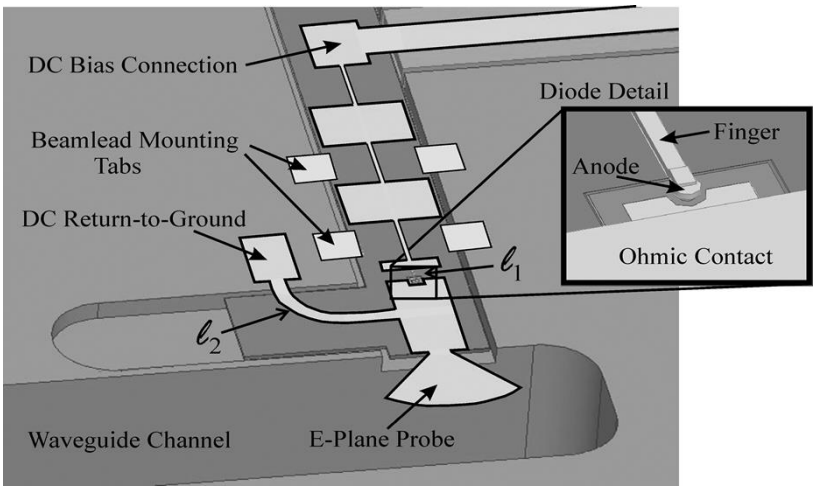


Figure 2.6: Ansoft's *High Frequency Structure Simulator* (*HFSS*) model of the 200 GHz phase shifter in E-plane split waveguide housing with the top waveguide cover removed.

As shown in Figure 2.6, the integrated phase-shifter circuit is designed to be housed in an E-plane split waveguide block, with four beamleads serving as mount tabs to support the chip. The beamleads labeled DC bias and DC return-to-ground are used to bias the diode. A radial stub protruding into the waveguide serves as a probe to couple the incident rectangular waveguide TE_{10} mode to the diode. Figure 2.7, shows a side view of the planar diode geometry and illustrates the parasitic circuit elements associated with the device. An inductance (L_f) is associated with length of the contact finger leading to the anode, and a π-network of capacitors represent fringing fields arising from the transition from the transmission line to the diode (C_{pp} and C_p). The intrinsic Schottky diode is represented by its junction capacitance C_j and series resistance R_s. The series resistance of the diode is composed of three contributions, the contact resistance (R_c), epi-layer resistance (R_{epi}), and spreading resistance (R_{sp}) [44].

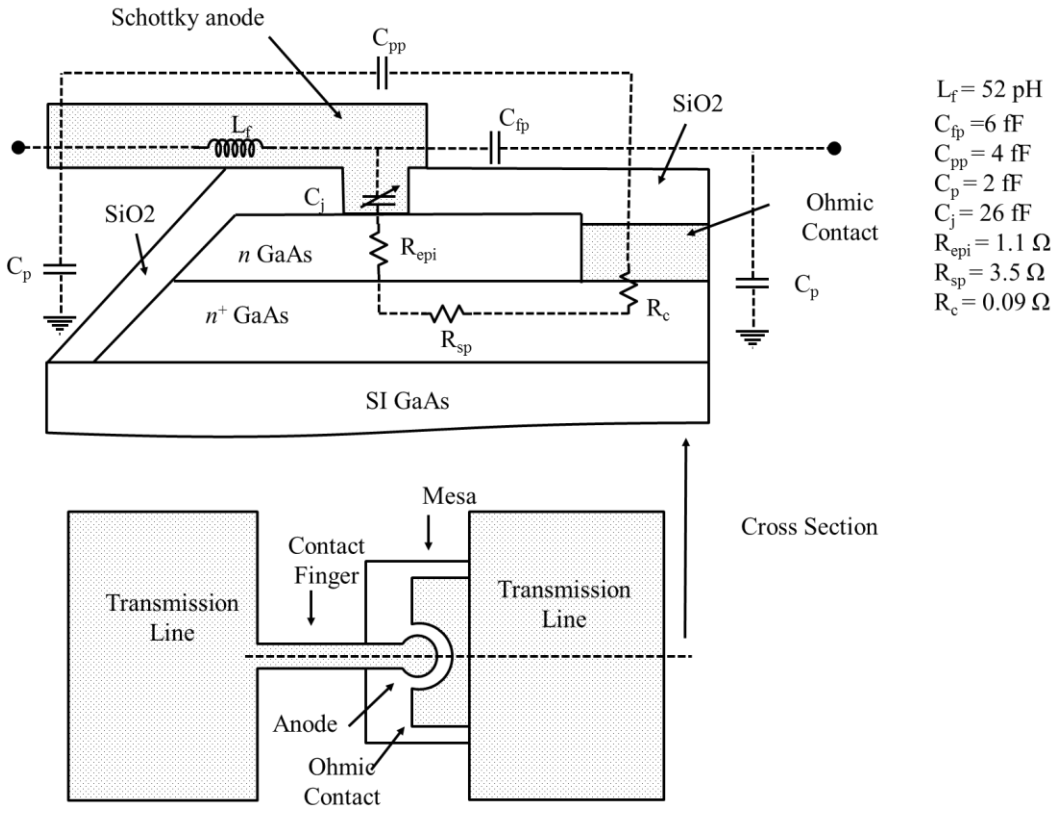


Figure 2.7: Cross sectional view of the planar diode with its associated parasitics.

The values for the parasitic elements in the diode model are obtained by finite-element modeling using Ansoft's *High Frequency Structure Simulator* (*HFSS*). The *HFSS* model in Figure 2.6 is divided into following segments: the diode, the low-pass filter and the waveguide transition. To obtain the values for the lumped components, the scattering parameters of the diode section are exported from *HFSS* and fit to an equivalent circuit model, shown in Figure 2.8, using Agilent's *Advanced Design System* (*ADS*). The finger inductance (L_f) is found to be 52 pH, the fringing capacitance between the finger and ohmic contact pad (C_{fp}) is 6 fF, and the capacitance between pads (C_{pp} and C_p) are 4 fF and 2 fF respectively. To simulate the complete phase shifter response at 200 GHz, the *HFSS* models for the waveguide radial transition and the low-pass filter were imported into *ADS* (Figure 2.8) and the diode bias voltage was varied over its full range (−4 V to 0.5 V, breakdown to forward conduction). The circuit transmission line

tuning elements, ℓ_2 and ℓ_1, were then adjusted to produce the desired phase shift and the *HFSS* model was updated.

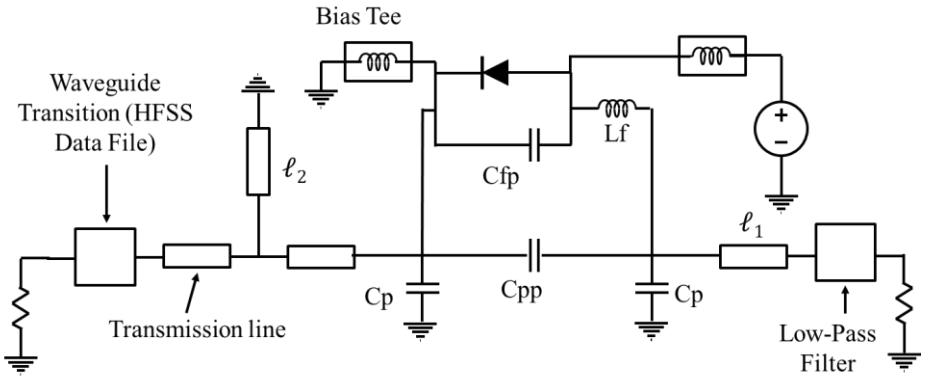


Figure 2.8: Equivalent model circuit used to model the phase-shifter.

2.3 Fabrication Process

The phase-shifter fabrication process is based on the work of Midkiff [35] which developed a quartz-based diode circuit for a 200 GHz phase-shifter. The diode fabrication process consists of six primary steps: (1) thinning and bonding of the GaAs epitaxy to a silicon-on-insulator (SOI) substrate, (2) deposition and annealing of the ohmic contacts, (3) etching the device mesa (4) deposition of the insulating oxide using plasma-enhanced-chemical-vapor-deposition (PECVD), (5) evaporating the Schottky metals and beamlead plating, and (6) finally, chip definition using a silicon extents etch. A detailed process sheet is provided in Appendix A.

The epitaxial layers of the GaAs and SOI substrates are shown in Figure 2.9. The GaAs wafer is composed of a semi-insulating handle, 2 μm AlGaAs etch stop layer, a 0.8 μm highly doped ($5x10^{18}$ cm^{-3}) layer for the ohmic contact and a lower doped ($1.7x10^{17}$ cm^{-3}) 0.22 μm layer for the Schottky contact. The SOI substrate is comprised of a 450 μm silicon handle, a 1 μm buried oxide layer, and a 15 μm high-resistivity (ρ > 10 kΩ-cm) silicon device layer.

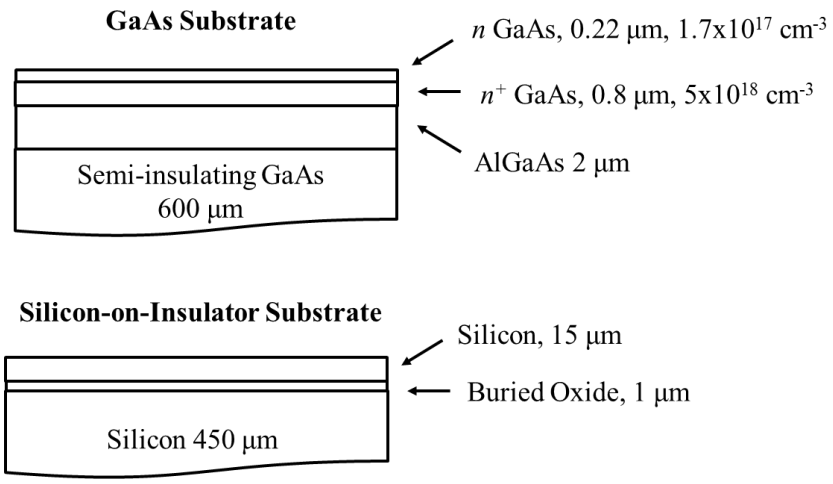


Figure 2.9: GaAs and silicon-on-insulator substrates.

The first processing step consists of bonding the GaAs wafer to a silicon carrier and thinning the semi-insulating GaAs layer. Figure 2.10 shows a partially completed process where the GaAs wafer is attached to a silicon carrier using Apiezon W wax, and thinned to the AlGaAs etch stop layer by lapping (Logitech Limited, PM5) and citric acid (5:1 citric acid:H_2O_2 at 50°C) wet etching. The AlGaAs is then removed in 49% hydrofluoric acid. Filmtronics FG65 spin-on-glass (SOG) is then spun on a SOI wafer at 3000 rpm for 30 seconds to a thickness 500 nm. The GaAs epilayers and the SOI substrate are then placed in a wafer press shown in Figure 2.11(a). The membrane press was designed by Edward Douglas and consists of an upper and a lower chamber separated by a silicone membrane (Figure 2.12(a)). In the press, the GaAs wafer is attached to a force distribution plate and the SOI substrate is placed on the heating block. After evacuating the press to -30 psi to outgas the SOG, the GaAs wafer and the SOI substrate are brought into contact and heated to 185°C to allow the SOG's polymethylsilsesquioxane polymer to crosslink. Following the curing step, the substrates are allowed to cool. Because the silicon carrier is attached to the GaAs epitaxial layers using only Apiezon W it can be removed after heating the wax. The resulting structure of GaAs on SOI is shown in Figure 2.11(a).

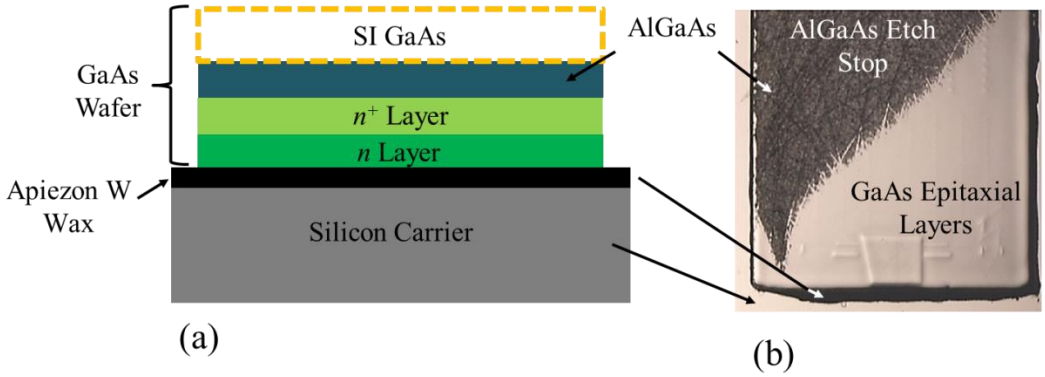


Figure 2.10: (a) GaAs wafer is bonded to a silicon carrier using Apiezon W wax and (b) partially completed etch to expose the GaAs epitaxial layers.

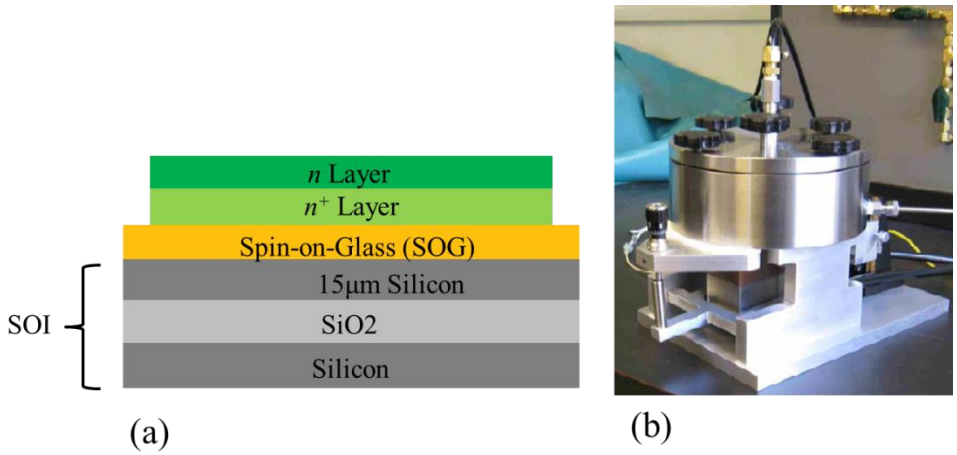


Figure 2.11: (a) GaAs epitaxial layers bonded to SOI substrate, (b) bonding press

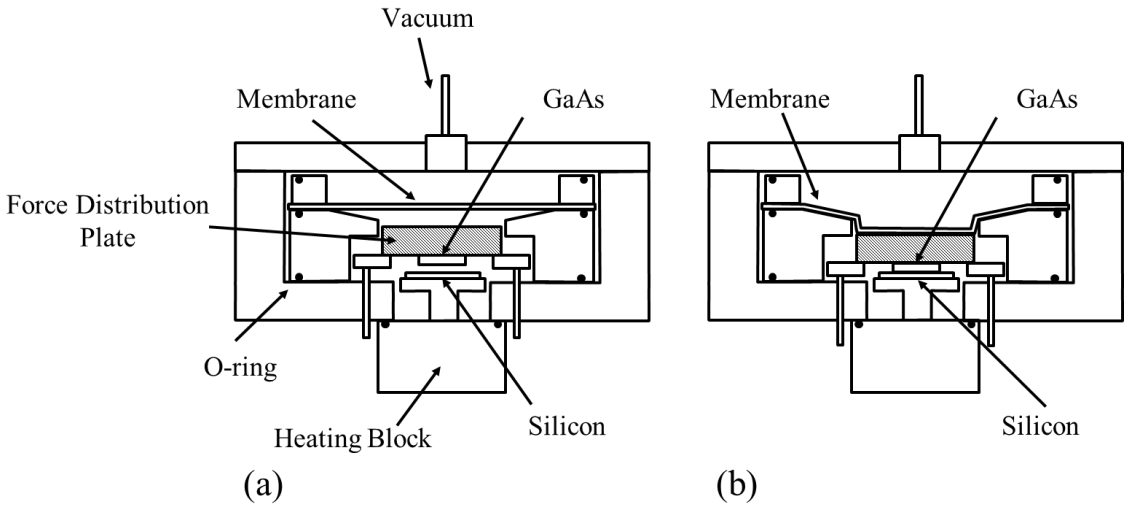


Figure 2.12: (a) cross section view of the membrane press before bonding GaAs to SOI, (b) view of the press during bonding

After transfer of the GaAs epitaxial layers to the SOI substrate, fabrication of the diode proceeds. The ohmic contact is formed by performing a citric acid (5:1 citric acid:H_2O_2) wet etch to reach the highly doped n^+ layer. AuGe/Ni/Au metal layers are then evaporated (Figure 2.13) on this layer. Lithography is done first to define the mesa. A second citric acid (5:1 citric acid:H_2O_2) wet etch is used to create the diode mesa, which isolates devices from one-another (Figure 2.14). The sample is then annealed at 400°C for 30s to form an ohmic contact alloy with a $5x10^{-6}$ Ω-cm^2 specific contact resistance.

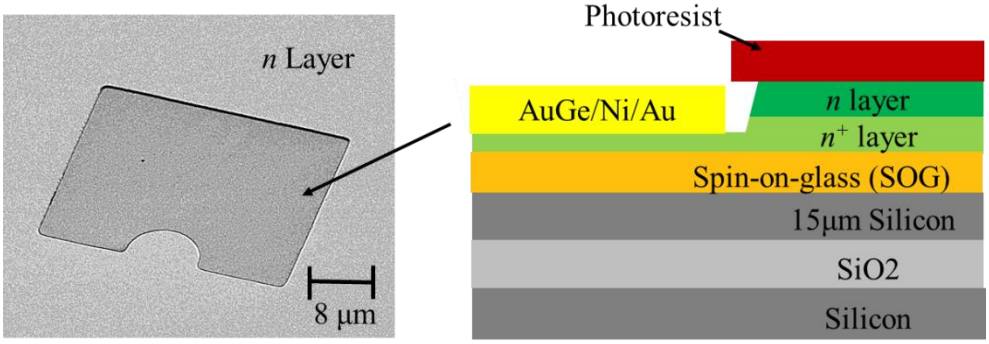


Figure 2.13: Ohmic contact formation

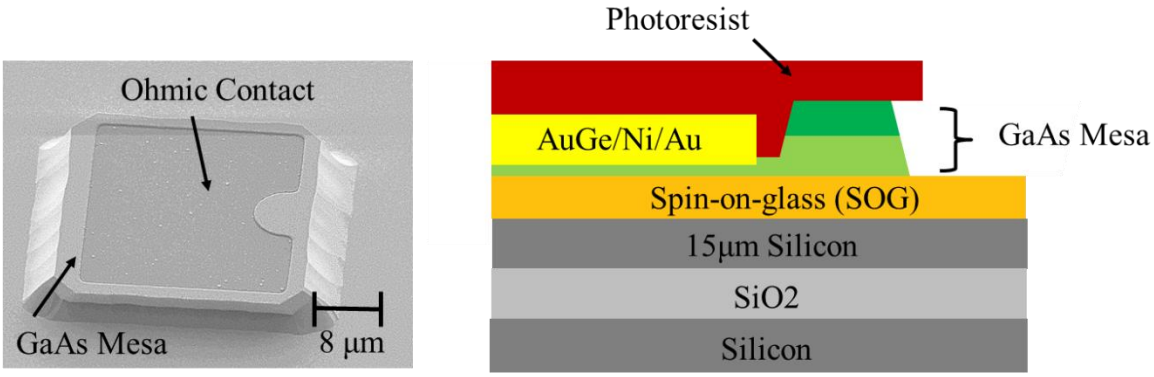


Figure 2.14: GaAs mesa formation

After ohmic contact formation, a one micrometer silicon oxide (SiO2) layer is deposited over the entire sample using PECVD. The Schottky anode and ohmic contact vias are then defined lithographically and formed using reactive ion etching (50 sccm CHF_3, 10 mTorr, 80W, 0°C) (Figure 2.15). A seed layer of titanium and gold (10/50 nm) is next evaporated over the entire substrate to create the Schottky contact and allow for plating of the beamleads and other circuit features through a photoresist mask (Figure 2.16).

The final front side processing step is the creation of alignment marks for the silicon extents etch. An RIE etch of the 15 μm device layer, which defines the chip's overall geometry during the last step of the backside processing is known as the extents etch. The extents etch alignment marks are defined by etching (35 sccm C_4F_8, 30 sccm SF_6, 15 mTorr, RF 40 W, ICP 500 W, 0°C) through the 15 μm of silicon and the 0.5 μm of SOG to reach the silicon dioxide etch-stop layer. Once again these marks are used during the final step of the backside processing.

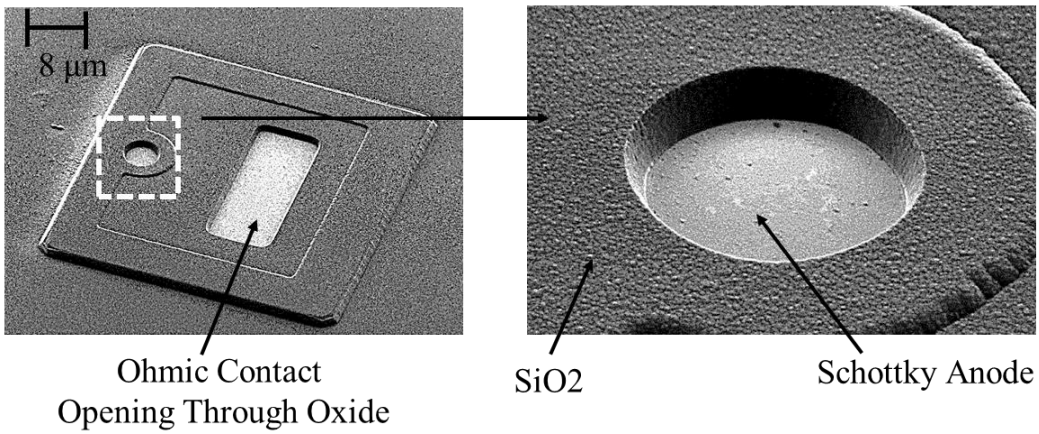


Figure 2.15: Silicon dioxide is used to define the Schottky anode.

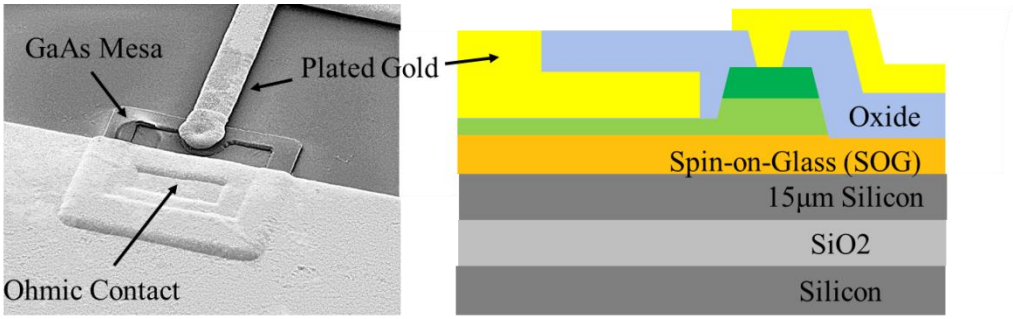


Figure 2.16: Plated metal

The completed device, shown in Figure 2.16, is next bonded device side down to a silicon carrier using Waferbond CR-200 adhesive in preparation SOI thinning. The SOI 450 μm silicon handle is then diced, leaving a 70 μm layer, and is etched with an RIE to reach the buried oxide (BOX). The BOX layer is next removed in a buffered oxide wet etch. After this backside processing, the alignment marks become visible for the extents etch. To release the individual chips, photoresist is patterned and the 15 μm silicon

device layer is etched with RIE. This final etch creates the beamleads and chip geometry (Figure 2.17). The released devices can then be mounted in the waveguide housing for testing (Figure 2.3).

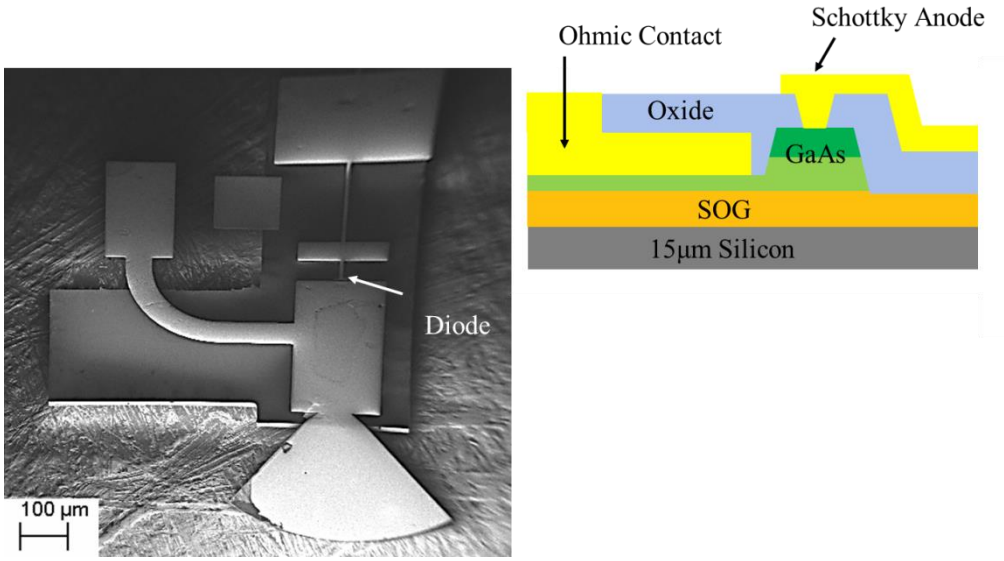


Figure 2.17: Released diode chip

2.4 Measurements

The 200 GHz phase shifter was characterized in the WR5.1 band using an Agilent 8510C vector network analyzer and Oleson Microwave WR-5.1 (140-220 GHz) extension head (Figure 2.18(a)). A one-port waveguide calibration was performed at the measurement port of the Oleson extension head using a short, delay short, and load standard from the Oleson (V05CAL) calibration kit. The extension head measurement port is therefore the reference plane for all measurements. After calibration, the circuit waveguide housing is attached to the extension head, and scattering parameters of the circuit measured as a function of bias within the 190-210 GHz band. The diode's bias was varied and the phase shift as a function of bias for different frequencies was found (Figure 2.18(b)). The magnitude of the 200 GHz phase-shifter's return loss at different bias points and a Smith chart plot of s_{11} at -4 V bias is shown in Figure 2.19.

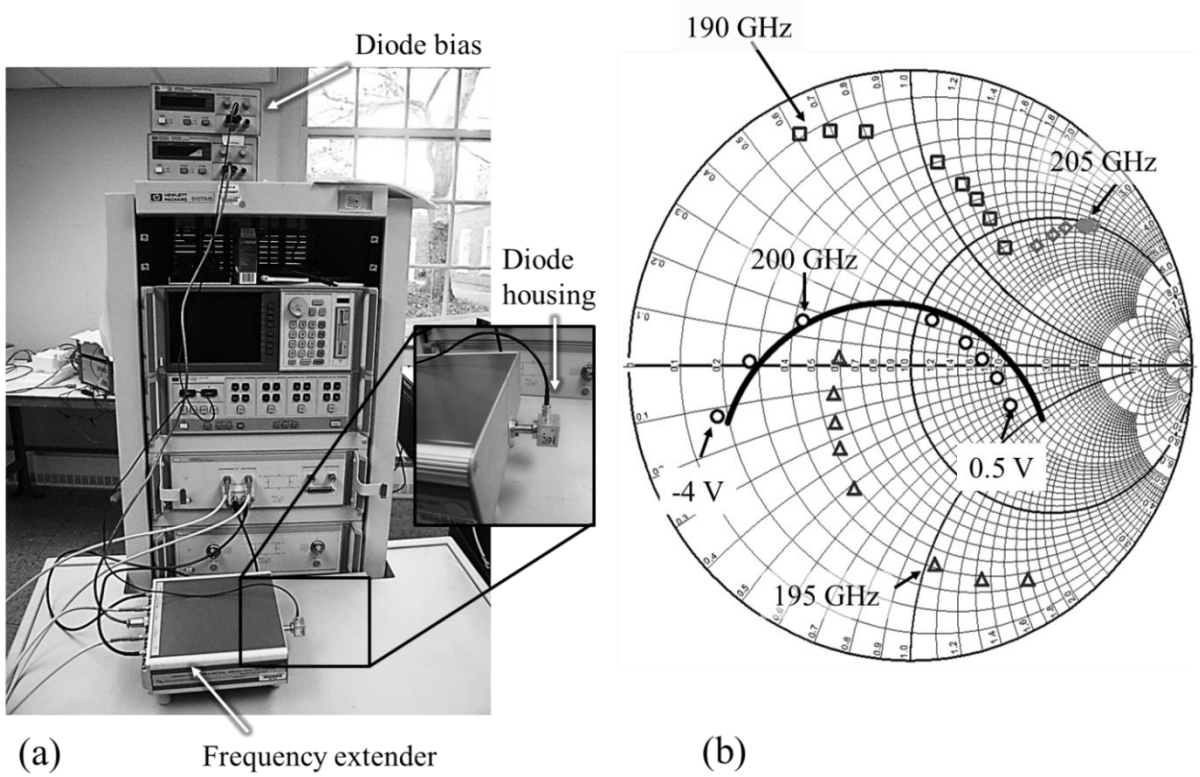


Figure 2.18: (a) measurement setup, (b) the simulated (solid line) and measured phase shift (dots) of the circuit at 200 GHz as the bias is varied from -4 to 0.5 V. Measured phase shift is also included for 190, 195, and 205 GHz.

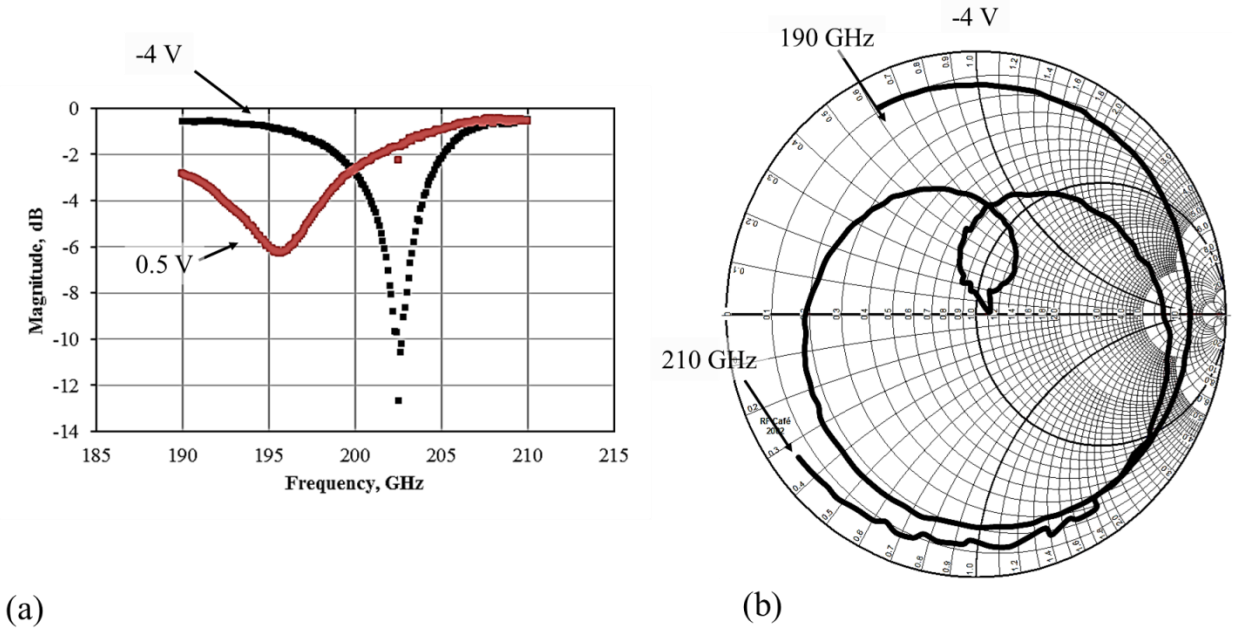


Figure 2.19: (a) magnitude of s_{11} at different bias points, (b) Smith chart plot of s_{11} at -4 V bias

The phase shift as a function of frequency is shown in Figure 2.20. At 200 GHz, a 180° phase shift is achieved but the performance quickly rolls off. The narrowband performance is mainly attributed

to discontinuity between cascaded simulation sections. The *HFSS* model of the radial stub should have included the diode and its matching network. Otherwise the simulation contained a discontinuity that was otherwise unobservable when modeling these two sections separately. At 190 GHz the measured phase shift with bias is 52˚ and at 205 GHz it is only 6˚.

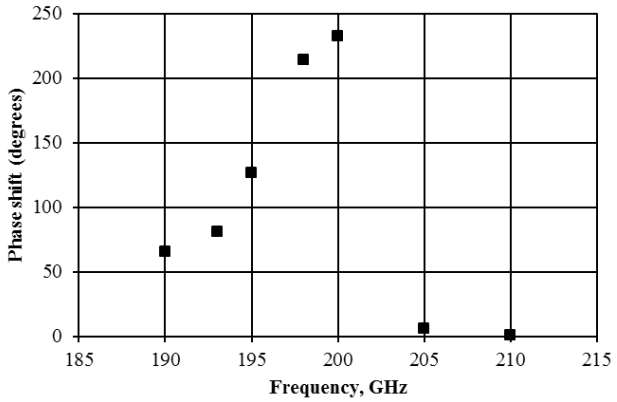


Figure 2.20: Total phase shit as a function of frequency as the diode's capacitance is varied between -4 to 0.5 V

The series resistance of the diode was anticipated to be 4 Ω [44] from calculation. However fitting the circuit model to the measured scattering parameters required the diode to have a series resistance of approximately 14 Ω. The larger-than-expected series resistance is hypothesized to be due to the thickness of the GaAs's n^+ layer. The skin depth of the GaAs's n^+ layer at 200 GHz, with a substrate doping of $5x10^{18}$ cm^{-3}, is 2.7 μm. Nonetheless, the primary objective of this work was as a proof-of-concept demonstration to study heterogeneous integration of GaAs epitaxy on silicon, and only a substrate with an 800 nm n^+ layer was available for this experiment. This thinner n^+ layer will contribute to the measured device loss due to skin effect. DC least-square fitting to the measured data resulted in a diode ideality factor (η) of 1.2, I_s of $1.2x10^{-13}$ and a series resistance of 9.3 Ω. These diode parameters are reasonable and are similar to the specification provided for commercial diodes [45]. The semi-log plot of the current-voltage characteristics is shown in Figure 2.21. The result from this work successfully illustrates GaAs epitaxial layer transfer to a SOI substrate and provides an initial foundation for creating high frequency Schottky diodes on robust silicon membranes.

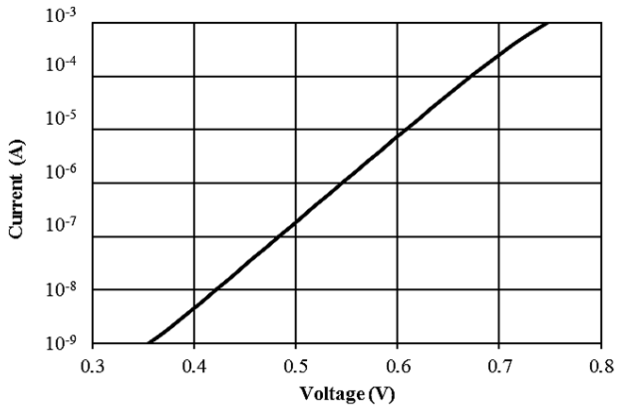


Figure 2.21: DC current-voltage characteristics of the WR-5 diode with 4.5 μm diameter anode

2.5 Summary

This chapter documents the initial work on transfer of GaAs epitaxy to silicon and provides the foundation for the research described in the remaining chapters. The fabrication process for a creating quasi-vertical diode, by thinning the GaAs handle and bonding to a silicon substrate, is analogous to the steps described in this chapter. Likewise, the simulation tools Agilent *ADS* and Ansoft's *HFSS* are employed to model the diode and its parasitics. Confirmation that the GaAs epitaxy could be successfully transferred to silicon and used to make diodes with properties similar to comparable devices is the main contribution of the 200 GHz phase-shifter design.

Chapter 3

Micromachined Probes for On-Wafer Characterization of Schottky Diodes

3.1 Background

The WR-5 (140-220 GHz) proof-of-concept phase-shifter, described in Chapter 2, exposed a number of shortcomings with the GaAs on SOI fabrication process. These include: (1) tearing of the GaAs epitaxial layers during substrate bonding due to the use of Apiezon W wax, (2) the delamination of silicon dioxide used for defining the Schottky anode, and (3) thickness variation of the spin-on-glass (SOG) glue used for bonding the GaAs epitaxial layers to SOI. Additionally, the varactor's series resistance was measured to be in the 9-14 Ω range instead the 4 to 5 Ω range expected from calculation. To address these issues, a new quasi-vertical Schottky diode geometry was investigated. This new geometry is discussed in detail in Chapter 4. In the quasi-vertical diode design, the ohmic contact is moved directly below the airbridge-contacted Schottky anode. This reduces the minimum distance at which the ohmic contact can be fabricated, and the diode current path is moved away from the semiconductor-air interface with its surface states and traps and confined to the epilayers. Hence, the quasi-vertical diode geometry is predicted to have a lower series resistance, and was design to mitigate the fabrication issues mentioned above.

To evaluate the quasi-vertical geometry, the scattering parameters of the structure shown in Figure 3.1 were measured in the 15-25 GHz range. Measurements indicated that placing the ohmic contact directly below the Schottky area does, as anticipated, reduce the diode series resistance. The *s*-parameter measurements were made using an Agilent 8510C vector network analyzer and GGB Industries, coplanar waveguide (CPW) Picoprobes (40A-GSG-150-P). Layout of the complete diode

structure characterized using on-wafer probes is shown in Figure 3.2. Single diodes, as well as diodes with tuning stubs (effectively forming a phase-shifter) were measured to evaluate the quality and performance of the quasi-vertical diode geometry.

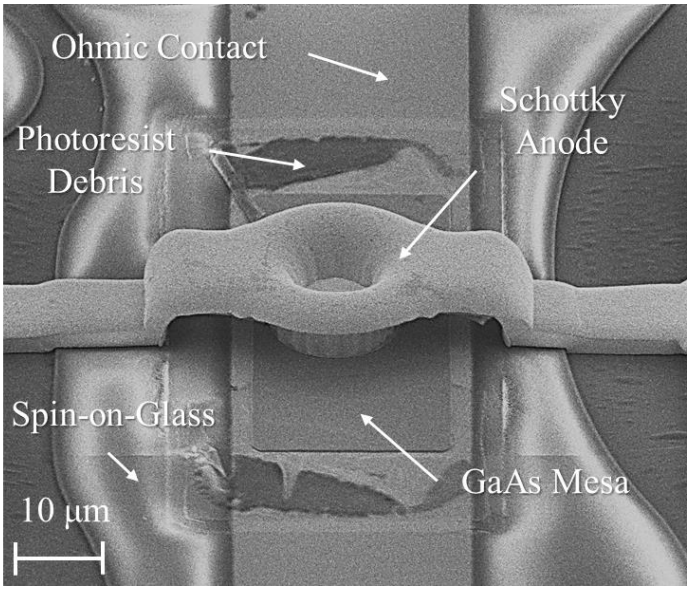


Figure 3.1: 15-25 GHz quasi-vertical diode geometry

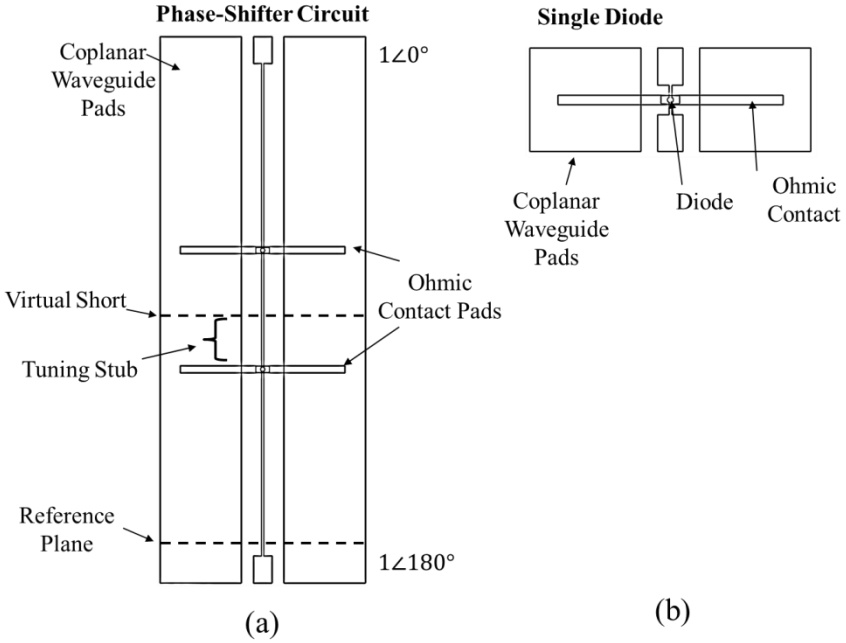


Figure 3.2: Coplanar contacted quasi-vertical diode structures for 15-25 GHz measurements, (a) phase-shifter diode or diode with a short circuited tuning stub for differential excitations, (b) single diode for two-port measurements

To characterize quasi-vertical devices designed for submillimeter-wave applications, on-wafer measurements in the 330-500 GHz, 500-750 GHz and 750-1100 GHz were performed using frequency extension modules (manufactured by Virginia Diodes, Inc.), a vector network analyzer, and on-wafer probes designed by Dominion Microprobes that incorporate a 90° twist. The twist mates the frequency extension units with the on-wafer probe block and is needed to rotate the polarization of the *E*-field from the frequency extender so that it couples properly to the probe. The measurement setup is shown in Figure 3.3.

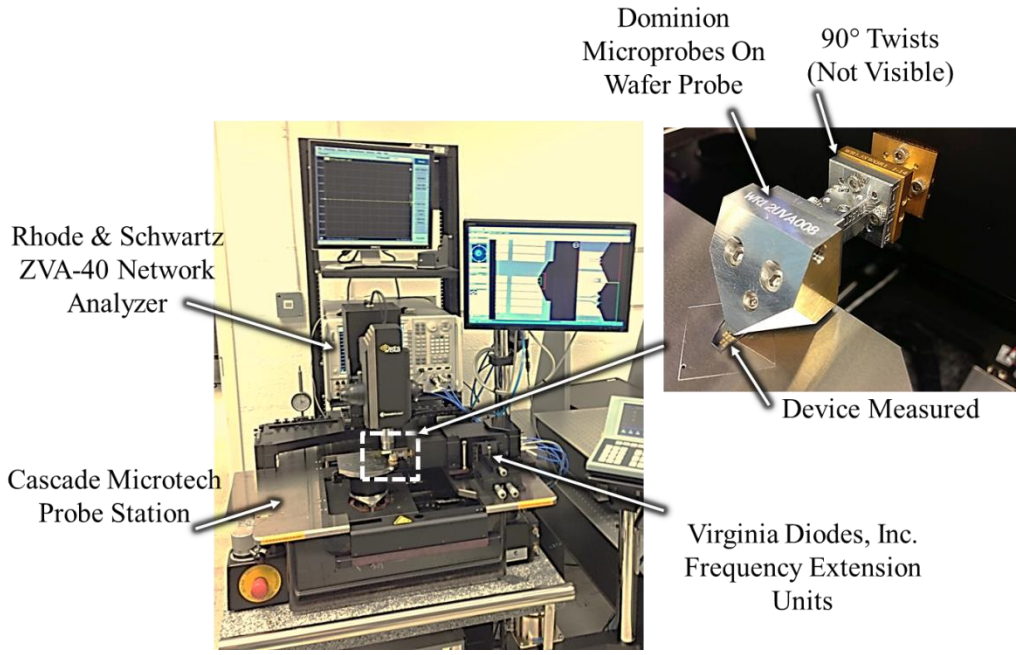


Figure 3.3: 330-1100 GHz measurement setup.

The micromachined on-wafer probe design implemented in this work is based on research by Reck [46], Chen [47] and Zhang, and the twist fabrication and simulation process originated from efforts by Stanec [48], Chen [49] and Yu [50]. This chapter documents and describes the structure and fabrication of the micromachined probes for diode characterization. The design and characterization of the probes are the work of Bauwens and are described in his dissertation [51], and the probe fabrication and process development, described in this chapter, are the work of the author.

3.2 Micromachined On-Wafer Probes

The micromachined on-wafer probe assembly (Figure 3.4) consists of a 15 μm microfabricated silicon chip, and a milled E-plane split-block waveguide manufactured using computer numerical control machining techniques. The housing block features milled recessions that self-align the probe chip within the block and allow it to be clamped in place between the two block halves without the need for adhesives. As shown in Figure 3.4, an intermediate transmission line is necessary to transport the energy from rectangular waveguide to CPW probe tips. This transmission line is made of the waveguide block metal shielding and the silicon substrate. The type of transmission line used leads to two basic probe designs: a microstrip [52] and a quasi-coaxial [53] design. In the microstrip design, the *E*-field distribution is mostly confined within the substrate, while in the quasi-coaxial probe chip the fields terminate on the waveguide block metal shielding. A detailed view of the 15 μm thick microfabricated silicon chip using the quasi-coaxial design is shown in Figure 3.5(a). The probe chip is composed of a DC connection tab, DC bias filter, E-plane waveguide transition, clamping tabs, and a transition from enclosed probe channel to coplanar tips. For DC biasing the DUT using the on-wafer probe, H20E silver epoxy is used to attach the DC connection tab to a gold plated quartz substrate, which in turn is soldered to the SMA connector using MWS Wire Industries MW80-C 48 SPN-155 wire. The DC bias filter is a low pass hammerhead filter and prevents the RF from seeing the DC connection tab in the waveguide band. The E-plane radial transitions and the enclosed probe channel to CPW transition allow the *s*-parameters of the device under test (DUT) to be measured. The clamp areas self-align the probe chip within the block and secure the chip in place to generate force during DUT probing.

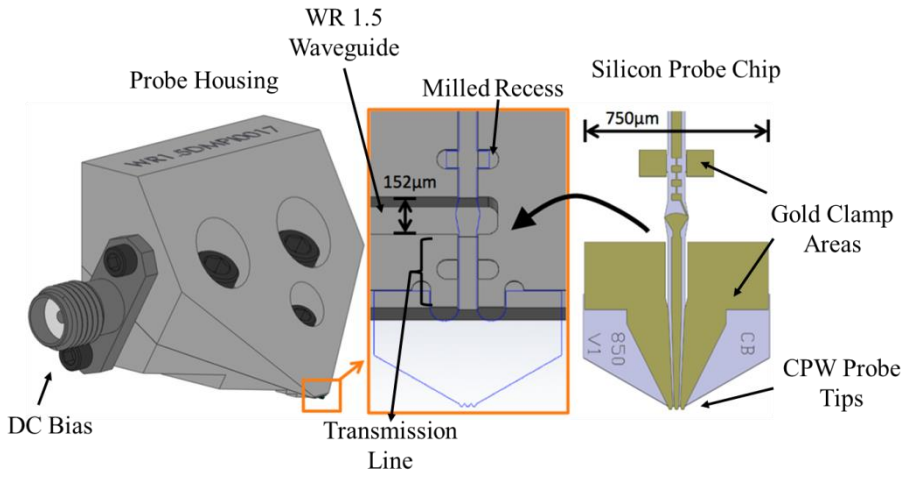


Figure 3.4: Dominion Microprobes WR1.5 (500-750 GHz) on-wafer probe assembly.

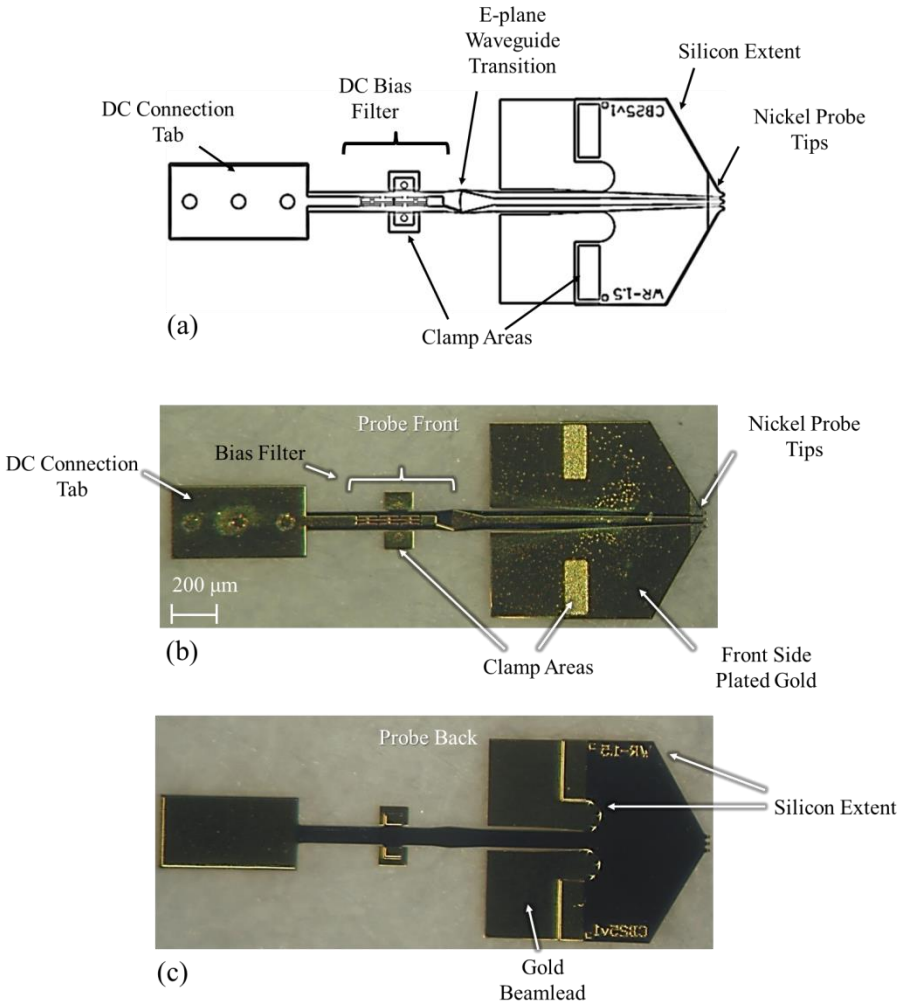


Figure 3.5: Detail view of WR1.5 microfabricated silicon chip, (a) device outline view, (b) front view of the fabricated probe, (c) back view of the etched probe.

3.3 Probe Fabrication

The silicon-on-insulator (SOI) substrate used for the on-wafer probe fabrication, is composed of a 15 μm high resistivity (>10 kΩ-cm) "device" layer, a 1 μm buried oxide (BOX) etch stop layer and a 450 μm "handle" layer. The probe fabrication process begins by reactive ion etching (RIE) of 24 μm vias through the 15 μm device layer. The vias are essential to the microstrip version of the probe chip design since they provide the transition from an enclosed microstrip channel to the coplanar waveguide tips. In the case of the enclosed probe channel version of the probe design, these vias prevent possible mode excitation in the silicon substrate of the clamping regions. After the via etch, a titanium and gold seed layer (7/22 nm) is sputtered over the wafer, photoresist is patterned and 1.5 μm gold is plated through this photoresist to create the front side metallization as shown in Figure 3.7(a) and (b). The front side metallization defines the DC connection tab, DC bias filter, E-plane waveguide transition, clamping regions, and the transition from enclosed probe channel to coplanar tips. The probe tips experience the most wear during use with the DUT and are protected with a second layer of hard metal. The metals plated and evaluated for the probe tips are cobalt hardened gold (plating solution Orosene 990), nickel (plating solution Technic, Inc. Nickel Sulfamate RTU), and rhodium (plating solution Rhodium HTRH225 and HORHSR magnesium based stress reducer). Cobalt hardened gold, nickel and rhodium were chosen due to their hardness (Table 3.1), and the fact that they could be readily plated. After plating the front metal and the tip protection layer, 18 μm thick gold clamps are fabricated as shown in Figure 3.6(c). These gold pillars will be compressed between the two halves of the E-plane split block housing to hold the probe in place.

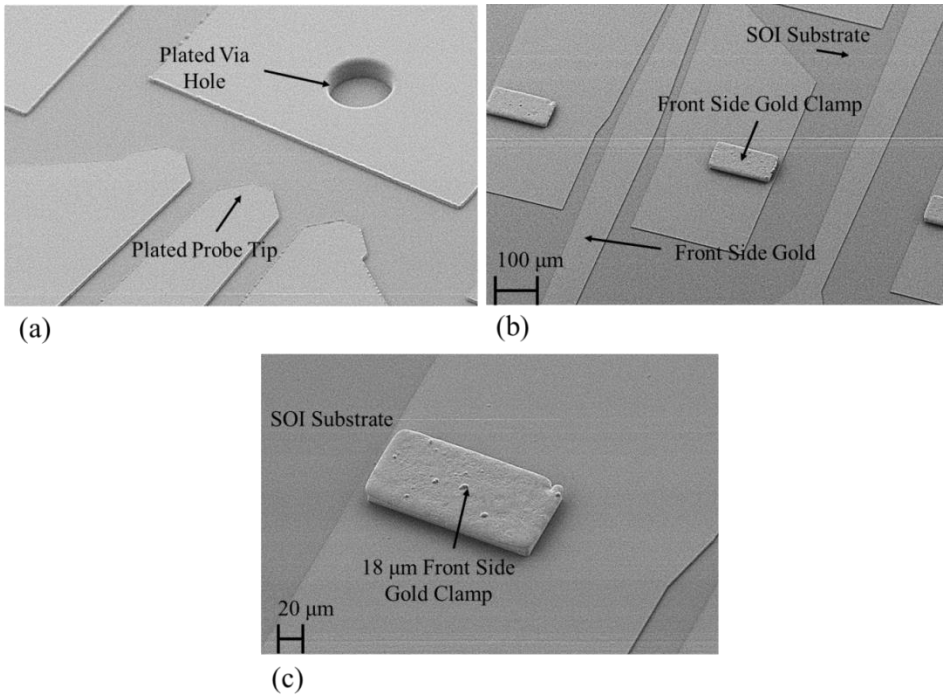


Figure 3.6: Front side processing, (a) gold plated via holes, (b) the front side gold clamp, (c) close up of the clamp region

The last front side processing step is removal of the gold seed layers using gold dry etch (80 sccm argon, 20 mT, DC -720V, RF 140 W, 10 minutes) and the removal of the titanium seed layer using a buffered oxide wet etch. The SOI wafer is then bonded to a silicon carrier using Waferbond CR-200, as shown in Figure 3.7(c). The bonding process involves spinning Waferbond on both the sample and the silicon carrier at 3 KRPM for 30 s. The sample and the carrier are then cured at 120°C for 2 minutes and 180°C for 2 minutes to remove the excess solvent from the Waferbond. Finally, the wafers are placed in a vacuum press and after outgassing at -30 psi for 5 minutes, are brought into contact and heated to 180°C for 2 minutes to bond the SOI sample to the carrier. The sample is then cooled to 70°C and is thinned using a combination of dicing and reactive ion etching (RIE) to reach the buried oxide etch stop layer. Buffered oxide etch is used to remove the BOX layer. Backside titanium and gold seed layers (10/50 nm) are then evaporated on the 15 µm thick device layer. Following this, gold is plated through a photoresist layer, and an RIE based extents etch (35 sccm C4F8, 30 sccm SF6, 0°C, 15 mT, RF 40 W, ICP 500 W) is used to define the silicon chips geometry, separate probes, and create the chip gold beamleads (Figure

3.7(d)). Scanning electron microscope (SEM) images of the backside processing after the extents etch are shown in Figure 3.8.

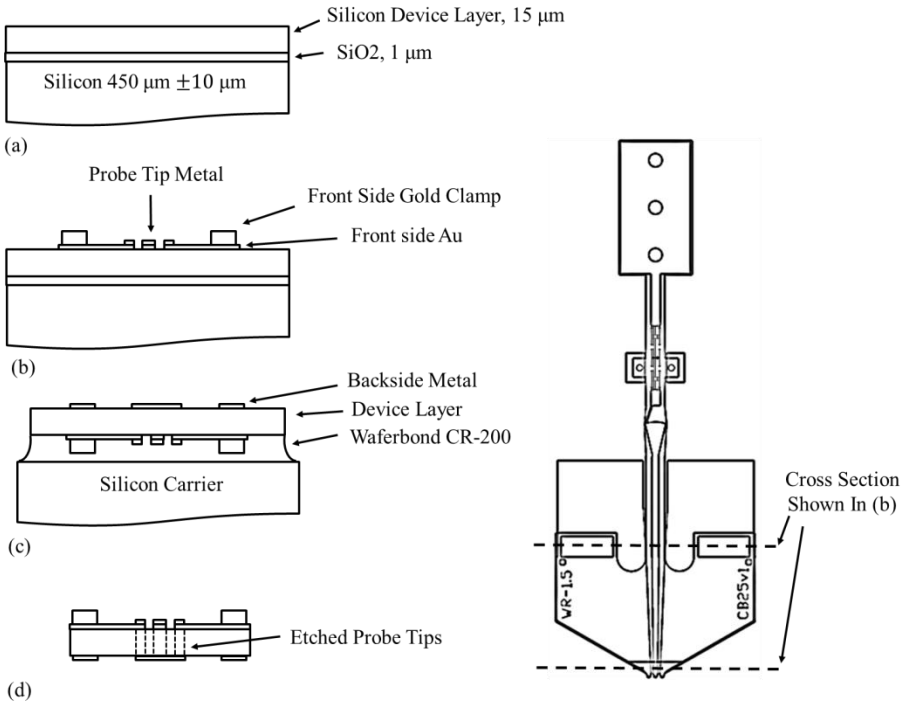


Figure 3.7: Probe fabrication steps, (a) SOI device layers, (b) front side metallization, (c) back side metallization, (d) silicon probe chip after extents etch and release

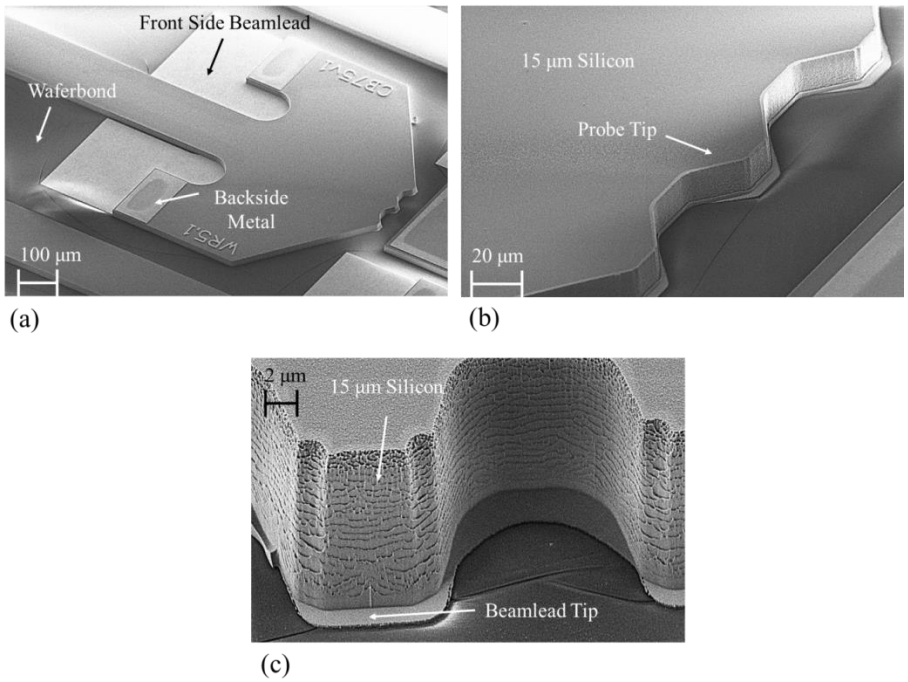


Figure 3.8: Back side processing, (a) backside metal, (b) details of the extent etch, (c) the probe tip beamleads

3.4 Twist Fabrication

As described in Section 3.1 the quasi-vertical diode measurement setup consists of a frequency extension module, a vector network analyzer, an on-wafer probe and a 90° waveguide twist. The twist mates the frequency extension unit with the on-wafer probe block and is needed to rotate the polarization of the E-field from the frequency extender so that it couples properly to the probe. Figure 3.9(a) shows the geometry of the twist used in this work and the sections of the waveguide to which it mates.

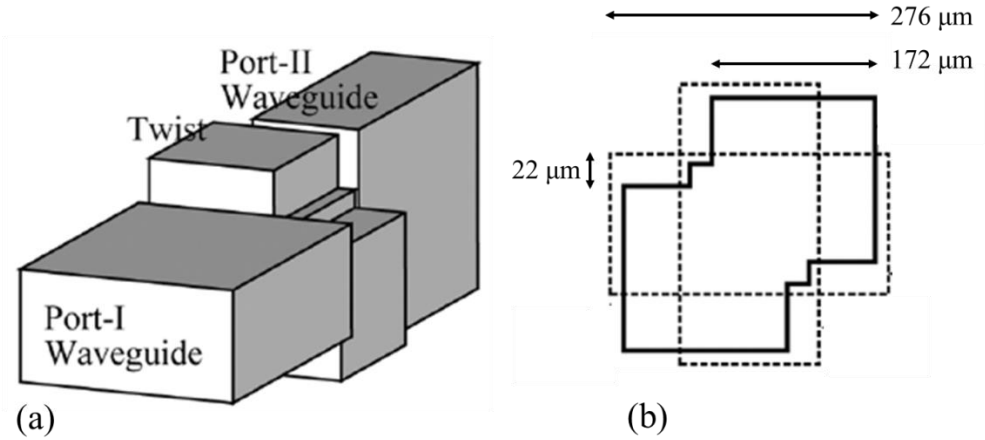


Figure 3.9: 90° twist shim, (a) diagram showing waveguide twist mating waveguides with different polarizations, (b) dimensions for WR 1.2 (600-900 GHz) waveguide twist

The twist fabrication process is discussed in this section, with greater detail provided in Appendix B. The twist shim is created by first pattering a KMPR photoresist mold and then plating nickel using this mold. The first processing step is the evaporation of a titanium/gold/titanium (20/50/20 nm) seed layer on a 1”x1” inch silicon substrate. The final titanium layer serves as an adhesion promoter for the KMPR 1050 negative photoresist. The substrate dimensions and the spin speeds determine the final thickness of the KMPR photoresist. For example, in the case of a 1”x1” inch silicon substrate: 800 RPM spin speed results in a 220 μm KMPR film, 730 RPM results in a 350 μm film, and 630 RPM results in a 450 μm film. The resist is typically spun so that the final film thickness is ~50 μm thicker than the desired shim width. This is because nickel does not plate the KMPR mold uniformly and a planarization step is required after nickel plating. After spinning KMPR, a 4 hour prebake is used to drive some of the solvent

from the resist at 100°C. This prebake is followed by ~10 minute exposure using a 350 nm UV filter. The long exposure time is required when working with KMPR resists thicker than 300 μm to allow radiation to penetrate the thick material. This is followed by a post exposure bake at 100°C for ~10 minutes. The photoresist is next developed in 300 MIF, as shown in Figure 3.10(a), and nickel is plated into the mold (Figure 3.10(b)). Finally, the twist shim is lapped to the desired thickness, released from the silicon handle using 1:3 KOH:H_2O soak (Figure 3.10(c)), and gold plated to further reduce the RF losses.

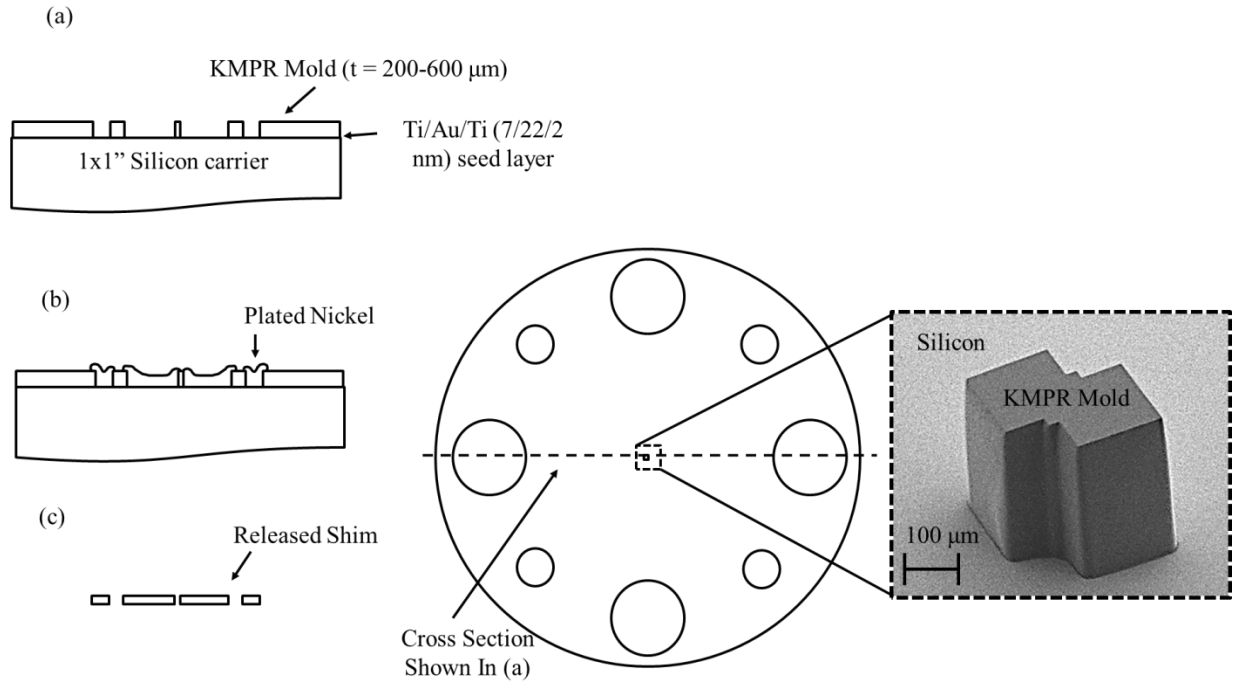


Figure 3.10: 90° twist shim fabrication processing steps, (a) KMPR mold development, (b) nickel plating the KMPR mold, (c) releasing the nickel ship from the mold

3.5 Probe Fabrication Results

As described in the introduction, the on-wafer probe chips were fabricated to characterize the quasi-vertical diodes at submillimeter wavelengths between 330-1100 GHz. The initial probe chip fabrication exposed a number of issues associated with the tip metallization. As shown in Figure 3.11, the probe's beamlead tips extend beyond the silicon substrate, and as the probe tips are brought into contact with a measured device the tips deflect and generate force at the contact points. During the measurement of

quasi-vertical diodes, this contact force would often create a bond between the hard gold tips and the gold coplanar contact pads. Upon lifting the probe, the tips would detach and remain on the DUT test pads as shown in Figure 3.12. It is speculated that for subsequent measurements, the bare silicon tip would erode the gold coplanar contacts pads as seen in Figure 3.13.

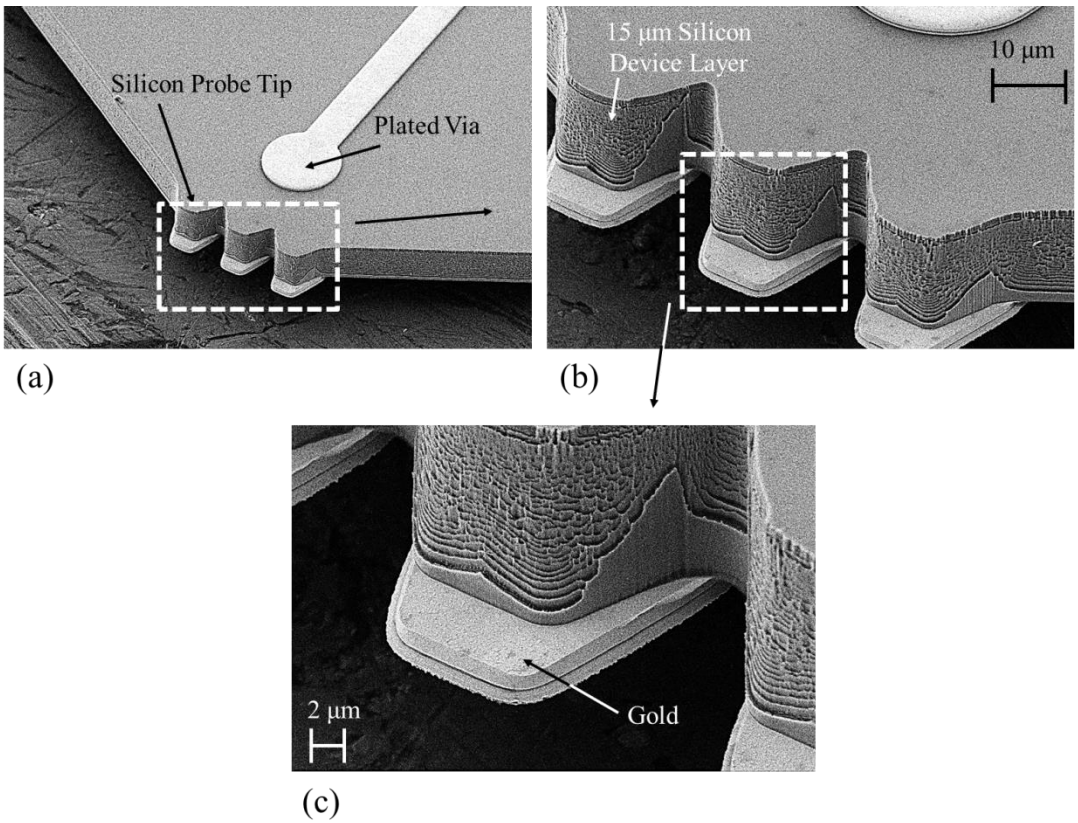


Figure 3.11: Detail of probe tip showing: (a) the RIE etched probe tips and the plated via hole for the enclosed microstrip channel version of the probe design, (b) probe tip detail, (c) gold beamlead extending beyond the tip.

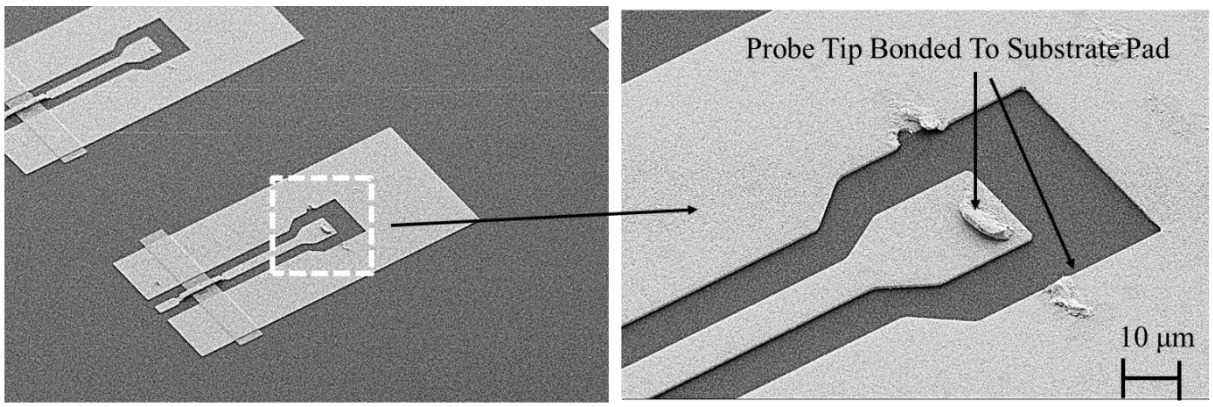


Figure 3.12: (a) coplanar waveguide (CPW) contacted quasi-vertical diode, (b) probe tip bonding and detaching on the CPW pad

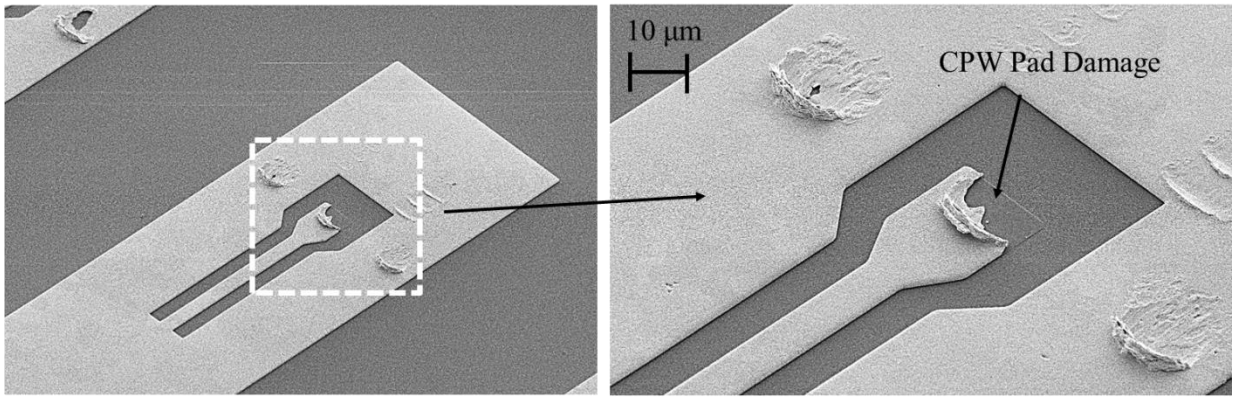


Figure 3.13: (a) delay short CPW calibration standard, (b) delamination of the gold CPW pads after quasi-vertical diode on-wafer probe measurement

A potential solution to this issue is to include a nickel or rhodium capping layer to the probe tips to prevent gold-to-gold compression bonding during measurements. Table 3.1 lists the different possible capping materials available to microfabrication lab. The elastic modulus and hardness measurements were made at the University of Virginia by John Gaskin using a nanoindentation method, and the conductivities were obtained using a Jandel four point probe with 1 mm contact spacing. Nanoindentation and four point probe measurements were made on a 1" diameter, 250 μm thick quartz wafer with an evaporated titanium and gold seed layer (10/50 nm), and 3 μm of plated metal. Only a 13x13 mm^2 area of the 1" diameter wafer was plated with metal for measurements. The hardness data in Table 3.1 refers to

the average value of more than twenty measurements, made 50 μm apart from one another. STD refers to the standard deviation of the measurements used to calculate the average. Porosity or roughness were not measured for these samples, but could also have an impact on the results.

Sample	Measured Elastic modulus (GPa)	Elastic modulus STD	Measured Conductivity (S/m)	Conductivity from literature (S/m)
Gold (Techni)	49.7	2.2	$3.2x10^7$	$4.1x10^7$
Hard gold	61.9	1.66	$5.8x10^6$	
Nickel	154.6	24.4	$7.6x10^6$	$1.43x10^7$
Rhodium 40 mL	195.9	40	$6.4x10^6$	$2.2x10^7$
Rhodium 160 mL	213	10	$5.7x10^6$	$2.2x10^7$
Evaporated gold			$1.3x10^7$	
Silver (Techni)			$1.0x10^7$	$6.3x10^7$

Table 3.1: Properties of plated metals.
Column labeled 'Conductivity from literature' is from the following reference [54]. Rhodium 40 and 160 mL refers to the amount of HORHSR magnesium based stress reducer in 1 liter of rhodium plating solution. 'Elastic modulus STD' refers to the standard deviation.

As seen in Table 3.1, the hard-gold plating solution is softer than nickel or rhodium. Furthermore, the hard gold tips were still observed to bond to the device pads during measurements. Scanning electron microscope images of the plated hard gold probe tip are shown in Figure 3.14.

The next metal studied for probe tip protection was nickel (Figure 3.15). Nickel's favorable properties are its elastic modulus (154 GPa compared to 62 GPa for hard gold) and its resistance to cracking or compression bonding to gold during on-wafer measurements. Using nickel tipped probes, quasi-vertical diodes were characterized without CPW pad damage as shown in Figure 3.16. Nevertheless, nickel forms an oxide, which must be penetrated for DC contact. This is not the case for rhodium or gold; therefore an important goal is to ultimately use rhodium as the tip protection layer.

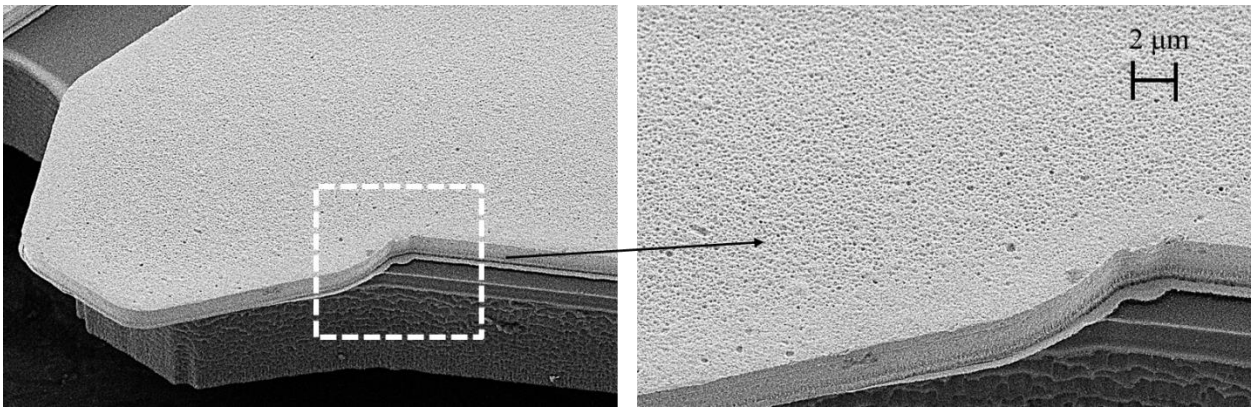


Figure 3.14: Detail of plated hard gold

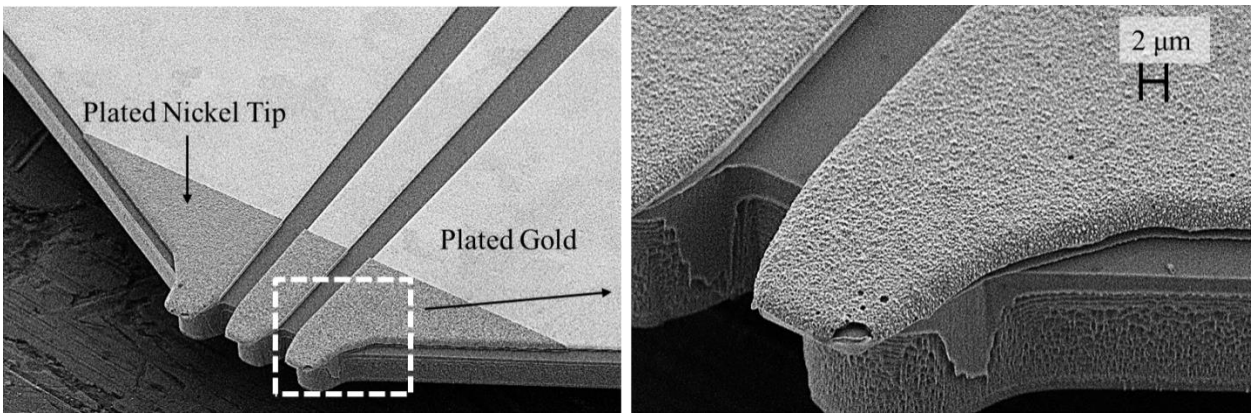


Figure 3.15: Nickel plated probe tips

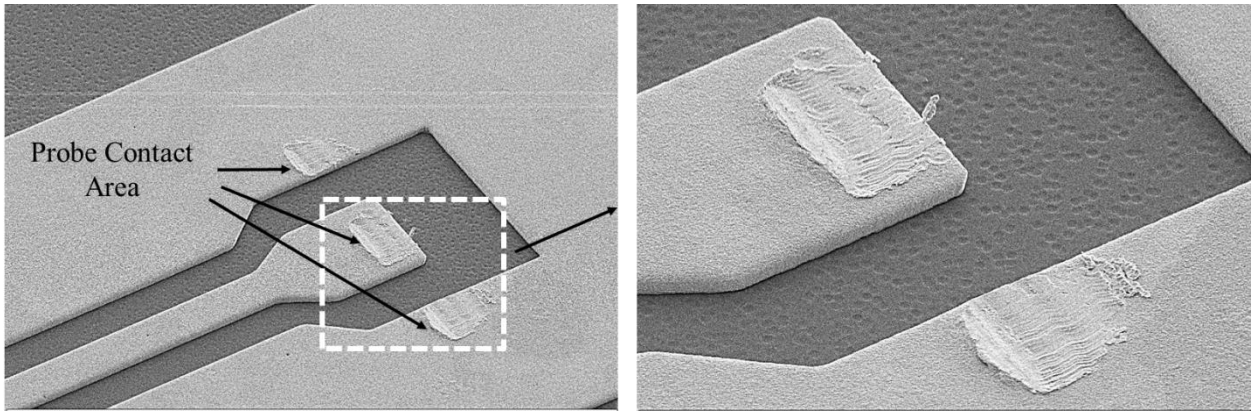


Figure 3.16: Detail of a CPW pad after contact by a nickel plated tip

Rhodium plated probe tips are shown in Figure 3.17. For this initial run, a magnesium based stress reducer was not used. Rhodium is intrinsically a brittle metal [55], and large cracks are immediately visible after plating a 1 µm rhodium layer on 1.5 µm of plated gold. Technic, Inc. recommends adding between 40 to 160 mL of HORHSR stress reducer per liter of rhodium plating solution to obtain better

films. Figure 3.18 shows the result for rhodium plated CPW tips when 40 or 160 mL of stress reducer is used. The stress reducer results in a smoother plated surface; however this film is still stressed, as the tips sheer after multiple contacts with the CPW pads. Future work should involve plating rhodium on nickel. In this case, nickel would reduce the bending of the beamlead tips during measurements, which could alleviate stress in the rhodium and prevent the tips from cracking.

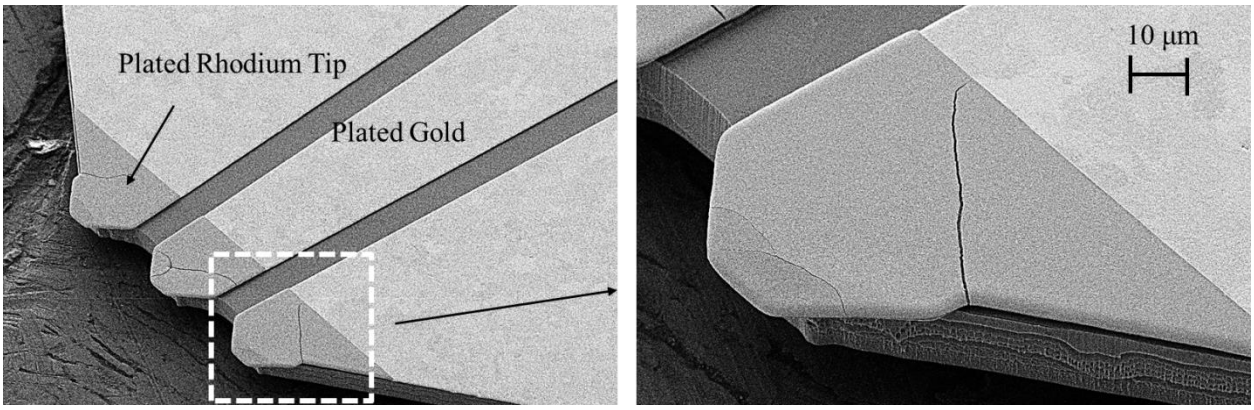


Figure 3.17: Plated rhodium with no stress reducer

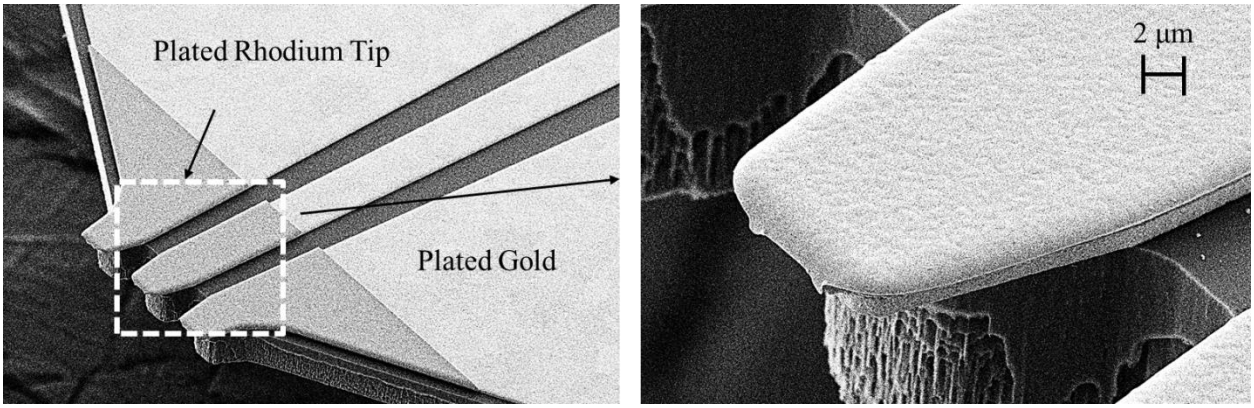


Figure 3.18: Plated rhodium with 40 or 160 mL/L stress reducer produce the same results

3.6 Conclusions

This chapter summarizes the fabrication, characterization and development of micromachined on-wafer probes used in the measurement of quasi-vertical diodes in the 330-500 GHz, 500-750 GHz and 750-1100 GHz band. Gold-to-gold compression bonding and tearing of the probe tips during initial measurements prompted the search for a durable CPW tip capping metal. Nickel was found to possess most of the

characteristics needed for making successful contacts to CPW DUT. Subsequent on-wafer measurements in Chapter 4 use nickel tipped probes for characterizing the quasi-vertical diode *s*-parameters.

Chapter 4

Quasi-Vertical Diodes for Submillimeter-Wave Applications

Over the decades, GaAs Schottky diodes have evolved from a simple, single-element whisker-contacted geometry [56], [57] to a planar chip with integrated finger contact [58] and finally to a fully-monolithic component that is commonly integrated into thin-membrane structures [59], [60] or heterogeneously bonded to host substrates supporting associated circuitry [61], [62], [63]. This evolution in diode geometry allows for the integration of Schottky diodes with their respective matching and biasing networks, which in turn facilitates the diode assembly and modeling process. The 200 GHz phase-shifter, described in Chapter 2, is the first demonstration of an integrated GaAs Schottky diode bonded to a host silicon substrate [64]. The advantages of utilizing silicon include superior mechanical robustness and higher thermal conductivity compared to GaAs or quartz. Moreover, the silicon-on-insulator (SOI) handle may be post-processed after diode fabrication to realize an ultrathin (5-15 μm thick) membrane device. Silicon micromachining also allows for etching of arbitrary geometries with beamleads for interconnects and mounting tabs, thus permitting near-seamless incorporation of the integrated diode into an external circuit housing without need for adhesives, wirebonding or solder connections.

4.1 Origins of the Quasi-Vertical Diode

The 140-220 GHz proof-of-concept phase-shifter project, presented in Chapter 2, nevertheless revealed a number of issues with the GaAs on SOI planar diode fabrication process. This process begins by bonding the GaAs wafer to a silicon carrier using Apiezon W or black wax, and thinning the GaAs semi-insulating layer to reach the epitaxial layers. The epitaxial layers on the Apiezon W wax are then bonded to a SOI

substrate using spin-on-glass (SOG), and the Schottky diode processing on SOI can then begin. The use of Apiezon wax for transferring the epitaxial layers to the desired substrate is based on the work of Midkiff [35] and this material reflows at the bonding temperatures of about 180°C, which does not pose a problem for epilayers thicker than 4 μm. However, when bonding GaAs layers as thin as 1μm, this method proved highly unreliable, resulting in fracturing of the epilayers. Therefore, an alternate thinning and bonding method was developed.

A number of other issues emerged with the 1 μm of silicon dioxide (SiO2) deposited using plasma enhanced chemical vapor deposition (PECVD). This layer was used to form the Schottky anode, as fabricating diodes with well characterized geometries is critical for designing proper matching networks for the diode. For the 200 GHz phase shifter project, reactive ion etching (RIE) was utilized to create the anode opening in the SiO_2. This etch removed 930 nm of SiO_2, leaving 70 nm to protect the GaAs from RIE damage. A buffered oxide wet etch (BOE) was used to remove the remaining silicon dioxide. As shown in Figure 4.1, it is difficult to visually determine whether the SiO_2 is completely removed from the Schottky anode area, even using a scanning electron microscope. An alternate method for determining the BOE anode opening times is to gold-plate an array of test anodes, and use the resulting etch times for the final devices. However, neither method is foolproof. The deposited oxide exhibits poor adhesion to GaAs and SOG, resulting in delamination during processing or after the extents etch (Figure 4.2 and Figure 4.3.)

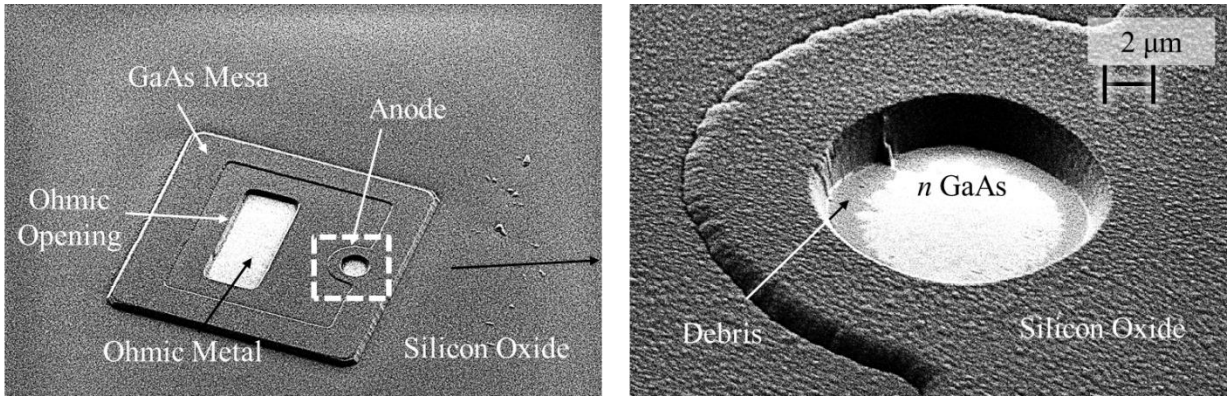


Figure 4.1: Anode opening through silicon oxide for 200 GHz phase shifter

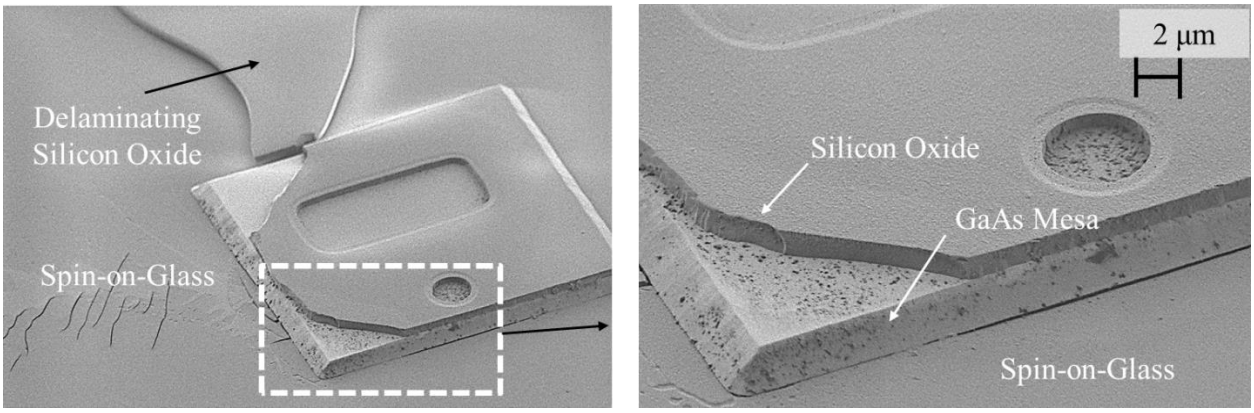


Figure 4.2: Silicon oxide delamination on GaAs mesa and SOG substrates

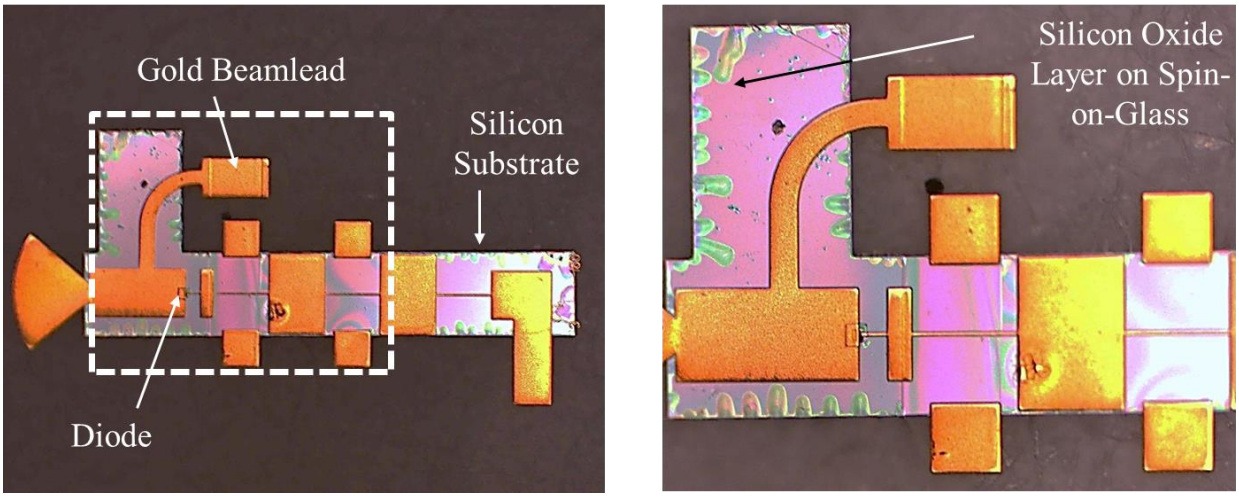


Figure 4.3: Silicon oxide delamination after silicon extent etch

Other issues discovered from the 200 GHz phase shifter work include non-uniformity of the AuGe/Ni/Au ohmic contacts after annealing, and uncertainty in the electrical and physical properties of spin-on-glass (Figure 4.4(b)). The surface roughness of the ohmic contact shown in Figure 4.4(a), gives rise to inconsistencies in specific contact resistivity measurements. This in turn results in large uncertainty in the diode's series resistance. At the same time, the electrical characteristic for FG65 SOG provided by Filmtronics, Inc. is only known to 10 MHz. The thickness of this SOG layer across the wafer was also non-uniform after the bond. It is therefore be difficult to accurately measure the dielectric constant and loss tangent of this adhesive material for 350-1100 GHz band.

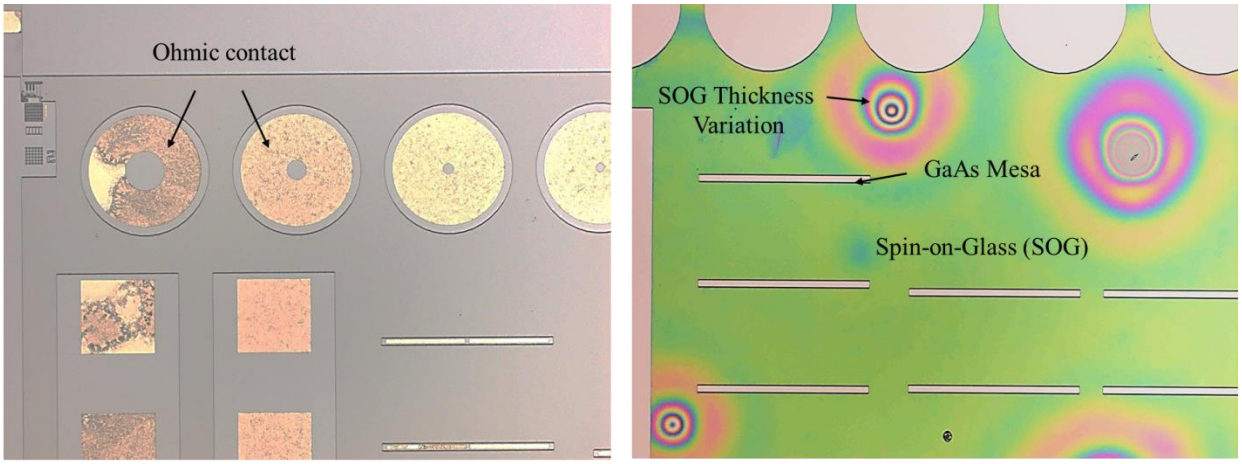


Figure 4.4: (a) AuGe/Ni/Au ohmic contact surface roughness after rapid thermal annealing, (b) SOG glue shown in green after the GaAs mesa etch and before silicon oxide deposition

The final motivation for research into a new diode geometry was the 200 GHz phase-shifter's measured series resistance. The series resistance of the 4.5 μm anode diameter diode was expected to be approximately 4 Ω from theory [65]. However, DC and scattering parameter data indicated a 9-14 Ω range of series resistance. It was unclear whether this difference was due primarily to the thin 800 nm n^+ GaAs ohmic contact layer (which is thinner than one skin depth) or if other processing steps also played a role. As shown in Figure 4.5, the current path from the Schottky contact to the ohmic area is along the semiconductor-silicon oxide interface for a planar device. Current must travel from anode through the lightly and highly doped epitaxial layers, before reaching the ohmic contact metal layers. The current must finally travel through the ohmic metal to reach the via to the plated metal. Traps and other imperfection along the path can contribute to the diode series resistance. This is illustrated in Figure 4.6 which shows the contributions to series resistance arising from the contact resistance (Rc), epi-layer resistance (Repi), and spreading resistance (Rsp).

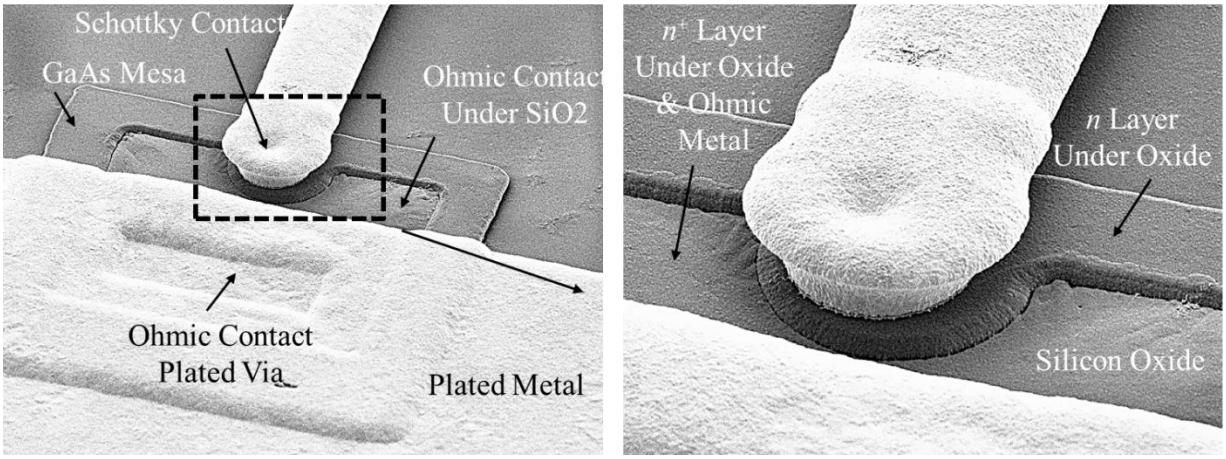


Figure 4.5: Planar GaAs Schottky diode anode and ohmic contact

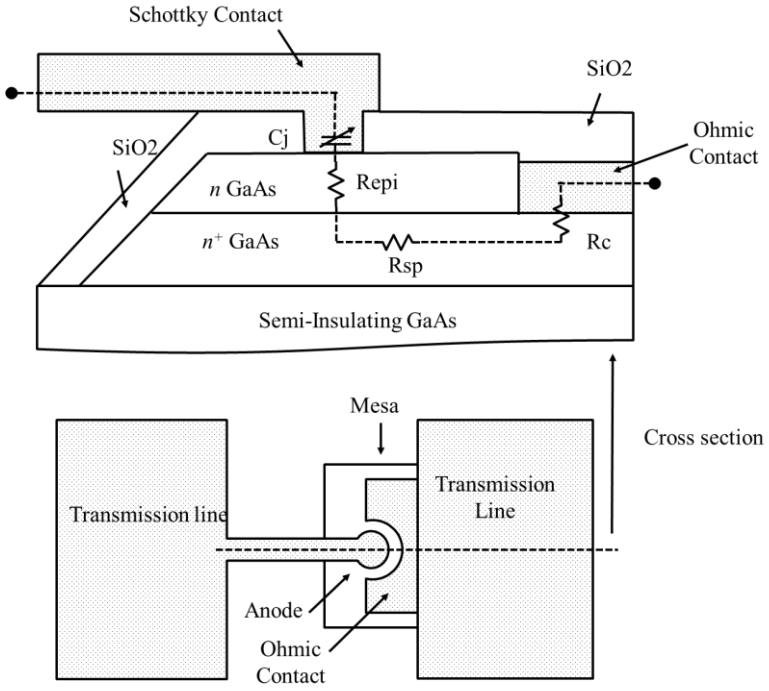


Figure 4.6: Contributions to planar diode series resistance

The quasi-vertical geometry shown in Figure 4.7 is proposed to address the issues encountered with the planar design. The silicon dioxide used to define the anode is replaced by sacrificial photoresist, black wax bonding is eliminated, all spin-on-glass is removed except for areas under the ohmic contact where it has no impact electrically, the ohmic contact metallurgy is changed to Ge/Pd/Au [66], and is moved directly under the Schottky anode. The final step is anticipated to lower the diode's series

resistance by bringing the ohmic contact in closer proximity to the anode and allowing current to flow through the material bulk. This feature minimizes the distance of the current path and redirects current to the epilayers and away from possible interface traps.

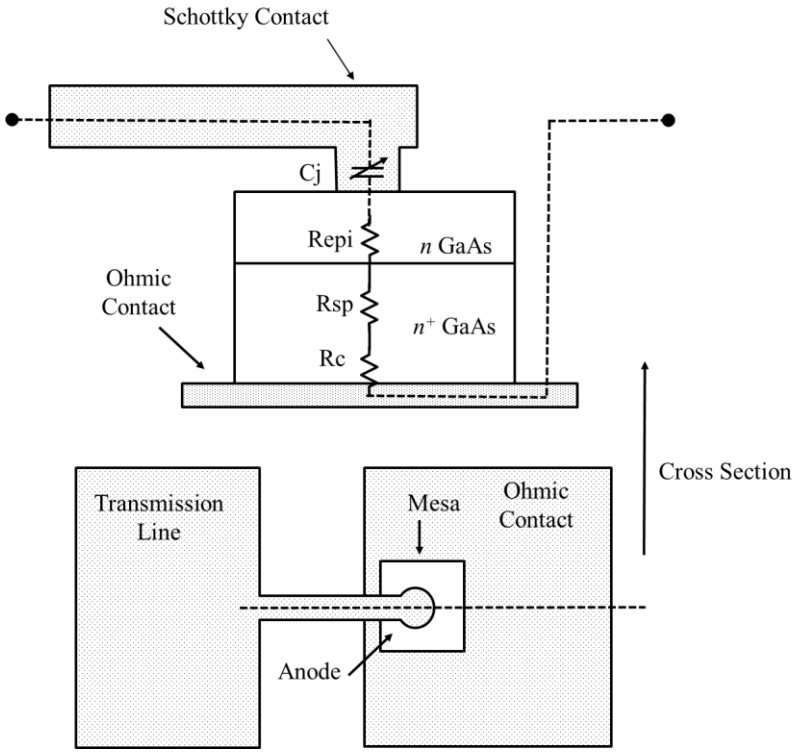


Figure 4.7: Geometry of quasi-vertical diode

4.2 Quasi-Vertical Diode Structure

As described above, a primary motivation for investigating the quasi-vertically-oriented diodes is their potential for smaller device parasitics (in particular, lower series resistance) compared to diodes that have coplanar anode and ohmic contacts [67]. Since doping concentration, epilayer thickness, anode size, and ohmic contact formation processes can differ significantly, depending on the fabrication method and intended application of the diode, direct comparison of series resistances of diodes must be done with prudence. Nonetheless, as a point of reference, Table 4.1 lists a number of millimeter and submillimeter-wave diodes reported in the literature and generally shows that the series resistance of planar diodes with anode diameters of 3 μm or less typically range from about 6 Ω or higher, for commonly used epilayer doping and thicknesses.

Diode type	1. Doping (cm^{-3})	Epilayer (μm)	R_s (Ω)	diameter (μm)	Year/Ref.
SC1T5	2×10^{17}	0.1	14	1.2	1997 [68]
varactor	1×10^{17}	0.5	28	1.8	2003 [34]
varactor	1×10^{17}	0.5	4.6	4.3	2003 [34]
varactor	3×10^{17}	0.22	41	1.4	2003 [34]
varactor	8.5×10^{16}	0.73	7	5.0	2006 [61]
SB4T2	3×10^{17}	-	8.5	2.5	2014 [69]
SB4T2	3×10^{17}	-	5.5	3.0	2014 [69]
Planar	2×10^{17}	0.27	8	3.6	2013 [70]
1T7†	2×10^{17}	0.9	12	1.1	1994 [71]
1T14†	1×10^{18}	0.4	9	0.5	1994 [71]

Table 4.1: Measured series resistance of submillimeter-wave diodes
†The 1T7 and 1T14 are whisker-contacted diodes. All others listed in the table are laterally-oriented planar diodes.

Three primary factors are known to contribute to this series resistance: conduction through the diode's undepleted epilayer, spreading resistance through the diode's highly-doped (n^+) buffer layer, and resistance of the ohmic contact [72], [73], [74]. Resistance associated with the undepleted epilayer is largely a consequence of the diode's intended use, as it depends on anode area, doping and epilayer thickness — design parameters that typically are chosen based on the device's application as a varistor or varactor. The remaining factors, spreading and contact resistance, however, are *true* parasitics in the sense they contribute loss but serve no function other than to connect the device to external circuitry. Spreading and contact resistance depend on the doping and thickness of the n^+ buffer layer and the geometry of the device, as well as the metallization and process used to form the ohmic contact alloy. Consequently, these parasitic resistances can be minimized, to some extent, through judicious choice of the diode geometry.

Since the ohmic contacts of planar-oriented diodes typically subtend only half the anode circumference (Figure 4.10(a)), their associated series resistance tends to be twice what could be achieved with a fully encircled anode. Moreover, numerical studies comparing diodes with identical device parameters, but differing geometries, indicate that the series resistance of vertically-oriented diodes can be 20 to 30% lower than that of comparable planar devices [67]. This reduction in resistance is attributed primarily to the reduction in dimensions of the GaAs mesa, thus mitigating current crowding due to the skin effect, and bringing the ohmic contact in closer proximity with the diode active region. As an

example, the diode described in [67] and [75] is a quasi-vertical geometry consisting of a thin suspended GaAs membrane with backside ohmic contact (Figure 4.8). The fabrication process for this type of diode involves deposition of silicon dioxide on an *n*-GaAs layer. The GaAs wafer is then mounted on a carrier and the GaAs semi-insulating substrate is thinned to 6-8 μm by lapping. Via through-holes are then wet etched into the back of the thinned GaAs layer to reach the AlGaAs etch stop, as shown in Figure 4.9(a). The AlGaAs epitaxial layer is then removed and Ni/AuGe/Ni ohmic metal is evaporated on the n^+ GaAs, annealed and further plated. After forming the backside ohmic contact, the diode mesas are etched on the front side (Figure 4.9(b)). The anode is then formed by reactive ion etching the silicon dioxide layer, and the final plating step creates the air bridge and the connection to the ohmic layer (Figure 4.9(c)).

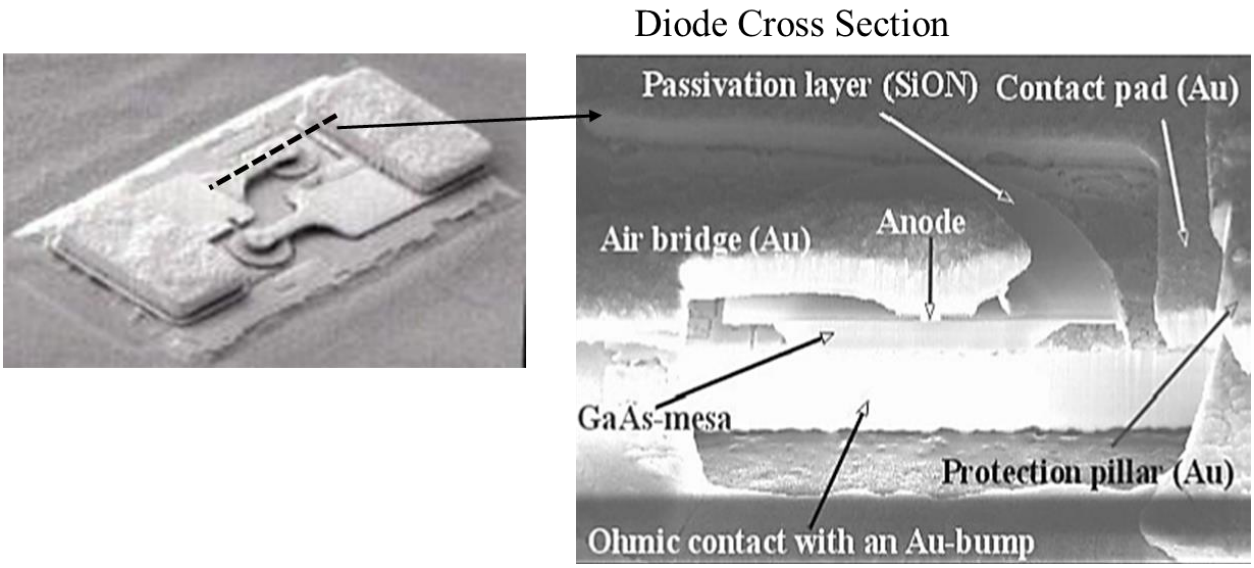


Figure 4.8: Darmstadt's flip-chip quasi vertical diodes, with device cross section

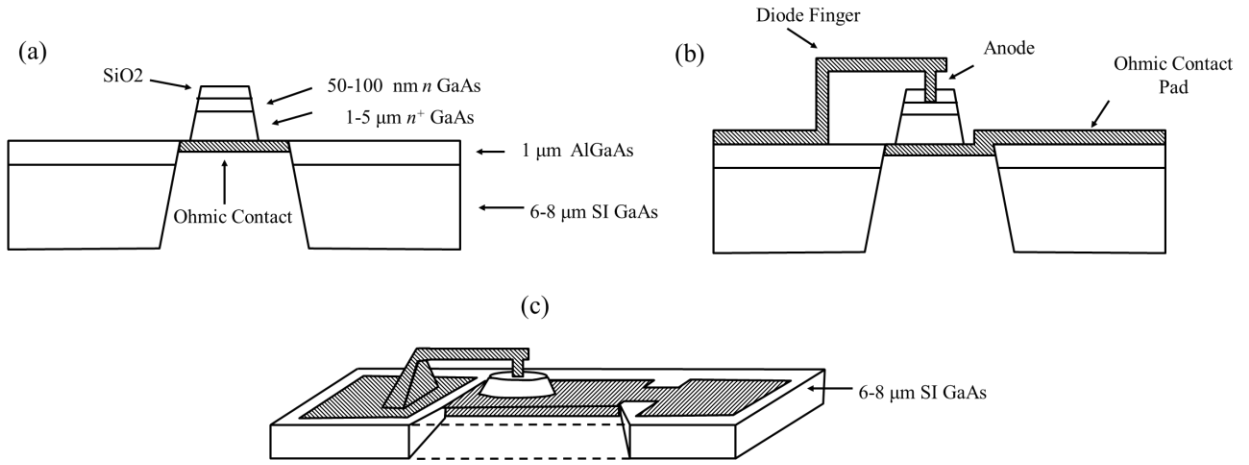
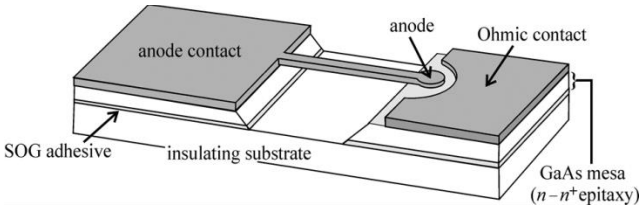


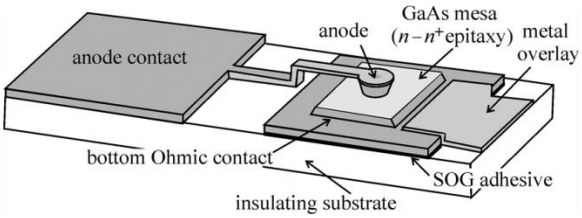
Figure 4.9: Darmstadt's flip-chip quasi vertical diode fabrication steps (a) ohmic contact formation, (b) Schottky contact creation, (c) finished flip-chip device.

In contrast, the quasi-vertical diode geometry presented in this work consists of a thin (1 μm or less) GaAs mesa that has been wafer-bonded to a host high-resistivity silicon substrate. The diode ohmic contact is formed prior to transfer of the epitaxy to the host silicon, and GaAs is not relied upon for structural integrity, resulting in a vertical diode supported by a mechanically-robust substrate.

Figure 4.10 illustrates the differences in geometry between the planar and quasi-vertical diode presented here. Both diode topologies make use of a finger airbridge contact to the anode. The ohmic contact for the quasi-vertical device, however, is formed on the back of a GaAs mesa, lies directly below the anode, and extends beyond the perimeter of the mesa. This arrangement permits electrical connection to the ohmic contact using a metal overlay rather than vias. Figure 4.11(a) details the diode geometry, showing an SEM of the anode contact region including the GaAs mesa, underlying ohmic contact, metal overlay and finger bridging the anode. Through post-processing of the silicon host substrate, diodes integrated onto silicon membranes, as thin as a few microns, with integrated beamleads for chip support and electrical connection can be readily created, as shown in Figure 4.11(b).

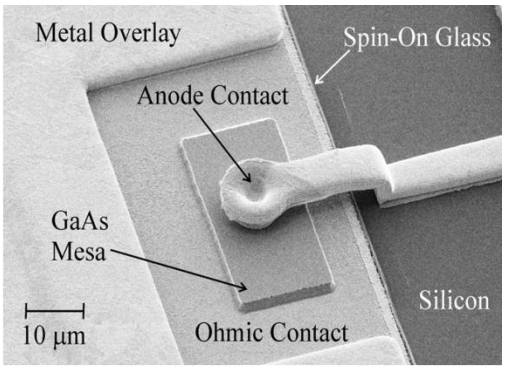


(a)

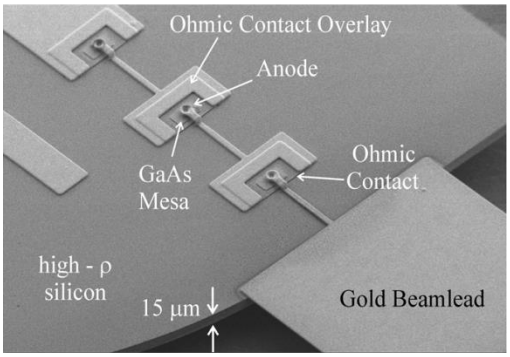


(b)

Figure 4.10: Diagrams showing the geometry of (a) a laterally-oriented planar diode and (b) a quasi-vertical diode integrated into a planar circuit



(a)



(b)

Figure 4.11: Scanning electron micrographs of the diodes studied in this work. (a) Image of the quasi-vertical diode showing the anode contact. (b) Image of a quasi-vertical diode array fabricated on a 15 μm thick high-resistivity silicon carrier with beamleads.

4.3 Prototypes for RF Characterization of Quasi-Vertical Diode

Quasi-vertical Schottky diodes based on the geometry of Figure 4.10(b), with 3, 2.4 and 1.8 μm diameter anodes were fabricated for characterization between 325-500 GHz, 500-750 GHz and 750-1100 GHz bands using the on-wafer measurement method described in Chapter 3. The test structures consisted of a single diode at the end of a coplanar waveguide (CPW) feed (Figure 4.12), as well as diodes with shunt tuning stubs (Figure 4.13). Both structures can be characterized by measuring their reflection coefficient using a one port on-wafer probe station.

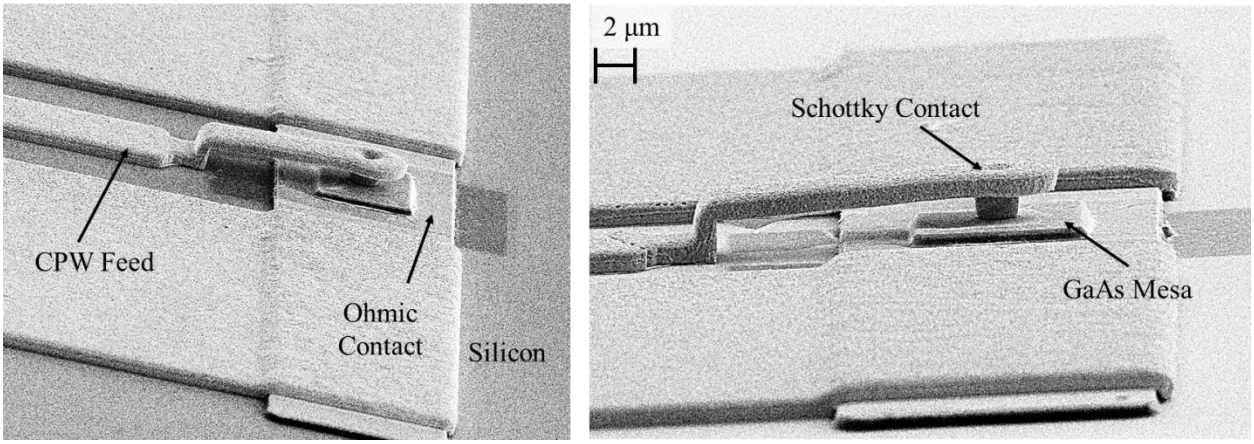


Figure 4.12: Single diode with coplanar waveguide (CPW) feed

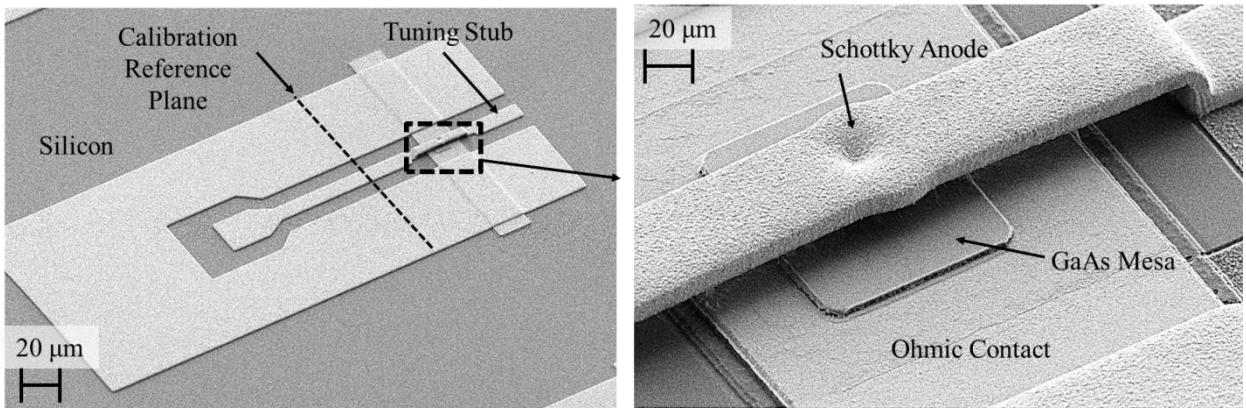


Figure 4.13: Diode with tuning stub

The design process for the above structures was iterative and used Ansoft's *High Frequency Structure Simulator* (*HFSS*) and Agilent's *Advanced Design System* (*ADS*). *HFSS* was used to determine

the scattering parameters (*s*-parameters) of the diode geometry, including the finger contact, as described in Chapter 2. These *s*-parameters were imported to *ADS* to model the performance of the diode with and without the open stub tuning element seen in Figure 4.13. The structures with an open stub were designed to produce a 180° phase shift of the reflection coefficient. When used as a phase-shifter, a varactor's capacitance-voltage dependence is exploited to modulate the phase of a reflected signal using an applied bias. For these circuits, the length of the tuning stub is varied to allow a 180° phase shift for a -6V to 0.5V diode bias tuning range at band center (Figure 4.14).

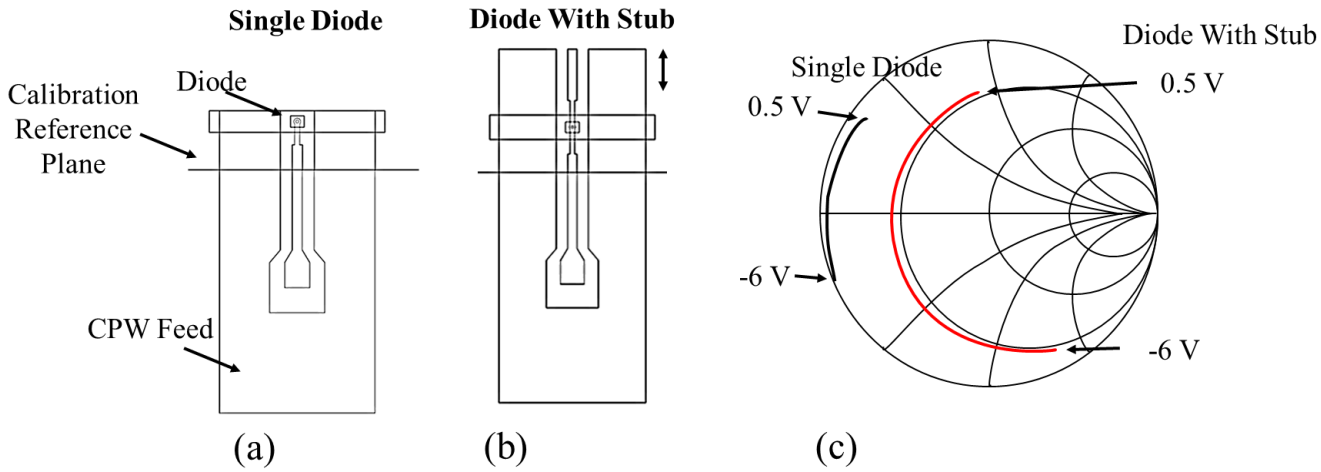


Figure 4.14: Single diode (a) without and (b) with stub and (c) Smith chart phase shift s-parameter data versus applied bias for the two structures

4.4 Diode Fabrication

This section gives an overview of the quasi-vertical diode fabrication process. Fabrication of the quasi-vertical diode starts with an epitaxial stack-up of GaAs (*n*+/*n*) and AlGaAs on semi-insulating GaAs, as shown in Figure 4.15(a). For this work, a 650 μm semi-insulating substrate with 2 μm AlGaAs, 200 nm *n*-GaAs (3×10^{17} cm^{-3}), and 1 μm *n*+-GaAs (5×10^{18} cm^{-3}) epitaxial layers was used. Lithography on the top n+ layer defines the ohmic contact regions which are formed from evaporated Ge/Pd/Au (30/40/50 nm) that are alloyed at 335°C for 90 seconds and electroplated with 400 nm of gold. Measurements performed using ohmic contact transmission line structures formed near the wafer perimeter give a specific contact resistance of 5×10^{-7} Ω-cm for these devices.

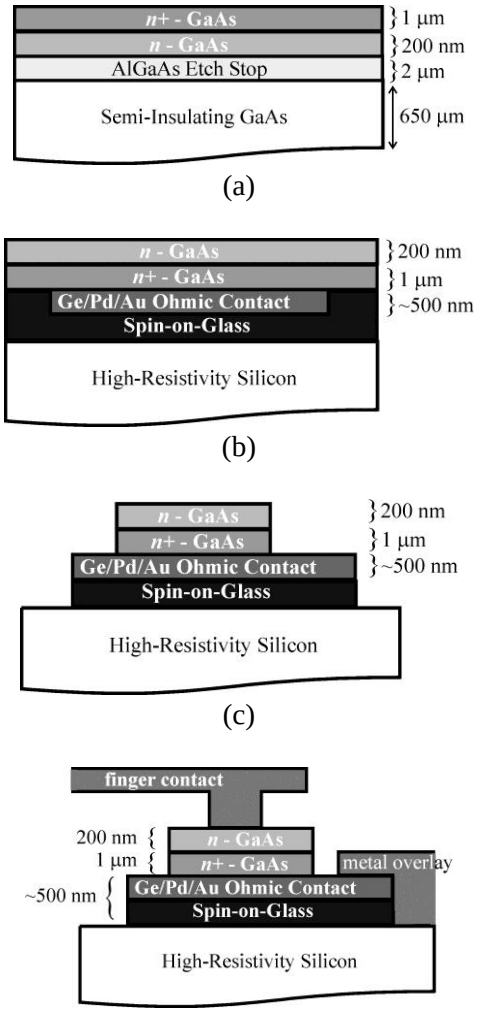


Figure 4.15: Outline of the quasi-vertical diode fabrication process: (a) GaAs epitaxy, (b) wafer bonding to silicon substrate, (c) mesa etch, and (d) final anode and cathode contact formation. Note the epitaxial layers shown in the figure are not to scale.

After formation of the ohmic contacts, the GaAs wafer is bonded, ohmic-contact-side-down, to a high-resistivity silicon wafer ($\rho > 10$ kΩ-cm) using spin-on-glass (Filmtronics FG65) applied at 3000 rpm for 30 seconds to yield an adhesive layer approximately 500 nm thick (Figure 4.15(b)). The bonding process involves mounting the GaAs and silicon substrates in a bonding press, pulling a vacuum in the chamber and bringing the substrates into contact. The press is then heated to 180°C before cooling to room temperature, permanently joining the two wafers.

Once bonded to the silicon substrate, the semi-insulating GaAs is removed in citric acid and the 2

μm thick AlGaAs etch stop is removed in hydrofluoric acid, leaving an *n*-*n*+-ohmic metal stack-up on silicon. The final device mesas are defined lithographically and all unneeded GaAs is removed with a second citric acid etch. Finally, residual spin-on-glass remaining on the exposed substrate is removed using reactive ion etching (Figure 4.15(c)).

The final step in the process is formation of the anode, finger contact, ohmic contact overlay metallization, and other circuit features on the silicon surface. To define the diode finger and other circuit features on the silicon surface, a sacrificial photoresist layer is patterned and titanium and gold (7/22 nm) are sputtered over this layer. A second layer of photoresist is spun over the sacrificial resist layer and patterned, and the areas of interest are then plated through this second photoresist mask. The Ti/Au seed layer and sacrificial resist are then removed as final step, leaving the finished device (Figure 4.15(d)). A process sheet documenting the fabrication steps for the diode is provided in Appendix D.

4.5 DC Characterization

Current-voltage characterization of the quasi-vertical diodes was done with a Keithley 236 Source-Measure Unit using the four point probe method. A typical DC characteristic (logarithmic scale) for a 3 μm diode is shown in Figure 4.16. Because the diode anode and cathode contact pads lie directly on high-resistivity (ρ >10 kΩ-cm) silicon, the substrate contributes a large shunt leakage resistance to the diode. Figure 4.16 also shows the logarithmic current-voltage characteristic for the diode pads on silicon alone, *without* the diode present (dotted line). Fitting a linear current-voltage characteristic to this measurement yields a substrate leakage resistance for the diodes of approximately 100 kΩ, which is largely insignificant compared to the diode impedance at millimeter and submillimeter-wave frequencies.

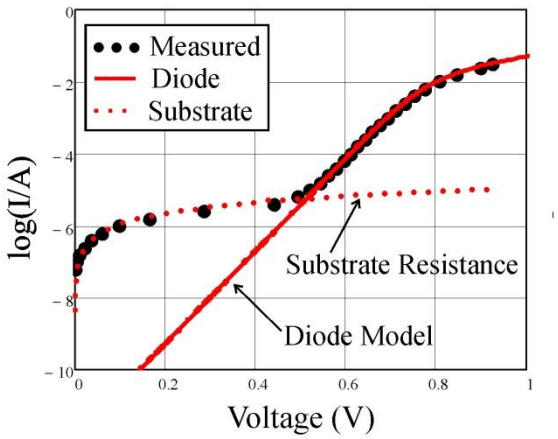


Figure 4.16: Measured current-voltage characteristic of a quasi-vertical diode with 3 μm diameter anode (dots), current-voltage characteristic of the contact pads without diode (dotted) and fitted current-voltage curve from the diode equation (solid).

Estimation of the diode reverse saturation current, ideality factor and series resistance can be found by performing a best-fit to the I-V curve in forward bias (applied voltage greater than 0.5 V), as shown in Figure 4.16. From this fit, the DC parameters for the nominal 3 μm diameter diodes are found to be I_{sat} of 1.4 pA, ideality factor (η) of 1.35, and R_s of 3.7 Ω, which is approximately 30% lower than comparable planar diodes reported in the literature [69]. The measured DC parameters for the diodes of all three anode sizes are given in Table 4.2.

Anode diameter (nominal), μm	Ideality factor	Resistance (Ω)	Saturation Current (pA)
3.0	1.35	3.7	1.4
2.4	1.28	4.5	0.4
1.8	1.25	6.0	0.1

Table 4.2: Measured DC parameters of quasi-vertical diodes

As discussed in [76], the thickness of the highly-doped buffer layer has significant effect on the series resistance of vertical diodes. While current spreading through the buffer layer contributes to resistive loss in the diode, some spreading is necessary to reduce the resistance associated with the ohmic contact, particularly for devices with high specific contact resistance [76]. Consequently, a series of experiments were carried out with the quasi-vertical diode to evaluate the effect of buffer layer thickness on measured series resistance. In these experiments, the nominal 1 μm *n*+ buffer layer of the device was

thinned using a brief etch prior to ohmic contact formation. Thickness of the buffer layer was measured using a Tencor AS-200 surface profiler. The remainder of the diode fabrication process was unchanged, resulting in a set of 1.8 μm and 3.0 μm diameter diodes with differing buffer layer thicknesses. For comparison, the vertical diode series resistance was calculated using the numerical simulation approach of Siedel [77], as shown in Figure 4.17. Siedel's method assumes a cylindrical diode chip geometry, with a Schottky contact centered on the top and ohmic contact on the bottom surface. This simplifies the finite difference calculations of the electromagnetic fields inside the *n*+-GaAs epitaxial layer. The *n*-GaAs epilayer is assumed to be very thin and does not contribute to the substrate resistance. Furthermore, the metal contacts are approximated to be perfect conductors with zero tangential fields at these surfaces. Although there is some uncertainty in the true anode size and buffer layer thickness, the data of Figure 4.17 show the expected trend of increasing series resistance as the buffer layer thickness is thinned much below 1 μm.

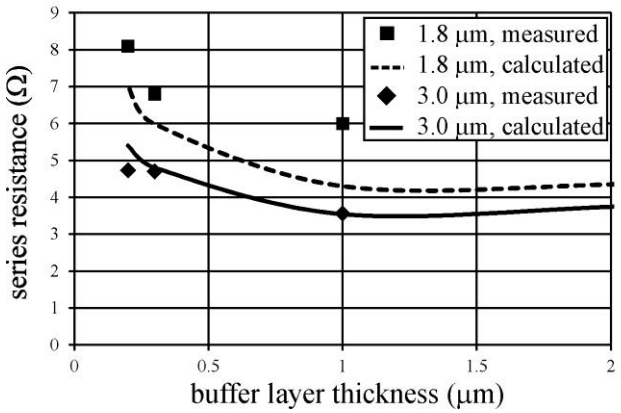


Figure 4.17: Measured and modeled series resistance of vertical diodes as a function of anode diameter and buffer layer (n+) thickness.

4.6 On-Wafer Characterization at Submillimeter Wavelengths

Measurement of the quasi-vertical diode capacitance-voltage characteristic using standard low-frequency techniques is problematic due to the background conduction of the silicon substrate, which tends to dominate the device response in reverse bias. In addition, heating effects can often produce lower-than-

expected series resistance values when found from DC forward-bias measurements. To address these issues, equivalent circuit parameters of the quasi-vertical diode were extracted at low and reverse bias voltages using measurements performed in the 325-750 GHz frequency range, where the substrate conductance is negligible compared to the diode's expected capacitive susceptance. These measurements were performed over two standard waveguide bands, WR-2.2 (WM-570) and WR-1.5 (WM-380), using a Cascade Microtech PA200 probe station equipped with frequency extenders from Virginia Diodes, Inc. and micromachined on-wafer probes developed previously at the University of Virginia [78], [79].

Diode structure incorporating the open tuning stub and data taken between 750-1100 GHz is not used for extracting device circuit models due to the added complexity of the tuning structure and the greater uncertainty observed in the measured data above 750 GHz. The open tuning stub is an additional variable in the circuit matching analysis that is an unnecessary complication when focusing on the development of diode equivalent circuit models. Structures with tuning stubs were fabricated solely to illustrate they could be employed to enhance the phase response of the varactors. Figure 4.18 illustrates that some data points in 750-1100 GHz range lie outside the Smith chart, indicating calibration error. Nevertheless, the data do show the expected change in phase with varactor bias and are the first on-wafer measurement of a diode at 1 THz. Improvements in the infrastructure for metrology at these frequencies as well as better calibration techniques will eventually allow this approach to be a useful tool for device measurement at 1 THz.

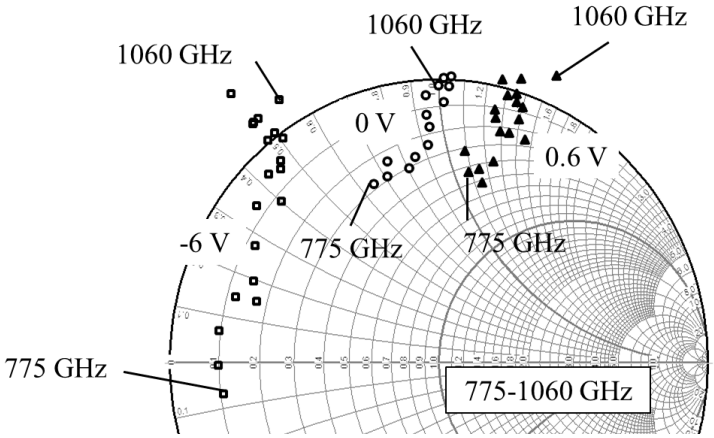


Figure 4.18: s_{11} vs. frequency for 1.8 μm diodes biased at -6 V, 0 V, and 0.6 V

Figure 4.19 shows the geometry and equivalent circuit model for the diodes fabricated for on-wafer characterization. A calibration is first performed using five coplanar offset short-circuit standards fabricated on the same substrate as the diodes. The reference plane for the scattering parameter measurement, noted in Figure 4.19(a), is set 30 μm from the diode finger for the WR-2.2 (325—500 GHz) and 20 μm from the finger for the WR-1.5 (500—750 GHz) measurements.

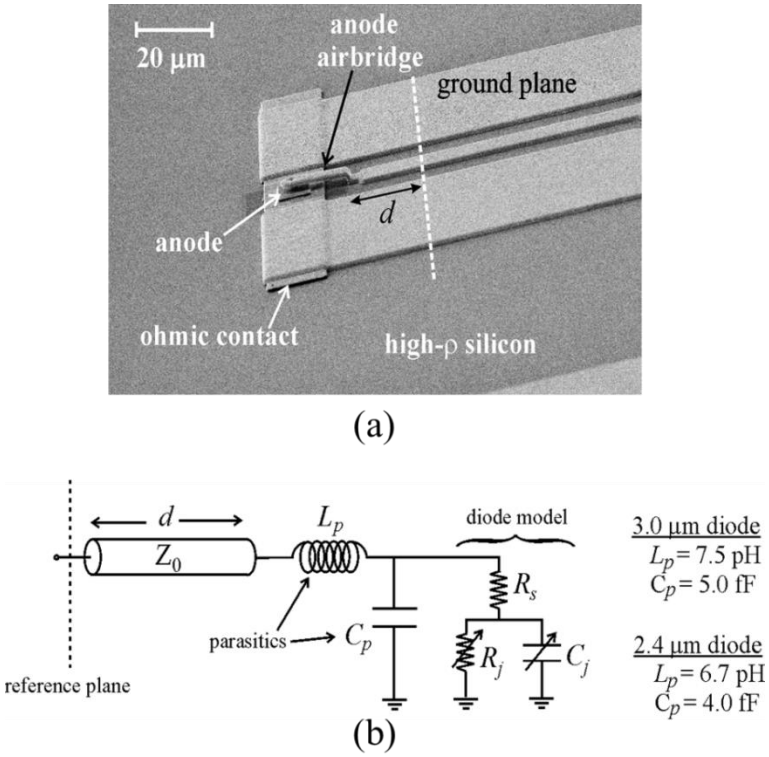


Figure 4.19: (a) SEM image of the quasi-vertical diode. The CPW feedline length (d) is 30 μm for the WR-2.2 measurements and 20 μm for the WR-1.5 measurements. (b) Equivalent circuit model used to represent the vertical diode. Parasitic elements found from *HFSS*.

Parasitics associated with the diode geometry − the short section of coplanar feed transmission line to the finger, the inductance associated with the finger, and the shunt capacitance between the finger and ohmic contact – are found by simulating the device structure in Ansoft's *High Frequency Structure Simulator* (*HFSS*) and fitting to the equivalent circuit model of Figure 4.19(b). The diode series resistance and junction capacitance are subsequently estimated by de-embedding them from the measured *s*-parameters using the parasitic values for the finger inductance and shunt capacitance, as determined by *HFSS*.

Figure 4.20(a) shows the measured reflection coefficient for the 3.0 μm diameter and 2.4 μm diameter diodes at center band as bias voltage is swept from −6 to 0.6 Volts. The larger, 3.0 μm diameter, devices are measured over the 325—500 GHz band with the corresponding data of Figure 4.20(a) taken at 425 GHz. Similarly, the 2.4 μm diameter devices are measured over the 500—750 GHz band with the data of Figure 4.20(a) taken at 550 GHz. The corresponding diode junction capacitance and series resistance, obtained from the *s*-parameter data and circuit model of Figure 4.19(b), are shown in Figure 4.20(b) and Figure 4.20(c).

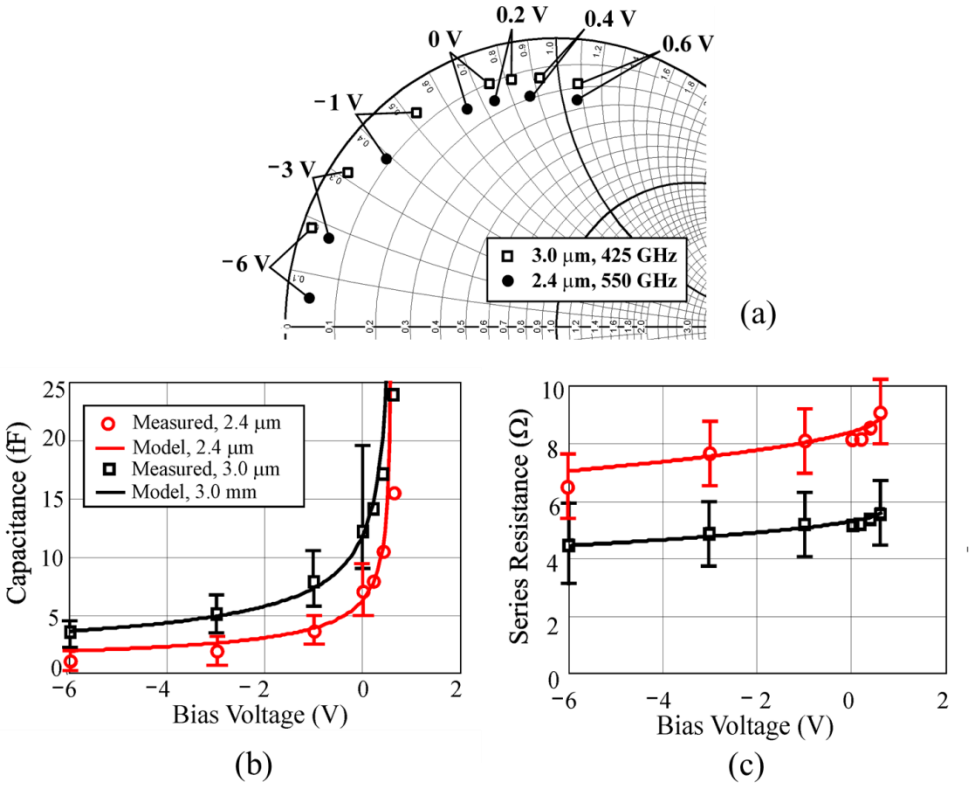


Figure 4.20: (a) s_{11} vs bias voltage for a 3.0 μm diameter and 2.4 μm diameter diode measured at 425 and 550 GHz, respectively. (b) The junction capacitance and (c) series resistance extracted from the s-parameter data and diode circuit model.

A least-squares fit of the well-known capacitance-voltage relation for Schottky diodes, where C_{j0} is the zero-bias junction capacitance and Ψ_{bi} is the built-in potential, is performed using Equation 4.1 for both diodes. This fit yields a C_{j0} of 12.2 fF and 7.0 fF for the 3.0 μm and 2.4 μm diameter diodes, respectively. In both cases the built-in potential, $\Psi_{bi,}$ was found to be 0.68 V.

$$C(V) = \frac{C_{j0}}{\sqrt{1 - V/\Psi_{\mathrm{bi}}}} \tag{4.1}$$

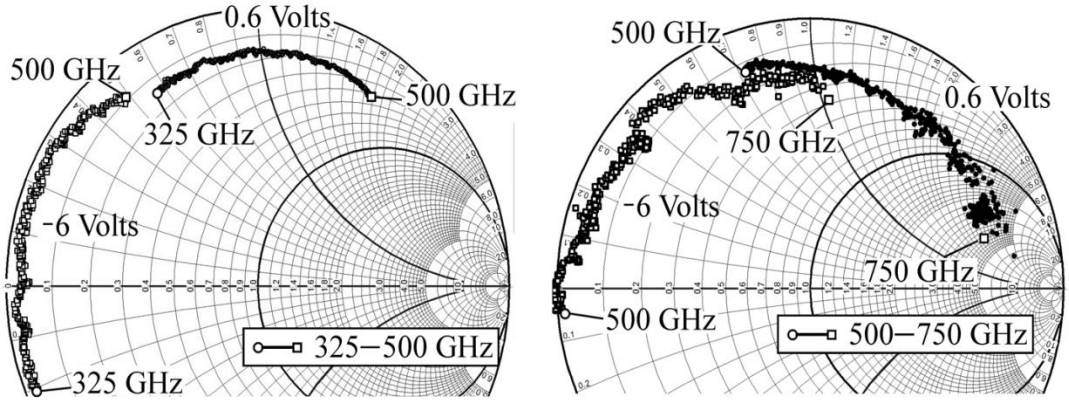
The voltage-dependent series resistance of diodes can be represented by Equation 4.2, where R_1 is the sum of voltage-independent spreading resistance, contact resistance, and zero-bias epilayer resistance. The second term in Equation 4.2 models the modulation of the epilayer resistance, which is a function of depletion layer width. A least-squares fit of Equation 4.2 to the data of Figure 4.20(a) yields R_1 of 5.7 Ω and 9.0 Ω for the 3.0 μm and 2.4 μm diameter diodes, respectively. For both diodes, the built-in potential, Ψ_{bi} was again 0.68 V and the epilayer resistance scaling term (R_2) was found to be 0.5 Ω. Figure 4.20(b) and Figure 4.20(c) show the resulting fit for the junction capacitance and series resistance obtained from Equation 4.1 and 4.2. The series resistance values obtained from these data are somewhat higher, but in reasonable agreement with those found from DC measurements (Figure 4.16 and Figure 4.17).

$$R_s(V) = R_1 - R_2\sqrt{1 - V/\Psi_{\mathrm{bi}}} \tag{4.2}$$

Skating of the on-wafer probes after landing on the coplanar contact pads will result in some uncertainty for the values obtained for the diode circuit parameters. With care, the contact point of the probes can be held to ± 5 μm of the nominal landing point. At 425 GHz and 550 GHz, this variation in offset distance corresponds to ±7° and ±10° of electrical length, respectively. This phase error results in uncertainty of the zero-bias junction capacitance extracted from the *s*-parameter measurements, shown with error bars on Figure 4.20(b). For comparison, the expected zero-bias junction capacitance calculated from the nominal device parameters [80] is 15 fF for the 3 μm device and 9 fF for the 2.4 μm device, which are close to the values extracted from the data of Figure 4.20 and within the uncertainty associated with probe placement. This measurement, in particular, illustrates the sensitivity of device equivalent circuit models derived from scattering parameter measurements at these frequencies and underscores the requirement of micrometer-level precision in probe positioning for on-wafer measurements at submillimeter wavelengths. The series resistance extracted from the scattering parameter measurements is

less sensitive to probe placement, exhibiting an uncertainty of approximately ±1.5 Ω for both the 3 μm and 2.4 μm diameter devices.

The data presented in Figure 4.20 were taken at single frequencies (425 GHz for the 3.0 μm diode and 550 GHz for the 2.4 μm diode). The measured reflection coefficients of the 3 μm and 2.4 μm diodes as a function of frequency, at –6 V and 0.6 V bias, are shown in Figure 4.21. For comparison, the corresponding scattering parameters predicted from the device equivalent circuit model (Figure 4.19(b)) using the best-fit device circuit values are shown in Figure 4.21(c)—(f). The device model of Figure 4.19(b) assumes frequency independent parameters and models the phase response of the diodes reasonably well over the full 325—750 GHz band. The frequency-independent diode model, which is often used in diode circuit design, respectably represents the magnitude response of the diodes within ±0.25 dB measurement uncertainty up to approximately 480 GHz. Beyond this frequency, there is a notable increase in return loss of approximately 6 dB per octave.



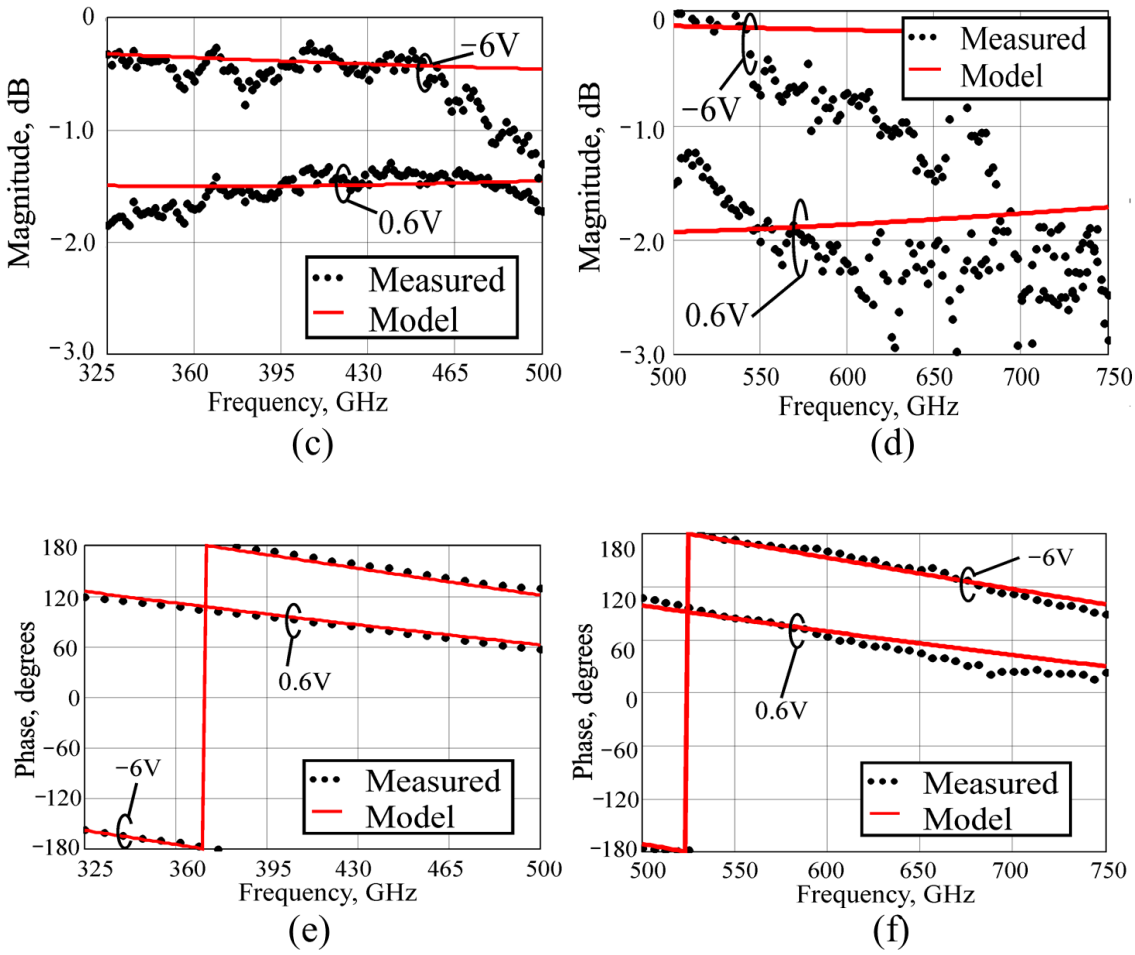


Figure 4.21: s_{11} vs. frequency for 3 μm (a) and 2.4 μm (b) diodes biased at -6 V and 0.6 V. Magnitude and phase of s_{11} for the 3 μm ((c) and (e)) and 2.4 μm ((d) and (f)) diodes compared to the response predicted by the equivalent circuit model (solid lines).

Figure 4.22 shows the zero-bias series resistance and junction capacitance, as a function of voltage for the diodes, extracted from the measured *s*-parameter data and model of Figure 4.19(b), as a function of frequency. The resistance and capacitance of the 3.0 μm diodes do not vary significantly with frequency, consistent with the frequency-independent device model. Data for the 2.4 μm diodes, measured over the WR-1.5 band, however do show a rise in series resistance with frequency and a notable bias-dependent increase in capacitance above 550 GHz.

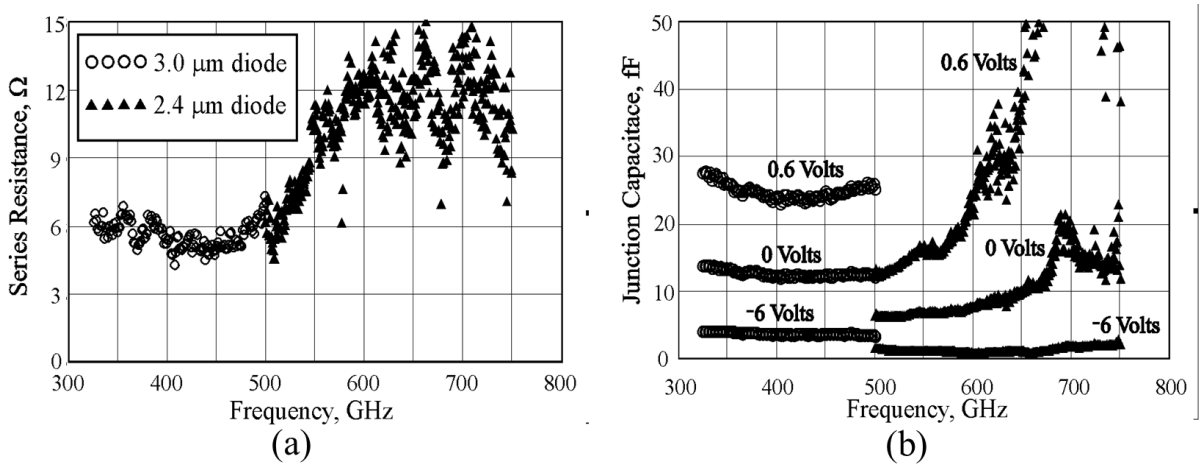


Figure 4.22: Series resistance (a) and junction capacitance v. bias (b) for the 3.0 μm diode (circles, 325—500 GHz) and 2.4 μm diodes (triangles, 500—750 GHz), extracted from the on-wafer scattering parameter data.

It should be noted that the skin depth of the GaAs epitaxy is approximately 1.2 μm at 500 GHz, which is close to the thickness of the diode mesa. Tang has observed that losses in planar diodes due to eddy currents and current crowding effects are anticipated to become more pronounced as the skin depth approaches the diode mesa thickness [81]. This loss is manifested as an increase of series resistance with frequency comparable to that observed in Figure 4.21(b), suggesting that these phenomena may play a role.

To further investigate the loss and behavior of the extracted capacitance observed in the diode measurements at high frequencies, a set of coplanar short-circuited transmission lines with dimensions identical to those used in the diode characterization were fabricated on high-resistivity silicon substrates and measured with the on-wafer probes. The resulting return loss for different lengths and frequency bands is shown in Figure 4.23.

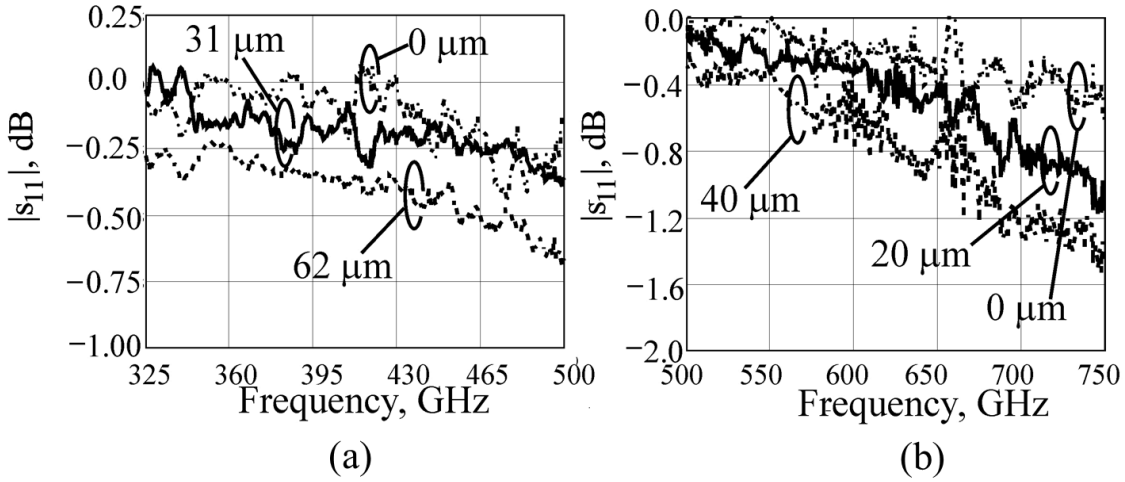


Figure 4.23: Measured insertion loss of coplanar delayed shorts on high-resistivity silicon in the (a) WR-2.2 and (b) WR-1.5 bands. All lines for these measurements had the same cross-section dimensions and nominal characteristic impedance of 50 Ω.

The phase response of the lines (not shown) exhibits the expected linear dependence on frequency and matches the delay predicted using the corresponding offset lengths noted in Figure 4.23. The attenuation of the lines, extracted from the return loss data and given line lengths, is plotted in Figure 4.24. The attenuation, in decibels per dielectric (silicon) wavelength is shown as a function of both frequency and coplanar line width (sum of the center line and gaps) normalized to dielectric wavelength. Because the width of the coplanar lines is an appreciable fraction of a dielectric wavelength, it is anticipated that loss to substrate modes for these structures will become significant near 500 GHz, where the line width is approximately 15% of the dielectric wavelength [82]. The data of Figure 4.23 shows a large increase in loss near 550 GHz, with attenuation near that expected from radiation into a thick substrate [82], supporting the premise that substrate mode excitation and standing waves in the silicon are being observed in the WR-1.5 on-wafer measurements.

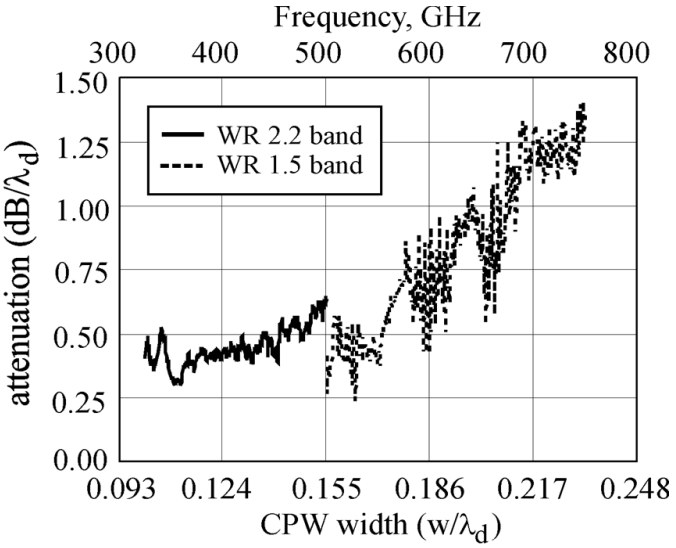


Figure 4.24: Coplanar waveguide attenuation per dielectric wavelength extracted from the data in Figure 4.23(a) (solid) and 4.23(b) (dashed). The horizontal scale is frequency (top) and coplanar waveguide width normalized to dielectric wavelength (bottom).

4.7 Discussion and Summary

The study in [81] as well as the coplanar loss measurements presented in Section 4.6 suggest that both current crowding effects and substrate mode loss are significant effects for the on-wafer measurements in the 500—750 GHz range. The increase in series resistance and sharp bias-dependent peak above 600 GHz in the capacitance measurement of Figure 4.22(b), in particular, are characteristic of radiation loss and standing waves being generated in the substrate. Although on-wafer metrology at terahertz frequencies is a developing field of research and there is clear need for improvements in both calibration and implementation, the data presented in Figure 4.20 to Figure 4.22 illustrate that simple measurement-based device models (such as that shown in Figure 4.19(b)) provide a reasonable approach for representing quasi-vertical diodes for circuit design at millimeter and submillimeter wavelengths. Moreover, the parameters extracted from these measurement-based models are near those expected from fundamental Schottky diode theory (Equation 4.1 and 4.2). It should be noted that extending the lumped-element model of Figure 4.19(b) to account for possible frequency-dependent effects was considered beyond the immediate scope of this work, but will be addressed in future efforts as the metrology infrastructure for such measurements advances and measurement precision is improved.

This chapter has described a new quasi-vertical Schottky diode architecture that is amenable to integration with planar components and circuits. The vertical geometry of the diodes permits engineering of the device to reduce series resistance, which is a primary factor that limits the performance of high-frequency diode-based circuits. The quasi-vertical diodes can be implemented on thin (< 15 μm), mechanically rigid, high-resistivity silicon membranes, allowing them to be used at submillimeter wavelengths where thick support substrates become problematic due to substrate mode loss.

A set of quasi-vertical diodes were fabricated and characterized using both DC and submillimeter-wave on-wafer measurements. The device parameters extracted from these measurements were in reasonable agreement with those expected from basic Schottky barrier diode theory, illustrating the utility of both on-wafer characterization of these devices as well as the applicability of simple lumped-element equivalent circuit models to represent them. Moreover, the measured series resistances of these devices were found to be comparable to or lower than that typically found from planar diodes of commensurable dimensions.

Chapter 5

Quasi-Vertical Schottky Diode Multipliers

This chapter reviews the design and fabrication of a high order GaAs quasi-vertical Schottky diode multiplier used as an application of the new diode structure. Frequency multipliers based on Schottky barrier diodes represent the most commonly-used solid-state device technology for generating power at frequencies ranging from 100 GHz to 1 THz. Over the years, these devices have remained critical to a variety of submillimeter-wave heterodyne-based instruments [83], including radiometers for space-borne applications, receivers for ground-based radio astronomy, and sources for vector network analyzer frequency extenders [84]. The design of varactor multipliers is a well-established topic and the fundamental issues have been understood since the work of Penfield and Rafuse [85]. From this foundation, a number of preferred multiplier circuit topologies have emerged — notably, the balanced doubler [56], [86] and tripler [87], [88], [89], [90] configurations that employ anti-parallel or anti-series connected diodes. These circuit configurations have become commonplace due to their inherent isolation of even and odd-order harmonics, eliminating the need for filters.

Generation of power at frequencies approaching 1 THz typically requires many stages of multiplication as the fundamental input signal is often in the microwave range where significant (watt-level) drive power is achievable. Direct multiplication to a high-order harmonic greater than the third is usually not considered practical as proper idling of all intermediate harmonics is a complex (and sometimes intractable) design problem. Consequently, submillimeter-wave multiplier sources typically consist of a chain of doublers and triplers, selected to yield the desired output frequency. Cascading multipliers is a pragmatic approach, with output powers of hundreds of milliwatts being obtained in the lower portion of the submillimeter band with this technique [91]. However, because the efficiencies for varactor doublers and triplers operating above 100 GHz are typically no greater that 25% [92], the overall

efficiency of a large multi-stage chain is often substantially lower than 1% [93]. Moreover, mismatches between adjacent multipliers in a cascade can readily disturb earlier multiplier stages by pulling them from their optimum operating point through loading effects, further reducing efficiencies and output power. As a result, intermediate matching or isolation networks are frequently inserted between adjacent stages, contributing to loss and system complexity. Moreover, the input stages of large multiplier chains must be capable of handling high power (several watts) to overcome the low efficiencies and yield usable output power, which is often on the order of 1 μW above 1 THz.

This chapter presents a frequency multiplier architecture that is intended to address a number of the issues noted above that frequently plague cascaded multipliers. The circuit topology consists of a pair of balanced frequency doublers that are driven in phase quadrature using hybrid coupler. This approach results, effectively, in a "unilateral" multiplier that presents a match to the input driving source, irrespective of the impedance of the doubler stages. The work presented here applies this architecture to implement an integrated frequency quadrupler with output frequency of 160 GHz using quasi-vertical GaAs varactors fabricated on thin silicon support membranes.

5.1 Quadrupler Architecture and Design

Figure 5.1 illustrates the basic architecture of the quadrupler circuit developed in this work. The input stage of the multiplier consists of a balanced pair of doublers that are driven through a quadrature hybrid, resulting in two outputs that are twice the fundamental input frequency (f_0) and out-of-phase. This circuit topology is widely familiar and often employed for balanced amplifiers and phase-shifters, as any power scattered due to mismatch from the output loads is directed to the isolation port, which serves as power "dump." Consequently, the input source (which may be another multiplier stage in a cascade) is presented with a match over the bandwidth of the hybrid and is not subject to variations in loading and performance due to changes in the operating conditions of the balanced doublers that it drives. The intermediate

outputs at $2f_0$ have the proper phasing to drive a second-stage balanced doubler that bridges the outputs of the two input-stage doublers, thus yielding a frequency quadrupler.

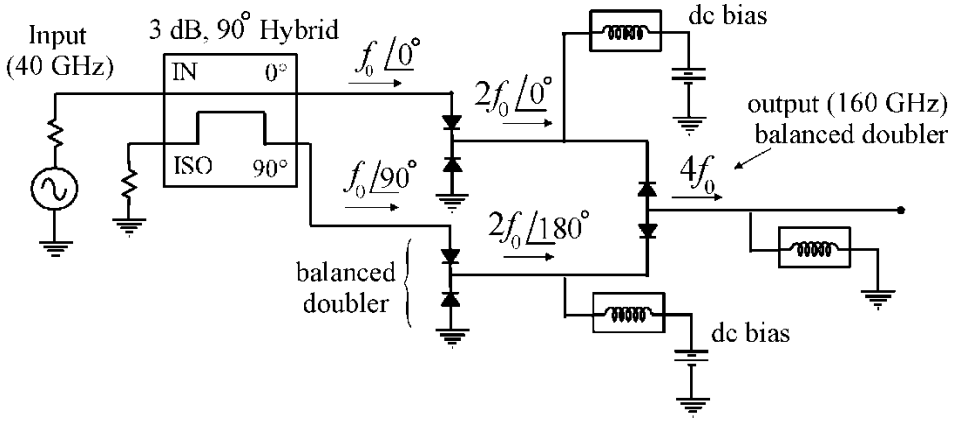


Figure 5.1: Diagram of the fundamental quadrupler circuit architecture.

The use of a balanced circuit architecture to realize "unilateral" multipliers that are insensitive to the loading effects of the output stages appears to have been first proposed by Gewartowski in 1964 [94] who later applied this approach to realize a quadrupler with 2.5 W of output power at 6 GHz [95]. The quadrupler presented here makes use of the same basic approach, but differs from that of Gewartowski as it uses a second-stage balanced doubler at the output to generate the fourth harmonic.

Design of the quadrupler circuit consists essentially of two steps — determining the proper embedding impedances to present to the varactors of the input balanced doubler driven at the fundamental input frequency of f_0 (40 GHz) and, similarly, determining the impedances to present to the diodes of the output doubler stage driven at a frequency of $2f_0$ (80 GHz). Figure 5.2 illustrates the three networks comprising the design: (1) a stepped impedance input matching circuit implemented in (WR-22) waveguide, (2) an intermediate matching/filtering network designed to present the proper load impedance to the input doubler and source impedance to the output doubler at $2f_0$, and (3) a matching circuit that couples the output at $4f_0$ to a waveguide probe in the WR-5.1 band.

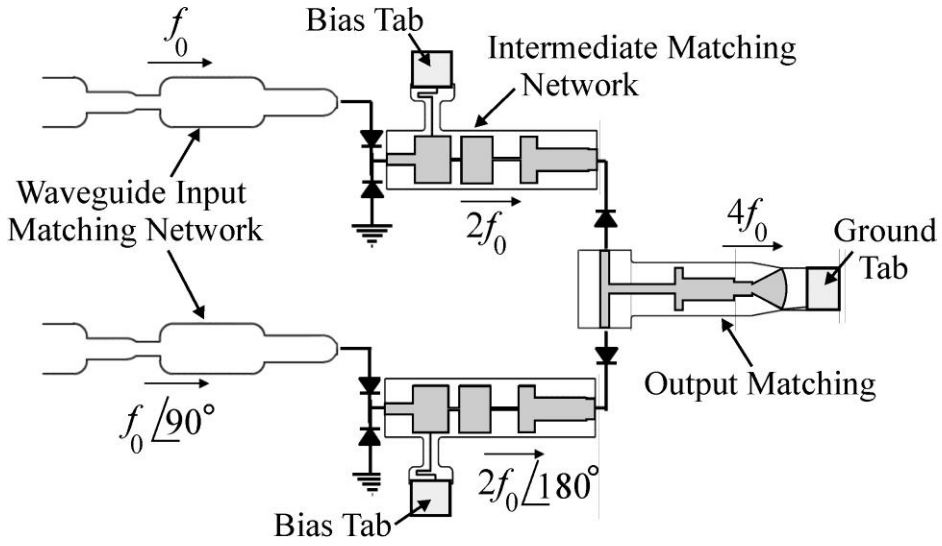


Figure 5.2: Geometry of the quadrupler matching and filtering networks.

The input stage of the quadrupler consists of a pair of identical balanced frequency doublers, driven by the TE_{10} mode of an input WR-22 (33–50 GHz) waveguide. Design of the doubler is based on the method of Porterfield [86] where an array of anti-series oriented varactors extends across a reduced-height waveguide to suppress excitation of the undesired TM_{11} mode, which has a field distribution that can couple to the opposing currents generated by the diodes at the second harmonic. Figure 5.3 shows the details of the waveguide stepped-impedance network and Figure 5.4(a) is a rendering of the top-half of the geometrically-symmetric input stage, detailing the transition from reduced-height waveguide to the diode array and suspended microstrip output circuit.

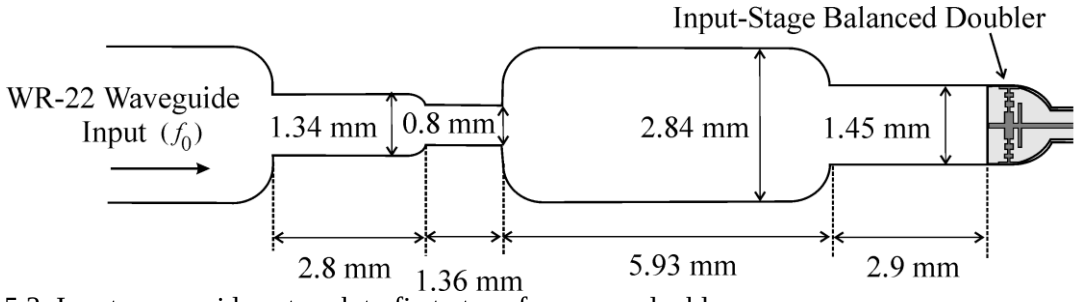
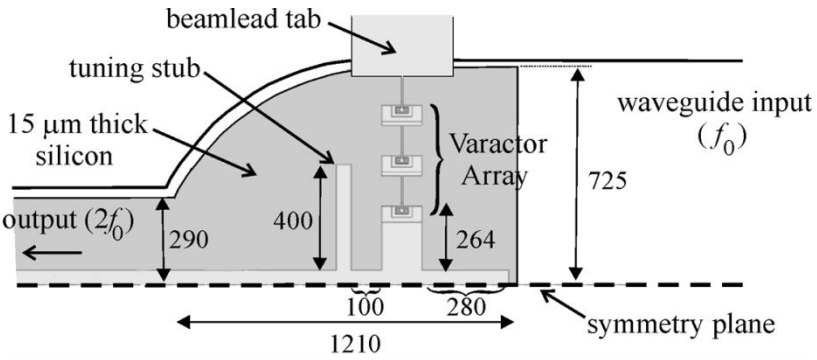


Figure 5.3: Input waveguide network to first-stage frequency doubler.



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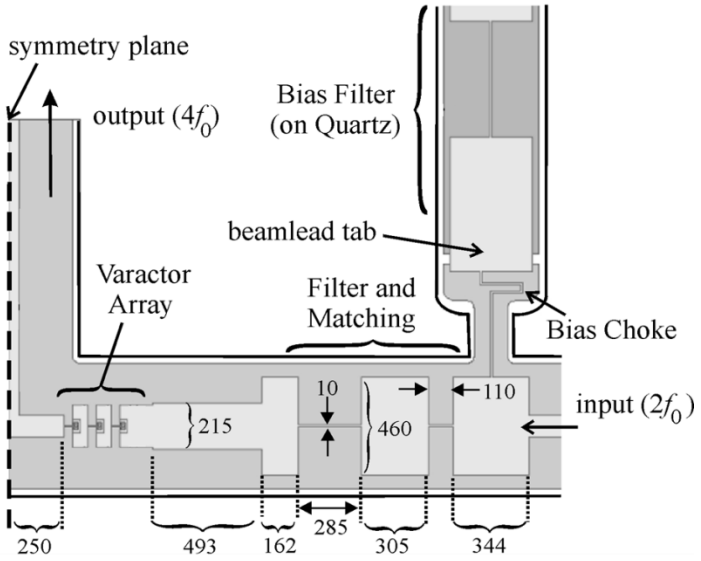

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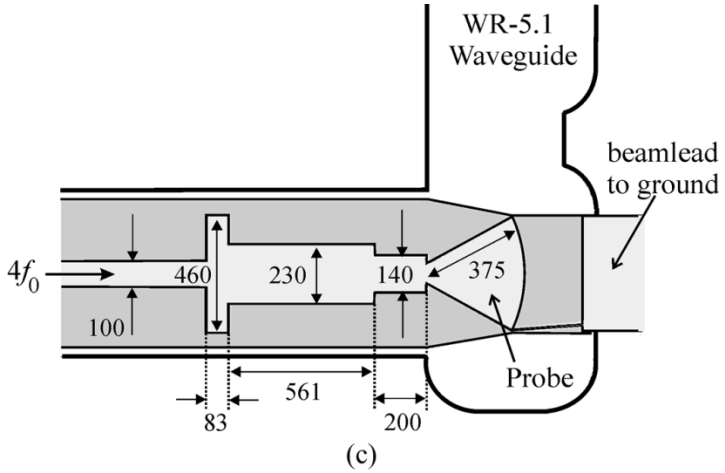


(c)

Figure 5.4: Layout of the three primary sections of the quadrupler: (a) input doubler circuit, (b) output doubler circuit with intermediate matching stage, and (c) output matching circuit and transition to WR-6 waveguide. All dimensions noted have units of μm.

The input frequency and available power determine the varactor anode size, substrate doping, epilayer thickness, and number of diodes required for the doubler [86], as these parameters directly impact the diode series resistance, breakdown voltage, and onset of velocity saturation [96]. Based on the 250 mW WR-22 source readily available in our laboratory, the GaAs epitaxy was selected to have an epitaxial modulation (*n*) layer 200 nm thick with doping concentration of 2×10^{17} cm^{-3} and a 1 μm thick highly-doped (5×10^{18} cm^{-3}) *n*+ buffer layer. With an anode diameter of 9.6 μm, these parameters are expected to yield diodes with zero-bias junction capacitance of 107 fF, reverse breakdown of approximately 9.5 V, and velocity saturation current of 460 mA [96], [86]. Current-voltage measurements of test diodes fabricated with the quadrupler circuit yielded a series resistance for these devices of 0.4 Ω.

As the design objective was to maximize quadrupler efficiency, a harmonic balance analysis using Agilent's *Advanced Design System* (*ADS*) was performed with the varactors described above to determine the optimum embedding impedances to present to the diodes in the input-stage doubler. These impedances were found to be 10 + *j*70 Ω for the source impedance at 40 GHz and 20 + *j*35 Ω for the output load at 80 GHz. The stepped-impedance waveguide transformer of Figure 5.3 was designed to present this impedance to each diode of the six-element diode array at 40 GHz. Figure 5.4(a) shows the circuit features of the first-stage doubler geometry which transitions from reduced-height waveguide to suspended enclosed microstrip. The symmetry plane is represented as an electric wall for the input fundamental signal, which is essentially unaffected by the microstrip circuit to the left of the diode array as it lies along a perfectly-conducting boundary. The impedance presented to a diode by the circuit was determined using Ansofts's *High-Frequency Structure Simulator* (*HFSS*) to analyze the structure of Figure 5.4(a). For the output second harmonic, a magnetic wall boundary condition is imposed on the symmetry plane and the output circuit designed accordingly to present an impedance of 20 + j35 Ω to the diode array at 80 GHz. This matching circuit consists of a 74 Ω transmission line section and shunt stub of length 400 μm placed 100 μm from the diode array, as seen in Figure 5.4(a). Figure 5.5(a) shows the impedances presented to a diode in the input and output stage circuits of Figure 5.4(a), as well as the optimum impedances found from harmonic balance.

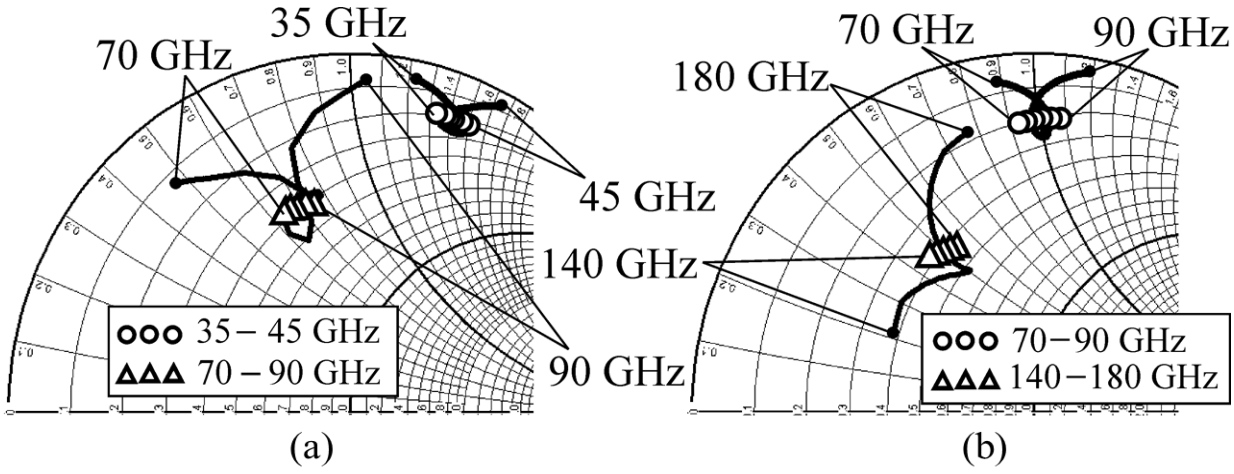


Figure 5.5: Input and output impedance of the (a) input-stage doubler and (b) output-stage doubler. The symbols represent the optimum impedances found from harmonic balance and the solid lines the impedances presented by the matching networks of Figure 5.4.

The geometry of the intermediate section of the multiplier, extending from the output of the first-stage doubler to the input of the second-stage doubler, is shown in Figure 5.4(b). This section includes a lowpass filter for the 80 GHz output of the first-stage doubler followed by a stepped-impedance transformer that presents 10 + *j*50 Ω to the input of the second-stage doubler. Because the outputs of the first-stage doublers are out-of-phase, the symmetry plane of Figure 5.4(b) is an electric boundary for the input at 80 GHz. This virtual electric boundary extends along the quadrupler output circuit, effectively removing its influence on the input at signal at $2f_0$ (80 GHz).

As with the input doubler stage, optimum impedances for the output doubler stage (10 + j50 Ω at 80 GHz and 20 + j25 Ω at 160 GHz) are found using harmonic balance analysis with *ADS*. The varactor diodes for the output stage make use of the same epitaxy as the input doubler, but the anode diameter is scaled to 8 μm to provide a zero-bias junction capacitance of 75 fF. Figure 5.5(b) shows the impedances presented to a diode in the second-stage doubler found from harmonic balance and *HFSS* simulations of the structure in Figure 5.4(b).

The final step of the quadrupler design consists of transforming the output impedance of the second-stage doubler to the TE_{10} mode of the output waveguide, thus maximizing power coupled to the output WR-5.1 waveguide at 160 GHz. The output matching network (Figure 5.4(c)) consists of a simple

shunt stub and stepped-impedance suspended-microstrip section that transforms the waveguide probe impedance to 20 + j25 Ω to the diodes of the doubler array.

Final design and optimization of the quadrupler is accomplished with a modular approach where the circuit is partitioned into its primary sections, as described above, and each analyzed using *HFSS*. Scattering parameters obtained for the matching networks from *HFSS* are imported into *ADS* to perform harmonic balance analysis and determine the resulting multiplier performance. This process is iterated, adjusting the geometry of the circuit each time, to bring the impedances presented to the varactors close to their optimum values.

Figure 5.6 shows the final geometry of the quadrupler chip resulting from this design process. The chip is a single drop-in unit, approximately 7.5 mm in length, made of 15 μm thick high-resistivity (>10 kΩ-cm) silicon that incorporates three sets of balanced doublers (totaling 18 varactor diodes) with associated matching networks, and includes gold beamlead tabs extending from the chip perimeter to accommodate alignment, mounting and bias connections.

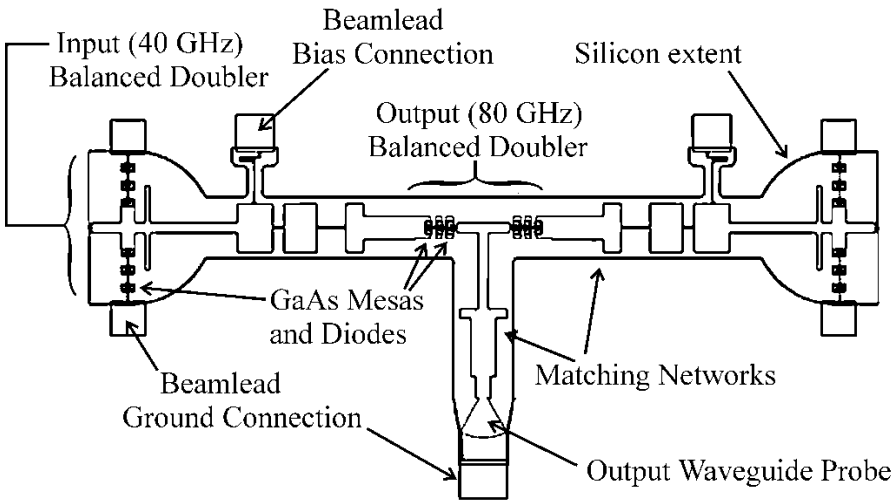
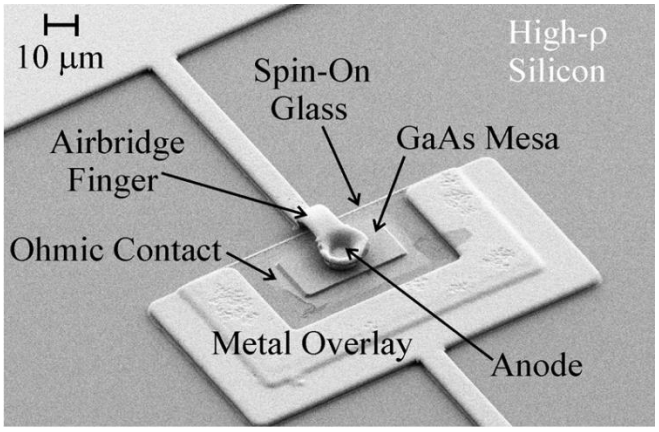


Figure 5.6: Layout of the full integrated quadrupler chip

5.2 Fabrication and Assembly

Fabrication of the multiplier chip shown in Figure 5.6 is based on a quasi-vertical diode process developed at the University of Virginia and detailed in Chapter 4. A key step of the process is transfer of

the GaAs epitaxy to a silicon-on-insulator (SOI) substrate that serves as the final carrier chip for the diodes and their associated circuitry. After initial formation of the device ohmic contacts, the diode epitaxy is bonded, ohmic contact-side-down, to the SOI substrate. Following this step, most of the GaAs is etched from the wafer, leaving only mesas for fabrication of the diodes. The remaining features of the diodes and multiplier circuits (anode, contact finger and cathode metallization) are fabricated using standard lithographic, metal deposition, and etching processes as described in [97]. Figure 5.7(a) is a scanning electron micrograph (SEM) showing the geometry of one of the quasi-vertical diodes of the quadrupler circuit. A view of an integrated multiplier circuit before the final etch that separates individual chips is seen in Figure 5.7(b).



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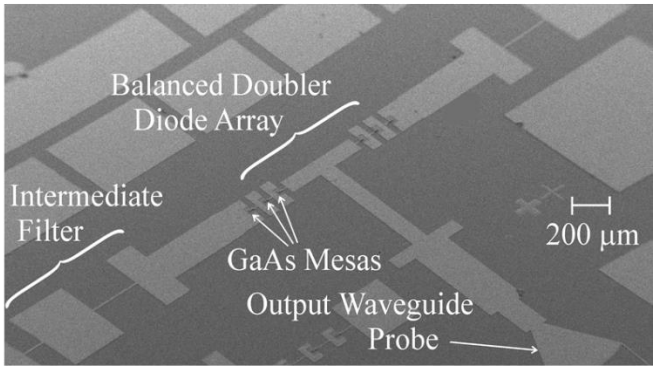


(b)

Figure 5.7: (a) SEM of the quasi-vertical diode showing the geometry near the anode. (b) Image of the completed quadrupler circuits prior to the backside extents etch and chip separation. The image shows the region near the output-stage doubler.

Following the diode processing steps, the wafer is bonded topside-down to a temporary carrier wafer, revealing the backside silicon handle of the SOI. This "handle" silicon is removed through reactive ion etching to the buried oxide layer, which acts as an etch stop. Buffered hydrofluoric (HF) acid is used to etch the oxide, leaving the multiplier circuits on a thin (15 μm), high-resistivity silicon membrane bonded to the carrier. A backside reactive-ion "extents" etch is used to separate the multiplier chips and define their geometry. The final step in the process is removal of the temporary carrier wafer, releasing the individual chips. Figure 5.8 shows a portion of a completed multiplier chip, detailing the input-stage doubler diode array, integrated beamlead tab, and the 15 μm silicon membrane.

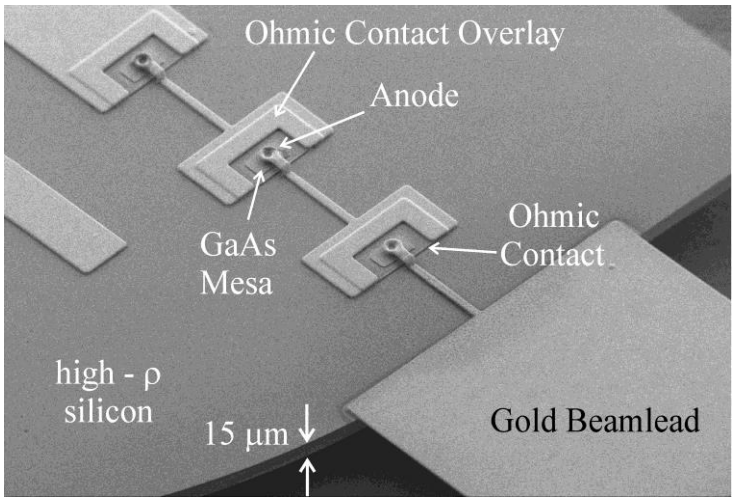


Figure 5.8: SEM of the input doubler diode array and beamlead portion of the chip.

The housing for the quadrupler circuit is fabricated as an E-plane split-block assembly from gold-plated aluminum using standard milling methods. As shown in Figure 5.9, the housing includes a WR-22 3-dB stepped branchline coupler [98] to provide in-phase and quadrature inputs to the quadrupler chip, WR-22 and WR-5.1 waveguide sections, and channels to accommodate quartz-supported filters for bias connections. External bias is supplied to the chip through low-profile GPPO connectors. The WR-22 input and isolation ports of the multiplier are designed to mate with standard UG-383 flanged waveguide and the output (WR-5.1) is a UG-387 interface.

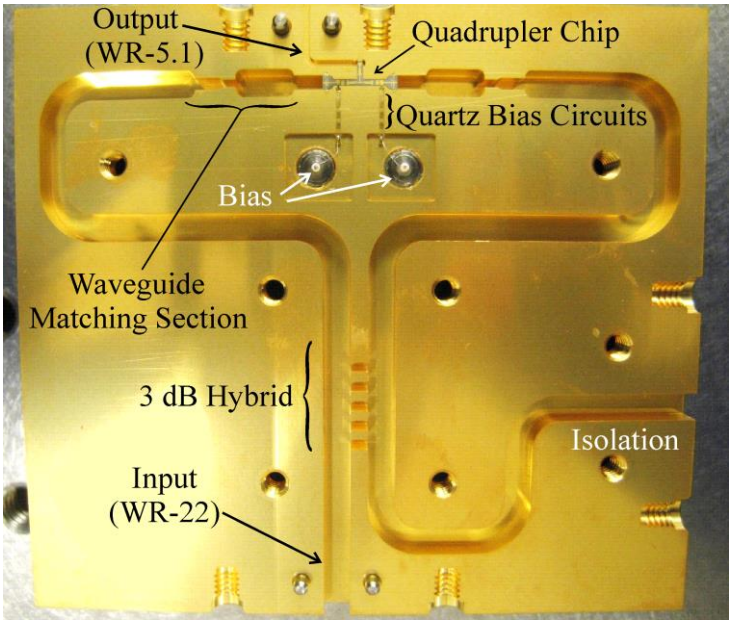


Figure 5.9: Photograph of the quadrupler housing assembly showing the mounted chip and waveguide design features.

Figure 5.10 shows a photograph of the quadrupler chip mounted to the housing. Beamlead tabs protruding from the chip at the two input-stage doublers and WR-5.1 output probe provide grounding and support the circuit as it is clamped in the split-block seam of the housing during assembly. Two additional beamleads protrude from hairpin bias chokes and are bonded to quartz-supported filters to provide DC bias to the diode arrays.

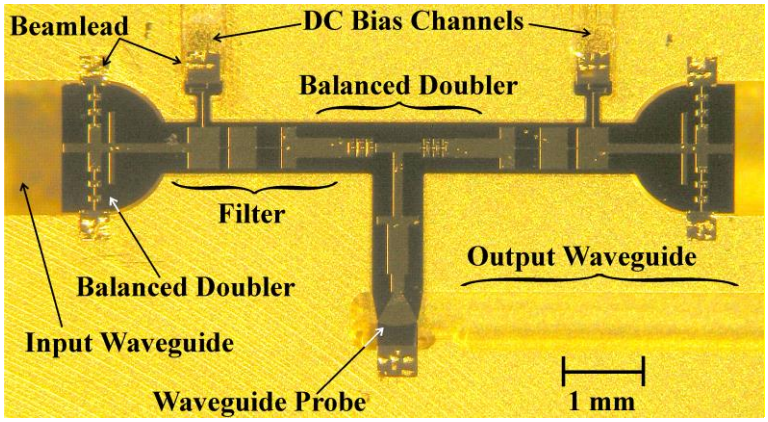


Figure 5.10: Image of the quadrupler chip mounted to the waveguide housing.

5.3 RF Measurements

Characterization of the quadrupler is done using the experimental setup shown in Figure 5.11. The input signal is supplied by an Agilent E8257D frequency synthesizer followed by a Spacek Labs SP408-35-26 amplifier with 35 dB gain, 36 to 43 GHz bandwidth and output power of 26 dBm at the 1 dB compression point. A WR-22 waveguide switch is used to monitor the available power as well as direct the input signal to the multiplier block. An Erickson PM1B power meter is used to measure the multiplier output power in the WR-5.1 band and a spectrum analyzer placed at the quadrupler isolation port monitors power scattered from the input-stage doublers, permitting the return loss of the multiplier to be measured during operation. Measurement of the quadrupler was done at the University of Virginia and repeated at Virginia Diodes, Inc. to ensure consistent results were obtained.

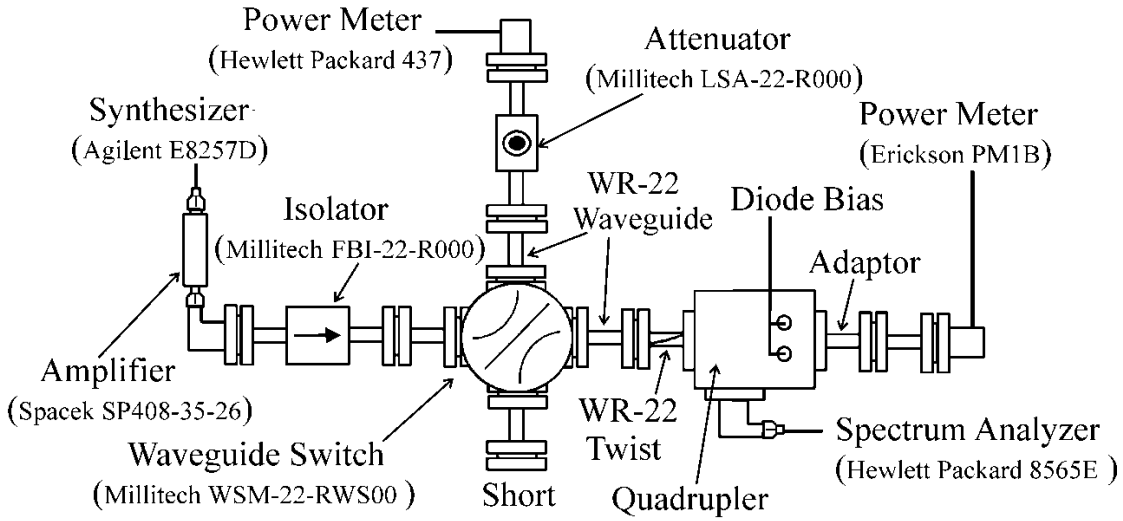
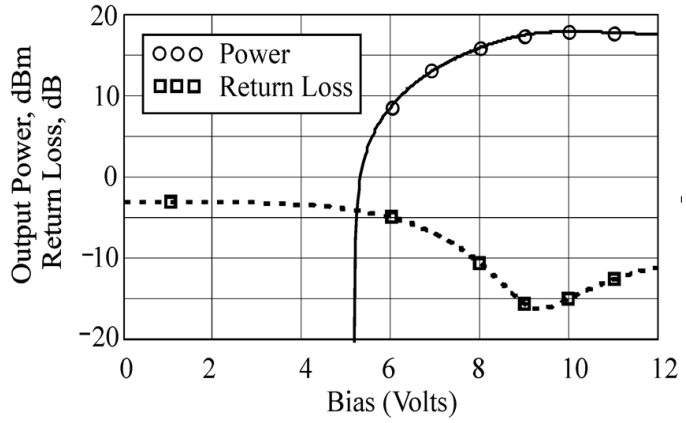


Figure 5.11: Diagram of the quadrupler measurement setup.

Figure 5.12(a) shows the measured output power of the quadrupler at 160 GHz as the (reverse) bias voltage to the diodes is varied. With 220 mW of available power at the input, a peak output power of 62 mW is obtained at a bias of -10 V [99]. Figure 5.12(a) also shows the return loss from the quadrupler, determined from the ratio of power measured at the isolation port to the available power at the input, as bias is varied. Below a bias voltage of -6 V, no output power was measured.



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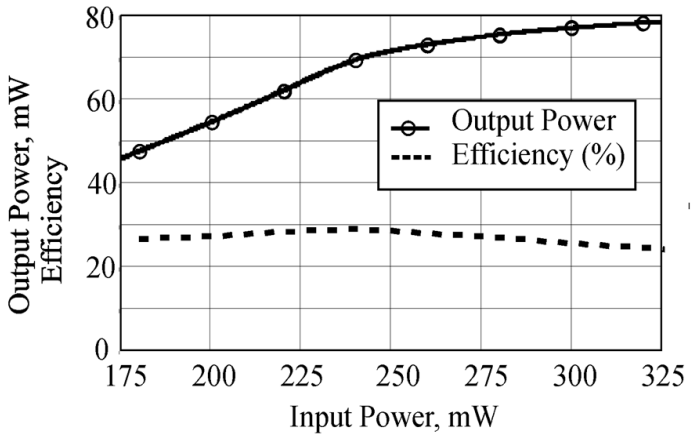

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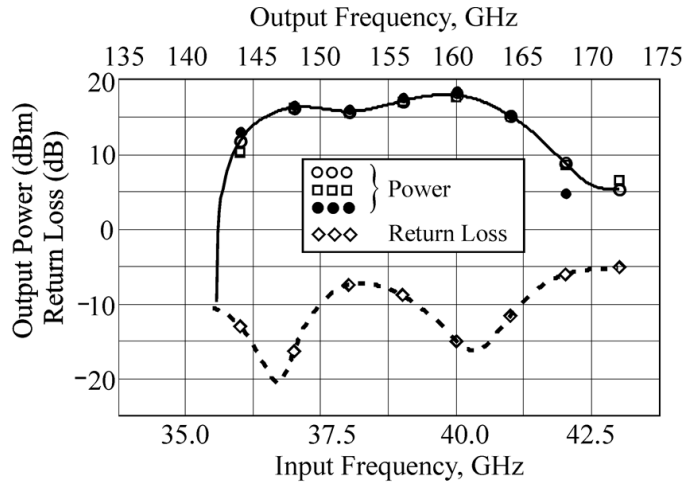

(c)

Figure 5.12: (a) Power and return loss of the quadrupler as a function of bias. (b) Quadrupler output power and efficiency, at a bias of -10 V and input power of 220 mW, as a function of input power. (c) Output power and return loss of the quadrupler.

The quadrupler output power at 160 GHz and bias of -10 V as a function of input power is shown in Figure 5.12(b). Over the 175—325 mW range of input power applied, the quadrupler efficiency remained approximately 25% or better, with a maximum efficiency near 30% at an input power of 240 mW. This is better the than published 10% efficiency for the commercial Q145 quadrupler utilizing two doublers within the same block [100]. At an applied input power of 325 mW, an output of 79 mW was obtained at 160 GHz.

Figure 5.12(c) shows the multiplier output power and return loss over the 142—172 GHz output frequency range, corresponding to the 36—43 GHz bandwidth of the input amplifier. These measurements were performed with 220 mW of input power and a voltage bias of -10 V. The 3 dB output bandwidth of the quadrupler is approximately 20 GHz, or 13%. The three sets of power data presented in Figure 5.12(c) correspond to separate assemblies of the quadrupler, each using different chips, illustrating a high degree of repeatability and consistency in performance resulting from the integrated architecture of the multiplier.

5.4 Thermal Characterization

As the input stage of a frequency multiplier chain is usually driven at the highest power levels (ranging from hundreds of milliwatts to several watts), thermal management and power handling often are important design considerations. Carrier velocity saturation will degrade a multiplier's performance at high applied voltages [15] and elevated temperatures increase the reverse saturation current of varactor diodes, contributing additional loss. Excessive heating is a significant issue for GaAs devices operating at submillimeter wavelengths as this material is generally a poor thermal conductor and is often thinned to only a few microns to mitigate excitation of substrate modes [101]. Consequently, researchers have directed significant effort towards improving the thermal grounding of these circuits, including bonding the GaAs-supported multipliers to highly thermal conductive substrates, such as diamond, to more efficiently remove heat [102].

To assess heating of the integrated quadrupler presented in this work, a single prototype input-stage doubler circuit was fabricated using the same diode design and process as described in Section 5.2. This approach was chosen as the input doubler is subjected to the highest power levels in the quadrupler design and use of a single doubler stage (shown in Figure 5.13) simplifies measurement and characterization. The doubler circuit incorporates the same input matching as the quadrupler design with its output coupled to a WR-12 waveguide. Because the quasi-vertical diode design utilized in the multiplier is bonded to silicon (which has thermal conductivity nearly a factor of three higher than GaAs) and the ohmic metal lies approximately 1 μm directly below the anode and GaAs epitaxy, the doubler is anticipated to perform favorably compared to GaAs membrane diodes with respect to heating.

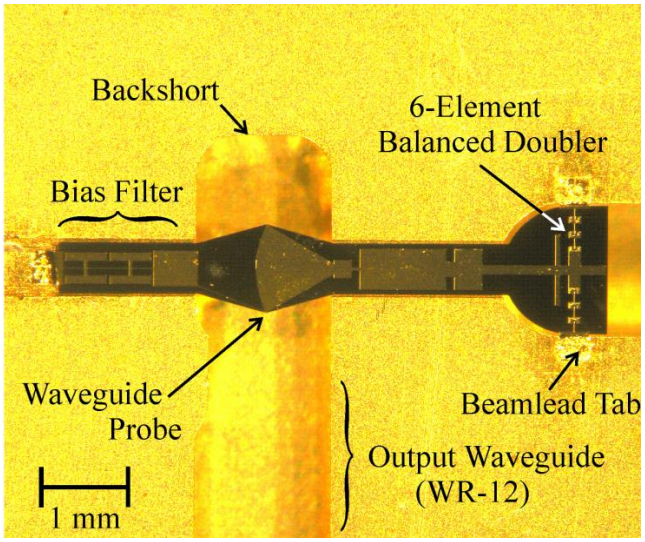

Figure 5.13: Image of frequency doubler integrated on 15 μm silicon for thermal characterization.

The RF performance of the doubler is summarized in Figure 5.14. Measurement of the doubler used the same basic experimental setup as shown in Figure 5.11, with an additional directional coupler placed at the input to monitor reflection from the circuit. A peak doubler efficiency of 62% (conversion gain of -2.2 dB) was achieved at 80 GHz for an input available power of 100 mW and bias of -10 V. The 3 dB bandwidth of the doubler (figure 5.14(b)) is approximately 18% and a maximum output power of 113 mW was achieved at 80 GHz with at input of 380 mW (the upper power limit of the Spacek amplifier). Above 400 mW of applied input power, the voltage swing across the diodes is predicted, from harmonic balance analysis, to exceed the 9.5 V breakdown voltage of the diodes.

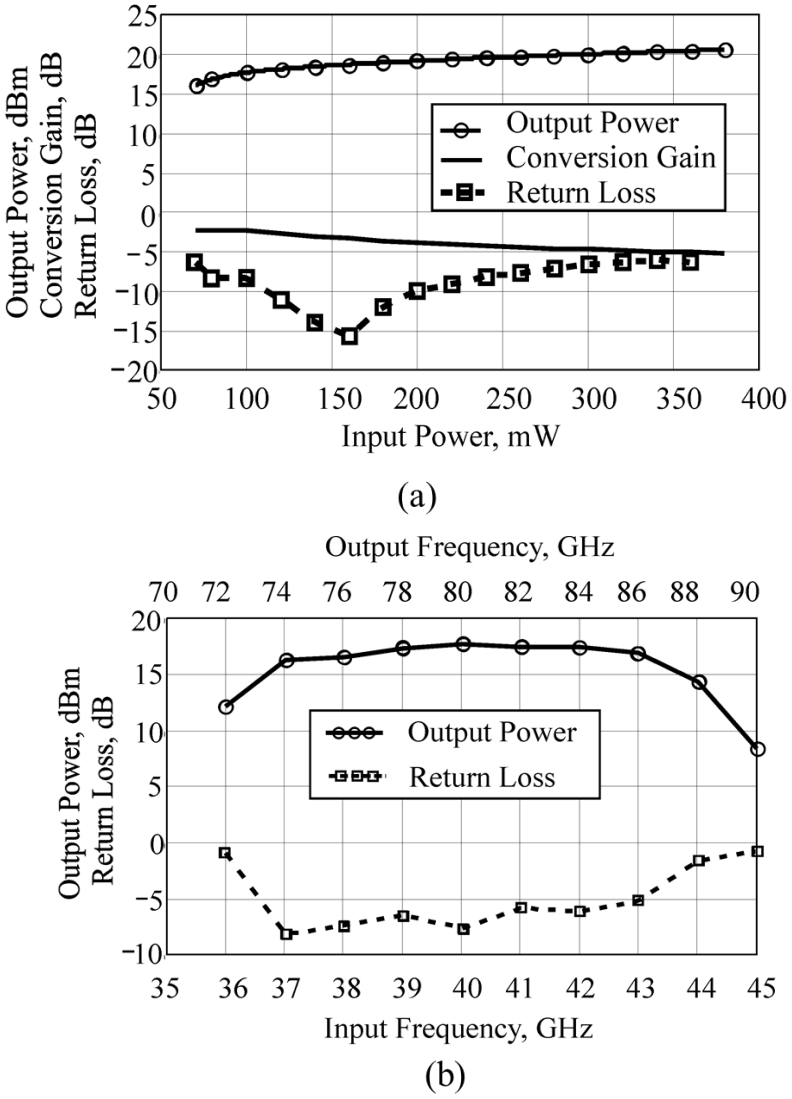

Figure 5.14:(a) Output power, conversion gain, and return loss of the input-stage doubler at input frequency of 40 GHz and bias of -10 V as a function of available input power. (b) Output Power and return loss of the doubler as a function of frequency.

To estimate the operating temperature of the varactors comprising the doubler, the current-voltage characteristic of the diodes was used as an in-situ thermometer. Initially, a set of DC current-voltage measurements of the six-element diode array were taken at temperatures ranging from 25°C to 90°C. These measurements were done with the doubler chip placed on a temperature-controllable hot plate, after the diodes were allowed to reach thermal equilibrium. Data taken from these measurements served as a calibration to permit the temperature of the diodes to be estimated when subjected to RF

power. Figure 5.15(a) shows the change in voltage drop across the diodes found from this measurement, at a fixed current bias of 100 μA and as a function of applied temperature.

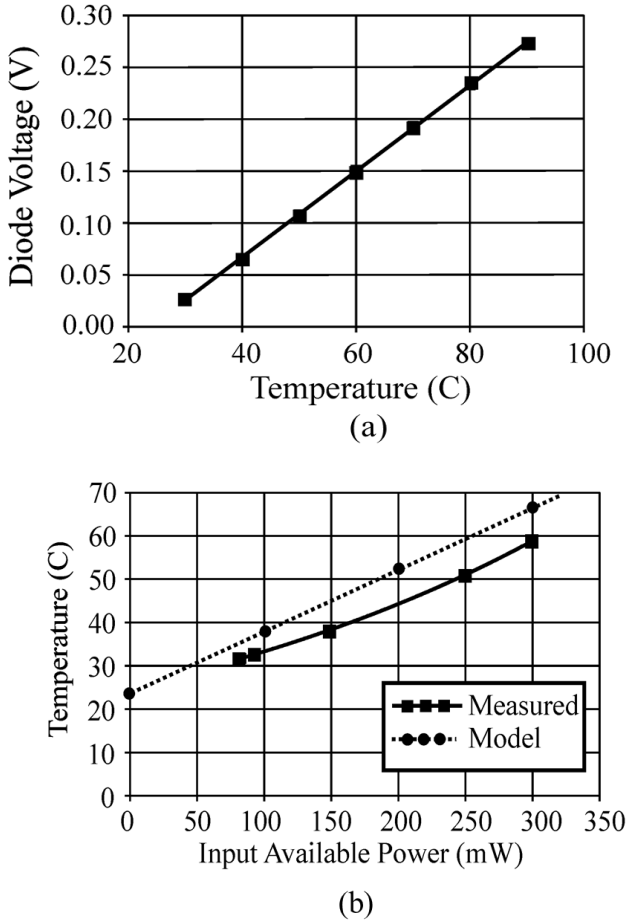

Figure 5.15: (a) Measured change in diode voltage as a function of temperature. (b) Estimated anode temperature of integrated doubler as a function of input power.

The estimated temperature of the diodes in the doubler circuit as a function of available input power at 40 GHz is provided in Figure 5.15(b). For this measurement, which was performed at Virginia Diodes, Inc. using a customized experimental setup, the doubler is pumped with the input RF signal at a fixed power for several seconds. Afterwards, the input power source is removed, a current bias of 100 μA immediately applied, and the diode voltage sampled and monitored over a time interval of 50 ms. Using the measured voltages, extrapolating, and applying the calibration data of Figure 5.15(a) allows the temperature of the varactors to be estimated. Although this method cannot give temperature estimates for

the individual diodes in the array, it does provide a measure of the approximate temperature rise of the devices when subjected to high input power levels. When driven at 100 mW for peak efficiency, the temperature of the varactors is estimated from these measurements to be 35°C, approximately 30°C lower than that calculated for the substrateless 100—200 GHz doubler and over 100 C cooler than the GaAs membrane multiplier investigated in [101], for the same input power.

To assess the reasonableness of the temperature estimations described above, thermal analysis of the doubler structure was performed with the Dassault Systèmes *Solidworks* finite element simulator. For this analysis, each of the six anodes is assumed to dissipate 8 mW of power, which accounts for 100 mW of incident power and a doubler efficiency of 50%. The thermal conductivities of the materials comprising the doubler in the *Solidworks* analysis were 56 W/m-deg for GaAs, 150 W/m-deg for silicon, and 0.6 W/m-deg for the spin-on glass used to bond the GaAs epitaxy to silicon (based on manufacturer's data). With the waveguide block acting as a heat sink at 23°C, simulation gives an anode temperature of 38°C (Figure 5.16), in respectable agreement with the temperature estimated from measurement. Figure 5.15(b) compares the results of the *Solidworks* simulation with measurement and suggest that the experimental approach likely underestimates the operating temperature of the varactors by a few degrees. It should be added that the peak efficiency of the integrated multiplier presented in this work (60%) is a factor approximately 2.5 times larger than the multipliers presented in [101], and this high efficiency clearly impacts heat dissipation and temperature rise in the devices. The maximum input drive level tested for the circuit was 300 mW, which yielded an estimated diode temperature near 60°C.

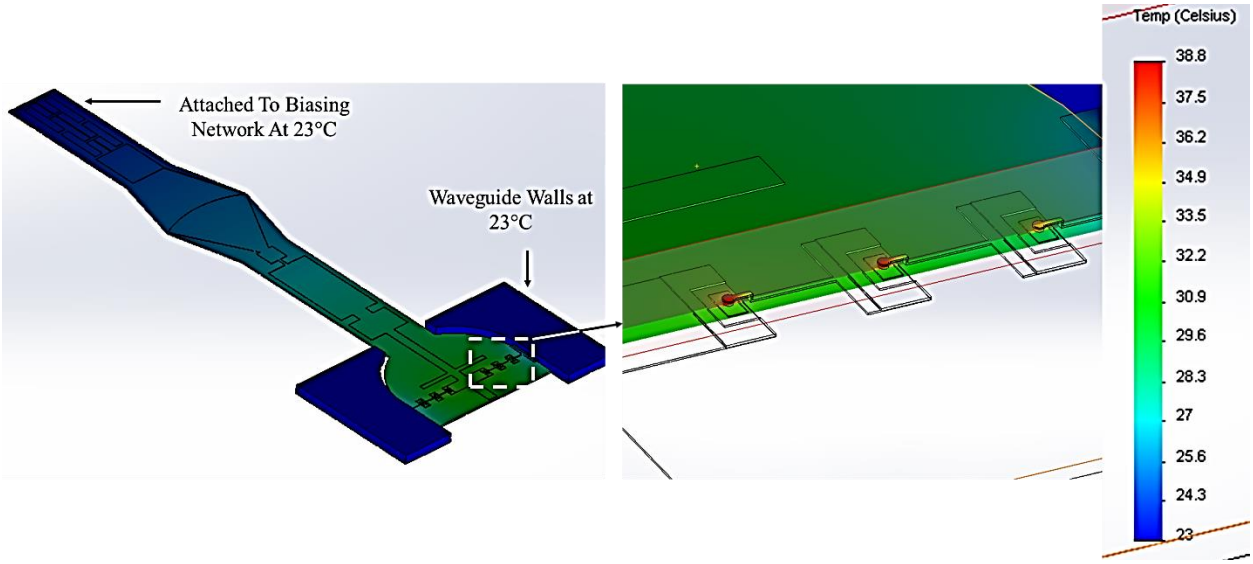

Figure 5.16: *Solidworks* simulated temperature for 50% efficiency at 100 mW input power (8.33 mW dissipated per anode).

5.5 Summary

The multiplier described in this work, is the first integrated quadrupler demonstrated above 100 GHz. The balanced circuit architecture of the quadrupler addresses a number of challenges inherent in multiplier design, namely degradation in performance due to mismatch between adjacent stages in a chain and improved power-handling. Several assemblies of the multiplier were characterized using different quadrupler chips, each giving consistent results and illustrating the high degree of reproducibility achievable using a fully-integrated design. The quadrupler yielded a peak efficiency at 160 GHz of 29% with output power of 70 mW.

A unique quasi-vertical GaAs diode was developed and employed to realize the quadrupler. Among the primary features of these devices are their vertical geometry with ohmic contact that underlies the GaAs epitaxy and anode. This structure brings the anode into close proximity with the ohmic metal and can be tailored to reduce device series resistance and improve heat-sinking. Moreover, the diode epitaxy is transferred to high-resistivity silicon that is subsequently micromachined to form a thin (15 μm) fully integrated drop-in module with beamleads for electrical connection, alignment, and mounting.

Estimates of the anode temperature for the input-stage doubler of the quadrupler were made using the varactors as integrated thermometers. These measurements determined the operating temperature of the multiplier to be substantially lower than for comparable circuits based on GaAs membrane diodes.

High power submillimeter wave circuits using GaAs diodes would benefit from the quasi-vertical diode geometry integrated on silicon membranes due to the lower diode series resistance, higher device efficiency and better heat dissipation. The cost of using this technology is the added complexity of the substrate replacement process and the larger on-wafer device size. Nevertheless, device efficiency is critical for high power multipliers since any input power not reflected or converted into the desired harmonic is dissipated in the diode. This necessitates more thermally conductive substrates such as AlN or diamond which are difficult to process. The high efficiency quasi-vertical diodes could also be fabricated on a diamond substrate, and would output more power than the equivalent low efficiency planar diode designs that must be driven harder and would have a higher chance of failure.

Chapter 6

Conclusions and Future Work

The focus of this thesis has been the integration of GaAs Schottky diodes on silicon-on-insulator (SOI) substrates for better control of the device parasitics and ease of assembly through higher level integration. An initial proof-of-concept 200 GHz phase-shifter on 15 μm high-resistivity silicon illustrated the concept and revealed a number of issues associated with the initial fabrication process, including limitations with the planar diode design. A quasi-vertical diode geometry was therefore developed for integration on SOI. This structure replaces the silicon oxide used for defining the diode anode with photoresist, removes the spin-on-glass used for epitaxial bonding from everywhere except from the ohmic contact areas, and brings the ohmic contact and the Schottky anode in close proximity to reduce the diode's series resistance. The quasi-vertical diode allows for the creation of a fully integrated circuit such as the 40/80 GHz doubler and a 40/160 GHz quadruplers presented in Chapter 5. The new and important contributions of this work to GaAs Schottky diode technology for terahertz metrology include:

- The first heterogeneous integration of planar GaAs varactor Schottky phase-shifters on thin silicon substrates. The device geometry is defined through silicon micromachining and integrated gold beamleads allow for DC biasing and attachment of the circuit to the waveguide housing without adhesives.
- The first quasi-vertical diode geometry on high resistivity silicon substrate with measured series resistance in the 3 to 7 Ω for diodes with anode diameter ranging from 3 to 1.8 μm. The series resistance was measured through DC fitting and verified through on-wafer measurements in the 350-1100 GHz range.
- First on-wafer characterization of diodes above 500 GHz.

- The first integrated quadrupler operating in 140-220 GHz frequency range, using a quasi-vertical diode design. This quadrupler incorporated a number of new design features, including a hybrid coupler, which alleviates the input loading of cascaded multiplier stages. The resulting circuit shows the highest reported efficiency for a high order quadrupler.

The primary drawback of the SOI process arising during the multiplier fabrication was chip bowing, as illustrated in Figure 6.1. This is believed to be a result of the spin-on-glass etching process. The bowing in the multiplier chips may cause the diode's embedding impedances to deviate from the simulated values. Clamping regions (Figure 6.2), similar to those fabricated for the on-wafer probe chips, would largely address this issue.

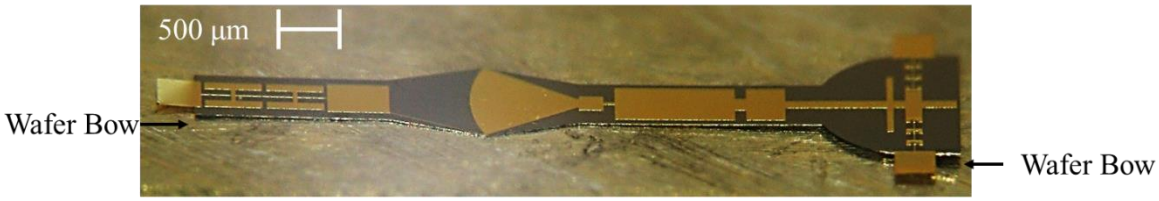

Figure 6.1: Frequency doubler circuit chip wafer bow

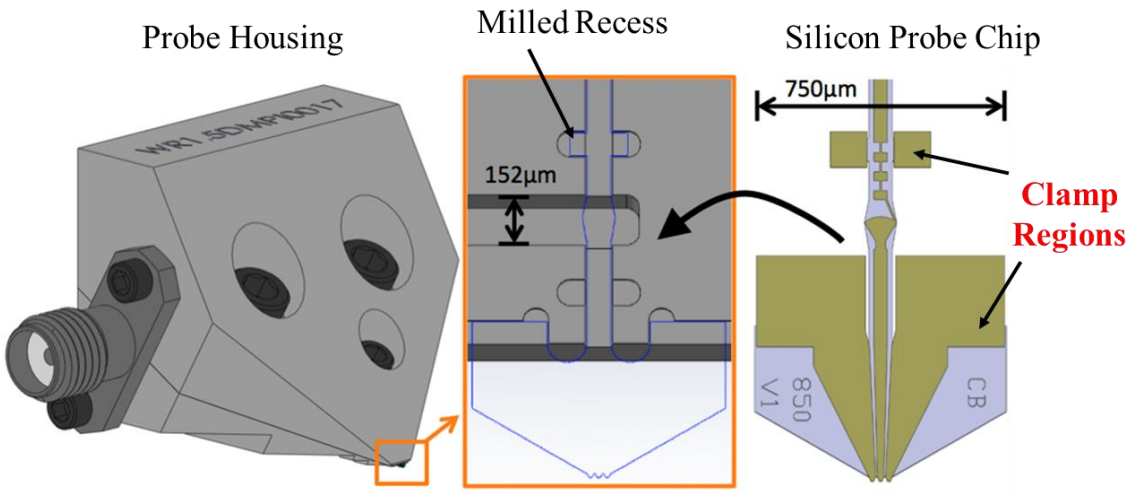

Figure 6.2: On-wafer probe clamping areas

6.1 Future Work

Directions for future research related to this dissertation should involve scaling the 40/160 GHz quadrupler design to higher frequencies, to realize multipliers (Figure 6.3) operating at submillimeter

wave frequencies. As with the 40/160 GHz quadrupler, the input of cascaded balanced multipliers would not load the driving stages and eliminates issues associated with cascading multipliers in a large chain. The reflected power from mismatches between stages would be terminated, allowing one to reach the 640 GHz and beyond with fewer multiplier blocks (or several chips integrated into a single block).

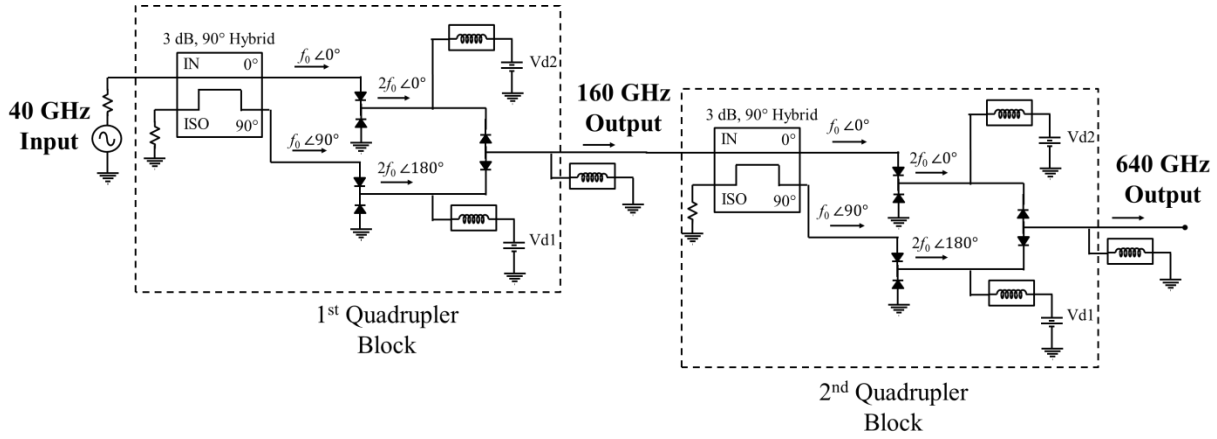

Figure 6.3: Two block 40/640 GHz multiplier

A second research direction should involve designing a high power doubler either on a silicon or diamond substrate to push the maximum input power handling and temperature limits of the quasi-vertical diode. Given that the 40/80 GHz doubler's average diode temperature was determined to be 35°C during operation, it would be valuable to design varactor Schottky diodes and study their performance specifically for higher input powers. As illustrated in Figure 6.4, to obtain frequencies in the THz range, a low frequency source is typically multiplied through a cascade of GaAs Schottky diodes, with each stage having a higher output frequency and lower efficiency. Therefore, to increase the available power for THz metrology it is desirable to pump each stage of the multiplier chain with the maximum power possible.

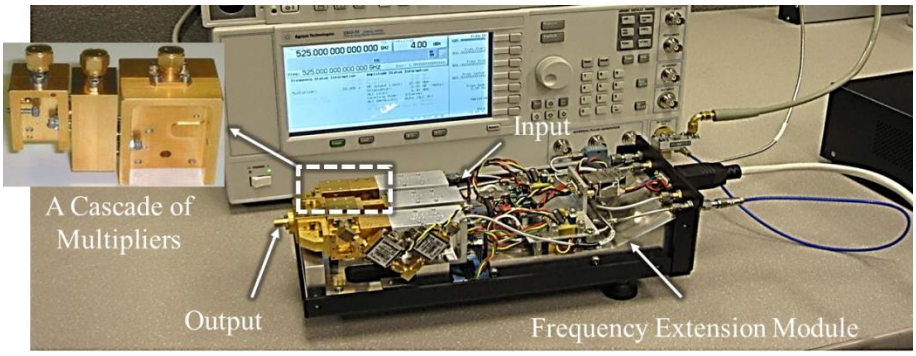

Figure 6.4: Vector network analyzer frequency extension module with highlighted GaAs Schottky multiplier chain.

Other possible research directions could involve the heteroepitaxy of III-V semiconductors other than GaAs with SOI to take advantage of silicon's robust processing infrastructure. Using the framework provided in this thesis, optical components could be fabricated on SOI to take advantage of silicon's mechanical and thermal properties, with the incorporation of gold beamleads for seamless device assembly.

The GaAs on SOI process can also be used to implement integrated measurement instruments, such as a six port reflectometer [103]. A six port reflectometer is used for vector measurements of scattering parameters and Figure 6.5 and Figure 6.6 demonstrate a possible layout for such a device integrated on an on-wafer probe chip. The six-port relies only on power measurements using four diode detectors and low pass filters. The diodes sample RF power on the transmission line, and after a somewhat involved calibration procedure, the *s*-parameter of the measured device can be determined. In this type of network analyzer the dynamic range is often limited by the detector sensitivity. However, it is a relatively inexpensive method for characterizing the reflection and transmission properties of devices and may be competitive with heterodyne techniques above 1 THz.

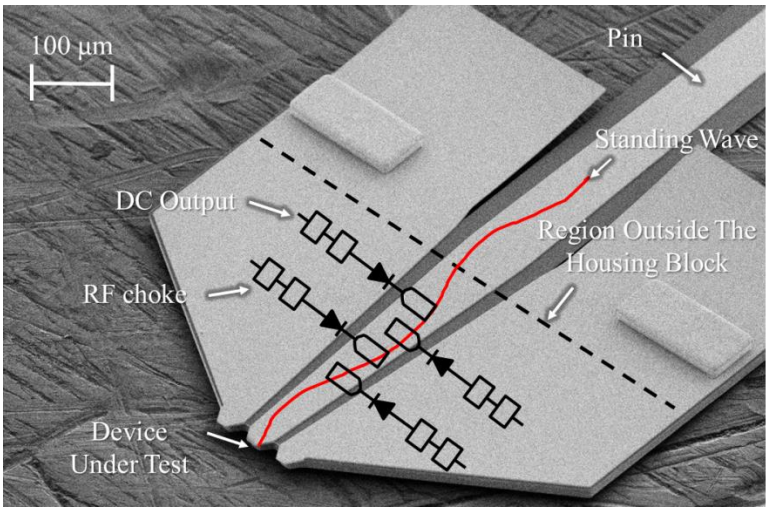

Figure 6.5: Concept layout for a six-port reflectometer integrated on an on-wafer probe

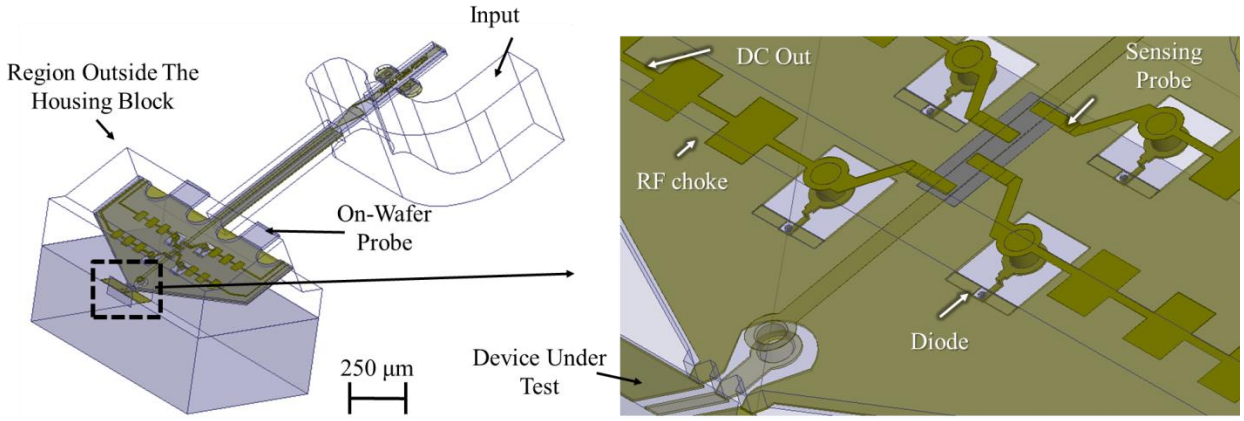

Figure 6.6: A possible *HFSS* layout for the six-port reflectometer integrated on an on-wafer probe

Finally, future improvements to the on-wafer probe design described in Chapter 3 could involve using rhodium instead of nickel for the tip metallization, as nickel oxidizes, has lower conductivity than rhodium and typically yields higher contact resistance. Such tips could be realized by plating rhodium/nickel/gold tips (200 nm rhodium/1 µm nickel/1µm gold), which may prevent the rhodium tips from cracking by providing a harder nickel supporting layer (Figure 6.7), or by reducing the plated tip's silicon overhang. In the current design, the plated probe tips extend past the silicon substrate by 5 µm (Figure 6.7) to account for possible misalignment. By devising a tighter alignment methodology, the tip's overhang could be reduced thereby mitigating the possibility of the tip cracking.

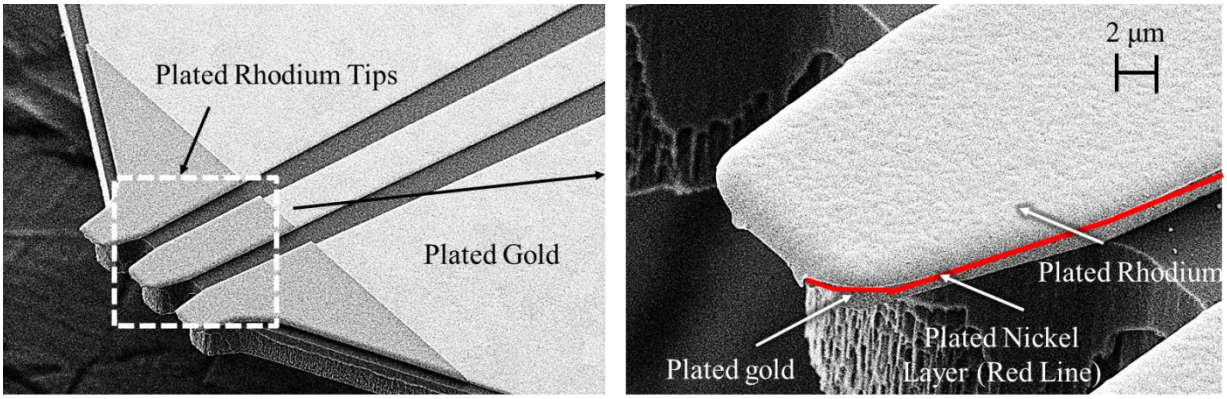

Figure 6.7: Triple layer plating for the probe tips: 200 nm rhodium/1 μm nickel/1μm gold

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Appendices

A. Planar GaAs Schottky Diode on Silicon-on-Insulator Process

Obtain a GaAs sample, epitaxial side of the GaAs wafer is waxed to the silicon carrier (epi side is also labeled on the bottom tab)
Starting wafer n/n^+/AlGaAs/Semi-insulating GaAs 220 nm/0.8um/2um/650um with doping of $1.7x10^{17}$ cm^{-3} and $5x10^{18}$ cm^{-3}
Clean surface w/ circular swab and acetone and methanol clean if necessary
March @ 200W 5 min, inspect

Bonding to Si:
Spin 2-proponal on SOI at same spin speed as SOG.
Spin SOG at 3KRPM
bake 1 min 100, 130, 150C

Bond GaAs to SOI in press jig for 15min at 195C
Thinning GaAs
Measure height sample on OnnoSoki
Place vertically in 1:6:1::HNO3:H2O2:H2O at 50C. Etch time ~20min
Want to reach ~70um from epi layers
Etch 3:1::Citric acid:H2O2 at 50C for ~40 hr to remove rest of GaAs
Rinse DI and move directly into HF, w/ agitation 1um AlGaAs clears in 1min.

Ohmic Contact Formation
Place sample in the HMDS evaporation beaker for > 3min, N2 blow, AZ4210 @ 6000 RPM, 30 s (~1.7um thick), pre-bake 100˚ C, 1 minutes
Use the edge beam mask and exposure for 300 s, hard contact (i-line or 365nm, 0.7mW/cm^2) on MJB4
Develop: DI:AZ400 4:1, 2 minute +15s after fully developed
Use the ohmic pattern mask and expose 45 s, vacuum contact.
Develop: DI:AZ400 4:1, ~1 minutes
Post-Bake 120˚ C, 1 minutes

Remove GaAs native oxide: 15 s NH4OH:DI (1:20)
Remove n^+ layer: 1:1:25 H2O2: H3PO4:DI, don't agitate, 1 min, determine etch rate on etch pattern & continue etch (etch rate ~200nm/min, etch n layer)

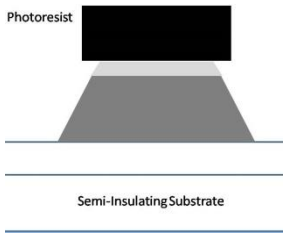
Or
10:1:: (50%)citric acid:(30%)H2O2 at 0.2um/min etch rate. 50% citric acid is 30g citric acid to 25mL of H2O (dissolve 50g of citric acid in such an amount of water that final volume is 100 mL)

Dry etch 2 scrap GaAs wafers w/ two 20x microscope dots (2min exposure), 1st dummy to determine etch rate after stripping photoresist (PR) (4 minute etch), 2nd dummy to determines total etch after stripping PR.
BCl_3 etches PR otherwise don't need dummies & measure real sample w/ PR. (etch rate ~50nm/min, PR etch 17nm/min?, want to etch ~200nm)
P=11mT, BCl_3=20sccm, RF=20W ,T=20˚C, He 4 Torr, V=80V
O2 clean Oxford chamber after chlorine etch

Remove GaAs native oxide: 10s BOE (keep wet), 15 s NH4OH:DI (1:20), blow dry
Evaporate metals Au/Ge 50 nm, Ni 25 nm, Au (variable thickness to fill RIE trench), Ni 25 nm (for SiO adhesion)
Or 50/50/100/50 AuGe/Ni/Au/Ni for total of 250 nm in RIE trench (7min)

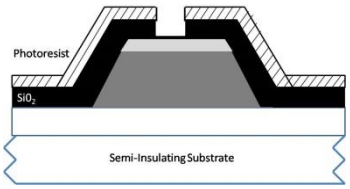
Lift-Off 1:1 NMP:propylene glycol @ 120˚C, or acetone boil @ 50°C
Clean with acetone, methanol, March 200W

RTA 400˚C, 60 s
Test ohmic contacts' specific contact resistance (Midkiff $1.5x10^{-5}$ ohm*cm^2)



Mesa formation
Place sample in the HMDS evaporation beaker for > 3min, N2 blow, AZ4210 @ 6000 RPM, 30 s (~1.7um thick), pre-bake 100˚ C, 1 minutes
Use the edge beam mask and exposure for 300 s, hard contact (i-line or 365nm, 0.7mW/cm^2) on MJB4
Develop: DI:AZ400 4:1, 2 minute +15s after fully developed
Use the ohmic pattern mask and expose 45 s, vacuum contact.
Develop: DI:AZ400 4:1, ~1 minutes
Post-Bake 120˚ C, 1 minutes

Remove GaAs native oxide: 15 s NH4OH:DI (1:20)
Remove n^+ layer: 1:1:25 H2O2: H3PO4:DI (~200nm/min), don't agitate, etches AlGaAs
Or
Anisotropic etch & selective to GaAs- 1:5::H2O2:citric acid (~400nm/min),
See color change once you reach AlGaAs etch stop
Etch for 1 minute & measure etch rate
To confirm that you are on AlGaAs use 4-point probe ensure no conduction
Remove resist acetone, methanol, March 200W



Oxide deposition & anode formation & ohmic contact opening

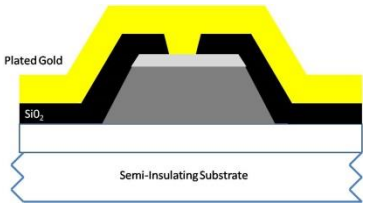
Need 4 dummy silicon samples: sample 1 for oxide thickness (microscope dot & 5min in BOE, double check w/ Filmetrics), sample 2 for dry etch rate of oxide (microscope dot, record PR, take out after 45min and measure w/ & w/o PR), sample 3 to determine total etch (real pattern), sample 4-wet etch rate oxide (real pattern)

Remove GaAs native oxide: 10s BOE (keep wet), 15 s NH4OH:DI (1:20), blow dry
"ascrub" to clean chamber PECVD chamber,
Samples & dummy in PECVD and use PECVD "SiO2Vart" recipe, deposition ~10nm/min

Spin PR for anode definition
PR is lost during dry etch (example: for 1um oxide and need ~1um resist and 300nm PR will be etched during RIE)
Dummy & sample HMDS >3min, AZx for 30 sec, edge bead
Aspect ratio should about 1:1 (ie if features are 1um then resist should be ~1um)
Use the edge beam mask and exposure for 300 s, hard contact (i-line or 365nm, 0.7mW/cm^2) on MJB4
Develop: DI:AZ400 4:1, 2 minute +15 s after fully developed
Use the ohmic pattern mask and expose 45 s, vacuum contact.
Develop: DI:AZ400 4:1, ~1 minutes
Post-Bake 120˚ C, 1 minutes

Dry etch SiO2 anode
Oxford: P=10mTorr, ICP=0W,RF=80W, CHF3=50 sccm,V=330V
~10nm/min SiO2 etch rate, 3nm/min PR etch rate
Want to leave about 70 nm of oxide to prevent damage to the GaAs that will form the Schottky anode
Trion: P=60mTorr, ICP=0, RF=100W, O2=5sccm, CF4=50sccm ~50nm/min SiO2 etch rate, 90nm/min PR etch rate (Sami though the oxide to resist selectivity was 1:3)

Use dummies 1 to 4 to determine the necessary etch rates
Wet etch SiO2 anode 40:1, DI :BOE (10nm/min), don't agitate
Remove resist acetone, methanol, March 200W for 5 minutes



Schottky contact & ohmic contact pad
Evaporate seed layer for Schottky contact
1 minutes NH4OH:DI (1:20), blow dry

100 nm titanium (adhesion layer), 100 nm gold, SEM to measure the anode
PR for contacts, HMDS >3min,AZx for 30 s, PR must be thicker than mesa
Pre-Bake, 100˚ C, 1 minutes
Use the edge beam mask and exposure for 300 s, hard contact (i-line or 365nm, 0.7mW/cm^2) on MJB4
Develop: DI:AZ400 4:1, 2 minute +15 s after fully developed
Use the ohmic pattern mask and expose 45 s, vacuum contact.
Develop: DI:AZ400 4:1, ~1 minutes
Post-Bake 120˚ C, 1 minutes

10min 150W O2 plasma
Measurement record PR thickness
Mount to slide, only glass and wafer should be in plating solution
Plate, ions are positive so ground sample.
Fill plating bath (50˚C), start w/ current of 1mA and voltage drop across solution of 0.5V. Increase current in progression
Measure deposited gold (do this in 5 minute increments)

Remove resist acetone, methanol, March 200W for 5 minutes, SEM
Seed layer removal: Iodine Au etch (15nm/min) HG-400 family (45s for 100nm is typical)
40:1, DI :BOE, ~25s (20s full BOE for 100nm titanium seed is typical)
Surface clean acetone, methanol, March 200W for 5 minutes

Extents etch alignment mark (if using SOI):
Spin resist for ~20min+1min overetch in Oxford, bake 100C 1min, expose and develop, bake 130C 3min
Oxford: 'Si etch C4F8=35 SF6=30 ICP 500 EP', C4F8 35sccm, SF6 30 sccm, 0C, use endpoint detection.
March 200W 10min, rinse resist in reagent alcohol
Bonding SOI to carrier:
Need 2" 500um Si carrier
Spin Waferbond CR-200 on sample and carrier at 3KRPM 30s
Clean back of sample and carrier w/ median swab and small amount of TCE sprayed
Bake 120, 180C 2min
Bond using Art's jig
Measure working thickness
Get the hubless blade for dicing (ALHUB1)
In dicing saw do the hair line alignment to find total thickness of the wafer
In Disco dicing work size +5mm on each side, measure Working distance
blade height = Working distance –456um+70um (leaving 70um results in ~40min Si etch)
Y index(distance btw cuts)=0.3mm, cut (number of cuts for 30mm wafer is 110 lines), dicing speed= 3mm/s

To remove rest of Si attach sample to Qz carrier wafer using L-grease
Oxford: 'Si Trion handle etch 30s 100W', 20C. This etch uses 30s of 100 and 50W RF to create the ions for ICP (500W) but use 0W RF for the final etch.
Use the WinTV camera to gauge when etch is done and give 5 minutes over etch
BOE 10:1, 20min, 1um of BOX layer

Extents etch:
Spin AZ4330 3KRPM, bake 100C 1 min, expose, develop, bake 130C 3min
Oxford: 'Si etch C4F8=35 SF6=30 ICP 500 EP', (35sccm) C4F8 & (30sccm) SF6, ~13min etch.
March 200W >10min, remove resist is reagent alcohol
Soak sample in TCE
Place circuit in 50mm petri dish covered in Al foil on top and bottom and 55mm filter paper.

B. 90° Twist Fabrication

Creating the plating mold
1x1" Si substrate w/ 20/50/20nm of Ti/Au/Ti
Remove KMPR 1050 from 0°C fridge

Thickness of the spun KMPR depends on substrate shape and spin speed. For 1x1":
800 RPM, ~220um, 100C 2.5hr prebake, expose 9.5 min, post-bake 30s 90C and 8min at 100C
730 RPM, ~350um, 100C 3hr prebake, expose 10 min, post-bake 30s 90C and 9.5min at 100C
630 RPM, ~450um, 100C 3.5hr prebake, expose 10 min, post-bake 30s 90C and 10min at 100C

If sample stick to the mask during exposure this is a good indicator that pre bake time is too short. You should be able to make hard contact w/o sticking to the mask.
Need a UV low pass filter that block UV above 350nm.
Develop with agitation for 4-10min in 300MIF TMAH developer, rinse with IPA, rinse in DI and blow dry

Plating Nickel
Technic Inc Nickel Sulfamate RTU @ 50C w/ pocket of boric acid to keep the pH constant for the 8-10 hours of plating needed. Don't use brightener since it increase the stress in the plated film and also need a strong agitation source.
Attach sample to metallic holder using electrical tape and conductive copper tape
Use brush and cover areas of sample you don't want plated in Miccro Super Spin off Lacquor XP2000
Cure the lacquer until hard.
Attach positive to Ni bars and negative to sample and build up to plating rate you are happy with (~1.4 volts).

Lapping
Attach sample to lapping plate using lapping wax and lap until surface is level.
Caution: sample might detach from the KMPR mold wile lapping so be careful when measuring the amount lapped since the bow and the detach sample might give the wrong rate.
Remove sample in from Si if sample is not already detached using 1:3 KOH:DI @ 80C

Final Plating
Gold plate nickel sample to prevent oxidation

C. On-wafer Probe Fabrication

Via etch
Clean the 2" wafer w/ swab and TCE/ACE/MET. Make sure the edge of the wafer is clean of debris.
March 200W for 10min
Spin HMDS & AZ4330 4KPRM, pre-bake 100C, expose 50s, develop ~1 ½ min, post-bake 100C ~3min
Use the following recipe in the Oxford: 'Si etch C4F8=35 SF6=30 ICP 500 EP', (35sccm) C4F8 & (30sccm) SF6, DC 159 (using Qz carrier), 0C, He flow 5sccm and L-grease sample to carrier on 100C hot plate (remove sample also on 100C hotplate)
SOG ER >140nm/min, hardened PR ER~112nm/min, SiO2 ER 36.32nm/min, Si ER 1.2 micrometer/min, unhardened PR ER ~153nm/min.

March 200W 10min

Front side metal
Then acetone clean rest of resist and inspect.
BOE 20s to make surface super hydrophobic
Sputter Ti/Au in sputt3 machine for 1.5 min/2.5min.

Spin HMDS & AZ4330 3KPRM, pre-bake 100C, expose 'Burn' 400s, develop 2 min.
Expose 'ExVia' 400s, **don't develop**. This is expose resist in the 15um via holes.
Expose Font side metal 70s, develop 2 min
March 200W for 20 min

Post bake AZ4330 100C 1min and 130°C 10min
Plate soft Au (13mA, ~0.6V, ~70nm/min)

Spin HMDS on top of AZ4330, spin AZ5209 4KRPM , prebake 100C 1min, expose 30s, postbake 100C 1 min 30s, flood expose 70s, develop 30s.
Ignore cracks in AZ4330 at this point

Plate Ni 1.3V, 3mA, 1.4V
or
Rh @2.2mA, ~1.5V, plate rate ~90nm/min.
Acetone spin clean, March 200W 15min to residual hardened resist.

Front side clamp
spin HMDS AZ4620 3 KRPM (10um), exacto edge bead removal, pre-bake 100C, spin AZ4620 2.5 KRPM to get 20um of resist, exacto edge bead removal, pre-bake 100C, expose Front Side Clamp MJB4 for ~600 s depending on the age of the resist.
Develop 5-14min 1:4 400K:DI

March 150W 5min

Plate soft Au (6mA, ~0.77V, 130nm/min and 11mA, ~0.87V, ~240nm/min)

Spin clean w/ acetone and March 200W for 10 min.

Seed removal
Remove Au seed using Semigroup Au etch (Ar x sccm since flow meter doesn't work, Press 20mT, DC 720V, RF 140W, 5min on 2 min off to cool
Remove Ti seed in BOE, 30s

Measure IV characteristics between Au pads
Should measure ~10e-5A current for a sweep 1e-9 to 30e-3A, w/ voltage limit set at 10V.

Thinning Silicon Handle
Spin Waferbond on SOI sample at 1.2KRPM 30s (20um of Waferbond) and bake at 120 and 180C for 2min.
Spin Waferbond on carrier sample at 3KRPM 30s (~8um of Waferbond) and bake at 120 and 180C for 2min

Place cross of L-grease on bonding jig's removable handle and attach SOI,
Place Si carrier in the jig
Pull a vacuum on the jig for ~5min, while heating to 50C
Bring two side into contact and turn on heat to 180C and wait ~ 7min
Spin clean back of sample and clean sample w/ TCE
Press hotplate should be at 200C to get 180C on the press.
Press in the following sandwich: lapping glass/ sample/silicon/laping glass/.75" teflon (in Art's cabinet) for ~ 10min

Measure working thickness using granite based gauge stand: working thickness-456um+70um and 70um is how much you are leaving of handle.
To measure working thickness do a few hairline alignment cuts.
In dicing saw center wafer, cutstroke/length wafer of 60mm (+5mm each side), Y-indx or kerf of 0.35mm, and speed of 3mm/s

After dicing clean sample in TCE/ACE/MET and make sure surface is clean.
Use Qz carrier and L-grease at 100C to attach sample for handle etch in Oxford 'Si Trion handle etch 30s 100W'-O2 2 sccm, SF6 20sccm, ICP 500W, 20C, P 20mTorr, ER 1.6um/min ~40 minutes etch.

Use the WinTV, give 2 minutes over etch. Gold via's become visible at the end of the the etch
BOE 10:1 25min (1um SiO2). The surface of Si should be superhydrophic indicating Si is gone

Backside metal
Evaporate Ti/Au 10nm/50nm 2 Angstrom/s & 2 Angstrom/s
Spin HMDS & AZ4210 4KPRM, pre-bake 100C, expose 40s using hard contact, develop 1min
March 150W 5min,

plate ~1um (8mA, 0.55V ~76nm/min, 10mA 0.6V plating rate is too fast).
Spin clean w/ acetone and March 200W for 10 min.

Remove gold seed layer using HG400 gold etch, ~30s
Remove titanium seed layer using BOE, ~30s

Measure IV characteristics between Au pads

Extents etch
Spin HMDS & AZ4620 3KPRM, pre-bake 100C, expose 180-250s, develop 2 min, post-bake 100C ~3min.
Oxford: 'Si etch C4F8=35 SF6=30 ICP 500 EP', (35sccm) C4F8 & (30sccm) SF6, He flow 10sccm, DC70-186V
This is 20-26 min etch w/ 3 min of over etch to get ride of rim problem (overetch doesn't noticeably round probe features).
March O2 200W 10min
Clean in acetone and methanol

Release chip
Soak wafer in 70°C TCE ~10min, until sample move slightly when container is moved.
Pour TCE in waste and clean in acetone and methanol.
Repeat TCE/acetone/methanol

Rinse and spread sample onto a 150mm Whatman filter paper and place on hot plate (50C) to dry solvent.
Place samples in an aluminum covered petri dish

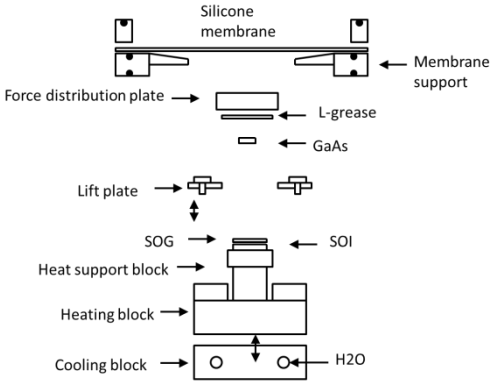
D. Quasi-Vertical GaAs Schottky Diode on Silicon-on-Insulator Process

Starting wafer N+/N/AlGaAs/SI 1um/0.28um/1um/650um
17 x 17mm GaAs (actual sample) and 25 x 25mm Si carrier (~450um thick).
Remove GaAs from dicing carrier and w/o cleaning mount face up on Si
Rinse sample of majority of black wax in beaker of TCE
TCE/reagent alcohol/methanol/N2 blow dry
March 150W 10minute.

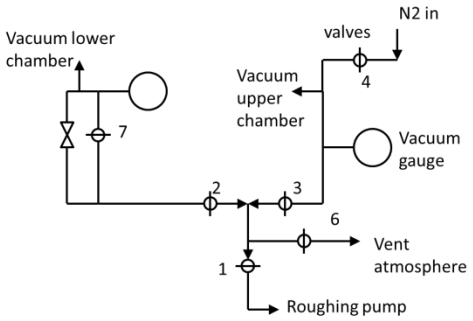
Ohmic contact:
Spin LOR10B @ 4 KRPM, 30s and bake 180°C 1 minute
Spin AZ4210 @ 4 KRPM, bake 90C 1minute
March 150W 5minute
20s BOE, 20s 1:10 NH4OH:DI
Evaporate 30/40/50nm of Ge/Pd/Au
Remove AZ4210 in ACE 50°C
March @150W for 5 minute
The Ohmic plating currents depends on area and could be .05mA-.4mA, ~0.4V, but want ~50nm/minute
Plate as much need for the skin depth
Evaporate 10nm Ti
Remove LOR in straight 400K solution for 1 minute
March GaAs 200W 10 minute
Anneal 335C 90s RTA

Bonding to Silicon or SOI:
Spin 2-proponal on SOI or GaAs at 3KRPM
Spin SOG on SOI or GaAs at 3KRPM
Must spin 2-proponal immediately before spinning SOG
bake 1 minute 100, 130, 150C

Bond GaAs to SOI in press jig for 15minute at 195C:



Pressing chamber



Connection to the chamber

Turn off all valves before plugging in diaphram vacuum pump
Raise lift plate to 2 on micromanipulator to create the separation between samples
L-grease larger carrier to force distribution plate at 150C and make sure it is flat and place GaAs sample on heat support block with very small amount of L-grease
Place membrane support for lower chamber then silicon membrane and membrane support for upper chamber
Cover the stack with the chamber cap
Evacuate upper chamber by turning valves 1 & 3 on. Upper chamber pressure will read -29" psi

Evacuate lower chamber to -29" psi by turnign 3 off and 2 &7 on. During lower chamber evacuation the the upper chamber pressure will drop to -23psi.
In pressing jig 5 minutes at 30C under full vacuum.
Then bring samples into contact using the micrometer.
Make sure lower sample reads -28" psi and upper chamber should read ~-10 psi. It takes until 70C when the chamber pressure is stable and valve 2 can be turned off.
Raise temperature to 195C takes ~11min
Hold for at least 15min at this temperature
To cool turn on chiller and bring cooling block into contact (~10min). Vacuum will be lost at this point and both chambers will be at atmosphere otherwise equalize pressure in upper & lower chamber by turning valve 1 off & 3 on, vent both chambers by turning 6 on.

Thinning GaAs
Measure height GaAs sample bonded to Silicon or SOI on OnnoSoki

Place vertically in 1:6:1::HNO3:H2O2:H2O at 50C. ER (should be ~24um/min)
Rotate sample 90° every 5min to get more uniform etch and measure ER every 10min.
Etch time ~20minute
Want to reach ~70um from epi layers
Etch 3:1::Citric acid:H2O2 at 50C for ~40 minute to remove rest of GaAs
Rinse DI and move directly into HF, w/ agitation 1um AlGaAs clears in 1minute.

Mesa etch:
Spin HMDS then spin AZ4210 @ 4 KRPM 30s, bake 100C, and open microscope dots over alignment marks using DIC setting, bake 130°C 3 minute. Etch 1:5 H2O2:Citric acid and remove resist.
Spin HMDS at the same speed as resist then spin AZ4210 @ 4 KRPM 30s, bake 100C 1 minute.
Expose>develop 1 minute>bake 130C for 5minute
Etch mesa in 1:5::H2O2:citric acid (ER 340nm/minute),

SOG etch:
Removing SOG in CHF3 etch for ~2hr (due to fact SOG is so uneven):
Leave mesa etch resist and spin HMDS then spin AZ4210 @ 4 KRPM 30s, bake 100C, expose, develop, bake 130C 1minute. L-grease to Si carrier wafer for SOG etch
CHF3 50 sccm, Pressure 10mTorr, RF 160W, DC bias ~551V, temperature 0°C on Oxford (L-grease to platter):
SiO2 ER 20nm/min, photoresist ER ~6nm/min, SOG ER 16nm/min, Si ER 4nm/min, Au ER 2.6nm/min

March 200W 10minute, rinse resist in reagent alcohol

Extent alignment mark:
Extents etch alignment mark (if using SOI):
Spin resist for ~20minute+1minute overetch in Oxford, bake 100C 1minute, expose and develop, bake 130C 3minute
Oxford: 'Si etch C4F8=35 SF6=30 ICP 500 EP', C4F8 35sccm, SF6 30 sccm, 0C, use endpoint detection.
SOG ER >140nm/min, hardened PR ER~112nm/min, SiO2 ER 36.32nm/min, Si ER 1.2 micrometer/min, unhardened PR ER ~153nm/min

March 200W 10minute, rinse resist in reagent alcohol

Sacrificial resist:
Sacrificial resist and plating:
Spin resist depending on anode size, bake 100°C 2minute, expose and develop 1 minute
March 150W 5 minute, 20s BOE, 15s 1:20::NH4OH:DI
Use Sputt3 tool, then sputter ~1.16minute Ti and Au.

Plating resist:
Spin resist to cover sacrificial resist

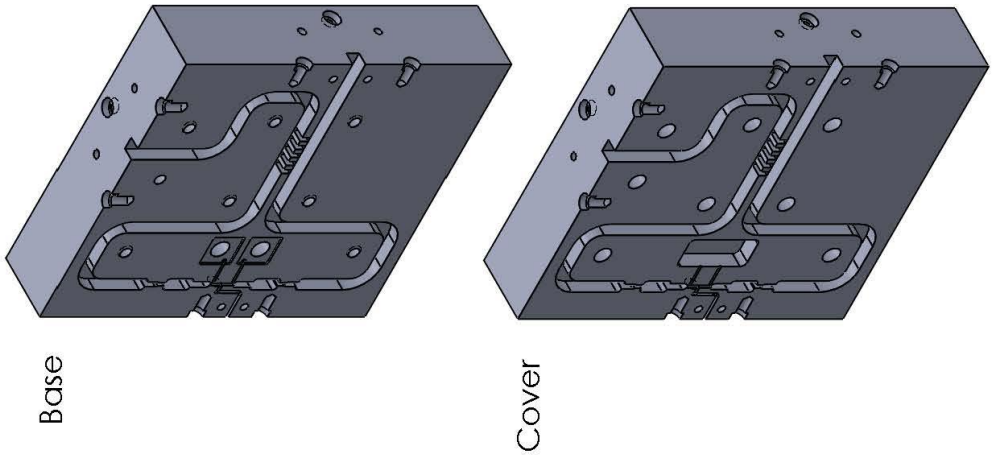
Bake 90°C 2min, expose and develop
March 150W for 5minute
Plating current could be btw 2-4mA, ~0.55V plating voltage
Remove resist used for plating by flood exposing on MJB4 and remove resist in 1:4::400K:DI.
March 200W for 20minute
Remove seed layer using HG400 ~20s and BOE ~25s
15min 50sccm, 100mT, 100W, -690V O2 clean in the Semigroup allows hardened sacrificial resist to be removed in Acetone.

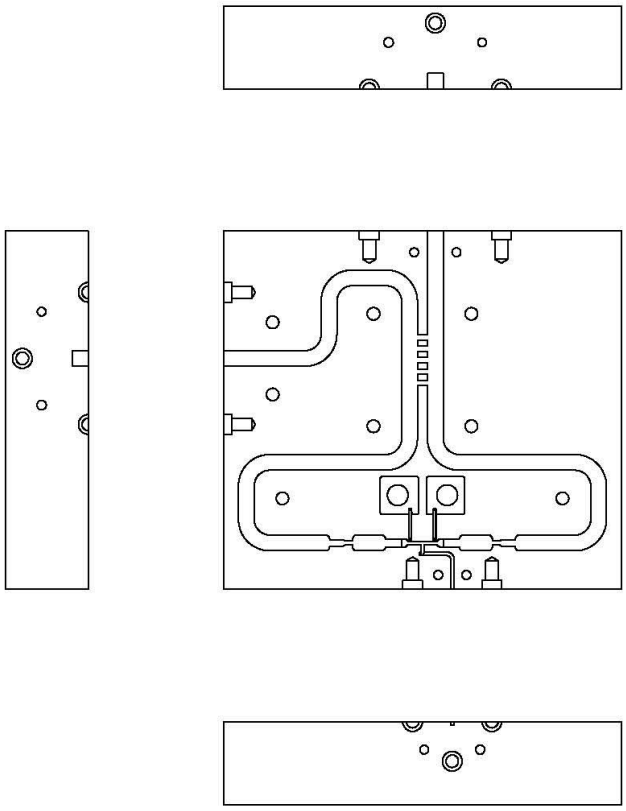
Remove silicon handle:
Bonding SOI to carrier to remove silicon handle:
Need 2" 500um Si carrier
Spin Waferbond CR-200 on sample and carrier at 3KRPM 30s
Clean back of sample and carrier w/ median swab and small amount of TCE sprayed
Bake 120, 180°C 2minute
Bond using Art's jig or Ed's press at 180°C
Measure working thickness
Get the hubless blade for dicing (ALHUB1)
In dicing saw do the hair line alignment to find total thickness of the wafer
In Disco dicing work size +5mm on each side, measure Working distance
blade height = Working distance –456um+70um (leaving 70um results in ~40minute Si etch)
Y index(distance btw cuts)=0.3mm, cut (number of cuts for 30mm wafer is 110 lines), dicing speed= 3mm/s

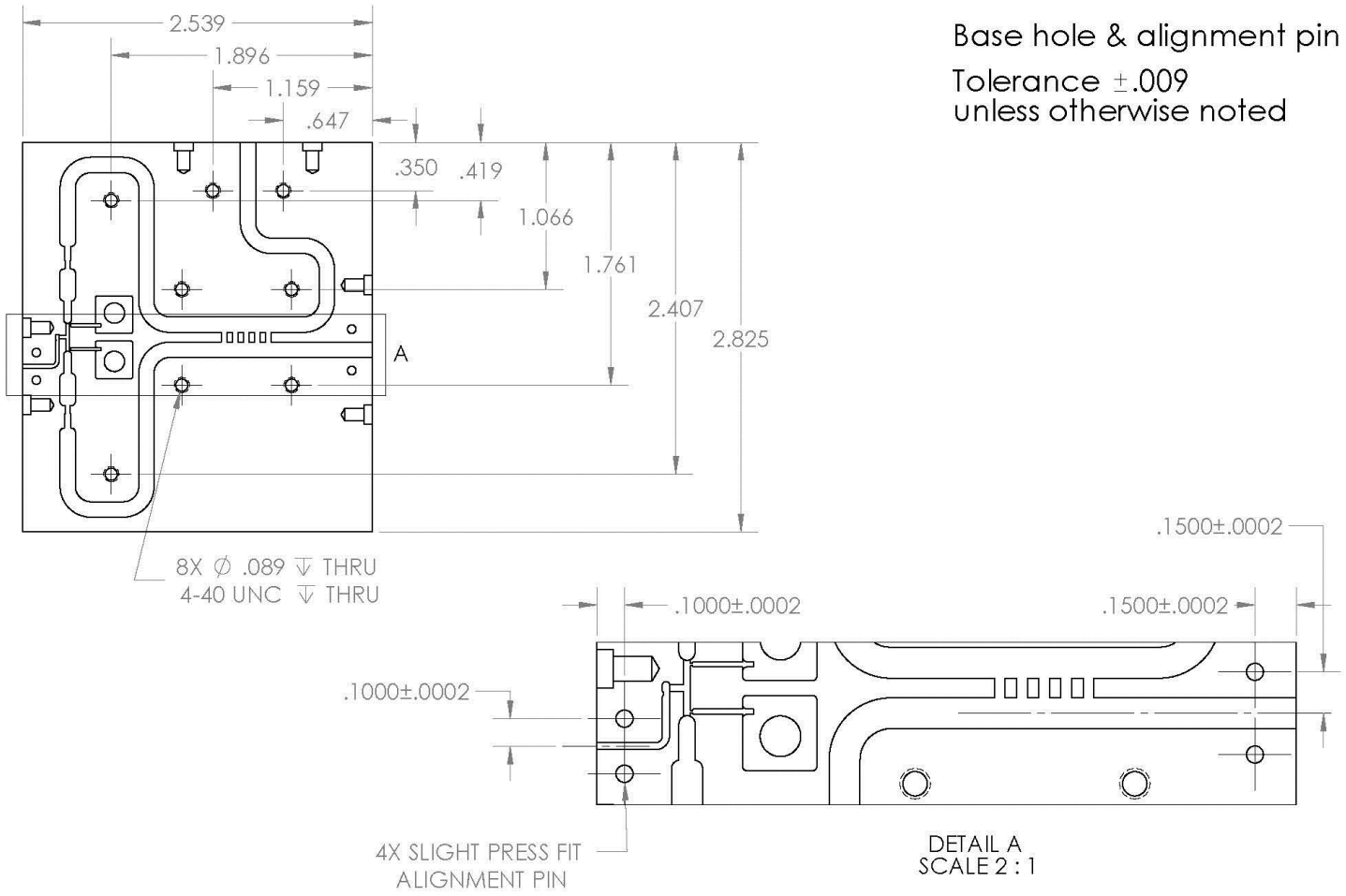
To remove rest of Si attach sample to Qz carrier wafer using L-grease
Oxford: 'Si Trion handle etch 30s 100W', 20C. This etch uses 30s of 100 and 50W RF to create the ions for ICP (500W) but use 0W RF for the final etch.
Use the WinTV camera to gauge when etch is done and give 5 minuteutes over etch
BOE 10:1, 20minute to etch 1um of BOX layer

Extents etch:
Spin AZ4330 3KRPM, bake 100C 1 minute, expose, develop, bake 130°C 3 minute
Oxford: 'Si etch C4F8=35 SF6=30 ICP 500 EP', (35sccm) C4F8 & (30sccm) SF6, ~13 minute etch.
March 200W >10minute, remove resist is reagent alcohol
Soak sample in TCE
Place circuit in 50mm petri dish covered in Al foil on top and bottom and 55mm filter paper.

E. Quadrupler Waveguide Block



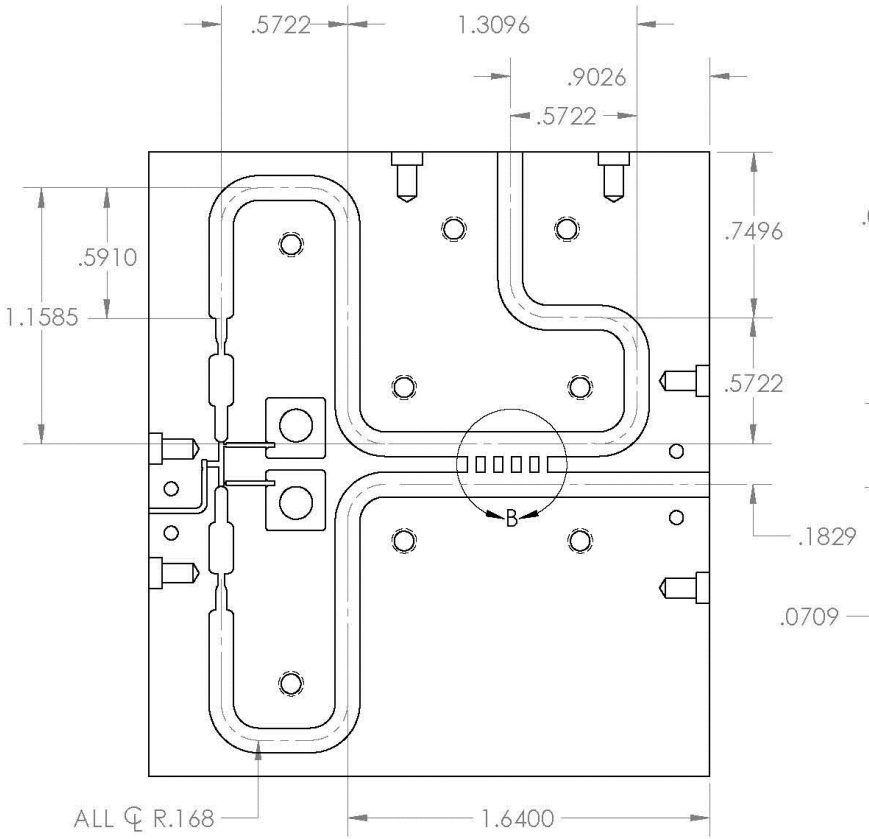


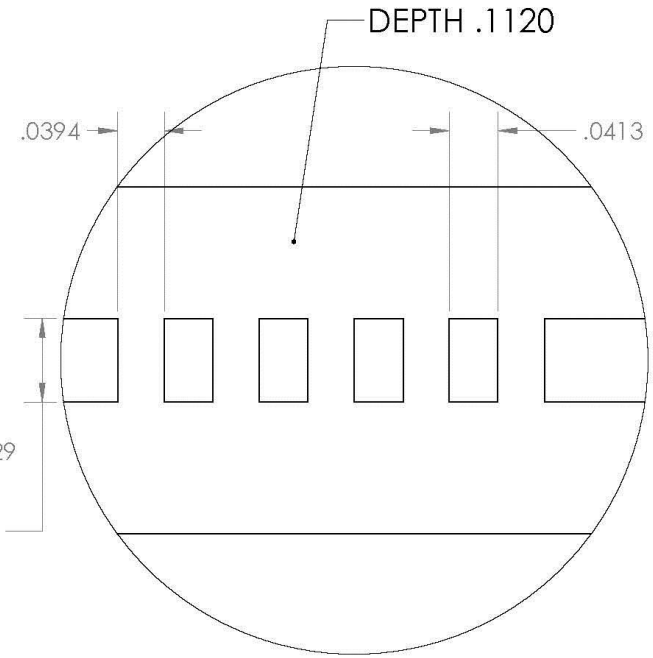


Base hole & alignment pin

Tolerance ±.009
unless otherwise noted

Base WR22 waveguide
Tolerance ±.0005
unless otherwise noted

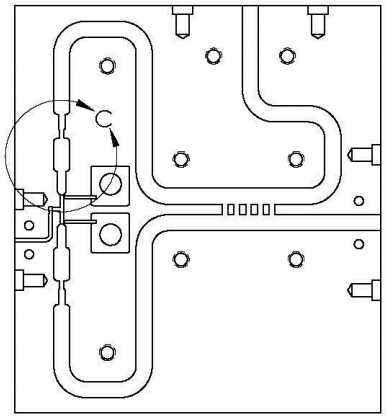


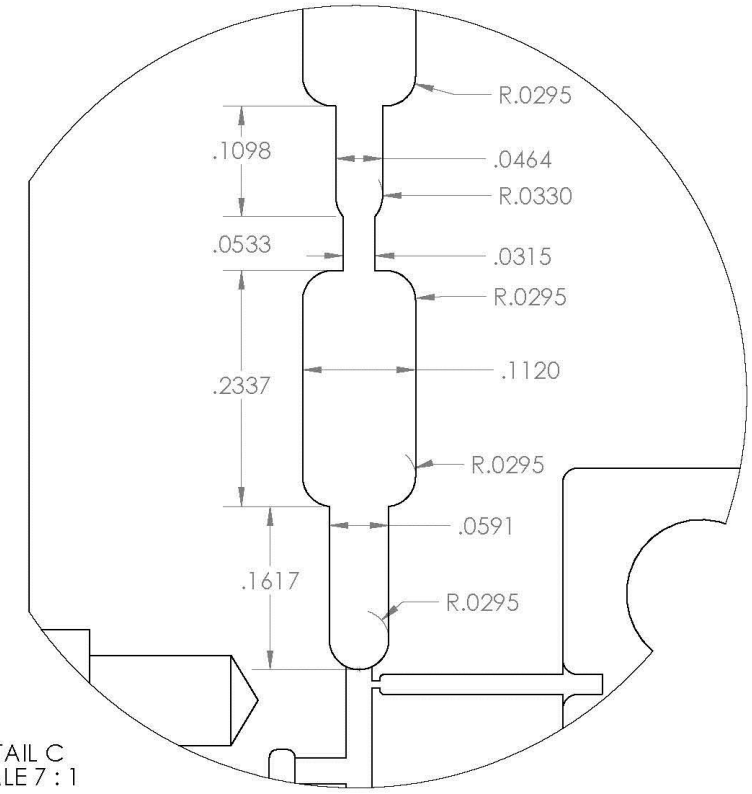


DETAIL B
SCALE 8 : 1

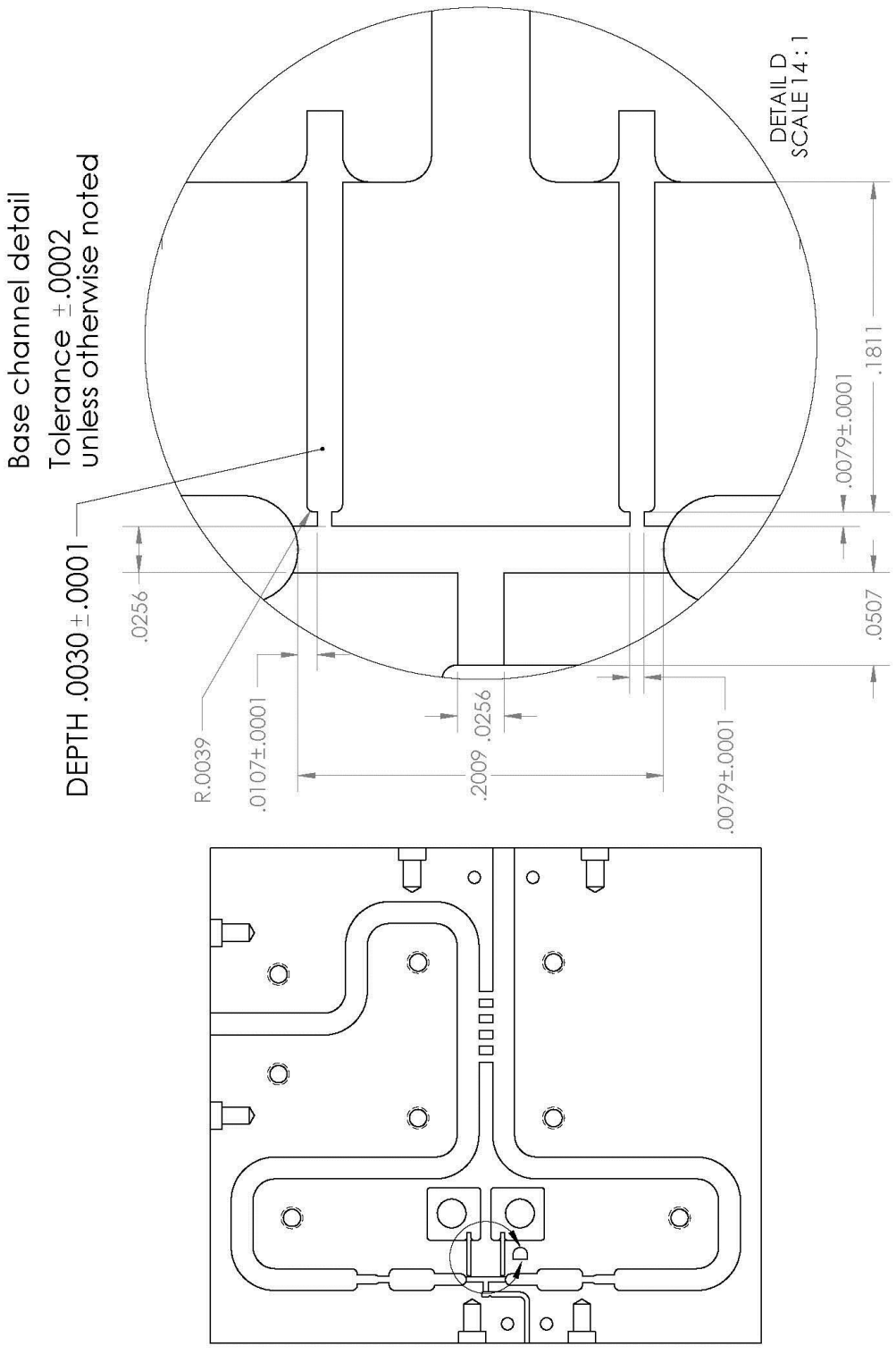
Base WR22 detail

Tolerance ±.0005
unless otherwise noted



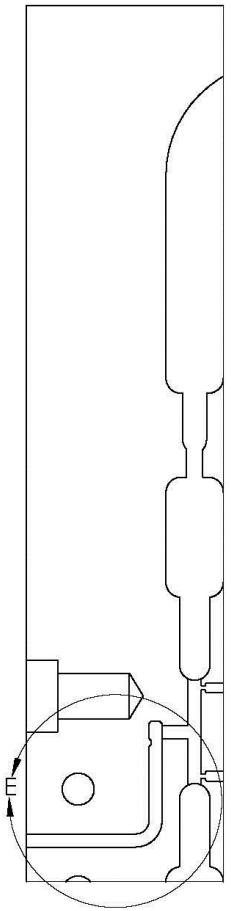


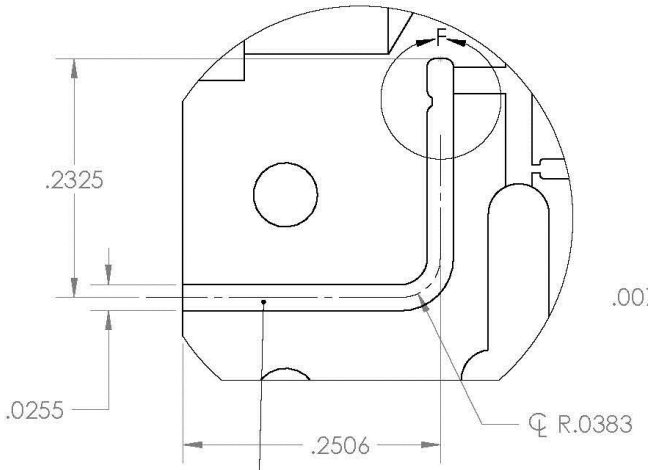
DETAIL C
SCALE 7 : 1


Base channel detail
Tolerance ±.0002
unless otherwise noted
DEPTH .0030±.0001
DETAIL D
SCALE 14 : 1
.0256
.0507
.0079±.0001
.1811
R.0039
.0107±.0001
.2009
.0256
.0079±.0001

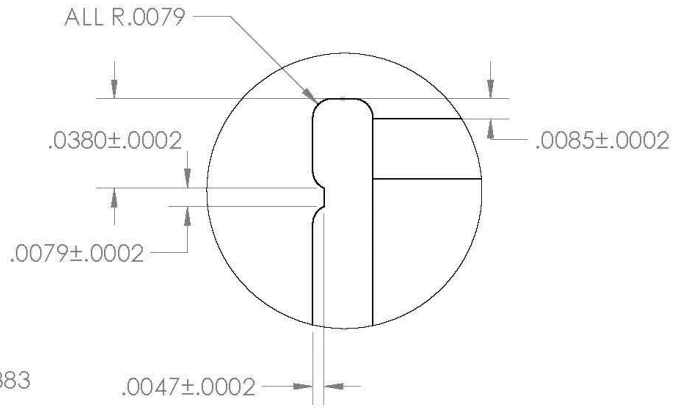
Base WR5 waveguide

Tolerance ±.0003
unless otherwise noted

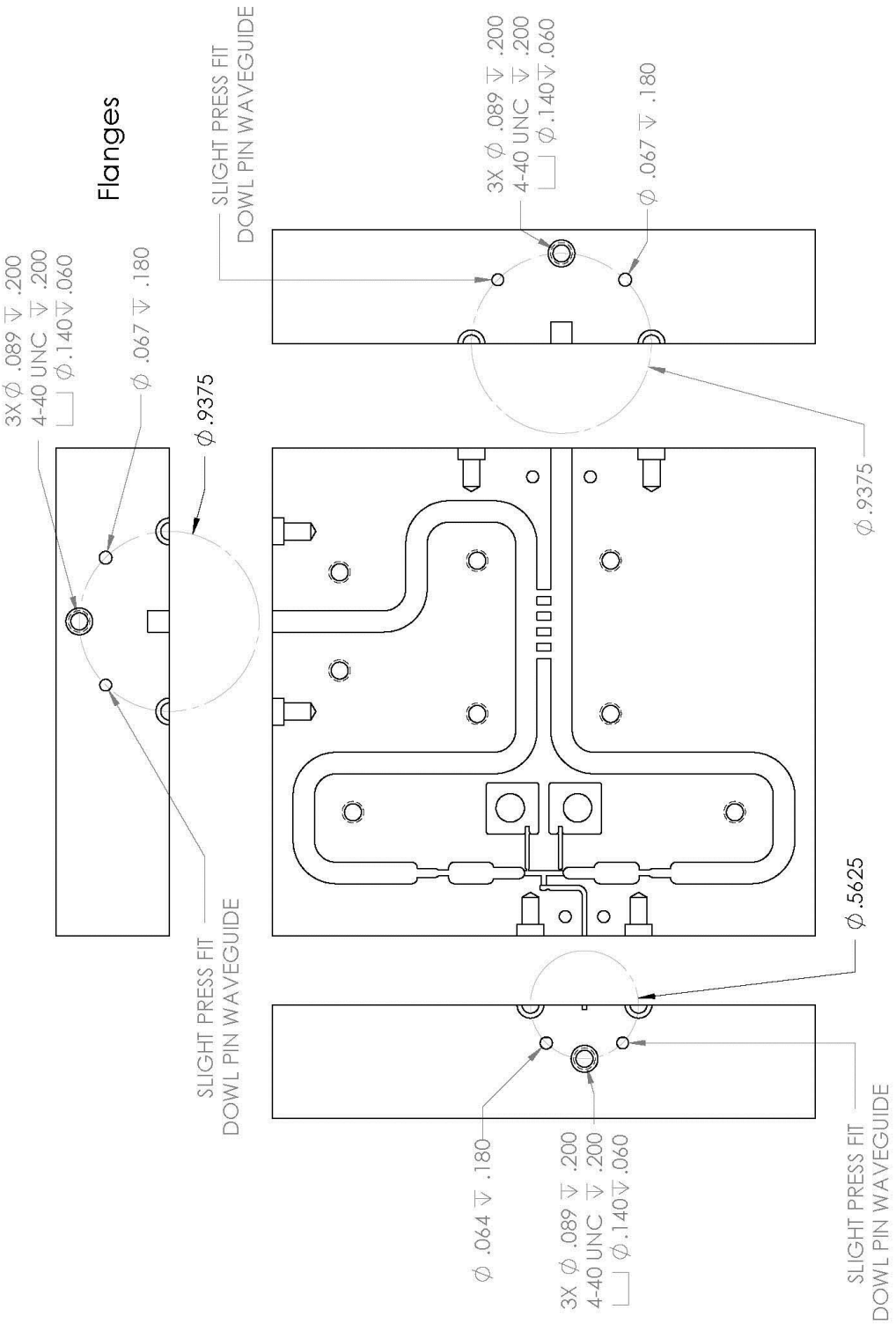


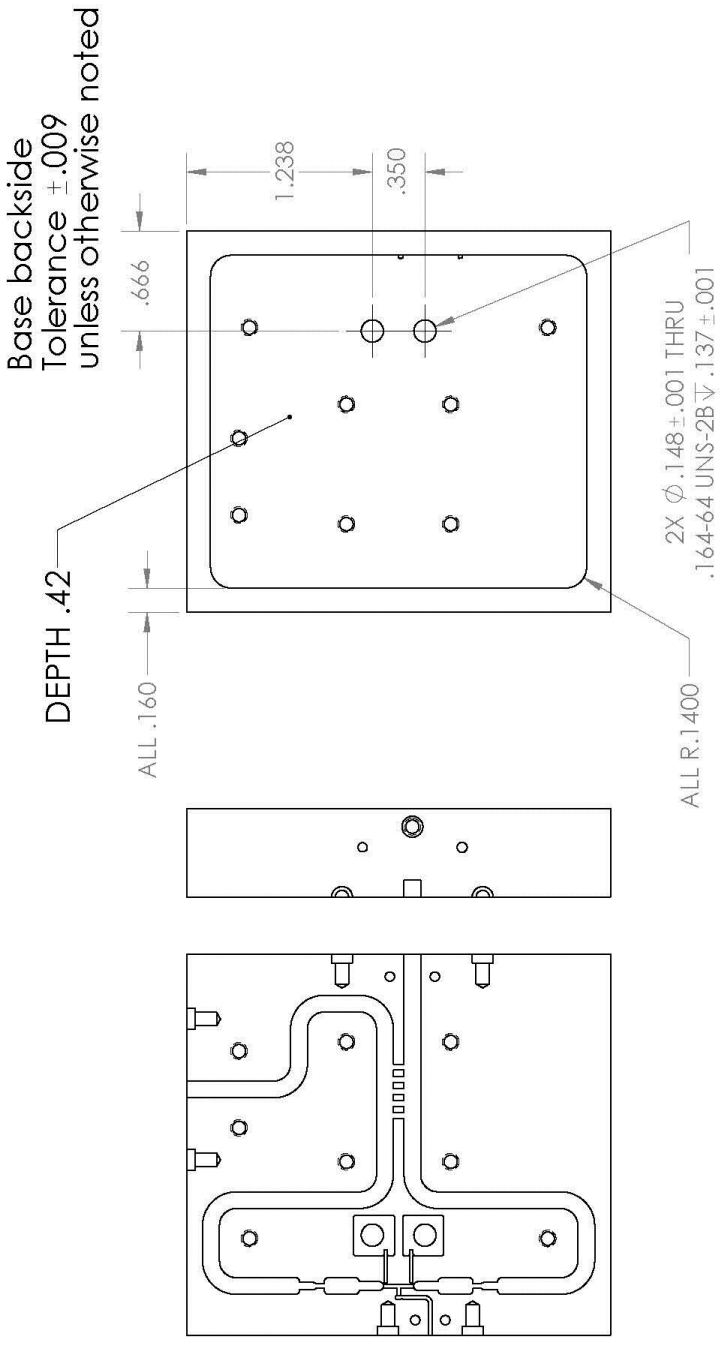


DETAIL E
SCALE 7 : 1

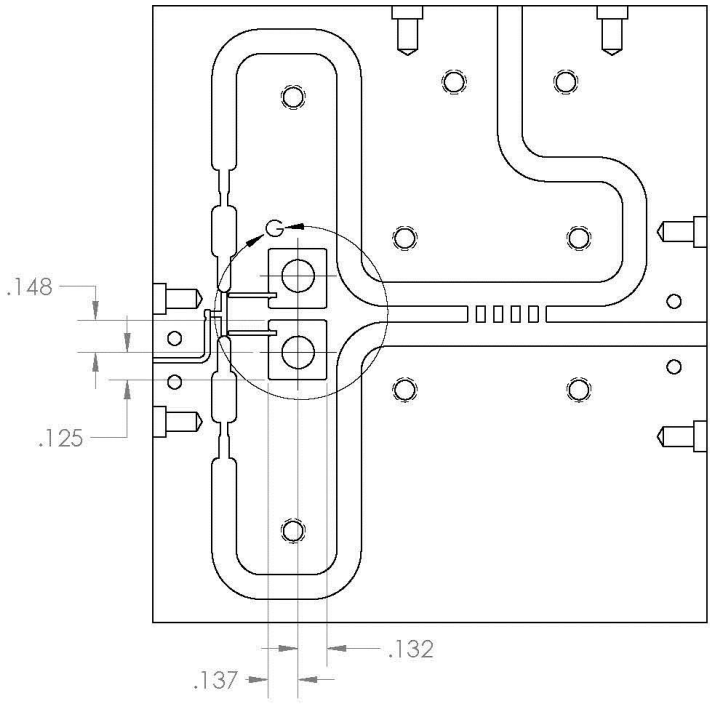


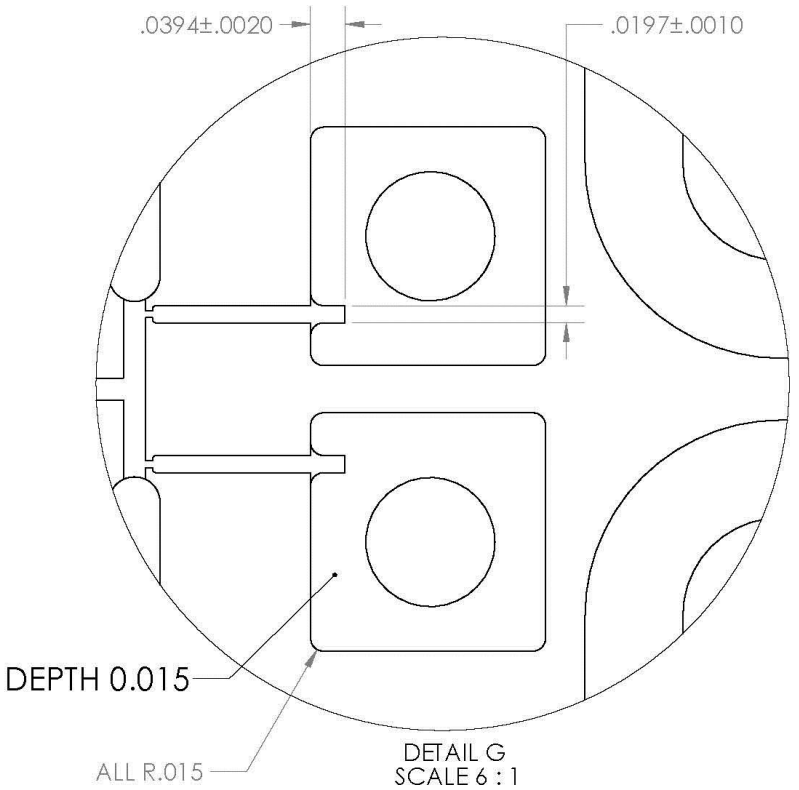
DETAIL F
SCALE 16 : 1


Flanges
SLIGHT PRESS FIT
DOWL PIN WAVEGUIDE
3X Ø .089 ↧ .200
4-40 UNC ↧ .200
⌴ Ø.140↧.060
Ø .067 ↧ .180
Ø.9375
Ø.9375
Ø.5625
Ø .064 ↧ .180
3X Ø .089 ↧ .200
4-40 UNC ↧ .200
⌴ Ø.140↧.060
SLIGHT PRESS FIT
DOWL PIN WAVEGUIDE


Base backside
Tolerance ±.009
unless otherwise noted
1.238
.350
.666
DEPTH .42
ALL .160
2X ∅.148±.001 THRU
.164-64 UNS-2B ↧.137±.001
ALL R.1400

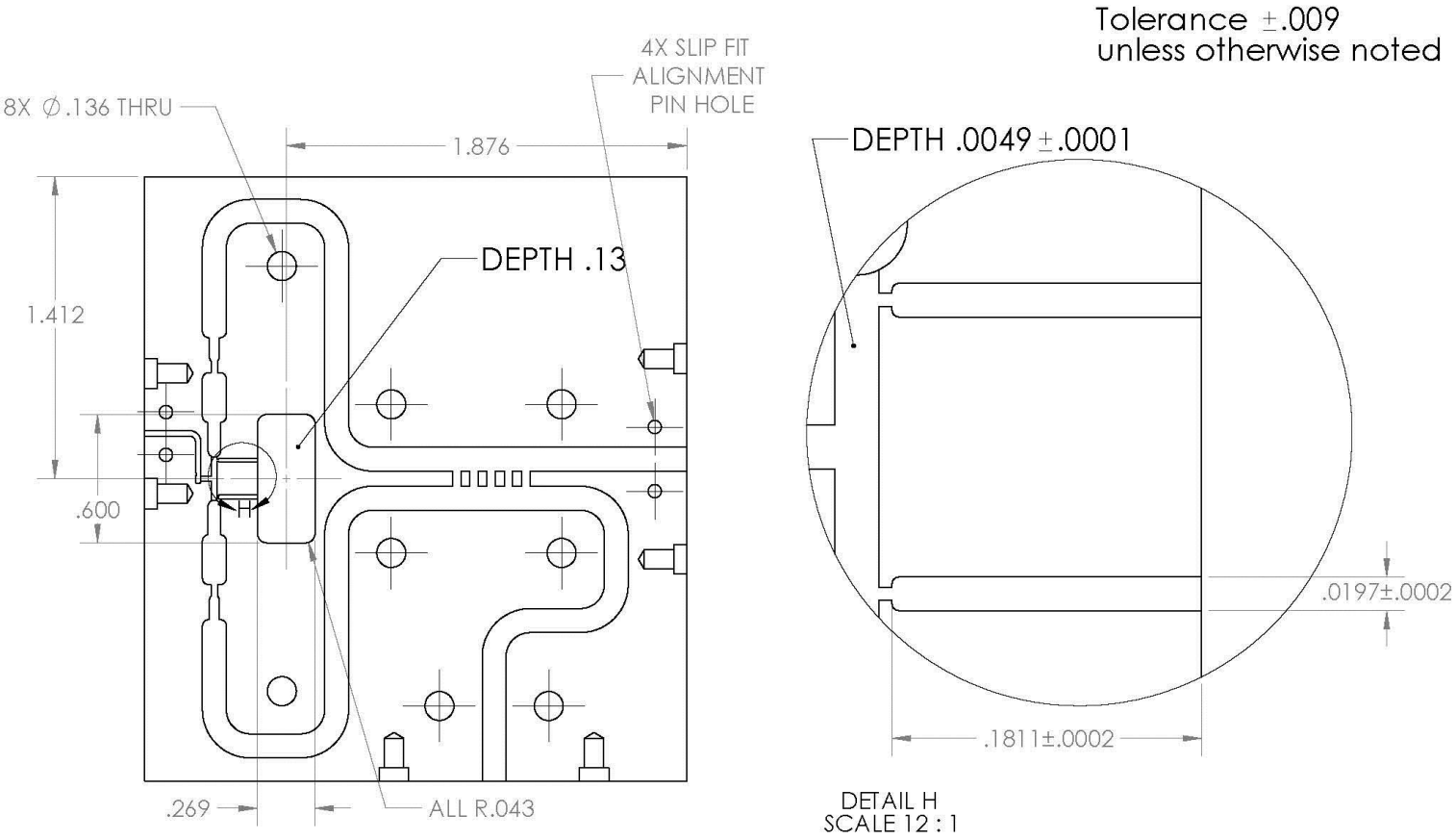
Base GPPO holes
Tolerance ±.009
unless otherwise noted





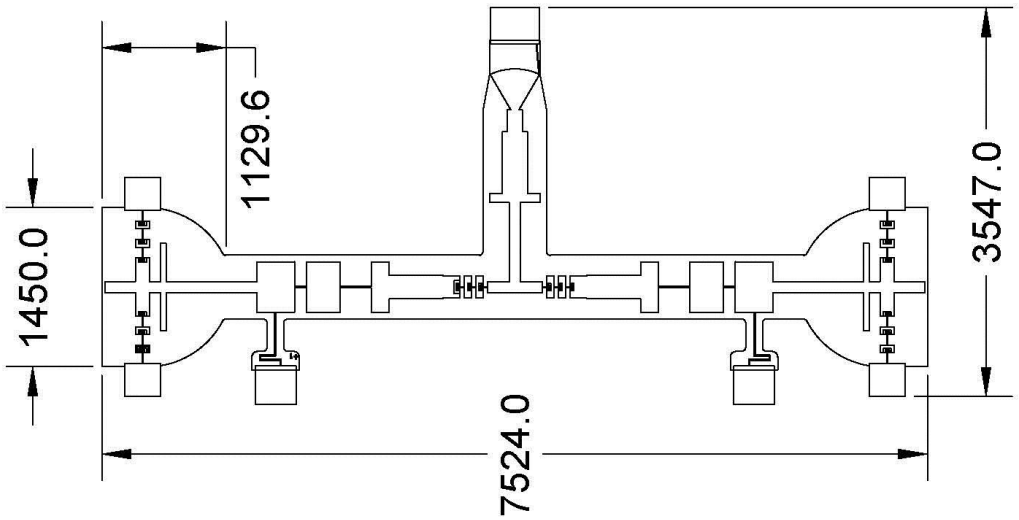
Quad cover is mirror symmetric to the base except for the following:

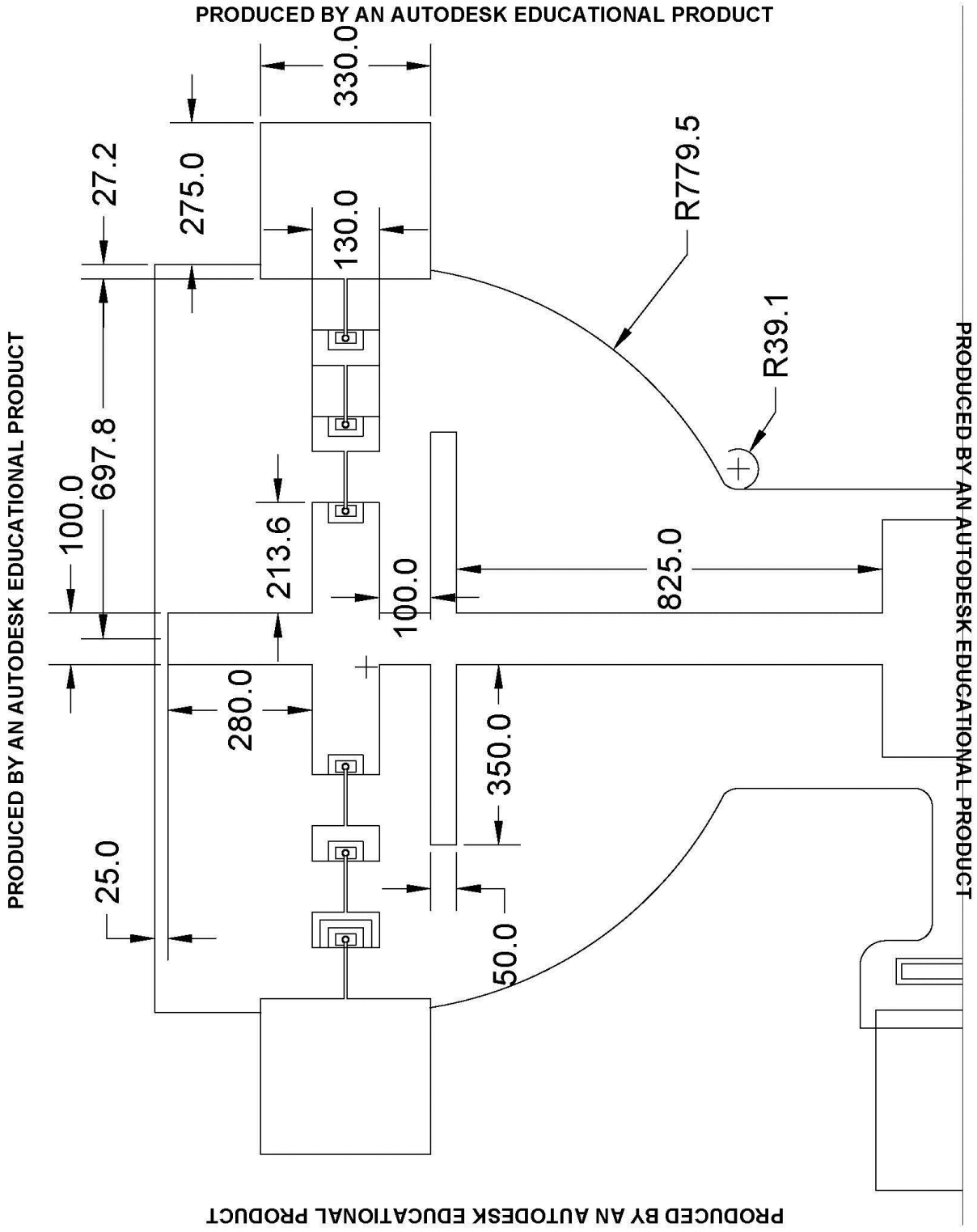
- #4-40 tapped holes on page 2 are replace with clearance holes
- GPPO holes on page 4 are removed
- channel depth on page 7 is changed from .0030±.0001 to .0049±.0001

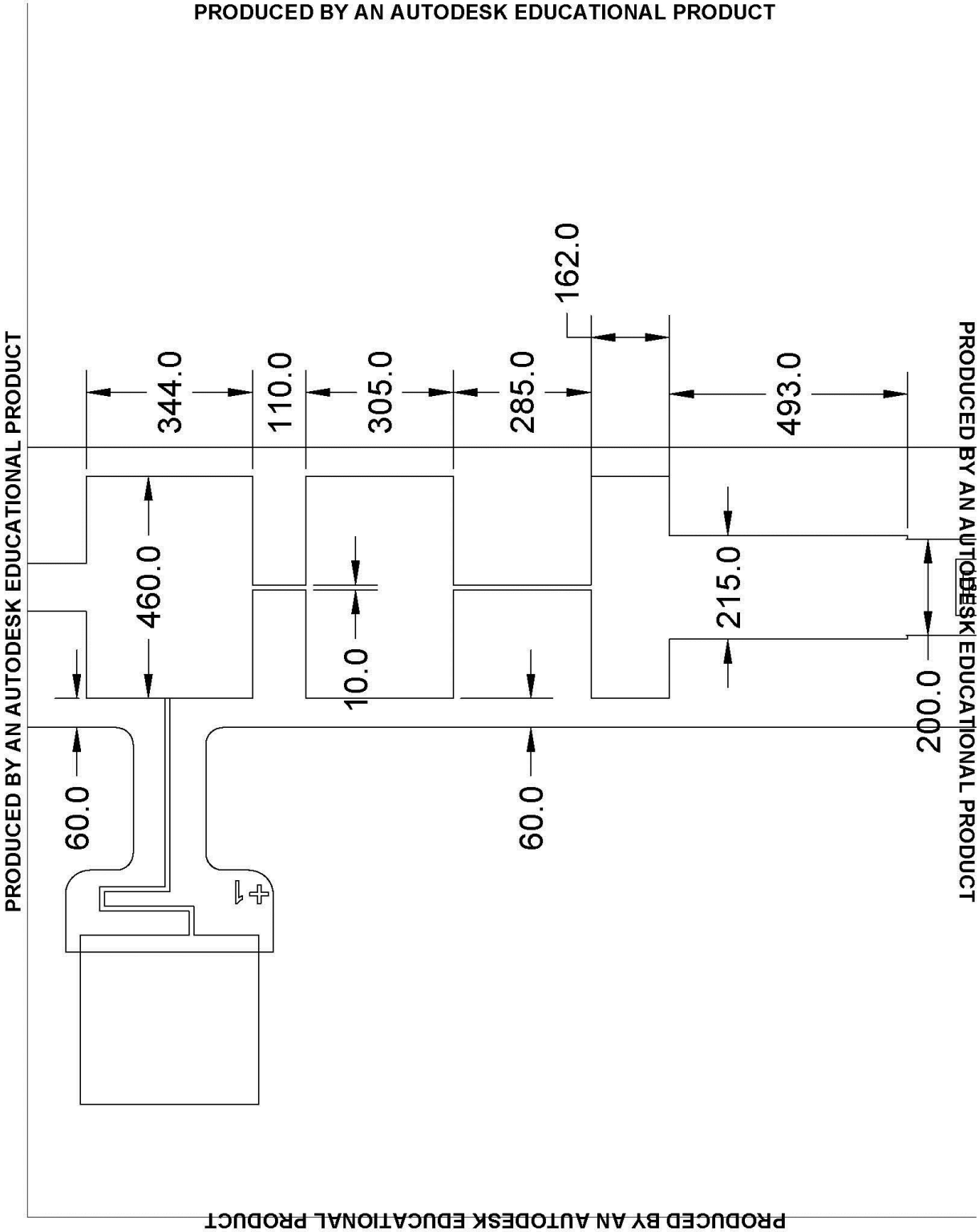


F. Quadrupler Circuit

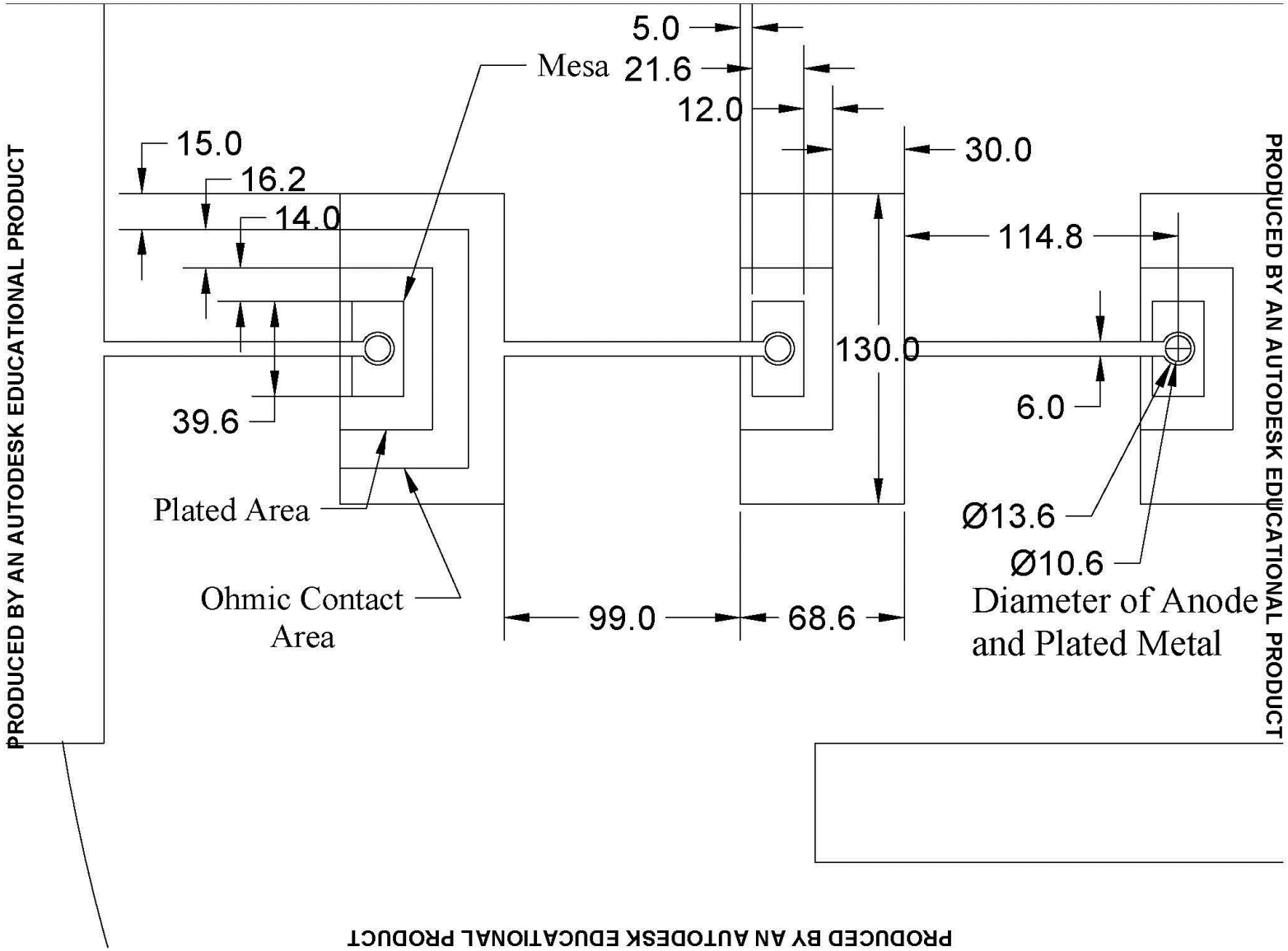
All dimensions
in microns

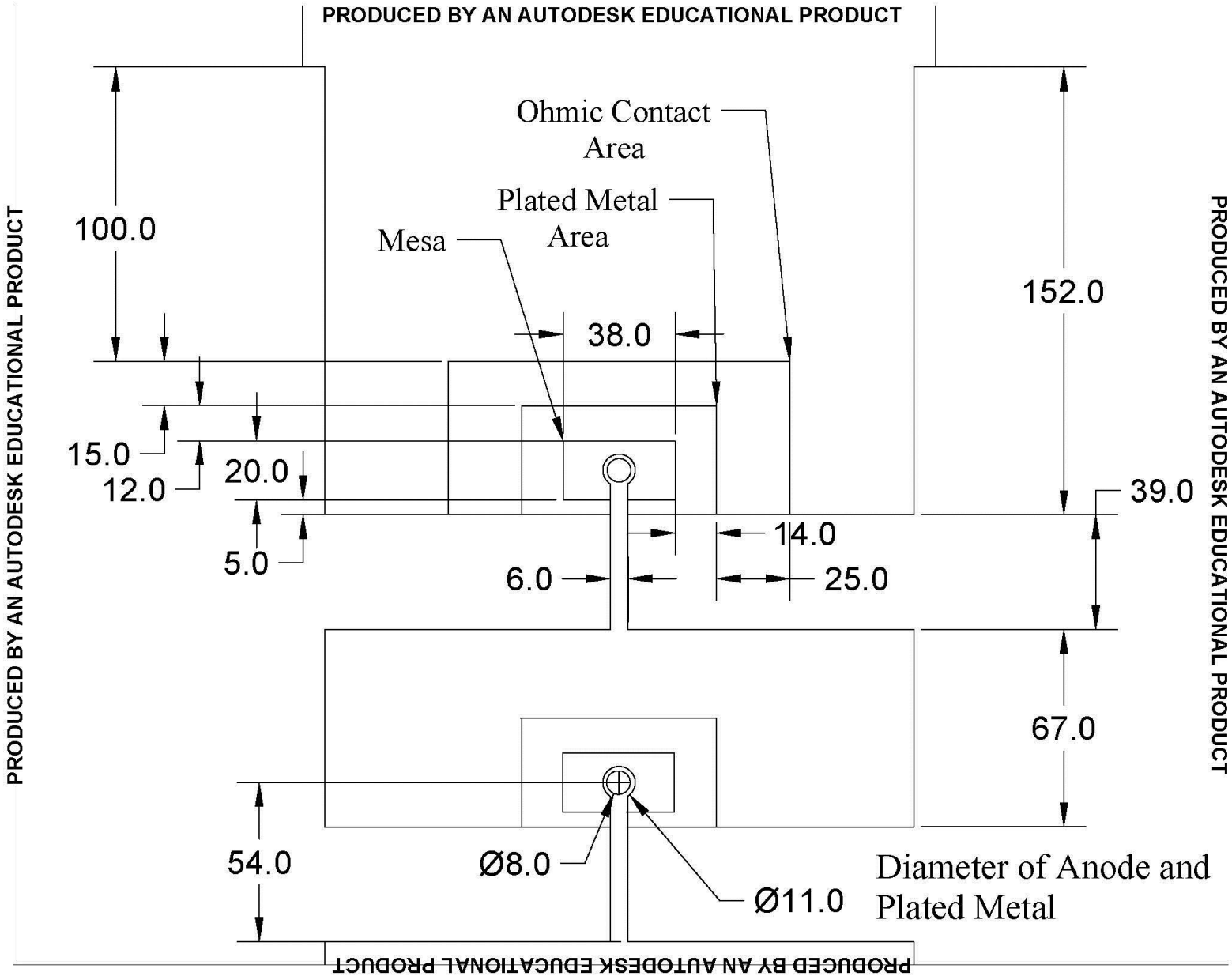



PRODUCED BY AN AUTODESK EDUCATIONAL PRODUCT
330.0
27.2
275.0
130.0
R779.5
R39.1
697.8
100.0
213.6
100.0
825.0
280.0
350.0
25.0
50.0
PRODUCED BY AN AUTODESK EDUCATIONAL PRODUCT
PRODUCED BY AN AUTODESK EDUCATIONAL PRODUCT
PRODUCED BY AN AUTODESK EDUCATIONAL PRODUCT

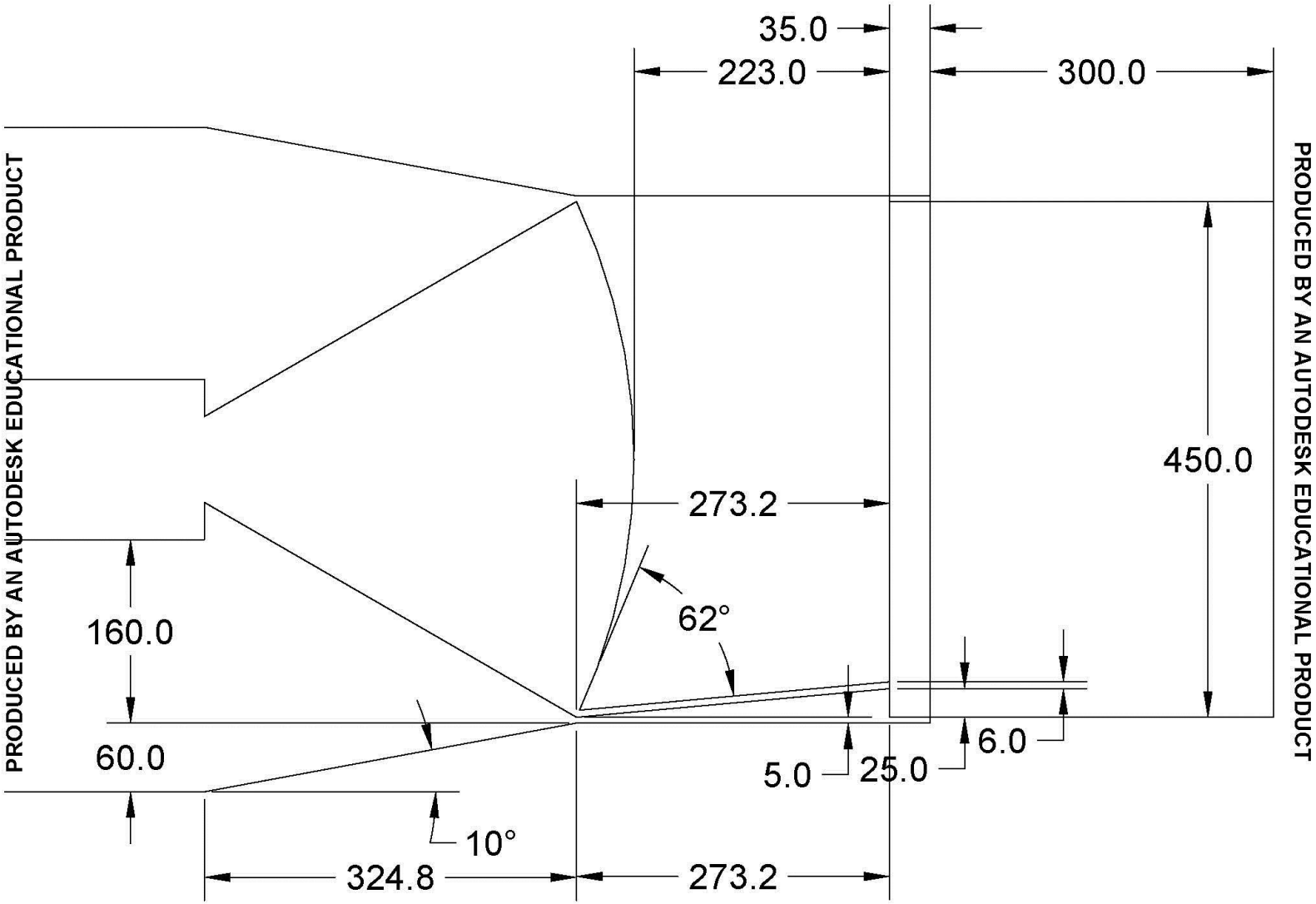

PRODUCED BY AN AUTODESK EDUCATIONAL PRODUCT
PRODUCED BY AN AUTODESK EDUCATIONAL PRODUCT
PRODUCED BY AN AUTODESK EDUCATIONAL PRODUCT
PRODUCED BY AN AUTODESK EDUCATIONAL PRODUCT
344.0
110.0
305.0
285.0
162.0
493.0
460.0
10.0
215.0
200.0
60.0
60.0

PRODUCED BY AN AUTODESK EDUCATIONAL PRODUCT
97.0
65.0
R35.0
10.0
390.0
50.0
165.0
70.0
135.0
R50.0
R35.0
50.0
50.0
35.0
PRODUCED BY AN AUTODESK EDUCATIONAL PRODUCT
PRODUCED BY AN AUTODESK EDUCATIONAL PRODUCT
PRODUCED BY AN AUTODESK EDUCATIONAL PRODUCT

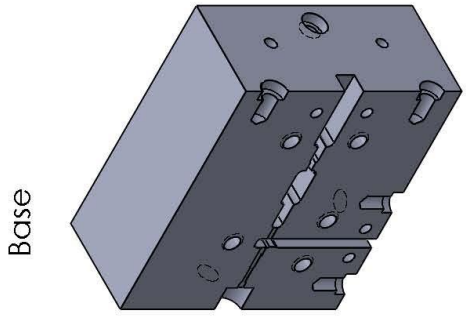


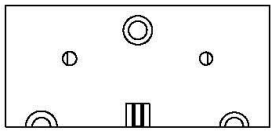


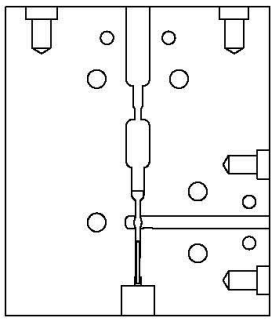
PRODUCED BY AN AUTODESK EDUCATIONAL PRODUCT
375.0
60°
200.0
75.0
140.0
60.0
230.0
561.0
83.0
R35.0
460.0
720.0
100.0
200.0
PRODUCED BY AN AUTODESK EDUCATIONAL PRODUCT
PRODUCED BY AN AUTODESK EDUCATIONAL PRODUCT
PRODUCED BY AN AUTODESK EDUCATIONAL PRODUCT

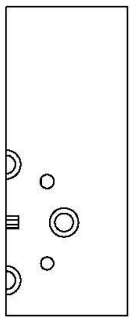


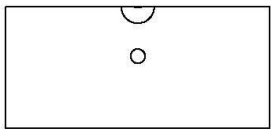
G. Doubler Waveguide Block





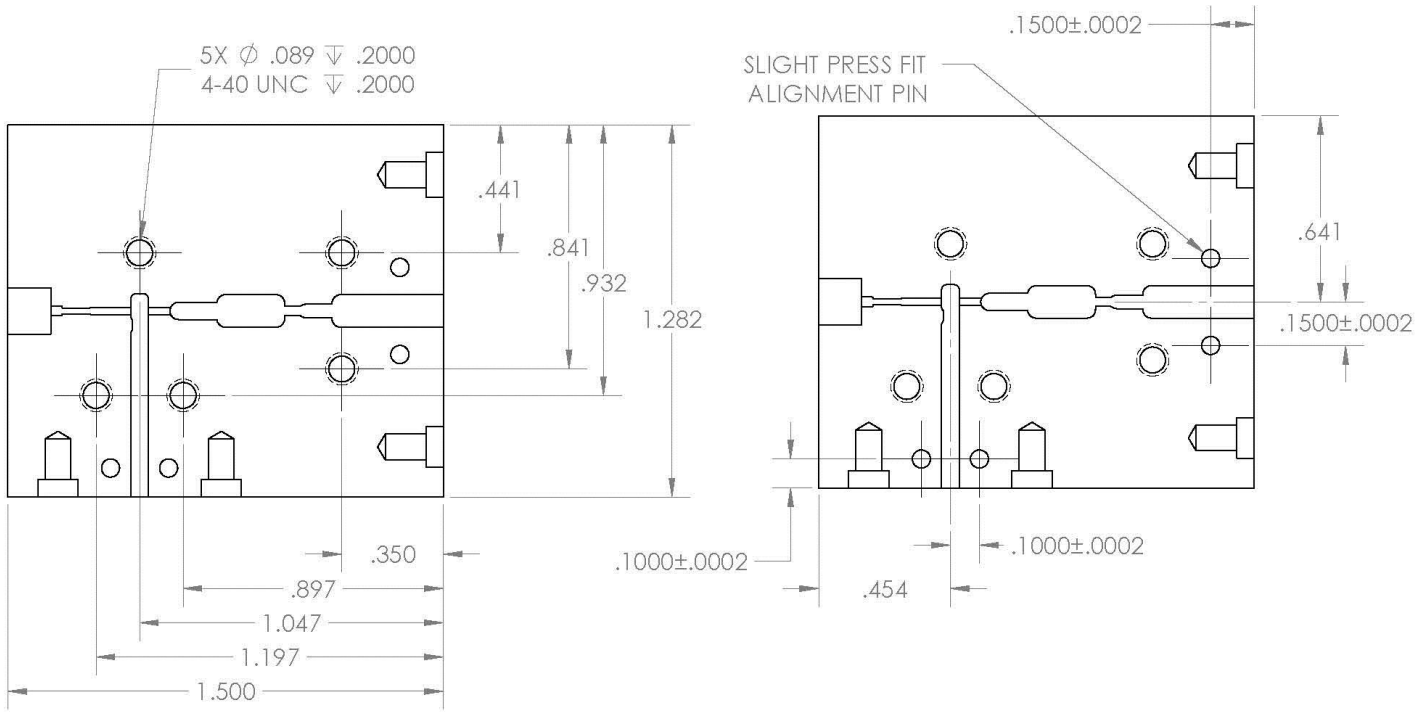






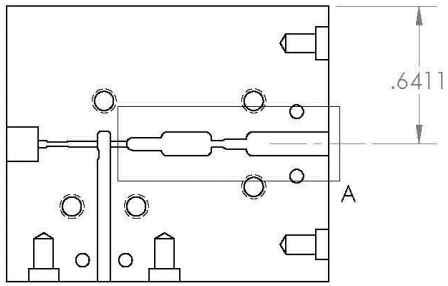
Base hole and pin locations
Tolerance ±.009
unless otherwise noted

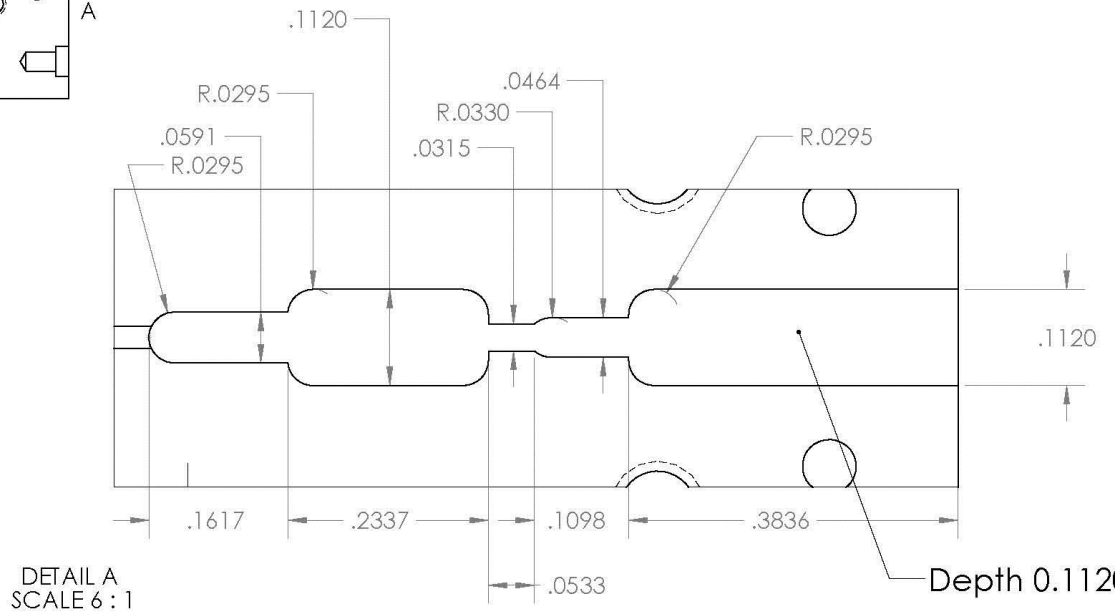
Same view left and right



Base WR22

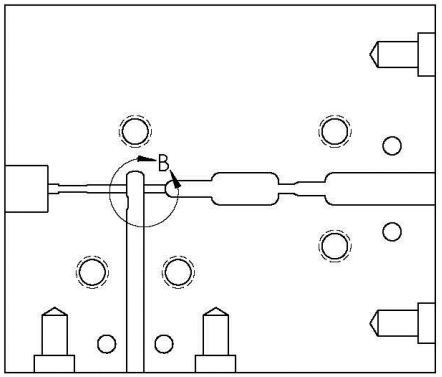
Tolerance ±.0005
unless otherwise noted

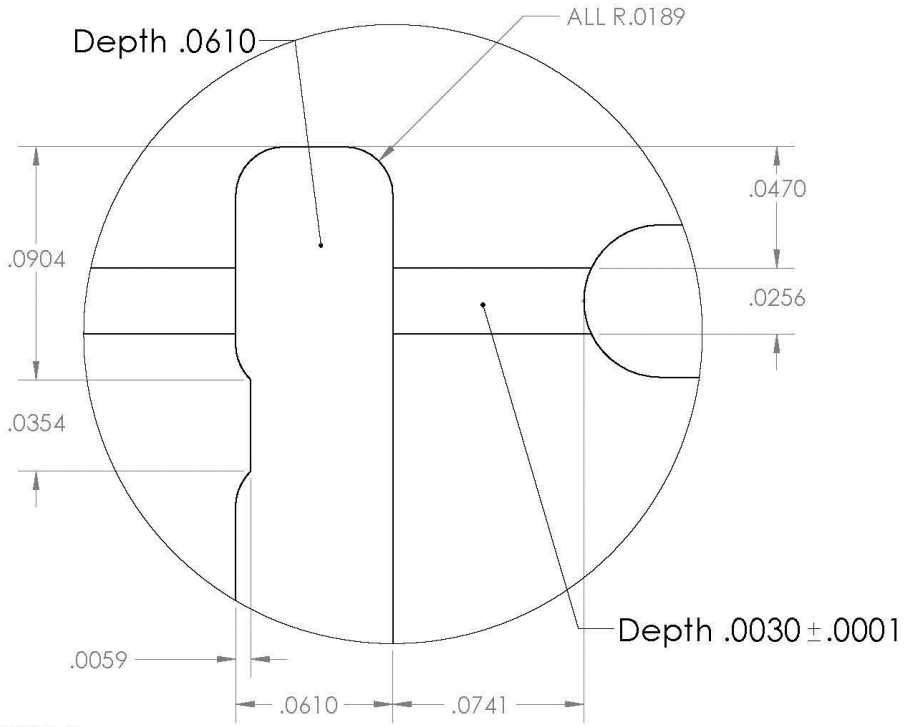




DETAIL A
SCALE 6 : 1

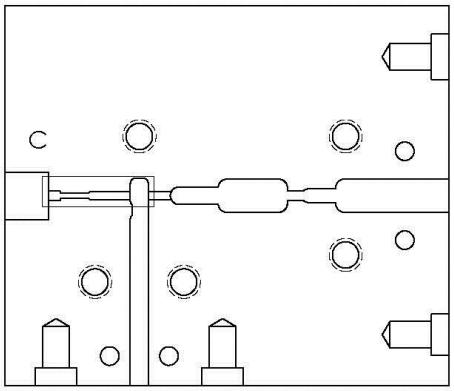
Base channel & WR12
Tolerance ±.0002
unless otherwise noted

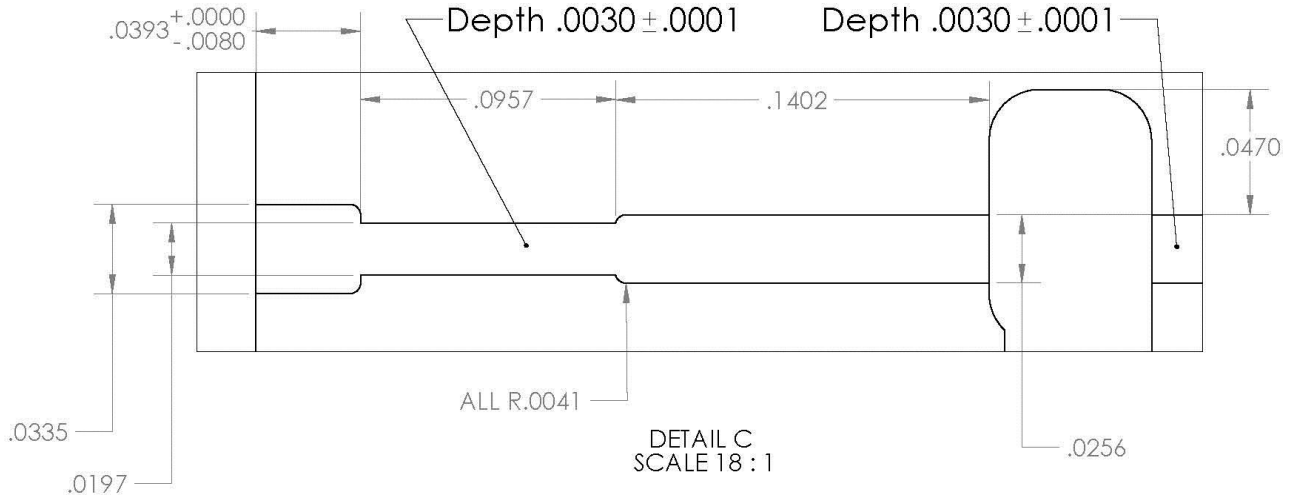




DETAIL B
SCALE 18 : 1

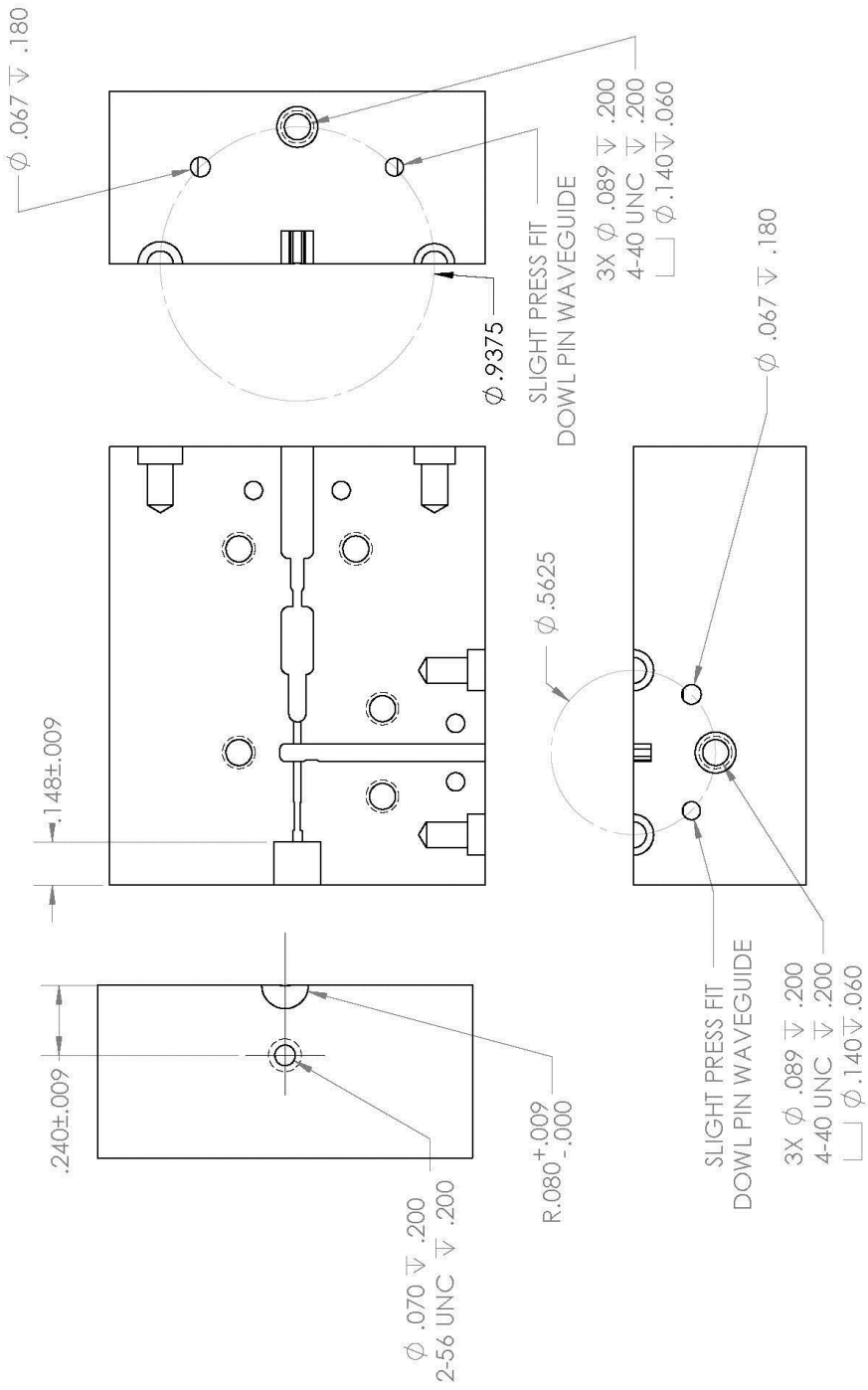
Base DC bias
Tolerance ±.0002
unless otherwise noted

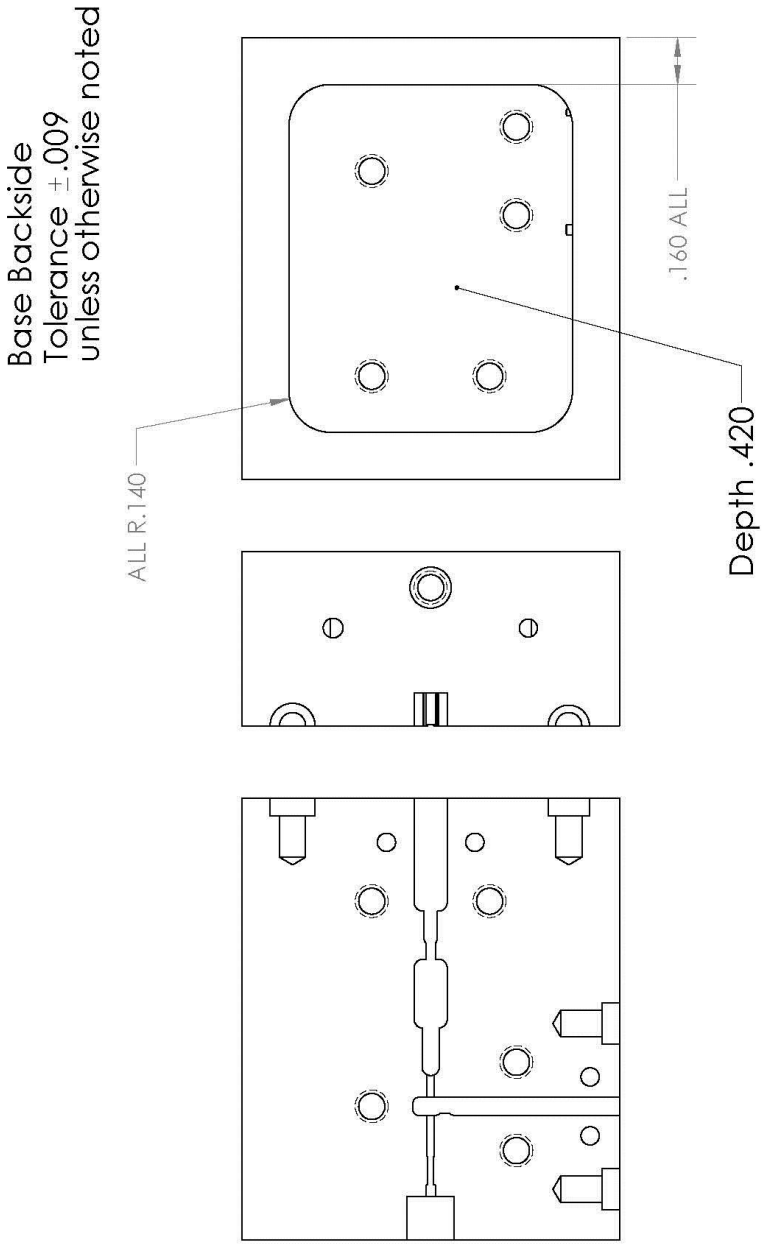




DETAIL C
SCALE 18 : 1

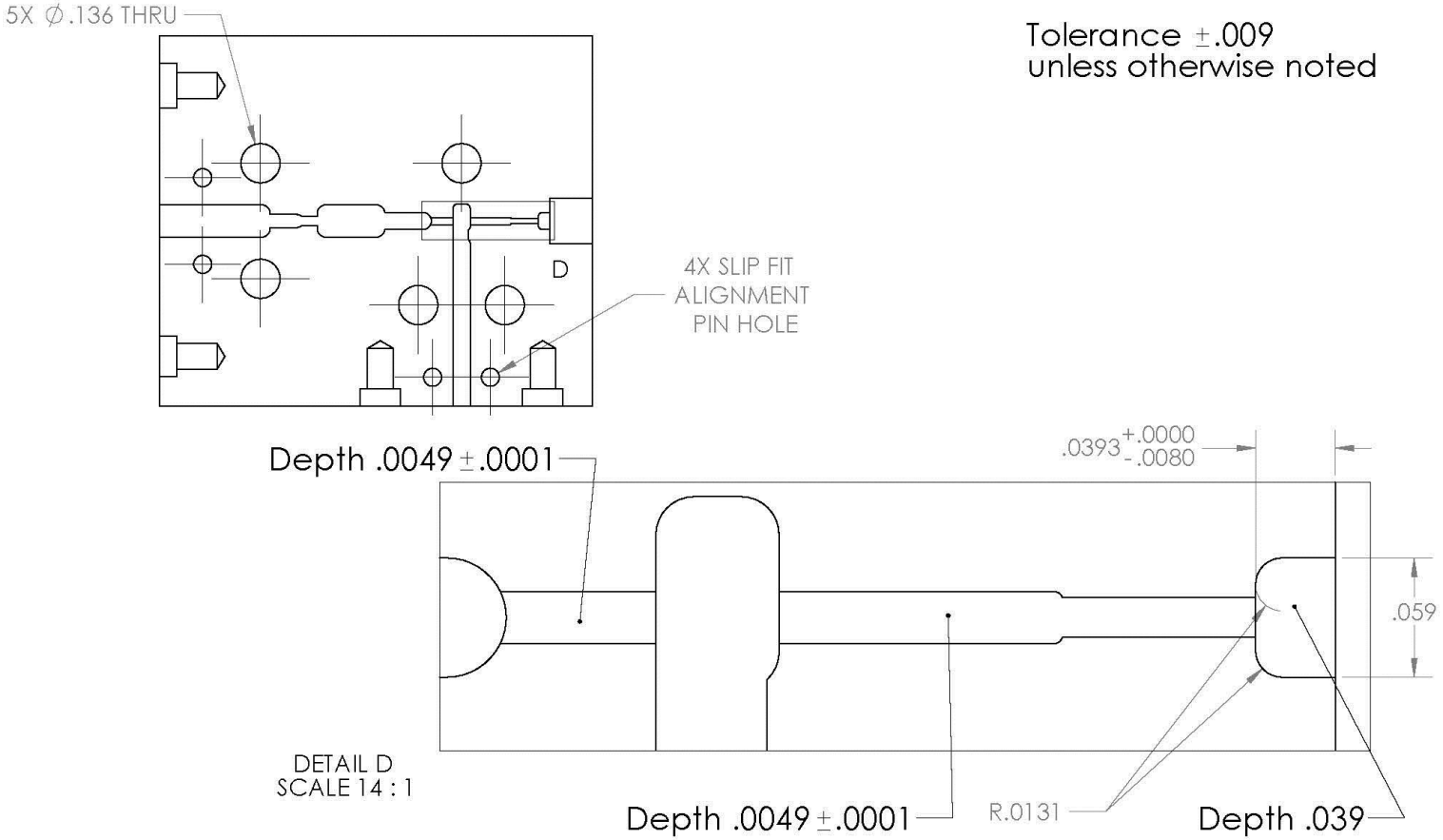
Flanges


⌀ .067 ⩛ .180
⌀.9375
SLIGHT PRESS FIT
DOWL PIN WAVEGUIDE
3X ⌀ .089 ⩛ .200
4-40 UNC ⩛ .200
⌴ ⌀.140⩛.060
.148±.009
⌀.5625
⌀ .067 ⩛ .180
.240±.009
⌀ .070 ⩛ .200
2-56 UNC ⩛ .200
R.080+.009 -.000
SLIGHT PRESS FIT
DOWL PIN WAVEGUIDE
3X ⌀ .089 ⩛ .200
4-40 UNC ⩛ .200
⌴ ⌀.140⩛.060


Base Backside
Tolerance ±.009
unless otherwise noted
ALL R.140
.160 ALL
Depth .420

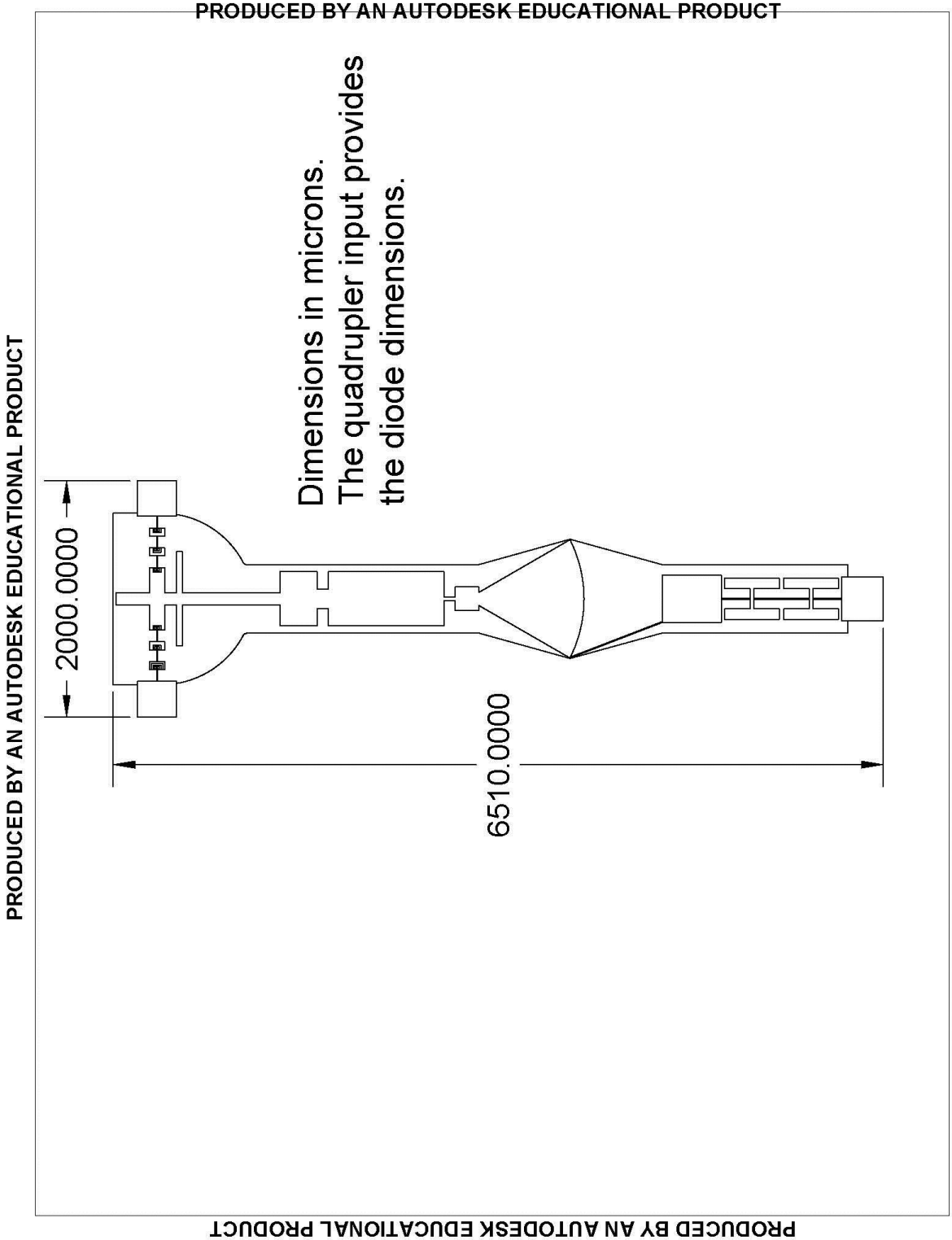
Doubler cover is mirror symmetric to the base except for the following:

- #4-40 screw holes on page 2 are replace with #4 through holes
- Channel depths shown on pages 4 & 5 are different



C+T

H. Doubler Circuit



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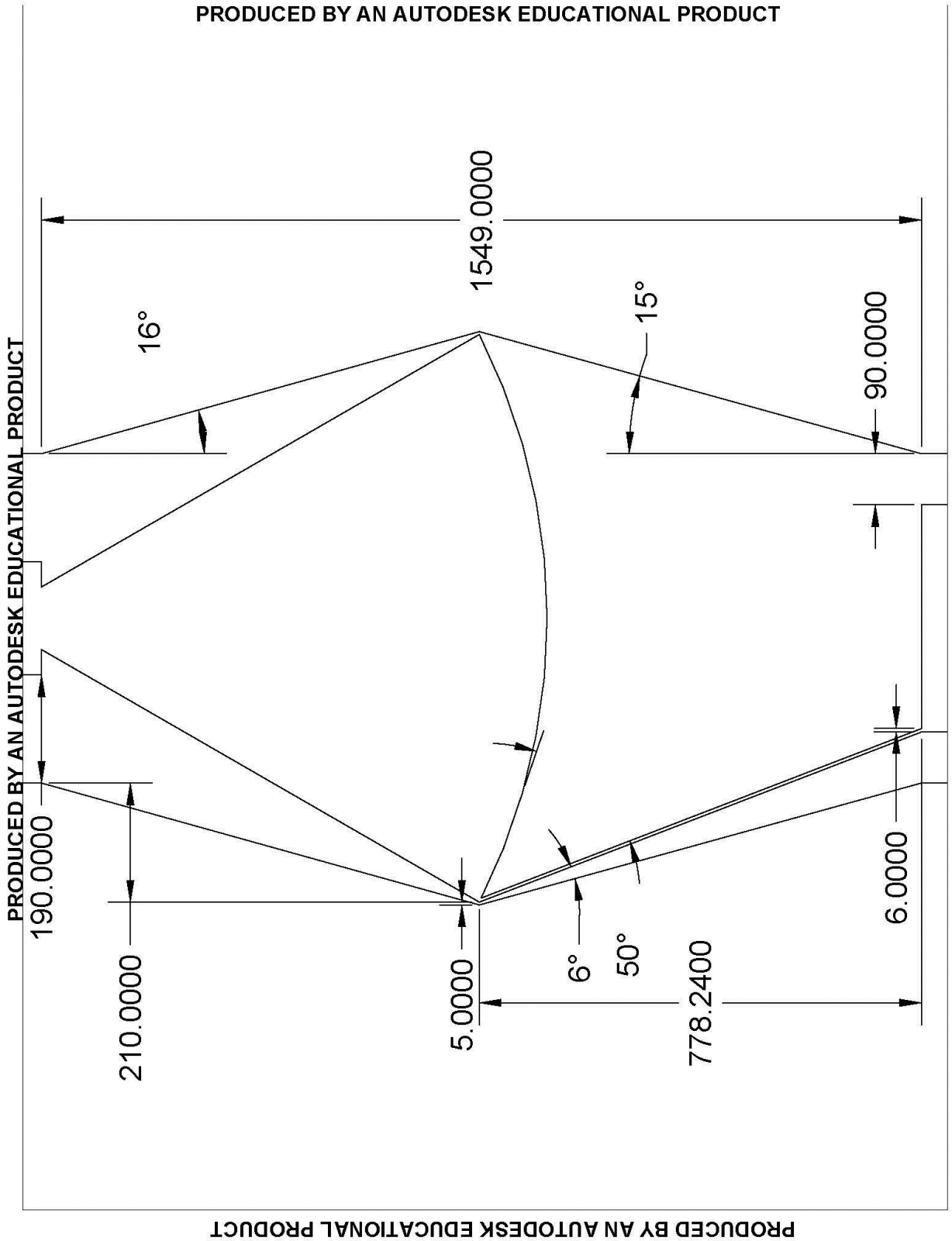
100.0000
460.0000
167.0000
460.0000
60.0000
30.0000
200.0000
890.0000
60°
313.0000
96.0000
976.0000
96.0000
200.0000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1549.0000
16°
15°
90.0000
190.0000
210.0000
5.0000
6°
50°
778.2400
6.0000

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90.0000
400.0000
10.0000
245.0000
30.0000
90.0000
80.0000
105.0000
370.0000
500.0000
30.0000
460.0000
40.0000
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