Fabrication Advancements and Characterization of Heterogeneously Integrated Gallium Arsenide Schottky Diodes and Circuits

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UVA

Thanks to my community for your support.

This Dissertation is submitted in partial fulfillment of the Doctor of Philosophy degree requirements.

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Chapter 1- Introduction

Abstract

This thesis presents an optimized fabrication process for heterogeneously integrated quasi-vertical gallium arsenide (GaAs) Schottky diodes (QVDs), building on prior work in our research group utilizing silicon micromachining. The process is tailored for compact membrane-based circuits, featuring closely spaced diodes with gold-plated, side-coated vias and freestanding 3-μm thick gold beam leads. The process has been optimized for <2 μm feature tolerance, minimizing or eliminating unwanted etch effects, such as undercutting, residue, and reduced processing time. One of these new approaches includes diffusion bonding, which achieves a metal-to-metal interface and enables integration onto silicon for enhanced thermal handling. The diffusion-bonded QVDs exhibit comparable electrical performance and superior thermal dissipation compared to previously fabricated adhesive-bonded diodes. Collaborative work with Virginia Diodes yielded membrane-based multiplier chip designs, where frequency doublers fabricated using the above-mentioned QVD process advancements were tested against lateral (planar) diode designs. The QVD offers potential advantages over the lateral/planar diode due to its geometry, including reduced parasitics, lower series resistance, and improved thermal handling.

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1.1 Introduction

Devices that operate in submillimeter-wave bands (100 GHz to 1 THz) and higher THz bands present unique engineering opportunities to investigate natural phenomena and produce high-capacity, short-range communication systems. This region is part of the electromagnetic spectrum between the microwave and optical domains. The size of the wavelengths of these signals, especially when using relatively high dielectric substrates such as silicon ($\varepsilon_R \approx 11.7$) are small and quarter-wavelengths ($\lambda_g \approx \frac{\lambda_0}{\sqrt{\varepsilon_R}}$), a typical size of an impedance-matching element is on the order of 50 microns (μm) near 500 GHz. This necessitates thin, narrow, short transmission lines, resulting in small circuits. These small circuits require non-linear and electromagnetic design in complex engineering software. The difficulty in realizing small circuits is compounded by the relatively scarce availability of solid-state devices, i.e., you can't order 200+ GHz components from large-scale distributors such as Digikey or Mouser. Historically, devices and circuits operating in this regime are made by specialized manufacturers, universities, and national laboratories.

A variety of technologies exist for high-frequency sources, frequency multipliers, mixers, and detectors. The following sections provide a brief overview of some of these technologies; however, a detailed review of the state-of-the-art capabilities of each is beyond the scope of this discussion.

For low-noise applications in this regime, cryogenic devices are optimal, such as Low Noise Amplifiers (LNAs), superconductor-insulator-superconductor (SIS), hot electron

bolometers (HEBs), and most recently, superconducting traveling wave parametric amplifiers [1-5]. Vacuum tube technology, such as gyrotrons, klystrons, and backward wave oscillators, is available for high-power sources in these frequency ranges. Recent research and development have seen these vacuum tube technologies miniaturize significantly, which is particularly interesting to those interested in high power; however, they aren't very efficient [6][7]. Low-power sources are also available through solid-state devices such as Resonant Tunneling Diodes (RTD), Transferred-Electron Devices (TED) also known as Gunn Diodes, Transit Time Diodes (TDD) such as the Impact Ionization Avalanche Transit Time (IMPATT) device. These devices can be low noise, stable, compact, and rugged, though relatively limited in output power [7].

Laser-pumped photodiodes have demonstrated steady progress in operating frequency, providing highly stable sources exceeding 300 GHz. However, their output power remains constrained in the submillimeter-wave band and beyond. The required laser power also produces lower system efficiency, making them less suitable for compact, power-constrained applications. Despite these limitations, advancements in photonic-based electronics and compact laser systems continue to enhance their capabilities, warranting careful evaluation for high-frequency applications [8][9][10].

Transistors, such as the high-electron-mobility transistor (HEMT), Hetro-junction Bipolar transistor, and the Pseudomorphic HEMT (PHEMT), have also seen significantly increased operating frequency past 1 THz [12][13][14]. The output power of transistor technology exceeds 30 dBm at 100 GHz, though it rapidly decreases in output power as it approaches 1 THz. [13]

While these technologies can produce signals in the high-frequency spectrum, there are several advantages to the Schottky diodes realized with high electron mobility materials such as GaAs. The Schottky diode is a majority carrier device with minimum charge storage, enabling extremely fast switching speeds and making them ideal for high-speed rectification, detection, and frequency multiplication and mixing. The Schottky diode has a relatively small junction capacitance that scales with the anode size, enabling efficient and relatively easy use at extremely high frequencies, upwards of 5 THz [15].

This research focuses on optimizing the quasi-vertical (QVD) Schottky diode for high-frequency applications, as the Schottky diode remains a robust, enduring technology that is unlikely to be replaced anytime soon. This work aims to characterize devices fabricated with several process advancements, propose further improvements to the fabrication process, and evaluate the performance of devices and circuits created using these enhanced methods.

1.2 Background

Schottky diodes are semiconductor devices based on a metal-semiconductor junction. Karl Ferdinand Braun first studied metal-semiconductor interactions in 1874, and in 1937, Walter H. Schottky identified a potential barrier from stable space charges within the semiconductor, now known as the Schottky barrier [16][17]. Since then, Schottky diodes have been widely used in microwave technologies, notably for radio-frequency detection. As early as

1904, Jagadis C. Bose used these diodes for millimeter-wave detection [18][19]. Today, they are crucial non-linear components in frequency conversion for THz heterodyne receivers.

In 1965, Young and Irvin, at Bell Telephone Laboratories in Murray Hill, NJ, USA, introduced the first photo-fabricated "honeycomb" diode [20]. This replaced the unreliable "cat-whisker" contact with an array of small, metal-semiconductor junctions with low parasitic capacitance, precise areas, and protected epitaxial interfaces. In October 1970, Bob Mattauch and his student Tom Viola developed their first functional diode, featuring 8-micron diameter anodes, based on work at Bell Labs. This diode demonstrated superior performance as a mixer in frequencies below 50 GHz [21]. By the late 1970s, GaAs Schottky diodes were advancing astronomical and spectroscopic receivers into the submillimeter-wave range [21-24]. While other groups, like Gerry Wrixon's at University College Cork, were producing THz diodes, Mattauch's diodes remained dominant in millimeter-wave receivers [21] [25][26]. In the early 1980s, JPL sought Mattauch's diodes for an Earth-observing instrument to study ozone depletion linked to chlorofluorocarbons [21]. These space-qualified diodes were launched in 1991 [21][27].

In the early 1980s, Bob Mattauch's Semiconductor Device Laboratory at the University of Virginia came under the direction of his former student, Tom Crowe. In 1985, Crowe, Bill Bishop, and Mattauch developed a geometry and lithography technique that transformed the whisker contact into a free-hanging metal air bridge, achieved by a final surface channel etching step to remove the GaAs substrate below the metal contact finger [21]. Later, in 1996, Crowe founded Virginia Diodes Inc. (VDI) in Charlottesville, VA. Initially, VDI focused on Schottky diodes for scientific applications like radio astronomy and high-frequency radar. By 2001, VDI

expanded into downtown Charlottesville and began selling complete mixer, detector, and multiplier products for 50–1000 GHz. In 2004, VDI further broadened its offerings to include THz Transmitter & Receiver modules [28]. Another significant contributor to the field of the Schottky diode worth noting is the work from Chalmers University, which has made significant advancements to the development of the GaAs Schottky Diode [29] [30].

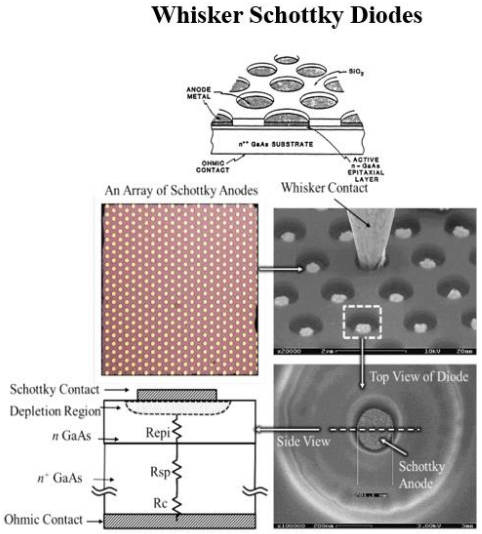


Figure 1 - Examples of the Honeycomb whisker Contact Diode [31]

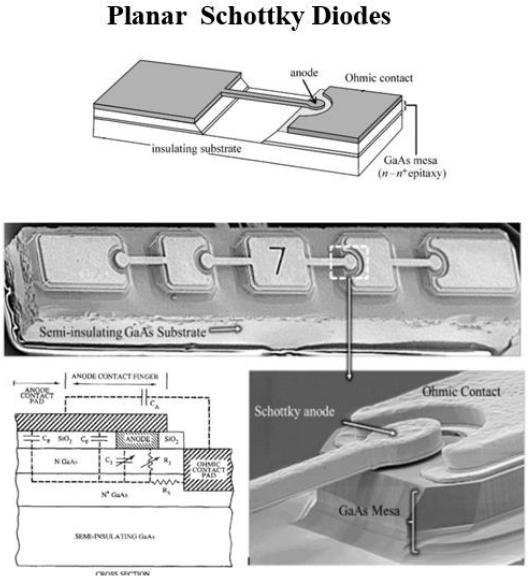


Figure 2 - Example of the Lateral Planer Diode [31]

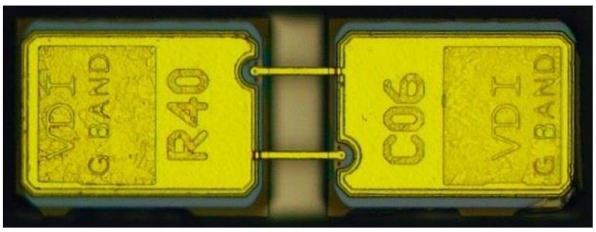


Figure 3 - Photograph of VDI Antiparrel Schottky Diodes [28]

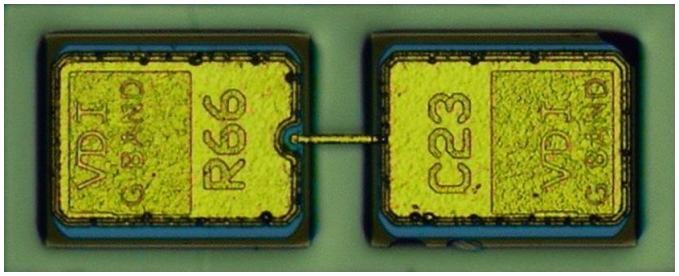


Figure 4 - Photograph of VDI Single Diode [28]

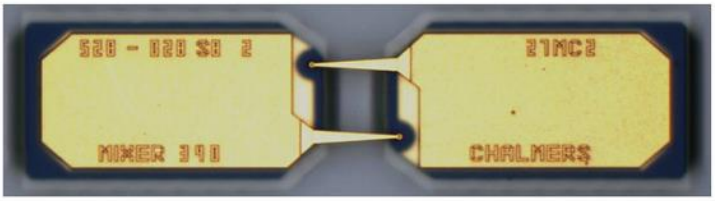


Figure 5 – Photograph of Chalmers Antiparrel Schottky Diodes[30]

Figure 6– Photograph of Chalmers AntiSeries Schottky Diodes [30]

In 1993, A. Simon presented a paper at the Fourth International Symposium on Space Terahertz Technology titled "Planar THz Schottky Diode Based on a Quasi-Vertical Diode Structure." This work introduced a novel approach to designing planar Schottky diodes for THz frequencies, denoted as the quasi-vertical structure [32]. The images below show this new structure.

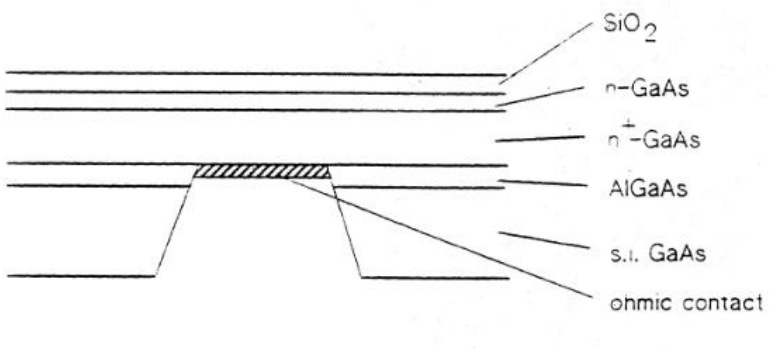


Figure 7 – Layers of Simon's Quasi-Vertical Diode [32]

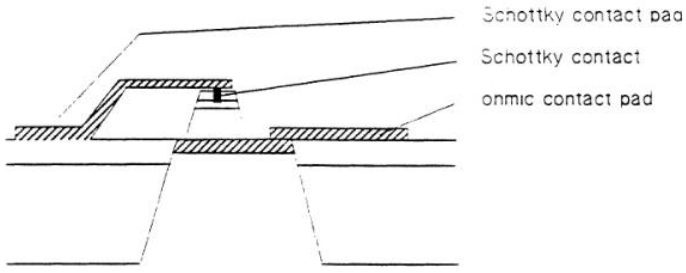


Figure 8 – Side Profile drawing of Simon's Quasi-Vertical Diode [32]

In 2005, Oleg Cojocari, while pursuing his PhD at the University of Moldova, published a paper on a quasi-vertical n-type GaAs Schottky diode designed to enhance the performance of high-frequency Schottky diodes. This improvement addressed the limitations of planar/lateral diodes, including parasitic capacitance, series resistance, and thermal challenges. These undesirable effects were attributed to the Schottky and Ohmic contacts being situated on the same plane, leading to current crowding. Current crowding was hypothesized to result in high current densities, which significantly elevated the electron temperature beyond their thermal energy, thereby generating excess noise in the device. Cojocari proposed that the quasi-vertical structure could mitigate these effects by maintaining an even field distribution across the entire anode area. This design would reduce current crowding and offer lower series resistance and capacitance compared to lateral diodes [33].

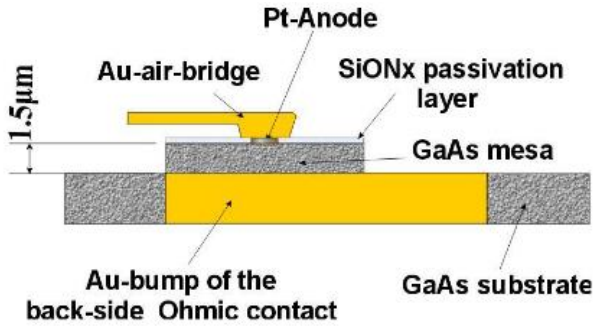


Figure 9 - Side Profile drawing of Cojocari's Quasi-Vertical Diode [32]

In 2006, Cojocari co-founded ACST GmbH, in Hanau, Germany, which became the first European commercial supplier of Schottky diodes for THz applications. ACST originated as a spin-off from the Technische Universität Darmstadt (TUD); ACST leveraged over two decades of research and development in THz technology to establish itself as a leading European supplier of Schottky diodes for mm-wave and THz applications [34].

The research conducted by these researchers (noted above) on terahertz diodes laid the groundwork for advancements in terahertz electronics. At that time, engineers developing semiconductor devices for high frequencies lacked the tools to accurately measure and characterize device performance. The standard testing method involved mounting ultra-thin chips, comparable in thickness to a human hair, into a fixture with connectors and instruments. This setup tested the semiconductor and often introduced interference from additional wiring and interfaces, which complicated the results. To address this issue, Weikle, Lichtenberger, and Barker engineered a specialized probe and used it to measure the first THz transistor in

collaboration with Northrup Grumman in 2010.[35] Shortly afterwards, in 2011, they founded Dominion MicroProbes, which is the sole provider of dual-band on-wafer probes and the Twave probe. These probes can measure DC-1.2 THz on wafer signals and are actively pursuing efforts to extend this range and capabilities [36].

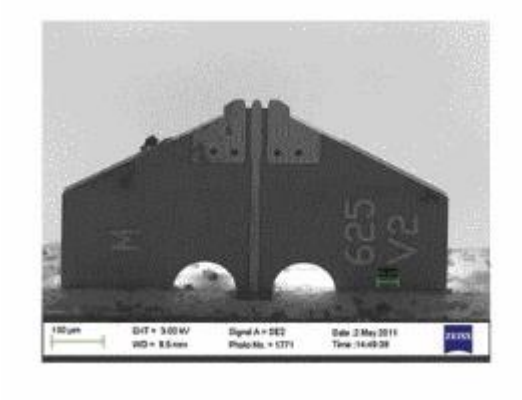


Figure 10 - Example of DMPI Silicon Probe [36]

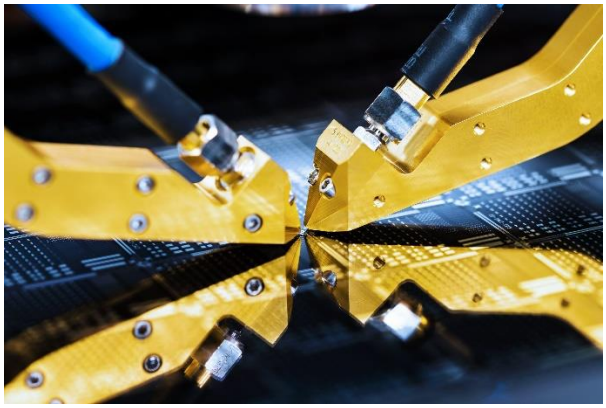


Figure 11- Example of a two-port measurement being taken with DMPI's on wafer probes [36]

The fabrication process used to make the probe required a unique dual-side (front and backside) process, including several wafer bonding steps. While these probes were being prototyped, Weikle's group pursued research on a new diode structure based on the reported quasi-vertical structures. The new processing advancements for the probe enabled new ideas and possibilities for processing with wafer bonding on thing substrates. In 2014, Alijarbarri published "Design and Characterization of Integrated Submillimeter-Wave Quasi-Vertical Schottky Diodes." This work introduced a vertically oriented Schottky diode design with an ohmic contact directly below the anode that was heterogeneously integrated into silicon. The diode is fabricated through backside processing and bonding the epitaxial layer to a high-resistivity silicon substrate, which supports the diode and its circuitry. The extracted circuit parameters aligned with the fundamental Schottky barrier theory, showing series resistance and capacitance, were comparable to the prior art.

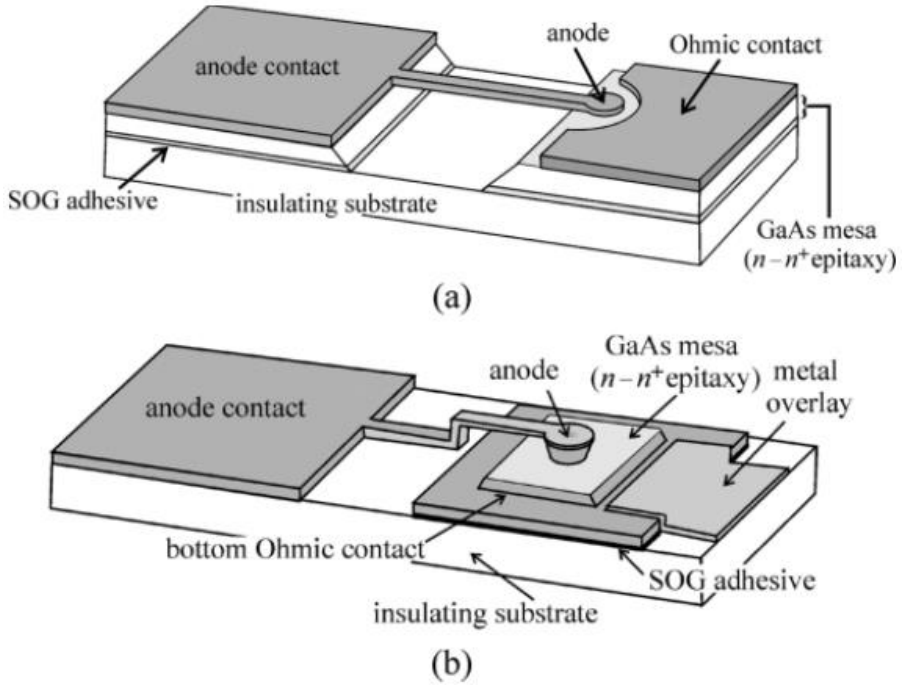


Figure 12 - Example of heterogeneously integrated Diodes (a) Lateral Diode (b) Quasi-Vertical [31]

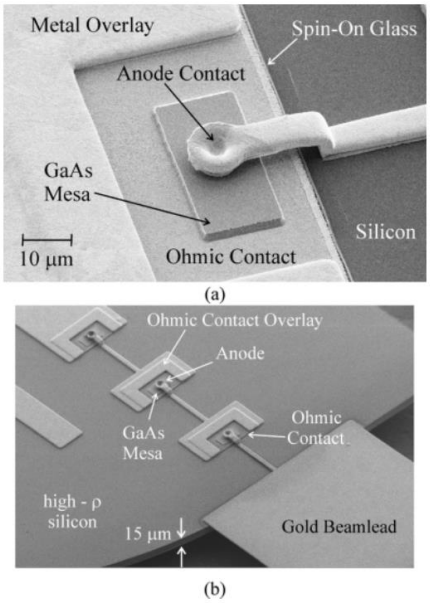


Figure 13 - Scanning Electron Microscope Images of Alijarbarri Diodes

As described above, the heterogeneous integration of these diodes onto silicon enabled highly integrated circuits, and to demonstrate this, Alijarbarri developed a fully-integrated 160 GHz frequency monolithic quadrupler, shown in Figure 14.

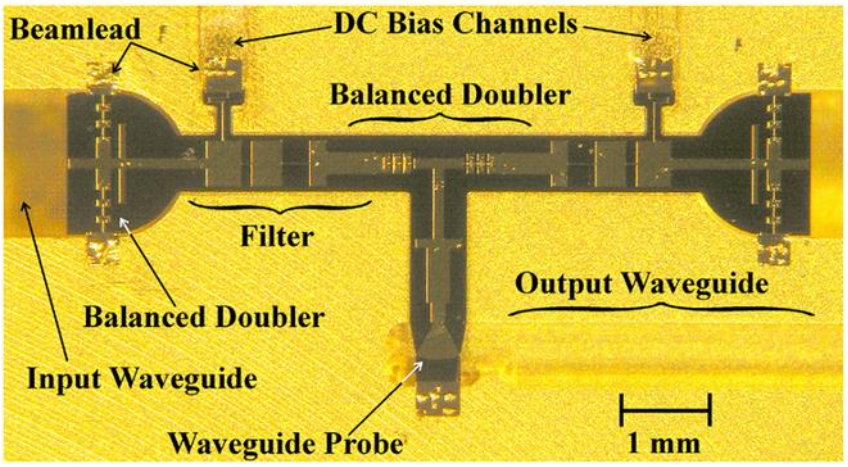


Figure 14 – 160GHz Quadupler made by Naser Alijarbari and Matthew Bawens

Following this demonstration, research focused on optimizing these diodes, redesigning the epitaxy and process to enable low-temperature processing. This work included developing highly integrated arrays and integrating the diodes on the probe [37][38]. The work also focused on characterizing the performance of these diodes, extracting parasitics, verifying cryogenic performance, and conducting rigorous thermal analysis, further supporting the hypothesis that quasi-vertical diodes may exhibit advantages compared to lateral diodes.

Today, DMPI, ACST, and Virginia Diodes are highly successful companies that have made significant advancements in their respective technologies.

1.3 Contrasting the various high-frequency diode technology

Whisker Diode

A whisker diode uses a fine wire (whisker) contact that lightly touches the semiconductor surface, forming the Schottky junction.

Advantages:

- **Low Parasitic Capacitance**: The whisker configuration provides extremely low parasitic capacitance, improving high-frequency performance.
- **Adjustable Configuration**: The whisker's positioning can be adjusted to optimize coupling, offering some flexibility.
- **Simple Fabrication**: Compared to planar diodes, the whisker diode is relatively simple to fabricate.

Challenges:

- **Fragility**: The whisker contact is delicate and prone to damage.
- **Reproducibility and Reliability**: Whisker contacts can be inconsistent and may lack long-term reliability.
- **Integration Limitations**: Integrating multiple whisker diodes is challenging and typically must be done post-fabrication, limiting scalability.

Planar (Lateral) Diode

Description:

A planar diode is fabricated with a semi-insulating substrate, creating a robust Schottky junction directly on the surface.

Advantages:

- **Ruggedness**: The semi-insulating substrate provides durability, making the diode more robust.
- **Stable Contact**: Once fabricated, the contact remains fixed, enhancing reliability and stability.
- **Ease of Integration**: The planar design facilitates the integration of multiple diodes and enables coupling circuit integration during fabrication.

Challenges:

- **Higher Parasitic Capacitance**: The high dielectric constant of the substrate can increase parasitic capacitance, potentially affecting high-frequency performance.
- **Fixed Geometry**: The geometry of the diode is fixed after fabrication, limiting tuning options.
- **Complex Fabrication**: The fabrication process is relatively intricate and time-consuming compared to whisker diodes.

Quasi-vertical diode

Description:

A quasi-vertical diode is fabricated by bonding the epitaxy to a thermally conductive high-resistivity substrate, creating a robust Schottky junction directly on the surface.

Advantages:

- **Ruggedness**: The heterogeneous integration process onto a high-resistivity substrate provides durability, making the diode more robust.
- **Stable Contact**: Once fabricated, the contact remains fixed, enhancing reliability and stability.
- **Ease of Integration**: The design facilitates the integration of multiple diodes and enables significantly more complex coupling circuit integration during fabrication.
- **Low Parasitic Capacitance**: The QVD configuration is expected to exhibit lower parasitic capacitance compared to the lateral diode, simplifying the device equivalent circuit model.
- **Thermal Handling**: Faster cooling and smaller thermal resistance.
- **Mounting improvement**: Allows for the mounting of face-up versus facedown.

Challenges:

- **Fixed Geometry**: The geometry of the diode is fixed after fabrication, limiting tuning options.
- **Complex Fabrication**: The fabrication process for heterogeneously integrated diodes is relatively intricate and time-consuming compared to whisker diodes. The fabrication process is likely more straightforward for making on-wafer probable diodes versus the lateral diode; however, the membrane diodes could be potentially more challenging than the lateral diodes due to the backside processing.

1.4 Background on the Schottky Diode

The Schottky diode operates based on charge transport across a metal-semiconductor Schottky barrier. This barrier is responsible for controlling the current conduction and its capacitance. High-frequency operation calls for high-mobility materials such as GaAs, where the electron mobility is approximately 8000 $\frac{cm^2}{V\,s}$. So, the efforts described above and in this thesis are based on n-type GaAs Schottky diodes.

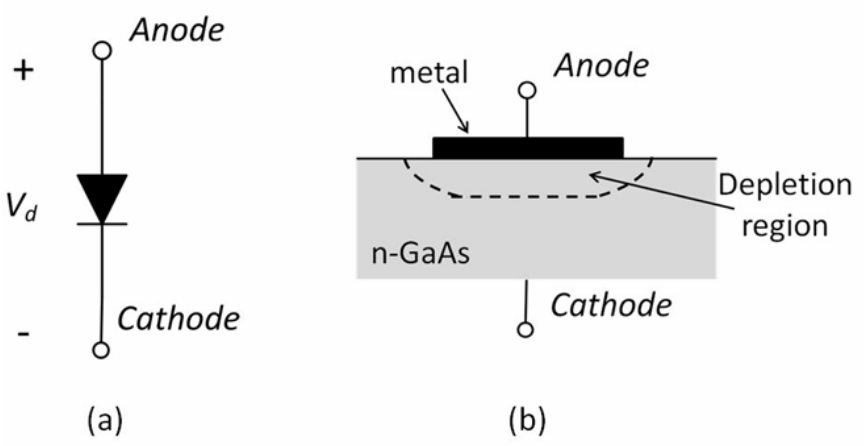


Figure 15 - Figure from Tangs Thesis (a) Schottky Diode Symbol (b) cartoon side profile of physical Schottky diode [30]

Several sources go through the physics of the devices given the band diagram of metal and semiconductor interface and derive voltage and current relationships given material parameters; a good reference is Physics of Semiconductor Devices by S.M. SZE [39]. This work has no modifications to this fundamental theory; thus, the detailed derivation of the diode equations will be omitted from this text. However, there are some critical relationships for completeness so the reader can understand the motivation and potential improvements for subsequent chapters.

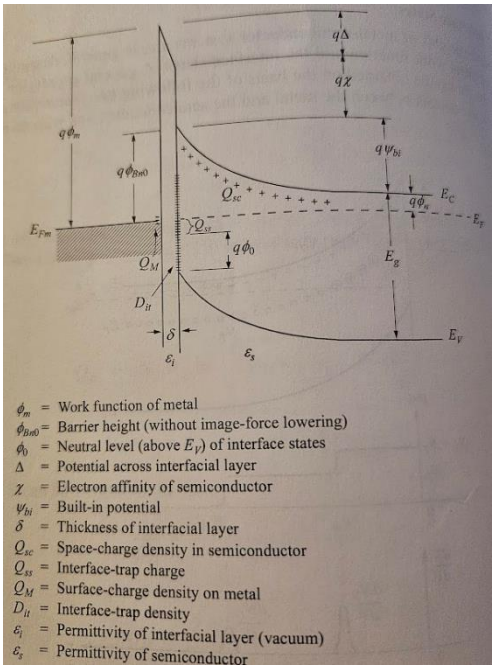


Figure 16 - Screenshot from [39] and shows the Schottky barrier and associated relationships associated with the device

Schottky Barrier Height: The above figure is a screenshot from [39] and shows the Schottky barrier and associated relationships associated with the device. The barrier height Φ_{bn} is the energy difference between the metal's Fermi level and the semiconductor's conduction band edge at the interface. Generally, it can be approximated as $\Phi_{bn} = \Phi_m - \chi$. Several factors can cause deviations from this generalization, resulting in a lower-than-expected barrier height, such as fermi level pinning, interface dipole formation, and image force lowering. This modified equation can also be found in literature and references such as SZE [39].

Below is a table of elements and their associated work functions. The Schottky diode made in this work used Ti/Au because of the target availability of the sputtering system used to define the anode. The higher the barrier height, the lower the reverse leakage current. A lower

barrier height reduces the turn-on voltage but increases the leakage current. The higher work function of the metal results in a larger built-in voltage, leading to a wider depletion region and, thus, lower capacitance. There are several factors to consider when choosing the metal for the Schottky contact, such as diffusion into the barrier, leading to less than optimal performance. Below is a table listing common elements for making these Schottky barriers.

Element	GaAs
Au	1.05
Cr	0.82
Cu	1.08
Ni	0.91
Pd	0.93
Pt	0.98
Ti	0.84
W	0.8

Table 1 – Common elements and associated work functions.

Current-Voltage relationship [39]

$$I(V) = A^* * T^2 * e^{\frac{-q*\Phi_{bn}}{k*T}} * \left(e^{\frac{q*V}{\eta*k*T})} - 1 \right) * \pi {r_d}^2$$

Where saturation current can be expressed as $I_{sat} = A^* * T^2 * e^{\frac{-q*\Phi_{bn}}{k*T}} * \pi {r_d}^2$

$$I(V) = I_{sat} * \left(e^{\frac{q*V}{\eta*k*T}} - 1 \right) * \pi {r_d}^2$$

In real devices, there is a series of resistances, R_s, due to the resistance of the semiconductor, contacts, and leads. We can modify the equation and account for this in the voltage term,

$V = V_d + IR_s$, thus

$$I(V) = I_{sat} * \left(e^{\frac{q*(V_d+IR_s)}{\eta*k*T}} - 1 \right) * \pi {r_d}^2$$

The series resistance is an important parameter for applications with the Schottky diode. It can affect efficiencies, sensitivities, and noise. Series resistance will be explored in Chapter 3, as the QVD improvement is the subject of that chapter. The ideality factor, η , is the parameter that characterizes how closely the diode follows the ideal diode equation. It is helpful to reinforce that an ideal diode depends on the material, temperature, and band bending at the semiconductor interface.

$$\eta = \left(k * T \left(\frac{\tanh\left(\frac{E_{00}}{kT}\right)}{E_{00}} - \frac{1}{2E_b} \right) \right)^{-1} \text{[30]}$$

E_{00}, is a material constant due to band bending that contains the doping concentration, dielectric permittivity, and effective electron mass.

$$E_{00} = 18.5 * 10^{-12} \sqrt{\frac{N_d}{m_e^* \varepsilon_r}} \text{[30]}$$

More useful is the ability to measure the ideality factor by using a non-linear curve fitting. Using the IV curve, you can measure the small signal conductance of the diode,

$$r_j = \frac{1}{g_j} = \left(\frac{di_d}{dV}\right)^{-1} = \frac{\eta kT}{qi_d}$$

Therefore,

$$\eta = \frac{r_j i_d}{kT}$$

The breakdown voltage of a Schottky diode is the fundamental characteristic that defines its reverse-bias operating limit. It also depends on the material parameters. The breakdown voltage limits how hard a diode can be driven with RF power and is used as a boundary condition for optimizing embedding impedances presented to the diode.

$$V_{bd} = 60 \left(\frac{E_g}{1.1eV}\right)^{\frac{3}{2}} \left(\frac{N_d}{10^{16}cm^{-3}}\right)^{-\frac{3}{4}} \text{[30]}$$

Finally, the capacitance characteristic of a diode is crucial. It determines the operating frequency by providing resonance at a specific frequency, enabling efficient power coupling into the junction. Capacitance also limits the bandwidth, as the impedance of a capacitor is inversely proportional to its capacitance. The diode's capacitance is voltage-dependent: as the reverse voltage increases, the depletion width also increases. The analogy of a parallel-plate capacitor and its analytical expression is helpful,

$$C = \frac{\varepsilon_r \varepsilon_0 A}{d}$$

Capacitance is inversely proportional to the distance between the plates; this explains why the depletion width and, thus, the applied voltage modulate the junction. The expression for the voltage-dependent depletion width and subsequent capacitance is as follows.

$$W_{bi} = \sqrt{\frac{2V_{bi}\varepsilon_r \varepsilon_0}{q * N_d}}$$

$$C_{j0} = \frac{\varepsilon_r \varepsilon_0 A_{anode}}{W_{bi}}$$

$$C_j(V_j) = \sqrt{\frac{q\varepsilon_r \varepsilon_0 N_d}{2(V_{bi} - V)}} * A_{anode}$$

1.5 Thesis outline.

This thesis focuses on advancing quasi-vertical technology, emphasizing optimizing various fabrication processes.

Chapter 2: Fabrication advancements of the Quasi-vertical GaAs Schottky diode heterogeneously integrated on silicon.

Chapter 3: Our team conducted characterization studies to ensure that the diffusion-bonded diodes performed comparable to prior art.

Chapter 4: Comparative study involving design, fabrication, and measurement in collaboration with Virginia Diodes with the Lateral vs Quasi-Vertical Structure.

Chapter 5: Conclusion, Future Work, References

Chapter 2- Improved process flow, fabrication, and characterization of GaAs Schottky diodes and process flow implementation to realize diffusion-bonded diodes.

The following publications are associated with the efforts and accomplishments contained in this chapter:

1. Moore, C., Cyberey, M., Widmann, D., Zhou, R., Weikle, R., Barker, S., & Lichtenberger, A. "Improved Process Flow of Heterogeneously Integrated Gallium Arsenide Schottky Diodes." International Symposium on Space Terahertz Technology (ISSTT), 2024.
2. Moore, C., Zhou R., Widmann, D., Lukaczyk, L. Cyberey M., Bawens, M., Weikle, R., Barker, S., & Lichtenberger, "Characterization and Fabrication of Diffusion Bonded GaAs Schottky Diodes." Accepted for Presentation at European Microwaves Conference (EuMEC), 2024.

2.1 Introduction

This chapter describes an improved process flow for fabricating heterogeneous integrated Quasi-Vertical Gallium Arsenide Schottky Diodes (QVDs). This chapter will also demonstrate the robustness of this process flow by realizing diffusion-bonded diodes. The diodes created in this work resulted in devices intended for the submillimeter-wave frequency band. These devices were characterized by DC and RF measurements. This work improves the process flow by reducing the number of processing steps and changing the order of said steps, both undertaken to minimize unwanted effects contributing to higher parasitics and reduced yield and to realize a more efficient process. The resulting circuits were found to have comparably low parasitics and improved performance compared to previous diodes quasi-vertical fabricated by our research group [31] [36][37][38] [40][41].

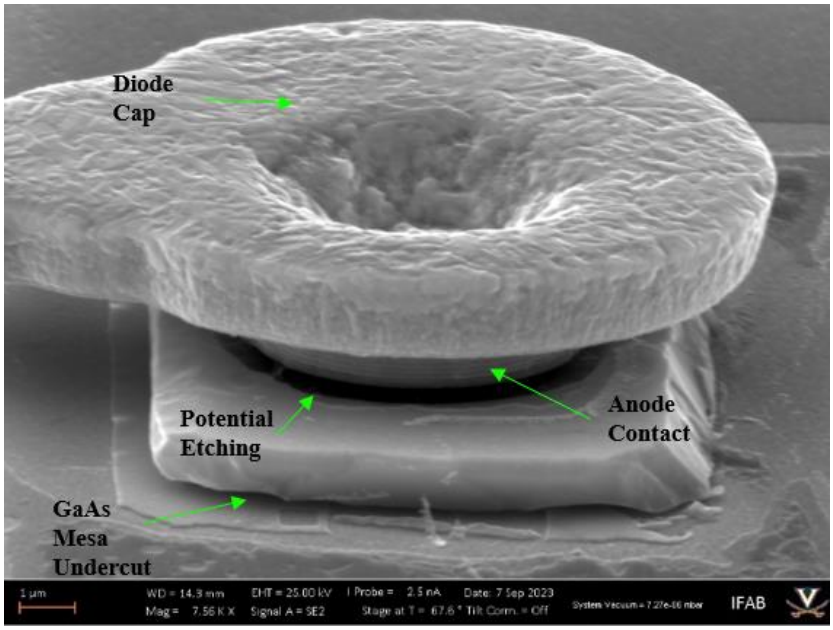


Figure 17 - Figure showing the undercutting of a GaAs Mesa from an older process without process modification

Figure 17 shows a scanning electron microscope (SEM) image of a prototypical quasi-vertical Schottky diode. This measurement captures one of the challenges associated with the previous process used to create QVDs: the undercutting of the GaAs mesa associated with wet etching processes.

A new fabrication process has been developed in collaboration with DMPI and researchers at the University of Virginia utilizing microstrip circuits realized on a silicon substrate with gold (Au) sidewall-coated vias co-fabricated with Au beam leads. This new process results in modest yields and improved thermal management and power handling, depending on the type of bonding used. This process may eliminate the need for additional power amplification and cooling systems, making it of particular interest to the space industry, manufacturers of consumer-grade electronics, or applications with strict power budgets [44].

The diodes described in this work were fabricated on two different substrates, 15 μm thick high resistivity (>10k$\frac{\Omega}{cm^2}$) silicon (for use as the dielectric layer for microstrip circuits) and a double-sided-polished 400um thick high resistivity silicon (>10k$\frac{\Omega}{cm^2}$) (for use in coplanar waveguide (CPW) circuits). The 15 μm thick high-resistivity silicon substrate was fabricated using silicon-on-insulator technology to create monolithically integrated circuits MMICs, specifically, high-frequency multipliers and a variety of membrane-type diode circuits. This included a process that produced backside metallization (the ground plane for microstrip) and plated side-coated vias, enabling continuity between top and bottom metalized features. This process also produced free-standing beam lead features for mounting waveguide blocks. The silicon parameters are shown in the table below.

	Silicon on Insulator	**Double-sided Polished**
Dopant:	P	N/Ph
Orientation	<100>	<100>
Thickness	15 +/-.5um	381+/-10
Resistivity:	>10,000 ohm-cm	>10,000 ohm-cm
Surface: Polished	Polished	Polished
Buried Oxide	1um +/- 5%	N/A
Handle Wafer	Flat/Notch: One SEMI Std Type/Dopant: P; Orientation: <100> Thickness: 450 +/- 10um Resistivity: 1-10 ohm-cm; Surface: polished	N/A
Type of Growth	Float Zone	Float Zone

Table 2 – Silicon Used for this work

The SOI process flow for QVDs was implemented with both adhesive bonding, using the UVA-developed approach of bonding GaAs to SOI with SU8, and separately, for the first time, diffusion (metal-to-metal) bonding GaAs to SOI using a separate wafer, but with a slightly modified process.

Adhesive bonding is advantageous when co-integrating multiple devices of different substrate types onto a common substrate, when sufficient surface cleanliness of the substrates can not be achieved, when thermal expansion coefficients are significantly mismatched, and when force and temperature constrain the bonding process. Adhesive bonding also allows for bonding in the presence of uneven topography, i.e., when predefined features exist on the bonding interface [41]. In both cases, adhesive and diffusion-bonded quasi-vertical Schottky diodes potentially offer advantages compared to lateral/planar-type diodes made on semi-insulating substrates due to the differences in geometry, a topic to be discussed in a later chapter. However, diffusion-bonded devices offer significantly better thermal performance by eliminating the thermal resistance of the adhesive layer. Figure 18 shows a side profile of the Schottky diode, including a graded InGaAs ohmic contact layer (discussed below) and the bonding layer (adhesive and diffusion interface layers).

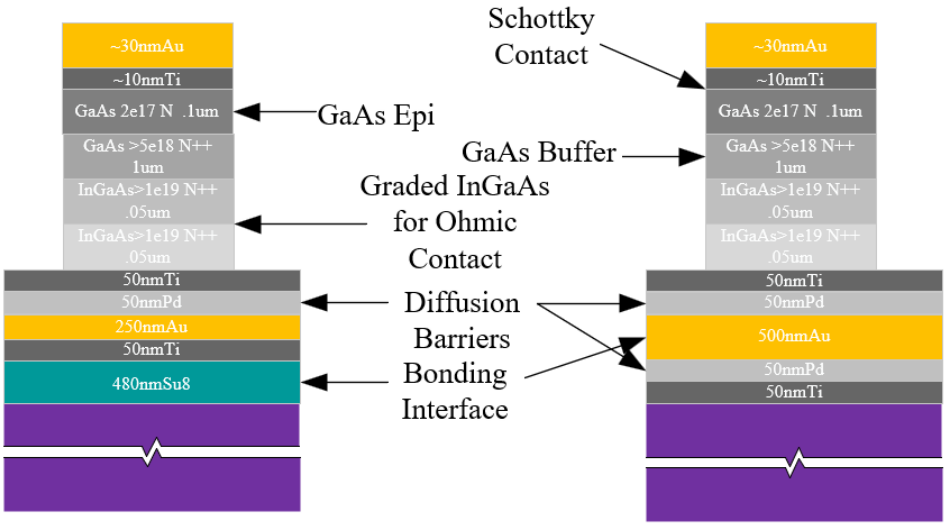


Figure 18– This cartoon side profile shows GaAs material bonded to Silicon with two distinctive bonding layers. The GaAs mesa comprises several layers, as the text below explains.

This work utilizes prior process flow improvements using a non-alloyed ohmic contact [37] [38]. The first implementation of the quasi-vertical diode adapted the ohmic metal stack from the prior art and provided sufficiently low specific contact resistance, ρ_c (5×10^{-7} W-cm^2) but required annealing, which proved challenging; prior efforts with rapid thermal annealing (RTA) exhibited susceptibility to small changes in surface cleanliness and pre-metal-deposition surface treatment. Therefore, this process was eliminated to simplify the process [37][38].

This change was implemented by redesigning the epitaxy to include a highly doped InGaAs layer to form an ohmic contact on the cathode side of the diode. The addition of indium gallium arsenide is used so that a graded epitaxy can be grown and doped sequentially until it achieves a layer with the doping of $> 10^{19}$cm^{-3} concentration.

The grading of the InGaAs composition makes a smooth transition in the conduction and valence bands, so there aren't discontinuities that could lead to carrier trapping. This effect is shown in the figure below. This grading layer can also lower defects since InGaAs and GaAs are lattice mismatched. The target doping concentration isn't achievable with the wider-band material of GaAs; the InGaAs has a narrower bandgap, which allows the higher carrier concentration.

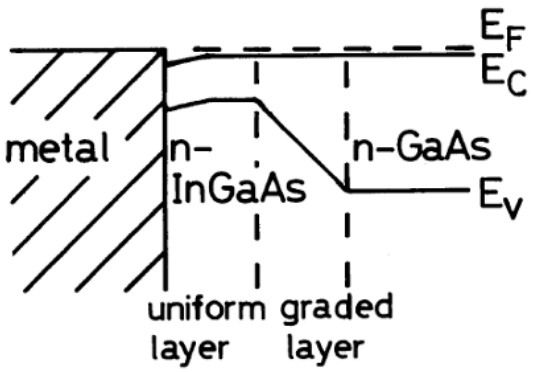


Figure 19 - Band Diagram for metal-InGaAs ohmic contact interface [38]

The theory behind establishing an ohmic contact is covered in [43]. In summary, an ohmic contact is a metal-to-semiconductor contact with negligible junction resistance relative to the total resistance of the semiconductor device. The ohmic contact should ideally not significantly perturb the device's performance. It can supply the required current with a voltage drop that is sufficiently small compared with the drop across the active region of the device. If the doping concentration is sufficiently high, field emission or quantum-mechanical tunneling of electrons through a barrier will be the dominant current transport process, which has a linear voltage-to-current relationship. In the case of highly doped InGaAs with $> 10^{19}$cm^{-3} doping concentration, a titanium layer as the

metal-to-semiconductor contact can result in a specific contact resistance on the order of 10^{-7} W-cm^2 sufficiently low not to perturb the device's performance.

This layer is hereby referred to as the InGaAs cap layer. This epitaxy design was used to fabricate the devices described in this chapter. Three GaAs-based substrates were used for this work and are shown in the figures below. The materials are sourced from Sumika Electronic Materials, Inc [42].

Epitaxial Structure								
No.	Material	Composition	Thickness Target (um)	Thickness Tol.	C/C (cm^{-3}) Target	C/C Tol.	Dopant	Carrier Type
6	$In_yGa_{1-y}As$	y = 0.60	0.0400	±10%	>1.0E19*	N/A	Te	N++
5	$In_yGa_{1-y}As$	y = 0 → 0.60	0.0500	±10%	>5E18→>1.0E19*	±10%	Te	N++
4	GaAs		1.000	±10%	>5.0E18	±10%	Si	N++
3	GaAs		**0.5000**	±10%	**1.0E17**	±10%	Si	N
2	$Al_xGa_{1-x}As$	x=0.50	1.0000	±10%	--	N/A	--	--
1	GaAs		0.0500	±10%	--	N/A	--	--
Substrate								

Epitaxial Structure								
No.	Material	Composition	Thickness Target (um)	Thickness Tol.	C/C (cm^{-3}) Target	C/C Tol.	Dopant	Carrier Type
6	$In_yGa_{1-y}As$	y = 0.60	0.0400	±10%	>1.0E19*	N/A	Te	N++
5	$In_yGa_{1-y}As$	y = 0 → 0.60	0.0500	±10%	>1.0E19*	±10%	Te	N++
4	GaAs		1.000	±10%	>5.0E18	±10%	Si	N++
3	GaAs		0.2800	±10%	2.0E17	±10%	Si	N
2	$Al_xGa_{1-x}As$	x=0.50	1.0000	±10%	--	N/A	--	--
1	GaAs		0.0500	±10%	--	N/A	--	--
Substrate								

Epitaxial Structure								
No.	Material	Composition	Thickness Target (um)	Thickness Tol.	C/C (cm^{-3}) Target	C/C Tol.	Dopant	Carrier Type
6	$In_yGa_{1-y}As$	y = 0.60	0.0400	±10%	>1.0E19*	N/A	Te	N++
5	$In_yGa_{1-y}As$	y = 0 → 0.60	0.0500	±10%	>5E18→>1.0E19*	±10%	Te	N++
4	GaAs		1.000	±10%	>5.0E18	±10%	Si	N++
3	GaAs		**0.1000**	±10%	2.0E17	±10%	Si	N
2	$Al_xGa_{1-x}As$	x=0.50	1.0000	±10%	--	N/A	--	--
1	GaAs		0.0500	±10%	--	N/A	--	--
Substrate								

Figure 20 - GaAs Materials used in this work were ordered from Sumika Electronic Materials. These are to be denoted as R6, R4, and R7, respectively.

The prior art has characterized this ohmic contact using the transmission line method (TLM). One can extract the specific contact resistance by patterning Ti/Pd/Au contact pads on the highly doped InGaAs cap of varying length.

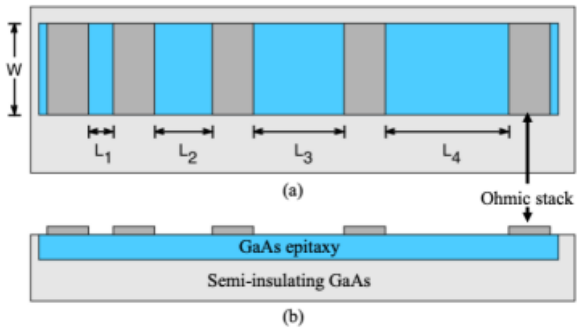


Figure 21 – Diagram illustrating the geometry used for TLM measurement (a) top view of the wafer, (b) side-view

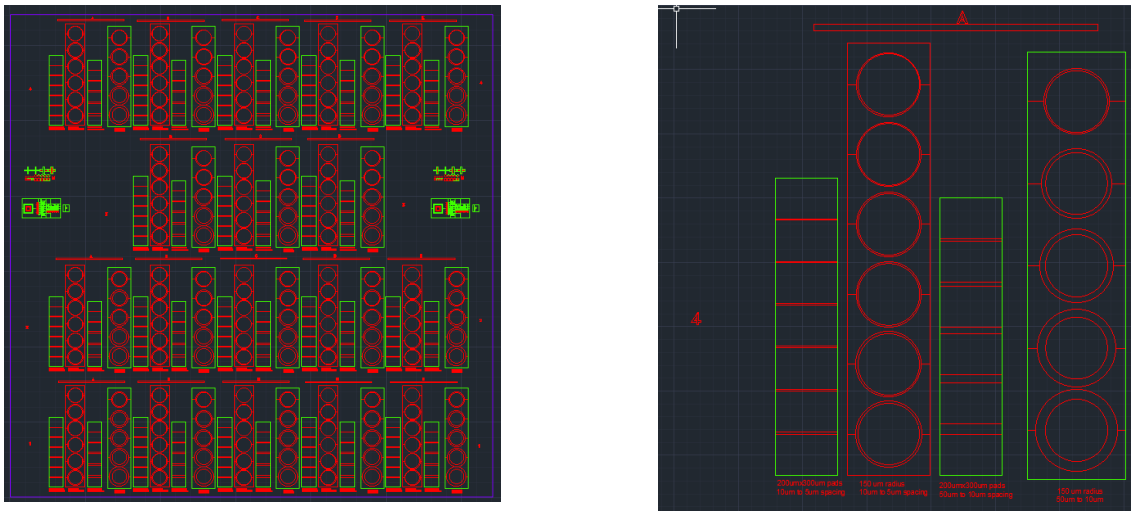
Sample	L_T (µm)	L'_T (µm)	ρ_c $(\Omega.cm^2)$	ρ'_c $(\Omega.cm^2)$	ρ_c^{avg} $(\Omega.cm^2)$
A	49.3	54.8	$7.25 * 10^{-7}$	$9.14 * 10^{-7}$	$8.19 * 10^{-7}$
B	54.4	52.5	$8.92 * 10^{-7}$	$8.19 * 10^{-7}$	$8.55 * 10^{-7}$

Figure 22 – Screen shot from Nardi's thesis with measurements and calculated values of specific contact

Prior art showed that the specific contact resistance between the pads is on the order of 10^{-7}. These measurements were verified in this work, and I've contributed the below work to assess the consistency of the ohmic contact's specific contact resistivity across the wafer.

A mask with annular slot rings and rectangular pads for the TLM measurements was made using a direct write laser lithography instrument, the ML3 Microwriter. The mask is created using a ¼ "thick Qz photomask with prespun with an AZ1500 resist layer; the exposure setting on the ML3 was 80 mJ/cm^2, using "normal" settings with 10mm mesh size. Four parts of deionized water and one part of AZ400K (Potassium Borate-based developer) are used for development. The development time is approximately 5-10 seconds, with vigorous agitation. One part deionized water and 1 part Transene CHROMIUM ETCHANT 1020 were used to etch away the chrome

layer on the mask to create features. The etch takes approximately 30-45 seconds at room temperature; it is done by placing a large open-mouth beaker with a diameter greater than 6 inches on top of a surface with topography so that you can see through the transparent Qz in the windows that are being etched away. Following the chrome etch, the residue resist is stripped with AZ300T heated to 80°C, followed by DI rinses and a quick 5-10 second 2% H2S04 98% deionized water etch to remove any "cloudiness" from the Qz (if there's excessive cloudiness on the transparent part of the photomask) and a final round of DI rinses.



(a) A new mask will be used to develop statistics for the consistency of ohmic contact. There are four rows across approximately a 1" x1" wafer. Totaling 16 measurements per set of geometries.

(b) This is the feature that is arrayed on the mask. There are rectangular structures that increase pad-to-pad spacing by 10um and 1 μm—the annular ring structure also increments by 10 and 1 um.

Figure 23 – Photolithography mask for creating TLM structures.

The first step to realize TLM structures defined with the mask is to spin AZ NLOF 2020 at 3000 RPM, corresponding to a 2.0-micron film thickness. This step is verified with a mechanical profiler. Films of 50 nm of Ti, 50 nm Pd, and 100 nm of Au were deposited and lifted off with 50°C heated acetone and isopropyl. Positively toned resist defines masking areas to isolate the

InGaAs, buffer GaAs, and epitaxial GaAs layers from the bulk GaAs. A chlorine-based dry etch defines these features, isolating the region to be measured.

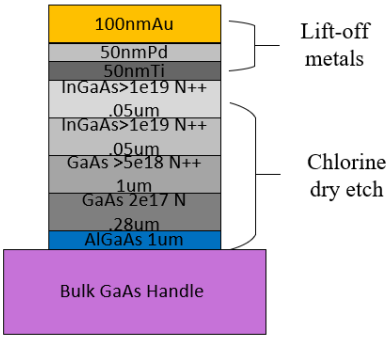


Figure 24 – Cartoon showing the Final cross-section after creating TLM structures.

For the TLM structures, the conductive layers of GaAs should sit on top of a semi-insulating layer; a table showing the individual conductivities is provided below. The calculations use the following conductivity equation: $\sigma = qn\mu$ (charge * doping * mobility), by making the approximation for that an n-type semiconductor $n \approx N_d$, and since mobility varies as $\mu \propto \frac{1}{\sqrt{N_d}}$. However, if we normalize the density of states, then $\mu \propto \frac{1}{\sqrt{\frac{N_d}{N_c}}}$, and finally, if taking into account scattering's impact on mobility and applying Matthiessen's rule, yields $\mu = \frac{1}{1+\sqrt{\frac{N_d}{N_c}}}$, which is used to estimate the conductivity values in the table below.

Material in Stack	Doping type	Doping Level (N_d)	Conductivity (σ) (S/m)
InGaAs	N++	>1E19	>1.46E5
InGaAs	N++	5E18->1E19	≈9.92E4 – 1.46E5
GaAs buffer	N++	>5E18	>9.92E4
GaAs Epi	N	2E17	1.33E4
$Al_{.5}\ (GaAs)_{.5}$	-	Not quoted	Not calculated
GaAs Handle	Not doped	Assumed Intrinsic	≈1E-4

Table 3 – Table of conductivities for R4 Material

The GaAs handle is not explicitly denoted as semi-insulating material; however, if intrinsic properties are assumed, it is relatively insulating and thus can be used for TLM measurements. Each of these structures is measured using the four-point probing method, which sources current with two probes on the far side of the contact pads and measures voltage between the pads. This measurement method eliminates the resistance due to the probe and probe cabling.

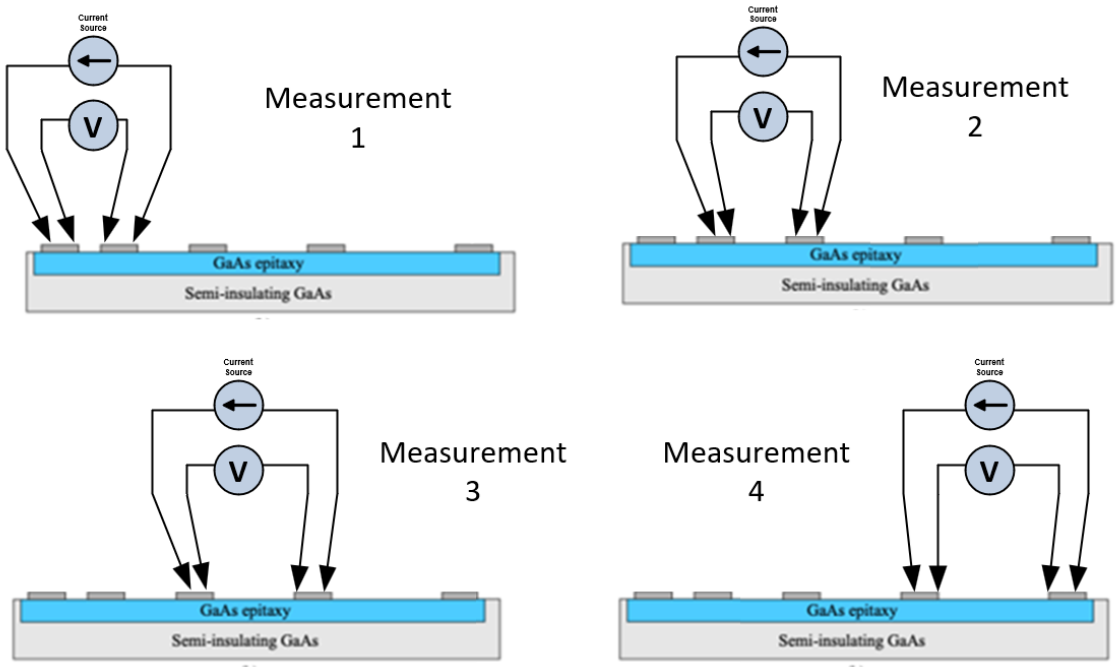


Figure 25 – TLM measurement procedure for five gaps.

The theoretical framework, as described in Williams and Sze [39] [43], is applied to extract the specific contact resistance using a linear fit on the data. The following quantities are calculated:

1. Contact resistance (R_c): This refers to the resistance at the interface between the contact and the semiconductor.
2. Transfer length (L_x): This is the characteristic distance current transfers from the contact into the semiconductor.
3. Specific contact resistance (ρ_c): The following relationship gives this $\rho_c = R_c L_x W$; Where W is the width of the pad, which in this case is 300 µm.

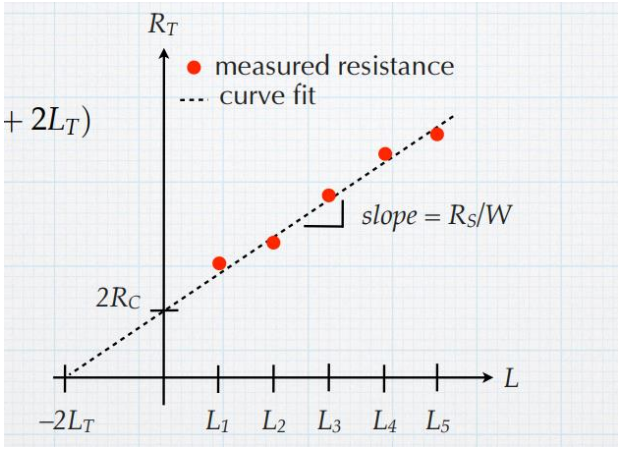
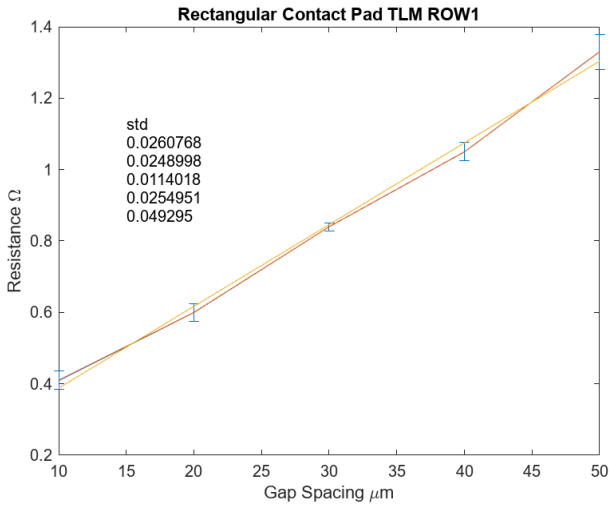
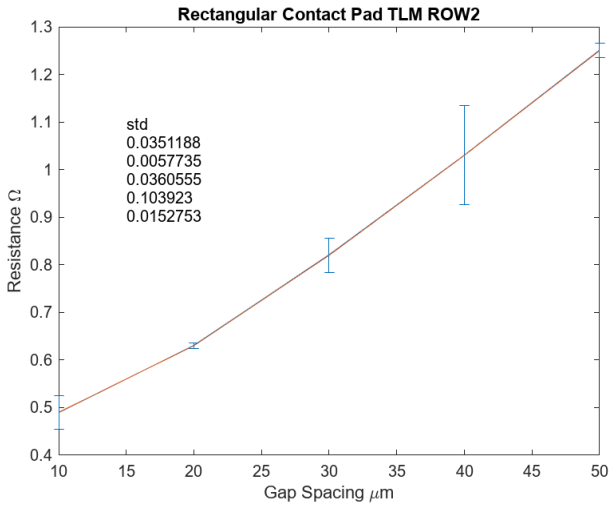


Figure 26 Drawing showing the method to extract quantities need to calculate specific contact resistance.

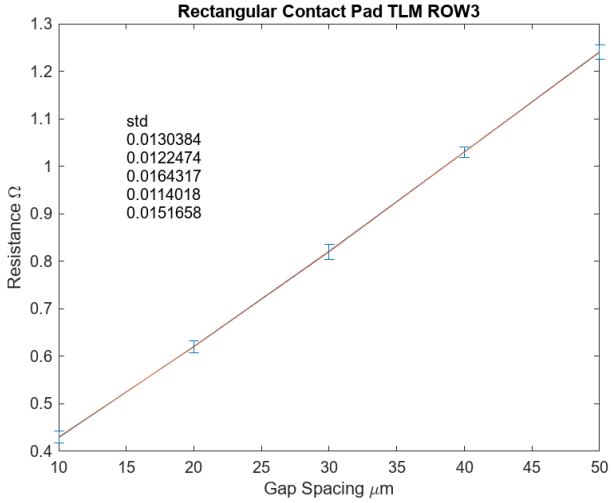
The measured results are below in Figure 27; use linear curve fitting to determine the slope and intercept. The slope is found to be .0229 $(\frac{\Omega}{\mu m})$, and the intercept is 0.159 (Ω). The separate plots (a-d) show the data, the standard deviation of each data point corresponding to a specific pad-to-pad spacing, and error bars are added to show the variation between similar pad-to-pad spacing across that row. Finally, plot (d) shows all the data across the entire set (entire wafer), the standard deviation is calculated, and error bars are re-plotted to show variation.



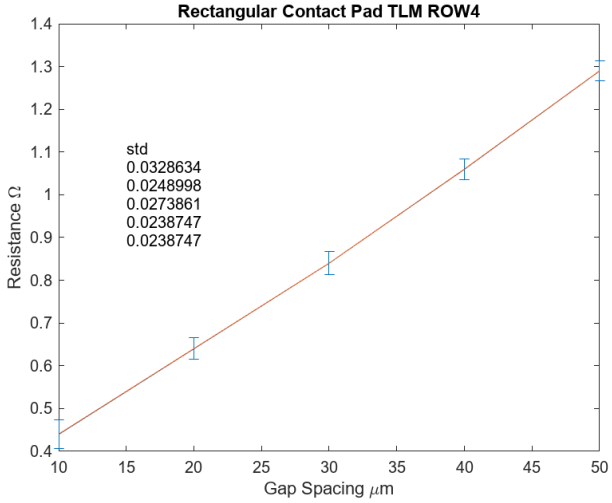
(a) Measurement results from row1



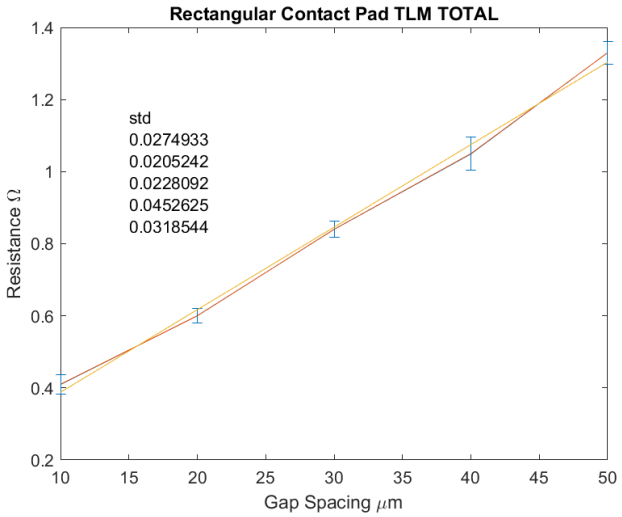
(b) Measurement results from row2



(c) Measurement results from row3



(d) Measurement results from row4



(e) This plot shows all the data from plots (a – d); the standard deviation and error bars are re-calculated and shown.

Figure 27 – Measurements for the ohmic contact

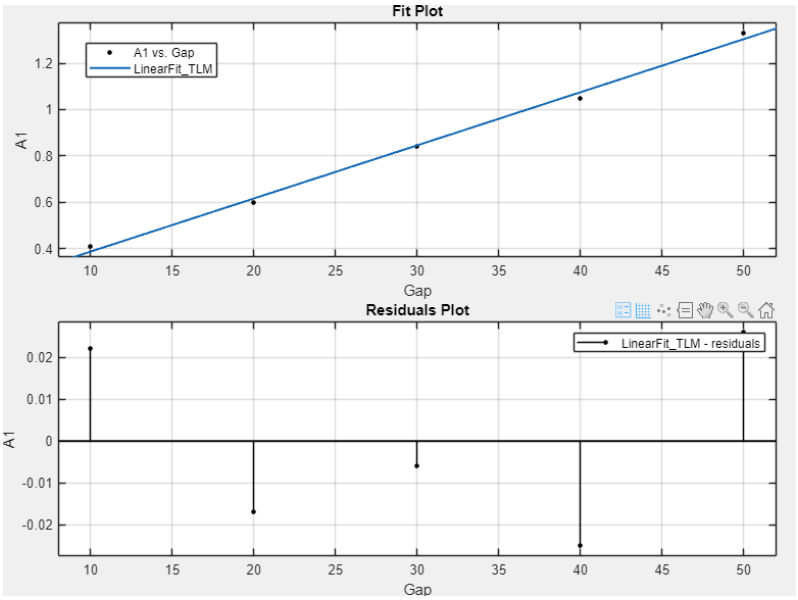


Figure 28 – Plot showing fit and residuals for the linear curve fitting.

Goodness of Fit

	Value
SSE	0.0021
R-square	0.9960
DFE	3.0000
Adj R-sq	0.9947
RMSE	0.0265

Figure 29 – Goodness of fit parameters

Using the fitted curve, $y = .0229x + .159$, $2 * R_c$ is found when x=0. $\frac{R_c}{2} = .0795\ \Omega$. $2 * L_x$ is found when y=0. $0 = .0229x + .159$. $\frac{L_x}{2} = 3.47\ \mu m$.

Using each of these values, one can calculate the specific contact resistance, $\rho_c = R_c L_x W\ [\Omega\ \mu m^2]$. However, when converted to cm^2, it is calculated as 8×10^{-7}W-cm^2. These results show that an ohmic contact can be uniformly realized across an entire wafer of GaAs. Previous work showed the specific contact resistance for this GaAs stack; however, we did not have insight into its uniformity. This contribution is essential to eliminate any suspicion that yield or performance issues are attributable to uniformity issues of ohmic contacts across the wafer.

2.2 Improved Process Flow

The improved fabrication process flow involves a unique epitaxy transfer method for bonding GaAs material to a silicon-on-insulator (SOI) substrate to create Schottky diodes [1-6]. GaAs epitaxy on a semi-insulating 650 µm GaAs handle featuring an AlGaAs etch stop layer, n-GaAs, n+-GaAs device layers, and a 90 nm highly-doped ($>10^{-19}\ cm^{-3}$) concentration graded InxGa(1–x)As cap layer (x:0->0.6) was used as the semiconductor material stack for the diode. The procedure used to create the devices is adapted from the process described in references [31] [36][37][38] [40][41].

Several masks were designed for this work, each accounting for various issues encountered during failed runs. However, the final version of the process used is presented for this work.

The screenshot below is of the mask set without any annotations. It comprises several features to assess the efficacy of the processes during fabrication.

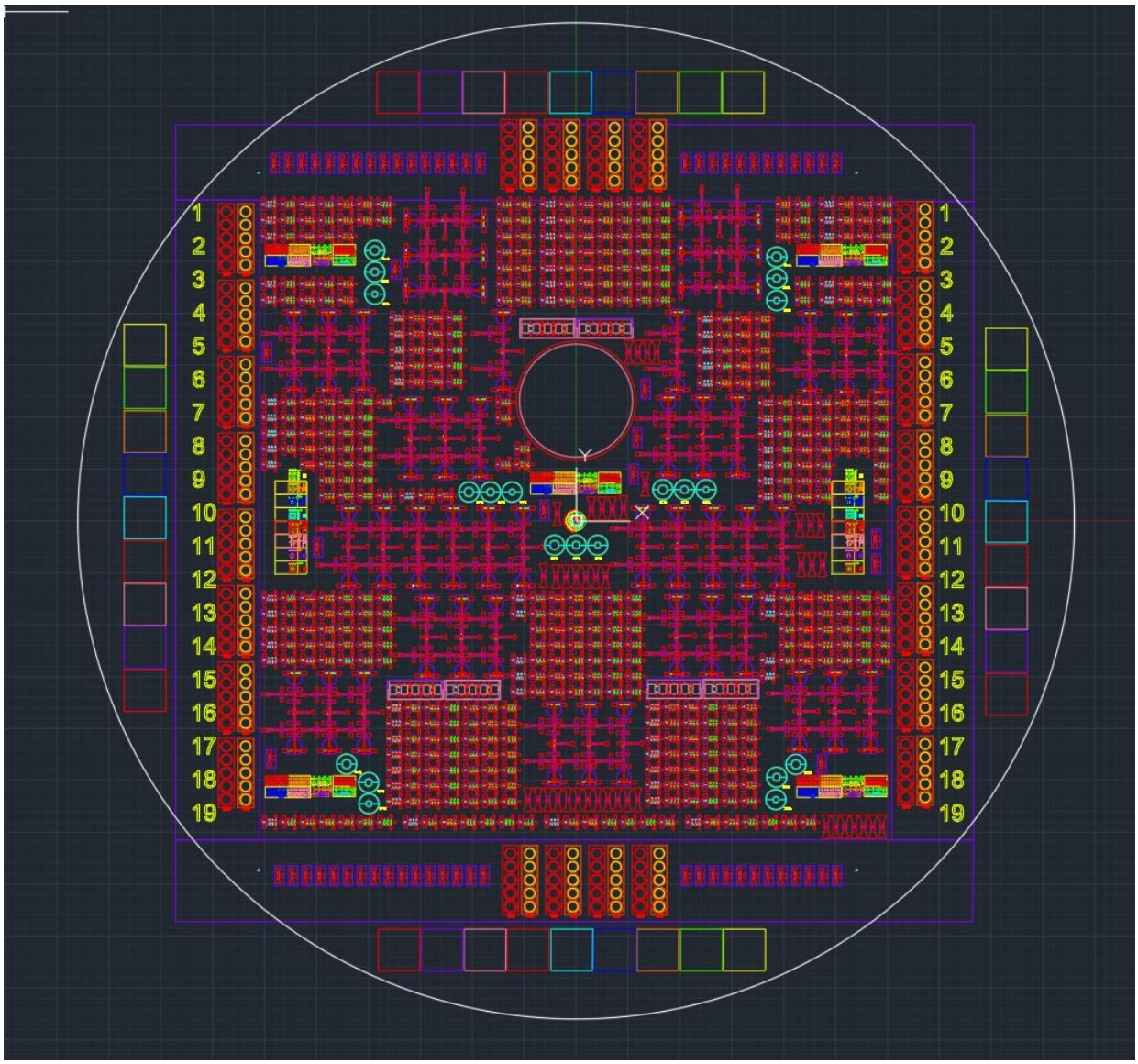


Figure 30 – Full Mask Set for Fabrication

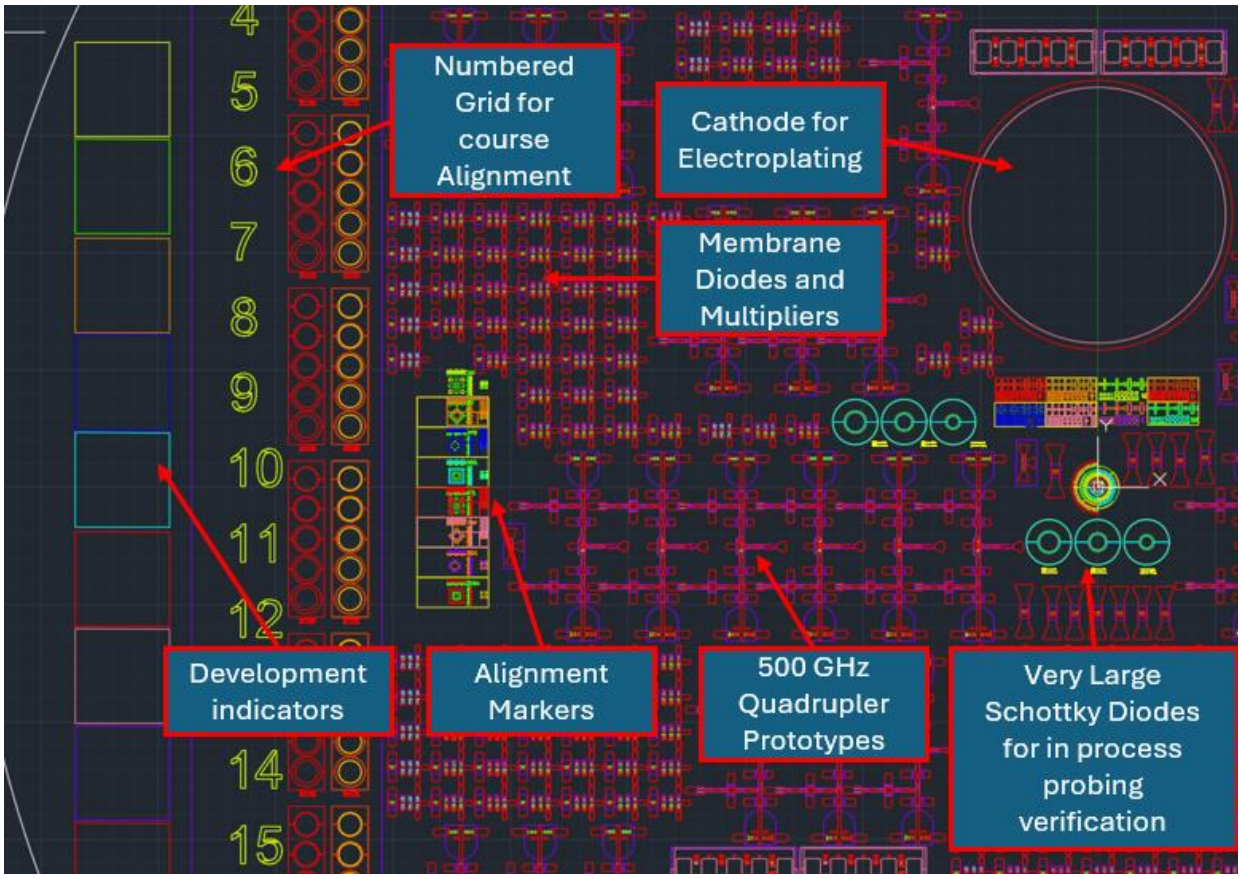


Figure 31 – Description of essential features

2.2.1 Substrate preparation and bonding

The process begins by preparing the substrates for ohmic metal deposition and bonding. The SOI substrates used in this work are produced from the foundry as 50.8 mm diameter or 100 mm wafers, which, in the case of the larger wafer, are laser cut, resulting in 30 mm or 50.8 mm diameter wafers. The SOI wafers to be laser cut have a thin layer of photoresist spun as a protective layer. During the laser cutting, the photoresist near the edges of the wafer is significantly hardened by the laser and impregnated with debris from the cutting process, making the photoresist at the perimeter of the laser cut wafers challenging to remove. The procedure for removing this photoresist is using a surgical scalpel under a microscope with a considerable working distance, meticulously scraping the surface around the edge of the wafer without significantly causing damage, e.g., excessive scratches. Following the scalpel, a 1um grit-sized piece of sandpaper is used to remove the top layer of the baked resist on top of the Silicon at the perimeter of the wafer. The wafer is held in a cellulose wipe and gently rotated 360° multiple times. Previously, the next step in this process would be to use a variety of solvents (acetone, isopropyl, regnant alcohol, and methanol) to spin clean the surface while applying light pressure with a wetted cleanroom swab. However, this process was inconsistent, often resulting in leftover residue from the laser-hardened photoresist. This work improved the SOI (and silicon) substrate preparation using Kayaku Remover-PG, which is N-Methyl-2-pyrrolidone (NMP) based with an added surfactant. The Remover-PG is prepared by heating

it to 80°C in a 250 mL beaker with a stir bar set to 200 RPM, ensuring thermal stability. After the Remover-PG has reached the desired temperature, it is poured into a Teflon spray bottle and used to spray the wafer while holding it over a second beaker for the waste product collection. This helps ensure that very little of the unwanted residual photoresist (from the scalpel and sandpaper process) is redeposited onto the surface of the wafer. The next step is to place the wafer facedown into a PTFE wafer mesh basket into another 250 mL beaker of Remover-PG with a stir bar programmed to spin at 200 RPM. This wafer is left in the solution for >1hrs. During this soaking/cleaning process, the GaAs surface of the semiconductor material wafer stack is cleaned.

The GaAs cleaning procedure was adopted from prior art, but it is worth noting that ammonium hydroxide is critical to removing GaAs native oxides [45]. This work uses a mixture of 2% Ammonium Hydroxide and 98% deionized water. This solution can also be used before the GaAs mesa etch to increase the uniformity of the etch, though not done for this work. This was found by collaborating with other researchers in the IFAB cleanroom when a problem was encountered in which a GaAs surface could not be etched.

Prior to loading the GaAs wafers for metal evaporation, each removable evaporator fixture part is sandblasted, wiped with wetted isopropyl cellulose wipes, and baked at >110°C for 1 hour. Afterward, the evaporator is reassembled. Each metal ingot's pocket is checked to ensure that the crucible is filled with at least 60% volume relative to the size of the crucible. Each metal is individually calibrated for appropriate thickness and inspected to ensure acceptable adhesion and surface roughness. A piezoelectric Qz crystal is used to monitor deposition thickness.

The GaAs wafers must be loaded immediately after the above pretreatment/cleaning with 2% Ammonium Hydroxide and 98% deionized water, which removes Gallium and Arsenic's native oxide. A 2" stainless steel carrier is sandblasted to clear out any residual metals from previous depositions so that when a wafer is mounted on it using double-sided Kapton tape, the adhesion to the carrier is sufficient. The tape is cut into a triangle, and a large portion of the tape is exposed under the GaAs so that it can be easily removed after the deposition.

The chamber is left to pump until vacuum levels have reached less than 9E-7 torr, at which point the deposition can begin. Titanium, palladium, gold, and titanium (Ti/Pd/Au/Ti) (20/40/150/20 nm) are deposited onto the InGaAs cap layer with electron beam physical vapor deposition. An in-situ ion mill pre-clean step is not used, as shown with the TLM measurements; a sufficient specific contact resistance can be achieved without the ion mill pre-clean step.

The time it takes to deposit the ohmic metals is a large enough processing window to prepare the SOI or silicon substrate intended for heterogeneous integration. The SOI or silicon wafer is unloaded from its PG remover's soak and immediately submerged in heated 80°C deionized water. After the Remover-PG has visually dissolved into the water, the wafer is sprayed with isopropyl. The wafer is then blow-dried and placed on a few wipes in the bottom of a wide-mouth PTFE dish. Ethylene glycol is poured over the wafer, and a swab is used to wipe away much of the ethylene glycol. The ethylene glycol helps remove remaining carbon-based residues and acts as an anti-static agent, aiding the removal of any particles that could be statically clung to the high-resistivity wafer. A standard solvent-based cleaning procedure is then performed, and the wafer is next subjected to >1hr of O2 plasma at approximately [60

sccms of O2, 800mT partial pressure, and 200W RF**.** This O2 plasma condition is standardized for the remainder of this process.

Afterward, the wafer is submerged in buffered oxide etch 10% HF; 50% Ammonium Floride, and 40% water. After the surface becomes hydrophobic, which is observed when the HF wicks off the wafer, it undergoes a standard solvent cleaning procedure augmented for this work with an anti-static N_2 blow dry and dehydration bake at 130°C for >10 min.

After dehydration, an anti-static N_2 blow dry is used immediately before applying the bonding layer of SU8 6000.5. SU8 to the wafer with a pipette, ensuring the resist completely covers the surface with no bubbles. The SU8 is spun onto the wafer at 10K RPM 4500RPM ramp per second, corresponding to ~450nm thick film. A ramp of half of the target spin speed was found to give the most uniform layer of SU8 6000.5.

This thickness was verified with ellipsometry using a Cauchy film model on a separate monitor wafer. The wafer should be inspected for large or deep streaks, which will be due to unremoved debris; if there are streaks, the wafer should be reworked.

A small-tipped swab is used with AZ EBR (AZ edge bead remover) to remove most of the edge bead and backside resist. The SOI (or Si) wafer is then placed onto a preheated ¼" thick quartz wafer on a 110°C hotplate and baked for 60 seconds. The wafer and the thick quartz wafer are removed in tandem and placed on an insulating surface (not metal) to cool slowly for precisely 10 minutes. This process prevents the photoresist from cracking and ensures a continuous smooth film.

After 10 minutes of cooling, the wafer is subjected to an iline (iLine filter is installed) flood exposure, ensuring that light with wavelengths less than 240nm is filtered to prevent unwanted

chemical reactions that could lead to blistering. The exposure is calibrated and timed to provide 410 mJ/cm^2.

Thermo-compression bonding is performed using one of two separate (one "homemade") bonding instruments. The process developed in this work for bonding using the commercial SUSS XB8 bonder is shown in the table below. This is the same bonding process documented in references [31] [36][37][38] [40][41], using the "homemade" bonding tool but adapted for the SUSS XB8 bonder.

Step	**Top Temp (°C)**	**Bottom Temp (°C)**	**Chamber Press (mBar)**	**Tool Force (N)**	**Log Data (Seconds)**	**Process time (hh:mm)**
1	30	30	Purge	0	1	0:30
2	30	30	Purge	0	1	0:30
3	30	30	5.00E-5	0	1	1:00
4	30	30	5.00E-5	0	1	1:00
5	30	30	5.00E-5	500	1	1:00
6	140	140	5.00E-5	500	1	1:00
7	140	140	5.00E-5	0	1	2:30
8	30	30	Purge	0	1	0:30

Table 4 - Bonding Process on the SUSS Microtech Bonding Machine

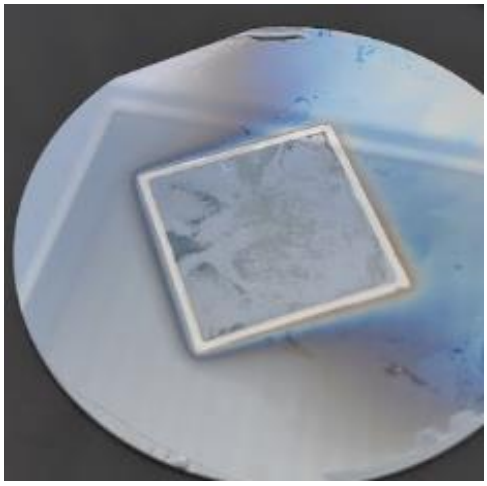
2.2.2 Semiconductor Stack: GaAs Handle removal

The handle of the GaAs epitaxy is an instric layer of GaAs and an AlGaAs etch stop, on which the doped layers are grown. The doped layers of GaAs total just over 1 μm, so it cannot be handled for processing without a thicker GaAs handle layer. After bonding, the handle can

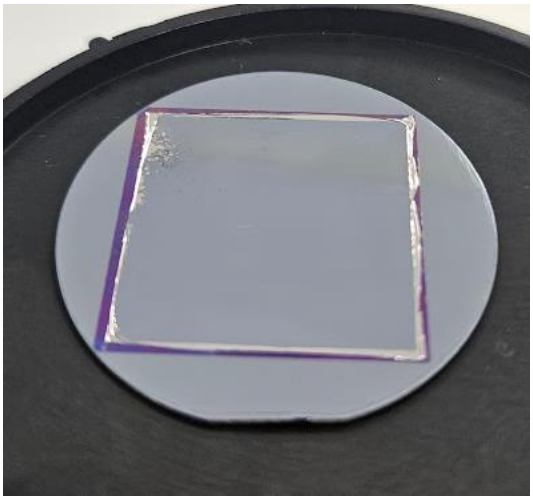
be removed. Similarly, the Silicon on the insulator material bonded to the GaAs also has an intrinsic silicon layer used as a handle; both of these handles are removed after bonding.

After bonding, the following process is used for handle removal: TCE and methanol are used with a wetted swab to remove any residual grease or debris from the bonding process. The GaAs handle removal is a multi-step process: O2 plasma, argon sputter etch, followed by a 50° C nitric-based etch, a 50° C citric-based etch step, and a room temperature hydrofluoric acid-based etch for the AlGaAs etch stop layer. Prior art had implemented the nitric and citric-based etches in an effort to increase the yield by decreasing the delamination of the bonded layers. This new process adds an O2 plasma and argon sputter etch to prepare the wafer for handle removal. The O2 plasma helps remove residual solvents from the cleaning of the wafer post bonding, and the argon sputter-etch etches the top surface of the GaAs handle, effectively ridding the surface of any other remaining contaminants and oxide, leaving a clean surface. Immediately after the sputter etches, the GaAs handle is removed with the nitric/water/hydrogen peroxide and citric/water/hydrogen peroxide etchant until the AlGaAs layer is exposed, which is very dark gray in color. Once the dark gray surface appears, 5 minutes of citric-based over-etching is done, ensuring that any of the remaining GaAs handle is removed. Adding a stir bar rotating at 75 RPM in the Nitric-based and citric-based etchants was found to realize more repeatable etch times. After the 5 minutes of over-etching, the wafer is submerged in ~50°C deionized water, with vigorous agitation for 5 seconds. This is followed by submerging the wafer in room temperature deionized water, with vigorous agitation for 5 seconds, before finalizing submerging into an AlGaAs etch. The AlGaAs etch stop layer is removed by lightly wafting in concentrated 49% AWR brand hydrofluoric acid. It is important

to note that if the wafer is exposed to either DI water or air for too long, the AlGaAs surface will become oxidized, and the AlGaAs oxide layer will no longer be removed in the HF, with those unetched regions, reducing the overall yield of working devices (i.e., these regions will not yield devices with good electrical characteristics). After this step, a picture of the wafer should be taken to avoid devices from these regions during testing. Special attention should be given to the age of the hydrogen peroxide used in the citric and nitric-based etches and how it's been stored. Hydrogen peroxide reacts with light, which causes it to convert to water slowly over time. One should, therefore, not use a bottle of H_2O_2 past its expiration date, and one should also avoid using a nearly empty bottle. Though a full study was not undertaken, limited data indicated that the AWR brand of HF provided the most consistent results for removing AlGaAs. Removing GaAs handle is still a challenging and long process, and future researchers can potentially improve it.



(a) Example of the wafer after thinning that has residual AlGaAs oxide.



(b) An example of a wafer after thinning showing no residual AlGaAs oxide.

Figure 32 – Examples of GaAs surface after handle removal

Figure 33 – Cartoon illustrating the GaAs handle removal process

The above Figure 33 illustrates the thinning process. From left to right, a nitric solution etchs of the GaAs handle layer, colloquially called the "Fast GaAs etch," followed by a citric etch, denoted as the "Slow GaAs etch." An HF solution is used to remove the AlGaAs until the lower doped epitaxy is exposed, which is used to form the Schottky Diode contact.

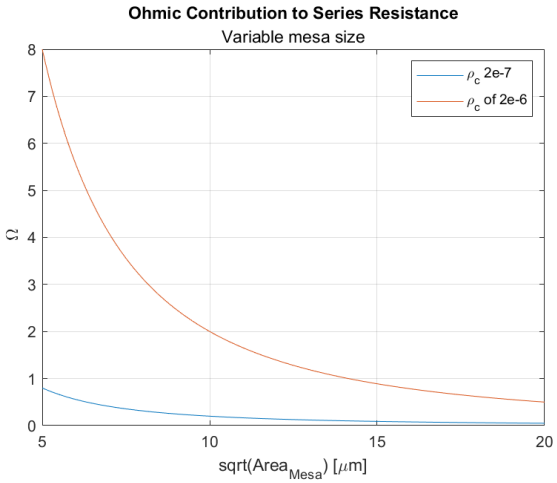
2.2.3 Mesa Etch

The mesa etch defines the area of the GaAs that contacts the ohmic metals. The resistance is approximately equal to the ratio of the specific contact resistance to the area of the geometry, assuming uniform current distribution.

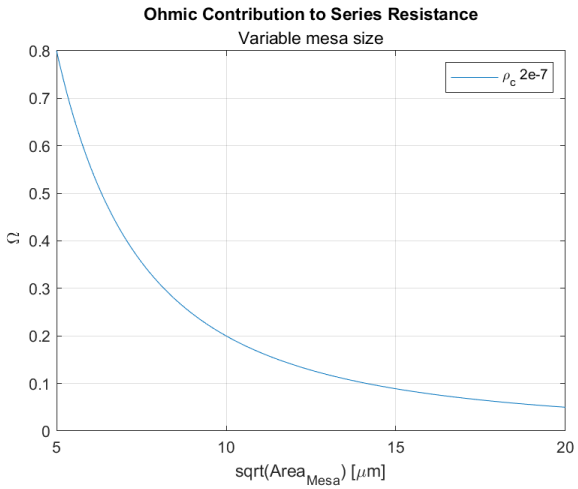
DC Resistance due to the

Ohmic contact area

$$\frac{\rho_c}{A_{ohmic}}$$



(a) Resistance due to the ohmic contact area. Multiple traces are shown representing the different specific contact resistance values.



(b) Resistance is due to the ohmic contact area, which only shows the specific contact resistance approximately equal to the measured results in the TLM section.

Figure 34 – Ohmic contribution to series resistance

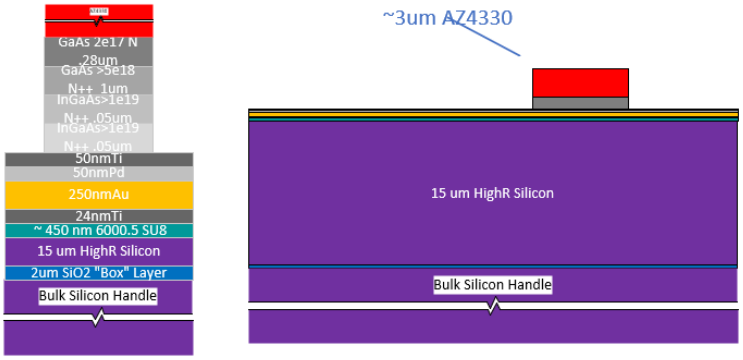


Figure 35: This figure captures the side profile of the GaAs mesa defined after the citric based etch. The thickness of the stack will be the film thickness plus the height of the mesa, which, in the case of the varactor material with .28um epitaxy thickness, corresponds to 3.3um+1.38=4.68um.

Photolithography and a citric-based etch form the GaAs mesas. The previous (before this dissertation was undertaken) process flow of this diode structure called for etching the ohmic layer first. Lithography and a GaAs etch are used to define the ohmic metal pad size, using an H_2SO_4 based etch. A second lithography and GaAs etch defined the GaAs mesa. Challenges that arose with the previous process include over-etching of the ohmic metal layers encroaching on the area of the mesa, which increases the resistance by shrinking the ohmic contact area. Performing the mesa etch first was therefore explored so that it would be protected during the ohmic etching and hence would reduce the number of GaAs etches in the fabrication flow.

This new process starts with a GaAs etch, e.g., "the mesa etch." A positive tone AZ4330 photoresist is spun at 4 KRPM, resulting in a film thickness of ~ 3.3 µm, where the edge bead and residual backside resist are removed with a reagent alcohol-wetted swab. This is followed

by a 110°C "softbake." A SUSS MABA6 contact aligner is used, with a narrow-band i-line filter installed, to deliver 250mW/cm^2. AZ400K developer is diluted with four parts of deionized water and used to develop the features, taking approximately 1 minute 30 seconds (including 20 seconds of overdevelopment after the "flash" when the resist features first appear). The wafer is developed in a two-step wafer-wafting process with one minute in the first beaker of developer and approximately 50 seconds in the second beaker. The wafer-agitation method consists of gently moving the vertically oriented wafer back and forth (wafting) in the beaker. The developer solution consists of accurately measured 600 ml of water and 150 ml of AZ400K, poured into a 1 l narrow-mouth polyethylene reagent bottle, and vigorously mixed, either by hand or stir bar. After development, a wafer hardbake is performed: 1 minute at 110° C and 3 minutes at 130°C. The soft bake, hardbake, edge bead/backside cleaning, and wafer-wafting development procedures are standardized for the rest of the processes and will not be described in subsequent sections.

Figure 36 shows an image captured from a scanning electron microscope. In contrast to the mesa shown in Figure 17, there is no undercutting, and the surface roughness is acceptable, which was determined through testing of the diode, data shown in subsequent chapters. The surface roughness of the mesa was not measured.

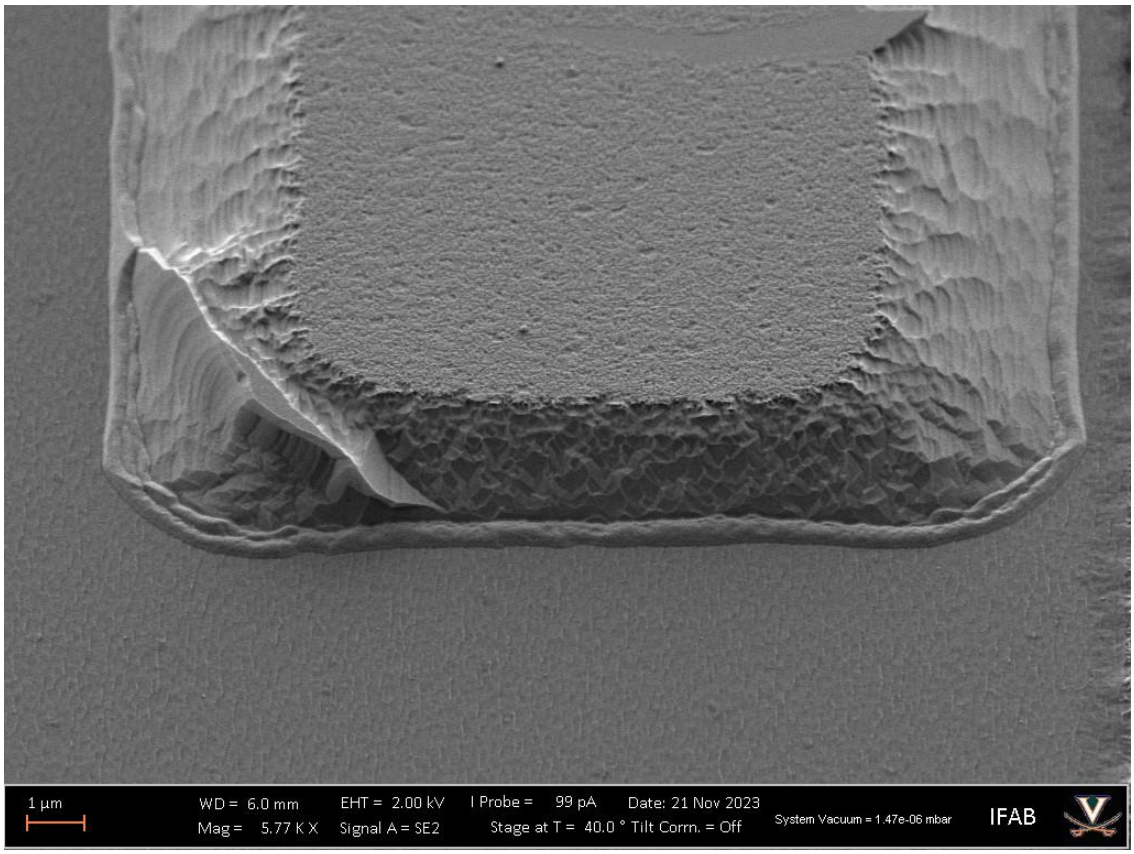


Figure 36 – Scanning electron microscope measurement of the mesa pad after the citric-based etch.

2.2.4 Ohmic Etch

Ideally, the ohmic contact should not significantly perturb the device's performance. The ohmic contact can support the required current with a voltage drop that is sufficiently small compared with the drop across the active region of the device, as discussed in section 2.1

The previous UVA ohmic etch procedure consisted of various "dry" (e.g., plasma) and "wet" (e.g., chemical solution) etches that were used to define the ohmic metal layer stack. The

ohmic metal layers consist of Ti, Pd, and Au. The ohmic metal layers establish the ohmic contact, which TLM characterized; results are shown in the beginning of this chapter, section 2.1. The previous ohmic process was not very selective in terms of photoresists and Silicon. The previous process: AZ4330 is spun at 4K RPM. After hardbake, the wafer is O_2 plasma etched to remove residual resist that could cause undesired masking during the subsequent etch. After the O_2 etching, the wafer is placed into a Semigroup reactive ion etcher (RIE) for a Ti etch with a CHF_3 (5 sccm), SF_6 (20 sccm), and N_2 (0.6 sccm) etch at 35 mT and 80 watts of RF power with a resulting rectified stainless steel substrate platter self-bias voltage of -300V. The wafer was placed in a plastic Petri dish on the stage to reduce the redeposition of back-sputtered material from the platter onto the wafer. After Ti layer removal, the Pd layer is exposed and ready to be etched; the wafer was subjected to a wet etch consisting of 2 parts Transene type A gold etchant and 1 part DI water for 10 seconds until the Pd layer was visibly removed. The Au layer is then removed by using a 60-120 second "HG" Au etchant (consisting of reagent alcohol, ammonium iodine, iodine, and DI water) developed at UVA. The wafer was next reloaded into the Semigroup RIE, and the aforementioned CHF3/SF6/N2 RIE etch process was used to remove the next layer of Ti. Following this second Ti etch, the revealed SU8 layer was etched with a CF_4 (23 sccm), 26 mT, RF 300W, with a resulting DC self-bias of -787 V.

One challenge imposed by the "HG" gold etch is due to the reagent alcohol that acts as a surfactant is included to improve the wetting of the wafer surface, which also tends to dissolve the resist. Even though the resist is hardened during hardbake, alcohol content causes the final feature size, defined by the resist, to be smaller than designed after the etch. Typically, a

significant over-etch is also required to etch the field of Au. This can lead to an inconsistent amount of Au undercutting relative to the resist feature across the wafer.

The existing Ti etch, and SU8 dry etch times were seemingly nonrepeatable, requiring frequent unloading and reloading of the wafer for visible inspection of etch progress. It also resulted in significant metal, resist, and fluorocarbon byproduct residue on the field of Silicon on the wafer.

The below figure shows the cross-section for the ohmic etch process step.

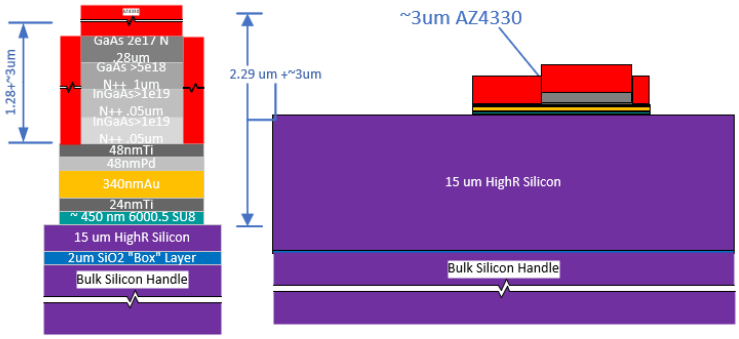


Figure 37 – Cross section of chip in processing showing ohmic etch defined geometry.

In this work, the process of etching the ohmic stack was simplified. The CHF3/SF6/N2 chemistry used to etch Ti was replaced with CF4/Ar. Several test samples composed of Si/Su8/Ti/Pd/Au/Ti were made by spinning on a thin layer of SU8 and curing using the same method mentioned in the bonding section. The ohmic metals Ti/Pd/Au/Ti, were deposited by Ebeam evaporation. The CF4/Ar approach was derived from the work of [47-50], where it is

noted that CF4/Ar chemically and mechanically etches the Ti, where the F forms volatile products with both the Ti and TiOx, and Ar increases the available energy of the etch and also helps remove various fluorocarbons and TiF. It was found that the same etch procedure could be used to remove the SU8, since the etch rate of Si with CF4/Ar is low (< 20 nm/min); because of the high selectivity, the Si serves as a suitable etch stop since slightly etching the Silicon doesn't destroy the performance of devices.

The resulting Ti and SU8 etch is CF4 (20 sccm), Ar (10 sccm), RF 150 Watts, and 30 mTorr with a corresponding rectified platter self-bias voltage of -460 V. The etch rate of Ti is 5.9nm/min. A quartz platter is used on the stainless-steel stage, with the wafer placed in a 110mm plastic petri dish. Adhesive thermometers were attached to the wafers, it was found that this etch can exceed 200°C for etch times greater than 5 minutes. The concern with a high-temperature etch is that you can burn the SU8 layer, making it virtually impossible to remove. In addition to burning the SU8, the etch rate of the titanium and the photoresist increases with temperature. For these reasons, the etch was implemented in cycles of 3 minutes of etching / 3 minutes of cooling (with gas on but RF off). The etch rate of Ti is 5.9nm/min. The existing UVA process using "HG" Au etchant for etching Au was replaced with a Transene Type-A based approach and then subsequently adapted by changing the etchant dilution from 2 parts Tranense Type-A gold etch: 1 part DI water, to 1 part Tranese Type-A gold etch: 1 part DI water. This more diluted etchant reduces the Pd and Au etch rates, offering more control and less undercutting when the wafer is etched until it's visibly clear of Au. Eliminating the HG-Au solution also proved beneficial since the reagent alcohol tends to dissolve the photoresist, providing more consistent results for defined precise geometries matching design. The

underlying Ti serves as a natural etch stop. The following set of figures shows the results; Figure 38 shows an SEM measurement after the ohmic etch and resist strip. The image shows there is residual resist that still needs to be removed, which was subsequently completed after this image was taken. Figure 39 shows just one of the ohmic pedestals shown in Figure 38; however, the stage is titled to 40°, and the magnification is increased to access the etch profile, namely undercutting. Figure 39 shows that the first and last etch of Ti, have no or very minimal undercutting; this is due to the dry etch process. However, the intermediate layers sandwiched between the two titanium layers does show undercutting. This undercutting is due to the isotropic nature of the wet etch used to etch the Au and Pd layers. This undercutting of Au and Pd can be minimized in future work by switching to a dry etch instead of a wet etch.

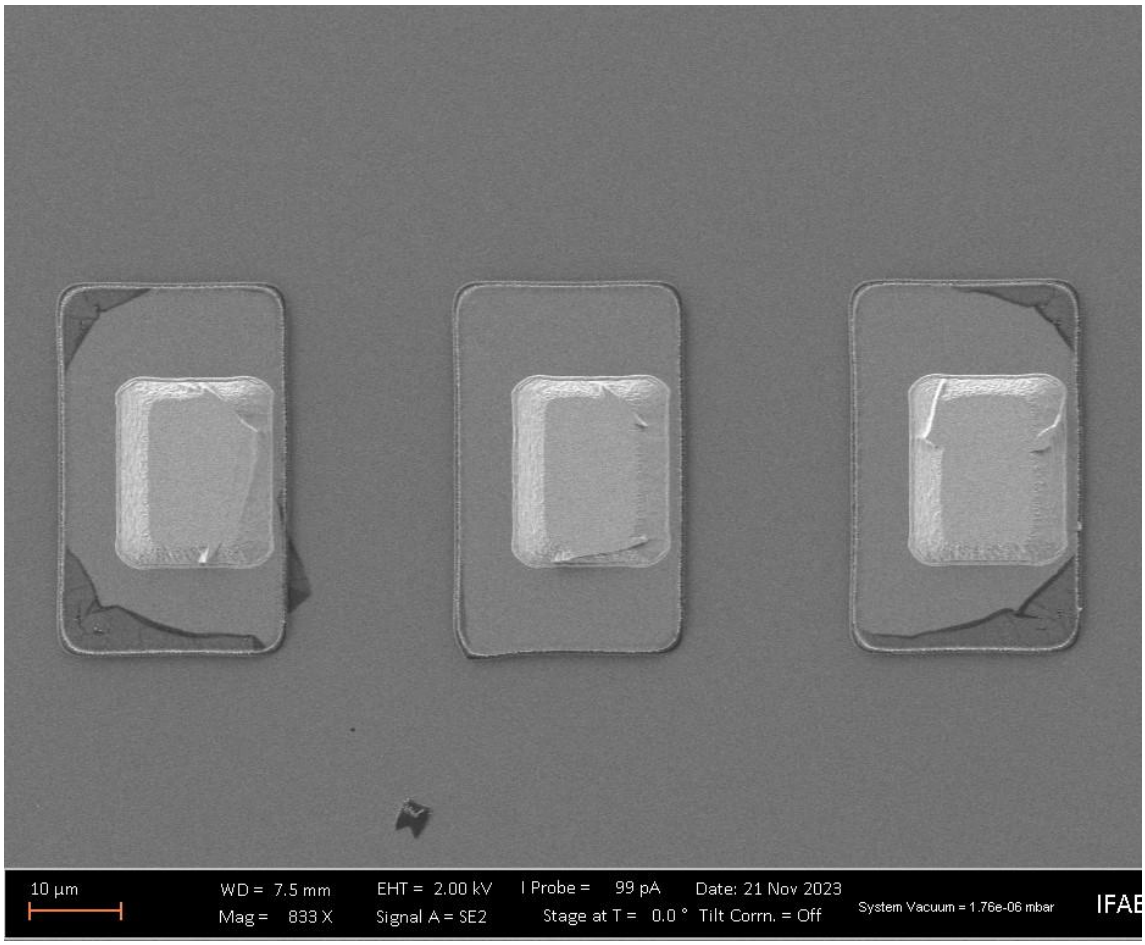


Figure 38- This SEM measurement shows the mesa and the ohmic layers

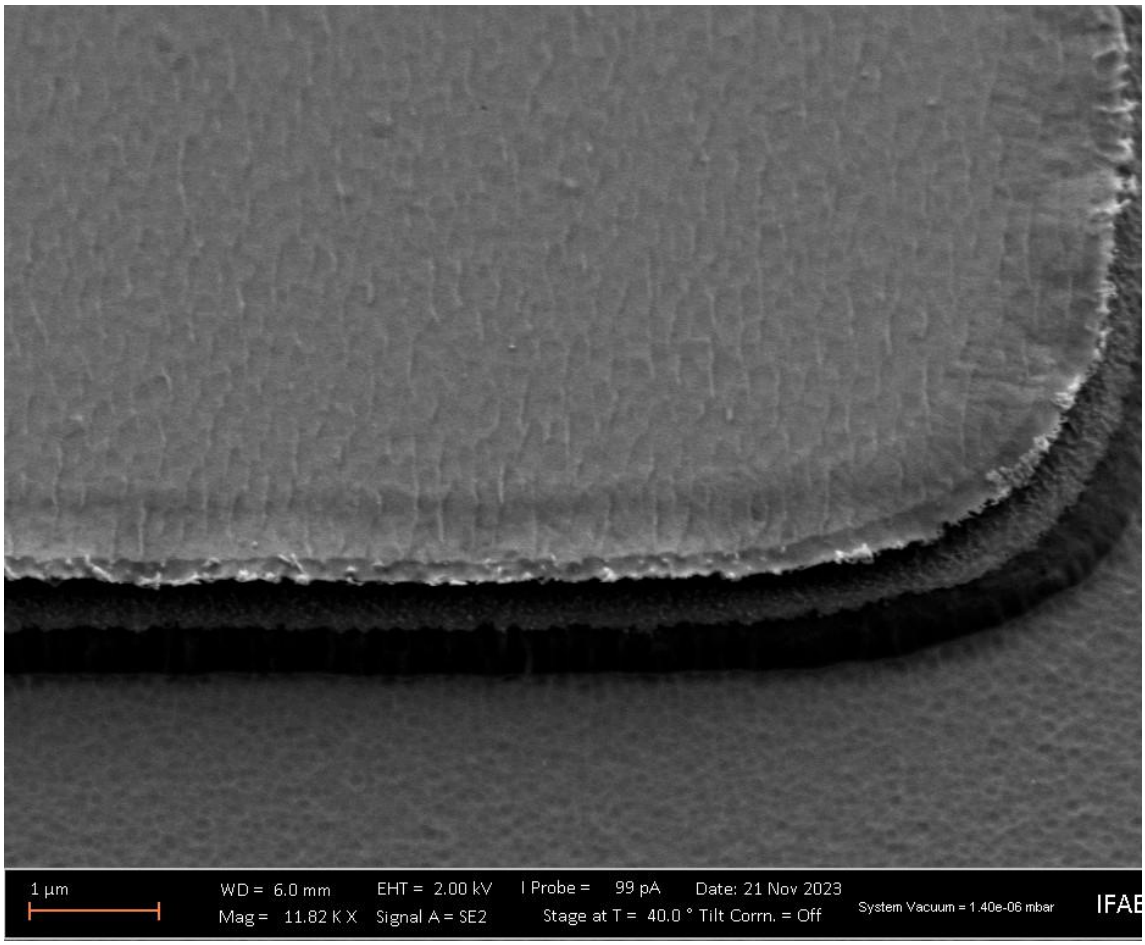


Figure 39 – Side profile of the Ohmic etch

2.2.5 Via Formation

The SOI via process was adopted from previous UVA processes. Lithography with AZ4330 resist spun at 3K RPM is first performed to define areas to be etched. The developed resist is hard baked at 110°C for 60 seconds and then 130°C for 180 seconds. After the hardbake, the wafer undergoes O2 plasma cleaning (standard processing conditions) for 10 minutes. The vias in the 15 µm Si layer are formed through a silicon Bosch etch. The silicon-on-insulator (SOI) wafer has a 1-µm thick silicon oxide insulating layer that serves as an etch stop for the Bosch Si etches. The etch rate for the Bosch etch is approximately 1 µm per cycle. The Silicon's device layer is 15 um thick; thus, ~20 cycles should completely etch through the Silicon; however, 40 cycles are used to ensure no residual silicon is left in the vias (particularly around the perimeter of the via). Figure 40 shows the cross-section of the chip after the via etch, showing the photoresist masking all areas except for areas to be etched and the 1um thin SiO2 etch stop layer.

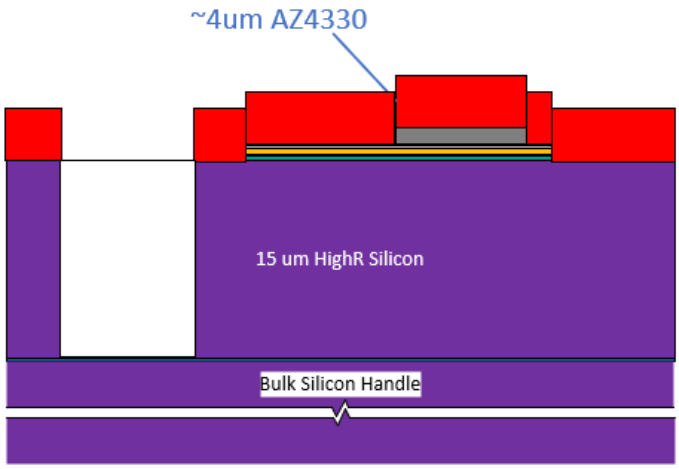
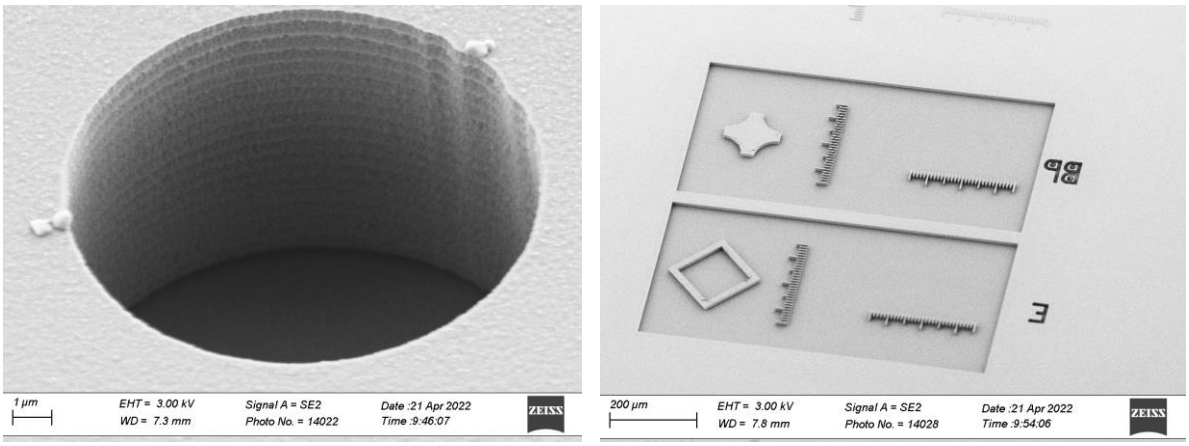


Figure 40 – Cross section of chip in processing showing via etch defined geometry.



(a) (b)

Figure 41 – (a) Sem Measurement showing via etch—the scalloping results for the two-step Bosch process.

(b) Sem measurement is shown via step-defining backside alignment markers.

2.2.5 Sacrificial Resist, (Exvia/Plateburn), and Metalization.

The existing UVA sacrificial resist step was also adapted for this work. A positive AZ4210 resist is spun at ~ 4K rpm to ~2 μm thickness, corresponding to the desired airbridge height. After spinning and soft baking, the photoresist, a >1hr rehydration pause is used to account for the thicker resist found in the 15um via holes; otherwise, the photo-chemical reaction, which requires some minimum amount of water, will not clear all the resist out of the via. After rehydration, the wafer undergoes an extra-via/plate burn exposure, using a mask designed explicitly with features slightly larger than and aligned to the vias, and then a development step, which is approximately the same dimensions as the via step.

This exposure is set up as a cycled exposure with periods of 101 seconds exposure and 120 seconds of wait time until a total of 600 mJ/cm^2 has been achieved. This results in features shown in Figure 42 below.

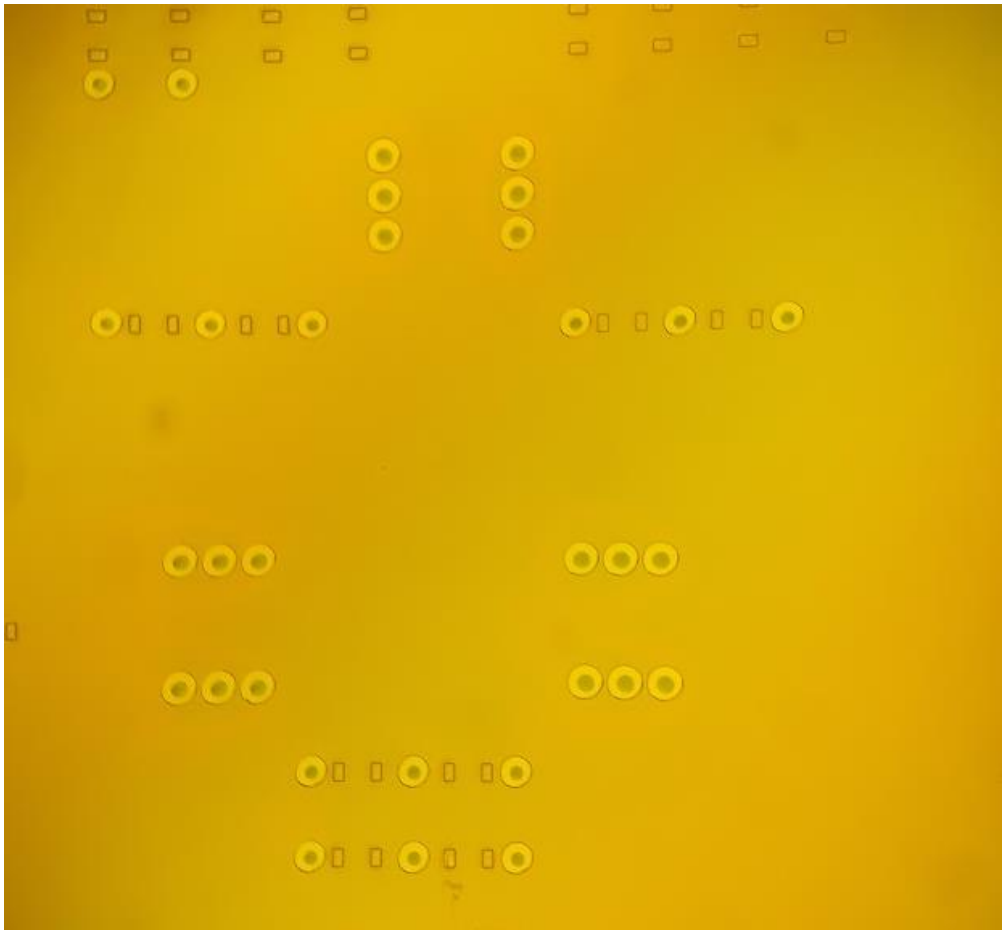


Figure 42- Image showing the results of the ex/via plate burn step

Figure 42 shows lithographic features larger than the vias (small blue circles). The blue circles are the 1um thick SiO2 etch stop layer beneath the 15um thick high-resistivity silicon.

This increase in size is due to the light guiding through the photoresist. The more power delivered during the exposure will increase the diameter of the features made during this step; therefore, the lithography was tuned by starting with >600 mJ/cm^2, and slowly reducing the power

until the exposed areas were not encroaching onto the ohmic metals features, as shown in Figure 42.

After development, a second exposure with the sac-resist mask forms the sacrificial resist layer that defines the anode, the region that the airbridge will sit on, the transmission lines, and the beam leads. A post-exposure bake of 90°C for 180 seconds is **critical** because other photoresist regions have already been exposed, and we don't want to over-develop those feature sizes. It was found during this work and in a previous work that HMDS can be used for improved photoresist adhesion to the GaAs. However, AZ400K or O2 plasma will subsequently be required to remove the HMDS from the GaAs region before forming the anode contact.

Nevertheless, after the sac resists lithography, development, and bake, the wafer undergoes 5 minutes of the standardized O2 treatment mentioned above; after the O2 treatment, the wafer is submerged in 1:20 Ammonium Hydroxide: DI water, for 1 minute, with modest wafting, while the wafer is held with a tweezer. Immediately after the ammonium hydroxide, the wafer is loaded into a uva homemade magnetron sputtering machine, nicknamed the "Sputt-3," performed using the homemade magnetron sputtering tool. Figures 44 through 46 show SEM images of this completed process.

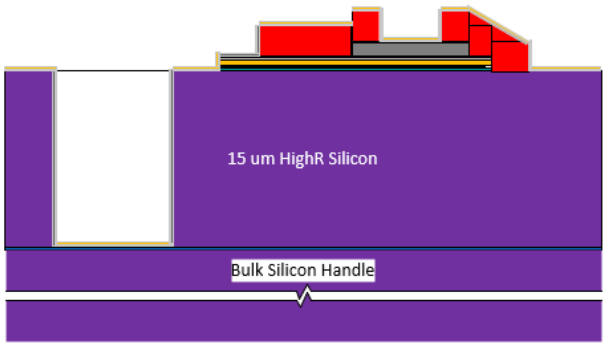


Figure 43 - Cross section of chip in processing showing SAC Resist defined geometry, and the seed layer to be discussed below this figure.

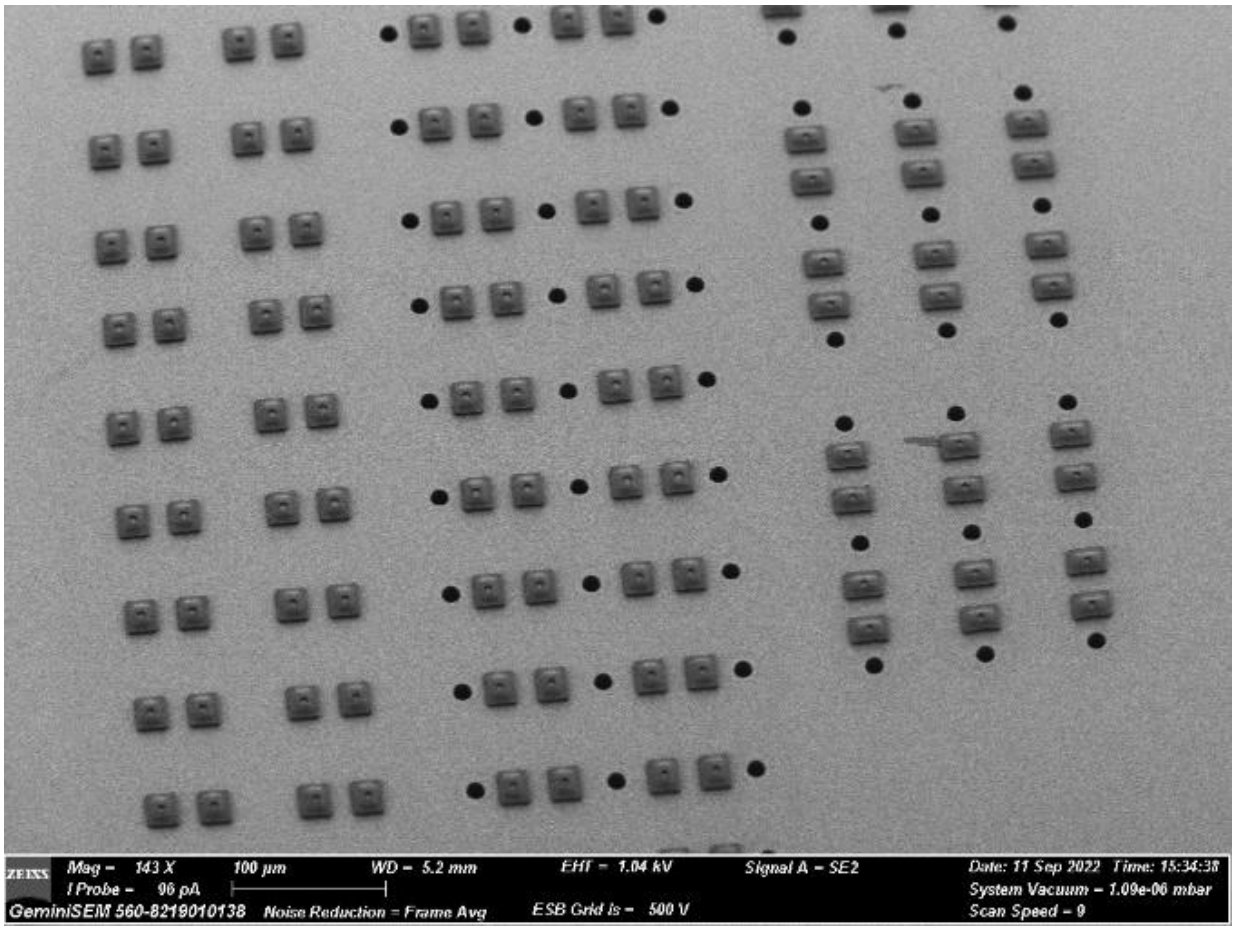


Figure 44 - Sem measurement showing the result of the Sac resist process.

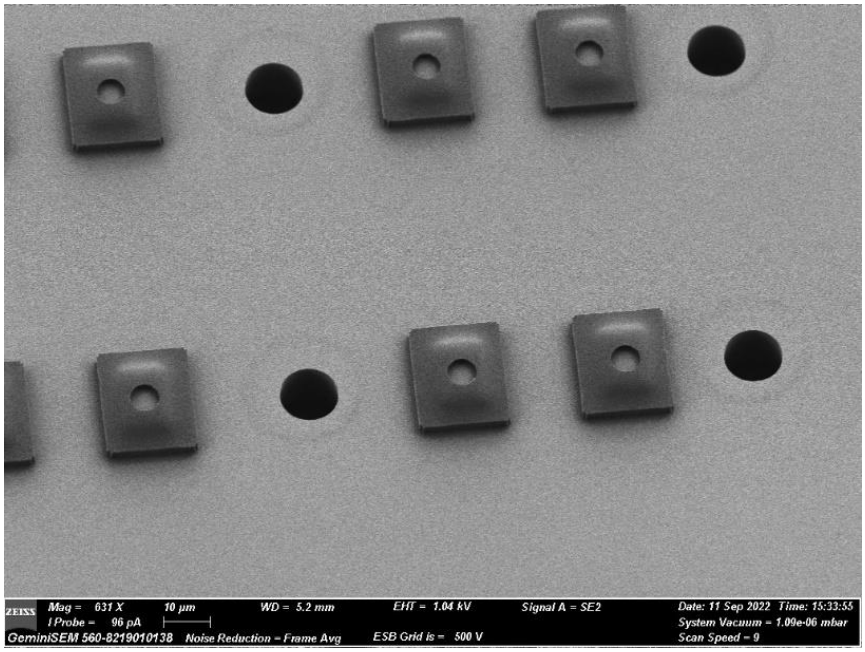


Figure 45 - SEM measurement showing the result of the Sac resist process.

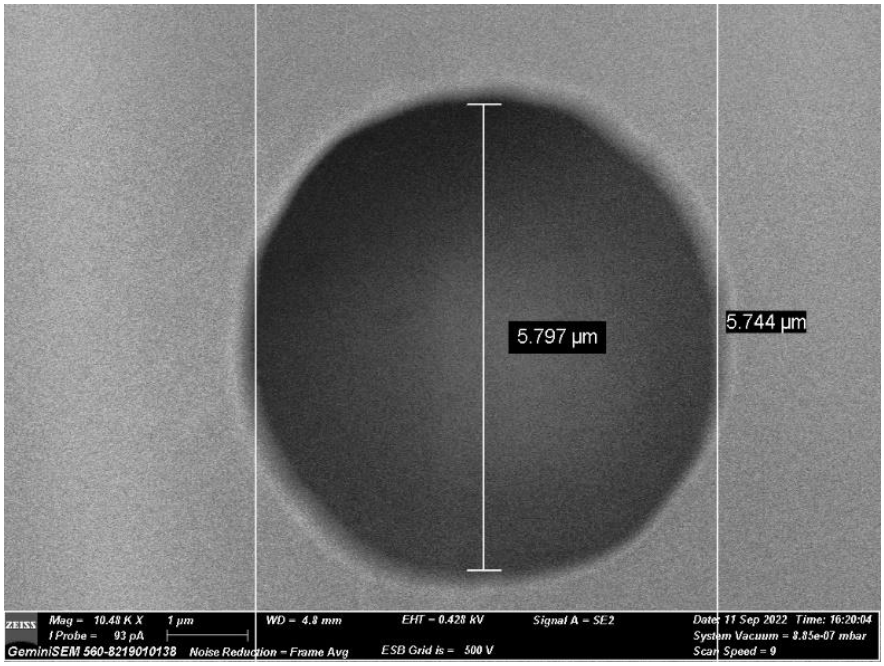


Figure 46 - SEM measurement measuring verifying the dimension of a 5.7um diameter anode.

2.2.6 –Electroplating

The sacrificial resist lithography defined the anode area, airbridge, transmission lines, and beam lead features. These features are defined with 3 μm thick plated Au metallization.

A positive AZ4330 resist is spun at ~ 3rpm to ~4 μm thickness, corresponding to the desired airbridge height. After spinning and soft baking, the photoresist, a >1hr rehydration pause is used to account for the thicker resist found in the 15um via holes; otherwise, the photo-chemical reaction, which requires some minimum amount of water, will not clear all the resist out of the via. After rehydration, the wafer undergoes an extra-via/plate burn exposure and then a development step, which is approximately the same dimensions as the via step.

This exposure is set up as a cycled exposure with periods of 101 seconds of exposure and 120 seconds of wait time until a total of 600 mJ/cm^2 has been achieved. This results in features shown in Figure 42.

Electroplating is performed to realize the thick Au metalized features. Electroplating requires a conductive surface on the wafer to serve as the cathode for the plating circuit. The plating setup is shown in Figure 47 below. A Pt-coated Nb mesh is used for the anode; both the mesh and the wafer are submerged into a plating solution, and a power supply sets a constant current. .68 mA of current is set constant and corresponds to approximately .6 volts.

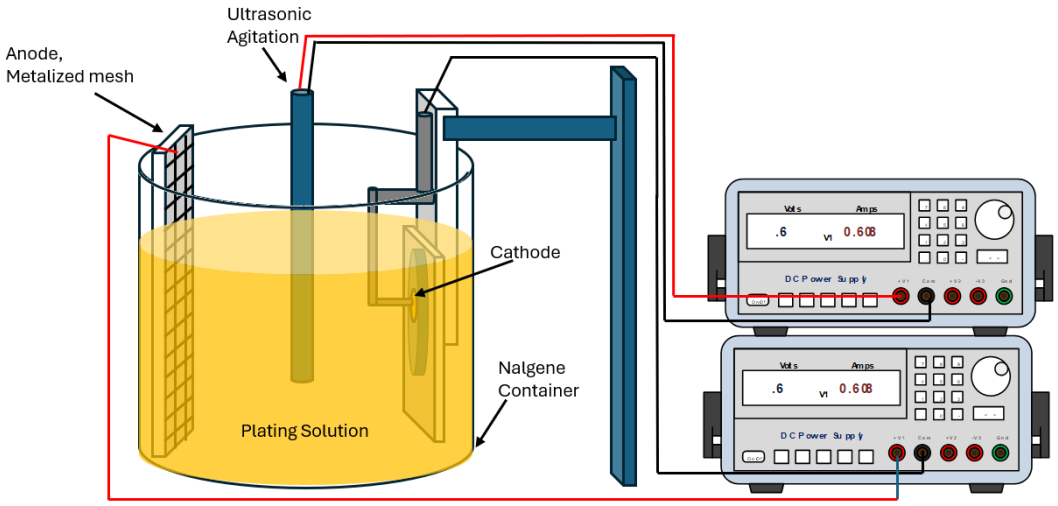
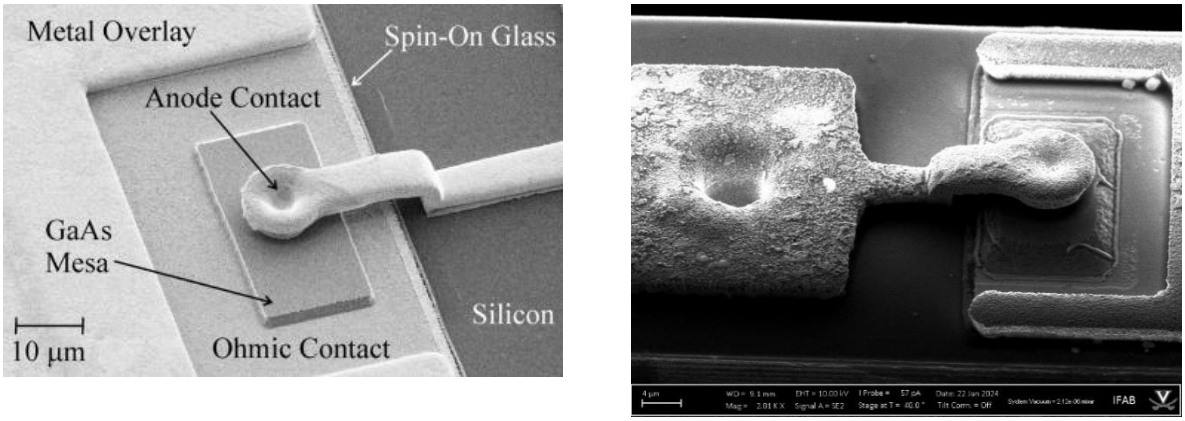


Figure 47 - Electroplating diagram

Once the sacrificial resist is defined, a pretreatment of diluted 20 parts water:1 part ammonium hydroxide is performed immediately before loading into a vacuum chamber for magnetron sputtering. Thin layers of Ti (~15nm) and Au (~30nm) are deposited on the wafer. Magnetron sputtering is used to realize sidewall metallization. This film forms the Schottky contact and serves as a seed layer for electroplating the various features to be metalized. Lithography defines the topside metallization, e.g., beam leads, transmission lines, side-coated vias, and transmission lines. O2 plasma is used after lithography before electroplating of the ~ 3.5 µm Au layer. Technic 25ES gold solution, heated to 50° C through a 50°C water bath, is used with light ultrasonic agitation and a magnetic stir bar (in the plating bath) to ensure a smooth surface finish and side wall metallization of defined vias by keeping fresh electrolyte at the plated surface. The movement of the electrolyte also helps clear hydrogen gas bubbles resulting from the chemical reaction at the surface, reducing "pitting."

The primary difference between this plating process flow (developed in this work) and the previous UVA process flows is the use of ultrasonic agitation, which helps coat the side walls of the vias. [51] [52] Some previous process flows also used two electroplating steps. However, this was unnecessary; the resulting diodes don't look as "crisp" visually but have comparable performance, which will be a topic of chapters 3 and 4.



(a)

(b)

Figure 48 – (a) Old Process Electroplated features after seed layer removal (b) New Process Electroplated features after seed layer removal.

The plating rate is measured with a companion wafer, with the same features defined and plated immediately beforehand. A mechanical profilometer measures the dummy wafer's plating thickness several times during electroplating. A plating rate is deduced and used to plate the production wafer to the desired thickness without being removed from the solution, which results in a smoother surface.

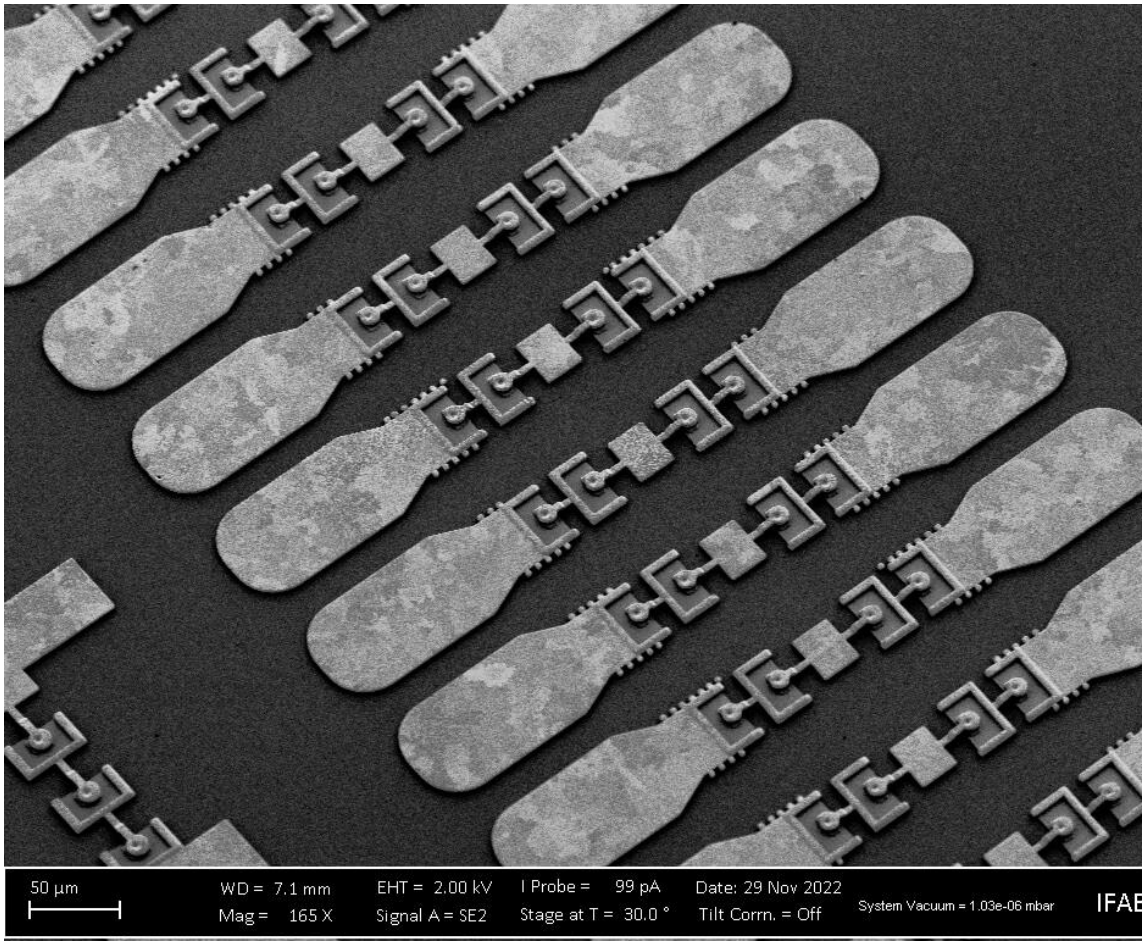


Figure 49 - Figure showing electroplated features.

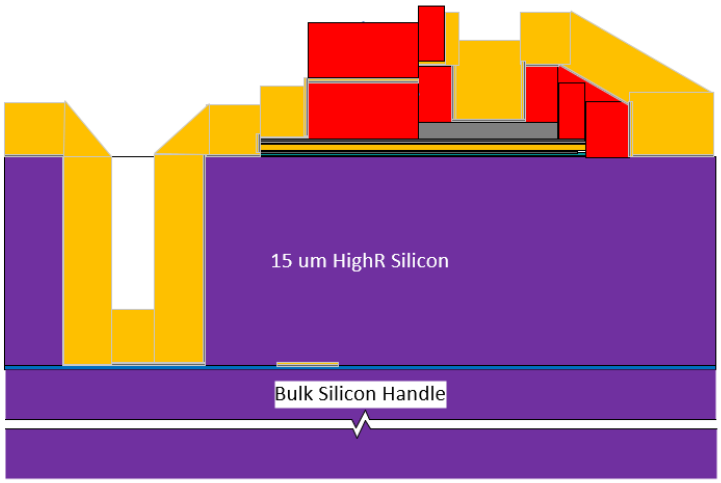


Figure 50 - Cross section of chip in processing showing SAC Resist defined geometry, the seed layer, and the electroplated features, with resist to be removed.

Removing the sacrificial resist and the seed layer is a multi-step process. A 1:1 mixture of acetone and isopropyl removes the top layer resist. Acetone, without isopropyl, is too aggressive and can lead to liftoff of the seed layer, causing deformation of the diode geometry. HG-800 gold etchant is used to remove Au seed layer. HG-800 is used here because it is less aggressive than TFA Gold Etch Type A, and results in a smoother finish; additionally, the alcohol content helps clear any residual resist that the acetone/isopropyl mixture didn't remove. The Ti is removed with three cycles of the Ti etch (detailed in the ohmic etch section). After the Ti is removed, the conductivity of the Si surface is measured using two needle probes; if the resistance is sufficiently high and there are no visible regions of metallization, the wafer is ready for the

sacrificial resist removal. The wafer is subjected to an iline flood exposure; in the MABA6 photo aligner, the dosage isn't precise, the wafer is exposed for 1 minute in order to develop away any photoresist on the wafer, and 4:1 Water/AZ400K solution is mixed. The wafer is submerged in the solution for 4 minutes and then immediately submerged into a mixture of Acetone and Isopropyl; finally, the wafer is subjected to 2 hours of O2 Plasma and imaged using the SEM iteratively until resist is removed from under the airbridges.

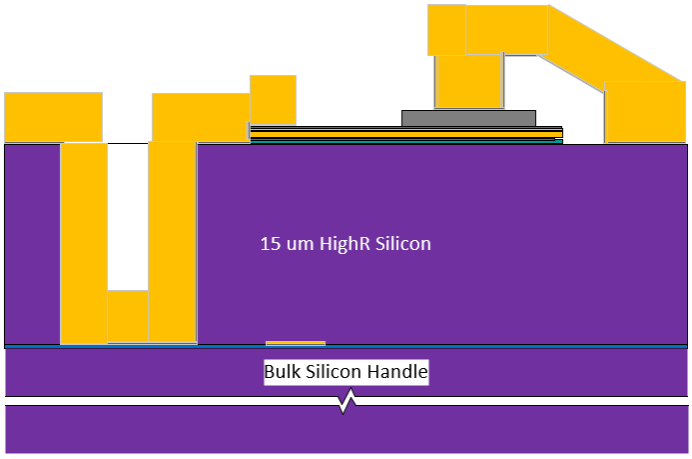


Figure 51 - Cross section of chip in processing showing SAC Resist defined geometry, the seed layer, and the electroplated features, with resist removed.

2.2.7 Backside SOI Processing:

In order to define backside features and to release membrane chips, the wafer needs to be bonded to the carrier wafer so that the SOI's handle can be removed. A combination of

WaferBOND and epoxy was used to create a semi-permanent bond of the SOI/ GaAs-circuit wafer to a Si carrier, allowing future debonding and release of the final chips. The Si handle layer of the SOI was removed through lapping and plasma etching. The SiO_2 BOX layer was removed with a buffered oxide etch (BOE). A microstrip ground plane is formed on the backside of the high-resistivity Si with photolithography, electron beam physical vapor deposition, and electroplating processes. Photolithographic and DRIE processes are used to define the outline of the chips ("extents"), realizing the precise formation of complex chip geometries that would otherwise be impossible through traditional dicing techniques. The finished chips are released through a heated solvent-based debonding process. The backside fabrication process uses Dominion Microprobes's (DMPI) process flow [36], which is a significantly improved version of [46].

2.2.8 Summary of fabrication process:

This enhanced fabrication process addressed several issues associated with the prior QVD process, resulting in an understanding of the specific contact resistance consistency across the entire wafer, eliminating any suspicions that the resistance due to the ohmic contact can be attributed to inconsistent performances and yield. Switching the order of the process from ohmic to mesa first allows us to protect the GaAs mesa during the ohmic process, reduces the number of times we etch the GaAs, and enables more precision fabrication. Optimizing the ohmic etch and removing the relatively volatile SF6 process gas also increases precision. The CF4/Ar etch has higher selectivity with the Silicon than the previous SF6-based etch and has increased selectivity with the photoresist. Replacing the HG gold etch (ammonium iodine, iodine, and alcohol) with TFA gold

etch type A (Potassium Iodine, Iodine, **no alcohol**) allows for higher fabrication precision since alcohol dissolves resist. The side-coated process was realized by optimizing a lithography process to include rehydration and a stepped lithography process to clear out photoresists entrenched in the vias. A custom ultrasonic agitator was created to optimize the electroplating process and ensure that metal was uniformly deposisted on the side wall of the via. In addition to these improvements, each process was characterized by various experiments and details of its components so that future students and researchers would understand the importance of each step.

2.3 Fabrication of Submillimeter-Wave GaAs Quasi-Vertical Schottky Diodes Diffusion Bonded to Silicon

This section presents the first metal-to-metal diffusion-bonded Gallium Arsenide Quasi-vertical Schottky diode heterogeneously integrated onto high-resistivity Silicon.

Coplanar waveguide (CPW) fed quasi-vertical Schottky diodes were fabricated alongside a 25 μm pitch on-wafer calibration kit and characterized with wafer probes and a vector network analyzer from 325-500 GHz. Diode parameters were extracted, and capacitance-voltage and current-voltage were measured for a variety of diodes. Results indicate these diodes are suitable for high-frequency applications and have a high current density capacity, thus allowing their RF characterization under forward-bias conditions.

2.3.1 Motivation for diffusion bonding:

Thermal management of GaAs Schottky diodes is essential for implementing frequency conversion circuits since these circuits generally exhibit relatively low conversion efficiencies driven by high-power low-frequency sources to realize usable output power in the submillimeter-wave spectrum. The quasi-vertical Schottky diode potentially offers advantages in terms of thermal management compared to planar, lateral-ohmic contacted devices. This advantage is due to the relatively large ohmic area buried beneath the Schottky contact and the subsequent current flow through the spreading resistance profile. A comparison between the lateral-ohmic contacted devices and the QVD will be a topic of Chapter 4. Nadri first reported on the thermal characterization of heating in the heterogeneously integrated quasi-vertical diode using thermoreflectance as a diagnostic tool [53]. His work included deducing a thermal circuit representation, shown in Figure 52. The thermal properties of the various materials in this circuit are shown in Figure 53.

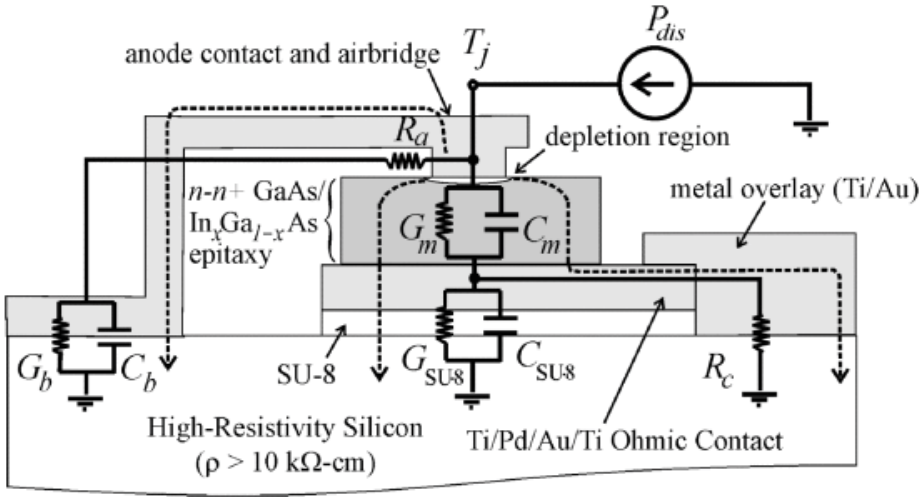


Figure 52 – Thermal circuit representation of diode stack

Material	Thermal conductivity (W/m K)	Thermal capacity (J/Kg K)	Mass density (Kg/m^3)
Diode Stack	<44	350	5320
Plated gold	214	129	19300
SU-8	0.25	-	-
Silicon	124	-	-

Figure 53 – Thermal material parameters for Diode stack

Figure 53 shows that the SU-8 has a much lower thermal conductivity than the layers it is sandwiched between. Souheil referenced work with AlN and diamond to use as low-less heat spreading substrates; however, the bonding interface will still limit heat spreading capability; thus, the motivation of this work is to engineer a new bonding interface and subsequently

enhance the thermal capability of the circuit; namely, it's ability to sink heat. Figure 54 shows an Ansys ICEPAK simulation with identical excitation and shows that the maximum temperature rise is 8°C, which is different between the diode with SU8 as a bonding layer and an Au diffusion layer.

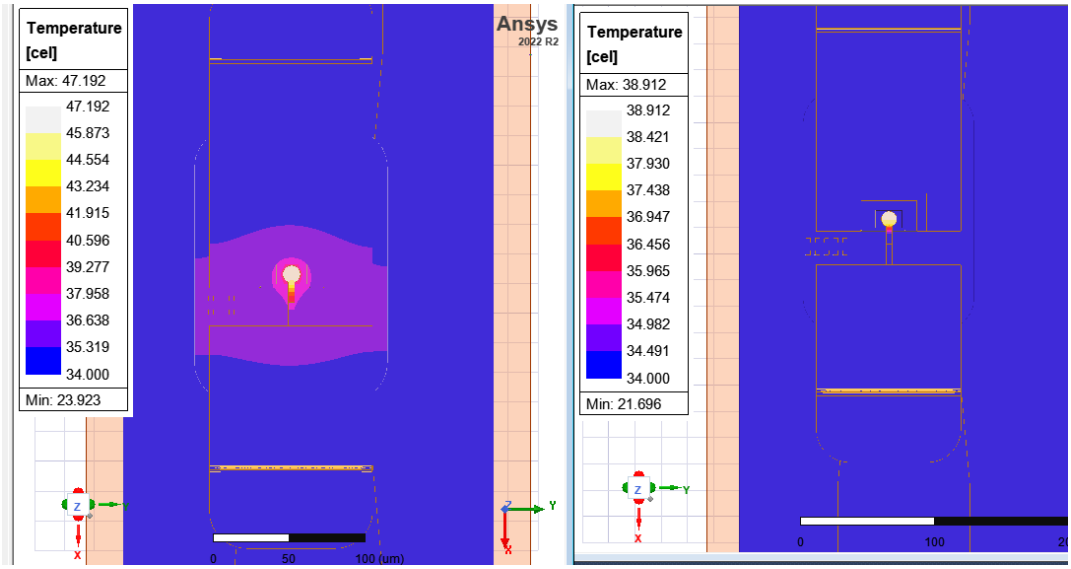


Figure 54- (a) QVD diode with SU8 as bonding interface (b) QVD diode with Au as bonding interface

2.3.2 Determining bonding parameters for metal-to-metal bonding

The first experiment was set up to determine if metal-to-metal bonding was possible using readily available, inexpensive bulk silicon wafers. 20nm of Ti and 250nm of Au were deposited on both wafers using EBPVD. The cross-section of these wafers is shown in Figure 55.

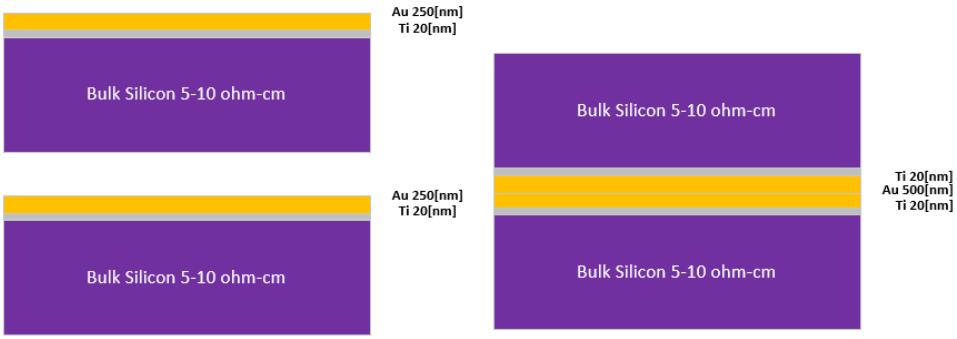


Figure 55 – Cross Section of the first experiment for diffusion bonding.

Bonding was performed using the SUSS Microtech wafer bonder, using the recipe shown in Figure 40; the size of the top wafer was roughly 1" x1", corresponding to a wafer pressure of 46.5 bar. The temperature used for bonding was 350°C.

Step	Top Temp (°C)	Bottom Temp (°C)	Chamber Press (mBar)	Tool Force (N)	Process time (hh:mm)
1	100	100	Purge	0	0:30
2	350	350	6.75E-5	0	0:30
3	350	350	6.75E-5	0	0:30
4	350	350	6.75E-5	3000	3:00
5	350	350	6.75E-5	3000	0:59
6	100	100	6.75E-5	0	0:30
7	100	100	6.75E-5	0	0:30

Table 5 - Initial Bonding Recipe

After bonding was completed, the wafer was diced in to access the bonding interface. Figure 56 shows the diced wafer mounted onto a fixture intended for loading into the scanning electron microscope.

Figure 56 – The diced wafer mounted for SEM imaging.

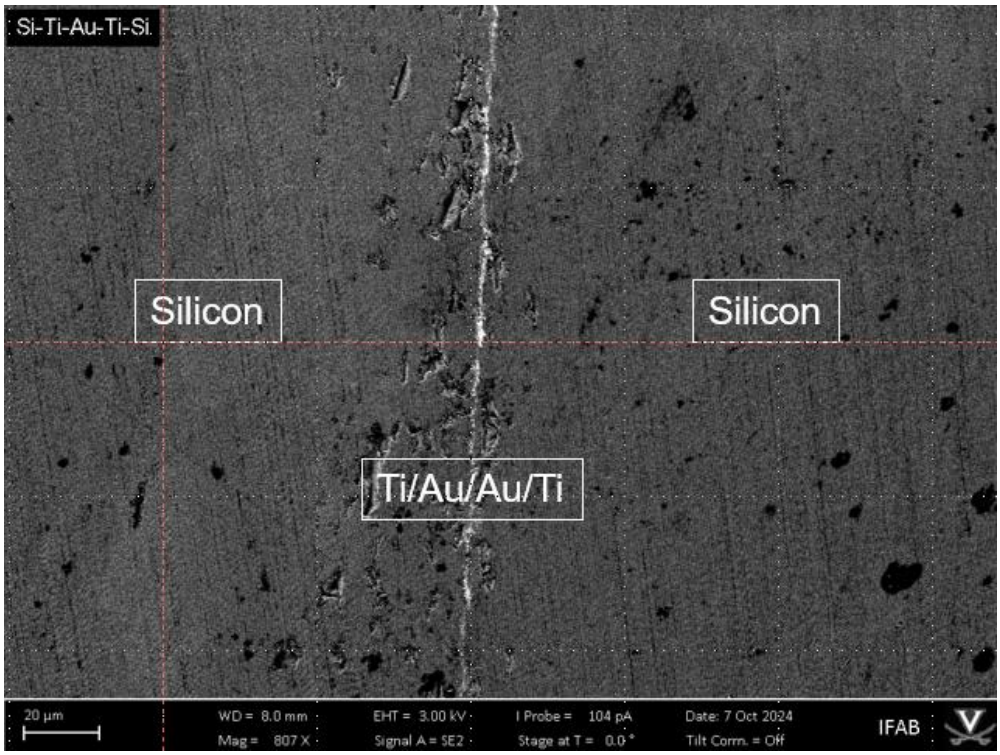


Figure 57 – Scanning Electron Microscope measurement showing the bonding interface.

This initial experiment demonstrated that metal-to-metal bonding was achievable using our tool and provided a set of initial conditions for bonding more complex materials, such as SOI and GaAs. The SEM measurement in Figure 57 shows a relatively continuous Au interface between the two wafers. The defects are likely due to dicing and the subsequent coarse lapping. These defects could be reduced using a finer grit lapping paper or a focused ion beam (FIB) for cutting. However, for this work, the dicing reveals a single layer of Au, with no distinguishable separate layers, indicating a sufficient bond.

We designed the following experiment to evaluate the potential improvements from changing the bonding interface from SU8 to Au. The experiment involves bonding two SOI wafers to a double-sided polished silicon wafer. Thin SOI wafers are used for two reasons: 1) to facilitate assessing the bond quality by removing the handle layer, leaving only a thin layer of Silicon, which allows for the observation of any blisters (i.e., unbonded regions), and 2) to enable steady-state thermoreflectance measurements for comparing the temperature rise of the SU8-bonded sample with that of the metal-to-metal bonded sample.

A double-sided polished high-resistivity silicon wafer, >10k cm-ohm, and a silicon on insulator wafer, with a 3um device layer, was prepared by dicing both into squares; the double-sided polished silicon wafer was diced to be larger than the SOI wafer. Metal evaporation was performed to deposit a 20 nm layer of Ti and a 250 nm layer of Au. After metal deposition and SU8 application, the wafers are bonded together. The SU8 bonding procedure is the same as shown in Section 2.2.1, and the metal-to-metal bonding procedure is shown in Table 5After bonding, the silicon handle is removed using a combination of dicing and dry plasma etching. The SiO2 layer is removed by submerging the wafer in 51% HF. Figure 58 shows an abbreviated fabrication process for this experiment.

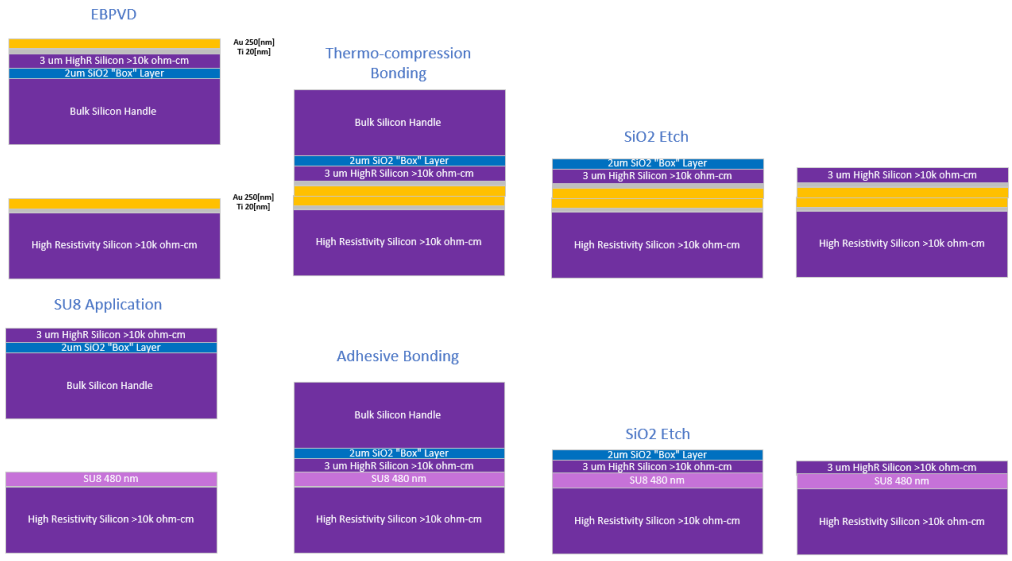


Figure 58- Abbreviated fabrication process for this SU8 vs. metal-to-metal experiment.

An example of the resulting metal-to-metal bonded wafer is shown in Figure 59. This image shows a blister-free bond.

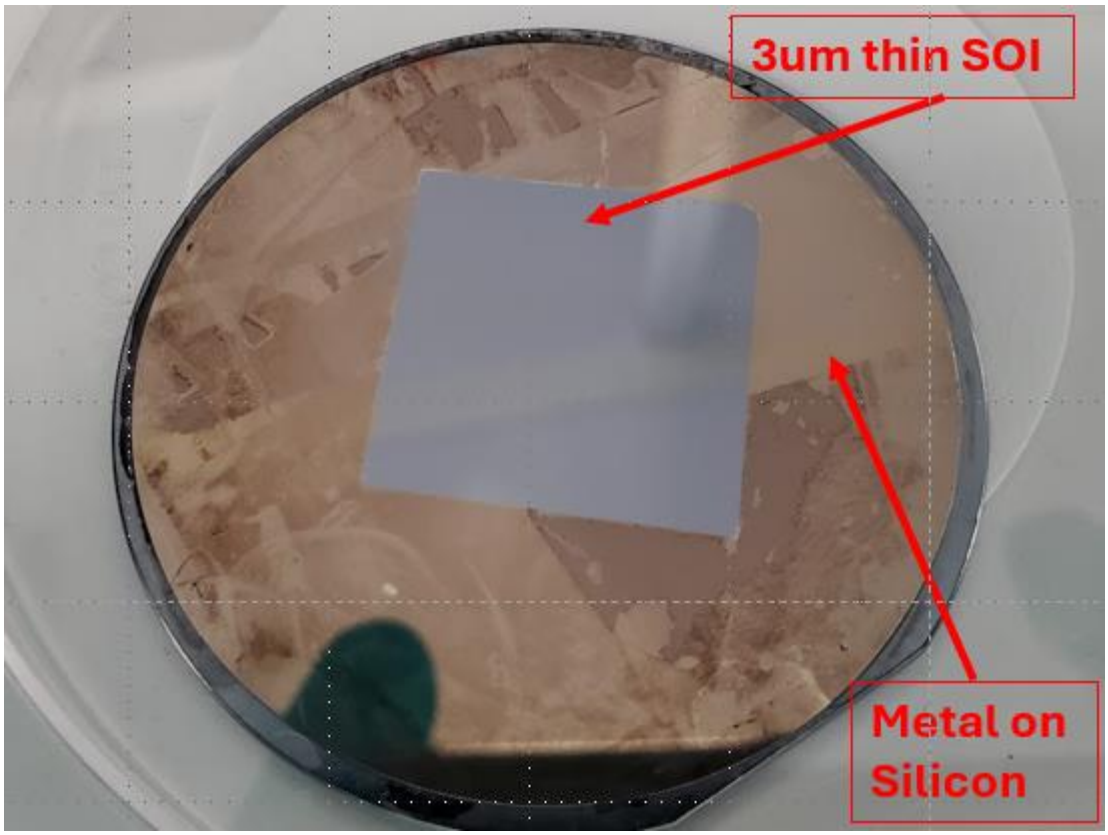


Figure 59 – Blister-free high resistivity silicon formed by diffusion bonding metal layers and then thinning the Silicon on the insulator

These prepared samples were provided to Laser Thermal. Laser Thermal used Steady-State Thermoreflectance in Fiber Optics (SSTR-F) to measure the temperate rise vs pump power. From the datasheet of the SSTR-F, "Steady-state thermoreflectance-based optical pump-probe technique to measure the thermal conductivity of materials using a continuous wave laser heat source. The technique works in principle by inducing a steady state temperature rise in a material via long enough exposure to heating from a pump laser. A probe beam is then used to detect the

resulting change in reflectance, which is proportional to the change in temperature at the sample surface. Fourier's law is used to determine the thermal conductivity by increasing the power of the pump beam to induce larger temperature rises." The results from this measurement are shown in Figure 60.

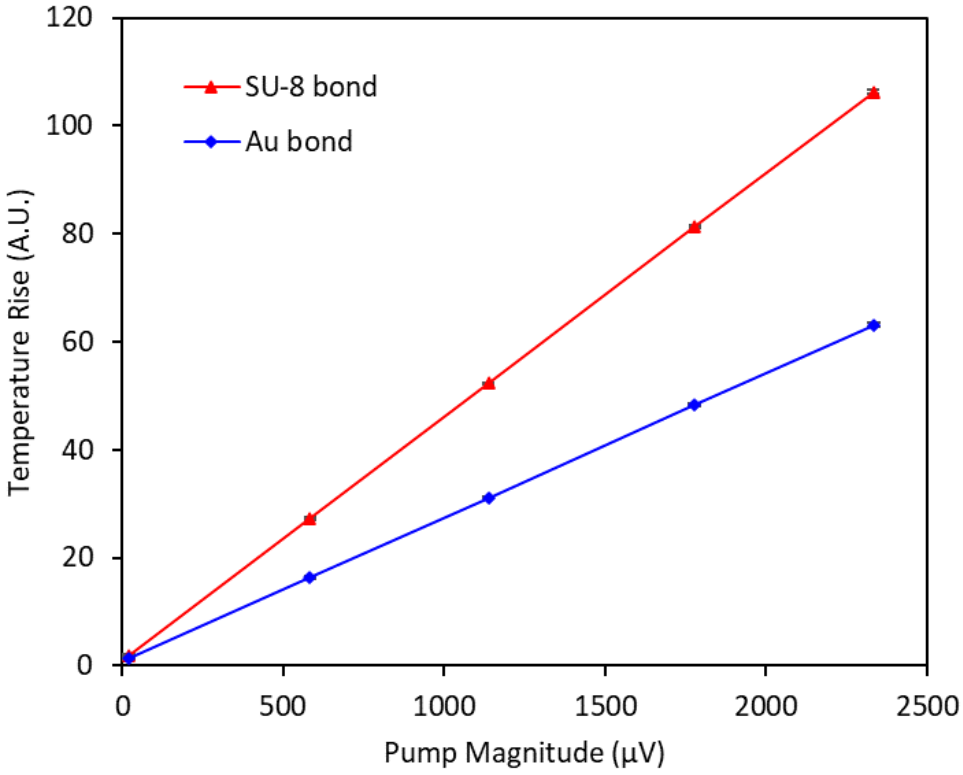


Figure 60 – Temperature Rise vs. Pump Magnitude for SU8 vs metal-to-metal bonded samples

The results from the SSTR-F measurement confirm the hypothesis that the metal-to-metal interface has an advantage over the SU8. The new interface addresses the low thermal conductivity of the SU8.

The initial experiments established the bonding parameters and compared the SU8 interface to the metal-to-metal interface. These results formed the foundation for attempts to fabricate a QVD using the new diffusion bonding method. The first approach involved using the same bonding recipe developed for the bulk Silicon and SOI wafers to bond GaAs to Silicon. However, this led to two primary challenges: 1) Cracking of the GaAs, and 2) Complete delamination of the wafer from the Silicon during the thinning process. These issues appear interconnected, as severe cracking across the wafer can result in an uncontrolled etch due to the isotropic nature of the nitric, citric, and HF wet etches. The first measure to solve these issues was to reduce the force gradually, e.g, the wafer pressure, until cracking was tolerable, which for this work was primarily based on intuition. Although the observed cracking of the wafer was reduced, complete delamination still occurred during the thinning process. Examination of the silicon wafer post-delamination revealed discoloration in the region where the GaAs had been pseudo-bonded to the Silicon. Following the bonding process, as expected, the silicon surface remained entirely covered by a gold film since Au was deposited on the wafer surface during EBPVD. Multiple gold wet etching steps were performed in an effort to remove the gold layer, but a region persisted where the gold could not be removed, indicating diffusion into the silicon substrate. This

observation concluded that diffusion was the primary mechanism driving the metal-to-metal bonding. A photograph taken after the Ti and Au etching is shown in Figure 61.

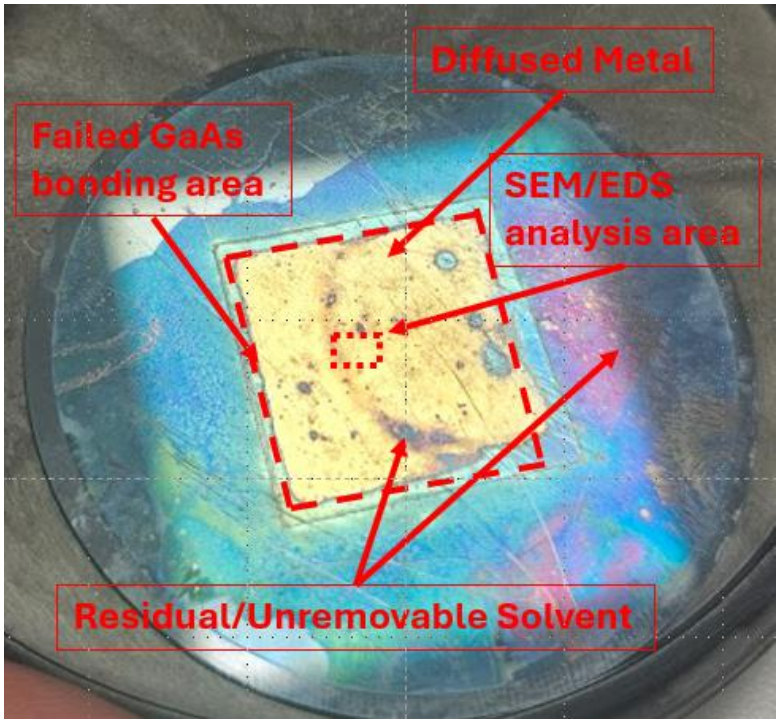


Figure 61 – Photograph of the failed GaAs bonding.

In order to confirm the hypothesis that the residual materials are metals, an SEM measurement is taken. This measurement is shown in the image in Figure 62. This measurement shows pits that weren't present before bonding and regions of thick Au on a field of Ti. Energy dispersive spectroscopy (EDS) is performed and clearly shows fields of metal present. This measurement is shown in Figure 63.

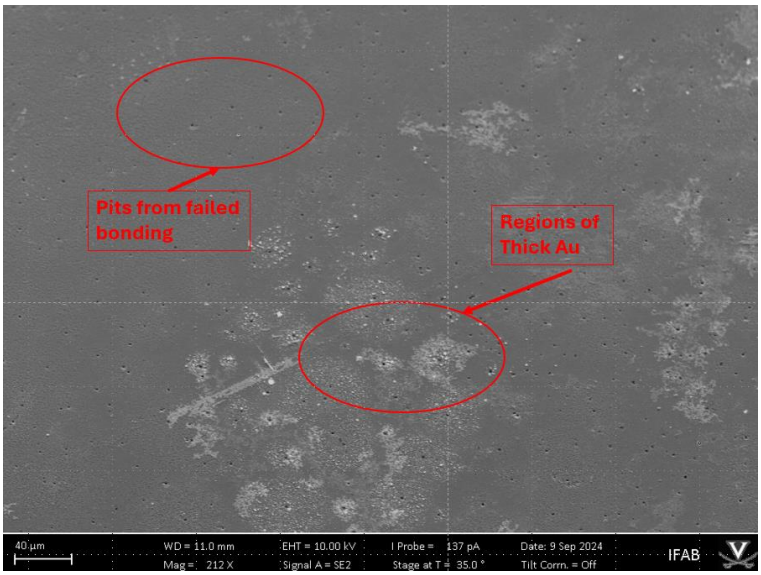


Figure 62 – SEM measurement of the failed GaAs bonding (Si wafer)

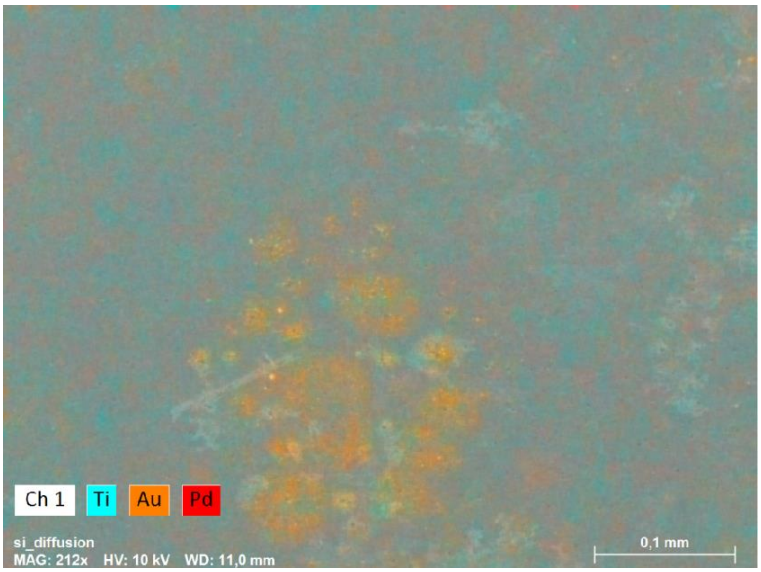


Figure 63 – EDS measurement of the failed GaAs bonding (Si wafer)

The SEM and EDS measurements data allowed us to determine that an additional diffusion barrier needed to be added. The final stack for the diffusion-bonded samples is shown in Figure 18. In addition to adding a diffusion barrier, the wafer pressure is relaxed to half that used for the silicon bonding. The final bonding procedure is shown in Table 6.

Step	**Top Temp (°C)**	**Bottom Temp (°C)**	**Chamber Press (mBar)**	**Tool Force (N)**	**Process time (hh:mm)**
1	25	25	Purge	0	1:00
2	100	100	6.75E-5	0	1:00
3	300	300	6.75E-5	0	1:00
4	300	300	6.75E-5	0	4:00
5	300	300	6.75E-5	1500	4:00
6	300	300	6.75E-5	1500	2:00
7	100	100	6.75E-5	0	0:30
8	25	25	Purge	0	0:30

Table 6 - Final bonding procedure for Diffusion-bonded samples

The diffusion-bonded sample is thinned using the thinning procedure discussed in section 2.2.2. The critical differences between thinning an SU8-bonded sample and a diffusion-bonded sample are the presence of cracks in the wafer and the reduced time required to etch through the GaAs handle in the diffusion-bonded sample—about half the time compared to the SU8-bonded sample. The leading theory to explain wafer cracks shown in Figure 64 is that cracks initiated during the dicing of the GaAs wafer into squares propagate further when pressure is applied during the thinning process. The leading theory to explain the faster thinning process is that galvanic effects increase the etch rates and that the SU8 acts as a passivation layer.

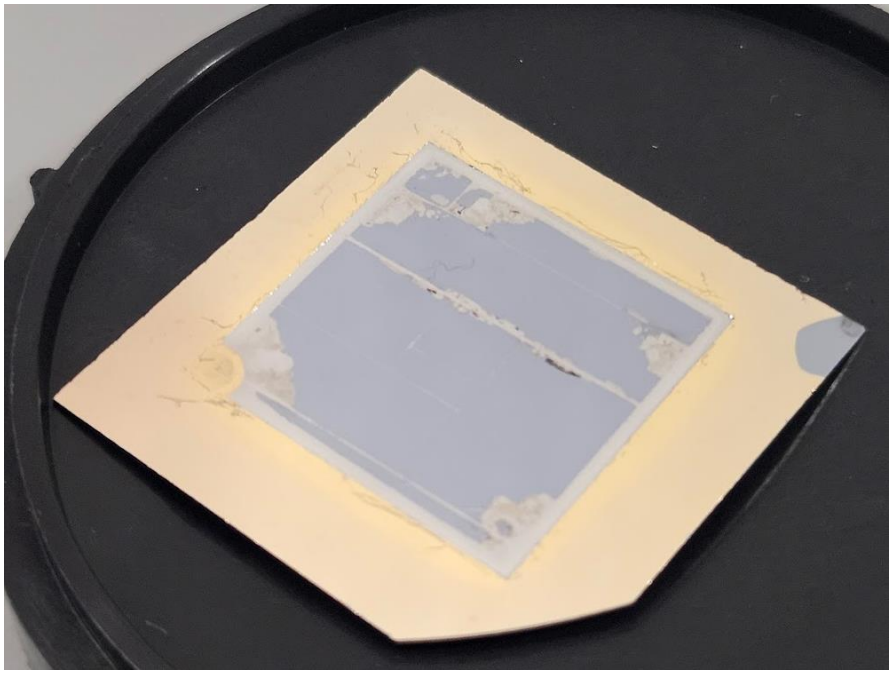


Figure 64 - Thinned wafer after diffusion bonding procedure

2.3.3 Fabrication procedure for metal-to-metal bonding

The fabrication of the quasi-vertical diode follows a similar procedure as outlined in the previous section. This initial experiment uses a thick, high-resistivity silicon wafer (>10k-ohm) instead of SOI. The experiment aimed to assess whether the quasi-vertical Schottky diode could be fabricated through diffusion bonding; thus, fabricating a set of on-wafer diodes was deemed

sufficient. Since we're not using SOI, the via steps can be eliminated, and the ExVia/Plateburn step can be eliminated since no photoresist in vias must be exposed/developed away.

The mesa etch follows the same process described in Section 2.2.3. However, as with the thinning procedure, the etch rate increased significantly, leading to over-etching in specific regions and reducing the yield of mesas. Notably, multiple diode circuits were completely over-etched, leaving only single diodes that successfully completed the process.

The Ohmic etch needed to be modified to accommodate the new stack. It was found that the TFA gold etch type A was insufficient to remove the Pd and Au. The modified ohmic etch starts with the CF4/Ar etch mentioned in section 2.2.4. However, when it is time to use the TFA gold etch type A, a second beaker of a HCL based Ti etch is used, and 20 seconds of wafting in the TFA etch and 20 seconds of wafting in the HCL etch is used until the wafer is visually finished etching, indicated by a smooth layer indicative of Ti. After reaching this smooth film during the wet etch, the CF4/Ar etch removes the remaining Ti. As mentioned, the sacrificial resist, sputtering, and electroplating steps are the same, except without the ExVia/Plateburn step. This abbreviated fabrication process is captured in Figure 65.

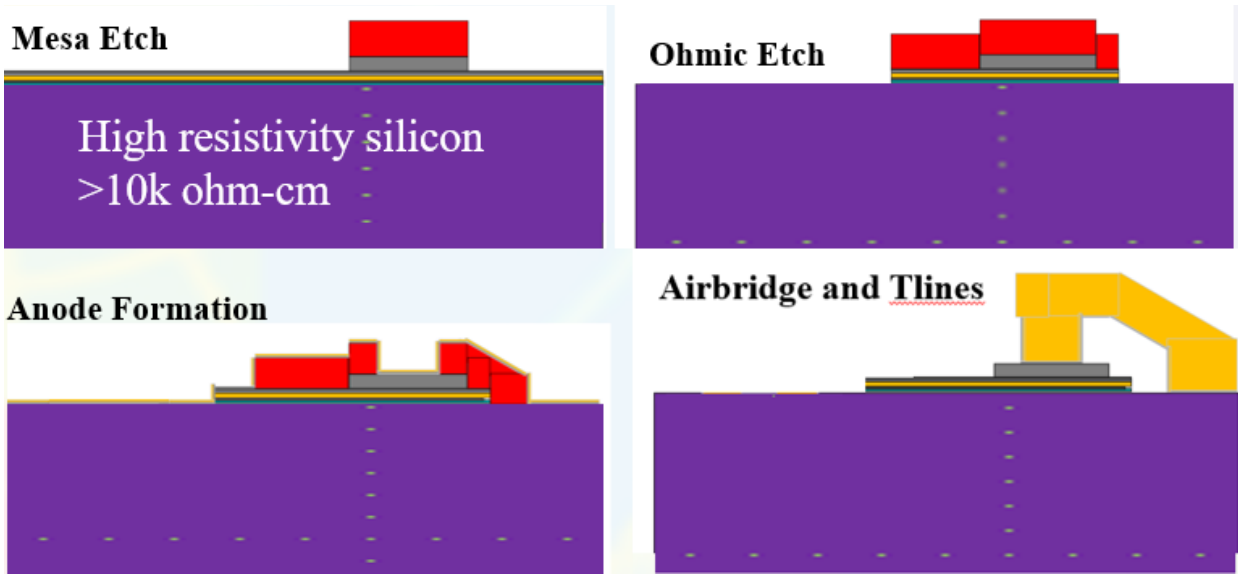
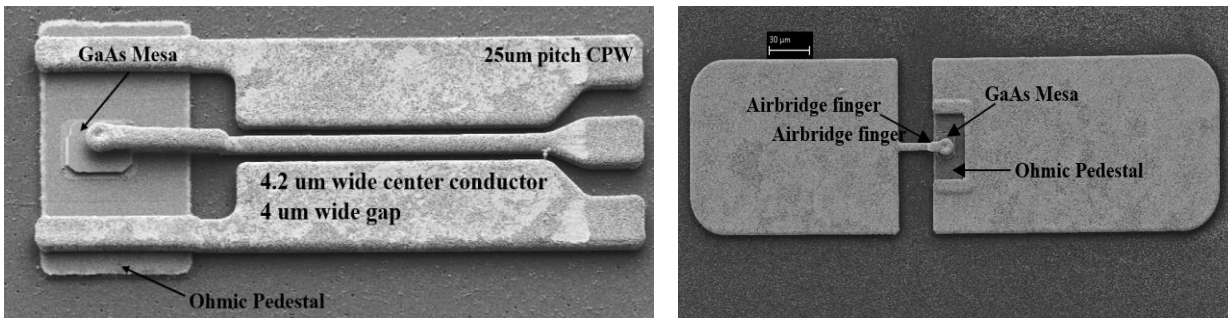


Figure 65 - Abbreviated fabrication process for Diffusion bonded QVDs

SEM was used to capture imagery of the single diodes fabricated in this process. These diodes are shown in Figure 66.



(a) (b)

Figure 66 – (a) CPW diode and (b) DC test diode fabricated in the diffusion bonded process.

2.2.4 Conclusion:

This work presents the first comprehensive ohmic characterization of our diode stack across an entire wafer, providing critical insights into its impact on yield. A dedicated mask and process were developed to collect statistical data and analyze yield as a function of wafer position. The fabrication process outlined in Section 2 demonstrates a method for miniaturizing diodes and circuits heterogeneously integrated on silicon-on-insulator (SOI). This process simplifies ohmic etching by introducing optimized etch rates for CF_4/Ar etching and replacing the resist-degrading HG solution with a diluted TFA gold etch type A, which effectively etches both Pd and Au layers. Additionally, it introduces a novel method for fabricating side-coated vias using a stepped lithography approach, as developed by Linli Xie, involving long exposure lithography, sputtering, and ultrasonic-assisted electroplating to define Au features. Notably, this work marks the first report of a diffusion-bonded metal-to-metal GaAs Schottky quasi-vertical diode (QVD) heterogeneously integrated into Silicon, a significant advancement in high-frequency Schottky diode technology, enabling higher power handling. Furthermore, it describes methods for diffusion bonding silicon to InGaAs/GaAs epitaxial stacks and fabricating quasi-vertical diodes using diffusion-bonded GaAs.

Chapter 3 - Characterization of Diffusion Bonded GaAs Schottky at Sub-Millimeter-Wave Frequencies

The following publications are associated with the efforts and accomplishments contained in this chapter:

3. Moore, C., Zhou R., Widmann, D., Lukaczyk, L. Cyberey M., Bawens, M., Weikle, R., Barker, S., & Lichtenberger, "Characterization and Fabrication of Diffusion Bonded GaAs Schottky Diodes." European Microwaves Conference (EuMEC), 2024.

3.1 Introduction:

Schottky diodes persist as an essential technology for realizing radio instruments from 100 GHz to more than 4 THz. The prior art has demonstrated heterogeneous integration of GaAs onto silicon, allowing quasi-vertical Schottky diodes (QVDs) fabrication using adhesive bonding with spin-on glass and SU8 photoresist [37-41]. QVDs have shown comparable and even superior performance to whisker and planar-type Schottky diodes, as described in [40]. The quasi-vertical Schottky diode, theoretically, can achieve lower series resistance compared to planar devices and has a simple parasitic circuit model due to its vertical structure and the associated reduction in spreading resistance compared to planar diodes. The QVD is fabricated with buried ohmic contacts, providing an integrated heatsink for the diode that provides a thermal path directly to the underlying silicon and metallization on top of the high-resistivity silicon platform. Adhesive-bonded QVDs have a direct thermal conductance path through metal circuitry contacting the device; however, the adhesive layer represents a considerable thermal resistance, constraining the thermal dissipation to the substrate underlying the metal features [53]. In addition to this limitation, the fabrication of these devices has been, until now, a complex process with lengthy processing time. The recent advances in fabrication, as shown in the previous chapter, have resulted in fewer steps, enabling rapid processing of devices [55]. The thermal dissipation density limitations of adhesive bonding for high-frequency diode operation have been addressed by utilizing non-adhesive plasma-assisted bonding at room temperature; however, this process suffers from delamination at elevated temperatures, which could occur in subsequent high-temperature processing or high-power operational conditions [56].

The metal-to-metal bonding process described in the previous chapter utilizes recent advancements in the fabrication process and a significant change from adhesive bonding to diffusion bonding, creating a metal-to-metal interface. This change directly addresses prior limitations in the thermal performance of the quasi-vertical diode. Heat dissipation in these devices is critical to reducing the size, weight, and power of compact systems and circuits for space and consumer-grade electronics. High-frequency design requires measurement-based modeling of these devices to account for the parasitics associated with the diode's geometry and to verify the diode equivalent circuit model. Prior art demonstrated a method of extracting these parameters, which characterized the electromagnetic fields near the diode and its associated parasitics [37-41]. This work resulted in an equivalent circuit representation and showed results consistent with ANSYS high-frequency structure simulation (HFSS). The same geometry used for previous work, which contained open and short-circuited diode structures, was included in this work; however, problems with fabrication caused significant degradation of these structures, not allowing us to measure them. The work reported here presents the performance of the quasi-vertical Schottky diode based on diffusion-bonded devices. We measured scattering parameters from 325-500 GHz and used them to develop a circuit model for fabricated devices. The diodes utilize material with a thinner epitaxial region than previously reported [37-41][53]. The general diode geometry is identical to the previously reported devices; however, several processing steps have been modified to simplify fabrication, expediting the development cycle of new diode circuits.

3.2 Experimental setup

The experiment was set up by designing a photolithography mask set comprised of six regions with TRL calibration kits. Each of the six areas is CPW-based heterogeneously integrated GaAs Schottky diodes. Scattered around these regions are single diodes intended for D.C. bias measurements. The photolithography mask sets are shown in Figures 67 and 68.

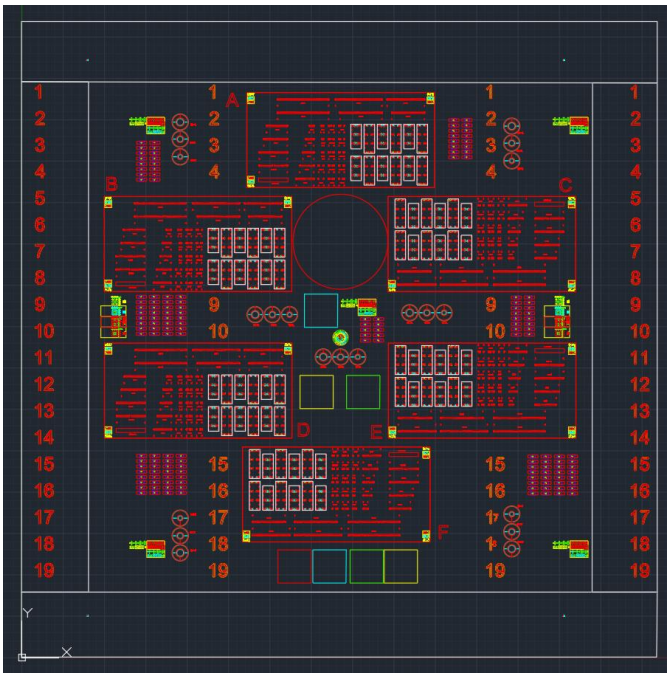


Figure 67 - Mask set for experiment

Below is an example of the experimental region set up for this work, with annotations.

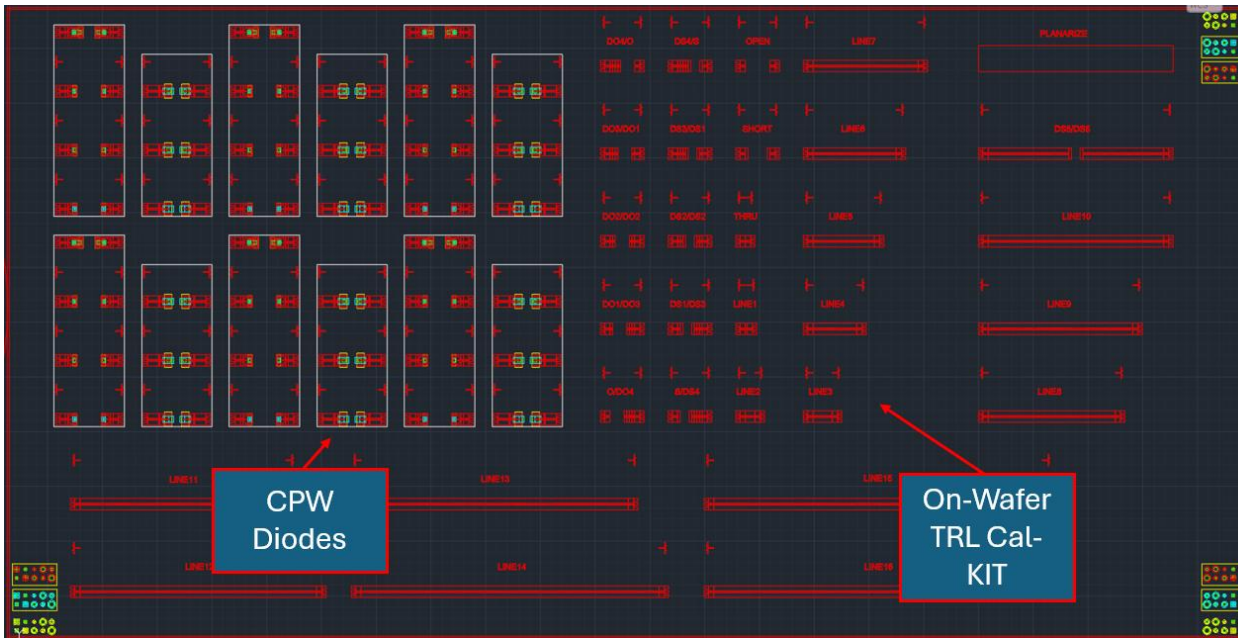


Figure 68 – Experiment region with CPW diodes and CPW TRL Cal kit

3.4 Calibration

The RF characteristics of the diodes were measured using a pair of 25 μm-pitch, WR-2.2 probes. A PNA-X vector network analyzer was configured to perform a sweep for the 325-500 GHz (WR-2.2 frequency band). Calibration standards were fabricated on the same substrate as the diodes, including an open, short, and four additional sets of delayed opens and shorts. An SEM image of the calibration standards is shown in Figure 69.

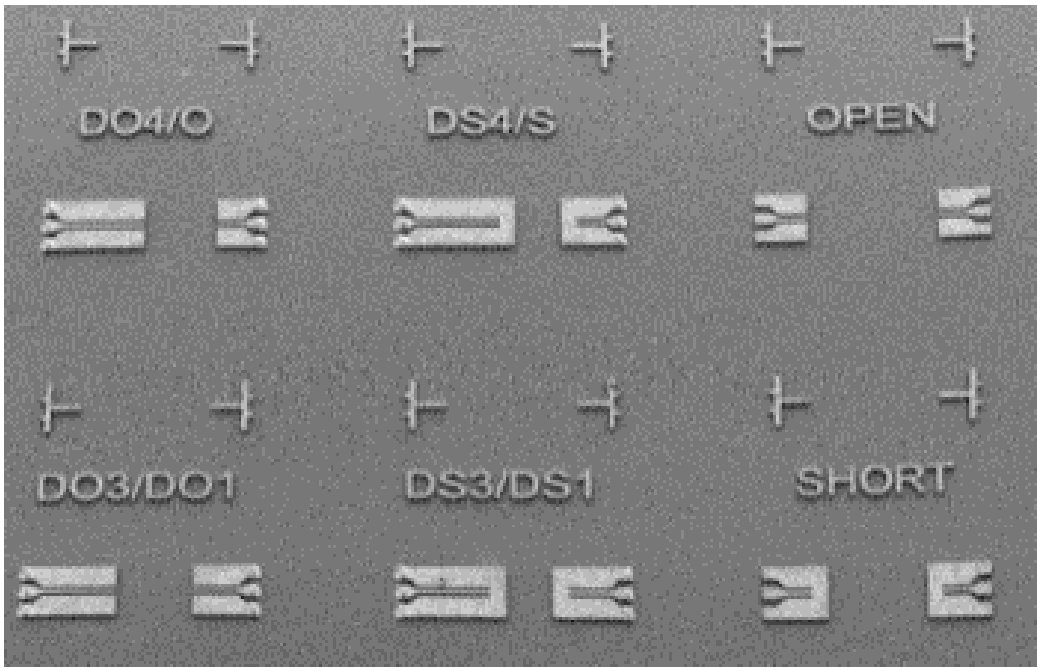


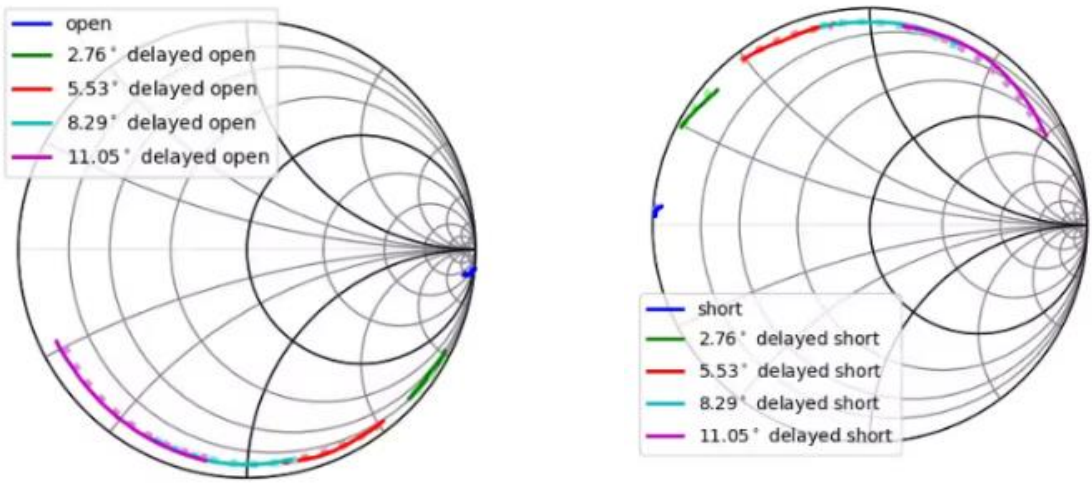
Figure 69 -Scanning Electron Microscope image showing a portion of the on-wafer calibration standards.

Figure 70 shows the measurements of the on-wafer standards after TRL calibration was performed and applied. The solid and dotted lines match calibrated measurements and the expected S_{11} of each standard, respectively.

The open-circuit, short-circuit, and thru (CPW) lines were simulated using HFSS. The thru line was simulated to determine the attenuation and propagation constants so that arbitrary lines could be synthesized using the scikit-rf python package. This was used to create delayed lines and de-embedding post-processing in measurement analysis. The calibration standards include delayed open and short circuit lines with delays of 0, 15, 30, 45, and 60 μm and a measurement reference plane at a distance of 30 μm (5.53° at 412.5 GHz) from the probe pad-CPW transition. These structures are shown in Figure 69. The calibration was applied using scikit-rf's OnePort function,

which applies the least squares solution to the usual three-term error model. Diode measurements were referenced to the calibration kit short reference plane.

Measurement of the calibration standards showed a significant, systematic phase difference, consistent with the phase constant being about 0.885× that of the simulation value. After compensating for this, the phase was within +/-2 degrees of the calibration ideal standards and magnitude within +/- 0.25 dB. Though not shown, simulations showed that this systematic phase difference was likely due to thicker plated features on the wafer versus what was used in simulations.



(a) (b)

Figure 70 - Calibrated S11 measurement of the on-wafer calibration standards: (a) open standards; (b) short standards.

3.4 Measurement and Analysis

The measurement setup for RF characterization of the diodes is shown in Figure 71. A PNA-X N5244B, WR-2.2 VDI VNA extender, and DMPI WR-2.2 probes were used to measure S_{11} data. The diode was biased through a Keithley 2470 SMU. The measured S_{11} of the diode swept across bias voltage at mid-band (412.5 GHz) is shown in Figure 71. The reverse bias voltage and forward bias current were stepped manually over 38 points, and a 325-500 GHz S-parameter sweep was taken for each bias point. The measurement is de-embedded to the start of the finger (84 µm past the probe-landing pads). S_{11} of the diode measurement indicates that as the diode bias from a high reverse voltage, such as -4V, towards zero bias, the reactance will increase, indicating an increase in capacitance. This means that reducing the voltage will lead to a higher capacitance while reverse-biased. As the diode becomes forward-biased, S_{11} begins to confine its movement along a circle of constant reactance toward decreasing resistance. This indicates the varistor component of a forward-biased Schottky diode because varying the forward bias will cause a change in resistance while keeping capacitance mostly constant.

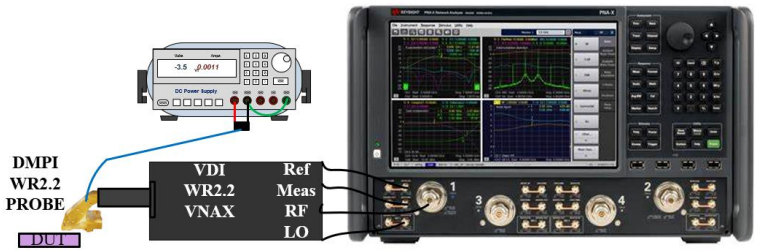


Figure 71 - Measurement setup for RF characterization of diodes.`

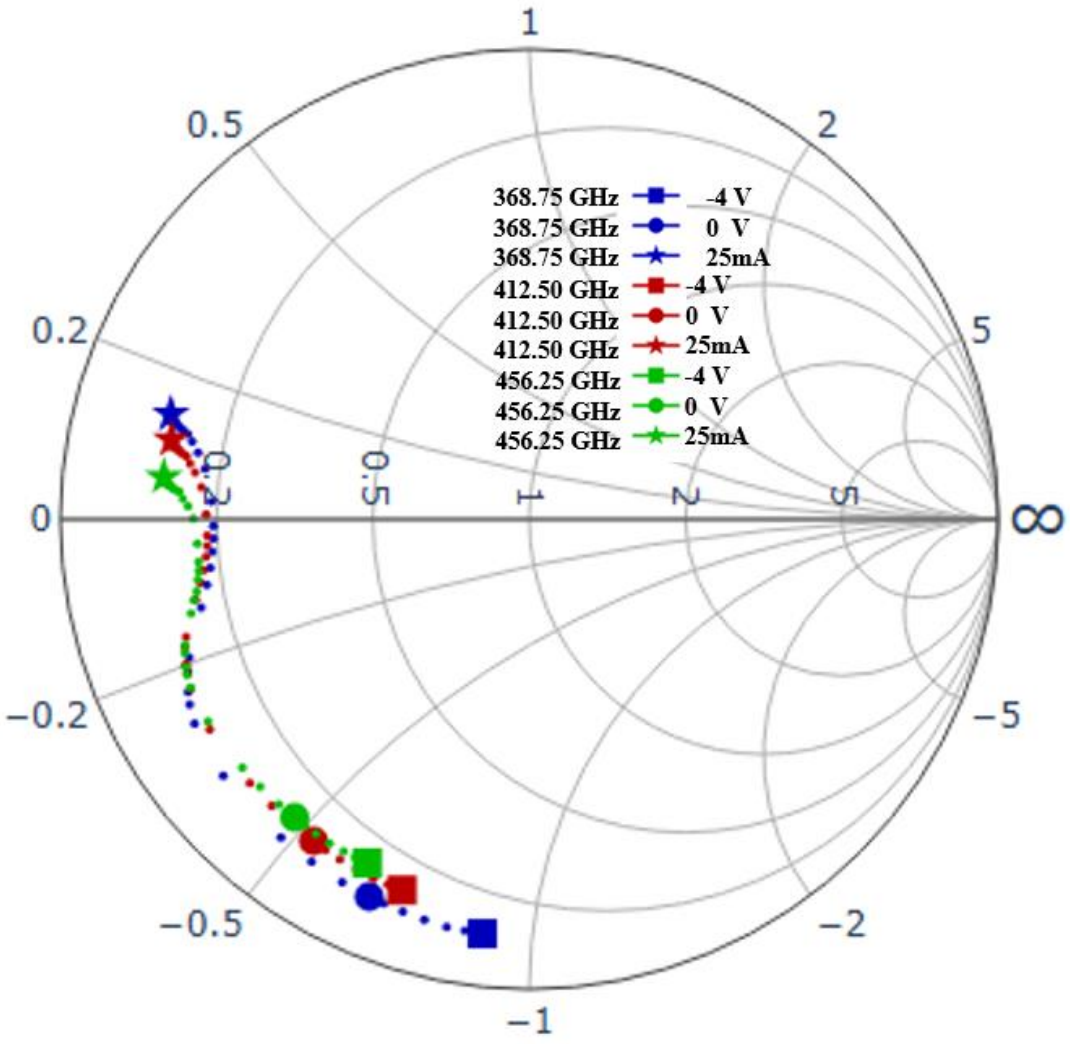
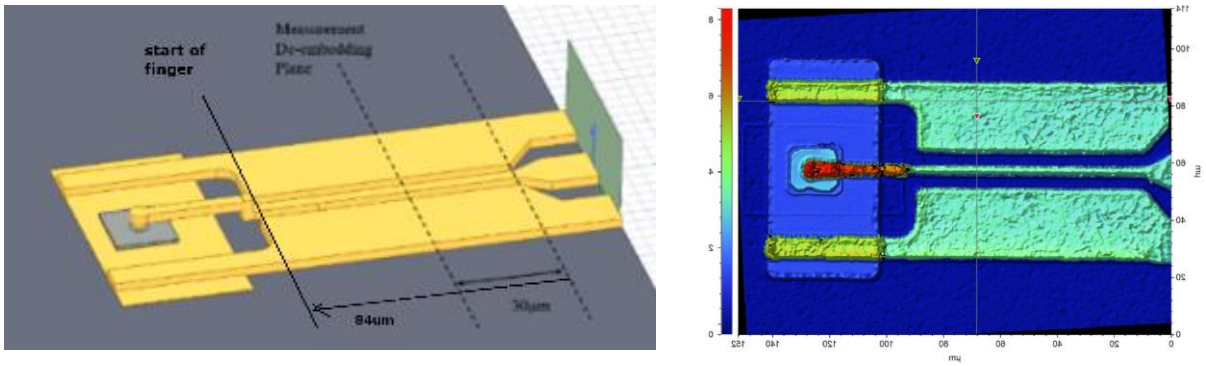


Figure 72- Measured S-parameters of the diode as function of bias at midband.

Diode parameters are extracted using the measured S-parameters and fit to the circuit model terminated to a touchstone file generated from an HFSS simulation representing the CPW diode structure. The HFSS model is based on a Bruker Contour GT-K optical profiler measurement of the various step heights across the geometry. The electroplated gold's root mean square surface roughness parameter was measured to be 70 nm and used as a finite conductivity boundary condition with 4.1×10^7 S/m conductivity in HFSS.



(a)

(b)

Figure 73-(a) HFSS model of the diode mounting structure. (b) Optical profiler measurement of diode CPW structure.

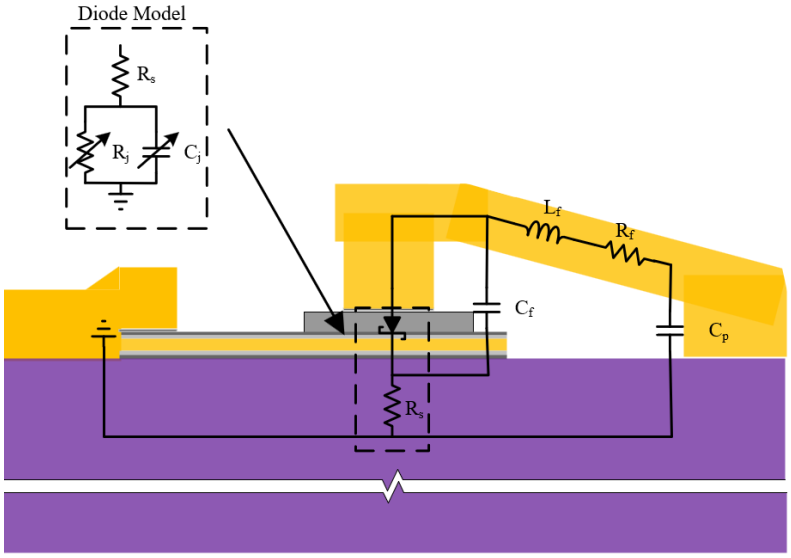
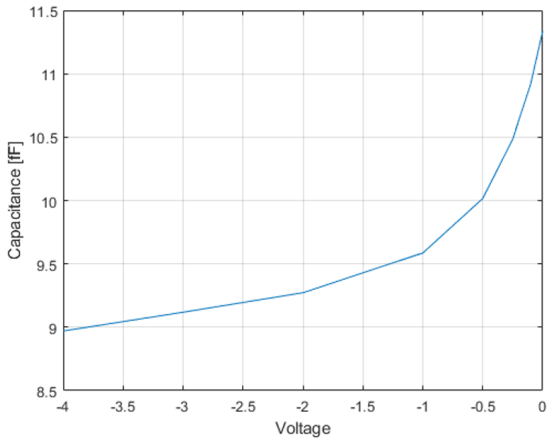
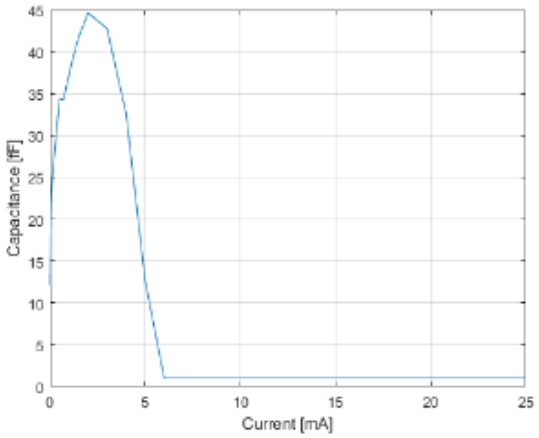


Figure 74- Simplified circuit model of the Schottky Diode

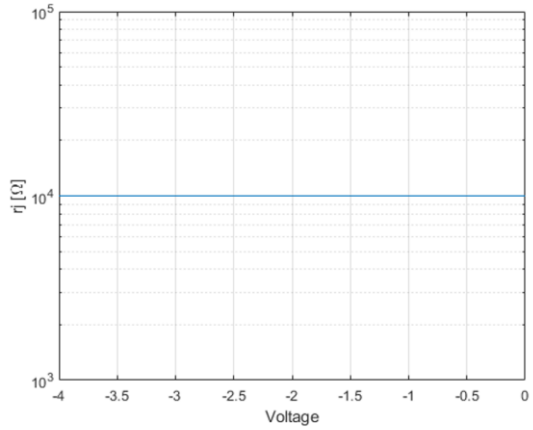
The circuit used to model the diode is shown in Figure 74 and consists of a series resistance (R_s) in series with a variable junction resistance (R_j) and variable junction capacitance (C_j). The parasitic capacitances and inductances of the diode mount are included in the measured data and must be included in the circuit model as well. These parasitics are captured with the HFSS simulation shown in Figure 73(a). The wave ports of the simulation are de-embedded so that the resulting s-parameters capture the effect of the mount from the measurement plane (30 mm past the probe landing pads) to the anode contact of the diode (where the anode touches the GaAs), like what was done in [38]. The fitted diode parameters at midband (412.5 GHz) are shown in Figure 75 and 76.


Capacitance [fF]
Voltage
11.5
11
10.5
10
9.5
9
8.5
-4
-3.5
-3
-2.5
-2
-1.5
-1
-0.5
0

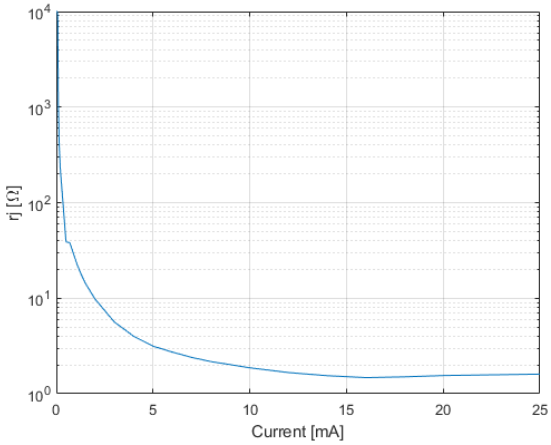
(a)


Capacitance [fF]
Current [mA]
45
40
35
30
25
20
15
10
5
0
0
5
10
15
20
25

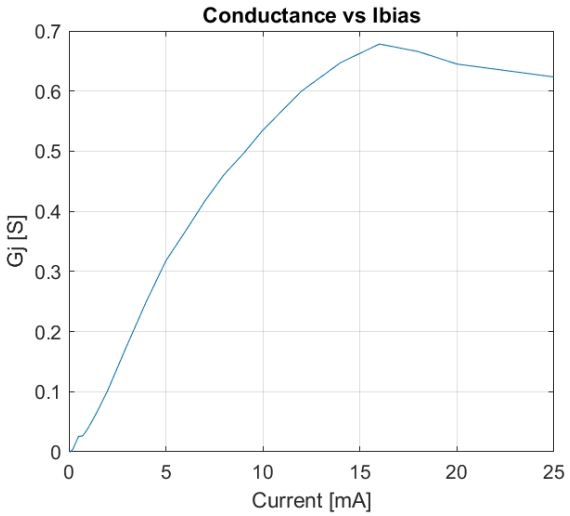
(b)


rj [Ω]
Voltage
10^5
10^4
10^3
-4
-3.5
-3
-2.5
-2
-1.5
-1
-0.5
0

(c)


rj [Ω]
Current [mA]
10^4
10^3
10^2
10^1
10^0
0
5
10
15
20
25

(d)



(e)

Figure 75. (a) Junction capacitance vs reverse bias voltage; (b) Junction capacitance vs forward bias current; (c) Junction resistance vs reverse bias voltage; (d) Junction resistance vs forward bias current (e) Conductance (1/Rj)

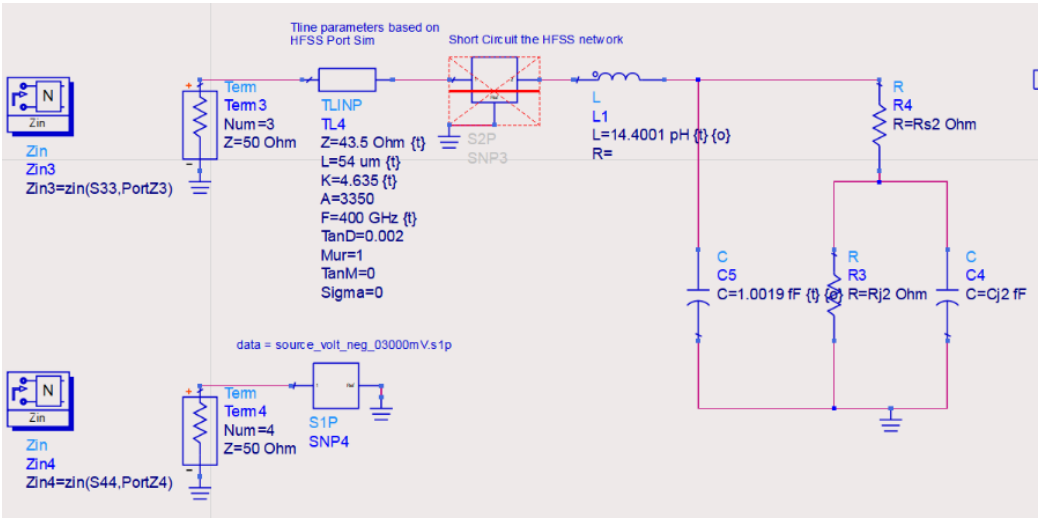


Figure 76 – Circuit to match diode measurements with model

The average rms impedance as a function of bias is shown in Figure 77. At reverse bias, a voltage was sourced, and under forward bias, the current was sourced, which is reflected in the units used in the figure. The methodology for extracting the circuit model involved first fitting separate R_s, R_j, and C_j parameters for each bias condition from reverse bias conditions up to 25 mA of forward bias. Then, the average R_s was calculated to be 3.27 and used for all further forward bias conditions. This permits a good fit of R_s since it dominates over the effect of R_j in this portion of the bias. ADS was used to optimize the extracted circuit model by minimizing the real and imaginary error components between the modeled and measured impedance. The RMS error between fitted and measured impedances, Z_{rms}, was calculated for each bias condition, and the average value over the WR-2.2 band was taken and is presented in plot.

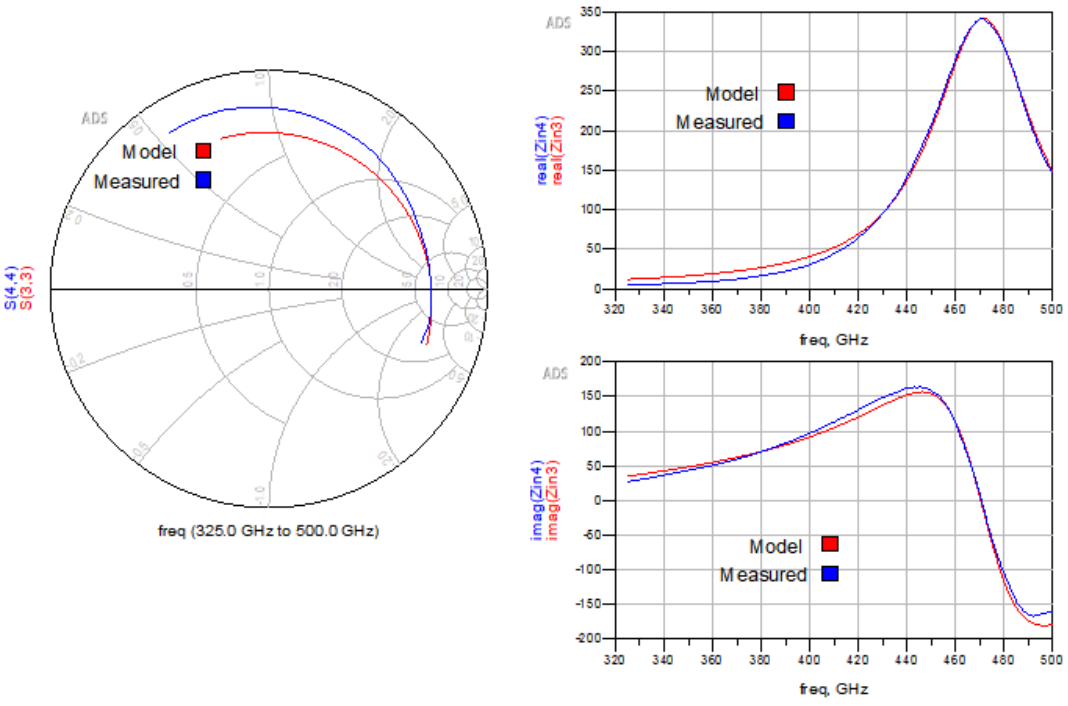


Figure 77 – Fitting Results in ADS (Not dembeded)

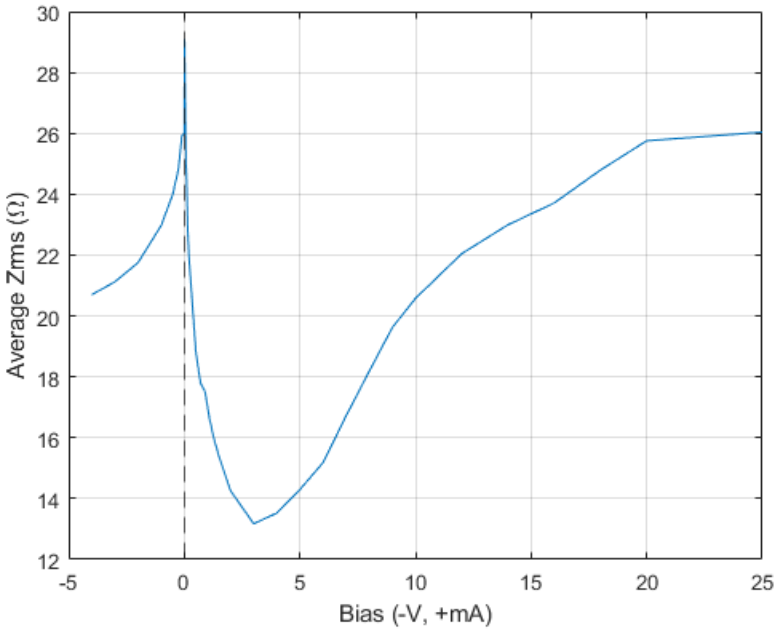


Figure 78 – Average Zrms as function of bias

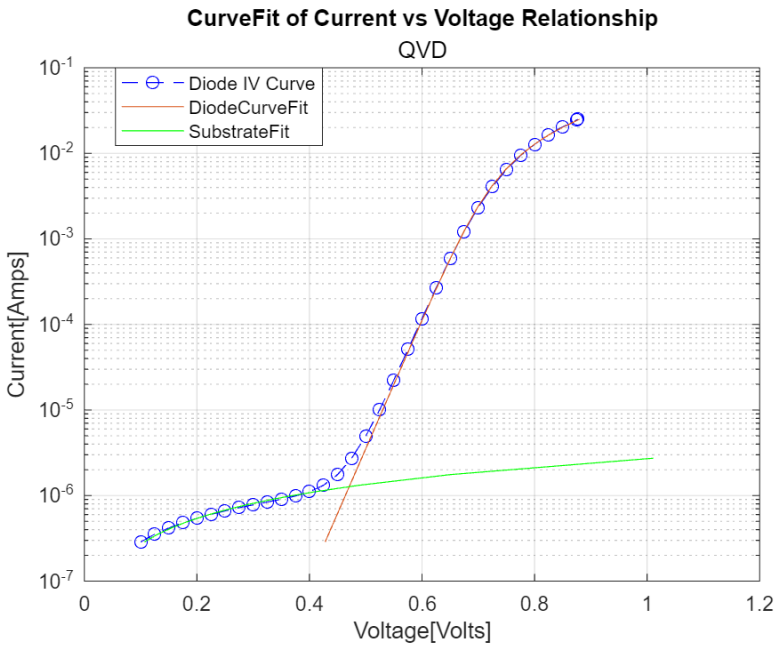


Figure 79- D.C. current-voltage characteristics for the diode shown in Figure 1b.

Figure 79 shows D.C. current-voltage characteristics for the diode shown in Figure 1b. The fitted model corresponds to a saturation current of 10^{-13} [A], an Ideality factor of 1.151, and a series resistance of 5 Ω. Substrate resistance was found to be 370k Ω. Reverse-bias sweep indicates that the breakdown voltage is approximately -7.5 VoAlts.

The current density was estimated by sourcing forward-biased current for 60-second intervals, plotting the DC-IV curve (fitted example in Figure 79), and inspecting the diode for damage. 100 mA forward current was found not to damage the 5.5 µm device, corresponding to 436 kA/cm^2 current density, though as shown for the DC conductance plot in Figure 75e, heating of the diode dramatically increases the series resistance; therefore, it's not practical to use the device with this

much forward current, hence, this number represents it's resilience to high heat, and ability to sink heat.

The primary motivation for this work was to increase the QVD's thermal handling ability. Initial experimental work, shown in the fabrication chapter, showed that the thermal conductivity of the metal bond of SU8-bonded SOI was lower than that of diffusion-bonded SOI. Initial simulations also indicated that changing the diode bonding interface could result in better thermal handling. After the RF characterization, a collaboration was undertaken with Zerbajari's group to measure the thermoreflectance of a diode of the same diameter made with adhesive bonding. The geometry wasn't the same; the SU8 QVD had much larger contact pads than the diffusion-bonded QVD, which would make the diode cool faster due to convection from the increased surface area.

The thermoreflectance measurement technique relies on the variation in refractive index (and, consequently, surface reflectivity) with temperature changes. The fractional change in reflectance ($\Delta R/R$) in response to a temperature change (ΔT) can be approximated, to first order, as:

$$\frac{\Delta R}{R} = \chi \Delta T.$$

The parameters used deviate slightly from Nadri's approach [38]. We found that we needed to use a higher voltage than in [38] to show heating during the test. The test setup is shown in the figure below:

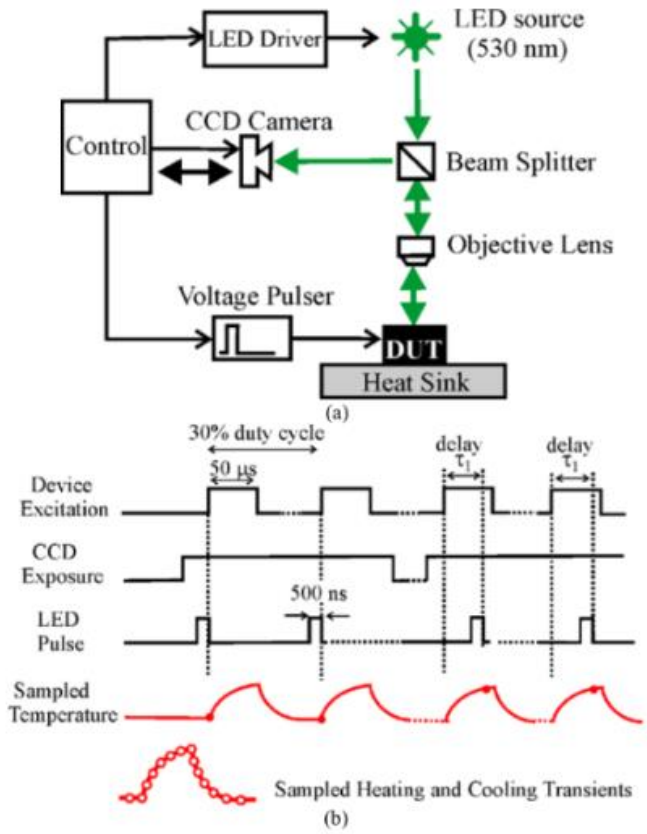


Figure 80- Test Setup for Thermo Reflectance

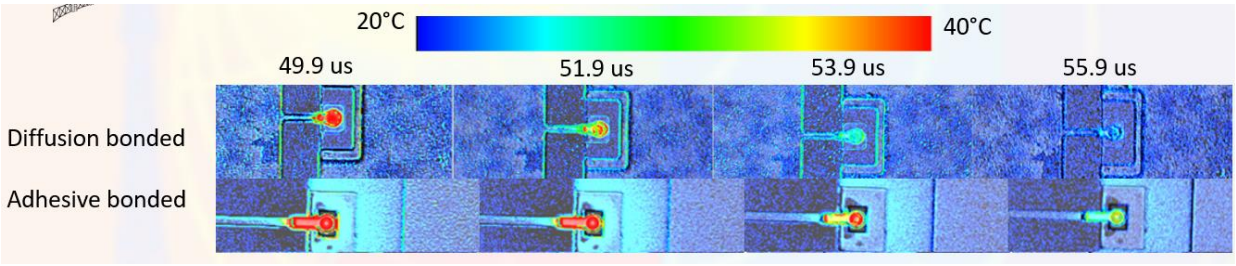


Figure 81 – Results from Thermo Reflectance measurement

Using the scale bar, figure 81 shows the measurement results; we can observe that the diffusion bonding device cools much faster than the SU8 diode, indicating higher thermal conductivity. To verify this result, an Ansys Icepk Simulation was set up.

In order to estimate the rate at which a device cools down (or heats up), it's essential to account for the exponential decay and understand the thermal time constants associated with different parts of the device. Newton's law of cooling is expressed as:

$$\frac{dT}{dt} = -k(T - T_{ambient})$$

This expression describes how the temperature of an object changes over time as it moves toward the ambient temperature of its surroundings. This law states that the rate of heat loss (or gain) is proportional to the temperature difference between the object and its environment. Additionally, heat capacity plays a significant role. For instance, a QVD made using SU8 bonding has a higher heat capacity than ohmic metals in QVD made with diffusion bonding, which can be advantageous in applications that require minimal temperature rise during operation. For completeness, Newton's law can be modified to include heat capacity, yielding the form:

$$\frac{dT}{dt} = -\frac{k}{C}(T - T_{ambient}).$$

Rearranging the variables, integrating, solving for T, and determining the value of constants with initial conditions, one may solve for temperature as a function of time.

$$T(t) = T_{ambient} + (T_0\text{-}T_{ambient})e^{\frac{-kt}{C}}$$

This equation is valid as long as the final ambient temperature of the materials is the same; otherwise, $T_0\text{-}T_{ambient}$ can be represented by a generalized coefficient, T_n.Though in literature,

researchers analyzing the cooling transients are looking at structures that have multiple materials with varying thermal conductivities and heat capacities; therefore, we express $\frac{k}{C}$ as τ, representing a 'time constant' of one of the various materials and used as a parameter for non-linear curve fitting. These different materials represent multiple time constants during a measurement, which are all captured in the equation from reference [58].

$$T(t) = T_{ambient} + (T_1)e^{\frac{-t}{\tau_1}} + (T_2)e^{\frac{-t}{\tau_2}} + \ldots + (T_n)e^{\frac{-t}{\tau_n}}$$

The thermal resistance of the entire structure can be calculated by heating it similarly to how the cooling transient is measured, taking the difference between the maximum and minimum temperatures and dividing it by the power used to heat the structure.

$$R_{\emptyset} = \frac{T_0 - T_{ambient}}{P}$$

ANSYS Icepak is used to model and simulate the cooling transients of the QVD, capturing how the device cools down from peak operating temperatures over time. It applies transient thermal analysis to track temperature changes as the QVD approaches ambient conditions. Icepak is also used to measure the thermal resistance by modeling the temperature gradient between the heat source and the device's structure, assessing heat transfer efficiency. The Icepak simulation is set with nearly identical QVD structures, the only difference being the bonding interface. One of the bonding interfaces is made with SU8, and the other is Au. Beneath the SU8 and Au is a thin layer of Titanium; in practice, the ohmic metal stack is more complex, as shown in Chapter 2; however, for a relative comparison, this is sufficient. The airbox faces are set to an opening (thermal

boundary condition) that allows ambient pressure conditions and ambient airflow. Airflow, for convection, is simulated by enabling gravity with 9.80665 m/s^2 ,-Z vector acceleration with the flow setting set to .001 $\frac{m^3}{s}$. The diode is on a 15-um thick silicon chip, placed on a copper block set to static ambient temperature (293.15K) to replicate measuring a real-world device on a large chuck. Au pads are placed on the contact pads to the overall diode structure and set to ambient temperature. The diode diameter for both simulations is 4um.

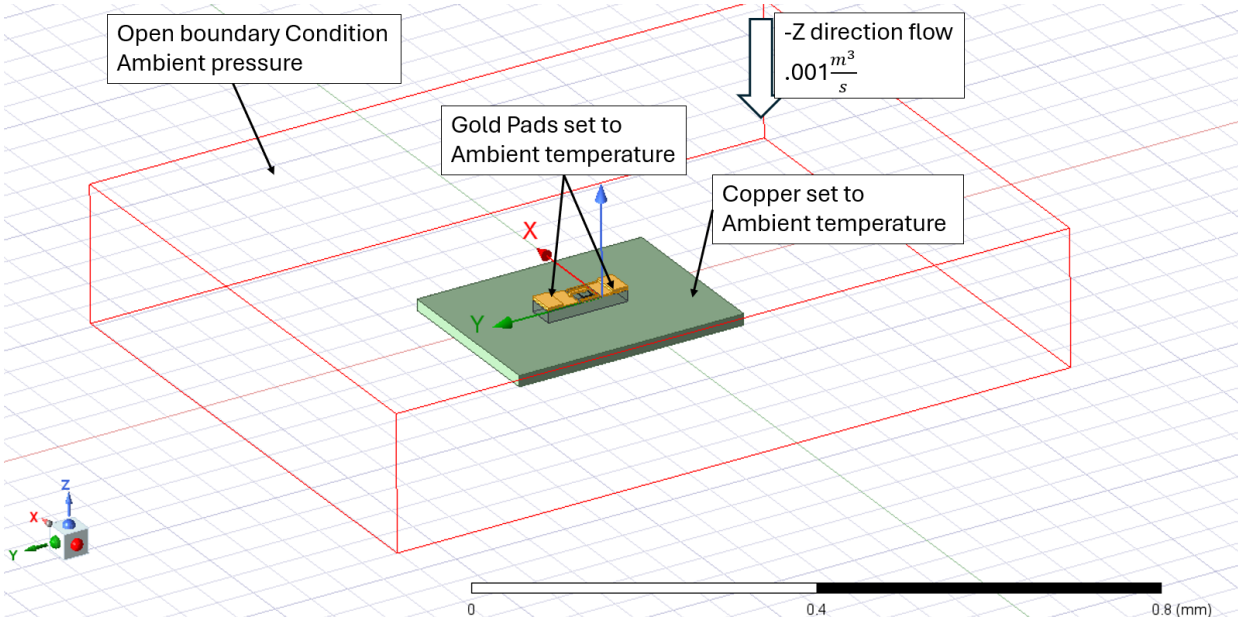


Figure 82 – ICEPAK Simulation setup for comparing Diffusion vs Adhesive bonded QVD

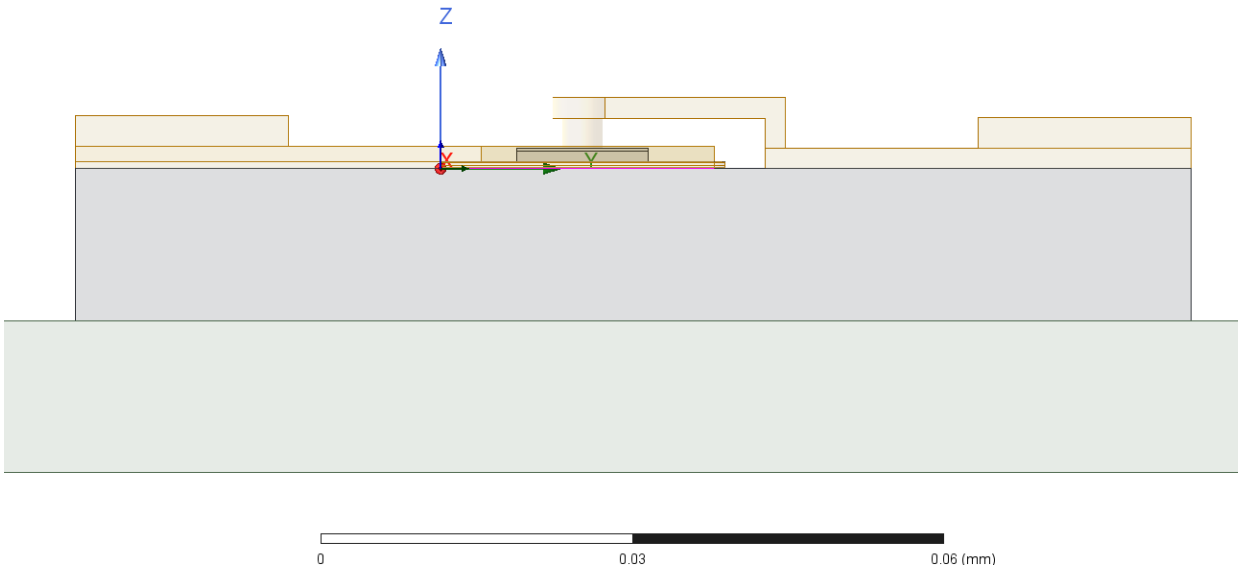


Figure 83- Side Profile of Diode sitting on 15um Silicon

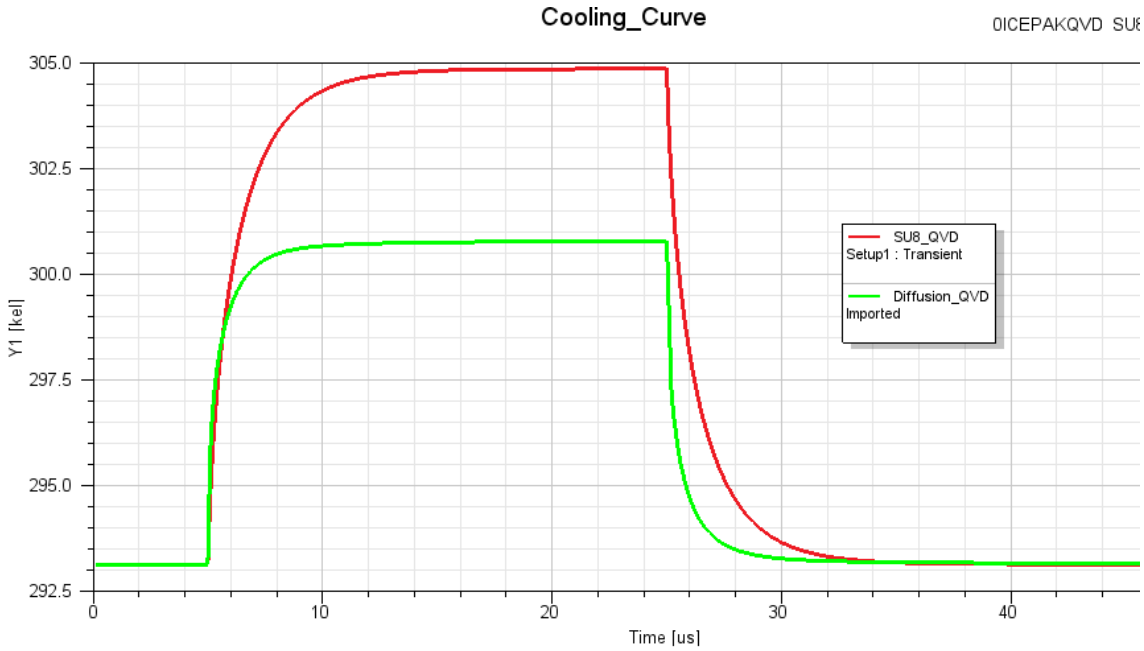


Figure 84 – Cooling Curves for the chip shown in Figure 17 of the SU8 and Diffusion bonding variant.

The cooling curves show that the thermal resistance is lower, e.g., it doesn't get as hot, and the diffusion-bonded sample cools faster. This data was exported to Matlab, the thermal resistance was calculated, and the cooling time constant was extracted through non-linear curve fitting. The fit for the Diffusion QVD proved challenging because it cooled too fast, requiring a very fine time sweep. This challenge can be seen in the discontinuity in the data presented below; the time corresponding time constant will be different with a better fit.

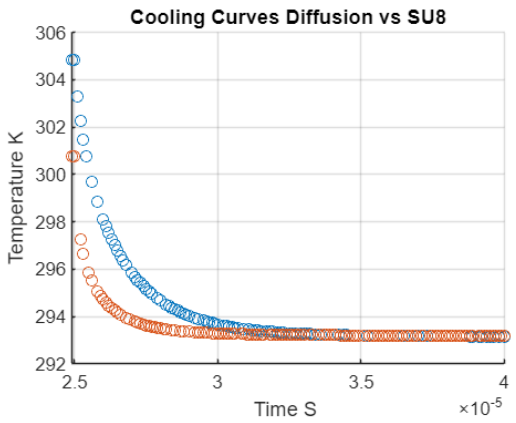


Figure 85 - Cooling curves replotted in Matlab.

	SU8 QVD	Diffusion QVD
Thermal Resistance ($R_{\emptyset}$)	2335	1523
Time constant ($\tau 1$)	14.6 uS (.998R^2)	7.02 uS (.983 R^2)
Time constant ($\tau 2$)	.97 uS (.998R^2)	1.2uS (.983 R^2)

Table 7 – Comparison between time constants and thermal resistances between Lateral diode and QVD.

3.5 Conclusion

This is the first report on a diffusion-bonded metal-to-metal GaAs QVD that is heterogeneously integrated into silicon. This device represents an advance in the development of high-frequency Schottky diode technology by enabling significantly higher single-device power handling, as demonstrated by the measured large current capacity far exceeding typical operating setpoints that are needed. We first characterize the reverse and forward bias conditions of a varistor-type QVD at high frequency. We have also described the characterization methodology at forward bias, uniquely showing forward bias conditions for the QVD. Future work will focus on optimizing the fabrication process. A thermoreflectance measurement indicated that the diodes made with diffusion bonding cool significantly faster than those made with SU8. Ansys ICEPAK simulations estimated the relative time constants associated with cooling and thermal resistances, validating the measurement done with thermoreflectance.

Chapter 4- A Study Comparing Laterally Oriented and Quasi-Vertical Schottky Diode Multipliers

4.1 Introduction

A hypothesis motivating this work is that the quasi-vertical diode (QVD) geometry offers potential improvements in multiplier performance compared to laterally oriented varactors. This chapter compares the planar and quasi-vertical Schottky diode through simulations and experiments in collaboration with Virginia Diodes.

4.1.1 Hypothesis 1 – Diodes with lower series resistance produce higher efficiency multipliers

In this section, a simulation study of a balanced multiplier is performed with series resistance as a swept variable to assess the impact of series resistance on multiplier efficiency.

The results indicate that when presented with the optimized embedding impedances, doubling efficiency to the second harmonic increases with decreasing series resistance (Rs). Furthermore, the value of series resistance impacts the optimal embedding impedances for the diode, which in turn influences the matching network of the circuit. However, when using Rs as a variable in the embedding impedance optimization, the efficiency is maximized when Rs is minimized. Figure 1 shows the doubler simulation described above. Efficiency is determined by sampling the voltage and current waveforms for the second harmonic signal (Eq1 below). Two ideal filters are included to only permit power flow at the fundamental frequency of the excitation source and the second harmonic produced by the diodes implemented in a balanced configuration. The values of the optimal impedances are approximately the same whether the diodes are biased individually or using a single shared DC source. Note that losses associated with a diode mounting structure are not included, so this simulation provides only insight into the effects of series resistance. Parasitics associated with diode's physical geometry are also omitted in this simulation.

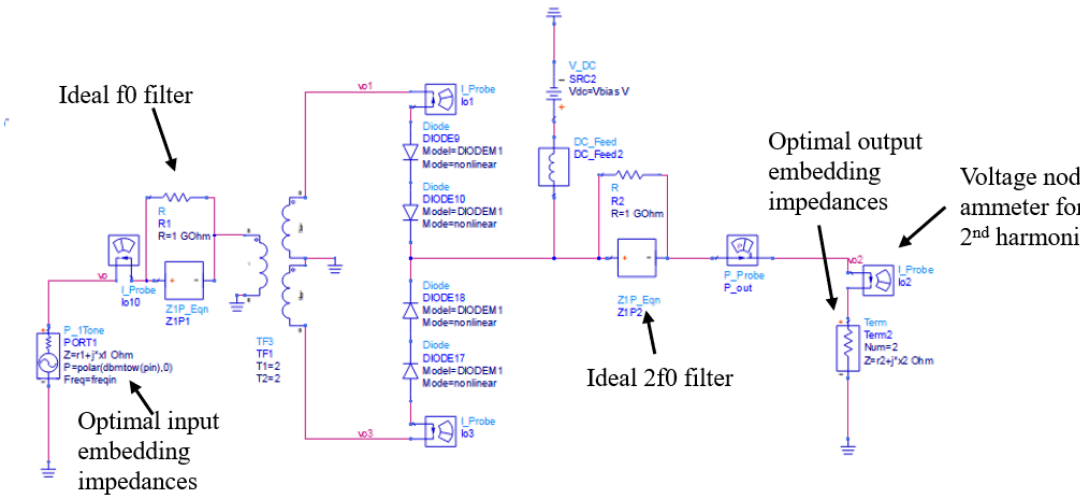


Figure 86 – ADS multiplier schematic for simulation

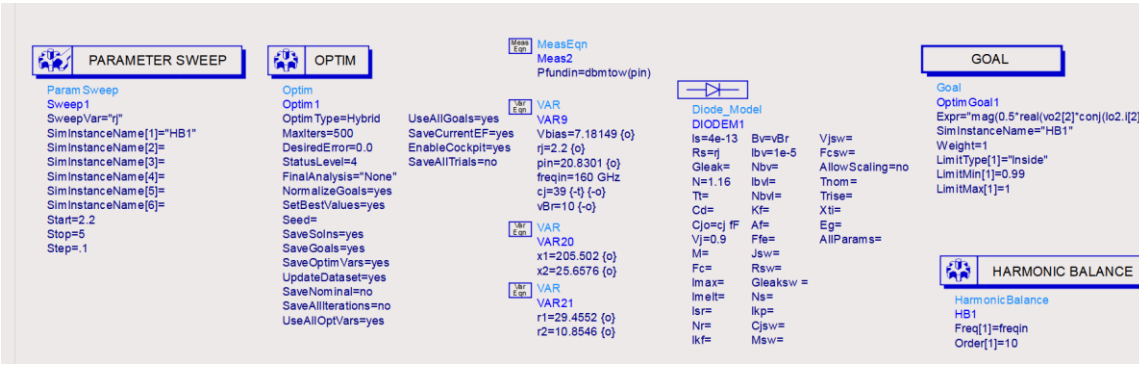


Figure 87 - Simulation Parameters

$$\text{Efficiency} = \frac{\text{re}(V_o[2]) * \text{conj}(I_o[2])}{\text{dBM}(P_{\text{in}})}$$

The parameters for this simulation are included so that readers can replicate it.

Figure 88 – Plot from simulation in Figure1

The material parameters of the diode are based on the R4 varactor epitaxy design detailed in Chapter Two.

The simulation demonstrates that provided a QVD has lower series resistance, multipliers based on this device will produce higher efficiency, as less power is dissipated in the series resistance than multipliers made with planar diodes.

4.1.2 Series Resistance of Schottky Diodes

Researchers have extensively studied the contributions to the series resistance of a Schottky diode. Methods for approximating these contributions are well-established. The following section reviews these expressions, supplemented by simulations.

At high-frequency, the series resistance of a Schottky diode is comprised of the following components [58][59]:

1.) The resistance arising from the lightly doped epitaxial modulation layer.
2.) For lateral diodes, a sheet resistance associated with surface current flows beneath the contact.
3.) Resistance associated with the interface of the ohmic contact with the semiconductor material.
4.) Spreading resistance associated with current flow through the highly doped epitaxial material.
5.) Skin effect contributions.

These contributions are shown in Equation 1.

$$Z_s = R_{epi} + R_{Sheet} + R_{Ohmic} + Z_{spread} + Z_{skin}$$

High-frequency effects, such as skin depth, are often incorporated into buffer region expressions and treated as part of the spreading resistance in the literature. However, in this analysis, they will be considered separately. For the formulation of the series resistance, the

doping concentration and thickness of the semiconductor are sufficient to approximate those mentioned above electrostatic attributed resistances.

The diode lightly doped epitaxial contribution to the series resistance can be approximated by,

$$R_{epi} = \frac{t_{epi}}{\sigma_{epi} * Anode_{area}}$$

When accounting for the diode's epitaxial resistance, the thickness (t_{epi}) of the epitaxial layer is both voltage and frequency-dependent. Under forward bias, the depletion width is assumed to be zero, resulting in the maximum contribution to R_{epi} . [Citations] If negligible current spreading is assumed, Repi can be approximated as:

$$R_{epi}(V_j) = \frac{t_{epi} - w_d(V_j)}{\sigma_{epi} * Anode_{area}}$$

When operating as a varactor for applications such as multipliers, the resistance of the epitaxial layer can be expressed as:

$$R_{epi}(V_j) = R_{epi,min} + \frac{\varepsilon_s}{\sigma_{epi}}(S_{max} - S(V_j))$$

$$S(V_j) = \frac{1}{C_j V_j}$$

The buffer region's contribution is the next component of series resistance to review and perhaps the most complicated when contrasting the lateral and quasi-vertical structures. The

buffer is a highly doped region of GaAs that facilitates the current flow from the epitaxial layer to the cathode's ohmic contact. The current spread out because the buffer layer has higher doping and, therefore, higher conductivity than the epitaxial layer.

Dickens showed an expression for DC spreading resistance using an oblate spheroidal coordinate system [62].

$$R_{spread} = \frac{1}{4\sigma r}$$

Where r is the radius of the metal contact.

Chaplin and Eisenstein found that the complex bulk-spreading impedance is given by [64],

$$Z_{spread} = R_{spread}(\left(\frac{1}{1 + j\frac{\omega_0}{\omega_c}}\right) + j\frac{\omega_0}{\omega_d})$$

They also found that the impedance due to the skin effect was given by,

$$Z_{skin} = \frac{\ln(\frac{r_{oc}}{r_a})}{2\pi}\sqrt{\frac{j\omega\mu_0}{\sigma}}\sqrt{\frac{1}{1+j(\frac{\omega}{\omega_s})+j(\frac{\omega}{\omega_d})}}$$

It's important to note that these equations were derived initially for point contact devices and adapted for the lateral device; however, due to multiple mechanisms affecting the diode structure's impedances, these should be treated as approximate models.

Similarly, Bhaumik found that the sheet resistance due to Ohmic Contact in the Lateral Diode is divided by the conductivity in the n++ region multiplied by the smaller values, the radius of the ohmic contact annulus, or the thickness of the substrate [63].

$$R_{sheet} = \frac{1}{\sigma \min(t_{sub}, r_{oc})}$$

The ohmic contact resistance can be approximated as follows:

$$R_{ohmic-contact} = \frac{\rho_c}{A_{contact}}$$

Virginia Diodes provided their material parameters for the diodes used in the experiment, described in Section 4.3. The conductivity and thickness of the various layers are set accordingly and the total series resistance is calculated for both diodes.

	Diode Parameters	
	UVA	VDI
Epi Thickness	$t_{epi} = 280nm$	$t_{epi} = 300nm$
Epi Doping	$N_d = 2 * 10^{17}$	$N_d = 3 * 10^{17}$
Buffer Doping	$N_d = 5 * 10^{18}$	$N_d = 1 * 10^{18}$
Buffer Thickness	$t_{buffer} = 1\mu m$	$t_{buffer} = 3\mu m$
Specfic Contact Resistance	ρ_c = 8*10^-7	ρ_c = 1*10^-6

Table 8 – Material parameters for the VDI and UVA diodes

The total series resistance is estimated for both diodes. The area of the ohmic layer used for the lateral was approximately 1500um^2, while the area used for the QVD was approximately 400um^2.

	Lateral Calculation Ω	QVD Calculation Ω
Repi	1.62	1.15
Rbuffer	.66	.66
Rskin	.62	.42
Rsheet	1.77	-
ROhmic	.1	.48
Total	4.77	2.29

Table 9 – Result of calculations using the equations above.

4.1.3 Electrostatic Simulation of Lateral and Quasi-vertical Diode

An Ansys Maxwell DC conduction simulation was conducted for both the QVD and the lateral diode. These simulations were designed to confirm the expected values of series resistance. Theoretically, the resistances arising from the epitaxial layer and spreading (excluding skin effects) can be validated through DC conduction simulations.

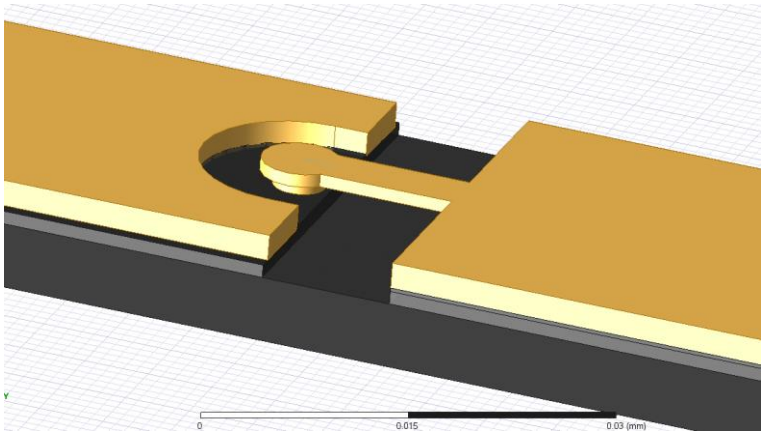


Figure 89 - Lateral Device model in Ansys Electronics Desktop

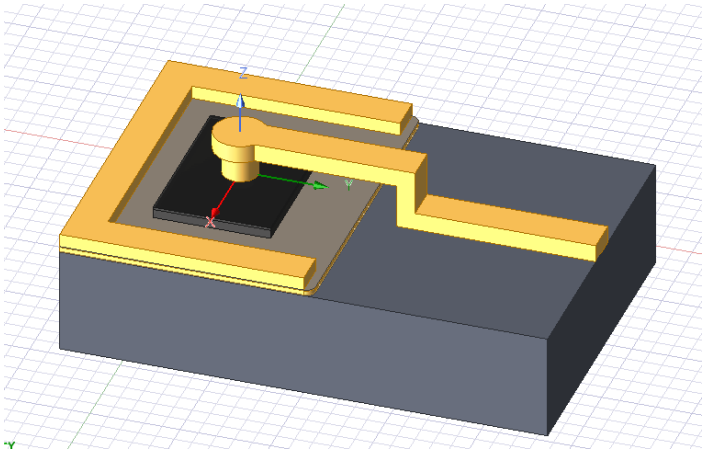


Figure 90 – QVD model in Ansys Electronics Desktop

A current source was used in this simulation, set to 1 mA. The sink for the current source is shown in the diagram below. The current source for both simulations was put on the finger of the diode, and the sink for the lateral device was set to the edge of the epi and the underlying

ohmic metal contact. For the first round of simulations, the conductivity for the epi and buffer layers was based on the R4 GaAs epitaxy, denoted in Chapter 2, and used for both simulations to isolate the differences between these two devices. The anode diameter is set to 4um for both simulations.

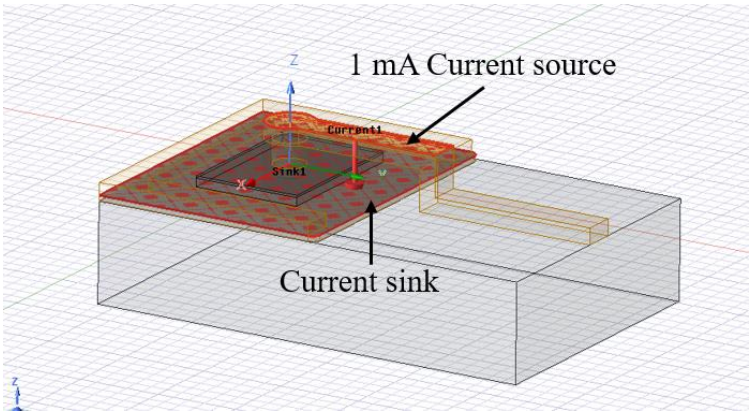


Figure 91 – Screenshot of the Maxwell CAD of the QVD showing the Maxwell Excitations

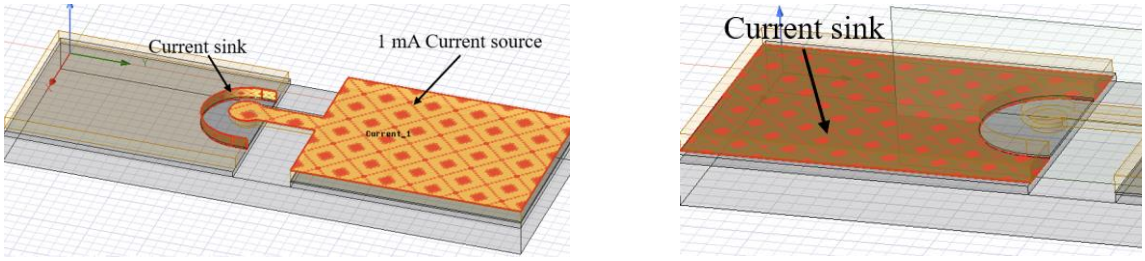


Figure 92 - Screenshot of the Maxwell CAD of the Lateral diode showing the Maxwell Excitations

The current density was plotted to visualize the current distribution and loss distribution. The plots are shown below. The lateral diode and QVD magnitude of the current density vector $|\vec{J}|$, contribute to our hypothesis that the lateral device's resistance could be twice that of the quasi-vertical device since the current is confined to one direction.

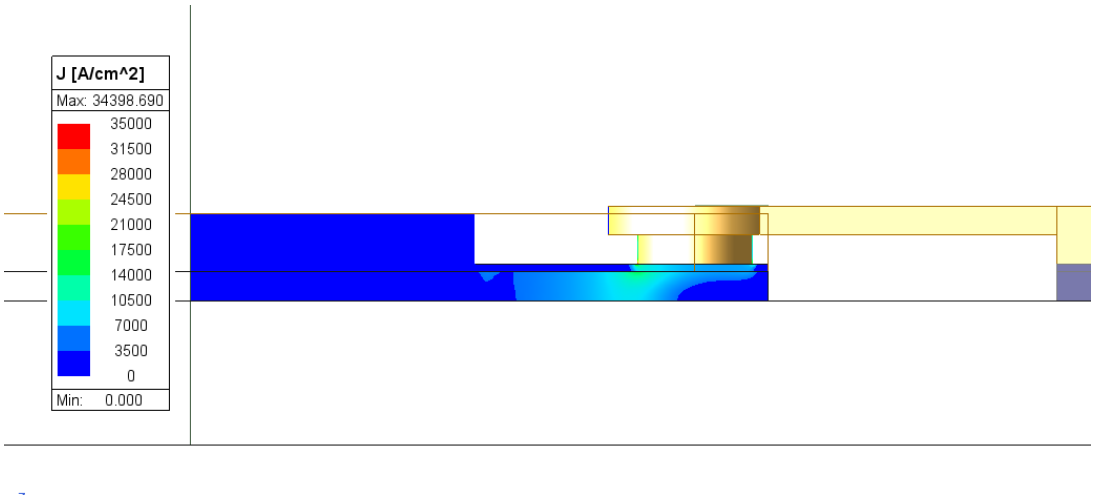


Figure 93- Lateral diode Magnitude of current density vector $\vec{J}$

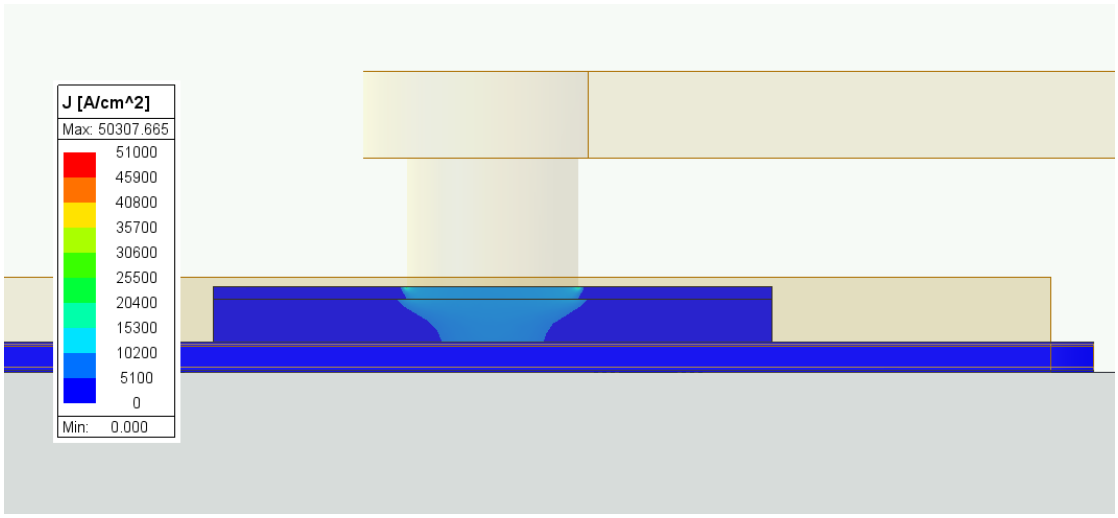


Figure 94-QVD Magnitude of current density vector $\vec{J}$

Ohmic or resistive loss occurs in conductive materials when an alternating current (AC) or direct current (DC) flows through them. It results from the material's electrical resistance, which dissipates energy in the form of heat. Ansys Maxwell enables users to isolate the specific materials in defined geometry and calculate its contribution to the total ohmic loss. Ohmic loss is defined with the equation below:

$$P = \iiint \frac{J \cdot J^*}{2\sigma} dx\, dy\, dz$$

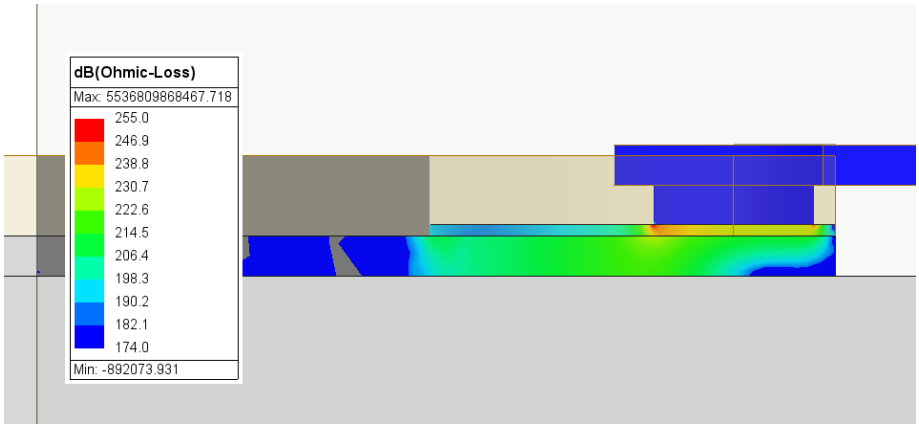


Figure 95 – Ohmic loss profile for Lateral Diode.

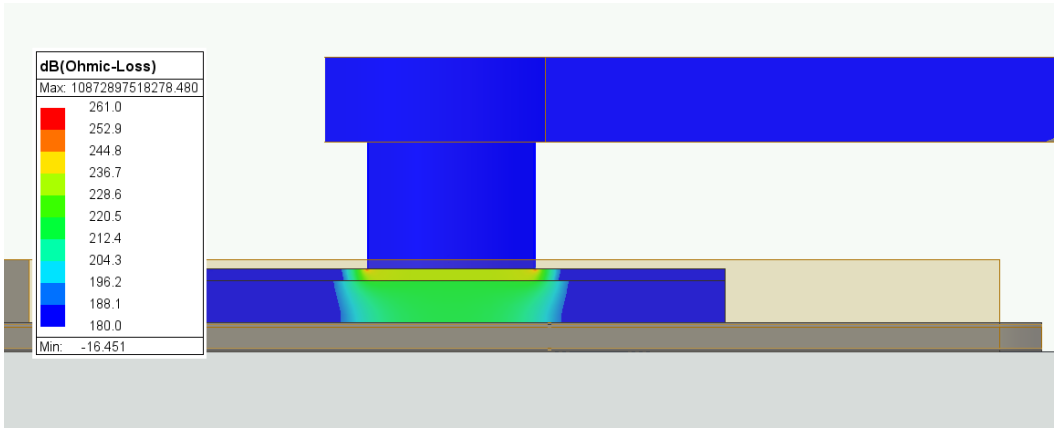


Figure 96 – Ohmic loss profile for QVD

Since we set the current source to 1mA, we can utilize the relationship between power and current, namely, $P = I^2R$, using the field calculator, we can extract the resistance.

QVD Components with 1um Buffer	R=$\frac{P}{I^2}$ (using 1 mA for I) and Integral of Ohmic loss in the volume (Epi and Buffer) for P.
Total	1.97 Ω
Epi	1.5 Ω
Buffer	.47 Ω

Table 10 – Maxwell Simulation Results for QVD

Lateral Components with 3um Buffer	R=$\frac{P}{I^2}$ (using 1 mA)
Total	3.32 Ω
Epi	1.69 Ω
Buffer	1.63 Ω

Table 11- Maxwell Simulation Results for Lateral

The solutions for the DC conduction simulation does not match the expected values from electrostatic expressions.

$$R_{epi-QVD} = \frac{t_{epi}}{\sigma_{epi} * Anode_{area}} = 1.15$$

This value is inconsistent with the resistance measured in the simulation. However, Crowe noted that the current is confined in a smaller area than in the diameter of the diode [61]. A parametric sweep in Maxwell of diode diameter was performed to determine the percentage of the anode area current is confined. The ohmic loss was measured and converted to resistance for each data point using the expression: $R = \frac{P}{I^2}$. This data was exported, and MATLAB's curve fitting toolbox was used to find a coefficient (k) scaling the area. It was found that k=.8696,

which potentially suggests that current is confided in 86.96% of the area set by the diameter of the anode.

$$R_{epi-QVD} = \frac{t_{epi}}{\sigma_{epi} * k * Anode_{area}} = 1.5$$

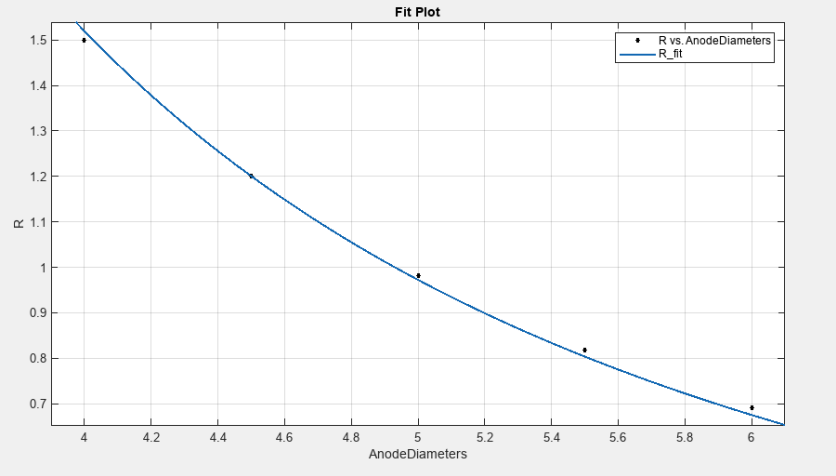


Figure 97 – Fit versus measured data

Goodness of Fit

	Value
SSE	0.0010
R-square	0.9976
DFE	4.0000
Adj R-sq	0.9976
RMSE	0.0158

Figure 98 – Goodness of fit for Figure 98

The modified formula for the epi's contribution to the resistance was sufficient to match the maxwell simulation for the lateral diode. It was found that k=.8696, meaning that current is

confided in 86.96% of the area set by the diameter of the anode for both the QVD, and this also works for the lateral diode with a .3um epi thickness. Note: Crowe did not find an expression for current that is confided to a smaller area under the anode.

$$R_{epi-lateral} = \frac{t_{epi}}{\sigma_{epi} * k * Anode_{area}} = 1.69$$

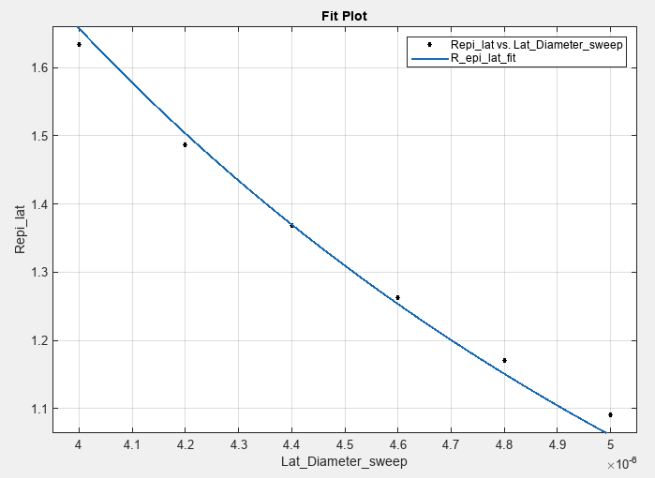


Figure 99 - Fit versus measured data

Goodness of Fit

	Value
SSE	0.0022
R-square	0.9891
DFE	5.0000
Adj R-sq	0.9891
RMSE	0.0212

Figure 100 – Goodness of fit for Figure 100

A similar procedure determined the correction needed for Dicken's spreading resistance formula. Using the formula derived from Dicken's oblate spheroidal, he obtained:

$$R_{spreading_{DC-QVD}} = \frac{1}{4\sigma r} = \ 0.665$$

This value is inconsistent with the resistance measured in the simulation; furthermore, there are multiple expressions to total the contribution to the spreading resistance, such as the contributions from Rsheet and Zpread, which would not be present and minimized in the quasi-vertical diode, respectively. Therefore, we opted to simplify the derivation of the spreading resistance as proof that the resistance is less in the QVD.

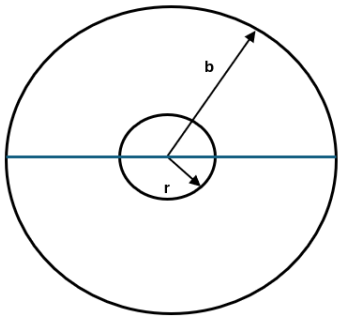


Figure 101 - Cylindrical shell diagram used to visualize the electric field's integration for the QVD.

For a cylindrical shell with an inner radius of r, the outer boundary at b, and height/thickness of t_{buff} the current density J is : $\vec{J} = \frac{I}{2\pi r t_{buff}}$, following Maxwell's correction to Ampere's law.

$$\vec{J} = \sigma\vec{E}$$

$$E = \frac{I}{2\pi\sigma r t_{buff}}$$

$$\mathrm{V} = \int_r^b \frac{I}{2\pi r t_{buff}} \cdot dl = \frac{I \ln(\frac{b}{r})}{2\pi\sigma r t_{buff}}$$

$$\mathrm{R} = \frac{V}{I} = \frac{\ln(\frac{b}{r})}{2\pi\sigma r t_{buff}}$$

It's unknown what the actual geometry of the current spreads in; it depends on several factors: conductivity of the epi and the buffer, if walls are chamfered or filleted, the diameter of the anode, whether the mesa is partially etched or passivated, etc. This approximation is used for non-linear curve fitting the simulation results from a parametric sweep of diode diameters, along with the observations from the Maxwell field distribution shown above to provide intuition as to the spreading geometry and confirm the hypothesis that the series resistance in the lateral diode is reduced in comparison to QVD.

A similar parametric sweep of the diode diameter was performed, keeping the buffer's thickness and all other values constant.

$$R_{buffer} = \frac{\ln\left(\frac{k * r}{r}\right)}{m * 2\pi r t_{buff}}$$

$R_{buffer\_QVD} = \frac{\ln\left(\frac{2.3*r}{r}\right)}{1.5*2\sigma\pi r t_{buff}} =$ 0.470076610147010, which is consistent with the simulation.

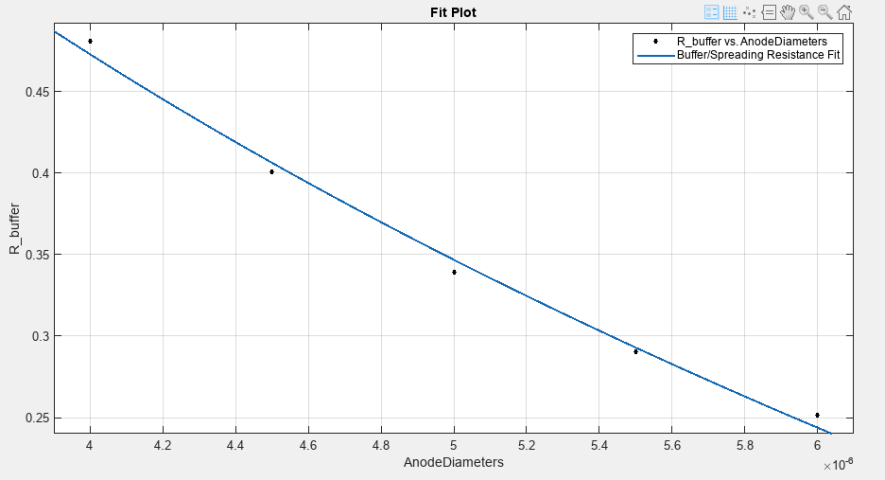


Figure 102- Fit versus measured data

Goodness of Fit

	Value
SSE	0.0002
R-square	0.9933
DFE	3.0000
Adj R-sq	0.9911
RMSE	0.0086

Figure 103 - Goodness of fit for Figure 103

The same procedure was applied to modify the lateral diode's spreading resistance equation. We expect the same formula to hold if the cylindrical shell is effectively halved, as the current spreads through only half of the structure.

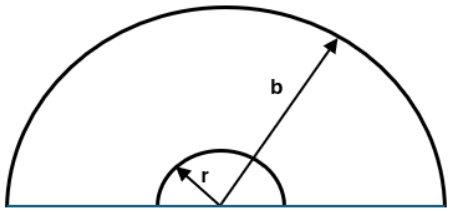


Figure 104- Cylindrical shell cut in half used to visualize the electric field's integration for lateral diode.

$$R_{buffer} = \frac{\ln\left(\frac{k * r}{r}\right)}{m * 2\pi\sigma t_{buff}}$$

$R_{buffer-lateral} = \frac{\ln\left(\frac{4.5*r}{r}\right)}{.5*2\sigma\pi r t_{buff}} =$ 1.6, which is consistent with the simulation.

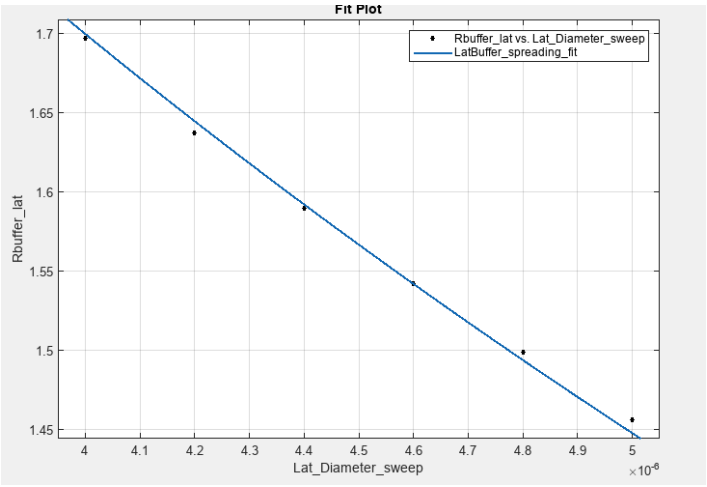


Figure 105 - Fit versus measured data

Goodness of Fit

	Value
SSE	0.0000
R-square	0.9992
DFE	4.0000
Adj R-sq	0.9989
RMSE	0.0029

Figure 106 – Goodness of fit for Figure 21

When comparing the buffer layer DC-attributed resistances, we can notice that the Buffer layer's contribution is approximately 3.4 times higher than that of QVD.

$$R_{buffer\_QVD} = \frac{\ln\left(\frac{2.3*r}{r}\right)}{1.5*2\sigma\pi r t_{buff}} = .47$$

$$R_{buffer-lateral} = \frac{\ln\left(\frac{4.5*r}{r}\right)}{.5*2\sigma\pi r t_{buff}} = 1.6$$

	QVD	Lateral
Buffer Fit parameter- k	2.3	4.5
Buffer Fit parameter - m	1.5	.5
R_{buffer}	.47 Ω	1.6 Ω
R_{epi}	1.5 Ω	1.68 Ω
$R_{buffer} + R_{epi}$	1.97 Ω	3.28 Ω

Table 12 – Summary of fitted results for QVD vs Lateral Diode.

This work shows that the DC-attributed resistance for the Lateral diode is approximately 1.67 times higher than that of the QVD. Future work will consider the RF-attributed resistances, and Chapter 5 will describe a procedure for simulating and measuring it. When these diodes are used as varactors, the resistance due to the epitaxial region is minimized proportional to the depletion width; therefore, the resistances captured in this section don't correspond to the exact resistance seen during AC operation; however, the impedances are scaled by these resistances.

4.3 Hypothesis 2: Improved Heat Dissipation

Our second hypothesis is that the QVD has improved thermal performance compared to the lateral diode.

This benefit is potentially due to several factors, including:

1) The buried ohmic contact provides an integrated heatsink, as it is directly under the buffer region for the QVD, potentially enabling better thermal conduction since the current doesn't have to spread through the buffer, resulting in less loss and less resistance to dissipate power.
2) The QVD is heterogeneously integrated into silicon, which has a higher thermal conductivity and specific heat capacity than AlGAs.

These factors suggest that QVDs have lower thermal resistance and faster cooling transients than lateral diodes. The prior art has characterized the thermal characteristics of both the lateral Diode and QVD separately, though there has not been a direct comparison between these two diodes. These results showed comparable measured thermal resistance and transient cooling times [53][57].

Icepak was used to compare the thermal resistance and transient cooling times using the same documented procedure as shown in Chapter 2.

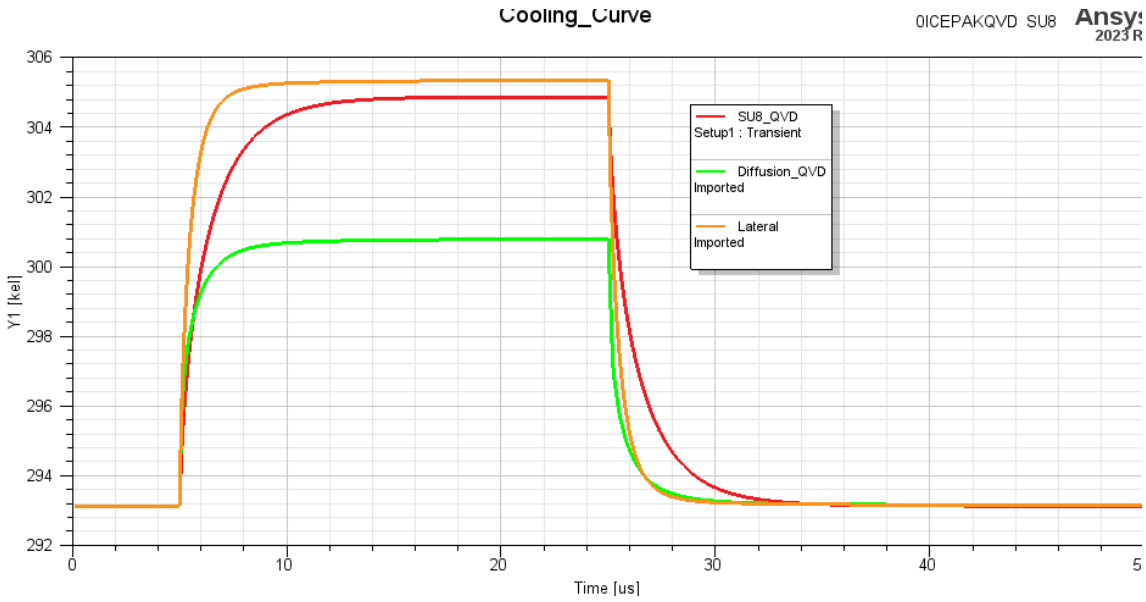


Figure 107 - ICEPAK Thermal Analysis

The cooling curve displayed shows the temperature response of different QVD types and a lateral diode over time. The plot compares the transient cooling behavior of SU8-QVD, Diffusion-QVD, and a Lateral diode. Initially, all devices experience a rapid increase in temperature, reaching peak values within approximately 5 microseconds. The SU8-QVD (red curve) reaches the highest temperature of about 305 K, indicating higher thermal resistance than the other two devices. The Diffusion-QVD (green curve) and the Lateral diode (orange curve) demonstrate lower peak temperatures, with the Diffusion-QVD peaking at 300 K. After reaching their peak temperatures, all devices exhibit a cooling phase, with the SU8-QVD cooling slower than the Lateral diode. In contrast, the Diffusion-QVD cools more efficiently, suggesting it may

be an ideal candidate for improved thermal management. However, the SU8-QVD and Lateral diode are primarily considered for comparing multipliers; therefore, we expect the SU8-QVDs not to get as hot.

4.4 Experiment

We set up an experiment to fabricate multipliers based on multiplier chips designed at Virginia Diodes. The CAD drawings for multipliers were provided by Virginia Diodes and incorporated into our photolithography mask set. The diode-to-diode spacing was kept constant; the airbridge distances were slightly different when accounting for UVA design rules. Several chips were fabricated with varying sizes of anode: 5.7, 5.5, 5.3, 4.7, 4.5, and 4.3 µm anode diameters to account for variations in fabrication. The bonding process used for these diodes used SU8. Three variations of these chips were produced:

1. Chips with free-standing beam leads.
2. Chips with side-wall plated vias.
3. Chips resembling Virginia Diodes' multiplier design are intended for flip-chip mounting. These featured only metalized pads on the top side for soldering onto a carrier substrate.

With the analysis presented above, we expect that the QVD-SU8 should have comparable heat performance and that the efficiency should be slightly increased due to lower series resistance.

Multiplier chips: These designs are shown in the Figure 109.

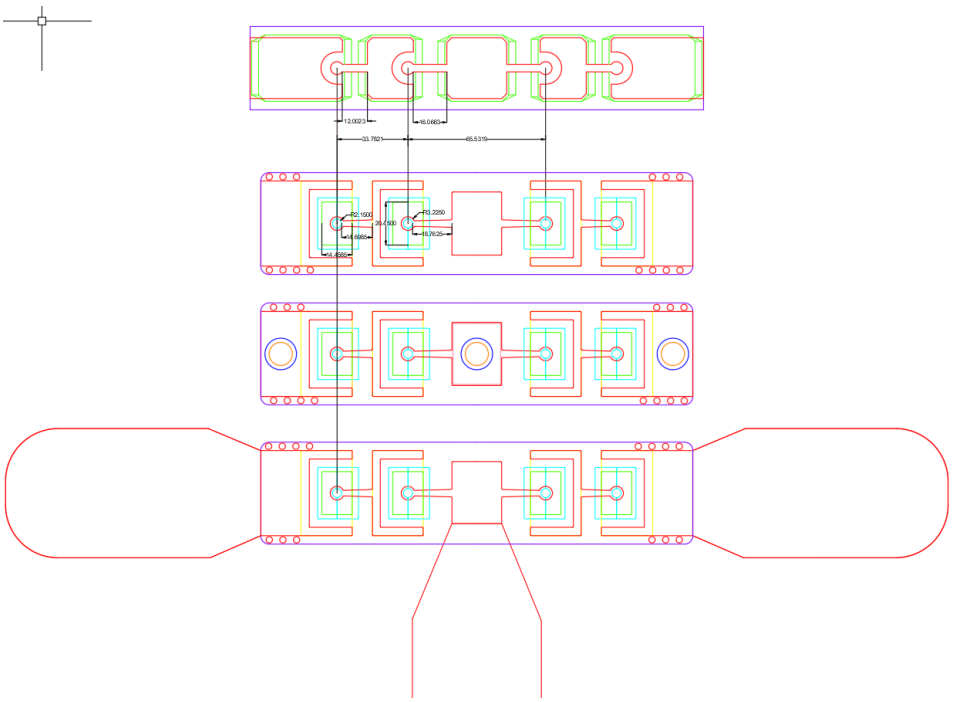


Figure 108 – Lateral diode chip versus QVD diode chips made for this experiment

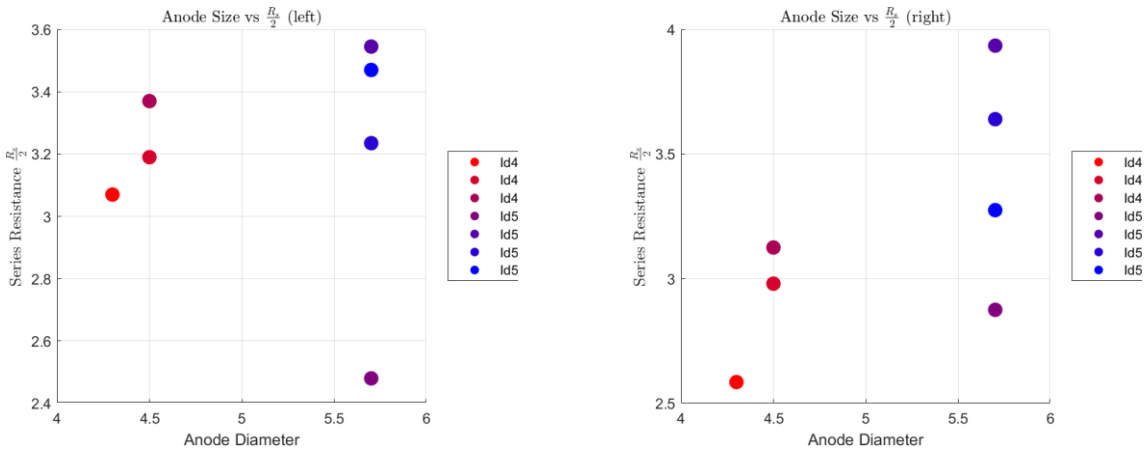
4.5 Experimental results

UVA delivered all the chips made from the fabrication process on the mask set mentioned in Chapter Two to Virginia diodes for testing and characterization.

4.5.1 Round 1

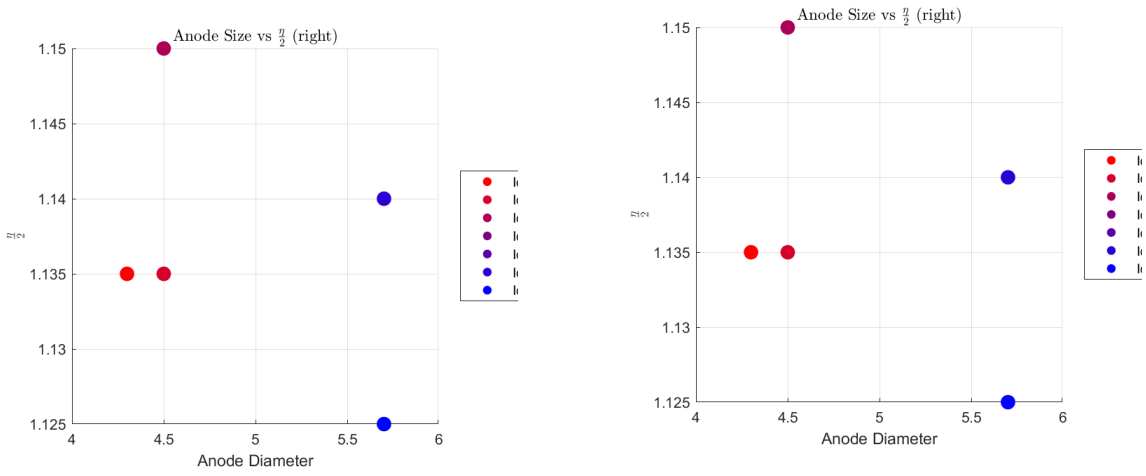
The first set of measurements was taken on 2/14/2024. VDI assembled and tested several multipliers using QVD-based chips. The DC current-voltage (IV) characteristics were measured

on chips containing two series-connected diodes. Due to the diodes being measured in series, the ideality factor and series resistance are approximately twice that of a single-diode device.



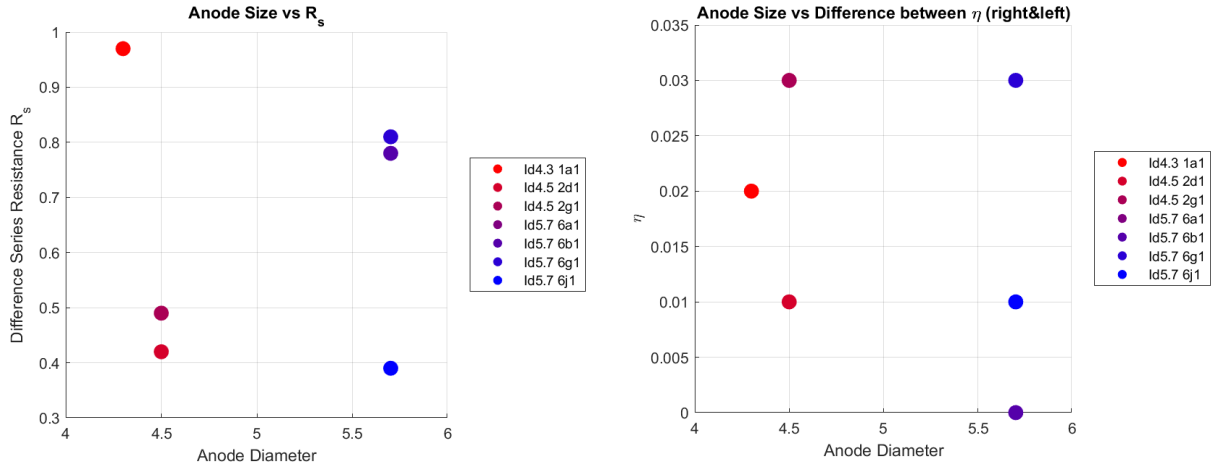
(a) (b)

Figure 109 – Series Resistance vs. Anode Diameter (a) left side of multiplier chip (b) right side of multiplier chip



(a) (b)

Figure 110 - Ideality factor vs Anode Diameter (a) left side of multiplier chip (b) right side of multiplier chip



(a) (b)

Figure 111 – (a) Difference in Series Resistance (left vs right) (b) Difference in Ideality(left vs right)

These results were used to select devices to incorporate into multiplier circuits. Steve Retzloff of Virginia Diodes tested these multiplier builds and compiled this plot comparing two UVA 5.7um anode diameter circuits labeled "VDI330X2_R1 B104B 5.7QVD" and "VDI330X2_R1 B103B 5.7 QVD."

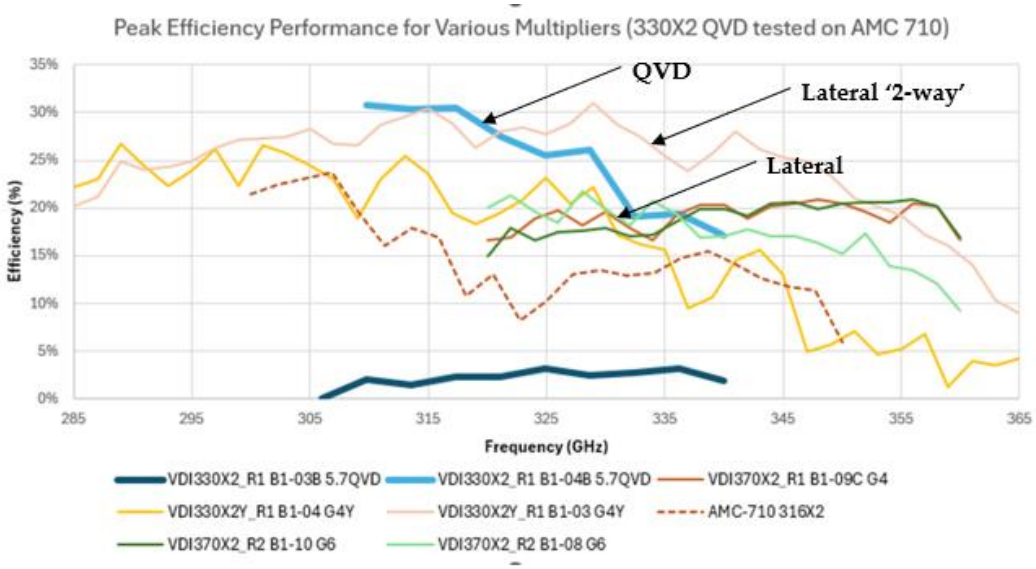


Figure 112 – Testing results from round 1 of testing QVDs vs previously tested lateral diodes.

The QVD circuit, B103B, didn't function. Since hundreds of devices are available to test, another multiplier was assembled instead of troubleshooting the problem. B1-04 did, however, function, showing >30% peak efficiency. Data from several previously tested VDI Lateral device multiplier builds were pulled for comparison. "VDI330X2Y_R1 V1-03 G4Y," a two-way power-combined multiplier, was the only lateral-based device with peak efficiency like the QVD build.

The "VDI370X2_R2 B1-08 G6" single-stage doubler shows >20% peak efficiency; however, its operating frequency range doesn't match the well-performing QVD build. These builds were further analyzed in MATLAB to visualize the various operating conditions.

The average chip temperature, output power, and efficiency were calculated using MATLAB's mean function. The temperature measurement technique is based on what is described in sections VI A & B of [57]. But instead of using a parameter analyzer, VDI has custom electronics that turn off the RF source while applying a fixed current to the varactor and then monitor the voltage as the diode cools. Between the transient setting times and DAQ acquisition rate, the first uS or two of cooling data is lost. This introduces some unknown offset in the measured temperature, but we can compare different builds as long as they are consistent.

	B1-04B 5.7 QVD	B1-08G6 Lateral	Difference
Average Chip Temp	303.4 [K]	312.8 [K]	9.367 [K]
Average Output Power	44.9 [mW]	27.8 [mW]	17.1 [mW], 12.3 [dBm]
Average Efficiency	25.3 [%]	17.2 [%]	8.03 [%]

Table 13 – Summary of Round 1 testing for B104B QVD and B1-08G6 Lateral

The average chip temperature, output power, and efficiency were calculated using MATLAB's mean function. These results are shown below:

	B1-04B 5.7 QVD	B1-03 Lateral	Difference
Average Chip Temp	303.4 [K]	311.7[K]	8.263 [K]
Average Output Power	44.9 [mW]	43.7[mW]	1.28[mW], 1.095[dBm]
Average Efficiency	25.3 [%]	23[%]	1.9[%]

Table 14 - Summary of Round 1 testing for B104B QVD and B1-03 Lateral (Two-way power combined multiplier)

4.5.2 Round 2

Round 2 compared power combined multipliers between the lateral and QVD and tested single 4.3 diameter-based multipliers. The power combined multipliers were two multiplier chips in parallel and power combined through a waveguide magic tee.

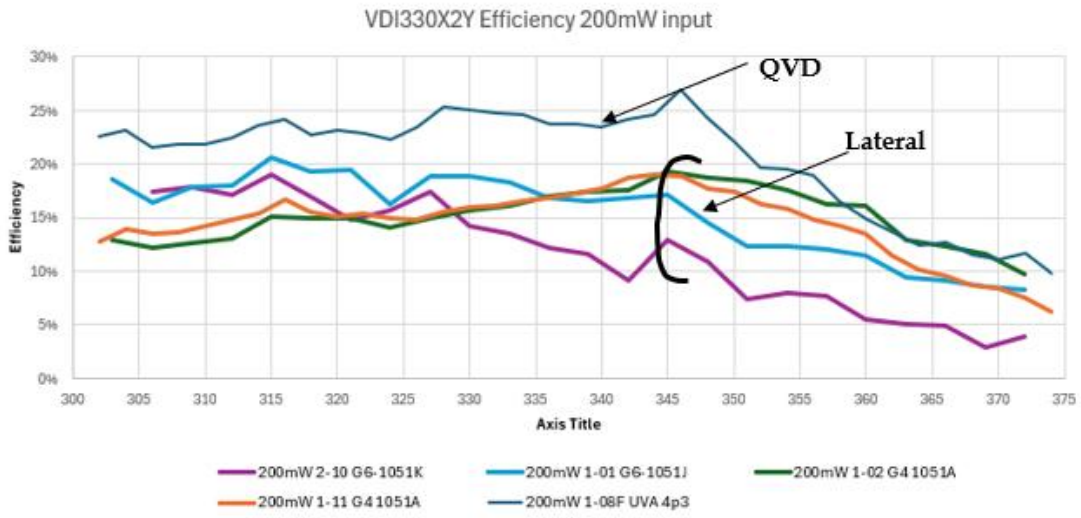


Figure 113 – Power combined multiplier comparison from Round 2 of testing.

During this round of testing, the only comparative study conducted focused on these power-combined multipliers. ChatGPT 4o with canvas was used iteratively to debug a MATLAB script to process the dataset provided by VDI. The maximum efficiency of the power-combined multipliers with the lateral diode variant was 20.9%, with a mean output power of 20 mW and corresponding maximum output power of 58 mW. Temperature was recorded on two separate channels representing the two multipliers, with mean values of 45°C for channel 1 and 40°C for

channel 2, and maximum temperatures of 56°C and 47°C, respectively. In the best case, the maximum output power reached 77 mW, corresponding to a mean efficiency of 17.3% and a peak efficiency of 20.6%. In this scenario, the temperature measurements were 45.6°C for channel 1 and 40°C for channel 2 (mean values), with maximum temperatures of 51°C and 43°C, respectively.

The maximum efficiency recorded for the power-combined QVD multipliers was 27%, with a mean output power of 38 mW and a maximum output power of 53 mW. Temperature was recorded on two separate channels representing the two multipliers, with mean values of 29.8°C for channel 1 and 29.6°C for channel 2, and maximum temperatures of 31.2°C and 31.8°C, respectively. The best-case maximum output power achieved was 87 mW, with a mean efficiency of 18% and a peak efficiency of 23%. In this scenario, the mean temperature was 33°C and 32.4°C, while the max temperature was 34.861°C and 33.681°C.

	Max Efficiency	Max Output Power in Max Efficiency Dataset	Temperature Channel 1	Temperature Channel 2
B210Y (Lateral)	20.9 %	58mW	56.4°C	47°C
B108Y (QVD)	27.0 %	53mW	31.2°C	31.8°C

Table 15 – Round two testing results B210Y Lateral versus B108Y QVD - Max Efficiency

	Max Output Power	Max Efficiency in Max Output Power Dataset	Temperature Channel 1	Temperature Channel 2
B210Y (Lateral)	77mW	20.6%	51.8°C	43.3°C
B108Y (QVD)	87 mW	18%	34.8°C	33.68°C

Table 16 - Round two testing results B210Y Lateral versus B108Y QVD- Max Output Power

4.5.3 Round 3

A final round of testing was done with single-stage multipliers across 300 – 420 GHz.

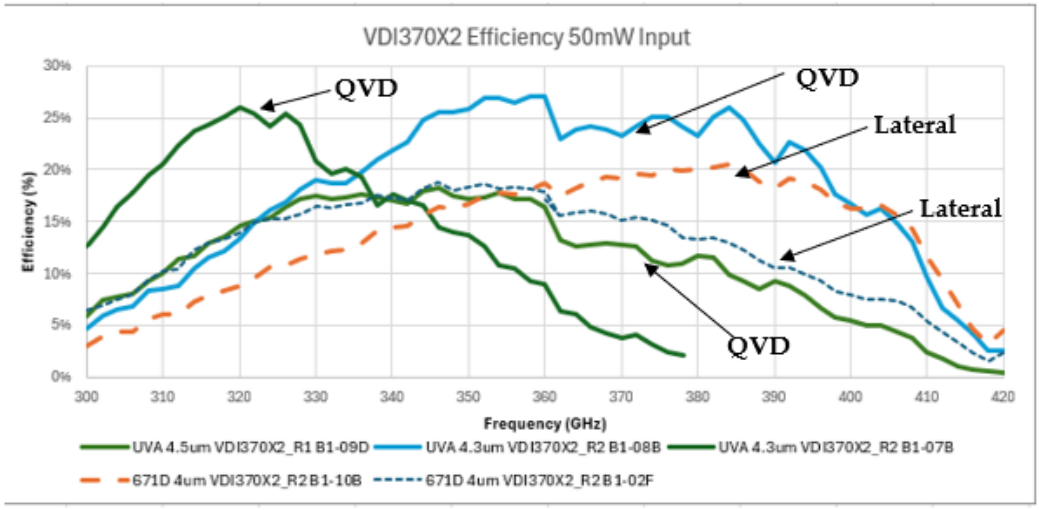


Figure 114 – Single-stage multiplier comparison from Round 3 of testing.

The results indicate that QVD- B108 had the highest record efficiency across the data set at 27.10% max efficiency, with a corresponding output power of 14 mW, and 30.47 C° max temperature for that dataset. The QVD-B108 had a maximum output power of 38.21 mW, corresponding to

	Max Efficiency	Max Output Power in Max Efficiency Dataset	MaxTemperature Channel 1
B109 QVD	21.92 %	33.3 mW	50.16° C
B102 Lateral	18.8 %	10.01 mW	33.18° C
B107 QVD	25.98 %	13.55 mW	32.37° C
B108 QVD	27.10 %	14.03 mW	30.47° C
B110 Lateral	20.8 %	30.61 mW	45.63° C

Table 17 – Summary of Result for Round 3 of testing – Max Efficiency

	Max Output Power	Max Efficiency in Max Output Power Dataset	Temperature Channel 1
B109 QVD	33.8 mW	21.92 %	50.15° C
B102 Lateral	24.73 mW	16.52 %	45.29° C
B107 QVD	38.21 mW	25.92 %	37.68° C
B108 QVD	38.21 mW	25.9 %	37.6° C
B110 Lateral	30.6 mW	20.8 %	45.63° C

Table 18 - Summary of Result for Round 3 of testing – Max Efficiency

4.5.4 Result Summary and Discussion

Round 1 tested two multiplier builds. One of the builds failed to function, while the second build indicated that the QVD performed well enough to justify further development and testing of additional multipliers. Round 1 showed a 10 K difference between the measured chip temperature of the QVD and the lateral/planar builds using VDI custom electronics. The QVD demonstrated higher output power and greater efficiency compared to single-stage multipliers selected by VDI for comparison. In datasets with comparable efficiency, power-combining multipliers were considered, but the chip temperature for the QVD was much lower, suggesting that the QVD diodes could handle significantly higher power levels than the lateral diodes before self-heating limits multiplication performance.

Round 2 compared power-combining multipliers. Similar to Round 1, the QVD produced better efficiencies, higher output power, and lower chip temperatures.

Round 3 compared single-diode builds and provided the best comparison in matching the devices' frequency bands. All of the QVDs showed higher efficiencies, greater output power, and lower chip temperature, although one of the builds did not perform as well thermally.

4.6 Conclusion

The simulations and measurements above suggest that the QVD (Quasi-Vertical Diode) offers several advantages over lateral diodes. The reduction in spreading resistance in the buffer layer could contribute to higher multiplier efficiencies.

Additionally, the lower operating temperature and faster cooling observed (in simulation) for the QVD suggest that less cooling power may be required in compact environments. This enhanced cooling and reduced thermal resistance could improve operational stability by maintaining mobilities and conductivities. When self-heating occurs, carrier injection into the material can increase scattering and other effects that degrade conductivity. These changes in conductivity impact current density and can reduce the current associated with the saturation velocity, which is a critical limiting factor in multipliers and other components utilizing Schottky diodes. The SU8-QVD multipliers demonstrated improved conversion efficiencies, likely attributable to decreased series resistance. The devices operated at lower temperatures and generated higher output power. The study represents a rigorous effort to standardize experimental conditions by fabricating chips with minimal variations, mounting them in similar blocks, and testing them under identical conditions. To the best of my knowledge, this is the only comparison of its kind and represents an important body of work. It contrasts the various resistance mechanisms and demonstrates the heating effects when simulated under closely matched conditions and geometries.

Chapter 5 - Conclusion, Future Work, References, Appendix

Conclusion

The research spans several critical aspects of the QVD, from developing dedicated masks and processes to analyze yield across an entire wafer, advancing the fabrication of closed-spaced diodes and circuits, and exploring thermal performance improvements through diffusion bonding. This thesis presents a comprehensive study on the ohmic characterization of quasi-vertical diodes (QVD), focusing on ohmic contact resistance as a function of position across the wafer. This focus was crucial to eliminate suspicions that inconsistent ohmic contact resistances could affect yield or performance variations across the wafer after fabrication.

The work introduces innovations in the fabrication process, such as changing the order of the fabrication steps in order to improve fabrication tolerances, optimized etch rates for CF_4/Ar etching of the ohmic metal layers, and improvements in wet-based metal etching by replacing the resist-degrading HG solution with a diluted TFA gold etch type A. Additionally, a new method for fabricating side-coated vias was developed using a stepped lithography approach involving long-exposure lithography, sputtering, and ultrasonic-assisted electroplating. Each process for manufacturing the QVD and its significance were described.

This optimized process enabled the first diffusion-bonded QVD and enabled the first report of a diffusion-bonded metal-to-metal GaAs Schottky QVD heterogeneously integrated onto silicon, representing a significant advancement in high-frequency Schottky diode technology by enabling higher power handling. Experiments were planned and conducted sequentially to achieve diffusion bonding. The process began by bonding two bulk-silicon wafers and using SEM to examine the interface, which showed distinct wafer layers with a continuous bonding interface. Afterward, multiple SOI wafers were bonded using both adhesive and diffusion techniques. After removing the wafer handle, a blister-free film was observed with the optimized bonding parameters. In collaboration with Laser Thermal, the differential thermal conductance between SU8 and diffusion bonding was characterized using steady-state thermoreflectance, confirming that diffusion bonding exhibited lower thermal resistance than SU8 adhesive bonding. Based on these findings, the decision was made to proceed with the more expensive GaAs material. Initial attempts to bond GaAs using the parameters and metal stack from SOI bonding were unsuccessful. By etching away the metals and conducting EDS, it was determined that Ti and Au had alloyed and diffused into the Silicon. This observation

highlighted that diffusion was the primary bonding mechanism for the metal layers. Consequently, it was hypothesized that adding a diffusion barrier to both sides of the metal interface would inhibit gold from alloying with titanium and diffusing into the Silicon, thereby promoting selective diffusion at the bonding interface. This approach proved effective, and the optimized process detailed in Chapter 2 was employed to fabricate the first diffusion-bonded GaAs QVD. Due to the alloying of the ohmic metals, a single process modification was required, necessitating the addition of an HCl etch alongside the previously used KI etch to remove the ohmic metal stack adequately.

A photolithography mask set was developed to characterize the QVD under both reverse and forward bias conditions. The results revealed that the diffusion-bonded devices demonstrated significantly higher power handling potential than adhesive-bonded diodes and had comparable results (ideality, series resistance, and high-frequency parasitic) with prior art. Transient thermoreflectance measurements and Ansys ICEPAK simulations showed that the diffusion-bonded QVDs cooled significantly faster than those fabricated using SU8, highlighting the advantages of diffusion bonding in reducing thermal resistance and improving cooling efficiency. These findings suggest that QVDs have the potential to operate at lower temperatures with enhanced thermal stability, which is critical for maintaining carrier mobility and conductivity while being pumped with RF, especially in high-frequency applications.

A direct comparison between lateral and QVD-based multipliers was conducted to evaluate the potential advantages of these technologies. This comparison involved collaboration with Virginia Diodes to design a chip that replicated their geometry, including diode-to-diode

spacing and finger lengths. The chips used in this experiment were fabricated before the development of the diffusion-bonded diodes, meaning the comparison was performed with adhesive-bonded diodes. Ansys Maxwell was employed to standardize comparing resistance mechanisms and thermal effects in QVDs versus planar diodes under closely matched conditions and geometries. Simulations indicated the advantages of QVDs over lateral diodes, particularly regarding reduced spreading and thermal resistance, which could contribute to enhanced multiplier efficiencies. Both lateral and QVD diode chips were assembled into identical waveguide housings with consistent matching networks. Frequency sweeps were conducted, and optimal DC biasing was determined for each frequency. Temperature and output power were recorded, and mean and maximum values for efficiency, output power, and temperature were calculated. The results demonstrated that QVD multipliers provided increased output power, improved efficiency, and lower temperatures compared to lateral diodes in most circuits tested. The improved thermal management observed in QVDs suggests reduced cooling requirements, which could be advantageous in compact environments. The higher output power and efficiency suggest that these devices could be used for space-constrained applications with overall power consumption constraints, including cooling power included in the power budget.

A bulleted summary of contributions:

To the best of my knowledge, these are contributions to the field.

1. "Mesa first" process change for QVD membrane-based multiplier chips.
2. Optimized ohmic etch procedure for adhesive-bonded QVDs.
3. First, to my knowledge to realize heterogeneously integrated QVD multiplier membrane chips with side-coated vias, beam leads, and backside metallization.
4. SSTR – First, to my knowledge, the comparison of differential thermal resistance of SU8 versus Diffusion bond SOI
5. Diffusion bond GaAs QVD
    a. Fabrication process to realize diffusion-bonded GaAs QVDs.
    b. First DC and RF Characterization of high-frequency diffusion bonded QVDs.
    c. Ohmic etch procedure for Diffusion bond QVDs for (Ti/Pd/Au/Pd/Ti) stack
    d. First Thermoreflectance characterization of Diffusion Bonded GaAs QVD
    e. ICEPAK simulation setup for thin membrane QVD circuits comparing adhesive bond versus diffusion bond thermal resistance and transient cooling times.
6. First, to my knowledge, Maxwell DC Conduction simulation comparing Lateral and QVD.
7. First, to my knowledge, ICEPAK Simulation comparing Lateral and QVD thermal performance.

8. First, to my knowledge, direct QVD vs Lateral multiplier comparison.

Future Work

1. Future work should focus on process integration and device optimization. We have developed a process flow for integrating capacitors on the top side of Silicon adjacent to GaAs Schottky diodes. Collaborating with Louis Lukacyzk, who designed complex circuits using capacitors to isolate and individually bias diodes, will enable impedance tuning and non-AC-coupled voltage sampling.

2. We should explore the integration of capacitors beneath the diodes. This approach suits high-frequency circuits requiring closely spaced, independently biased diodes. The thermal simulations that I've shown can be used to optimize the dielectric material for thermal handling, so we aren't adding a layer of low thermal conductivity similar to the SU8-made diodes. These circuits could enable interesting multiplier and mixer circuits.

3. It's essential to explore the transition from a sacrificial resist method for defining the anode to a pillar process, which offers more precise anode geometry by eliminating topographical interference during the photolithography alignment during anode definition. The classical method, involving multiple resist applications over existing mesa and ohmic layers, often leads to alignment errors, potential oxide formation, and surface damage, which degrade

diode performance, including junction capacitance and subsequent operating frequency. A pillar process is expected to enhance alignment accuracy and improve yield by mitigating these issues.

4. Investigating higher thermal conductivity substrates, such as diamond or silicon carbide, to further optimize the thermal resistance and transient times would improve the QVD, especially when paired with the diffusion bonding process.

5. Investigating improved silicon substrates that offer higher resistivity is worth exploring, as Silicon is a robust substrate compatible with all of the UVA processes.

6. Comparing the Lateral and QVD mounted on a CPW transmission line will allow a novel on-wafer probe experiment, allowing researchers to determine the differences between RF-attributed resistances. This should be done by collaborating with Virginia Diodes and laying out a CPW circuit that can accommodate mounting single diodes.

7. This same circuit proposed in 6, could also be used to do a relative thermoreflectance measurement. Comparing the Lateral and QVD with transient thermoreflectance will be a novel direct comparison.

8. The most critical future work is to leverage the advancements in this technology to finish a development effort of a 500GHz frequency quadupler. The architecture of the quadrupler

is shown in Figure 1(a). The general architecture of the circuit is the same as what was seen with Alijabbari's, with the input and output frequencies scaled to 130 GHz and 520 GHz, respectively.

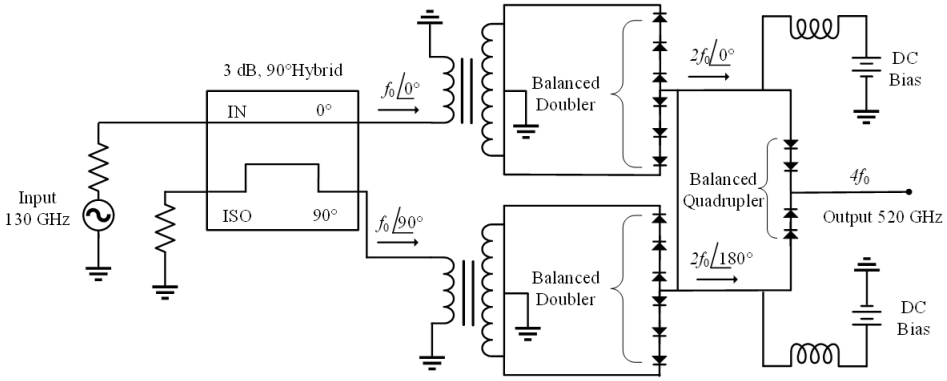


Figure 115 – Balanced Quadupler Diagram

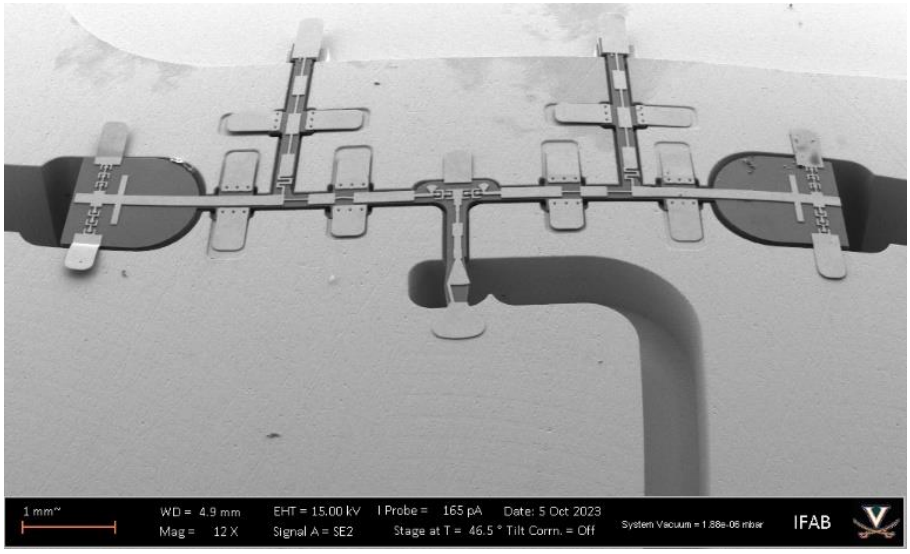


Figure 116 – SEM image of a prototype balanced quadupler chip.

An initial prototype, shown above, was made based on these process advancements (not the diffusion bond). However, problems with the design resulted in low output powers and efficiencies; these problems have been identified and should be subject to future work.

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