Development of Zero-bias Waveguide Photodiodes and O-band Waveguide Photodiodes on Silicon using Micro-transfer-printing

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This dissertation is dedicated

to my parents and girlfriend for their love and support

Contents

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Abstract

In recent years, as promising alternatives to all-electrical coaxial cable systems, optical radio-frequency (RF) which can provide benefits in large bandwidth, high-power handling capability, low loss, immunity to electromagnetic interference (EMI), and reduced size and weight, have been a widely investigated in tremendous number of microwaves applications in both defense and civilian areas such as radio-over-fiber, antenna remoting, and communications. As the optical-to-electrical converter in optical links, high performance photodiodes (PDs) are a key component in these applications. In this dissertation, three different high performance photodiodes are developed and demonstrated for applications in microwave photonics and communications.

First, for high-gain analog optical links and photoacoustic signal detection applications, a large-area modified uni-traveling-carrier (MUTC) photodiode with a high RF output power and high responsivity at 1550 nm is designed, fabricated and characterized. In this work, surface normal MUTC PDs with diameters of active areas from 100 μm to 600 μm were fabricated. A 100-μm-diameter photodiode achieved an RF output power of 23 dBm at 2 GHz and a dark current of 20 nA at -8 V. The 3-dB bandwidth and responsivity were 1.8 GHz and 0.63 A/W, respectively.

Furthermore, a waveguide photodetector with high speed and high responsivity at zero bias which has applications in radio over fiber links, dense photonic integrated circuits and PD arrays is developed and characterized. A bandwidth of 66 GHz under zero-bias operation and 102 GHz bandwidth at -1 V have been successfully demonstrated for a PD with an active area of 4×4 μm^2. Larger PDs (5×7 μm^2) have 56 GHz bandwidth and an internal responsivity of 0.48 A/W at 0 V. This performance is among the highest reported for all zero-bias photodiodes and, to the best of our knowledge, represents a new record for waveguide photodiodes.

In addition to PDs designed for 1550 nm, I also have designed, fabricated, and characterized high performance waveguide MUTC PDs at 1310 nm that are successfully integrated on a Si photonic platform by using micro-transfer-printing technology. To the best of our knowledge, this is the first waveguide MUTC photodiode transfer-printed on Si for 1310 nm. At -3 V, the waveguide photodiodes on Si achieved 54 GHz bandwidth, 0.29 A/W internal responsivity, and 5.7 dBm output power at 30 GHz measured from bar-level PDs. Based on its high-speed, high-power and compatibility with micro-transfer printing, these PDs can be used in Si photonic chips such as photonic integrated circuits for integrated microwave photonics.

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Chapter 1 Introduction

Ever since electromagnetic waves were proved by Heinrich Hertz in late 1880s and coaxial cables, waveguides, and antennas were invented to transmit radio frequency (from 3 kHz to 300 GHz) signals, there have been a tremendous number of applications of microwaves such as radio broadcasting, radar, and wireless communications. With the demand for high bandwidth in applications such as satellite communications, the carrier frequency has already moved into microwaves and mm-Waves regimes which are electromagnetic waves with frequency ranging from 300 MHz to 300 GHz. However, in wired connections, loss in coaxial cables increases rapidly with transmitted signal frequency which is fatal for long-haul transmission.

In 1965, Charles Kuen Kao was the first to promote the idea that the attenuation in optical fibers could be reduced to make fibers a practical communication medium [1]. With the development of optical fiber, fiber optic links have become a powerful alternative to electrical coaxial cable systems for broad applications areas as they can provide ultra-low loss [2]. This has enabled massive amounts of information that can be transmitted over a long distance with minimal loss.

1.1 Analog Optic Link

Microwave photonics describes novel optoelectronic systems based on the interaction between light and microwaves, which was first introduced in 1991 [3] [4]. The interaction between an optical signal and a microwave signal is also called analog photonics. An analog optic link is the most basic transmission unit in microwave photonics to transmit microwave signals through fibers. As shown in Figure 1-1, an analog optic link typically consists of a transmitter (i.e. lasers) as optical source, a modulator, an optical fiber as transmission medium and a receiver (i.e. photodiodes). First, the electrical RF signal is modulated onto an optical carrier by an E/O modulator. After the transmission through optical components such as optical fiber, optical amplifier, filter and attenuator, the photodiode is used to convert the optical signal back to electrical RF signal for further processing. Besides low propagation loss in fiber optical transmission, analog optic links can also provide benefits in large bandwidth, immunity to electromagnetic interference, and small size and weight [5-8]. With these tremendous advantages over traditional electrical coaxial-cable-based links, analog optic links have been widely investigated in many microwave applications such as phased array radars [9], antenna remoting [10], radio-over-fiber [11], and analog-to-digital converters [12].

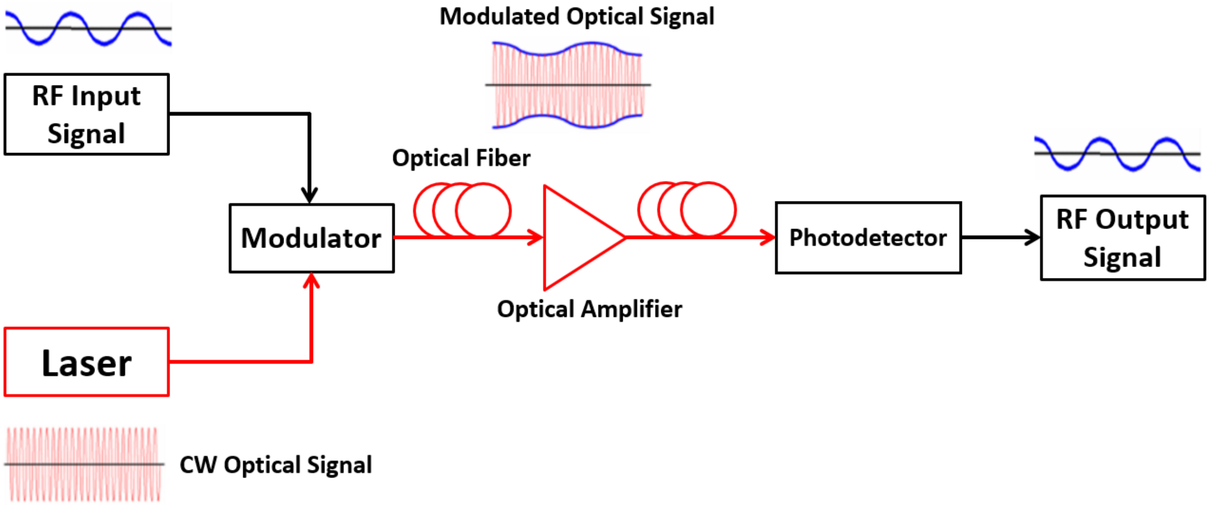


Figure 1-1. Schematic of a typical analog optic link

In general, it is beneficial to reduce the loss of a transmission link. Even if the loss in the optical fiber is very low, the RF loss of an analog optical link relies heavily on the O/E and E/O conversion efficiencies at the transmitter and receiver ends and the available optical power. One key component at the receive side is the photodiode (PD) that is required to have high O/E conversion efficiency while maintaining high. On the other hand, larger information capacities are required in future optical communication, which will lead to more power consumption in multi-channel integrated photonic systems. In addition to high O/E conversion efficiency, the energy consumption of photodiodes can also be important for dense high-performance analog optic links.

1.2 Silicon Photonics

Silicon (Si) photonics is a silicon-based material platform from which photonic systems such as photonic integrated circuits (PICs) can be made. Ever since the first studies of waveguides in silicon-on-insulator (SOI) wafer structures by Soref in 1985 [13], silicon photonics is now widely accepted as a key technology in next-generation communications systems and data interconnects. The practicality and promise for Si photonics advanced with the realization of novel silicon-based heterogeneous photonic devices, such as lasers [14], electro-absorption modulators [15], Mach–Zehnder (MZ) modulators [16], and photodiodes [17].

The most well-known motivation for Si photonics is its potential for bringing the large wafer size, volume throughput and the low cost of creating photonics for mass-market applications by exploiting the mighty IC industry [18]. In addition, at telecommunication wavelengths (around 1550 nm), due to the high index contrast between silicon (n=3.45) and SiO_2 (n=1.45), SOI becomes an ideal platform for creating planar waveguide circuits with high optical confinement which makes it possible to scale photonic devices to the hundreds of nanometer level for compatibility with IC processing [19]. Besides these two motivations, for photonics devices, silicon has some excellent material properties such as high thermal conductivity and high third-order optical nonlinearities.

However, silicon is a rather poor optical absorber at commercial telecommunication wavelength (1550 nm and 1310 nm) because of its large bandgap of 1.12 eV (1100 nm). In addition to the indirect bandgap of silicon, it remains a challenge to achieve active photonic devices such as photodiodes and lasers. To push the absorption of Si-based photodiodes up to 1550 nm, two-photon absorption and the introduction of lattice damage through selective ion implantation have been used [20]. However, high reverse bias is needed for these photodiodes and the responsivity is very small. Recently, germanium (Ge) photodiodes have been developed [21] [22] [23] due to their strong absorption in the near infrared wavelength range (up to 1.55 μm) and low-cost and high-throughput integration scheme which is compatible with the CMOS fabrication processes. One recent Ge photodiode has achieved a bandwidth higher than 70 GHz, a responsivity close to 1 A/W, and a dark current close to 1 μA [24]. However, the integration of Ge-on-Si remains a significant challenge due to the large lattice mismatch (4.2%) between Si and Ge. Besides Ge, III-V based materials are also be considered due to their extraordinary performance. The hybrid integration of III-V materials on Si enables high-power, high-speed and high-efficiency photodiodes on Si platforms. However, integration technologies for III-V materials on Si tend to be more complex and less cost-effective. Thus, it is essential to develop a simple and low-cost integration technology for III-V based materials and devices on Si to improve and enhance the quality of photonic devices on the Si platform such as photodiodes, modulators, and lasers.

1.3 Dissertation Organization

This work focuses on demonstration of large-area high-power photodiodes, high-speed zero-bias waveguide photodiodes and O-band high-speed waveguide photodiodes on a SiN/Si platform using micro-transfer-printing integration. In my Ph.D work experimental devices have achieved the following performance:

- Large-area high-power MUTC photodiodes with output RF powers of 23 dBm at 2 GHz, 20 nA dark current at -8 V and responsivity of 0.63 A/W.

- First demonstration of high-speed waveguide zero-bias type-II MUTC photodiodes.
- High-speed waveguide zero-bias type-II MUTC photodiodes with record high bandwidth (66 GHz at 0 V and 102 GHz at -1 V) and high internal responsivity of 0.48 A/W.
- High-speed waveguide zero-bias type-II MUTC photodiodes with small dependence on bias.
- First waveguide MUTC photodiodes transfer printed on SiN/Si platform for 1310 nm demonstrated.
- Waveguide MUTC photodiodes transfer printed on SiN/Si platform with record high bandwidth (54 GHz at -3 V) and high internal responsivity of 0.29 A/W at 1310 nm.
- Waveguide MUTC photodiodes with record high 5.7 dBm RF output power at 30 GHz at 1310 nm.

Chapter 2 introduces the high-power and high-speed photodiodes and integration technologies for Si photonics; Chapter 3 introduces the fundamentals of photodiodes and the fabrication processes. Chapter 4 describes the realization of large-area high-power MUTC photodiode; Chapter 5 demonstrates high-speed waveguide zero-bias type-II MUTC photodiodes; Chapter 6 introduces the micro-transfer-printing technology and presents waveguide MUTC photodiodes transfer printed on SiN/Si platform for 1310 nm; Chapter 7 provides the summary and future work.

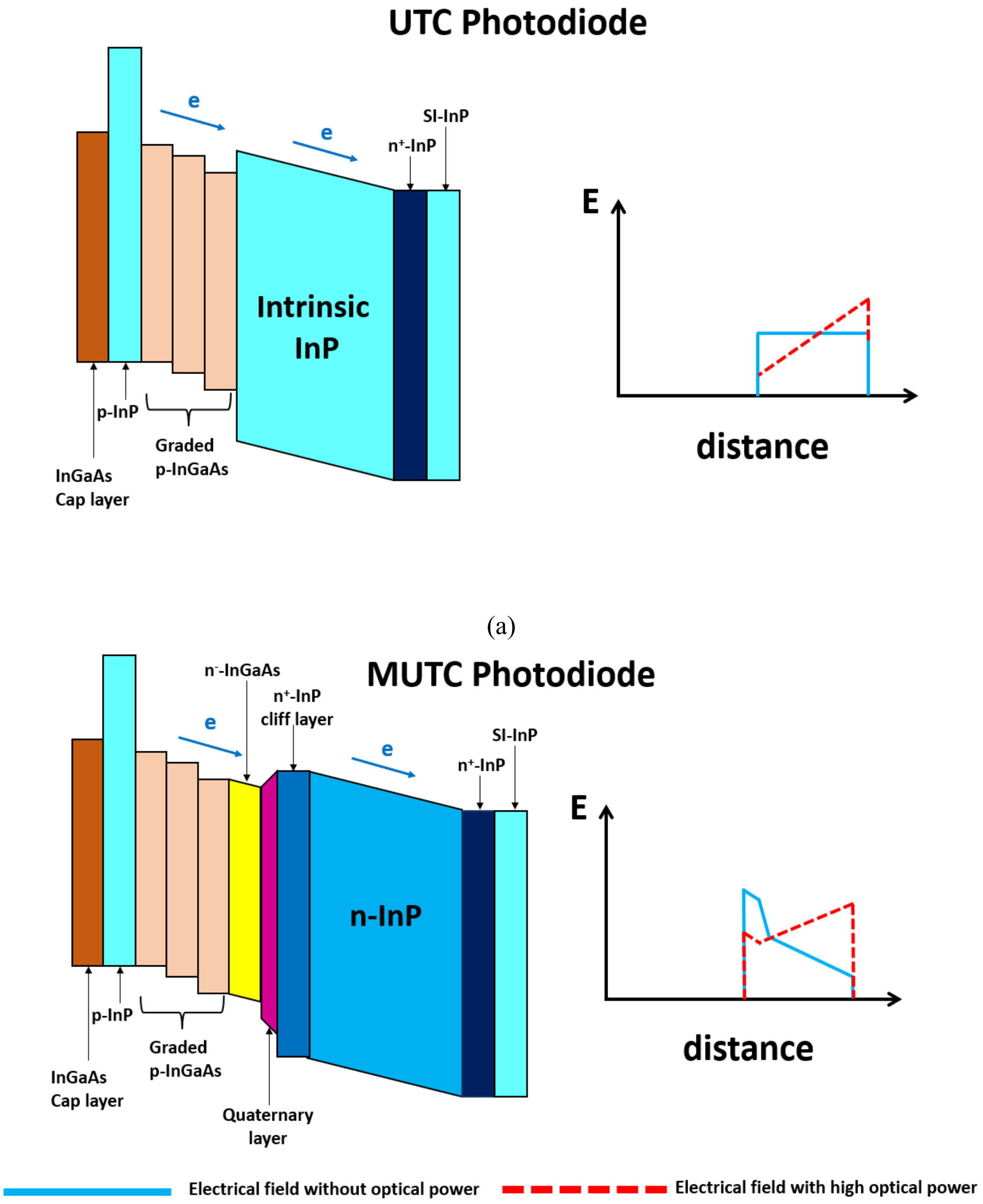
Chapter 2 Zero-Bias Photodiodes and High-speed Photodiodes Integrated on Si Platform

2.1 Introduction

As mentioned in Chapter 1, one figure of merit for photodiodes is energy consumption, which mainly comes from the reverse bias voltage on the photodiode. Thus if a photodiode can work without external bias voltage (zero-bias), no extra electrical energy would be dissipated at all and the dark current would be zero. Also, since there is no bulky bias circuit needed, system complexity in dense photonic integrated circuits can be relaxed and electrical cross-talk reduced. In addition, thermal stress due to Joule heating can be low and the device footprint could be very small. In this chapter, first, structures of MUTC zero-bias photodiode, and some previous work about zero-bias photodiodes are discussed. Then, for Si photonics applications, some work about high performance photodiodes integrated on Si are discussed. Finally, techniques used for heterogeneous integration on Si are introduced.

2.2 MUTC and Zero-bias Photodiodes

Previously, several photodiode structures have been proposed and demonstrated to achieve high speed and high power operation, including conventional PIN photodiodes, the dual depletion region (DDR) photodiode [25], the partially depleted absorber (PDA) photodiode [26], and uni-traveling carrier (UTC) photodiode that was first demonstrated by T. Ishibashi et al. [27]. Figure

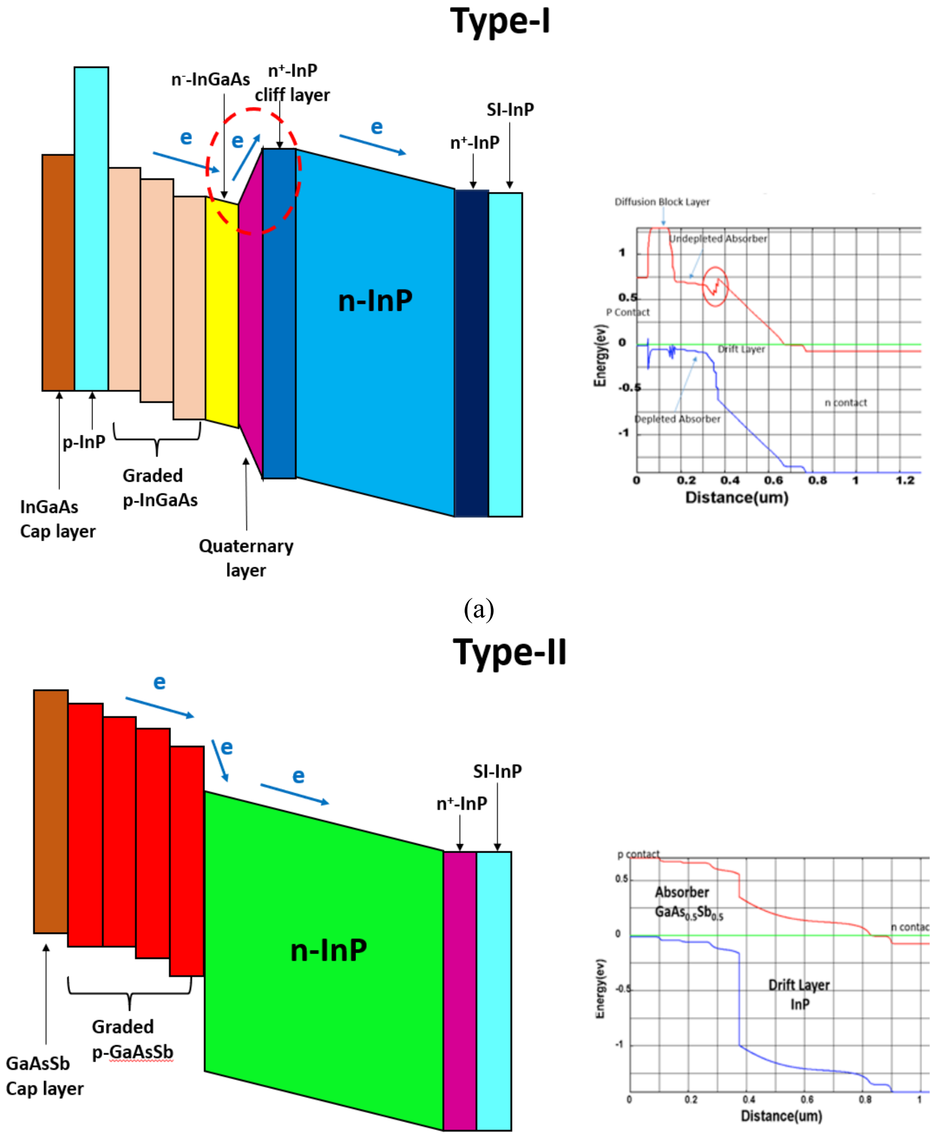


(a)

(b)

Figure 2-1. Band diagram and electric field distribution of UTC (a) and MUTC (b) photodiodes

2-1 (a) shows the energy band diagram and electric field distribution of a UTC photodiode which consists of a p-doped InGaAs undepleted absorption layer and a transparent InP drift layer. Since only electrons traverse the depletion region, the bandwidth of UTC photodiodes can be much higher than PIN photodiodes in which holes with low velocity also contribute to the frequency response. Furthermore, in a UTC photodiode, a wide band materials used as the drift region, which lowers the dark current and makes the photodiode less susceptible to thermal run away. However, the space charge effect remains at high optical power levels owing to single carrier injection, which induces the electric field collapse at the edge of the depleted region and limits the output RF power. Another issue for the UTC photodiode is that at high input optical power levels the injection of electrons from the undepleted absorption layer into the collector region is impeded by the energy barrier between the narrow bandgap material (InGaAs) and the wide bandgap material (InP). To solve these issues and improve the performance of UTC PDs, several modifications of the epitaxial-layer structure have been made on UTC PDs, called modified UTC (MUTC) PDs. Figure 2-1 (b) shows the band diagram and electric field distribution of MUTC PDs. Compared with UTC PDs, first, the partially depleted absorption layer accomplished by adding a lightly n-doped layer to the absorption region improves the responsivity without sacrificing bandwidth [28]. And it also prevents field collapse at the heterojunction interfaces and aids injection from the absorber to the drift layer at high current levels. Second, a thin "cliff layer" [29] as charge layer was added between the depleted InGaAs layer and the InP collector layer to enhance the electric field in the depleted InGaAs absorption layer to maintain a high electric field across the heterojunction interfaces. Third, the InP collector layer is slightly n-doped to pre-distort the electric filed so that a flat field profile can be achieved at high photocurrent level as illustrated in Figure 2-1 (b), which increase the RF output power [30]. Finally, quaternary InGaAsP layers are inserted at the heterojunction interface to smoothen the bandgap discontinuity which can further mitigate the charge accumulation. Recently, a very high-power MUTC photodiode flip-chip bonded on diamond with 1.8 W output power at 10 GHz under -14 V [31] and a high-speed evanescently coupled waveguide integrated



(a)

(b)

Figure 2-2 Schematic and simulated band diagrams of type-I (a) and type-II (b) photodiodes.

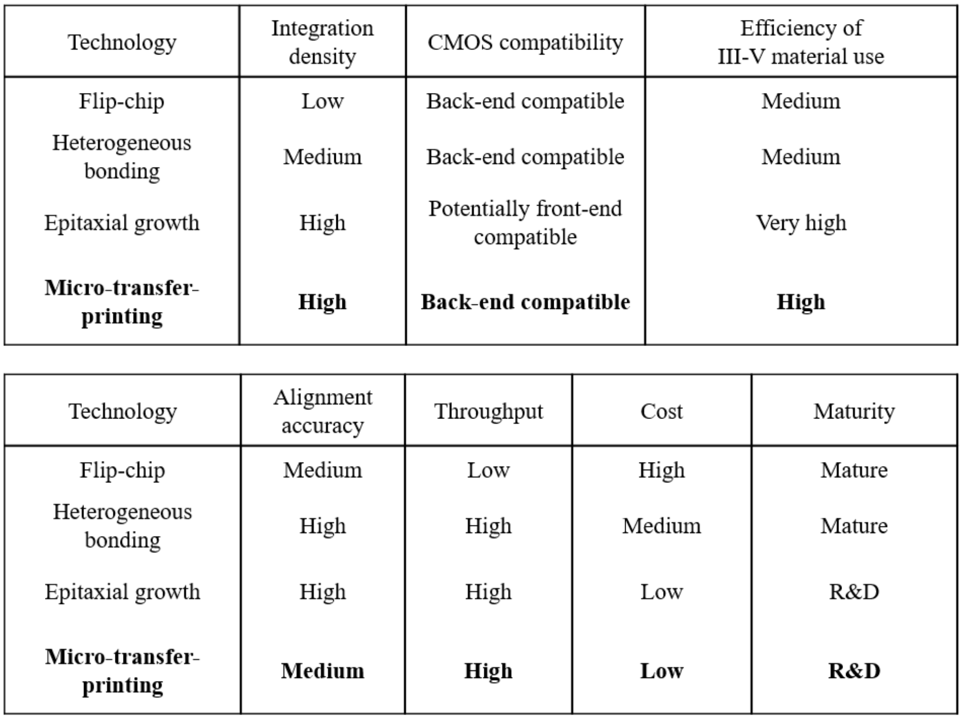
MUTC photodiode with 105 GHz bandwidth at -3 V [32] have been reported.

However, at low or zero bias, a bandwidth limitation often arises from discontinuities in the band diagram which can impede carrier transport in these heterojunction (type-I) MUTC PDs [33], as shown in Figure 2-2. To avoid the potential barrier in the conduction band between the absorber and the wide-bandgap drift layer in an UTC PD at low bias, a staggered band lineup (type-II) is beneficial [34]. Such a type-II GaAsSb/InP photodiode with 170 GHz bandwidth at zero bias was demonstrated by Jhih-Min, et al., in 2017 [35]. Besides this work, there are also some other zero-bias photodiodes have been demonstrated in recent years such as zero-bias Ge PIN photodiode with 27 GHz bandwidth at 0 V [36] and surface normal UTC photodiode with 110 GHz bandwidth at 0 V [37].

2.3 Photodiodes on Si and Integration Techniques

As mentioned in Chapter 1, silicon photonics exploits the high-volume manufacturing capability of the CMOS microelectronics industry emerging as a promising platform for building complex and powerful PICs. Compared with several mainstream photonic integration platforms including silica-on-silicon, InP, Si has the obvious advantages of CMOS compatibility and high refractive index contrast, which allows high-volume production of compact photonic circuits with strong light-matter interaction, resulting in low cost, low power consumption and high bandwidth devices [38]. High-performance photodiodes are key components in PICs for conversion of microwave and mm-Wave signals and high-speed communication. Photodiodes that can be heterogeneously integrated on a Si platform with high speed and high responsivity are particularly beneficial since they can be combined with optical components based on other materials such as lasers and modulators to form multi-functions photonic systems in PICs. With the intention to integrate high-performance photodiodes on Si for PICs, several integration approaches such as direct III-V growth [39], flip-chip bonding [40] and die-to-wafer bonding [41] are being studied. A comparison of the pros and cons of these aforementioned approaches is summarized in Table I [73]. The heteroepitaxial growth method is still at an early stage with much work to be done on the integration of these process modules in the silicon photonics process flow [42]. As for flip-chip bonding technology, the low integration density makes it difficult to scale up and reduce the cost of resulting PICs. In heterogeneous bonding technology, wafer bonding is a process that is completed before the definition of the III-V structure and back-end metallization. In this case, the back-end process flow has to be modified to accommodate the III-V devices and the III-V devices can only be tested after they have been integrated on the silicon photonic wafer which can affect the compound yield [43]. In addition, integrating different material stacks can be challenging if high density is required. Micro-transfer-printing is a novel pick-and-place integration technology whereby devices on the III-V source wafer can be selectively picked using a polydimethylsiloxane stamp and printed on a silicon photonics target wafer with high alignment accuracy [44]. By using this approach, the efficiency of the use of source materials can be significantly improved and different materials/devices can be intimately integrated on a common substrate.

Table I A comparison of different III-V-on-Si wafer-level heterogeneous integration approaches [73]



Technology	Integration density	CMOS compatibility	Efficiency of III-V material use
Flip-chip	Low	Back-end compatible	Medium
Heterogeneous bonding	Medium	Back-end compatible	Medium
Epitaxial growth	High	Potentially front-end compatible	Very high
Micro-transfer-printing	**High**	**Back-end compatible**	**High**

Technology	Alignment accuracy	Throughput	Cost	Maturity
Flip-chip	Medium	Low	High	Mature
Heterogeneous bonding	High	High	Medium	Mature
Epitaxial growth	High	High	Low	R&D
Micro-transfer-printing	**Medium**	**High**	**Low**	**R&D**

Chapter 3 Fundamentals of Photodiodes

3.1 Introduction

This chapter describes the fabrication process of waveguide photodiodes and the photodiode characterization techniques. First, the fabrication of waveguide photodiodes is introduced with the details of the processing steps. Then, electrical and optical measurement techniques are discussed for device characterization, including current-voltage, capacitance-voltage, responsivity, S-parameter, bandwidth, and saturation measurements.

3.2 Fabrication of Waveguide Photodiodes

Figure 3-1 shows a schematic, a top-view photograph, cross sectional view, and a scanning electron microscope (SEM) view of the waveguide photodiode. The photodiode has a double mesa structure with metal deposited on top of each mesa layer, and an air-bridge connecting the p- and n-metal to the probe pad on the semi-insulating substrate. The sidewall of the mesa is passivated with SiO_2 to reduce surface leakage current. The critical fabrication steps for making the above features include p-metallization, p-mesa etch, n-mesa etch, n-metallization, waveguide etch, p-contact open, seed layer and electroplating, and cleaving.

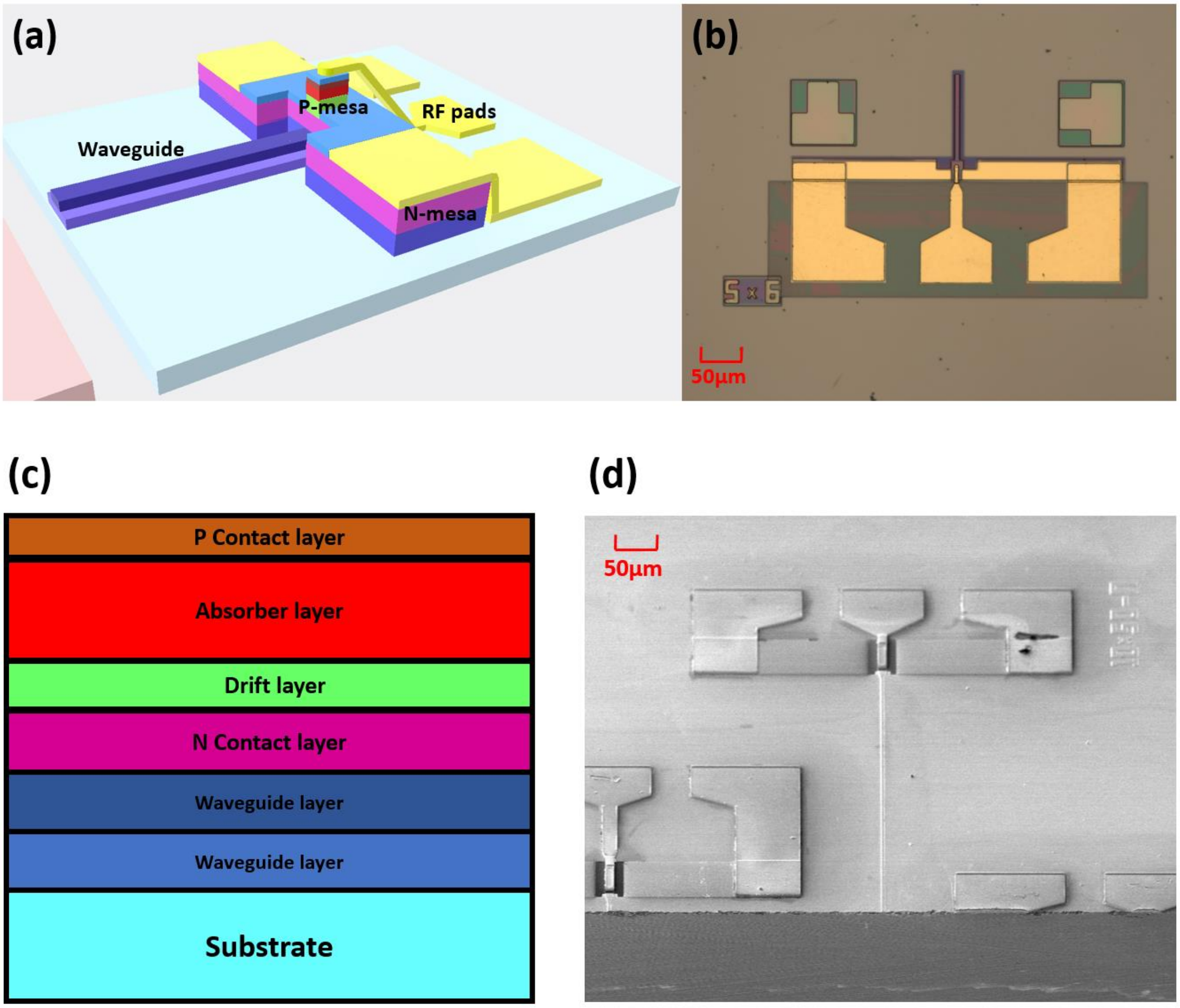


Figure 3-1. (a) Schematic, (b) top-view photograph, (c) cross sectional view, and (d) SEM view of the waveguide photodiode after cleaving.

3.2.1 P-metallization

P-metallization means metal deposition on p-contact layer to form Ohmic contacts, which is critical since a major part of the device series resistance comes from the p-type contact. For our

MUTC epitaxial design, a thin layer of p-type InGaAs contact layer is always preferable to achieve a low series resistance. Metal layer stacks of Ti/Pt/Au/Ti (20/30/50/30 nm) on the thin p-type InGaAs surface provide low contact resistance and good adhesion. The titanium (Ti) is used for adhesion to the InGaAs top layer. The platinum prevents gold migration into the semiconductor, which can form gold spikes that short device [45]. The Au provides good electrical conductance and the base for gold-up-plating. After cleaning the original wafer with IPA+Acetone+O_2 plasma, the metal stack is deposited using E-beam evaporation. After loading into the E-beam chamber, the evaporation is carried out in vacuum level below ~1e-7 Torr. Then, four metal films (Ti/Pt/Au/Ti) are deposited in sequence to avoid defects or contamination at the metal interfaces.

3.2.2 P-mesa Etch

The mesa etch is carried out in two steps: p-mesa and n-mesa etch. The p-mesa etch defines the active region which can absorb light and generate carriers. This etch is terminated at the n-layer on which the n-type contact is formed. To avoid isotropic etch and lateral undercutting, a dry etch technique is used instead of wet etch. To this end, a SiO_2 hard mask instead of photoresist (PR) is used to transfer the pattern and avoid side wall damage during the dry etch which may lead to higher dark current. After p-metallization, a SiO_2 with 600 nm (the thickness of SiO_2 depends on the thickness of p-mesa and dry etch rate) is deposited by plasma-enhanced chemical vapor deposition (PECVD). Next, to form the mesa pattern using lithography, AZ 5214 photoresist is spun on the wafers and pre-baked at 100 ºC for 2 min before exposure. We use a SUSS MA/BA6 mask aligner for exposure. Then the wafer is developed in AZ 300 MIF developer. After lithography, part of the SiO_2 hard mask is removed by dry etching with SF_6 using Oxford inductively coupled plasma (ICP) reactive ion etch (RIE) machine. Finally, the p-mesa is dry etched by Oxford with Cl_2:N_2 gas mixture. Typically a dummy SiO_2 wafer with the same thickness as the SiO_2 on device wafer is prepared to monitor the etch rate of the hard mask during mesa etch.

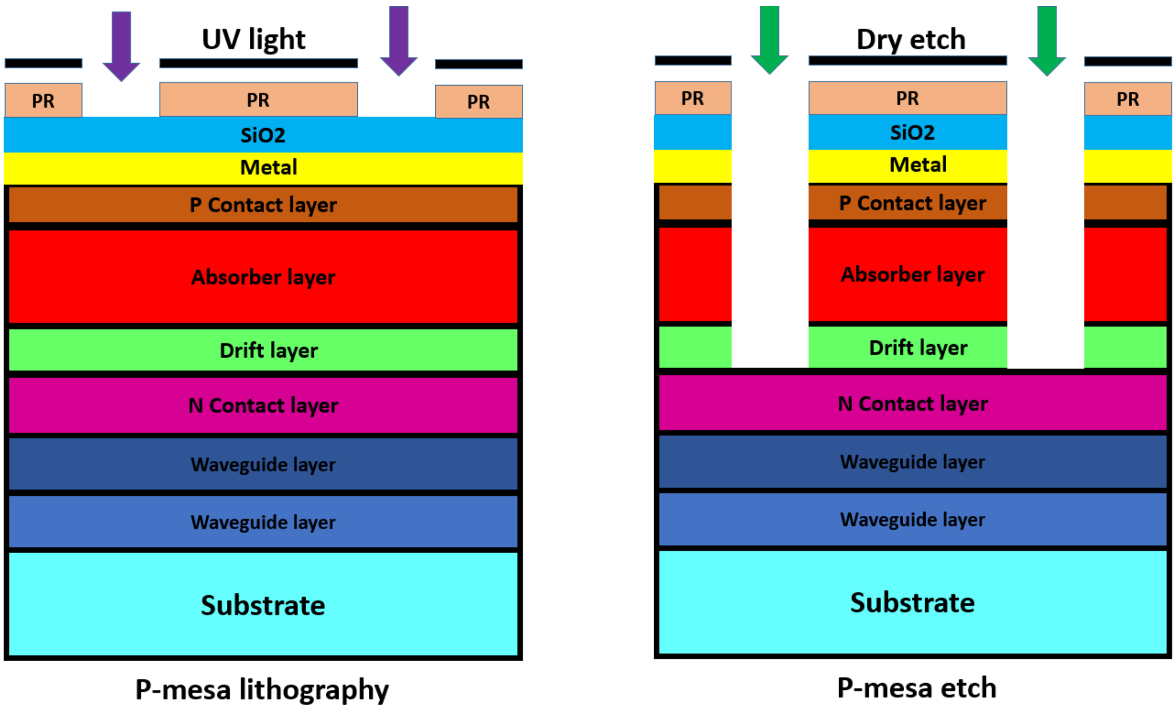


Figure 3-2 Schematic of cross section view of p-mesa etch

The thickness of the SiO_2 is measured with ellipsometry. The step height of the mesa plus oxide can be determined by a profilometer. With step height of the mesa plus mesa and remaining oxide on the mesa, the thickness of etched away III-V material can be precisely measured. Figure 3-2 shows a schematic cross section of the photodiode after mesa lithography, SiO_2 removal, and p-mesa etch.

3.2.3 N-mesa Etch

Following the p-mesa etch, the n-mesa is etch, which provides isolation between devices and reduces capacitance by etching down to the semi-insulating waveguide layer. This also greatly reduces the dark current. Same with the p-mesa etch steps, the n-mesa area is defined with lithography and a SiO_2 hard etch mask is used. It should be mentioned that the SiO_2 hard mask for n-mesa etch also serves as the passivation layer to protect the side walls of the p-mesa and reduce the surface leakage current and preventing device degradation. As shown in Figure 3-3, standard lithography with the n-mesa pattern is followed by a hard mask etch and III-V etch into the semi-insulating substrate.

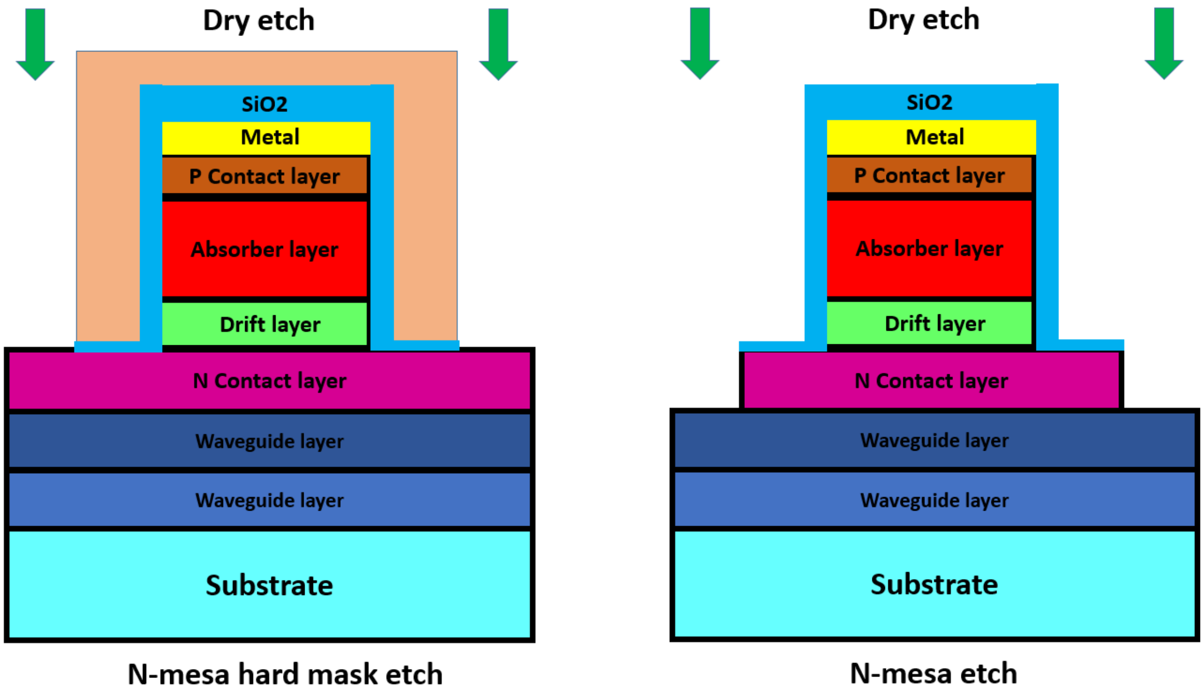


Figure 3-3 Schematic of cross section view of n-mesa etch.

3.2.4 Waveguide etch

For high efficiency light coupling, the designed optical waveguide includes a rib waveguide and a slab waveguide as shown in Fig 3-1(a). To form the rib and slab waveguide structure, same as p-mesa and n-mesa etch steps, ICP RIE was used to dry etch the double mesa structure with the SiO_2 hard mask layer. It should be mentioned that the RIE ICP power is reduced from 300W to 200W which results in a lower III-V etch rate to control the small rib and slab thickness more precisely. Fig 3-4 shows a cross section view of the photodiode after waveguide etch in two different directions.

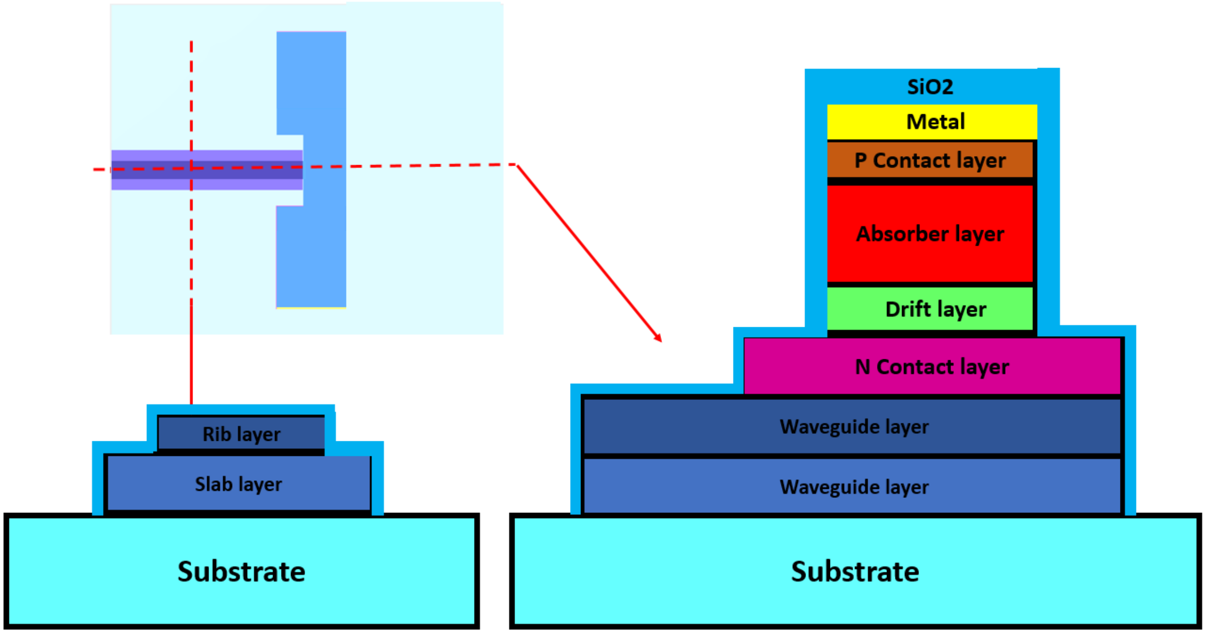


Figure 3-4 Schematic of cross section view after waveguide etch.

3.2.5 N-metallization

For the n-metal formation, the contact metal stack consists of AuGe (30 nm)/ Ni (20 nm)/Au (100 nm), where the function of the AuGe is to provide good adhesion to n-type InP, Ni is to prevent Au penetration. Also, AuGe alloy with lower barrier height can be formed and Ge settles in the indium vacancies as a donor during the rapid annealing, which leads to low resistance [46]. First the photoresist is coated on the wafer. After lithography, the photoresist on part of n-contact layer area is removed for metal deposition. Then BOE is used to remove the SiO_2 on part of n-contact layer area for metal contact. Similar to P-metal stack, n metal layer is deposited by E-beam evaporation on the whole wafer. Finally, a lift-off process is done to remove the unwanted metal together with photoresist. Fig 3-5 shows a cross section view of the photodiode before and after n-metal lift-off process.

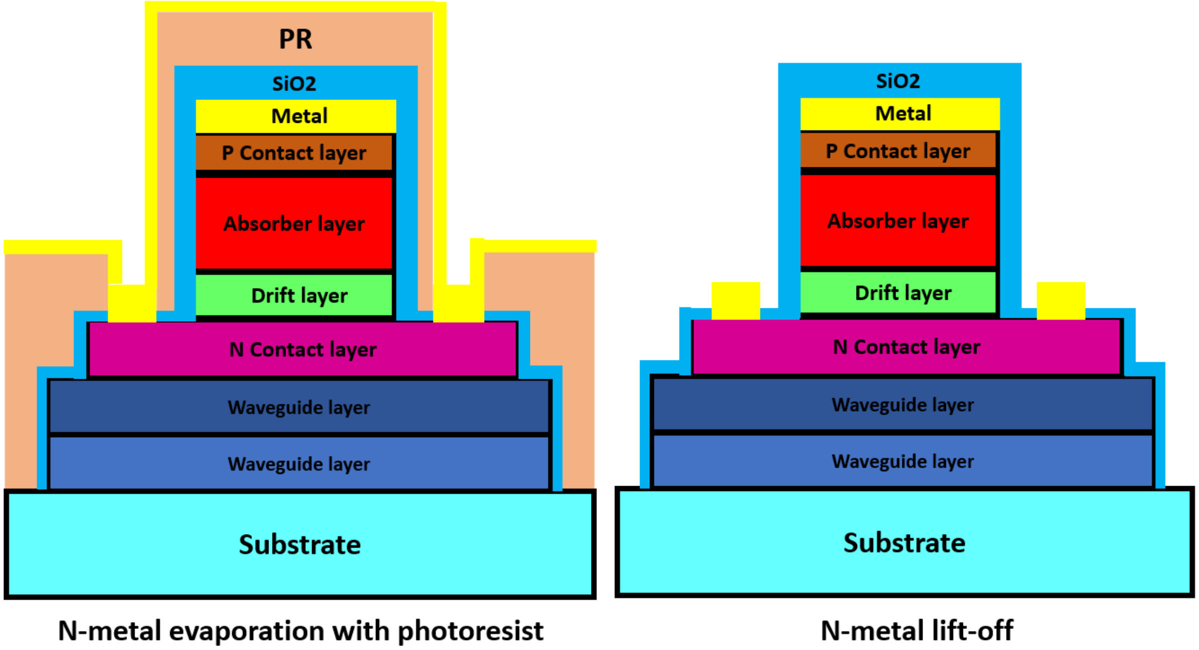


Figure 3-5 Schematic of cross section view before and after n-metal lift-off.

3.2.6 P-contact Open

The most critical step is opening the p-contact following the n-metal deposition. The SiO_2 layer on the top of p-mesa needs to be first removed to expose the metal on p-contact layer for future connection to RF pads. Same with p-mesa etch step, lithography and dry etch are used to remove the SiO_2 layer on the top of p-mesa. It should be mentioned that lithography is critical because the contact opening is small for high-speed devices. If the sidewall of the p-mesa is exposed, the protective SiO_2 layer on the sidewall will be etched and the metal deposited in the following step will short the device. After etching away the SiO_2 layer on the top of p-mesa by ICP RIE, the device is ready for preliminary current-voltage measurements. Fig 3-6 shows a cross section view of the p-contact open steps.

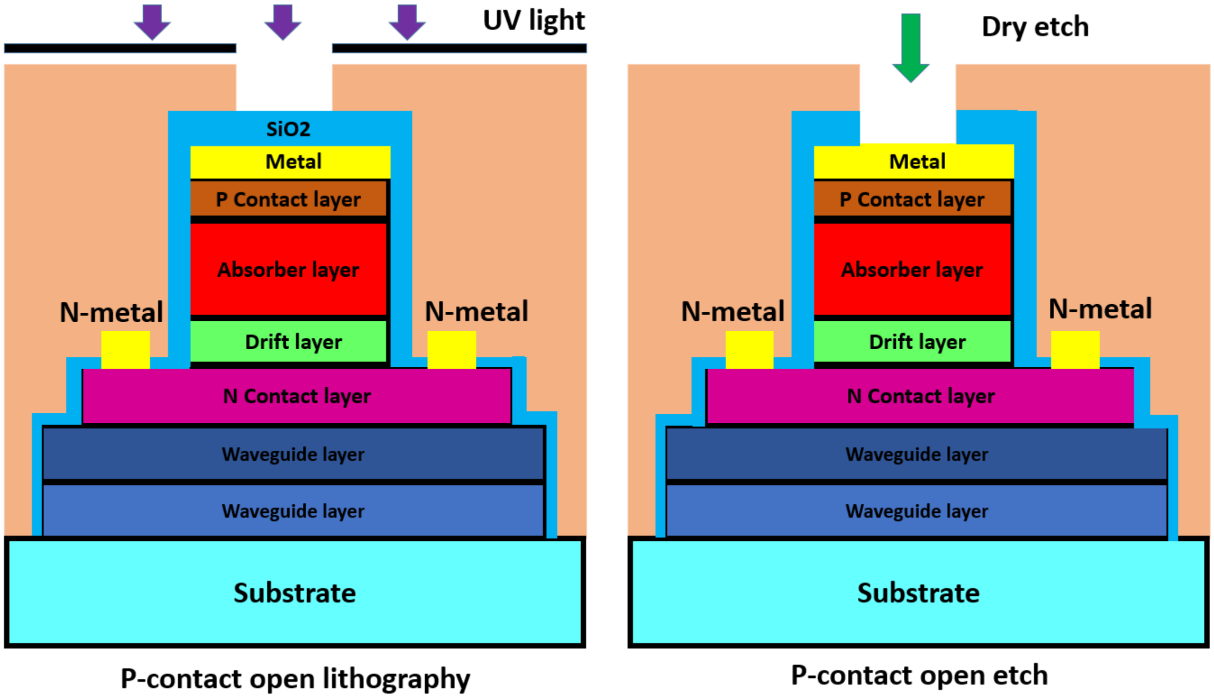
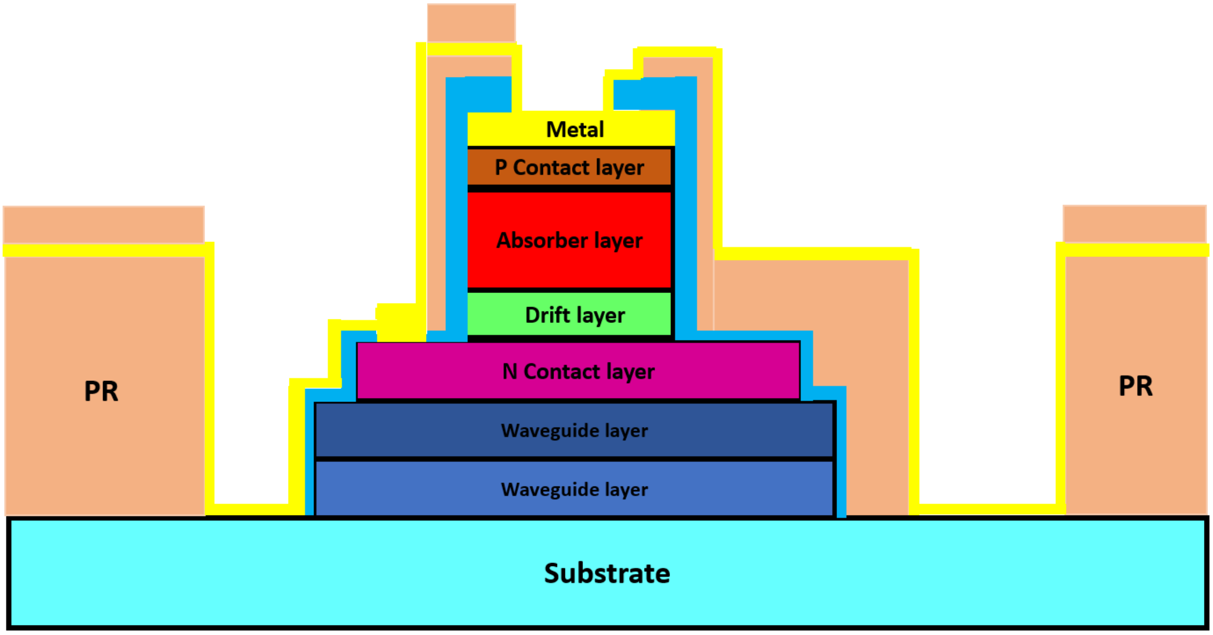


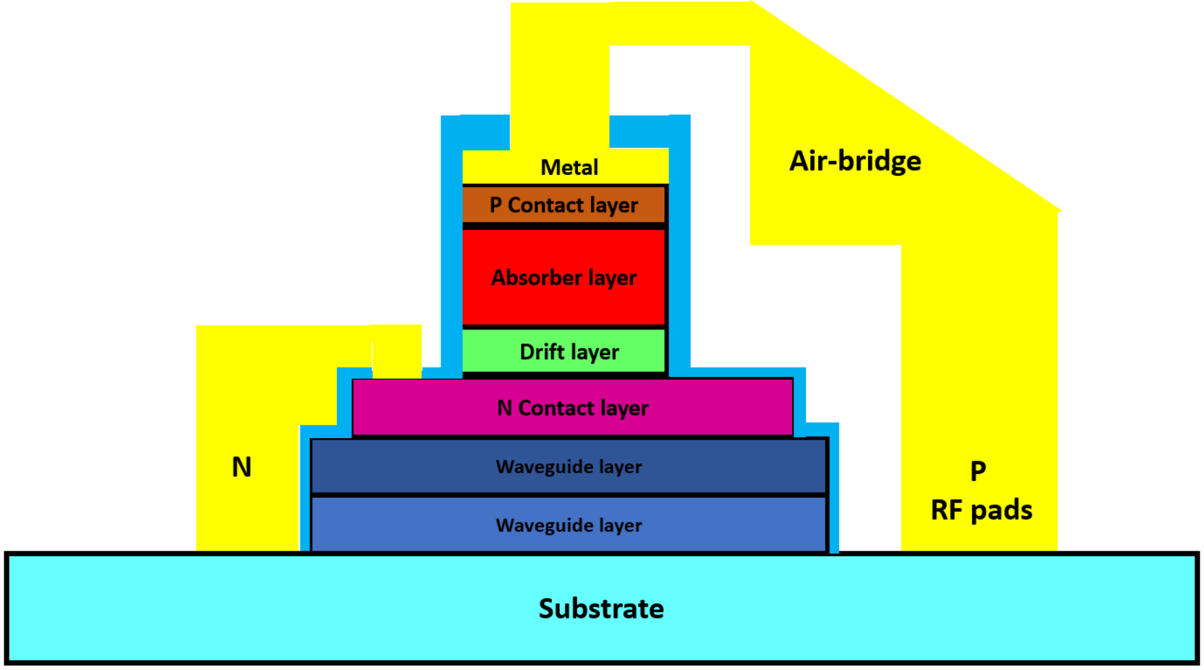
Figure 3-6. Schematic cross section view of p-contact open steps.

3.2.7 Seed Layer and Electroplating

After exposing the metal on the p-contact layer, a metal bridge structure on top of an air gap (called air-bridge) is used to connect the p-mesa and RF pads as shown in Figure 3-1 (a). Figure 3-7 shows the schematic cross section view of steps about realizing the air-bridge. Two lithography steps are processed in sequence. The first lithography creates thin photoresist on top of the p-metal and the regions of p-contact and RF pads are open. Then, Ti/Au (20/80 nm) is evaporated as a seed layer. The second lithography is done on top of the first photoresist to open the same region as first lithography plus the air-bridge regions. Next, electroplating is performed with plated ~ 2 µm gold in the open area to form the RF pads and air-bridge. Then the top layer photoresist is removed with O_2 plasma and the seed layer is etched with gold etchant. Finally, after lift-off process in ultrasonic cleaner, all photoresist together with unwanted metal are removed to complete the whole photodiode fabrication process.



Two lithography and one seed layer deposition



Electroplating and lift off

Figure 3-7. Schematic cross section view of seed layer and electroplating steps.

3.2.8 Cleaving

After all the fabrication process introduced above, and before testing the waveguide photodiode, the facet surface of the waveguide needs to be exposed for light input coupling. Compared with dicing, cleaving is a much better choice to produce a flat and defect-free surface. The clean and flat surface can obviously improve the light coupling efficiency and the responsivity of the waveguide photodiode. A microscope, vacuum system, and a dicing tool named Lattice Ax 120 from LatticeGear Corporation (shown in Figure 3-8) are used for cleaving process. The microscope is used for the inspection of wafer and vacuum system is used for securing the wafer on the cleaving stage. The Ax 120 consists of a diamond indenter with polished face for accurate

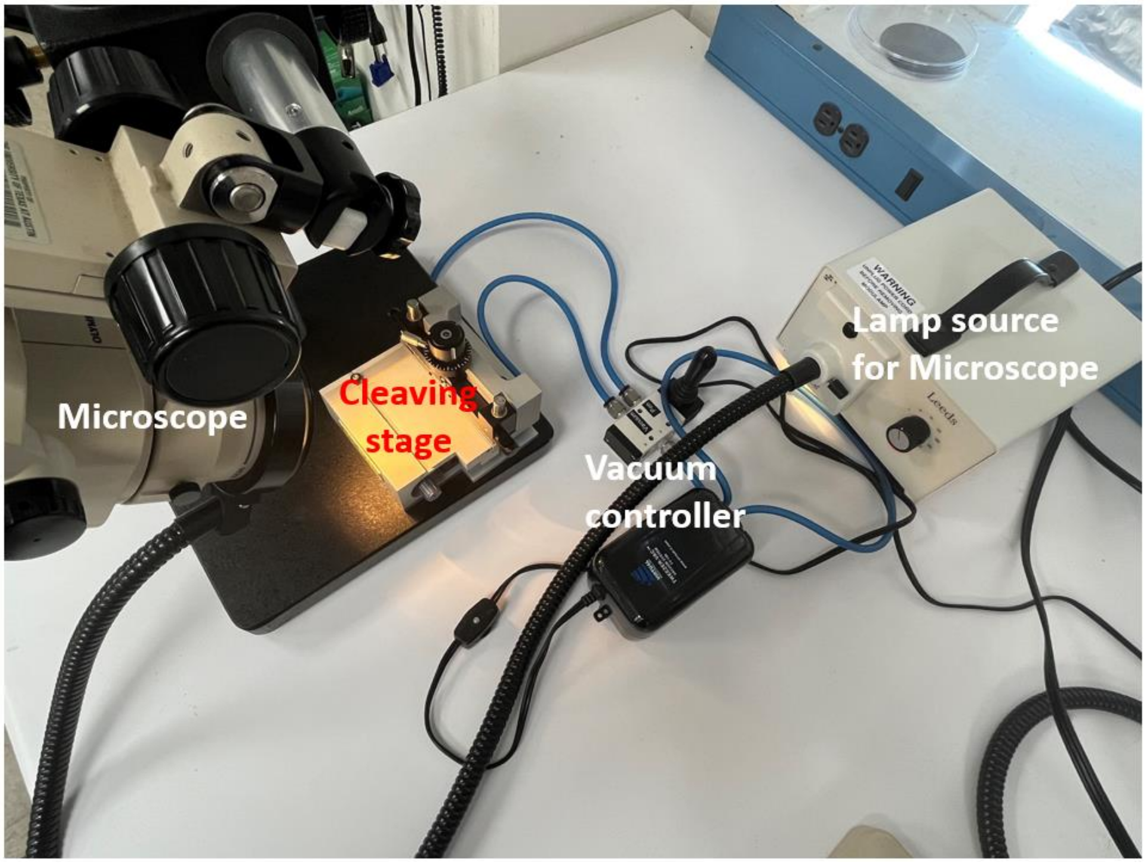


Figure 3-8. Cleaving system.

positioning, position control of indenter with 5 μm step size, cleaving bar with ruled marking and handle, and a sample guide with locking knob. The first step of cleaving is to put the wafer onto the stage and secure it with vacuum. Next, the diamond indenter is directed by the control knob to indent at a desired location on the wafer with a little force. Then, the cleaving bar is lifted up and the wafer is extended to sit on top of a metal rod underneath the cleaving bar. Finally, the control knob was turned to push the cleaving bar down to the wafer and the two protruded rubber sections on the cleaving bar press and cleave the wafer. The size of the smallest chip the Ax 120 can cleave is 1.2×1.2 cm^2.

3.3 Characterization of Photodiodes

3.3.1 Current-Voltage and Capacitance

Figure 3-9 shows a typical current-voltage (I-V) curve of a photodiode, which is one of the important photodiode's characteristics. Different modes can be achieved in terms of which quadrant a diode operates in. The modes include the laser mode, the photodiode mode, the avalanche mode and the photovoltaic mode. Our photodiode operates under reverse bias and the third quadrant of the IV curve is the region we are interested in. I_d, I_{ph} and I_L present the dark current, photocurrent and total current respectively. Dark current is the current in the photodiode when there is no incident light. This can be one of the main sources of noise in the photodiode. Low dark current is always preferable in photodiodes which means low noise. Dark current increases with temperature. Another source of dark current comes from the surface leakage. Photocurrent presents the current when photodiode is illuminated by light. It should be mentioned that photodiodes can be operated without any voltage bias (zero-bias), which will be discussed in chapter 5 with more details. V_{oc} and V_{bd} present the open voltage in photovoltaic devices (also called solar cell) and breakdown voltage. Breakdown voltage is the largest reverse voltage that can be applied to the photodiode before there is an exponential increase in leakage current or dark current. Photodiodes in my work are operated below this maximum applied reverse bias.

Besides I-V curves, capacitance is also a very critical parameter in the photodiode as it can directly impact the speed of the photodiode. The capacitance in the photodiode consists of junction capacitance, capacitance coming from the RF pads and parasitic capacitance. In general, the junction capacitance dominates. Junction capacitance is created by the depletion region in the photodiode where the boundaries of the region act as the plates of a parallel plate capacitor. Junction capacitance is inversely proportional to the width of the depletion region. Reverse voltage also influences the capacitance of the diode. Because the reverse bias causes the potential across the depletion region to increase and the width of the depletion region to increase.

The I-V curves shown in the following chapters are measured by using a HP 4156B semiconductor parameter analyzer. The capacitance-voltage (CV) measurement is performed with a HP 4275A Multi-Frequency LCR meter at 1 MHz and the max voltage is 35V.

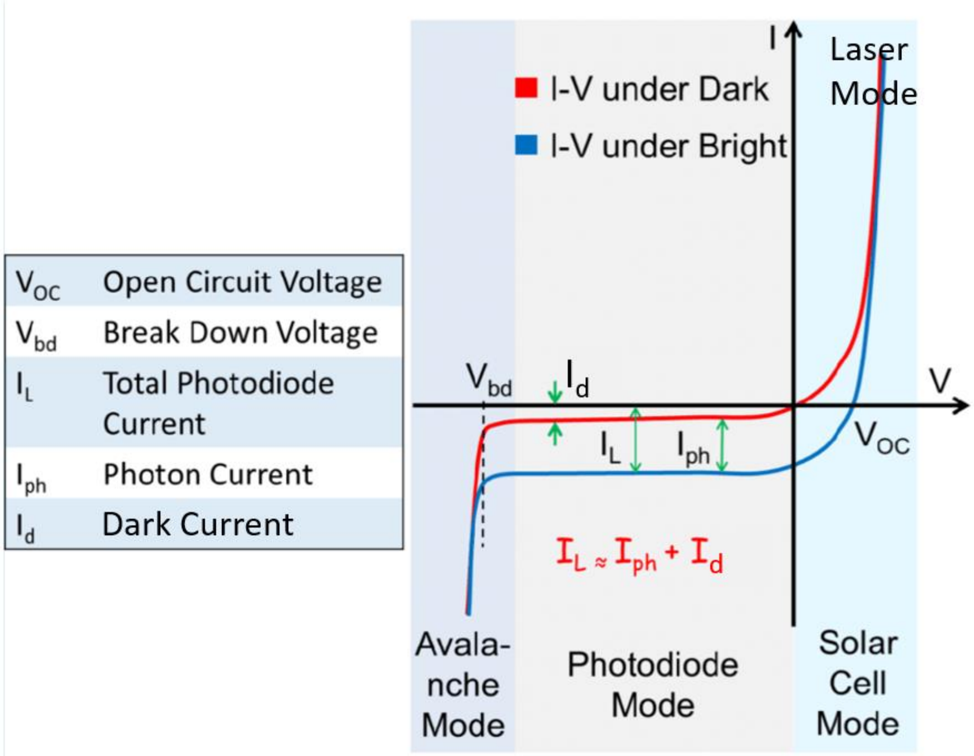


Figure 3-9 Typical I-V curves of photodiode.

3.3.2 Responsivity

The responsivity (R) of a photodiode is the ratio of generated photocurrent and incident optical power in the units of amperes per watt (A/W), which can also be expressed as:

$$R = \frac{I_p}{P} \tag{3.1}$$

Where Ip and P present the photocurrent and incident optical power.

Responsivity represents how effectively a photodiode converts light into current. The responsivity is directly related to the external quantum efficiency (η) of photodiode at certain optical wavelength (λ). The relationship between responsivity, quantum efficiency and wavelength can be expressed as:

$$R = \eta \frac{\lambda q}{hc} \tag{3.2}$$

where h is the Plank constant, q is the elementary charge and c is the speed of light.

For conventional normal-incidence photodiodes, external quantum efficiency which directly determine the responsivity depends on the absorption coefficient of material, absorption layer thickness and the reflectivity at the surface. This relationship can be express as:

$$\eta = (1-\rho)[1-e^{-\alpha(\lambda)L}] \tag{3.3}$$

where ρ is the surface reflectivity, α is the absorption coefficient of the material in absorption layer and L is the thickness of the absorption layer. Based on this equation, generally there are three ways to improve the responsivity of normal-incidence photodiode: increasing absorption coefficient by changing material, increasing the thickness of the absorption layer and reducing the reflectivity at the surface by an anti-reflection coating.

However, there is a trade-off between responsivity and bandwidth when increasing the thickness of absorption layer to improve the responsivity. Larger thickness of the absorption layer leads to longer carrier transit-times which severely limit the bandwidth of the photodiode. To improve the bandwidth and responsivity simultaneously, the waveguide integrated photodiode is a very good choice since the light is coupled evanescently and the responsivity depends on the length of the photodiode instead of its thickness. Details about waveguide design and responsivity measurement for high responsivity in waveguide photodiode are discussed in chapter 5 and chapter 6.

The responsivity is measured together with the bandwidth measurement, which will be discussed in section 3.3.4. In a waveguide photodiode, the external responsivity is directly measured and calculated by using the optical input from the optical attenuator and the DC photocurrent read from the source meter. After taking into account the coupling loss between the lensed fiber and the waveguide facet, which generally includes mode mismatch loss and reflection loss, the internal responsivity of a waveguide photodiode can be calculated based on external responsivity.

3.3.3 S-Parameters

Scattering parameters, also called S-parameters represent the linear characteristics of RF electronic circuits and components. Photodiodes can be seen as an equivalent RF circuit with lumped elements such as resistors, capacitors and inductors. The S11-parameter of a photodiode is measured to analyze and extract the photodiode equivalent circuit parameters such as series resistance, junction capacitance, and series inductance. A Keysight PNA network analyzer is used for one-port S-parameters measurements. The network analyzer consists of two parts: an N5227A module for measuring from 10 MHz to 67 GHz and an extender for measuring frequencies from 67 GHz to 110 GHz. S11 can be used to expect how much power is reflected from the device, hence is known as the return loss. Since the photodiode is a one-port device when treated purely electrical, S-parameters in photodiode can be known through S11 measurement. After an on-wafer calibration, during the measurement, the photodiode is probed with a microwave Ground-Source-Ground (G-S-G) probe which is connecting to the network analyzer through a bias-T to record the S11 data.

3.3.4 Bandwidth

Bandwidth, also called 3-dB cutoff frequency, is defined as the frequency at which the output RF power decreases by 3 dB relative to its low frequency value. Bandwidth describes the speed and frequency response of a photodiode. Bandwidth is primarily limited by the resistance-capacitance (RC) circuit response time and the carrier transit times. If assuming these two factors have Gaussian response and are independent, the total 3-dB bandwidth of photodiode can be expressed as [47]:

$$f_{3dB} = \frac{1}{\sqrt{\frac{1}{{f_{RC}}^2} + \frac{1}{{f_{tr}}^2}}} \tag{3.4}$$

where f_{3dB}, f_{RC} and f_{tr} represent the total 3-dB bandwidth, the RC-limited bandwidth and transit-time-limited bandwidth respectively.

Ignoring stray capacitance in the equivalent circuit model of a photodiode (discussed more in section 5.4.2), the simplified RC-limited bandwidth can be written as:

$$f_{RC} = \frac{1}{2\pi C_{pd}(R_l + R_s)} \tag{3.5}$$

where C_{pd} is the capacitance of photodiode, R_l is the load resistance and R_s is the PD series resistance which includes bulk, sheet, and contact resistances. The capacitance of a photodiode is given by:

$$C_{pd} = \varepsilon \varepsilon_0 \frac{A_{active}}{d} \tag{3.6}$$

where ε is the relative static permittivity of the material in the depletion region, ε_0 is the permittivity of free space, A_{active} is the photodiode junction area and d is the depletion region width.

The carrier transit time is the time required for the photo-generated electrons and holes to be collected by the metal contacts after generation in the absorption layers. Since both holes and electrons travel in the depletion region of a traditional PIN photodiode, the holes determine the transit-time-limited bandwidth because their saturation velocity is much lower than that of electrons. For the UTC structure mentioned in section 2.2, transit-time-limited bandwidth is improved compared to PIN PDs since only electrons need to travel through the depletion width. In a UTC structure, the transit time includes the diffusion time in the absorption layer and the electron drift time in the drift layer. The transit-time-limited bandwidth of a UTC photodiode can be written as [27]:

$$\frac{1}{f_{tr}} = \frac{{W_A}^2}{2D_e} + \frac{W_A}{v_{th}} + \frac{W_D}{v_e} \tag{3.7}$$

where W_A, W_D, D_e, v_{th} and v_e represent the absorption width, drift layer width, electron diffusion coefficient, thermionic emission velocity and electron velocity, respectively.

Using the equations above, it is obvious that, to make a high speed photodiode with large bandwidth, several methods can be used: reducing the PD capacitance, reducing the series resistance, or reducing the widths of absorption and drift layers.

The bandwidth of a photodiode can be measured by an optical heterodyne setup which is illustrated in Figure 3-10. In order to provide a heterodyned RF optical signal, two distributed feedback (DFB) lasers with wavelengths near 1550 nm are used. In the measurement discussed in chapter 6, the two DFB lasers were substituted by two external cavity lasers (ECL) with wavelengths near 1310 nm. By controlling the DFB laser temperature, the frequency of one DFB laser is tuned over wide frequency range to sweep the optical beat frequency from DC to hundreds of GHz. The output power of the DFB lasers needs to be matched by controlling the injection current and adjusting the polarization controllers to achieve 100% modulation depth. Then the 50/50 coupler splits the mixed optical signal into two arms. One arm which is further split into two arms is used to monitor the beat frequency by a spectrum analyzer along with photodetector (for RF frequency between 9 kHz and 50 GHz) and an optical wavelength meter with 0.001 nm resolution (for RF frequency above 50 GHz). In another arm, the heterodyned optical signal is amplified with an Erbium doped fiber amplifier (EDFA), attenuated by an optical attenuator and focused through a lensed fiber on the photodiode. The electrical signal from the photodiode is probed with GSG microwave probe connected to a bias-T which is also connected to a source meter and RF power meter. The source meter can provide a DC bias on the photodiode and reads out the DC photocurrent as well. The AC signal transmitted through the bias tee is detected with an RF power meter. A computer with a Labview program is responsible for controlling the measurement progress through standard GPIB cables connected to all the equipment as seen in Figure 3-10.

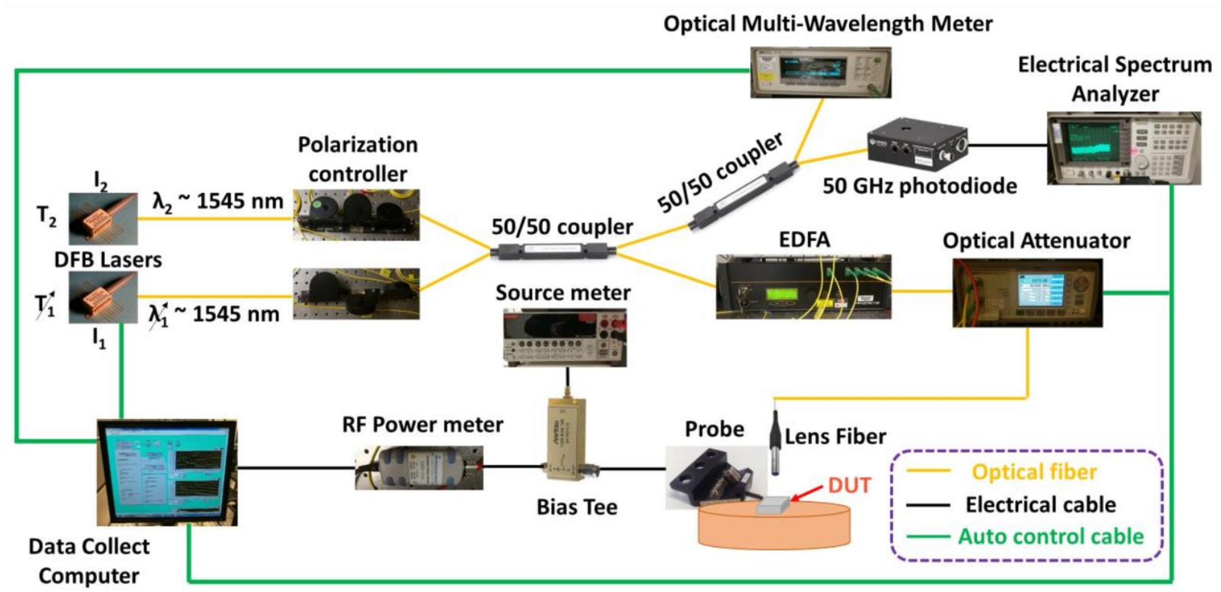


Figure 3-10. Optical heterodyne setup for bandwidth and saturation measurement. (DUT: device under test) Pictures from Qinglong Li.

3.3.5 Output RF Power

Typically, output RF power refers to the amount of AC power delivered to a 50 Ω load from the photodiode. Assuming 100 % modulation depth, the DC photocurrent which can be measured by source meter is equal to the peak amplitude of the AC current. Ideally, the RF power delivered to the load can be written as:

$$P_{RF} = \frac{1}{2} {I_{dc}}^2 R_{load} (50\ \Omega) \tag{3.8}$$

where I_{dc} current is DC photocurrent and R_{load} is load resistance. Ideally, the output power will increase quadratically with photocurrent or input optical power. However, when the photodiode is operated under extremely high power illumination, the output increases less strongly owing to the space-charge effect. This is referred to as saturation. After saturation, device failure can happen if the input optical power is further increased due to thermal effects or dielectric breakdown. The RF compression is defined as the deviation of the measured RF output power from the ideal linear output (on a log-log scale) calculated from Eq. 3.8. The photodiode RF saturation is defined as the point where the RF compression decreases 1 dB from its peak value.

The measurement of RF output saturation power uses the same setup used in bandwidth measurement shown Fig 3-10. Same with bandwidth measurement, 100% modulation is desired. The RF frequency is fixed during measurement. While increasing the input optical power, the RF output power is recorded until the compression curve drops 1 dB from the peak value.

Chapter 4 Large Area High-Power Photodiodes

4.1 Introduction

As the optical-to-electrical converter in analog optical links which require high link gain and low noise figure, it is very advantageous for large-area photodiodes to operate at very high photocurrent levels and thus, high RF output power [48]. Also, large-area PDs allow for multimode fiber input-coupling. In order to increase the output power, various photodiode device structures have been developed [26][33][49]. Previously, a 100-µm-diameter charge compensated uni-traveling-carrier photodiode (UTC) on InP achieved a responsivity of 0.45 A/W and 28 dBm RF output power at 2 GHz [50].

In this chapter, I present a 100-µm-diameter InGaAsP/InP MUTC photodiode with partially depleted absorber with 0.63 A/W responsivity and an RF output power of 23 dBm at 2 GHz.

4.2 Device Structure and Fabrication

The MUTC structure was grown on semi-insulating double-side-polished InP substrates by metal organic chemical vapor deposition (MOCVD). The epitaxial layer structures, schematic and top view of the fabricated PDs are shown in Figure 4-1 and Figure 4-2. The epitaxial layer design includes an 850 nm-thick partially depleted InGaAs absorber layer for large responsivity, 50 nm cliff layer to reduce the deleterious effect of space-charge at high photocurrent levels to improve PDs power and a wide-bandgap 900-nm-thick InP drift layer. Two top layers are a 100 nm p+ InP electron blocking layer and a 50 nm p+ $In_{0.53}Ga_{0.47}As$ contact layer. The function of the two 15 nm InGaAsP quaternary layers is “smoothing” the abrupt conduction band barrier at the InGaAs-InP heterojunction interface. The wafer was fabricated into back-illuminated mesa photodiodes and top using contact photolithography and inductive coupled plasma etching processes. The mesa sidewalls were passivated with a 460 nm-thick layer of SiO_2. Microwave contact pads and air-bridge connections to the top p-contact layer were fabricated to allow for microwave

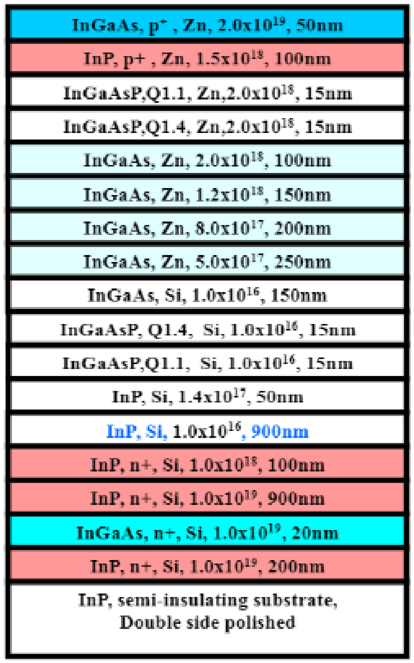


Figure 4-1. The epitaxial layer structure of large-area MUTC photodiode.

measurements (Figure 4-2). Finally, a 260 nm-thick SiO_2 film was deposited on the back of the wafer as an antireflection coating.

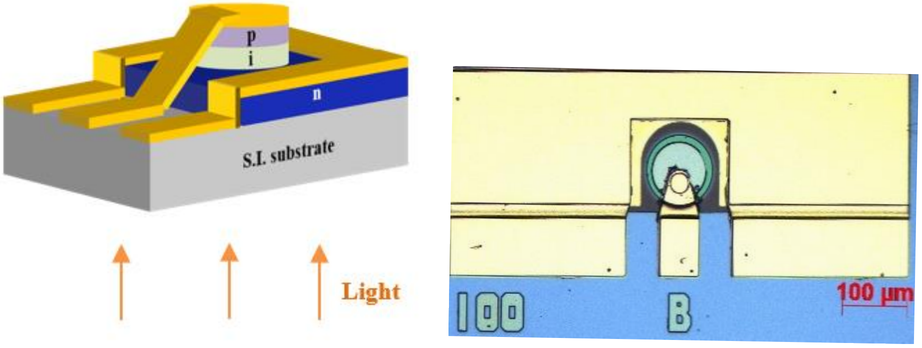
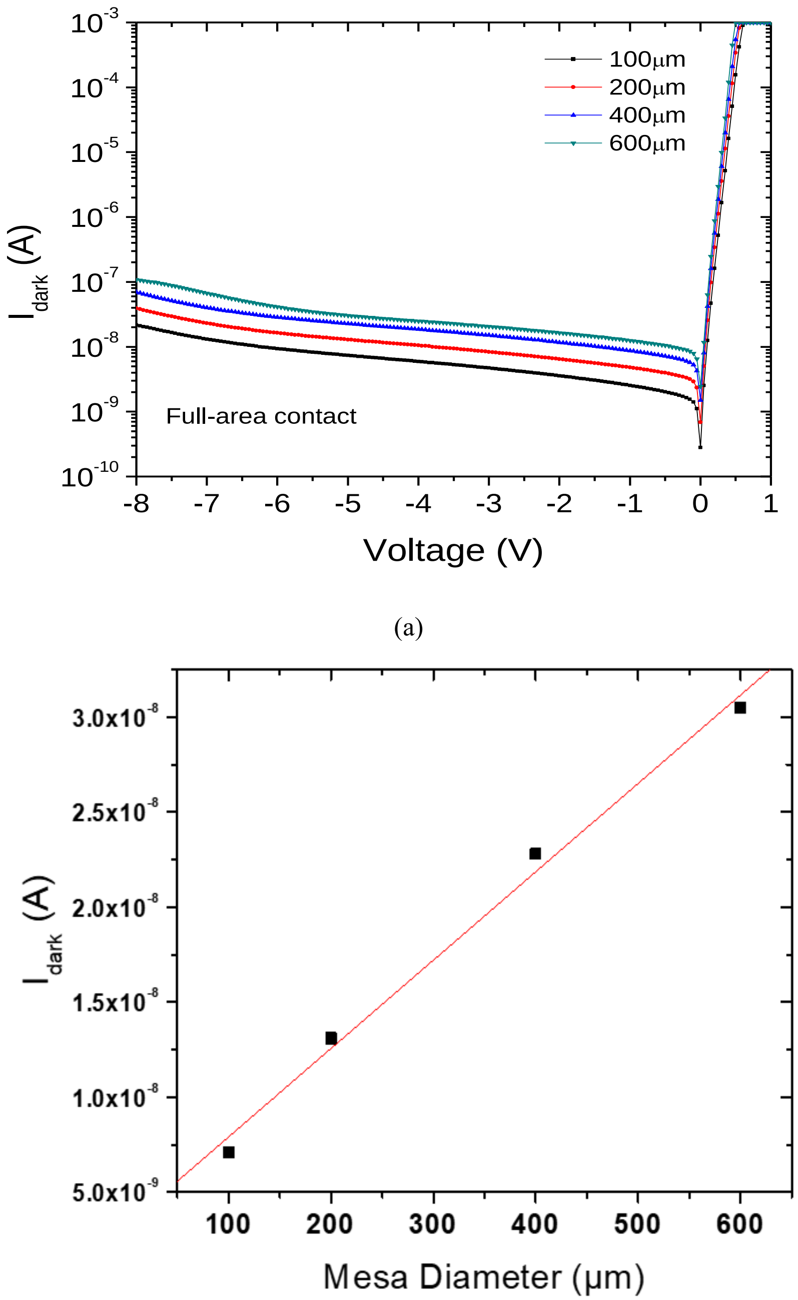


Figure 4-2. Schematic of large-area MUTC photodiode and top-view micrograph of fabricated PD.

4.3 Device Characterization

The dark current of a 100-µm-diameter PD was as low as 20 nA at -8 V, which is shown in Fig 4-3(a). The linear relation between dark current and PD diameter revealed in Fig 4-3(b) indicates that the dark current is dominated by surface leakage.

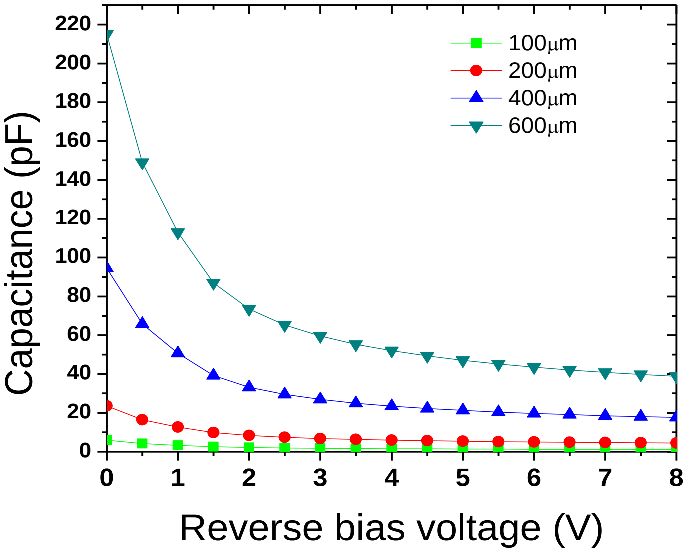
The capacitance-voltage characteristics (Fig 4-4(a)) showed that the photodiode is fully depleted at a reverse bias above 5 V. For 100-µm-diameter PDs, the capacitance was 1.4 pF at -5 V. The series resistance of a 100-µm-diameter PD was 12 Ω as measured from the I-V curve under forward bias at 30 mA. The responsivity at 1.55 µm wavelength was 0.63 A/W (Fig 4-4 (b)).



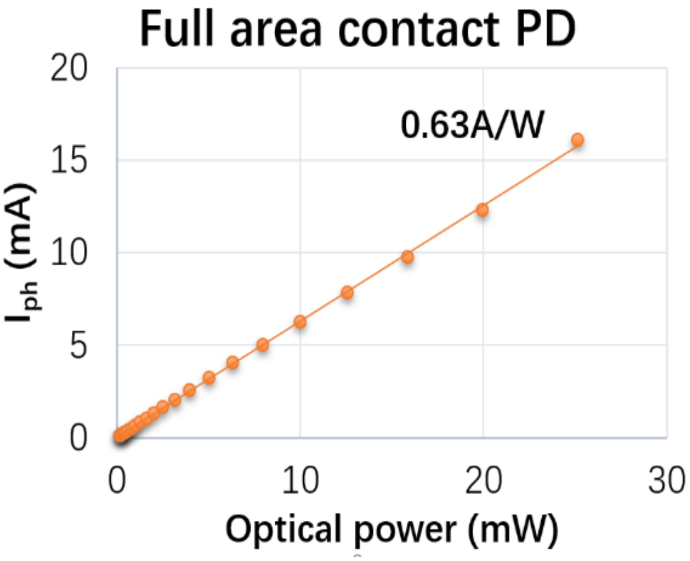
(a)

(b)

Figure 4-3. (a) I-V, (b) dark current at -5 V vs. PD diameter.



(a)



(b)

Figure 4-4 (a) C-V, (b) responsivity.

One distributed feedback laser with wavelengths of 1550 nm, a signal generator, and a modulator were used to generate a modulated optical signal. The frequency of the optical signal was controlled by tuning the frequency of the signal generator. The frequency responses of 100, 200, 400, 600-µm diameter PDs under -5 V bias voltage and 0.5 mA photocurrent are shown in Fig 4-5. The bandwidth of 100 µm diameter device can reach above 1.8 GHz at 0.5 mA photocurrent with 5 V reverse bias. Because the large size of our device, our devices are all RC limited.

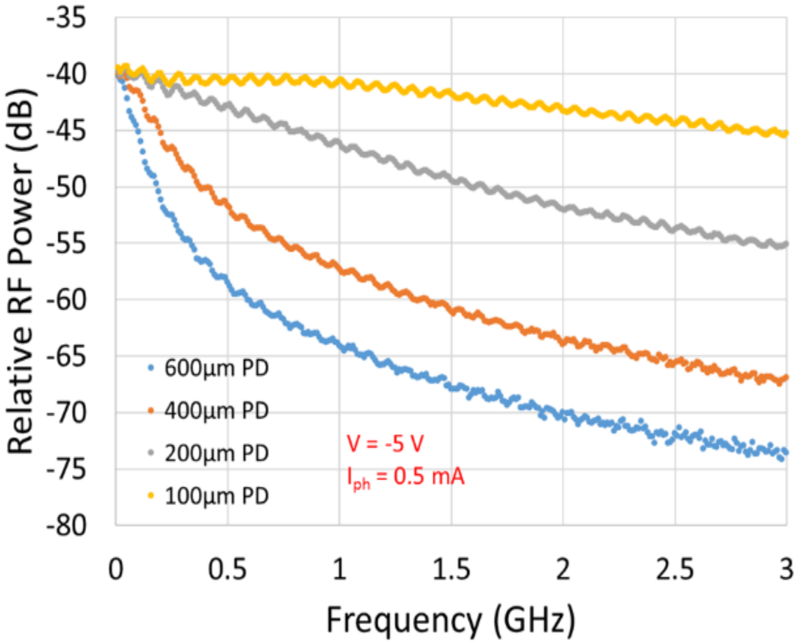


Figure 4-5. Measured frequency responses at -5 V of PDs with different areas.

The RF saturation current is defined at the point where the RF compression curve drops by 1 dB from its peak value. We observe that the power increases super linearly with increasing photocurrent before it saturates due to the space charge effect. Note that as the photocurrent increases, the RF output power approach closer to the ideal power. The RF compression and output power for a 100-µm PD are shown in Fig. 4-6. The output RF power for 100-µm PD was 23.2 dBm at 2 GHz under 5 V reverse bias. The saturation current was 195 mA.

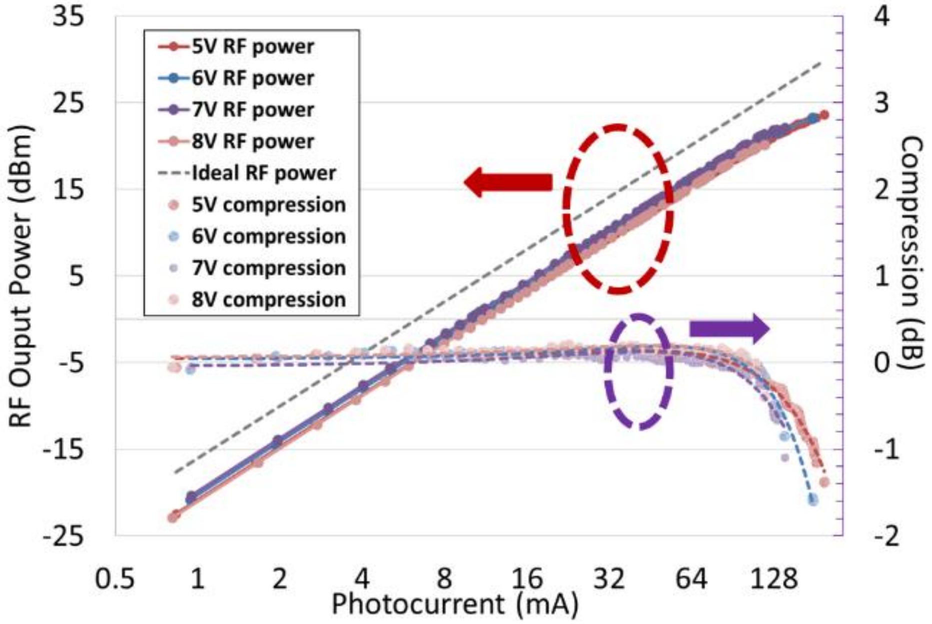


Figure 4-6. RF output power and compression curves versus average photocurrent at 2 GHz.

4.4 Summary

In this chapter, I have demonstrated back-illuminated high-power MUTC photodiodes on InP substrate with a low dark current and high responsivity. A 100-µm-diameter photodiode achieved an RF output power of 23 dBm at 2 GHz and a dark current of 20 nA at -8 V. The 3-dB bandwidth and responsivity were 1.8 GHz and 0.63 A/W, respectively. Based on its large active area and high RF output power, these PDs can be used in free space analog photonics system such as photoacoustic imaging systems, antenna remoting and photonic oscillator systems.

Chapter 5 High-speed Zero-bias Waveguide Photodiodes

5.1 Introduction

Photodiodes that can be operated at zero bias are particularly beneficial since they require no power supply and alleviate the electrical cross-talk that occurs with tight metal wiring in dense photonic integrated circuits and PD arrays [51]. Moreover, since zero-bias photodiodes do not have bulky bias circuits, the smaller footprint of zero-bias photodiodes eases packaging and system design. A staggered band lineup (type II) is beneficial to avoid the potential barrier in the conduction band between the absorber and the wide-bandgap drift layer in a traditional UTC PD [34]. Such a type-II $GaAs_{0.5}Sb_{0.5}/InP$ photodiode with 170 GHz bandwidth at zero bias was demonstrated by Jhih-Min, et al., in 2017 [35]. This device was top-illuminated.

In this chapter, I describe design and fabrication of a novel evanescently coupled waveguide type-II UTC PD with dual-integrated waveguide-depletion layer that can achieve high efficiency and high speed simultaneously. A bandwidth of 66 GHz under zero-bias operation and 102 GHz bandwidth at -1 V have been successfully demonstrated for a PD with an active area of $4\times4\ \mu m^2$. Larger PDs ($5\times7\ \mu m^2$) have 56 GHz bandwidth and an internal responsivity of 0.48 A/W at 0 V.

5.2 Device Epitaxial Design

Previously, a high-speed and high-power evanescently coupled waveguide integrated modified uni-traveling- carrier (MUTC) photodiode with 105 GHz bandwidth at -3 V has been demonstrated in my group [32]. However, at low or zero bias, a bandwidth limitation often arises from discontinuities in the band diagram which can impede carrier transport in these heterojunction PDs [33]. As discussed in section 2.2, to avoid the potential barrier in the conduction band between the absorber and the wide-bandgap drift layer in a uni-traveling carrier (UTC) PD at low bias, a

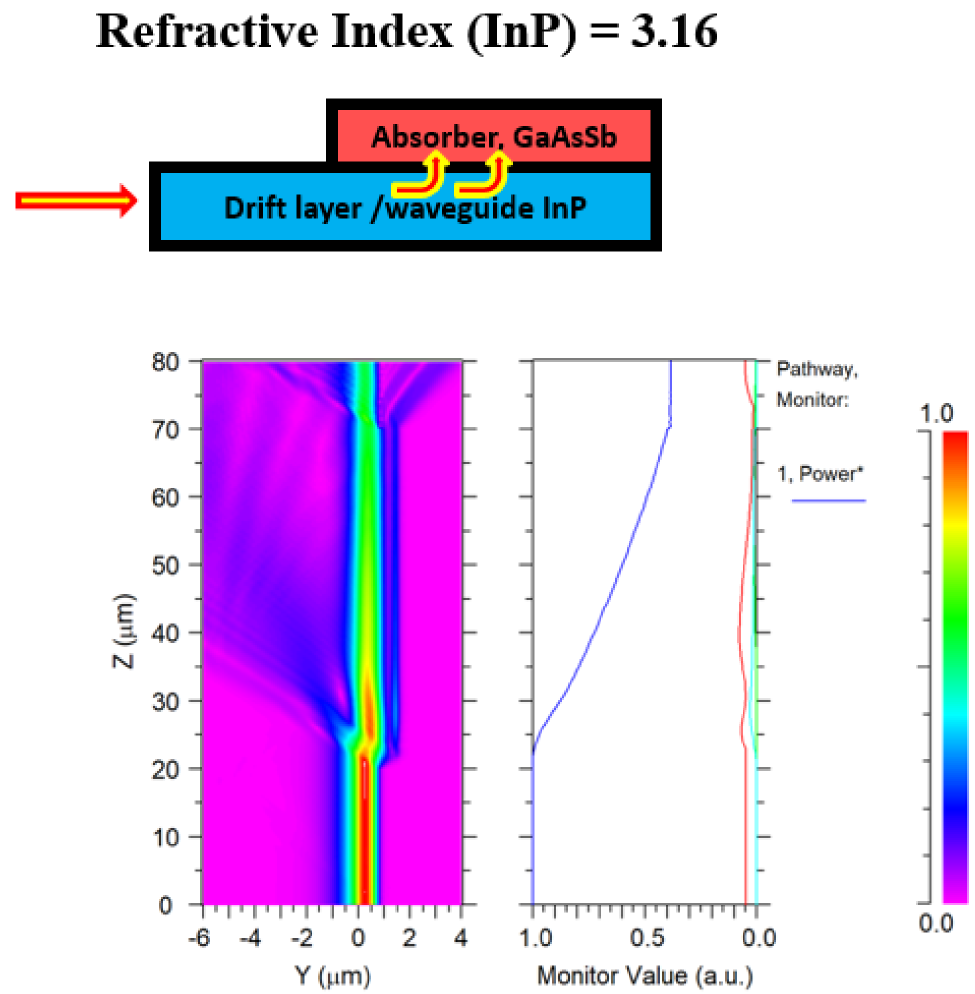


Figure 5-1. Light absorption in InP waveguide-GaAsSb absorber structure on InP substrate.

staggered band lineup (type-II) is beneficial [34]. In addition, to achieve high speed and high efficiency simultaneously at zero bias, I designed a novel evanescently coupled waveguide type-II MUTC PD with dual-integrated waveguide-depletion layer.

For traditional zero-bias type-II waveguide photodiode in [35], InP is used for carrier collection layer. However, InP is not suitable material for waveguide to improve the light absorption efficiency. Here I chose to use InAlGaAs as the material in the dual-integrated waveguide-

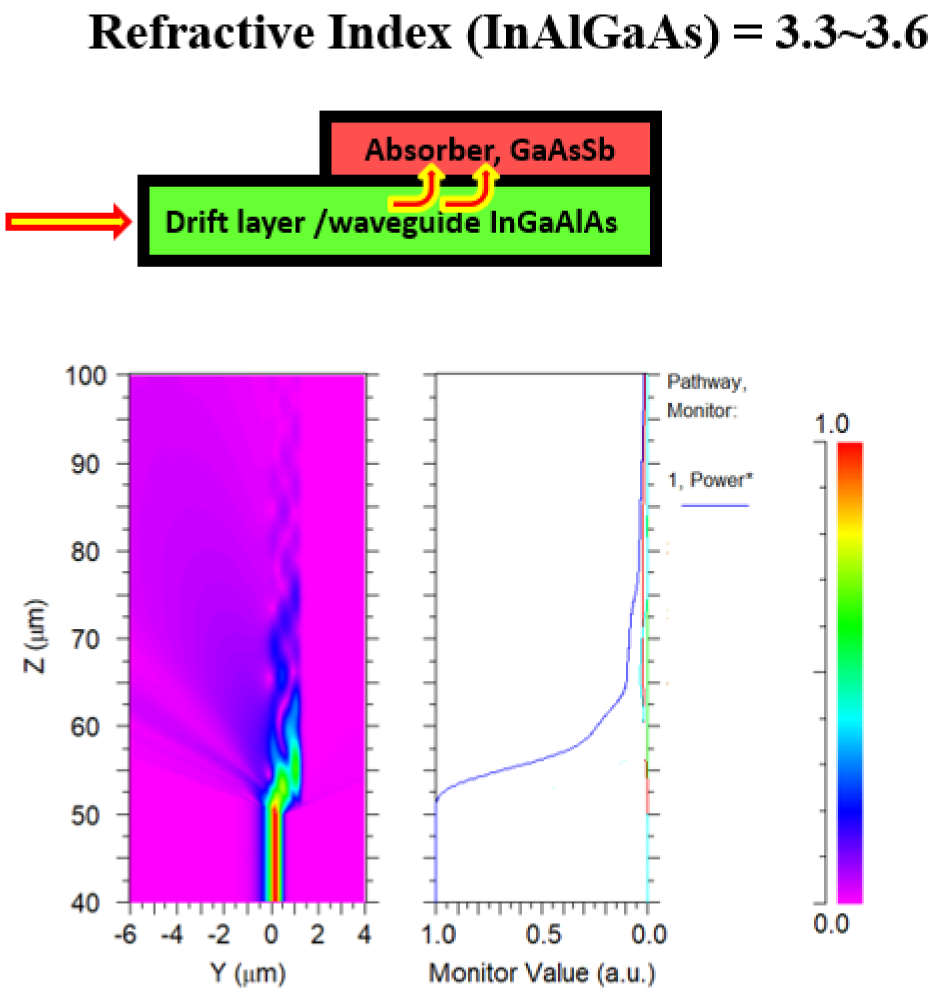


Figure 5-2. Light absorption in InAlGaAs waveguide-GaAsSb absorber structure on InP substrate.

depletion layer. I use commercial software named R-soft to perform an optical simulation. As shown in Figure 5-1 and Figure 5-2, because the refractive index of InP (3.16) is much lower than InAlGaAs (3.55) the simulation results show that only 60% optical power can be absorbed when the length of the PD is 50 μm. But if we use InAlGaAs as waveguide material, most light can be absorbed when the length of PD is 20 μm.

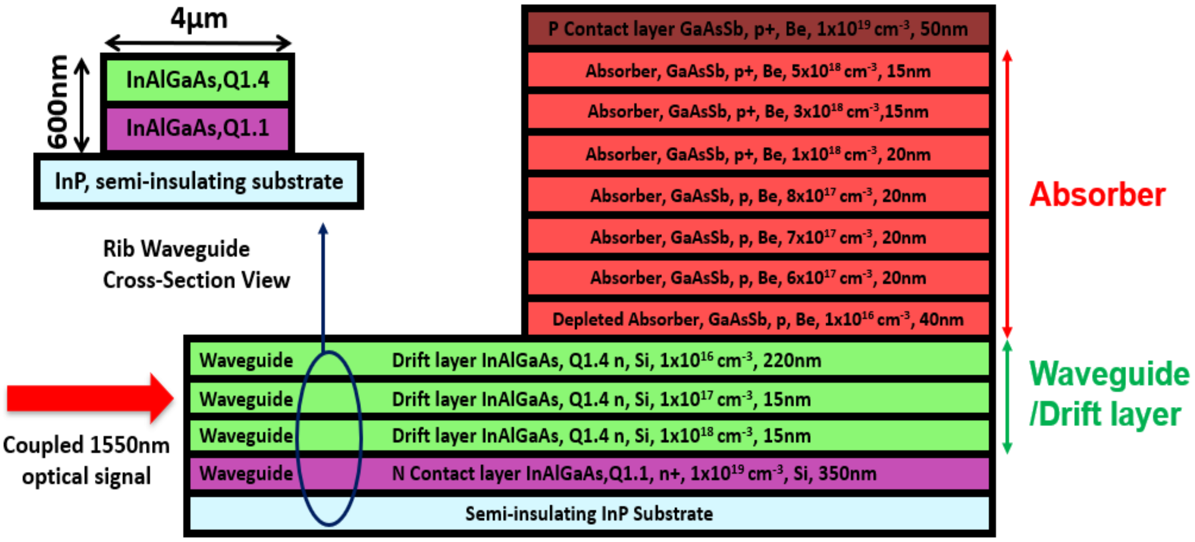


Figure 5-3. Epitaxial layers of zero bias waveguide PD.

The epitaxial layer structure of the waveguide PD is shown in Figure 5-3. In order to achieve high efficiency, I utilized an $In_xAl_yGa_{1-x-y}As$ dual-integrated waveguide-depletion layer. The light absorption situation in this epi-structure has been simulated. As shown in Figure 5-4, more than half of the light can be absorbed when the length of our PD is only 5 µm and more than 80% light can be absorbed when the length of our PD is 10 µm.

The epitaxial layer design consists of two primary parts: a narrow-bandgap GaAs$_{0.5}$Sb$_{0.5}$ absorber layer and an In$_x$Al$_y$Ga$_{1-x-y}$As waveguide-drift layer. Fig 5-5(a) and 5-5(b) show the simulated band

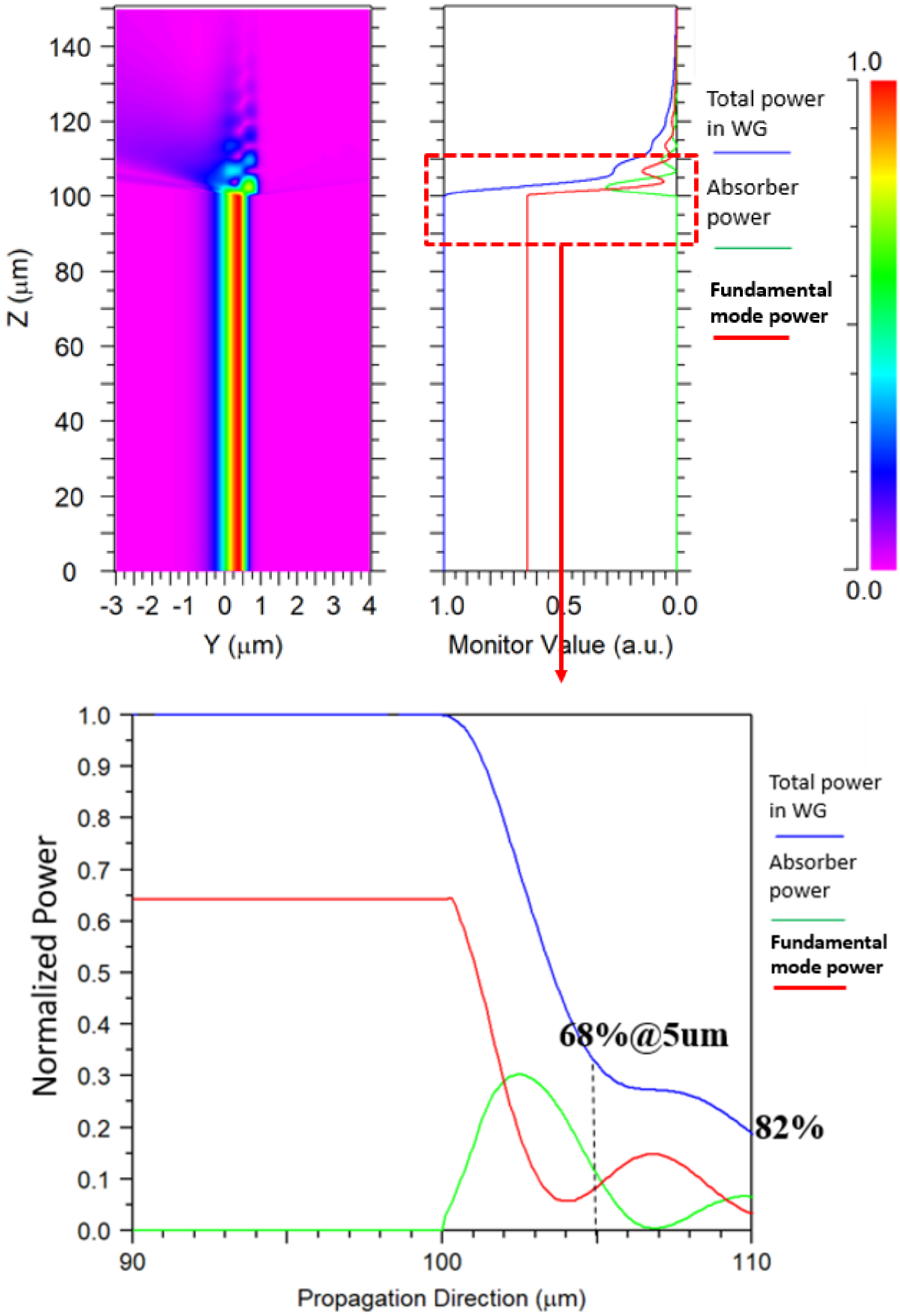


Figure 5-4. Light absorption in zero-bias waveguide photodiode (blue curve presents the total power in entire device).

diagram and electric field distribution inside the absorption and drift layer for the demonstrated device structure under zero-bias using a commercial software (APSYS). A 350 nm–thick heavily n-doped $\mathrm{In_{0.53}Al_{0.25}Ga_{0.22}As}$ n-contact layer (purple) was first deposited followed by the 250 nm $\mathrm{In_{0.53}Al_{0.09}Ga_{0.38}As}$ waveguide-drift layer (green) with graded doping profile (1×10^{16} $\mathrm{cm^{-3}}$-1×10^{18} $\mathrm{cm^{-3}}$) to provide sufficiently large field under zero-bias (over 10 kV/cm under 1 mW/μm^2 light illumination) for high electron velocity which is shown in Figure 5-5 (b). A low background carrier concentration in the drift layer is a key aspect for achieving a steep band slope (Figure 5-5(a)) and a uniform internal electric field distribution (Figure 5-5(b)) in the drift layer, which can enable high-speed carrier transport at zero bias [17].

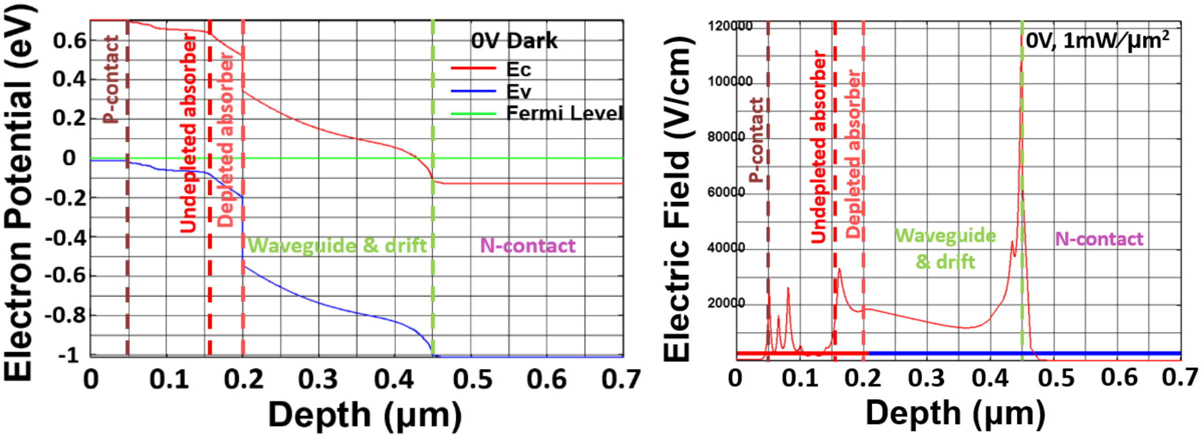


Figure 5-5. (a) Simulated band diagram at 0 V. (b) Simulated electric field distribution at 0 V and 1 mW/μm^2 light illumination at 1550 nm.

In this design, the core layer of the passive feeding waveguide serves simultaneously as the electron drift layer in the PD which facilitates efficient light coupling from the waveguide into the absorber over a short length [18]. To ensure that the optical mode is mostly confined in regions with low doping, the waveguide-drift layer has a higher refractive index than the underlying highly doped n-contact layer resulting in a confinement factor of 0.6 in the waveguide. Then, for high bandwidth at zero bias, we adopted 150 nm-thick graded doped (5×10^{18} cm^{-3}-1×10^{16} cm^{-3}) $GaAs_{0.5}Sb_{0.5}$ as absorber layer which results in type II band alignment at the interface to the $In_{0.53}Al_{0.09}Ga_{0.38}As$ drift layer (shown in Fig 5-5 (a)) and a built-in electric field for electron acceleration (shown in Fig 5-5(b)). Finally, the p-type contact was formed using 50 nm heavily p-type doped (5×10^{19} cm^{-3}) $GaAs_{0.5}Sb_{0.5}$. The epitaxial layer structure of the wafer, shown in Figure 5-3, was grown on semi-insulating InP substrate by IntelliEPI using molecular-beam epitaxy and in situ-doped with beryllium (p-type) and silicon (n-type) dopants.

5.3 Device Fabrication

Figure 5-6 (a) shows a schematic of the waveguide photodiode with the electrode configuration. The waveguide PDs were fabricated by using a double-mesa etching process which is similar to the process introduced in section 3.2. The first etch was to define the p-mesa and a 4 µm-wide rib waveguide. Then, a second dry etching process was adopted to remove the $GaAs_{0.5}Sb_{0.5}$ on top of the $In_{0.53}Al_{0.09}Ga_{0.38}As$ waveguide rib and to form the n-mesa simultaneously. AuGe/Ni/Au and

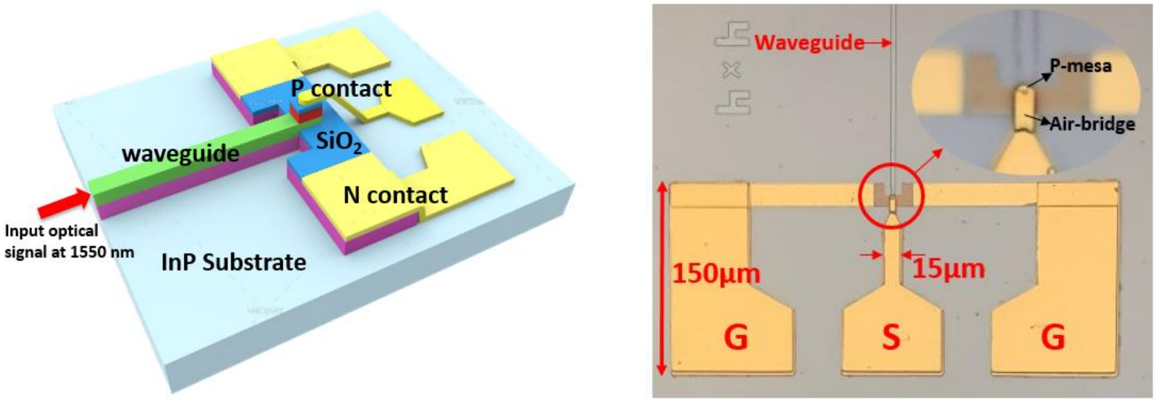


Figure 5-6. (a) Illustration of zero bias waveguide PD, (b) micrograph of the zero bias waveguide PD.

Ti/Pt/Au metal stack were deposited as n-metal and p-metal contacts, respectively. As shown in Figure 5-6(a), the PDs were connected to gold-plated coplanar waveguide (CPW) RF pads through an air-bridge. In order to increase the PD bandwidth, we carefully designed the signal (S) and ground (G) conductors' lengths and widths (Figure 5-6 (b)), which varied with the size of the mesa to provide inductive peaking. After fabrication, the completed wafer was cleaved to expose the waveguide facets for light input coupling.

After cleaving, focused ion beam (FIB) was used to etch away small part of the waveguide at the facet to improve the quality of the waveguide facet, which can improve the light coupling efficiency between the lensed fiber and the III-V waveguide. This is critical for improving the external responsivity of the photodiode. As shown in Figure 5-7, the quality of the waveguide facet has been improved obviously after using FIB.

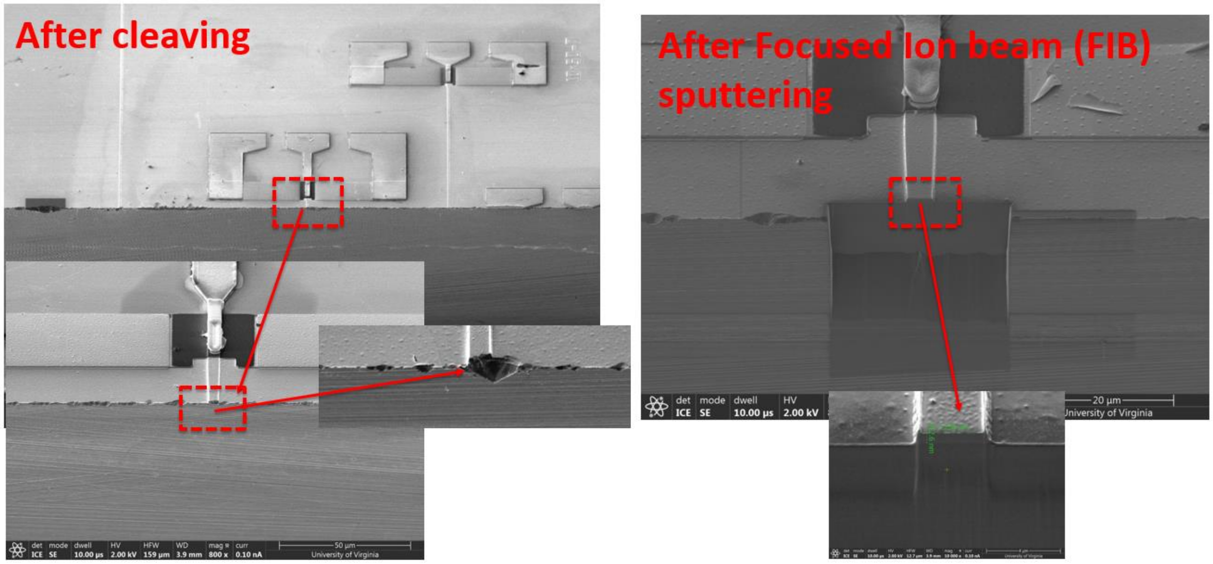


Figure 5-7. SEM picture of waveguide facet before and after FIB.

5.4 Device Characterization

5.4.1 Current-Voltage and Capacitance-Voltage

Waveguide PDs with active areas from 16 μm^2 (4×4 μm^2) to 2000 μm^2 (20×100 μm^2) were fabricated and the dark current versus voltage curves are shown in Figure 5-8. All PDs have a low dark current in the range of 10-100 nA at -3 V bias.

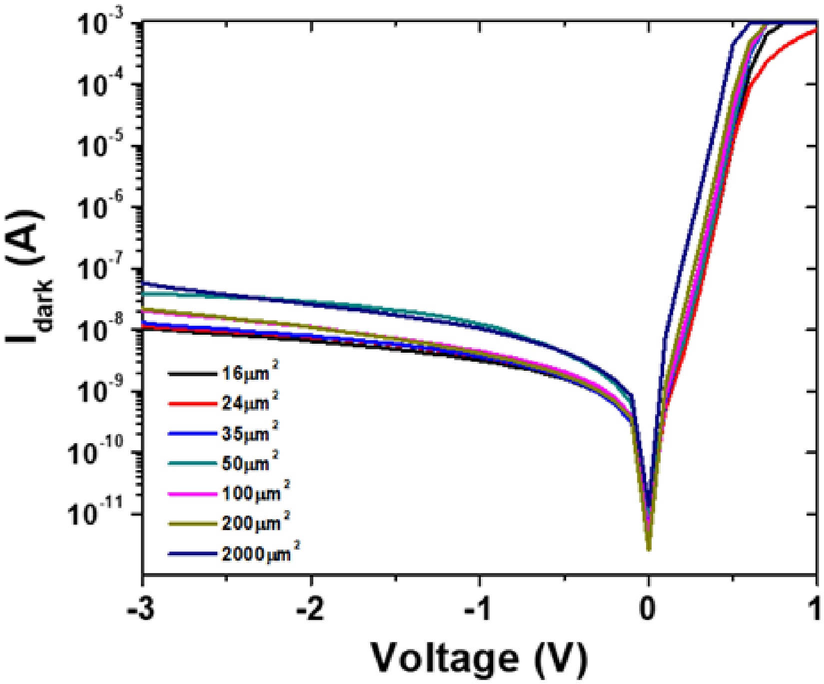


Figure 5-8. Dark current versus bias voltage.

The total capacitance C_{total} of different sized PDs were measured by using an LCR meter and the results are shown in Figure 5-9. The capacitance depends only slightly on bias between -0.5 V and -2 V which indicates that our PDs are approaching full depletion in this range.

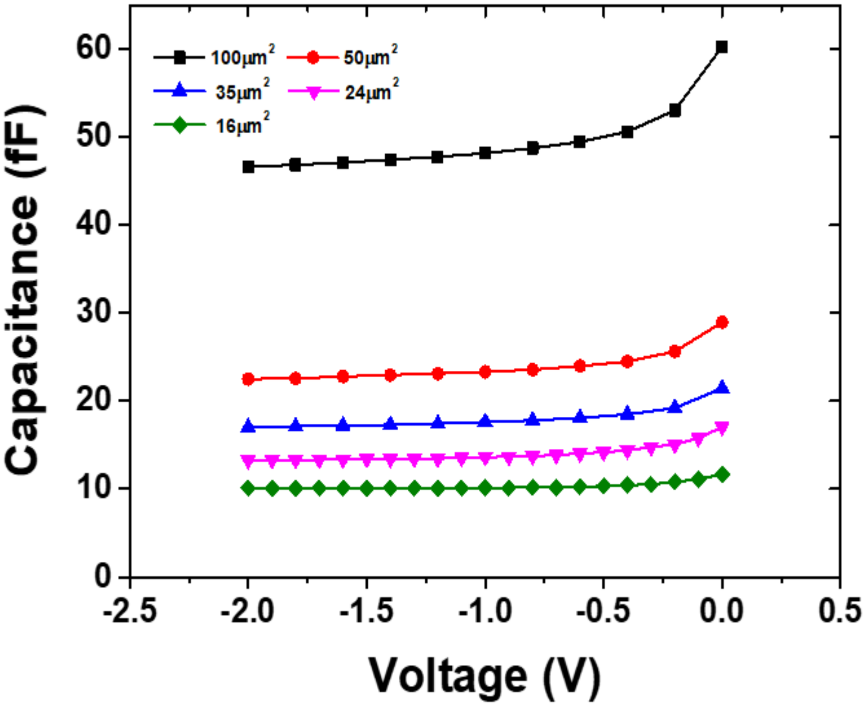


Figure 5-9. Measured capacitance versus voltage.

Figure 5-10 shows the measured capacitance at 0 V, and as expected, a linear relationship between C_{total} and the PD area can be seen. Figure 5-10 also shows the calculated junction capacitance (C_{pn}), which uses the parallel plate capacitor equation (inset in Figure 5-10.), where ε_0, ε_r, A and d are the permittivity of free space, the dielectric constant (12.7), PD active area, and the depletion width (290 nm), respectively. We attribute the slope difference between measured and calculated capacitance to the additional capacitance that originates from the RF pads (C_{cpw}) and the fact that the PDs are not fully depleted at 0 V. Our results suggest that for a 16 µm^2 waveguide photodiode the capacitance from the RF pads makes up a third of the total capacitance, indicating that the RF pads play a significant role in the RC component of the bandwidth in the smallest photodiode.

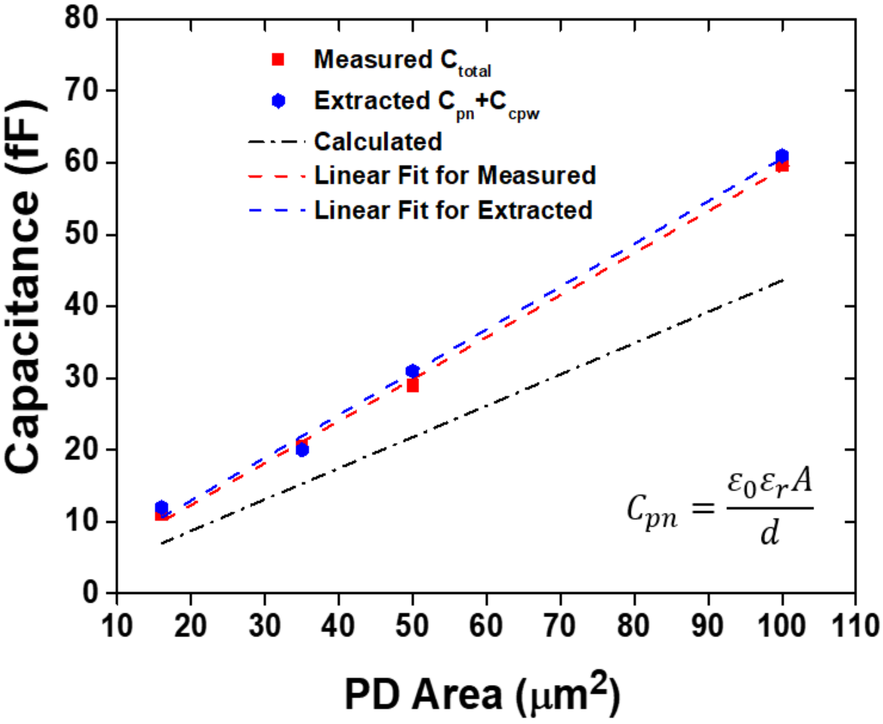


Figure 5-10. Measured, extracted from S11 simulation, and calculated capacitance versus PD area at 0V.

5.4.2 S-Parameter Measurement

The scattering parameter S11 of the PDs was measured up to 67 GHz under zero bias operation by using a vector network analyzer and the results are shown as blue lines in Fig. 5-11(a). In order to estimate the RC bandwidth of our devices, a simple photodiode equivalent circuit model (Fig. 5-11(b)) was used to extract the circuit elements through S11 fitting using Advanced Design System (ADS). R_s, R_d, L_{cpw} and R_{load} represent the series resistance, junction resistance, inductance of the CPW pads, and load resistance, respectively. As shown in Fig. 5-10, the fitting curves (red lines) and measured S11 (blue lines) for two PDs with different areas coincide very well on the

Smith Charts.

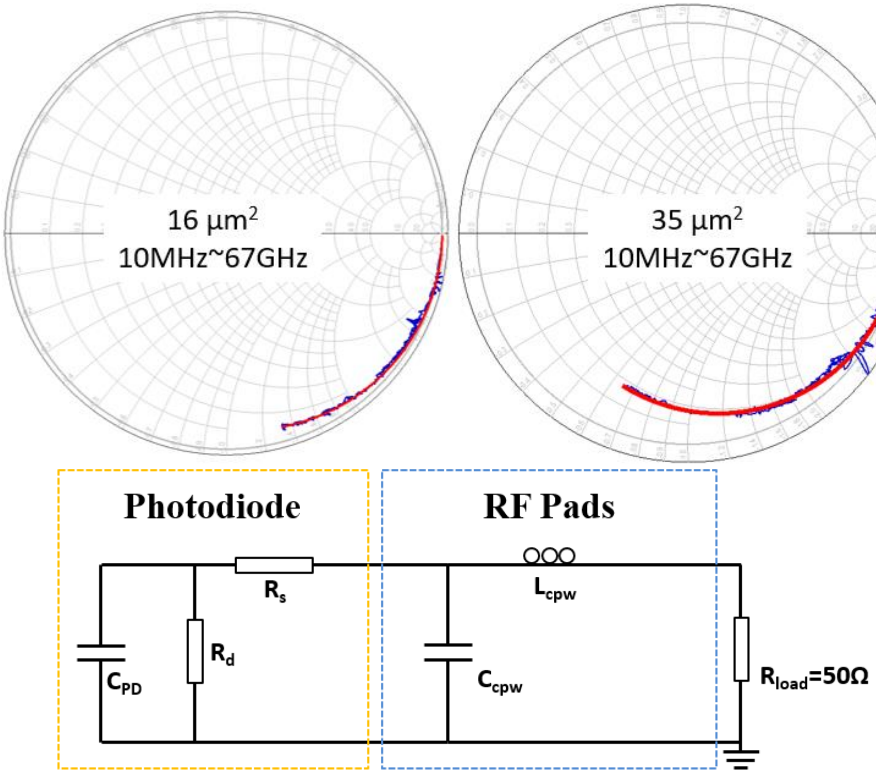


Figure 5-11. (a) Measured (blue line) and fitted (red line) S11 data for devices with active areas of 16 μm^2 and 35 μm^2. (b) Circuit model of zero-bias waveguide PDs for S11 fitting.

Table II summarizes the extracted circuit elements at 0 V from ADS, the measured total capacitance, and the calculated C_{pn} and RC bandwidths for different PD active areas. We found a good agreement between the calculated, measured, and extracted values of the capacitance, which is also shown in Fig. 5-10. We also found that R_s does not significantly scale with the PD's active area, which indicates a small p-contact resistance and that the bulk resistance dominates. Note that the extracted inductances and capacitance of the CPW pads, L_{cpw} and C_{cpw}, vary with the PD area as the size of the RF pads was optimized for each device.

Table II Calculated, extracted, and measured parameters of zero-bias waveguide PDs

PD area (μm^2)	Calculated	Extracted from S11 fitting (0V)						CV measurement
	C_{pn} (fF)	R_d (MΩ)	C_{CPW} (fF)	L_{CPW} (pH)	R_s (Ω)	C_{pn} (fF)	RC BW (GHz)	C_{total} (fF)
16	7	3	4	70	15	8	204	11
35	15	3	6	75	22	14	111	21
50	22	3	7	80	17	24	77	29
100	44	3	9	85	16	52	40	60

5.4.3 Responsivity

The responsivities of the waveguide PDs were measured at 1550 nm wavelength under zero bias operation and the results are listed in Table III.

Table III Responsivity summary of zero-bias waveguide PDs

PD area (μm^2)	Responsivity (A/W)	
	External R	Internal R
16 (4x4)	0.06	0.17
24 (4x6)	0.08	0.23
35 (5x7)	0.17	0.48

The external (fiber-coupled) responsivities were measured using a single-mode tapered optical fiber for input coupling and include the fiber-chip coupling and reflection losses. We expect that the external responsivities can be further increased once we use an anti-reflection coating and reduce the fiber-chip mode-mismatch by, for example, implementing a dual-step coupling scheme similar to the design in ref. [52].

After taking into account the 3 dB fiber-chip mode mismatch loss that was calculated using Beamprop software, and 1.5 dB reflection losses at the waveguide facet, the internal responsivities of waveguide PDs with areas of 4×4 μm^2, 4×6 μm^2 and 5×7 μm^2 are 0.17 A/W, 0.23 A/W, and 0.48 A/W respectively, which indicates that responsivity increases with PD length. Also, since we used a highly doped n-contact layer beneath the waveguide-drift layer, we estimated the losses from free carrier absorption using an absorption coefficient of 0.65 cm^{-1} and Beamprop software. Owing to the small mode overlap with the 1×10^{19} cm^{-3} n-type layer, we found a loss of only 0.1 dB/mm, which indicates that free carrier absorption is not be a main source of waveguide loss. Fig. 5-8 shows the bias dependence of the internal responsivity for 4×4 μm^2 and 5×7 μm^2 PDs at 1550 nm wavelength. Note that when the voltage changes from 0 V to -2 V the internal responsivity of our waveguide PD has very small variations (0.17 A/W vs. 0.18 A/W and 0.48 A/W vs. 0.51 A/W), which reveals that the built-in electric field is sufficient to collect almost all photogenerated carriers.

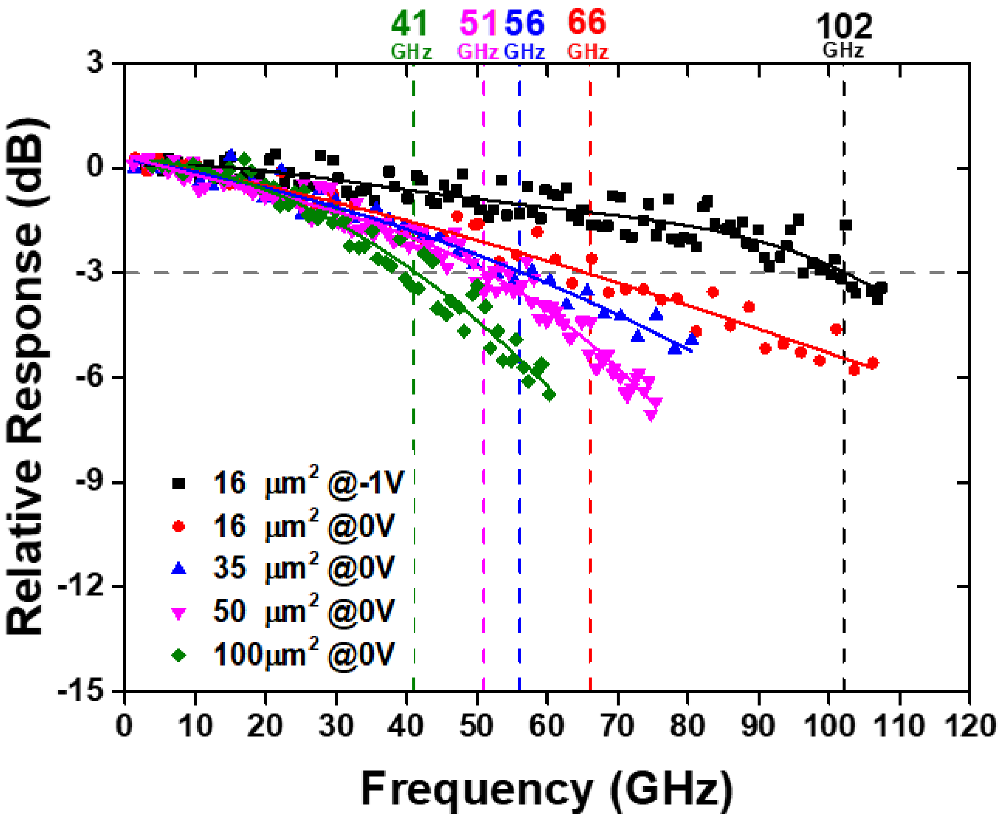


Figure 5-12. Frequency responses of waveguide PDs with different PD area at 1mA. (Solid line: polynomial fit)

5.4.4 Frequency Response

An optical heterodyne setup was used to measure bandwidth and saturation characteristics. Light with a wavelength near 1550 nm from two distributed feedback lasers was heterodyned to generate an optical signal with a modulation depth close to 100 %. We controlled the frequency of the beat signal by thermally tuning the wavelength of one laser. The RF output power was detected using a calibrated power meter with a frequency range from dc to 110 GHz. Figure 5-12 summarize the frequency responses of the devices with various active areas at 1 mA at 0 V and at low bias. At 0 V, waveguide photodiodes with active areas of 16 μm^2, 35 μm^2, 50 μm^2 and 100 μm^2 have bandwidths of 66 GHz, 56 GHz, 51 GHz and 41 GHz, respectively. For the device with an active area of 16 μm^2 a 3-dB bandwidth of 102 GHz was measured when applying -1 V.

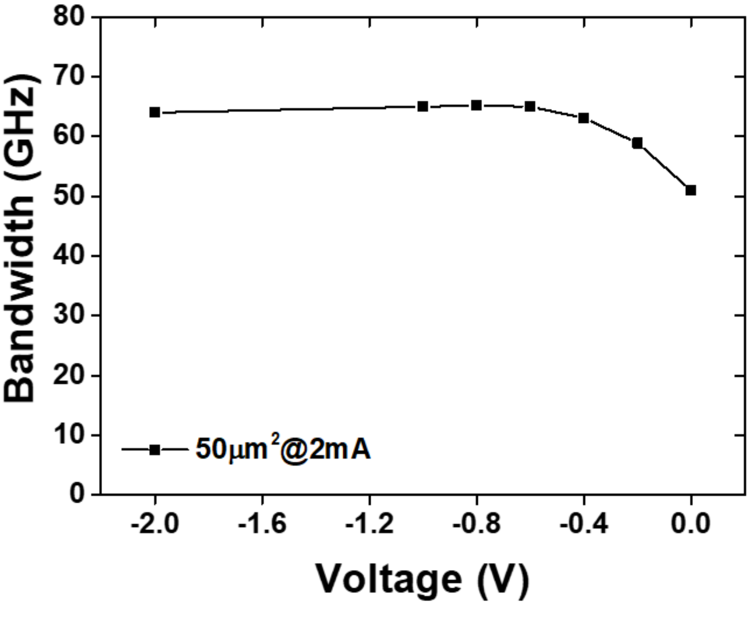


Figure 5-13. Measured bandwidth versus reverse bias voltage of 50 μm^2 waveguide PD at 2 mA.

The bias dependence of the bandwidth for a 50 μm^2 PD at 2 mA is shown in Figure 5-13. It is obvious that there is only a small roll-off in bandwidth of 20 % below 0.5 V reverse bias, which indicates that the drift layer is nearly depleted under zero bias operation. However, and as shown in Figure 5-14, the bandwidths of our devices decrease when applying higher reverse bias (<-1 V). Most likely, the observed bias dependent phenomenon can be attributed to the velocity overshoot of electrons in the drift layer, which has been previously observed in UTC PDs [53] [54].

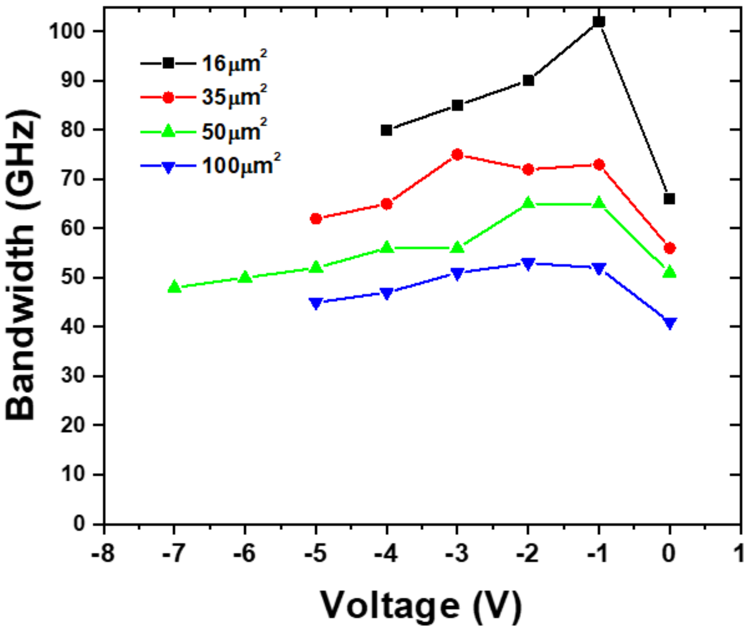
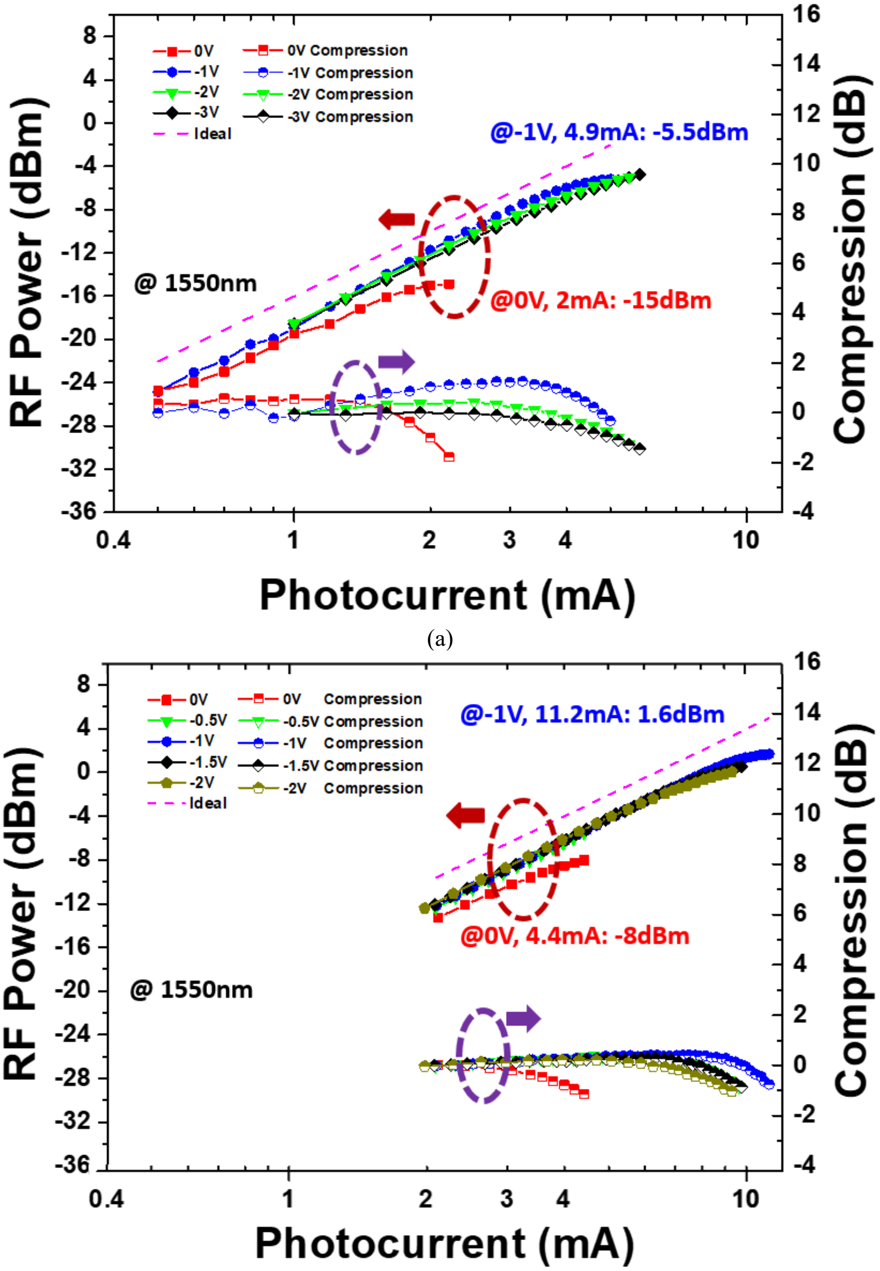


Figure 5-14. Bandwidth at 1550 nm versus reverse bias voltage of PDs with different active area at 2 mA.

As shown in Figure 5-14, this effect is less pronounced for PDs with large areas since their bandwidth limitation has a larger RC component. For example, the calculated RC bandwidth of a 100 μm^2 PD is 40 GHz (table II), which is much lower than the simulated transit time limited bandwidth of 120 GHz using CROSSLIGHT APSYS. For these large-area PDs we expect that a reduction of the doping concentration in the drift layer can ensure full depletion at 0 V which will further increase the RC-component of the bandwidth.

5.4.5 RF Saturation Characteristics

In Figure 5-15, the RF saturation was characterized by measuring the RF output power as a function of the average photocurrent at a fixed frequency.



(a)

(b)

Figure 5-15. RF output power and RF power compression versus photocurrent.

(a) 4×4 μm^2 at 100 GHz (b) 5×20 μm^2 at 40 GHz.

Figure 5-15 (a) and (b) show the RF output power of 16 μm^2 and 100 μm^2 waveguide PDs at 100 GHz and 40 GHz at different voltages, respectively. We found that the power increases super linearly with increasing photocurrent before it saturates. This is the well-known bandwidth enhancement due to the current-induced electric field in the graded absorption layer [49]. In general, as photocurrent increases, the space-charge effect causes an electric field reduction in the depletion region which impedes carrier transport. It ultimately leads to power saturation. We defined the saturation current and power as the photocurrent and power where the RF power compression curve drops by 1 dB from its peak value. When there was no bias, waveguide PDs with 16 μm^2 and 100 μm^2 achieved -15 dBm at 2 mA and -8 dBm at 4.4 mA. At -1 V, the same PDs achieved -5.5 dBm at 4.9 mA and 1.6 dBm at 11.2 mA which can be explained by a reduced space-charge effect. It should be mentioned that the saturation power decreases at higher reverse voltages due to the bandwidth reduction shown in Figure 5-14. This behavior is in contrast to previous work on high-power waveguide integrated InGaAs/InP MUTC photodiodes which achieved a higher RF output power at high reverse bias [55].

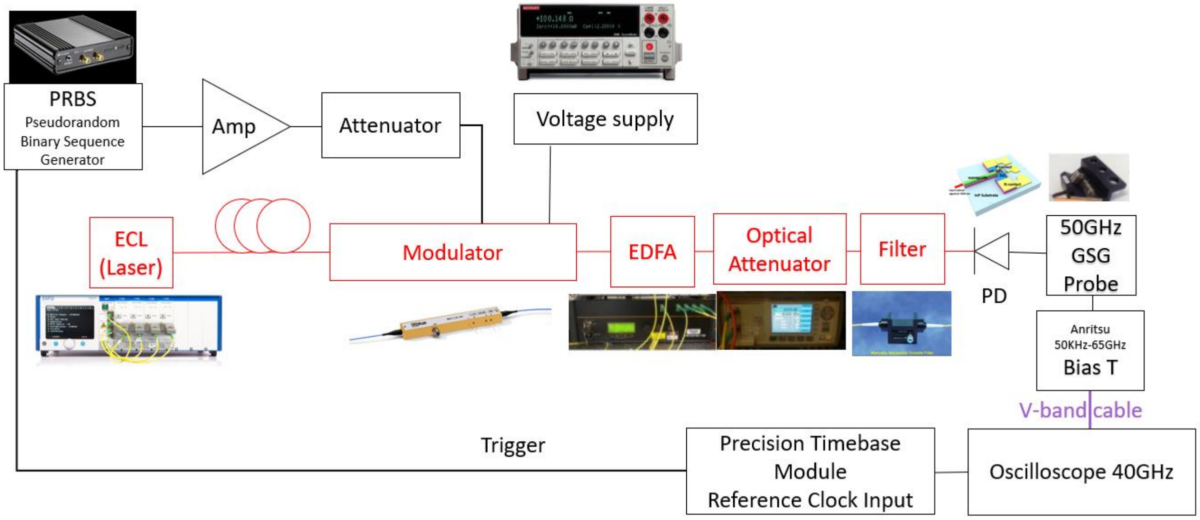


Figure 5-16. Experimental setup for eye diagram measurement.

5.4.6 Eye diagram

To evaluate our photodiodes for use in high-speed digital optical links we also measured the non-return-zero eye diagrams. Due to equipment limitations in our experiment, the highest

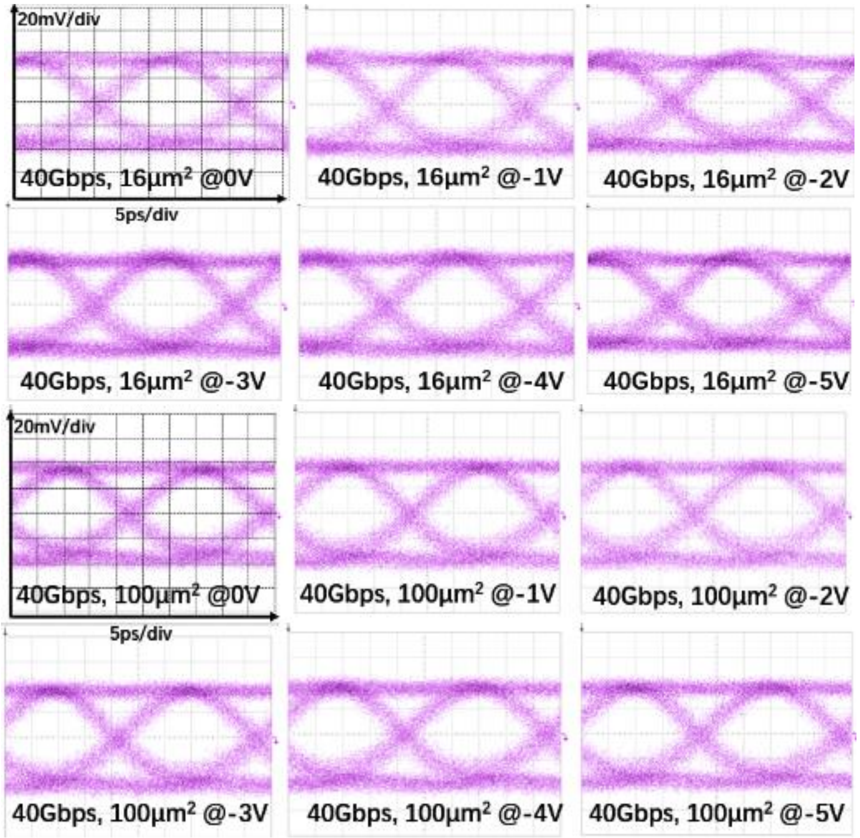


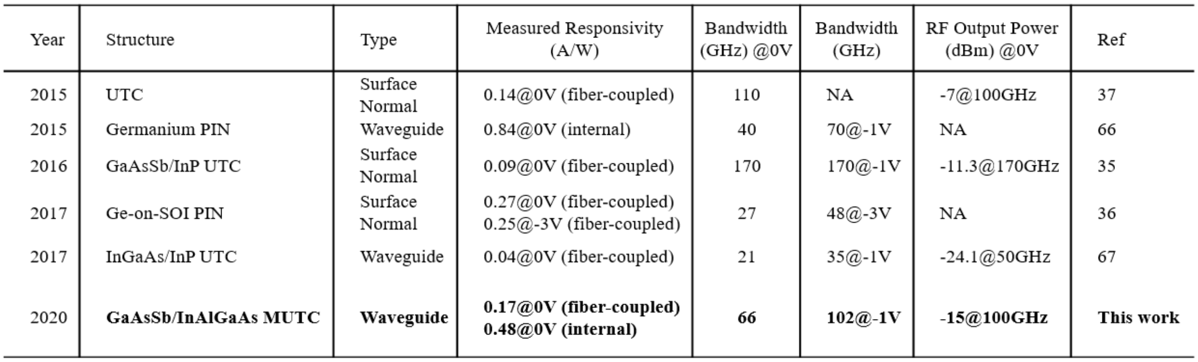
Figure 5-17. 40 Gbit/s eye diagrams of the 4×4 μm^2 and 5×20 μm^2 zero-bias waveguide PDs at 0, -1, -2, -3, -4, -5 V. (5 ps/div, 20 mV/div). (EDFA: Erbium-doped fiber amplifier)

available bit rate was 40 Gbit/s. We used a 40 Gbit/s pseudo random binary sequence generator and a 40+ Gbit/s Mach-Zehnder (MZ) modulator from EOspace as the signal source. An optical filter from OZ optics with full width at half maximum (FWHM) linewidth of 1 nm was used to ensure the wavelength of optical signal. Figure 5-16 shows the experimental setup for on-wafer measurements of eye diagrams. By using a commercial 40 Gbit/s $LiNbO_3$ modulator which was driven by a pseudorandom bit sequence (PRBS) generator to modulate 1550 nm light from an external cavity laser (ECL), an optical non-return-to-zero (NRZ) PRBS data pattern at 40 Gbit/s was formed. The PRBS optical signal with pattern length of 2^{31}-1 was delivered to the waveguide facet of our waveguide PDs. The 40 Gbit/s eye diagrams of the PDs with 16 μm^2 and 100 μm^2 active area at 0, -1, -2, -3, -4, and -5 V are shown in Figure 5-17. The extinction ratio was 4.8 dB. We observe widely open eye diagrams with a peak voltage of 80 mV at 40 Gbit/s at 0 V, indicating a high-quality data reception performance which is independent of the PD bias.

5.5 Summary

In this Chapter, a novel evanescently coupled waveguide type-II $GaAs_{0.5}Sb_{0.5}/In_{0.53}Al_yGa_{0.47-y}As$ MUTC photodiode with high bandwidth and high responsivity at zero bias was successfully demonstrated. At 0 V, the photodiodes achieved 66 GHz bandwidth, 0.48 A/W internal responsivity, and -15 dBm output power at 100 GHz. This performance is among the highest reported for all zero-bias photodiodes (Table IV) and, to the best of our knowledge, represents a new record for waveguide photodiodes.

Table IV Performance comparison for zero-bias photodiode



Year	Structure	Type	Measured Responsivity (A/W)	Bandwidth (GHz) @0V	Bandwidth (GHz)	RF Output Power (dBm) @0V	Ref
2015	UTC	Surface Normal	0.14@0V (fiber-coupled)	110	NA	-7@100GHz	37
2015	Germanium PIN	Waveguide	0.84@0V (internal)	40	70@-1V	NA	66
2016	GaAsSb/InP UTC	Surface Normal	0.09@0V (fiber-coupled)	170	170@-1V	-11.3@170GHz	35
2017	Ge-on-SOI PIN	Surface Normal	0.27@0V (fiber-coupled) 0.25@-3V (fiber-coupled)	27	48@-3V	NA	36
2017	InGaAs/InP UTC	Waveguide	0.04@0V (fiber-coupled)	21	35@-1V	-24.1@50GHz	67
2020	**GaAsSb/InAlGaAs MUTC**	**Waveguide**	**0.17@0V (fiber-coupled)** **0.48@0V (internal)**	**66**	**102@-1V**	**-15@100GHz**	**This work**

Chapter 6 High-power O-band Waveguide Photodiodes Integrated on Silicon Platform using Micro-transfer-printing

6.1 Introduction

As discussed in section 2.3, micro-transfer-printing technology has many advantages: suitable for high integration density, high efficiency of III-V material use, high throughput and low cost. In the past few years, several demonstrations of this technology have been reported, including transfer printed photodiodes [56-59], and lasers [60] [61], which show the potential of the technology. Compared to silicon-on-insulator waveguides, SiN waveguides have excellent properties such as low-loss, wide transparency window, and do not suffer from two-photon absorption at high optical power [62]. This gives silicon-nitride-based PICs the ability to handle much higher on-chip optical powers which is crucial for microwave photonics applications. Previously, a GaAs-based metal-semiconductor-metal photodetector on SiN waveguide layer with a bandwidth of 20 GHz at 850 nm was demonstrated by Guanyu, *et al.,* in 2018 [63]. And a GaAs p-i-n photodiode with responsivity of 0.3A/W at 850nm was demonstrated by Jeroen, *et al.,* in 2020 [57]. However, in these works the PD was transfer-printed on top of a silicon nitride grating coupler that redirects the light into the PD's absorber. This coupling method can limit the responsivity for high-speed PDs with very thin absorber.

To decouple the light-coupling efficiency from the active layer design of the PDs, here I present a MUTC PD with carefully, independently designed III-V waveguide which can facilitate efficient light coupling from the SiN waveguide into the III-V waveguide and the absorber of PD over a short length. This evanescent coupling design can potentially achieve higher power and better bandwidth-efficiency product since the PD and III-V waveguide can be optimized independently. On the other hand, to the best of our knowledge, very few demonstrations are geared toward detection at 1310 nm. Previously, I have demonstrated a high-power evanescently coupled waveguide integrated MUTC photodiode with 32 GHz bandwidth at -3 V for 1310 nm [64].

Based on the structure of this waveguide PD, in this chapter, I present a high-power waveguide MUTC photodiode on SiN/Si platform using micro-transfer-printing for 1310 nm. A 3-dB bandwidth of 54 GHz and dark current below 20 nA at -3 V have been measured for transfer printed PDs with an active area of 5×6 μm^2 under 1310 nm. Larger transfer printed PDs (7×15 μm^2) have 38 GHz bandwidth and an internal responsivity of 0.29 A/W at -3 V under 1310 nm.

6.2 Device Design and Fabrication

O-band high-speed MUTC waveguide photodiodes for transfer-printing were first fabricated on an InGaAs/InGaAsP/InP wafer. Fig 6-1 shows a schematic cross section of the epitaxial layer structure of the wafer before transfer-printing process, which was grown on semi-insulating InP substrate by LandMark using metal organic chemical vapor deposition and in situ-doped with zinc (p-type) and silicon (n-type) dopants [64]. The epitaxial layer design consists of four primary parts: a narrow-bandgap InGaAs absorber layer, a wide-bandgap InGaAsP drift layer, a non-intentionally doped (n.i.d) InGaAsP waveguide layer and an InAlAs release layer.

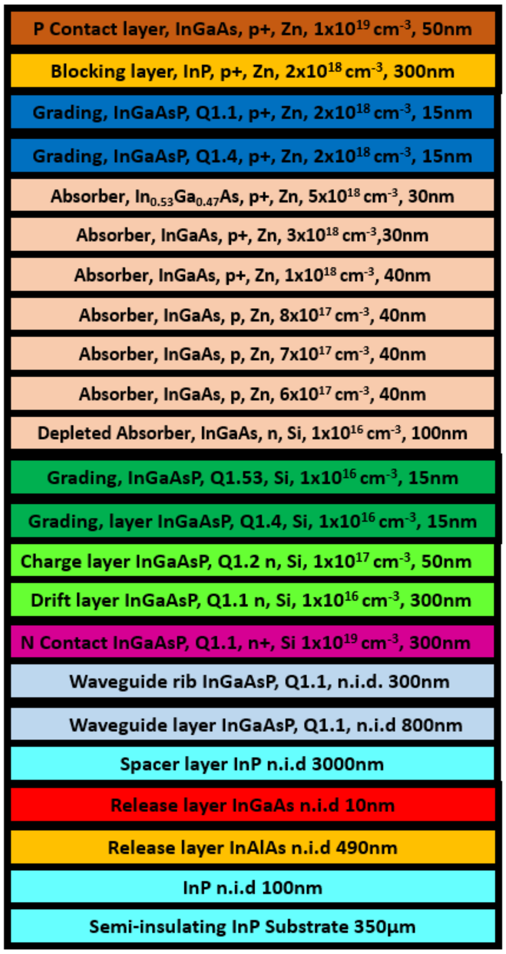


Figure 6-1. Details of epitaxial structure of PD. All layers are lattice-matched to InP.

As shown in Figure 6-1, a 490 nm InAlAs release layer was first deposited for the undercut etch to release the device coupon being transfer-printed on Si [65], followed by a 10 nm InGaAs layer as an etch-stop layer. Then, a 3 μm-thick n.i.d InP spacer layer was grown for a vertical match of the waveguides after transfer printing on the SiN platform. A 1.1 μm-thick n.i.d InGaAsP quaternary layer including 300 nm rib waveguide layer and 800 nm slab waveguide layer was deposited. The height, thickness and shape of the InGaAsP waveguide have been carefully simulated and designed for best light coupling efficiency between SiN waveguide and InGaAsP waveguide after transfer-printing to improve the responsivity of the PD. More details will be discussed in section 6.3. On top of the waveguide layer, a 300 nm-thick heavily n-type doped InGaAsP contact layer was deposited. A 300 nm-thick electron drift layer was grown with a light n-type doping ($1 \mathrm{x} 10^{16}$ cm^{-3}) for charge compensation and is followed by a 50 nm n-type doped ($1 \mathrm{x} 10^{17}$ cm^{-3}) charge layer. We have previously shown that this charge layer can help to reduce the deleterious effect of space charge at high photocurrents and thus increase the output power of the PD [49]. Between the InGaAsP drift layer and InGaAs light absorption layer, two 15 nm-thick lightly n-type doped InGaAsP layers were grown to suppress charge accumulation at the heterojunction interfaces. The InGaAs absorber layer includes a carefully designed 220 nm graded doping which results in a high built-in electric field for electron acceleration and a 100 nm depleted absorber to improve quantum efficiency [28]. Two 15 nm-thick InGaAsP layers and a 300 nm heavily p-type doped InP layer were deposited followed by a 50 nm-thick heavily p-type doped InGaAs contact layer to block electrons from diffusing to the p-type contact layer and to assist hole collection.

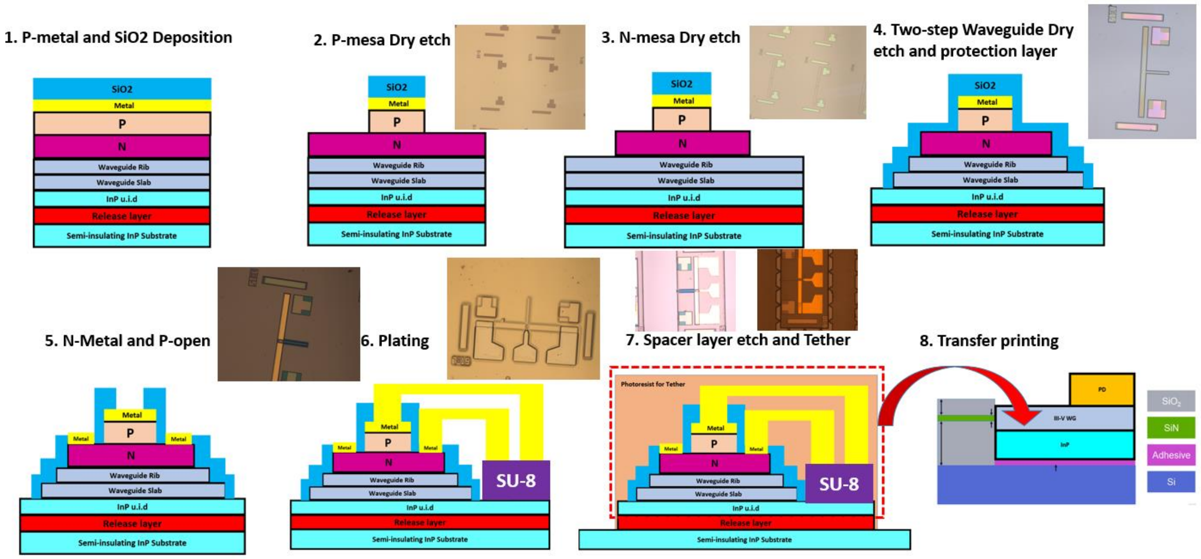


Figure 6-2. Schematic of fabrication process flow and micrographs of each step.

The process flow including cross section schematics and micrographs is shown in Figure 6-2. The first step of fabrication is p-metal deposition. After Ti/Pt/Au p-metal deposition, the first etch, which defined the p-mesa, stopped at the n-contact layer. The n-mesa was formed later by dry etching to the waveguide InGaAsP quaternary layer. Then, a double mesa process together with a rib waveguide dry-etching process were used to fabricate the waveguide PDs and define the waveguide facets. A 300-nm waveguide rib dry-etch and another 800 nm waveguide slab dry-etch was used to define the waveguide. To protect the sidewalls of the waveguide and the PD during release-layer etch, 300 nm SiO_2 was deposited as shown in Fig 6-2. AuGe/Ni/Au were deposited on the n-mesa for n-metal contacts. As shown in Fig 6-2 the photodiodes were connected to gold-plated coplanar waveguide (CPW) RF pads through an air-bridge. To avoid surface leakage current and dielectric loss in the n.i.d InP, a 2-µm SU-8 layer was added between CPW pads and n.i.d InP layer.

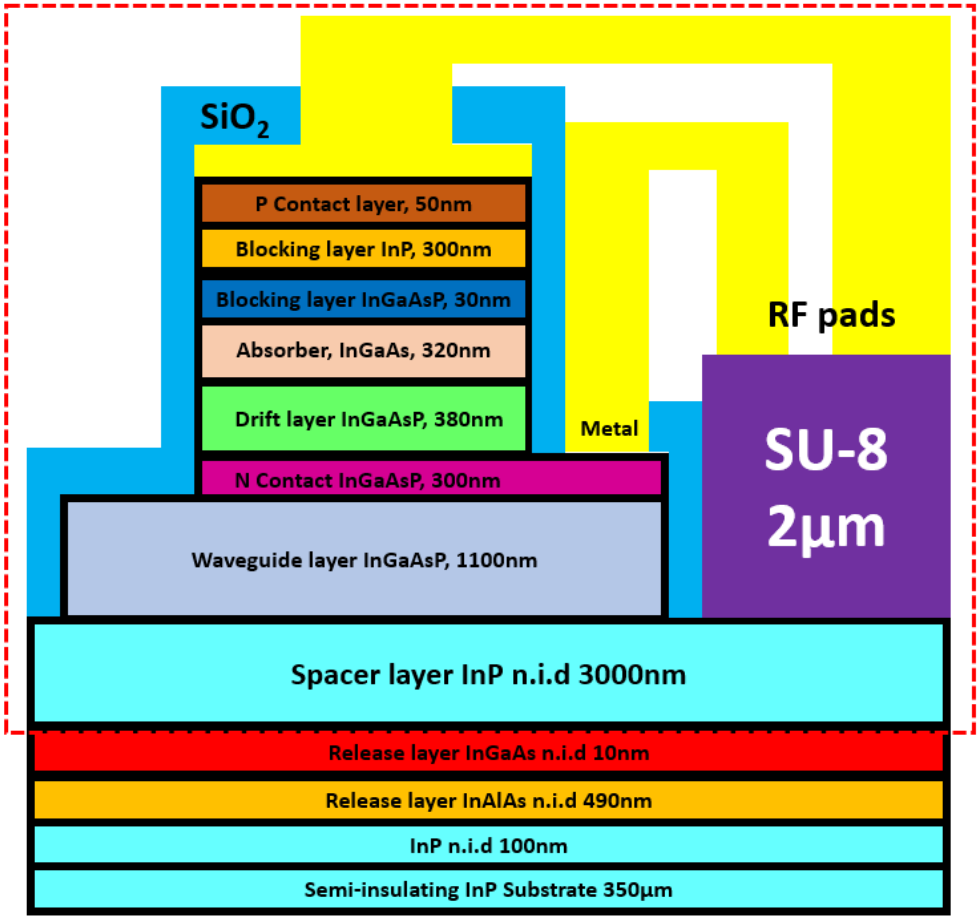


Figure 6-3. Cross-sectional view of PD before transfer-printing.

After the fabrication process of the waveguide PD on the source wafer, the cross-sectional view of PD before transfer-printing is shown in Figure 6-3.

Figure 6-4 shows the fabrication steps related to micro-transfer-printing. To make the PDs printable, I defined 300 µm × 600 µm coupons by dry-etching through the 3 µm n.i.d InP layer and the InAlAs release layer to reach the InP substrate. Next, the devices are encapsulated with ~5.5 µm thick photoresist as tether structures that will anchor the devices to the InP substrate during the

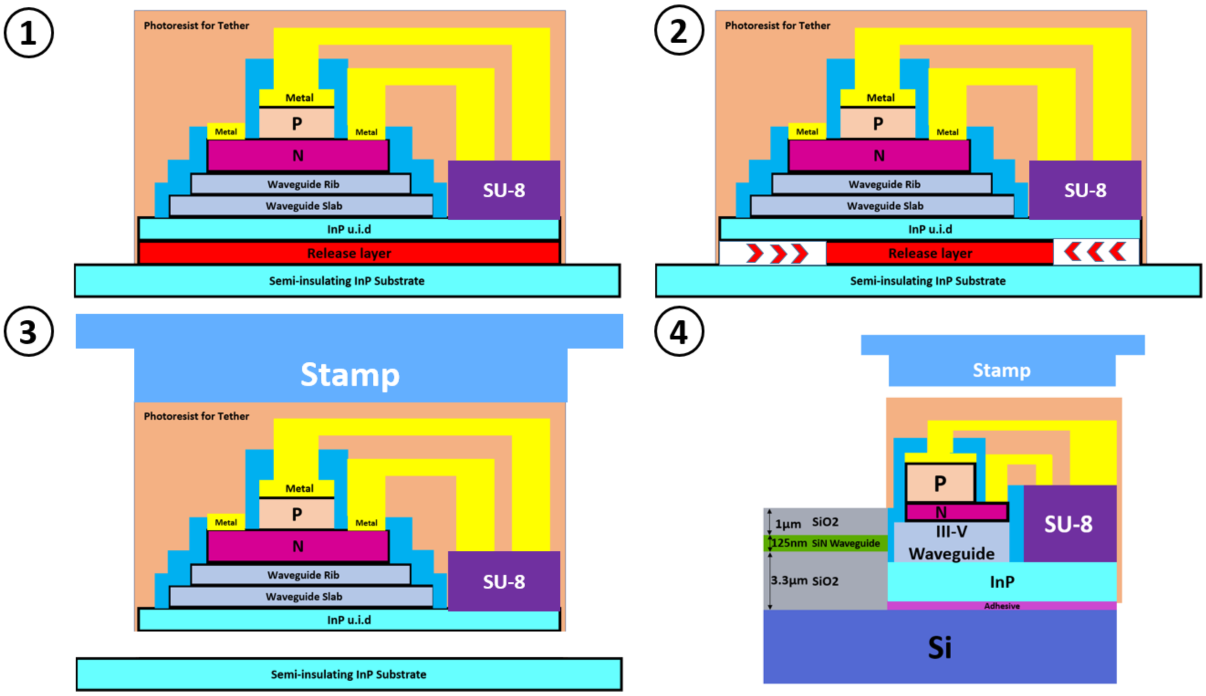


Figure 6-4. Cross-sectional views of PD during transfer-printing.

release process while at the same time exposing the InAlAs release layer. The thick photoresist also protects the III-V waveguide facet during transfer-printing. Finally, the devices are released from the InP substrate by underetching the InAlAs release layer and then print into blank chiplet pockets on the Si wafer with SiN waveguide. More details about III-V device transfer printing development can be found in [56], [61] and [65].

Fig 6-5 shows the cross-sectional views of the PD after transfer-printing process. Figure 6-6 shows the top-view microscope image of a fabricated waveguide PD which has been transfer printed successfully onto the SiN platform. The III-V waveguide facet and SiN waveguide should be aligned as shown in Figure 6-6 for the best light coupling. After all the fabrication processes, the Si-based wafer was diced to expose the SiN waveguide facets for light input coupling. Details and recipe of fabrication are in Appendix I.

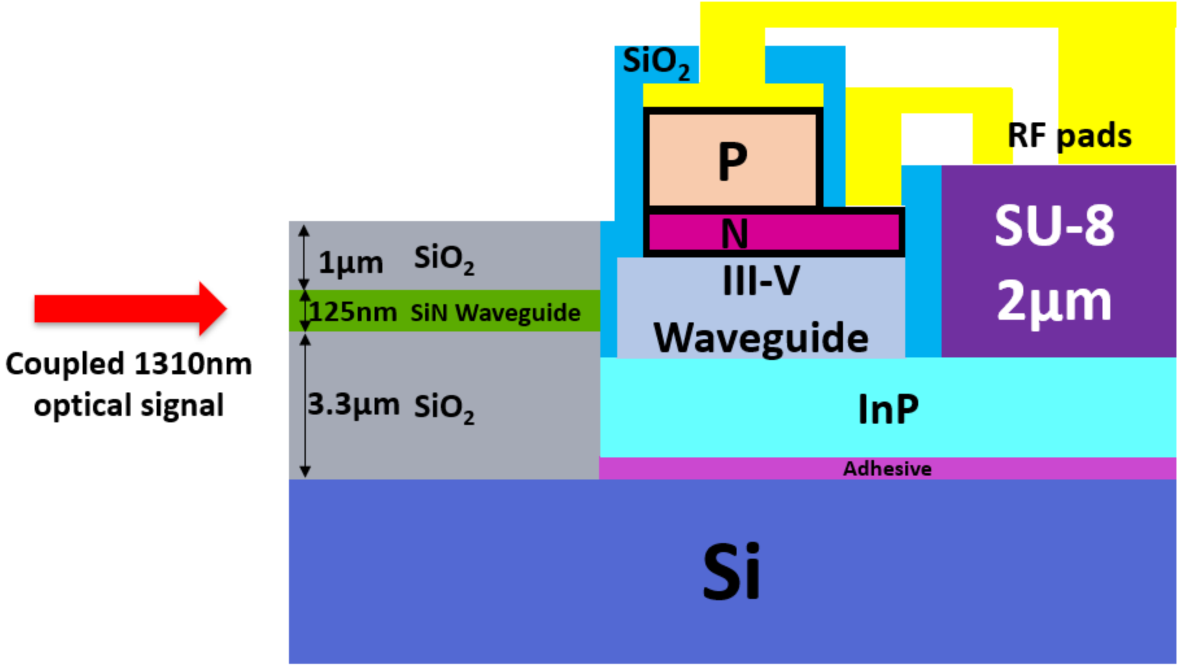


Figure 6-5. Cross-sectional view of PD after transfer-printing.

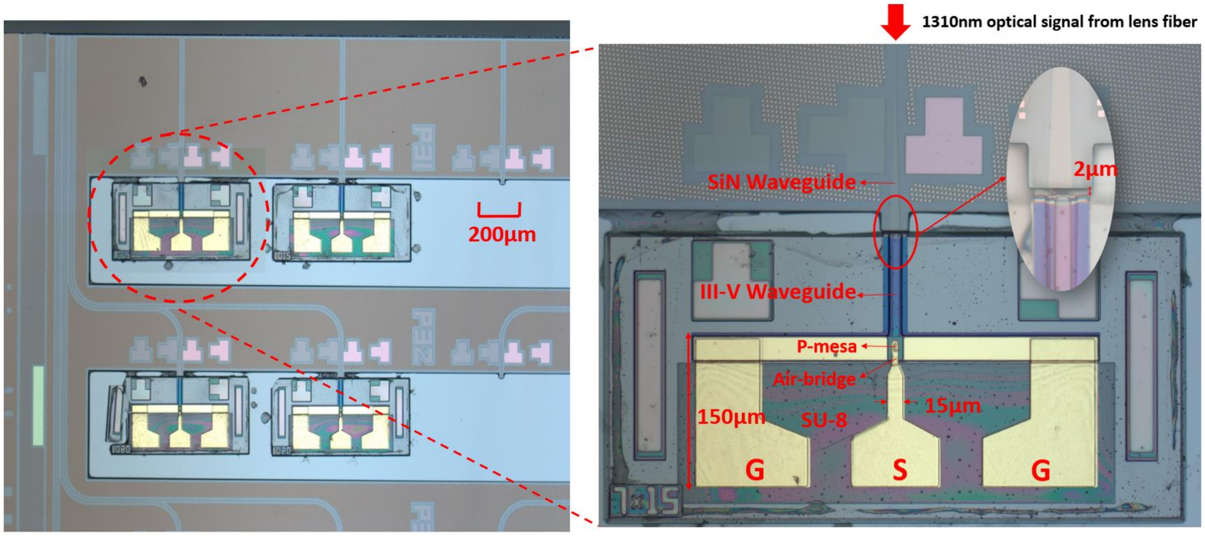


Figure 6-6. Micrographs of the transfer-printed waveguide PDs and SiN waveguides.

6.3 Waveguide Design and Protection

To achieve the best responsivity of the transfer-printed waveguide photodiode, one key point of the design is to minimize the coupling loss between the SiN waveguide and III-V waveguide. A commercial software named FIMMWAVE was used for the optical simulation of coupling loss between these two waveguides. Figure 6-7 shows the 3-D schematic of the model and the refractive index I used in simulation at 1310 nm.

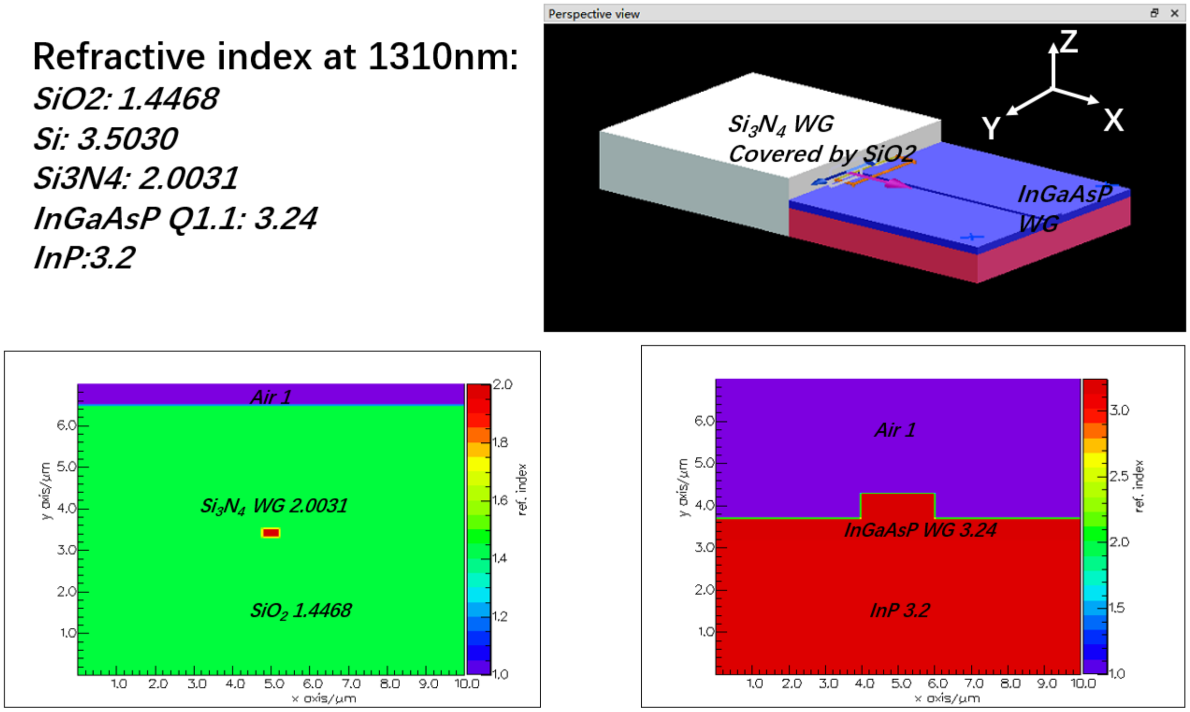
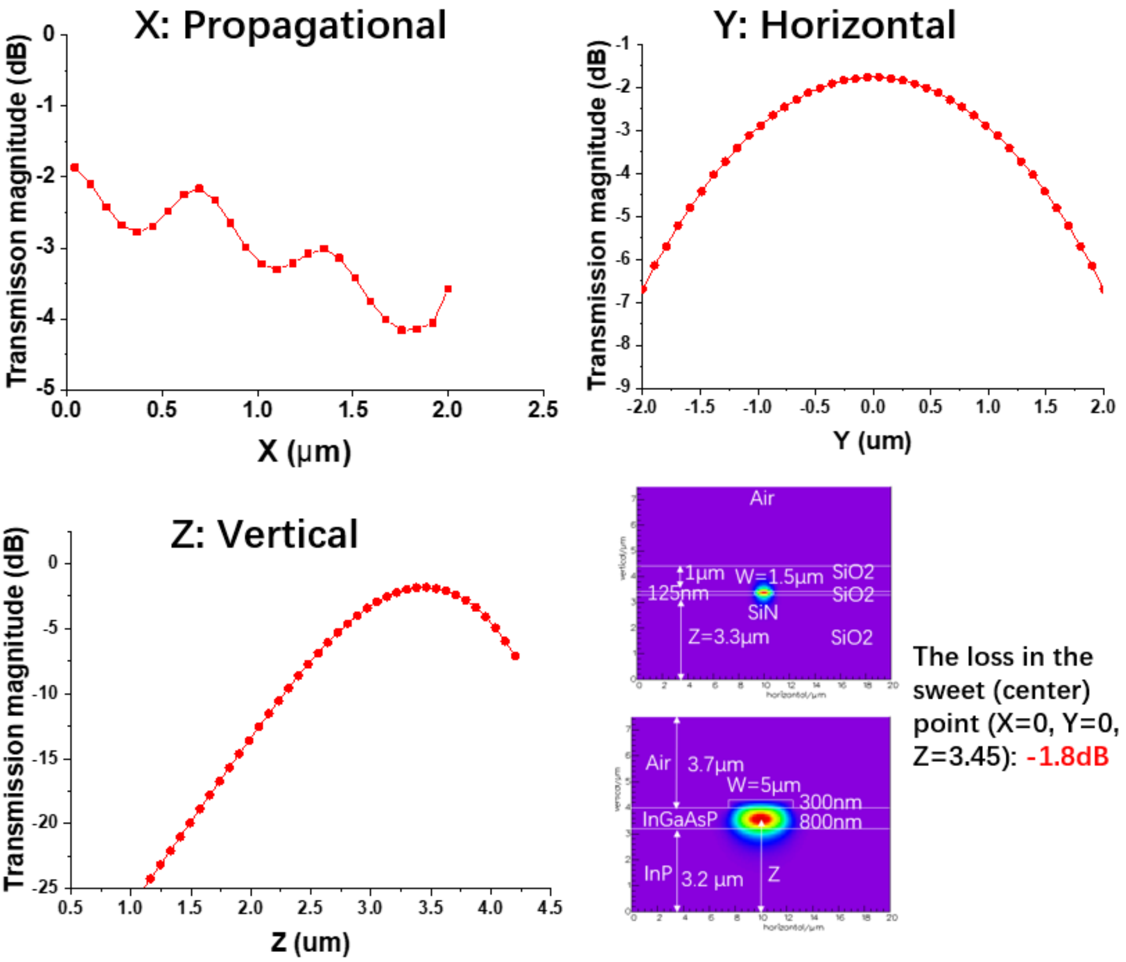


Figure 6-7. 3-D schematic of the simulation model and the refractive indices in SiN waveguide and III-V waveguide.

I aligned the center of optical modes in the SiN waveguide and III-V waveguide at the same location to get the sweet spot for smallest mode mismatch and lowest coupling loss. While fixing the shape of SiN waveguide (thickness times width, 0.125×1.5 μm^2), the shape of the III-V waveguide can be optimized for best light coupling efficiency by sweeping the width and thickness of rib waveguide and slab waveguide. The optimization results were shown in the right bottom of

Figure 6-8. According to the simulation, at the sweet spot, the estimated coupling loss between SiN waveguide and III-V waveguide is 1.8 dB due to mode mismatching (X=0, Y=0, Z=3.45 µm).



The loss in the sweet (center) point (X=0, Y=0, Z=3.45): -1.8dB

Figure 6-8. Optical simulation results of coupling loss between III-V and SiN waveguide and misalignment tolerance in three directions.

During the transfer-printing process, misalignment can happen. Thus I also simulated the misalignment tolerances in three directions for coupling loss, which is shown in Figure 6-8. The fundamental TE modes in the two waveguides are also shown in the bottom left of this figure. X, Y and Z present the misalignment during micro-transfer-printing processes in propagational, horizontal and vertical direction. In the X direction plot, if there is a 2 µm air gap between SiN waveguide and III-V waveguide, the coupling loss would be increased to 4 dB.

Besides the coupling loss simulation, I also simulate the light absorption efficiency in the III-V waveguide-photodiode structure to estimate the internal responsivity of this waveguide photodiode at 1310nm. In the simulation, a metal on the top of mesa was included. The absorption coefficient and refractive index of the absorber is 15000 cm^{-1} and 3.55. The refractive indices of InP and InGaAsP are shown in Figure 6-7. Figure 6-9 shows the optical simulation results including light absorption versus transmission length and the optical mode in the III-V waveguide and waveguide-PD structure. Based on the simulation result this waveguide photodiode should have 55% internal quantum efficiency and internal responsivity of 0.58 A/W when the length of PD is 15 μm at 1310 nm.

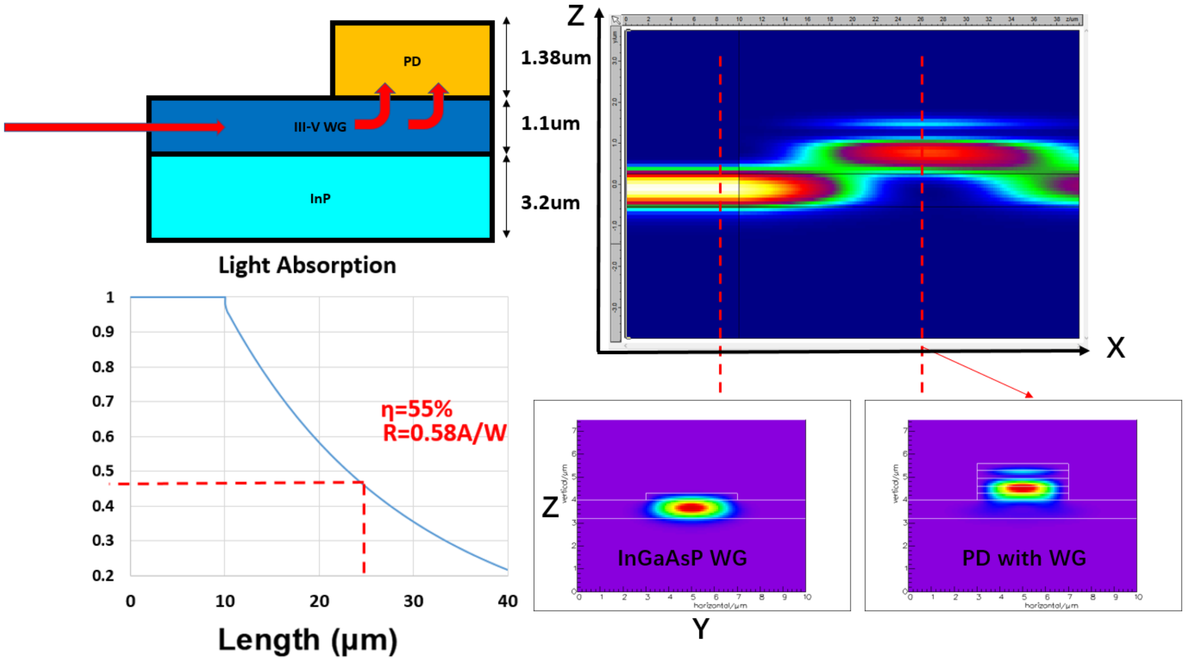


Figure 6-9. Optical simulation results of light absorption in waveguide-PD structure.

During the fabrication processes, the III-V waveguide and especially its facet for light coupling needs to be protected to avoid under-cut etch. The under-cut etch can happen during a wet etch of the spacer layer and release layer etch. It will damage the facet of the waveguide so that nearly no light can be coupled into the III-V waveguide after transfer-printing even if there is no misalignment between waveguides. To protect the facet of the III-V waveguide, first I chose to deposit SiO_2 on both waveguide rib and slab as hard mask for dry etching the waveguide structure. Second, after waveguide etch, a 300 nm SiO_2 was deposited again as the protection layer to further protect the sidewall facet of the waveguide. Third, I choose dry etch for the whole spacer layer etch step to avoid the under-cut etch. Finally, after spacer layer etch when coating the tether on the photodiode, on the waveguide side the tether area is a little bit larger (1 μm) than the edge area of III-V waveguide. Thus the tether covers the sidewall of the waveguide and can further protect the waveguide facet during the release layer etch step. Figure 6-10 shows the waveguide facet changes during the whole fabrication processes.

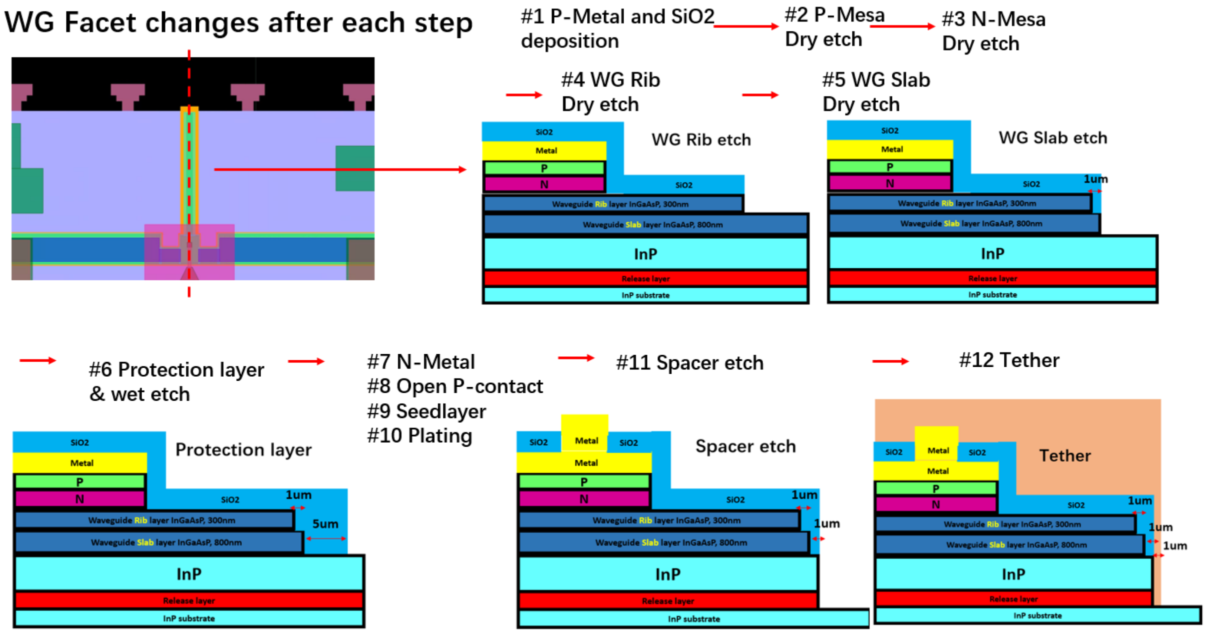


Figure 6-10. The waveguide facet changes during the whole fabrication processes.

6.4 Bar-level PD Characterization

Bar-level PD means here that the photodiode fabrication stops before the spacer etch step on the III-V substrate. Bar-level PDs have the same mesa structure, RF pads and waveguide size as the transfer-printed waveguide PD. I fabricated the bar-level PDs and characterized them first before fabricating the transfer-printed PDs. After all the fabrication processes in section 6.2 except for the process of SU-8, spacer etch, tether and transfer printing, the InP-based wafer was cleaved

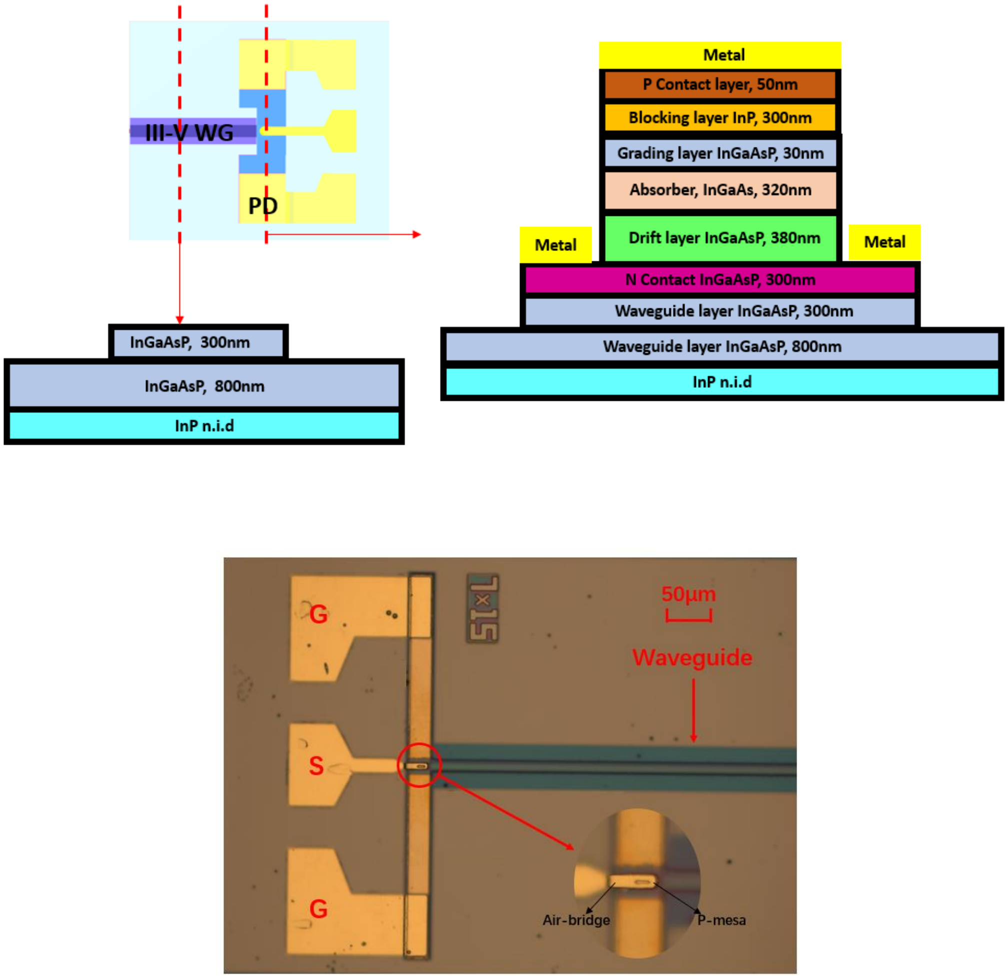


Figure 6-11. Cross sections of the bar-level waveguide PD and the top-view micrograph of a fabricated bar-level waveguide PD.

to expose the SiN waveguide facets for light input coupling. Figure 6-11 shows the cross sections of the bar-level waveguide PD and top-view micrograph of a fabricated bar-level waveguide PD.

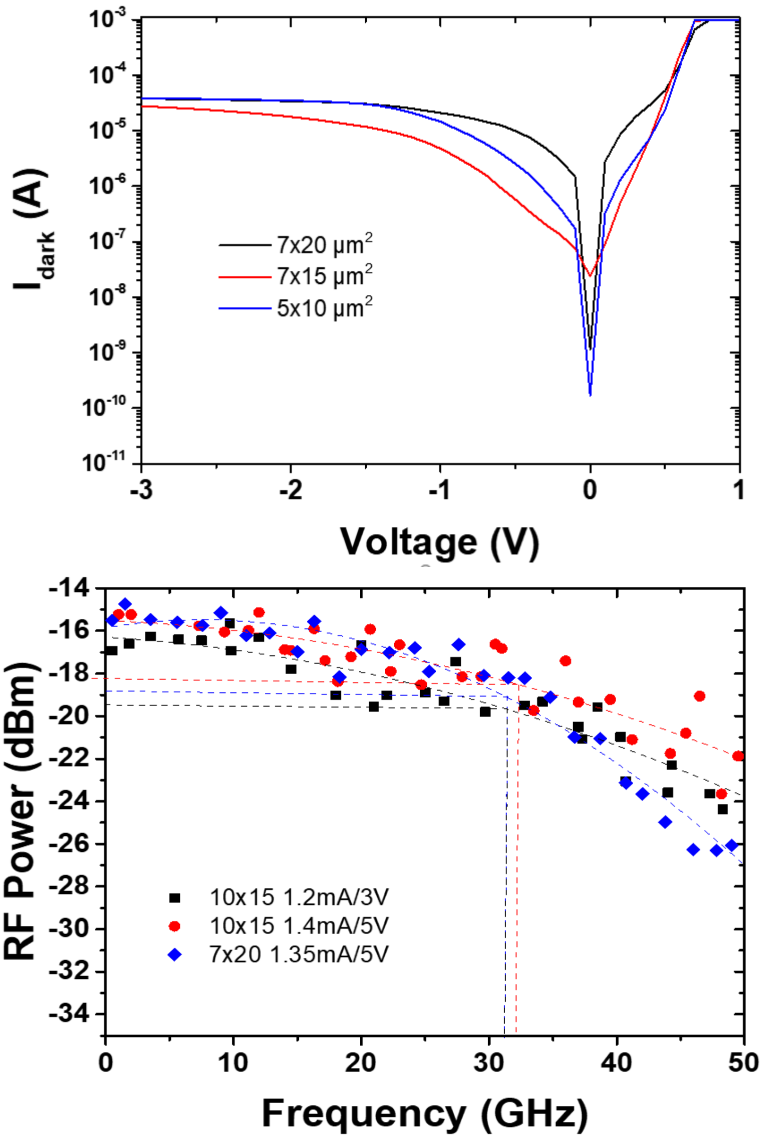


Figure 6-12. Measured I-V curves and frequency responses at 1310 nm of bar-level waveguide PDs with different areas.

The dark current of the bar-level PDs with RF pads is shown in Figure 6-12. It is obvious that there is a large leakage current which indicates that the background doping level of the n.i.d InP (~ 10^{15}cm^{-3}) is not sufficient for pad insulation as it is much higher than semi-insulating Fe-doped substrate which is what I usually use for high-speed PDs. This was confirmed by dark current measurements on simple mesa PDs without RF pads on the same wafer which showed low dark currents below 500 nA at -5 V. In order to improve the bandwidth of the 1310 nm waveguide PDs, I added a SU-8 layer between to avoid this high leakage current and capacitance between CPW pads and n.i.d InP layer for transfer-printed PDs. The improved dark current is shown in Figure 6-14. It should be mentioned that an epitaxially grown semi-insulating InP spacer layer can be used, too, however, S.I. epi layers are less available and were not provided by our commercial crystal growers.

The external (fiber-coupled) responsivities of bar-level PDs were measured using a single-mode tapered optical fiber for input coupling and include the fiber-chip mode mismatch loss and the reflection loss at the photodiode waveguide facet (no anti-reflection coating was used). The external responsivity of bar-level waveguide PD with an active area of 10×15 μm^2 was 0.28 A/W. In order to determine the internal responsivity, the coupling loss between the tapered fiber and the waveguide was estimated using a commercial software. Assuming a mode mismatch loss of 3 dB and 1.4 dB reflection loss at the waveguide facet, the internal responsivity is estimated to be as high as 0.77 A/W which corresponds to an external quantum efficiency of 72 % at the 1310 nm wavelength.

The frequency responses of bar-level waveguide PDs with various active areas are shown in Figure 6-12. Waveguide photodiodes with active areas of 7×20 μm^2 and 10×15 μm^2 had bandwidths of 31 GHz and 32 GHz at -5 V, respectively. Also, the 10×15 μm^2 PD reached its maximum bandwidth of 31 GHz at -3 V which indicates that the drift layer can be fully depleted at this voltage.

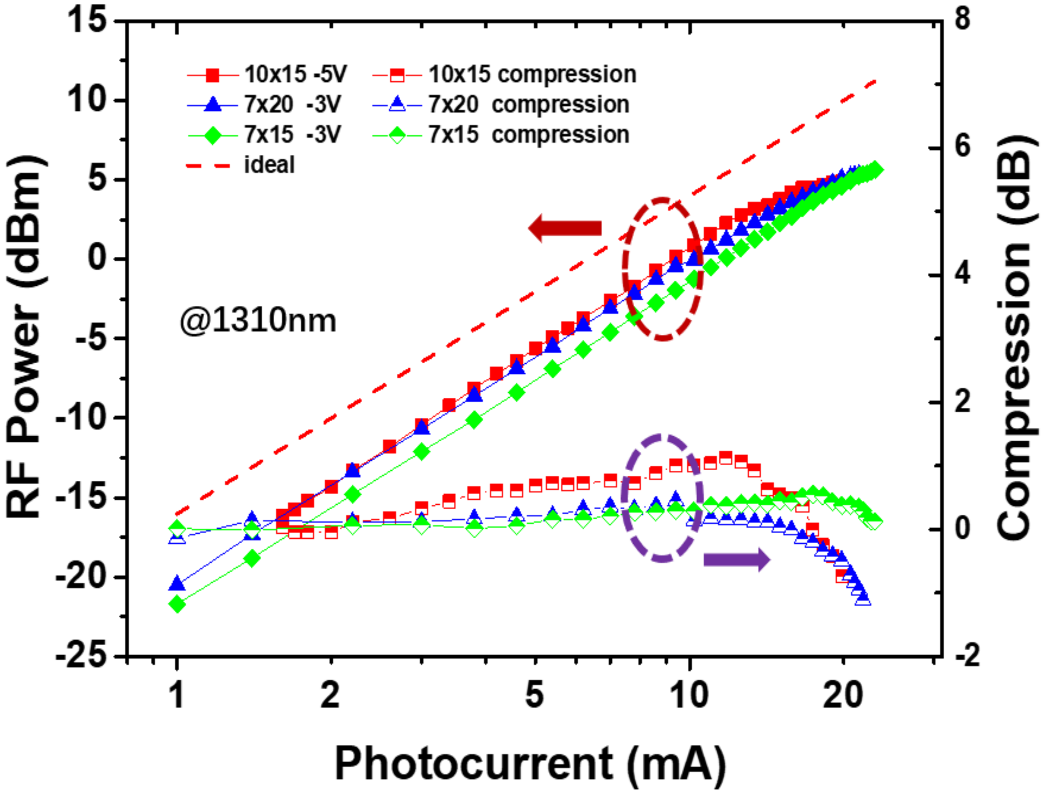


Figure 6-13. RF output power and RF power compression versus average photocurrent at 30 GHz. The dashed line represents the ideal RF power at 50 Ω.

As shown in Figure 6-13, the RF saturation was characterized by measuring the RF output power as a function of the average photocurrent at 30 GHz. The output RF power increases super-linearly with increasing photocurrent before it begins to saturate. Same as section 3.3.5, the saturation current as the photocurrent was defined where the RF power compression curve drops by 1 dB from its peak value. At -5 V, waveguide PDs with an active area of 10×15 μm^2 achieved

4.9 dBm output power and the saturation current was 19.8 mA. Waveguide PDs with 7×15 μm^2 and 7×20 μm^2 reached 5.7 dBm at 23 mA and 5.3 dBm at 21.3 mA, respectively. It should be noted that these PDs were not yet fully saturated and achieved high RF output power at a reverse of only -3 V bias.

6.5 Transfer-printed waveguide PD Characterization

6.5.1 Current-Voltage and Capacitance-Voltage

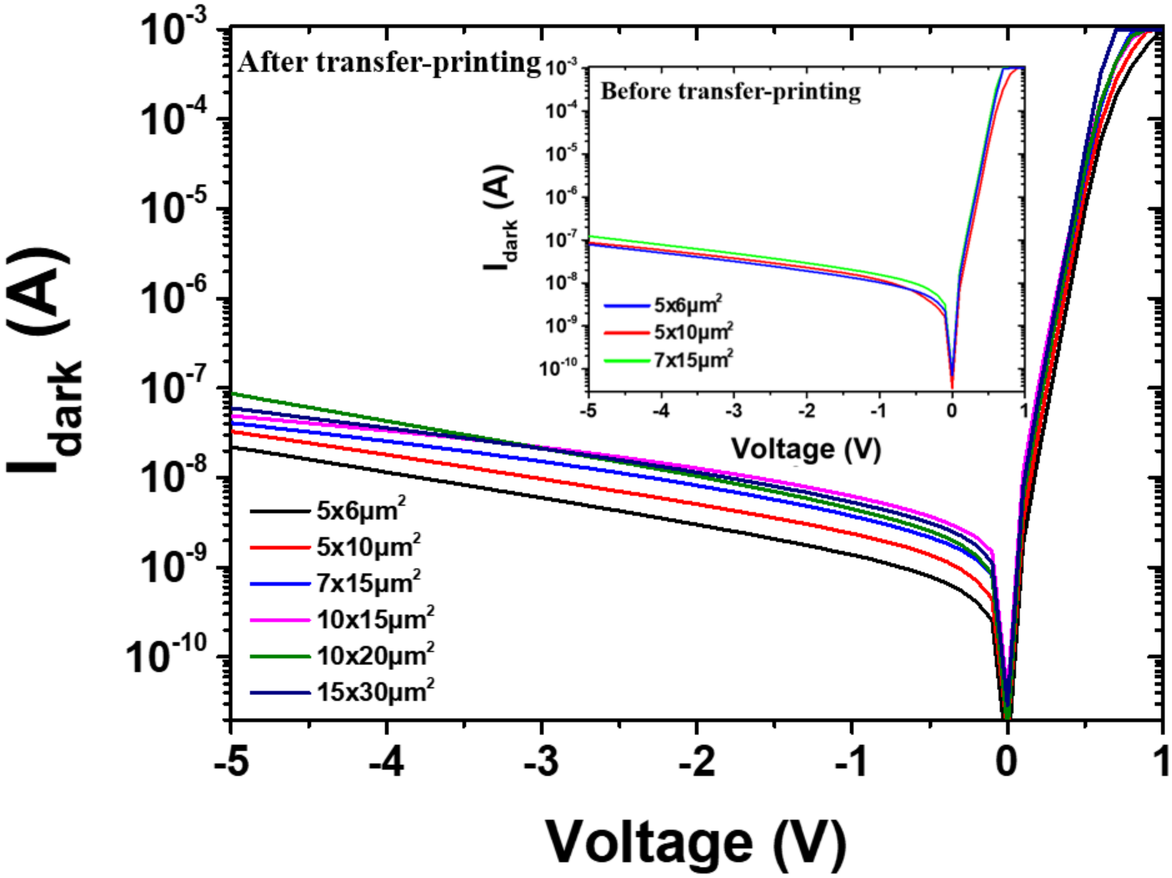


Figure 6-14. Dark current versus voltage before and after transfer-printing.

O-band MUTC waveguide PDs with active areas from 30 μm^2 (5×6 μm^2) to 400 μm^2 (15×30 μm^2) were fabricated on InP substrate and transfer printed on SiN platform. As shown in Figure 6-14, the dark current versus voltage curves were measured before and after transfer-printing. The dark current is almost unchanged after transfer-printing which indicates that the process does not degrade the performance. After transfer printing, all PDs have a very low dark current below 20 nA at -3 V and the smallest PD (5×6 μm^2) has a dark current of only 6 nA at -3 V, which indicates that surface leakage has been successfully eliminated due to the newly introduced SU8 layer.

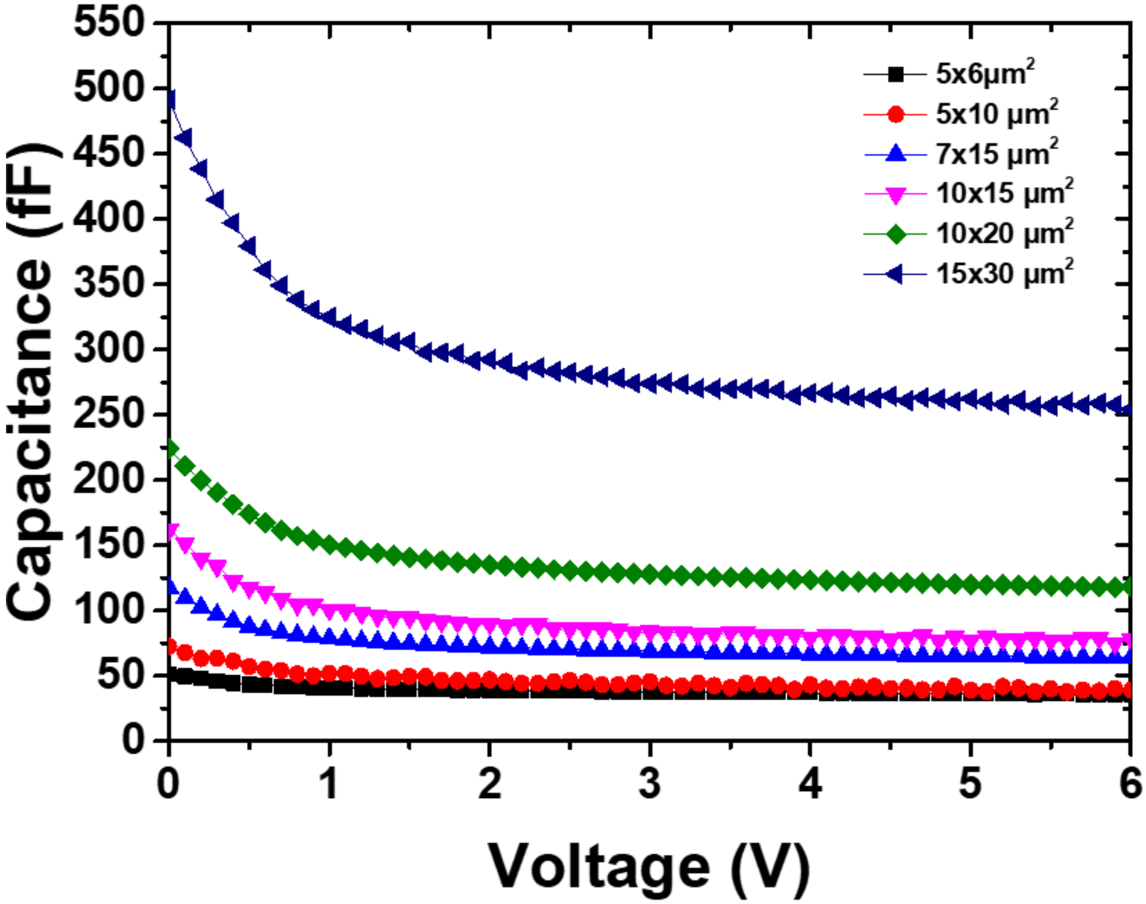


Figure 6-15. Measured capacitance versus bias voltage.

The total capacitance C_{total} of different sized PDs were measured by using an LCR meter and the results are shown in Figure 6-15. The capacitance depends slightly on bias when the reverse voltage is larger 3 V which indicates that our PDs are approaching full depletion at -3V. The blue squares in Figure 6-16 show the measured capacitance at -3 V, and as expected, a linear relationship between C_{total} and the PD area can be seen. The blue dashed line shows the linear fitting curve of measured total capacitance in Figure 6-16. At the intercept we find a capacitance of 13 fF that can be attributed to some parasitic.

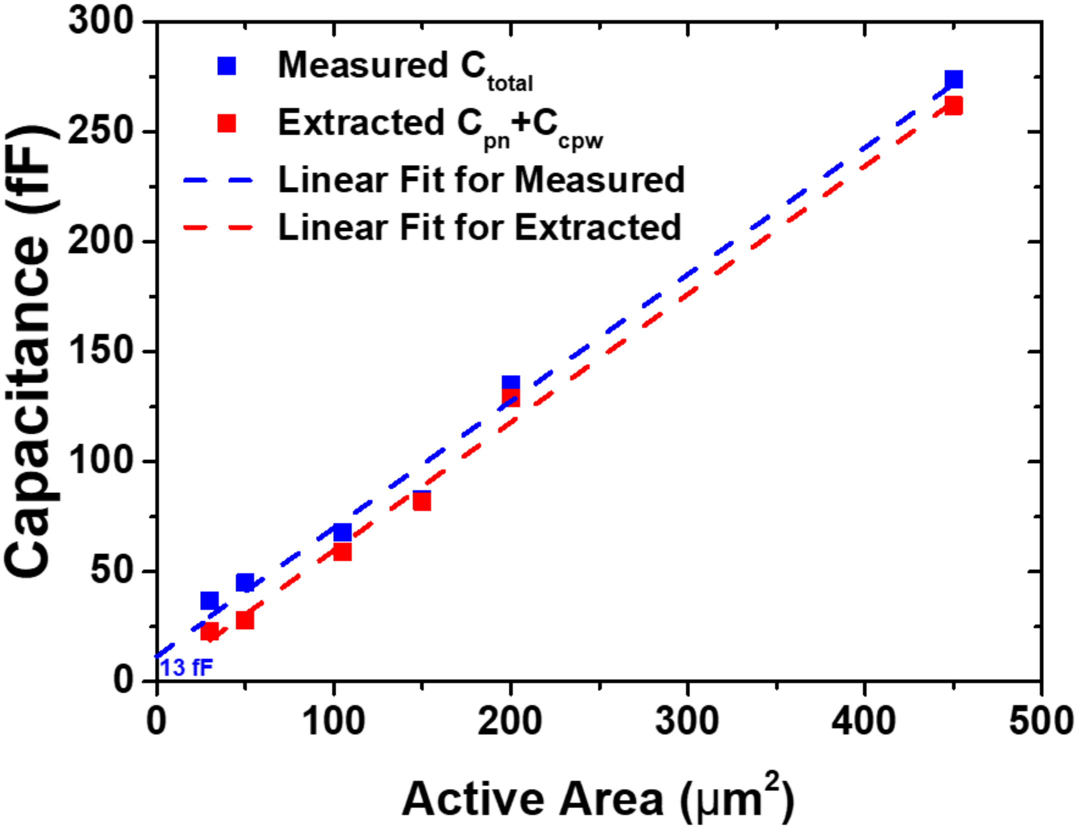


Figure 6-16. Measured capacitance versus voltage.

6.5.2 S-Parameter Measurement

I measured the scattering parameter S11 of the PDs up to 50 GHz at -3 V by using a vector network analyzer. The results are shown as red lines in Figure 6-17(a). In order to estimate the frequency response of our devices, a simple photodiode equivalent circuit model (Figure 6-17(b)) was used to extract the circuit elements through S11 fitting using Advanced Design System (ADS).

C_{pd}, C_{cpw}, R_s, R_j, L_{cpw} and R_{load} represent the junction capacitance of PD, capacitance of the CPW pads, series resistance, junction resistance, inductance of the CPW pads, and load resistance, respectively.

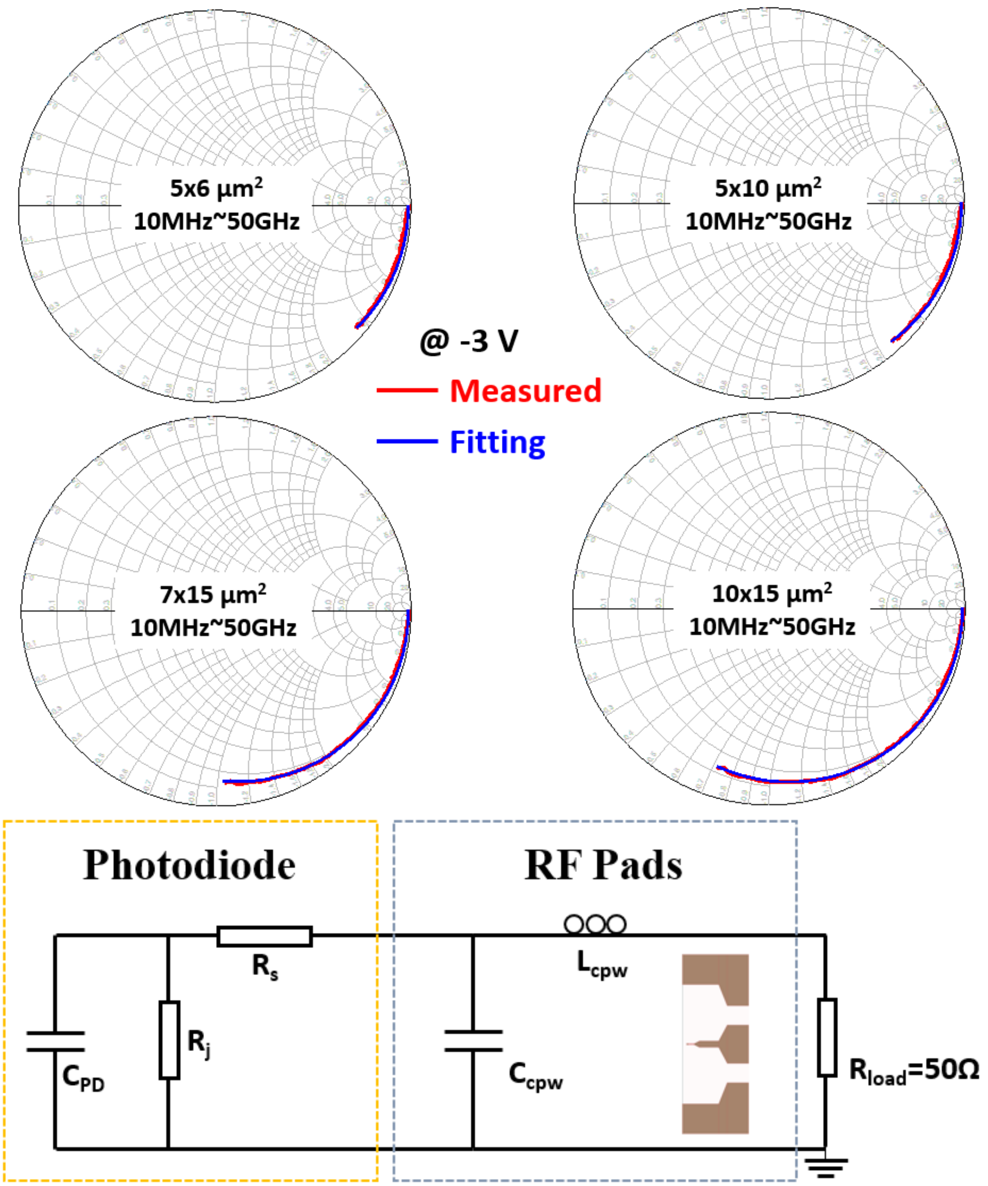
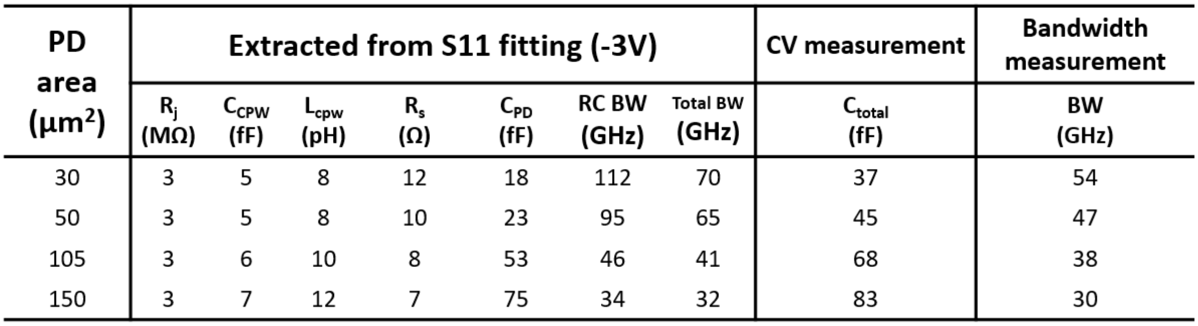


Figure 6-17. (a) Measured (red line) and fitted (blue line) S11 data for devices with active areas of 30 μm^2, 50 μm^2, 105 μm^2, and 150 μm^2. (b) Circuit model of the waveguide PDs for S11 fitting.

In Figure 6-17(a), the fitting curves (blue lines) and measured S11 (red lines) for four PDs with different areas coincide very well on the Smith Charts. Table V summarizes the extracted circuit elements at -3 V from ADS and the measured total capacitance for different PD active areas. We found a good agreement between the measured and extracted values of the capacitance, which is also shown in Fig. 6-16. We attribute the value difference between measured (blue) and extracted (red) capacitance to the parasitic capacitance. From Table V, we also found that R_s does not significantly scale with the PD's active area, which indicates a small p-contact resistance and that the bulk resistance dominates. Note that the extracted inductances and capacitance of the CPW pads, L_{cpw} and C_{cpw}, vary a little with the PD area as the size of the RF pads was optimized for each device.

Table V Extracted and measured parameters of transfer-printed waveguide PDs

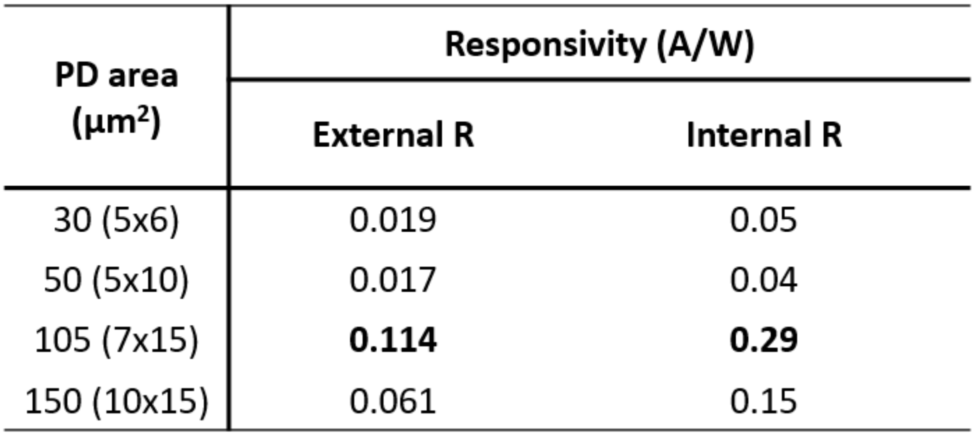


PD area (μm^2)	Extracted from S11 fitting (-3V)							CV measurement	Bandwidth measurement
	R_j (MΩ)	C_{CPW} (fF)	L_{cpw} (pH)	R_s (Ω)	C_{PD} (fF)	RC BW (GHz)	Total BW (GHz)	C_{total} (fF)	BW (GHz)
30	3	5	8	12	18	112	70	37	54
50	3	5	8	10	23	95	65	45	47
105	3	6	10	8	53	46	41	68	38
150	3	7	12	7	75	34	32	83	30

6.5.3 Responsivity

The responsivities of the waveguide PDs with different sizes were measured at 1310 nm wavelength at -3 V and the external responsivities are listed in Table VI. The external (fiber-coupled) responsivities were directly measured using a single-mode tapered optical lensed fiber. First, the 1310 nm light coming out of lens fiber was coupled into SiN waveguide. Then the light is guided by the SiN waveguide into the III-V waveguide and is finally absorbed by the PD.

Table VI Responsivity summary of transfer-printed waveguide PDs



PD area (μm^2)	Responsivity (A/W)	
	External R	Internal R
30 (5x6)	0.019	0.05
50 (5x10)	0.017	0.04
105 (7x15)	**0.114**	**0.29**
150 (10x15)	0.061	0.15

The total coupling losses mainly consist of the fiber-chip coupling loss between lensed fiber and the facet of SiN waveguide and the losses coming from the interface of the SiN waveguide and the III-V waveguide. We measured the coupling loss between lensed fiber and facet of SiN waveguide by using fiber-in & fiber-out method on a passive SiN waveguide. And the coupling loss between lensed fiber and facet of SiN waveguide was 4 dB. As mentioned in section 6.3, at the optimum, the coupling loss is 1.8 dB due to mode mismatch and light reflection (sweet point). After taking into account the 4 dB fiber-SiN coupling loss, the internal responsivities of waveguide PDs with different areas are listed in Table II. The best internal responsivity we've measured is 0.29 A/W from one of 7×15 μm^2 PDs at 1301 nm, which is very close to what we simulated (0.38 A/W) in FIMMWAVE (shown in Figure 6-18). In Figure 6-18, the differences of internal responsivity between the simulated results and measured results come from the visible misalignment and the narrow SiN waveguide at interface.

Due to the slight misalignment of each waveguide PD during micro-transfer-printing process, the responsivities of PDs with different sizes don't strictly depend on the length of PDs. As we sweep the wavelength of the input optical signal, the responsivities change and the average wavelength dependent loss (ratio of the maximum and minimum responsivity for the two wavelength) of 1.7 dB is estimated. It can be attributed to the gap between SiN waveguide and III-V waveguide caused by the misalignment during micro-transfer-printing. We also found that the responsivity changes while changing the polarization which can be attributed to the small size (0.125×1.5 μm^2) of the SiN waveguide (supports only fundamental TE mode), which however, does not present a major drawback for applications. I've tried adding a fluid with 1.5 refractive index in the gap between SiN waveguide and III-V waveguide. However, there was no significant improvement. Potentially a fluid with larger index can help reduce the coupling loss between these two waveguides.

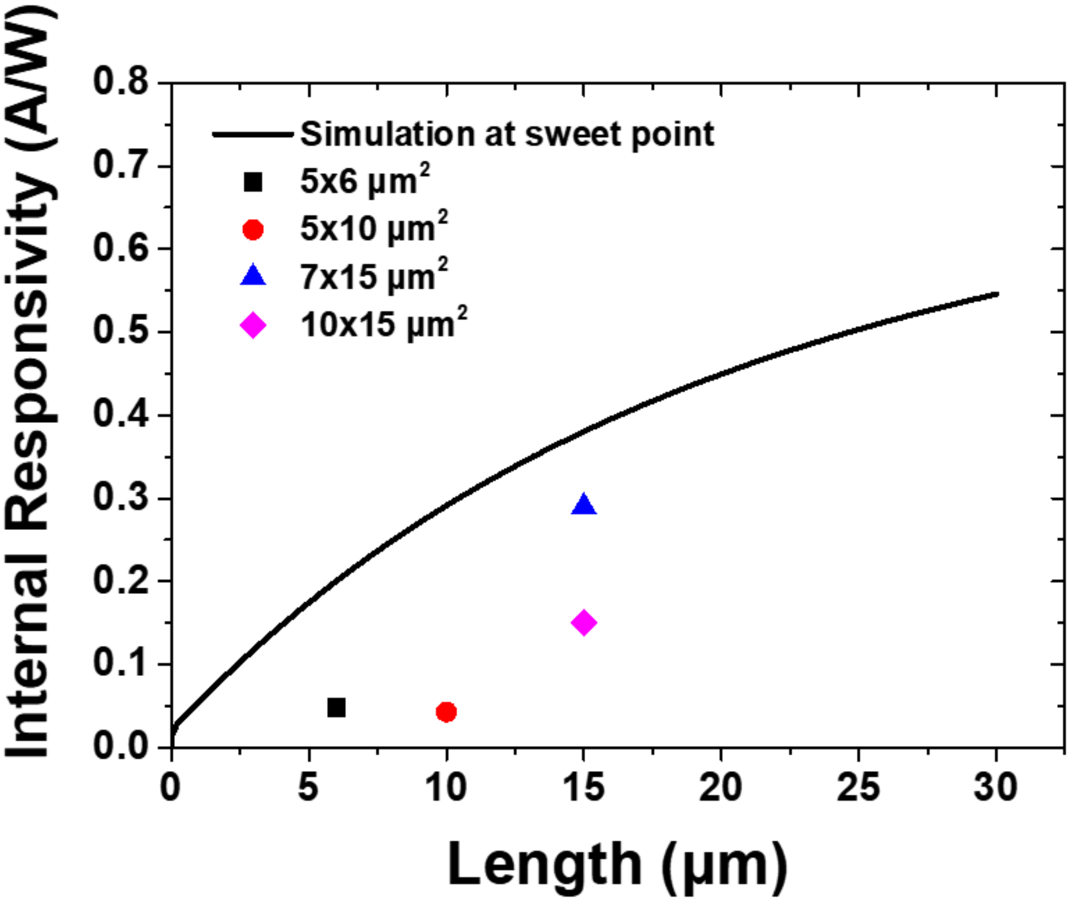


Figure 6-18. Simulated and measured quantum efficiency.

6.5.4 Frequency Response

Bandwidth and saturation characteristics were measured by using an optical heterodyne setup. Light with a wavelength near 1310 nm from two external cavity lasers was heterodyned to generate an optical signal with a modulation depth close to 100 %. The frequency of the beat signal was controlled by tuning the wavelength of one laser. The optical signal is amplified by a praseodymium-doped fiber amplifier (PDFA). The max output power of the PDFA is 22 dBm.

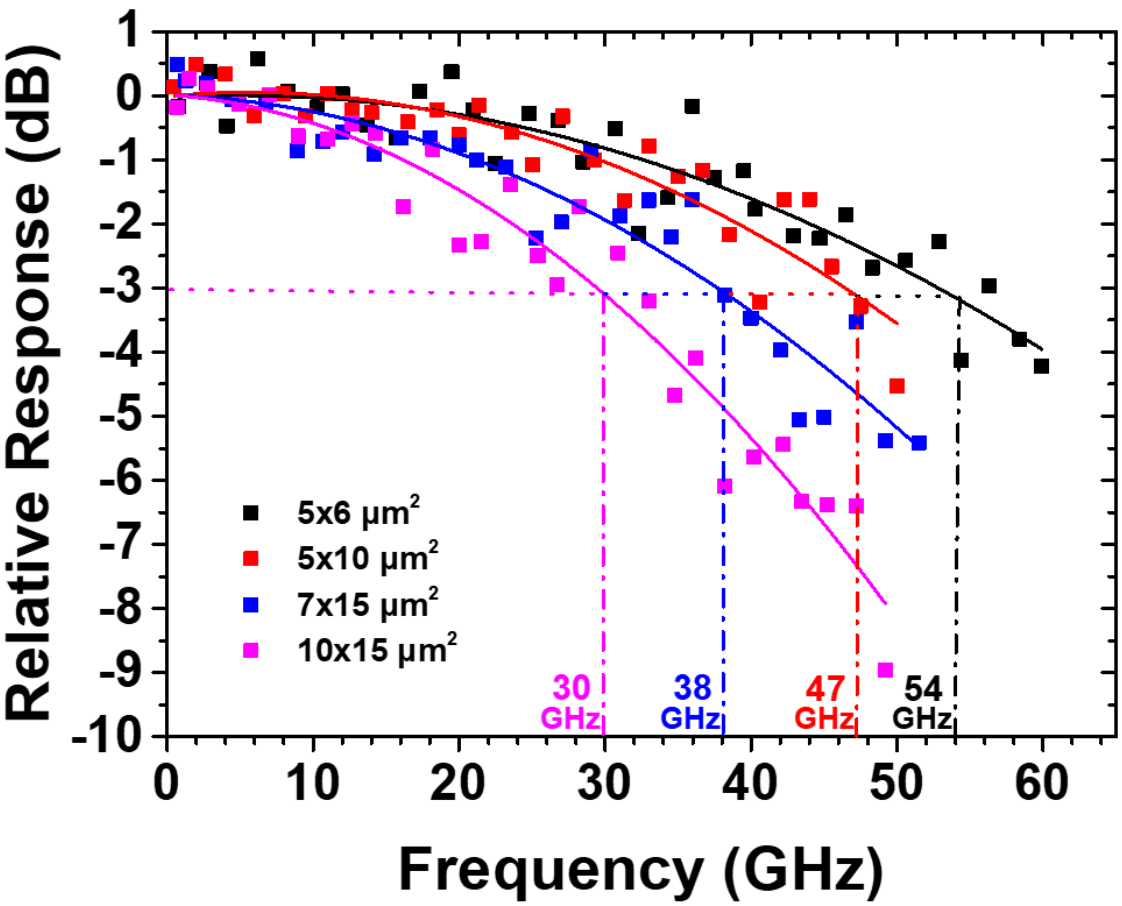


Figure 6-19. Frequency responses of waveguide PDs with different PD area (Solid line: polynomial fit)

The RF output power was detected using a calibrated power meter with a frequency range from dc to 50 GHz and a Rohde Schwarz electrical spectrum analyzer with a frequency range from 50 GHz to 60 GHz. Figure 6-19 summarize the frequency responses of the devices with various active areas at -3 V. Waveguide photodiodes with active areas of 30 μm^2, 50 μm^2, 105 μm^2 and 150 μm^2 have bandwidths of 54 GHz, 47 GHz, 38 GHz and 30 GHz, respectively. For the device with an active area of 150 μm^2 a 3-dB bandwidth of 30 GHz at -3V is constant with the bandwidth of bar-level waveguide PDs discussed in section 6.4. Considering the estimated transit time limited bandwidth of 90 GHz (from equation 3.7, W_A=320 nm, W_D=380 nm, D_e=110 cm^2/s, v_{th}=5.5×10^5m/s and v_e=2×10^5m/s), these measured bandwidths match the RC limited bandwidth from parameter extraction in Table I very well.

6.5.5 RF Saturation Characteristics

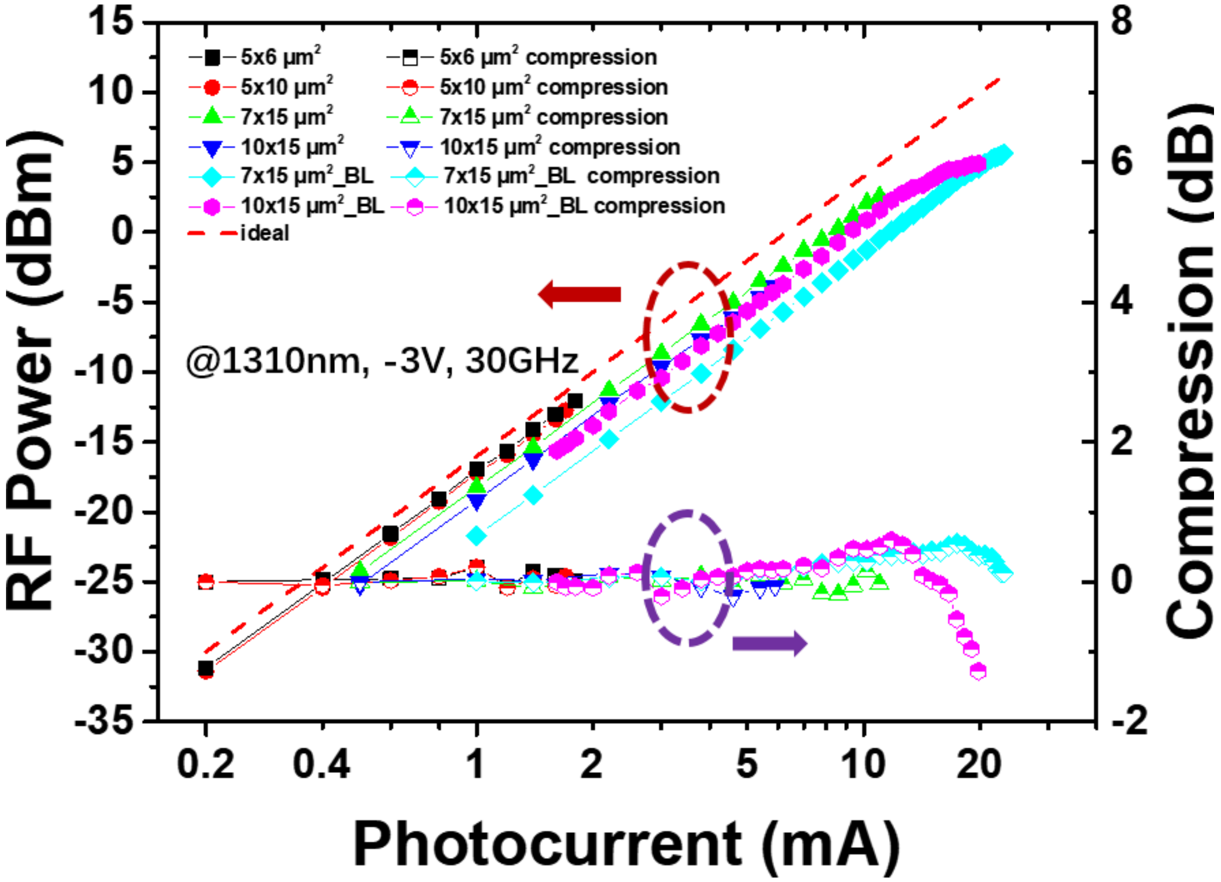


Figure 6-20. RF output power and RF power compression versus photocurrent at -3V, 30GHz.

As shown in Figure 6-20, the RF power of both bar-level (BL) waveguide PDs and transfer-printed waveguide PDs was measured as a function of the average photocurrent at 30 GHz. As discussed in chapter 3.3.5, the saturation current and power were defined as the photocurrent and power where the RF power compression curve drops by 1 dB from its peak value. As reported in section 6.4, when the bias was -3V, the bar-level waveguide PDs with active area of 7×15 μm^2 and 10×15 μm^2 achieved 5.7 dBm and 4.9 dBm output power at 23 mA and 19 mA, respectively. It should be noted that the 7×15 μm^2 PD was not yet fully saturated but died at 23 mA. For the transfer-printing PDs, due to the limitations of the external responsivity and output power in our praseodymium-doped fiber amplifier, we couldn't measure the saturation RF power of these PDs. At -3V, the highest RF power we could measure from transfer-printed PDs with 5×6 μm^2, 5×10 μm^2, 7×15 μm^2 and 10×15 μm^2 are -12 dBm at 1.8 mA, -12.7 dBm at 1.7 mA, 2.6 dBm at 11 mA and -3.8 dBm at 5.9 mA, respectively.

6.5.6 Eye diagram

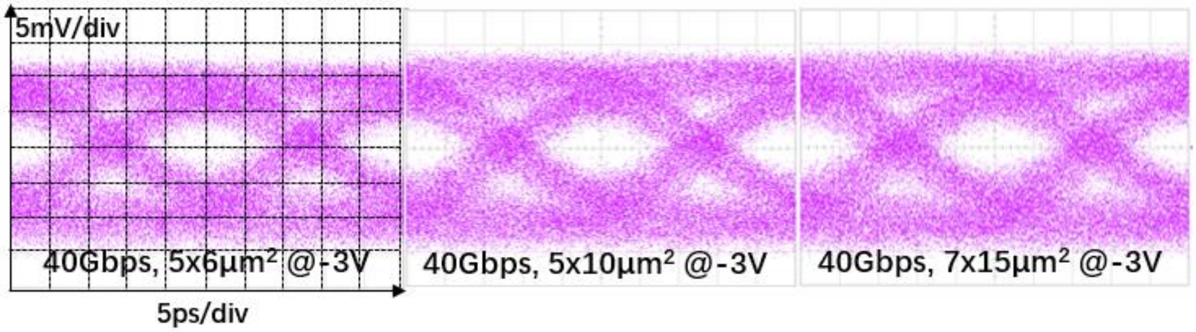


Figure 6-21. 40 Gbit/s eye diagrams of the 5×6 μm^2, 5×10 μm^2 and 7×15 μm^2 transfer-printed waveguide PDs at -3V. (5 ps/div, 5 mV/div).

The non-return-zero eye diagrams ware also measured to evaluate our photodiodes for use in high-speed digital optical links. Due to the equipment limitation including the lack of a high-speed 1310 nm modulator and only having 40 Gbit/s PRBS mentioned in section 5.4.6, the same experimental setup as shown in Figure 5-13 was used to measure the non-return-zero eye diagram at 1550 nm for transfer-printed PDs. The 40 Gbit/s eye diagrams of the PDs with 30 μm^2, 50 μm^2 and 105 μm^2 active area at -3V with 1mA photocurrent are shown in Fig. 6-21. Widely open eye diagrams with a peak voltage of 20 mV at 40 Gbit/s were observed, indicating a high-quality data reception performance of the transfer-printed PD.

6.6 Summary

In this chapter, a waveguide MUTC photodiode on a SiN/Si platform using micro-transfer-printing with record-high bandwidth and high responsivity at 1310 nm was successfully demonstrated. At -3 V, the photodiodes achieved 54 GHz bandwidth, 0.29 A/W internal responsivity. This performance is among the highest reported for all transfer-printed photodiodes (Table VII) and, to the best of our knowledge, represents a new record for transfer-printed photodiodes on Si.

Table VII Performance comparison for transfer-printing photodiodes

Year	Structure	Type	Measured Responsivity (A/W)	Wavelength (nm)	Bandwidth (GHz)	Dark current (nA)	Ref
2017	InGaAsP PIN	Surface Normal	0.49 (vertical coupling)	1310	11.5	600 @-3V	56
2018	InGaAs PIN	Surface Normal	0.55 (grating coupler)	1550	8	20 @-2V	68
2018	Ge PIN	Surface Normal	0.66 (trident coupler)	1550	14	12 @-1V	59
2019	InGaAs PIN	Surface Normal	0.6 (grating coupler)	1550	14@-3V	900 @-1V	70
2020	GaAs PIN	Surface Normal	0.3(grating coupler)	850	NA	0.02 @-2V	57
2021	Si PIN	Surface Normal	0.19 (grating coupler)	800	6	0.107 @-3V	71
2021	InGaAs/InP UTC	Surface Normal	0.8 (10 μm long)	1550	NA	2×10^4 @-1V	72
This work	**InGaAs/InGaAsP MUTC**	**Waveguide**	**0.29@0V (internal)**	**1310**	**54@-3V**	**6 @-3V**	

Chapter 7 Conclusions and Future Work

7.1 Conclusions

The main focus of my PhD work has been to develop three different high-performance photodiodes for different applications: 1. Large-area high-power MUTC photodiode for high-gain analog optical links and photoacoustic signal detection applications, 2. High-speed zero-bias waveguide MUTC photodiode for dense photonic integrated circuits, 3. O-band high-speed waveguide MUTC photodiode integrated on Si platform by micro-transfer-printing for Si photonics. These works include design, fabrication and characterization for each photodiode.

First, for free space analog photonics system such as photoacoustic imaging systems, antenna remoting and photonic oscillator systems, a large-area high-power MUTC photodiode has been developed to achieve both easy free space light coupling and high output RF power for high link gain simultaneously. The large-area high-power MUTC photodiode has achieved output RF powers of 23dBm at 2GHz, 20nA dark current at -8V and responsivity of 0.63 A/W.

Second, for low power consumption, a zero-bias high-speed waveguide MUTC photodiode has been demonstrated. To avoid the low carrier transmission velocity in traditional MUTC waveguide at 0V, a staggered band lineup (Type-II) structure is achieved in the conduction band between the absorber and the wide-bandgap drift layer by using GaAsSb as absorption material and InAlGaAs as drift layer material. Also, compared with traditional back-illuminated photodiode which has trade-off between quantum efficiency and speed, a novel dual-integrated waveguide-depletion layer was used in a evanescently coupled waveguide type-II MUTC PD to achieve high efficiency and high speed simultaneously. The zero-bias high-speed evanescently coupled waveguide type-II MUTC PD has achieved a record high bandwidth (66GHz at 0V and 102GHz at -1V), high internal responsivity of 0.48 A/W, and very little performance dependence with bias voltage. It is the first type-II MUTC photodiode with waveguide structure for zero-bias operation.

Third, for Si photonic applications such as photonic integrated circuit, I developed a high-power waveguide MUTC photodiode at 1310 nm, which is integrated on SiN/Si platform using micro-transfer-printing. Micro-transfer-printing technology was chosen as the integration method due to its high integration density capability, high efficiency of III-V material use, high throughput and low cost. Similar to my second project of zero-bias PDs, an evanescently coupled III-V waveguide structure was used to achieve better bandwidth-efficiency product of photodiode and good light coupling efficiency with SiN waveguide on Si. Beside this, it can also decouple the light coupling efficiency on SiN platform and the performance of PDs, which means the III-V waveguide for light coupling with SiN waveguide on Si and photodiode can be designed separately. The high-power waveguide MUTC photodiode integrated on SiN/Si platform has achieved a record high bandwidth (54 GHz at -3V) and high internal responsivity of 0.29 A/W at 1310 nm. The bar-level waveguide MUTC photodiode achieved a record high 5.7 dBm RF output power at 30 GHz at 1310 nm. It is the first MUTC waveguide PD transfer-printed on SiN/Si platform.

7.2 Future Works

7.2.1 New wafer epitaxial layer design for zero-bias waveguide PD

As mentioned in chapter 5, I have demonstrated a high-speed waveguide PD at zero bias. In order to improve the RF output power and responsivity while not sacrificing the bandwidth, a new epitaxial structure needs to be designed.

For the new epitaxial structure design, I first focused on responsivity. In previous design, the thickness of $In_xAl_yGa_{1-x-y}As$ drift and n-contact layer are key parameters affecting the optical coupling efficiency. The measured external responsivity is smaller than what we expected. Also, if we did some over etch on the p-mesa step, the waveguide mode would be cut-off which is beyond our expectation. InGaAsP could be a better choice to substitute InAlGaAs due to its higher refractive index. Figure 7-1 shows the initial optical simulation results for 50 μm and 10 μm long PD's absorber. The blue line of monitor value shows the total optical power, red line shows the single mode optical power and green line shows the power absorbed in absorber. If the PD have the size of 5×7 μm^2, when Z=107 μm, 70% optical power has been absorbed which means the internal responsivity would be 0.87 A/W at 1550 nm. This value is much higher than the responsivity we measured and showed above in Table III.

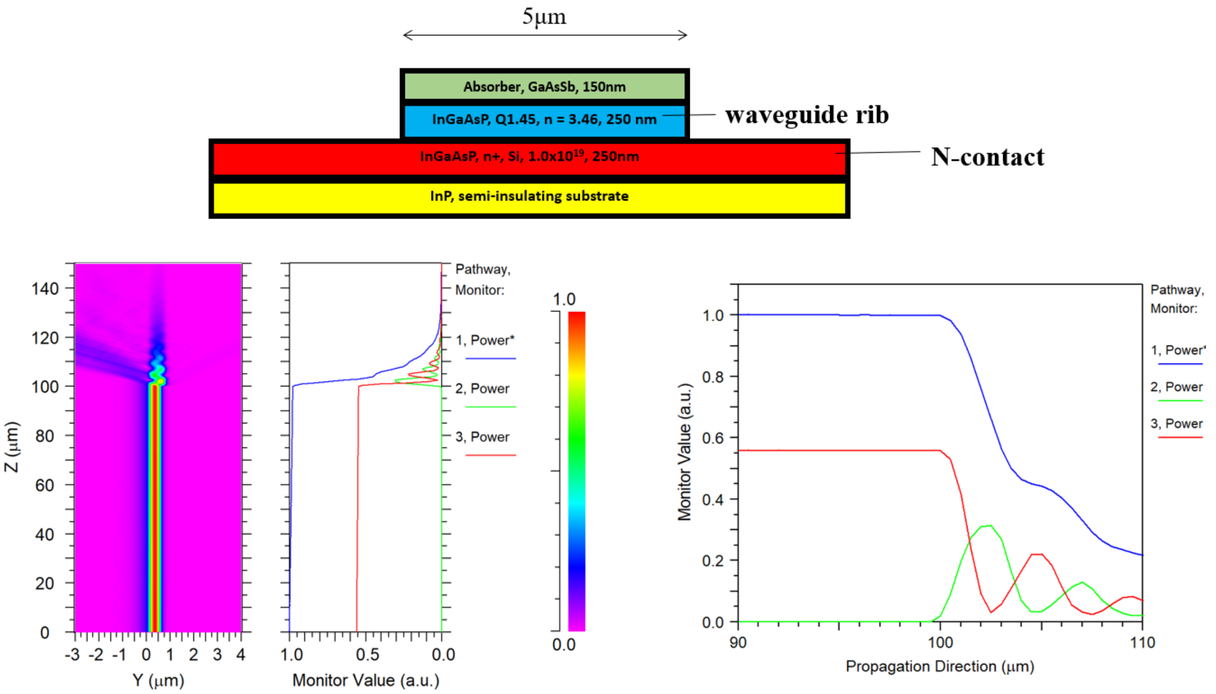


Figure 7-1. Optical simulation of InGaAsP waveguide with GaAsSb absorber.

In order to improve the RF output power, a 50 nm n-type doped ($1x10^{17}$ cm^{-3}) charge layer with 200 nm-thick light n-type doping ($1x10^{16}$ cm^{-3}) electron InGaAsP drift layer can be used for charge compensation. This 50 nm charge layer can help to reduce the deleterious effect of space charge at high photocurrents and thus increase the output power of the PD [49]. To confirm this high-power design, I did an electric field simulation using a commercial software (APSYS) and the results are shown in Figure 7-2 (the rest epitaxial structure in the simulation is the same with Figure 5-1). The input optical power is 40 mW/μm^2 which means 4 W light irradiate on a 10×10 μm^2 device. Under this high input optical power, the structure with charge layer has a near-double higher electrical field (16200 V/cm) than the traditional drift layer (9360 V/cm) which indicates that charge layer can reduce space charge effect at high photocurrents and increase the output power of PD. In the future, more simulation about the impact of the thickness and doping levels for each layer on PD performance needs to be done to maximize the bandwidth, RF power, and responsivity.

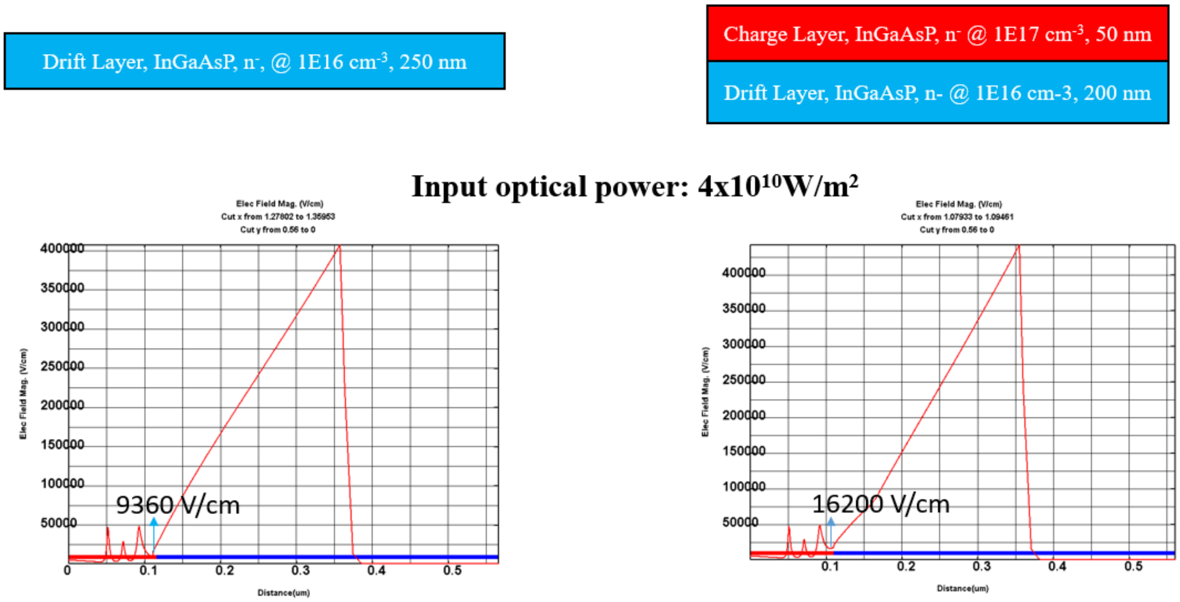


Figure 7-2. Simulated electric field distribution at 40 mW/μm^2 light illumination at 1550 nm.

7.2.2 Zero-bias waveguide photodiodes on Silicon using micro-transfer-printing

In chapter 5, a high-speed zero-bias waveguide photodiode with the advantages of low power consumption and small footprint has been demonstrated. And in chapter 6, a high-speed waveguide photodiode which is capable of being integrated on Si platform for Si photonics applications has been demonstrated. Based on these two works, a novel waveguide photodiode which can have the advantages of both two photodiodes simultaneously can be designed and fabricated.

As mentioned in section 7.2.1, InGaAsP could be a better choice to substitute InAlGaAs to achieve better quantum efficiency. Same as the simulation method used in section 5.2, if substitute InAlGaAs for InGaAsP in drift layer and keep other structure same, band diagram and electric field distribution inside the absorption and drift layer has been simulated under zero-bias. The simulation results are shown in Figure 7.3. Compared with Figure 5-5, there is nearly no difference which means that using InGaAsP as drift layer material can maintain the high speed of photodiode.

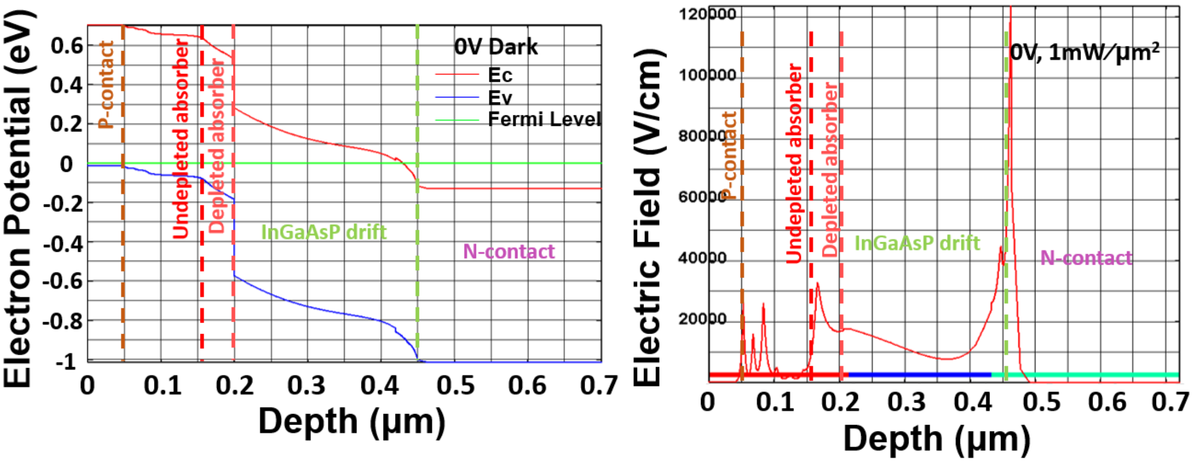


Figure 7-3. (a) Simulated band diagram at 0 V. (b) Simulated electric field distribution at 0 V and 1 mW/μm^2 light illumination at 1550 nm.

The new epitaxial design of the novel zero-bias waveguide which can be integrated on Si/SiN platform is shown in Figure 7-4. In this design, 50 nm InGaAsP charge layer is added to reduce the deleterious effect of space charge at high photocurrents and thus increase the output power of the PD, which has been proved in section 7.2.1. Different from the dual-integrated waveguide-depletion layer design in chapter 5, the waveguide layer is designed below the n-contact layer

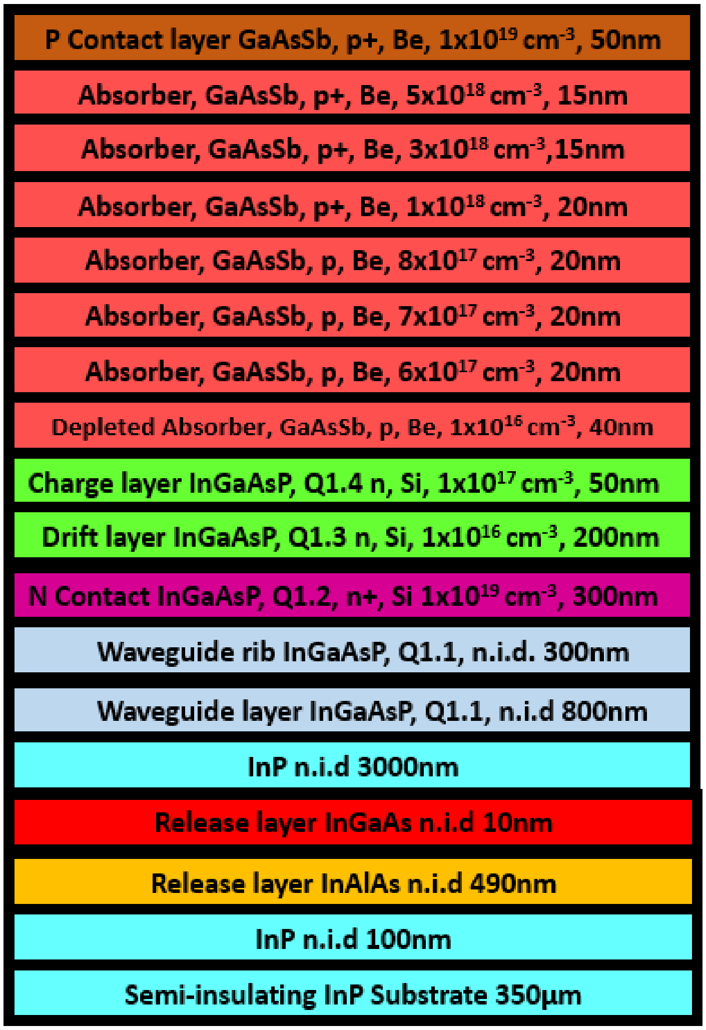
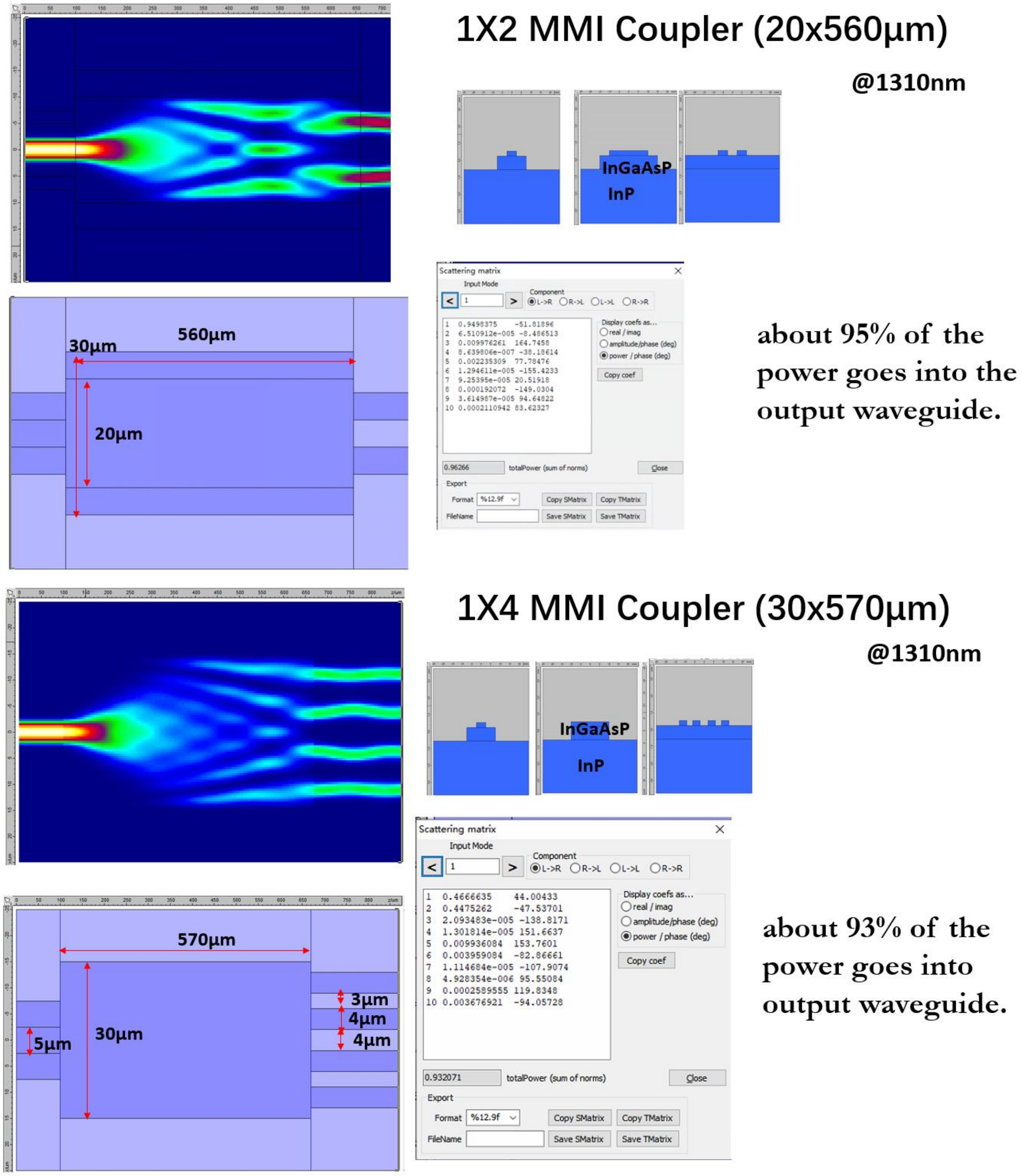


Figure 7-4. Details of epitaxial structure of zero-bias PD can be transfer-printed on SiN/Si platform. All layers are lattice-matched to InP.

which is very helpful to decouple the light coupling efficiency on SiN platform and the performance of PDs. Assuming the size of SiN waveguide on Si platform is the same as the waveguide mentioned in chapter 6, the thickness of rib and slab InGaAsP waveguide shown in Figure 7-4 can induce very good coupling efficiency between SiN waveguide and III-V waveguide for high quantum efficiency and responsivity of this new photodiode. Also, it should be mentioned that the speed of this novel zero-bias waveguide would be as high as the zero-bias photodiode introduced in chapter 5 since the thickness of absorption layer and drifter layer is the same. As for the responsivity, compared with the O-band transfer-printed waveguide photodiode in chapter 6, the responsivity of the novel zero-bias photodiode should be larger since the thinner drift layer which means the waveguide is closer to the absorption layer for better mode beating and light absorption.

To improve the RF output saturation power of this photodiode, a PD array with multi-mesa structure is a good option since multi-mesa structure can directly improve the power handle capability of photodiode. One option is to use multimode interference (MMI) coupler for light input coupling and light splitter to guide the light waves into each mesa of PDs. Figure 7-5 shows the simulation results of MMI design in FIMMWAVE to minimize the optical loss during the light transmission. For 1×2 MMI (one input and two outputs) coupler, about 95% of the optical power can go into the output waveguide ribs. For 1×4 MMI (one input and four outputs) coupler, about 93% of the optical power can go into the output waveguide ribs. Actually in the work introduced in chapter 6. I've fabricated the PD arrays and the micrograph of PDs before transfer-printing is shown in Figure 7-6. However, they are not transfer-printed successfully due to the large size of PD arrays chiplet. For bar-level PD arrays, the external responsivity of 0.1 A/W in 5×10 μm^2 4-PD-array with 1×4 MMI has been measured successfully, which prove the practicality of the MMI design.

The fabrication processes of this novel zero-bias waveguide photodiode transfer-printed on SiN/Si platform are very close to the processes in section 3.2 and 6.2.



1X2 MMI Coupler (20x560μm)

@1310nm

Input Mode: 1

Component: ● L->R ○ R->L ○ L->L ○ R->R

Display coefs as...: ○ real / imag ○ amplitude/phase (deg) ● power / phase (deg)

```
1  0.9498375    -51.81896
2  6.510912e-005 -8.486513
3  0.009976261  164.7458
4  8.639806e-007 -38.18614
5  0.002235309  77.78476
6  1.294611e-005 -155.4233
7  9.25395e-005 20.51918
8  0.000192072  -149.0304
9  3.614987e-005 94.64822
10 0.0002110942 83.62327
```

0.96266 totalPower (sum of norms)

Format: %12.9f

FileName:

about 95% of the power goes into the output waveguide.

1X4 MMI Coupler (30x570μm)

@1310nm

Input Mode: 1

Component: ● L->R ○ R->L ○ L->L ○ R->R

Display coefs as...: ○ real / imag ○ amplitude/phase (deg) ● power / phase (deg)

```
1  0.4666635    44.00433
2  0.4475262    -47.53701
3  2.093483e-005 -138.8171
4  1.301814e-005 151.6637
5  0.009936084  153.7601
6  0.003959084  -82.86661
7  1.114684e-005 -107.9074
8  4.928354e-006 95.55084
9  0.0002589555 119.8348
10 0.003676921  -94.05728
```

0.932071 totalPower (sum of norms)

Format: %12.9f

FileName:

about 93% of the power goes into output waveguide.

Figure 7-5. Simulation results of MMI.

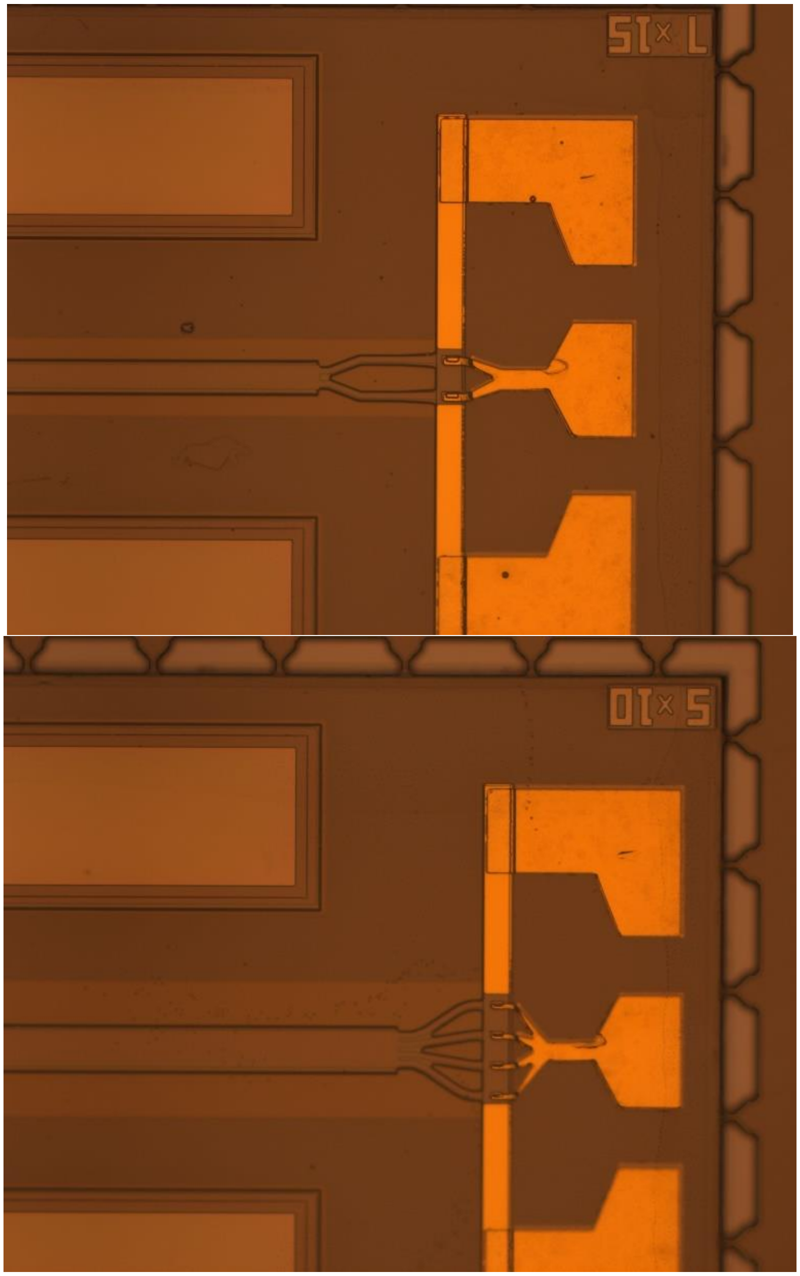


Figure 7-6. Micrograph of fabricated PD arrays with MMI.

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Appendix I (Fabrication recipe template for transfer-printed waveguide PD)

1. P-Mesa (Mesa 1)

1.1 p-metal

- Clean wafer Rinse in Acetone, DI______________________________(_)(_)(_)
  bake-out 5min 110C ______________________________(_)(_)(_)
- O2 plasma power: 200, gas: 80, 600sec ______________________________(_)(_)(_)
- Metal deposit Ti: 200-Å (1.0 A/s); ______________________________spin(_)
  Pt: 300-Å (1.0 A/s); ______________________________spin(_)
  Au: 500-Å (1.5 Å/s);______________________________spin(_)
  Ti: 300- Å (1.0 A/s); ______________________________spin(_)
- Alphastep Si Dummy (~300nm); ______________________________

1.2 Hard mask SiO2

- Clean wafer Acetone, DI, bake-out 5min 90C, 5min 110C ____________________(_)(_)(_)
- PECVD recipe “OXIDE 2” in VT (for 600 nm): ____________________(_)(_)(_)
- Profilometer Film thickness on dummy Si after deposition:

____

- Clean wafer Acetone, IPA, DI, slow bake-out 3min 100C ____________________(_)(_)(_)
- O2 plasma power: 200, gas: 80, 600sec ______________________________(_)(_)(_)
- Lithography Spin HMDS, spin resist AZ5214: 40sec, 3000 rpm, soft bake 100C 2 min __________(_)(_)(_)

Recipe “AZ5214_AB” in MA/BA6
Exposure mask “p-mesa”: vacuum contact,______________________________(_)(_)(_)

Develop AZ300MIF 30 sec (agitate) ____________________(_)(_)(_)

Post bake 110C, 50 sec ______________________________(_)(_)(_)

Alphastep PR thickness (~1.6µm thick): ______________________________

____

- SiO2 dry etch Oxford ICP RIE: “OPTSiO2CHF3 ETCHXXJ” 20 nm/1min sec, selectivity SiO2 : PR = , (_)(_)(_)

  Calculation(____s) ______________________________

  ____

- Alphastep PR+SiO2 thickness: ______________________________
- Remove Resist Acetone, IPA, DI, slow bake-out 5min 90C, 5min 110C ____________________(_)(_)(_)
- O2 plasma power: 200, gas: 80, 600 sec ____________________(_)(_)(_)
- -Alphastep SiO2 thickness (~nm): ______/_______/______on Dummy (~nm): ____________________

1.3 Mesa 1 dry etch

- Oxford ICP RIE Conditional: “OPT-InP Etch” (Cl2/N2) 3 min at 50° C w/4-in Si carrier wafer ____________
- ICP RIE dry etch “OPT-InP Etch-EP”, wafer die w/ Fomblin oil, see laser monitor____________________

  ____

  ____

  ____

  ____

  ____

- Oxford clean Use 5-inch quartz wafer for cleaning (20 – 50° C)____________________
- Profilometer SiO2 Dummy thickness (~ 600 nm): ____________________
- Alphastep SiO2+mesa thickness ______________________________
- Mesa1 height : ______________________________

2. N-Mesa (Mesa 2)

2.1 Hard Mask SiO2

- Clean wafer Acetone, DI, bake-out 5min 90C, 5min 110C ____________________(_)(_)(_)
- PECVD recipe “OXIDE 2” in VT (for 300 nm): ____________________(_)(_)(_)

- Profilometer Film thickness on dummy Si after deposition:

____

- Clean wafer Acetone, IPA, DI, slow bake-out 3min 100C ________________(_)(_)(_)

- O2 plasma power: 200, gas: 80, 600sec ________________(_)(_)(_)

- Lithography Spin HMDS, spin resist AZ5214: 40sec, 3000 rpm, soft bake 100C 2 min ________(_)(_)(_)

Recipe “AZ5214_AB” in MA/BA6
Exposure mask “n-mesa”: vacuum contact,________________(_)(_)(_)

Develop AZ300MIF 30 sec (agitate) ________________(_)(_)(_)

Post bake 110C, 50 sec ________________(_)(_)(_)

Alphastep PR thickness (~1.6μm thick): ________________

____

- SiO2 dry etch Oxford ICP RIE: “OPTSiO2CHF3 ETCHXXJ” 20 nm/1min sec, selectivity SiO2 : PR = , (_)(_)(_)

Calculation (____s) ________________

____

- Alphastep PR+SiO2 thickness: ________________

- Remove Resist Acetone, IPA, DI, slow bake-out 5min 90C, 5min 110C ________________(_)(_)(_)

- O2 plasma power: 200, gas: 80, 600 sec ________________(_)(_)(_)

-Alphastep SiO2 thickness (~nm): ______/_______/______on Dummy (~nm): ________________

2.2 Mesa 2 Dry etch

- Oxford ICP RIE Conditional: “OPT-InP Etch” (Cl2/N2) 3 min at 50° C w/4-in Si carrier wafer ____________

- ICP RIE dry etch “OPT-InP Etch-EP”, wafer die w/ Fomblin oil, see laser monitor________________

____

____

____

____

- Oxford clean Use 5-inch quartz wafer for cleaning (20 – 50° C)________________

- Profilometer SiO2 Dummy thickness (~ 300 nm): ________________

- Alphastep SiO2+mesa thickness ________________

- Mesa 2 height : ________________

3. Rib waveguide (Mesa 3)

3.1 Hard Mask SiO2

- Clean wafer Acetone, DI, bake-out 5min 90C, 5min 110C ________________(_)(_)(_)

  - PECVD recipe “OXIDE 2” in VT (for 300 nm): ________________(_)(_)(_)

- Profilometer Film thickness on dummy Si after deposition:

- Clean wafer Acetone, IPA, DI, slow bake-out 3min 100C ________________(_)(_)(_)

- O2 plasma power: 200, gas: 80, 600sec ________________(_)(_)(_)

- Lithography Spin HMDS, spin resist AZ5214: 40sec, 3000 rpm, soft bake 100C 2 min ________(_)(_)(_)

Recipe “AZ5214_AB” in MA/BA6
Exposure mask “Rib waveguide”: vacuum contact, ________________(_)(_)(_)

Develop AZ300MIF 30 sec (agitate) ________________(_)(_)(_)

Post bake 110C, 50 sec ________________(_)(_)(_)

Alphastep PR thickness (~1.6μm thick): ________________

- SiO2 dry etch Oxford ICP RIE: “OPTSiO2CHF3 ETCHXXJ” 20 nm/1min sec, selectivity SiO2 : PR = , (_)(_)(_)

Calculation (____s) ________________

- Alphastep PR+SiO2 thickness: ________________

- Remove Resist Acetone, IPA, DI, slow bake-out 5min 90C, 5min 110C ________________(_)(_)(_)

- O2 plasma power: 200, gas: 80, 600 sec ____(_)(_)(_)

-Alphastep SiO2 thickness (~nm): ______/_______/______on Dummy (~nm): ____________________

3.2 Mesa 3 Dry etch

- Oxford ICP RIE Conditional: “OPT-InP Etch” (Cl2/N2) 3 min at 50° C w/4-in Si carrier wafer ____________

- ICP RIE dry etch “OPT-InP Etch-EP”, wafer die w/ Fomblin oil, see laser monitor________________________

____

____

____

____

____

- Oxford clean Use 5-inch quartz for cleaning (20 – 50° C)____

- Profilometer SiO2 Dummy thickness (~ 300 nm): ____

- Alphastep SiO2+mesa thickness ____

- Mesa 3 height : ____

4. Slab waveguide (Mesa 4)

4.1 Hard Mask SiO2

- Clean wafer Acetone, DI, bake-out 5min 90C, 5min 110C ______________________________(_)(_)(_)

- PECVD recipe “OXIDE 2” in VT (for 300 nm): __________________________________(_)(_)(_)

- Profilometer Film thickness on dummy Si after deposition:

____

- Clean wafer Acetone, IPA, DI, slow bake-out 3min 100C ______________________________(_)(_)(_)

- O2 plasma power: 200, gas: 80, 600sec ____(_)(_)(_)

- Lithography Spin HMDS, spin resist AZ5214: 40sec, 3000 rpm, soft bake 100C 2 min _________(_)(_)(_)

Recipe “AZ5214_AB” in MA/BA6
Exposure mask “Slab waveguide”: vacuum contact,____________________(_)(_)(_)

Develop AZ300MIF 30 sec (agitate) ____________________(_)(_)(_)

Post bake 110C, 50 sec ____________________(_)(_)(_)

Alphastep PR thickness (~1.6μm thick): ____________________

____

- SiO2 dry etch Oxford ICP RIE: “OPTSiO2CHF3 ETCHXXJ” 20 nm/1min sec, selectivity SiO2 : PR = , (_)(_)(_)

  Calculation (____s) ____________________

  ____

- Alphastep PR+SiO2 thickness: ____________________
- Remove Resist Acetone, IPA, DI, slow bake-out 5min 90C, 5min 110C ____________________(_)(_)(_)
- O2 plasma power: 200, gas: 80, 600 sec ____________________(_)(_)(_)
- Alphastep SiO2 thickness (~nm): ______/_______/______on Dummy (~nm): ____________________

4.2 Mesa 4 Dry etch

- Oxford ICP RIE Conditional: “OPT-InP Etch” (Cl2/N2) 3 min at 50° C w/4-in Si carrier wafer ____________
- ICP RIE dry etch “OPT-InP Etch-EP”, wafer die w/ Fomblin oil, see laser monitor____________________

  ____

  ____

  ____

  ____

  ____

- Oxford clean Use 5-inch quartz wafer for cleaning (20 – 50° C)____________________
- Profilometer SiO2 Dummy thickness (~ 300 nm): ____________________
- Alphastep SiO2+mesa thickness ____________________
- Mesa 4 height :

  ____

5. Protection layer

SiO2 deposition

- Clean wafer Acetone, DI, bake-out 5min 90C, 5min 110C ______________________________(_)(_)(_)
  - PECVD recipe “OXIDE 2” in VT (for 300 nm): ___________________________________(_)(_)(_)
- Profilometer Film thickness on dummy Si after deposition:

____

- Clean wafer Acetone, IPA, DI, slow bake-out 3min 100C ______________________________(_)(_)(_)
- O2 plasma power: 200, gas: 80, 600sec ____(_)(_)(_)
- Lithography Spin HMDS, spin resist AZ5214: 40sec, 3000 rpm, soft bake 100C 2 min _________(_)(_)(_)

Recipe “AZ5214_AB” in MA/BA6
Exposure mask “Protection layer”: vacuum contact,____(_)(_)(_)

Develop AZ300MIF 30 sec (agitate) _______________________________________(_)(_)(_)

Post bake 110C, 50 sec ____(_)(_)(_)

Alphastep PR thickness (~1.6µm thick): ____

____

- SiO2 dry etch Oxford ICP RIE: “OPTSiO2CHF3 ETCHXXJ” 20 nm/1min sec, selectivity SiO2 : PR = , (_)(_)(_)

Calculation (____s) ____

____

- Alphastep PR+SiO2 thickness: ____
- Remove Resist Acetone, IPA, DI, slow bake-out 5min 90C, 5min 110C ______________________(_)(_)(_)
- O2 plasma power: 200, gas: 80, 600 sec ____(_)(_)(_)
- -Alphastep SiO2 thickness (~nm): ______/_______/______on Dummy (~nm): _____________________

6. N-Metal deposition

6.1 Open n-contact layer

- Clean wafer Acetone, IPA, DI, slow bake out 3 min 100C _______________________________________

- Lithography Spin HMDS, spin resist AZ5214: 40sec, 3000 rpm, soft bake 100C 2 min __________(_)(_)(_)

Recipe “AZ5214_AB” in MA/BA6
Exposure mask “N-metal”: vacuum contact, __________(_)(_)(_)

Develop AZ300MIF 30 sec (agitate) __________(_)(_)(_)

Post bake 110C, 50 sec __________(_)(_)(_)

Alphastep PR thickness (~1.6µm thick): __________

____

- Wet Etch BOE (10:1) SiO2 (150nm/min): Calculation: __________nm, __________ sec

____

____

____

____

- O2 plasma power: 200, gas: 80, 300 sec __________(_)(_)(_)

Alphastep PR+SiO2 thickness (~ µm thick): __________

____

6.2 Deposit metal

- Metal deposit AuGe: 300-Ǻ (1.0 A/s); __________spin(_)

Ni: 200-Ǻ (1.0 A/s); __________spin(_)

Au: 1000-Ǻ (2.0 Ǻ/s); __________spin(_)

- Lift-Off Acetone soak + Ultrasonic (small Ultrasonic 20-50 units) ________ __________(_)(_)(_)

7. SU-8 deposition

Deposit SU-8

- Clean wafer Acetone, IPA, DI, ____

- Lithography Spin resist SU-8 2002: 30sec, 3000 rpm, soft bake 100C 3 min __________(_)(_)(_)

Recipe “SU-8-2002_AB” in MA/BA6
Exposure mask “SU-8”: vacuum contact, ______________________(_)(_)(_)

Post bake 95C, 3 min ______________________________(_)(_)(_)

Develop in SU-8 developer 1 min (agitate) ____________________(_)(_)(_)

Post bake 110C, 50 sec ____________________________(_)(_)(_)

Alphastep PR thickness (~2 µm thick): __________________________

____

8. Open p-contact

- Clean wafer Acetone, IPA, DI ________________________________(_)(_)(_)

- Lithography Spin/Steam HMDS, spin resist AZ5214: 40sec, 3000rpm, soft bake 100C 2 min: ___(_)(_)(_)

Recipe “AZ5214_AB” in MA/BA6
Exposure mask “P-open”: vacuum contact,_____________________(_)(_)(_)

Develop AZ300MIF 30 sec (agitate) _______________________(_)(_)(_)

Post bake 110C, 50 sec ____________________________(_)(_)(_)

Alphastep PR thickness (~1.6µm thick): __________________________

____

- SiO2 dry etch Oxford ICP RIE: “OPTSiO2CHF3 ETCHXXJ” 20 nm/1min sec, selectivity SiO2 : PR:

Alphastep PR+SiO2 thickness: ______________________________

____

- I-V Test Measure I-V characteristics on larger-area PD:

(_______): _____V @ 1mA, _____mA @ -5V; (_______): _____V @ 1mA, _____mA @ -5V

(_______): _____V @ 1mA, _____mA @ -5V; (_______): _____V @ 1mA, _____mA @ -5V
(_______): _____V @ 1mA, _____mA @ -5V; (_______): _____V @ 1mA, _____mA @ -5V

(_______): _____V @ 1mA, _____mA @ -5V; (_______): _____V @ 1mA, _____mA @ -5V

(_______): _____V @ 1mA, _____mA @ -5V; (_______): _____V @ 1mA, _____mA @ -5V

(_______): _____V @ 1mA, _____mA @ -5V; (_______): _____V @ 1mA, _____mA @ -5V

- Clean wafer Acetone, IPA, DI, ____(_)(_)(_)

9. Seedlayer (Pad Metal) and Plating

- Clean wafer Acetone, IPA, DI, blow nitrogen, ____(_)(_)(_)

- Lithography Spin/Steam HMDS, spin resist AZ5214: 40sec, 3000rpm, soft bake 100C 2 min: ___(_)(_)(_)

Recipe “AZ5214_AB” in MA/BA6
Exposure mask “Seedlayer”: vacuum contact,_________________________________(_)(_)(_)

Develop AZ300MIF 30 sec (agitate) ____(_)(_)(_)

Post bake 110C, 50 sec ____(_)(_)(_)

Alphastep PR thickness (~1.6µm thick): ____

- Metal deposit Ti: 200-Ǻ (1.0 A/s); ____spin (_)

Au: 800-Ǻ (1.0 Ǻ/s);____spin (_)

- Lithography Spin/Steam HMDS, spin resist AZ5214: 40sec, 3000rpm ____________________(_)(_)(_)

Soft bake 90C 45sec STOP when Bubbles! min______________/____________/ __________

Recipe “AZ5214_AB” in MA/BA6
Exposure mask “Plating”: vacuum contact, ___________________________________(_)(_)(_)

Develop AZ300MIF 30 sec (agitate) ____(_)(_)(_)

Post bake 110C, 50 sec ____(_)(_)(_)

Alphastep PR thickness (~1.6µm thick): ____

- Plating Plating Au solution (ready-to-use), 50C,
Keysight source meter, Set current: 0.2mA, V ~0.4V...0.5V, (~0.5µm/25min) – *exp. 100min (2um)*
time = ____________ I= __________ V= __________ Step = ____
time = ____________ I= __________ V= __________ Step = ____
time = ____________ I= __________ V= __________ Step = ____
time = ____________ I= __________ V= __________ Step = ____
time = ____________ I= __________ V= __________ Step = ____
time = ____________ I= __________ V= __________ Step = ____
time = ____________ I= __________ V= __________ Step = ____

- O2 plasma Remove top PR layer, power: 150, gas: 80, ~4 hours 40 min ____________________(_)(_)(_)

Alphastep PR thickness ____(_)(_)(_)

- Seed layer etch Gold etch HG400 to remove Au seed layer (sec) ___________________________(_)(_)(_)

- Lift-Off Acetone soak + Ultrasonic (large Ultrasonic 45 units) 10min ___________________(_)(_)(_)

____

10. Spacer layer etch (Mesa 5)

10.1 AZ 4620 Photoresist Mask

- Clean wafer Acetone, DI, ____(_)(_)(_)

- Lithography Spin HMDS, spin resist AZ4620: 45sec, 4000 rpm, soft bake 90C 3 min 30 s ______(_)(_)(_)

Recipe "AZ4620_AB" in MA/BA6
Exposure mask "Spacer layer": vacuum contact, _____________________________________(_)(_)(_)

Develop AZ400K : DI 1:3 50 sec (agitate) _________________________________(_)(_)(_)

Post bake 100C, 2 min ____(_)(_)(_)

Alphastep PR thickness (~7 µm thick): ____

____

10.2 Mesa 5 Dry etch

- Oxford ICP RIE Conditional: "OPT-InP Etch" (Cl2/N2) 3 min at 50° C w/4-in Si carrier wafer ____________

- ICP RIE dry etch "OPT-InP Etch-EP", wafer die w/ Fomblin oil, see laser monitor________________________

____

____

____

____

____

- Oxford clean Use 5-inch quartz wafer for cleaning (20 – 50° C)___________________________________

- Profilometer SiO2 Dummy thickness (~ 1.2 µm): ____

- Alphastep PR+SiO2+mesa thickness ____

- Mesa 5 height :

- remove photoresist Acetone, DI, ____(_)(_)(_)

11. Tether

Tether Photoresist Coating

- Clean wafer Acetone, DI, ____(_)(_)(_)

- Lithography Spin HMDS, spin photoresist SPR220-4.5: 40sec, 3000 rpm,

1. Soft bake 80-90C 30 s ____(_)(_)(_)
2. Soft bake 100C 30 s ____(_)(_)(_)
3. Soft bake 115C 2/3 min ______________________________________(_)(_)(_)

Recipe "SPR220_AB" in MA/BA6
Exposure mask "Tether": vacuum contact____________________________________(_)(_)(_)

1. Post bake room temperature 1 hour ____________________________(_)(_)(_)
2. Post bake 50C, 60 sec ____(_)(_)(_)
3. Post bake 80-90 C, 30 sec _____________________________________(_)(_)(_)
4. Post bake 100C, 30 sec ____(_)(_)(_)
5. Post bake 115C, 90 sec ____(_)(_)(_)

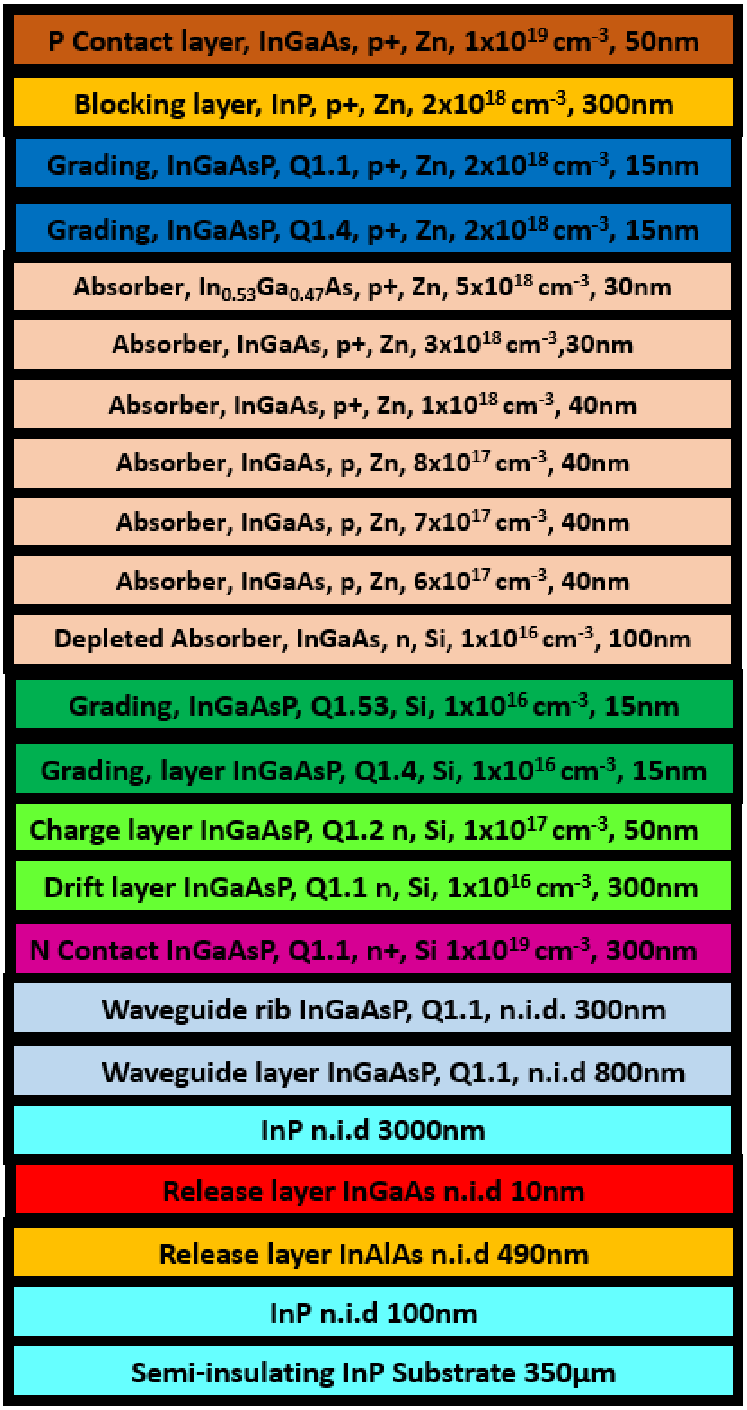
Develop in Megaposit MF-26A developer >2 min (agitate) ________________(_)(_)(_)

Alphastep PR thickness (~5.5 µm thick): ________________________________

____

READY For Transfer-printing processes!

Appendix II (Epitaxy wafer for transfer-printed waveguide PD)



P Contact layer, InGaAs, p+, Zn, 1×10^{19} cm^{-3}, 50nm

Blocking layer, InP, p+, Zn, 2×10^{18} cm^{-3}, 300nm

Grading, InGaAsP, Q1.1, p+, Zn, 2×10^{18} cm^{-3}, 15nm

Grading, InGaAsP, Q1.4, p+, Zn, 2×10^{18} cm^{-3}, 15nm

Absorber, $In_{0.53}Ga_{0.47}As$, p+, Zn, 5×10^{18} cm^{-3}, 30nm

Absorber, InGaAs, p+, Zn, 3×10^{18} cm^{-3},30nm

Absorber, InGaAs, p+, Zn, 1×10^{18} cm^{-3}, 40nm

Absorber, InGaAs, p, Zn, 8×10^{17} cm^{-3}, 40nm

Absorber, InGaAs, p, Zn, 7×10^{17} cm^{-3}, 40nm

Absorber, InGaAs, p, Zn, 6×10^{17} cm^{-3}, 40nm

Depleted Absorber, InGaAs, n, Si, 1×10^{16} cm^{-3}, 100nm

Grading, InGaAsP, Q1.53, Si, 1×10^{16} cm^{-3}, 15nm

Grading, layer InGaAsP, Q1.4, Si, 1×10^{16} cm^{-3}, 15nm

Charge layer InGaAsP, Q1.2 n, Si, 1×10^{17} cm^{-3}, 50nm

Drift layer InGaAsP, Q1.1 n, Si, 1×10^{16} cm^{-3}, 300nm

N Contact InGaAsP, Q1.1, n+, Si 1×10^{19} cm^{-3}, 300nm

Waveguide rib InGaAsP, Q1.1, n.i.d. 300nm

Waveguide layer InGaAsP, Q1.1, n.i.d 800nm

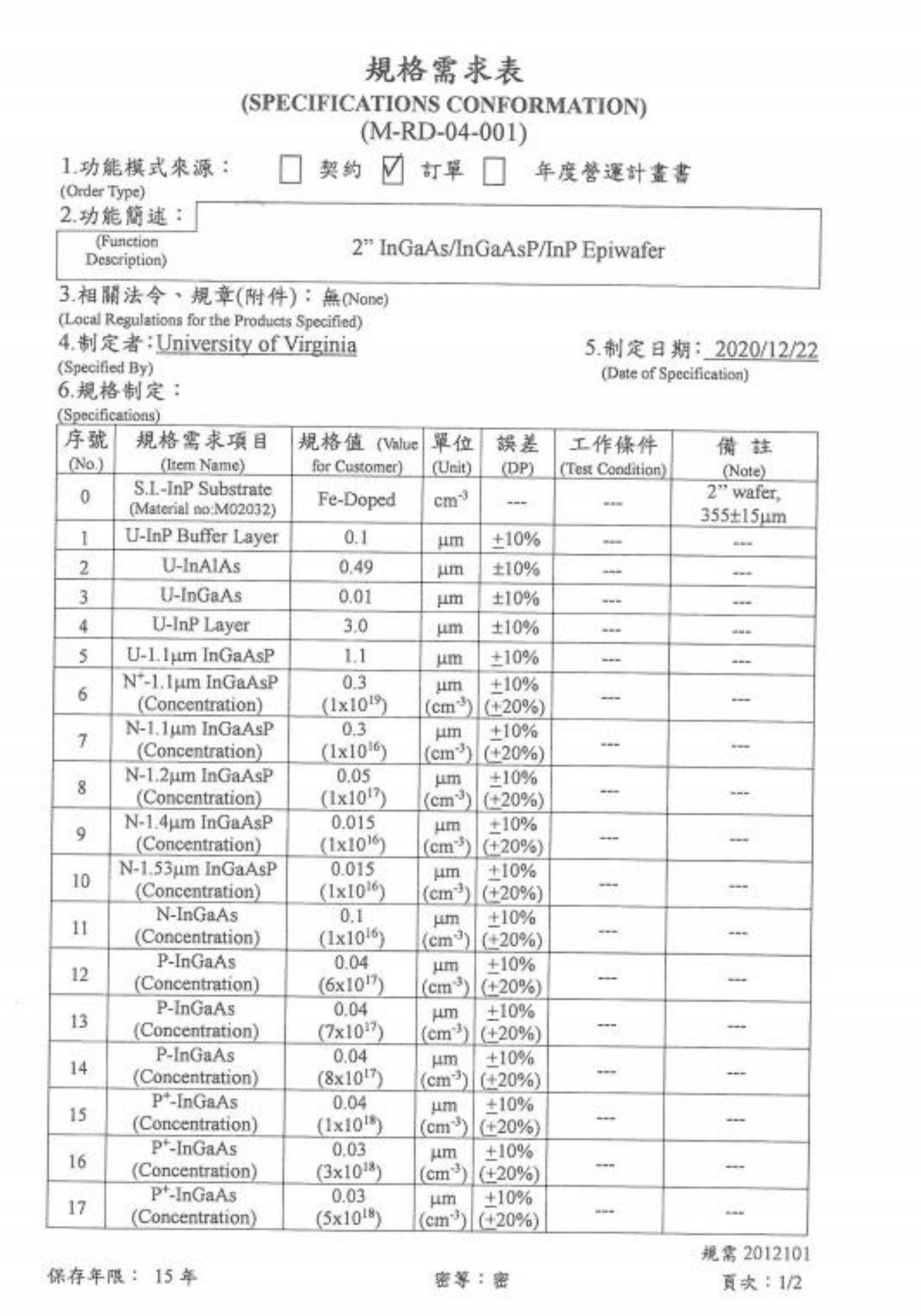
InP n.i.d 3000nm

Release layer InGaAs n.i.d 10nm

Release layer InAlAs n.i.d 490nm

InP n.i.d 100nm

Semi-insulating InP Substrate 350µm



規格需求表
(SPECIFICATIONS CONFORMATION)
(M-RD-04-001)

1.功能模式來源： □ 契約 ☑ 訂單 □ 年度營運計畫書
(Order Type)

2.功能簡述：
(Function Description) 2" InGaAs/InGaAsP/InP Epiwafer

3.相關法令、規章(附件)：無(None)
(Local Regulations for the Products Specified)

4.制定者：University of Virginia
(Specified By)

5.制定日期：2020/12/22
(Date of Specification)

6.規格制定：
(Specifications)

序號 (No.)	規格需求項目 (Item Name)	規格值 (Value for Customer)	單位 (Unit)	誤差 (DP)	工作條件 (Test Condition)	備 註 (Note)
0	S.I.-InP Substrate (Material no:M02032)	Fe-Doped	cm^{-3}	---	---	2" wafer, 355±15μm
1	U-InP Buffer Layer	0.1	μm	±10%	---	---
2	U-InAlAs	0.49	μm	±10%	---	---
3	U-InGaAs	0.01	μm	±10%	---	---
4	U-InP Layer	3.0	μm	±10%	---	---
5	U-1.1μm InGaAsP	1.1	μm	±10%	---	---
6	N^+-1.1μm InGaAsP (Concentration)	0.3 ($1x10^{19}$)	μm (cm^{-3})	±10% (±20%)	---	---
7	N-1.1μm InGaAsP (Concentration)	0.3 ($1x10^{16}$)	μm (cm^{-3})	±10% (±20%)	---	---
8	N-1.2μm InGaAsP (Concentration)	0.05 ($1x10^{17}$)	μm (cm^{-3})	±10% (±20%)	---	---
9	N-1.4μm InGaAsP (Concentration)	0.015 ($1x10^{16}$)	μm (cm^{-3})	±10% (±20%)	---	---
10	N-1.53μm InGaAsP (Concentration)	0.015 ($1x10^{16}$)	μm (cm^{-3})	±10% (±20%)	---	---
11	N-InGaAs (Concentration)	0.1 ($1x10^{16}$)	μm (cm^{-3})	±10% (±20%)	---	---
12	P-InGaAs (Concentration)	0.04 ($6x10^{17}$)	μm (cm^{-3})	±10% (±20%)	---	---
13	P-InGaAs (Concentration)	0.04 ($7x10^{17}$)	μm (cm^{-3})	±10% (±20%)	---	---
14	P-InGaAs (Concentration)	0.04 ($8x10^{17}$)	μm (cm^{-3})	±10% (±20%)	---	---
15	P^+-InGaAs (Concentration)	0.04 ($1x10^{18}$)	μm (cm^{-3})	±10% (±20%)	---	---
16	P^+-InGaAs (Concentration)	0.03 ($3x10^{18}$)	μm (cm^{-3})	±10% (±20%)	---	---
17	P^+-InGaAs (Concentration)	0.03 ($5x10^{18}$)	μm (cm^{-3})	±10% (±20%)	---	---

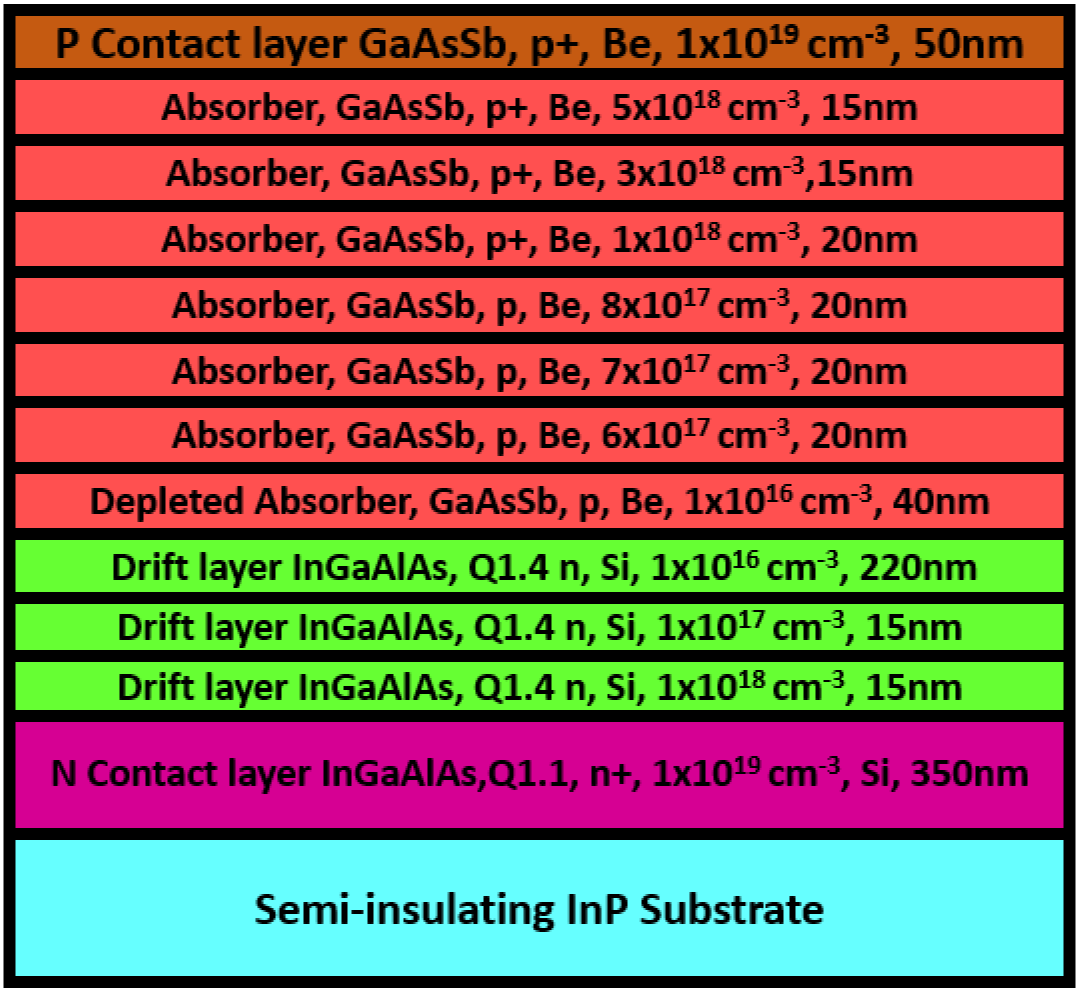
規需 2012101

保存年限： 15 年　　密等：密　　頁次：1/2

18	P$^+$-1.4μm InGaAsP (Concentration)	0.015 (2×10^{18})	μm (cm^{-3})	$\pm$10% ($\pm$20%)	---	---
19	P$^+$-1.1μm InGaAsP (Concentration)	0.015 (2×10^{18})	μm (cm^{-3})	$\pm$10% ($\pm$20%)	---	---
20	P$^+$-InP (Concentration)	0.3 (2×10^{18})	μm (cm^{-3})	$\pm$10% ($\pm$20%)	C-V measurement	On test wafer
21	P$^+$-InGaAs (Concentration)	0.05 (1×10^{19})	μm (cm^{-3})	$\pm$10% ($\pm$20%)	---	---
#	Lattice Mismatch	<$\pm$1000	ppm	---	DCXD measurement	Test on center of epiwafer

Note:The out-diffusion of dopant can't be avoided.The doping profile will not be guaranteed.

Appendix III (Epitaxy wafer for zero-bias waveguide PD)



P Contact layer GaAsSb, p+, Be, 1x10^{19} cm^{-3}, 50nm

Absorber, GaAsSb, p+, Be, 5x10^{18} cm^{-3}, 15nm

Absorber, GaAsSb, p+, Be, 3x10^{18} cm^{-3},15nm

Absorber, GaAsSb, p+, Be, 1x10^{18} cm^{-3}, 20nm

Absorber, GaAsSb, p, Be, 8x10^{17} cm^{-3}, 20nm

Absorber, GaAsSb, p, Be, 7x10^{17} cm^{-3}, 20nm

Absorber, GaAsSb, p, Be, 6x10^{17} cm^{-3}, 20nm

Depleted Absorber, GaAsSb, p, Be, 1x10^{16} cm^{-3}, 40nm

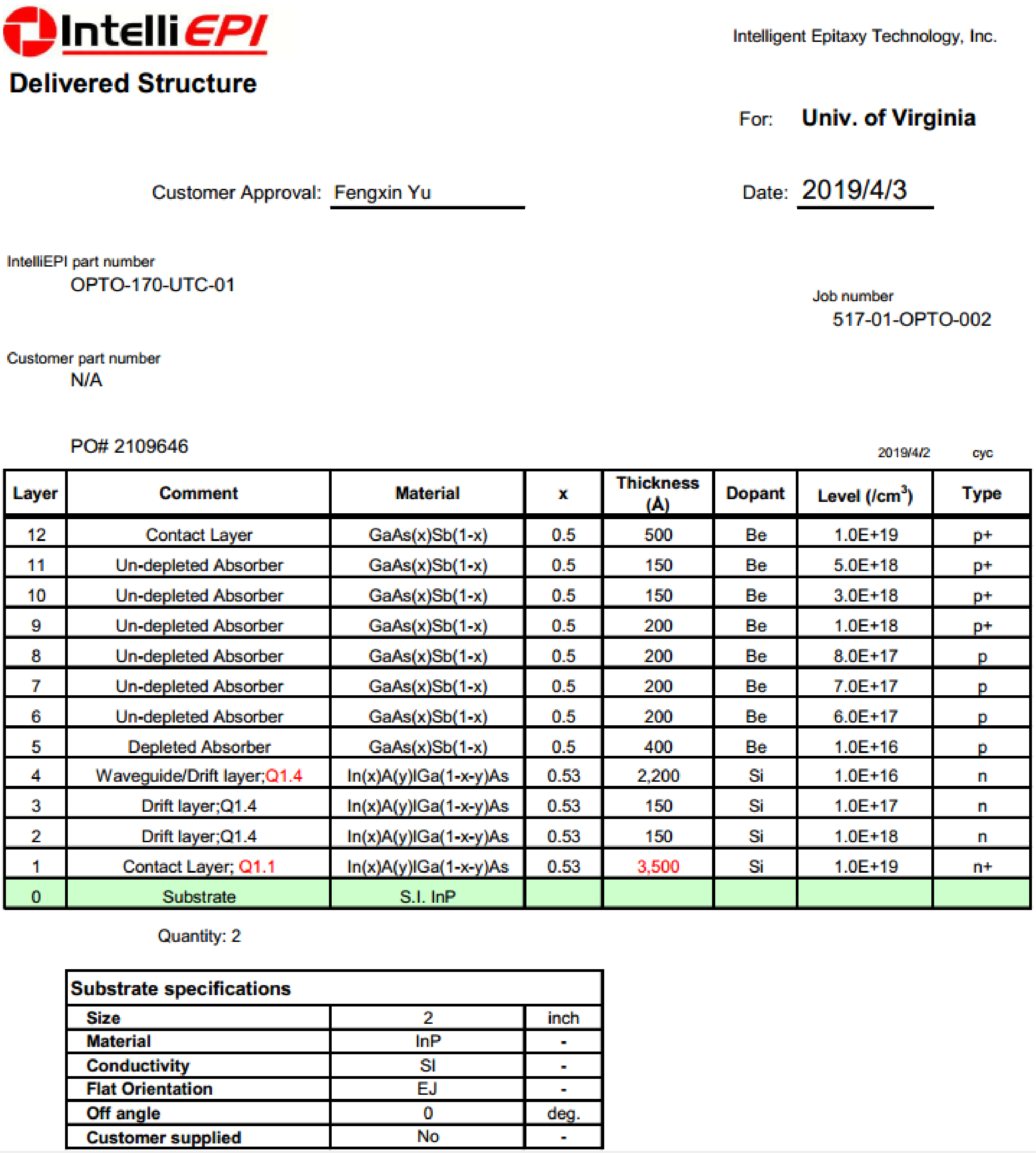
Drift layer InGaAlAs, Q1.4 n, Si, 1x10^{16} cm^{-3}, 220nm

Drift layer InGaAlAs, Q1.4 n, Si, 1x10^{17} cm^{-3}, 15nm

Drift layer InGaAlAs, Q1.4 n, Si, 1x10^{18} cm^{-3}, 15nm

N Contact layer InGaAlAs,Q1.1, n+, 1x10^{19} cm^{-3}, Si, 350nm

Semi-insulating InP Substrate



IntelliEPI

Delivered Structure

Intelligent Epitaxy Technology, Inc.

For: **Univ. of Virginia**

Customer Approval: Fengxin Yu

Date: 2019/4/3

IntelliEPI part number
OPTO-170-UTC-01

Job number
517-01-OPTO-002

Customer part number
N/A

PO# 2109646

2019/4/2 cyc

Layer	Comment	Material	x	Thickness (Å)	Dopant	Level (/cm^3)	Type
12	Contact Layer	GaAs(x)Sb(1-x)	0.5	500	Be	1.0E+19	p+
11	Un-depleted Absorber	GaAs(x)Sb(1-x)	0.5	150	Be	5.0E+18	p+
10	Un-depleted Absorber	GaAs(x)Sb(1-x)	0.5	150	Be	3.0E+18	p+
9	Un-depleted Absorber	GaAs(x)Sb(1-x)	0.5	200	Be	1.0E+18	p+
8	Un-depleted Absorber	GaAs(x)Sb(1-x)	0.5	200	Be	8.0E+17	p
7	Un-depleted Absorber	GaAs(x)Sb(1-x)	0.5	200	Be	7.0E+17	p
6	Un-depleted Absorber	GaAs(x)Sb(1-x)	0.5	200	Be	6.0E+17	p
5	Depleted Absorber	GaAs(x)Sb(1-x)	0.5	400	Be	1.0E+16	p
4	Waveguide/Drift layer;Q1.4	In(x)A(y)lGa(1-x-y)As	0.53	2,200	Si	1.0E+16	n
3	Drift layer;Q1.4	In(x)A(y)lGa(1-x-y)As	0.53	150	Si	1.0E+17	n
2	Drift layer;Q1.4	In(x)A(y)lGa(1-x-y)As	0.53	150	Si	1.0E+18	n
1	Contact Layer; Q1.1	In(x)A(y)lGa(1-x-y)As	0.53	3,500	Si	1.0E+19	n+
0	Substrate	S.I. InP					

Quantity: 2

Substrate specifications		
Size	2	inch
Material	InP	-
Conductivity	SI	-
Flat Orientation	EJ	-
Off angle	0	deg.
Customer supplied	No	-

A. List of Publications

1. **Fengxin Yu**, Keye Sun, and Andreas Beling. "Large-Area High-Power Modified Uni-Traveling Carrier Photodiodes." *2018 IEEE Photonics Conference (IPC)*. IEEE, 2011.
2. **Fengxin Yu**, Keye Sun, Qianhuan Yu, and Andreas Beling. "Zero-bias high-speed evanescently coupled waveguide Type-II UTC photodiode." In *Optical Fiber Communication Conference*, pp. W4G-6. Optical Society of America, 2020.
3. **Fengxin Yu**, Keye Sun, Qianhuan Yu, and Andreas Beling. "High-speed evanescently-coupled waveguide type-II MUTC photodiodes for zero-bias operation." *Journal of Lightwave Technology* 38, no. 24 (2020): 6827-6832.
4. **Fengxin Yu**, Keye Sun, Junyi Gao, and Andreas Beling. "32GHz high-power MUTC waveguide photodiode for 1310nm." In *Optical Fiber Communication Conference*, Optical Society of America, 2022.
5. **Fengxin Yu**, Ta-Ching Tzu, Junyi Gao, Chris Reyes, Keye Sun and Andreas Beling. " O-band High-Speed MUTC Waveguide Photodiodes on SiN/Si platform using Micro-Transfer-Printing Integration." *Journal of Selected Topics in Quantum Electronics* (2022) in preparation.
6. Xiangwen Guo, Linbo Shao, Lingyan He, Kevin Luke, Jesse Morgan, Keye Sun, Junyi Gao, Ta-Ching Tzu, Yang Shen, Dekang Chen, Bingtian Guo, **Fengxin Yu**, Qianhuan Yu, Masoud Jafari, Marko Lončar, Mian Zhang, and Andreas Beling, "High-performance modified uni-traveling carrier photodiode integrated on a thin-film lithium niobate platform," *Photon. Res.* 10, 1338-1343 (2022)
7. Qianhuan Yu, Ze Wang, Keye Sun, **Fengxin Yu**, Jizhao Zang, Joe C Campbell, Andreas Beling, “Zero-Bias GaAsSb/InP Photodiode with 40 GHz Bandwidth.” In 2018 IEEE Photonics Conference (IPC) (pp. 1-2). IEEE (2018)
8. Beling, Andreas, Ta Ching Tzu, Junyi Gao, Jesse S. Morgan, Keye Sun, Nan Ye, Bassem Tossoun, **Fengxin Yu**, and Qianhuan Yu. "High-speed integrated photodiodes." In *2019 24th OptoElectronics and Communications Conference (OECC) and 2019 International Conference on Photonics in Switching and Computing (PSC)*, pp. 1-3. IEEE, 2019.

B. Vita

Fengxin Yu (余丰心), son of Linzhang Yu (余林章) and Xiang Huang (黄香), was born on March 16th, 1995 in Wuhan, Hubei Province, China. After completing his study at First High School Affiliated to Central China Normal University in 2013, he began his undergraduate study at Huazhong University of Science and Technology (HUST), majoring in Optoelectronic Information Science and Engineering. In August 2017, he joined Dr. Andreas Beling's group as a Ph.D. student at University of Virginia. His current research focuses on the high performance photodiodes and their applications in analog photonic links and silicon photonics.

This dissertation has been typed by the author.