Foundry-Enabled High-Power Photodetectors and Micro-Transfer Printable Mach-Zehnder Modulator for Microwave Photonic Applications

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APPROVAL SHEET

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Abstract

Integrated microwave photonics is being considered the next cornerstone for reducing size, weight, and power (SWaP) in next generation microwave photonic systems. To realize an integrated microwave photonic system, CMOS-compatible and heterogeneously integrated III-V-on-silicon photonic platforms are two promising approaches that have been developed over the past decade based on the growing maturity of advanced semiconductor fabrication technology in photonics. Since high-speed photodetectors and modulators are key components inside a microwave photonic system, significant research has been devoted recently on developing fully integrated photodetectors and modulators on Si and other photonic platforms. This to be the research motivation, my dissertation is structured into three main topics: (1) high-power arrayed photodetector, traveling-wave photodetector, and group array photodetector combiner enabled by a silicon foundry platform for microwave photonic applications, (2) micro-transfer printable InP-based O-band multi-quantum well Mach-Zehnder modulator, and (3) heterogeneously integrated III-V-on-silicon distributed array photodetector.

In the first part of my work, an 8-element photodetector array with a record-high 14.3 dBm RF output power at 5 GHz has been demonstrated using AIM Photonics foundry. To expand the bandwidth and overcome the resistance-capacitance (RC) bandwidth limitation, I developed a new traveling-wave photodetector with integrated biasing circuit with 32 GHz bandwidth and 6 dBm output power at 44 mA photocurrent. An integrated 20 GHz receiver based on a pair of balanced photodiodes and a Mach-Zehnder delay line interferometer was also successfully demonstrated in an optical phase-modulated link. Balanced photodiodes are a vital component in some analog photonic links to suppress common mode noise, and a novel balanced traveling-wave photodetector with fully integrated biasing circuit was introduced to improve the radio frequency (RF) performance demonstrating a 25 GHz bandwidth and 30 dB common mode rejection ratio. Finally, a new 32-PD fully distributed group array photodetector combiner has been demonstrated with 15 GHz bandwidth which can be used as a massive RF power combiner inside a microwave photonic system. Also, I developed a balanced type of the group array photodetector combiner with 13 GHz bandwidth and 30 dB common mode rejection ratio.

In the second part of my work, I report a > 67 GHz bandwidth InP-based transfer printable multi-quantum well Mach-Zehnder modulator (MZM) with 17 dB extinction ratio at 1310 nm

wavelength. A clear 40 Gbps optical eye diagram is presented to show its large signal modulation ability. To the best of my knowledge, this is the first high-speed multi-quantum well MZM for 1310 nm wavelength that has been reported. In this work, I have designed the undercut insensitive multimode interference coupler, and adapted the concept to the modulator fabrication process development. ~ 1dB excess loss was achieved. Finally, initial results from transfer-printed modulators on a SiN photonic platform are reported with measurement results and process flow analysis.

In the final part of my work which will be continued as the future work, I used heterogeneously integrated uni-traveling carrier photodiodes to develop a group array photodetector combiner with improved RF output power. Design and simulated RF performance of the device are presented in this work followed by initial device fabrication, measurement results and analysis.

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Chapter 1 - Introduction and Motivation

1.1 - Microwave photonic system

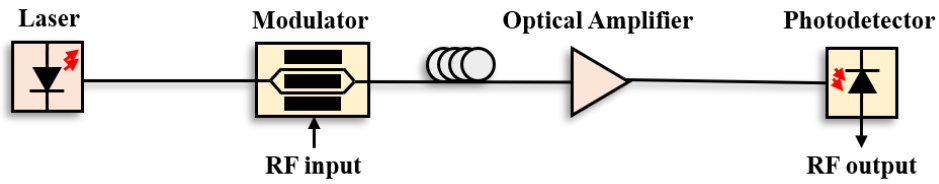


Figure 1.1 The fundamental building blocks of an analog photonic link.

Microwave photonic technologies have been developed for more than two decades. The applications in this field involve the frequency span from hundreds of MHz (RF domain) up to hundreds of GHz. Taking advantage of the ultra-wide bandwidth of fiber, broadband devices, low transmission loss, and immunity to electromagnetic interference, microwave photonic system can potentially be deployed in next-generation wireless communication systems, remote antenna systems, radio-over-fiber systems, and satellite communication systems [1]-[4]. A simple analog photonic link shown in the Fig. 1.1 is the backbone of this technology. It includes an electrical-to-optical (E/O) converter (laser and modulator), optical fiber as the low-loss transmission medium, optical amplifier (optional), and an optical-to-electrical (O/E) converter (photodetector). For the EO converter, a directly modulated laser or, as shown here, a continuous wave (CW) laser followed by a Mach-Zehnder modulator (MZM) as the external modulation source can be used depending on the desired modulation bandwidth. The RF signal is fed into the modulator to implement EO conversion using the optical signal sent from the laser and pass through the optical fiber to finally arrive at the photodetector for the OE conversion. Since high-fidelity analog signal transmission is essential in analog photonic links, signal-to-noise ratio (SNR), spur-free Dynamic Range (SFDR), and bandwidth are often the three important figures of merit to be investigated for optimizing a system. To maximize SNR, components that have low noise and high-power handling capability are beneficial. Usually this requires a high-power CW laser that has low relative intensity noise (RIN), together with a modulator and photodetector that can work under high power and support the desired bandwidth and high linearity. Such a link has the potential to reach a high

link RF gain with large dynamic range [5,6]. To this end, developing high-power photodetectors and modulators for the next-generation analog photonic links and microwave photonic applications has become the motivation of my PhD research.

1.2 - Si photonics foundry and heterogeneous Si platform

While the microwave photonics field has been growing, integrated photonics is the other revolutionary technology that has matured and increasingly shifted to the commercializing stage in the past few years. Integrated photonics is a promising technology for a wide range of applications including communications, sensing, and computing. However, this growing momentum has been mainly focused on digital applications including high-capacity data communication system and optical interconnects [7]-[10]. Due to the growing maturity of the semiconductor industry, the realization of low cost and mass producible integrated photonics has become more feasible for the photonics industry [11]-[15]. To this end, integrated microwave photonic systems have gained more attention because this could eventually transition the microwave photonic system to a small size, weight, and power form factor with higher performance instead of using all individual optical components for building up the whole bulky system [16]-[18].

Presently, the two main platforms for integrated photonics are silicon-on-insulator (SOI) [12,13] and the heterogeneous III-V-on-silicon platform [19]. SOI or Si photonics has been developed mostly for the datacom and telecom industries for the past decade. The key advantage of this platform is that except for the light source, almost all active and passive components can be fabricated on the same wafer, while having the potential for integration with electronics circuits together on the same fab run to achieve low cost and mass production. However, the laser continues to be an issue to be resolved on this platform since silicon is not an ideal material for light sources which means that III-V-based external light sources will be needed in the near future. Apart from the light source, another downside of using silicon photonics integrated microwave photonic systems is the optical waveguide loss due to two photon absorption (TPA) induced by high optical power in Si [20]. In addition, silicon-based high-speed modulators and photodetectors cannot currently reach the performance of their III-V-based (for photodetectors) and lithium niobate based (for modulators) counterparts in terms of linearity and high-power handling capability that is

critical for most RF photonic applications. Take photodetector for example, InP has higher electron mobility than Ge which means that the RF output power of a Ge-PD based on a p-i-n structure will be dominated by the space charge effect at lower optical injection than a InP p-i-n structure. Also, taking the advantage of ternary and quaternary lattice-matched compounds of the III-V material system, we can design various types of uni-traveling carrier photodetectors (UTC-PD) using bandgap engineering to reduce the space charge effect and improve power handling capability. However, for the UTC Ge-PD [21-23], the options are limited to silicon and germanium, and the other issue is that Ge is not lattice-matched to Si which makes the dark current larger which can be a problem at high reverse bias.

To this end, converging different material systems together has become the most promising path for next generation integrated RF photonic systems. One of the popular and already commercialized heterogenous integration techniques is die-to-wafer or wafer-to-wafer bonding. The very first heterogeneously integrated III-V-on-Si laser was introduced in 2006 using the wafer bonding technique [24]. Followed by that, several papers have demonstrated heterogeneously integrated III-V on Si low noise lasers [25], high-speed and high-linearity modulators [26,27], and uni-traveling carrier photodiodes (UTC-PD) with high power handling capability [28]. However, the two-photon absorption remains an issue in the silicon waveguide of the devices on this heterogenous platform. Hence, the research focus has been shifted to heterogeneously integrated III-V-on-SiN/Si platforms recently due the fact that SiN waveguides are not affected by the two-photon absorption at the telecom wavelength at 1550 nm. In 2020, the very first UTC-PD heterogeneously integrated on the SiN platform was demonstrated using a wafer bonding technique that achieved 20 GHz bandwidth with 0.94 A/W (high responsivity) and 20 nA dark current at 8V reverse voltage (low dark current) [29].

However, this wafer bonding technology lacks efficiency of III-V material use, and has limited integration density, in particular, when different III-V material stacks need to be integrated in close proximity on the same wafer. Therefore, micro-transfer printing (micro-TP) technology, as another promising alternative, was introduced [30]-[32]. In micro-TP, the idea is to pick micron-sized devices (chiplets) in a massively parallel way from a source substrate and place them onto a target substrate with high alignment accuracy. In this way, the efficiency of source material used can be

improved and no modification of the silicon photonics back-end process flow is necessary. To date, there are several reports on micro-transfer printed lasers, optical amplifiers, and photodetectors, [33]-[35] but, a modulator has not been demonstrated yet. To this end, developing a micro-transfer printable modulator on the SiN platform has been another goal of my PhD research work.

1.3 - Overview of the dissertation

My dissertation is organized as follows:

The first part of the work includes 3 chapters with the focus on using one of the leading Si photonics foundry platforms - AIM photonics, to develop Ge-on-Si high-power photodetectors for microwave photonic applications.

- Chapter 2 - this chapter gives an overview of waveguide-based high-power photodetectors and addresses the limiting factors for high power photodetector performance. Next, pros and cons of using Ge-on-Si or III-V-on-Si based photodetectors for high-power is reviewed. Finally, the traveling-wave PD concept is introduced by describing how both, Ge-on-Si and III-V-on-Si based PDs can be incorporated into a distributed circuit.
- Chapter 3 - utilizing the AIM Photonics platform with its process design kit (PDK), arrayed photodetectors are reported to demonstrate high RF output power but with rather limited bandwidth due to the RC time constant. A balanced photodetector integrated with MZI delay line is introduced together with a phase modulated analog photonic link demonstration as an example of a fully integrated microwave photonic receiver.
- Chapter 4 - a distributed circuit concept is used to incorporate the arrayed photodetectors in order to improve the bandwidth performance and to further improve the bandwidth × saturation current product. Moreover, a traveling-wave photodetector integrated with an on-chip biasing circuit is introduced. In this work, a balanced traveling-wave photodetector with integrated biasing circuit design is also presented for the first time. The limiting factors in terms of bandwidth and power handling capability are discussed.

The second part of my work includes the demonstration of a transfer printable InP-based Mach-Zehnder modulator (MZM).

- Chapter 5 - firstly, the working principle of MZM is reviewed. Next, the fabrication process flow of the modulator will be explained. Then, the InP-based bar level modulator design and measurement results are reported. Initial results from transfer printed modulators will be reported with future work for improvements.

The final part of my work presents the conclusion and future work

- Chapter 6 - firstly, the conclusion of the dissertation will be given. Then, III-V-on-Si heterogeneously integrated GAPC will be introduced. This work uses heterogeneously integrated III-V-on-Si PDs based on the wafer bonding technique for demonstrating the Group Array Photodetector Combiner (GAPC) concept. The device design is introduced followed by the fabrication process flow and some initial measurement results. Future improvements are discussed.

Chapter 2 - Overview of the Waveguide High-Power Photodetector

2.1 - Ge-on-Si-based p-i-n photodetector

The two important figures of merit of a p-i-n PD for supporting high power operation are the bandwidth and RF saturation current. The bandwidth is generally limited by the carrier transit time and the RC time constant which is explained in the Fig. 2.1.

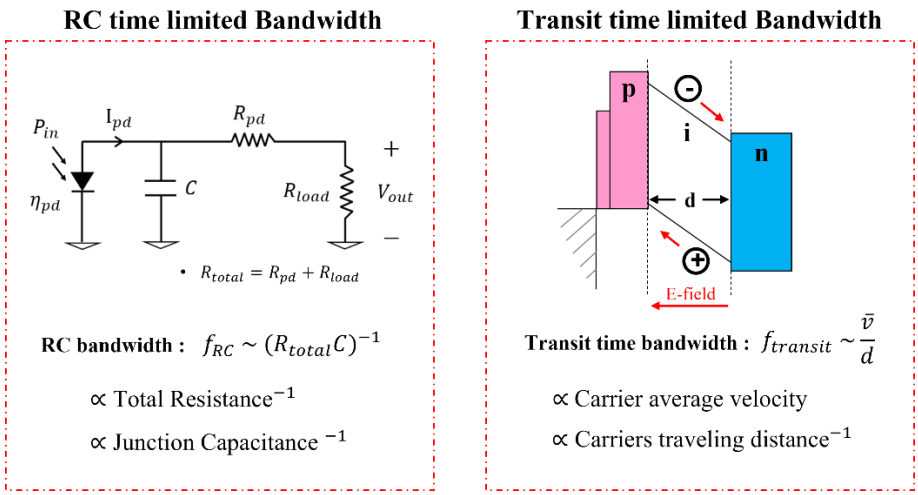


Fig. 2.1 Bandwidth limiting factors in a p-i-n PD structure.

$$C = \frac{\varepsilon_0 \varepsilon A}{d} \qquad \textbf{Eq 2.1}$$

The transit time bandwidth (right side of the Fig. 2.1) is generally limited by the thickness d of the intrinsic layer e.g. Ge. When using a foundry process, d is fixed. On the other hand, the RC limited bandwidth (left side of the Fig. 2.1), is determined by the photodiode series resistance (R_{pd}) from the contact layers (including contact resistance) and the junction capacitance determined by the area A of the (Ge) active region and the depletion width d which is described in equation 2.1 based on the parallel plate capacitor model. To be noted that ε_0 and ε represent the permittivity of free space in vacuum and the dielectric constant of Ge. Generally, to improve the 3-dB bandwidth when depletion width d is fixed, minimizing the RC bandwidth is considered the first approach. However, to achieve high RF output power and high 1-dB compression current, reducing the active area is not an option since high optical input power in a relatively small active PD area can eventually

cause thermal failure in addition to the heat sinking problem in the active region. Another reason why scaling down the area is not a good idea is that the photocurrent density gets larger in smaller PDs which means saturation occurs at a lower photocurrent. Also, a simple p-i-n structure suffers from the well-known space charge effect when the PD is operated under high optical input power. Under high level optical injection, a significant number of electron-hole pairs will be generated. Holes are accumulated near the interface between intrinsic layer and p-contact layer because the drift velocity of the holes is around 49% slower than the drift velocity of electrons which reduces the average carrier velocity ($\bar{v}$). The hole accumulation together with the electrons in the i-layer cause the electrical field to collapse which slowdowns the carrier velocities and extends the transit time, which reduces the bandwidth and saturates the RF output power. To date, several high-power Ge-PDs have been demonstrated by various Si photonics foundries. Most of the works have focused on customized designs of the PD to minimize the space charge effect induced bandwidth degradation and power saturation [36]-[38]. A few works, including the one in this dissertation, have instead addressed the problem on a circuit level, by demonstrating arrayed photodetectors [39]-[40]. The concept is shown in Fig. 2.2. By splitting the optical input to multiple waveguides that feed into multiple photodetectors that are combined in parallel, the optical power incident on each PD is reduced and the space charge effect can be mitigated. However, this approach suffers from a decreased RC limited bandwidth since the total capacitance scales with the number of PDs in the array. Using my work [40] as an example, the overall bandwidth trends (estimated vs. measured) are shown in the Fig. 2.3 based on the equation 2.2.

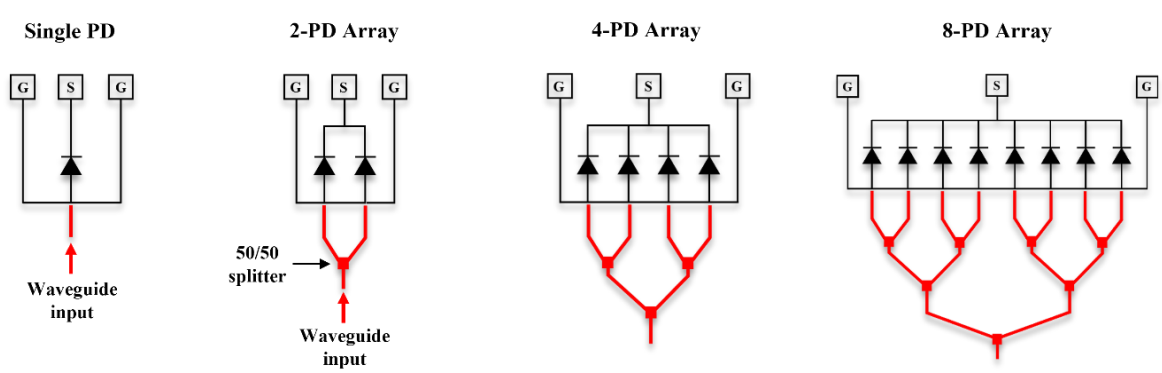


Fig. 2.2 Schematics of n-PD arrays.

$$f_{PD} = \sqrt{\frac{1}{1/f_{RC}^2 + 1/f_{Transit}^2}} \qquad \textbf{Eq 2.2}$$

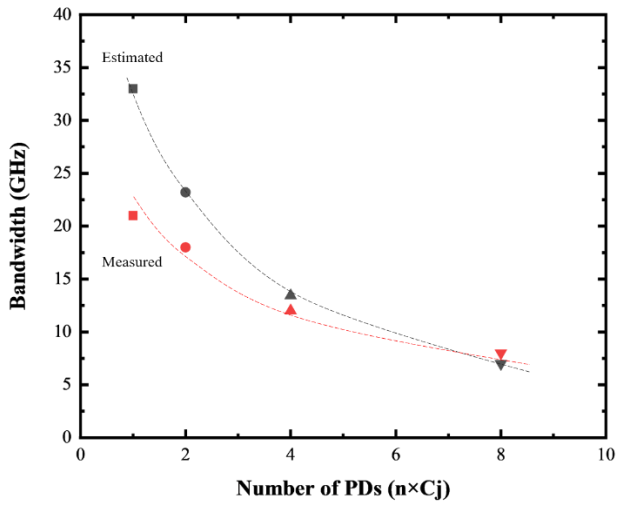


Fig. 2.3 Expected and measured bandwidth vs. PD count n in the array.

2.2 - III-V-on-Si uni-traveling carrier photodetector

In contrast to Ge-on-Si based PDs, the III-V uni-traveling carrier PD (UTC-PD) is well-known for its high power and high bandwidth performance and its application in microwave photonic systems [41]-[43]. With the development of heterogeneous integration techniques, III-V UTC-PDs on silicon waveguides are now possible [24],[44]-[45] and have become another solution when high power high-speed photodetection is required. Recently, CMOS foundries have also been developing heterogenous integration techniques for the laser integration [46]. This could ultimately lead to mature foundry-enabled III-V-on-Si platforms that not only provide integrated lasers but also high-performance modulators, photodetectors, and other components that may need IIIV-on-Si based devices.

Figure 2.4 shows a comparison between a p-i-n PD and a UTC-PD. In a p-i-n PD, shown in figure 2.4 (left); electrons and holes contribute to the output current in both, UTC and pin PDs. The difference is that there is no hole drift current in the UTC. Due to the difference in carrier drift velocities, the 3-dB bandwidth is typically dominated by the slower hole transport. The UTC-PD shown in figure 2.4 (right), on the other hand, consists of a quasi-neutral (p-type) absorption layer

and a wide bandgap, depleted electron drift (collection) layer. The minority electrons that are generated in the absorption layer will diffuse and/or drift into the collection layer. There is also a diffusion block layer that provides electrons unidirectional motion toward the collection layer. Also, by forming a graded bandgap or graded doping, a small electric field in the absorption layer is generated, which makes it possible to reduce the electron diffusion time effectively. Because holes are the majority carriers, their transport behavior depends on the electron current. This makes the fast electrons the dominant carriers in the photo-response of a UTC-PD, and therefore their performance superior to that of a p-i-n PD. Noted that only the faster electrons drift through the collection layer. Therefore, less accumulation happens near the interface between the drift layer and the n-contact layer under the high optical injection which helps to significantly reduce the space charge effect to further improve the RF output power. While there is still a space charge effect in the drift layer due to electrons, the difference is that even if the electric field becomes smaller, electrons maintain relatively large velocity (in contrast to holes) so transit time does not increase much. Also, we have used space charge compensation through n-type doping (positive donor ions) that compensate some of the negative charge of the electrons [47]. Compared with Ge, III-V materials can take advantage of their material properties and offer quaternary and ternary compositions to form the UTC-PD structure.

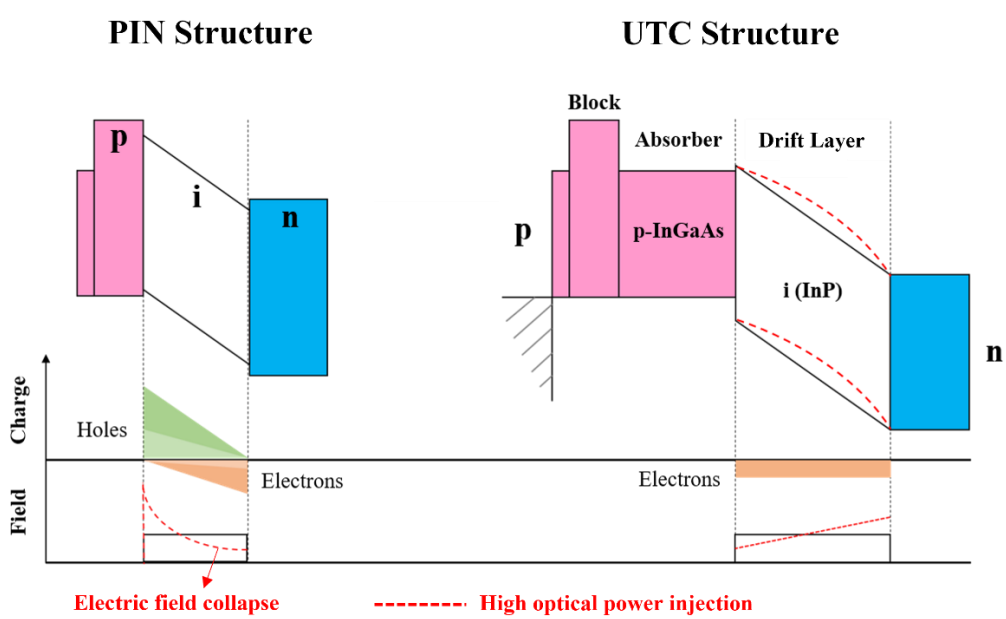


Fig. 2.4. Comparison between p-i-n and UTC PD.

2.3 - Traveling-wave photodetector

Previous works have addressed the high-power handling capability of Ge PDs and UTC PDs, mostly on the component level. Whether these are standalone PDs or arrayed PDs, in general the bandwidth performance remains limited by the RC time constant due to the lumped-element nature of the circuit when the shortest RF signal wavelength is much larger than the device length. To overcome the RC limitation, the PD array can be embedded in a fully distributed circuit to form a traveling-wave photodetector (TWPD). This concept represents a milestone to further improve the high power and bandwidth performance simultaneously [48]. Figure 2.5 compares a lumped photodetector circuit and a distributed circuit loaded photodetector. To be noted that R_s and C_j represent the series resistance and the junction capacitance of the photodiode. In the lumped PD array circuit, the PD series resistances are combined in parallel resulting in $R_{s'}$, which is connected in series with parallelly combined PD capacitances which is why this type of array is usually limited by the RC-time constant. And it should be mentioned that the PD series resistance R_s is usually small compared to the 50 Ω load, therefore, the combined $R_{s'}$ cannot compensate the increase in C_j. On the other hand, in a TWPD with capacitive loading, the PDs are incorporated into a high impedance transmission line for an impedance match to the external 50 Ω load. Ideally, when an RF signal is traveling along the TWPD, it will not 'see' the RC low-pass filter that can be calculated from the total capacitance in the circuit. In Fig. 2.5, R, L, G, and C represent the resistance, inductance, conductance, and capacitance per unit length of the transmission line.

Here, as an example, we take an 8-stage TWPD which is shown in the Fig. 2.6 (detailed design description will be given in the later sections). To be noted that TL denotes the single section length of the loaded transmission line. Since now we have expanded the PD array from a lumped-element circuit to a distributed circuit, the device length of a TWPD is comparable to the shortest wavelength of the RF signal so that optical and electrical waves can 'co-propagate' over some length so that now phase match becomes important. To this end, the electrical velocity is determined by the dimensions of the transmission line and the amount of capacitive loading and typically does not match the optical velocity in the Si waveguide. Hence, to ensure in-phase summation of the electrical signals at the external load, eight different optical delay lines are connected right after the 1-to-8 optical splitter. In the figure, τ represents the length of a single section optical delay line. These delay lines are designed to make sure that the RF signal from, for

example, PD1 arrives at the same time at the load as the RF signal from PD7. On the opposite side of the load, a 50 Ω termination R_{term} needs to be used to eliminate the back-reflected signal in order to mitigate potential deconstructive interference with the forward propagating signal. This will help to boost the bandwidth of the photodetector. Figure 2.7 illustrates this improvement by comparing a measured TWPD bandwidth to the lumped element PD arrays from figure 2.3. of the TWPD is added. We can see that the reported 8-stage TWPD achieves nearly the same bandwidth performance as a standalone PD but has the same PD count as the 8-PD array. This proves that the RC limitation has been overcome by using the distributed circuit.

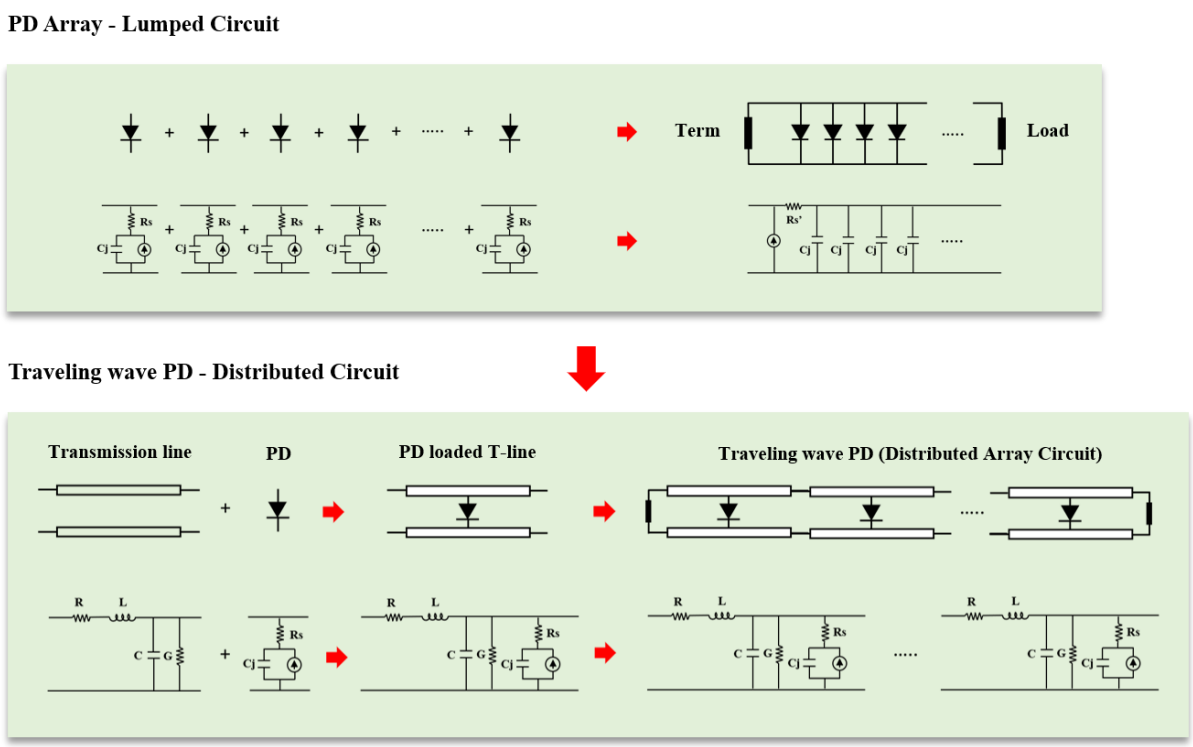


Fig. 2.5 Comparison of lumped PD array and traveling-wave PD circuit.

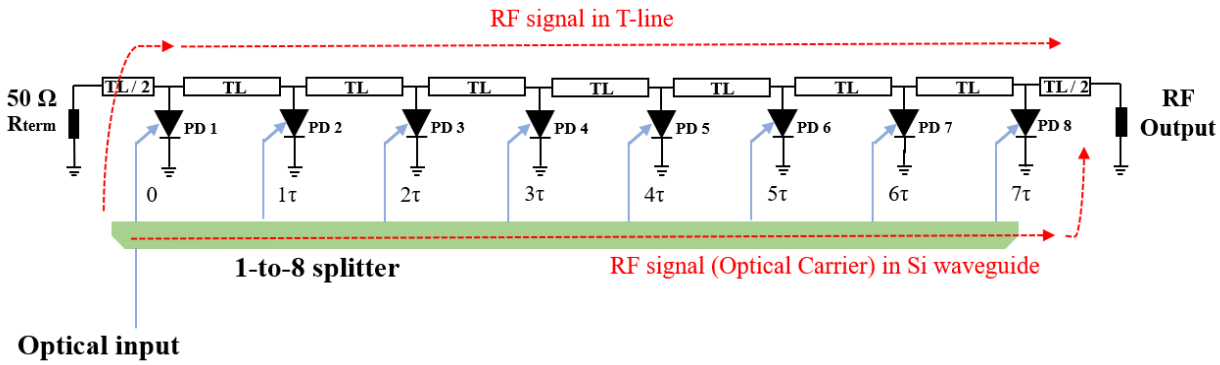


Fig. 2.6 Schematic of the 8-stage traveling-wave PD

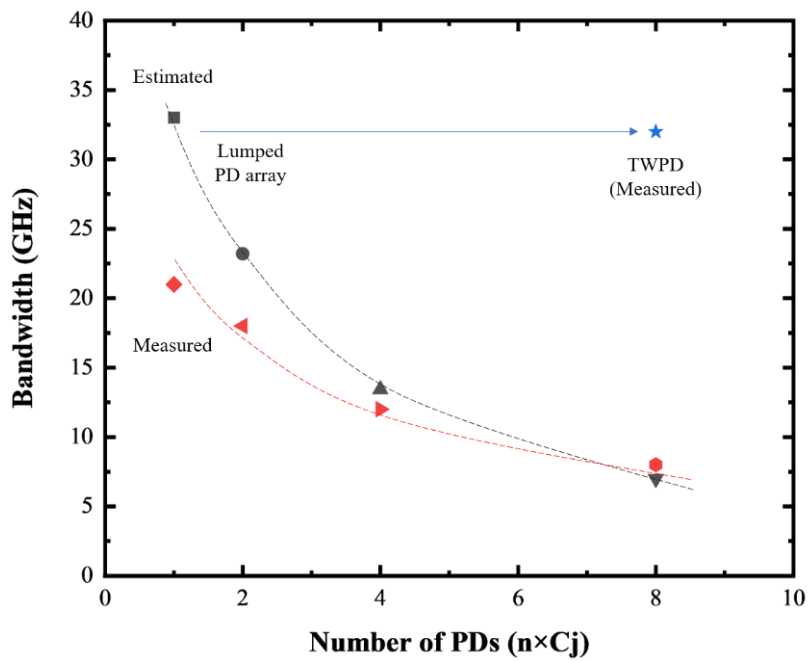


Fig. 2.7 Expected and measured bandwidth trend vs. PD count n in the array - lumped PD array vs. TWPD.

Chapter 3 - Foundry-Enabled High-Power Photodetectors for Microwave Photonics

3.1 - Introduction

In this chapter, I demonstrate arrayed germanium-on-silicon waveguide photodetectors for high-power analog applications utilizing the AIM Photonics silicon foundry. Photodetector arrays with 2, 4, and 8 elements reach output powers of -0.4 dBm, 10 dBm, and 14.3 dBm at 18 GHz, 12 GHz, and 5 GHz respectively. The 4-photodiode array has an output third order intercept point (OIP3) above 20 dBm up to 12 GHz and shows a 5-dB improvement over a single photodiode. An integrated 20 GHz receiver based on a pair of balanced photodiodes and a Mach-Zehnder delay line interferometer is successfully demonstrated in an optical phase-modulated link.

3.2 - PD Arrays

3.2.1 Device Layout

Fig. 3.1 (a) shows top view, schematic, and circuit representation of a single PD with a Si edge coupler for optical input coupling. The electrical output of the PD is extracted from the ground-signal-ground (GSG) probe pads on top of the dielectric layer. In order to improve the PD power handing capability, we designed PD arrays in which the optical input power is equally divided between several PDs to reduce the space charge effects and increase the saturation power. For the 2-PD array in Fig. 3.1 (b), the edge coupler is connected to a waveguide Y-junction to split the optical signal into two equal paths feeding two PDs that are connected in parallel through the shared GSG pad. Fig. 3.1 (c) and (d) show the 4- and 8-PD arrays that include three and 7 Y-junctions, respectively. The waveguide optical loss was 2.5 dB/cm at 1550 nm wavelength and the nominal insertion loss of the Y-junction was less than 0.35 dB. It should be noted that the silicon edge coupler of the 4-PD array is compatible with an interposer chip to facilitate future packaging. Moreover, we also studied designs with inductive peaking to enhance bandwidth. Fig. 3.2 (a) shows a single PD with an integrated spiral inductor which has the total area of an 80 µm × 80 µm. In Fig. 3.2 (b), a 70-µm long metal line was used to connect the PD array and the probe pads.

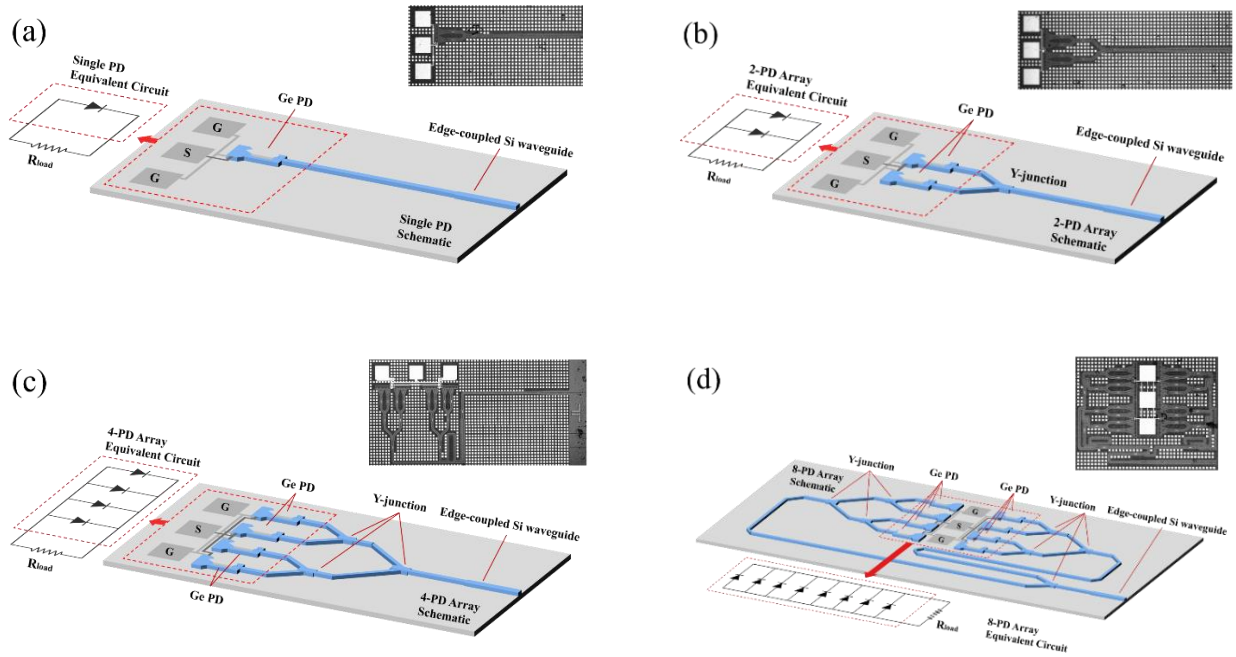


Fig. 3.1 Circuit representations (left), schematics (center), and top view pictures (right) of (a) a single analog PD, (b) a 2-PD array, (c) a 4-PD array, and (d) an 8-PD array. R_{laod} is the external load resistor.

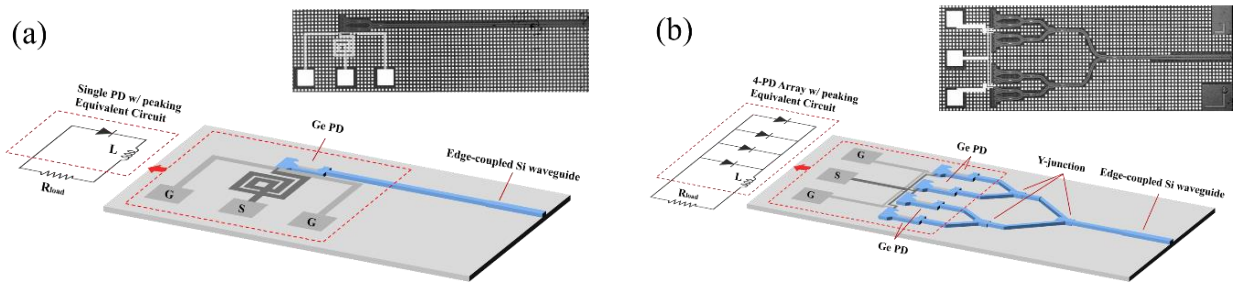


Fig. 3.2 Circuit representations (left), schematics (center), and top views picture (right) of (a) a single analog PD with integrated spiral inductor, and (b) a 4-PD array with enhanced inductive peaking. R_{laod} is the external load resistor.

3.2.2 DC Characterization

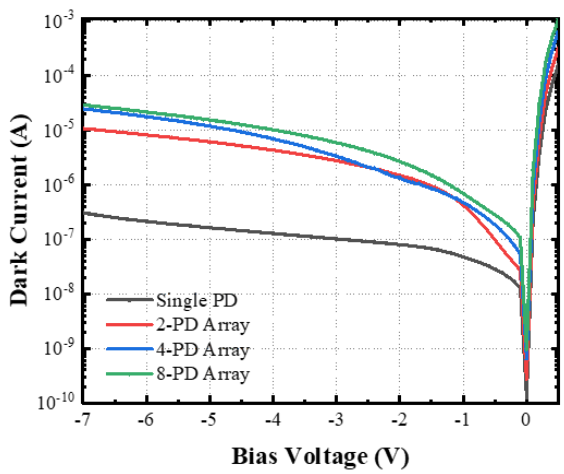


Fig. 3.3 I-V characteristics.

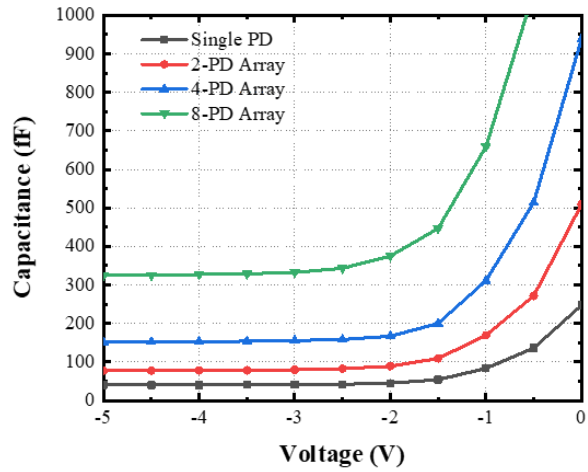


Fig. 3.4 C-V characteristics.

The current-voltage characteristics of a single PD, a 2-PD array, a 4-PD array and an 8-PD array are shown in Fig. 3.3. The dark current of a single PD is 1.6×10^{-7} A at -5 V. The total dark currents are 6×10^{-6} A, 1×10^{-5} A and 1.5×10^{-5} A at -5 V for the 2-, 4- and 8-PD arrays, respectively. We attribute the fact that the total dark does not scale exactly with the number of PDs in the array to variations in the Ge quality across the chip. The capacitance-voltage (C-V) characteristics of a single PD, a 2-PD array, a 4-PD array and an 8-PD array are shown in Fig. 3.4. Operation above a reverse voltage of 4 V fully depletes the PD at a capacitance of 40 fF. The capacitances of the 2-, 4-, and 8-PD arrays are 77 fF, 151 fF, and 324 fF, and scale well with the number of PDs in the array.

To measure the DC responsivity a polarization controller was used to adjust the optical signal polarization before it was launched into the Si waveguide edge coupler from a tapered fiber with 3 µm spot diameter. Single PDs had an external responsivity of (0.23±0.03) A/W at 1550 nm wavelength (no anti-reflection coating on the edge coupler facet). From the comparison with the nominal internal responsivity of 0.85 A/W, we estimated the coupling loss from the tapered fiber into the waveguide edge coupler to be around 5.7 dB in our measurements. The single PDs with spiral inductor, 2-PD arrays, 4-PD arrays, 4-PD arrays with long metal line, and 8-PD arrays had external responsivities of 0.22, 0.21, 0.22, 0.21 and 0.21 A/W (±0.03 A/W), respectively, indicating that we did not observe a significant drop in external responsivity for larger PD arrays.

This can be attributed to the low insertion loss of waveguides and Y-junctions and minor differences in the quality of the waveguide facets in our experimental devices.

3.2.3 RF Bandwidth

The frequency response under high photocurrent operation were carried out with an optical heterodyne setup that produces a tunable optical beat signal with nearly 100% modulation depth. The PDs were biased using a dc source meter (Keithley 2400) through a bias-tee connected to the microwave probe. The RF power was measured by a wideband power meter with 50 Ω input impedance. Fig. 3.5 (a)-(d) show the frequency responses of the single PD, the 2-PD array, the 4-PD array and the 8-PD array, respectively, under different photocurrents. At -5 V bias, the bandwidth of the single PD reaches 21 GHz at 3 mA and remains as high as 20 GHz at 7 mA. The 2-PD array has a bandwidth of 18 GHz at 3 mA, which reduces to 16 GHz at 15 mA. Bandwidths of 12 GHz and 10 GHz are achieved by the 4-PD array at 3 mA and 20 mA, respectively. Owing to its larger resistance-capacitance (RC) time constant, the 8-PD array has bandwidth of only 5 GHz at 3 mA and reaches to 8 GHz at 30 mA. The single PD with integrated spiral inductor has 35 GHz bandwidth at 3 mA and saturates at 32 GHz at 7 mA as shown in Fig. 3.6 (a). The inductance of the spiral inductor was extracted from S-parameters of a test structure. The equivalent circuit model is shown in Fig. 3.6 (b). The inductance, resistance and stray capacitance were determined to be 380 pH, 2 Ω and 10 fF, respectively. These values are similar to the values of the spiral inductor with similar dimensions reported in [49]. The measured and calculated bandwidth of the single PD with and without spiral inductor are shown in Fig. 3.6 (c). The transit time of the PD was taken into account in the circuit model as a frequency-dependent current source I(ω) in the circuit model. As can be seen, the calculation using the equivalent circuit model agrees well with the measurement results. Fig. 3.7 shows the frequency response of the 4-PD array with the extended metal line. Due to inductive peaking the bandwidth reaches 14 GHz at a photocurrent of 20 mA.

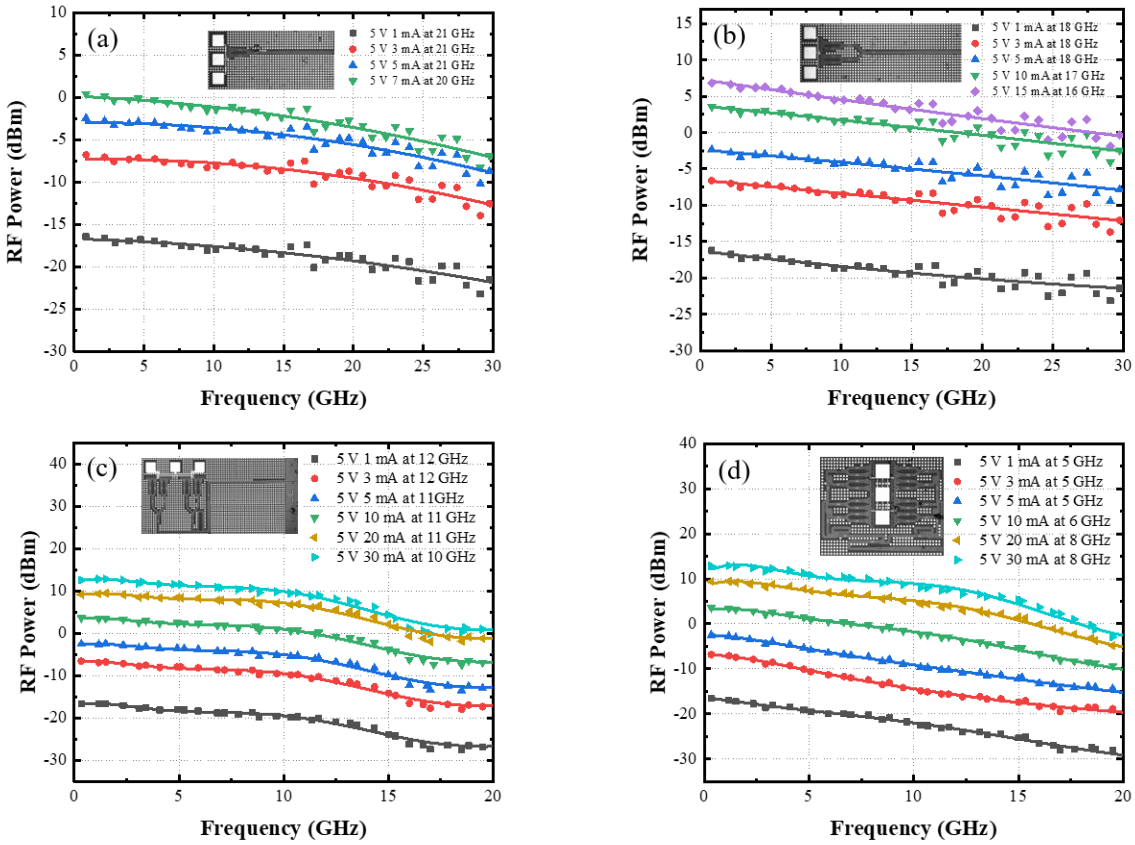


Fig. 3.5 Frequency responses of (a) a single PD, (b) 2-PD array, (c) 4-PD array and, (d) 8-PD array at various photocurrents.

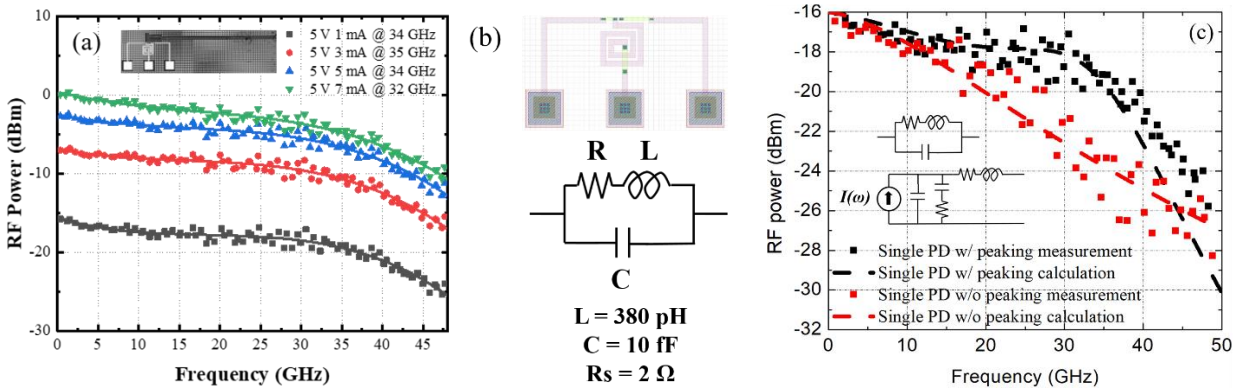


Fig. 3.6 Frequency responses of (a) a single PD with integrated spiral inductor; and (b) equivalent circuit model of spiral inductor. (c) Bandwidth measurements and calculation results of single PD with and without spiral inductor. The insets show the equivalent circuit model of the PD and spiral inductor used in the calculations.

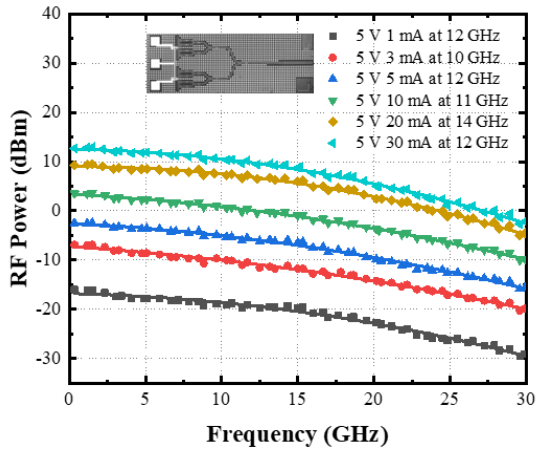


Fig. 3.7. Frequency response of 4-PD array with long metal wire at various photocurrents.

3.2.4 RF-Power Saturation

The saturation characteristics are measured by extracting the RF output power at a fixed frequency and gradually increasing the optical input power until the power meets the 1-dB compression point. Fig. 3.8 (a) shows the RF output power of the single PD at 5 GHz under various bias voltages. The saturation power (at 1-dB compression) reaches 2.5 dBm at an average photocurrent of 11 mA and 5 V. At the 3-dB bandwidth of 21 GHz, the output power saturates at -4.7 dBm and 6 mA (fig. 3.7 b). Fig. 3.9 (a) shows the RF output power of the 4-PD array at 5 GHz under various bias voltages. The saturation power reaches 13 dBm at the photocurrent of 36 mA and the reverse voltage of 5 V. When measured at the 3-dB bandwidth of 12 GHz, the output power saturates at 8 dBm at a photocurrent of 27 mA and 5 V (Fig. 3.9 (b)).

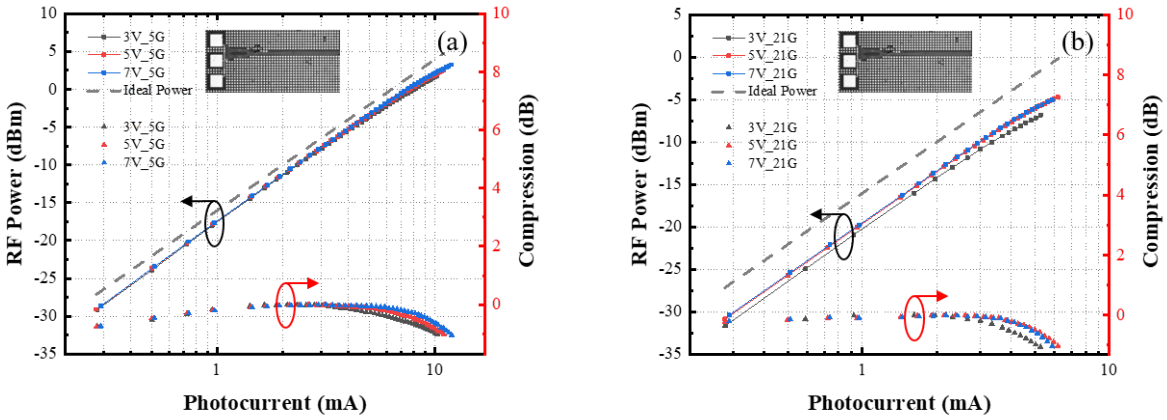


Fig. 3.8 Saturation current and power of a single PD at (a) 5 GHz and (b) at the 3-dB bandwidth of 21 GHz under different bias voltages.

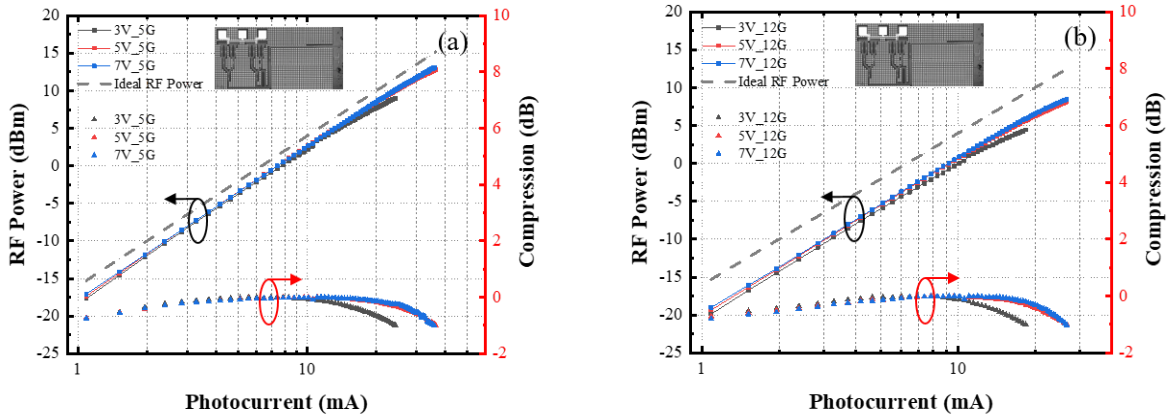


Fig. 3.9 Saturation current and power of a 4-PD array at (a) 5 GHz and (b) 3-dB bandwidth of 12 GHz under different bias voltages.

A summary of the saturation characteristics of our single and arrayed PDs at 5 GHz and -5 V bias are shown in Fig. 3.10 (a). The single PD saturates at 11 mA with 2.5 dBm output RF power. The saturation power reaches up to 9 dBm at 21 mA for the 2-PD array. The 4-PD array has a saturation power of 13 dBm at 36 mA. A similar, but un-saturated power of 14.3 dBm at 48 mA was measured for the 8-PD array. However, it should be mentioned that here the input optical power was the limitation as high-power damage of the silicon edge coupler was observed at photocurrents beyond 48 mA. The saturation current of the 8-PD array is expected to be as high as 70 mA. Fig. 3.10 (b) shows a comparison of the saturation characteristics measured at the 3-dB bandwidths and -5 V. For the single PD, we find that by utilizing the spiral inductor for bandwidth enhancement from 21 GHz to 34 GHz, the saturation power remains unchanged at -5 dBm. For the 4-PD array with 70-μm long metal line, a high saturation power of 10 dBm at 31 mA is achieved.

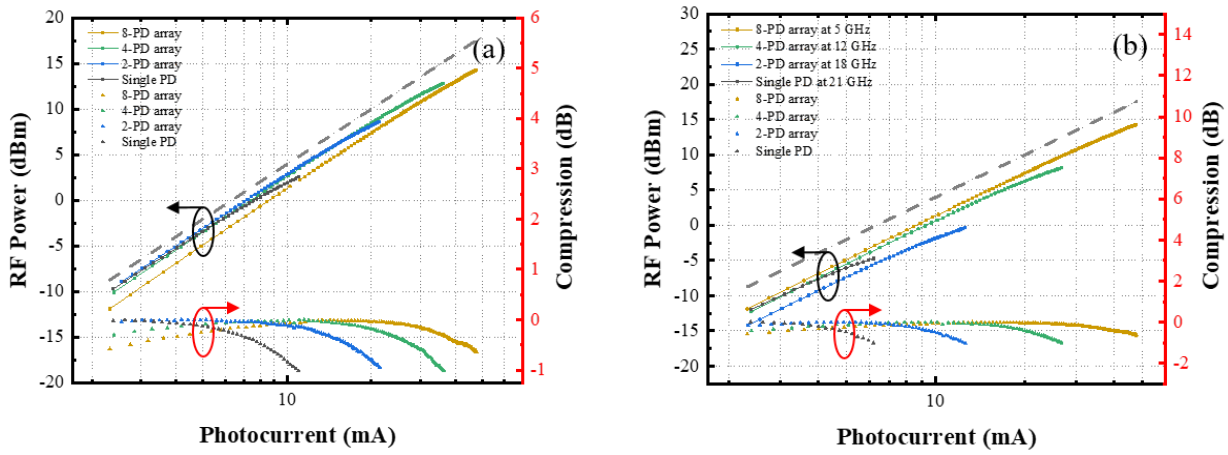


Fig. 3.10 Summary showing output power and compression at (a) 5 GHz and (b) the 3-dB bandwidth frequency of the devices in this study.

3.2.5 Output third-order intercept point (OIP3)

To determine photodetector linearity, we measured the OIP3 with a three-tone setup similar to the one described in [50]. Fig. 3.11 shows the frequency dependence of the OIP3 for the 4-PD array and a single PD at photocurrents of 15 mA and 30 mA. Owing to a reduced space charge effect in the photodiodes of the 4-PD array at 5 V reverse bias, the OIP3 reaches 27.5 dBm at low frequency and remains above 20 dBm up to 12 GHz and 30 mA. In contrast, the OIP3 of the single PD at the highest measured photocurrent of 15 mA is only 22.5 dBm at low frequencies and 18 dBm at 6 GHz. Here, the OIP3 was not measurable at higher frequencies which we attribute to the highly compressed fundamental tone and intermodulation distortion products below the noise floor of the spectrum analyzer.

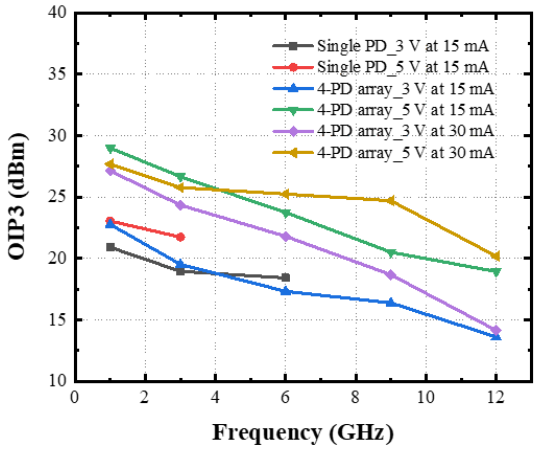


Fig. 3.11 Frequency dependence of OIP3 for the single PD and 4-PD array.

3.2.6 PD array results and discussion

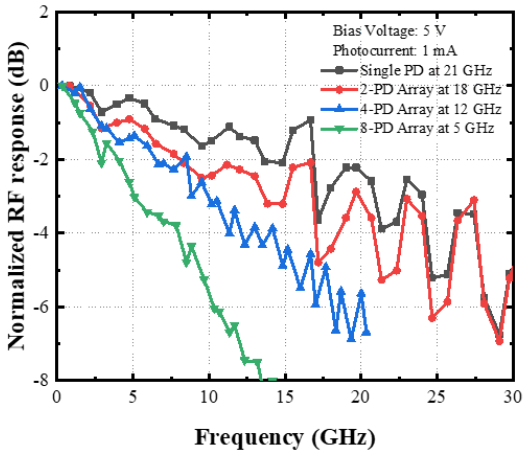


Fig. 3.12 Normalized frequency response of single PD and PD arrays.

Fig. 3.12 summarizes the normalized RF frequency responses of the studied devices measured at 1 mA. As expected, the 3-dB bandwidth (BW) decreases with increasing number of PDs in the array since each PD added into the array increases the total capacitance and consequently reduces the resistance-capacitance (RC)-limited bandwidth. The 3-dB bandwidth of the 8-PD array is approximately half of that of the 4-PD array. However, the BW reduction is not strictly proportional to the number of PDs for the 2-PD and 4-PD arrays since here the carrier transit time bandwidth limitation, which is independent of the number of PDs, plays a stronger role in limiting the overall bandwidth. The trade-off between RF bandwidth and RF saturation power is shown in Figs. 3.10. The saturation power at low frequency (5 GHz) is higher than the one at high frequency (3-dB bandwidth) due to the frequency response roll-off. Ideally, and at low frequencies, the saturation power can be 6 dB higher if the number of PDs in the array is doubled. This trend is approximately followed in the measurement results at 5 GHz (2.5, 9, 13 and > 14.3 dBm for single, 2-, 4- and 8-PD arrays, respectively). The observed slight deviation might result from imbalances in the Y-junctions. It should be mentioned that arrays with more than 8 PDs are currently not useful due to the limited power handling capability of the facet. We have also observed that PD arrays can effectively increase the linearity performance at high photocurrents. The OIP3 of the 4-PD array at 30 mA was around 4 dB higher than that of the single PD at 15 mA, which we attribute to severe saturation in the single PD which causes strong non-linearities. Inductors can be used to enhance the PD bandwidth without sacrificing RF power saturation performance and responsivity (Figs. 3.6). The bandwidths of a single PD was increased from 21 GHz to 33 GHz by integration of an on-chip spiral inductor. The inductor value should be designed so that the peaking can effectively compensate the frequency response roll-off. The only moderate bandwidth improvement from the 4-PD array with extended metal line suggests that a much larger inductance value is needed in arrays with high capacitance.

3.3 - Balanced PD

In a balanced photodiode pair, two PDs are connected in an anti-parallel fashion (Fig. 3.13 (a)) and as a result, only the differential input signals are detected while the common mode input signals are cancelled. Such balanced PD configuration can greatly suppress the common mode input noise and enhance the system performance in terms of signal noise ratio and SFDR in microwave photonic applications.

3.3.1 Device Layout

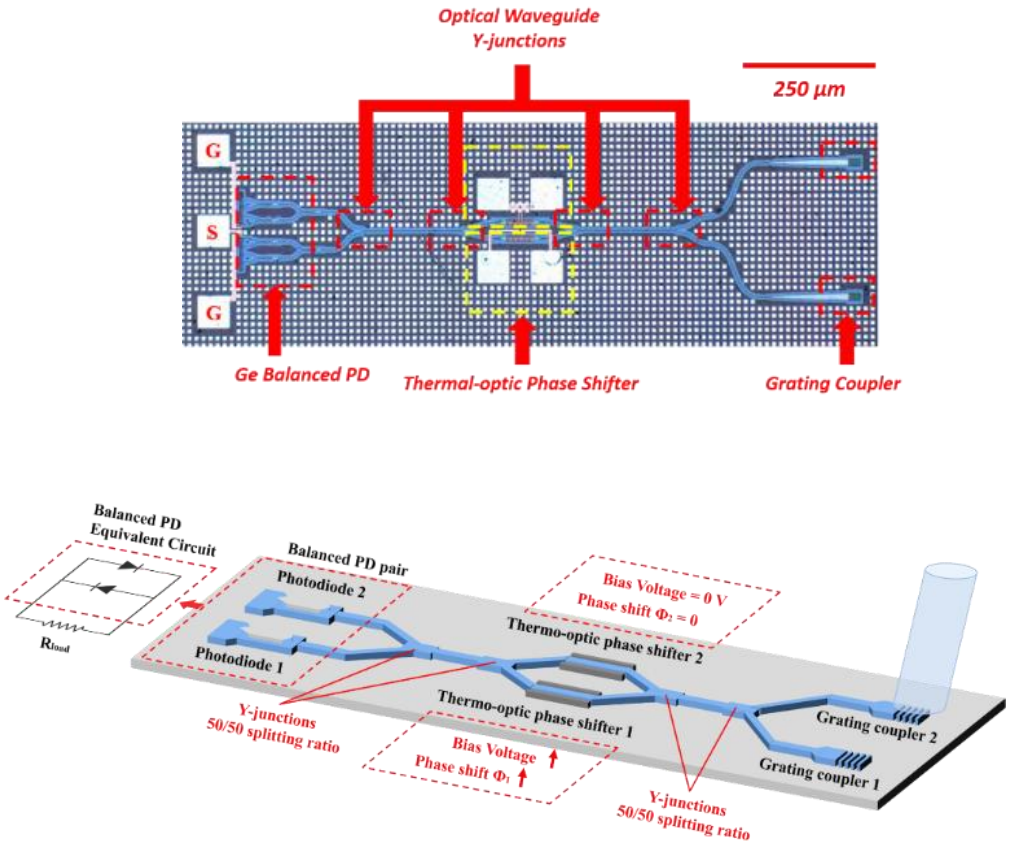


Fig. 3.13 (a) Top view, (b) circuit representation, and schematic of balanced PDs integrated with thermo-optic phase shifters and grating couplers. R_{laod} is an external load resistor.

The top view, circuit representation, and schematic of a balanced photodiode pair with two thermo-optic phase shifters are shown in Figs. 3.13. The function of the thermo-optic phase shifter is to adjust the ratio of optical power injected to the two individual PDs. In the following measurements, we only applied a voltage to thermo-optic phase shifter 1 in order to characterize the PDs one at a time or in common mode.

3.3.2 DC Characterization

The IV characteristic of both PDs in the balanced photodetector are shown in Fig. 3.14. The dark current is 1×10^{-7}A for PD1 and 2×10^{-7} for PD2 at a reverse voltage of 5 V. The balanced photodetector has a fiber-coupled responsivity of 0.25 A/W at 1550 nm wavelength when measured with a SMF-28 through the grating coupler.

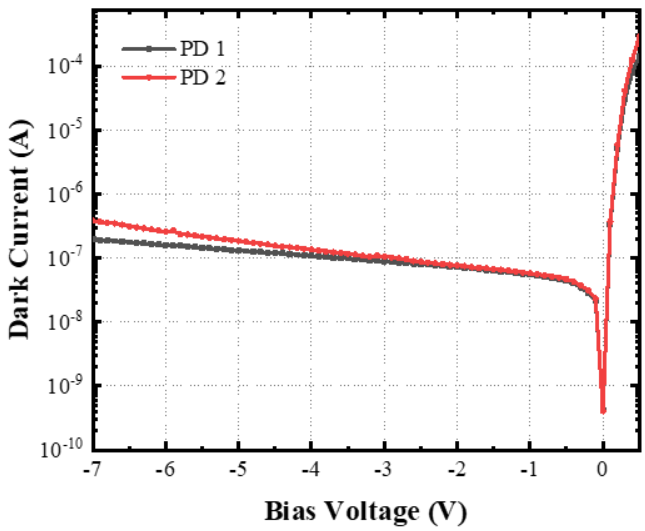


Fig. 3.14. Dark currents of the two individual PDs in the balanced pair.

3.3.3 Thermo-optic Phase Shifter Characterization

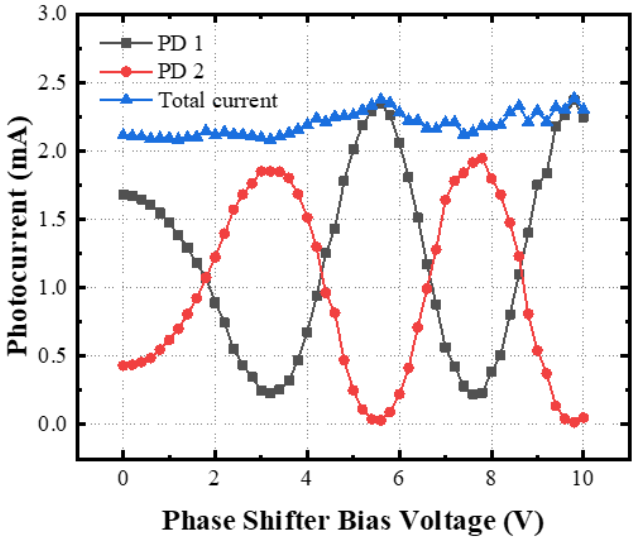


Fig. 3.15 Transmission spectrum of the thermo-optic phase shifter.

To characterize the thermo-optic phase shifter, only one grating coupler was used for input-coupling of the CW laser light. Fig. 3.15 shows the photocurrents in PD1, PD2, and PD1+PD2 as a function of applied voltage. We observed that the transmission spectrum did not provide 100% extinction ratio across the applied voltages which suggests a slight power imbalance in the optical paths most likely due to an uneven split ratio of the Y-junctions. From the transmission spectrum, we observe a Vπ of 4.5 V. The quadrature point at 4.5 V and a voltage point for maximum

photocurrent in PD1 was also determined for later use in bandwidth and power measurements. The consumed power of the thermo-optic phase shifter was 0.028 W.

3.3.4 Bandwidth and Power Saturation

The frequency response of the balanced photodetector was measured at a reverse bias of 5 V that we applied through a custom-designed RF probe to both PDs. For single PD illumination, the optical signal was launched into the lower grating coupler in Fig. 3.13. A voltage of 5.7 V was applied to the thermo-optic phase shifter to measure PD1. For PD2, we moved the fiber input to the upper grating coupler. Due to limitations in our current layout we calculated the frequency response in differential mode by adding up the RF powers of the two individual measurements of PD1 and PD2. For common mode, the RF power was measured by applying a bias voltage at the thermo-optic phase shifter at the quadrature point of 4.5 V. Fig. 3.16 presents the two individual PD frequency responses, the calculated differential mode and the measured common mode frequency responses of the balanced photodetector at individual PD photocurrents of 7 mA. We found that the common mode rejection ratio is large than 37 dB over the entire bandwidth of 21 GHz indicating a highly symmetric high-speed response from both PDs. Fig. 3.17 presents the output power and compression of the balanced photodetector at 21 GHz for the case that only one PD is illuminated. At 1-dB compression, we measured -7 dBm at 6 mA which is somewhat lower than a single photodiode.

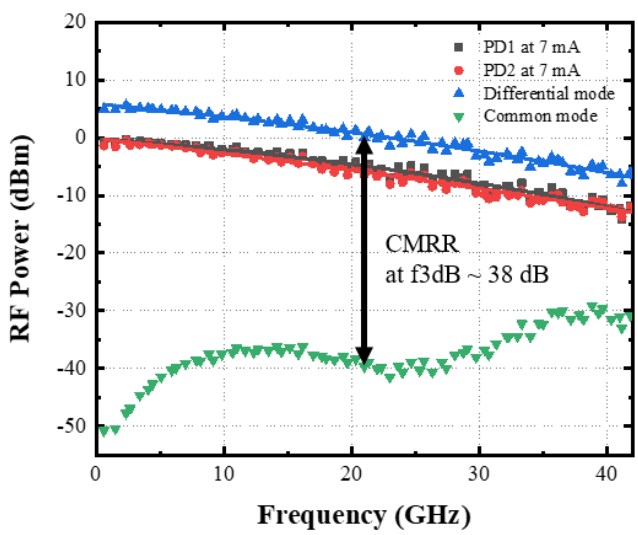


Fig. 3.16 Frequency responses of two PDs in the balanced pair, calculated differential response and common mode of the balanced PD at 7 mA per PD.

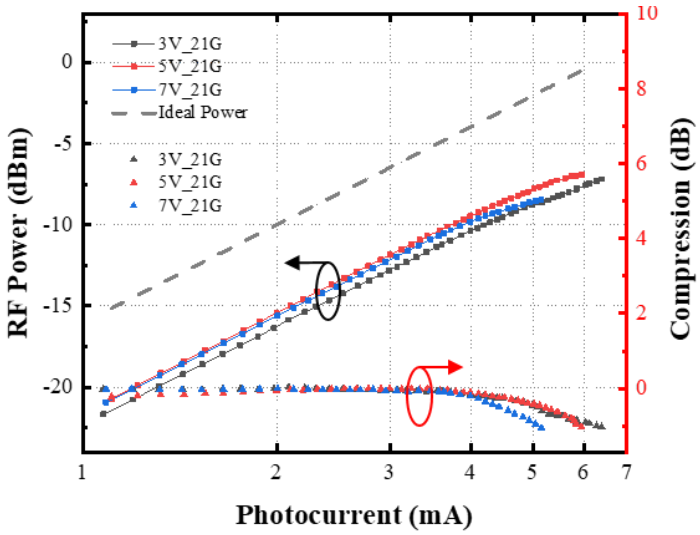


Fig. 3.17 Saturation current and power of the balanced PD at 21 GHz under various reverse bias voltages.

3.4 - Integrated Balanced PDs with Mach-Zehnder Delay Line Interferometer

To evaluate the benefits and limitations of the Si platform for microwave photonics applications, we designed a balanced PD pair integrated with a MZ DLI and characterized the device in a phase-modulated analog photonic link. While intensity modulation with direct detection has been widely used in analog photonic links [51, 52], phase modulation has some distinct advantages including less susceptibility to fiber nonlinearities, larger peak gain and a lower noise figure, and reduced complexity at transmitter [53-56]. However, phase modulation requires an optical demodulator on the receive side which in the following is monolithically integrated with balanced PDs.

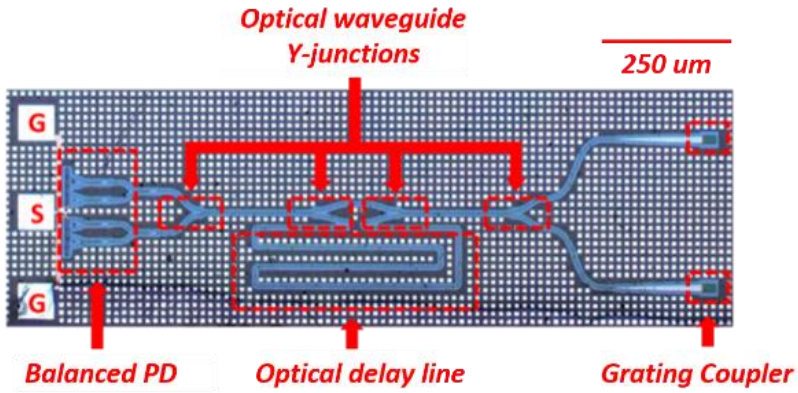


Fig. 3.18 Top view of the integrated balanced receiver with MZ DLI.

3.4.1 Device Layout and MZ DLI Characterization

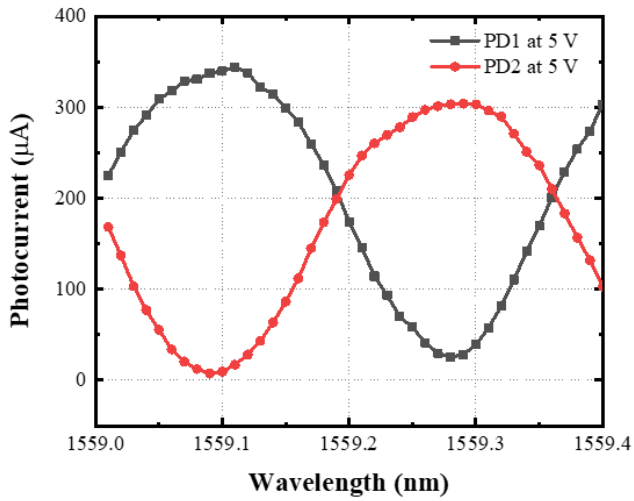


Fig. 3.19 Transmission spectrum of the MZI structure.

A balanced photodetector integrated with a Mach-Zehnder delay line interferometer (MZ DLI) is shown in Fig. 3.18. One arm in the interferometer includes a 1.4 mm-long silicon waveguide to delay the optical signal by 25 ps to allow for interferometric demodulation of phase modulated signals. To characterize the MZ DLI, we used a tunable laser and measured the photocurrent in each PD as a function of wavelength. Fig. 3.19 shows the measured transmission spectrum with a free spectral range (FSR) of 0.8 nm (38 GHz).

3.4.2 Phase-modulated Analog Photonic Link

To evaluate the balanced photodetector with integrated MZ DLI in a phase modulated photonic link, we used an experimental setup (Fig. 3.20) similar to the one described in [57].

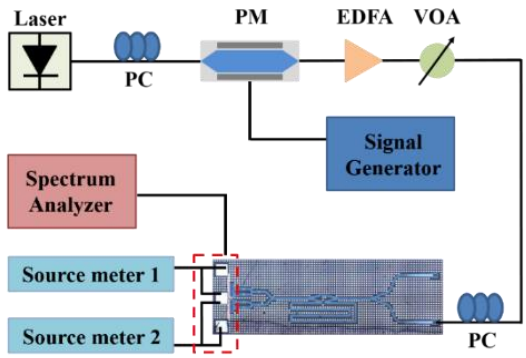


Fig. 3.20 Experimental setup of the phase modulated photonic link.

A 1550-nm wavelength laser is followed by a polarization controller (PC), a commercial lithium niobate phase modulator (PM) (Thorlabs, MACH-40), an erbium doped fiber amplifier (EDFA), and a variable optical attenuator (VOA). A second PC was used to optimize input coupling into the grating coupler of our integrated balanced photodetector with MZ DLI. The RF signal was extracted by an RF probe which connected to the spectrum analyzer for measuring the link gain spectrum. In our phase modulated analog photonic link, the MZ DLI was operated at the quadrature point by tuning the wavelength of the laser source to 1559.2 nm. The small signal link gain of a phase modulated link at quadrature point can be expressed as [57]

$$\boldsymbol{g_q = \frac{4\beta^2 I_{dc}^2 sin^2(\pi f \tau) Z_0 Z_{in} \pi^2}{V_\pi^2} \left|H_{pd}\right|^2} \quad \textbf{Eq. 3.1}$$

where $\beta = \frac{\varsigma-1}{\varsigma+1}$, where ς is the extinction ratio in the modulator, f is the input RF signal frequency, τ is the time delay between the two branches in the MZI, Z_0 is the load resistance, Z_{in} is the input resistance of the phase modulator, V_π is the half-wave voltage of the phase modulator and H_{pd} is the frequency response of the photodetector. To estimate the link gain in our experiment we used, $\beta = 0.95$, $V_\pi = 7$ V, $Z_{in} = Z_0 = 50\ \Omega$, $\left|H_{pd}\right|^2 = \frac{1}{2}$ and $\tau = 25$ ps for 38 GHz FSR. Fig. 3.21 (a) and (b) show the measured and calculated gain spectra at total photocurrents of 4 mA and 14 mA, respectively. While Equation 3.1 agrees well with the measurement at 4 mA, we found that bandwidth limitations of the balanced PDs lead to a lower than predicated gain at 14 mA. However, once the measured frequency response was included in Equation 3.1, a good agreement between theory and measurement was found. We expect that arrayed balanced photodetectors together with a low V_π modulator will further increase RF link gain.

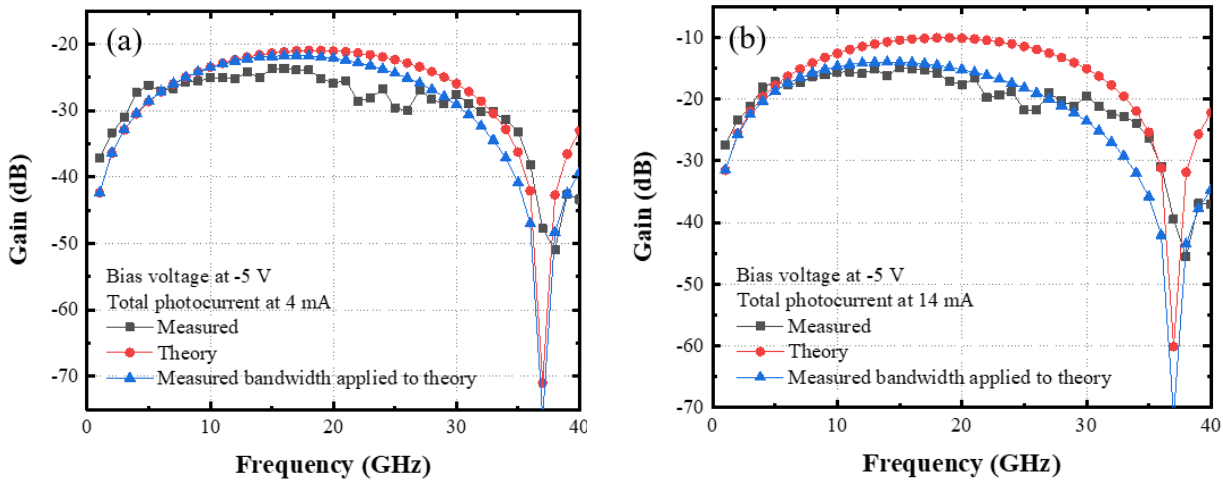


Fig. 3.21 Measured and calculated gain spectra of the phase modulated photonic link for (a) 4 mA and (b) 14 mA total photocurrent.

3.5 - Summary of this work

In summary, the first part of my work has demonstrated the performance of the fundamental building blocks for microwave photonic applications such as arrayed photodetectors, balanced photodetectors, and the first time ever integrated optical receiver for phase modulated analog photonic links, using a Si photonics foundry. Fig. 3.22 summarizes recent reports for germanium-based high-power photodetectors. Previously, the 3 dB bandwidth of our single PD (21 GHz), 2-PD array (18 GHz), 4-PD Array (12 GHz), and 8-PD Array (5 GHz) have been shown. To summarize and compare to other works at the same base line, Fig. 3.22 is comparing the RF power versus 1 dB compression photocurrent at 10 GHz (and 5 GHz if noted) with recent reported foundry-based Ge PDs. Generally speaking, we can observe that, by including more photodetectors in the array circuit, the RF output power saturation can be improved with higher 1 dB compression photocurrent. And in my work, 4-PD and 8-PD arrays reach the highest RF output power at 5 GHz with high saturation photocurrent. It should be mentioned, that these PD arrays reached record-high output power of any Ge-on-Si PDs reported to date at frequencies up to 12 GHz. This clearly shows the strength of the arrayed photodetector for providing high power handling capability for analog photonic link applications in a frequency range up to 12 GHz.

However, as we incorporate more photodetectors into the array, the RC-limited bandwidth decreases accordingly. While these larger PD arrays deliver higher saturation photocurrents (or, 1

dB compressed photocurrents), the RF power does not increase. To overcome the RC limited bandwidth, the traveling-wave photodetector was introduced to address the issue, and the result is also shown in this Fig 3.22 in Ref [58 and 59]. It should be noted that at lower frequencies (< ~15 GHz), the lumped PD array with its smaller footprint, less complex circuit, and shorter waveguides outperforms the TWPD and represents a better choice for applications that target high RF output.

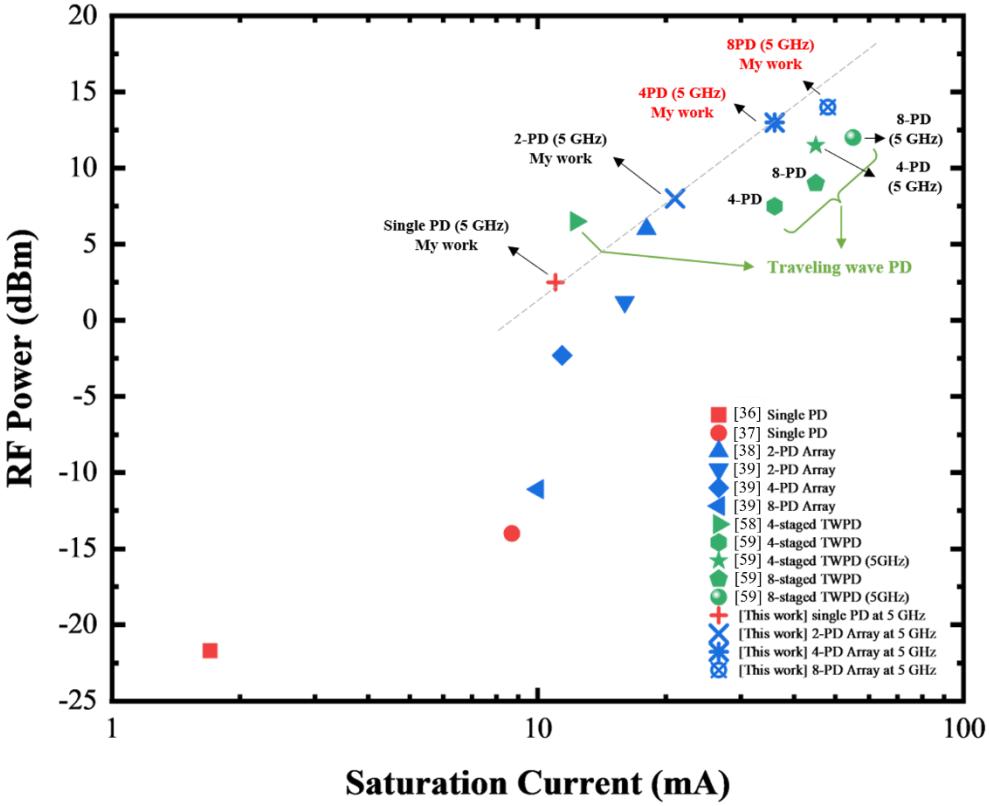


Fig. 3.22 Summary of RF power of high-power Ge PDs at 10 GHz (and 5 GHz) at 1 dB compression.

Chapter 4 - Foundry-Enabled Traveling-wave Photodetectors

4.1 - Introduction

In this chapter**,** I focus on utilizing the AIM Photonics platform and demonstrating foundry-enabled traveling-wave photodetectors. A TWPD with a compact, integrated bias circuit, 32 GHz bandwidth, and 6 dBm RF output power at 44 mA photocurrent is demonstrated and proved to have a similar bandwidth performance as a TWPD without integrated bias circuit. Moreover, to the best of my knowledge, I have demonstrated the first traveling-wave balanced photodetector (TWBPD), with an integrated on-chip bias circuit. The bandwidth of the TWBPD is measured to be 25 GHz with high common mode rejection ratio of 30 dB up to 40 GHz measured at 10 mA. Finally, I propose and experimentally demonstrate a low-loss, radio frequency (RF) photonic signal combiner with bandwidth from DC to 15 GHz and low group delay variation of 9.3 ps. This distributed group array photodetector combiner (GAPC) is implemented in a scalable Si photonics platform and has applications in RF photonic systems that rely on combining massive numbers of RF photonic signals.

4.2 - Traveling-wave photodetector and integrated bias circuit

4.2.1 Design Concept

By distributing the input light to multiple PDs and adding their photocurrents, we have previously demonstrated an 8-PD array that achieved high RF output power of 14 dBm [40]. However, the bandwidth was only 5 GHz due to the large resistance-capacitance (RC) time constant that scales with the number of PDs in the array. To overcome the RC bandwidth limitation, here I incorporate the PDs in a distributed circuit concept to form a traveling-wave photodetector. A simplified circuit of our TWPD is shown in Fig 4.1. The optical input is split into eight waveguides and fed into eight photodetectors respectively. I use a total of 7 low loss Y-junctions (<0.5 dB loss each) to perform 1-to-8 splitter function. The photodetectors are periodically loaded into an electrical microstrip coupled line. To match the TWPD's impedance to the external 50 Ω load, R_{50}, and to counter the capacitive loading of the PDs, I designed a high impedance transmission line with spacing l_{Δ} between PDs. The electrical phase velocity is then determined by the dimensions of the transmission line and the amount of capacitive loading and can be used to determine the necessary

optical delays to achieve in-phase summation of the photocurrents from each PD at the external load. To this end, I designed 7 different optical delay line waveguides (1τ..7τ) that connect right after the 1-to-8 splitter. Opposite to the RF output, I implemented a 50 Ω termination, R_{term}, that eliminates any back-reflected signals which can cause deconstructive interference at the RF output and decrease the bandwidth. It should be mentioned that this configuration can result in an improvement of 4X in usable saturation photocurrent and 6 dB increase in RF output power compared to a single PD.

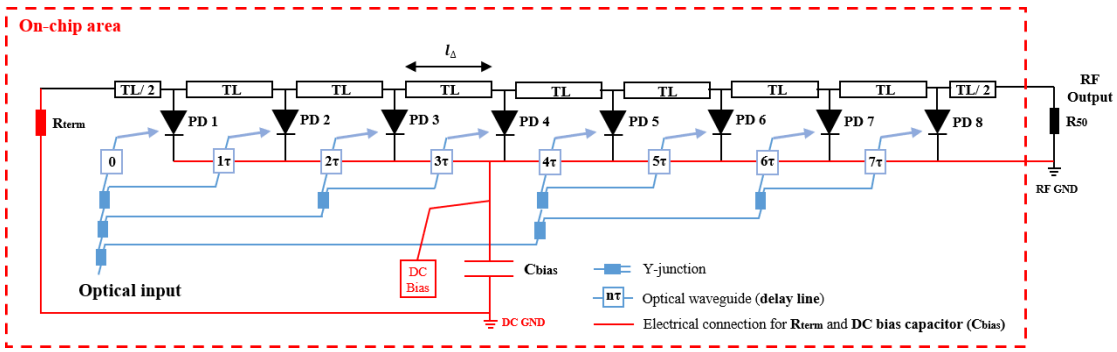


Fig. 4.1 Schematic of TWPD with integrated bias circuit.

To design the transmission line dimensions, I initially assumed a lossless circuit, and used the following equation [48] to determine the inductance, *L*, and capacitance, *C*, per length of the unloaded TL:

$$\boldsymbol{Z} = \sqrt{\frac{\boldsymbol{L}}{\boldsymbol{C}+\frac{\boldsymbol{C_p}}{\boldsymbol{l_\Delta}}}} = \mathbf{50}\ \ (\boldsymbol{\Omega}) \qquad \textbf{Eq. 4.1}$$

C_p is the PD junction capacitance and was measured to be 40 fF. To match the impedance, I chose a ground-signal (GS) TL with 15 µm gap. Ground line width and signal line width were 60 µm and 15 µm, respectively. Using ADS momentum EM simulation, I obtained 7×10^{-7} H/m for *L* and 8×10^{-11} F/m for *C*. The spacing l_Δ between PDs was chosen to be 200 µm. To determine the electrical phase velocity v_e and the optical group velocity v_o, I used

$$\boldsymbol{v_e} = \frac{\mathbf{1}}{\sqrt{\boldsymbol{L}(\boldsymbol{C}+\frac{\boldsymbol{C_P}}{\boldsymbol{l_\Delta}})}}\,(\mathbf{m/s}) \qquad \textbf{Eq. 4.2}$$

$$\boldsymbol{v_o = \frac{c_0}{n_g}\ (\mathrm{m/s})} \qquad \textbf{Eq. 4.3}$$

n_g (4.2) and c_0 represent the effective group index of the silicon waveguide and the speed of light in the vacuum, respectively. For our design, we calculated 7.1×10^7 m/s for both velocities, meaning that the required optical delay length for each segment is identical to l_Δ to achieve phase matching at the RF output.

To avoid the large current (~100 mA) at R_{term} when reverse biasing the PDs, I incorporated a bias capacitor, C_{bias}, that decouples the PDs' n-contacts from RF ground (Fig. 4.1). Another advantage is that the reverse bias is applied through a separate DC pad and no external bias T is needed which eases the complexity in the measurements and in future chip packaging. I then also included loss factors into the circuit model that was implemented in ADS to simulate bandwidth (see section 4.2.2). In general, the RF loss is mainly contributed by PD series resistance, transmission line ohmic loss, and substrate loss. I used a PD series resistance (R_s) of 20 Ω based on previous S11 parameter extraction from a standalone PD [40]. For transmission line loss, I used a conductivity of 5.8×10^7 (S/m) for copper. Finally, I have also considered a Si substrate resistivity of 8~10 Ω·cm in our model.

4.2.2 Experimental Results

TWPDs were designed and fabricated using the AIM Si photonics Process Design Kit (PDK) and foundry service. Our TWPD includes 8 'analog PD' elements from the PDK, each with a nominal bandwidth of 37 GHz (estimated transit time limited bandwidth: 40 GHz), internal responsivity of 0.9 A/W, and 100 nA dark current at 5 V. To construct the bias capacitor, I used two different metal layers to form a metal-insulator metal (MIM) structure. The RF ground of the transmission line (1600 µm × 60 µm) is set to be the top metal layer of the capacitor, while the lower metal line is connected to the PD's n-contacts and the DC bias pad. The value of the capacitor is designed to be 6 pF. The R_{term} is designed to be 50 Ω. Figure 4.2 (a) first shows the top view of the TWPD without on-chip capacitor and resistor. This device is mainly used to verify the loaded transmission line characteristics and as a bandwidth reference compared to the proposed TWPD with integrated bias circuit which is shown in Fig. 4.2 (b).

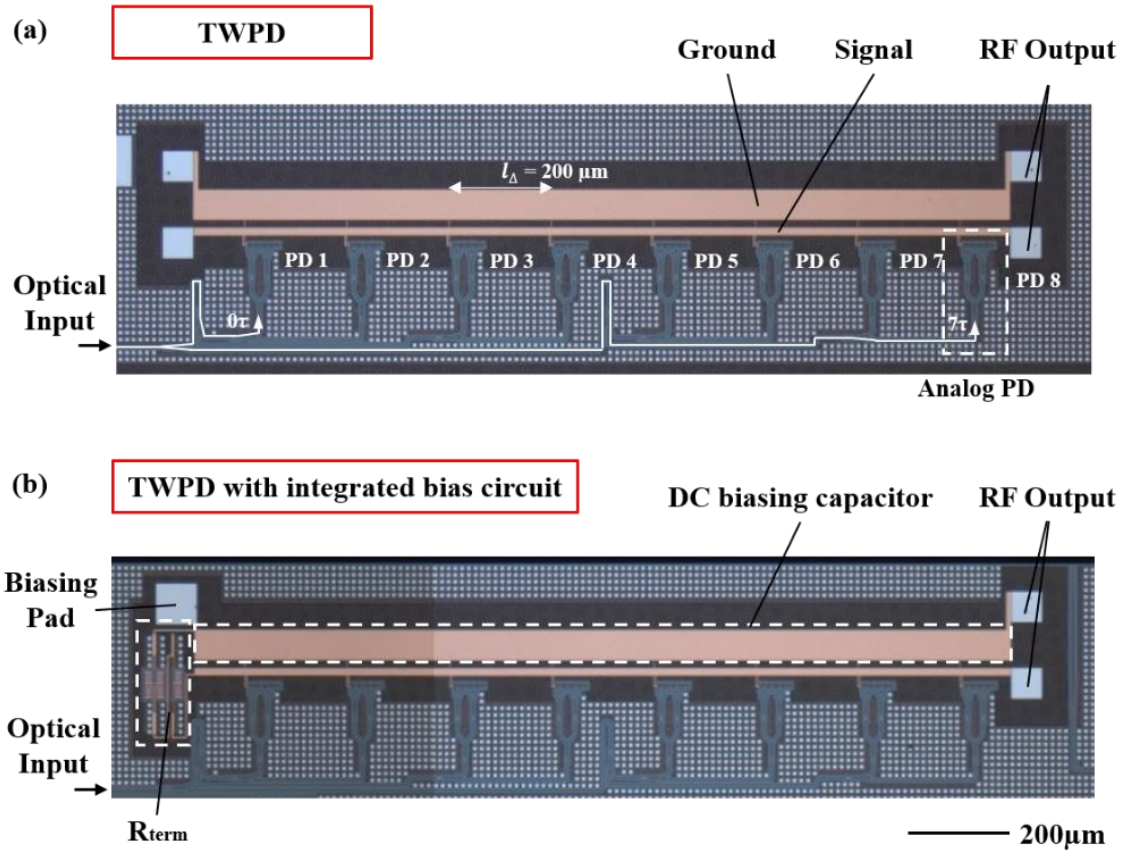


Fig. 4.2 (a) and (b) shows the top view of the TWPD and TWPD with integrated bias circuit respectively.

The first step to verify the RF performance is to conduct S parameters measurements to investigate the loaded transmission line characteristics. Fig. 4.3 (a) and (b) show the measured S11 and S21 of the TWPD at 5 V reverse bias and compare to simulation, respectively. The S11 is well below -15 dB up to 40 GHz, and the S21 is down to 6 dB up to 40 GHz indicating good impedance match to 50 Ω (Fig. 4.4(a)). The velocity matching between electrical and optical velocities is also shown in the Fig. 4.4(b).

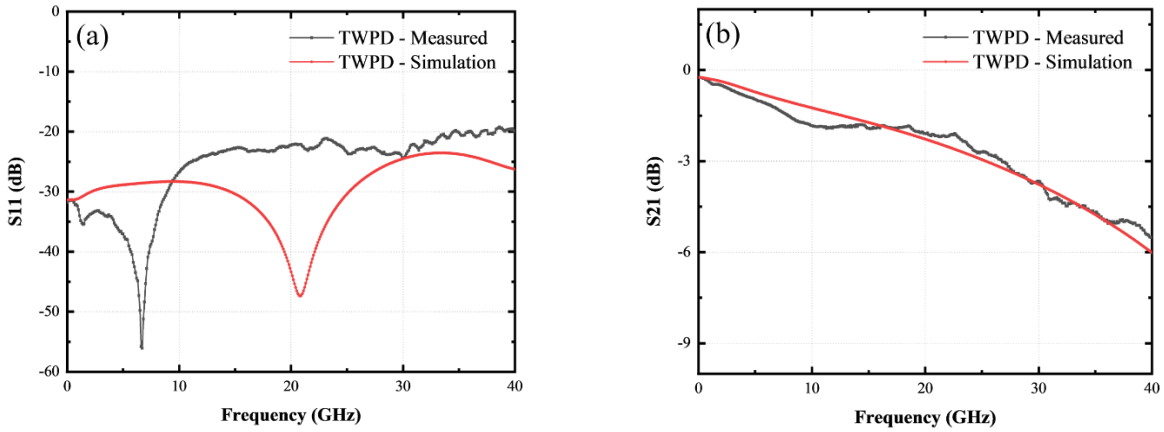


Fig. 4.3 (a) S11 and (b) S21 of the TWPD measured at 5 V.

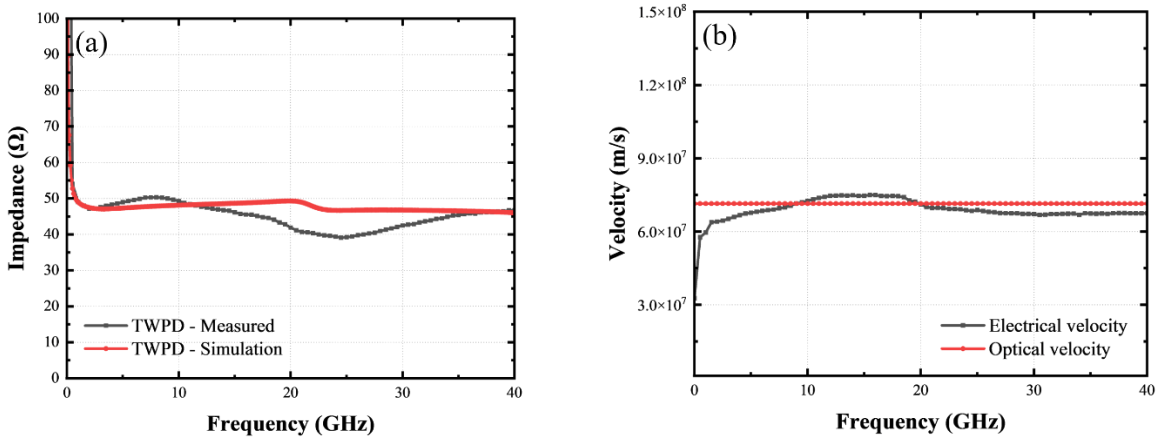


Fig. 4.4 (a) Characteristics impedance and (b) Velocities comparison of the TWPD measured at 5 V.

Next, I measured the O/E frequency response. The measurement was conducted using a 1550 nm laser, a commercial lithium niobate modulator (40 GHz bandwidth), and Keysight network analyzer (67 GHz). The responsivity of the TWPD is measured to be 0.17 A/W. By correcting the 5.7 dB coupling loss between tapered fiber (2.6 µm spot size) and the waveguide edge coupler which was measured in a fiber-in and fiber-out test structure, the internal responsivity is 0.67 A/W. The 1.5 dB excess loss is from the waveguide delay lines and Y-junctions. The OE frequency response of the TWPD without integrated bias circuit was measured at 1 mA at 5 V from 10 MHz to 40 GHz which is shown in figure 4.5 (a). The bandwidth is 30 GHz and shows a good agreement with the simulation results. In the figure 4.5 (b), the same OE frequency response is compared to the bandwidth measurement using an optical heterodyne approach [28] and showing a similar bandwidth trend.

For the TWPD with integrated bias circuit, I first present the measured OE frequency response up to 40 mA at 5 V from 10 MHz to 40 GHz and compare it with the simulation result that shows a good agreement of a 32 GHz bandwidth from Fig. 4.6 (a). And compared to the TWPD that needs the external 50 Ω termination resistor and has achieved a 30-GHz bandwidth at 1 mA at 5 V (figure 4.5), it can be concluded that no negative impact on the RF performance is observed by embedding the on-chip bias circuit into the TWPD design. Also, in figure 4.5, a significant bandwidth degradation can be observed from the TWPD OE frequency response measured without connecting the external 50 Ω termination resistor. This indicates that the TWPD overcomes the RC-limited bandwidth based on the capacitive loaded distributed circuit design.

On the other hand, an optical heterodyne measurement was used to characterize the TWPD high-power performance under large-signal modulation condition. The bandwidth of the TWPD with integrated bias circuit is measured from 1 mA with 30 GHz bandwidth and further pushed up to 40 mA with a little bit bandwidth roll-off to 27 GHz which are shown in figure 4.6 (b). This also matches the RF roll-off we observed in Fig. 4.6 (a) (PNA measured OE frequency response). To further investigate the saturation photocurrent, the same optical heterodyne setup is used, to gradually adjust the optical input power fed to the TWPD for measuring the 1 dB compression point. Figure 4.7 shows the RF saturation measurement results at 5 GHz (Black) and 30 GHz (Red). For both cases, we could not reach the 1 dB compression point due to the fact that on-chip optical input power higher than 19 dBm resulted in failure of the waveguide edge coupler. Nevertheless, we have achieved a photocurrent up to 44 mA with RF output power of 6 dBm at 30 GHz. Based on the compression curve, the 1 dB compressed point is expected to happen at ~ 50 mA with the potential to reach even higher RF power.

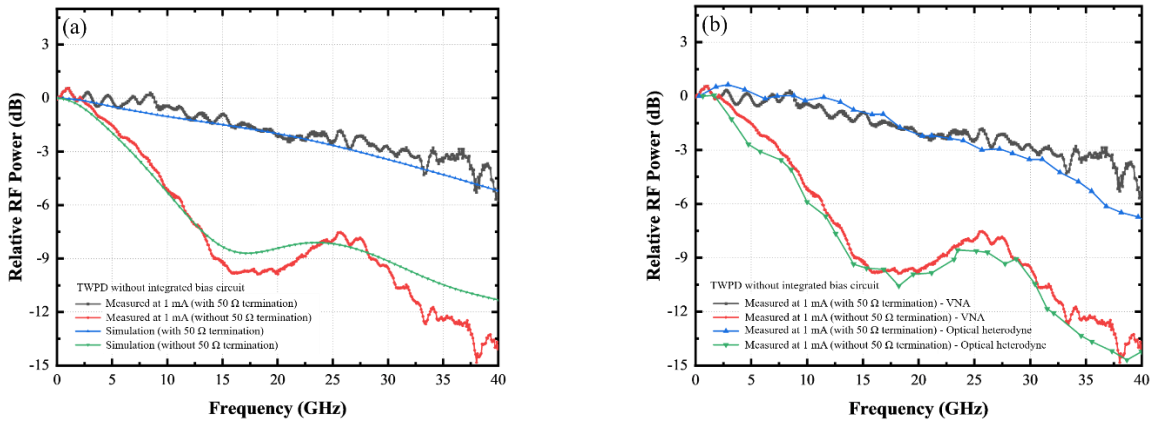


Fig. 4.5 OE frequency responses of TWPD without integrated bias circuit with and without external 50 Ω termination resistor measured at 1 mA compared to the (a) simulation and (b) optical heterodyne approach.

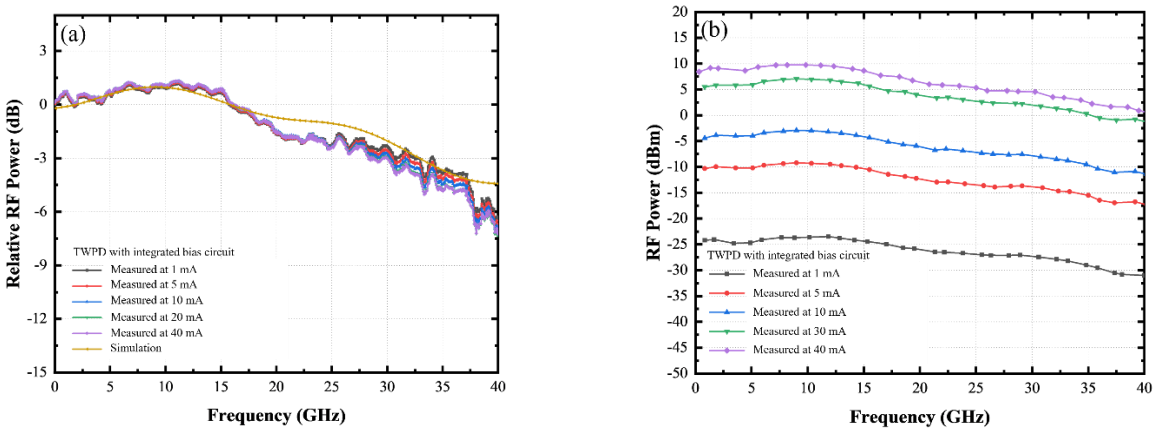


Fig. 4.6 (a) OE frequency responses of the TWPD with integrated bias circuit measured up to 40 mA compared to simulation and (b) bandwidth measurements of the TWPD with integrated bias circuit using optical heterodyne approach measured up to 40 mA.

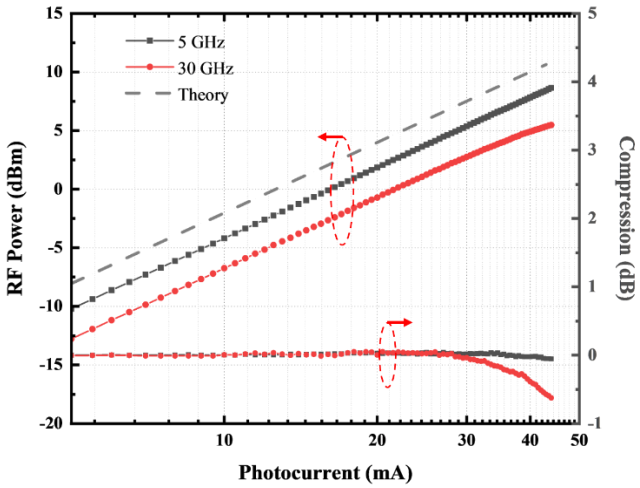


Fig. 4.7 RF saturation measurement of the TWPD with integrated bias circuit at 5 GHz and 30 GHz.

4.3 - Traveling-wave balanced photodetector (TWBPD) with integrated bias circuit

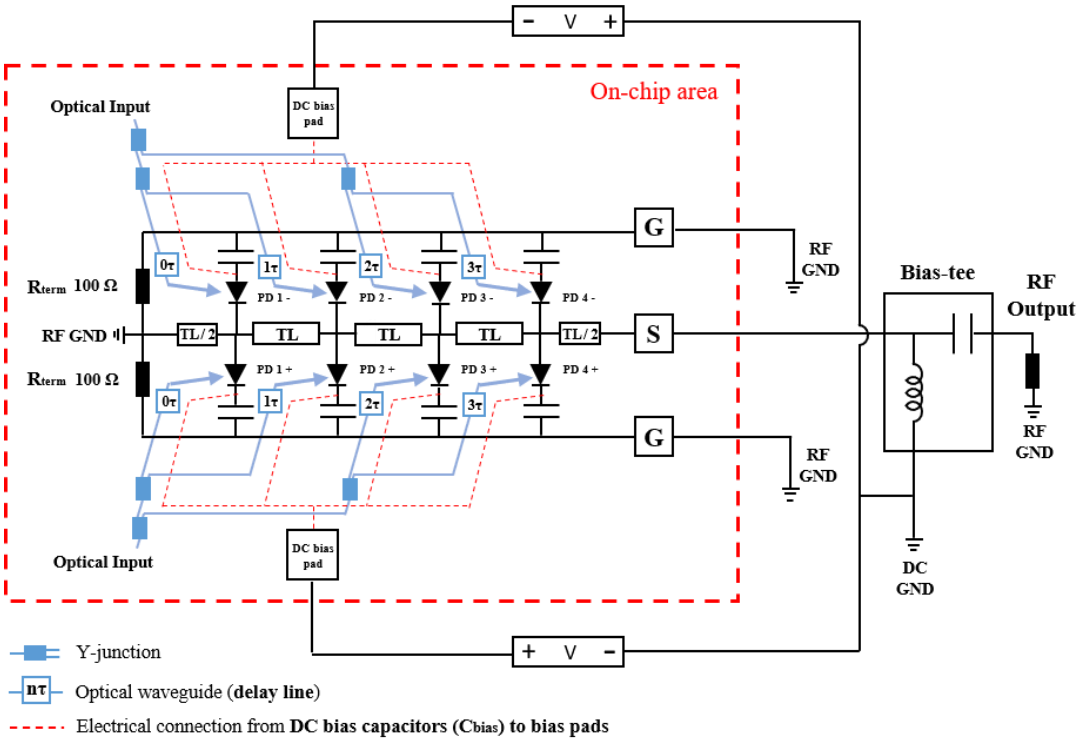


Figure 4.8 Schematic of the TWBPD circuit.

A balanced type of a traveling-wave photodetector with on-chip biasing circuit has also been designed and the schematic circuit is shown in Fig. 4.8. In total 8 “analog” PDs are used in the TWBPD design in order to load 4 pairs of balanced PDs into the distributed circuit. For each balanced pair with two PDs (PD+ and PD-) in an anti-parallel connection, the n-contact of one PD is connected to the p-contact of the other PD. Note that the TWBPD requires two opposite DC bias to properly reverse bias all PDs. Compared to the TWPD in fig. 4.1, the capacitive loading is now doubled which I addressed through a doubled length of each segment of loaded transmission line, now to be 400 µm. And the transmission line is designed to be a coplanar waveguide in GSG configuration that has 60 µm wide ground line and 5 µm wide signal line. The gap between the ground and the signal line is designed to be 25 µm. The TWBPD with integrated bias circuit significantly eases the measurement setup which is usually done using two customized and bulky GSG probes with external capacitor and termination resistor in our lab. In the schematic circuit

shown in Fig. 4.8, on the left side (termination side), two 100 Ω on-chip resistors are parallel-connected to provide the 50 Ω termination. Next, we inserted 8 individual on-chip metal-insulator-metal capacitors with the dimension of 60 µm × 320 µm (1.2 pF) between the 8 individual PDs and the ground, respectively. These capacitors work as the on-chip DC blocking capacitor for the photodetectors. Fig. 4.9 shows the top view of the TWBPD. To achieve phase match at the RF output, the single segment optical waveguide delay line length (τ) is designed to be 510 µm since the optical velocity is 22% faster than the electrical velocity based on the designed transmission line.

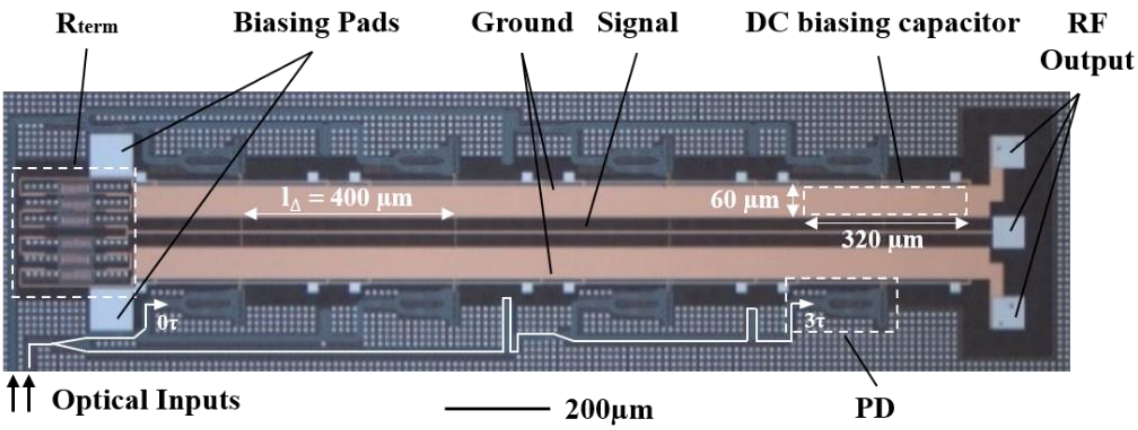


Figure 4.9 Top view of TWBPD.

4.3.1 Experimental results

First, the OE frequency response was measured separately for all PD(-) and PD(+) and is shown in Fig. 4.10 (a) at different photocurrents from 1 mA to 10 mA, and no significant bandwidth degradation was found. We measured a 25 GHz bandwidth from TWBPD. To be noted that, PD- and PD+ are labelled as upper side and lower side of a PD pair in the Fig. 4.9. Compared to the TWPD in section 4.2 that is also loaded with 8 "analog" PDs but 32-GHz bandwidth, the TWBPD has a somewhat lower bandwidth that is caused by two reasons which were observed from the simulation: First, the TWBPD has a narrower signal line width of 5 µm compared to the TWPD that has 15 µm wide signal line, and this could lead to additional RF transmission loss under the same transmission line length between TWBPD and TWPD. Secondly, the R_{term} of the TWBPD turned out to be ~ 60 Ω instead of 50 Ω which I characterized by using resistance test structure, and this can further degrade the TWBPD bandwidth.

Next, I used an optical heterodyne setup with a tunable optical delay line to generate differential and common mode optical input signals and measured the bandwidth at 10 mA. A simplified experimental setup is shown as an inset in Fig. 4.10 (b). 25 GHz bandwidth was achieved from the differential mode measurement with ~ 6 dB RF power improvement that is also shown in Fig. 4.10 (b). Moreover, since the PD- and PD+ demonstrate a very good balanced RF response, higher than 30 dB common mode rejection ratio (CMRR) was measured from 530 MHz up to 40 GHz. To the best of our knowledge, this is the first high-speed balanced TWPD with high CMRR and integrated bias circuit that has been demonstrated on a Si photonics platform.

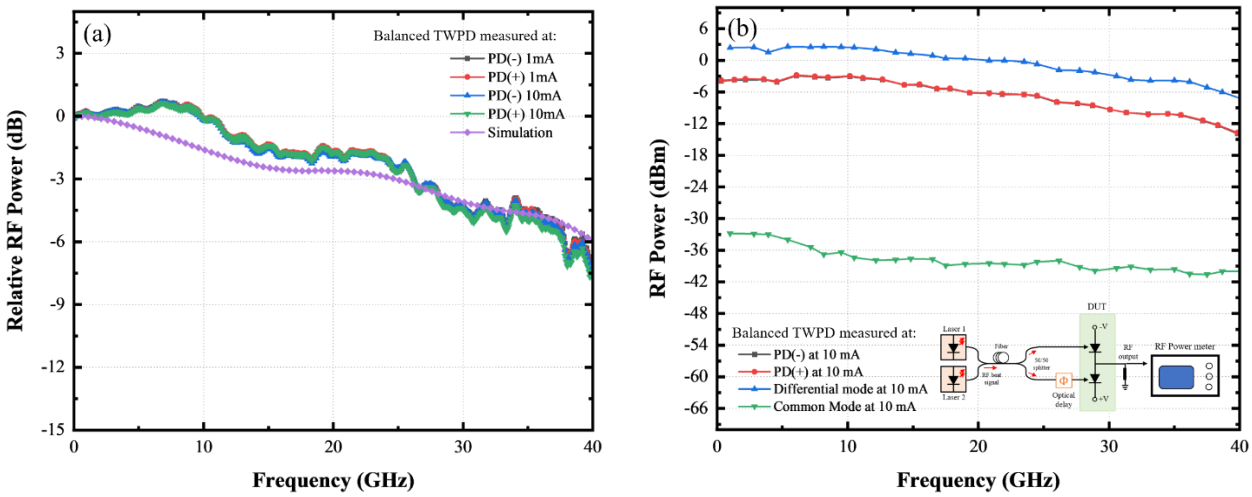


Figure 4.10 (a) OE frequency responses and (b) differential mode and common mode measurements of the TWBPD.

4.4 - Discussion

In this section, the major limitations to the RF performance of the TWPD concepts presented above based on the AIM Photonics platform are discussed. To be noted that the following conclusions may also be helpful for any future TWPD designs using other CMOS foundry platforms. The two main factors that limit RF performance are: (1) Optical-waveguide-loss and (2) RF-transmission loss.

4.4.1 Optical-waveguide-loss

One of the main limiting factors impeded us to explore the upper boundary of RF power saturation for the TWPD designs in this work is due to the silicon waveguide loss caused by high optical input induced two photon absorption (TPA) and free carrier absorption. Table 4.1 shows the lengths of the silicon waveguides that are used as the waveguide routing sections before entering the devices and the longest delay sections used in these three different designs. Comparing the TWPD without integrated bias circuit and TWBPD with integrated bias circuit designs that has 1.9 mm and 4 mm of waveguide routing sections, respectively, that are limited by the optical input/output arrangement on the tape-out, the TWPD with on-chip bias circuit is the only design in this work that is able to reach near its 1 dB compression point (~ 50 mA) during the saturation measurement due to the fact that there is only 0.8 mm additional waveguide routing (400 µm long silicon edge coupler included) before entering the device. Based on the 1.1 mm waveguide routing difference between the TWPD with and without integrated bias circuit, more than half of the optical power can already be absorbed by the waveguide routing section of the TWPD design due to the TPA when the optical input is increased up to 275 mW. This indicates that part of the input optical power will also be absorbed by the TWPD delay sections from all three designs shown in the table 4.1 to further limit the power performance. On the other hand, we have also found that ~ 19 dBm (325 mW) on-chip optical input power is measured to be the upper limit of the silicon edge coupler before structure failure. This is due to the fact that silicon edge couplers are designed based on a multi-layer structure as a mode evolution converter for optimizing the coupling efficiency from the fiber tip to the coupler [60]. And while the optical power has been leveling up and sending to the devices to compensate the loss caused by TPA, the mode transitioning from different layers of the edge coupler cannot sustain high power operation which eventually leads to the structure failure. To this end, one of the solutions to resolve this issue is to replace the silicon edge coupler with a silicon nitride (SiN) edge coupler from the AIM PDK component [60] together with replacing the silicon waveguide optical delay sections with the SiN waveguides in the TWPD design to further mitigate the TPA at 1550 nm [61].

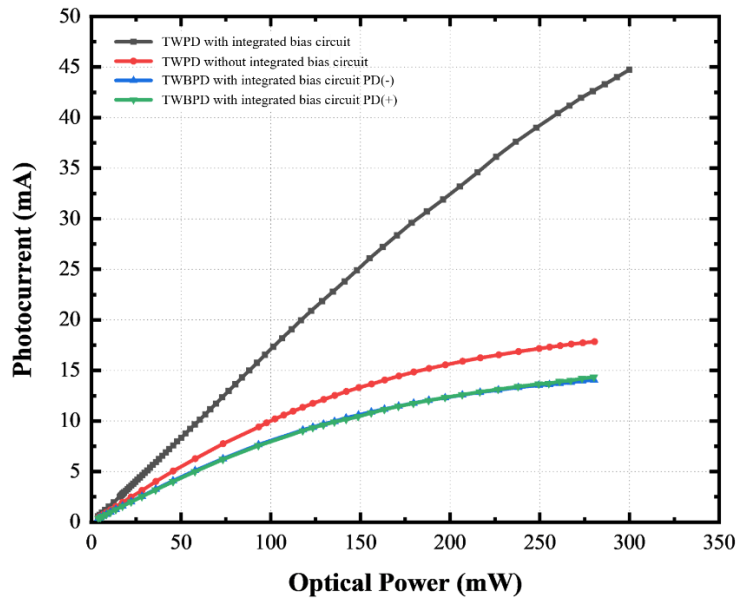


Fig. 4.11 optical DC responses of TWPD (w/o integrated bias circuit), TWPD (w/ integrated bias circuit) and TWBPD (w/ integrated bias circuit).

Table 4.1 Waveguide sections breakdown for different designs in this work

	Waveguide routing before entering the device (400 um long edge coupler included)	**Longest delay section in different designs**
TWPD w/o integrated bias circuit	1.9 mm	1.4mm
TWPD w/ integrated bias circuit	0.8 mm	1.4mm
TWBPD w/ integrated bias circuit	4 mm	1.5mm

4.4.2 RF-transmission-loss-limited factor

In general, the RF loss mechanism can be categorized into three: (1) photodiode series resistance, (2) ohmic loss from the conductor (copper), and (3) low substrate resistance induced dielectric loss. Here, the 8-stage TWPD is used for the analysis. To begin with, Si substrate resistance has been investigated. Usually, low resistivity (8-10 Ω·cm) Si substrate is used in CMOS foundries including this work. However, this type of substrate is not the best choice for low-loss RF transmission lines. If the metal layer used for the transmission line is too close to the Si substrate and the electric field is distributed into the substrate region, the RF signal will experience additional dielectric loss. Two options can be adopted to reduce this type of substrate loss. First is to choose those foundries that can provide high resistivity substrate such as 750 Ω·cm reported in Ref [82]. The other one is to get access to the upper metal layers that is further away from the Si

substrate, for example in our case, there is at least 5 µm distance from the substrate using the M2 layer. In Fig. 4.12 (a), the simulations are conducted based on the same PD series resistance of 20 Ω and included with ohmic loss in the model. And based on the same 5 µm distance between the M2 layer to the substrate, there is no significant RF loss to further degrades the frequency response from using 1000 Ω·cm substrate to the 10 Ω·cm one. On the other hand, based on the same 10 Ω·cm substrate, the RF response degrades less than 1 dB if the distance between the M2 layer and the substrate is only 2 µm. Overall, there is only 5 GHz bandwidth variation between the three scenarios which indicates that substrate loss is the secondary factor in the loss mechanism. The photodiode resistance and ohmic loss which are presented in Fig. 4.12 (b). The simulations are conducted under several scenarios: (1) a lossless model, (2) only include substrate loss, (3) include substrate loss and PD series resistance, and (4) include all loss factors. In summary, figure 12 (b) clearly shows that PD series resistance is the most significant factor that dominates the RF loss in the TWPD circuit when compared with conductor loss and substrate loss.

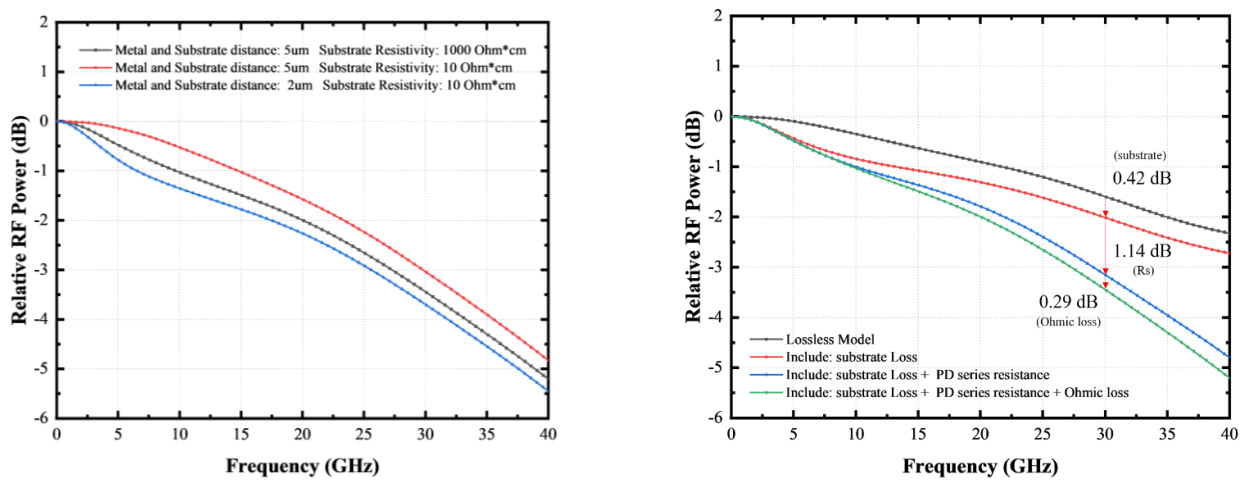


Fig. 4.12 (a) Substrate loss investigation between different resistivity and metal-substrate distance and (b) loss investigation to include PD series resistance, ohmic loss, substrate loss and compare to a lossless model.

Based on the limiting factors, the design trade-off between the maximum PD count to be used in the TWPD circuit and the optimized RF output power is worth to be analyzed. As mentioned, one of the major limitations on exploiting the RF power of the arrayed PDs and TWPDs is the on-chip optical input to the silicon edge coupler. Here, except for the edge coupler upper input limitation of 325 mW, we assume that there is no silicon waveguide and RF transmission loss. And then, we could potentially build a 40-staged TWPD that has ~280 mA saturation current at 40 GHz (transit-time limited bandwidth) which is estimated by the measured single PD saturation current of 7 mA

at 35 GHz and the reported internal responsivity of a single analog PD from AIM PDK document. However, by taking the loss factors into account, a 15 GHz bandwidth with only 14 mA maximum achievable photocurrent from the 32PD-loaded TWPD that we have also designed in this tape-out has been measured. And this low usable photocurrent is mainly caused by the TPA induced waveguide loss and edge coupler. Therefore, we believe that TWPD in this work that has 32 GHz bandwidth with the near saturated current of 44 mA is close to the optimized TWPD design on this platform. In figure 4.13, we compare the high-power performance in terms of the bandwidth × saturation current product ($BW \cdot I_{sat}$) with the reported arrayed PDs [40] and TWPDs [58,59] in the literature. To make a "fair comparison", we plot the output photocurrent that is available at the external load resistor by cutting the maximum photocurrent of the TWPD by half. This is due to the fact that the TWPD in general has to be terminated with an extra 50 Ω resistor for the impedance matching, and this termination contributes a 50% reduction in usable photocurrent (or 6 dB lower RF output power at the external load). Based on this comparison shown in the figure 4.13, the TWPD demonstrated in this work has achieved a 660 GHz · mA of bandwidth × saturation current product which is higher than previous reports. It should be noted that in Ref. [58], the aperiodically loaded TWPD is presented with an open circuit termination. Therefore, the saturation photocurrent used in this figure remains unchanged because there will be no power dissipation on the termination end. Finally, compared to our previous reported arrayed PDs [40] on the same AIM Photonics platform, the TWPD does show its strength in terms of high-power handling capability and at the same time can high bandwidth. Comparing to the 8-PD array in [40], both unsaturated, the TWPD in this work has 2.75X improvement in the bandwidth × saturation current product. In future designs, using the SiN edge coupler and SiN optical delay lines could help to further increase the RF output power since SiN has virtually no TPA due to its large bandgap. Also, taking the similar approach such as the aperiodically distributed TWPD concept that is shown in [58] by avoiding extra power dissipation on the termination end is considered to be another promising approach to further improve the RF power performance of the TWPD.

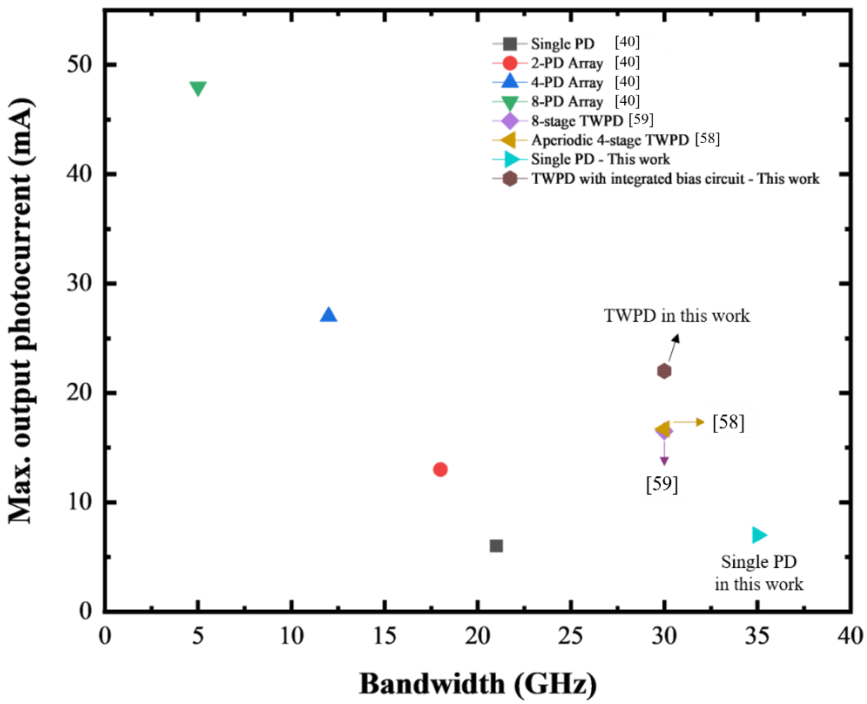


Fig. 4.13 Summary of the bandwidth*saturation current product for arrayed PDs and multi-staged TWPDs.

4.5 - Group array photodetector combiner

4.5.1 Introduction

Receive-mode electronically steerable phased array (Rx-ESA) systems are widely used in defense and commercial applications, however, especially large phased arrays (many antenna elements) working at high frequencies have limited performance and capabilities that originates from electronic combining of the many RF signals, plus from mixing spurs in electronic down-conversion systems using RF mixers [62-64]. New photonics-based Rx-ESA systems can overcome these issues by taking advantage of a massive RF photonic signal combiner, that combines many optical signals into a single electrical RF output with low loss and large bandwidth [65]. Such a massive RF photonic signal combiner can be used in other photonic systems with optical channels. In this work, I demonstrate for the first time a group array photodetector combiner (GAPC) that can enable such Rx-ESA and other massively parallel RF photonic systems.

The GAPC, first conceived by P. Morton in Ref. [65], can combine ‘n’ RF photonic signals from ‘n’ antenna elements, each signal including amplitude and time delay control that can be carried out in an RF Beamforming photonic integrated circuit (PIC). An example system schematic is

shown in fig. 4.14; this system includes a photonic channel for each antenna element; laser, modulator, plus delay/amplitude control, with the signals from each antenna element being combined in the GAPC to provide a single RF beamforming output. The GAPC has the capability of combining very large numbers of RF photonic signals with low loss, a capability that is crucial for this Rx-ESA and other RF photonic applications. Each RF photonic signal in fig. 4.14 is applied to its own PD, with the photocurrents from all PDs combined in the GAPC to provide a single RF output - this avoids the possibility of optical interference of the different photonic signals within a single PD, which would add significant noise to the system.

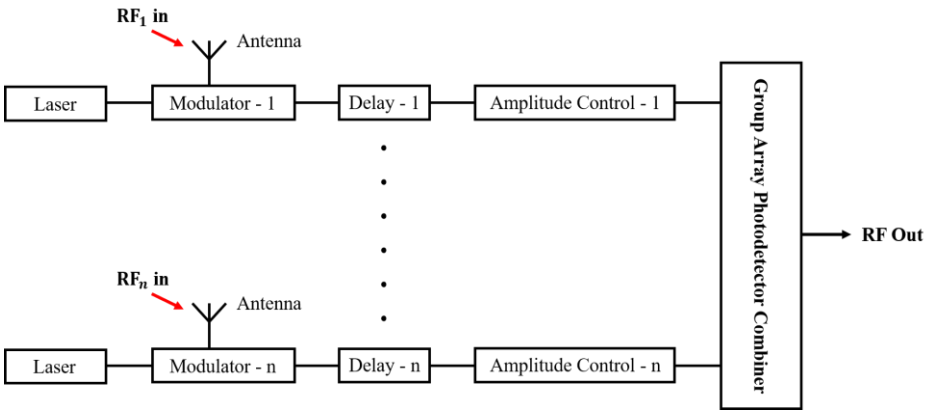


Fig. 4.14 Rx-ESA system using GAPC RF photonic signal combining.

The simplified system in fig. 4.14 can be extended by the use of wavelength division multiplexing (WDM), in which case multiple RF photonic signals at different (non-interfering) wavelengths, are combined in a WDM multiplexer, before being applied to a single input/PD of the GAPC device. This multiplies the number of supported antenna elements by the number of wavelengths, e.g. a 32 PD GAPC device combined with 32 wavelength WDM can support 1024 antenna elements. This dual multiplexing scheme (WDM plus current combining) requires high power analog PD devices, the ideal approach being using a GAPC device composed of modified uni-traveling carrier (MUTC) PD devices [28].

A further extension, required for some systems with the highest spurious free dynamic range (SFDR) requirements, and for systems operating in frequency bands such as 5G cellular, is to include optical down-conversion within the system design, to overcome issues found with electronic mixing [66]. Converting RF photonic signals down near baseband allows the use of a

high-performance ADC, e.g. from 2 to 4 GHz, in this case reducing the required bandwidth of the GAPC device, i.e. operation to 5 GHz with low group delay variation would meet this need.

The use of a GAPC device provides tremendous gain in an Rx-ESA system, due to low loss combining of many RF photonic signals, e.g. 1024 signals, which may allow for the removal of low noise amplifiers (LNAs) at each antenna element, as well as providing sufficient optical power to support many RF Beams simultaneously [65].

4.5.2 The GAPC device

The GAPC is a fully distributed PD array that can maintain high bandwidth and low group delay variation across all inputs. In this sense, it acts as an RF photonic combiner by adding photocurrents from each optical input in phase at its RF output. Compared to traditional RF combining and optical combining into a single photodetector, the approach has several advantages, including seamless integration with the photonic front-end, low loss and wide bandwidth, and high-power capability. To meet the requirements for X-band phased array systems, the GAPC acts as an RF photocurrent combiner that can achieve very small group delay difference and wideband operation (0.1-15 GHz) i.e. flat frequency response in both, amplitude and phase, for all input signals. By using one PD in the GAPC for each channel, larger signals can be combined. This is not possible when using an only a single PD in a system, that will have limited power handling capability due to saturation effects, especially if a large number of signals are input to the single PD. Additionally, a single PD requires signal combination in the optical domain by couplers or multiplexers which will inevitably add extra loss to the system. However, it is well known that by increasing the number of PDs in a lumped-element PD array, more RC roll-off the array-photodetector will appear in the frequency response [40], and this creates nonlinear phase response which consequently produces larger group delay variation across frequencies. To compensate this, two approaches for PD integration are included in this work: (i) the traveling-wave circuit concept using fully distributed circuit elements in a transmission line, and (ii) loading PDs in an artificial transmission line based on lumped circuit elements. Fig. 4.15 (a) shows the 32-channel GAPC which uses a total of 32 PDs that are arranged in 8 groups and are distributed along a transmission line. The GAPC design is fully compatible with standard silicon photonics foundry processes and process design kits (PDKs), thus taking advantage of the ability to produce very large scale

photonic integrated circuit with high yield, and the devices in this work were fabricated at AIM Photonics.

Figure 4.15 (b) shows the GAPC chip which uses 32 of the AIM Photonics standalone Ge 'analog photodetectors', each with >34 GHz bandwidth according to the AIM PDK 4.0 document. Since each PD in the GAPC receives only a small fraction of the total optical input power, potential saturation effects can be 32 times smaller when compared to a single PD. Incorporating the photodetector array into a distributed circuit to form a traveling wave photodetector (TWPD) is crucial to maintain large bandwidth. To this end, a termination resistor R_{term} (50 Ω) is needed that minimizes reflections from the transmission line end that is opposite to the RF output. We combined 4 PDs in parallel as a "Group PD" (8 groups in total) in these GAPC devices; fewer or more PDs per group are possible, although there is an optimization in GAPC performance based on the number of PDs per group, e.g. a single Group of all of the PDs would provide a low bandwidth, while a single PD per group would make a more standard traveling wave array PD, however, with much larger RF losses due to higher Group PD resistance and very long transmission lines.

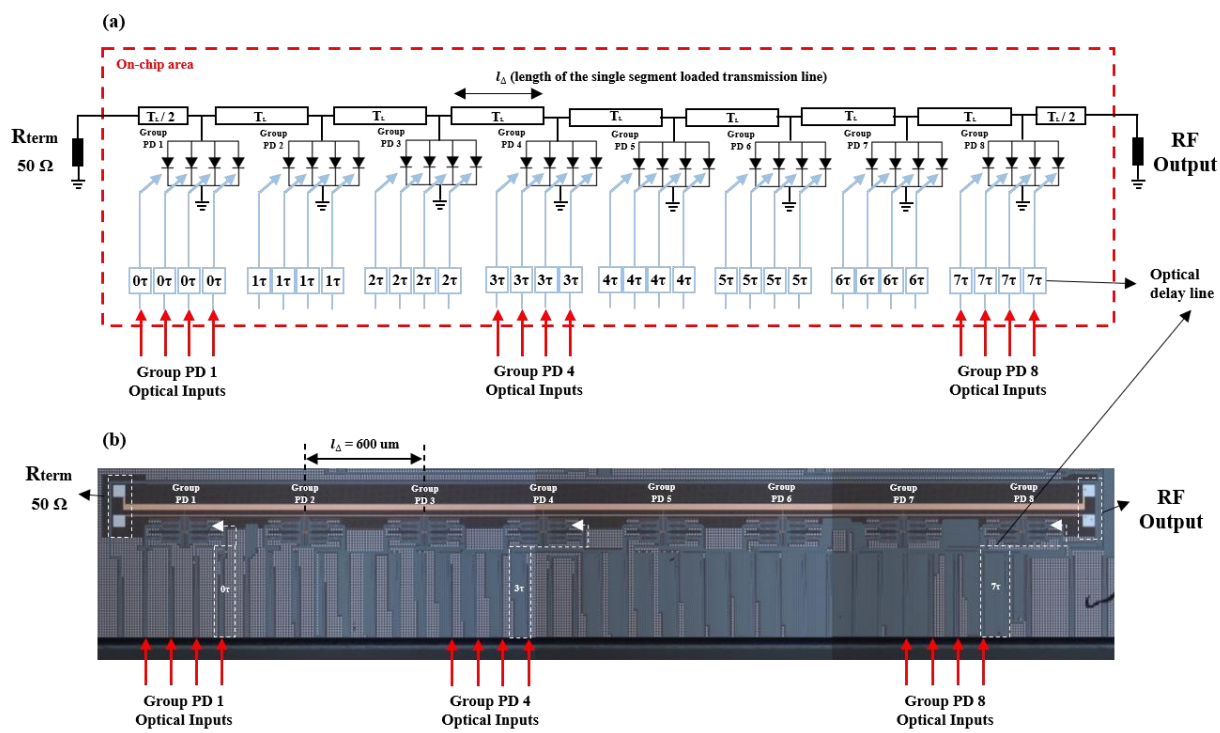


Fig. 4.15 (a) 32-channel GAPC (a) circuit and (b) chip microscope picture. To achieve RF phase matching and to account for the difference in optical and electrical signal velocities, we used 8 different optical delay line lengths that are labelled 0τ...7τ.

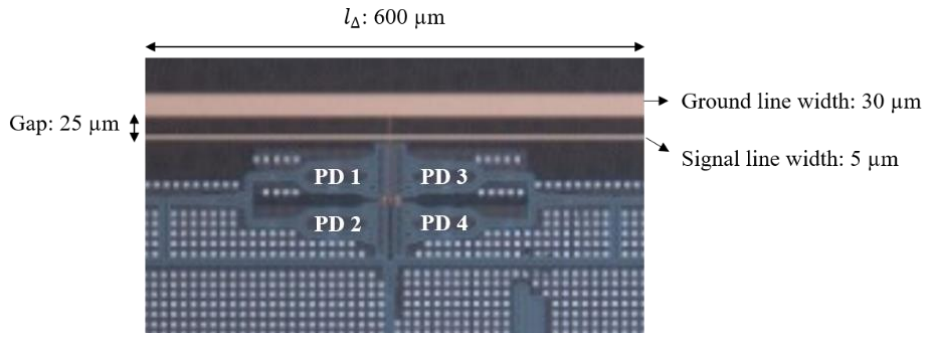


Fig. 4.16 Top view of single group in the GAPC consisting of 4 analog photodetectors from the PDK.

The first step of designing the GAPC is to build a distributed circuit including a transmission line model by incorporating the capacitive loading from single PDs that are readily available in the AIM Photonics PDK. This means a similar design approach by using Eq. 4.1 - Eq. 4.3 to design the loaded transmission line but the difference is that now C_p in the equations represents the total junction capacitance of 160 fF from each PD group. Figure 4.16 shows the dimensions of the single segment loaded transmission line connected to a Group PD. The length l_Δ is 600 µm with 30 µm and 5 µm width ground and signal lines, respectively. The gap between the signal and ground line is determined to be 25 µm. The designed impedance of the un-loaded and loaded transmission line are 140 Ω and 53 Ω. The electrical velocity v_e is 5.3×10^7 m/s which is 26% slower than the optical group velocity v_o (7.14×10^7 m/s). To compensate for this mismatch and to achieve RF phase match at the output of the GAPC, the lengths of optical delay lines are determined to be (N-1) × 810 µm (τ = 11.3 ps) for the N Group PDs.

To test the GAPC performance with using all 32 input signals simultaneously, and to simplify the experimental setup in terms of the number of required input fibers with matched lengths, we have also designed the GAPC with only a single optical input waveguide followed by integrated power splitters and the appropriate optical delay lines for phase matching of each PD group. Starting with a single input, light is split into 8 different delay lines, before it is then split again into the 4 PDs of each group PD. Fig. 4.17 shows the top view of the GAPC with single optical input.

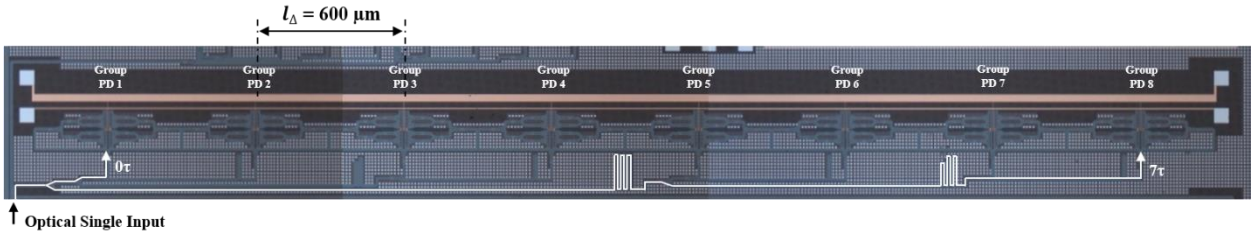


Fig. 4.17 Microscope picture of GAPC chip with single optical input.

4.5.3 DC Characteristics

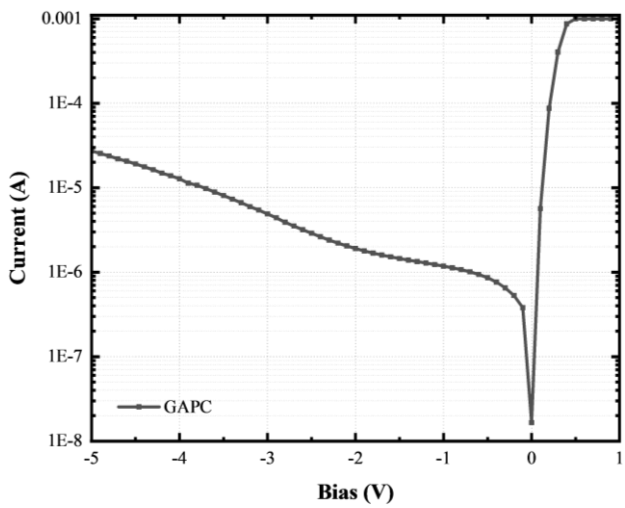


Fig. 4.18 I-V measurement of 32-channel GAPC.

Fig. 4.18 shows the I-V measurement of the GAPC. Since it is composed of 32 PDs, the dark current from all PDs is added and is measured to be 20 µA at -5 V which is somewhat higher than expected due to non-uniformity issues on this particular chip. To measure the DC responsivity, a laser at 1550 nm is used and fed through a polarization controller that is followed by a lensed fiber (2.6 µm spot size) for optimizing the light coupling from fiber to the waveguide edge coupler. After correcting for the fiber-chip coupling loss (5.8 dB), the responsivity of PDs in Group PD 1 is 0.87 A/W and 0.42 A/W in Group PD 8. It should be noted that for the Group PD 8, and in order to fit the 5.67 mm long optical delay line in a very limited tape-out space on the chip, 28 of the 90-degree bends with 5 µm bending radius are used which accounts for the 3 dB extra optical loss from the optical delay line. This extra loss can be prevented by using waveguide bends with larger radius at the expense of a slightly larger chip size.

4.5.4 RF Characteristics

4.5.4.1 S parameter Analysis

The first step is to verify the RF performance based on 2-port S parameters and determining reflection, insertion loss, characteristic impedance, and microwave effective index of the loaded transmission line. The measurement is done by using a Keysight PNA 67 GHz network analyzer without any light input. Fig. 4.19 (a) and (b) show the S11 and S21 respectively and compare between measurement and simulation results of the GAPC at 5 V reverse bias. For the S11, we measured -15 dB up to 20 GHz which corresponds to a 50 Ω impedance transmission line as shown in Fig. 4.20 (a). On the other hand, the insertion loss (S21) is measured to be 3 dB down up to 12 GHz and 10 dB down up to 18 GHz. The RF loss is mainly contributed by the photodiode series resistance (Rs), ohmic loss from the copper (Cu) based transmission line, and the relatively low Si substrate resistivity (8-10 Ω-cm). For the phase matching, we measured the microwave effective index to be around 5.6 up to 20 GHz (4.20 (b)). Compared with the optical effective group index of 4.2, the electrical velocity is ~26% slower than the optical group velocity as expected. In other words, the implemented optical delay line design should provide sufficient phase matching. This phase matching will again be verified in the next section from the bandwidth measurement results.

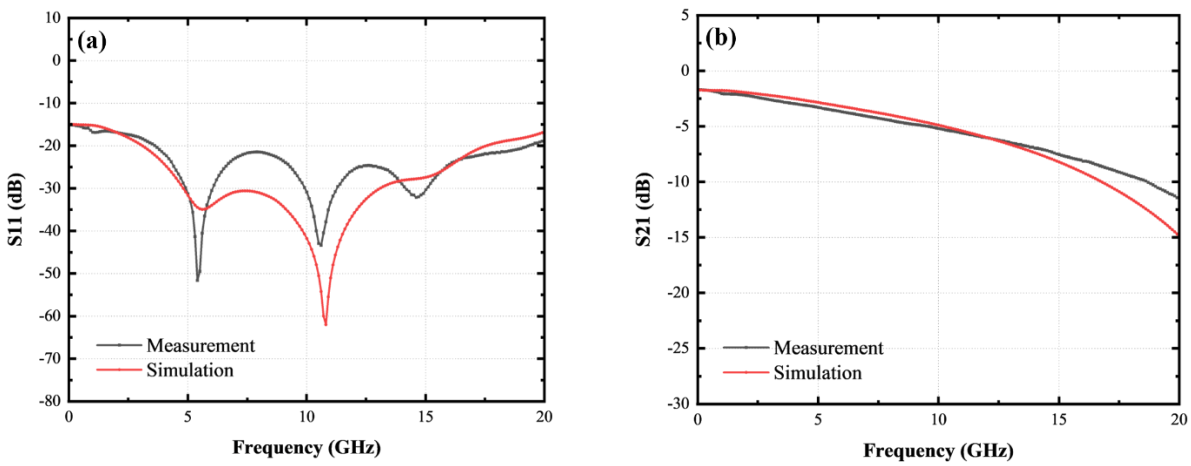


Fig. 4.19 Comparison of measurement and simulation results of the GAPC, (a) S11 and (b) S21.

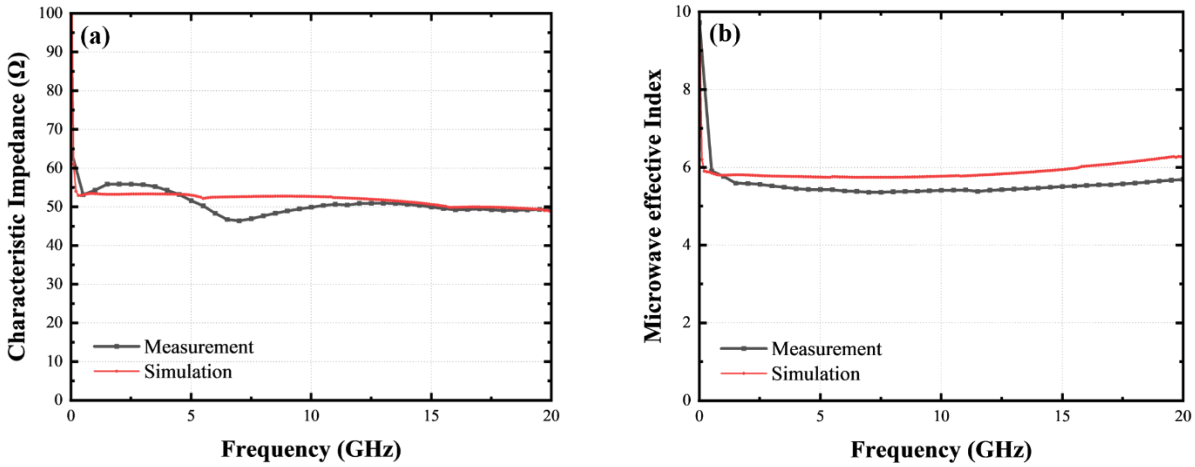


Fig. 4.20 GAPC (a) characteristic impedance and (b) microwave effective index.

4.5.4.2 RF Output Power and Bandwidth

With the verified performance of the GAPC from S parameter characterization, we then to shift the focus to the GAPC for its o/e RF performance, phase response and group delay (shown in the next section) investigation. First part of the demonstration is to use the same optical heterodyne approach reported in [40] to measure the absolute RF output powers by fixing it at -5 dBm for 5 GHz and -10 dBm for 10 GHz with the corresponding photocurrents from all the 32 channels in the GAPC (Fig. 4.21 (a)). To match the RF power from all the channels to -5 dBm at 5 GHz, ~11 mA photocurrent has measured from the Group PD 8 and with a gradual increase current up to ~15 mA from the Group PD 1 for compensating the RF loss. And for matching the power to -10 dBm at 10 GHz, 5 mA current has measured from Group PD 8 and increased up to 10 mA form Group PD 1. For the 10 GHz signal, the maximum imbalance of photocurrent is up to 5 mA between all groups since the Group PD 1 has a larger RF roll-off at 10 GHz that can be seen from the later introduced S21 measurement shown in Fig. 4.22 (a).

Next part of the demonstration is the bandwidth performance. Here, the PNA is used together with a commercial 40 GHz Lithium Niobate (LN) modulator for measuring the GAPC's frequency response. To obtain the bandwidth of the GAPC, all the losses from the RF cable, adapters, and modulator RF response are calibrated out after the measurement. A 1550 nm laser is used and fed into the modulator which is followed by a polarization controller and taper lensed fiber. In Fig. 4.21 (b), the frequency responses of all four PDs in the Group PD 5 are shown with an almost

identical bandwidth of 21 GHz showing identical RF behavior within the Group PD. The measured frequency responses of each group PD (from Group 1 to Group 8) are shown in Fig. 4.22 (a) and are compared to the simulation in Fig. 4.22 (b) with a good agreement. Since the total length of the GAPC is 5 mm, the RF signal is expected to suffer RF transmission loss mostly from the photodiode series resistances and the conductor loss especially for the Group PD 1 that has the farthest transmission distance from the load side. Therefore, as expected, the bandwidth degrades from Group PD 8 of 30 GHz down to Group PD 1 of 15 GHz. In particular, for the frequency range of interest from 2 GHz to 5 GHz, all group PDs have flat frequency responses.

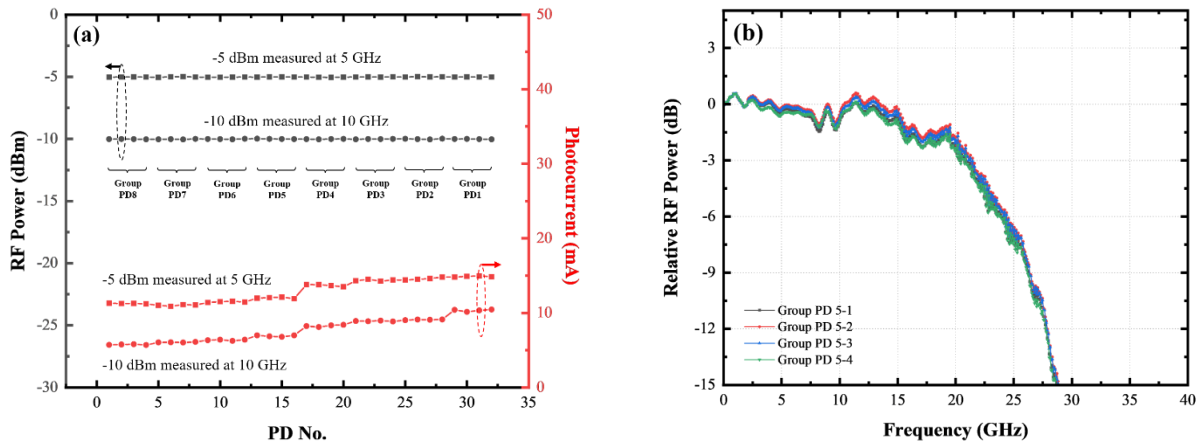


Fig. 4.21 (a) -5 dBm and -10 dBm measured RF power with the corresponding photocurrents from 32 PDs at 5 GHz and 10 GHz respectively and (b) the frequency responses of all four PDs of one Group PD in the GAPC.

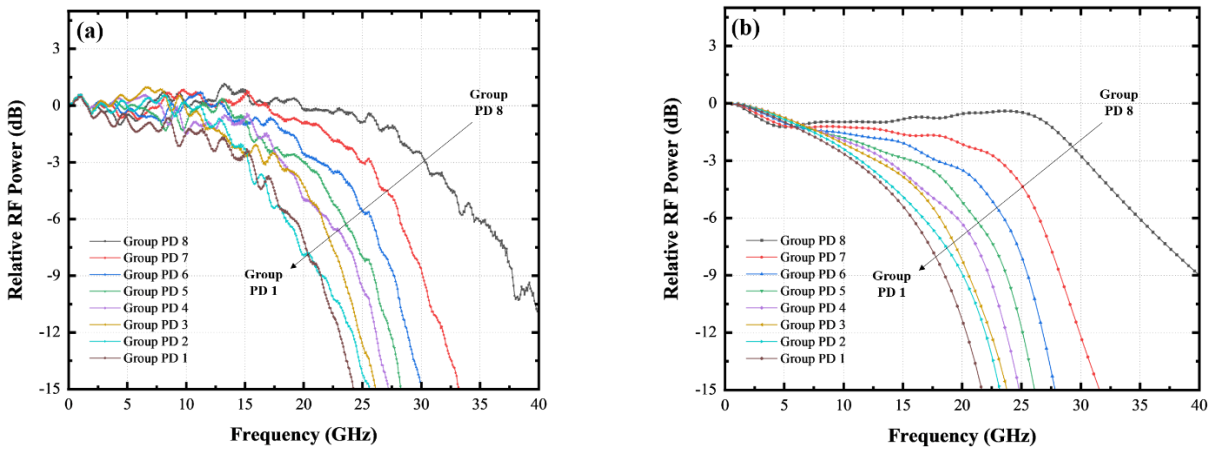


Fig. 4.22 The S21 of each group PDs (Group 1-Group 8) in the 8-element GAPC individual inputs (a) measurement (b) simulation.

The RF saturation measurements are also conducted from one of the PDs in Group PD1 and Group PD8 at 5 GHz (Fig. 4.23 (a)) and 10 GHz (Fig. 4.23 (b)). At 5 GHz, we have measured the saturation output power at -5 dBm from Group PD 8 and -6.5 dBm from Group PD 1. And the 1dB saturation currents of both Group PDs are 10.5 mA. On the other hand, -7.5 dBm output power from Group PD8 and -12 dBm from Group PD1 are measured at 10 GHz. And the 1-dB saturation currents of both Group PDs are 8.5 mA. To this end, we have first verified that the GAPC is able match the RF output power to the same -5 dBm level at 5 GHz from all 32 channels shown in figure 4.21 (a). Also, in figure 4.23 (a), we have characterized the saturation current of the loaded PD in the GAPC at 5 GHz to be 10.5 mA which leads to the output power of -5 dBm. This means that the GAPC has the potential to combine the signals from all channels at the total photocurrent of, for example, 10.5 mA × 32 = 336 mA. In should be mentioned that a GAPC transmission line test structure has been tested to sustain DC photocurrents as high as 350 mA.

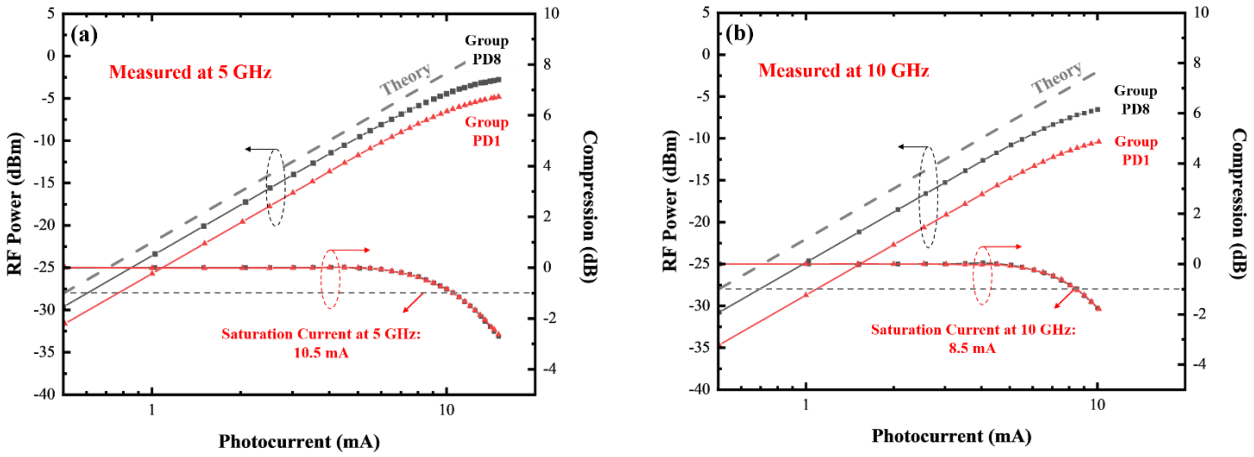


Fig. 4.23 RF saturation measurements of one of the PD in Group PD1 and Group PD8 at (a) 5 GHz and (b) 10 GHz.

Next, I measured the bandwidth of the GAPC with single optical input to verify the overall frequency response. This GAPC test structure is used to further verify whether phases are matched based on the silicon waveguide characteristics. In Fig 4.24, 15 GHz bandwidth is measured at 10 mA total photocurrent and good agreement with the simulation is found. I also measured the frequency response when the left side of the GAPC is not terminated with a 50 Ω resistor (i.e. open) and obtained a bandwidth of only 2.5 GHz. This can be attributed to the fact that the reflected signal does not add in phase at the output of the GPAC. A slightly degraded bandwidth of 13 GHz

is measured when increasing the photocurrent to 10 mA. At this photocurrent the GAPC delivers -1 dBm RF output at the load which is sufficiently high to drive the following electronics such as an A-to-D converter.

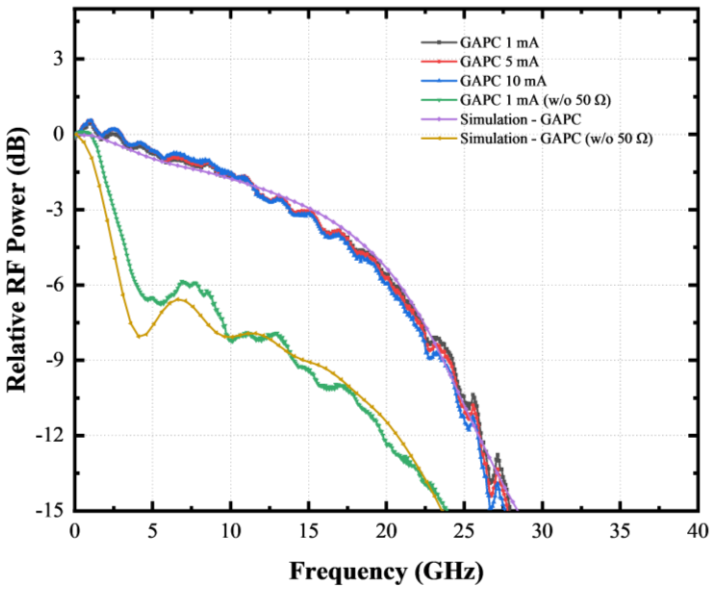


Fig. 4.24 Frequency responses of the GAPC and simulation results.

4.5.4.3 Phase Response and Group Delay

For applications that require wideband signals such as pulsed signals, a linear phase response i.e. low group delay scatter or group delay variation in the GAPC is essential to maintain high signal integrity across all channels. The group delay for each group PD was calculated from the phase response that was measured with the PNA. Fig. 4.25 (a) shows the measured and fitted phase responses based on the second order polynomial function for all group PDs. The GAPC shows a linear phase response and a group delay scatter of only 6 ps up to 10 GHz (Fig. 4.25 (b)). I also calculated the phase response of an ideal, but lumped element 32-PD array that has larger 9.8 ps group delay differences up to 10 GHz to illustrate the advantage of our fully distributed GAPC design.

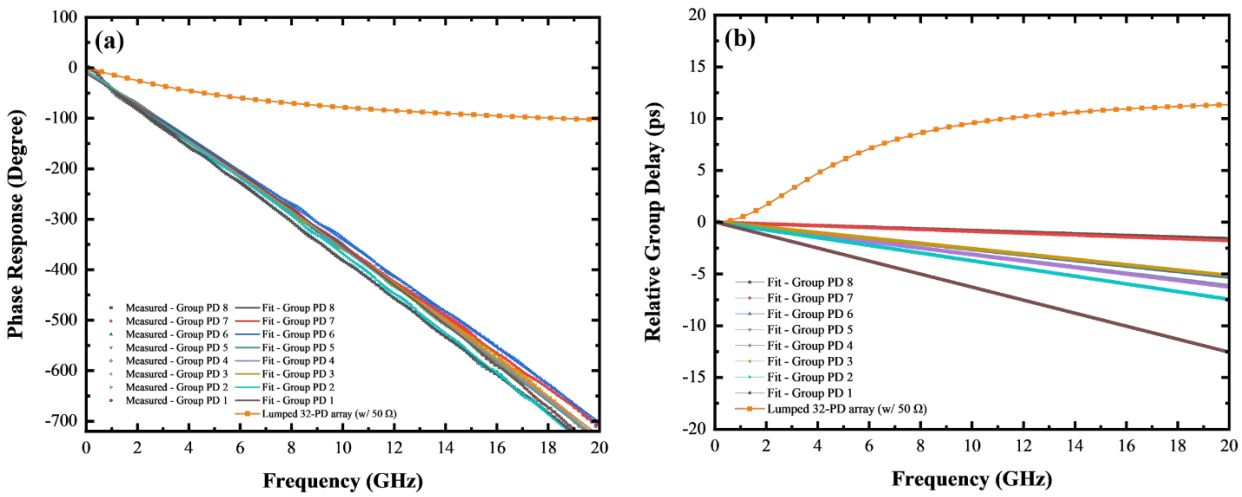


Fig. 4.25 (a) the phase response of Group 1 to Group 8 PDs in the 8-stage GAPC and compare with lumped 32 PD array (b) the group delay from the first derivative of the fitted phase response of Group 1 to Group 8 PD in the 8-stage GAPC and compare with lumped 32 PD array.

4.5.5 Balanced GAPC

In RF photonic systems, balanced PDs are useful for common mode suppression and, for example, in photonic up- and downconverters where the signal is mixed with a local oscillator (LO) signal. Hence, I also demonstrate a balanced type of GAPC in this work. In this design, I take an alternative method to construct the balanced GAPC (B-GAPC) using lumped circuit elements to achieve an impedance match to 50 Ω. To connect Group PDs, I now use spiral inductors which are designed to compensate the capacitive loading of the Group PDs. Similar bandwidth performance but roughly 50% total device length reduction is expected owing to the fact that we can design a larger inductance per length with a spiral inductor that this is not possible with a transmission line. To design the circuit, now the difference is that I use eq. 4.1-3 and replace the C and L per unit length with the absolute numbers from the spiral inductor. Again, the C_p represents the total photodiode junction capacitance of the group and L is the value of the designed spiral inductor. The inductor is a square-loop type spiral inductor that is 10 µm wide and has an overall footprint of only 120 µm by 120 µm. Based on the ADS EM simulation, the inductor has an inductance of 80 pH, 20-fF self-capacitance, and 3-Ω series resistance. Therefore, the total capacitance of each stage used in the eq. 4.1-3 is now the summation of the junction capacitance C_p (160 fF) and the 20 fF self-capacitance from the spiral inductor. As shown in fig.4.26, I have designed a B-GAPC with 4 Group PDs each having a total of 8 PDs in balanced configuration. PDs that require a

negative [positive] bias are labeled as PD(-) [PD(+)]. The design includes on the left side two parallel combined 100 Ω resistors for on-chip termination. Additionally, I have incorporated an on-chip biasing circuitry made of metal-insulator-metal (MIM) on-chip capacitors and metal resistors. I included 8 MIM capacitors that are connected in series with the different Group PDs respectively (4 Group PD on each side). These capacitors serve as DC blocks and allow us to apply the two opposite voltages to reverse bias the PDs. The key advantage of this design is that now it merely needs one regular GSG probes for biasing which eases the measurement setup significantly. It also simplifies a potential future packaging of the chip. Each capacitor has the dimension of 70 µm × 340 µm and 1.5 pF. For testing, I designed the B-GAPC with two optical input waveguides followed by power splitters and optical delay lines. This way we can separately illuminate all PD(-) and all PD(+) PDs in the B-GAPC (fig. 4.26). The length of the optical delay line for a single segment is designed to be 1.61 mm based on C_p and L from the model to match the RF phase. Figure 4.27 shows a picture of the fabricated chip.

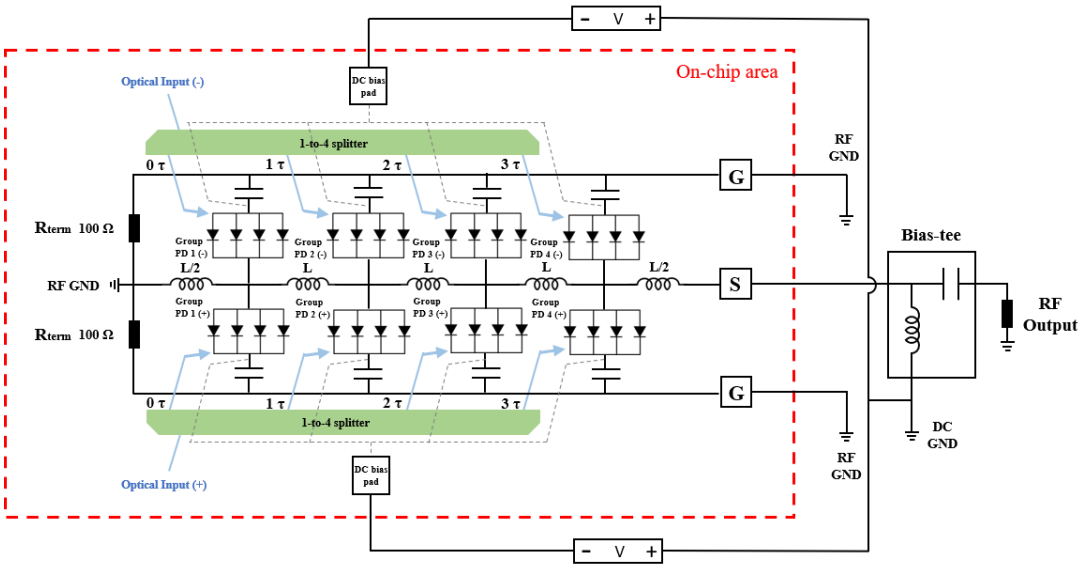


Fig. 4.26 Schematic of the 16-channel B-GAPC circuit.

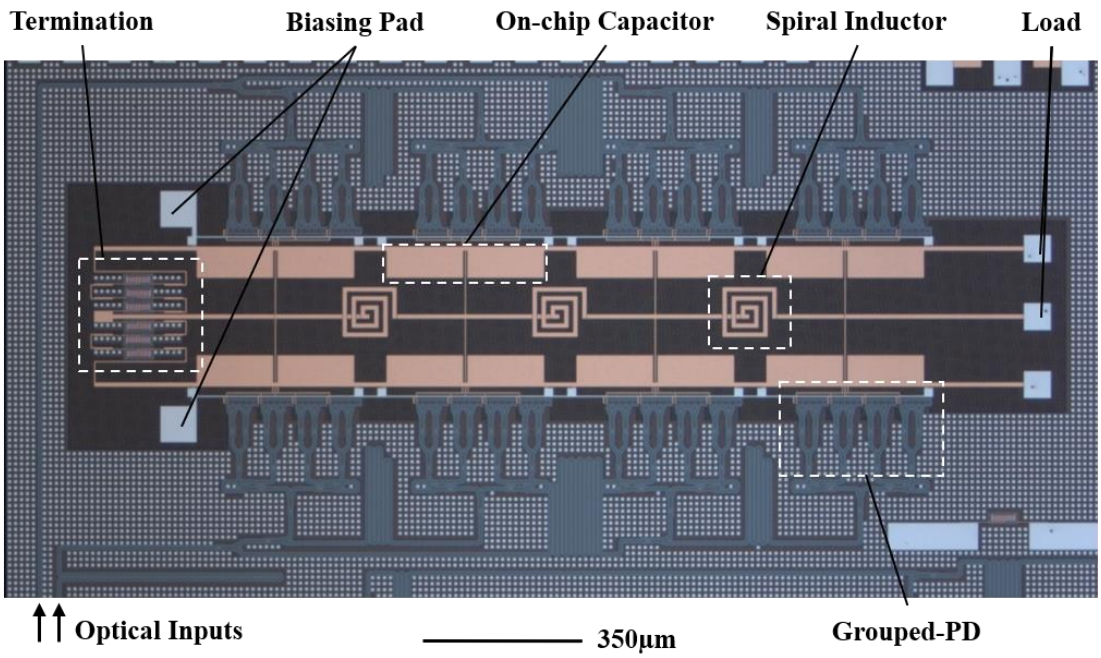


Fig. 4.27 Top view of the B-GAPC chip.

4.5.6 RF Characteristics

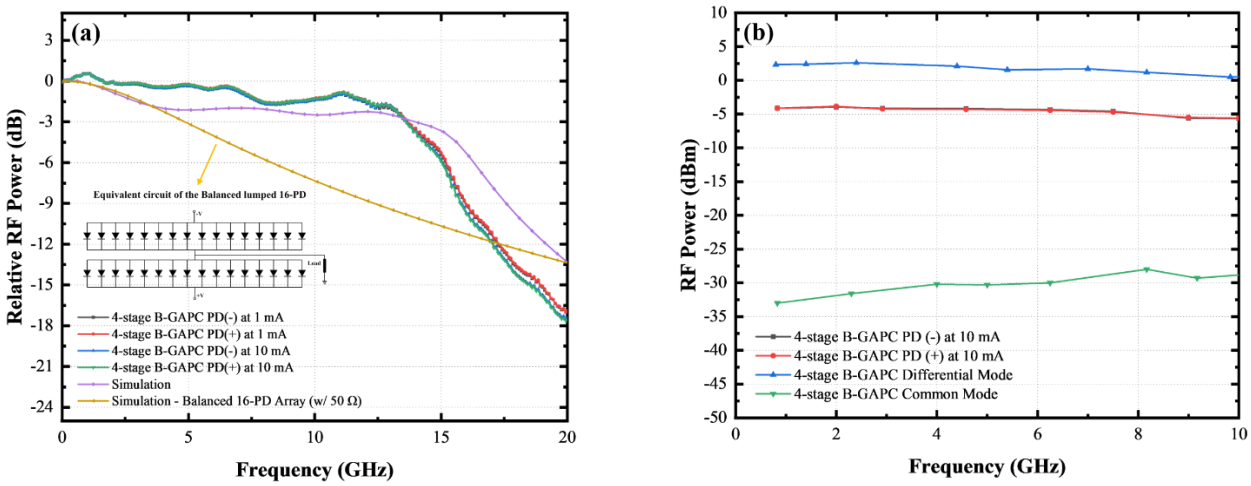


Fig. 4.28 (a) measured and simulated frequency responses of the B-GAPC by PNA approach and compare with a simulated lumped balanced 16-PD and (b) measured bandwidth for the PD(-) and PD(+), differential mode, and common mode using the optical heterodyne setup.

Fig. 4.28 (a) shows the bandwidth measurements at 1mA and 10 mA together with the simulation results. The frequency responses of the PD(-) and PD(+) are in very good agreement up to the 3-dB bandwidth of 13 GHz at 1 mA. A slight bandwidth degradation can be observed at 10 mA. It

is worth noting that compared to a balanced lumped 16-PD array, a 2.5X bandwidth improvement is achieved using the impedance matched B-GAPC. Figure 4.28 (b) also shows the bandwidth measurements of PD(-) and PD(+) in both, differential and common mode. In differential mode we observe the expected 6 dB RF power improvement while the common mode rejection ratio is 30 dB up to 10 GHz. Fig. 4.29 (a) shows the B-GAPC phase responses up to 20 GHz indicating a linear response. For the group delay shown in Fig. 4.29 (b), we have successfully demonstrated the group delay difference to be 2 ps of the GAPC concept between 2 to 5 GHz which is 2X better than that of a lumped PD array that was added for comparison.

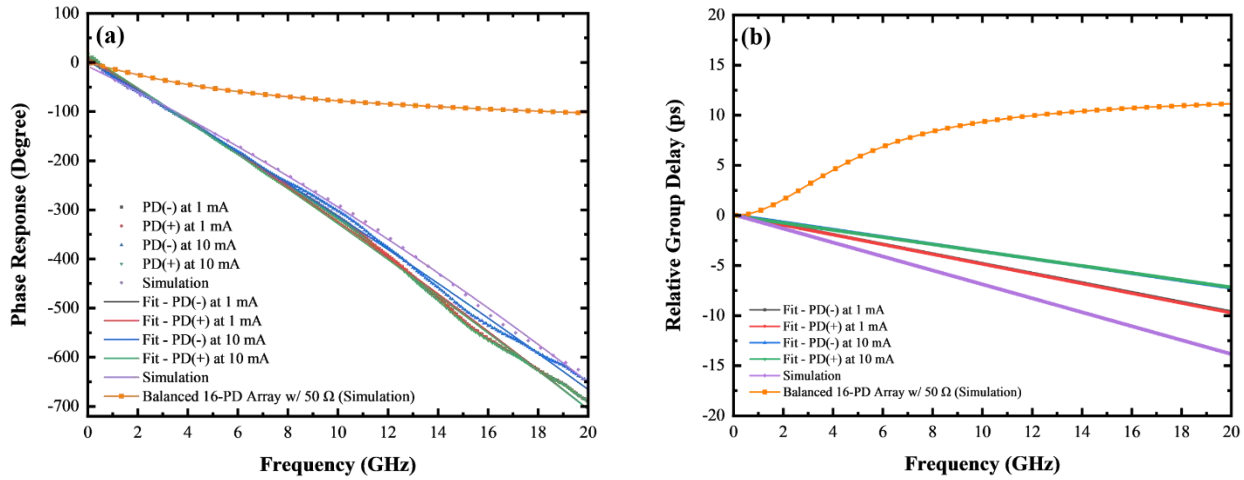


Fig. 4.29 (a) Measured and simulated phase responses of the B-GAPC at 1 mA and 10 mA. Also shown is the simulated response of a lumped balanced 16-PD array (b) measured and simulated group delay of the B-GAPC at 1 mA and 10 mA and compare with a lumped balanced 16-PD array.

4.6 - Summary of this work

In this chapter, TWPD and a new balanced TWPD with integrated bias circuits enabled by AIM Photonics platform and its PDK are demonstrated. For the TWPD with integrated bias circuit, 32 GHz bandwidth measured at 1 mA has been achieved, and 6 dBm RF output power at 44 mA at 30 GHz has been demonstrated. On the other hand, a 25-GHz-bandwidth TWBPD with integrated bias circuit that has above 30 dB common mode rejection ratio up to 40 GHz is reported. This is the very first silicon-foundry-based high-speed balanced TWPD. Additionally, a novel Group Array Photodetector Combiner (GAPC) was demonstrated in a Si photonics foundry process. Firstly, 8-element GAPC (32 PDs loaded) of the 32 individual-inputs type and the GAPC test structure have been demonstrated. The bandwidths of all group PDs in the 8-stage GAPC -

individual inputs are demonstrated with rather flat response up to 10 GHz when compared with lumped PD array. The 8-element GAPC test structure (single input) has achieved 15 GHz and 13 GHz bandwidth at 1 mA and 10 mA respectively. Accordingly, more linear phase response has achieved from the 8-element GAPC together with < 5 ps group delay difference comparing with the lumped type (< 10 ps) within 10 GHz. In the second part of the work, 4-stage balanced GAPC (16 PDs loaded on each side) has also been introduced by integrating with on-chip biasing capacitor and termination resistor. The 3-dB bandwidth of 13.5 GHz has been reached at 1mA and 10 mA. Using the optical heterodyne approach, the differential mode with 13.5 GHz bandwidth and 6 dB RF power improvement and the common mode rejection ratio of > 30dB up to 10GHz are demonstrated.

Last but not least, the state-of-the-art Ge-on-Si PDs with the reported RF output power as a function of measured frequency are shown in the figure 4.30. Based on this figure, we can see that the lumped PD arrays described in chapter 3 achieved a record high RF output power in the frequency range between 5-20 GHz. Additionally, the TWPD with integrated bias circuit introduced in this work has achieve 6 dBm output power at 30 GHz. The measured power is close to the other reported numbers, however, the RF output power at 6 dBm is not saturated yet but limited by the silicon edge coupler failure and the TPA induced optical loss. To further improve the RF output power, replacing the silicon waveguide delay line and edge coupler with the SiN counterparts for TWPD redesigning will be the next promising step.

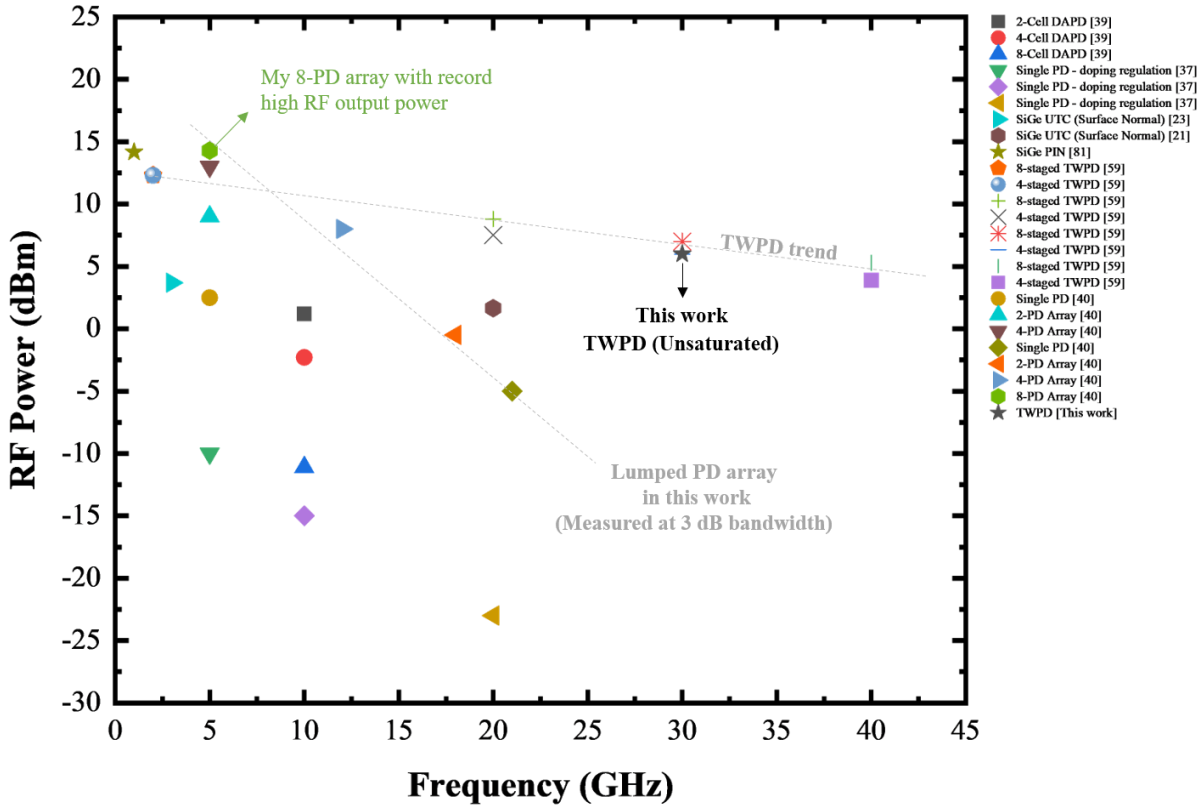


Fig. 4.30 The state-of-the-art Ge-on-Si PD with the reported RF output power versus measured frequency.

Chapter 5 - Micro Transfer Printable O-band InP-based MZM Modulator

5.1 - Introduction

In this chapter, a micro transfer printable high-speed O-band multi-quantum well (MQW) Mach-Zehnder modulator is introduced. The electro-optic effects that are used in the push-pull scheme modulator will be explained first. Then, MQW epi layer design and printable modulator fabrication process flow will be discussed. Finally, characterizations of bar level modulators (not for printing) will be presented including passive section testing, static characterization, RF performance. Followed by this, a summary and future works will be given.

5.2 - Review of modulator working principle

5.2.1 Electro-Optic Effects

The electro-optic effect is a physical mechanism that plays a critical role in a modulator. By applying a reverse bias to the modulator active section that is consisted of a semiconductor p-i-n junction, the presence of the electric field in the depleted region will change the refractive index of the junction material based on the crystal direction. The index change leads to a change of the optical phase which can then be converted to an intensity modulation in a Mach-Zehnder interferometer (MZI).

The main two electro-optic effects that are involved in our modulator active section are listed below:

- Pockels effect

  The Pockels effect is an anisotropic effect that is proportional to the electric field which is also called linear electrooptic effect. When applying an electric field, the index change is proportional to the field as shown in below,

  $$\Delta n_{pockels} = \frac{1}{2} n^3 r_{41} E \qquad \textbf{Eq. 5.1}$$

  where n is the refractive index of the material, r_{41} is the Pockels effect coefficient, and E is the applied electric field. To be noted that the Pockels effect depends on the direction of the applied electric field to the orientation on the crystal.

- Quantum confined stark effect (QCSE)

  The QCSE is the key electro-optic effect that we utilized in our modulator. This is a second order EO effect that is proportional to the square of the applied field inside the MWQ layer in the active section of the modulator and which can be written as:

$$\Delta n_{QCSE} = \frac{1}{2} n^3 R E^2 \qquad \textbf{Eq. 5.2}$$

  where R is the quadratic EO coefficient. [67]

5.2.2 Push-Pull MZI Modulator

By incorporating the EO effect into a MZI structure, both arms can be driven simultaneously by an externally applied electric field (same reverse voltage level) to produce a differential drive, and this type of modulator is working under the push-pull scheme. Compared to a single arm drive MZM modulator, the push-pull scheme can provide the same amount of phase shift with a lower voltage and chirp can be eliminated. The Fig. 5.1 shows the working principles of a single drive and a push-pull MZI modulator. And table 5.1 is to define the modulator metrics that will be used in the later sections.

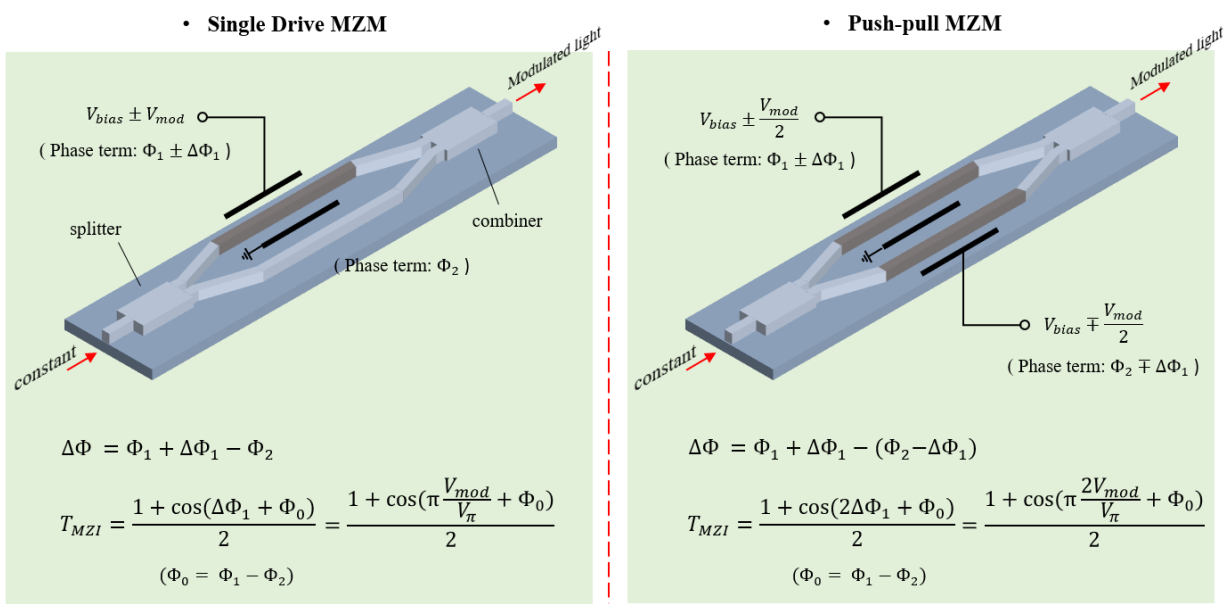


Figure 5.1 Single drive and push-pull MZM Modulator.

Table 5.1 Modulator metrics.

Metric	Unit
V_π	V
$V_\pi \cdot L$	V·cm
Extinction Ratio (ER)	dB
Insertion loss	dB

To be noted that in the table 5.1, V_π (halfwave voltage) represents how much voltage is needed to generate a π phase shift based on the modulator sinusoidal transfer function. And $V_\pi \cdot L$ describes how much V_π is needed for a given modulator active length L. Usually, V_π or $V_\pi \cdot L$ should be as low as possible to achieve low power consumption and relatively short modulators with small footprint. The extinction ratio is defined to be the power on-off ratio based on the modulator transfer function. Finally, the insertion loss in this work is defined to be the on-chip device loss after calibrating out the fiber-to-chip and chip-to-fiber coupling loss.

5.3 - Modulator Epi design and fabrication flow

The modulator epi layers are shown in Fig. 5.2. Starting from the p-type top layers, a 50 nm InGaAs contact layer is grown on top of a 1000 nm thick InP cladding layer to reduce the series resistance. Beneath the p cladding layers, 54 pairs of $In_{0.53}Al_{0.17}Ga_{0.3}As$/ $In_{0.53}Al_{0.35}Ga_{0.12}As$ multi quantum wells (700 nm thick) are designed for reducing the junction capacitance and the absorption edge at 1200 nm wavelength. The MQWs are sandwiched by the P-type cladding and the N-type InP bottom cladding and highly doped contact layers. To be noted that, the thickness of p cladding layer and n cladding layers are optimized to avoid metal contact layer and induced free carrier absorption and an adequate mode confinement factor to offer a better absorption efficiency for the fundamental optical mode in the active junction region that acts as the waveguide core. Then, a 2309 nm thick n.i.d. InP layer is inserted below the n-contact layer as the spacer layer. This spacer layer is used to match the height difference between the III-V waveguide and the SiN waveguide after it is transfer printed for efficient optical coupling. Finally, the 10 nm InGaAs (upper layer) and 490 nm InAlAs (lower layer) are embedded between the spacer and the InP substrate layer as the release layer. During the transfer printing step, these two layers will be etched away to detach the modulator chip from the InP source substrate.

P-contact, $In_{0.53}Ga_{0.47}As$, 50 nm, p++, Zn, 1e19
P-cladding, InP, 300 nm, p+, Zn, 5e18
P-cladding, InP, 400 nm, p+, Zn, 1e18
P-cladding, InP, 300 nm, p, Zn, 5e17
QW Top barrier, $In_{0.53}Al_{0.35}Ga_{0.12}As$, 5nm, u.i.d
MQW QW, $In_{0.53}Al_{0.17}Ga_{0.3}As$, 8nm, u.i.d
MQW barrier, $In_{0.53}Al_{0.35}Ga_{0.12}As$, 5nm, u.i.d
N-cladding, InP, 200 nm, n, Si, 5e17
N-contact, InP, 300 nm, n++, Si, 1e19
Spacer, InP, 2309 nm, u.i.d
Release layer, $In_{0.53}Ga_{0.47}As$, 10 nm, u.i.d
Release layer, $In_{0.52}Al_{0.48}As$, 490 nm, u.i.d
S.I. InP substrate

Figure 5.2 Modulator epi layers (designed by Dr. Keye Sun).

Overall, there are 17 steps to finish the printable modulator, and these are shown in figure 5.5 (step 1 – step 11) and figure 5.6 (step 12 – step 15). Starting with steps 1 to 11, the bar level modulator fabrication is completed first. And after the step 11, figure 5.4 shows the modulator chip layout (where to cleave) and the top view microscope pictures of the cleaved portion of bar-level modulators and printable modulators. Above the red dashed line are modulators for bar-level testing while all other devices are designed for transfer-printing. After finishing the fabrication step (Fig 5.5), all modulators on the chip are plated with gold to form probing pads and are ready for IV testing. We then cleaved the modulators for the bar-level testing only portion, and more steps are needed for preparing the lower part of the die for transfer printing (the part of the layout below red dash line) which are shown in Fig. 5.6 step 1 to step 7. And, Fig. 5.3 shows a more

detailed view of a bar-level modulator. Each modulator has two heater sections that sit aside of the two modulator arms respectively. And two RF pads matched to 50 Ω are connected to the two p-types active sections on each arm, respectively. Another DC pad connects to the N mesa for DC biasing.

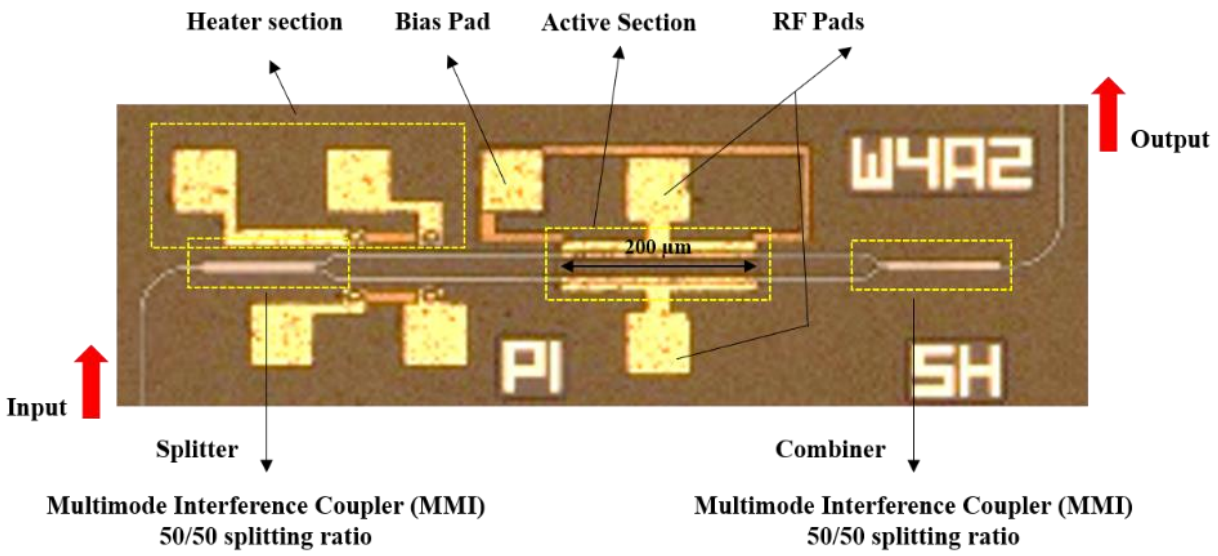


Figure 5.3. Fabricated bar-level MZM modulator.

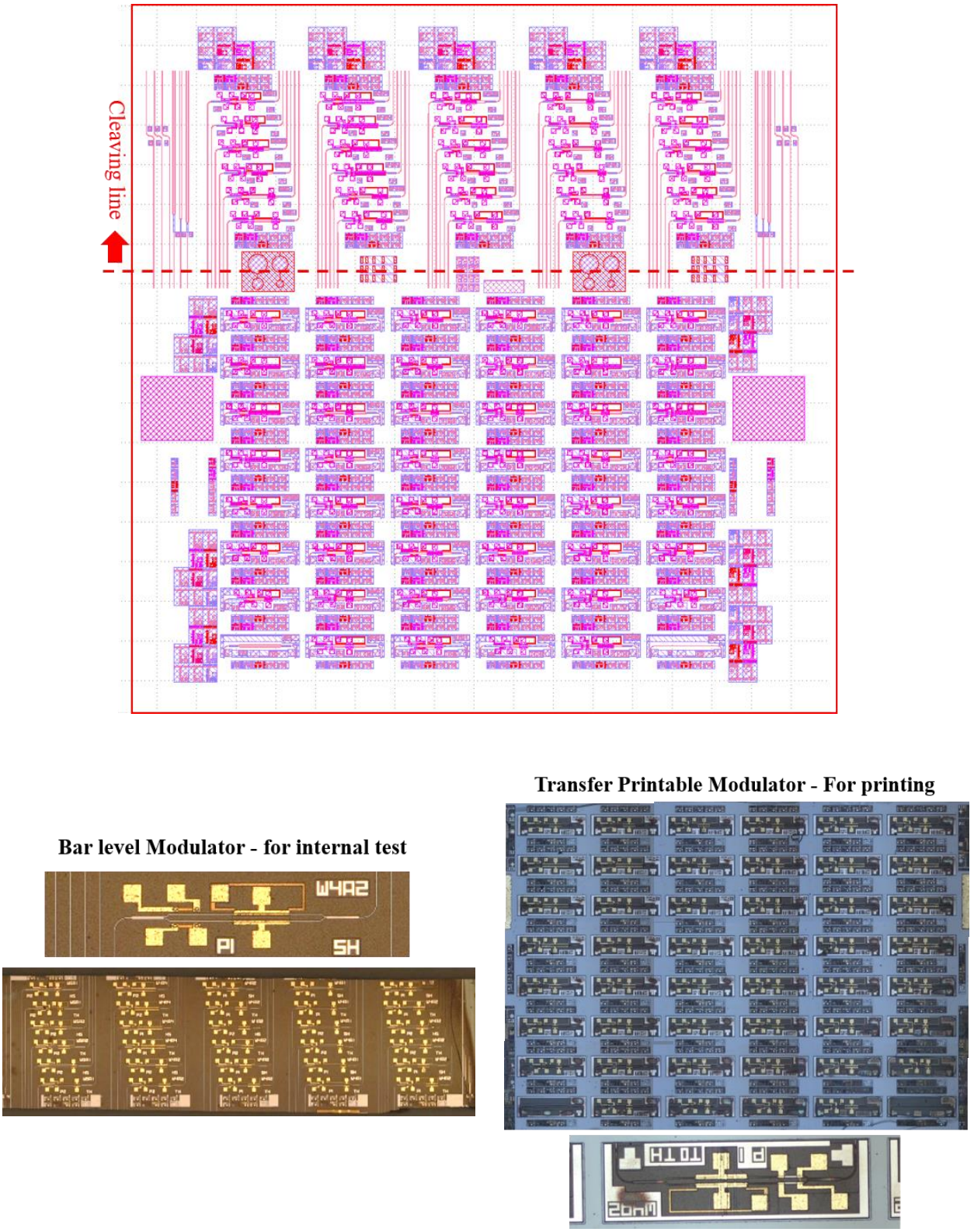


Figure 5.4 Modulator chip layout (top) and fabricated bar-level (bottom left) and printable modulator (bottom right) portions after chip was cleaved.

Here, the modulator fabrication process flow will be shown in detail that is based on a printable modulator top view, active cross-section view, and the etched facet cross-section view. Before the process, we decided to fabricate the modulator (waveguide active section) along both the [110] and [-110] InP crystal orientations to investigate how Pockels and QCSE effects can affect the V_{pi} characteristic. The fabrication, from Fig. 5.5 step 1-step 11, was carried out by depositing a P metal, Ti/Pt/Au/Ti (20nm/20nm/20nm/20nm), on top of the p cladding layers (step 2). And next, around 700 nm SiO_2 is deposited on top of the p metal for the waveguide hard mask formation (step 3). Then, a N_2/Cl_2-based recipe was used in the Oxford ICP RIE to dry etch through the P mesa and MQW layers for the waveguide formation and to stop at the N contact layer (step 4). Most importantly, the modulator facets for printed modulators are etched and formed in this step. Next, in step 5, the N mesa will be defined by dry etching deeper to the InP spacer to make sure all the modulators on the chip are fully electrical disconnected. In the meantime, the p-type passive portion of the modulator will be etched and thinned down to 400 nm for defining the active section. To be noted that this step is also to form the printed modulator chiplet area. After this step, the N metal and heater metal with 20 nm Ti and 80 nm Au are deposited on top of the N contact layer and n-type InP spacer accordingly (step 6). Next, in step 7, the MQW wet etch undercut will be conducted to make the MQW waveguide narrower and ensure single mode operation. A 300 nm thick SiO_2 is then deposited on top of everything as a protection (passivation) layer. The SU8 planarization followed by O_2 plasma etch-back is carried out by coating a thick SU8 layer on top of the protection layer (step 8 + step 9). After the planarization, dry etching with a combination of O_2 plasma and CHF_3 will be used to open the P and N contact window (step 10) for the final step 11 - seed layer and gold plating. After this step, bar level InP-based modulators are ready to be cleaved and tested.

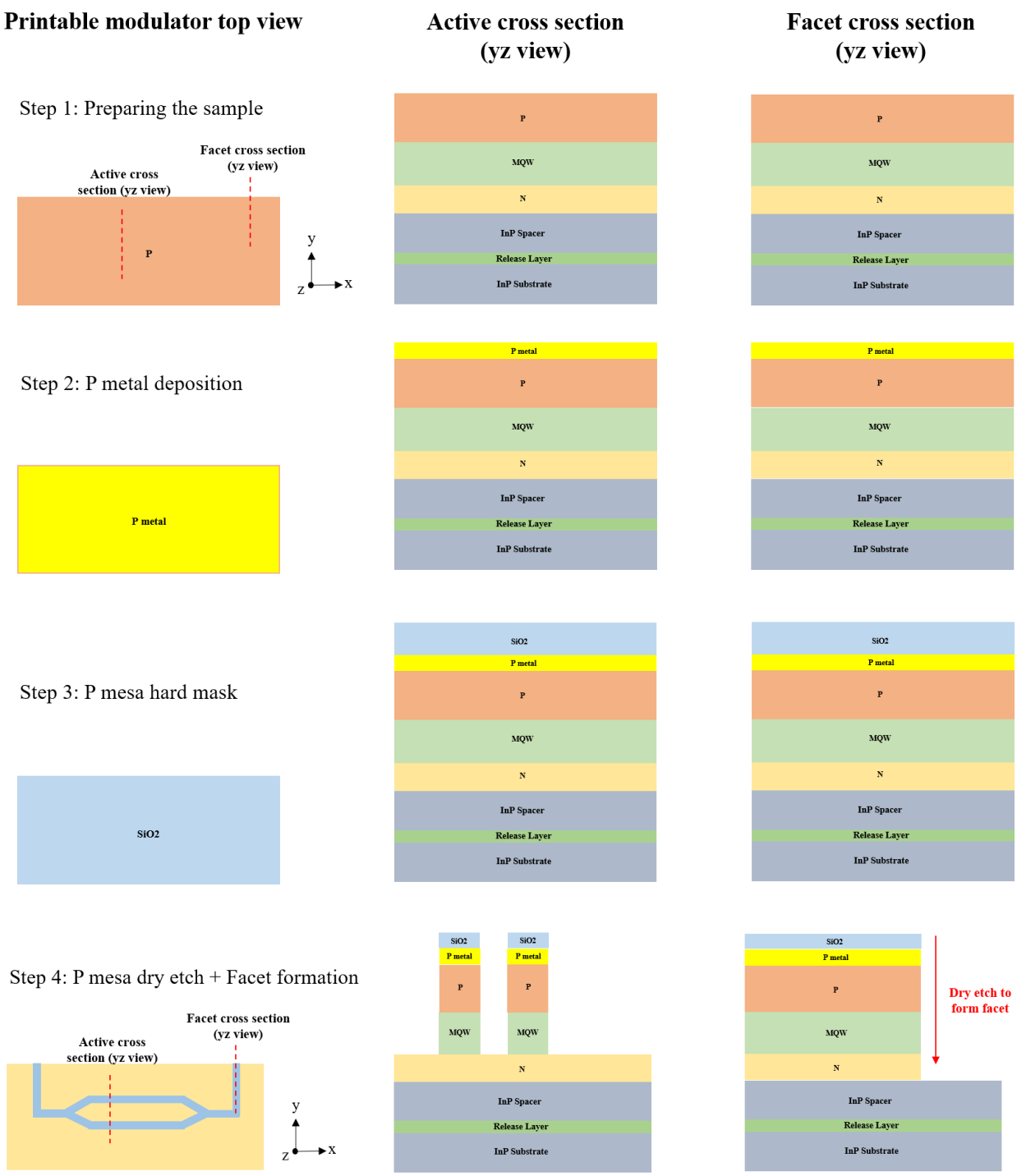


Figure 5.5 Step 1 - step 4: Modulator fabrication process flow showing the printable modulator top view, active, and facet section.

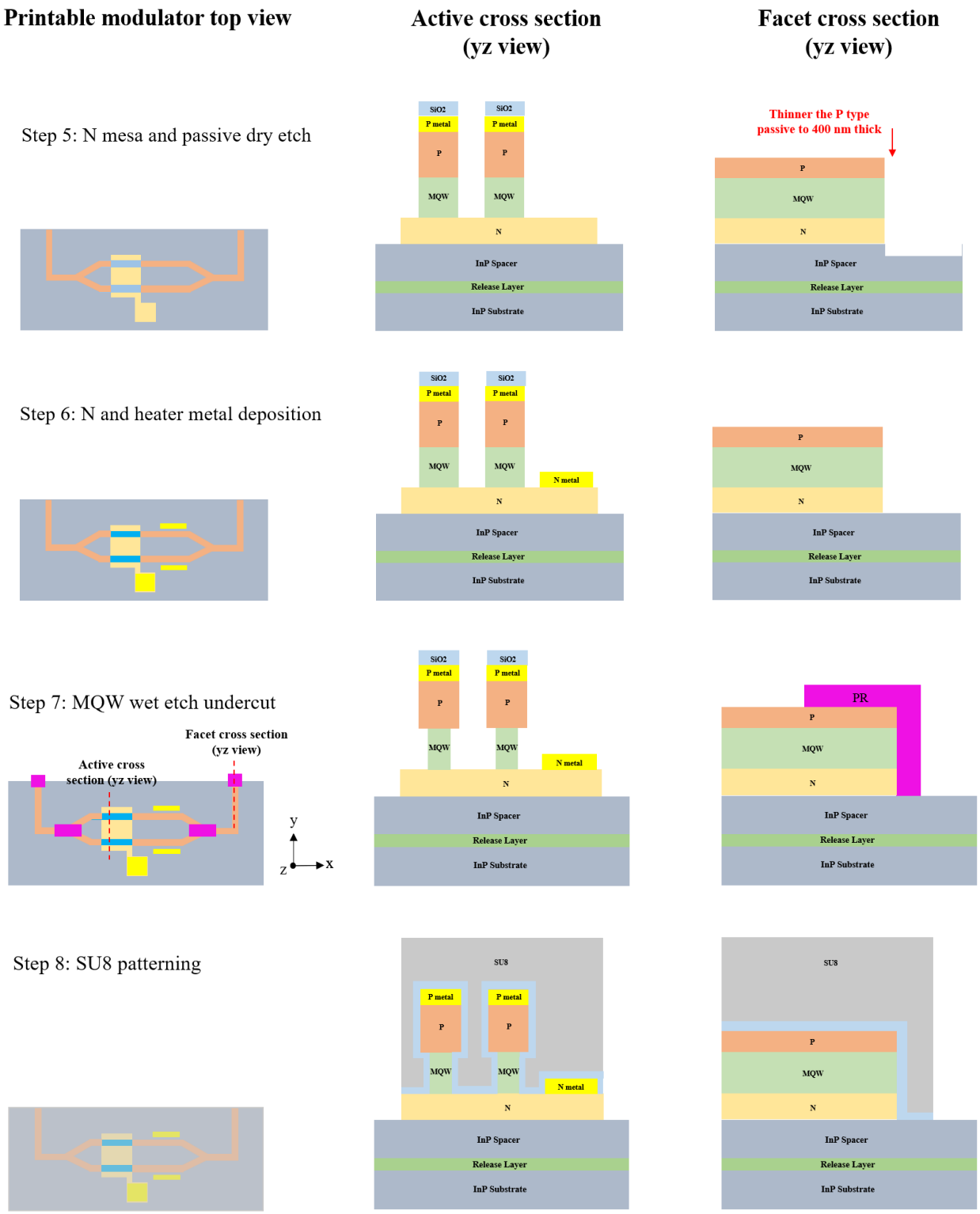


Figure 5.5 Step 5 - step 8: Modulator fabrication process flow showing the printable modulator top view, active, and facet section.

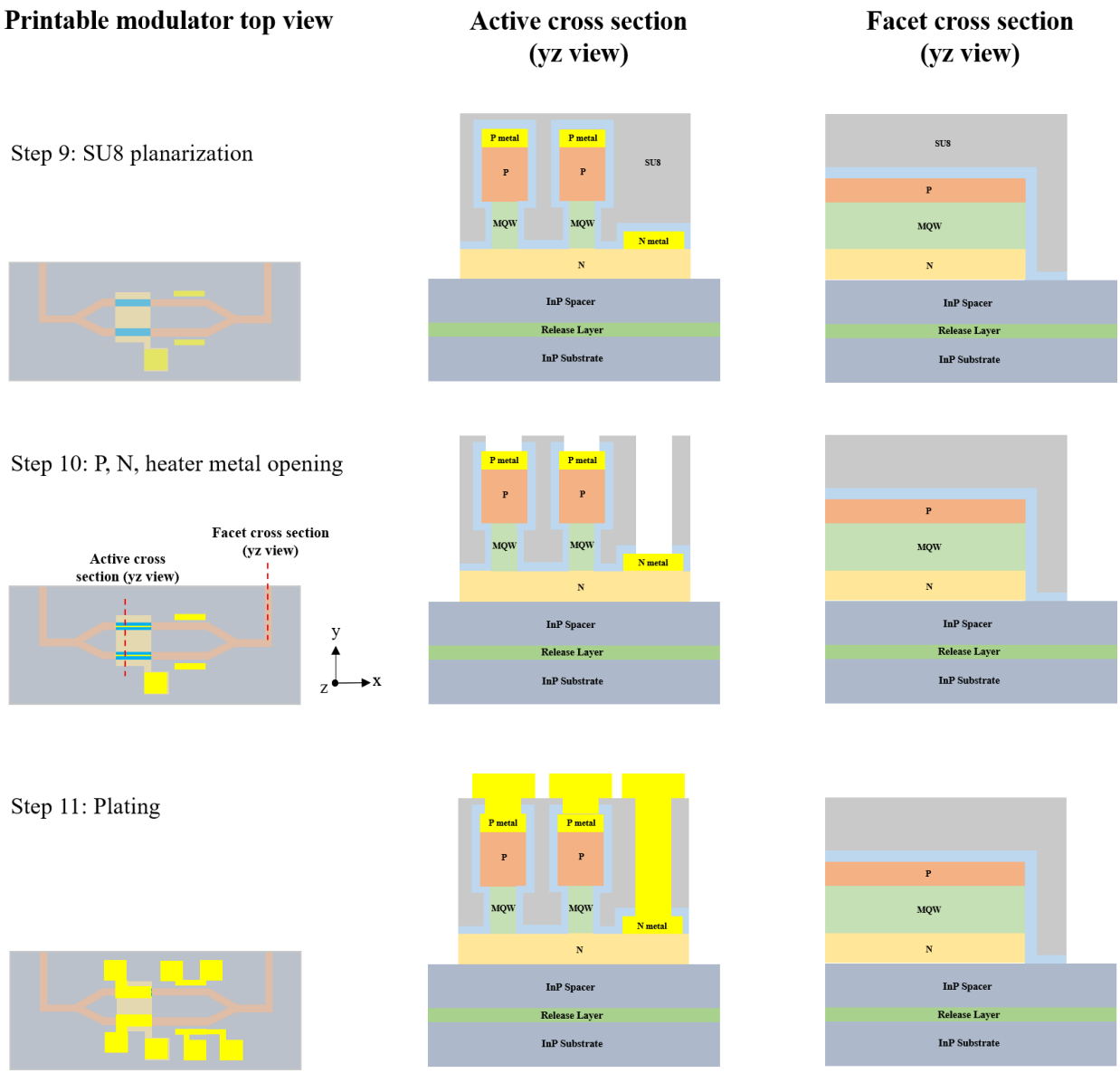


Figure 5.5 Step 9 - step 11: Modulator fabrication process flow showing the printable modulator top view, active, and facet section.

After the bar level modulator part of the die has been cleaved, more steps are needed for preparing the lower part of the die for transfer printing (the part of the layout below red dash line in the figure 5.4) which is shown in Fig. 5.6 step 12 to step 17. Firstly, a dry etch step is done to etch the InP spacer layer down to the release layer (step 12). Secondly, in step 13, H_3PO_4:H_2O_2:H_2O (1:1:10) solution is used to etch the release layer through to the InP substrate. Finally, a photoresist (PR) tether layer is coated on top of all the modulator chiplets in step 14. The die with the modulator chiplets on it is then sent to our collaborator X-Celeprint for transfer-printing. Fig 5.6 from step 15 to step 17 shows the steps that are done by X-Celeprint. First, the releasing chiplets step-15 is executed to make sure chiplets are completely disconnected from the InP substrate. Secondly in step 16, a stamp picks up the chiplet by breaking the tether bond to the InP substrate. Finally, the chiplet is transferred into a pocket on the target substrate in step 17, sent back to UVA, and after the tether removal, the printed modulator is ready to be used and tested. Fig. 5.6 step-17 shows the top and side view of how the modulator is placed on the target pocket on the target wafer, and to be noted that there will be a 150 nm adhesive layer (Intervia 8023) to be used to fix the modulator chiplet on the target wafer to prevent it falling off or moving away after aligned. Figure 5.7 shows top views of the real fabricated modulators before printing (Fig 5.7 (a)) and after printing (Fig 5.7 (b)) into the pockets integrating with SiN waveguide on the Si substrate.

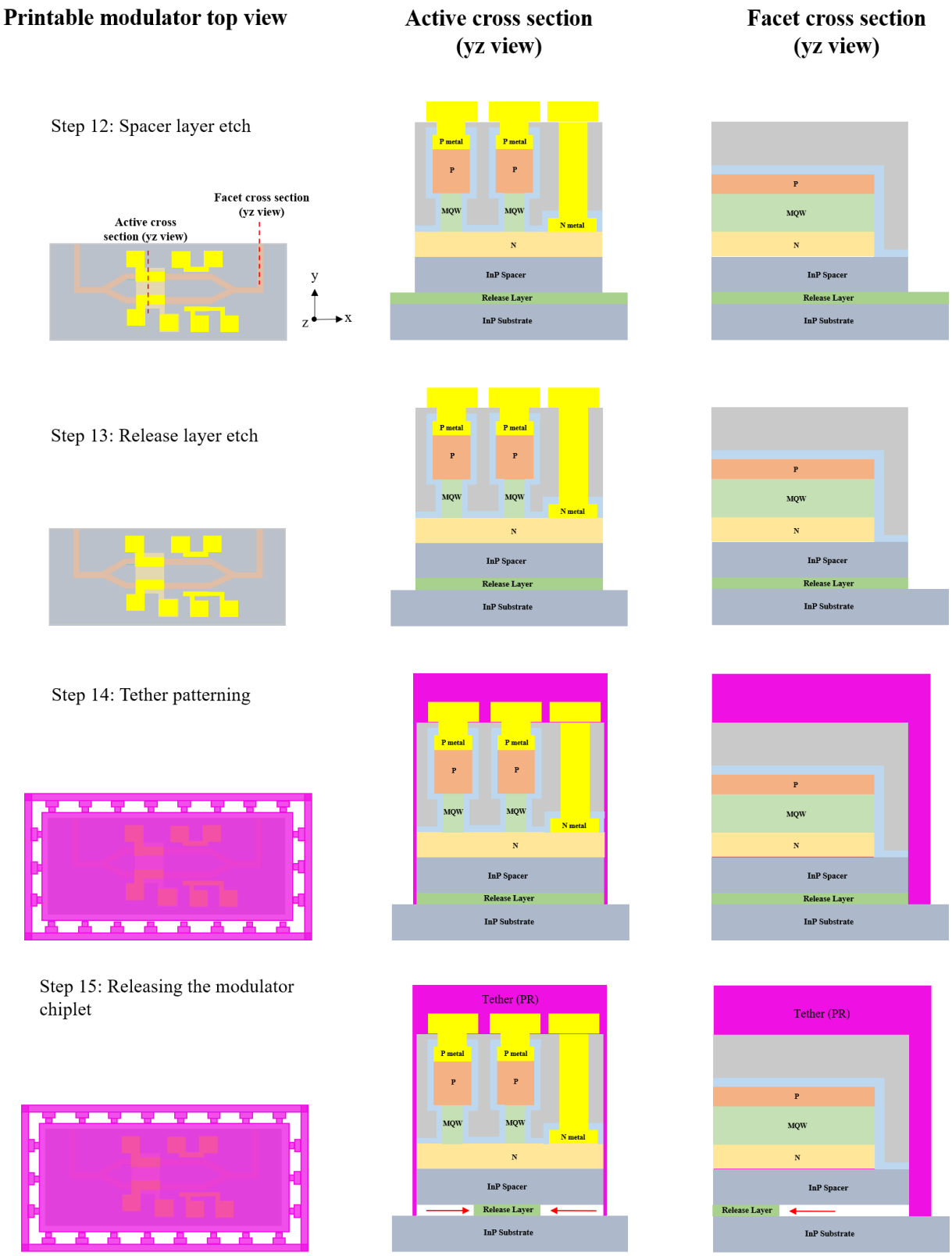


Figure 5.6 Step 12 - step 15: Modulator fabrication process flow showing the printable modulator top view, active, and facet section.

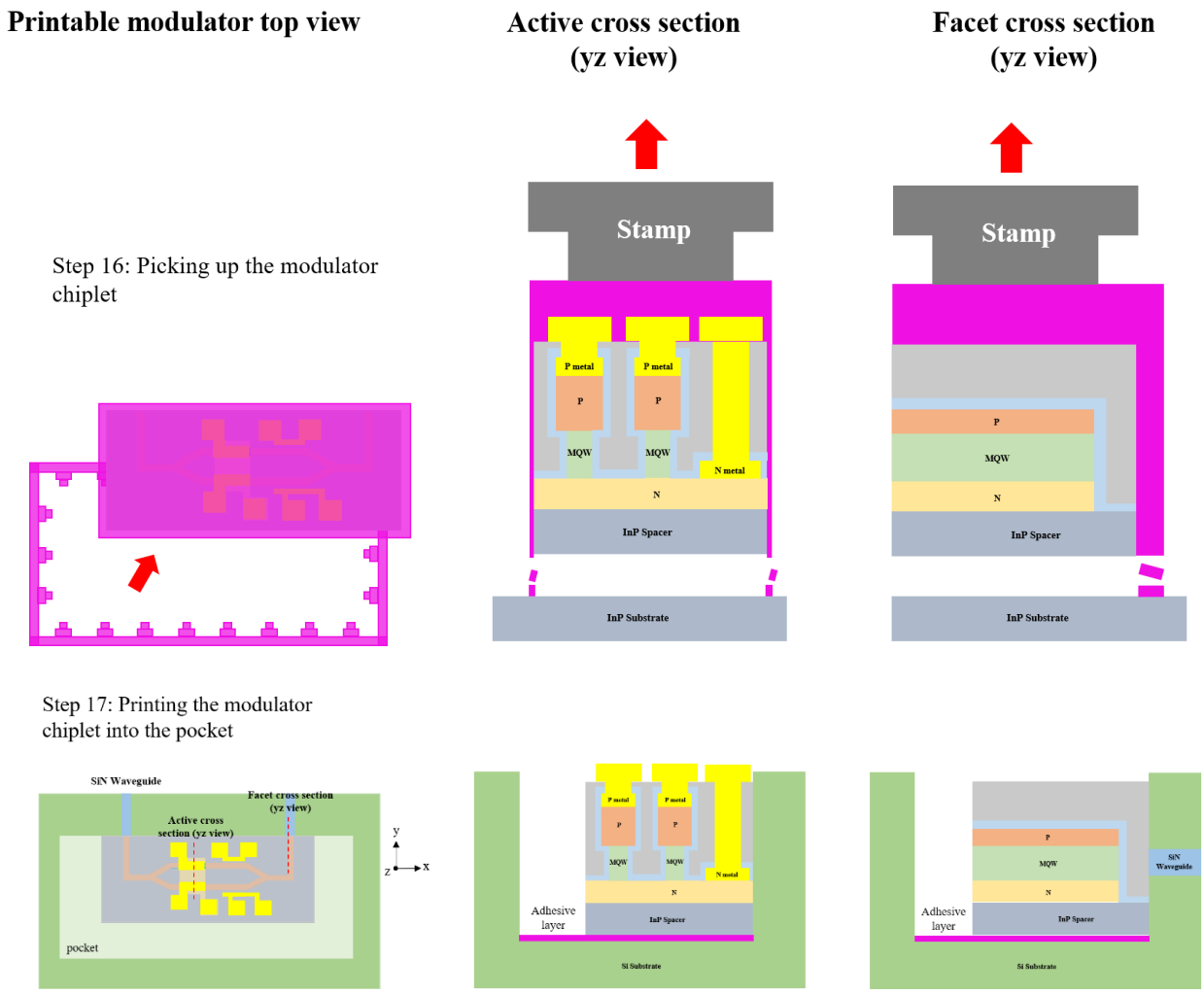


Figure 5.6 Step 16 - step 17: Modulator fabrication process flow showing the printable modulator top view, active, and facet section.

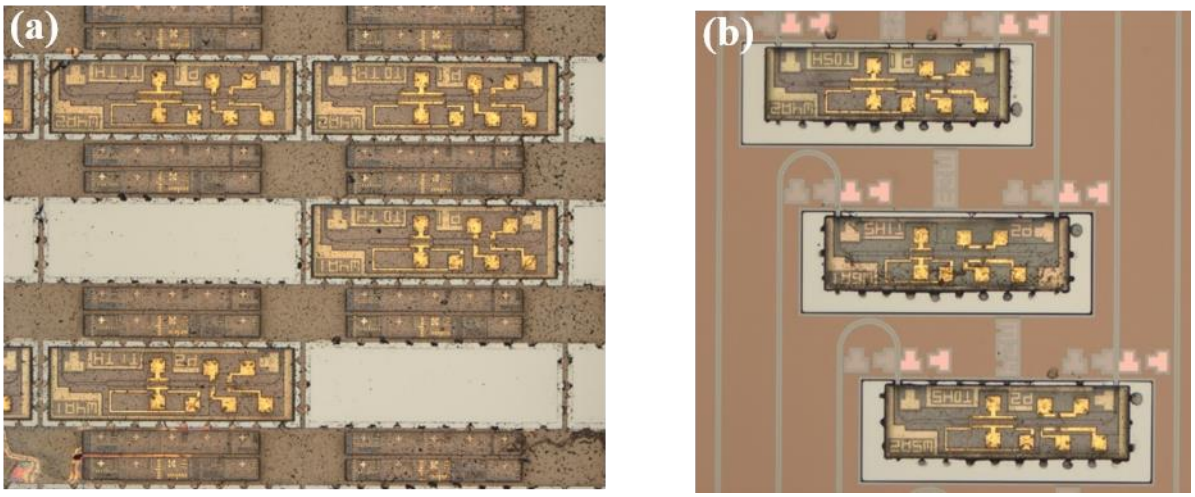


Fig. 5.7 Printable modulators (a) before printing and (b) after printing.

5.4 - Modulator Passive Component Design

This section discusses the multi-mode interference (MMI) splitter/combiner design. The Fig. 5.8 shows a cross-sectional view of the waveguide dimension. The passive waveguide width is designed for supporting single mode transmission through the modulator. On the left is the waveguide in the active section, and on the right is the passive waveguide section after waveguide undercut step. The MQW waveguide width is designed to be 1.2 μm in order to support only the fundamental mode, while also further reducing the junction capacitance to improve the RC bandwidth.

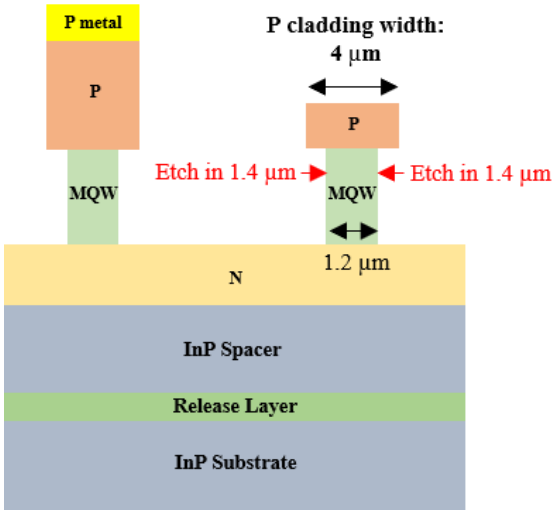


Fig. 5.8 simplified modulator cross sections of active and passive sections.

The MMI splitter is a critical component in the MZM modulator design which is required to exhibit a low insertion loss and 50/50 splitting ratio. However, typically, an MMI has a very low fabrication tolerance with regard to its width because this directly affects the interference pattern inside the structure. By just dry etching to form the passive waveguide and MMI portion, followed by MQW undercut etch next is not an ideal option (Fig. 5.9). The major factor to be considered is the waveguide undercut depth variation. There are two crystal orientations in the MMI structure that are exposed to the etchant, and the wet etch rates on these two directions are different. Hence, this makes the MQW width very easy to deviate from its original design. Fig. 5.9 and 5.10 show

that under the original MMI design, and with only a 100 nm waveguide undercut variation, the device suffers 2 dB more excess loss. Therefore, in this section, I developed a new waveguide undercut insensitive MMI design that is, as shown in Fig. 5.11, protected by photoresist before undercut wet etching. Now, only input and both output arms will experience waveguide undercut etch. Based on the simulation result shown in Fig. 5.12, now even with a 200 nm waveguide variation during etching, we will only get < 0.5 dB excess loss.

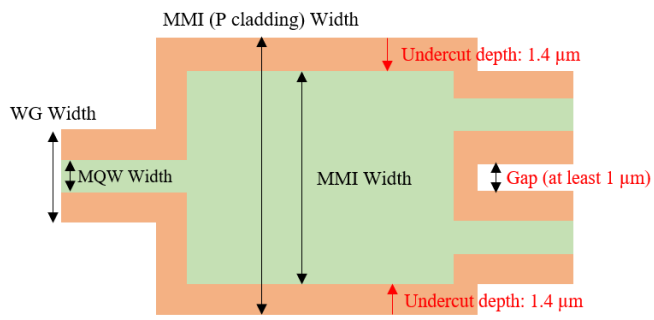


Fig. 5.9 Initial thought for Modulator MMI design.

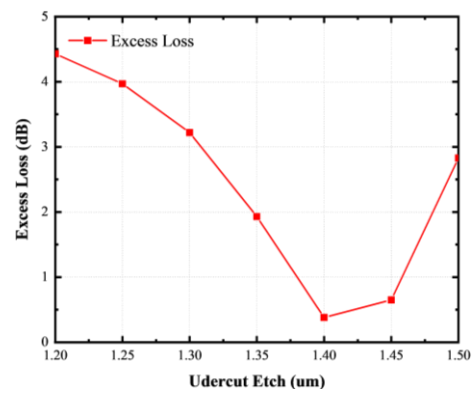


Fig. 5.10. Excess loss for different undercut etch depth to the MMI.

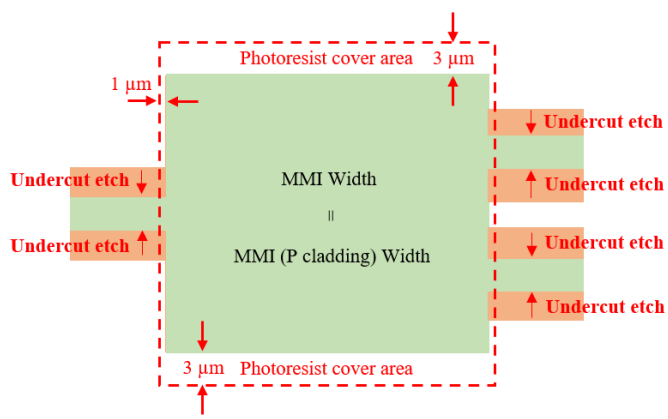


Fig. 5.11 Proposed Modulator MMI design.

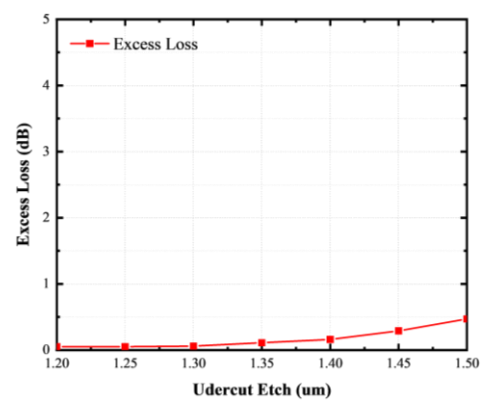


Fig. 5.12 Different undercut etch depth to the new MMI.

5.5 - InP-based Modulator Characterization and Analysis (Bar level modulator)

This section presents the measurement results and analysis for the InP-based bar level modulator starting with the epi characteristics, modulator passive structure testing, key figures of merit from the static and RF characterization to understand the performance of this MWQ MZM modulator before transfer printing. These intend to help providing good benchmarks for testing transfer printed modulators.

5.5.1 Active Section - Absorption Spectrum

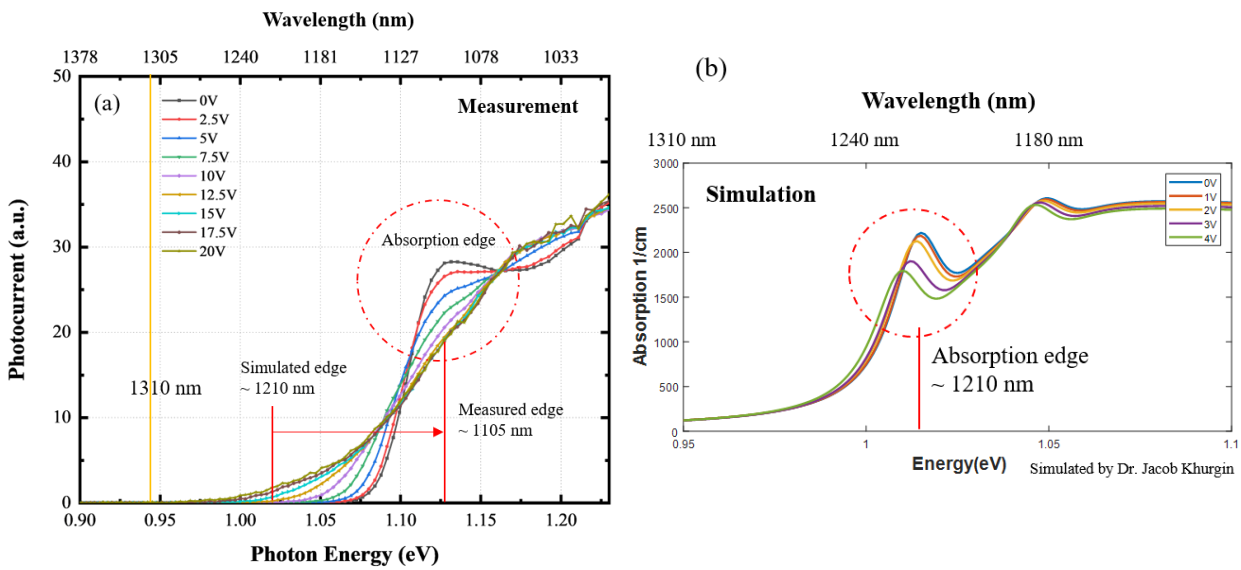


Fig. 5.13 (a) measured absorption curve based on the simple mesa PD (b) simulated absorption curve based on the epi (simulated by Dr. Jacob Khurgin).

As mentioned previously, the epi design for this MQW MZM is designed to operate at 1310 nm (O-band). Therefore, by using the QCSE effect to manipulate the absorption to further changing the phase on the two modulator arms, it does not require change in absorption based on the Kramers Kronig relation [67]. In other words, the modulation mechanism is taking the advantage of the absorption tail with a minor change instead of the absorption edge with a drastic change in the absorption spectrum under different biases which can be seen from the simulation curve in Fig. 5.13 (b). Based on the simulation, we expect the absorption edge located at 1210 nm so that at 1310 nm there will be only a minor change in the absorption. However, compared with the measurement results from the surface normal simple mesa photodetector that was fabricated based on this epi which is shown in Fig. 5.13 (a), we have found that the absorption edge has ~100 nm blue shift which leads to a minor change on the absorption curve at 1310 nm. Qualitatively

speaking, the absorption edge is further away from the operating wavelength which means that any change in the real part of the refractive index can be expected to be smaller. This implies that for the fabricated modulator, it will need a larger bias (i.e. 10-30 V in this case) in order to reach the V_π. A future redesign of the MQW epi is required to shift the absorption edge closer to the design goal.

5.5.2 Passive Section - Test structure for passive loss investigation

To investigate the passive component loss from the modulator, several individual components were fabricated as the test structures for further analysis. The upper part of the Fig. 5.14 shows the test structure with ~ 2.8 mm long straight waveguide (waveguide width: 4 µm) included with a S bend that has a 50 µm bending radius. Based on the measurement results shown in Fig. 5.15, we have concluded that the III-V waveguide loss is ~ 1 dB/mm. This estimation is based on the simulated 5-dB III-V-waveguide-to-fiber coupling loss and 0.3 dB S bend bending loss. These results indicate that the III-V passive waveguide loss is not the major contribution to the modulator high insertion loss (presented in the later sections) since our transfer-printable modulator designs have only 100 µm, 200 µm, and finally up to 400 µm long active section. Next, for the lower part of the Fig. 5.14, this shows another test structure that has a 1-to-2 MMI (splitter/combiner) design based on the 4 µm width waveguide dimension. For the two arms on the left side, each of the arm is connected with a S bend of 15 µm bending radius which has ~ 3.5 dB bending loss per S bend according to the simulation. Based on this estimation and the measurement results shown in Fig. 5.16, ~1 dB excess loss would be expected from this undercut insensitive MMI. However, due to this 3.5 dB bending loss from each S bend, each modulator is anticipated to have rather high insertion loss (at least 8 dB) since each modulator is equipped with 4 small S bends from the two MMIs.

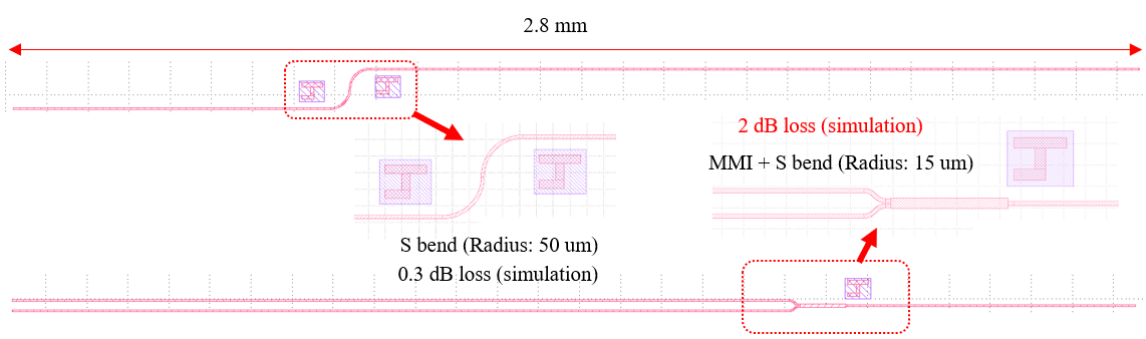


Fig. 5.14 Passive test structures.

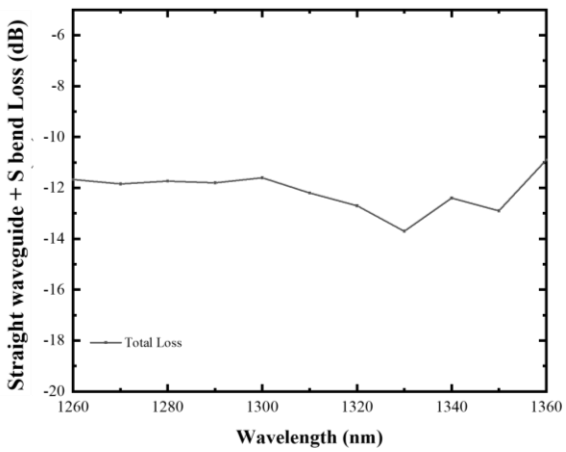


Fig. 5.15 Passive waveguide loss measurement.

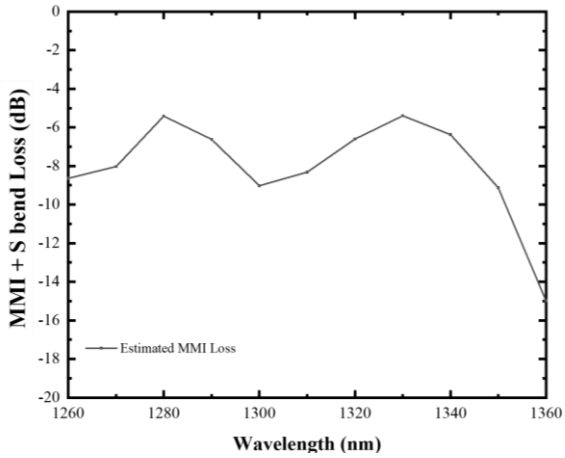
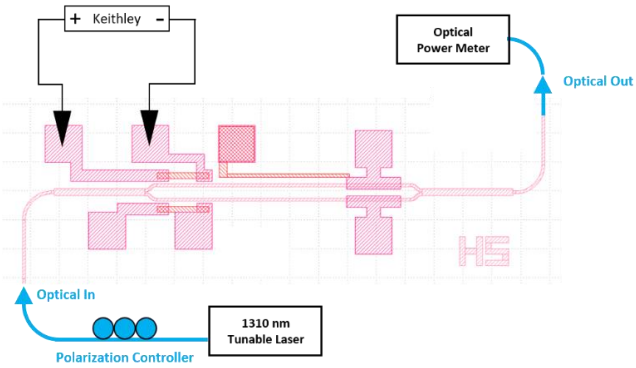


Fig. 5.16 MMI + S bend loss measurement.

5.5.3 Static Characterization - Heater and MMI-MZI



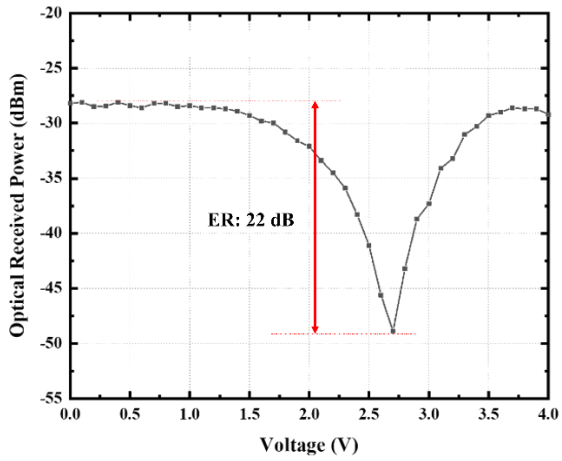


Fig. 5.17 Measurement setup for testing ER ratio of the MMI-MZI. Fig. 5.18 Measured ER of the MMI-MZI

The first static characterization of the modulator is to measure its modulation depth by applying a voltage to the heater section. The measurement setup for the extinction ratio (ER) of the MMI-MZI is shown in the Fig. 5.17. Two lensed fibers with 2.4 μm spot size diameter are used on both optical input and optical output waveguide cleaved facets. A polarization controller is utilized to optimize the polarization state before sending the optical signal through the fiber. An optical power meter is connected with the output lensed fiber for measuring the insertion loss of the MMI-MZI as a function of the heater voltage. The purpose of the heaters is to provide additional phase shift in when both MZM arms are not fully symmetrical after fabrication. Figure 5.18 shows that an ER of 22 dB was measured which indicates a good balance of two arms with splitting ratio close to

50/50 and that the losses in each arm are similar. Table 5.2 also shows the comparison of the ER from various MMI-MZI designs reported using different fabrication tools and platforms. This again shows that this undercut insensitive MMI design with its designed process flow is robust enough to be compatible with the UVA cleanroom tool, and meanwhile offers competitive performance compared to other works.

Table 5.2 Comparison of the performance of the MMI-MZI from other works.

MMI-MZI	Extinction Ratio (dB)	Material	Wavelength (nm)	Fab Tool (Resolution)
[68]	32	SOI	1550	DUV-193
[69]	24	SOI	1550	DUV-248
[70]	> 20	SOI	1550	E-beam Lithography
[71]	25	SiN	1550	ASML Stepper (500 nm)
[72]	30	SOI	1550	E-beam Lithography
[73]	18	InP	1550	N/A
This work	22	InP	1310	SUSS MA6 (1 μm)

5.5.4 Static Characterization - $V_\pi \cdot L$, Extinction ratio, and Insertion loss

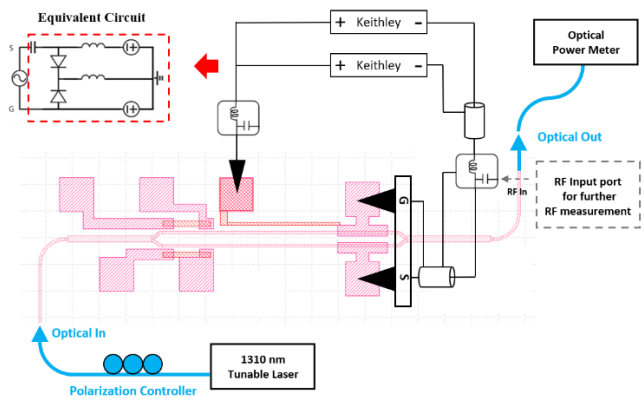


Fig. 5.19 Setup for modulator static characterization.

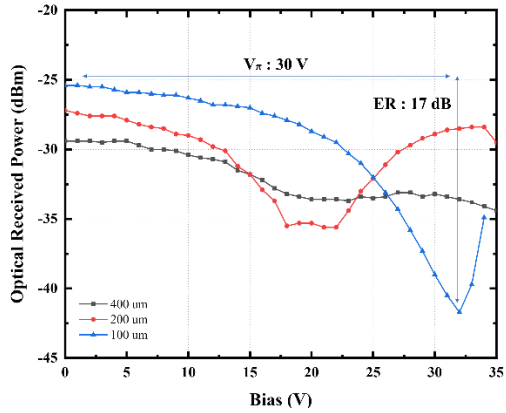


Fig. 5.20 Modulator V_π measurement.

Next, I used the experimental step shown in Fig. 5.19 to measure the V_π and the optical insertion loss. Now, two Keithley source meters are used so that photocurrents in both arms can be observed simultaneously when reverse bias is applied. For the electrical connection, to probe on the bias pad (N metal), two Keithley's anodes are connected together followed by an inductor (here, we use a bias-tee's inductor) to decouple the RF signal from the Keithley. On the RF pads side (P metal), a GS probe is used and followed by a bias-tee inductor part (the RF port (capacitor side) is left open for only static testing). The ground and signal of the inductor (DC) port from this bias-tee will split out into two individual dc paths that then are connected to the two Keithley cathodes, respectively. By setting the optical input power to 16 dBm, we measured the average insertion loss from bar level modulators with cleaved waveguide facets to be around 20 dB. This value is corrected for 5 dB coupling loss per facet. Next, the V_π is measured for modulators with different active section lengths L of 100 µm, 200 µm, and 400 µm. The results are shown in Fig. 5.20 which shows V_π of 30 V, 20 V, and 10 V respectively. For a modulator, usually $V_\pi \cdot L$ is the important figure of merit since this product is (ideally) constant for a particular design. We find the $V_\pi \cdot L$ to be 0.3 V·cm, 0.4 V·cm, and 0.6 V·cm for a 100 µm, 200 µm, 400 µm long modulator, respectively. Compared with recent results from published modulators, our $V_\pi \cdot L$ of 0.3 V·cm is rather low for this type of modulator which indicates good mode overlap with the active region [74]-[80]. The ER can also be determined from the V_π measurement. As mentioned previously, having a large extinction ratio usually indicates that the MMI is fabricated with high symmetry in both arms which is a good way to identify the MMI performance in a modulator. Fig 5.20 also shows the V_π measurements with

different modulator lengths, and a 17 dB extinction ratio is achieved on the 100 μm long modulator. Also from this measurement, we have verified the insertion loss to be 20 dB after excluding the fiber-to-waveguide coupling loss of 5 dB per facet. This shows that the modulator has relatively high insertion that is possibly due to the small bending radius S bends (radius: 5 μm) that add 3.5 dB loss per bend to the modulator. We have also observed that longer modulators have a smaller extinction ratio. This is potentially due to loss imbalance in the active arms that scale with length due to the waveguide formation and especially the MWQ wet etch undercut so that the phases from two arms are not matched perfectly at the combiner for the destructive and constructive interference. The table 5.3 shows a summary of the modulator static performance parameters. It should be noted that these measurements are based on modulators that are fabricated on the [110] crystal orientation. To investigate how the Pockels effect affects the V_π based on the crystal orientation, we have also fabricated modulators along [-110] direction, and measured their V_π. However, we found almost identical V_π as shown in Fig. 5.21 (a) and (b). A potential reason for this is that this epi has rather smaller absorption at 1310 nm because of the spectrum blue shift so that relatively high voltages of 10 V to 30 V are needed to achieve the desired phase change. This also indicates that the QCSE seems to dominate the V_π of our modulators.

Table 5.3 Static performances for modulators with different active lengths.

Active Length (μm)	**Vπ (V)**	**Vπ·L (V·cm)**	**Extinction Ration (dB)**
100	30 V	0.3	17
200	20 V	0.4	~ 10
400	15 V	0.6	~ 3

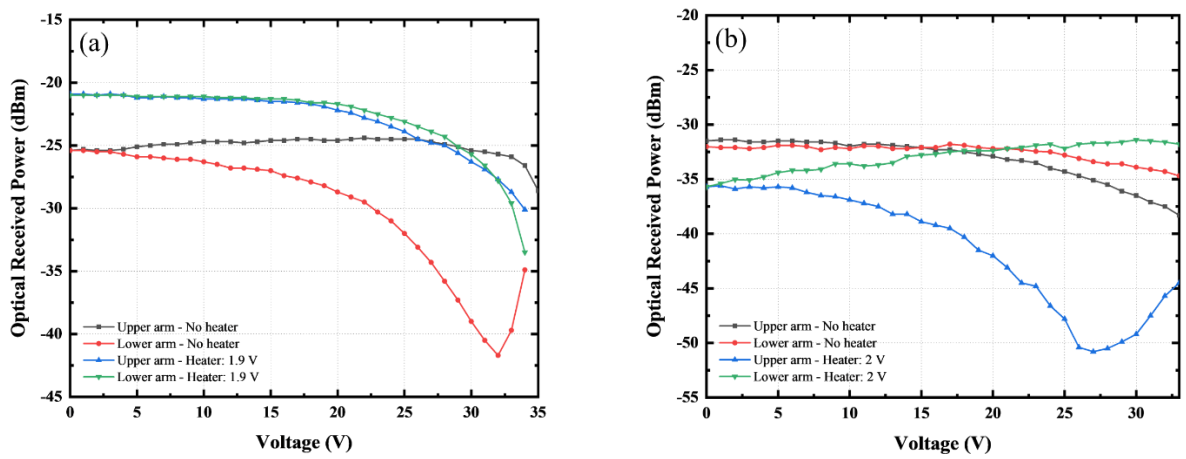


Fig. 5.21 Modulator V_π measurements of the 100 µm active length that are fabricated based on (a) [110] and (b) [-110] crystal orientations.

5.5.5 Small signal modulation

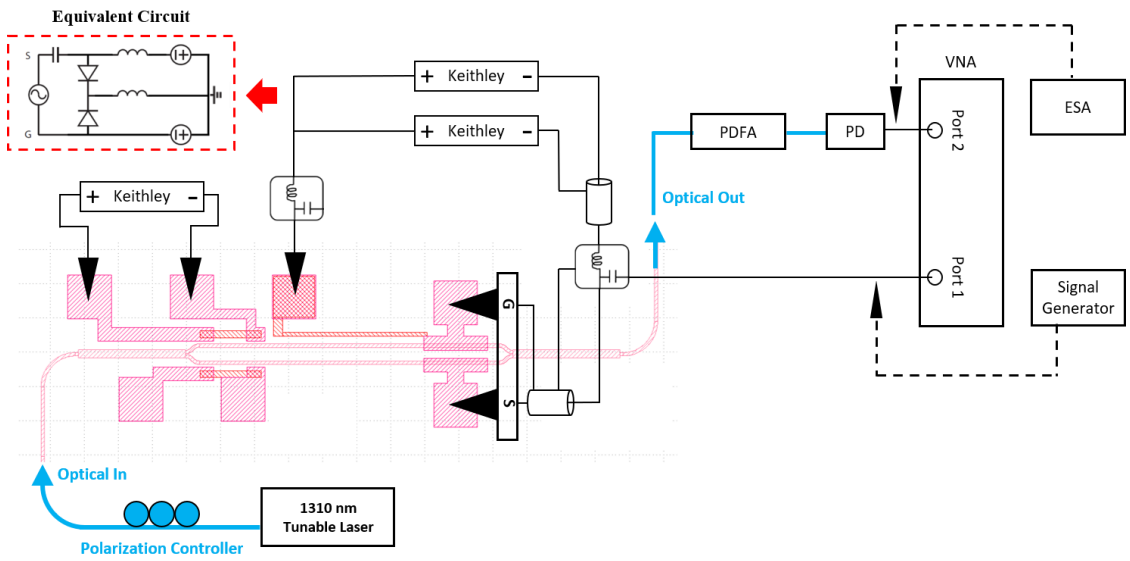


Fig. 5.22 Modulator bandwidth measurement setup.

The bandwidth measurement setup is shown in the Fig. 5.22. The biasing scheme is same as the one for static measurements. The difference is that an RF signal input to the bias-tee attached GS probe that is probed on the RF pads is added. I took two approaches for the bandwidth measurements and compared their results: The first approach is to use a vector network analyzer (VNA) and connect its port 1 signal to the modulator as the driving RF signal. Port two of the VNA is connected to a 50 GHz photodetector to do OE conversion of the modulated optical signal.

Then, the S21 is measured as the EOE bandwidth of the modulator. This method has the advantage that the RF portion in the experimental setup can be readily calibrated using the calibration routine in the VNA. The second approach is to use an RF signal generator on the driving side that feeds into the modulator. On the receiver side, the same 50 GHz photodetector is connected to an electrical spectrum analyzer (ESA). This method can provide a larger dynamic range due to the favorable noise performance of the ESA and the higher power that is available from the signal generator. Fig. 5.23 (a) shows the bandwidth measurements using the VNA approach. Our 100-µm long modulator reached a high bandwidth of > 67 GHz. And, as expected, larger modulators reached lower bandwidths of 50 GHz and 22 GHz for our 200 µm and 400 µm long modulators, respectively. Moreover, and as shown in the Fig. 5.23 (b), we found a good agreement between VNA and ESA measurements with a deviation of <±1 dB.

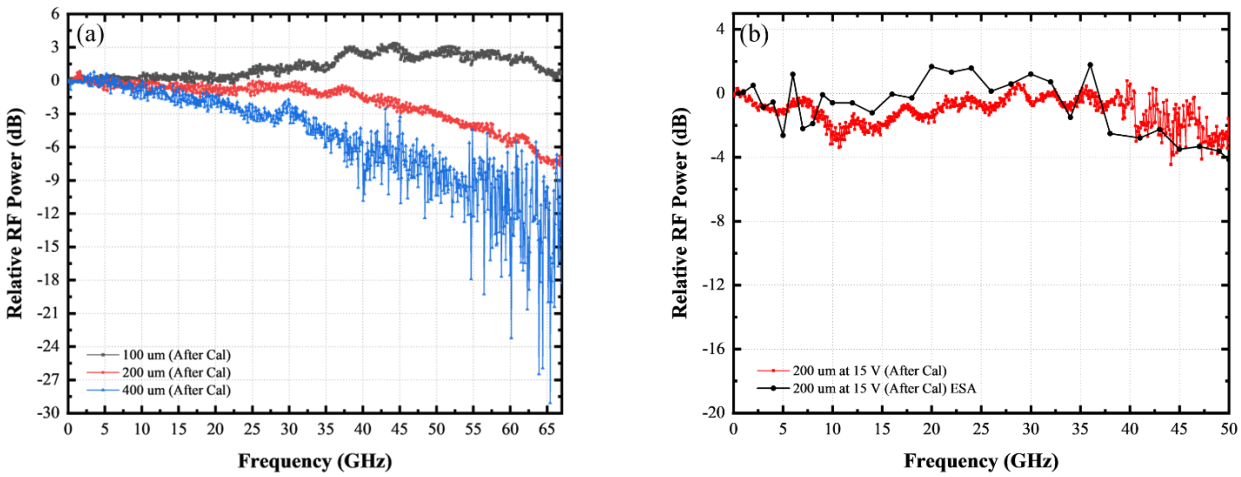


Fig. 5.23 (a) Measured modulator bandwidth with various active lengths based on the VNA approach and (b) bandwidth comparison between the VNA approach and the ESA + signal generator approach for a 200 µm long modulator.

5.5.6 S Parameter extraction

S parameters have been measured for the circuit analysis using the VNA. Figure 5.24 shows the simplified modulator equivalent circuit which includes junction capacitance C_j, series resistance R_s, metal line inductance L, RF pads stray capacitance C_{pad}, and the substrate resistance and capacitance R_{sub} and C_{sub} which are referred to the not intentionally doped (n.i.d.) InP spacer layer. Based on this circuit, I have simulated the S11 and adjusted the circuit parameters to fit the measured S11. In Figure 5.25 (a)-(f), S11 in magnitude and phase for different modulator lengths

are shown and a good agreement between circuit fitting and the measurement was obtained. The fitted circuit parameters are shown in the table 5.4. The simulated bandwidth from the fitted circuit shows a good agreement with the measured 200 µm and 400 µm ones. This indicates that the shortest 100 um long modulator has potential to achieve a bandwidth of 89 GHz. However, it should be mentioned that the extracted modulator junction capacitances (C_j) from the table 5.4 are still lower than what they were designed to be. This is possibly due to two reasons. First, the designed value of the C_j is based only on the junction depletion width which means that the additional stray capacitances from, for example, via metals does not include into the design. Secondly, the MQW wet etch undercut etched less than expected so that we end up having a wider junction width.

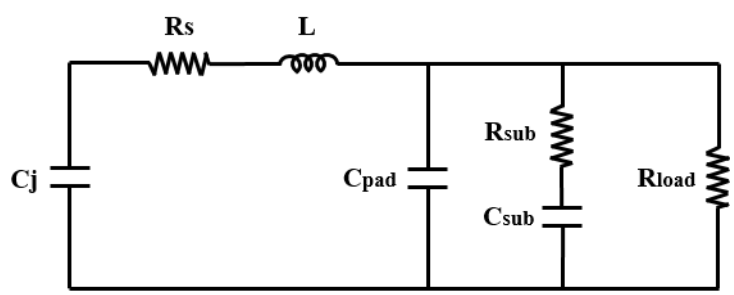


Fig. 5.24. Simplified modulator equivalent circuit.

Table 5.4 Circuit parameters based on the S11 fitting.

Parameter	100 µm	200 µm	400 µm
C_j	25 fF (Design: 10 fF)	58 fF (Design: 20 fF)	146 fF (Design: 40 fF)
R_s	1.2 Ohm	1.2 Ohm	2.2 Ohm
L	2 pH	8 pH	30 pH
C_{pad}	10 fF	10 fF	10 fF
R_{sub}	776 Ohm	664 Ohm	664 Ohm
C_{sub}	32.8 fF	49.2 fF	63.1 fF
Sim. BW	89 GHz	46 GHz	20 GHz
Meas. BW	> 67 GHz	~ 50 GHz	~ 25 GHz

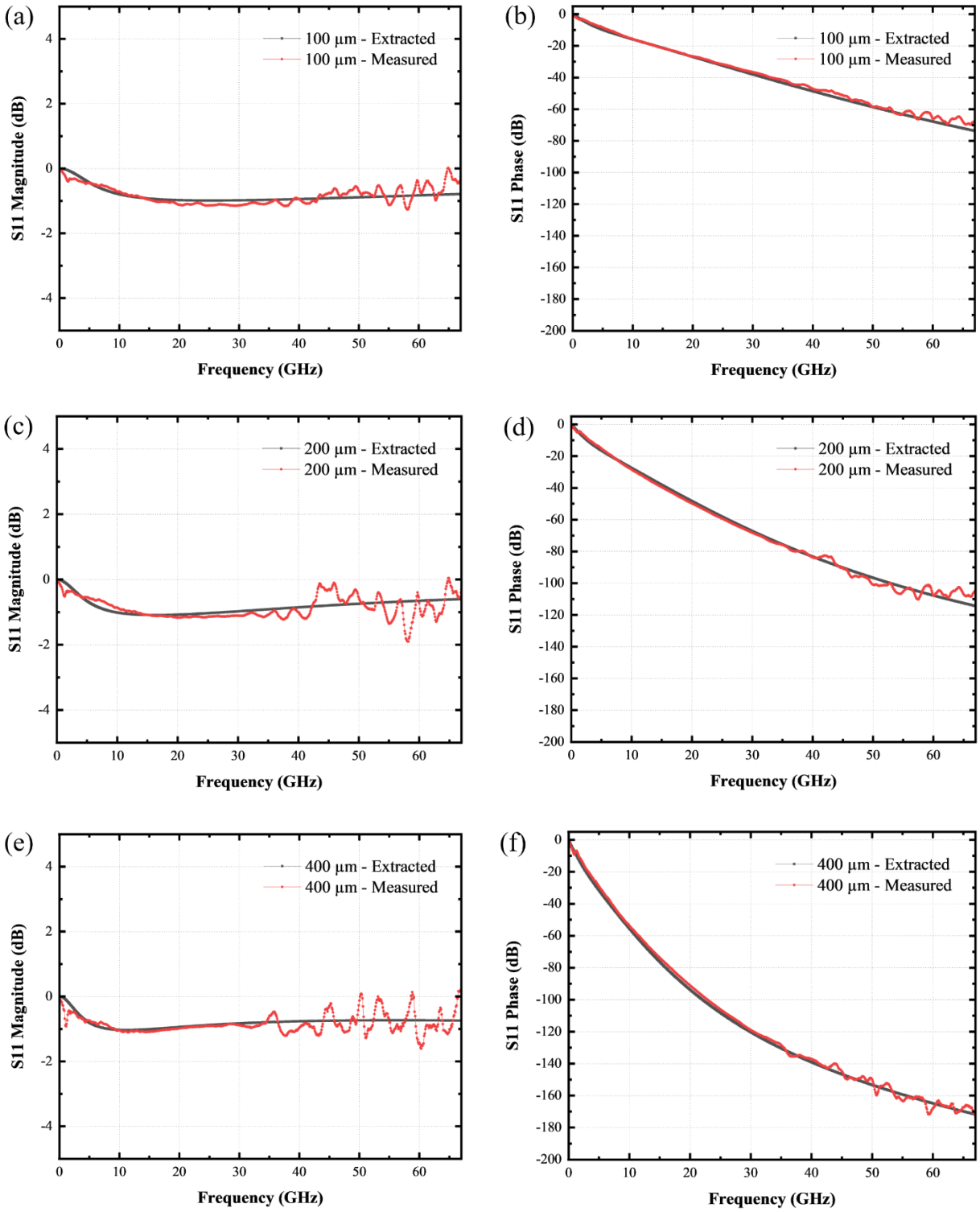


Fig. 5.25 Comparison of the S11 (magnitude and phase) between simulation and measurement for 100 µm ((a) and (b)), 200 µm ((c) and (d)), and 400 µm ((e) and (f)).

5.5.7 Large signal modulation

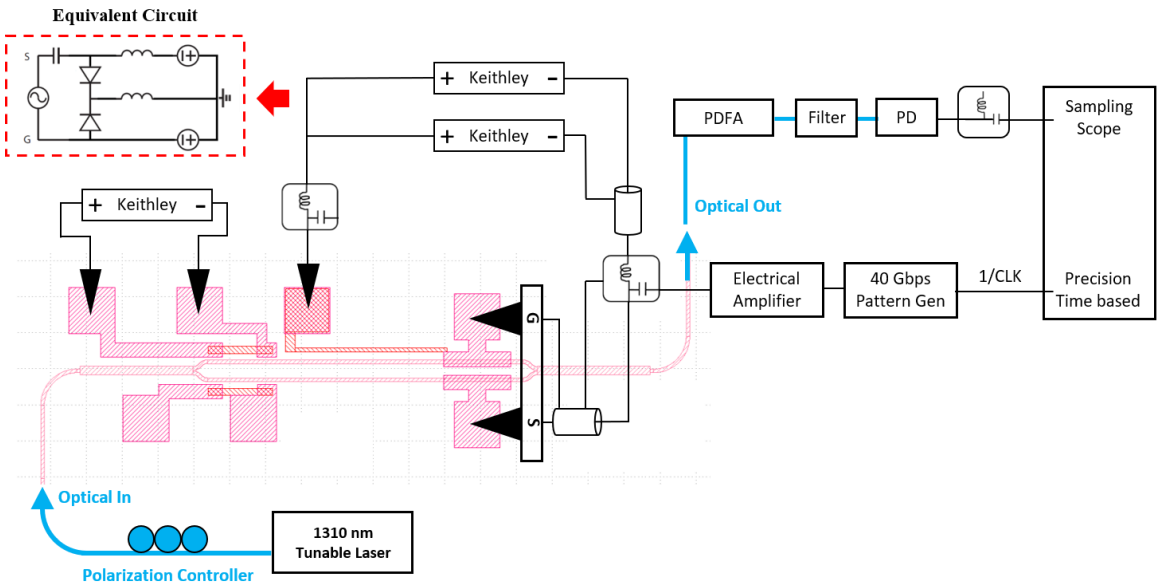


Fig. 5.26 Modulator eye diagram measurement setup.

The eye diagram measurement setup is shown in the Fig. 5.26. The RF input to the modulator comes from a 40 Gbps pattern generator that is followed by a high-speed (40 GHz) RF amplifier (~ 6 V peak-to-peak voltage). The optical input is fixed at 15 dBm from a 1310 nm tunable laser. On the modulator optical output side, the signal is fed into a praseodymium-doped fiber amplifier (PDFA) to amplify the signal up to the level that can provide ~ 2 mA photocurrent for the photodetector. A bias-tee is used after the photodetector as a DC block. Then after the OE conversion, the electrical signal is fed into the sampling scope to observe the eye performance. In Fig. 5.27 (a), the 40 Gbps electrical eye with pseudorandom binary sequence (PRBS) with a pattern length of 2^{15}-1 bits (PRBS 15) is shown with a 5 dB extinction ratio and 6 dB signal-to-noise (SNR). Due to the fact that the optical signal will experience significant insertion loss inside the modulator, the weak output signal amplified by PDFA will end up with very low signal-to-noise ratio. The other detrimental factor is that there is considerable impedance mismatch between the 50 Ω system and the modulator, and this can cause significant RF reflection from the modulator back to the probe. In other words, the exact voltage swing applied to the modulator is a lot smaller than expected. Therefore, it can be seen that the optical eye in Fig 5.27 (b) is noisy which is most likely dominated by amplified spontaneous emission noise (ASE) from the PDFA itself. It should be noted that a 0.6 nm FWHM optical filter has already been used to reduce the ASE. To improve

the noisy eye, I added another GS probe connected with a 50 Ω termination to the RF pad to lower the input impedance of the modulator. Fig. 5.26 (c) shows the improved 40 Gbps clear eye diagram measured with the 50 Ω termination resistor.

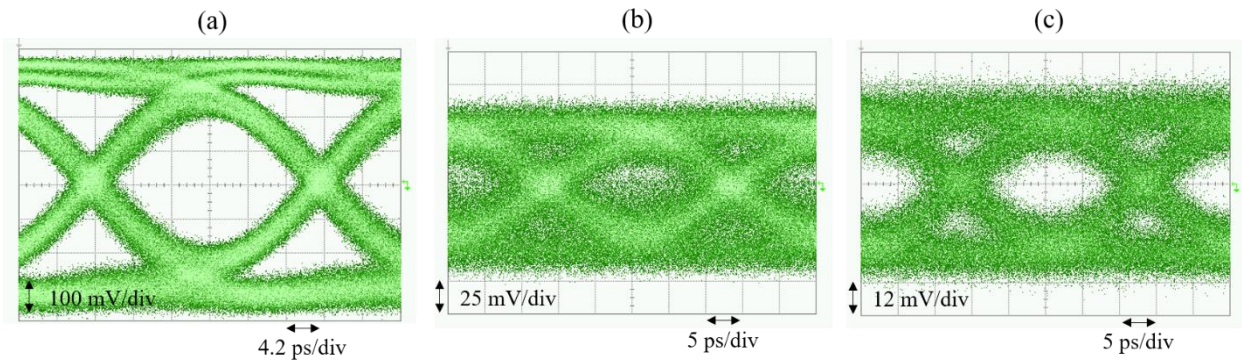


Fig. 5.27 The 40 Gbit (a) electrical eye, (b) optical eye without a 50 Ω and (c) optical eye terminated with a 50 Ω.

5.5.8 Performance Summary

The performance summary is shown in the table 5.4. Our bar level O-band MQW MZM has very high bandwidth and low V_{π}·L due to the unique thick MQW design that provides low capacitance and high mode overlap with the MQW. This is the first > 67 GHz InP-based O-band MQW MZM with 0.3 V_{π}·L and 17 dB ER. Because of its small footprint, this modulator is fully compatible with micro-transfer printing technology during the transfer step.

Table 5.5 Modulators performance summary.

Push-pull MZM	3-dB Bandwidth (GHz)	Vπ·L (V·cm)	Extinction Ratio (dB)	Insertion loss (dB)	Material	Wavelength (nm)
[74] Traveling-wave	20	0.66	19	N/A	InP	1550
[75] Traveling-wave	35	1.75	18	9	InP	1550
[76] Traveling-wave	80	0.6	25	8.5	InP	1550
[77] Traveling-wave	9	0.96	9	16	InP	2000
[78] Traveling-wave	18	0.24	18.4	~10	InP on Si	1550
[This work] Lumped	> 50	~ 0.3	17	20	InP	1310

5.6 - Printed modulator summary and potential future work

To date a few modulators have been printed onto the target substrate as shown in Fig. 5.7. Since the optical waveguides of the modulator and the target substrate are butt-coupled, the loss is highly depending on the dry etched III-V facets from the modulator and also the alignment accuracy of the printing technique. At this moment we are seeing more than 80 dB insertion loss from printed modulators so that no other measurements can be done due to such a high loss. We have concluded the major reason is because that the facet protection was etched away during the spacer dry etching step that is explained in the figure 5.28. In the process flow, firstly, the SU8 layer covered on top of the four edges of the modulator chiplet should be flat and has ~ 3 µm thick on top of it which is shown in figure 5.28 (a). In reality, we have found out that the SU8 layer that covered around the chiplet edges is thinner than expected. This is the first reason to cause the facet protection got weakened. Secondly, during the spacer dry etch step, a photoresist AZ4330 with 7 µm thick is spin-coated as the dry etch mask on top of the modulator chiplet. So in theory (Fig. 5.28 (b)), a vertical dry etch is expected during the spacer etch step because the chiplet region has already been protected by the photoresist. However, in reality (figure 5.28 (e)), we have found that during the dry etch step the photoresist shrinks because of the elevated temperature. This leads to the SU8 and protection layer exposure during the spacer etch and then these two layers will subsequently get thinner. So that during the release layer etch step or the releasing step from X-Celeprint side, the etch solution will not only etch away the release layer but also infiltrates through the small holes or gaps that are created during the spacer etch and to start etching away the MQW layer near the facet (figure 5.28 (f)) which can completely degrade the coupling mechanism.

Figure 5.29 shows the printed modulator with closer facet top views with different zoom-in magnitude. Based on this printed modulator, a SEM picture was taken and shown in the figure 5.30. It can be seen from the picture that the printed modulator has went through the release layer etch step and also the printing step, and because the SU8 and the protection layers are all removed during the etch near the facet so that the MQW layer was exposed and etched to create the gap. This means that there is not waveguide core near the facet anymore which leads to a significant degradation of the III-V-to-SiN waveguide coupling efficiency. To prevent this, the future work needs to focus on developing thick enough SiO_2 protection layer so that after the spacer dry etch step, the modulator facet will still be protected for moving to the releasing and printing step.

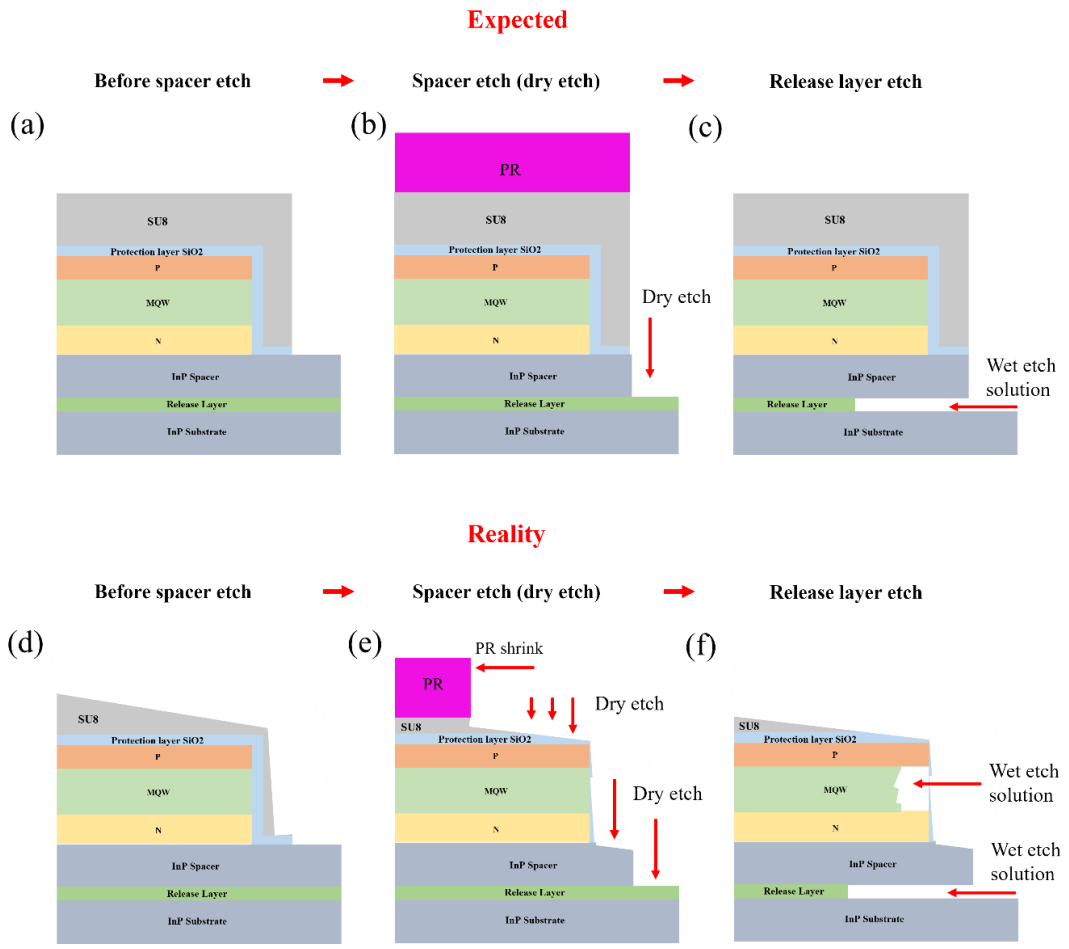


Fig. 5.28 Facet status during spacer etch and release layer etch that compares between expected (a)-(c) and in reality (d)-(e).

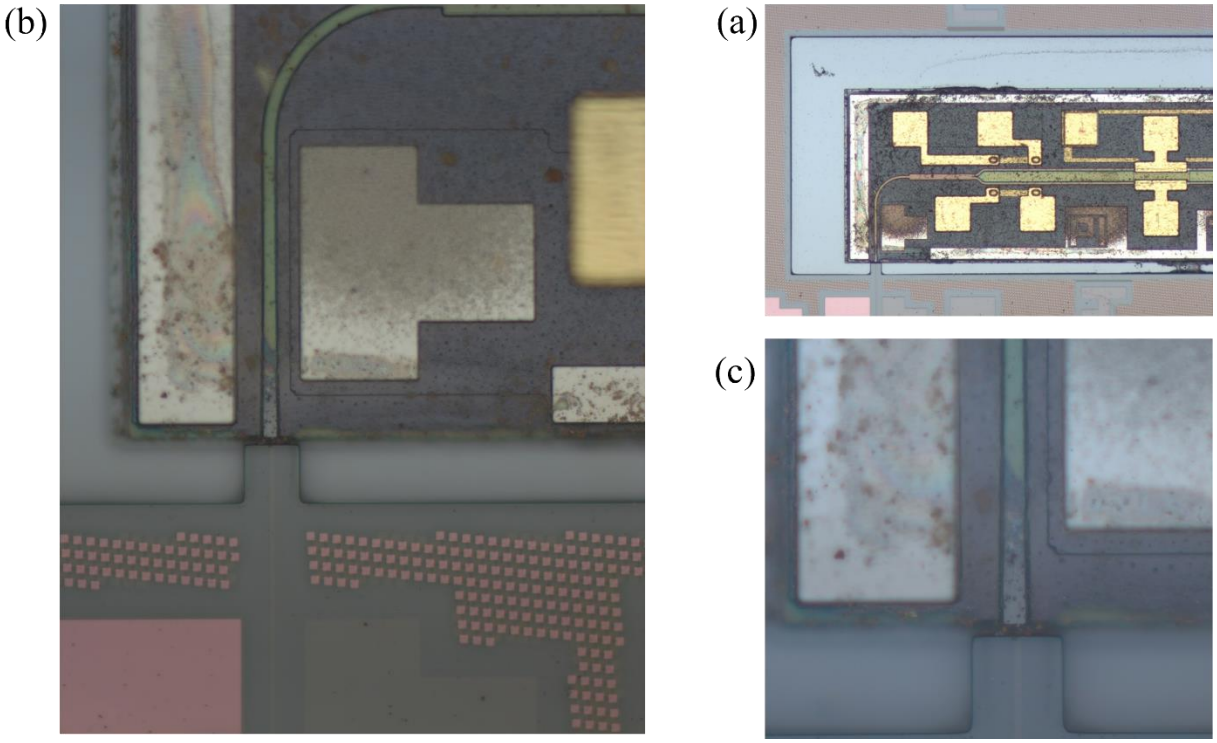


Fig. 5.29 Facet top views (a)-(c) of the printed modulator from different zoom-in magnitude.

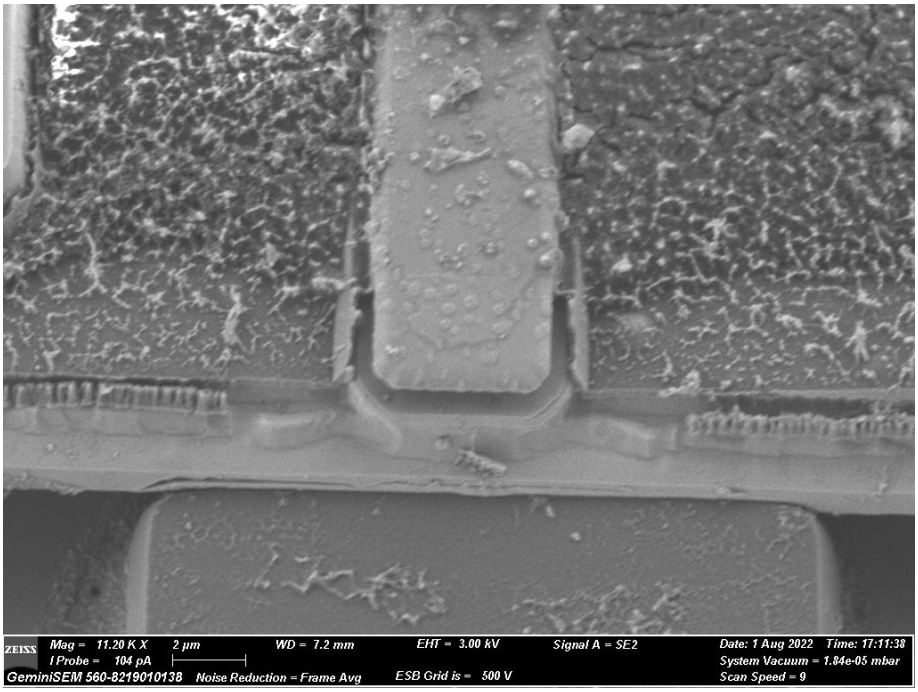


Fig. 5.30 SEM picture of the printed modulator facet view based on figure 5.29.

Chapter 6 - Conclusion and Future work

6.1 - Conclusion

In this dissertation, I have been focusing on developing both lumped and distributed arrayed photodetectors for achieving high RF output power and bandwidth for microwave photonic applications. These photodetectors are designed and fabricated based on silicon photonics foundry: AIM Photonics. The key is trying to exploit its PDK component capability, and to build up the photodetector designs fully depend on these components to avoid spending extra effort on designing any customized design. One of the advantages of designing photodetector based on this platform is that it offers the potential to be integrated with the electronic circuit on the same fab run. To this end, for the very first time, TWPD and TWBPD integrated with biasing circuit have been demonstrated with 32 GHz and 25 GHz bandwidth at 1 mA respectively. And for the TWPD with integrated bias circuit, 6 dBm output power has been achieved at 44 mA photocurrent without hitting 1-dB saturation. To the best of our knowledge, this design has the best bandwidth × saturation current product compares with other TWPD works. And compare to our previous work on the same platform which shows the lumped 8-PD array that has only 5 GHz bandwidth, distributed PD array shows its strength to push the high-power handling capability to the higher operational frequency. Additionally, for the very first time, a 32-PD loaded fully distributed group array photodetector combiner (GAPC) has been demonstrated to have 15 GHz bandwidth and with < 5 ps group delay difference comparing with the lumped type (< 10 ps) within 10 GHz. The GAPC is expected to be used as a massive RF power combiner for the RF photonic system which has the potential to carry 350 mA DC photocurrent based on the transmission line test structure. This leads to ability of operating all 32 loaded PDs around 10.5 mA of 1-dB saturation current at 5 GHz and combining all the RF power to the output. In the end, the balanced type of GAPC has been introduced with 13.5 GHz bandwidth with common mode rejection ration above 30 dB up to 10 GHz.

Another research focus of my PhD work is to explore heterogeneous integrated modulator and photodetector. Firstly, one of the popular heterogeneous integration techniques: micro-transfer printing technology is utilized to demonstrate transfer printable InP-based MQW MZM. In this work, I have demonstrated > 67 GHz bandwidth and 17 dB ER transfer printable InP-based MQW

MZM. 40 Gbps large signal modulation has also been reported. Due to the huge coupling loss measured from the modulators printed on the SiN platform, the fabrication process flow of the modulator facets has been fully investigated and discussed.

6.2 - Future work - III-V-on-Silicon heterogeneously integrated GAPC

6.2.1 Introduction

In contrast to the foundry-based Ge-PD, we shift the focus to the III-V-on-Si heterogeneously integrated PD in the future work. In this way, we can take the full control over the PD design for not only the active section width and length but also the junction thickness so that we can aim for a PD with ultra-low junction capacitance that makes it easier to design 50 Ω matched loaded transmission line for the distributed PD array. A low-capacitance PD can also help to design the distributed circuit that has a higher Bragg frequency. Therefore, this chapter aims at demonstrating the group array photodetector combiner (GAPC) architecture by using heterogenous PDs in the TWPD. Firstly, different epi designs based on the UTC-PD structure will be proposed along with an integrated silicon taper waveguide design and followed by the GAPC circuit simulation results. Secondly, the fabrication process flow will be described. Initial fabrication results and measurements will be discussed. Future work is summarized in the final section.

6.2.2 Evanescent-coupled waveguide UTC-PD based GAPC

Previously, our group has demonstrated various types of heterogeneous modified UTC PDs on SOI platform using low-temperature oxygen-plasma-assisted wafer bonding technique supported by UCSB/Aurrion [24], [44,45]. The PDs can generally be categorized into two types of design: P-down and P-up design which are shown in the Fig. 6.1 and Fig. 6.2. The P-down design means that the p contact layer is faced down to be bonded onto the silicon waveguide. The advantage of using P-down design is that the absorption layer of the UTC PD structure is closer to the silicon waveguide, therefore, a higher responsivity can be achieved. However, one disadvantage is that the maximum achievable p-type doping levels in the transparent InP layer are typically lower than in InGaAs, which will affect the PD series resistance and bandwidth. To this end, we have developed the P-up version of the heterogeneous UTC PD. In this design, much higher n-type doping levels can be achieved in the InP n contact layer, e.g. as high as 10^{19} 1/cm^3. However, a downside of this design is that the absorption layer is now far from the waveguide which is

illustrated in Fig. 6.2. The light from the silicon waveguide needs to couple through the whole drift layer to be absorbed, and this drift layer is usually hundreds of nm's thick. Therefore, and as shown in the Fig. 6.3 (a), I designed a narrow tapered waveguide to create a weakly confined mode beneath the active region from the originally highly confined mode in the silicon input waveguide so that the mode is expected to have a larger overlap with the high index absorption layer. Compare with the narrow type of taper section from the P-up design, the wider taper section along with P-down design offers more flexibility in the waveguide design to potentially achieve uniform illumination which is shown in Fig. 6.3 (b). In short, a trade-off would need to be considered between the responsivity and series resistance limited bandwidth by choosing between the P-up or P-down design.

(a) (b)

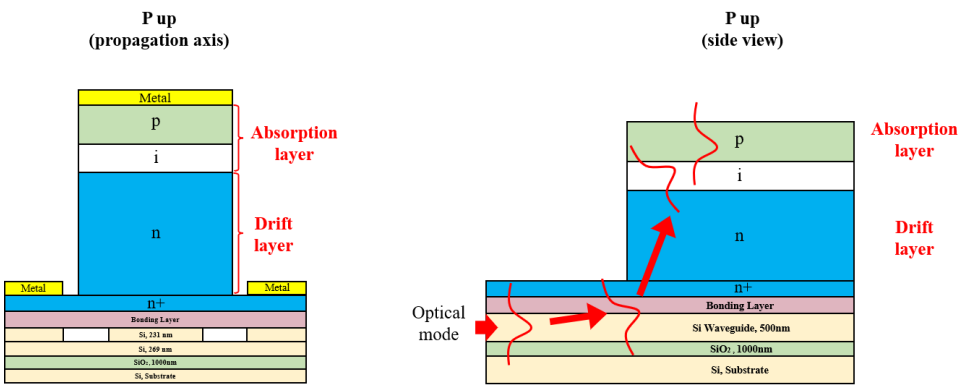


Figure 6.1. P-up design (a) in propagation axis and (b) side view.

(a) (b)

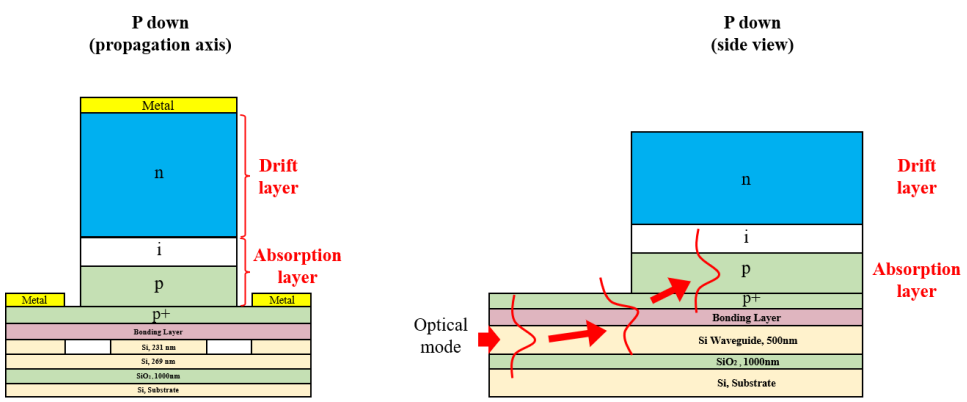


Figure 6.2. P-down design (a) in propagation axis and (b) side view.

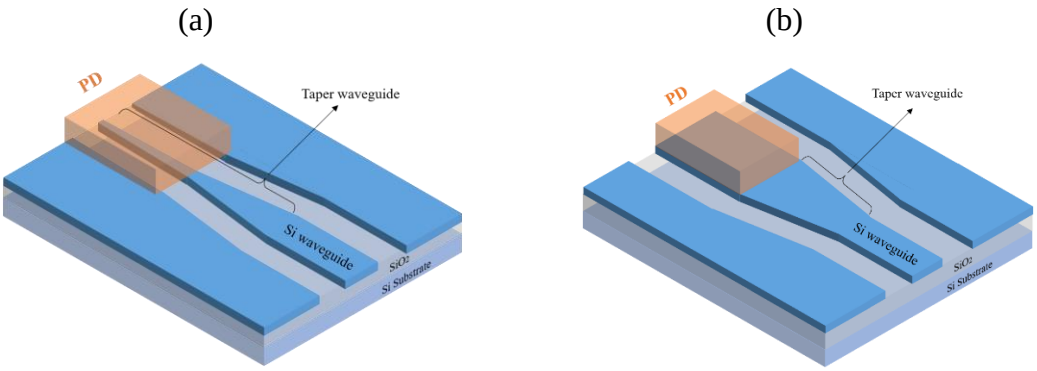


Figure 6.3. Schematic of tapered waveguide for (a) P-up design and (b) P-down design.

To be potentially compatible with the integrated heterogenous laser and modulator process [25]-[27], the P-up design is considered first. Next, to avoid having a long loaded transmission line which would result a lower cut-off frequency of the GAPC, the goal is trying to design the photodiode with low junction capacitance for loading into the GAPC circuit. To minimize the capacitive loading in the GAPC, it is beneficial to reduce the junction capacitance C_j. This can be achieved through a thicker depletion width, whereby the transit time limit represents the upper limit (see Eq. 2.2). With relatively low capacitive loading, the overall device length can be reduced (see Eq. 4.1) since shorter transmission line section between PD groups can be used. This can decrease potential transmission line loss that negatively impacts the bandwidth. To study the impact of PD capacitance on the GAPC performance, for the Epi 1 and Epi 2, I designed 2 μm (30 GHz transit time bandwidth) and 4 μm (15 GHz transit time bandwidth) depletion widths, respectively.

For the Epi 1, we chose Intelli Epi as the vender grower using Molecular-beam Epitaxy (MBE) technique and the InP/InGaAs/InAlGaAs material system. Starting from the InP substrate, a 100 nm thick InGaAs contact layer is grown on top of the substrate, followed by a 100 nm thick InP blocking layer. Next, 200 nm InGaAs (undepleted absorber) + 500 nm InGaAs (depleted absorber) are sandwiched between the InAlGaAs grading layers. A 1500 nm thick InP drift layer is grown which is followed by a 185 nm thick matching layer. Finally, 2 pairs of 15 nm thick InP/InAlGaAs super lattice layers with a 10 nm thick InP layer are used as the bonding layers and to prevent potential migration of defects. For the Epi 2, we chose Landmark as the epi grower using the Metal

Organic Chemical Vapor Phase Deposition (MOCVD) technique using the InP/InGaAs/InGaAsP material system. The structure is very similar to the Epi 1, but the difference is that now all the InAlGaAs layers are replaced by InGaAsP. And specifically, the depleted absorber and the drift layer are now 1500 nm and 2500 nm, respectively, to form a 4 µm thick depletion width.

The P-down design (Epi 3) is designed to be similar to [44]. This design has been previously demonstrated and has a relatively low risk to achieve high responsivity. And since the transit time bandwidth is designed to be 71 GHz, this leads to a higher junction capacitance than Epi 1 and 2 design based on the same PD active dimension since the depletion width now is reduced to 1.1 µm. For wafer growth, we chose IntelliEpi, and the material system of InP/InGaAs/InAlGaAs is used. Starting from the InP substrate, a 100nm InGaAs contact layer is first grown on top of the substrate that is followed by a 100 nm thick InP block layer. Then a 1000 nm thick drift layer is grown next with a 10 nm InP layer (cliff layer). After that, 60 nm InGaAs (depleted absorber) and 200 nm InGaAs (un-depleted absorber) are used and sandwiched by a pair of 40 nm InAlGaAs grading layers. Then, 350 nm InP p-type contact layer is grown. Finally, 2 pairs of 15 nm thick InP/InAlGaAs super lattice layers plus a 10 nm thick InP layer are used as the bonding layers.

Next, I simulated the responsivity based on the three epis and the desired active section and waveguide dimensions by using Rsoft Beamprop software (scalar mode). The results are shown in table 6.1 and in Fig. 6.5 (a) and (b) respectively.

Table 6.1 Epi structures design parameters.

Epi type	**Epi 1 - P up**	**Epi 2 - P up**	**Epi 3 - P down**
Depletion width (µm)	2	4	1.1
Active area - width(µm)*length(µm)	5*40	5*40	5*35
Junction capacitance - Cj (fF)	12	6	18
Transit-time BW (GHz)	30	14	71
Responsivity (A/W)	0.78	0.85	0.96

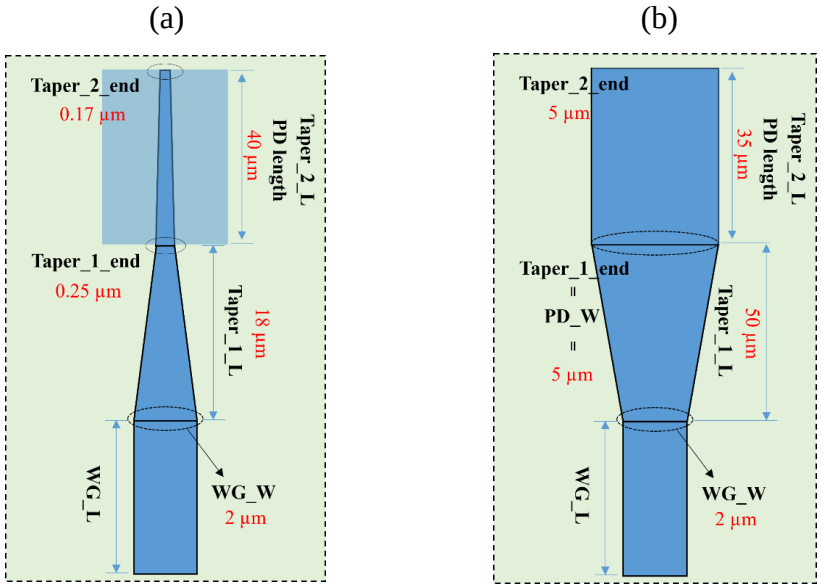


Figure. 6.5 Tapered waveguide and active area dimensions for (a) P-up and (b) P-down design.

For the PD width, I decided to fix it at 5 µm for in all simulations based on the optimized resolution of the photolithography tool in the UVA microfabrication facility. And for the photodetector length, I used 40 µm for all the P-up designs and 35 µm for the P-down design based on the responsivity data from my optical simulation. A two-staged narrow tapered waveguide is introduced in Fig. 6.5 (a) for the P-up design that starts from 2 µm width and tapers down to the final waveguide tip with 170 nm width. This is to provide a weakly confined mode for easing the mode coupling from silicon waveguide to the absorption layer. The simulated responsivity of the Epi 1 and Epi 2 are 0.78 A/W and 0.85 A/W respectively. The Epi 2 has the higher responsivity and this is due to the thicker absorption layer. Both of the values are smaller than the Epi 3 that can achieve 0.96 A/W using the wide taper section shown in the Fig. 6.5 (b). Here, we specifically reduce the PD length of the Epi 3 down to 35 µm to lower the junction capacitance but this will eventually sacrifice some of the responsivity. However, and as expected, the simulated responsivity is still higher than the P-up designs (Epi 1 and Epi 2). This indicates the major advantage of the P-down structure with its absorber being in close proximity to the waveguide which is a robust design to achieve high responsivity.

6.2.3 Heterogeneous 8-stage GAPC circuit simulation

Due to various delays in the GAPC project, the design work for the P-up Epi 2 and P-down Epi 3 were not fully completed. In the following, I will focus on the GAPC design using **the Epi 1**, its fabrication process flow, initial fabrication results, and measurement results. The layout of an 8-stage GAPC (8 PDs lumped together as a group, 64 PDs in total) is shown in Fig. 6.6. And Fig. 6.7 shows a zoom-in of the layout of a single segment of the GAPC. For each segment, the transmission line length is designed to be 1400 µm which is same as the optical delay line of each segment for the phase matching. The optical group index of 3.8 is used for the silicon waveguide delay line. On the other hand, the transmission line with GS configuration that has 140 µm width for both ground and signal line and 20 µm gap between ground and signal are designed to match the 50 Ω by loading with 8 evanescently coupled MUTC-PDs, and each PD has 12 fF junction capacitance (96 fF in total for each Group PD).

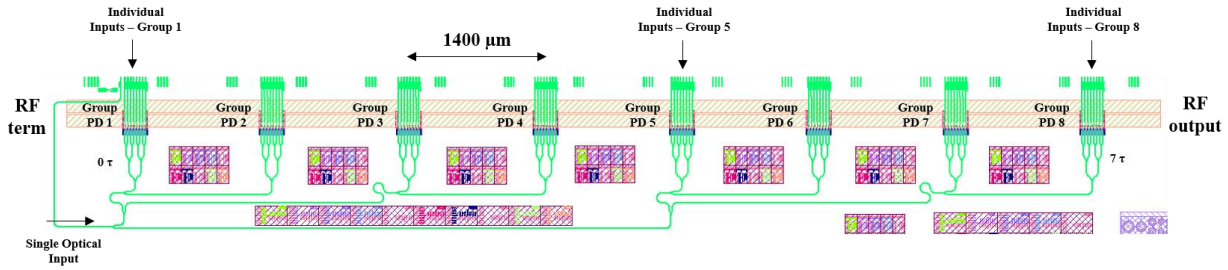


Figure. 6.6 Layout of the 8-stage GAPC (8 PDs lumped as a group).

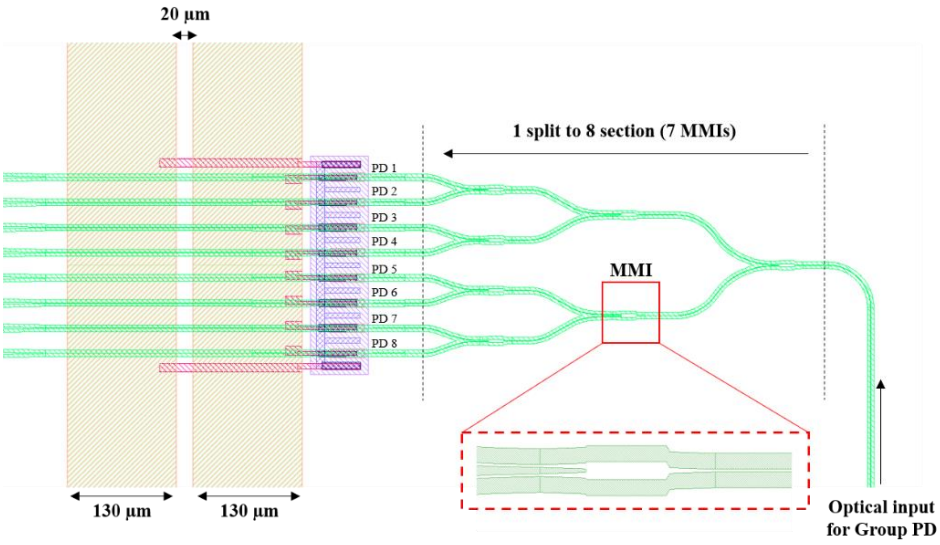


Figure. 6.7 Layout of a single segment in 8-stage GAPC.

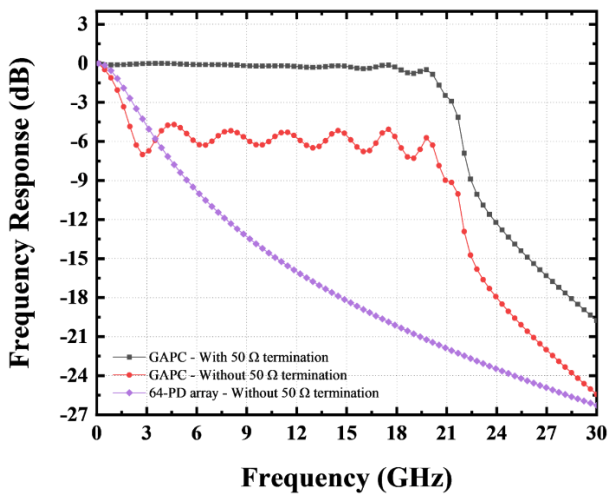


Figure. 6.8 Simulated bandwidth of the 8-stage GAPC and a lumped 64-PD array.

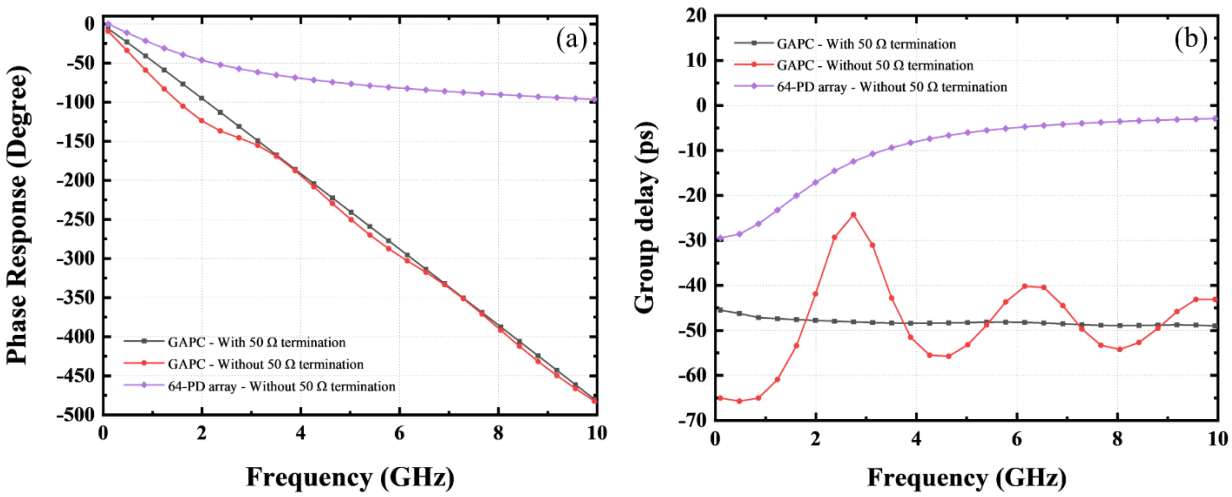


Figure. 6.9 Comparison of (a) phase response and (b) group delay of an 8-stage GAPC and a lumped 64-PD array.

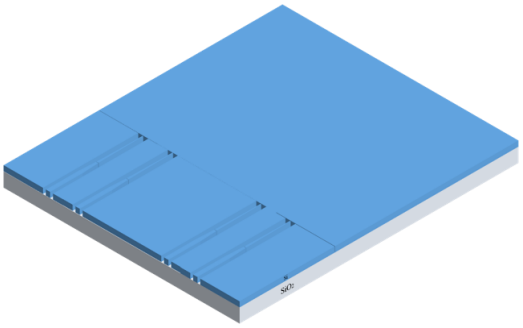
Figure 6.8 shows the simulated bandwidth comparison between the GAPC with and without termination 50 Ω resistor. With 50 Ω and phase match, the bandwidth has improved from 1.5 GHz to 21 GHz. After 21 GHz, we see the sharp cut-off which is attributed to Bragg reflection inside the transmission line. Compared with a lumped 64-PD array (without 50 Ω termination), an almost 7X bandwidth improvement can be found. The phase response from the GAPC shows a linear characteristic and as expected, this leads to very small group delay difference (< 5 ps) which is significantly lower than the lumped PD array that has 27 ps group delay difference up to 10 GHz which is shown in figure 6.9 (a) and (b) respectively.

6.2.4 Heterogeneous GAPC fabrication process flow

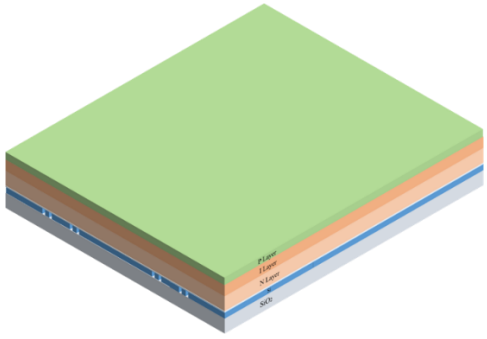
The fabrication process flow of the GAPC P-up design is presented in this section (Fig. 6.10). The silicon waveguides that include all the optical delay line, splitters, and taper structures were fabricated by our collaborators at USCB. In step 2, the bonding layer of the 2-µm will be faced down to the waveguide and bonded on to the silicon waveguide layer by direct (molecular) bonding. To be noted that during this oxygen-plasma-assisted boding process, a 10 nm thin SiO_2 layer will be formed onto of the silicon waveguide layer. Then, the InP substrate will be removed by using HCI + H_2O (3:1). This step was done by UCSB. Then a Ti/Pt/Au/Ti (20nm/20nm/80nm/20nm) metal stack was deposited on top of the p-contact layer followed by deposition of SiO2 as hard mask (step 4). In steps 5 and step 6, a layer of photoresist (AZ5214) was coated for patterning the hard mask and then the hard mask was formed by dry etching SiO_2 using CHF_3. After this, the sample was put into O_2 plasma for cleaning overnight to fully remove the hardened photoresist residual. Next (step 7), a Cl_2/N_2 based recipe was used for dry etching and forming the P mesa all the way down to stop at the n contact layer. Then a layer of SiO_2 as N mesa hard mask was grown, and the N mesa hard mask is formed by CHF_3 recipe (steps 8 and 9, respectively). For the N mesa formation (step 10), I used a combination of the dry (Cl_2/N_2) and wet etching (Citric acid + H_2O_2). Dry etching stops when the InP n contact layer is only ~ 50 nm, and then wet etching will fully remove the rest of the layers to eventually stop at the 10 nm SiO_2 layer formed on top of the silicon waveguide layer as the etch stop layer. This combination is to prevent the silicon waveguide to be over-etched if only the dry etching step was used. Step 11 and step 12 use CHF_3 to open the N contact followed by the N metal deposition: AuGe/Ni/Au/Ti (20 nm/20 nm/80 nm/20 nm) and P metal windows, respectively. In step 13, the first layer of the SU8 (SU8 2002) with 2 µm thickness is patterned for the metal wire routing. Then in step 14, Ti/Au (20 nm/100 nm) is used to pattern the metal wire routing by using AZ 5214 for later on connecting the p and n metal parts to the transmission line layer. Step 15, the second layer of the SU8 (SU8 2002) with the via holes is spun and patterned and to sandwich the metal routing. After second layer SU8 patterning with the via holes opened, the ends of the metal wire are exposed and ready to be connected with the transmission line layer that is deposited on top of the second layer SU8. This leads to the final step 16; a transmission line seed layer (Ti/Au 20nm/50nm) is grown and followed by the plating step to eventually thicken the transmission line up to 3 µm. It should be mentioned that I developed

this completely new two-layer SU8 process to avoid using air bridge to connect N metal to the ground transmission line which in this case is ~ 200 µm long distance that may be vulnerable to the lift-off process.

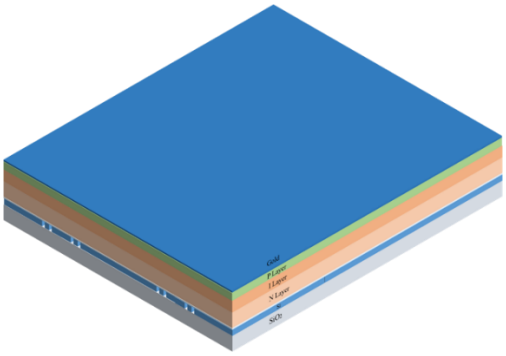
Step 1 – Si waveguide etched



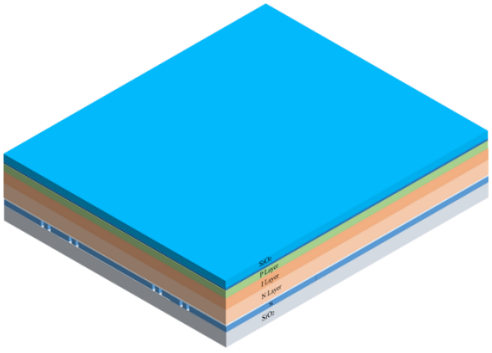
Step 2 – IIIV bonding on SOI / substrate removal



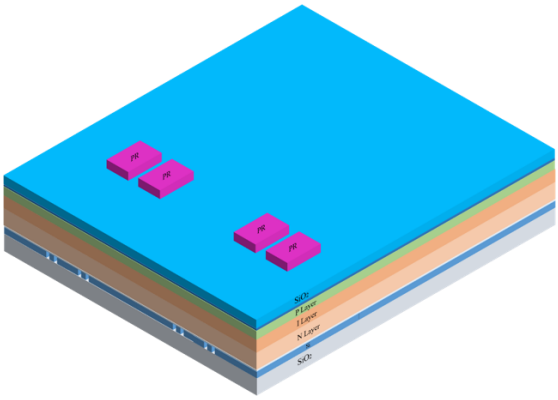
Step 3 – P Metal deposition



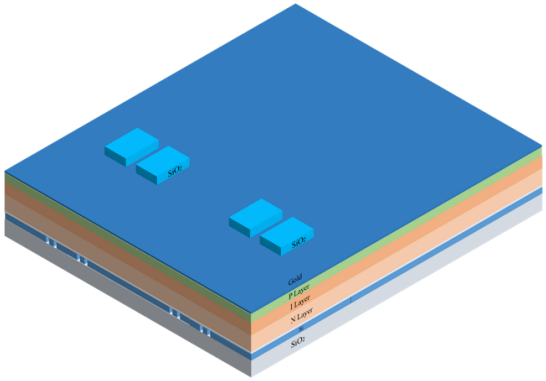
Step 4 – P mesa hard mask SiO2 deposition



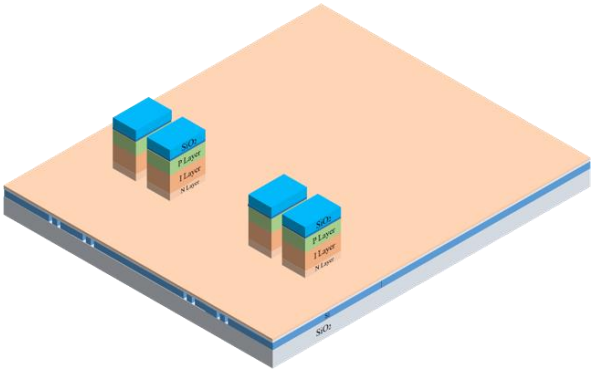
Step 5 – P mesa hard mask patterning



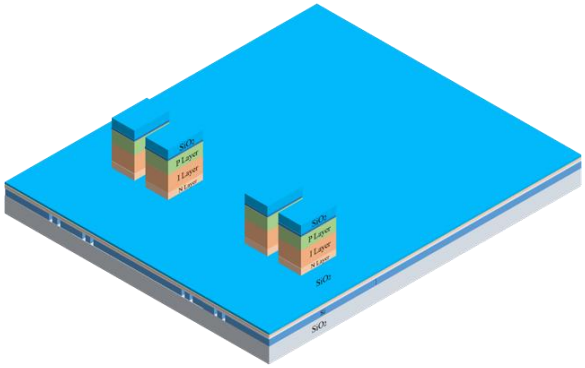
Step 6 – P mesa hard mask formation



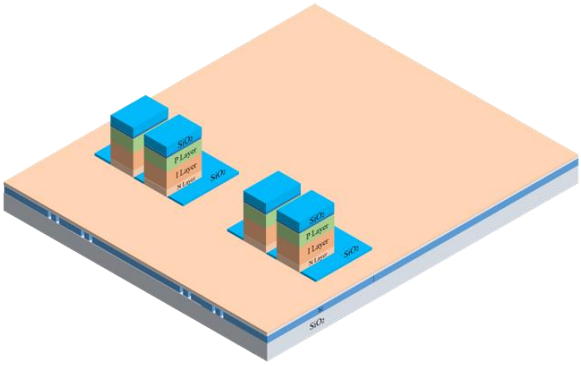
Step 7 – P mesa formation (dry etch)



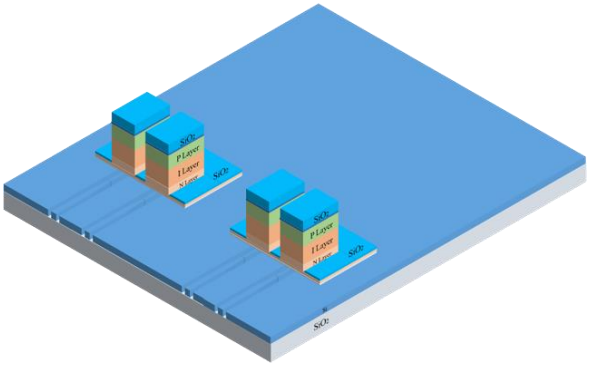
Step 8 – N mesa hard mask deposition



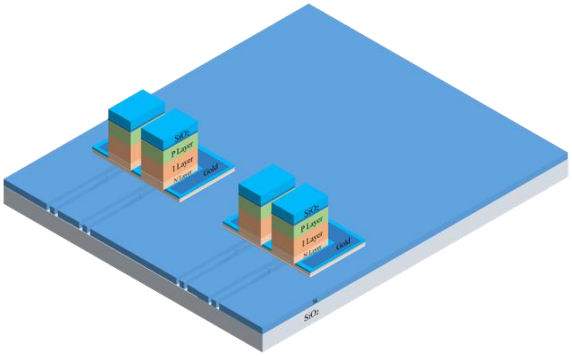
Step 9 – N mesa hard mask formation



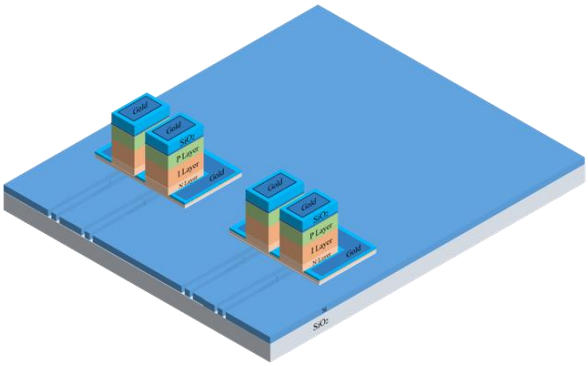
Step 10 – N mesa hard formation (dry + wet etch)



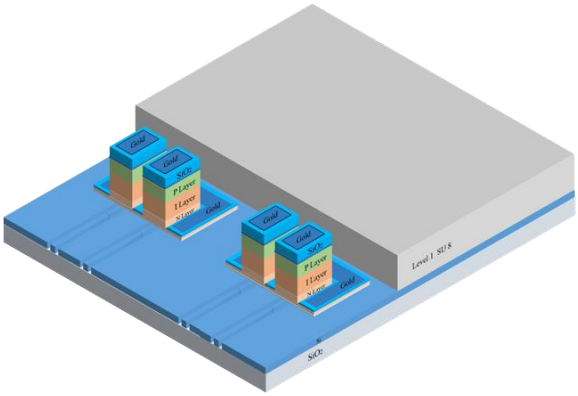
Step 11 – N contact open + N metal deposition



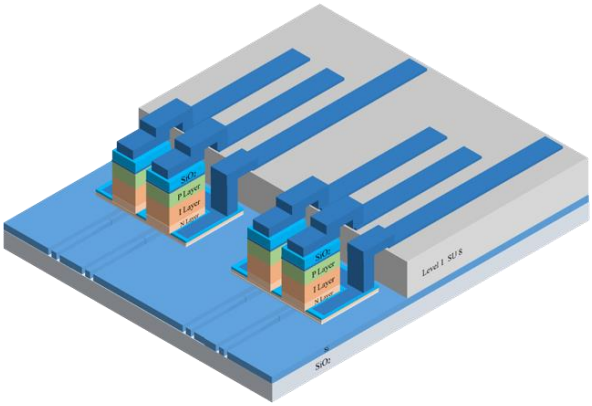
Step 12 – P metal open



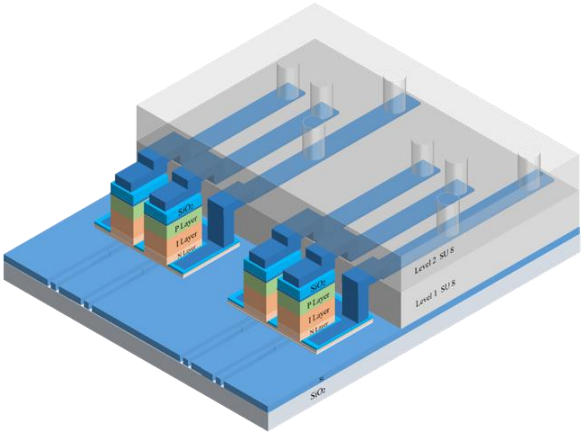
Step 13 – First SU8 layer patterning



Step 14 – metal wire routing deposition



Step 15 – Second SU8 layer patterning (w/ via holes)



Step 16 – transmission line metal plating

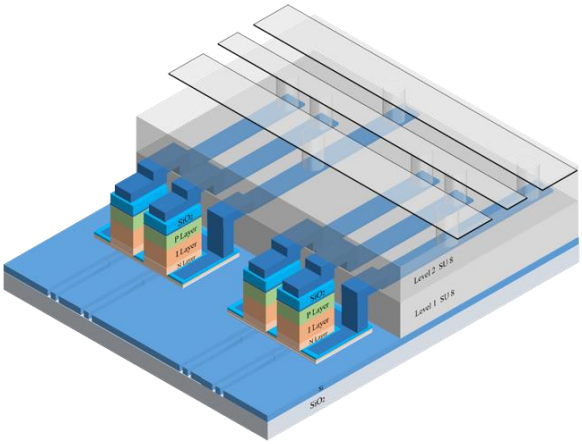


Figure 6.10 GAPC fabrication process flow from step 1 to step 16.

6.2.5 First fabrication run, initial measurement results, analysis, and future work

This section reports some of the microscope pictures of the very first GAPC fabrication run with the fab steps described above. Fig. 6.11 shows the III-V epi after step 1. Additionally, Fig. 6.12 (a), (b), and (c) show the SEM pictures of the 1-to-2 MMI, 600-nm wide straight silicon waveguide used for the optical delay line portion, and the taper waveguide tip respectively. Some fabrication errors were identified on the taper waveguide tip. A 170 nm taper waveguide end was designed, however, we found waveguides as narrow as 78 nm. This could potentially affect the PD responsivity. Fig. 6.13 shows the chip at step 10. In this figure, 8 p mesas can be clearly seen. It can be noticed that after dry and wet etching of the n mesa, some residual III-V material can still be seen inside the waveguide trench. Fig. 6.13 (c) shows a picture after 10 more minutes of etch to fully remove the residuals inside the waveguide trench using the same citric acid + H_2O_2 recipe. Next, fig. 6.14 (a) shows the chip after the n and p metal windows are opened. Figure 6.14 (b) shows the chip after step 14, patterning the first layer SU8 and with the metal wire routing for later connecting the p and n metal to the transmission line. I used an IV measurement (figure 6.16) to verify that the metal routing does indeed connect the p and n metal. The result shows a working group PD but indicates a potentially higher series resistance. Figure 6.14 (c) shows the second layer SU8 patterned with the via holes opening and figure 6.15 (a) shows the chip with the completed transmission line fabrication.

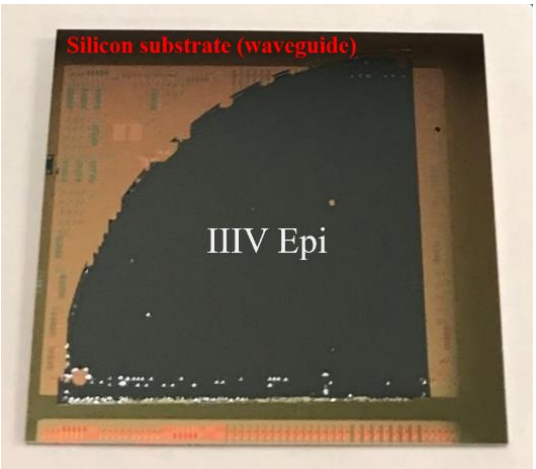


Figure 6.11 III-V epi bonded on the patterned silicon.

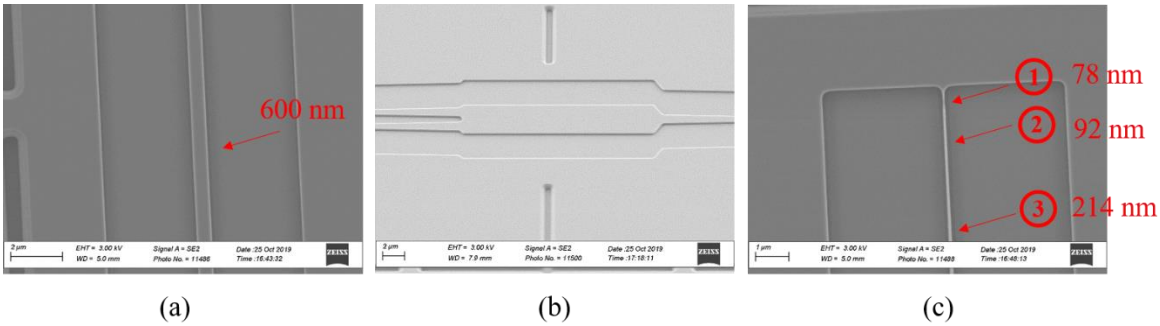


Figure 6.12 Passive structures on the patterned silicon: (a) straight silicon waveguide, (b) 1-to-2 MMI, and (c) narrow taper waveguide end with measured waveguide width.

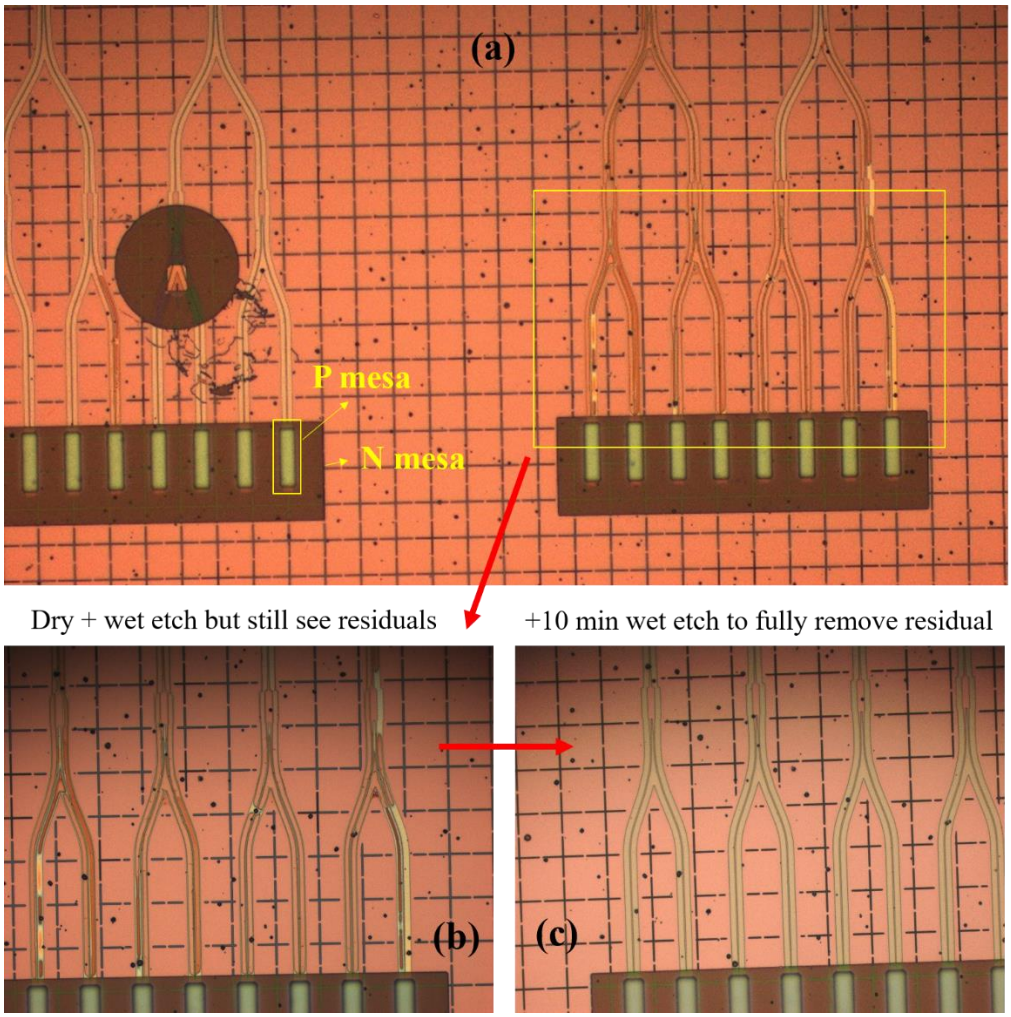


Figure 6.13 (a) after first run of N mesa dry etch and wet etch with residuals left, (b) zoom in picture of the yellow box in (a), and (c) adding 10 mins of wet etching to fully remove the N mesa residuals.

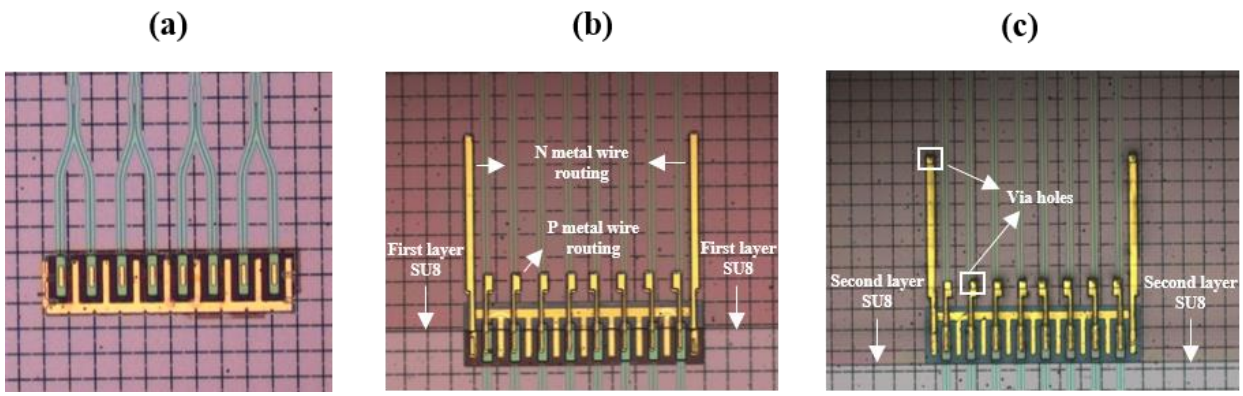


Figure 6.14 (a) after step 12 that p metal has opened, (b) after step 13 that first layer SU8 has been patterned and step 14 metal wire routing has been patterned, and (c) after step 15 that second layer SU8 with vie holes has been patterned.

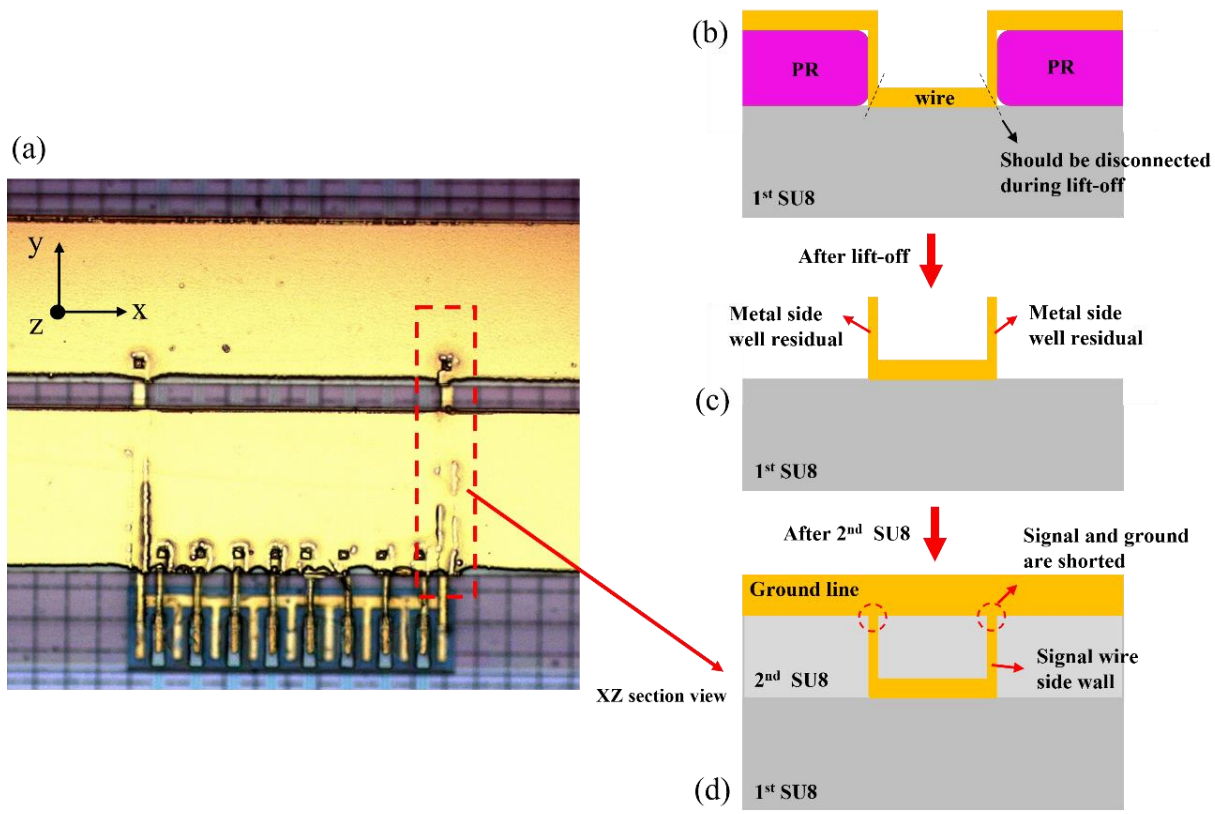


Figure 6.15 (a) after step 16 that the transmission line metal layer has been plated and (b) to (d) describes the reasons why the metal wire is shorted to the transmission line layer.

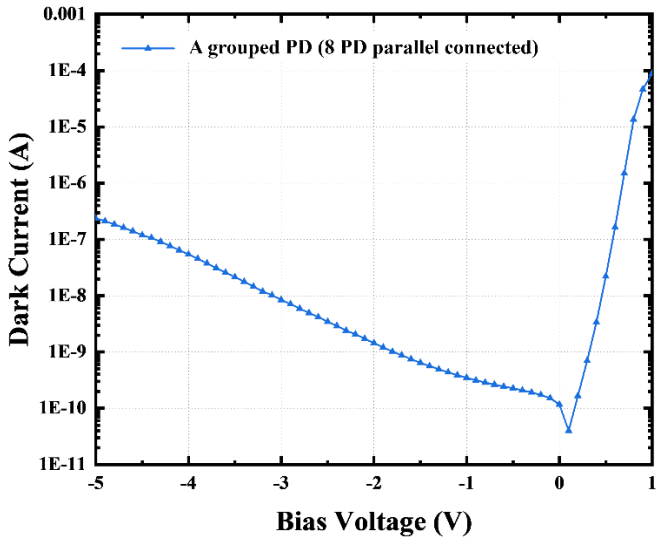


Figure 6.16 IV measurement that is done after step 13 that first layer SU8 has been patterned, and to measure the IV from the metal wires deposited on top of the SU8 that are connected to the P and N metals respectively.

Unexpectedly, the fabricated GAPC device showed a short circuit after the transmission line metal lift-off step. The issue was caused by the metal wire routing step (step 14) which is described in the figure 6.15 (b)-(d). The photoresist AZ 5214 was originally used for the step 14 for the metal wire lift-off process. However, since the overall height of the AZ 5214 is only 1.7 µm thick which is thinner than the height of the p mesa (2.8 µm) and the first layer SU8 (2.5 µm) layer, the patterned AZ 5214 on top the first layer SU8 for the metal wire routing was even thinner than the 1.7 µm. This leads to a more difficult lift-off process for the metal wire because now the metal side wall residuals are hard to be taken off together with the photoresist during the lift-off process. Therefore, as shown in the figure 6.15 (d), at least a few µm high metal side wall penetrated through the second layer SU8 and connected to the ground and signal transmission line to cause the short circuit. To solve this issue for future runs, thicker PR such as AZ 4330 or 4620 are recommended for using to ease the metal lift-off process in step 14.

Several single photodetectors with different active lengths were also fabricated which are shown in figure 6.17 for testing the PD responsivity and investigating waveguide coupling mechanism based on the P-up GAPC design. Very low responsivities were measured from these single PDs. The results are shown in table 6.2. In theory, the PD with longer active sections should achieve higher responsivity due to the longer absorption length. However, this trend cannot be observed

based on the measurement results which indicates that the responsivity was negatively affected for all PDs potentially during certain fabrication steps.

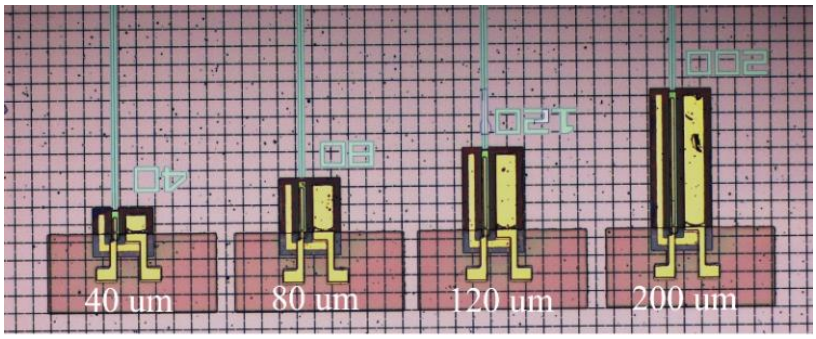


Fig. 6.17 Single PDs with different active lengths after the step 13.

Table 6.2 Measured responsivities of different length single PD after step 16.

WG PD Types	Responsivity (A/W)
35 µm	0.048
40 µm	0.001
80 µm	0.002
120 µm	0.004
200 µm	0.003

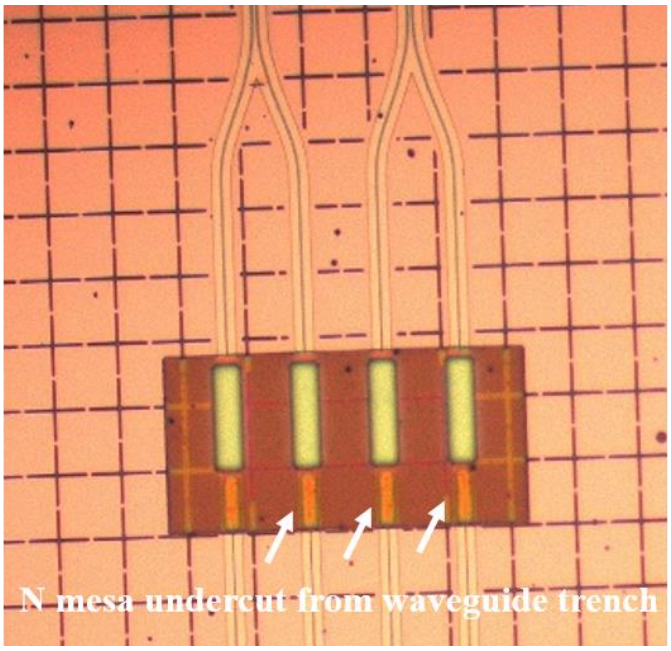


Figure 6.18 Bottom side of N mesa undercut during wet etching from the waveguide trench.

Most likely, the N mesa wet etch step is the main reason that causes the low responsivity. During this step, wet etch solution can enter from the bottom of the N mesa through the waveguide trenches and etch away part of the bonding layers and N mesa layer from underneath. This can create an air gap between the taper waveguide and the N mesa which can impair the optical coupling especially in this type of narrow taper waveguide. To analyze this more, I did optical simulations. First, instead of using only scalar mode to calculate the responsivity from the Rsoft BeamProp, this time I used the Semi-vector mode to analyze the TE and TM modes individually because during the simulation I observed a different responsivity by using TE and TM fundamental mode separately as the input mode. Also, I used Lumerical FDTD to further compare the results between the two commercial softwares. According to the simulation results which are shown in the table 6.3, the TM polarized light has a stronger response than the TE polarized light. Based on the fig. 6.19 (a) and (b), it can be seen that compared with the TE polarized light, TM polarized light is quickly absorbed. In contrast, the TE polarized light, remains highly confined in the tapered waveguide section all the way to the waveguide end. In figure 6.20, the cross-section views of the optical intensity at different propagating distances into the active section are shown and it can be further verified that the TE light remains highly confined in the waveguide. On the other hand, the TM light is already distributed uniformly in the active layer and absorbed within the very first 10 µm into the active section which is shown in figure 6.20 (g).

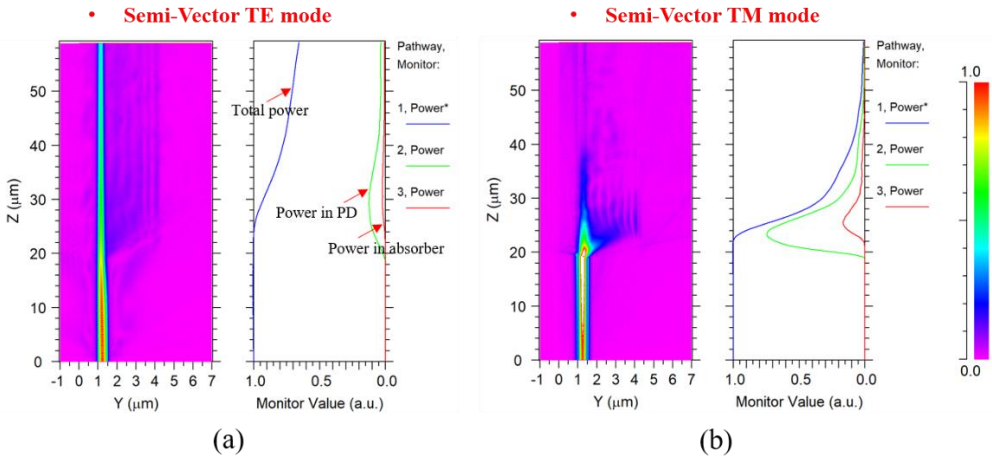


Figure 6.19 GAPC P-up Rsoft optical simulation using (a) semi-vector TE mode and (b) semi-vector TM mode.

Table 6.3 Simulated responsivity of GAPC P-up using Rsoft and Lumerical for both TE and TM

Responsivity (A/W)	TE mode	TM mode
Rsoft	0.36	1
Lumerical FDTD	0.38	0.77

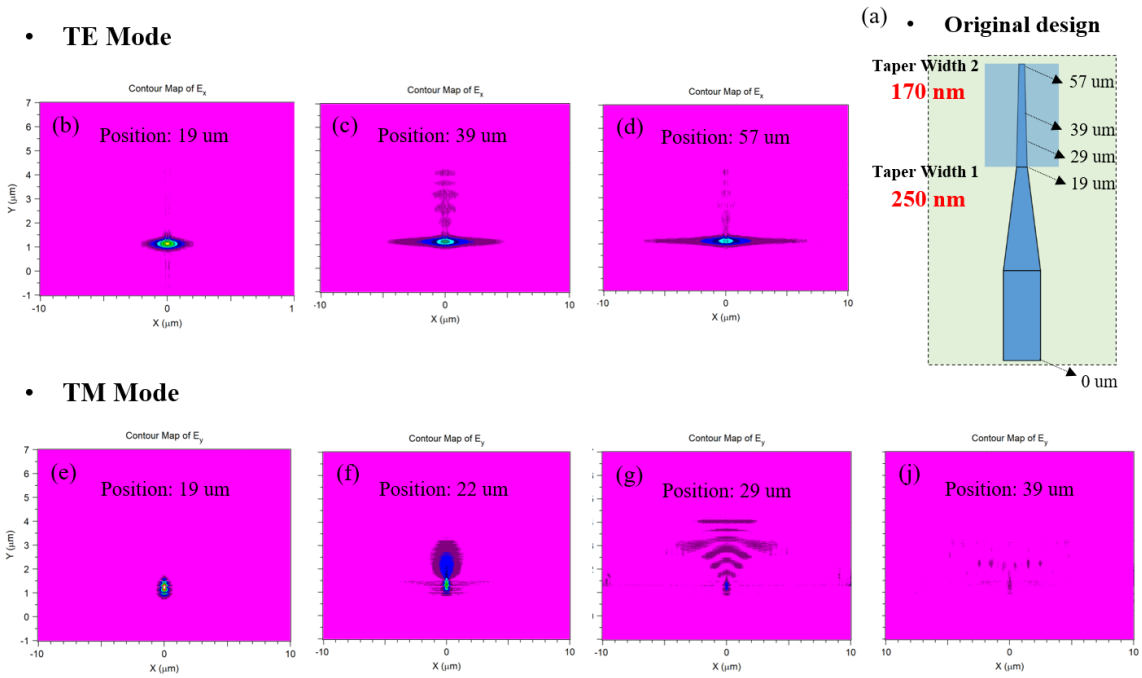


Figure 6.20 (a) top schematic view of the taper waveguide section with PD active region, (b)-(d) TE mode cross section views at different transmission distance based on the markers on (a), and (e)-(j) TM mode cross section views at different transmission distance

The potential air gap generated between the N mesa and the silicon waveguide (in figure 6.21 (a)) can be detrimental to the mode coupling especially for the TM polarized light based on its mode distribution property. The simulation results shown in the Fig. 6.21 (b) supports this assumption. This figure shows that by having a 100 nm thin air gap created during the wet etch this can significantly reduce the responsivity for TM polarized light from 1 A/W down to 0.1 A/W. Compared with the TE responsivity that is reduced from 0.32 A/W down to 0.08 A/W, TM seems to be the major limiting factor to the responsivity in this fab run.

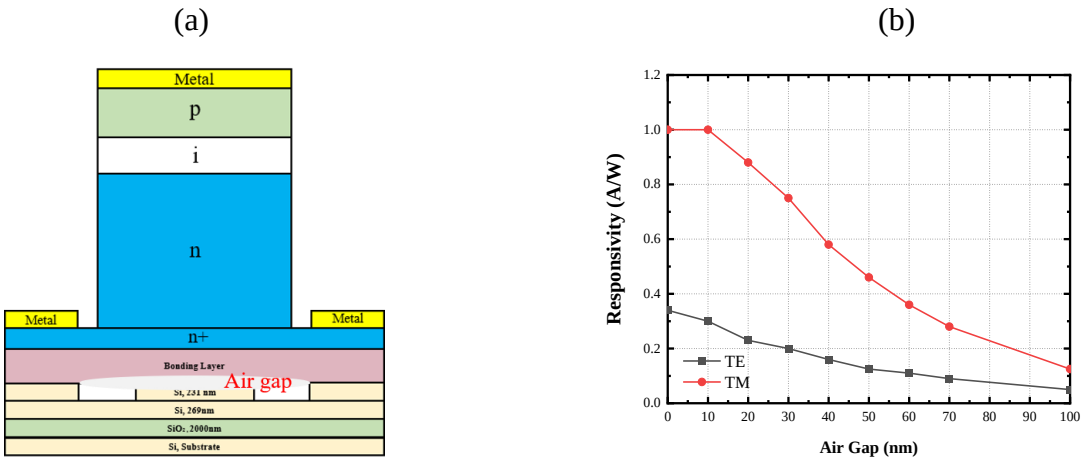


Figure 6.21 (a) Schematic of the created air gap during N mesa wet etch and (b) simulated responsivity of GAPC P-up design with various air gap thicknesses created by N mesa wet etch.

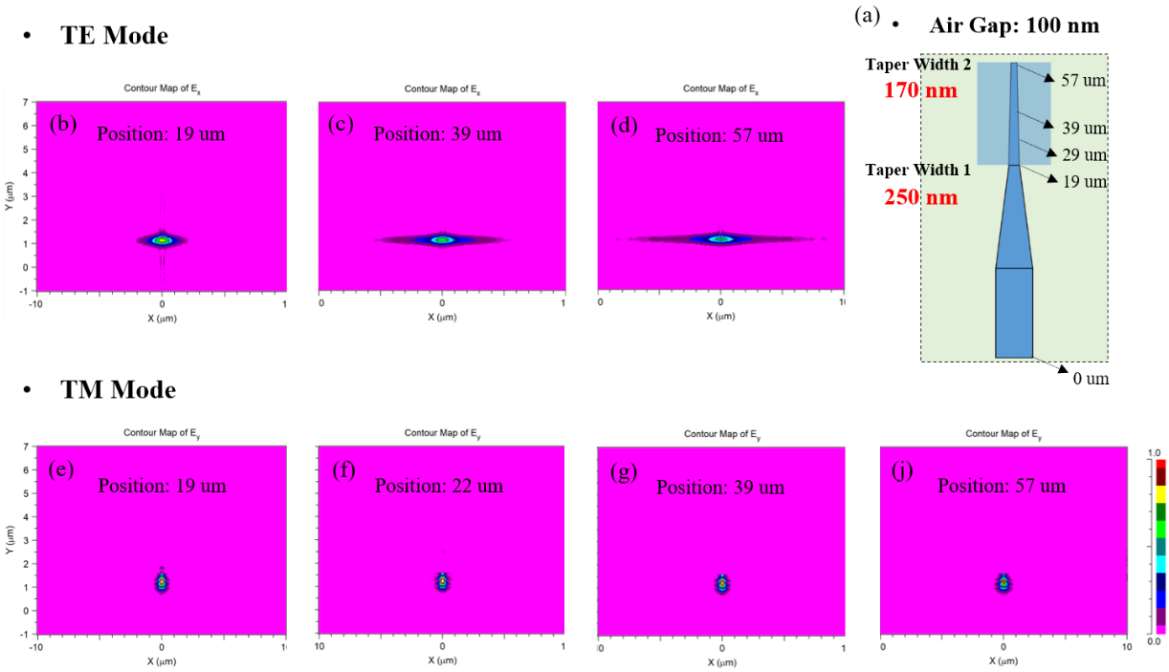
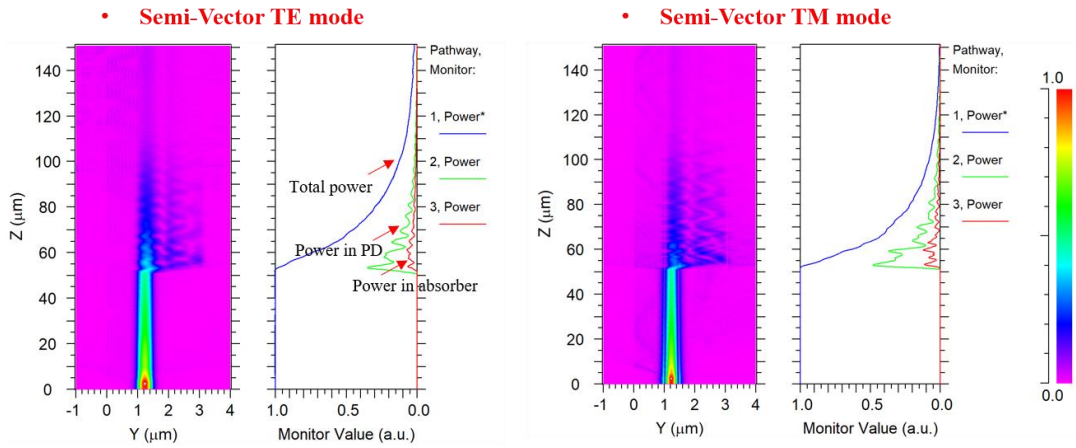


Figure 6.22 (a) top schematic view of the taper waveguide section with PD active region under the airgap scenario, (b)-(d) TE mode cross section views at different transmission distance based on the markers on (a), and (e)-(j) TM mode cross section views at different transmission distance

Since the wet etch undercut is difficult to be avoided, a way to resolve the responsivity issue is to use the P-down design. As shown in the Fig 6.5 (b), for the P-down design, the wide taper waveguide dimension is matched the be exactly the same as the PD active region. This greatly reduce the chances of wet etch solution entering the waveguide trenches and etching the bottom

layers during the N mesa wet etch. And most importantly shown in the figure 6.23 and table 6.4, the simulation results based on our previous P-down work [44] show that this type of waveguide structure is not very polarization dependent. Both, the responsivity of TE and TM polarized light can be both designed to be around 1 A/W. In conclusion, the next step for demonstrating the GAPC concept based on the heterogenous platform with the P-down option will be the most promising way to move forward.



(a) (b)

Figure 6.23 GAPC P-down Rsoft optical simulation using (a) semi-vector TE mode and (b) semi-vector TM mode.

Table 6.4 Simulated responsivity of GAPC P-down using Rsoft and Lumerical for both TE and TM mode.

Responsivity (A/W)	TE mode	TM mode
Rsoft	1	1.12
Lumerical FDTD	0.96	1.01

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List of Publications

Journal Articles

[1] **Tzu, T.C**., Fatema, T., Gao, J., Sun, K., Morton, P.A., and Beling, A., High-Power traveling-wave photodetector and balanced traveling-wave photodetector on Si with integrated circuit. *(Under preparation)*

[2] **Tzu, T.C**., Fatema, T., Gao, J., Sun, K., Morton, P.A., and Beling, A., 32-channel wide-bandwidth photonic RF combiner based on distributed group array photodetector. *(Under preparation)*

[3] **Tzu, T.C**., Sun, K., Costanzo, R., Ayoub, D., Bowers, S.M. and Beling, A., 2019. Foundry-enabled high-power photodetectors for microwave photonics. *IEEE Journal of Selected Topics in Quantum Electronics*, *25*(5), pp.1-11.

[4] Gao, J.*, **Tzu, T.C**.* Sun, K., Morton, P.A., and Beling, A., > 67 GHz InP-based micro transfer printable Mach Zehnder Modulator. *(Under preparation)* ***(* Equal contribution)***

[5] Yu, F., **Tzu, T. C.**, Gao, J., Fatema, T., Sun, K., Singaraju, P., ... & Beling, A. (2022). High-Power High-Speed MUTC Waveguide Photodiodes Integrated on Si 3 N 4/Si Platform Using Micro-Transfer Printing. *IEEE Journal of Selected Topics in Quantum Electronics*.

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Conference Proceedings

[1] Sun, K., Costanzo, R., **Tzu, T.C.**, Bowers, S.M. and Beling, A., 2020. Foundry-Enabled Ge Photodiode Arrays on Si on Insulator (SOI) with On-Chip Biasing Circuit. In *2020 IEEE Photonics Conference (IPC)* (pp. 1-2). IEEE.

[2] Sun, K., **Tzu, T.C.**, Costanzo, R., Yu, Q., Bowers, S.M. and Beling, A., 2019, October. Ge-on-Si balanced periodic traveling-wave photodetector. In *2019 IEEE Photonics Conference (IPC)* (pp. 1-2). IEEE.

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