An Analysis of a Symmetric Circuit Topology for Ultra-Low Power Voltage Scaling in Deep Nanoscale CMOS

A Thesis

Presented to

the faculty of the School of Engineering and Applied Science

University of Virginia

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in partial fulfillment

of the requirements for the degree

Master of Science

by

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May

2015

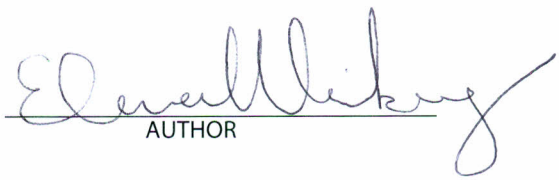
APPROVAL SHEET

The thesis

is submitted in partial fulfillment of the requirements

for the degree of

Master of Science



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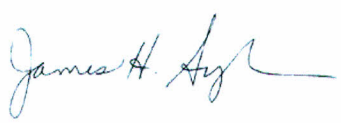

Dean, School of Engineering and Applied Science

May

2015

ACKNOWLEDGMENTS

I have a number of people to thank for helping to make this work possible. First of all, I would like to thank my advisor, Dr. Mircea Stan, for his guidance and support in this project. His feedback has been invaluable and has greatly improved my abilities as a researcher. I would also like to thank my committee members, Dr. Joanne Dugan and Dr. Gabriel Robins for all their time and support in my work.

I would like to thank Dr. Dugan for her support and patience in helping me acclimate to a new field as a teaching assistant for digital logic design these past two years. Thank you to all the professors who spent countless office hours helping to catch me up on fundamentals of Computer Engineering: Dr. Ben Calhoun, Dr. Marty Humphrey, Dr. Dan Weller, Dr. Gabriel Robins, Dr. John Stankovic, Dr. Kevin Skadron, and Dr. Jacalyn Huband. Thank you to Natalie Edwards for always offering help and support in administrative tasks as well as her friendly smile and perspective.

I would like to thank all my peers and colleagues on the 3rd floor of Rice Hall who have each spent hours with me troubleshooting software bugs, teaching me how to use new tools, and catching me up on more fundamentals. Without these folks I would certainly not have been able to learn an entire undergraduate's worth of Computer Engineering (along with the graduate-level material) over the course of a couple years. A special thank you to all my High Performance Low Power (HPLP) lab mates: Alec Roelke, Andy Whetzel, Ben Melton, Kaushik Mazumdar, Mateja Putic, Mehdi Kabir, Runjie Zhang, Tommy Tracy, and Xinfei Guo. I would also like to say a special thank you to Farah Yahya, Christopher Lukas, Divya Akella, Seyi

Ayorinde, Arijit Banerjee, Ahmed Aly, Philip Asare, Yu Huang, Kevin Leach, Sourav Maji, Andrea Vaccari, Tamal Batabyal, Harsh Patel, Jim Boley, Alicia Klinefelter, and others.

Last, I would like to thank all my family and friends. It would have been very difficult to do this without all of their love and support throughout this process.

ABSTRACT

As integrated circuits (ICs) continue to scale, power consumption has become an important concern, making sub-threshold (sub-VT) operation an attractive route for ultra-low power (ULP) applications, especially those that harvest energy from the environment. However, a major roadblock lies in increased sensitivity to process variations both at near- and sub-VT. Additionally, temperature variations can be detrimental to circuit functionality for energy harvesting applications operating in outdoor environments. This vulnerability to variations at the device level is exacerbated by imbalances between pull-up (PUN) and pull-down (PDN) networks at the circuit level. This thesis presents a symmetric circuit topology in conjunction with a biasing scheme that maintains symmetrically robust operation of ULP energy harvesting systems in a variety of climates, including extreme temperatures. Through noise-analysis and Monte Carlo (MC) simulations performed in a commercial 28nm Fully Depleted Silicon On Insulator (FDSOI) technology, the robustness to variations and extreme temperature ranges of the proposed symmetric 2-to-1 multiplexer design (mirror mux) with bias is demonstrated and compared to conventional 2-input NAND and NOR-based circuits. The linearity between temperature and bias makes this scheme easily applicable for programmable sensors in a variety of applications requiring environmental adaptability.

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CHAPTER 1

INTRODUCTION

As integrated circuits (ICs) continue to scale, power consumption becomes an increasingly important concern, making sub-threshold (sub-VT) an attractive route for many ultra-low power (ULP) applications. Many such applications utilize energy harvesting, a mechanism by which energy already present in the environment is collected and stored by a device and used as its power supply [1]. Such energy may occur naturally (e.g. solar energy, body heat) or be available as a side effect of some other technological activity (e.g. electromagnetic RF energy, mechanical vibrational energy, etc.). Because the energy is already present, it makes it essentially free; thus, energy harvesting is a very promising avenue for designers with ULP applications. A major roadblock to usability of such applications lies in increased sensitivity to variations both at near- and sub-VT, especially at the low voltages typical for energy harvesting, and the wide temperature ranges encountered by outdoor systems.

In this work, the trade-offs associated with symmetric circuit design are explored. A symmetric 2-to-1 multiplexer design (mirror mux) is compared to 2-input NAND and NOR gates as universal logic elements for digital circuit design. The mirror mux's symmetric design is hypothesized to be optimal for robust ULP operation in the weak inversion regime. This work also investigates balancing circuit functionality with temperature and back-gate biasing, body biasing for Fully

Depleted Silicon On Insulator (FDSOI) devices. This analysis provides insight into additional ULP digital circuit design knobs.

This thesis presents a symmetric circuit topology in conjunction with a back-gate biasing scheme for ULP energy harvesting applications operating in variable and extreme temperatures. The relationship between temperature and required bias is linear, making this scheme easily applicable for programmable sensors in a variety of applications requiring environmental adaptability. The following sections motivate mux-based design, discuss the negative impacts of asymmetric circuit topologies typical of conventional CMOS logic gates, and present the mirror mux as an alternative optimal for variation-tolerance in sub-VT. The mechanism of back-gate biasing in FDSOI and related work are also discussed. The contributions of this thesis are as follows:

- A symmetric topology ideal for robustness to variations in sub-VT.
- A back-gate biasing scheme for balancing circuits that require adaptability to a variety of temperatures, including extreme temperatures.
- The discovery of the linear relationship between required bias and temperature, allowing the proposed scheme to be readily implemented in energy harvesting applications.
- An analysis demonstrating the importance of symmetry in sub-VT.
- An analysis of the trade-offs associated with symmetric sub-VT circuit design.
- A flow for implementing mux-based designs optimal for variation-tolerance in sub-VT.

Circuit Asymmetry and Its Impacts in Sub-VT

Circuit imbalances are amplified in sub-VT. This is because the degraded I_{on}/I_{off} ratio makes sub-VT circuits more prone to effects from threshold voltage shifts, the most common device-level side effect from process variations [2]. Transistor drive current in the weak inversion (i.e. sub-VT) regime is given by [3]:

$$I_{DS} = I_0 \exp((V_{GS} - V_T)/nV_{th}) \quad (1)$$

$$I_0 = \mu_o C_{ox} (W/L)(n - 1)V_{th}^2 \quad (2)$$

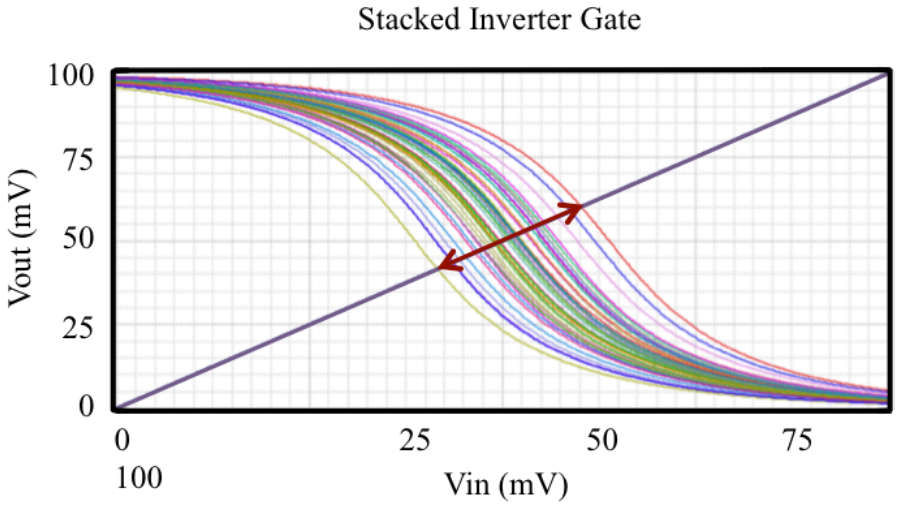
where I_0 is the drain current when V_{GS}=V_T, V_{GS} is the voltage between gate and source, V_T is the transistor threshold voltage, V_{th} is the thermal voltage (given by kT/q), n is the sub-threshold slope factor, and C_{ox} is the capacitance of the oxide.

Note in (1), threshold voltage is an exponential factor, which illustrates the high sensitivity to threshold voltage shifts experienced by circuits in sub-VT. Moreover, the quadratic thermal voltage term in (2) illustrates the strong relationship between temperature and drive strength. The relationship between temperature and leakage is explained in greater detail in [21]. The impacts of this relationship on device parameters are also shown in later sections.

Asymmetric Circuit Topologies

The impact of parallel and stacked transistors in conventional CMOS gates is magnified and can influence functionality in sub-VT circuits. Therefore, the inherent asymmetry between pull-up (PUN) and pull-down (PDN) networks in most CMOS implementations is detrimental to circuit robustness in the sub-VT domain. This is demonstrated in Figure 1, where 50-point Monte Carlo (MC) simulations show the

greater impact of variations on the asymmetric NAND and NOR topologies, shown in (b) and (c), respectively, as compared to a stacked inverter gate, shown in (a). A *stacked* inverter gate (an inverter with two pMOS devices in series as the PUN and 2 nMOS devices in series as the PDN) is used instead of a regular inverter so that our comparison between gates is consistent in terms of sizing, area, and device parameter variations. It is clear from Figure 1 that having a *balanced* circuit topology as well as balanced PDN-PUN drive strength, as is the case for the inverter, is important in terms of robustness and reliability. Figure 2 (a) and (b) show the asymmetric circuit topologies of conventional NAND and NOR CMOS gates.



(a)

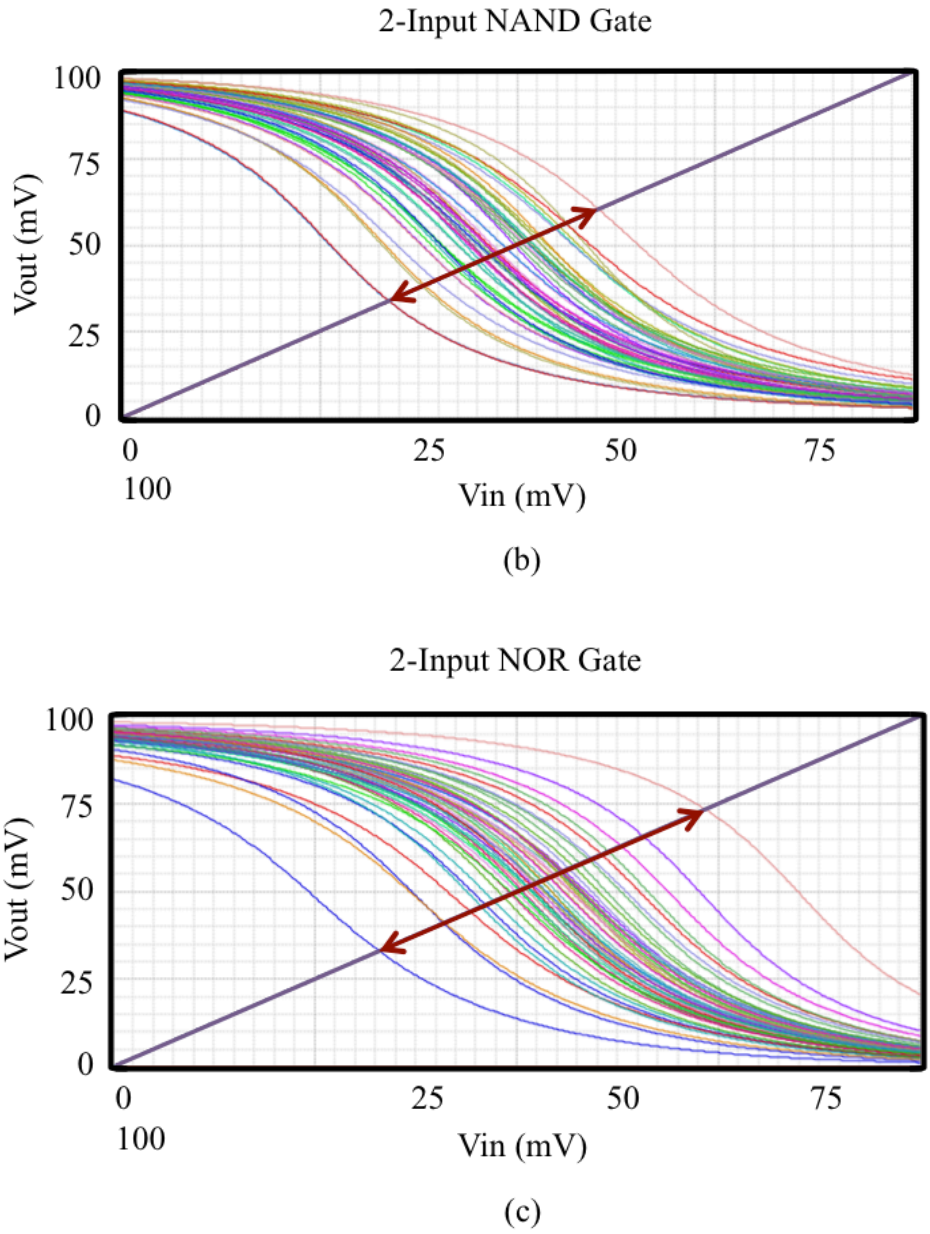


Figure 1: The impact that asymmetric topology has on circuit robustness. 50-point MC simulations at *VDD*=100mV for (a) a stacked inverter gate, (b) a 2-input NAND gate, and (c) a 2-input NOR gate. Notice the large spread in values for the NAND and NOR gates shown in (b) and (c), respectively, as opposed to the stacked inverter gate shown in (a).

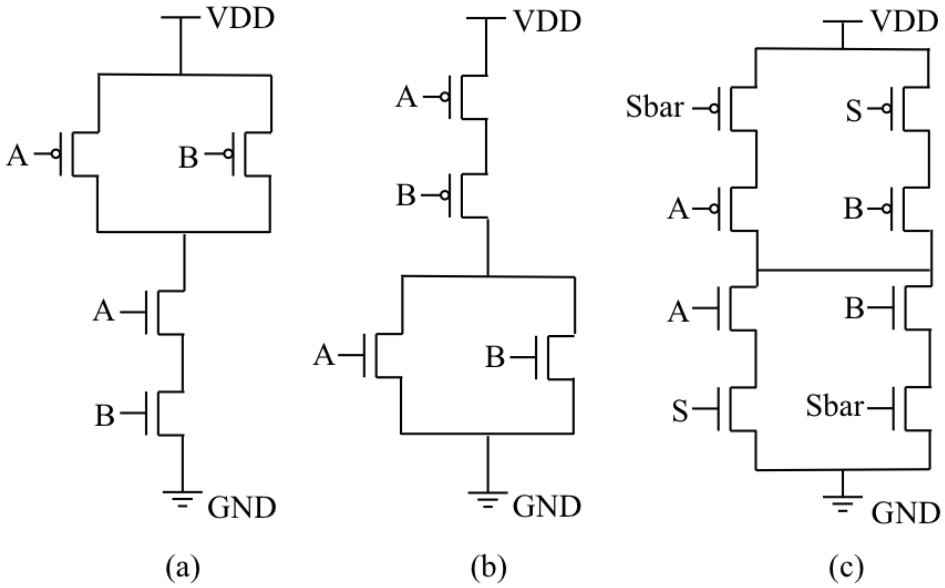


Figure 2: (a) 2-input NAND gate and (b) 2-input NOR gate. The asymmetry inherent to these universal logic gates is harmful to robustness in sub-threshold. (c) Our proposed 2-to-1 mirror mux topology.

Functional Asymmetry and Temperature Fluctuations

Many energy-harvesting applications are designed to operate in outdoor environments. They have to be able to withstand a wide range of extreme temperatures. Moreover, with continued scaling, drastic gains in power density have made operation in extreme heat an important characteristic of current ICs. [4] discusses the strong impact that temperature variations have on sub-VT leakage. Variations are harmful to SRAM cells, which frequently have to tolerate high heat during operation. This makes adaptability to a variety of temperatures an important characteristic of many such designs. In addition to quadratic V_{th}, decreased I_{on}/I_{off} in sub-threshold makes having a balanced design extremely important since the voltage swing consists of a much smaller margin. I_{on} is given by (1). Setting V_{GS}=0 gives the expression for I_{off}:

$$I_{off} = I_0 \exp(-V_T/nV_{th}) \quad (3)$$

(3) demonstrates that the relationship between temperature and power consumption persists for sub-VT leakage. Figure 3 illustrates the impact of temperature variations on static noise margins (SNMs) for an inverter between *VDD*=50mV and *VDD*=400mV.

Related Work

A great deal of work has been done in the area of sub-VT optimization. [6] conducts an analysis of logic families optimal for sub-threshold. Some work has been done in the exploration of symmetric topology and design methodology, though none like the one proposed here. [4] presents an analysis of the strong impact that temperature variations have on sub-VT leakage and describes how harmful this is to SRAM cells. [7] discusses at length the effectiveness of using body bias to mitigate the harmful effects from process variations. [8] proposes back-gate biasing for high performance applications with ultra-lower power consumption. One of the more closely related works is [9], in which the authors design a symmetric SRAM cell to save area.

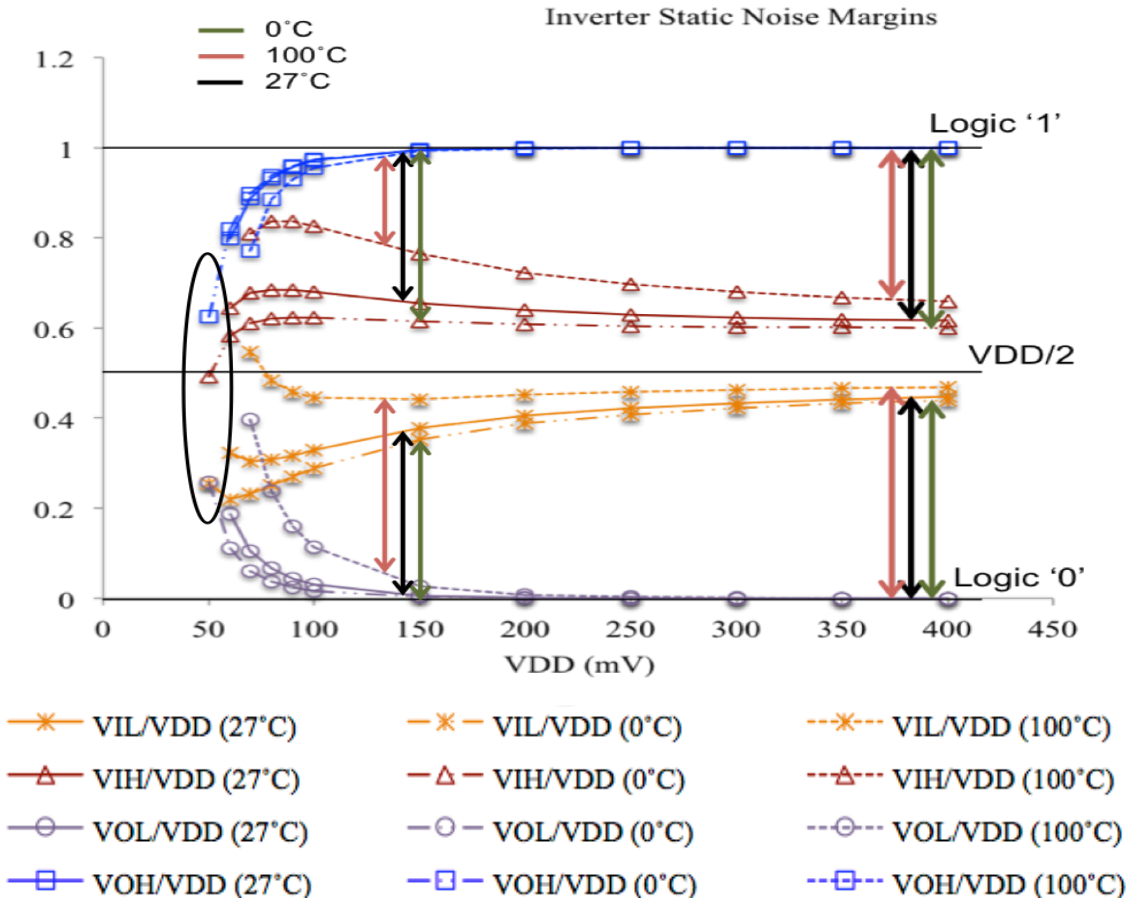


Figure 3: The impact that temperature fluctuations have on device SNMs between *VDD*=50mV and *VDD*=400mV. Normalized VIL, VOL, VIH, and VOH are plotted against supply voltage here. Normalization is with respect to *VDD* as shown in the legend. Note the significance of the variation in SNMs between operation at 0˚C, 27˚C, and 100˚C, particularly at lower supply voltages. According to nominal simulation, a circuit running at 0˚C can operate as low as 50mV, lower than for 27˚C and 100˚C.

CHAPTER 2

DEEP NANOSCALE FDSOI FOR ULP OPERATION

Due to the high amount of power consumed by bulk CMOS circuit implementations, alternative transistor designs have been introduced in recent years. Multi-gate devices, like FinFETs are one route that has shown great promise in offering better performance and power consumption for ICs at smaller technology nodes. Another technology is Silicon on Insulator (SOI). SOI devices have a layer of silicon dioxide (SiO_2) right beneath the surface of the device. This is referred to as the buried oxide (BOX). SOI technologies can either be Partially Depleted (PD) or Fully Depleted (FD). The difference is in the depth of the BOX layer [10]. The BOX layer for an FDSOI device is typically less than 50nm and scales with the SOI device. The small scale of the BOX layer poses a manufacturing challenge associated with large-scale production of FDSOI MOSFETs. Figure 4 (a) shows the structure of a typical bulk CMOS transistor and Figure 4 (b) shows the structure of an FDSOI transistor. Due to its modified structure, biasing FDSOI devices is called “back-gate biasing” instead of “body biasing”.

The most common way to balance circuits conventionally is by increasing the width of p-type devices (e.g. the 2-to-1 or 3-to1 “rule of thumb” pMOS to nMOS sizing for CMOS inverters). However, especially in sub-VT, as devices become smaller the imbalance becomes much more significant, so that the widths of PUN devices must be upsized much more than for super-VT. Figure 5 (a) shows that even when sizing PDN devices 4 times minimum size, PUN devices must still be

sized 8 times that of PDN devices. Moreover, Figure 5 (b) shows that in order to balance your circuit with PDN devices only 2 times minimum size, PUN devices must be upsized by 17 times their PDN counterparts. This requires a tremendous sacrifice in area and can also increase leakage power. Back-gate biasing allows you to control the threshold voltage in FDSOI devices, and serves as an alternate knob for controlling circuit balance. [11] discusses the benefits of FDSOI technology and its optimality for sub-VT in greater detail.

FDSOI As Optimal for Sub-VT

FDSOI technology has a number of advantages over standard bulk CMOS, including reduced stack effect and negligible drain to substrate capacitance [10]. Static noise margins for the inverter exist down to 60mV for this technology. [11] describes the advantages of using FDSOI for ULP applications in greater detail.

Back-Gate Bias for Balanced Sub-VT Circuits

Balance becomes all the more important in FDSOI technology where there is an increase in threshold voltage variation due to the dependence of threshold voltage on the BOX thickness, and the inevitable variation in wafer thickness [10]. The FDSOI biasing mechanism, called back-gate biasing, serves as a knob to tune threshold voltage, much like body biasing in bulk MOSFETs. Back-gate biasing offers much more flexibility than bulk CMOS body biasing. Unlike bulk MOSFETs, FDSOI MOSFETs allow a wide range of bias voltages to be applied without concern for energy or capacitance parasitics [12]. This offers a knob to improve

performance where desired or to improve robustness for lower performance applications.

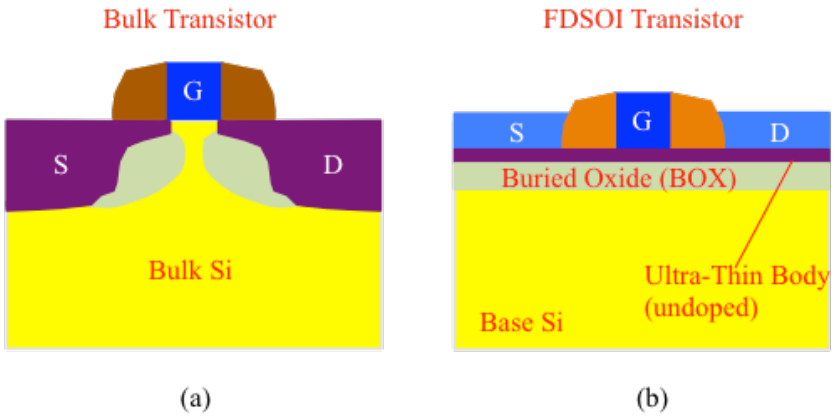


Figure 4: (a) Bulk CMOS transistor and (b) FDSOI transistor (based on [18])

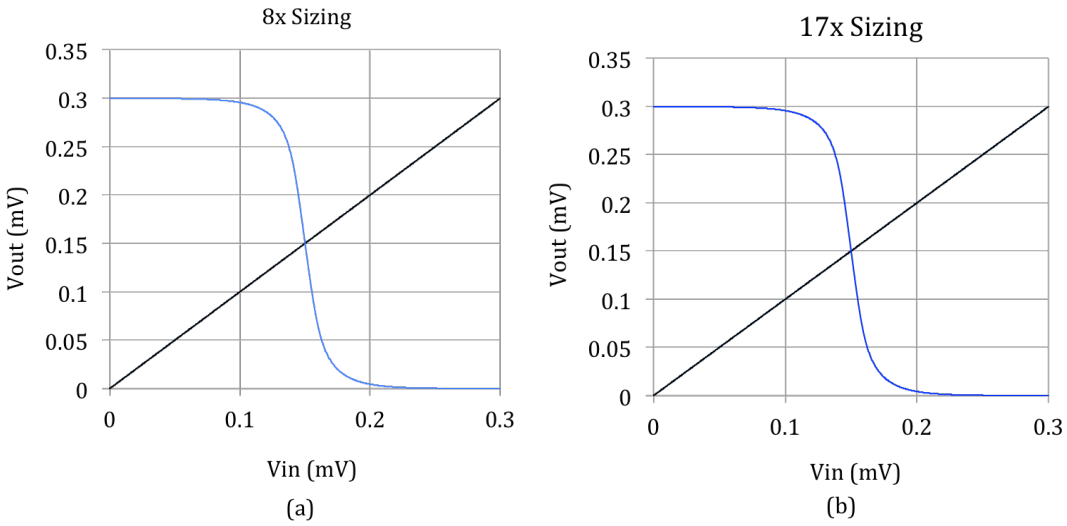


Figure 5: VTC's at VDD=300mV for an inverter balanced by sizing up the PUN. In (a), n-type devices are 4x minimum size. To balance the inverter here, p-type devices must be sized 8x that of n-type devices, meaning they must be sized 32x minimum size. In (b), n-type devices are 2x minimum size. To balance the inverter here, p-type devices must be sized 17x that of n-type devices, meaning they must be sized 34x minimum size.

CHAPTER 3

MUX-BASED LOGIC FOR PUN AND PDN SYMMETRY

As discussed in the previous chapters there are a variety of ways to balance a design depending on the environmental and design-based factors involved. In the following sections multiplexer (mux) -based logic design is motivated and the use of binary decision diagrams (BDDs) as a synthesis tool is explained. The two ways in which this work explores symmetry will also be discussed. The first way is in design or circuit topology. The exploration of a symmetric multiplexer gate design, a "mirror mux", is discussed as optimal for variation-tolerance in sub-VT. The second way in which balance is explored is from an adaptability standpoint. From this it is determined that there exists a linear relationship between the bias required to balance a design and the operating temperature.

Mux-Based Logic Design and BDDs

The Shannon Expansion Theorem

In 1938, Claude Shannon proposed what is today referred to as the Shannon Expansion [16]. The Shannon Expansion Theorem states that given any Boolean function and any of its inputs, that function can be expressed as follows [18]:

$$F(x_1, x_2, \ldots, x_i, \ldots, x_n) = x_i F(x_i = 1) + x_i' F(x_i = 0) \quad (3)$$

where F is some Boolean function, n is the total number of inputs to F, and x_i is some input to function F. This relationship creates a way to manipulate arbitrarily complex combinational logic. Moreover, (3) shows clearly that the Shannon

Expansion Theorem is highly compatible with mux-based logic design. Arbitrary combinational logic can easily be expressed as a mux-based implementation using the given relationship. This is an extremely valuable tool for debugging complex circuits, as a mux can behave like any logic gate simply by changing its inputs. Because of their flexibility as logic gates, muxes are also commonly used for programmable applications, like Field Programmable Gate Arrays (FPGAs). Shannon's Expansion also laid the groundwork for BDDs and Boolean satisfiability solvers.

BDDs for Logic Synthesis

BDDs were first proposed in [17]. They are a means of defining the functionality of a given circuit such that the design can be verified with computational tools. Much like Shannon's Expansion, this allows for analysis of arbitrarily complex circuits. The BDD is produced by looking at the inputs to a function and determining all possible outputs. By this process, a tree-like structure can be generated and used as a functional description. Thus, any arbitrary combinational logic can be mapped to a BDD. [19] takes this further to say that each node of the BDD can then in turn be mapped to a 2-to-1 mux. Moreover, logic sub-blocks can easily be combined with a BDD-based (i.e. mux-based) implementation. BDDs are therefore used for a number of applications, including CAD and verification tools, as well as heuristics for solving Boolean satisfiabilty.

Sizing and Topology

In this section the topology for the mirror mux is presented. A number of sizing options are explored and findings are discussed.

Topology

The mirror mux design is illustrated in Figure 2 (c). Note the symmetry between the PUN and PDN. This design promotes variation-tolerance because it has equivalent stacked and parallel transistors. Since the effects from stacked and parallel transistors are amplified in sub-VT, this is an important characteristic for ULP circuit design. It is shown later on that this design is in some cases optimal for very-low-voltage operation.

Sizing

PDN devices are sized 4 times minimum size. pMOS devices are sized twice that of the nMOS, as is typical, and sizing for stacks is also accounted for. Gates are balanced using back bias instead of using sizing ratio, opting to size four times the minimum for PDN devices because it struck the best balance between area and bias voltage. From this point forward the width used for PDN devices will be referred to as "minimum sized". Six sizing options are explored for the mux within the standard 2:1 ratio, all having the same overall area. These sizing options are illustrated in Figure 6.

The first option tested is all PDN devices sized the same, twice minimum size for the stack and PUN devices all sized the same, twice that of PDN devices, accounting for the stack (Figure 6 (c)). The next option and the option ultimately found to offer the most robustness to variations is the one in Figure 6 (a) where the

data inputs are sized larger than the select inputs. The third option tried is the sizing shown in Figure 6 (b), where the select inputs are sized larger than the data inputs. Each of these combinations is also tried with the select inputs on the inner transistors instead of the outer shown in Figures 6 (d) through (f). Placing the select inputs on the outside was found to provide better leakage control, which is why the design shown in Figure 6 (a) was ultimately chosen.

As stated, the sizing in Figure 6 (a) represents the sizing found to be optimal in terms of variation-tolerance. This can likely be attributed to the leakage paths closest to ground being smaller. It is worth noting that in terms of performance, the sizing combination selected is suboptimal, however, the aim of this work is improved stability, not performance. Results from this analysis are shown in Figure 7. Figure 8 will be explained in greater detail in a later section.

Back-Gate Biasing Scheme

FDSOI back-gate biasing is utilized instead of sizing to tune the metastable voltage of an inverter to balance the drive currents of the pMOS and nMOS devices. This is done by selecting the bias that gives the inverter a metastable voltage, V_M, of $VDD/2$. The pMOS and nMOS are biased with equal voltages to allow for greater simplicity in the design space.

Mirror Mux Characterization with Additional Input

In order to best characterize the mirror mux design, it is evaluated while varying the non-selected data input called B. This is also a technique used to determine the

qualities that promote variation-tolerance. Figure 7 shows the impact of the B input on SNMs at 0˚C, 27˚C, and 100˚C for the sizing schemes illustrated in Figure 6. Figure 8 displays the results from the performance analysis conducted on a 49-gate ring oscillator (RO) made from mirror muxes, illustrating that Figure 6 (a) provides the most stable signal, while Figure 6 (b) provides the least stable but highest frequency signal.

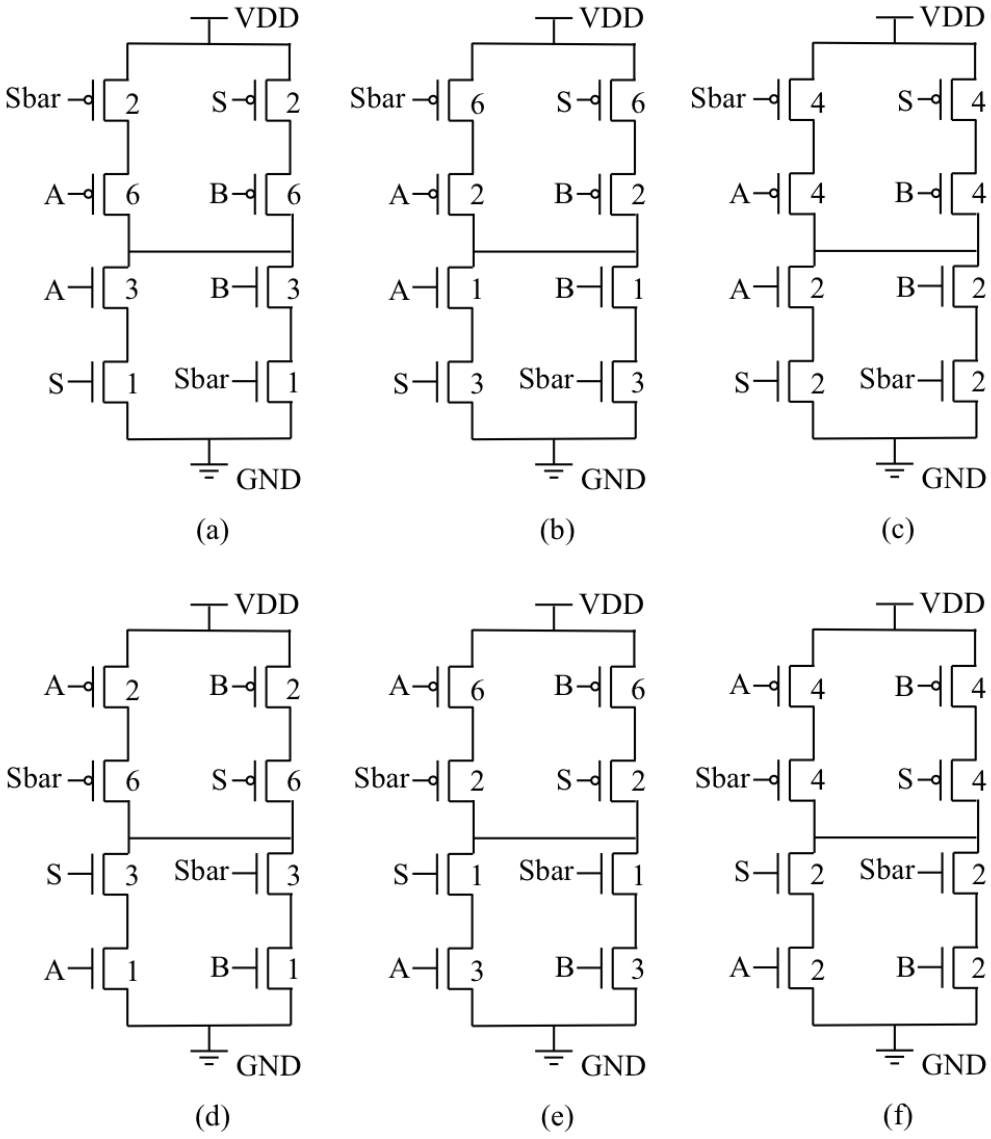
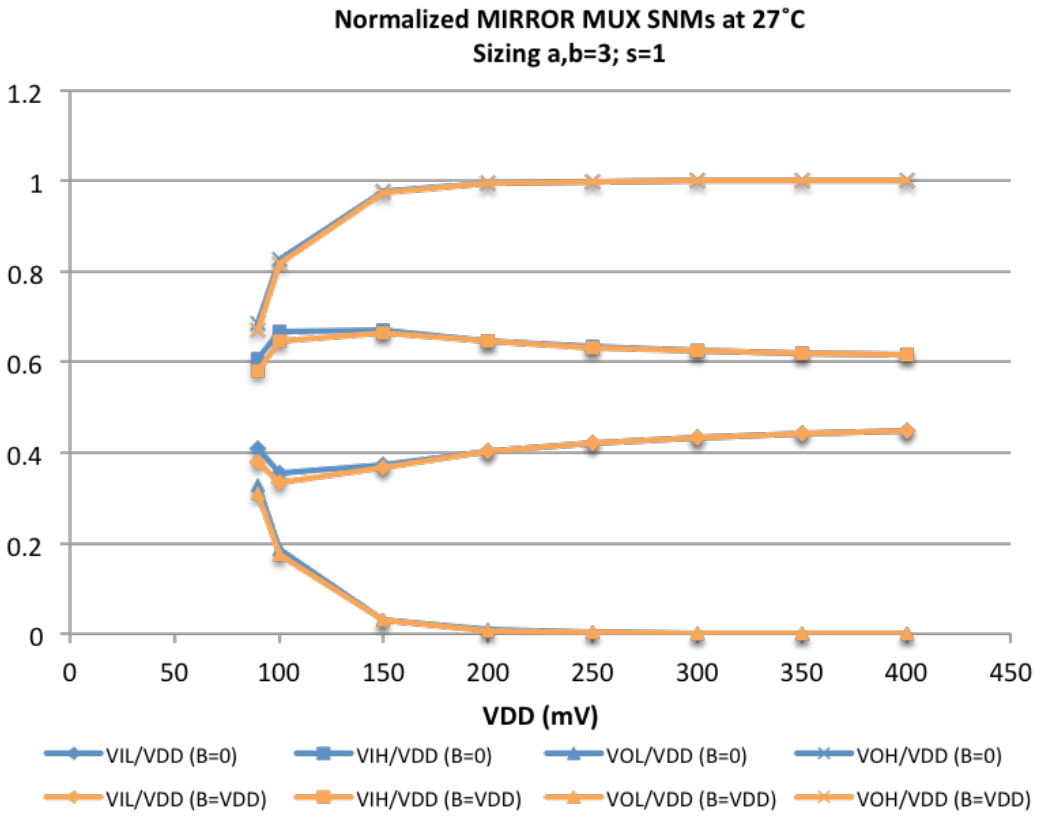
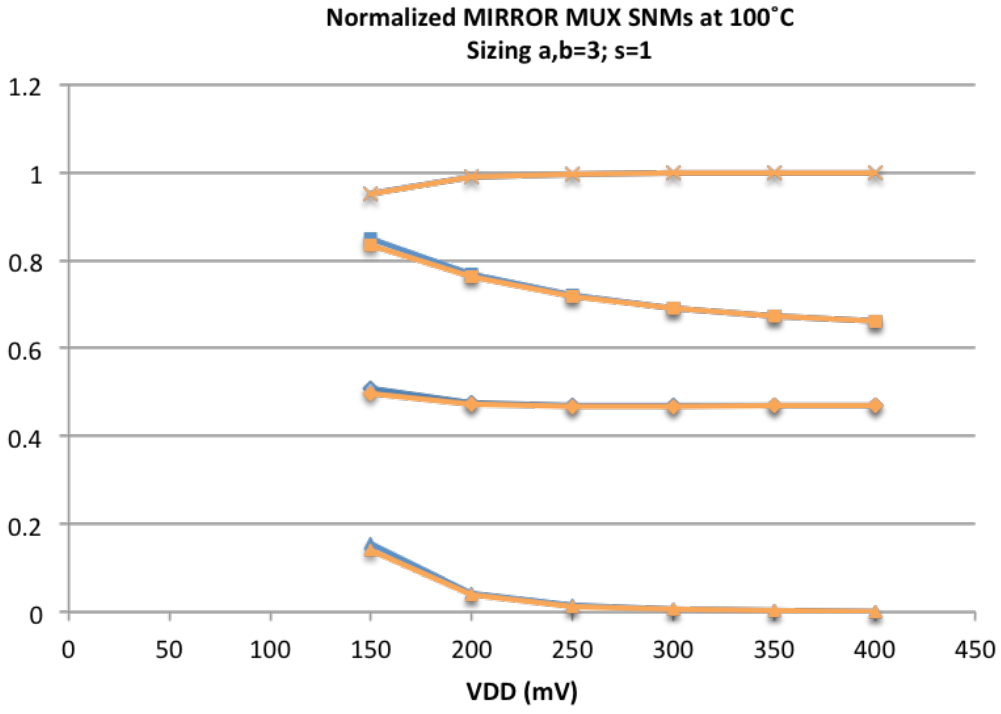


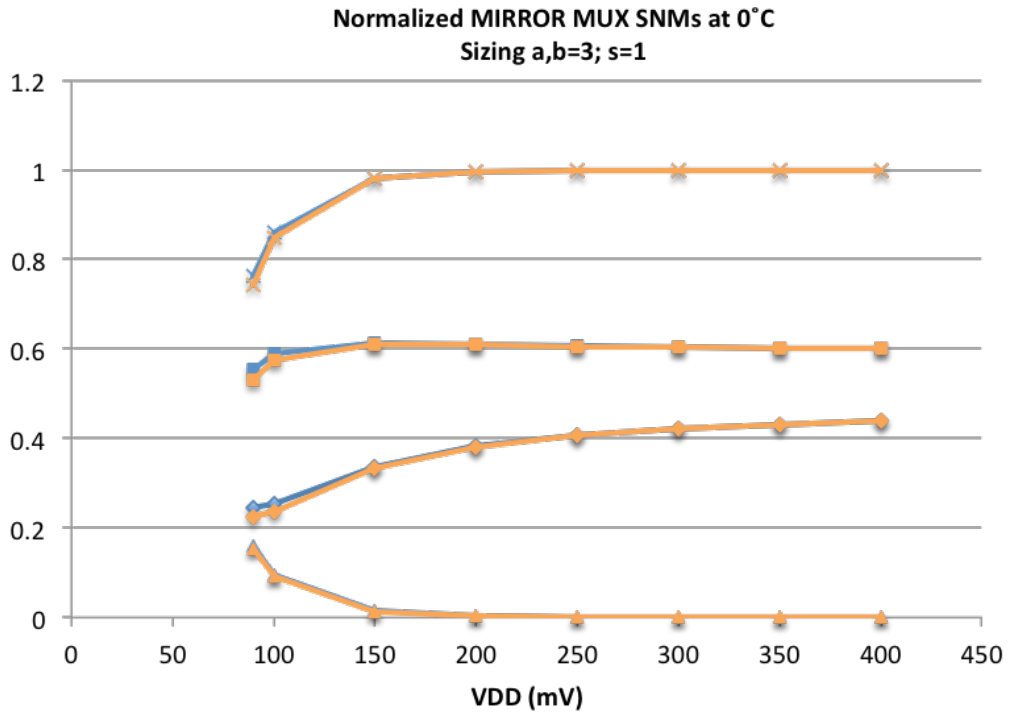
Figure 6: The sizing schemes explored for the mirror mux. (a) shows the sizing found to be most robust in terms of frequency stability and overall circuit reliability. It is worth noting that the sizing shown in (b) provides a higher average frequency and the sizing shown in (c) provides the best balance between reliability and frequency. However, the aim of this work is improved stability, not performance, so this study was conducted using (a).


Normalized MIRROR MUX SNMs at 27˚C
Sizing a,b=3; s=1
1.2
1
0.8
0.6
0.4
0.2
0
0
50
100
150
200
250
300
350
400
450
VDD (mV)
VIL/VDD (B=0)
VIH/VDD (B=0)
VOL/VDD (B=0)
VOH/VDD (B=0)
VIL/VDD (B=VDD)
VIH/VDD (B=VDD)
VOL/VDD (B=VDD)
VOH/VDD (B=VDD)

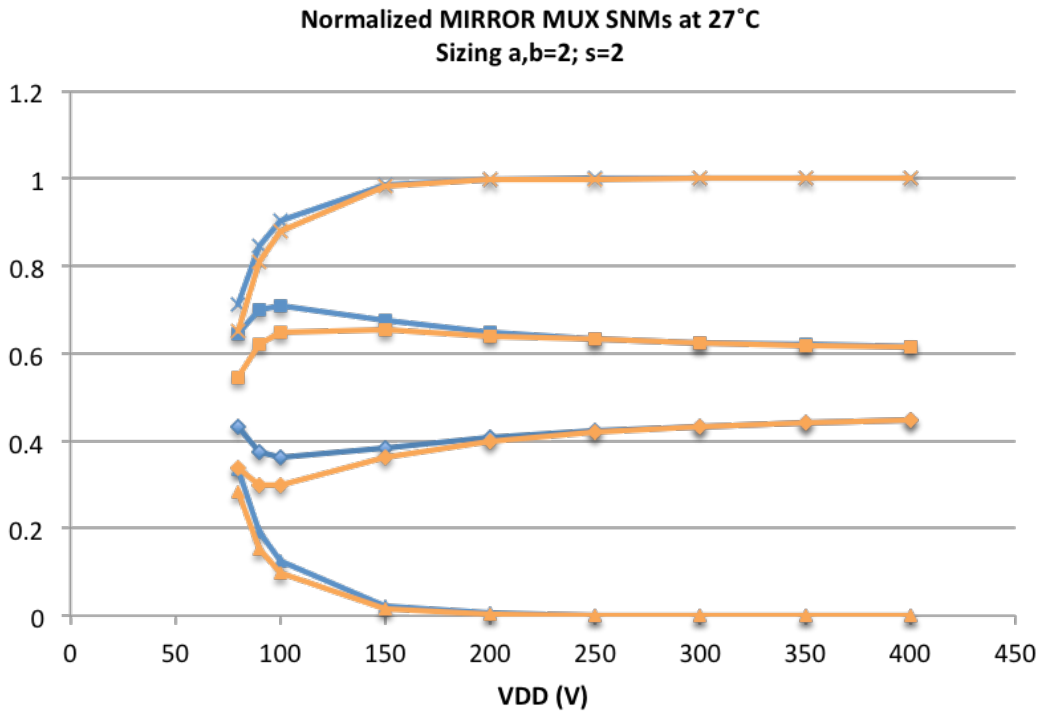
(a)


Normalized MIRROR MUX SNMs at 100˚C
Sizing a,b=3; s=1
1.2
1
0.8
0.6
0.4
0.2
0
0
50
100
150
200
250
300
350
400
450
VDD (mV)

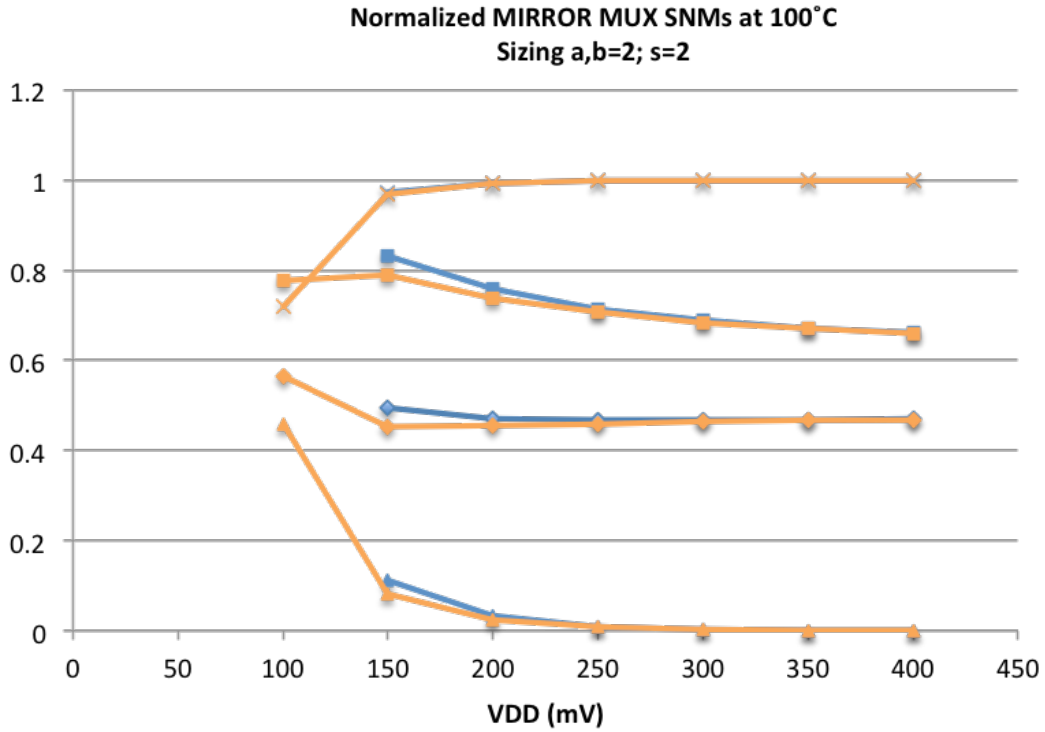
(b)


Normalized MIRROR MUX SNMs at 0˚C
Sizing a,b=3; s=1
1.2
1
0.8
0.6
0.4
0.2
0
0
50
100
150
200
250
300
350
400
450
VDD (mV)

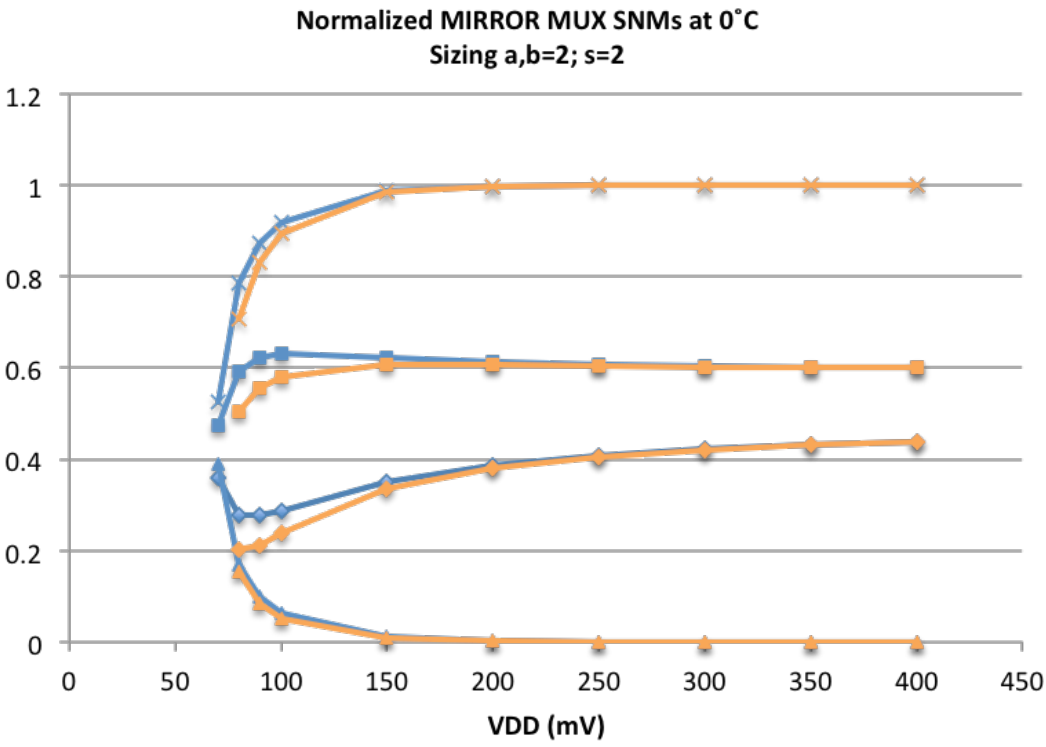
(c)


Normalized MIRROR MUX SNMs at 27˚C
Sizing a,b=2; s=2
1.2
1
0.8
0.6
0.4
0.2
0
0
50
100
150
200
250
300
350
400
450
VDD (V)

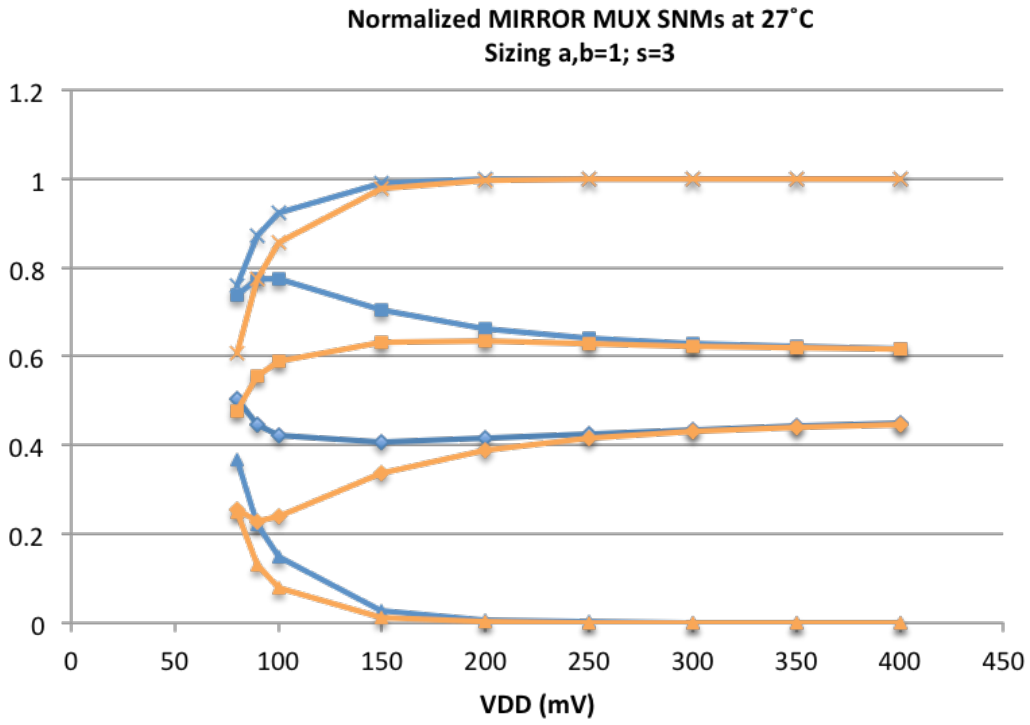
(d)


Normalized MIRROR MUX SNMs at 100˚C
Sizing a,b=2; s=2
1.2
1
0.8
0.6
0.4
0.2
0
0
50
100
150
200
250
300
350
400
450
VDD (mV)

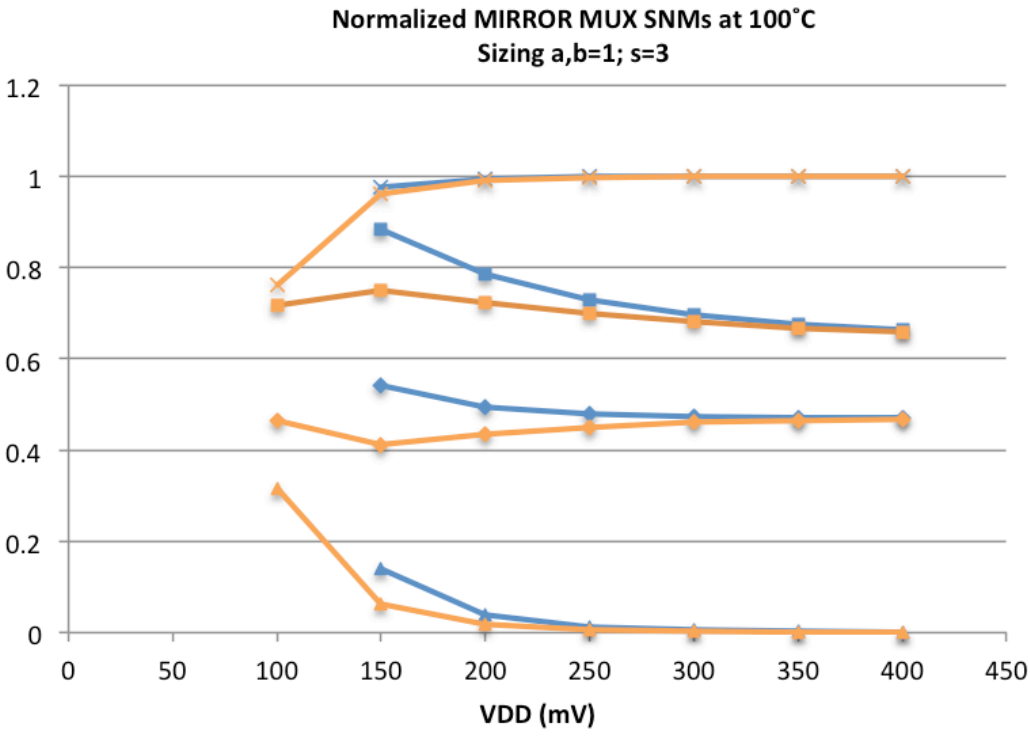
(e)


Normalized MIRROR MUX SNMs at 0˚C
Sizing a,b=2; s=2
1.2
1
0.8
0.6
0.4
0.2
0
0
50
100
150
200
250
300
350
400
450
VDD (mV)

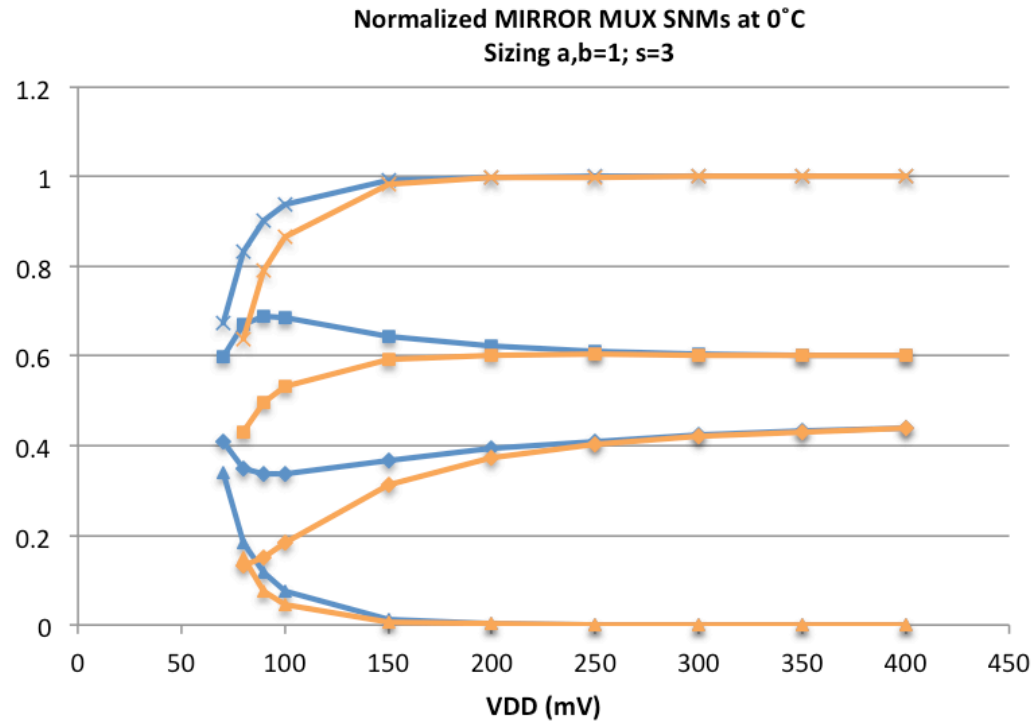
(f)


Normalized MIRROR MUX SNMs at 27˚C
Sizing a,b=1; s=3
1.2
1
0.8
0.6
0.4
0.2
0
0
50
100
150
200
250
300
350
400
450
VDD (mV)

(g)


Normalized MIRROR MUX SNMs at 100˚C
Sizing a,b=1; s=3
1.2
1
0.8
0.6
0.4
0.2
0
0
50
100
150
200
250
300
350
400
450
VDD (mV)

(h)



(i)

Figure 7: Normalized mirror mux SNMs for sizing schemes. The legend in (a) applies to (a)-(i). (a), (d), and (g) correspond to Figure 6 (a) at 27˚C, 100˚C, and 0˚C, respectively. (b), (e), and (h) correspond to Figure 6 (c) at 27˚C, 100˚C, and 0˚C, respectively. (c), (f), and (i) correspond to Figure 6 (b) at 27˚C, 100˚C, and 0˚C. Note the extreme impact that varying the other input B has on (c) as compared to (a). This effect holds for extreme high and low temperatures, as shown in (d)-(f) and (g)-(i), respectively.

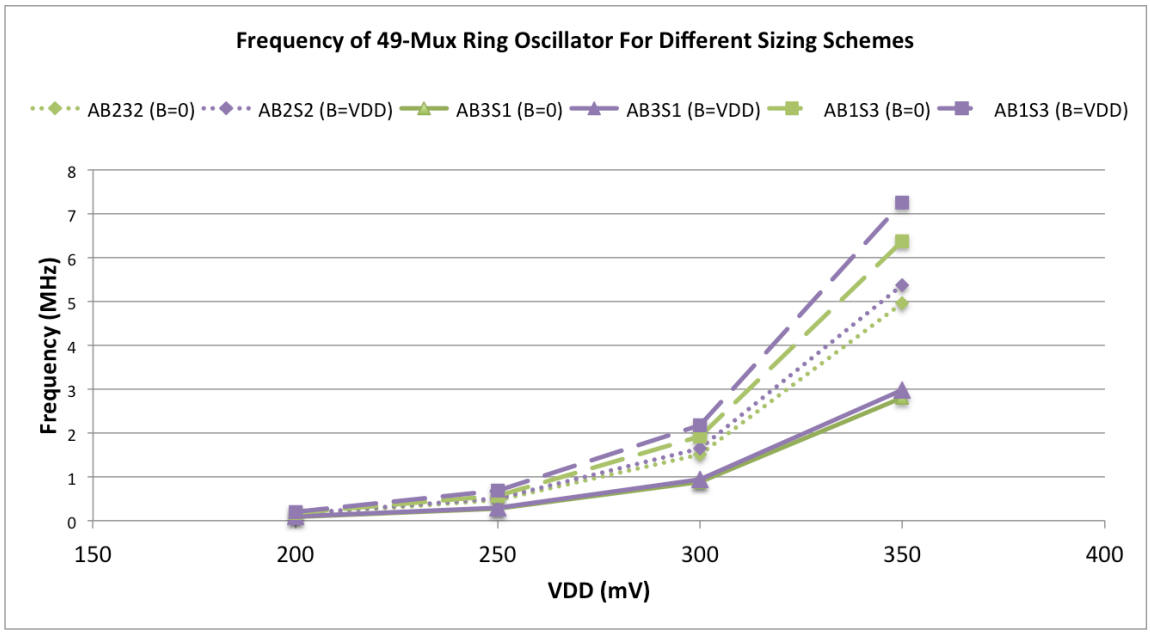


Figure 8: Frequencies generated from nominal simulation of a 49-stage mirror mux ring oscillator. Note the difference in frequency between B=0 and B=VDD. The topology we selected was the one with the least variation in frequency from changing the B-input. The trade-off between frequency and stability is illustrated here.

CHAPTER 4

SYMMETRY RESULTS

In this chapter, the results from noise-analysis and MC simulations are presented. Simulations are run for temperatures between -55°C and 125°C, the military standard for device robustness to temperature.

Static Results and Linear Correlation

To evaluate the steady-state behavior of this methodology, 1000-point MC simulations are conducted for symmetrically functioning designs at -55˚C, 27˚C, and 125˚C, and then for imbalanced designs that do not utilize the biasing scheme. The voltage transfer characteristic (VTC) curve of a basic inverter gate is balanced for a number of supply voltages and temperatures. A VTC is defined as balanced for metastable voltages of exactly half the supply voltage, V_M=$VDD/2$. The bias voltages for -55˚C, 0˚C, 27˚C, and 125˚C are measured. The results from this analysis for a supply voltage of 300mV are presented in Figure 9. The linear relationship between bias voltage and temperature illustrated in Figure 10 is the basis for the proposed biasing scheme. The linear relationship allows extrapolation between sampled temperatures and even potentially beyond. This relationship holds for temperatures as low as -100˚C and for supply voltages as low as 50mV, well beyond existing inverter SNMs according to nominal simulations. From this the relationship between temperature, supply voltage, and bias voltage was derived:

$$V_{bias}\,(\text{mV}) = 2.6T + 0.56V_{DD} - 451 \qquad (4)$$

where T is the temperature in degrees Celsius and V_{DD} is the supply voltage in millivolts at which your design operates.

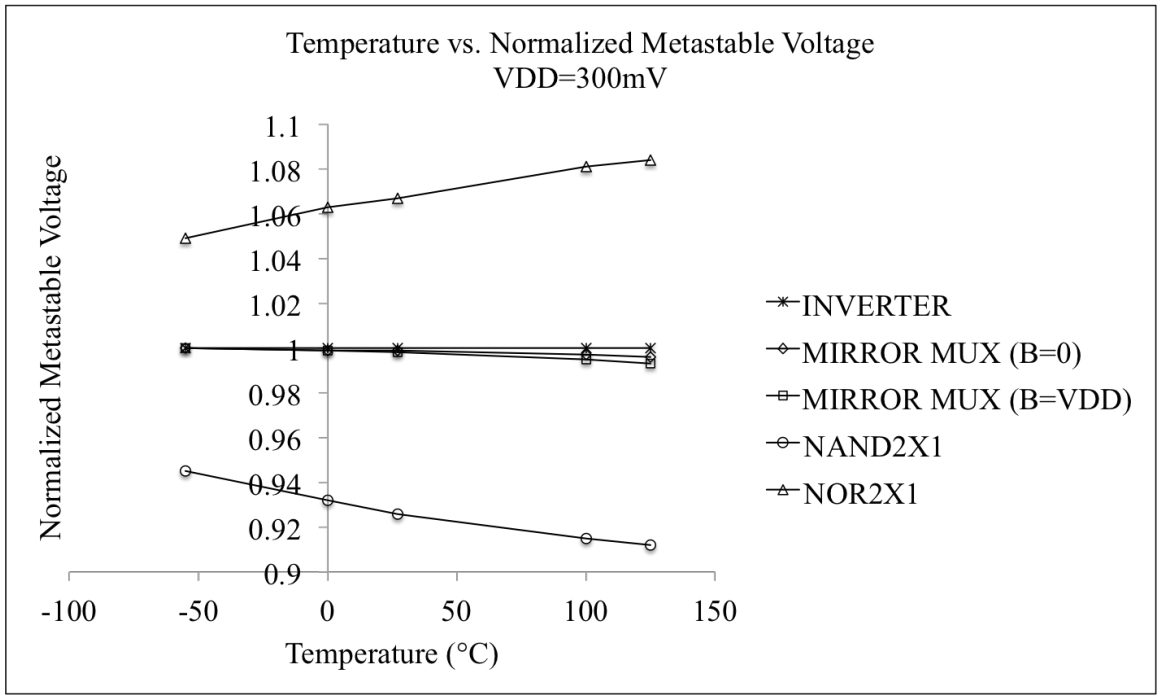


Figure 9: The normalized metastable voltage (V_M) plotted against temperature for 2-input NAND and NOR gates and the mirror mux for both B=0 and B=VDD. The gates are normalized with respect to the balanced inverter's V_M, which for *VDD*=300mV is 150mV.

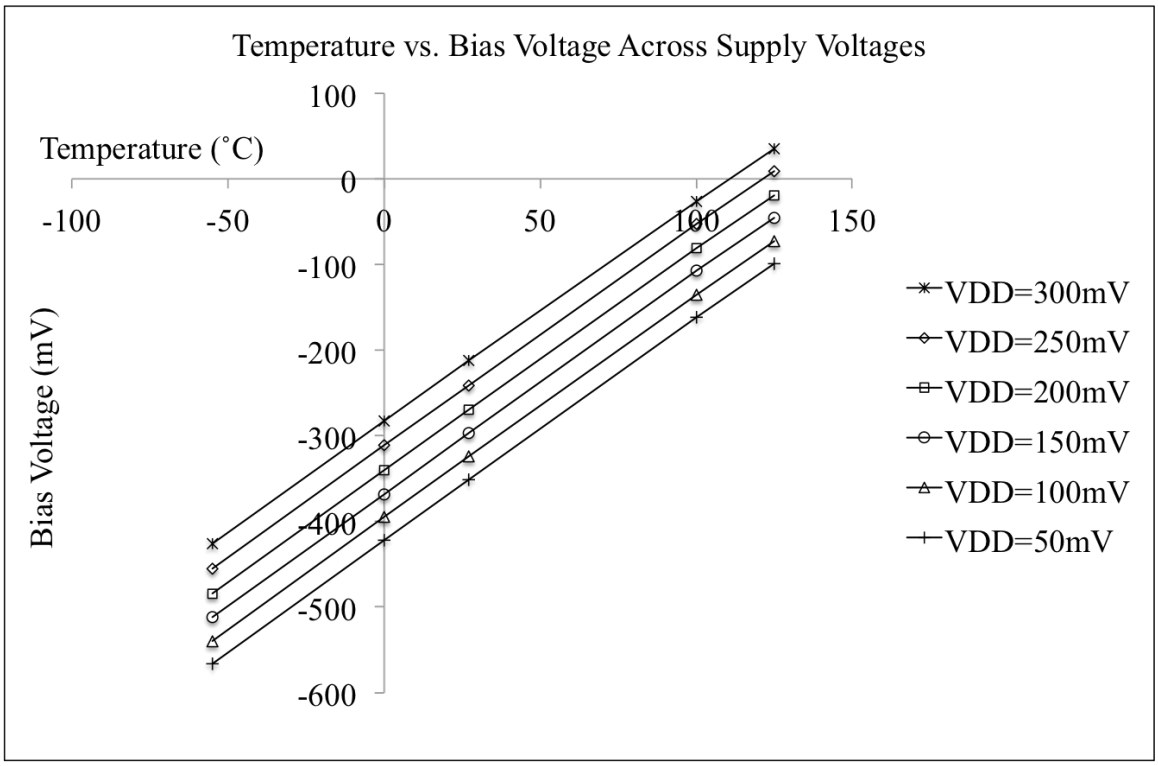
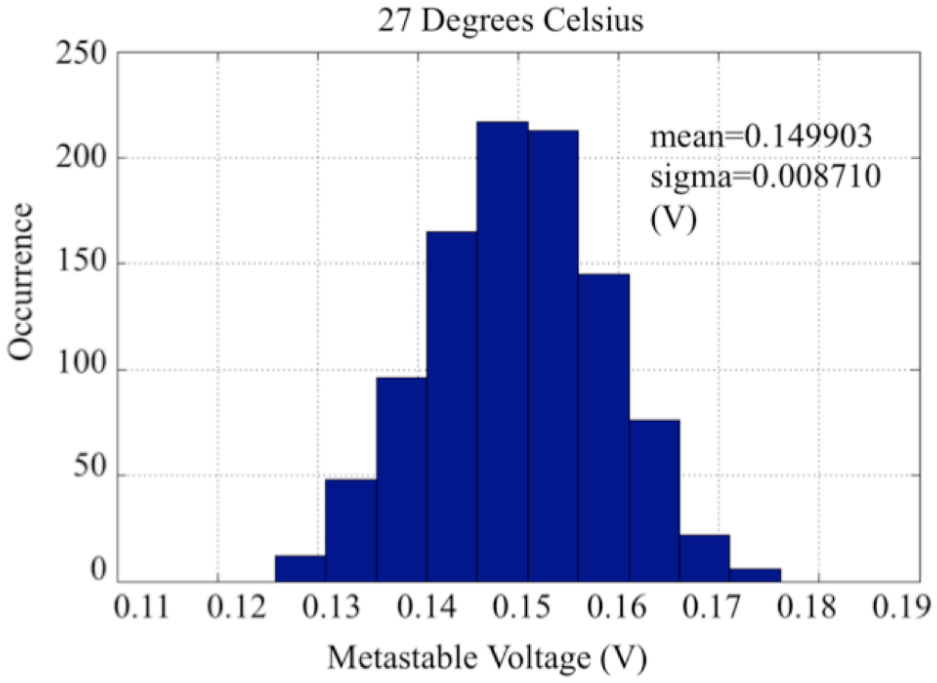
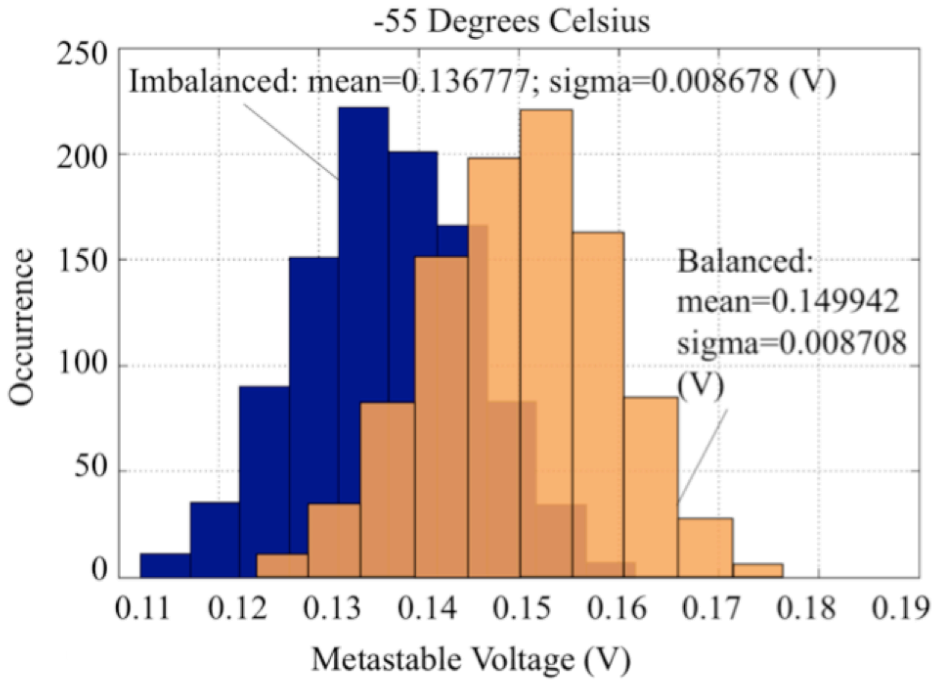


Figure 10: The linear relationship between temperature and bias voltage for a given supply voltage can be expressed as V_{bias} (mV) = $2.6T + 0.56V_{DD} - 451$. The bias voltage here is the bias voltage at which the metastable voltage, V_M=$V_{DD}/2$. This is the point at which the PUN and PDN are balanced.

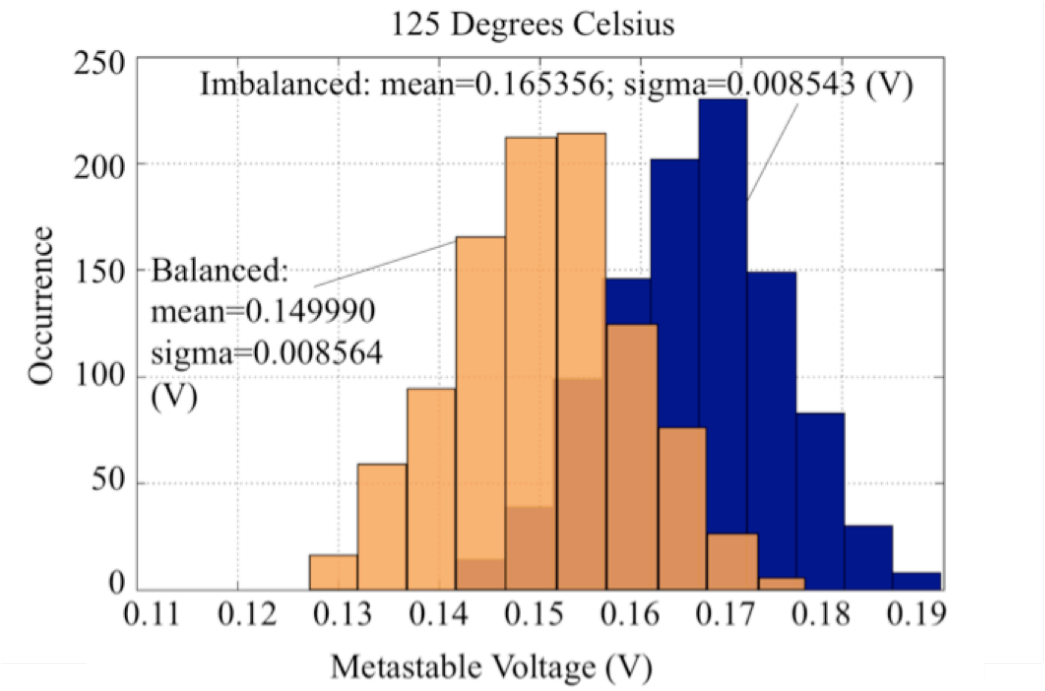
The results from MC analysis are illustrated in Figure 11. Note how the balanced bias voltage shifts the distribution of metastable voltages so that it is centered over $VDD/2$. While the standard deviation of the distribution does not seem to be heavily impacted by the threshold voltage shift, from the mean it is clear that the distributions employing the proposed biasing scheme are much more balanced than their counterparts employing use of a universal bias voltage. In the next section, impacts on circuit functionality are discussed, including frequency, leakage and active power, and minimum supply voltage.


27 Degrees Celsius
mean=0.149903
sigma=0.008710
(V)
Occurrence
Metastable Voltage (V)
0
50
100
150
200
250
0.11
0.12
0.13
0.14
0.15
0.16
0.17
0.18
0.19

(a)


-55 Degrees Celsius
Imbalanced: mean=0.136777; sigma=0.008678 (V)
Balanced:
mean=0.149942
sigma=0.008708
(V)
Occurrence
Metastable Voltage (V)
0
50
100
150
200
250
0.11
0.12
0.13
0.14
0.15
0.16
0.17
0.18
0.19

(b)



(c)

Figure 11: Plots showing the distribution of the metastable voltage for an inverter at an operating voltage of 300mV from 1000-point MC simulations. (a) shows the distribution at nominal temperature (27˚C), (b) shows the distributions for balanced and imbalanced cases at -55˚C, and (c) shows the distributions for the balanced and imbalanced cases at 125˚C. For the imbalanced cases, the bias voltage is set to -212mV, the voltage at which the inverter VTC is balanced at room temperature (27 degrees Celsius), and the temperature is raised up to 125 degrees Celsius and down to -55 degrees Celsius. Note the imbalanced cases share a similar standard deviation to the balanced cases but their distributions are not centered over *VDD*/2 as the balanced results.

Transient Results

Transient analyses conducted include frequency, active power, and leakage power on 49-stage ROs consisting of inverters, 2-input NAND and NOR gates, and the inverting mirror mux topology. 100-point MC simulations are run in order to gain some insight into the impacts of variation on this methodology. This section presents statistical data with respect to frequency, active power, and leakage power

from HSPICE simulations of MC with both random process and mismatch variations. Presented here also is an analysis of the minimum supply voltage for cases where the circuit is balanced with V_{bias} and cases where it is imbalanced attained with nominal simulation.

MC results show the mirror mux has the lowest standard deviation in frequency across temperatures of gates tested in both imbalanced and balanced cases. It is found that at 125˚C and *VDD*=150mV, for the case where the mirror mux alternate input, B=VDD, 7 out of 100 MC runs fail for the imbalanced case. Moreover, when B=0, 18 out of 100 MC runs fail for the imbalanced case. The topologies that are balanced do not fail at 125˚C. In general, topologies that are not balanced have much higher minimum supply voltages than those that are balanced. Balancing the gates also increases RO frequency and, in some cases, decreases power consumption of ROs. The mirror mux also consumes the least amount of active power, even less than the inverter.

Tables 1, 2, and 3 show the standard deviations and mean of the RO frequencies at *VDD*=300mV for the gates tested. Tables 4, 5, and 6 show the standard deviations and means of the RO frequencies at *VDD*=150mV. It can be seen here that the mirror mux offers the most stable frequency of all the gates, which is an important characteristic for clock generation. Key values are highlighted in light gray. Tables 7-18 show the distributions of total, active, and leakage power for *VDD*=150mV and *VDD*=300mV. The mux has the highest leakage of the topologies. This is a curious characteristic of the topology, as stacking transistors is typically a method used for leakage control. However, it must be noted that while the mirror

mux does have more stacked transistors than its NAND and NOR counterparts, which should improve leakage, it also has more parallel paths. Therefore, the large amount of leakage can likely be attributed to the smaller effective resistance through the gate due to the presence of more parallel paths. The mux, in general has the lowest power consumption at a supply voltage of 300mV, though at high temperatures this no longer holds. This also ceases to hold at lower supply voltages, as can be seen in Tables 13-18.

Table 1: Distribution of Frequencies at -55˚C and *VDD*=300mV

	Balanced		Imbalanced	
Gate	StdDev (Hz)	Mean (Hz)	StdDev (Hz)	Mean (Hz)
INVERTER	2.67E+04	9.67E+04	2.35E+04	8.49E+04
MIRROR MUX B=0	5.185E+03	1.838E+04	4.562E+03	1.545E+04
MIRROR MUX B=VDD	5.476E+03	1.907E+04	4.721E+03	1.586E+04
NAND2X1	1.970E+04	6.847E+04	1.799E+04	6.248E+04
NOR2X1	1.451E+04	4.975E+04	1.302E+04	4.317E+04

Table 2: Distribution of Frequencies at 125˚C and *VDD*=300mV

	Balanced		Imbalanced	
Gate	StdDev (Hz)	Mean (Hz)	StdDev (Hz)	Mean (Hz)
INVERTER	4.79E+06	4.68E+07	4.83E+06	4.58E+07
MIRROR MUX B=0	1.01E+06	1.01E+07	9.795E+05	9.787E+06
MIRROR MUX B=VDD	1.068E+06	1.073E+07	1.071E+06	1.051E+07
NAND2X1	3.309E+06	3.363E+07	3.249E+06	3.215E+07
NOR2X1	2.341E+06	2.349E+07	2.349E+06	2.278E+07

Table 3: Distribution of Frequencies at 27˚C and *VDD*=300mV

Gate	StdDev (Hz)	Mean (Hz)
INVERTER	6.29E+05	3.68E+06
MIRROR MUX B=0	1.30E+05	7.52E+05
MIRROR MUX B=VDD	1.38E+05	7.95E+05
NAND2X1	4.494E+05	2.621E+06
NOR2X1	3.215E+05	1.856E+06

Table 4: Distribution of Frequencies at -55˚C and *VDD*=150mV

	Balanced		Imbalanced	
Gate	StdDev (Hz)	Mean (Hz)	StdDev (Hz)	Mean (Hz)
INVERTER	1.93E+02	5.78E+02	1.76E+02	5.23E+02
MIRROR MUX B=0	4.26E+01	1.26E+02	3.94E+01	1.14E+02
MIRROR MUX B=VDD	4.52E+01	1.33E+02	4.10E+01	1.17E+02
NAND2X1	1.47E+02	4.19E+02	1.40E+02	3.90E+02
NOR2X1	1.04E+02	2.94E+02	9.82E+01	2.67E+02

Table 5: Distribution of Frequencies at 125˚C and *VDD*=150mV

	Balanced		Imbalanced	
Gate	StdDev (Hz)	Mean (Hz)	StdDev (Hz)	Mean (Hz)
INVERTER	5.69E+05	4.20E+06	5.58E+05	4.08E+06
MIRROR MUX B=0	1.12E+05	8.53E+05	1.07E+05	7.91E+05
MIRROR MUX B=VDD	1.17E+05	8.96E+05	1.09E+05	8.40E+05
NAND2X1	3.98E+05	3.02E+06	3.72E+05	2.82E+06
NOR2X1	3.01E+05	2.21E+06	2.93E+05	2.15E+06

Table 6: Distribution of Frequencies at 27˚C and *VDD*=150mV

Gate	StdDev (Hz)	Mean (Hz)
INVERTER	2.27E+04	1.08E+05
MIRROR MUX B=0	4.96E+03	2.32E+04
MIRROR MUX B=VDD	5.25E+03	2.46E+04
NAND2X1	1.67E+04	7.80E+04
NOR2X1	1.21E+04	5.50E+04

Table 7: Distribution of Total Power at -55˚C and *VDD*=300mV

	Balanced		Imbalanced	
Gate	StdDev (W)	Mean (W)	StdDev (W)	Mean (W)
INVERTER	1.75E-10	6.35E-10	1.54E-10	5.56E-10
MIRROR MUX B=0	1.39E-10	4.89E-10	1.200E-10	4.110E-10
MIRROR MUX B=VDD	1.366E-10	4.805E-10	1.179E-10	4.021E-10
NAND2X1	1.886E-10	6.601E-10	1.757E-10	5.948E-10
NOR2X1	1.974E-10	6.769E-10	1.759E-10	5.832E-10

Table 8: Distribution of Total Power at 125˚C and *VDD*=300mV

	Balanced		Imbalanced	
Gate	StdDev (W)	Mean (W)	StdDev (W)	Mean (W)
INVERTER	5.05E-08	4.13E-07	5.24E-08	4.19E-07
MIRROR MUX B=0	9.64E-08	6.63E-07	1.05E-07	7.02E-07
MIRROR MUX B=VDD	9.507E-08	6.583E-07	1.048E-07	7.022E-07
NAND2X1	6.968E-08	5.313E-07	7.351E-08	5.416E-07
NOR2X1	6.829E-08	5.350E-07	7.099E-08	5.411E-07

Table 9: Average Active Power at *VDD*=300mV in Watts

Temperature (˚C)	-55		125	
Gate	Balanced	Imbalanced	Balanced	Imbalanced
INVERTER	6.20E-10	5.48E-10	2.96E-07	2.69E-07
MIRROR MUX B=0	4.73E-10	3.95E-10	2.71E-07	2.65E-07
MIRROR MUX B=VDD	4.65E-10	3.86E-10	2.70E-07	2.84E-07
NAND2X1	6.49E-10	5.83E-10	3.13E-07	3.00E-07
NOR2X1	6.66E-10	5.72E-10	3.26E-07	3.17E-07

Table 10: Distribution of Power at 27˚C and *VDD*=300mV

	Total		Active	Leakage	
Gate	StdDev (W)	Mean (W)	Mean (W)	StdDev (W)	Mean (W)
INVERTER	4.38E-09	2.49E-08	2.34E-08	4.020E-10	1.496E-09
MIRROR MUX B=0	4.57E-09	2.41E-08	1.98E-08	1.170E-09	4.312E-09
MIRROR MUX B=VDD	4.52E-09	2.38E-08	1.96E-08	1.135E-09	4.241E-09
NAND2X1	4.870E-09	2.698E-08	2.45E-08	7.056E-10	2.464E-09
NOR2X1	5.117E-09	2.830E-08	2.60E-08	6.330E-10	2.320E-09

Table 11: Distribution of Leakage Power at -55˚C and *VDD*=300mV

	Balanced		Imbalanced	
Gate	StdDev (W)	Mean (W)	StdDev (W)	Mean (W)
INVERTER	2.859E-12	1.536E-11	9.910E-13	8.272E-12
MIRROR MUX B=0	3.002E-12	1.581E-11	2.916E-12	1.578E-11
MIRROR MUX B=VDD	2.859E-12	1.536E-11	3.036E-12	1.606E-11
NAND2X1	1.972E-12	1.134E-11	1.970E-12	1.144E-11
NOR2X1	1.712E-12	1.070E-11	1.867E-12	1.111E-11

Table 12: Distribution of Leakage Power at 125˚C and *VDD*=300mV

	Balanced		Imbalanced	
Gate	StdDev (W)	Mean (W)	StdDev (W)	Mean (W)
INVERTER	2.108E-08	1.170E-07	2.715E-08	1.498E-07
MIRROR MUX B=0	7.003E-08	3.923E-07	7.938E-08	4.375E-07
MIRROR MUX B=VDD	6.859E-08	3.883E-07	7.491E-08	4.179E-07
NAND2X1	4.008E-08	2.187E-07	4.504E-08	2.419E-07
NOR2X1	3.695E-08	2.090E-07	4.031E-08	2.238E-07

Table 13: Distribution of Total Power at -55˚C and *VDD*=150mV

	Balanced		Imbalanced	
Gate	StdDev (W)	Mean (W)	StdDev (W)	Mean (W)
INVERTER	5.23E-13	2.61E-12	5.11E-13	2.58E-12
MIRROR MUX B=0	9.87E-13	4.52E-12	9.86E-13	4.51E-12
MIRROR MUX B=VDD	9.75E-13	4.45E-12	1.00E-12	4.56E-12
NAND2X1	7.70E-13	3.66E-12	7.60E-13	3.66E-12
NOR2X1	7.72E-13	3.52E-12	7.88E-13	3.51E-12

Table 14: Distribution of Total Power at 125˚C and *VDD*=150mV

	Balanced		Imbalanced	
Gate	StdDev (W)	Mean (W)	StdDev (W)	Mean (W)
INVERTER	7.70E-09	4.64E-08	8.33E-09	4.98E-08
MIRROR MUX B=0	2.43E-08	1.42E-07	2.88E-08	1.62E-07
MIRROR MUX B=VDD	2.40E-08	1.42E-07	2.74E-08	1.56E-07
NAND2X1	1.41E-08	8.18E-08	1.58E-08	8.98E-08
NOR2X1	1.36E-08	8.00E-08	1.46E-08	8.47E-08

Table 15: Average Active Power at *VDD*=150mV in Watts

Temperature (˚C)	-55		125	
Gate	Balanced	Imbalanced	Balanced	Imbalanced
INVERTER	8.60E-13	7.59E-13	6.37E-09	6.64E-09
MIRROR MUX B=0	7.70E-13	6.76E-13	5.90E-09	6.70E-09
MIRROR MUX B=VDD	7.65E-13	6.46E-13	5.80E-09	6.40E-09
NAND2X1	9.53E-13	8.84E-13	7.35E-09	7.40E-09
NOR2X1	9.48E-13	8.37E-13	6.43E-09	7.00E-09

Table 16: Distribution of Power at 27˚C and *VDD*=150mV

	Total		Active	Leakage	
Gate	StdDev (W)	Mean (W)	Mean (W)	StdDev (W)	Mean (W)
INVERTER	1.35E-10	5.58E-10	1.63E-10	1.03E-10	3.94E-10
MIRROR MUX B=0	3.72E-10	1.45E-09	1.57E-10	3.39E-10	1.30E-09
MIRROR MUX B=VDD	3.68E-10	1.45E-09	1.55E-10	3.35E-10	1.29E-09
NAND2X1	2.35E-10	9.05E-10	1.80E-10	2.01E-10	7.25E-10
NOR2X1	2.28E-10	8.84E-10	1.73E-10	1.89E-10	7.11E-10

Table 17: Distribution of Leakage Power at -55˚C and *VDD*=150mV

	Balanced		Imbalanced	
Gate	StdDev (W)	Mean (W)	StdDev (W)	Mean (W)
INVERTER	2.29E-13	1.75E-12	2.58E-13	1.82E-12
MIRROR MUX B=0	7.13E-13	3.75E-12	7.40E-13	3.83E-12
MIRROR MUX B=VDD	6.98E-13	3.69E-12	7.64E-13	3.91E-12
NAND2X1	4.50E-13	2.71E-12	4.67E-13	2.78E-12
NOR2X1	4.22E-13	2.57E-12	4.66E-13	2.67E-12

Table 18: Distribution of Leakage Power at 125˚C and *VDD*=150mV

	Balanced		Imbalanced	
Gate	StdDev (W)	Mean (W)	StdDev (W)	Mean (W)
INVERTER	7.06E-09	4.00E-08	7.63E-09	4.31E-08
MIRROR MUX B=0	2.36E-08	1.37E-07	2.78E-08	1.55E-07
MIRROR MUX B=VDD	2.33E-08	1.36E-07	2.68E-08	1.49E-07
NAND2X1	1.33E-08	7.44E-08	1.50E-08	8.24E-08
NOR2X1	1.26E-08	7.36E-08	1.36E-08	7.77E-08

CHAPTER 5

IMPLEMENTATION DETAILS AND APPLICATIONS

The Benefits of Symmetry in Layout

Symmetry in circuit design is not only important for circuit robustness, but also for physical implementation. With the small scale at which manufacturing now occurs, the more regularity the better, when it comes to designs. Etching on such a small scale makes precision difficult, and therefore, the more symmetric your design the lower the cost of manufacturing.

Mux-Based Design and Synthesis with BDDs

In order to utilize mux-based design a tool flow is proposed. The tool flow uses BDDs to synthesize arbitrary combinational logic into a mux-based hardware implementation. The flow is implemented using the CUDD package [13]. Figure 12 illustrates the flow. Beginning with a Verilog script, ODIN II, a component of VPR [14], an FPGA synthesis tool, is used to convert the Verilog to Berkeley Logic Interchange Format (BLIF), the input file type for CUDD. CUDD is then used to convert arbitrary logic into a mux-based implementation. The output file is BLIF format and therefore needs to be converted to Verilog using ABC [20]. A top-level design synthesis is attainable using commercial EDA tools.

As a test case, the ISCAS ’89 c17 benchmark circuit is taken through the flow. The typical implementation of this circuit is illustrated in Figure 13. Figure 14 shows top-level synthesis of the Verilog code associated with c17. Figure 15 shows

the mux-based implementation generated by top-level synthesis. Implementing the mux-based design for this circuit requires two additional inputs that are held constant—one is tied to ground and the other is tied to VDD. The area of the mux-based design is about three times that of the non-mux design, and the delay is just under three times that of the non-mux design. However, it should be noted that the top-level synthesis tool inserts a number of unnecessary buffers into the design. If these were removed, the area and delay of the mux-based design would decrease quite a bit.

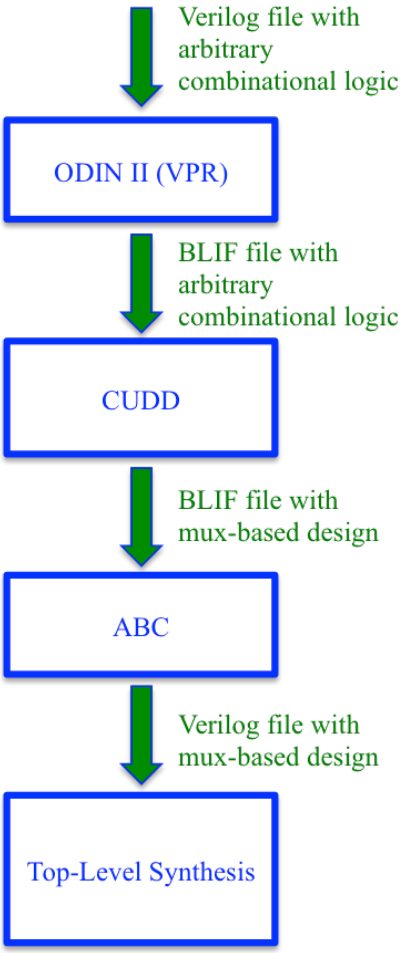


Figure 12: The proposed tool flow for mux-based design.

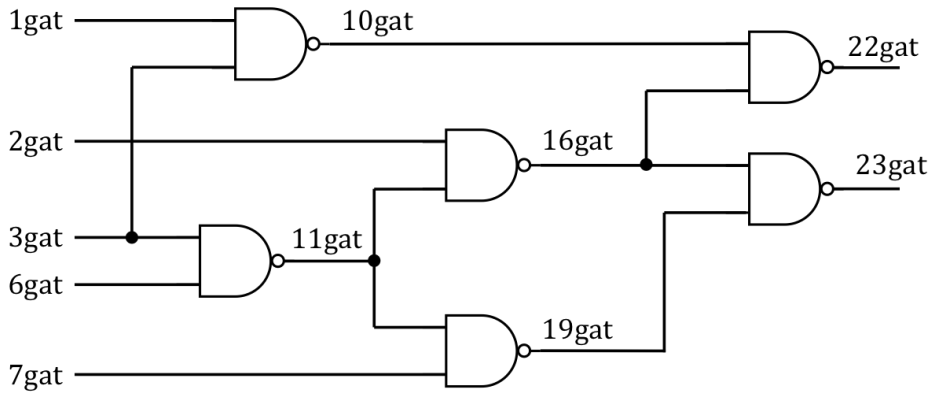


Figure 13: ISCAS '89 c17 benchmark circuit (based on [22])

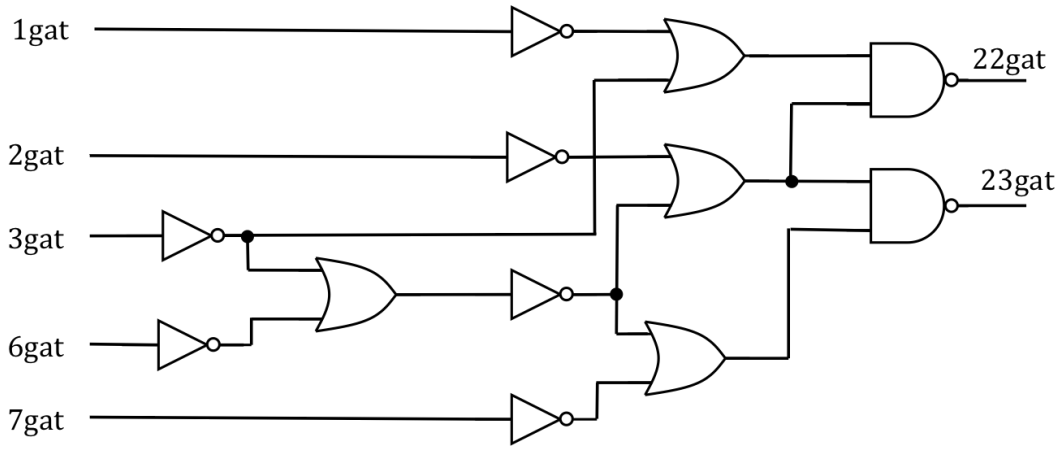


Figure 14: Top-level synthesis of c17 benchmark circuit without mux-based design constraint.

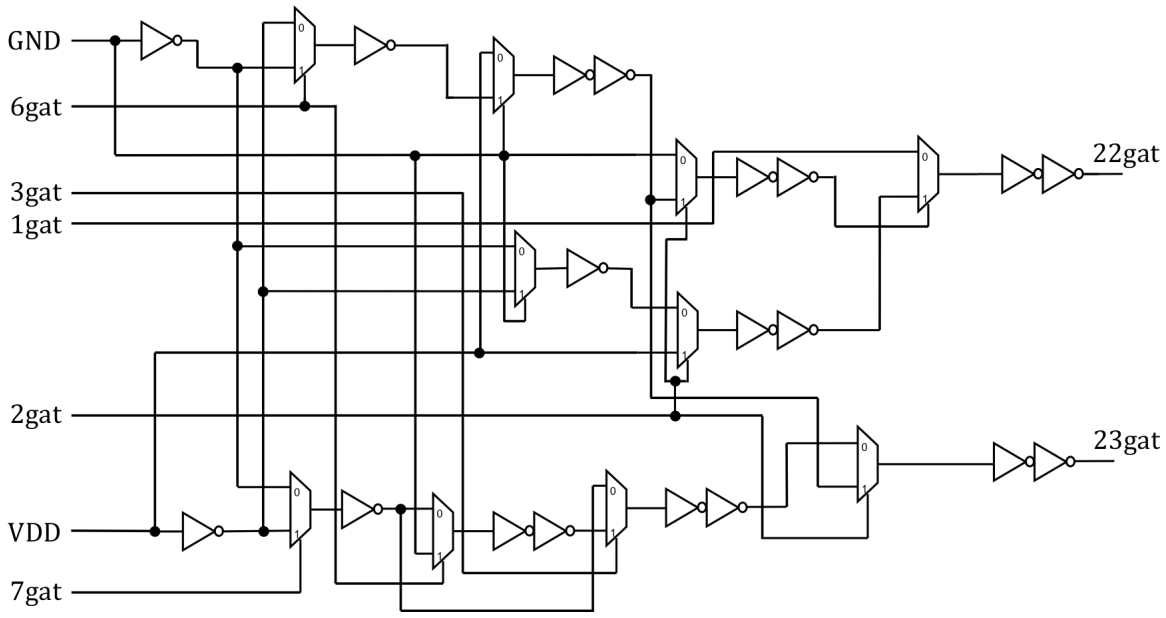


Figure 15: Top-level synthesis of c17 benchmark with mux-based design constraint. The area of the design shown here is about 3x the area of the non-mux implementation shown in Figure 14. However, this implementation has a number of unnecessary buffers inserted between gates that, if removed, would reduce the area.

CHAPTER 6

DISCUSSION AND FUTURE WORK

There are a number of results that would be worth examining in greater detail. It is assumed in this analysis that the change in the alternate input, B, is a good indication of variation-tolerance. This may not be the case, as low variation in metrics with respect to the B-input does not appear to correlate with configurations that result in the minimum supply voltage. In future work, it would be interesting to take all transient data with the other sizing combinations and see how the frequency and power compare to the selected sizing combination. Another reason for the lower minimum *VDD* associated with the two other sizing schemes could be increased I_{on}/I_{off}. Since these schemes have a higher average frequency, this could mean that the transistors are being turned on "harder" in these cases than the case selected as most robust. Thus, it would be interesting to see how the data for the other sizing schemes compares with the one used.

The next unexpected result worth exploring further is the higher leakage experienced by the mirror mux topology. One explanation for this could be that while there are more stacked transistors (by stack effect this should reduce leakage), there are also more parallel paths, which can result in greater leakage due to lower equivalent resistance. For example, in the case of the NAND gate, the PDN exercises good leakage control because it consists only of two stacked transistors and no parallel paths. The mirror mux has an extra possible leakage path in its PDN. The same case can be made when comparing the NOR gate's PUN to that of the

mirror mux. From this standpoint, the stacked inverter gate introduced in Chapter 1 is the best-case topology for variation-tolerance and low leakage ULP circuit design, however, the inverter is not a universal logic element and, therefore, could not take the place of NAND and NOR gates.

The analysis presented in this work suggests that the metrics used in this study to indicate variation-robustness may not be suitable. For example, low standard deviation was expected to indicate variation-tolerance. However, it appears that simplicity of circuit topology and higher average frequency may be better indications of a variation-tolerant design. Ultimately, the NAND and NOR gates function at lower minimum supply voltages than the mirror mux, and the frequencies generated by ROs constructed from NANDs and NORs is higher. Their standard deviations are higher than the mirror mux, when it was expected that lower standard deviation would allow a circuit to function at a smaller minimum supply voltage. Though the active power consumed by the mirror mux is less due to its low performance, the NAND and NOR gates consume less total power ar low voltages because of the large amount of leakage through the mirror mux. The theory was that the symmetric topology and many stacked transistors would encourage robustness to variations and lower leakage. If there were a way to get the leakage power under control in the mirror mux, it would be highly optimal for sub-VT.

The relationship between bias and voltage, on the other hand, is a very exciting finding, and appears to be highly effective. The effectiveness is primarily seen at very high temperatures. Therefore, if the circuit is expected to run at room

temperature or even at very low temperature, no measures to bias adaptively are necessary. This scheme is also in need of greater analysis. For future work, it would be useful to see how much smaller of a supply voltage this biasing scheme allows for a circuit to go. This scheme increases average frequency and in some cases decreases average energy.

CHAPTER 7

CONCLUSION

Power is a growing concern for the semiconductor industry, and sustainable technologies may be the key to continuing to advance in this power-constrained age. Energy harvesting is an extremely exciting option for a variety of ULP applications. However, in order for energy harvesting to become a viable option for commercial distribution, schemes for maintaining robust circuit designs in the weak inversion regime are crucial. This thesis presented a biasing scheme that allows for operation at lower supply voltages with greater stability than a typical universal biasing or sizing technique. A symmetric mirror mux topology was presented and shown to be optimal for some ULP applications.

APPENDICES

APPENDIX A

NOTES ON THE BDD TOOL FLOW

There are certain items to note with respect to implementing the proposed tool flow in Figure 11. In order to use this tool flow, modifications must be made to the standard cell library used, as well as the output script. Due to the optimization done by the EDA tools, muxes are not the first choice for implementation of the design. So, modifications must be made to the standard cell library that force the EDA tools to choose muxes. Removing the "first choice" gates from the standard cell library is one option. Another approach is to change the way gates are characterized in the standard cell library by increasing the area or delay assigned to a gate. It may also be necessary to tell the tools to optimize for a particular design characteristic. These techniques may be used in conjunction, and the best way will depend on the circuit one wishes to synthesize. For example, optimizing for area in conjunction with increasing the area depicted in the standard cell library of a gate that is selected before the mux may be necessary.

Another important note with respect to the flow is that the internal nodes will be of type "wire" when ABC generates the Verilog script. Each internal node must be changed from "wire" type to "inout" type, and the variable names must be added to the module declaration. This is likely due to the way in which the EDA tools interpret an inout as compared to a wire. It is worth noting that changing from wire to inout impacts area. For inout types buffers are inserted between gates. This is not the case for wires, so the area is increased significantly. Based on the EDA tool analysis, area is increased by over two times with this change.

BIBLIOGRAPHY

[1] Mitcheson, Paul D., et al. "Energy harvesting from human and machine motion for wireless electronic devices." *Proceedings of the IEEE* 96.9 (2008): 1457-1486.

[2] Pu, Yu, Henk Corporaal, and Yajun Ha. "Vt balancing and device sizing towards high yield of sub-threshold static logic gates." *Proceedings of the 2007 international symposium on Low power electronics and design*. ACM, 2007.

[3] Alice Wang, Benton H. Calhoun, and Anantha Chandrakasan.*Sub-threshold Design for Ultra Low-Power Systems,* Springer, 2006.

[4] Singh, Rajesh, et al. "Analysis of the Effect of Temperature Variations on Sub-threshold Leakage Current in P 3 and P 4 SRAM Cells at Deep Sub-Micron CMOS Technology." *International Journal of Computer Applications* 35.5 (2011).

[5] Zhao, Wenfeng, et al. "Robustness-driven energy-efficient ultra-low voltage standard cell design with intra-cell mixed-V t methodology." *Proceedings of the International Symposium on Low Power Electronics and Design*. IEEE Press, 2013.

[6] Zhang, Y.(2013). Synthesis Based Design Techniques for Robust, Energy Efficient Subthreshold Circuits. Retrieved from http://libra.virginia.edu/catalog/libra-oa:3899

[7] Narendra, Siva, Dimitri Antoniadis, and Vivek De. "Impact of using adaptive body bias to compensate die-to-die Vt variation on within-die Vt variation."*Proceedings of the 1999 international symposium on Low power electronics and design*. ACM, 1999.

[8] Choi, Hoon, et al. "Improved current drivability with back-gate bias for elevated source and drain structured FD-SOI SiGe MOSFET." *Microelectronic Engineering* 86.11 (2009): 2165-2169.

[9] Saeidi, Roghayeh, Mohammad Sharifkhani, and Khosrow Hajsadeghi. “A subthreshold symmetric SRAM cell with high read stability.” *Circuits and Systems II: Express Briefs, IEEE Transactions on* 61.1 (2014): 26-30.

[10] Sakurai, Takayasu, Akira Matsuzawa, and Takakuni Douseki. Fully-Depleted SOI CMOS Circuits and Technolgy for Ultralow-Power Applications. The Netherlands: Springer, 2006.

[11] Vitale, Steven A., et al. “FDSOI process technology for subthreshold-operation ultralow-power electronics.” *Proceedings of the IEEE* 98.2 (2010): 333-342.M. Young, The Technical Writer’s Handbook. Mill Valley, CA: University Science, 1989.

[12] “Learn More About FD-SOI.” *ST Microelectronics*. 1 Jan. 2015. Web. 20 Feb. 2015. <http://www.st.com/web/en/about_st/learn_fd-soi.html>.

[13] F. Somenzi, “CUDD: CU decision diagram package release 2.5.0,” University of Colorado at Boulder, 1998.

[14] J. Luu, J. Goeders, M. Wainberg, A. Somerville, T. Yu, K. Nasartschuk, M. Nasr, S. Wang, T. Liu, N. Ahmed, K. B. Kent, J. Anderson, J. Rose and V. Betz “VTR 7.0: Next Generation Architecture and CAD System for FPGAs,” ACM TRETS, Vol. 7, No. 2, June 2014, pp. 6:1 - 6:30.

[15] Cauchy, Xavier. “Questions and Answers on Fully Depleted SOI Technology for next Generation CMOS Nodes.” *SOI Industry Consortium*. 1 Apr. 2010. Web. 20 Feb. 2015. <http://www.soitec.com/pdf/SOIconsortium_FDSOI_QA.pdf.

[16] Shannon, Claude Elwood. "A symbolic analysis of relay and switching circuits."*American Institute of Electrical Engineers, Transactions of the* 57.12 (1938): 713-723.

[17] Akers, Sheldon B. "Binary decision diagrams." *Computers, IEEE Transactions on* 100.6 (1978): 509-516.

[18] Rutenbar, R.A. (2013) *VLSI CAD: Logic to Layout* [1-63].

[19] Lee, Daesung, et al. "Combinational logic design using six-terminal NEM relays." *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on* 32.5 (2013): 653-666.

[20] Berkeley Logic Synthesis and Verification Group, ABC: A System for Sequential Synthesis and Verification, Release 5a3f4545e2fd. http://www.eecs.berkeley.edu/~alanmi/abc/

[21] Shukla, Neeraj Kr, et al. "Analysis of the Effect of Temperature and Vdd on Leakage Current in Conventional 6 T-SRAM Bit-Cell at 90 nm and 65 nm Technology." *International Journal of Computer Applications* 26.10 (2011).

[22] "Circuit Modeling." Web. 29 Mar. 2015. <http://ssdi.di.fct.unl.pt/~fa/phd/Chapter2_Circuit_Modelling.pdf>.