A 2-Dimensional mm-Scale Network-on-Textiles (kNOTs) for Wearable Computing with Direct Die-to-Yarn Integration of 0.6×2.15mm^2 SoC and bySPI Chiplets

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On my honor as a University Student, I have neither given nor received unauthorized aid on this assignment as defined by the Honor Guidelines for Thesis-Related Assignments

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A 2-Dimensional mm-scale Network-on-Textiles (kNOTs) for Wearable Computing with Direct Die-to-Yarn Integration of 0.6mm x 2.15mm SoC and bySPI Chiplets

This paper proposes a scalable, 2-dimensional Network-on-Textiles (kNOT) comprised of systems-on-chip (SoCs) and "bySPI" networking chiplets that are jointly capable of supporting heterogeneous programming, multiple sensing modalities, and a distributed memory system. Emerging e-textiles must retain the flexibility and comfort of their host garment to be viable in wearable applications for healthcare, virtual reality, and sports [1]-[4]. Prior integration efforts have demonstrated textile computing by weaving flexible filament circuits [5]-[7], embroidering conductive yarns [8], and fabricating electronic fibers [9]-[10]. Still, these works suffer from a combination of bulky, rigid components, high cost, or 1-dimensionality (Fig. 1). To preserve the textile's look and feel, SoCs for fabric integration must also be highly miniaturized, feature minimal area-hungry IO interfaces, be easily programmable, and be fully integrable. The e-textile system in [11] integrated a health sensing chip onto a planar fashionable circuit board, yet the board (25mm x 25mm) is 40x larger than the chip itself. The System-in-Fiber from [12] is fully autonomous but has many IO pads, is limited to 1D networks, and requires an interposer (4.7mm x 3.7mm) that is 3.8x larger than the die. Most recently, a battery-less e-textile system in [13] integrates cm-scale harvesting tiles and an inductor onto a shirt, but it lacks an integrated SoC. Many wearable applications also demand substantial on-garment storage, yet large memories are unsuited for comfortable textile integration due to their sizable footprint. Our proposed kNOT solution addresses this by replacing monolithic memory units with a distributed set of smaller memories. However, networking these chiplets via existing bus standards incurs significant area and power penalties [14]. Existing Body Area Networks highlight the potential of multi-chip solutions, but they lack seamless textile integration [15-17]. Hence, to truly realize a fabric computing system, we propose a board-and interposer-free 2D kNOT built with the direct-die attachment of two miniaturized chiplets: 1) an SoC with an array of reconfigurable pads, fault-tolerant global bootup, SoC-to-SoC clock synchronization, and dynamic network configuration; and 2) a bySPI chiplet which is a COTS-compatible, reduced-wire enhancement of the bypass-

SPI (bySPI) protocol [14] capable of connecting to any number of receivers (RXs) using three wires. The chiplets are directly interconnected to braided composite yarns, which are comprised of para-aramid structural yarns and insulated 25µm-diameter conductors [26]. For each pad, a yarn is embroidered into a cotton substrate and its insulation is selectively ablated using a laser. Solder paste is deposited, the chiplet is placed to align its pads with the yarns, and the solder is reflowed. The interconnections are then encapsulated to provide mechanical and environmental protection. This textile-chiplet interconnection approach is compatible with automated high-throughput 2.5D electronics manufacturing methods, enabling the production of textile-integrated systems at scale (Fig. 1).

Fig. 2 shows a system diagram of the proposed kNOT, where SoCs are linked with other SoCs, sensors, and memories via bySPI chiplets in a 2D tree-like network that can be distributed across a garment. To provide a scalable and distributed approach towards wearable computing, our kNOT system utilizes a miniaturized SoC with a Cortex M0+ core and 32kB SRAM (Fig. 2), optimized for kNOTs using: 1) a linear array of reconfigurable pads spaced at a pitch of 180um (Fig.7), which dominate the chiplet size. To meet IO requirements despite the limited area for pads, the pads are internally muxed to different signals at runtime. 2) a custom bySPI-compatible receiver (RX) that enables SoCs to boot up globally from the upstream network, reducing the number of off-chip components (i.e., NVMs) required in the network compared to previous SoCs [18]-[22]. Using this feature, different SoCs can be programmed with either the same or different programs via bySPI protocol. 3) an on-chip clock architecture with tunable fast and slow clock sources that can be synchronized across SoCs using a high-precision clock synchronization algorithm. The bySPI architecture (Fig. 2) supports kNOT routing with: 1) A one-to-many 3-wire SPI protocol that allows the transmitter(TX) to bypass signals to the intended RX, 2) A group access feature that allows for simultaneous access to multiple chiplets within a downstream group, 3) A Chip Select (CS)-free soft reset to address the lack of a conventional CS signal and a timeout state to address dropped clock edges (Fig.2, bottom left), 4) a CS generator to interface with COTS modules using 4-wire SPI. Both chiplets communicate at 1.8V, with

the digital core running at 1.1V generated by a fully-on-chip low-dropout regulator (LDO) (Fig. 3) comprising a PMOS pass transistor, 300mV V_{ref}, and a 1:4 feedback network of 4 pseudo resistors to save area. An RC circuit is added for stability compensation, and the on-chip output capacitor is a well-biased MOS [23] +MOM+MIM design to achieve a high capacitor density of 9.95fF/μm^2(simulated value) over existing designs [24].

In our kNOT system, both chiplets can interface with COTS sensor and memory nodes by reconfiguring their pads to use 4-wire SPI. The upstream network can be any preprogrammed SoC or TX capable of sending SPI signals and setting up the network. Fig. 3 explains the tailored algorithms we developed for this kNOT system. We propose a global bootup process based on asynchronous handshaking between upstream chiplets and SoCs, where the TX reads back and validates the written program to correct any data corruption in the yarns. The handshake and timeout features collectively ensure that the SoCs in a kNOT are programmed reliably. We introduce a clock and timestamp synchronization protocol [25], depicted in Fig. 3 (right), that surpasses traditional schemes requiring a crystal oscillator (XO) for each chip in a network. Timestamps are appended to data packets before storage to ensure seamless reconstruction during read-out. Addressing the impracticality of using XOs for each SoC, this approach employs a periodic reference timestamp sent by the upstream network. Downstream SoCs compare this reference to a locally generated value from a timer peripheral, enabling precise tuning of on-chip clocks based on the difference in timestamp values. The custom bySPI chiplet uses a SPI-like protocol with 8-bit commands to identify the access target in the downstream network and reduce pad count vs. conventional SPI. By sending bypass instructions to set the output direction of the bySPI chiplet, the TX can build a channel in the kNOT system to communicate with the target. The Function and Direction Controller block (Fig. 2) decides whether to enter the "selected" or "unselected" state based on instructions received from the TX. To enter the “unselected” state, bySPI must receive a bypass command, after which it transmits signals to the downstream chip. To enter the “selected” state from the “unselected” state, bySPI must receive a reset path command followed by an access

command, enabling it to respond to future read and write commands. The soft-reset instruction resets the bySPI state machine upon receiving at least fifty 1's followed by a 0, allowing communication to be recovered following a partial signal loss.

The SoC and bySPI chiplets are fabricated in 65nm CMOS. Fig. 4(top) shows a demo kNOT system of SoCs (S1-S3) and bySPI chiplets (b1-b3), with a COTS sensor (BME280) and memory (MX25U12843G). Once S1 is programmed, it sets up the bySPI link b1-b2 and performs read and write operations with the sensor and memory. The measured waveform in Fig. 4 shows the b1-b3 bySPI tree being configured to bypass signals in the desired direction and transmit to multiple leaf nodes. While programming S1, we intentionally send some corrupted data packets to validate the fault-tolerant bootup algorithm. The read and write operation with COTS components is achieved using the protocol conversion feature of b2, and Fig. 4 (bottom right) shows in-textile measured waveforms. Fig. 5 shows the measured electrical performance of the LDO and measured waveforms for example operations from the bySPI protocol. At a frequency of 10 MHz, the SoC consumes 3.3318 mW while the bySPI chip consumes 1.9296 mW. The LDO consumes a quiescent current of 9.8 μA, and its output voltage is 1.125 V when the load current is 0 A. The LDO has a voltage variation (ΔV) of 98 mV when the load current (ΔI) changes by 10 mA in 40 μs.

Fig.6 compares the proposed kNOT solution with state-of-the-art textile integrated systems and SoCs. The kNOT system excels in textile integration while offering capabilities for processing, networking, and data collection using the bySPI and SoC chiplets. Fig 7. shows the die micrograph of the SoC and bySPI chiplets and a comparison with miniaturized SoCs. The seamless integration of yarns, chiplets, and protocols positions the kNOT as an integratable, scalable choice for creating a distributed garment-wide, 2D network of interconnected chiplets.

[Placeholder for acknowledgements]

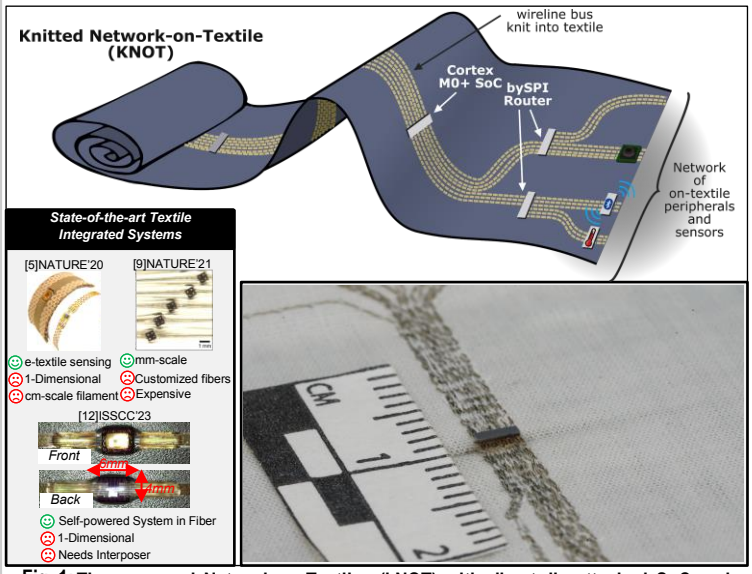


Fig. 1: The proposed Network-on-Textiles (kNOT) with direct-die attached SoC and bySPI chiplets (top); Comparison of the State-of-the-art Textile Integrated Systems(bottom left); Integration of a chiplet in textiles (bottom right)

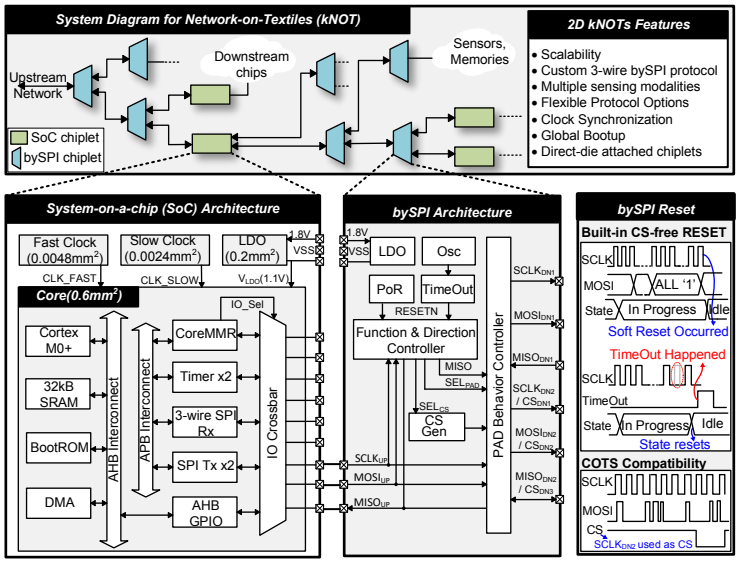


Fig. 2: System Diagram of kNOT demonstrating SoC and bySPI chiplets linked together(top); Architecture of the proposed SoC and bySPI chiplet(bottom left);bySPI soft-reset behavior independent of CS signal (bottom right)

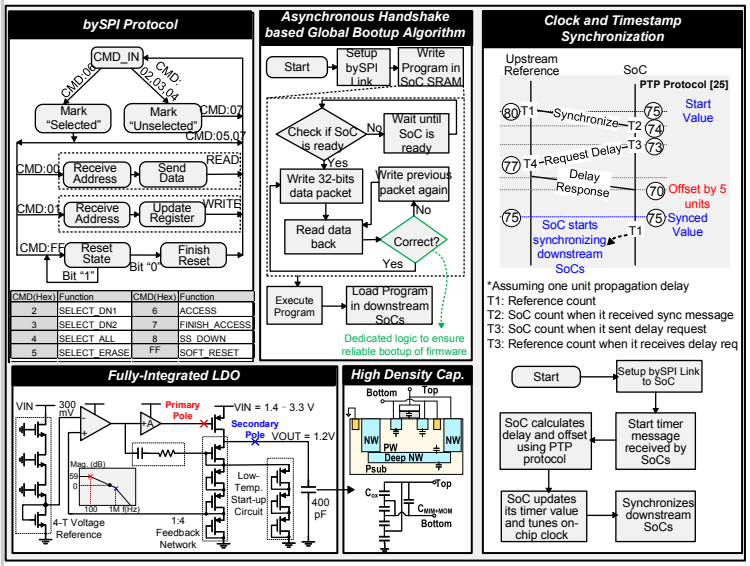


Fig. 3: Proposed 3-wire bySPI Protocol (top left); Global Bootup Algorithm (top middle); Architecture of Fully-Integrated LDO with high density cap (bottom left); Clock and Timestamp synchronization (bottom right)

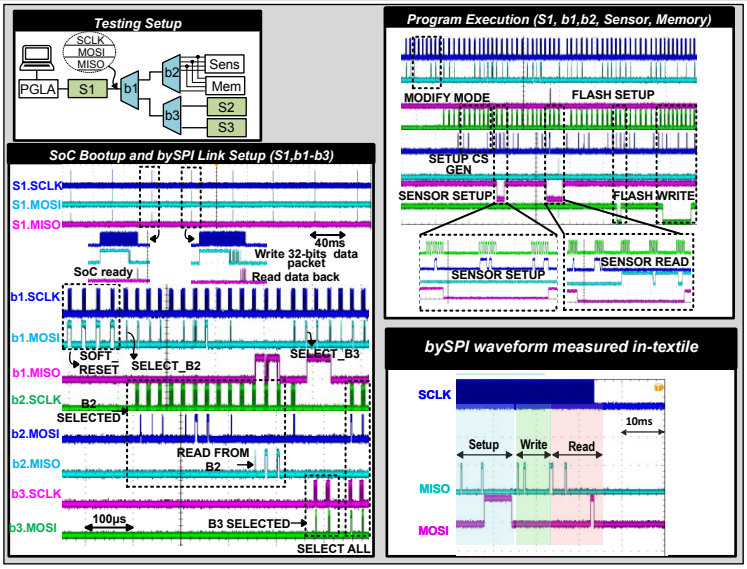


Fig. 4: Test setup for kNOT (top); measured waveforms for SoC bootup and bySPI link configuration (left), for program execution (top), and in-textile bySPI (bottom).

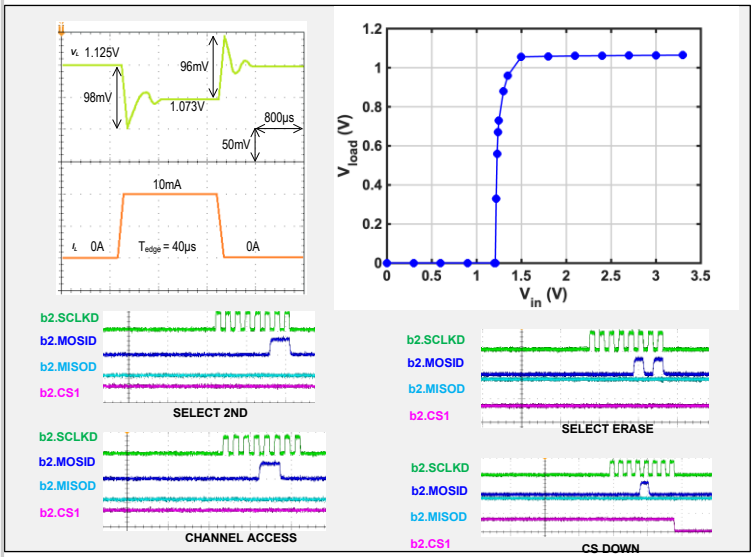


Fig. 5: Measured electrical performance for the on-chip LDO and measured waveforms for example operations from the bySPI protocol.

		This Work	ISSCC'23 [12]	VLSI'24 [13]	ISSCC'08[11]	Advanced Materials'19 [6]	NATURE'21[9]	NATURE'20[5]
Application		Network on Textiles	Systems-in-Fiber	E-textile Walking Step Counting System	Wearable Monitoring System	Wearable E-textiles	Fabric based ML Interface	E-TeCS for Physiological Sensing
2D Network Scalability		Yes	No	N/A	No#	No	No	No
Processor		Cortex M0+	RISCV	N/A	RISC	ATTiny20	STM32F401	MetaWearR module from MbientLab
Memory per chiplet		32kB SRAM	6kB DLS SRAM	DLS Memory	SRAM 2kb(Code) + 6kb(Data)	2kB Flash + 128B SRAM	512kB Flash + 96kB SRAM	256kB Flash + 16kB RAM
Processor Integrated in Textile		Yes	Yes	No*	Yes	Yes(COTS)	No	No
PCB/interposer required for textile integration		No	Yes	Yes*	Yes	Yes	Yes	Yes
Size of Processing Module(mm²)		0.6x2.15	3.15x2	1.95x2.73	3x5	1.4x1.55**	10x10	26x17**
Size of module integrated(mm²)		0.6x2.15	4.7x3.7	20x20	25x25	1.5x2.5	0.84x0.84	6x10
Boot-up Function		Global Boot-up	Ripple Boot-up	N/A	From external programming	From on-chip flash	From on-board flash	From on-board flash
Clock Sync Across Network		Yes	No	N/A	No	No	No	No
Supports Multiple Sensing Modalities in Network		Yes	No	No	No	No	Yes	Yes
Communication	Protocol	3-wire bySPI	4-wire SPI	NFC	Both wireless and wireline	4-wire SPI	I2C	I2C
	No. of TX pins to control N RXs	3	N + 3	N/A	-	N + 3	2	2
	Constant Static Power Dissipation	Low	Low	Low	Low	Low	High##	High##

*SoC Integration on Textile not demonstrated **Taken from datasheet
#Not demonstrated ##Due to pull up resistor when the bus is driven low

Fig. 6: Comparison of kNOT with prior state-of-the-art textile integrated systems. kNOT scales to 2D and has the smallest integratable processing modules.

	This Work		ISSCC'23[12]	JSSC'18[18]	VLSI'18[19]	ISSCC'08[11]
	SoC	bySPI				
Technology	65nm	65nm	65nm	130nm	55nm	250nm
Power Management	Fully Integrated LDO	Fully Integrated LDO	On-chip EHPMU, off-chip cap	PMU + External Power Management IC	PV + No regulator	Battery
Clock Source	On-chip FAST and SLOW clock	On-chip FAST clock	On-chip Adaptive Clock Generator	Crystal Oscillator	On-chip Subthreshold Oscillator	On-chip clock Generation
Operating Voltage	1.4-3.3	1.4-3.3	1.2-1	3.5-1.2	0.65	2
Number of Pads	12	12	>50	>100	-	12
Operating Frequency	10MHz	10MHz	<850Hz	110MHz	48Hz	1MHz
Components included in system power	MCU+SRAM+ROM+CLK+LDO	CLK+LDO+Digital	Sensor+MCU+SRAM+ROM+CLK+EHPMU+	MCU	MCU + Tx + Temp Sensor + SRAM	MCU + SRAM + Clk gen + CDR + Cap Sensor
Power Consumption	3.34mW	1.93mW	33nW@0.183V	33.6uW/MHz/core	16nW	1.12mW
Chip Size(mm^2)	0.6x 2.15	0.6x 2.15	3.15x2	4.768x4.368	0.36x0.4	3x5

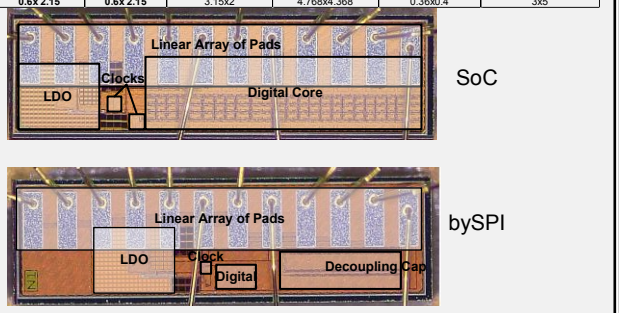


Fig. 7: Testing setup for chiplet characterization using packaged dies on PCBs for rapid network testing of different SoC and bySPI configurations.

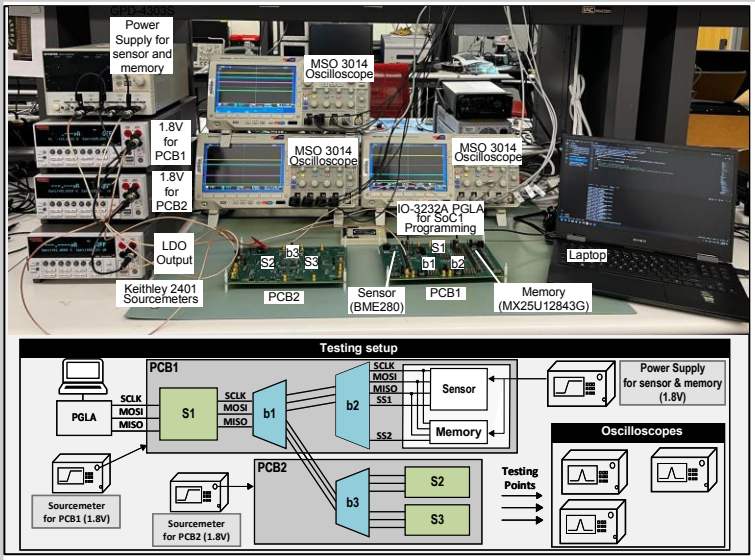
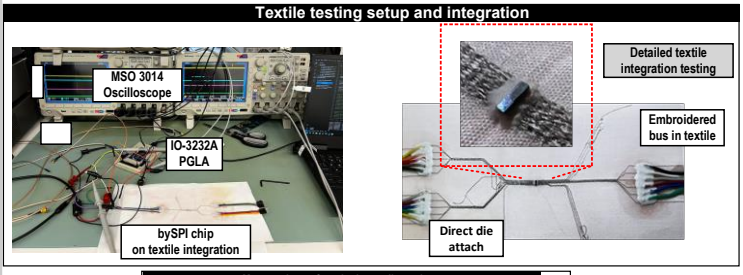


Fig. S1: Testing setup for chiplet characterization using packaged dies on PCBs for rapid network testing of different SoC and bySPI configurations.



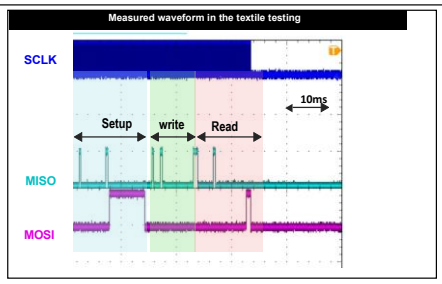


Fig. S2: Example of in-textile integrated testing setup for measuring communication using textile-attached bySPI die.

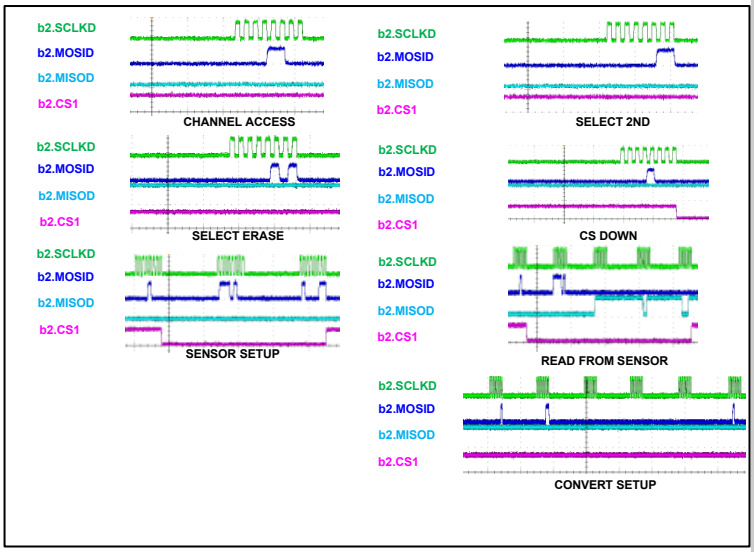


Fig. S3: Measured waveforms for various operations using the bySPI protocol.