Fabrication and Read-out of Integrated Photonic High Frequency Acoustic Wave Detectors

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Bachelor of Science, School of Engineering

Xiangwen Guo

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Technical Project Team Members

Andrew Tiggs

Adam Turflinger

On my honor as a University Student, I have neither given nor received unauthorized aid on this assignment as defined by the Honor Guidelines for Thesis-Related Assignments

Harry Powell, Department of Electrical Engineering

Andreas Beling, Department of Electrical Engineering

Mouse Brains - Fabrication and Read-out of Integrated Photonic High Frequency Acoustic Wave Detectors

Xiangwen Guo, Andrew Tigges, and Adam Turflinger

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Capstone Design ECE 4440 / ECE4991

Signatures

Xiangwen Guo ______________________________

Andrew Tigges ______________________________

Adam Turflinger ______________________________

Statement of work:

Xiangwen Guo

I mainly focused on the fabrication process of the ring resonator sensor. I designed the process of deep etching a membrane on a chip with the dimension of 2 x 4mm. I designed in AutoCAD and created in-house a lithography mask which was designed to enable back alignment for fabrication of the sensor on our integrated photonics chip. The dimension of the membrane was specifically designed to maximize the sensitivity of this sensor. Many types of masks for surviving this deep etch were designed and attempted including AZ9620, SiO2, Aluminum and AZ5412. Different etching processes were also attempted including BOE, Aluminum wet etch, SiO2 dry etch, and Bosch process. Process was also designed to be able to handle a chip with this small dimension and protect the features on the back. SEM images were also taken.

I have also communicated with Professor Beling's graduate student Ta Qing Tzu who worked on this previously designed chip earlier and figured out the dimension of the designated ring we will be using as our sensor, the waveguide and how to feed in the optical signal into it and where to read out the signal, and how to operate the tunable laser.

As for the readout system, I was in charge of parts ordering and PCB soldering.

I have made all the weekly update presentation slides, the poster, and the final video.

Andrew Tigges

My main focus in this project is the programming of the myRIO. The main focus of the programming was to use the high throughput personality to reach the max sampling rate of 250 MHz. This was performed using a real time while loop block for data storage, and another while loop for data output. Since there was difficulty reading the output directly, the FPGA target interface to receive the value at the analog input directly. This allowed us to use two invoke methods in series, the first to read out the number of data points and wait until there were one thousand. The next invoke method then received the block of a thousand data points and added them to a queue. This was a queue of ten one thousand point arrays. These arrays were then displayed on the front panel using the waveform graph block. The program also allowed for the change of the sampling rate and varying the analog offset.

Another of my responsibilities was adapting the existing LabVIEW laser control program for RS-232. This would allow the MyRIO to be a standalone computer controlling both the calibration and analog output portions. This would be relayed to a computer monitor using USB. The RS-232 required reading considerable documentation and changing standard VISA blocks to MyRIO serial RS-232 blocks. This portion was not demoed because the photonics portion was not able to be completed due to problems not within the control of the group.

I also created the circuit for that was eventually demoed on the presentation day. This consisted of two light emitting diodes, one that had a sine wave voltage across it. The other LED was pointed toward the first LED and used as a photodiode. A current was thus produced in the second LED that was used as the input to the transimpedance amplifier. This was then the output on the front panel of the LabVIEW program.

Adam Turflinger

I helped design the first attempt process flow for fabricating our sensor. I aided in an attempt to show the Bosch process working on an empty silicon-on-insulator wafer using the AZ5214 photoresist. When this failed on account of the photoresist thickness, I met with Dr. Mike Cyberey to design a new process flow using the AZ9260 photoresist. Using his data on the photoresist development and etch selectivity, I designed the initial process flow including photoresist thickness ($thickness > \frac{700\, microns}{50} = 14\, microns$), the time for the photoresist to rehydrate before development (approximately 60 minutes dependent on the clean room humidity), and the exposure energy for development ($800 mJ/cm^2$ in the laser writer). This process helped create the first wave of sensor fabrication. At this point, I shifted my focus to the electronics and read-out to ensure timely delivery of the demo.

I created the circuitry to amplify and filter the photodiode current and interface with the myRIO. With Professor Powell's suggestion, I selected the OPA380 transimpedance amplifier to convert the current into a samplable voltage. I then designed the amplifier using the photodiode current ranges such that it will maximize the 5V available for power on the myRio with a 1V offset to avoid clipping ($R_f = \frac{4V}{1mA - .01mA} \approx 4000\Omega$) and the feedback capacitor to minimize noise while maintaining a high bandwidth ($C_f < \frac{1}{2\pi R_f f} \rightarrow C_f = 390pF$). I then designed a unity gain fourth order cascaded low-pass sallen-key filter for anti-aliasing before sampling on the myRIO. I designed the Q at the Butterworth characteristic (.707) by cascading filters with Q-values of .5496 and 1.31. We are sampling at 250kHz with 12 bits of resolution, so I calculated the necessary attenuation at the Nyquist rate, 125kHz, as $\alpha = \frac{1}{2^{12}} = -72dB$. Using this, I calculated the necessary corner frequency for anti-aliasing as $f_c = 250kHz * 10^{-72/80} \approx 31kHz$and calculated component values to fulfill this design. I also designed additional circuitry to implement RS232 communication with the tunable laser, although this feature was not implemented. I implemented all of this circuitry into 3 waves of PCB orders and tested the features for correct functionality once they were soldered. This PCB was used in the development of software to characterize the resonator as well as the real-time display of the signal used in our demonstration.

Finally, I wrote the LabVIEW software for locking the laser into a resonant frequency to calibrate the readout system. I received the drivers for controlling the laser from a graduate student and interfaced it to the laser using GPIB. Using the myRIO and my custom PCB, the software sweeps the laser frequency and measures the output voltage on the PCB to create a resonance curve. It then manipulates this data to find and set the biasing wavelength of the laser properly. This software was not used in the demo as the sensor was not fully completed on account of clean room renovations, however it will be used in system calibration once the sensor is fabricated.

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Abstract

Sufficiently thin silicon waveguides shift dielectric constants and therefore waveguide modes in strained states. This effect has been used to demonstrate ultrasonic sensing using photonic microring resonators on membranes. We created the process flow for fabrication of such an ultrasonic sensor with area less than $1mm^2$ using integrated photonics circuitry and fabrication processes. We also designed and created software and hardware for calibration and real-time display for a low frequency demonstration of the sensor. These sensors have application in photoacoustic microscopy which demonstrates optical-resolution imaging without the need for contrast agents.

Background

In considering a capstone project, our group sought something which could tie our interests in the physics of materials, photonics, and electrical design into a project that could produce results in one semester. Xiangwen and Adam had recently finished Professor Andreas Beling's Optoelectronic Device Fabrication and Measurement Lab and looked to him for a project which could serve as a natural extension of the skills built in this course. Professor Beling posed the idea of an acoustic sensor fabricated from optical resonators and, with the addition of Physicist and Computer Engineer Drew and his expertise in digital embedded systems and theoretical condensed matter physics, our capstone project came to light.

This project arose as a result of Professor Song Hu's work both in his PhD at Washington University in St. Louis and as a Professor at the University of Virginia's Department of Biomedical Engineering in optical-resolution photoacoustic microscopy (OR-PAM). This imaging technique works through the acoustic waves released when biological tissues are bombarded with photons of a certain frequency and contain characteristic information about the tissue [1]. Professor Hu uses the unique benefits of OR-PAM to characterize biological processes using mice, for example in protein identification in brain capillaries [2]. However, the current method for measuring the relevant acoustic waves involves a complex and cumbersome system of piezoelectric materials which require the mouse to be anesthetized, limiting the OR-PAM to unconscious and immobile subjects [1]. This alters the physiology of the tissues thus leading to images which are not necessarily characteristic of an active subject. To bypass this issue, a lightweight ultrasonic acoustic sensor is necessary.

Our project attempts to offer a solution in acoustic membranes fabricated into integrated photonic microring resonators. In 2008, a group from the University of Michigan created a similar solution using polymer microring optical resonators as an improvement over the previous piezoelectric technologies. The incident pressures from sound waves alters both the dielectric constant of the polymer as well as the geometry of the membrane causing a change in the effective refractive index in the waveguide and a subsequent shift in the resonant frequency of the ring. This shift in resonant frequency could be read by measuring the transmission change in the system biased near a highly non-linear point of the frequency response. They found the polymers allowed for a high bandwidth signal through integration with waveguides giving the spectrum of the optical wavelengths, 5 orders of magnitude larger than that of ultrasonic signals [3]. In 2013, a group at Northwestern University fabricated a similar polymer microring resonator and were able to extend the bandwidth to 150Mhz [4]. In 2015, a group at Delft University fabricated a microring resonator in industrial-grade silicon and found it matched state-of-the-art piezoelectric transducers with a 60 times smaller physical footprint [5]. These sensors also see easy implementation in large arrays by tuning the resonators to different frequencies and using a broad-band optical input signal and frequency multiplexing. However, their fabrication required specialized dicing blades and laser etches to cleanly fabricate the membranes.

Our project seeks to extend the work at Delft University to an entirely industrial-grade CMOS fabrication process. To start, the microring resonators will be sourced from silicon-on-insulator (SOI) foundry-fabricated chips. The membranes will then be etched using typical industrial fabrication techniques including the Bosch process for high aspect ratio deep etches and wet sulfuric acid etches for final etches. The Bosch process, patented in 1996 by Bosch Corporation, alternates between isotropic plasma etching with sulfur hexafluoride and deposition of an inert polymer to ensure stability and verticality of the etch edges [6]. These processes are both able to be completed in the University of Virginia's Microelectronics Laboratory (UVML). More important, each process is highly selective and can be completed with a hard mask created using common evaporation and photoresist processes. Thus, this demonstration would extend microring resonators from a University cleanroom to an industrial scale in which they could be mass produced and easily integrated with photonic circuits.

This project requires knowledge from several physics and electrical and computer engineering courses. As previously stated, the membrane fabrication draws on skills gained from ECE4501: Optoelectronic Device Fabrication and Measurement which also served as a laboratory extension of ECE3103: Solid State Devices. The membrane's electrical properties as well as the waveguides and impedance matching surrounding the resonator rely on knowledge from a combination of ECE3209: Electromagnetic Fields, ECE6501: Guided Waves & Antennas, ECE5241: Optics & Lasers, and PHYS3430: Electricity & Magnetism I for their design. The design of these components also builds from a physical picture developed in PHYS3650/3660: Quantum Physics I and II, PHYS 3620: Condensed Matter Physics, and MSE4055: Nanoscale Science & Technology. The resonance shift of the microring harkens to the picture of frequency response built in the ECE Fundamentals series (ECE 2360, 2660, and 3750). The light transmission readout depends on a high-speed photodiode sensor which was also developed in ECE3103 and fabricated in ECE4501. The readout of this sensor requires a microcontroller as developed in ECE3430: Embedded Systems as well as digital sampling as developed in ECE3750. Through this, our project culminates almost the entirety of our combined backgrounds in electrical engineering, computer engineering, physics, and materials science.

Constraints

Design Constraints

The fabrication of our sensor was entirely constrained by parts already available and processes available in the University of Virginia's Microelectronics Laboratory (UVML or clean room). The integrated photonics chip containing a waveguide coupled to a microring resonator and a photodiode on the output had already been obtained from previous a previous project. The UVML's renovation limited the processes available for a hard mask. For example, we do not currently have a plasma enhanced chemical vapor deposition (PECVD) tool, so all silicon dioxide we deposit must be from sputtering. We also do not have a dedicated Bosch process machine, so we complete it in an Oxford inductive coupled plasma reactive ion etch (Oxford ICP RIE) machine. This creates additional delay in chemical supplies and requires further tweaking of the normal process.

Our project was generally limited in scope by the hardware and software available. The National Instruments (NI) myRIO was available and the obvious choice for a project in sampling and displaying a signal. However, the myRIO's FGPA has a maximum sampling rate of 250kHz. Coupled with the need for an analog anti-aliasing filter, this massively limits the maximum signal which can be passed through the circuitry from the ultrasounds (as desired for the research) to tens of kilohertz. Furthermore, the myRIO limits programming to LabVIEW, which provides a strong library of packages and simplicity, but also limits the potential complexity of our program on account of its block diagram structure.

Our PCB was limited by the manufacturing capabilities of our supplier. This included a minimum trace width and spacing of 10mils (or .01 inches). Furthermore, the edges of the board also had to be widened to 10mils. The parts available for our PCB were limited by orders from certain manufacturers and part orders in discrete and regular intervals. In general, this limited part orders to Digikey, Mouser, and Amazon, and parts orders only occurred approximately every two weeks (in line with board sendouts). This created a need to have our PCB and parts ready on a regulated schedule.

Economic and Cost Constraints

Our project was limited by the costs for fabrication. It costs $1,000 per student per month to use the clean room, which was necessary for the design of our process flow. This was supplied by Professor Beling's group as it contributes to his research output. The read-out system of our project was limited by the budget for our capstone group, around $100. Our project did not require many specialized or expensive components, however we were limited in the number of iterations we could create for costs' sake.

External Standards

Since the fabrication of membrane involves using the clean room, the UVML cleanroom safety standards would be strictly followed. The chip with the ring resonator is a standardized industrial foundry chip with dimensions 8.5mm by 6mm on a 600um Si substrate with 2um thick silicon dioxide for insulation of the photonic circuit. This chip and our manufacturing process will follow the the Silicon Photonics Process Design Kit from AIM Photonics, APSUNY PDKv3.0 [6]. These standards limit the components, spacing, and performance of our photonic chip. Furthermore, we would like our process to be compatible with these standards for mass production.

Control of the laser through software requires computer interfacing. Done through a computer's USB port, this is done through NI's GPIB interface. This is standardized by IEEE standard 488.2 [7]. When the RS232 serial port on the laser is used, this is standardized by the RS232 voltage levels, although there is not necessarily a standard pinout [8].

Communication to the MyRIO was done using the universal serial bus (USB) interface. This is an industry standard and is maintained by the USB-implementers forum.

The standards for our PCB manufacturing were sourced from IPC. These limited the thickness of our traces and the trace spacing to give a manufacturable product without errors [9].

Tools Employed

The final fabrication process used a variety of clean room equipment and related software. A sputtering tool was used to deposit the aluminum used as a hard mask. A centrifuge was used to spin AZ5214 photoresist for patterning. The photoresist was exposed using a photolithography mask aligner. The mask for this process was created using AutoCAD [10]. The exposed photoresist was developed with AZ300MIF developer. The features were etched in the mask using aluminum etchant and the rest of the photoresist was removed using acetone. The subsequent pattern was etched using the Oxford ICP RIE available in the clean room [11] to complete the process.

The use of a sputtered aluminum hard mask was new for us as we had previously only used masks created with plasmas (such as PECVD silicon dioxide) or evaporation (such as evaporated aluminum). We thought this would damage material quality, but it did not. The etching of aluminum using the wet aluminum etchant was also new to us. Xiangwen had to learn AutoCAD to create the photolithography mask. While a Bosch process had already been programmed into our Oxford by Dr. Mike Cybery, we had not used it before this semester. The final process flow, as well as the experimental process flows used before the final result, required the learning of many new clean room processes.

Our circuit was designed and simulated in NI's Multisim then transitioned into a PCB using NI's Ultiboard. While many components were familiar, Adam had to learn how to choose and design a transimpedance amplifier. He also had to learn about RS232 standards for implementation of our board layout.

The LabVIEW software used the NI myRIO in different capacities. The calibration software combined pre-written laser LabVIEW with the real-time microcontroller. Adam had to learn how to operate the laser's LabVIEW and integrate it with the myRIO's real-time microcontroller, which he had not used before. In particular, he had to learn how to use the RT FIFO to generate real-time operation. Drew's real-time display software used the myRIO's high-throughput FPGA personality to sample and display the signal from the PCB. Drew had to learn how to program the FPGA on the myRIO as well as learn LabVIEW to create a functional front panel.

Ethical, Social, and Economic Concerns

Environmental Impact

Our project seeks to create a product manufacturable in a typical silicon CMOS microelectronics foundry. These foundries are associated with high environmental impact in both the need for environmentally damaging chemicals (including fluorine gas and hydrochloric acid) as well as large amounts of power and cooling (one study found over 2 million gallons of water and 240,00 kilowatt hours of energy a day [12]. While measures are in place to minimize the environmental impact of these foundries, their presence is still damaging by its very nature.

Sustainability

Silicon is abundantly available, so its use is relatively sustainable. The high power use mentioned above, however, is not sustainable at the moment as we do not have infinite clean energy sources. Thus our project further leads to sustainability issues.

Health and Safety

The fabrication of microelectronics by its nature produces many hazardous chemicals. However, it is relatively simple to minimize these issues. In a research-oriented clean room, many standards are already in place to prevent injuries, including the use of industrial gloves and a robust ventilation system. Scaled to a foundry-level, many of the human factors are taken out with automation. Rigid protocol for the safe operation of the foundry and disposal of chemicals, then, mitigates health and safety risks.

Silicon and integrated photonic circuits, once manufactured, are not hazardous and are even relatively biodegradable (dependent on other components of the circuits). At the very worst, they may create a choking hazard in the wrong hands.

Manufacturability

As mentioned above, the sensors can easily be manufactured in typical CMOS microelectronics foundries. All processes are available through adherence to the SUNY PDK for integrated photonics production. These foundries are strictly controlled to mitigate risk. The manufacturing would be relatively cheap leading to a very cheap and effective ultrasonic sensor available for medical imaging. This can lead to reduced cost for medical imaging and subsequent diagnosis of issues. This would benefit society as a whole with cheaper medical costs.

Ethical Issues

The automation of the foundries used to create our project reduces jobs available. The scaling of our product to mass production thus leads to the increasing wave of automation replacing jobs. It does, however, produce many jobs in the supply chain of the chemicals, materials, and science in a foundry as well as job related to foundry operations.

Intellectual Property Issues

The concept for our sensor was patented in 2009 [3]. The group from Michigan claimed the use of photonic circuits with strained micro-ring resonators for the measurement of high frequency acoustic waves. The concept was independent, although some details are dependent on the photonic circuit waveguide and microring resonator patents.

The process flow for our project heavily relies on the Bosch process, which was patented in 1996 as “Method for anisotropically etching silicon” [13]. The Bosch process alternate between isotropically etching with a known silicon etching plasma and passivating with a polymer such that a feature can be cut highly vertically in silicon. Laermer and Schilp claim this process in their patent. The overall process is a dependent claim as the use of a plasma to etch silicon has been previously patented, however it offers an independent claim on the ability for polymers to passivate the edges of etching for higher anistropicness.

The start-up Butterfly Network launched their hand-held ultrasonic sensor Butterfly IQ in 2019 using MEMS technology [14]. The device is wand-like and connects to a smartphone app for ultrasonic imaging at home. Subsequently, ButterFly Network holds many patents relating to integrated circuit ultrasonic imaging. One such patents the methods of integrating an ultrasonic sensor with analog-to-digital conversion [15]. They claim placing an ultrasonic transducer on a chip along with analog-to-digital conversion along with several different integrated methods of data compression. The claim for integration on silicon is independent. However, the specifics of integration with ADCs and compression methods are dependent on older patents of these specific technologies.

The concept of creating arrays of sensors using frequency multiplexing was patented in 2017 by Hassel et. al [16]. They claim the use of an excitation signal across an array of sensors and subsequent frequency de-multiplexing to extract individual sensor data. Their claims also extend this to excitations that are switched and which are used to cross thermal thresholds. The claim to the readout through excitation and frequency de-multiplexing is independent. The subsequent claims for alternate methods are dependent as they are specific to the read-out methods of specific sensors.

These patents cover many of the subsets and applications of our project. Directly, our sensor is not patentable. Our fabrication process is not directly patentable as we almost entirely rely on the Bosch process. We could, however, potentially patent the application of the Bosch process to fabricating membranes in SOI (although there is competition from other research groups, e.g. [17]). Butterfly IQ's MEMS technology does not really overlap with ours, however its relevant technologies do. Most notably, the integration of an ultrasonic sensor in integrated circuits is not patentable, although integration with photonic integrated circuits might be. Finally, the application of our sensor in large arrays is not patentable, although specific techniques for de-multiplexing could be.

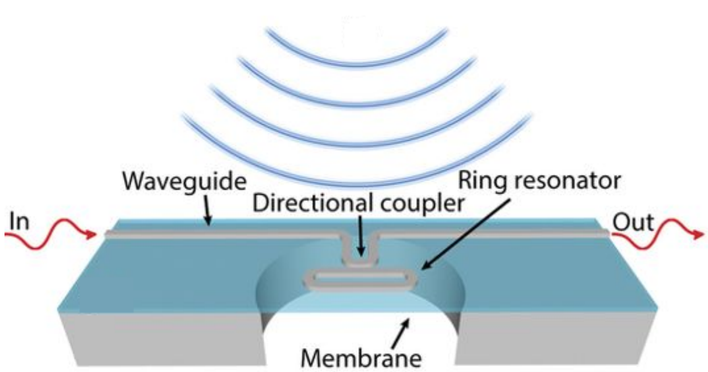
Detailed Technical Description of Project

Our technical project is divided into 4 separate parts: the working principles of the ultrasonic sensor, the designed process flow for fabricating the sensor, the circuitry and PCB used to read-out the sensor, and the software for demonstrating the sensor's functionality.

Ultrasonic Sensor Operating Principles

The sensor works through a photonic microring resonator. A waveguide bring in an incident light wave. This wave approaches a ring which provides interference patterns. Most wavelengths constructively interfere and pass through to the output waveguide, but a certain wavelength and a very narrow band around it are destructively interfered. This creates a very high Q optical band-reject filter.

If the substrate behind the microring resonator is removed to create a membrane, the material surrounding the microring resonator will strain with incident pressure waves (Figure e - left). This will alter the geometry of the waveguides as well as alter the dielectric constant of the photonic circuit. This will then change the resonant frequency of the band-reject filter (Figure e - right).These pressure waves can create as much as a 30dB modulation in optical intensity about a specific wavelength. A sound wave, by its nature, is plane waves of pressure fronts, thus sound waves will induce this intensity modulation.



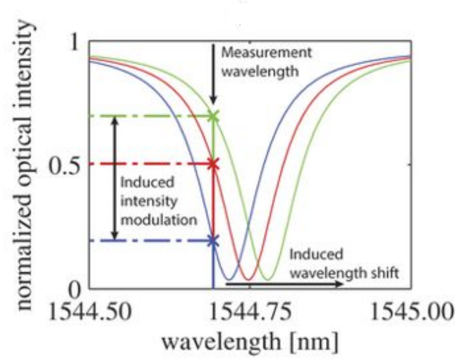


Figure e Ultrasonic Sensor Operating Principles [5]

The intensity of the output light can be measured with a photodiode to convert to an electrical signal. If the input signal is a narrow-band laser biased in the most non-linear portion of the resonance curve, a sound wave can be read from the photodiode as the change in photocurrent. This is the basis for an ultrasonic sensor. In our case, we will build the photonic circuit on an SOI wafer using integrated photonics processes. We will then cut through the silicon substrate around the microring resonator to create the membrane. The details of cutting vertically through a silicon substrate are difficult, leading to the design of our process flow. This process, however, will create an ultrasonic sensor which can be manufactured in a typical CMOS microelectronics foundry for a very low price.

Fabrication Process Flow

We sourced the microring resonator photonic circuit from a previous project. This chip has multiple functional devices. This project involves two of the ring resonators: Ring#1 and Ring#2 shown in Figure 2. Ring#1 consists of four waveguide connections: input, drop, through and add (from left to right). Ring#2 is connected to a balanced photodiode circuit with optical input waveguide connection at the bottom and three port at the top being negative, ground and positive for the diodes. As stated before, the goal of our fabrication process is to etch through the silicon substrate behind these rings to make membranes.

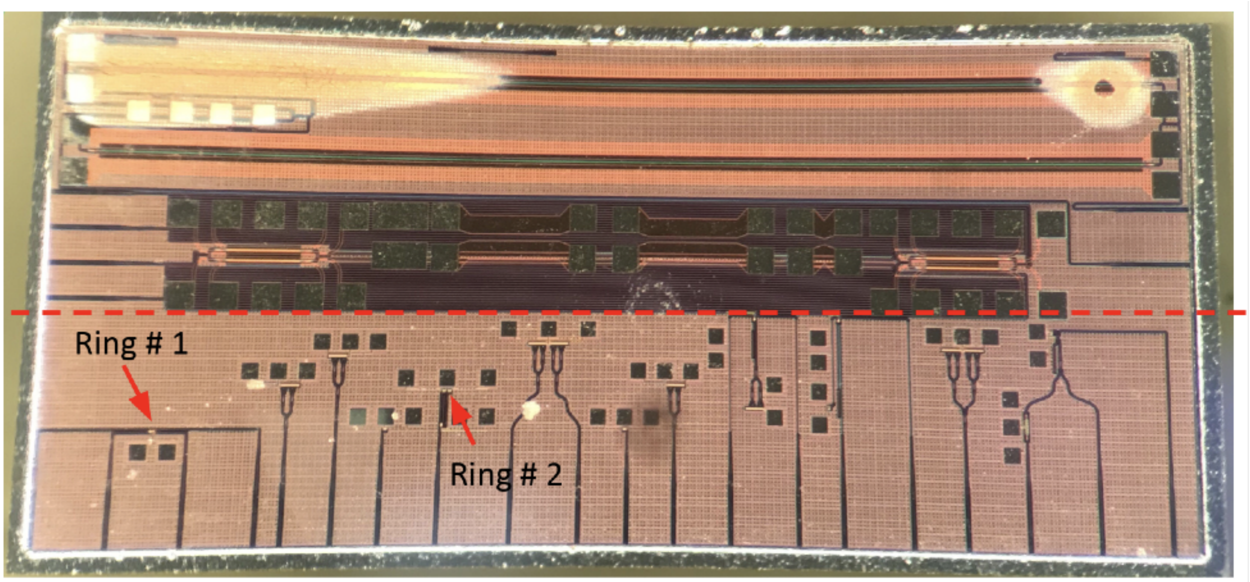


Figure 2 Front View of the Chip

The etching process will be done from the back of this chip in order to have these two ring resonators sit on a membrane. The material structure of this chip was expected to be SiO2, Si, SiO2, Si in the order from top to bottom. Devices are made of Si, sitting in between two oxide layers and a thick Si substrate layer on the back. The thickness of the silicon substrate was expected to be around 700um. In order to reach the oxide layer, approximately 700um of silicon needed to be etched away to make the membrane. Typical etching processes are isotropic. This means the etch will broaden the features of a mask created over time. This is fine for etches on the order of microns, but a 700um etch will create a large crater rather than a hole through the silicon. It was determined to use the Bosch process for deep anisotropic (vertical) etches, but the several iterations were needed to determine a suitable hard mask for etching the circular pattern into the silicon.

AZ5412 ([18]) is the common photoresist used as a mask in silicon dry etch recipes. However, early trials found the selectivity of the Bosch process between silicon and photoresist is around 37 meaning a thickness of at least 18.9um photoresist is needed in order to survive this etch without etching into the surrounding substrate. AZ5412 only spins to a maximum thickness of 2um. Therefore, an alternate mask is needed. With the help of Dr. Micheal Cyberey, AZ9260 ([19]) was introduced to us. This photoresist is designed to achieve relatively higher film thickness. After a long set of trials attempting to develop a thick photorersist in the UVML, a film thickness of 28um photoresist was successfully deposited on a silicon substrate. A process flow using AZ9260 as the etching mask is shown in Figure 3.

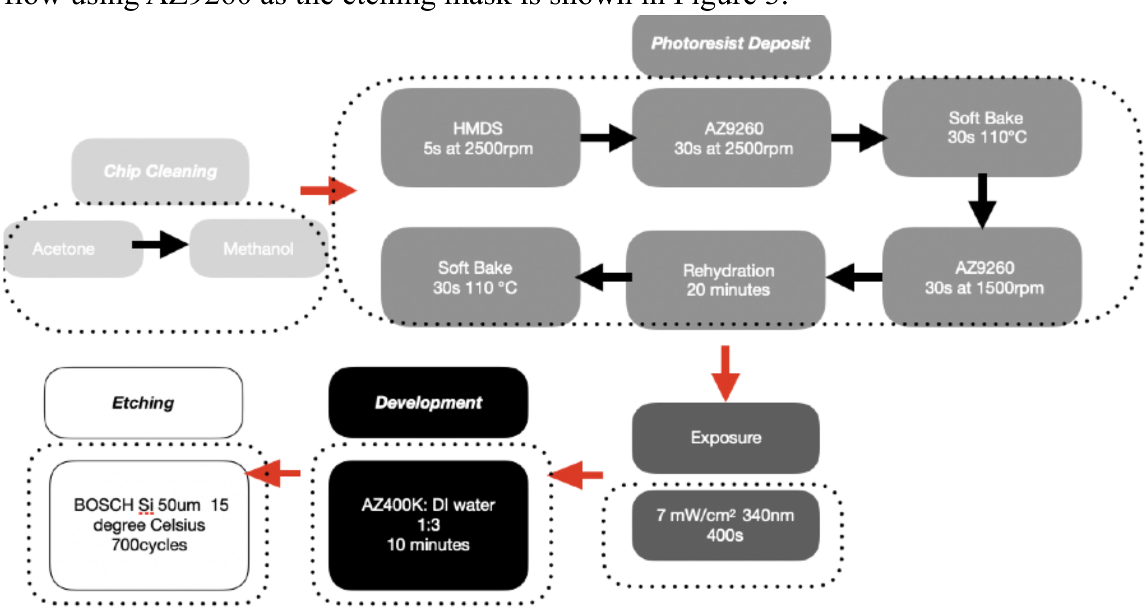
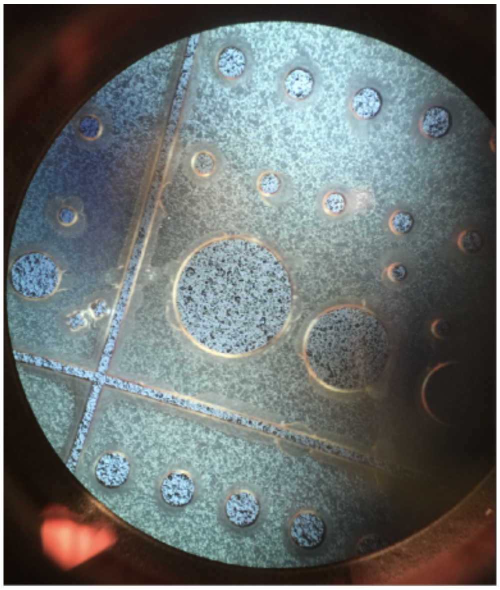


Figure 3 Fabrication Process Flow Using AZ9260 Mask

This process as shown in Figure 3 had been tested but the result did not meet our expectations of high material quality. Due to the viscous nature of AZ9260, it is extremely hard to evenly distribute the film on silicon substrate. Figure 4 shows developed AZ9260 (left) and the same film after etching with the Bosch Process (right).



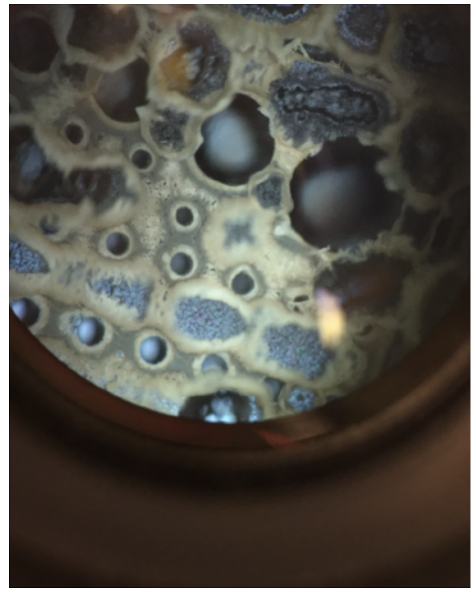


Figure 4 **Figure 4** **Developed AZ9260 Before (left) and After (right) Bosch Process Etching**

As can be seen, the uneven photoresist coating caused deteriorated feature shape.. Thus, a new process was designed to resolve this problem.

A hard mask is a mask made by depositing a layer of material on top of the target etching material. This hard mask can then be patterned using photoresist and a higher quality etching process. Silicon dioxide (SiO2) is one of the most common hard masks used when the target material is Si on account of its lattice matching and high selectivity with a fluorine dry (plasma) etch. The selectivity of SiO2 to silicon for Bosch process was experimentally tested to be 200 on a dummy wafer. Therefore, a 3.5 um thick of SiO2 was needed to grow on the silicon substrate to allow complete etching. However, when SiO2 is too thick, it can deform or even crack. Thus, a decision was made to use SiO2 as a hard mask to etch away the first 400um of silicon the silicon substrate. The SiO2 would then be removed and the chip would be realigned with photoresist to etch away the remaining silicon. Jesse Morgan, a PhD student under Professor Beling's group, helped to grow 2um of oxide in Virginie Tech's clean room on a wafer along with two testing dummies. Unfortunately, the oxide layer on the real chip had many material defects. The Bosch process etch was applied to less than stellar results as can be seen in Figure s.

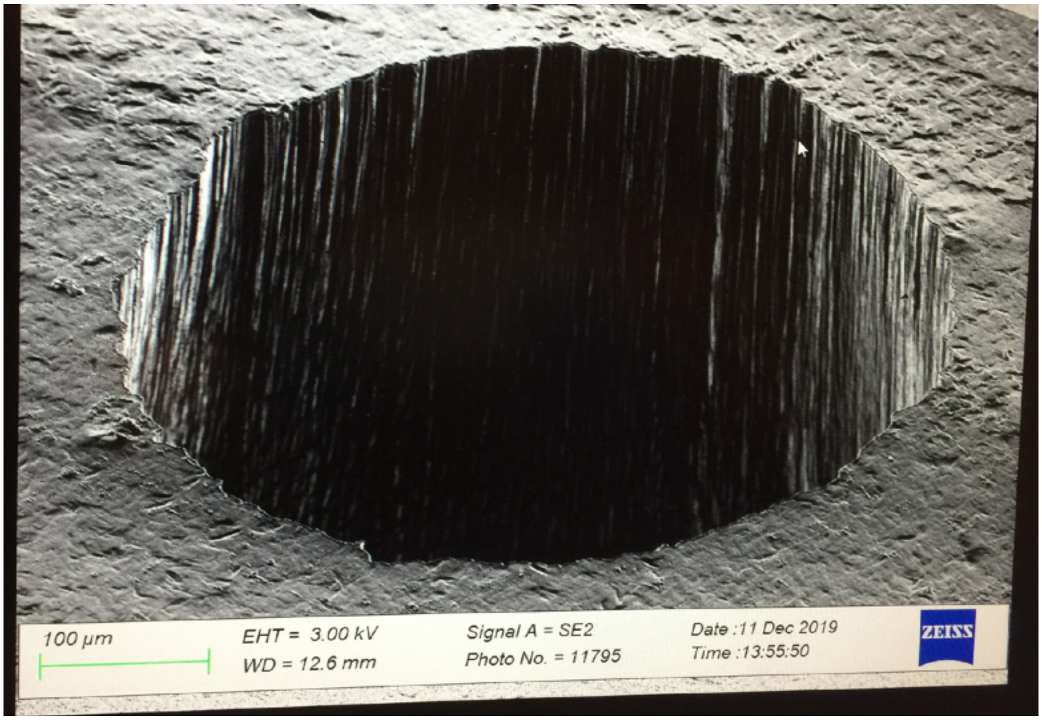


Figure s Scanning Electron Microscope Image of Silicon Dioxide Hard Mask Process Flow on Blank SOI Wafer

At the advisement of many graduate students, Aluminum was tried as an alternate hard mask. Dr. Micheal Cyberey helped deposit 0.4um of aluminum by sputtering onto the silicon substrate. I then developed AZ5214 photoresist on the aluminum and etched the desired pattern using Aluminum etchant type D [20]. Thus a hard mask of aluminum was achieved. According to prior literature ([21]), Bosch process etching does not chemically affect aluminum at all. Interestingly enough, when the chip to be used for the sensor went through Bosch process etching, it came out flat meaning nothing was etched. The patterned area (not covered by aluminum) turned green. By constantly monitoring the change of color, that green layer of unknown material was removed by buffering oxide etching (using wet Hydrufluoric acid, [22]) for a total of 20 minutes. This process flow is summarized in Figure 5.

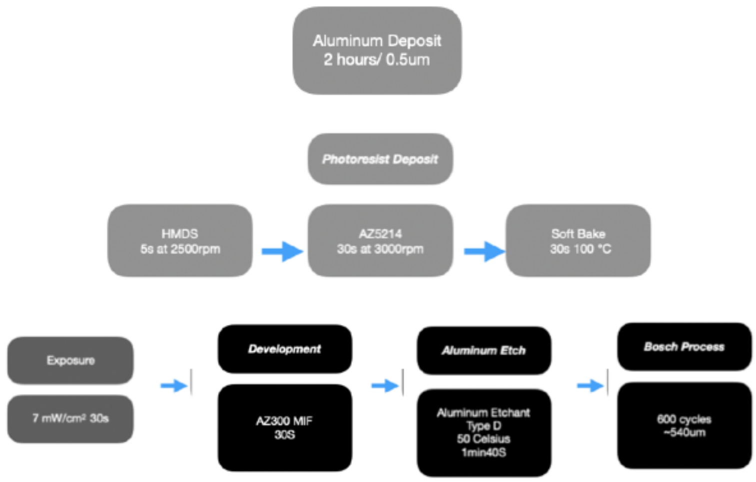


Figure 5 Final Designed Process Flow using Aluminum Hard Mask

This process was first demonstrated on a dummy silicon-on-insulator (SOI) wafer. A scanning electron microscope (SEM) image of the result is shown in Figure 6.

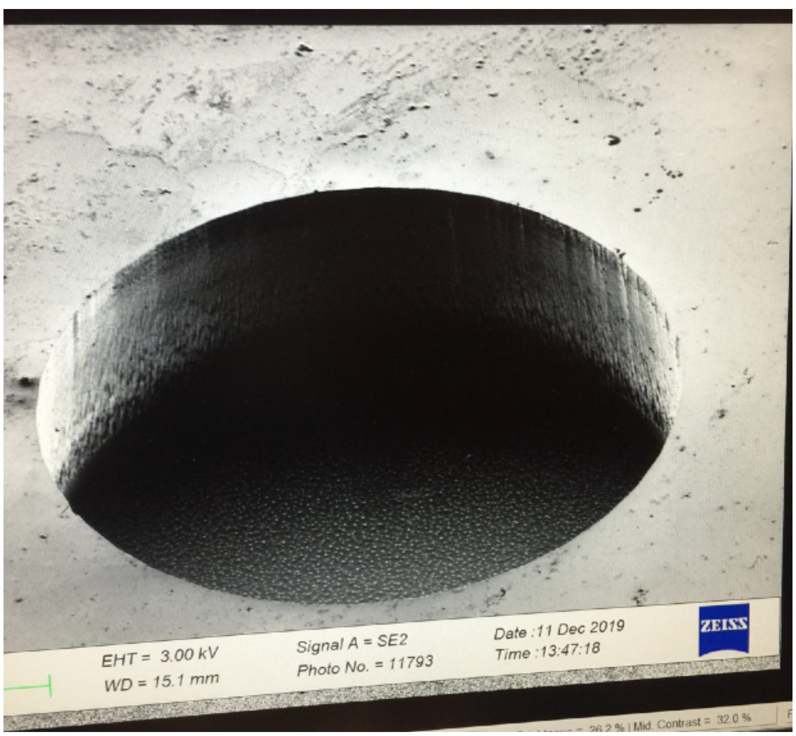


Figure 6 SEM Image of Aluminum Hard Mask Process on Blank SOI Wafer

Unfortunately, issues with the Oxford ICP RIE delayed final sensor fabrication and the actual attempt was not attempted until after the in-class demonstration. Two days after the demonstration, the etch was completed on the actual chip to create a finished sensor. As can be seen in Figure 7, two membranes were successfully cut around the resonators.

Figure 7 Completed Fabricated Sensor Using Aluminum Hard Mask Process

Circuitry and PCB

Our circuitry (and subsequently, the PCB) underwent three design iterations. The circuit served to carry out several functions summarized in the block diagram below (Figure xx).

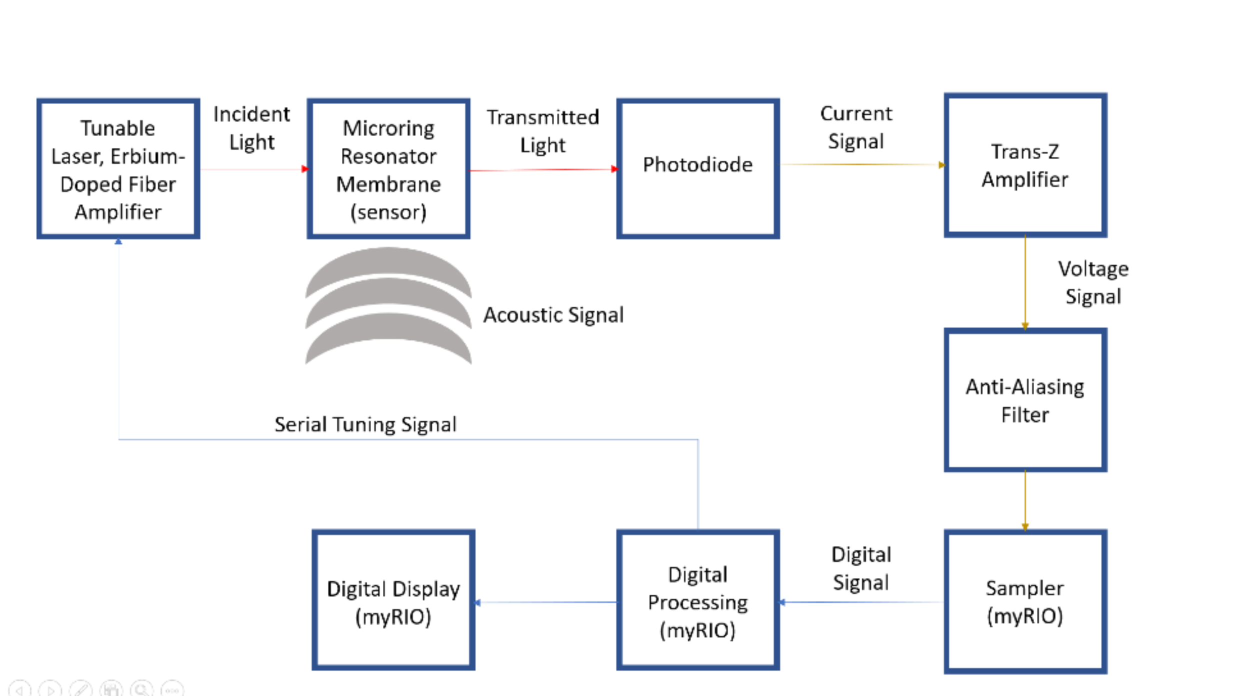


Figure xx Overall Project Block Diagram

The circuitry starts at the incident current signal from the photodiode, converts this current to a voltage on a corresponding linear scale in the trans-impedance amplifier, anti-aliasing filters the signal, and sends it to the myRIO's analog input pins for sampling. The circuit also contains the necessary components to send communications via UART with the tunable laser, The PCB contained connectors to interface with the different external systems.

Circuit Design

The current-to-voltage conversion stage was designed from pre-existing data on the micro-ring resonator chips. By wavelength sweeping the laser fed through erbium-doped fiber amplifiers to vary the intensity, Figure xy was generated comparing the photodiode current to wavelength at different laser intensities.

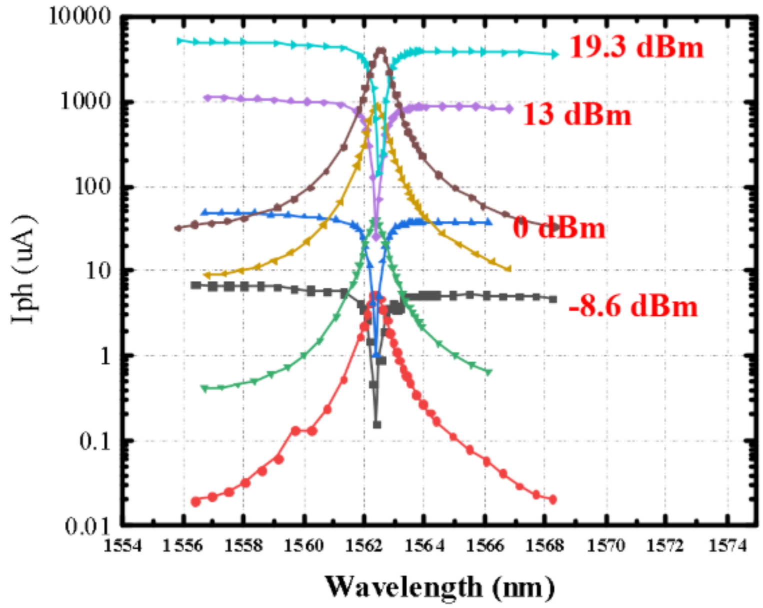


Figure xy Photocurrent vs. wavelength and laser intensity

From this, an incident beam of 0dBm (or 1mW) was chosen to give a photodiode current ranging from 10-1,000uA (or .01-1mA). This current range was chosen to maximize signal-to-noise ratio while also minimizing the thermal effects of a high intensity beam incident on the micro-ring. From this, a transimpedance amplifier was designed to convert the photodiode current into a samplable voltage. The schematic is shown in Figure xz.

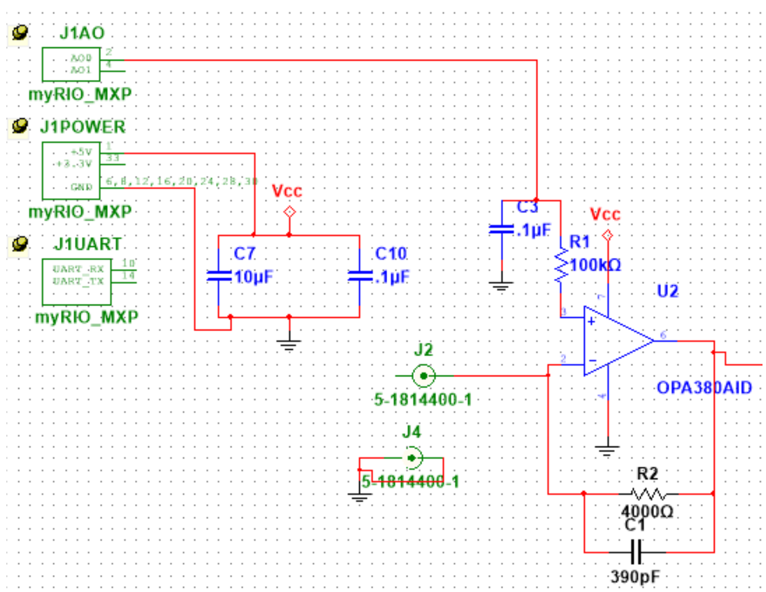


Figure xz Transimpedance Amplifier Schematic

The OPA380AID transimpedance amplifier [23] was chosen for its very low 1/f noise at our acoustic signal frequency, $10\frac{fA}{Hz^{1/2}}$ at 10kHz signals and 5V supply rails. Our supply rail was chosen as the 5V supply on the myRIO as it fits within the specifications of the OPA380. An output offset of 1V was set using the analog output pins of the myRIO as recommended in the datasheet. Given the input current range of .01mA to 1mA and the available voltage without clipping from 1V to 5V as well as a desired bandwidth of 100kHz, the feedback resistor and capacitor were calculated as:

$$R_f = \frac{5V - 1V}{1mA - .01mA} \approx 4000\Omega$$

$$C_f = \frac{1}{2\pi B R_f} = \frac{1}{2\pi(100kHz)(4k\Omega)} \approx 390pF$$

Thus, the transimpedance amplifier takes an input current ranging from .01mA to 1mA and amplifies it to a voltage from 1V to 5V with noise stability from the feedback capacitor.

This voltage is then passed through a fourth-order butterworth characteristic low-pass sallen-key filter for anti-aliasing (Figure yx).

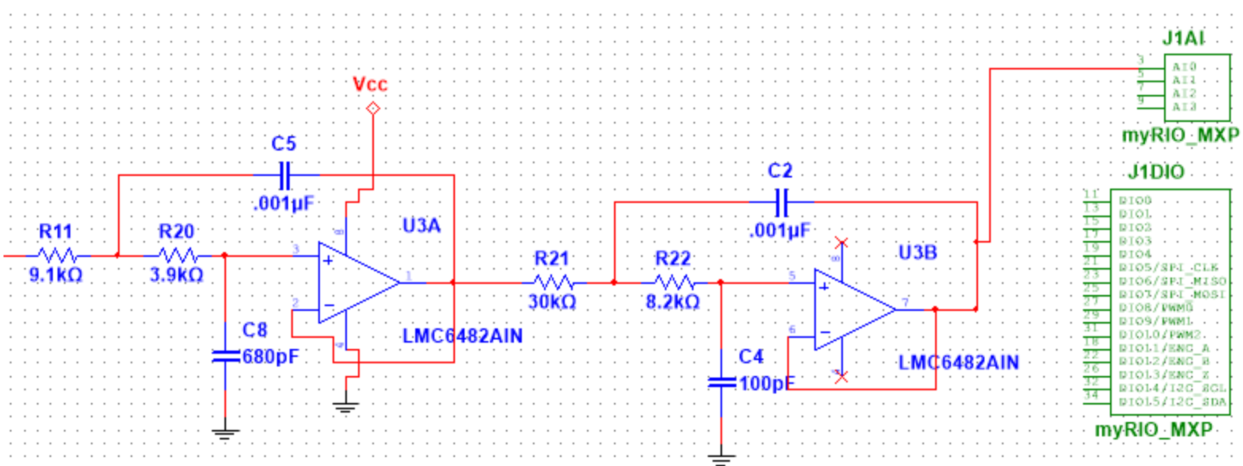


Figure yx - Anti-Aliasing Filter Schematic

The myRIO is able to sample at a maximum rate of 500kHz with 12 bits of resolution giving a Nyquist rate of 250kHz. The attenuation needed at the Nyquist rate was calculated as:

$$\alpha = \frac{1}{2^{12}} \approx -72dB$$

Given the 4th-order system has a slope of -80dB/decade, the cut-off frequency to attain -72dB at 250kHz was calculated as:

$$f_c = 250kHz * 10^{-72/80} \approx 31kHz$$

Given this corner frequency and Q values of 0.5496 and 1.3065 to cascade into a Butterworth system (Q = .707), the two filters were designed. It was desired to use the same 5V myRIO supply voltage as used for the transimpedance amplifier. Thus, the LMC6482AIN operational amplifier ([24]) was chosen for its low supply voltage operation. The output then feeds into an analog input pin of the myRIO for sampling. Simulating with an ideal current source, this circuit yielded the correct output at .01mA (1V), 1mA (5V), cut-off frequency (31kHz), and response (Butterworth) (Figures a-c).

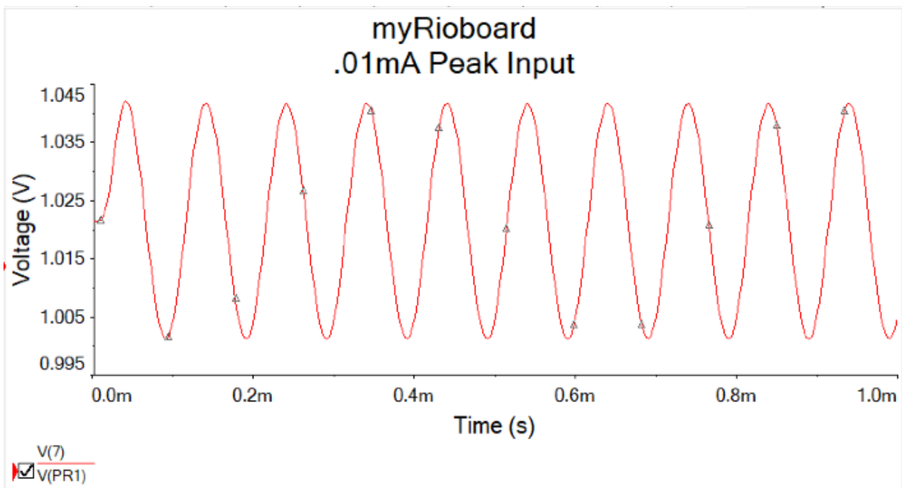


Figure a .01mA Current Output

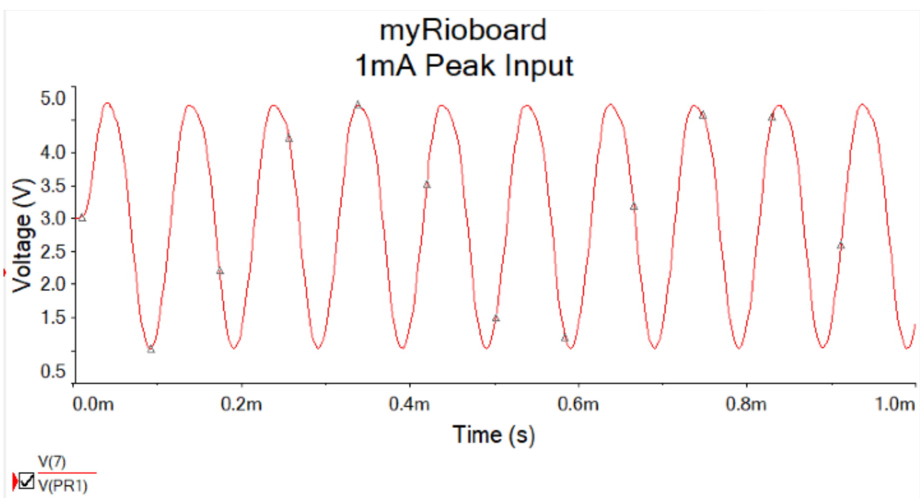


Figure b 1mA Current Output

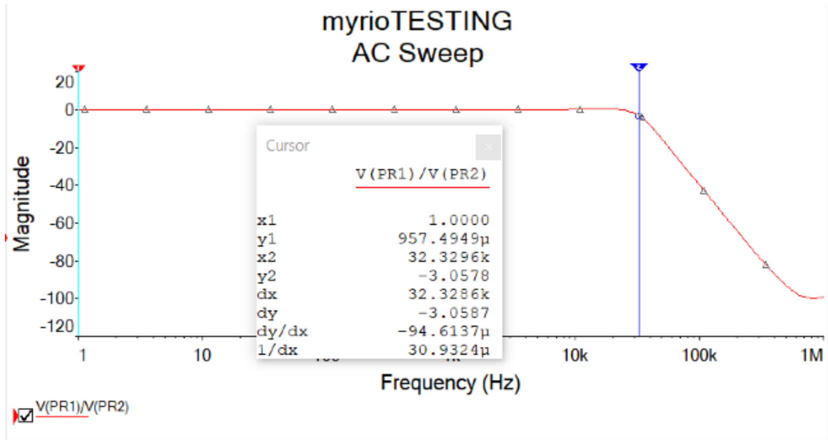


Figure c Filter Frequency Response

Concurrently, the circuit must also be able to create and send the RS232 levels necessary for communication with the tunable laser. This was first implemented in the third iteration of the circuit with direct pins to Vcc, ground, and the myRIO's UART TX and RX pins for interfacing with a breakout board ([25]). In the third iteration of the circuit, the RS232 levels were reached using the MAX232EPE+ chip ([26]) then directly connected to a female serial connector ([27]). Capacitors were connected to the MAX232EPE+ as advised in the component datasheet (Figure yy).

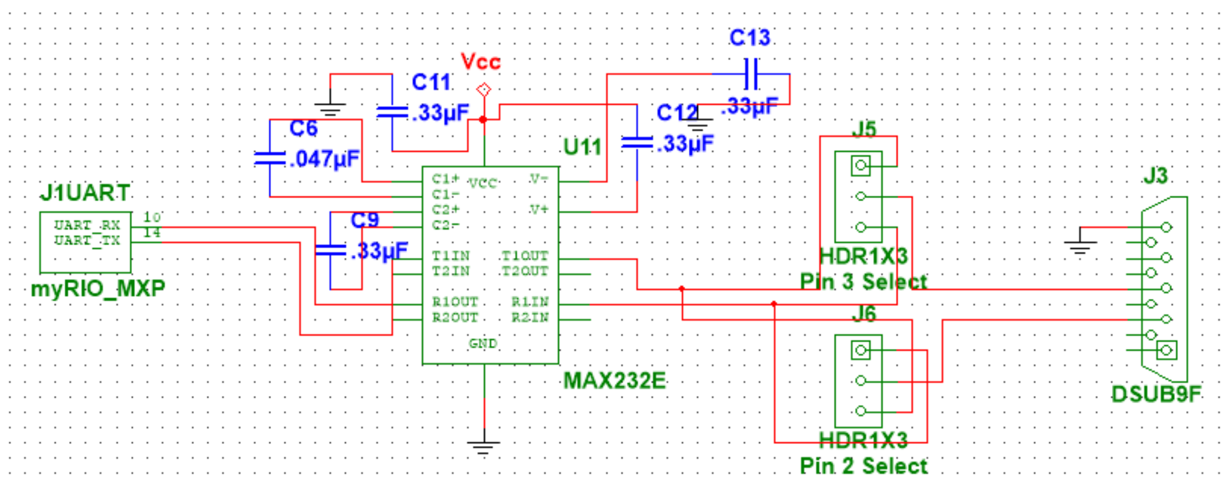


Figure yy RS232 Serial Communication Schematic

Components J5 and J6 are triple pin jumpers ([28]) used to switch the RX and TX lines if necessary. This was implemented because the RS232 standards of the tuning laser were not made explicitly clear [29].

PCB Design

The PCB was designed to both interface with the external components necessary as well as implement the circuitry described above (Figure yz).]

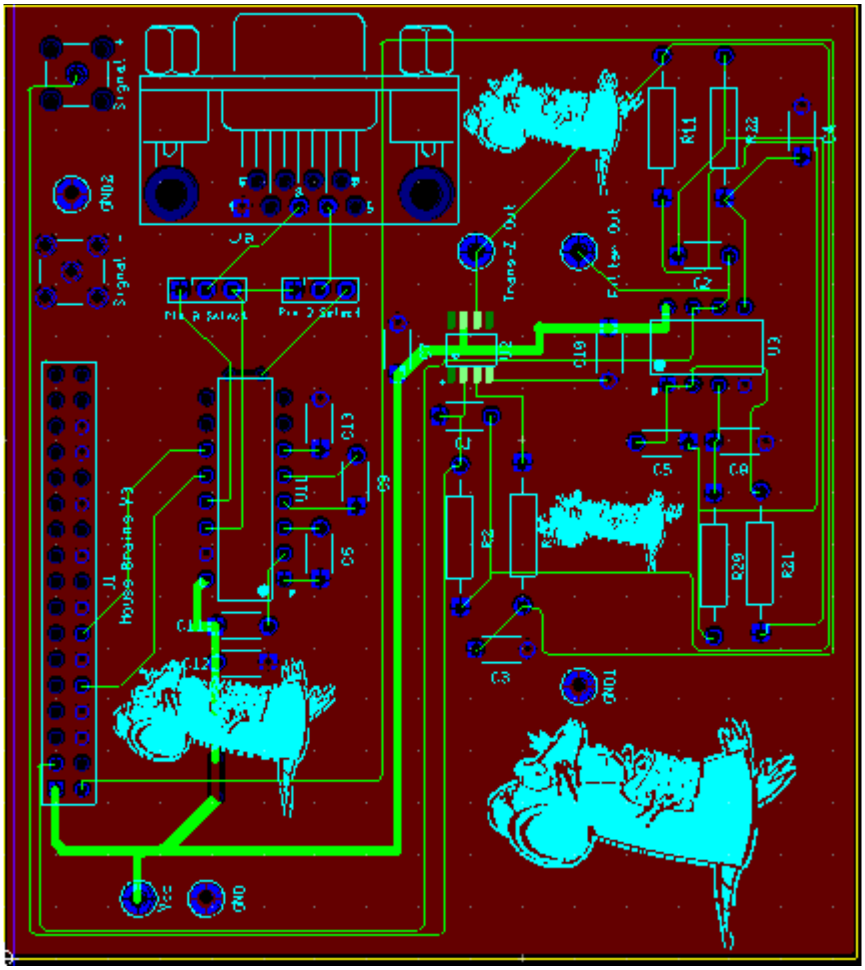


Figure zz Final PCB Design

Connection to the myRIO was implemented through a pin connector using the 1-534206-7 package ([30]). This could then be directly connected to the myRIO through an MXP extender cable ([31]).

The input photocurrent was to come from SMA connectors, so SMA connectors ([32]) were used on the board. These currents then fed directly fed into the transimpedance amplifier. The AID package of the OPA380 ([23]) and the AIN package of the LMC6482 ([24]) were chosen as they were easier to solder than the smaller ICs available. Red (power, [33]), white (signal, [34]), and black (ground, [35]) test pins were placed in important spots throughout the circuit to test operation.

The PCB was designed to attempt to minimize the distance the power lined travelled. It was also designed to ensure the MXP extender could connect to the pins. Finally, distinctive labels and images were added for uniqueness. The soldered board is shown below (Figure p).

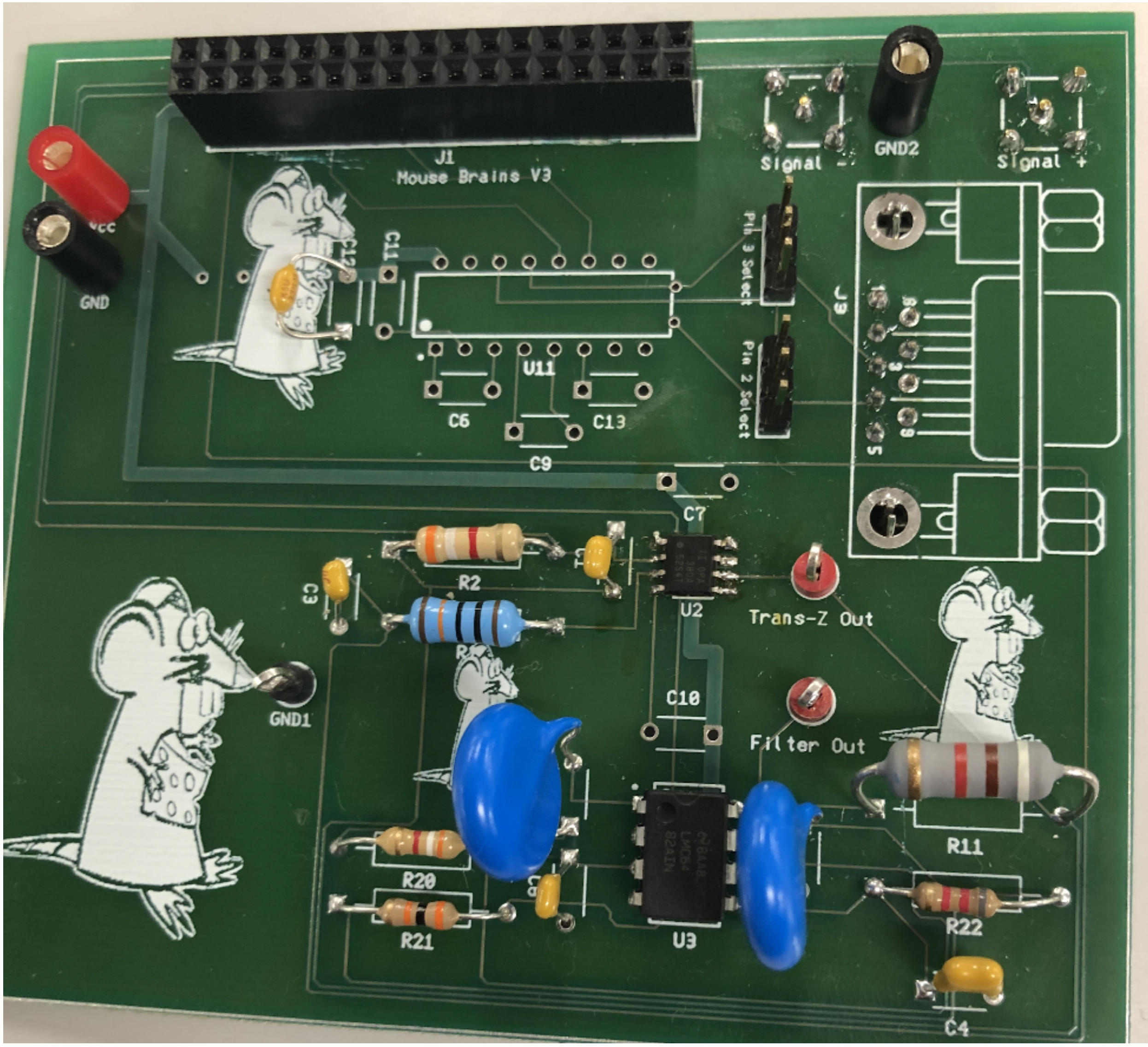


Figure p Soldered Final Board with Unadded RS232 Expansion

Problems and Modification

The main circuitry was not modified after its original design. The R232 functionality was added in the second iteration to interface with a breakout board before its final design with on-board RS232 level setting and output.

The RS232 section of the board was neither soldered nor tested as it was not necessary. The laser could be controlled through the GPIB USB interface more easily, and delays in the sensor fabrication altered our demo thus not requiring this functionality.

The other used components of the board did not have issues with functionality. However, a mis-soldering of the connector pins for the myRIO did requiring desoldering by 3W to prevent unreliability. The transimpedance amplifier proved very difficult to test as an ideal current source does not really exist. However, it proved testable using a green LED as a photodetector.

Software

Our system featured two sets of software, both written in LabVIEW. The first set calibrated the system for demonstrating sensor functionality. The second sampled and displayed the output of the sensor in real-time.

Calibration Software

Calibration required an algorithm to determine where to bias the laser. This subsequently required the ability to tune the laser from the program (Figure za).

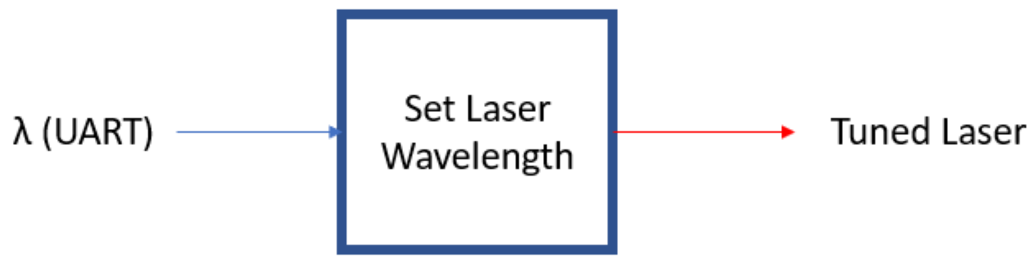


Figure za Laser Tuning

This process was completed by modifying original LabVIEW written for the tunable laser [36]. After initializing the connection, the wavelength was set by passing in a value and setting the units as nanometers through a false input to the unit input.

Using this, the calibration algorithm needs to sweep the laser wavelength while measuring the output from the photodiode to construct a bode plot of the resonance curve. The laser tunes by rotating a diffraction grating, so we were advised to always adjust from low to high wavelengths to ensure proper calibration. Once the bode plot is created, it is necessary to determine the point of highest non-linearity using a discrete derivative. The laser can then be tuned to this point, again restarting from low wavelengths. The wavelengths 1561-1565nm were chosen as they contained a resonance peak. This is summarized in the block diagram (Figure zb).

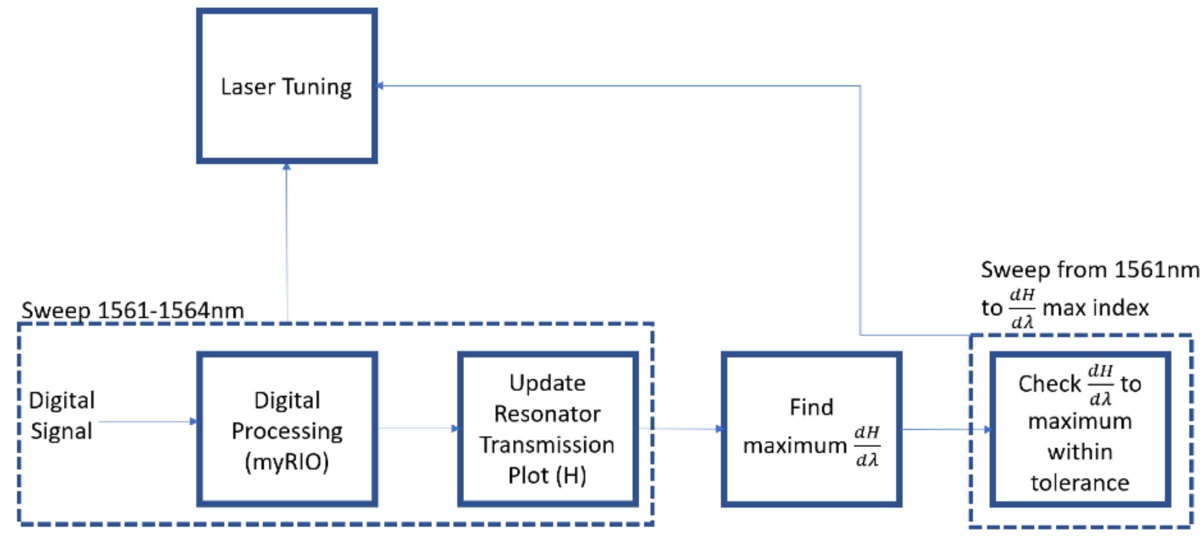


Figure zb Laser Calibration Algorithm

This algorithm was implemented using LabVIEW with the real-time myRIO microcontroller. This was chosen as the laser software was already written in LabVIEW and the data did not need to be taken as waveforms.

To make best use of real-time operation, a RT FIFO was populated with the wavelengths which were then used to tune the laser, read out the circuitry, and update the graph. First, the FIFO and laser visa were initialized (Figure zc).

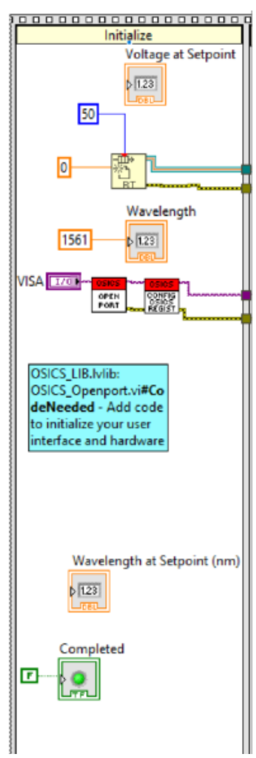


Figure zc Initialization for Calibration

Next, the FIFO was populated with wavelengths (Figure zd).

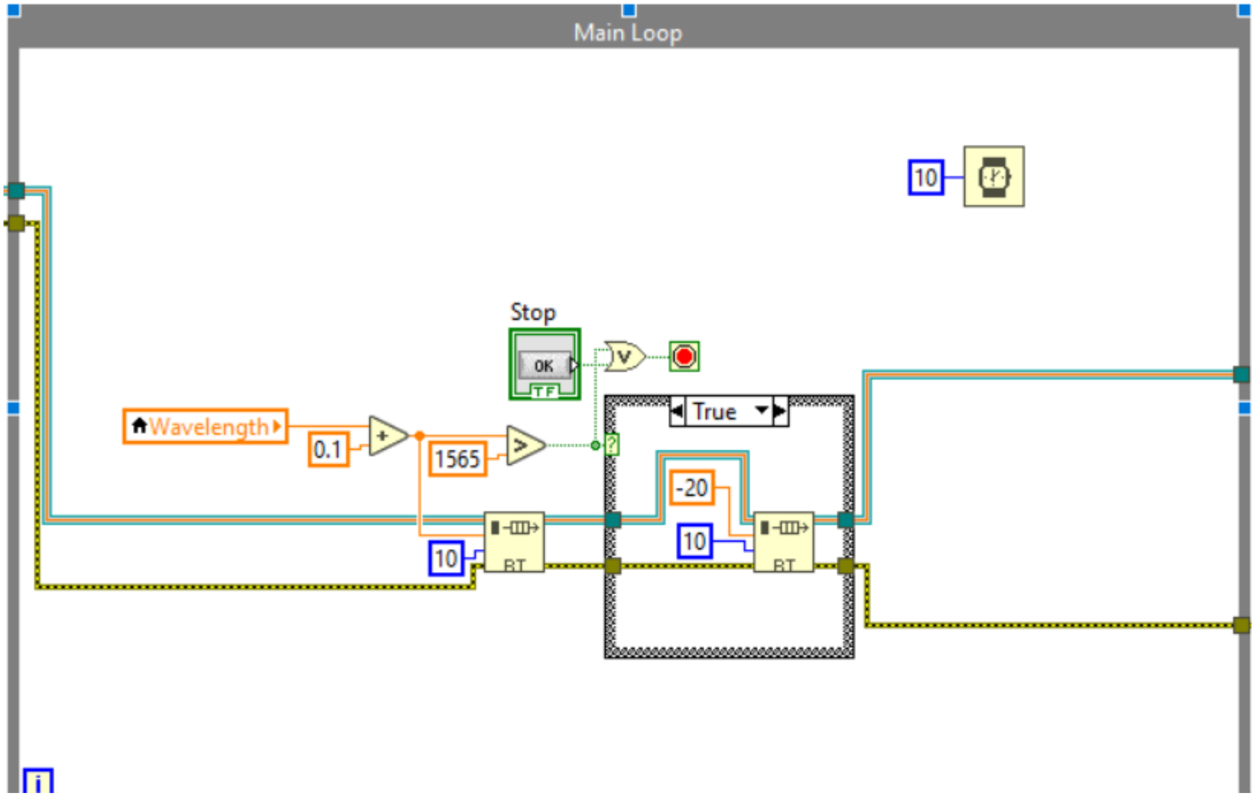


Figure zd FIFO Population for Calibration

The wavelength values from the FIFO were then read out and used to tune the laser. The time-averaged circuit voltage at this wavelength was then read and used to update the bode plot (Figure ze).

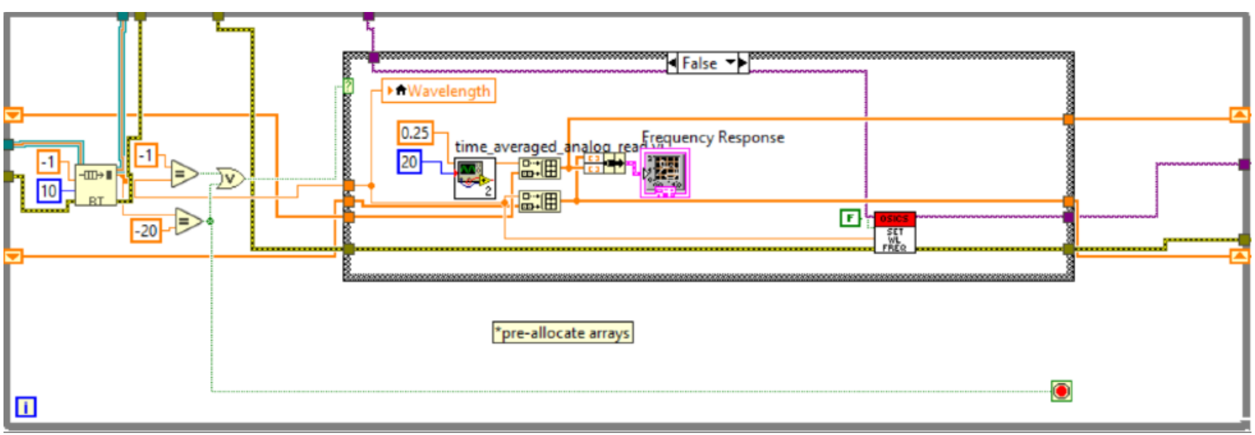


Figure ze Calibration Data Collection and Graphing

The "time_averaged_analog_read" VI was written to output the 1V analog output necessary to prevent clipping and to take an input number of samples across an amount of time and output the average and standard deviations (Figure zf).

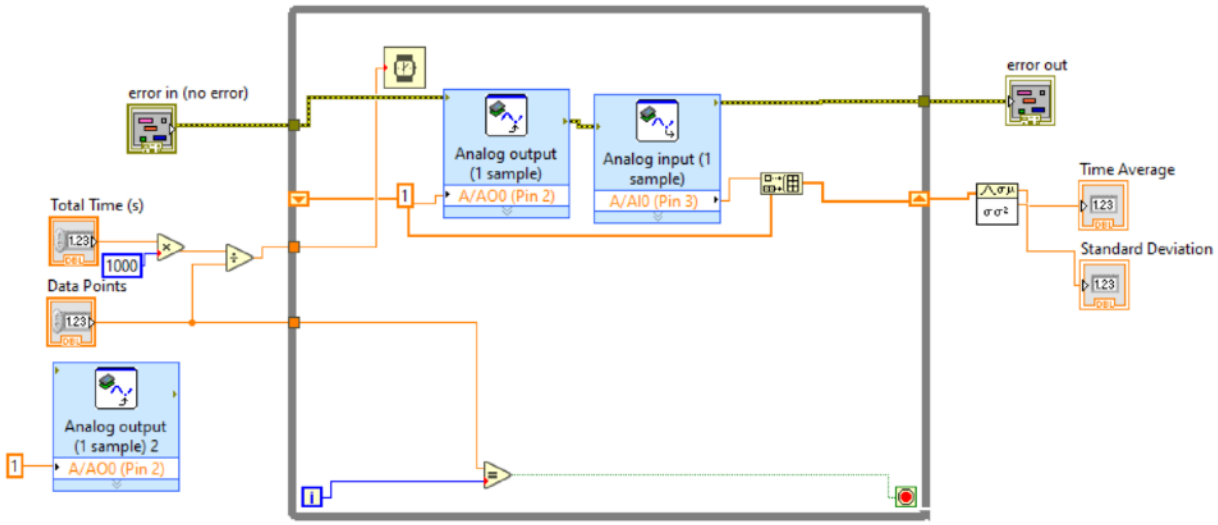


Figure zf Time-Averaged Analog Read for Calibration

The discrete derivative of this data was then taken and used to calculate and display the wavelength which showed the highest change in voltage, ignoring edge cases, and displays the wavelength and its corresponding voltage value (Figure zg).

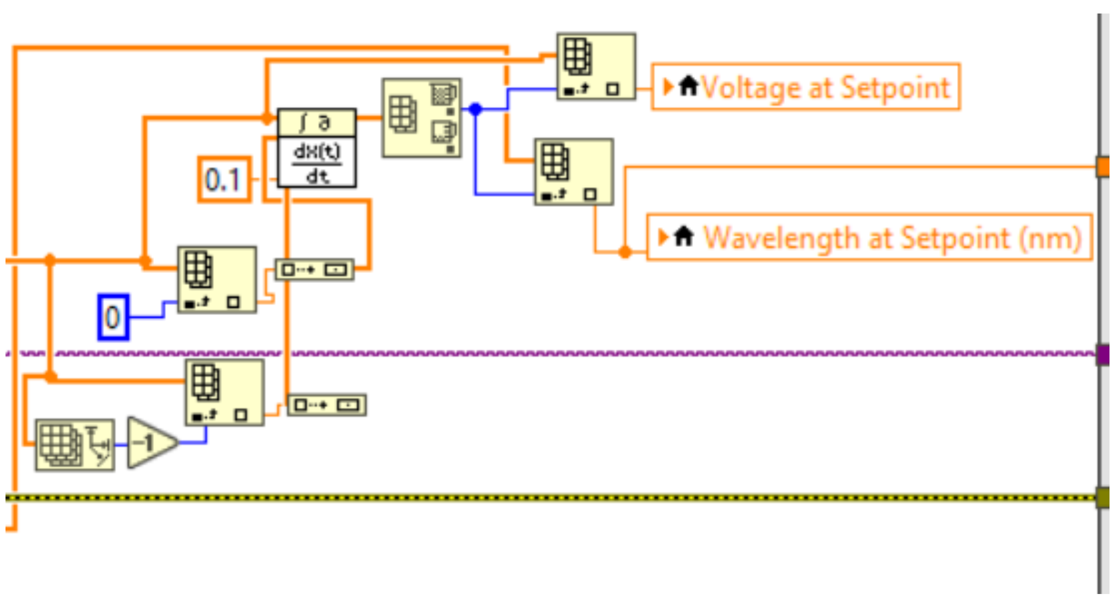


Figure zg Calibration Maximum Finding

The wavelength is then set, sweeping from the lower limit (Figure zh).

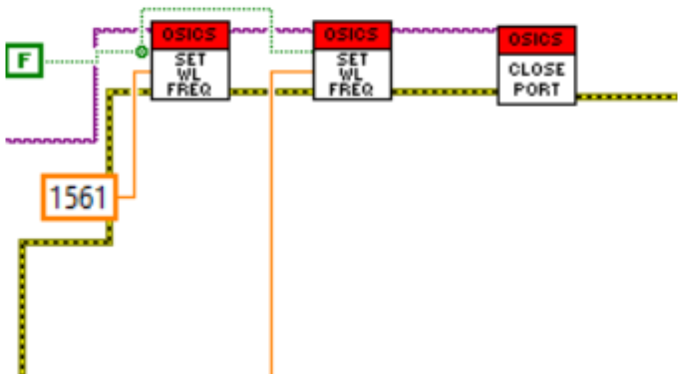


Figure zh Wavelength Setting

Finally, the myRIO port is closed. This results in the following front panel after running (Figure zi).

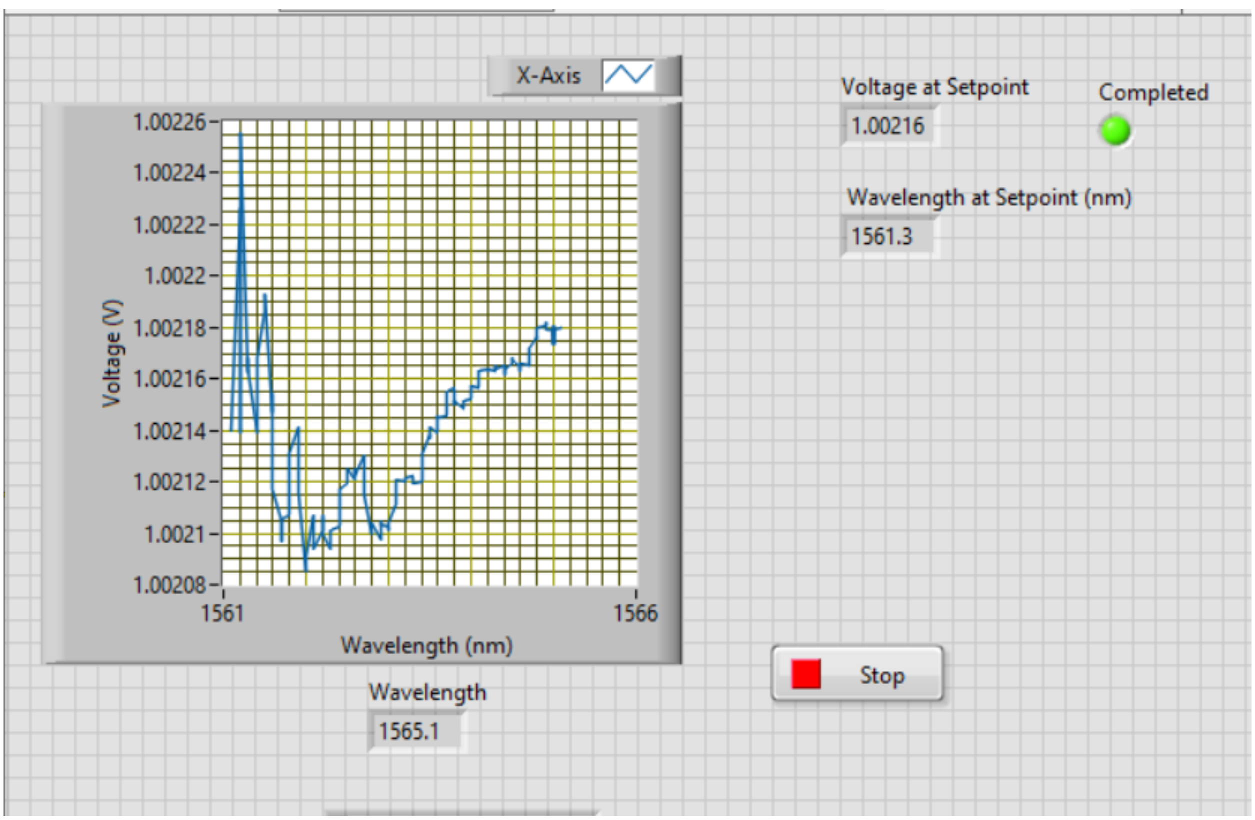


Figure zi Calibration Front Panel After Trial, No Signal (approximately constant 1V)

The decision to create the calibration software in the real-time myRIO microcontroller means it is not directly integratable with the real-time sampling and display program demonstrated. However, it greatly simplified using the laser tuning functions. This software was not directly tested on the sensor as our sensor fabrication was delayed by clean room renovations. As such, its testing was limited to displaying the 1V input signal received through the circuitry (or other constant values).

Sample and Display Software

This portion of the project sought to take amplified and filtered waveforms from the PCB and create a real-time display on a computer, all in a single integrated and connected package.

The sampling was done via the NI myRIO's high-throughput FPGA personality. The myRIO has ten total analog inputs and outputs but only one of each was necessary in this project. The signal coming into the analog input was coming from the output of the PCB which was designed to create a voltage from 0-5V. This matches the analog input range of the MyRIO. A DC offset through the analog output was also to be provided to the circuitry to prevent clipping. The myRIO was programmed using LabVIEW, leveraging the strong compatibility of the hardware and software because they are both produced by National Instruments. One of the key advantages of using the myRIO is the wide range of FPGA tools available. The LabVIEW project began with the initialization of an FPGA target and the initialization of a queue data structure (Figure ta). The queue was initialized to hold integers because the values received by the ADC are 12-bit unsigned integers. Since the 16-bit unsigned integer data type was used in LabVIEW, the four most significant bits are unused. These integers are bundled into arrays of which the queue can hold ten. LabVIEW's default overflow is to kick the one closest to the beginning of the queue to make space for the next array. This is important because the latency of the waveform graph is not affected as much.

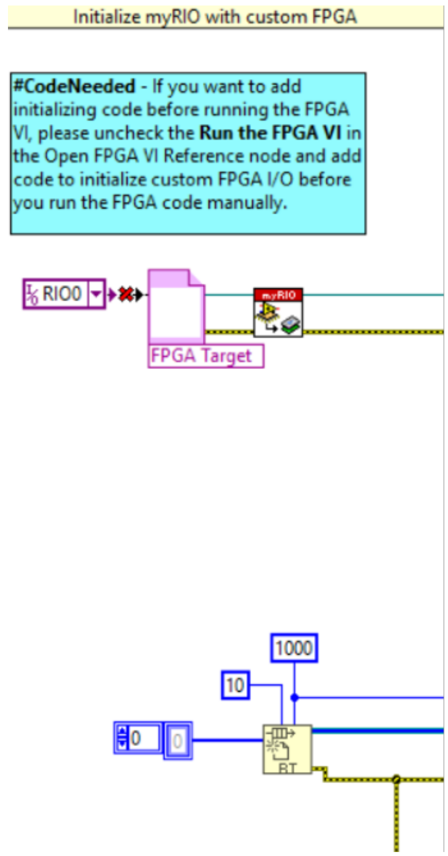


Figure ta LabVIEW Initialization Segment including FPGA target block and queue block

The next portion of the LabVIEW program is acquiring and processing the incoming data. The incoming data went to a real time while loop block for data storage. Since there was difficulty reading the output directly, the FPGA target interface to receive the value at the analog input directly. This allowed us to use two invoke methods in series, the first to read out the number of data points and wait until there were one thousand. The next invoke method then received the block of a thousand data points and added them to a queue. The real time loop also included system ready and button indicators, and analog offset and sample rate inputs. This portion is shown in Figure tb.

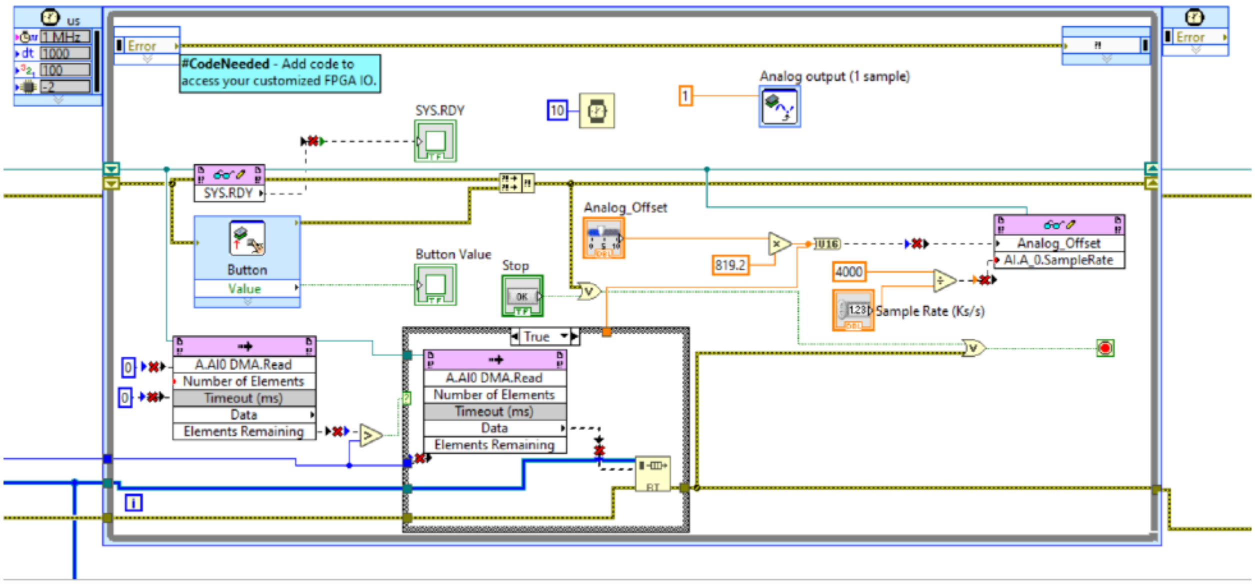


Figure tb LabVIEW Real Time Block Diagram for Data Acquisition and Processing

The data from the queue then goes below to the second loop where it is fed into a waveform graph. The data values are first scaled by a double value to display them in terms of volts. Since the total range is 5V and the number of bits is 12, the max integer number is 4095 and the bits per volt is 4096/5 or 819.2. This is then input into a bundle that contains the x0, time step, and voltages. This section is shown in Figure tc.

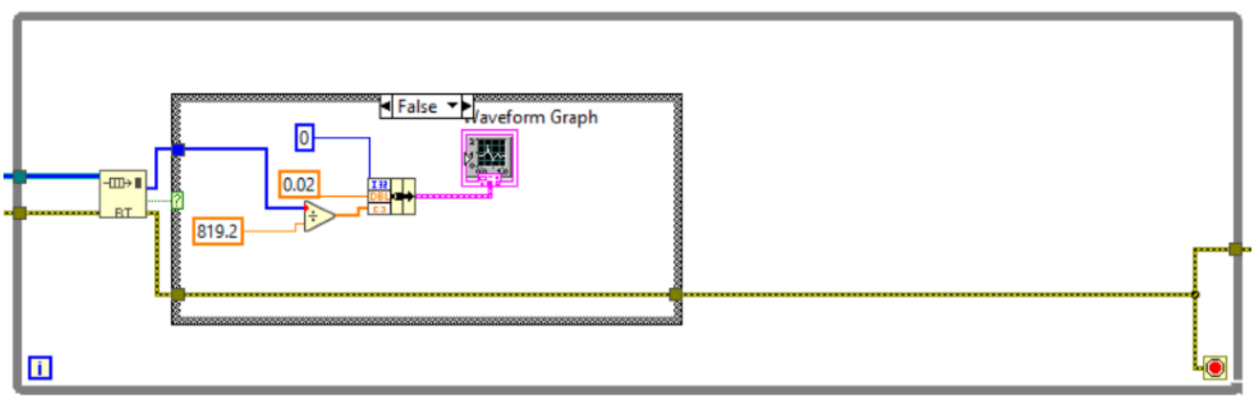


Figure tc LabVIEW Block Diagram for Data Display

The last section of the LabVIEW program is the close section. This contained a bundle that combined all of the separate error values and input them into the close function for the queue. This is displayed in Figure td.

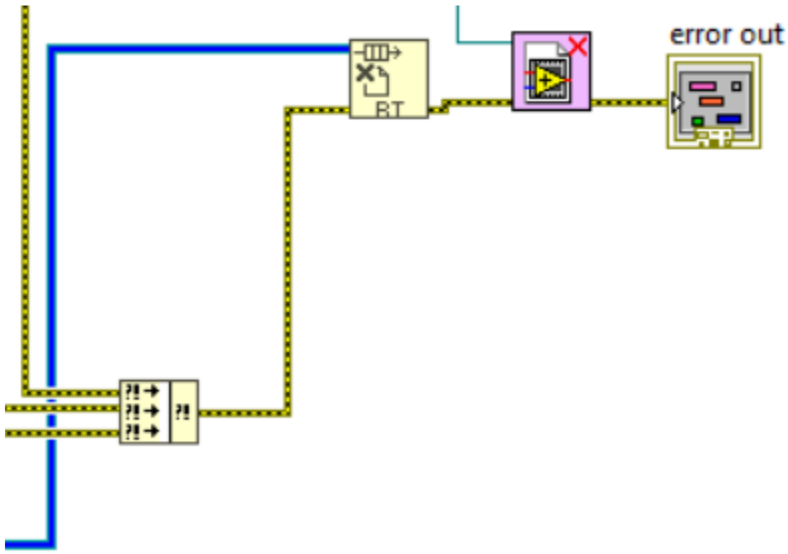


Figure td LabVIEW Close Section

The front panel of the LabView program was necessary for two main purposes: the analog offset input and the waveform graph. However there was a stop button that allowed the user to halt the program. This was useful if the user wanted to pause the graph and see what was being displayed at that current moment. There was also a sample rate input but this was exclusively held at 250 KHz during actual testing although it defaults to 10 KHz upon reopening the program. The final block was the error out block. These components are displayed in there testing configuration in Figure te.

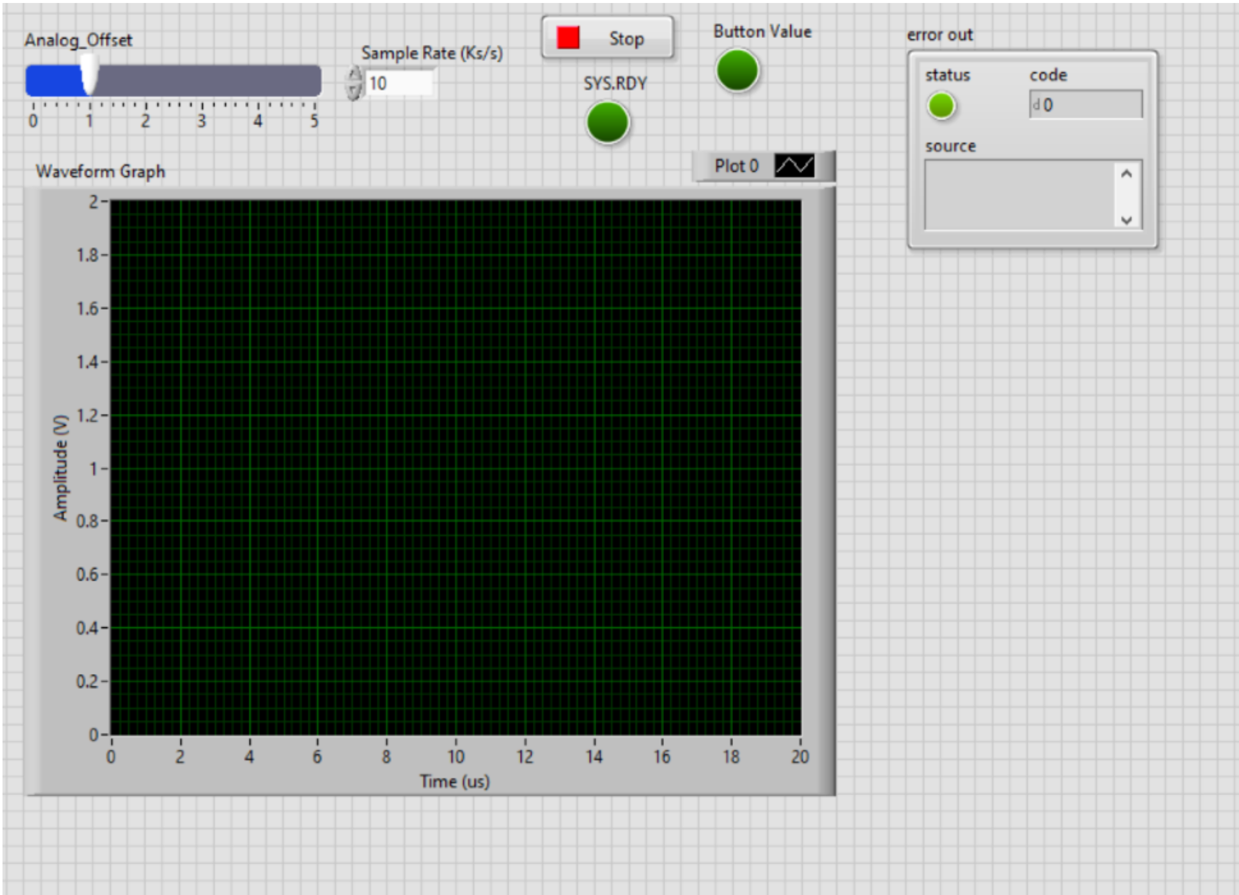
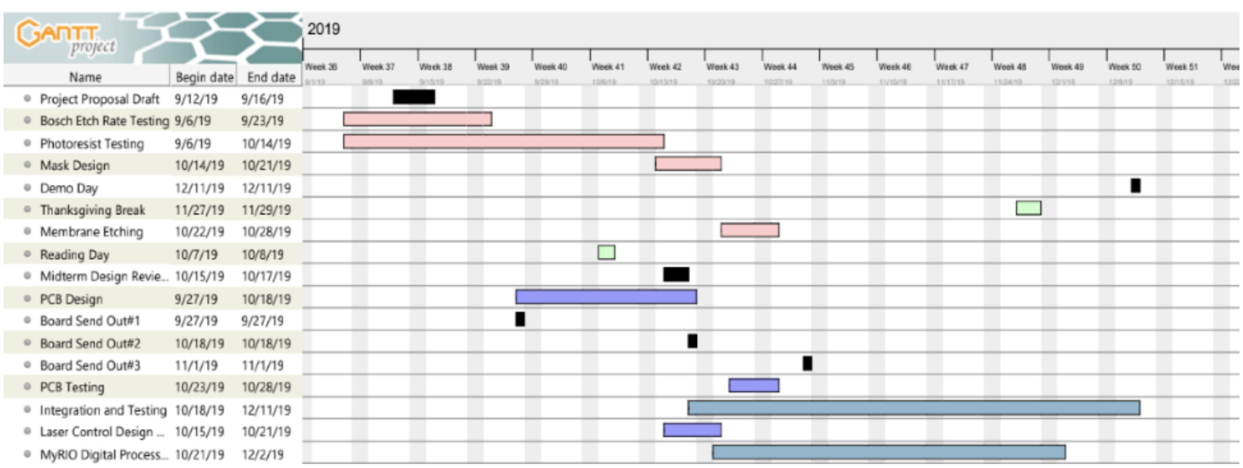


Figure te LabVIEW Front Panel for Data Acquisition and Display

Project Timeline

Our initial Gantt chart is shown in Figure g.



Color	Meaning
	Deadline

	MyRIO Programming & Testing
	Clean Room
	PCB & Laser Programming & Testing
	Breaks

Figure g Initial Gantt Chart

The actual completion of the project largely diverged in the changes to the process and demonstration. First, the photoresist fabrication process did not yield the desired results. Additional time was then spent on alternate fabrication methods. Subsequent delays in the fabrication process then altered our demonstration. We had to develop a circuit to demonstrate the successful completion of the hardware project. These changes are reflected in Figure g2.

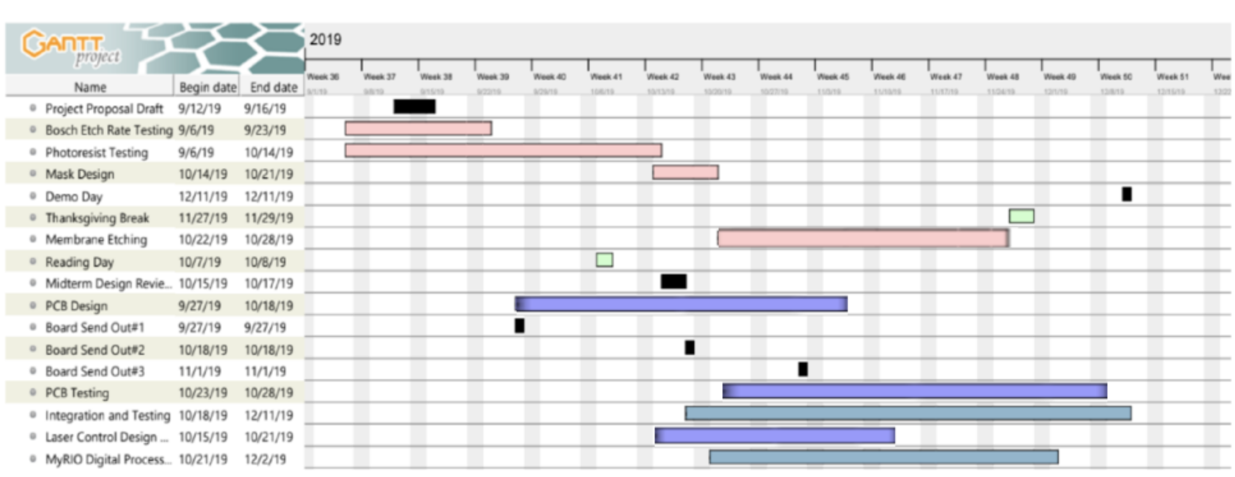


Figure g2 Actual Gantt Chart (same code as Figure g).

This section should include the Gantt chart from your proposal as well as a final chart (showing the differences). You should explain the following and how your time lines changed throughout the course of the semester.

The components of our project were able to be developed almost entirely in parallel after a calibration phase of figuring out the exact constraints and connections of each component. The fabrication could be completed entirely independently. The circuitry and PCB to be designed or tested for functionality. The software could be tested without the PCB before integration with the PCB. At the end, we had a period of integrating our efforts to create our demonstration.

The general order of our work was dictated by deadlines and the individual working on each part. Xiangwen focused on the fabrication after early stages, and her work was completed independently. Adam initially created PCBs to coincide with the board sendout deadlines, while

Drew worked on the FPGA programming for signal read-out in parallel. Adam worked on the calibration software in the down time between waiting for iterations of PCBs and parts to come in. This allowed us to have a functioning subsystem demo of the calibration software as well as complete our full demonstration on time.

Test Plan

You should show the test plan from your proposal and explain how you followed this plan or how you modified it. You should explain each of your testing procedures, and how you divided your system into testable sub modules. If testing caused a partial redesign of your device, you should explain how you arrived at that conclusion and how it influenced your redesign.

Our original test plan featured two separate parts: PCB testing (Figure zj) and system testing (Figure zk).

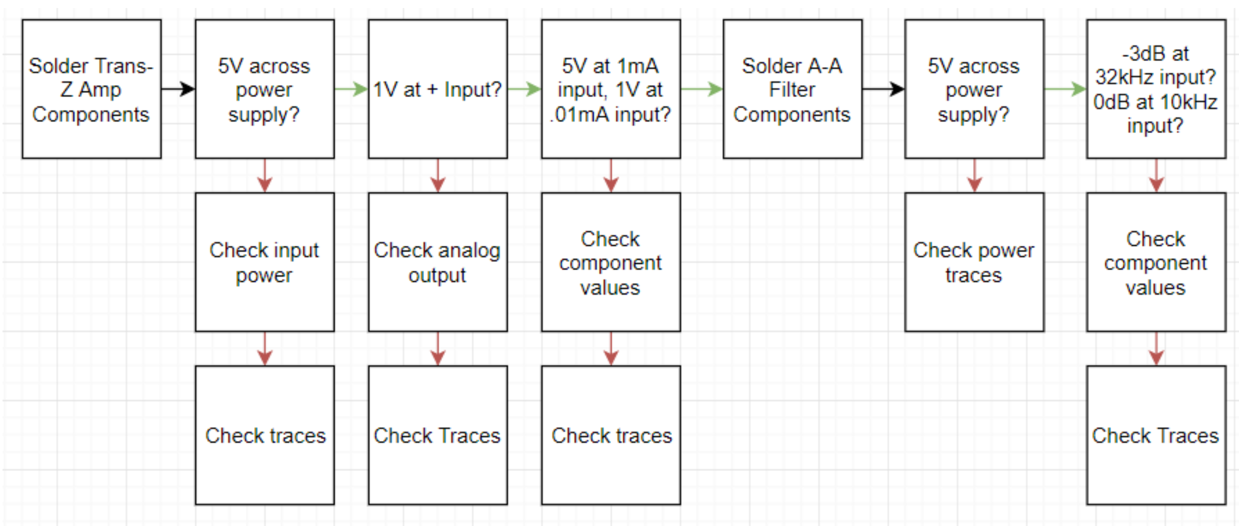


Figure zj Original PCB Test Plan

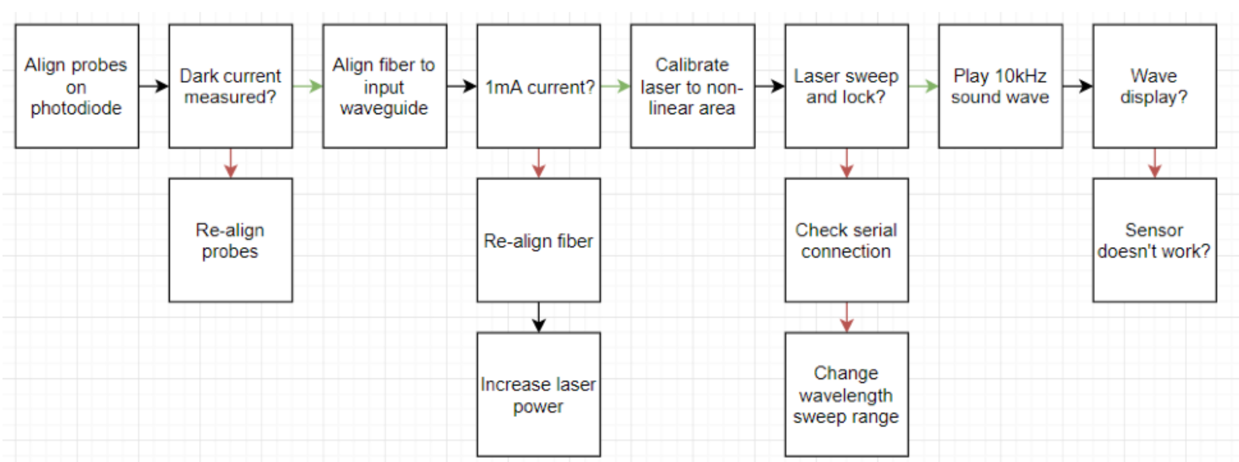


Figure zk Original System Test Plan

The test plan for the PCB stayed entirely intact and all tests passed on the first try. One unforeseen issue was the difficulty in directly testing the functionality of the trans-impedance amplifier. This was overcome by using a calibrated LED current to demonstrate a trans-impedance that was expected.

The system test plan was entirely redesigned when our demo shifted from a sensor demonstration to a demonstration with an LED as a simulated photodiode. Now, our system test plan revolves around putting two LEDs back-to-back, one with a sinusoidal wave passing through it, and connecting the output of this LED to the input of the circuitry (Figure r). We expected to see what was on the oscilloscope, 1V peaks at a spacing of 2us, which we did.

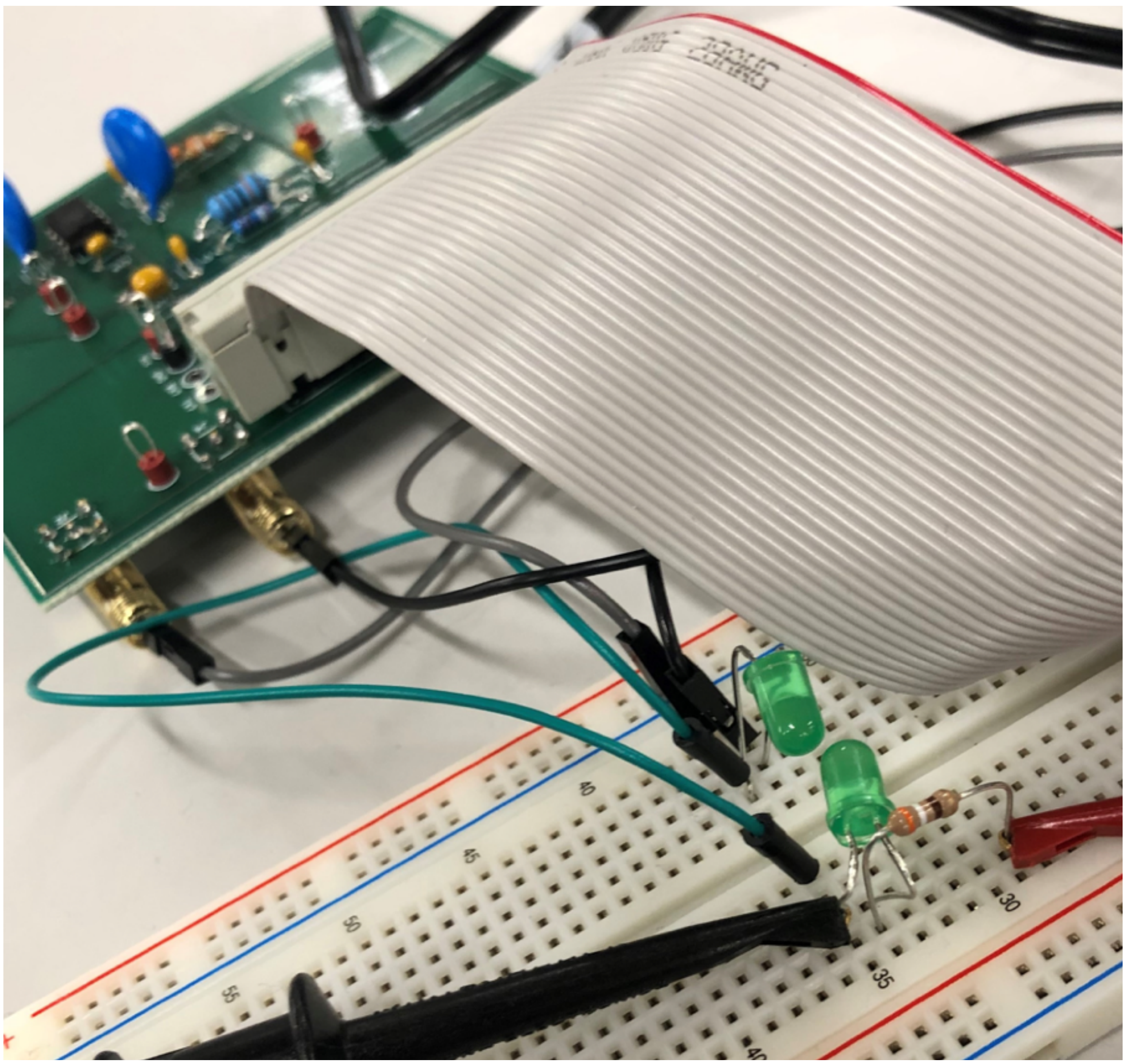


Figure r Testing and Demonstration Setup

Additional test plans needed to be added at the software level. The calibration software was tested by running example sweeps, ensuring the laser changed frequency, and checking that the maximum was correctly extracted using probes and visual estimates from the created graph.

The maximum extraction was initially not correct as it tended towards huge changes at the edges of the array, but this was fixed by adding corrections for the array ends. The real-time display software was tested by inputting signals across the frequency range of the circuitry and checking that all amplitudes are properly displayed in the LabVIEW front panel (checking against an oscilloscope). We did not have issues with the sampling and display of the signal, but we were not able to get a 1V analog output using the FPGA despite numerous tries. This included testing with a digital multimeter directly on the myRIO analog pins instead of the circuitry.

The fabrication process flow was tested through direct measurements of chips as well as scanning electron microscope (SEM) images. As shown in the technical section, the SEM images provided clear evidence of etch and material quality. A diffraction-gated microscope was also used to determine if photoresist had fully developed.

Final Results

The fabrication process flow was not implemented to make an actual sensor on account of clean room issues. However, the process flow was fully designed and demonstrated on a dummy wafer. In this respect, the fabrication portion of our project was a success as we knew finishing the fabrication was a lofty goal.

The circuitry and software portion of our project was a success relative to our proposal. The circuit completely worked in producing correct current gain, filtering, and interfacing with the myRIO. The software on the myRIO FPGA was successfully able to sample, filter, and display this information in real-time as desired. We could not make the analog output of the FGPA work, however it did not seem to introduce clipping on the signal. This fully met the expectations of our proposal as we conditioned the signal and displayed it in real-time.

The calibration software for the laser, while unused, was also successful. It interfaced correctly with our PCB, produced a bode plot while interfacing with the laser, calculated the setpoint, and set the laser at this setpoint. RS232 communication was not implemented, but it was not necessary as the GPIB interface still worked. This functionality was not, however, fully tested on the actual resonator as we did not finish the sensor to test. This software was not part of our original proposal, but will be very useful in continuing research.

Costs

A spreadsheet was produced estimating the total cost of our demo (see Appendix A1). Through this analysis, it was found the single board cost at $211.71. This does not include clean room fees, which ostensibly could put this number in the thousands as clean room usage is $1,000 per month per student. This is not directly attributable to the project, however, as this includes all research happening in that time period. The most significant costs came in RS232 components, including a $150 antiquated serial cable, a breakout board to figure out the RS232 levels, and the integrated circuit to set the RS232 levels. Ideally, in a mass production (10,000+ items), research-style lasers would not be used. Instead, a pre-biased semiconductor laser, which costs $1 or less, could be used entirely bypassing these components. With this analysis in mind, the unit price for a mass produced version of our board drops to $25. Furthermore, the sensor could be completed almost entirely in a foundry, which would remove the cost of clean room use and drop production costs to less than a dollar.

Future Work

Our largest difficulty came in the scope of the project. The design of the process flow itself was very time consuming and required a large amount of outside assistance. On account of this, we were very unfocused on the other components of the project. We managed to design our read-out circuitry well, but we were not exactly sure how we were going to demonstrate our project.

We were not able to finish our sensor before the demonstration on account of clean room renovations shutting down the machines we needed to finish the actual fabrication of our sensor. On one hand, our process flow is well documented, but the sensor, which we put a very large amount of time into, did not yield any type of demo. This also required us to entirely re-create our demo and test plan for the full system at the last minute. It would have been better to plan for this and have a higher current photodiode ready to calibrate and demonstrate the system without the need for the sensor. Obviously, a future work is testing the actual sensor and demonstrating it in a similar means.

One large mistake we made was the lack of ability to bias a photodiode with our circuitry. Read-out of the sensor requires photodiode biasing, but the photocurrent will then run through the biasing. This would have made it difficult to use our circuitry in a real sensor demonstration without opening up the equipment used to bias the photodiode. Making this bias in the circuitry would have proved very useful.

The LabVIEW software could have been much more focused. The calibration software would have made sense to not run through our circuitry at all. Rather, using a high-precision DC current device, already in our lab and interfaced with LabVIEW, would have made the system easier to write and more accurate. This also would have alleviated need to think about using RS232 as it would not have gone through the myRIO at all. This software would also see use in other projects in Professor Beling's group.

A natural extension of this project is in the creation of detector arrays. An array of these detectors can be fed by a single wide-band light input with a single waveguide running through them. By tuning each resonator to a noticeably different wavelength, the entire array can be read through a single output photodiode and parsed using frequency multiplexing to obtain an entire image. This technique is already used in microwave kinetic inductance detectors (MKIDs, [37]) and was patented in 2018 for use in terahertz thermal bolometers [16].

Large imaging arrays of our sensors would allow for the integration of ultrasonic sensing with integrated photonics and circuits. In particular, it would create a better replacement for the piezoelectric receivers used in photoacoustic microscopy. By using a sensor with a footprint more than 60 times smaller and integratable into much larger arrays, higher resolution images could be created with photoacoustic microscopy without the need for incapacitation of the subject. One concept for this would include low-power brain imaging helmets for mice which use internet of things technology to send image data over a free range for the mice.

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Appendix

1A: Cost Analysis for Project

Part	Single Price	Bulk Price (10,000	Number Needed	Total Cost, Single	Total Cost, Bulk
10uF Cap	0.79	26720	1	0.79	2.672
.068uF Cap	0.36	939.4	2	0.72	0.18788
100kO Res	0.54	1084.2	1	0.54	0.10842
47kO Resistor	1.74	7280	1	1.74	0.728
9.1kO Resistor	0.32	437.2	1	0.32	0.04372
3.8kO Res	0.1	72.9	1	0.1	0.00729
30kO Res	0.1	72.9	1	0.1	0.00729
8.2kO	0.1	72.9	1	0.1	0.00729
100pF Cap	0.33	874	1	0.33	0.0874
10,000pF Cap	0.65	3004.3	3	1.95	0.90129
680pF	0.3	802	1	0.3	0.0802
390pF Cap	0.3	724.5	1	0.3	0.07245
opamp	5.05	25336.5	2	10.1	5.0673
trans-z	5.46	2734.7	2	10.92	0.54694
SMA Connectors	2.61	15130	2	5.22	3.026
red test	0.84	4883	3	2.52	1.4649
black test	0.84	4883	3	2.52	1.4649
white test	0.84	4883	3	2.52	1.4649
Serial Cable	149	0	1	149	0
Serial Connector	0.77	0	1	0.77	0
RS232ic	3.9	0	1	3.9	0
triple connector	0.13	0	2	0.26	0
breakout	15.95	0	1	15.95	0
0.33uF Cap	0.33	33000	1	0.33	3.3
1uF Cap	0.41	41000	1	0.41	4.1
2 Layer Board	10	50000	1	10	5
Semiconductor L	0	10000	1	0	1

Total Cost:

- Single production: $211.71
- Bulk Production (10,000 units, unit cost): $25.34

Note that bulk analysis ignored the costs associated with RS232 connectivity of a research laser in favor of a pre-biased land thermally controlled low-cost semiconductor laser. Additionally, fabrication of the sensor was not included in the costs due to the difficulty in direct attribution; UVML clean room costs are approximately $1,000 per student per month.