Two Dimensional Thermoelectric Transport and Transient Energy Conversion

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Doctoral Dissertation

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Declaration

This certifies that the thesis titled "Two Dimensional Thermoelectric Transport and Transient Energy Conversion" was carried out by Farjana Ferdous Tonni in the Department of Electrical and Computer Engineering at the University of Virginia.

This dissertation, in whole or in part, has not been submitted elsewhere for the award of a degree.

Approval Statement

This certifies that the thesis submitted by Farjana Ferdous Tonni, titled *"Two Dimensional Thermoelectric Transport and Transient Energy Conversion,"* has been approved by the committee in partial fulfillment of the requirements for the Doctor of Philosophy in Electrical Engineering.

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"To my parents, whose endless love and sacrifices have made my academic journey possible"

"To my beloved husband and dear friend- Your unwavering support, love, and friendship have been my strength throughout this journey"

"To my beloved daughter and my soon-to-be-born son- You are my greatest inspiration. Every day, I strive to grow into someone you can look up to—someone who makes you proud"

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Abstract

Thermal management is crucial to modern electronic technology as ICs are becoming denser each decade. With higher density comes the challenge of managing the increased energy dissipation densities and large local temperatures. The stable and reliable operation of modern advanced electronics requires good thermal management. The primary objective of this dissertation is to study thermal and thermoelectric transport in two-dimensional thin-film systems of materials for good thermal management applications. A high-efficiency thermoelectric device can draw heat to convert it into electrical energy efficiently, and hence it can be used to cool on-chip devices. Such thermoelectric devices can also be used to convert waste heat into electrical power. Traditional bulk thermoelectric modules cannot be effectively integrated into on-chip applications. Two-dimensional geometries, including thin films and few-layer 2D materials, offer better compatibility, scalability, and potential for integration. This research aims to investigate in-plane thermal transport in two-dimensional systems, including silicon-based nanostructured thin films and layered materials ($NbSe_2$, 2H-$MoTe_2$, and $PtSe_2$), addressing limitations in traditional measurement techniques. By studying their temperature dependence, this work aims to expand the scarce literature on in-plane thermal conductivity, particularly in transition-metal dichalcogenides (TMDs) and group III monochalcogenides. Measuring nanometer-thick samples provides fundamental insights into phonon transport, advancing their potential for thermal management applications.

Beyond thermal properties, I explore thermoelectric performance in BiSb thin films on nanostructured substrates and two-dimensional γ-InSe, examining key factors influencing efficiency in device applications.

Finally, this research concludes with a novel solid-state energy conversion device operating on a thermodynamic cycle inspired by the Otto cycle. Unlike conventional thermoelectric or thermionic generators, it harnesses electron gas dynamics for energy conversion, operating beyond Carnot's efficiency and unlocking new possibilities for thermal-to-electrical energy conversion.

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Chapter 1

Introduction

Modern electronics with advanced technologies are made possible with continuous miniaturization of electronic and optoelectronic devices. The most astounding technological observation was made by Gordon Moore in 1965 in an article when he proposed that the number of transistors per integrated circuit would double annually. His second paragraph about the effects of such growth is as follows: "Integrated circuits will lead to such wonders as home computers-or at least terminals connected to a central computer-automatic controls for automobiles, and personal portable communications equipment. The electronic wristwatch needs only a display to be feasible today" [1]. This has been proved to be true by the art of miniaturizing electronic devices. It has opened a new era of technology, from portable computers, smartphones, and new medical devices to the Internet of Things and 5G wireless devices, as well as AI, all enabled by smaller yet more powerful computing systems. However, this miniaturization of electronic devices comes with challenges of managing the increased energy dissipation densities and large local temperatures [2–4]. This necessitates effective local and on-chip thermal management, which involves not only dissipating excess heat from the chip but also, where possible, harnessing this waste heat to generate electricity for powering low-energy devices. The aim of this thesis is to explore materials for efficient heat management and to develop novel energy conversion strategies for harnessing waste heat.

With this in mind, this dissertation first explores thermoelectric transport in two-dimensional systems, focusing on material structures such as thin films and 2D materials. The objective is to measure the in-plane thermal conductivity of 2D materials and

their temperature dependence, overcoming the limitations of traditional measurement techniques in 2D. This work aims to contribute to the scarce literature on the in-plane thermal conductivity of 2D materials, which is the main topic of Chapter 2. The material family of interest in this chapter includes two-dimensional transition metal dichalcogenides (TMDs). These measurements of the low dimensional materials of micrometer length scale help bridge existing research gaps but also provide fundamental insight into the phonon transport mechanisms, enabling their consideration for appropriate thermoelectric and thermal management applications.

In Chapter 3, we broaden our investigation beyond thermal properties to include thermoelectrics as well. Our focus in this chapter consists of investigating the thermoelectric properties of BiSb thin films with nanostructured substrates as well as two-dimensional $\gamma - InSe$, a member of group III monochalcogenides, and exploring the factors that affect their thermoelectric performance in a device.

Finally, in Chapter 4, within the broader theme of thermal-to-electrical energy conversion, a new device has been proposed and developed that operates on a thermodynamic cycle in the solid-state regime, fundamentally distinct from conventional solid-state thermoelectric or thermionic generators. The thermodynamic cycle is designed in analogy to the Otto cycle and includes compression, heating, and release of an electronic gas. During the electron gas expansion, part of the energy is delivered to the load, while the remainder is rejected to the lattice. Given the non-equilibrium and transient nature of the device, it is not constrained by the Carnot efficiency.

What follows now is a brief discussion on the fundamental principles of these topics, and the motivations behind these projects, providing the necessary background before delving into the details of the subsequent chapters.

1.1 Thermal Transport in Thin Films and 2D Layered Materials

The application of Fourier's law in one dimension in the framework of steady-state temperature gradients facilitates the easiest understanding of the notion of thermal energy transport. The steady-state temperature gradient, $\nabla T(r,t)$, along a material's length,

determines the rate of thermal transport or the heat flux, $Q(r,t)[W/m^2]$, through that material. The ratio of these numbers,$\frac{Q}{\Delta T}$, is equal to the negative of the thermal conductivity, $\kappa[W/mK]$, of the material. This relationship is mathematically expressed by Fourier's law of heat conduction:

$$Q(r,t) = -\kappa \nabla T(r,t) \tag{1.1}$$

In solid-state systems, heat conduction arises from a complex interplay of multiple energy carriers, including electrons and holes (electronic carriers), phonons (lattice vibrations), magnons (spin waves), and plasmons (plasma oscillations). These carriers continuously exchange energy through both intra-carrier scattering within their own subpopulations and inter-carrier interactions, leading to a dynamic and intricate thermal transport process. While electronic heat conduction is often attributed to electrons, holes, and other excitations, plasmonic oscillations can also play a crucial role in certain materials. Ultimately, the total thermal conductivity of a material emerges as the collective contribution of all these mechanisms, each governed by distinct scattering processes and energy exchange dynamics. Electronic thermal conductivity can be effectively described using the nearly free electron model in a periodic potential, leading to the derivation of the Wiedemann-Franz law:

$$L_0 = \frac{\kappa_e}{\sigma T} \tag{1.2}$$

where σ represents the electrical conductivity, and the Lorentz number L_0 is expressed in terms of fundamental constants—the Boltzmann constant and the electronic charge. This law holds most reliably when the Fermi level is deep inside the band (metals) and at high temperatures, where inelastic scattering of charge carriers is minimal. In pure metals such as gold and silver, thermal transport is almost entirely governed by free electrons, and the phononic contributions are considerably smaller. For semiconductors, a similar relationship can be derived based on the equilibrium distribution of both electrons and holes with a modified Lorenz number, extending the Wiedemann-Franz framework to a broader class of materials.

A comprehensive theoretical treatment of lattice thermal conductivity must account for multiple scattering mechanisms, including impurity scattering, isotope effects, and other perturbations. While in materials with moderate impurity concentrations, the dominant phonon approximation often provides a sufficiently accurate description of

phonon-mediated thermal transport, a complete understanding requires a deeper exploration of phonon interactions. Traditional models of electronic and phononic thermal transport assume negligible electron-phonon correlations, yet this assumption overlooks critical phenomena in many materials. In a crystalline lattice, phonons scatter through a variety of mechanisms—such as phonon-phonon interactions, impurity scattering, electron-phonon coupling, and boundary effects—each playing a vital role in shaping the material's thermal transport properties.

As we go from bulk to thin films phonon transport becomes constrained by the material's boundaries, causing the thermal conductivity of the thin films to be lower than their bulk counterparts—sometimes dramatically so. For example, at room temperature, the thermal conductivity of a 20 nm silicon film can be up to five times smaller than its bulk single-crystal counterpart [5]. Thermal conductivity can generally be attributed to two main factors. First, thin film synthesis techniques often introduce more impurities, disorder, and grain boundaries compared to bulk single crystals, all of which reduce thermal conductivity. Second, thin films experience reduced thermal conductivity due to boundary scattering, phonon leakage, and related interactions [6]. Both of these mechanisms typically affect in-plane and cross-plane thermal transport differently, resulting in anisotropic thermal conductivity in thin films, even for materials whose bulk forms exhibit isotropic behavior. In this context, 2D layered materials, with their unique thermal properties, emerge as promising candidates for nanoscale power generation and waste heat recovery. The distinct crystal structure of 2D layered materials results in high thermal anisotropy, with 50–300 times slower cross-plane heat conduction than in-plane heat conduction[7]. In a 2D layered material, each layer is stacked by van der Waals interactions, and each layer's atoms are covalently bound. This causes a slower rate of heat transfer across the layers Compared to in-plane heat transport. Despite the fact that the majority of research on the thermal conductivity of 2D materials is theoretical it is well understood how heat is transported in these systems both in the monolayer and bulk. In the first part of this proposal, I aim to experimentally investigate thermal transport in nanostructured thin films as well as 2D layered materials. Although several experimental techniques are available, in-plane thermal conductivity measurements of thin-film samples are still difficult to perform in practice because they frequently call

for film suspension [8–10] and are labor-intensive in terms of the microfabrication procedures required. Among the available measurement techniques for thin films and 2D materials, thermal conductivity measurement methods can be divided into two categories based on the sample's thermal equilibrium: transient techniques and steady-state techniques. When the surroundings have not reached thermal equilibrium, thermal conductivity is measured in the time (or frequency) domain using transient methods. The 3ω method [11] and time-domain thermoreflectance (TDTR) spectroscopy [12] are the two most often utilized transient techniques. In the steady-state procedures, thermal equilibrium is established for the measurements. The micro-bridge method [13] and the Raman thermometry-based thermal conductivity measurement method [14] are the two most often utilized steady-state techniques but both techniques require film suspension. As the thin films and the 2D layered materials are extremely delicate, in order to prevent sample damage during the substrate removal procedure, it is preferable to measure the samples directly on the substrate. There are few choices when it comes to thin films supported on a substrate, which is very common in devices. In the event that the samples are isotropic, a cross-plane measurement may be performed utilizing either the TDTR method or the 3ω method. In the case of anisotropic samples, two established in-plane measurement techniques are the variable-linewidth 3ω method [15, 16] and the heat spreader method [6, 17]. The in-plane thermal conductivity value can only be determined using the variable-linewidth 3ω method if the cross-plane value is known. Also, this method requires narrow heater lines to be deposited and has constraints in the range of measurable thermal conductivity values. The heat spreader method is helpful in situations where the variable-linewidth 3ω method cannot be used. This process involves Joule heating a thin film after a heater is deposited at one end of it. When heat flow reaches the thin film of interest supported by a substrate with low thermal conductivity, the heat is spread laterally through it. Therefore, by determining the temperature decay profile along the film, its in-plane thermal conductivity can be extracted. It is necessary to pattern a number of metallic lines along the sample. To measure the local temperature, these metallic lines are employed as resistance thermometers. However, the number of deposited thermometers and the lithography limit reduce the number of data points that can be extracted for thermal conductivity. Moreover, metallic thermometers are used in

both procedures, conductive samples must have an insulating layer applied to them in order to stop current leaks. This can be challenging to do and lowers accuracy because the temperature is no longer directly monitored on the sample. A new hybrid method was introduced in our group recently that combines the thermoreflectance (TR) imaging and heat spreader method which solves the problem of lithography for multiple heater lines as well as the indirect temperature measurement using resistance thermometers [18]. With the TR imaging system, a temperature map of the sample surface can be acquired based on how surface reflectivity changes with respect to temperature variations. The temperature is measured directly on the sample, in a noncontact mode using optical means, and continuously along the film with a spatial resolution on the order of 100 nm.

1.1.1 Heat Diffusion Imaging for in-plane Thermal Transport Measurement

The TR imaging system captures the changes in the reflected light intensity (ΔR/R) due to the changes in the refractive index of the sample surface with the temperature variations (ΔT) following the equation $\frac{\Delta R}{R}$ = $C_{TR}\Delta$T, where C_{TR} is the thermoreflectance coefficient, and it depends on the material and the wavelength of the light source. A relative temperature variation profile of the sample surface is plotted by mapping the spatial changes in the reflectivity. We use an LED light source of 530 nm wavelength (green light) for illumination and this is synchronized with the current pulse generated by the function generator that is applied to the heater line fabricated on the sample. As the heater gets heated due to the applied current pulse, the temperature change modifies the surface reflectivity. The modified reflected light intensity is then captured by a charge-coupled device (CCD) camera and sent back to the control unit for analysis. The captured thermal image is taken many times when the LED is activated and deactivated at a certain delay time synchronized with the thermal excitation cycles and finally averaged to provide a complete temperature map of the area of interest to optimize the signal-to-noise ratio. The in-plane thermal conductivity is then extracted from the temperature decay along the film taking into account the heat leak to the substrate:

$$T(x) - T(\infty) \propto e^{-\beta x} \tag{1.3}$$

$$\beta(x) = \sqrt{h_i/\kappa_x d} \tag{1.4}$$

where κ_x is the in-plane thermal conductivity of the thin film of interest, and d is its thickness. The variable h_i=κ_{iz}/d_i involves κ_{iz} is the cross-plane thermal conductivity of the substrate insulator where we use the measured temperature-dependent values of fused SiO_2 [19], and d_i is the SiO_2 insulator layer thickness. We first fit the temperature decay to extract β value as shown in Figure 1.1b, where plain Si thin film was initially used as a benchmark, comparing its values with those measured by in-plane TDTR and reported in the literature. Using the thickness of the film and value of h_i, we can extract the in-plane thermal conductivity κ_x at room temperature. The measurement is repeated from low temperature (25K) up to room temperature inside an ARS cryostat coupled with the thermoreflectance setup. The concept of heat spreader method coupled with thermo-reflectance imaging has been successfully applied to systems as thin as a few layers, demonstrating its effectiveness in such thin materials [18, 20]. This allows us to use heat diffusion imaging techniques for samples that are tens of nanometers thick.

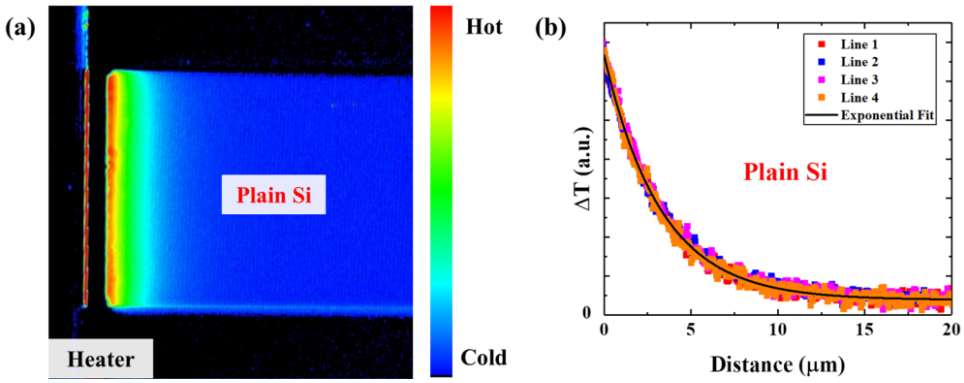

Figure 1.1: Example temperature map of (a) the plain Si sample under 100× magnification at room temperature, (b) A few representative temperature decay curves and their corresponding exponential fitting curves [Figure ref. Zhu et al. 2020].

1.2 Thermoelectric Properties and Efficiency

The principle of thermoelectrics is based on the Seebeck effect. In the Seebeck effect, the presence of a temperature gradient across a material induces a voltage in the direction of the gradient. The Seebck coefficient is then defined as the ratio of this voltage devel-

oped to the temperature gradient. Thermoelectric devices are built based on this effect. The thermoelectric performance of a material is evaluated by its dimensionless figure of merit, $zT = \frac{\sigma S^2}{\kappa}$, where σ is the electrical conductivity, S is the Seebeck coefficient and κ is the thermal conductivity. The higher the zT of a material, the better would be the thermal-to-electrical energy conversion of a device made from it. Using the following variables for energy carriers: Fermi-Dirac probability function for electrons= $f = \frac{1}{e^{\frac{E-\mu}{kT}}+1}$, Bose-Einstein probability function for phonons = $f_b = \frac{1}{e^{\frac{E}{kT}}-1}$, average squared-velocity of the particles at a given energy = $\langle v(E)^2 \rangle$, Relaxation time = $\tau(E)$, differential conductivity = $G(E) = \langle v(E)^2 \rangle \tau(E) DOS(E)$, these three intrinsic parameters can be expressed as:

Electrical conductivity,

$$\sigma = q^2 \int_{-\infty}^{\infty} G(E) \frac{-\partial f}{\partial E} dE \tag{1.5}$$

Seebeck coefficient,

$$S = -\frac{\Delta V}{\Delta T} = \frac{\nu}{\sigma} \tag{1.6}$$

where,

$$\nu = q \int_{-\infty}^{\infty} G(E) \left(\frac{E-\mu}{T} \right) \frac{-\partial f}{\partial E} dE \tag{1.7}$$

Total thermal conductivity,

$$\kappa = \kappa_e + \kappa_l \tag{1.8}$$

where,

$$\kappa_e = \int_{-\infty}^{\infty} G(E) \frac{(E-\mu)^2}{T} \frac{-\partial f}{\partial E} dE - S^2 \sigma T \tag{1.9}$$

$$\kappa_l = \int_{0}^{\infty} G_b(E) \left(\frac{E^2}{T} \right) \frac{-\partial f_b}{\partial E} dE \tag{1.10}$$

Taking a closer look at these three intrinsic parameters of a material reveals their intricate relationship with the material's dimensionality, the density of states (DOS), and scattering parameters. Improving the zT of a material can be achieved by increasing the power factor ($PF = \sigma S^2$) through band structure engineering or by decreasing the thermal conductivity (κ) via suppressing phonon transport without significantly affecting electron transport [21]. While band structure engineering aims to tune the electronic properties, like the Seebeck coefficient (S) and electrical conductivity (σ), reducing thermal conductivity (κ) involves structural engineering focusing on controlling the mate-

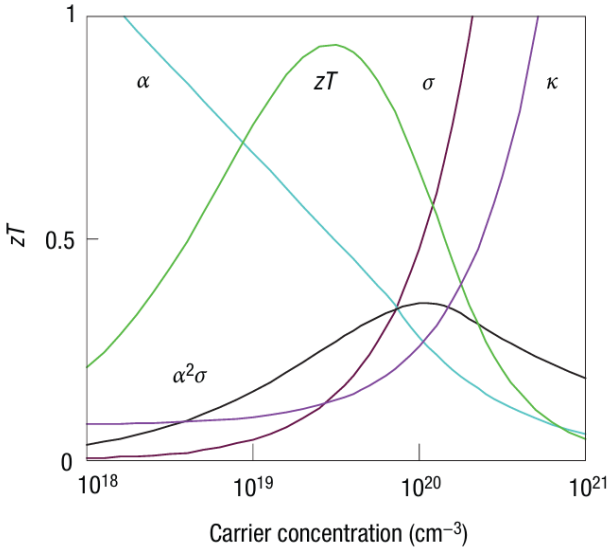

Figure 1.2: Role of Seebeck coefficient (α), electrical conductivity (σ), thermal conductivity (κ) in optimizing figure of merit, zT. [Figure ref. Snyder et al. 2008]

rial's microstructure, such as creating nanostructures to enhance phonon scattering. Ideally, both strategies should be applied simultaneously to achieve the maximum possible efficiency. However, designing high-performance thermoelectric materials is challenging because these transport properties are interconnected as can be seen in Figure 1.1 (where thermal conductivity, κ; plotted on the y axis from 0 to a top value of 10 $Wm^{-1}K^{-1}$ and Seebeck coefficient, α; 0 to 500 μVK^{-1} with electrical conductivity σ; 0 to 5,000 $\Omega^{-1}cm^{-1}$). Here, the zT is modeled from Bi_2Te_3 empirical data [22]. Typically, a good thermoelectric material is a heavily doped semiconductor with a carrier concentration between 10^{-19} and 10^{-21} carriers per cm^3. Changing one parameter often impacts others in a way that can hinder overall performance. For instance, increasing electrical conductivity may reduce the Seebeck coefficient, or reducing thermal conductivity could lower the electrical performance. The key challenge is to decouple these competing effects, finding a balance that enhances all the properties required for optimal thermoelectric performance.

1.2.1 Thin Films and Nanostructuring

Incorporating nanostructures into a material system enables the decoupling of thermal and electrical transport, allowing independent control over S, σ, and k for enhancing zT. This approach relies on increasing phonon scattering through additional boundaries or

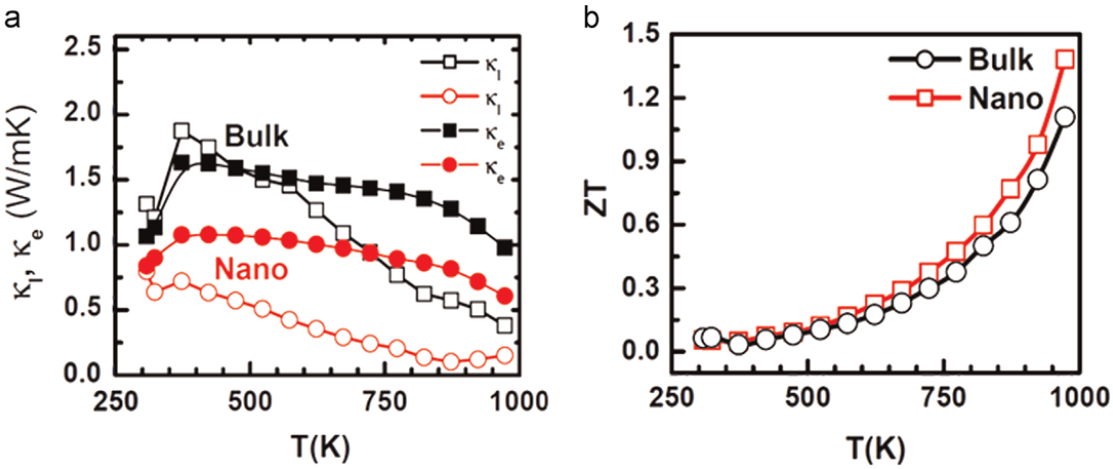

Figure 1.3: Temperature-dependent thermoelectric behavior comparison between bulk and nanostructured $Cu_{1.98}Se$ samples: (a) variations in lattice and electronic thermal conductivity, and (b) ZT performance [Figure ref. Tyagi et al. 2015].

interfaces, effectively reducing lattice thermal conductivity. Since charge carriers typically have much shorter mean free paths (MFPs) than phonons, their transport properties remain largely unaffected. Thin films make appealing platforms for nanostructuring beacause of their already reduced length scales and consequently lower thermal conductivity. Figure 1.2 illustrates such a scenario applied in the case of $Cu_{1.98}Se$ to improve its performance [23]. Effective nanostructuring methods include incorporating nano-arrays and adding either random or periodic porosity. Random porosity is typically introduced through partial densification of the material, while periodic porosity requires precise lithographic techniques. Spark Plasma Sintering (SPS) is highly effective for achieving nanostructuring. Unlike conventional hot-pressing, which relies on external heating, SPS generates internal heat through an electric field, enabling rapid heating and cooling rates of up to 1000 K/min. Structural designs incorporating crystal imperfections, such as point defects, dislocations, interfaces and inclusions are also commonly used to enhance thermoelectric performance by lowering thermal conductivity [24, 25]. Moreover, by confining length scales, nanostructuring can also modify the band structure, leading to an enhanced Seebeck coefficient and improved power factor [26–28].

1.2.2 Two Dimensional Materials

Reducing the dimensionality can help increase the number of modes within the Fermi window near the band edges, which is beneficial in improving the electronic properties [29]. As we scale down the dimensions, a sharp density of states (DOS) profile at the band edge is created due to the quantum confinement effect [28]. Superior electron mobility has been observed in many 2D crystals and 2D transition metal dichalcogenides (TMDs). For example, mobilities exceeding 200,000 $cm^2.V^{-1}.K^{-1}$ were achieved at electron densities of approximately 2x10^{11} cm^{-2} by suspending a single layer of graphene [30]. In single-layer graphene suspended over a large trench on a Si/SiO_2 substrate, a room temperature thermal conductivity of $5.30 \pm 0.48 \times 10^3$ W/mK was reported [31]. Additionally due to the classical size effect reduced thermal conductivity is commonly observed in low dimensional systems relative to the bulk systems [32]. Lower thermal conductivity is advantageous for cooling using traditional thermoelectric coolers, while high thermal conductivity makes graphene and other materials with similar behavior a suitable candidate for active cooling applications. Hence, 2D materials show great promise for a diverse range of cooling techniques. Besides this, 2D materials have shown great promise for flexible electronics as illustrated in Figure 1.3 [33]. Over the past few years, there has been an increase in interest in understanding the thermal properties of 2D materials. Although many research studies focus on the micro/nano components of two-dimensional materials on their electrical, mechanical, and optical properties, there are very few reports on thermal transport studies in 2D materials. Hence understanding the thermal transport phenomena by measuring the in-plane thermal conductivity of materials is of significant importance in thermoelectricity.

1.3 Monte Carlo Simulation

The Boltzmann Transport Equation (BTE) offers a strong foundation for modeling the transport properties of electrons in solids, especially when the system is not in equilibrium. It is widely used in fields such as semiconductor physics, materials science, and nanotechnology to illustrate how electrons move and interact with one another in a solid, taking into account external influences like electric fields and scattering processes

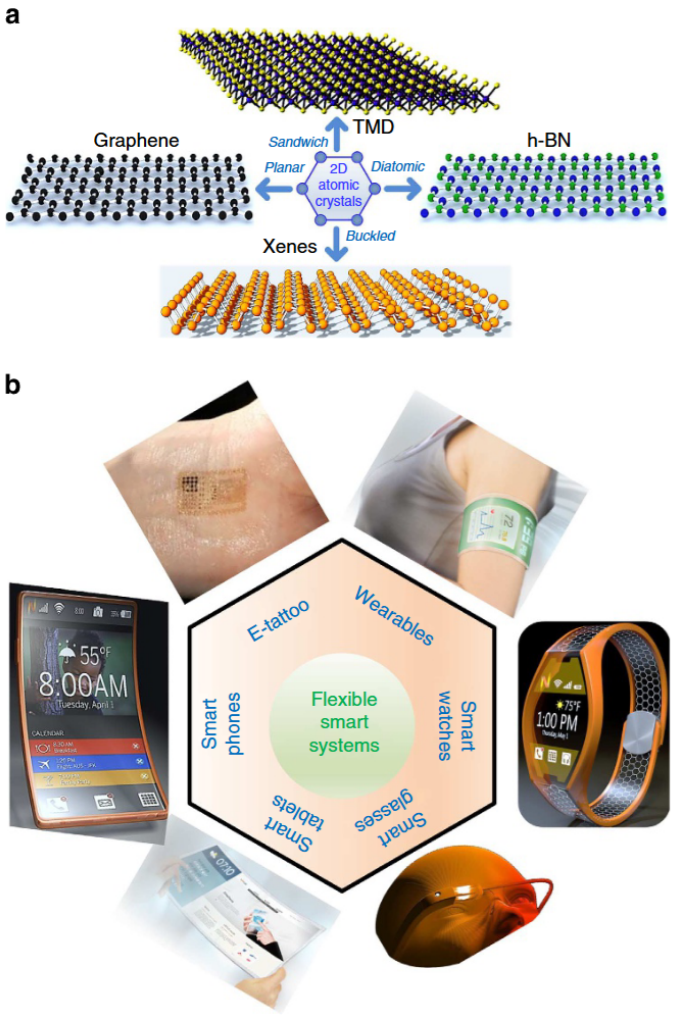

Figure 1.4: An illustration of 2D monolayer materials and examples of flexible smart systems showcasing their potential applications in advanced technologies [Figure ref. Akinwande et al. 2014].

(for example, electron-phonon or electron-electron interactions). Solving the BTE directly is complex due to the non-equilibrium nature of transport processes and the need to account for various scattering events. However, there are a number of solutions and approximations. The way the BTE is simplified by each of these approaches varies based on the type of transport process being examined, the level of approximation needed, and the material system. In this section, a brief overview of the Boltzmann Transport Equation (BTE) and some of the possible solution methods will be presented, followed by an exploration of the Monte Carlo method for solving the BTE to stimulate carrier transport in semiconductor materials and devices.

The Boltzmann Transport Equation (BTE) describes the evolution of the electron distribution function under an external perturbation, such as an electric field, in relation to the equilibrium distribution. This distribution provides information about how electrons are distributed in momentum space (k-space), and from this, various transport properties can be calculated [34].

Let $f(\mathbf{r}, \mathbf{k}, t)$ be the local occupation of electrons in a region around position $\mathbf{r}$ in a given state $\mathbf{k}$. The evolution of this distribution function over time is controlled by the BTE. A shift in the distribution function can be caused by three primary factors: (a) electron motion (diffusion) due to thermal energy, leading to changes in their spatial distribution $\mathbf{r}$, (b) externally applied field (drift) which accelerates the electrons in a specific direction, thus modifying their momentum $\mathbf{k}$, and (c) scattering processes due to interactions with phonons, impurities, or other electrons. These scattering events can randomize the electron's momentum, affecting the distribution function in $\mathbf{k}$ state. Under steady-state conditions, the drift, diffusion, and scattering terms combine in the Boltzmann Transport Equation to yield a balance where the change in the distribution function due to electron motion, the externally applied field, and scattering processes is zero. This can be expressed as:

$$\left.\frac{\partial f_k}{\partial t}\right|_{\text{diffusion}} + \left.\frac{\partial f_k}{\partial t}\right|_{drift} + \left.\frac{\partial f_k}{\partial t}\right|_{\text{coll}} = 0 \tag{1.11}$$

The diffusion term is expressed as:

$$\left.\frac{\partial f_k}{\partial t}\right|_{\text{diffusion}} = -\frac{\partial f_k}{\partial r} \cdot \frac{\partial \vec{r}}{\partial t} = -\frac{\partial f_k}{\partial t} \vec{v}_k \tag{1.12}$$

where $\vec{v}_k$ is the velocity of a carrier in the state k. The drift term can be expressed as follows if we consider an electric field $\mathbf{F}$ as the only external applied field:

$$\left.\frac{\partial f_k}{\partial t}\right|_{drift} = -\frac{\partial f_k}{\partial k} \cdot \frac{\partial \vec{k}}{\partial t} = -\frac{e}{\hbar} \vec{F} \cdot \frac{\partial f_k}{\partial k} \tag{1.13}$$

If the system is disturbed from equilibrium, typically by an external force or a sudden change in conditions (like an applied electric field or temperature gradient). This causes the distribution function $f(\mathbf{r}, \mathbf{k}, t)$ to vary with time. The general form of the BTE under non-steady-state is:

$$\frac{\partial f}{\partial t} + \vec{v}.\vec{\nabla}_r f + \vec{F}.\vec{\nabla}_p f = \left.\frac{\partial f}{\partial t}\right|_{coll} + S \tag{1.14}$$

Here,

$\frac{\partial f}{\partial t}$: transient term

$\vec{v}.\vec{\nabla}_r f$: diffusion term, and $\vec{F}.\vec{\nabla}_p f$: drift term as shown above,

S : source term, and finally

$\left.\frac{\partial f}{\partial t}\right|_{\text{coll}}$: scattering term is the most challenging to analyze. It can be expressed in terms of the scattering rate from the state k to the state k', and vice-versa. The probability of transitioning from state k to state k' is the product of the probability of being in state k (f_k), the scattering rate from k to k' ($W_{k\to k'}$), and the probability that state k' is empty ($1 - f_{k'}$).

The rate of change of the distribution function for state k over time is then equal to the rate at which electrons move from all occupied states k' to the unoccupied state k, minus the rate at which electrons leave the occupied state k and transition to all unoccupied states k':

$$\left.\frac{\partial f_k}{\partial t}\right|_{\text{coll}} = \int \left[f_{k'}\left(1 - f_k\right) W_{k',k} - f_k\left(1 - f_{k'}\right) W_{k,k'}\right] \frac{d^3k'}{(2\pi)^3} \tag{1.15}$$

This integral is difficult to solve analytically due to the complex nature of the scattering rate. A commonly used simplification is to approximate the scattering term as the difference between the distribution function and the equilibrium distribution, divided by a time constant, τ_f.

$$\left.\frac{\partial f_k}{\partial t}\right|_{\text{scattering}} = -\frac{f_k - f_k^0}{\tau_f} \tag{1.16}$$

This is called relaxation time approximation. The BTE under the relaxation time approximation (RTA) simplifies the scattering term by assuming that the distribution function relaxes towards equilibrium exponentially with a characteristic time constant τ_f. In this approximation, the BTE is written as:

$$\frac{\partial f}{\partial t} + \vec{v}.\vec{\nabla}_r f + \vec{F}.\vec{\nabla}_p f = -\frac{f_k - f_k^0}{\tau_f} \tag{1.17}$$

The relaxation time τ_f is a measure of how long it takes for the system to return to equilibrium after a disturbance (like an applied field). The RTA simplifies the treatment of scattering processes, making the equation solvable under various conditions. However, the RTA is only valid when the system is close to equilibrium, and it may not accurately capture the dynamics in strongly non-equilibrium situations or in systems with complex

scattering mechanisms. It is important to keep in mind that the theory involves other significant time constants, and one should carefully differentiate between them [35].

In some cases, it may be possible to solve the BTE directly without resorting to approximations like RTA. This involves solving the BTE in its full form, including the scattering term and all transport effects (e.g., diffusion, drift). Numerical methods involving discretizing the momentum space and time, and iterating the solution for each time step to capture the evolution of the distribution function are used. The direct solution is particularly useful for nanostructures, thermoelectric materials, and semiconductor devices, where non-equilibrium effects and complex scattering processes significantly influence transport properties. However, it is computationally intensive and requires efficient handling of the scattering terms and boundary conditions.

A more exact solution of the BTE can be obtained using the Monte Carlo (MC) simulation. Monte Carlo is a statistical approach used to simulate the movement of carriers within a semiconductor device. It involves considering an ensemble of carriers whose motion is influenced by the forces acting on each individual carrier. One of the key strengths of this method is its ability to incorporate local variations in factors such as electric fields, charge density, and temperature. Additionally, Monte Carlo simulations are particularly valuable for studying transport under high-applied fields, providing much of our understanding of high-field transport. The method is also effective in investigating transient transport properties in submicron devices. The standard Ensemble Monte Carlo algorithm to simulate nonequilibrium transport in semiconductor materials and devices is extensively detailed in many textbooks and review articles [34–38].

In these simulations of carrier transport, a random walk is generated using modern computer-based random number algorithms to model the stochastic motion of particles undergoing collisions. This random walk process is part of a broader technique used for solving integral equations and is closely related to random sampling methods for evaluating multi-dimensional integrals [38]. The method involves simulating the free motion of particles (known as free flight), which is interrupted by instantaneous random scattering events. The Monte Carlo algorithm shown in Figure 1.2 operates by generating random free-flight times for each particle, determining the type of scattering event at the end of the free flight, updating the particle's energy and momentum post-scattering, and

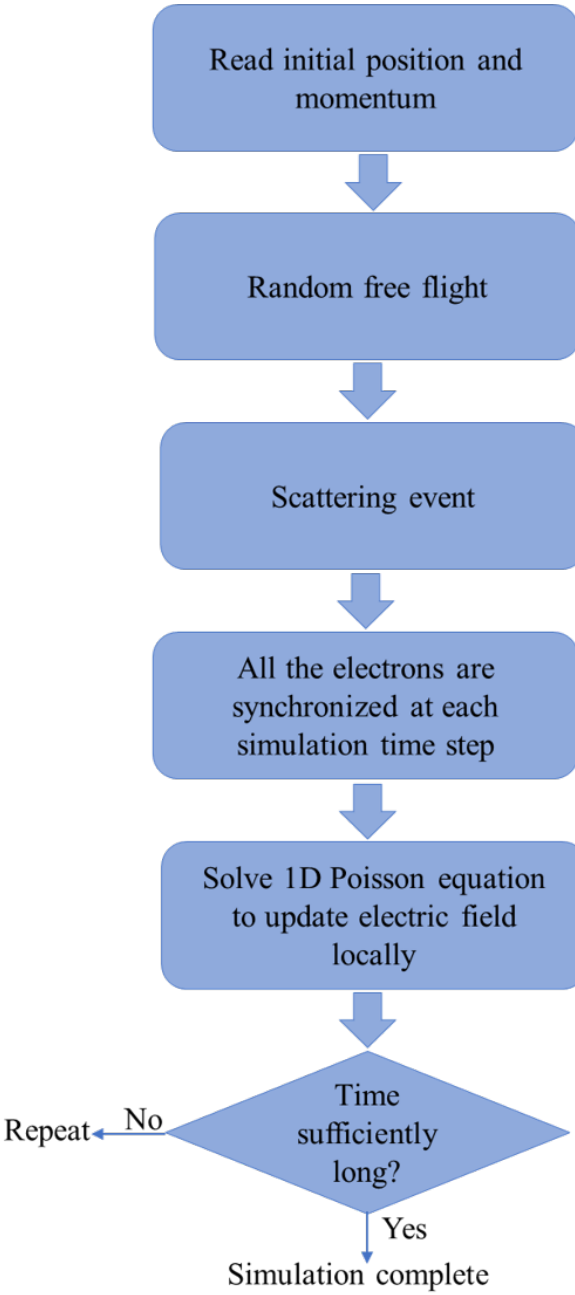

Figure 1.5: Algorithm of Monte Carlo Simulation of carrier transport.

repeating this cycle for subsequent free flights. By sampling particle motion at various points during the simulation, key physical quantities—such as the single-particle distribution function, average drift velocity under an applied electric field, and mean particle energy—can be statistically estimated. Simulating an ensemble of particles representative of the system enables the study of the non-stationary, time-dependent evolution of electron and hole distributions under varying external forces. More details of the sim-

ulation in the context of non-equilibrium electron transport in a GaAs-based device are presented in Chapter 3.

Chapter 2

Thermal transport in thin films and 2D materials

2.1 In-plane Thermal Conductivity in Holey Silicon

Silicon thin films with periodic nano-sized holes were fabricated at the Institute of Industrial Science, The University of Tokyo, Japan. The thermoelectric transport characterization was done by Tianhui Zhu and the thermal conductivity measurement was done by Farjana Ferdous Tonni under the supervision of Dr. Mona Zebarjadi.

2.1.1 Motivation and Objectives

Being the second most abundant element in the earth's crust, silicon is a relatively low-cost material for producing chips, and due to industrial process compatibility, silicon thin films are potential candidates for thermoelectric applications such as on-chip thermal management and power generation for wearable electronics. It has been shown that silicon thin films are flexible and upon transfer to flexible substrates, they can be used for wearable electronic applications [39]. The lattice thermal conductivity of pristine bulk silicon is large at 300 K, it can reach $\sim$150 $Wm^{-1}K^{-1}$ [19] and $\sim$100 W/mK [40] for heavily-doped bulk silicon. Heavily p-doped bulk silicon exhibits a relatively large thermoelectric power factor times temperature (PFT) of $\sim$2.24 $Wm^{-1}K^{-1}$ [40], indicating its potential as a highly effective thermoelectric material. A large power factor and a high thermal conductivity make silicon a great option for active cooling applications

[41, 42]. However, for traditional thermoelectric applications, silicon's high thermal conductivity is not desired as it leads to a low thermoelectric figure of merit zT. This study investigates the improvement of zT with the usage of holey silicon thin films by demonstrating 3D surface doping. An effective way to reduce the thermal conductivity of Si is by introducing various scattering processes to increase the scattering rates through the addition of nanostructures or increasing surface roughness, thus limiting the phonon mean free path (MFP). This can be done by adding grain boundaries, holes, and porosity, and defects and impurities, which introduces more phonon scattering and limits the MFP Here, we study Si thin films with patterned arrays of nano-sized holes which are referred to as holey silicon thin films or sometimes as phononic crystals [43–46]. Studies have indicated that the neck size (the separation between neighboring holes) determines the thermal conductivity [46]. Depending on the neck size and the temperature, thermal conductivity can be reduced to one or almost two orders of magnitude compared to thin film without holes [40, 45]. The optimum design for such nanostructuring requires the neck sizes to be in between the electron and the phonon MFP to selectively limit phonon diffusion with minimal effect on electron mobility, thus improving zT [18, 47, 48]. In this work, we study single-crystalline silicon thin films with patterned nano-holes with sizes comparable to the phonon MFP to suppress thermal conductivity.

2.1.2 Experiment and Results

The holey silicon thin-film devices were fabricated from silicon on insulator (SOI) wafers, which had an active Si layer of 220 nm thick on top of a 3 μm-thick SiO_2 layer. Laser lithography and reactive ion etching (RIE) were used to define device areas of 200×30 μm^2. Subsequently, e-beam lithography and RIE patterned the nano-sized hole arrays onto each device. The holes were kept at a fixed pitch distance of a = 300 nm, and the neck size n of each device varied from 22 nm to 169 nm. Given the limitations of the e-beam lithography tool, the smallest neck size that could be reliably patterned was 22 nm. Lastly, electrodes of 500 nm Al and a 50 nm Au capping layer (Au helps Al prevent oxidation) were evaporated onto the sample to serve as thermometers, heaters, and voltage probes. The Si layer was mildly boron-doped with a resistivity of 10 Ωcm, which corresponds to a hole concentration of $\sim 10^{15}$ cm^{-3}. The regions under the contacts were

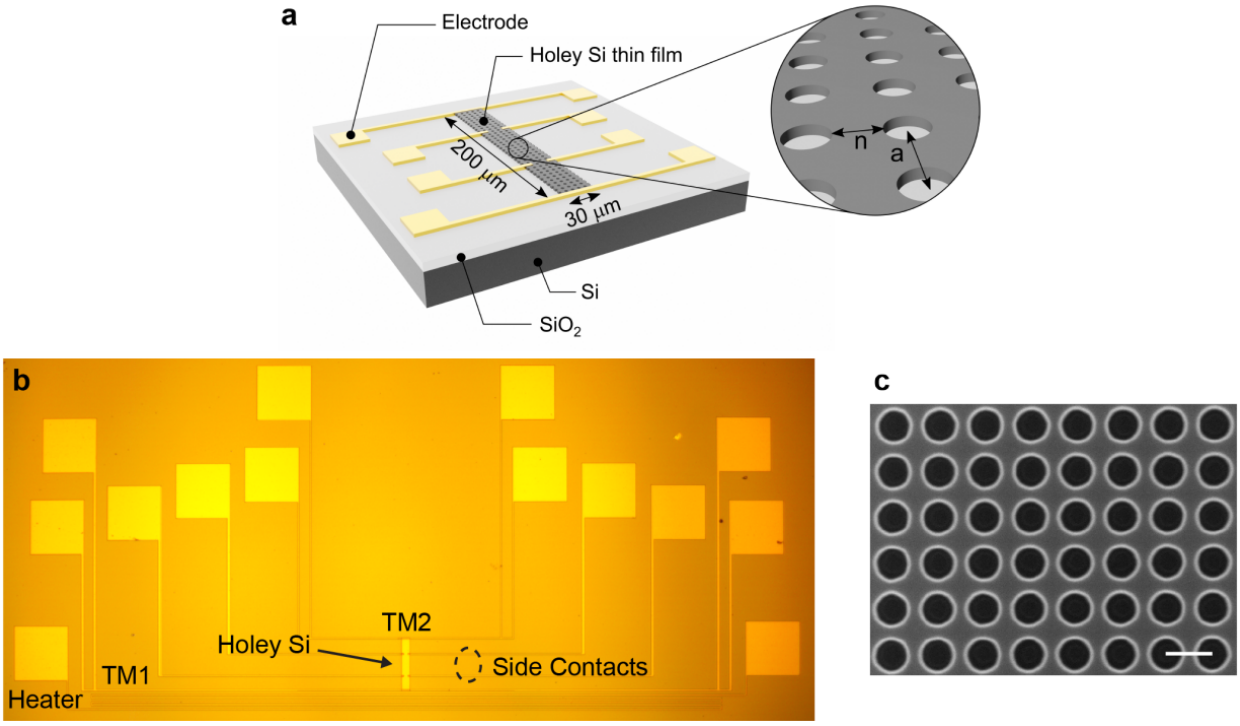

Figure 2.1: (a) Schematic and (b) optical image of the holey silicon device, which includes one heater, two thermometers (TMs), and four side contacts. (c) Scanning electron microscope image of the hole configuration, for sample with 120 nm neck size. The scale bar is 300 nm.

doped to 10^{20} cm^{-3} to ensure Ohmic contacts. The schematics of the hole configuration, as well as the device configuration, are shown in Fig. 2.1.

Heat diffusion imaging was used to measure the in-plane thermal conductivity. A voltage pulse of 5V is passed through the thermometer placed directly on top of the thin film. As the injected heat flow propagates along the thin film of interest, a temperature map is obtained from the surface reflectivity changes using microsanj setup. The thermal conductivity values are extracted based on how the temperature rise decays along the thin film. Details are described in chapter 1. The in-plane thermal conductivity of the holey silicon thin film depends on the neck size. Fig. 2.1 shows that as the neck size decreases from 169 nm to 22 nm, the room temperature thermal conductivity decreases from 26.4 $Wm^{-1}K^{-1}$ to 4.7 $Wm^{-1}K^{-1}$, nearly 5 times reduction. The smaller neck size suppresses the phonon transport more and leads to smaller thermal conductivity values, hence the neck size can be considered as the limiting dimension for phonon transport.

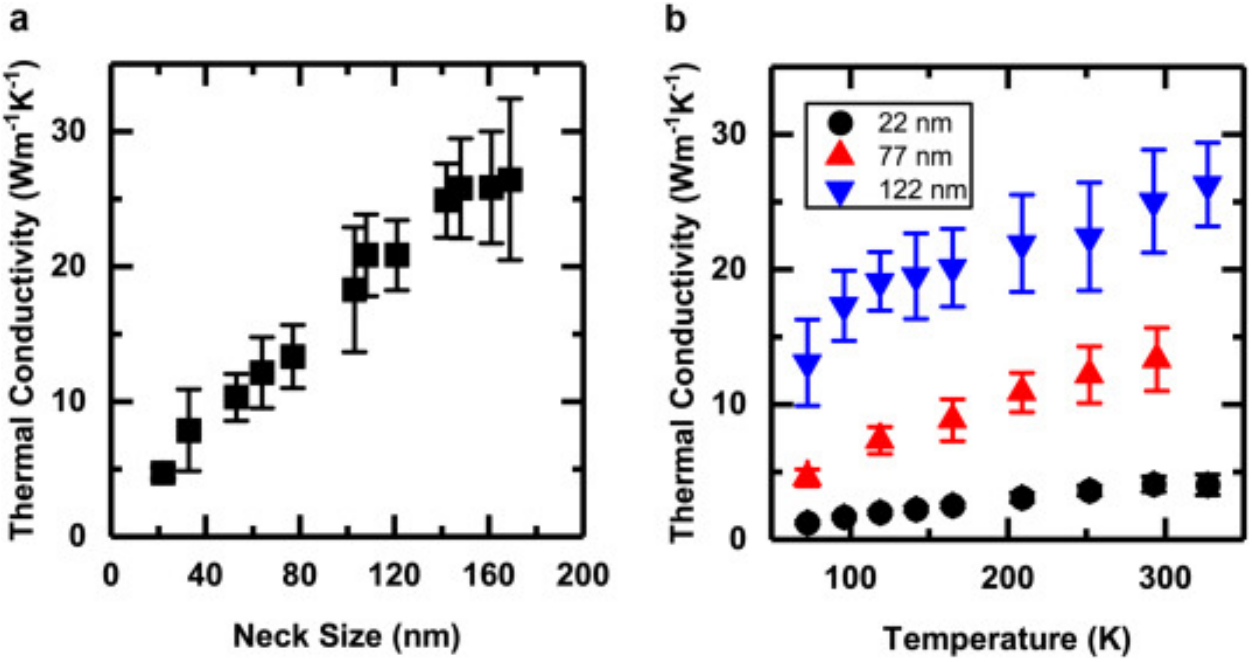

Figure 2.2: (a) Room temperature in-plane thermal conductivity for neck sizes from 22 nm to 169 nm and (b) temperature-dependent thermal conductivity from 50 K to 350 K for neck sizes 22 nm, 77 nm, and 122 nm.

The trend is consistent with those summarized in the literature [46]. In comparison, the room temperature thermal conductivity of a silicon thin film of the same thickness (220 nm) without any holes is about 90 $Wm^{-1}K^{-1}$ [49]. The reduction in thermal conductivity with periodic holes is as high as 19-fold (see Fig. 2.2a) compared to 90 $Wm^{-1}K^{-1}$. The thermal conductivity of three different neck sizes as a function of temperature was also obtained and is plotted in Fig. 2.2b. Their temperature-dependent trends are consistent: as the temperature increases from 75 K to above room temperature, the thermal conductivity increases, and the rate of change becomes smaller at higher temperatures. The overall change in this range is about 2–3 times. Figure 2.2b shows that smaller necks result in a flatter temperature dependency, and the Umklapp peak in κ(T) is absent due to a faster phonon boundary scattering rate [50].

2.2 In-plane Thermal Transport in Few-layer $NbSe_2$

4-layer (4L) $NbSe_2$ was grown by Molecular Beam Epitaxy (MBE) on SiO_2/Si substrate by Peter M. Litwin in Dr. Stephen J. McDonell's group. A single crystal bulk 2H–$NbSe_2$ sample

grown by chemical vapor transport (CVT) by Dr. Sergiy Krylyuk from Dr. Albert Davydov's group at the National Institute of Standards and Technology was used as a reference. Tianhui Zhu fabricated the devices and performed the thermoelectric transport measurements. Md Golam Rosul performed the DFT calculations. Md Sabbir Akhanda contributed to the measurements in VERSALAB. The temperature-dependent thermal conductivity measurements were done by Farjana Ferdous Tonni and Tianhui Zhu under the supervision of Dr. Mona Zebarjadi.

2.2.1 Motivation and Objectives

Transition metal dichalcogenides (TMDs), are an important part of the family of 2D materials. Due to their distinctive structural, mechanical, optical, electrical, and thermal properties, they have sparked a great deal of research interest in them [51–53]. $NbSe_2$ is particularly interesting among TMDs. In its 2H phase, superconductivity and charge density waves (CDWs) coexist at low temperatures (below 7 K for bulk crystals), with thickness determining the CDW transition temperature and the superconducting state [54–56], demonstrating a significant influence on both fundamental physics and potential industrial applications. 2H–$NbSe_2$ has been thoroughly examined in both theoretical and experimental contexts as a model system for highly correlated electronic states [54–58]. Its electrical and magneto-transport properties have been used at low temperatures to identify the superconducting or the CDW phase of the sample [54, 55, 59]. It has been found that upon applying an in-plane magnetic field to a few-layer $NbSe_2$, it exhibits two-fold rotational symmetry in the superconducting state as opposed to three-fold lattice symmetry [60]. Few-layer $NbSe_2$ has the ability to be fabricated into superconducting antenna devices, which exhibit a reversible non-reciprocal sensitivity to electromagnetic waves with a broad range of frequencies, because of its non-centrosymmetric superconductivity [61].

However, less research has been done on the thermal transport property of niobium diselenide, although it is critical to the dependability and efficiency of electronic or spintronic devices. In-depth knowledge of the thermal transport property and the capacity to tune this property also takes center stage as a potential thermoelectric candidate, necessitating additional research from both computational and experimental perspectives. In this study, temperature-dependent thermal conductivity is reported, which, to the

best of our knowledge, is the first temperature-dependent in-plane thermal transport characterization of a few-layer $NbSe_2$. Other thermoelectric properties have also been investigated for this sample.

2.2.2 Experiment and Results

4-layer (4L) $NbSe_2$ was grown on 285 nm thick SiO_2/highly p-doped Si by MBE. The device was fabricated with photolithography: the full coverage thin film was first etched by CF4 plasma (30 W, 120 s) to a well-defined rectangular area, then the electrodes (5 nm Ti/50 nm Au) were deposited using e-beam evaporation (base pressure of 10^{-6} Torr, the deposition rate of 0.4 Å/s for Ti and 2.0 Å/s for Au). The thermal conductivity measurement was done using one of the thermometers deposited on top of the two ends of the samples by applying the HDI method.

The thermal conductivity of 4-layer thick 2H-$NbSe_2$ was measured using the HDI

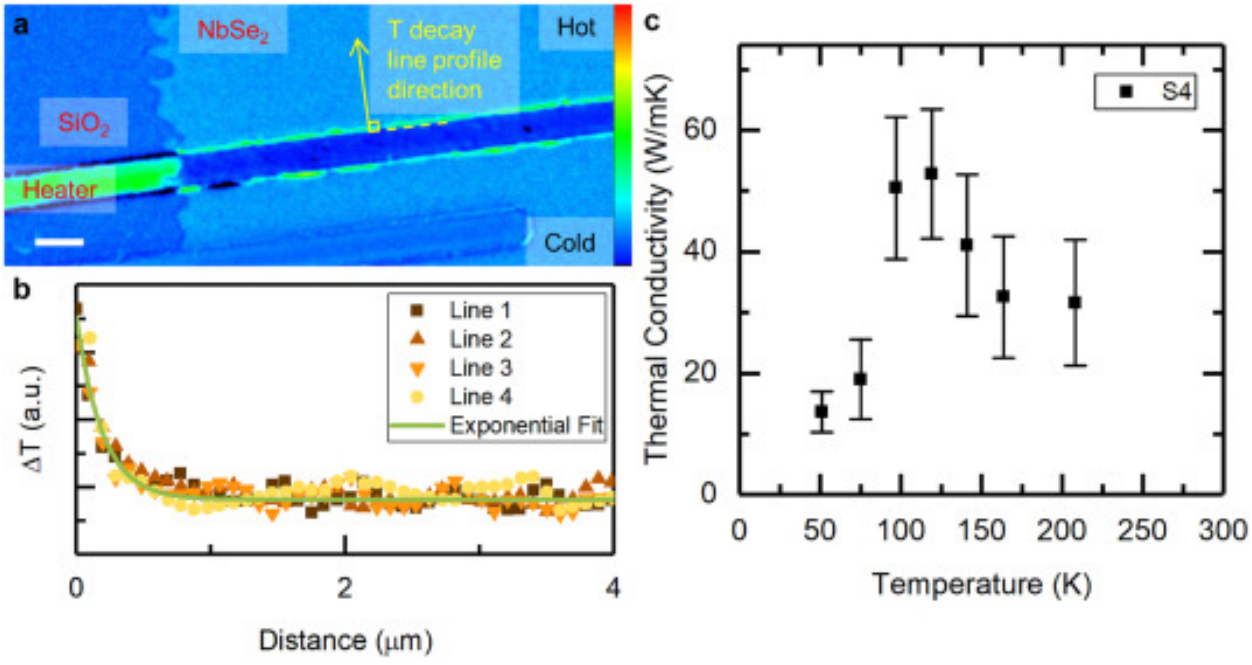

Figure 2.3: (a) Example temperature map at 50 K, (b) example temperature decay curves taken from (a) and their corresponding exponential fitting curve, and (c) temperature-dependent in-plane thermal conductivity from 50 K to 210 K. The scale bar in (a) is 5 μm.

method at low temperatures. As shown in Fig. 2.3, the thermal conductivity rises to

a maximum of about (53 $\pm$ 11) $Wm^{-1}K^{-1}$ as the temperature increases from 50 K to 120 K, then gradually decreases as the temperature gets closer to room temperature at 200 K and reaches a value of (32 $\pm$ 10) $Wm^{-1}K^{-1}$. 2H-$NbSe_2$ is a weak metal. The electrical conductivity of 7 nm thick 2H-$NbSe_2$ sample fabricated following the same procedures was measured to be 1.68 $\times$ 10^5 Sm^{-1} and the Seebeck coefficient 15 μVK^{-1}. It is interesting to note that a positive Seebeck coefficient was obtained for this sample after being exposed to air (kept in a desiccator after Se cap removal) for roughly a week, while another sample, which was not exposed, has a negative Seebeck coefficient at room temperature. The observed positive Seebeck coefficient matches the reported values for $NbSe_2$ nanosheet samples [62, 63], in which the existence of oxide Nb_2O_5 has been confirmed by XPS measurements. The Wiedemann-Franz law estimated the electronic thermal conductivity to be about 1.5 $Wm^{-1}K^{-1}$ at 200 K, comprising less than 5% of the total value. Thermal transport was dominated by phonons. More phonon-phonon scattering is expected with increasing temperature and therefore leads to shorter temperature decay length. Our measurement at higher temperatures was limited by optical resolution. This increasing then decreasing trend in thermal conductivity with respect to increasing temperature resembles that in a previous report on bulk $NbSe_2$ [64], although the maxima occur at different temperatures and the overall thermal conductivity is surprisingly larger than the bulk equivalent. The largest thermal conductivity is reached at 120 K for the 4L $Nb_{1+x}Se_2$. In another few-layer TMD, 4L-MoS_2, the largest thermal conductivity also occurs at around 120 K, where the behavior below 120 K is attributed to phonon-boundary scattering and that above 120 K is attributed to phonon-phonon scattering [65]. To the best of our knowledge, this is the first in-plane thermal conductivity measurement of few-layer $NbSe_2$ samples in this temperature range. However, a room temperature value of (15 ± 4) $Wm^{-1}K^{-1}$ for exfoliated 2H–$NbSe_2$ flakes (about 20 nm–25 nm thick) using the Raman method was reported in a recent master's thesis [66].

2.3 Temperature Dependent In-plane Thermal Transport of 2H-$MoTe_2$

Thin 2H-$MoTe_2$ flakes were exfoliated from $MoTe_2$ crystals which were grown by the Chemical Vapor Transport (CVT) method by Dr. Sergiy Krylyuk from Dr. Albert Davydov's group at the National Institute of Standards and Technology. The electrical, and thermoelectric characterizations were done by Tianhui Zhu, the temperature-dependent thermal conductivity measurements were taken by Farjana Ferdous Tonni, and the DFT calculations were done by Sree Sourav Das under the supervision of Dr. Mona Zebarjadi. The theoretical lattice thermal conductivity was calculated by solving the phonon Boltzmann transport equation by Safoura Nayeb Sadeghi under the supervision of Dr. Keivan Esfarjani.

2.3.1 Background and Motivation

2H-$MoTe_2$ is a semiconducting molybdenum-based TMD material with an indirect gap of 0.83 eV in the bulk form and a direct gap of 1.1 eV in the monolayer limit [67, 68]. The majority of research on 2H-$MoTe_2$ has been directed toward electronic [69–72] and optoelectronic [70, 73] applications While there have been few studies on the material's thermoelectric properties. Seebeck coefficient of n-type single crystal bulk $MoTe_2$ was measured to be around -400 μVK^{-1} from 77 K to 300 K [74]. At room temperature, its electrical conductivity was about 750 Sm^{-1}, and its PFT was 0.036 $Wm^{-1}K^{-1}$ [74]. A 330 nm thick 2H-$MoTe_2$ thin film prepared by magnetron co-sputtering showed a p–n type transition with increasing temperature, giving a maximum PFT of 0.15 $Wm^{-1}K^{-1}$ at 460 K for p-type conduction and 0.55 $Wm^{-1}K^{-1}$ at 670 K for n-type conduction.31 At room temperatures, the sample was p-type with σ = 1.5x10^{-4} Sm^{-1}, S = 25 μVK^{-1} and a PFT of 0.0028 $Wm^{-1}K^{-1}$ [75]. The enhancement in PFT at higher temperatures was a result of increased Seebeck coefficient values with increasing conductivity, which was unusual and was attributed to improved mobility. Investigations of the thermal conductivity of $MoTe_2$ are also very limited. Yan et al. determined the c-axis thermal conductivity of 2H-$MoTe_2$ as 1.5 $Wm^{-1}K^{-1}$ at 300 K using the time-domain thermoreflectance (TDTR) method [76]. DFT calculations estimated the in-plane lattice thermal conductivity of monolayer 2H-$MoTe_2$ to be around 60 $Wm^{-1}K^{-1}$ at room temperature [77]. These stud-

ies indicate that 2H-$MoTe_2$ can be a potential candidate for thermoelectrics, especially in the few-layer limit when the band structure changes due to quantum confinement and the chemical potential can be tuned by the gate voltage. In this work, I have studied the temperature-dependent thermal conductivity to report a comprehensive experimental and theoretical study of room-temperature in-plane thermoelectric transport in thin 2H-$MoTe_2$ flakes.

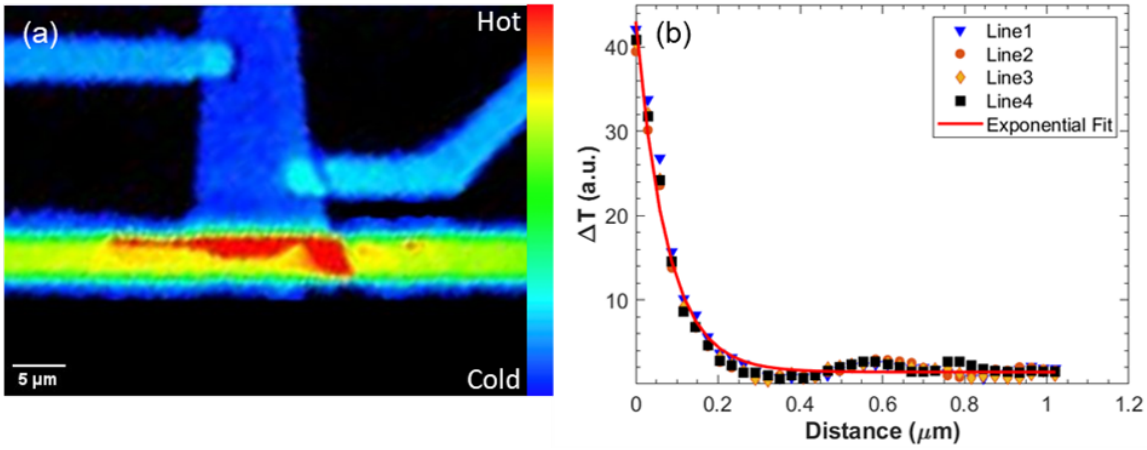

Figure 2.4: (a) Thermal image (temperature map) of the sample surface with 5 V supplied to the heater. Temperature decay curves were taken along the sample perpendicular to the heater. (b) Temperature decay curves and their corresponding exponential fit for thermal conductivity extraction.

2.3.2 Experiment and Results

In-plane thermal conductivity was measured for two flakes of 2H-$MoTe_2$. The first one was 25 nm in thickness and was annealed for the electrical measurements at room temperature. The second flake was 90 nm thick flake that was not annealed for which we extended our measurements down to 190 K. Fig. 2.5 summarises the measurements for these two flakes as well as data from the literature for bulk, [78] supported, and unsupported flakes [79]. The thermal conductivity measurement versus thickness follows an expected trend where the thermal conductivity is reduced for thinner samples. According to the Wiedemann–Franz law, [80] the electronic contribution to the thermal conductivity is only on the order of 0.01 $Wm^{-1}K^{-1}$, which is negligible even with back

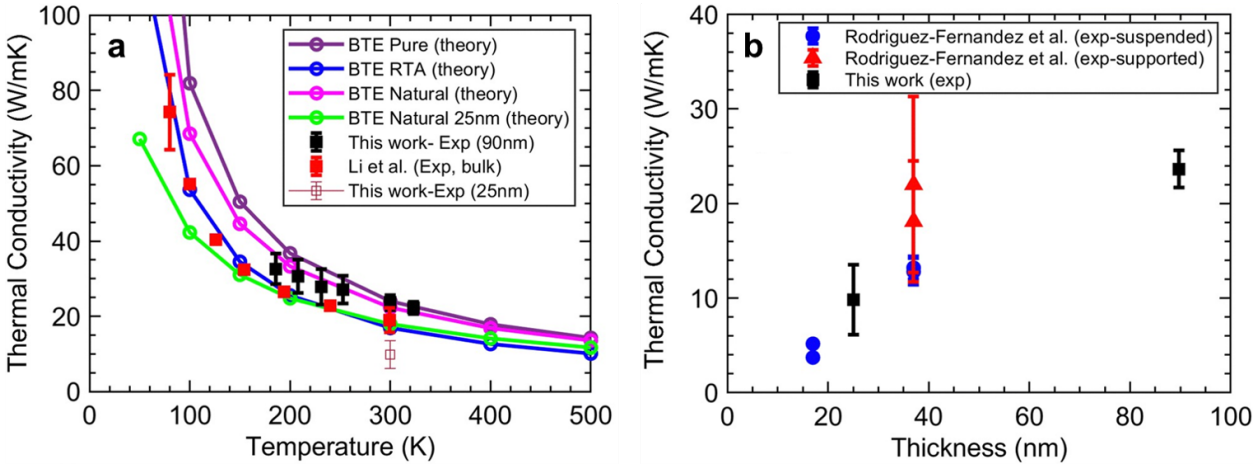

Figure 2.5: (a) Calculated thermal conductivity versus temperature of natural and pure 2H-$MoTe_2$ bulk along the in-plane direction using iterative solutions of BTE. The green line represents the theoretical thermal conductivity when boundary scattering (25 nm size) is included and results for RTA solutions of BTE (bulk-non-iterative) are plotted in blue for comparison. Experimental in-plane thermal conductivity of 90 nm (not annealed) and 25 nm (annealed) thick flakes and literature data of bulk 2H-$MoTe_2$ are shown with squares. (b) Experimental in-plane thermal conductivity of 2H2H-$MoTe_2$ as a function of thickness at room temperature, compared with flakes measured by opto-thermal Raman technique.

gate modulation added. Consequently, we presume that gating has no effect on thermal conductivity. For the same reason, we only incorporate lattice thermal conductivity calculations using first principles in our theoretical approach. Fig. 2.4a shows the temperature dependence of the calculated thermal conductivity of bulk 2H-$MoTe_2$ along the in-plane direction. The lattice thermal conductivity of 2H-$MoTe_2$ is calculated within both the relaxation time approximation (RTA) considering 3-phonon processes and the full iterative solution to the phonon Boltzmann transport equation for an isotopically pure sample. It is well known that the RTA solution provides a poor approximation to the lattice thermal conductivity when compared to the full iterative method, even though the RTA results are closer to the experimentally measured bulk values. These results are obtained by considering the interaction cutoff for cubic inter-atomic force constants calculations up to the seventh nearest neighbor. At room temperature, the calculated thermal conductivity of the isotopically pure bulk 2H-$MoTe_2$ is 24 $Wm^{-1}K^{-1}$. The addition

of the naturally occurring isotope scattering lowers the thermal conductivity by 10% to 22 $Wm^{-1}K^{-1}$. This value is close to 19 $Wm^{-1}K^{-1}$ reported for bulk 2H-$MoTe_2$ [78] and 23.6 $\pm$ 1.96 $Wm^{-1}K^{-1}$ measured for our 90 nm thick flake. The measured thermal conductivity value for our 25 nm thick sample is much smaller and is 9.8 $\pm$ 3.7 $Wm^{-1}K^{-1}$ which as shown in Fig. 2.4b is consistent with other literature data reported but it is not consistent with the theoretical calculations. Part of the difference is coming from the boundary scattering. The addition of the size effect in the simplest approximation can be done by adding a v/L term, where v is the group velocity and L is the thickness, to the scattering rates to serve as the boundary scattering. The addition of this boundary scattering term lowers the theoretical thermal conductivity further by 22% and is shown in the plot by the green dashed line. This is still larger than the experimentally measured value for the thin 25 nm flake. The difference can be attributed to defects (Te vacancies) inside the experimental sample as well as phonon–electron scattering rates. We note that our thin flake was annealed and hence contains more Te vacancies which are beneficial in increasing the electrical conductivity.

2.4 Thermal Transport of 2D Polycrystalline $PtSe_2$ Thin Films

Polycrystalline $PtSe_2$ Thin Films were synthesized via post-selenization of a pre-deposited Pt film prepared by low-pressure chemical vapor deposition (LP-CVD) in Dr. Sang-Kwon Lee's group at the Department of Physics, Chung-Ang University, South Korea. The electrical, and thermoelectric characterizations were done by Jung-Min Cho, and Min-Jeong Kim respectively under the supervision of Dr. Sang-Kwon Lee, the temperature-dependent thermal conductivity measurements was taken by Farjana Ferdous Tonni, and the DFT calculations were done by Sree Sourav Das under the supervision of Dr. Mona Zebarjadi.

2.4.1 Motivation and Objective

2D $PtSe_2$ has the potential to be utilized in TE devices, as it exhibits semiconducting behavior in a single-crystalline monolayer and transitions to a semi-metallic nature with

an increase in the thickness to three or more layers [81, 82]. The semiconductor-to-semiconductor transition characteristics of 2D $PtSe_2$ are advantageous for improving the power factor of TE devices by simultaneously enhancing the Seebeck coefficient and electrical conductivity [83–85]. Moreover, Lee et al. observed the interface-induced Seebeck effect in stacked 2D/2D $PtSe_2/PtSe_2$ homostructures, which played a crucial role in increasing both the Seebeck coefficient and the power factor of the sample [86]. This significant improvement in the TE performance is a result of the additional Seebeck effect generated by the longitudinal temperature gradient of the 2D/2D $PtSe_2/PtSe_2$ homostructures. However, more detailed studies on the temperature-dependent electronic and phononic transport in single-layer $PtSe_2$ and stacked 2D/2D $PtSe_2/PtSe_2$ films have not yet been conducted. This issue motivated us to investigate the temperature-dependent in-plane thermoelectric characteristics at temperatures ranging from 40 K to 300 K.

2.4.2 Experiment and Results

The temperature-dependent in-plane thermal conductivity was measured using heat diffusion imaging. The in-plane thermal conductivity for a single $PtSe_2$ film (3 nm) was determined to be ∼24.9 W/mK at 300 K. Temperature-dependent in-plane thermal conductivity for the single $PtSe_2$ film is presented in Figure 4d and compared with the theoretical values calculated using the Callaway model. In particular, the measured value shows that the Umklapp peak of the single $PtSe_2$ film was slightly shifted to a higher temperature compared with the theoretical calculation. This phenomenon is related to phonon-boundary scattering at the surface, which causes polycrystalline $PtSe_2$ to form small single-crystalline nanograins. The thermal conductivity reached a maximum value of ∼94.5 W/mK at 97 K, and decreased to ∼12.1 W/mK when the temperature dropped to 42 K. The thermal conductivity value for 2-stacked $PtSe_2/PtSe_2$ (3 nm/3 nm) homostructures was found to be ∼19.7 W/mK at 300 K which is within the error bar of the single $PtSe_2$ film in comparison. This may be attributed to the fact that stacking of the second $PtSe_2$ might have introduced boundary effects, causing the sample to have an effective thickness of 3 nm for the phonon transport.

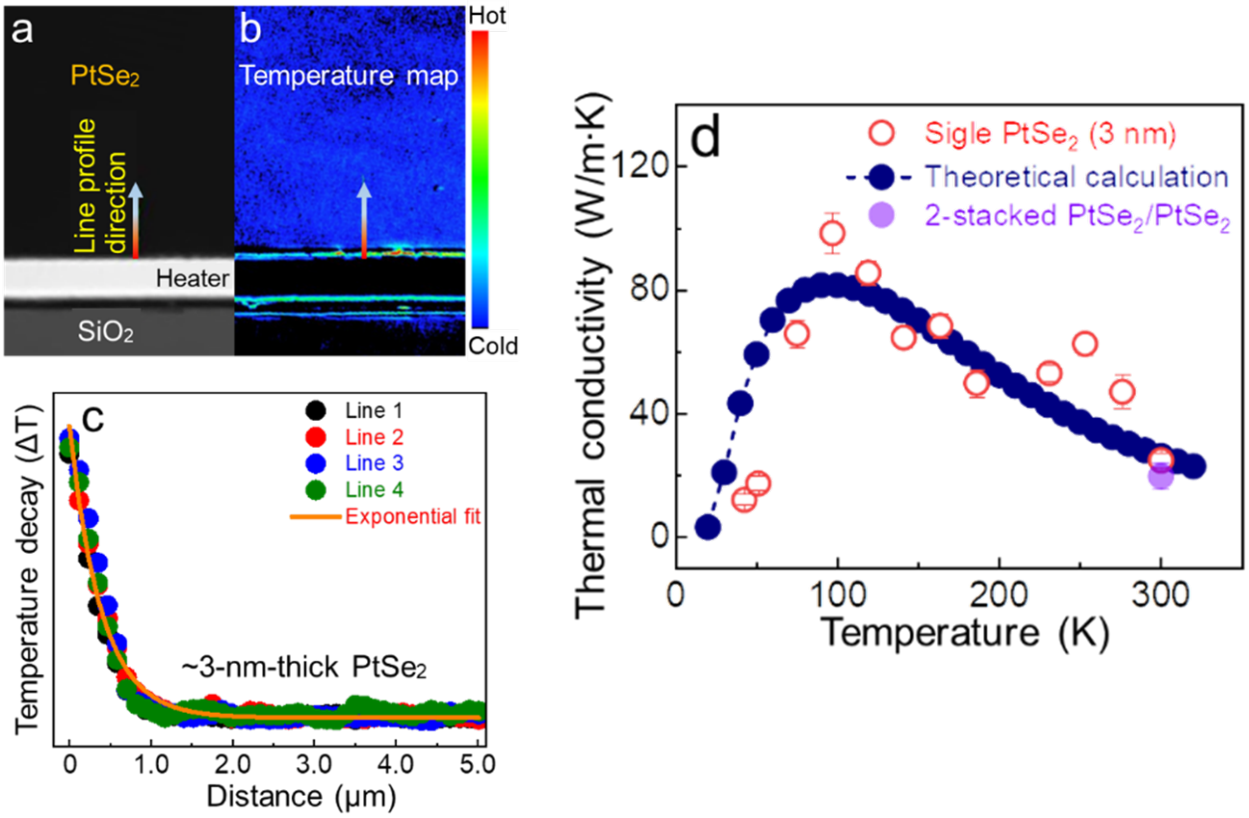

Figure 2.6: Temperature-dependent in-plane thermal conductivity measurements of the single $PtSe_2$ thin films. (a) Optical image of the 3-nm-thick $PtSe_2$ with a Cu heater line, (b) Temperature map of the PtSe2 sample at 300 K, (c) Four representative temperature profiles and their corresponding exponential fitting curves at 300 K. (d) Temperature-dependent in-plane thermal conductivity of the single $PtSe_2$ film and the corresponding theoretical results obtained using the Callaway model. The purple circle represents the in-plane thermal conductivity of the 2-stacked $PtSe_2$ homostructure.

Chapter 3

Thermoelectric Transport in thin films and 2D layered materials

3.1 In-Plane Thermoelectric Transport in $Bi_{77}Sb_{23}$

$Bi_{77}Sb_{23}$ thin films grown on nano-patterned InP substrates were fabricated at the University of Warwick, UK. The thermoelectric transport characterization was done by Farjana Ferdous Tonni under the supervision of Dr. Mona Zebarjadi.

3.1.1 Background and Motivation

Topological insulators are promising candidates for thermoelectric energy harvesting as they have conducting surface states with high mobility while insulating in the bulk (due to bandgaps) allowing efficient charge transport with minimization in electronic heat conduction through the bulk material. Since the bulk does not conduct electrons efficiently, the Wiedemann-Franz law suggests that electronic heat transport is also suppressed. $Bi_{1-x}Sb_x$ is such a material that has enormous potential for use in thermoelectric applications. $Bi_{1-x}Sb_x$ is the first 3D topological insulator to be experimentally discovered [87] after being theoretically predicted by Fu and Kane [88]. A 3D topological insulator has metallic conductivity properties solely on its surface, supporting topologically protected gapless states [89, 90]. Nonmagnetic impurities do not affect these states as the surface states are topologically protected. As a result, backscattering is reduced, increasing the surface conductance [91, 92]. Achieving the perfect scenario of a topo-

logical insulator with an entirely non-conductive interior is challenging due to common narrow gaps and the existence of defect-related residual bulk carriers that contribute to the conduction. Nanostructuring may be used to suppress bulk electronic conduction by increasing the surface-to-volume ratio, which enhances surface state transport while limiting the contribution from the insulating bulk [93]. Several ways of nanostructuring have been studied. For example, making ultra-thin membranes or nano-ribbons could accomplish this, but they have limited practicality in device manufacturing. Another method is to introduce a large number of holes in bulk BiSb samples to enhance the surface-to-bulk ratio. This can improve zT due to two factors: 1) the surface states' contribution to the conductance, and 2) the suppression of phonon thermal conductivity [94]. Similar nanostructuring might be accomplished by depositing thin films of the appropriate thickness on nanostructured substrates. The advantages of a nanostructured substrate include preserving the high electrical conductivity of topologically protected interface and surface states while suppressing phonon transport due to enhanced scattering at the complex, three-dimensional substrate–TI interface. Thermoelectricity of non-stoichiometric $Bi_{1-x}Sb_x$ has been studied for decades; depending on the composition, the electrical behavior of bulk specimens varies from semimetallic to TI to semiconductor [95–99]. Because the band structure of the alloy depends on the Sb composition as shown in Figure 3.1, for a Sb composition lower than 7%, the $Bi_{1-x}Sb_x$ band structure is the same as that of pure Bi. In other words, $Bi_{1-x}Sb_x$ behaves as a semimetal since there exists an overlap between the valence band and the conduction band. Within the range $0.07 < x < 0.22$, the system exhibits characteristics similar to those of semiconductors where the bandgap of the system typically lies between 0.2 eV to 0.4 eV, and an increase in x beyond 22% results in a transition to semimetallic behavior [100].

In the groundbreaking work of Fu and Kane [88], the narrow gap superconductor $Bi_{1-x}Sb_x$ is anticipated to exhibit strong topological insulator characteristics for the range $0.07 < x < 0.22$. As mentioned before, this prediction was subsequently verified through experimental investigations conducted by Hsieh et al [87], utilizing Angle Resolved Photo Emission Spectroscopy (ARPES) on a $Bi_{0.9}Sb_{0.1}$(111) surface. It's been confirmed that the thin-film nanostructuring can extend the presence of surface states beyond the bulk topological insulator region for $0.22 < x < 0.35$, due to quantum size

effects that open an external bandgap and delineate the boundary with the semimetallic region [98]. According to Gunes et al. [101], ball-milled nanostructured samples exhibit broader semiconducting composition regions $(0 < x < 0.5)$ compared to bulk samples, which have $0 < x < 0.22$. This work aims to exploit this advantage by fabricating nanostructured substrates with rough surfaces and depositing BiSb thin films on them to induce topological insulator-like behavior beyond the compositional limit of $0 < x < 0.22$.

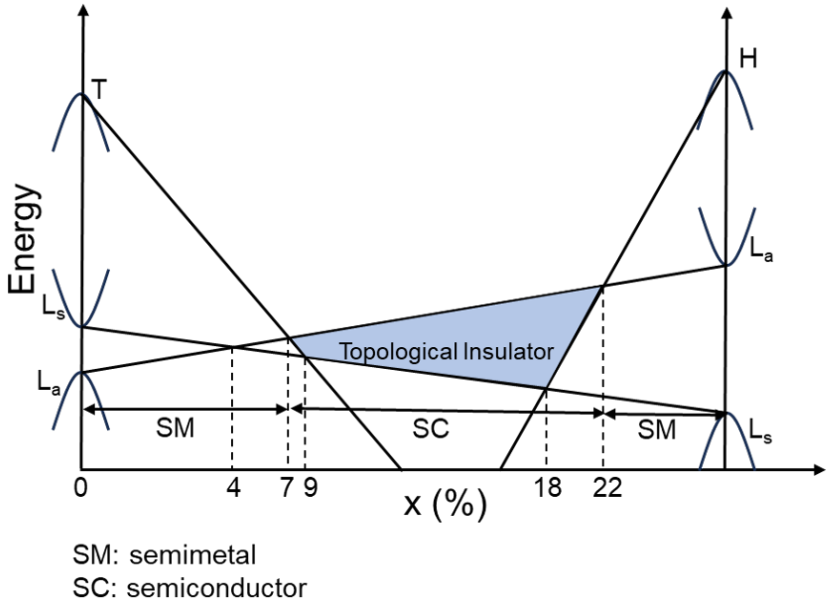

Figure 3.1: $Bi_{1-x}Sb_x$ band structure as a function of Sb composition (x) [Figure ref. Lenoir et al. 1995].

BiSb films are typically grown using molecular beam epitaxy (MBE). In this work, $Bi_{77}Sb_{23}$ thin films have been prepared using thermal evaporation in a conventional thin-film deposition system. The films were deposited on both conventional flat InP substrates and Ar-sputtered nano-patterned InP substrates, and their thermoelectric properties were compared.

3.1.2 Devices and Methods

Sample Fabrication

Six samples were prepared on flat and patterned InP substrates in the commercial Mantis thin film deposition system using thermal evaporation as listed in Table 4.1. These

samples were prepared via three major steps. Firstly, five patterned InP (8 mm × 8 mm) substrates were heavily bombarded by accelerated Ar+ ions inside the High Vacuum (HV) system. The substrates were initially degassed inside the chamber using an IR lamp for about 15 minutes to reach a temperature of around 200°C. After degassing, Ar + sputtering was started for different time durations (5-30 minutes) at a pressure of (2.5 ± 0.5) $\times 10^{-4}$ mbar at an energy of (2.6 ± 0.2) keV. The position of the substrates was chosen to collect the maximum number of Ar ions. All were under nitrogen to minimize surface oxidation. Before BiSb growth, they were etched into a diluted solution of 5% HCl in IPA (i.e. volume wise, concentrated HCl to IPA) and then kept in IPA. The flat substrate of sample MP50 was left for 60 seconds in the solution to remove any contaminants and the oxide layer, more than the other patterned substrates, which were rinsed for only 20 seconds to preserve the patterning. Secondly, all of the substrates were dried using a nitrogen gun, then masked and loaded quickly in the Mantis chamber to avoid surface reoxidation. Subsequently, the substrates were degassed at 250°C at 10^{-7} mbar and then left at this temperature with rotation to achieve a uniform composition of BiSb deposition. Bi and Sb thermal boats were heated to a low growth rate (0.5 nm /min) to obtain high-quality crystalline samples. After deposition, all samples (InP substrates with BiSb films on) were rinsed in an acetone ultrasonic bath for 90 s, to remove any extra BiSb dust. Third, a layer of gold (i.e. contact electrodes) was deposited using the lithography technique: on the masked samples by sputtering a gold target (50% power) with Ar + with a flow of 3 cm^3 / min (at 3.5×10^{-3} mbar) for 7 min. The lift-off process was completed by rinsing each sample in an ultrasonic bath of acetone to remove the residual gold and photoresist materials.

Characterization

The distribution of the elemental composition of the samples was confirmed with scanning electron microscopy with energy dispersive X-ray spectroscopy (SEM-EDX) from the flat sample and averaged from 5 scans in two different pieces, with a difference of 1%, confirming the compositional uniformity. Since all BiSb thin films were grown under identical conditions, the representative composition was determined from the flat sample only, assuming minimal variation among the rest. The thickness was measured

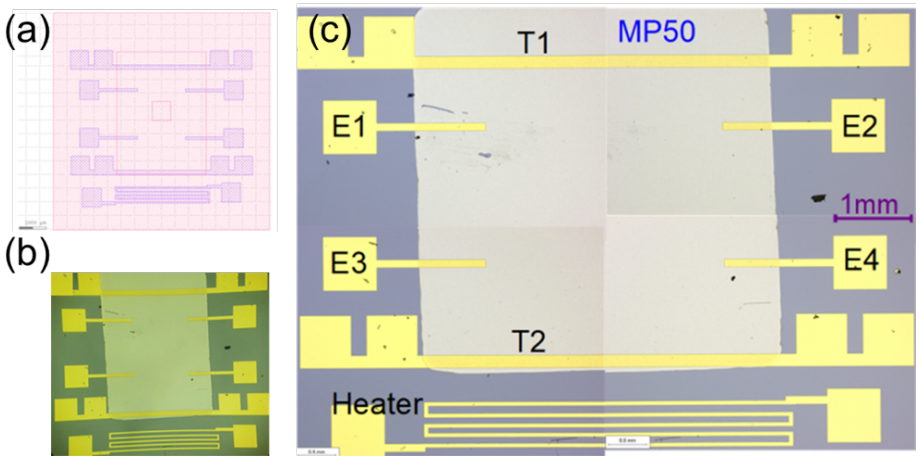

Figure 3.2: The BiSb thermoelectric device (a) The design of the photoresist mask (b) The final BiSb device used (MP50) contains three layers, an InP flat substrate, a BiSb film, and the gold electrodes. (c) Magnified images of MP50 gold pattern, comprising four electrodes (E), two thermometers (T), and a heater. The electrode pads (E1-E4) are 0.7mm wide, see scale bar in panel (c).

by scanning the AFM tip over a step, it was then averaged from 4 scans at different locations on the MP50 sample (147 $\pm$ 3 nm). Similarly, the gold layer thickness was measured to be (120 $\pm$ 5 nm). The AFM was also used to study the surface morphology of the patterned substrates and the deposited BiSb films. Figure 3.3(a) shows a correlation between the RMS roughness and the SR value to the sputtering time of the patterned samples. After increasing monotonically for the first ten minutes of sputtering, both parameters plateaued at a surface ratio of 1.8 and a roughness of 40 nm. This implies that sputtering for more than ten minutes does not increase the patterned sample's surface area. Panels (b-l) demonstrate 3D images of the patterned substrates next to their corresponding BiSb films (MP50-MP55). Overall, the nano-patterning was observed in all the Ar+-sputtered InP substrates' morphologies. The surface morphology of the BiSb films is, somehow, correlated to their substrates. Table 3.1 lists the RMS roughness, SR values, and the corrected thickness of the prepared films. In the form of the device, the structure of the flat one (MP50 sample) and the other patterned one (MP54 sample) were investigated using XRD, Bragg-Brentano geometry. MP50 and MP54 exhibit a texture dependency on the substrate type. Figure 3.4 shows the XRD patterns of these samples compared to the $Bi_{80}Sb_{20}$ (PDF 04-023-9518) card [102]. The flat sample MP50 has BiSb

Sample	MP50	MP51	MP52	MP53	MP54	MP55
Sb (at %)	23.4	-	-	-	-	-
Bi (at %)	76.6	-	-	-	-	-
Thickness (nm)	147.0	-	-	-	-	-
Ar+ Sputtering time (min)	0	5	10	15	25	30
RMS roughness (nm)	9.7	24.0	38.0	35.0	45.0	40.0
SR (substrate)	-	1.22	2.15	2.12	2.44	2.08
SR (film)	-	1.10	1.49	1.27	1.38	1.48
SR (avarage)	-	1.16	1.82	1.69	1.91	1.78
Average thickness (nm)	147.0	126.7	80.9	86.8	77.2	82.5

Table 3.1: The EDX composition and AFM parameters of the MP50-55 series. The thickness of the flat sample is determined from the AFM line profile (see Figure 3.3).
The SR values are extracted from topographs in Figure 3.2

(003) and (006) peaks, confirming the (003) orientation with some minor (012) phase. In contrast, the patterned sample (MP54) has the dominant (012) phase, with some (003) and polycrystalline portions. The origin of the '*' labeled peak is unknown; it may be split from the InP (200) peak due to sputtering-induced strain. Other peaks in the XRD pattern belong to the InP substrate and the gold electrodes.

Electrical Resistance Measurement

The samples were packaged in DIP and wire-bonded to the package legs. Then these devices were mounted on a JANIS cryostat for electrical transport measurements in the 10 K-300 K temperature range under vacuum ($\sim 10^{-6}$ torr). The standard 4-point probe configuration was used for all electrical resistance measurements. Electrical currents were sent through the contacts at the two ends of the samples, and electrical voltages were measured by the two contacts on the side of the samples, between the current leads.

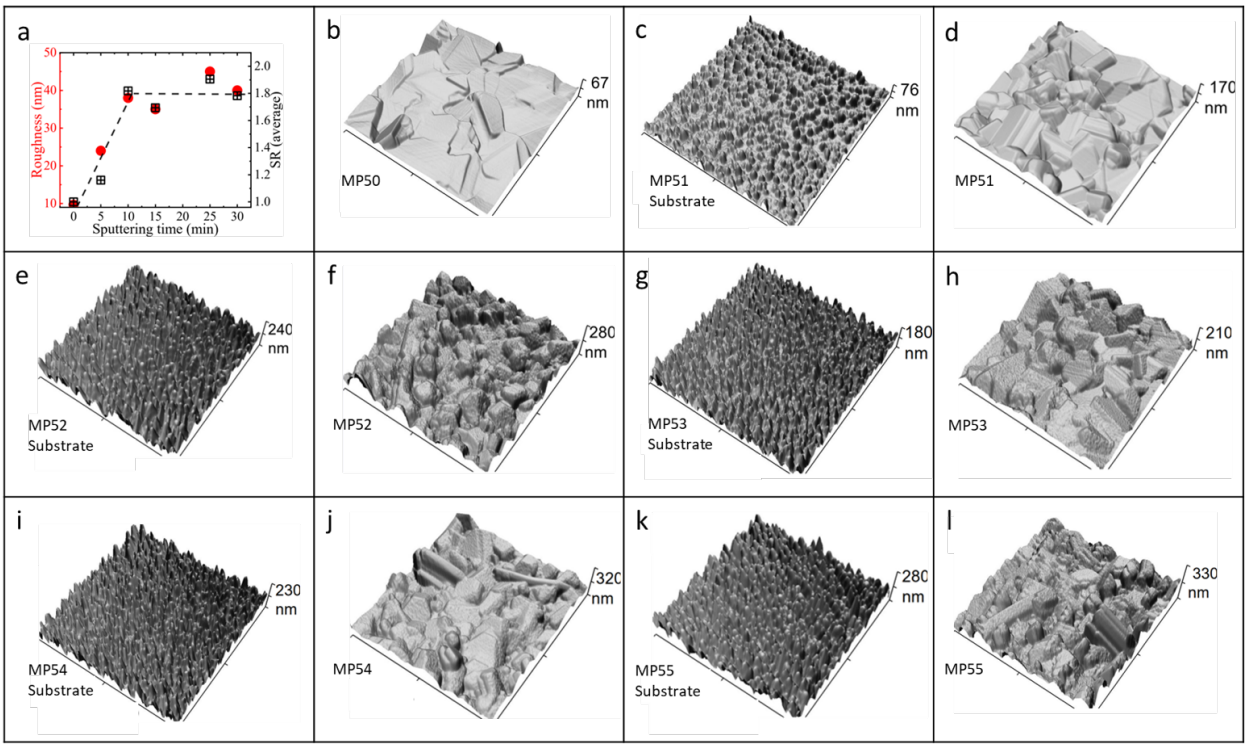

Figure 3.3: (a) Roughness and average SR values as a function of the Ar+ sputtering time. The dashed line is included as a guide to the eye. (b)-(l) AFM 3D topographs of BiSb films on the flat (MP50) and the patterned (MP51-55) samples next to their corresponding patterned InP substrates. The scan dimension is 2µm ×2µm for each topography.

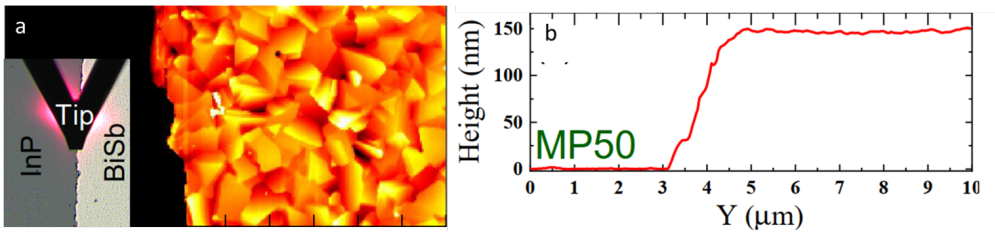

Figure 3.4: (a) AFM Thickness measurements of BiSb on InP substrate (MP50) at the edge; (inset shows zoomed-out-image of the position of the AFM tip during the measurements) (b) the corresponding mean height profile at the edge.

Seebeck Coefficient Measurement

The Seebeck coefficient was measured using a resistive heater and two calibrated thermometers in the temperature range of 100 K to 300 K. The current was applied to the heater to generate a temperature difference across the two ends of the samples as a result of Joule heating. This temperature difference and the produced Seebeck voltage

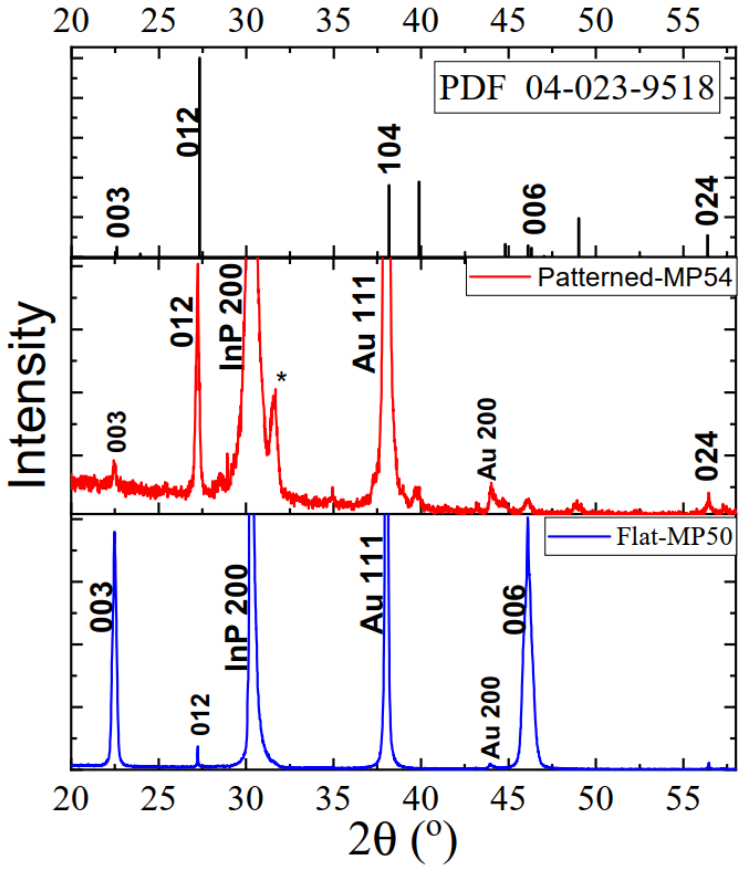

Figure 3.5: XRD patterns of the flat (MP50) and the patterned (MP54) samples with their gold electrodes on. The top panel is $Bi_{80}Sb_{20}$ (PDF 04-023-9518) card [Figure ref. Gates et al. 2019]; all indexed peaks belong to that card except specified. The intensity axis is linear and scaled to maximize the BiSb peaks.

were measured using the two thermometers at the two ends of the samples using the Keithley 2182A nanovoltmeter. The Seebeck coefficient was measured in the one-heater two-thermometer configuration. Up to 105 mA current is passed through the heater during measurements, and the generated Seebeck voltage is recorded by the Keithley 2182A nanovoltmeter. The temperature difference was interpreted from the resistance changes of the two gold thermistors at the two ends of the thin films.

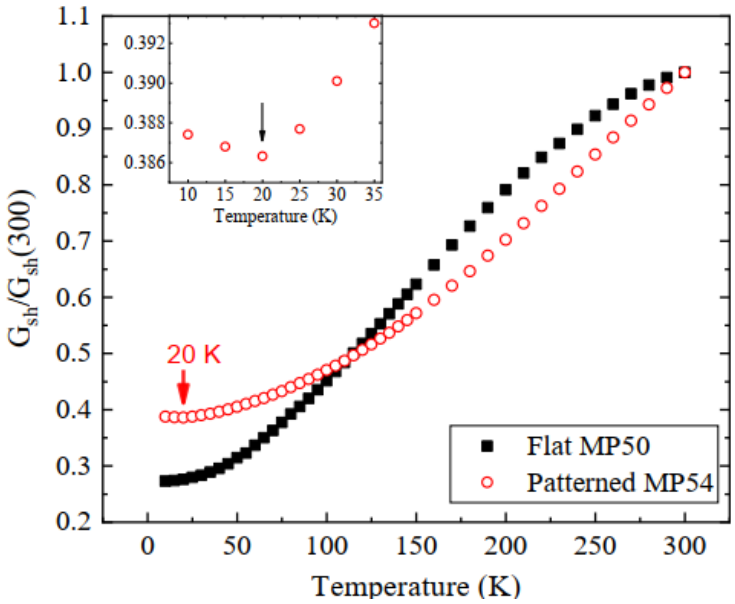

Figure 3.6: The temperature dependence of the total sheet conductance in the flat, MP50, and the patterned, MP54 samples normalized to the value at 300 K. The inset shows the minimum conductance value in the patterned sample.

3.1.3 Results and Discussions

Temperature dependent conductivity

To investigate the effect of nanostructured substrates on the electrical conductivity of the samples, the temperature-dependent electrical conductivity measurement has been done in the temperature range 10 K to 300 K. The sheet conductance of the topological insulators (Gsh) comes from two channels, the bulk conductance (G) and the surface states conductance (Gss), such that $G_{sh} = G_{ss} + G$. The way that G and G_{ss} depend on temperature is different. For a semiconducting interior, $G = G_o e^{-\Delta E/K_B T}$, where G_o is constant and ΔE is the thermal activation energy for electrical conduction. ΔE used to be considered as $E_g/2$ [103], which is valid in cases such as single crystal semiconductors with no gap states measured at high temperature, but not with low-temperature measurements in disordered material [104]. The behavior of G_{ss}, on the other hand, is different because it shows a metal-like conduction that decreases with temperature. Both the flat sample (MP50) and the patterned sample (MP54) had their conductance measured from 300 K to 10 K in order to examine the conduction mechanism in the samples. The conductance of the patterned film ($G_{sh} = 0.018S$) was approximately five

times lower than that of the flat film ($G_{sh} = 0.1S$) at 300 K. There might be three possible causes for the observed differences: (1) The BiSb film on the patterned sample is thinner and exhibit non-uniform thickness, leading to variations in its properties, (2) the carriers in the patterned film might experience scattering due to the roughness at the InP/BiSb interface, which could affect transport properties, and (3) the BiSb film on the patterned sample shows a different crystallographic texture, with the (012) orientation being less well-ordered compared to the (003) orientation, which could explain the variation in material properties. The calculated band structure of Bi_3Sb is highly anisotropic [105], and the composition used in this work $Bi_{77}Sb_{23}$, is similar to Bi_3Sb in terms of crystallographic symmetry and electronic characteristics. As a result, it is highly probable that thin films oriented in (003) and (012) directions will have different effective bulk conductivities, reflecting the anisotropic nature of the material's electronic structure. The bulk conductance decreases and the metallic conduction increases at varying rates as the samples cool. The conductance of both films, normalized to its value at 300 K, is shown in Figure 3.5. Both films' conductance generally drops with cooling, indicating that bulk semiconducting behavior predominates. In other words, the bulk conductance decreases more quickly with cooling than the metallic conductance increases. The patterned sample MP54 exhibited a minimum conductance value at 20 K, which was not observed in the flat one (see inset). At this minimum, the decrease in bulk conductance is equal to the increase in metallic conductance. This demonstrates two things: (1) that the sample contains metallic states; and (2) that the patterned sample has a greater contribution from surface states to conduction than the flat one because of the higher surface-to-bulk ratio in the former.

Thermoelectric measurements

To gain a clearer understanding of how patterning influences thermoelectric performance, the resistance and Seebeck coefficient of the samples were measured. Due to the increase in SR and the creation of a rough surface from the patterning, the thickness of the patterned samples becomes non-uniform, resulting in a lower average value, as shown in Table 3.1. Hence, in this section, we analyze and compare the resistance (R), Seebeck coefficient (S) and (S^2/R) values for all the flat and patterned samples, rather

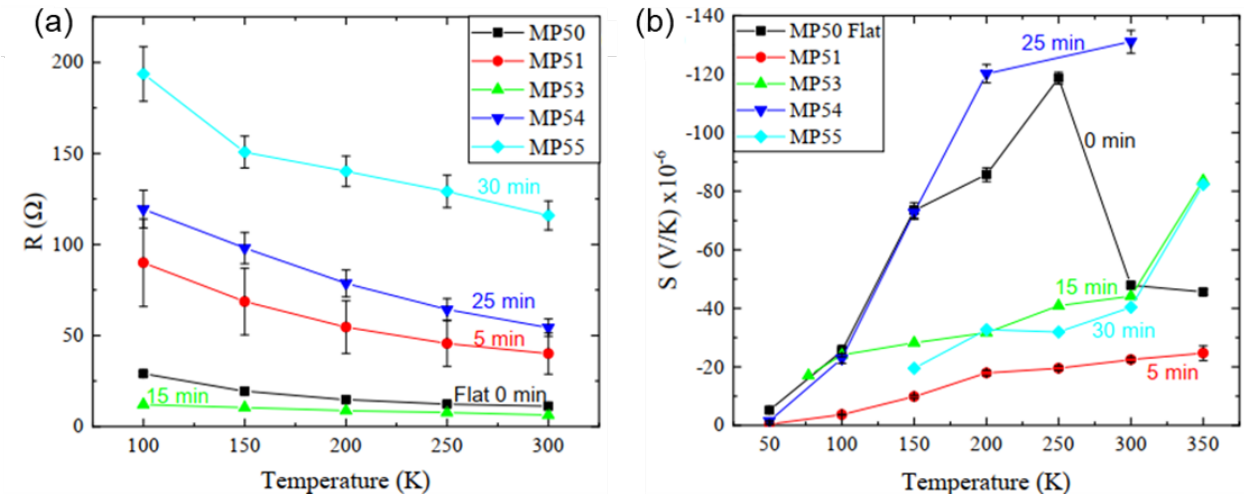

Figure 3.7: The effect of nano-patterning the substrates on the thermoelectric parameters of BiSb thin films: (a) The resistance as a function of temperature; (b) the Seebeck coefficient as a function of temperature. Each plot is labeled with the corresponding substrate sputtering time (in the same color).

than using conductivity and power factor. Overall, the patterning of the samples had a substantial impact on their thermoelectric performance. Figure 3.6 shows the dependence of the resistance and the Seebeck coefficient on both the temperature and the Ar+ sputtering time. In Figure 3.6a, the resistance of all samples decreases with temperature, demonstrating the dominant semiconducting behavior of all flat and patterned samples as previously discussed. The resistance increased with the sputtering time because of the smaller average thickness, phase difference, and increasing non-uniformity except for the 15-minute sputtered sample (MP53). The low resistance of sample MP53 suggests that we may have found an optimal SR ratio that maximizes the contribution from surface states, due to the increased surface-to-bulk ratio. However, since we only have one sample of each, additional evidence is required by creating more samples with nanostructured InP substrates subjected to 15 minutes of Ar+ sputtering to confirm the consistency of the results. All samples exhibit negative Seebeck coefficient (S) values as shown in Figure 3.6b, confirming the n-type semiconducting behavior in the grown films. The Seebeck coefficient (S) increases with temperature in all patterned samples, but peaks at 250 K in the flat sample before decreasing, likely due to the bipolar effect at higher temperatures. The bipolar effect occurs when both electrons and holes contribute

to the charge transport, which tends to reduce the Seebeck coefficient as the temperature increases. In our samples, we rely on the nanostructured substrates to induce topological insulator-like behavior, where surface conduction dominates. In contrast, the flat substrate, lacking nanostructuring, likely exhibits semimetallic behavior, as suggested by the Sb composition in the sample, which can lead to a different temperature dependence of the Seebeck coefficient. While no clear trend is observed between S and sputtering time, patterning generally leads to a reduction in S values. For comparison, the S values at 300 K range from 22 µV/K to 130 µV/K, which is close to the 90 µV/K observed in (012) ball-milled $Bi_{77}Sb_{23}$ samples.[106]. The resultant power-factor-equivalent term (S^2/R) is plotted in Figure 3.7a versus the temperature of the prepared films. The maximum value for the flat sample occurs at 250 K, while the randomness in the Seebeck coefficient (S) values with sputtering time is also reflected in the (S^2/R) values. In other words, patterning the InP substrate leads to an uncontrollable reduction in the variation of the (S^2/R) values. Figure 3.7(b) shows the power factor of the flat sample (MP50) versus temperature. At a temperature of 250 K, the power factor reaches a maximum value of 6 mW/mK^2, which is higher than the maximum power factor of 4.6 mW/mK^2 reported for (003)-oriented $Bi_{80}Sb_{20}$ co-sputtered films with a thickness of 100 nm [107]. It also exceeds the maximum power factor of 5.3 mW/mK^2 for a $Bi_{91}Sb_{09}$ thin film grown on CdTe(111), which also peaked at 250 K [108].

A thermal transport study was not possible because the Microsanj setup uses the thermoreflectance method, which is sensitive to surface reflectivity and roughness. This method was unable to capture accurate thermal images from the rough samples with nanostructured substrates. To fully evaluate the impact of nano-patterning on the thermoelectric figure of merit (zT), a thermal conductivity measurement using a more suitable setup is necessary.

To estimate the figure of merit (zT) for the flat sample, we used the temperature-dependent thermal conductivity values of the polycrystalline 150-nm $Bi_{80}Sb_{20}$ thin film published by Völklein et al. [109]. Estimated zT values peak to reach 0.67 at 250 K, this peaking trend was observed in different-composition, different-thickness BiSb thin films at 200-250 K [110]. This zT is greater than both the $Bi_{88}Sb_{12}$ hot-pressed samples (0.28-0.3 around 250 K) [111] and the melt-spun n-type $Bi_{85}Sb_{15}$ bulk samples with micron-sized

grains, which have a zT of around 0.6 at 125 K [112]. Estimating the figure of merit

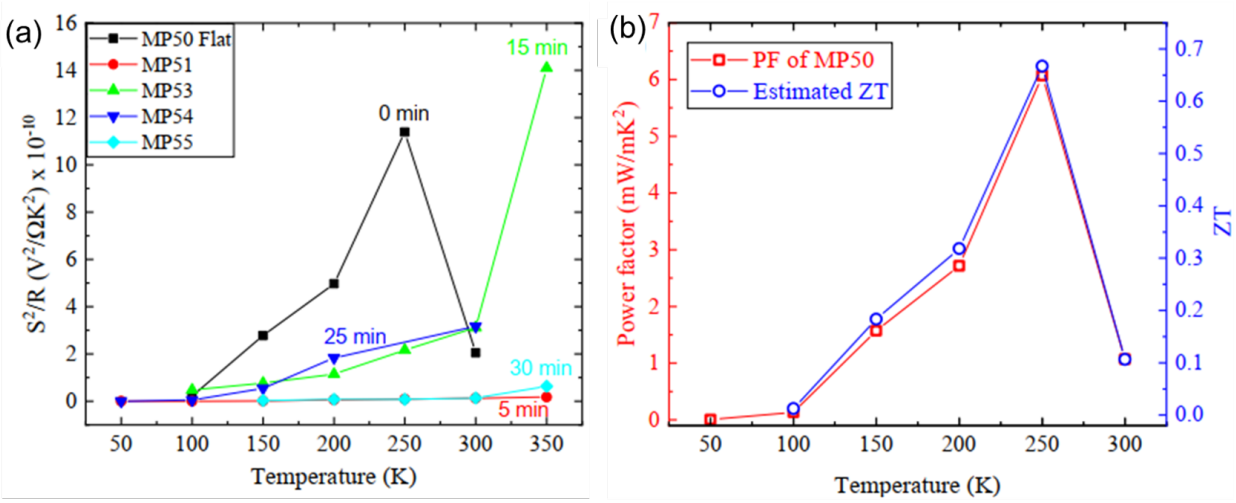

Figure 3.8: (a) The dependence of power factor equivalent term (S^2/R) on the substrates patterning in the BiSb samples. (b) The power factor as a function of the temperature of the flat BiSb sample (MP50); zT is estimated using thermal conductivities from the literature [Figure ref. Völklein et al. 1987].

(zT) for patterned films is challenging. Even when using the average thickness approach to estimate the conductivity and power factor values, the thermal conductivity of the patterned samples remains unpredictable. However, the thermal conductivity of $Bi_{75}Sb_{25}$ (012)-oriented ball-milled samples is 2.51 W/mK at room temperature [106], which is not far from the polycrystalline value of 3 W/mK that we used in our estimation [110]. Additionally, for the patterned samples, other important factors are believed to hinder heat conduction. These samples are thinner, less textured, and likely have smaller grains, which results in more grain boundaries and potentially increased phonon scattering. This would lead to lower thermal conductivity. Consequently, a comprehensive dataset of thermal conductivity values is required to accurately evaluate the zT values.

3.2 In-Plane Thermoelectric Transport in $\gamma - InSe$

γ-InSe crystals which were grown by the vertical Bridgman-Stockbarger method by Dr. Sergiy Krylyuk from Dr. Albert Davydov's group at the National Institute of Standards and Technology. Thin flakes of both intrinsic and n-type γ-InSe were exfoliated from the γ-InSe crystals,

appropriate devices were made, and temperature-dependent thermal conductivity measurements, and electrical, and thermoelectric characterizations were done by Farjana Ferdous Tonni under the supervision of Dr. Mona Zebarjadi.

3.2.1 Background and Motivation

Two-dimensional (2D) layered materials are promising candidates for nanoscale and flexible electronics, owing to their distinctive mechanical, thermal, electronic, and physical properties. These materials consist of atomically thin layers connected by weak van der Waals forces in the out-of-plane direction while maintaining strong covalent bonds between atoms within each layer. The discovery of monolayer graphene through mechanical exfoliation [113] marked a pivotal moment in 2D materials research, opening a new era of exploration. It has been demonstrated that 2D materials exhibit exceptional electronic and thermal properties attributable to their unique band structure. Thermal properties of 2D materials, such as phosphorene and phosphorene-based materials, transition-metal dichalcogenides (TMX_2, TM = Mo, W; X = S, Se, and Te), and III-VI metal monochalcogenides (MX, M = Ga, In; X = S, Se, and Te), have attracted significant attention and spurred intense research interest. The anisotropy of their structure is reflected in their thermal conductivity. For example, these materials are proposed as an anisotropic interface to connect 2D devices to the substrate, dissipating heat in the in-plane direction while minimizing cross-plane heat exchange between the substrate and the device when such exchanges are not desired [114]. Among 2D layered materials Indium selenide (InSe) stands out with remarkable performance in the fields of electronics, optoelectronics as well as spintronics owing to its high electron mobility [115, 116], moderate bandgap [117], high photoresponsivity [118], and strong spin-orbit coupling [119]. Such a wide range of applications requires a clear understanding of thermal transport in the material for efficient thermal management. The study of thermal transport in bulk InSe is well-established, while investigations on the thermal conductivity of 2D flakes have yielded inconsistent results. The objective of this study is to investigate the thermal conductivity of 2D InSe flakes, aiming to clarify these inconsistencies and provide a deeper understanding of the thermal transport properties at the nanoscale. In addition, the Seebeck coefficient and electrical conductivity were also examined to evaluate the

overall thermoelectric performance of the 2D InSe flakes. The thermal conductivity (κ) of bulk γ-InSe was previously reported to be from 10.42 $Wm^{-1}K^{-1}$ to 12 $Wm^{-1}K^{-1}$in the in-plane direction at room temperatures [120–122]. Though several works on the thermal conductivity κ of 2D InSe have been reported, significant discrepancies exist in reported values. The in-plane thermal conductivity of 27.5 $Wm^{-1}K^{-1}$ at room temperature was reported for a 4 nm thick 2D InSe on SiO_2 substrate with a SiO_2 capping layer using temperature-dependent Raman spectroscopy by Botcha et al. in 2018. Adopting Al_2O_3 substrate instead of SiO_2 improved the κ to 65.1 $Wm^{-1}K^{-1}$ due to the compressive strain on Al_2O_3 [123]. Similar study has shown that adding an Al_2O_3 capping layer to a 30 nm thick γ-InSe flake on SiO_2 substrate can enhance the κ from 38.2 $Wm^{-1}K^{-1}$ to 53.1 $Wm^{-1}K^{-1}$, due to the interface charges [124]. In contrast with these high thermal conductivity values, in 2021 Buckley et al. reported significantly lower thermal conductivity for 2D γ-InSe using scanning thermal microscopy. They investigated the size and thickness-dependent κ of 2D γ-InSe in thin or small flakes (less than 5 layers or the lateral area is less than 2 μm^2) noting boundary scattering effects. In addition, the in-plane κ of thicker InSe flakes with larger areas remains below 1.4 $Wm^{-1}K^{-1}$ due to the ability of the InSe flake to dissipate heat from the SThM tip is lower than that of SiO_2. The study further demonstrated that the κ of 2D InSe can be significantly enhanced by a high-k h-BN substrate and suppressed by a low-k PMMA substrate, making them useful for heat dissipation and thermoelectric applications, respectively [125]. The variations in reported κ values of 2D InSe highlight the strong dependence of thermal transport on external factors such as substrate, flake size, and measurement techniques. While substrates like Al_20_3, and h-BN enhance thermal transport via strain or interface effects, low-k substrates like PMMA suppress it, making InSe tunable for applications in both heat dissipation and thermoelectrics. The methods employed to measure thermal conductivity can directly contribute to the observed discrepancies. Temperature-dependent Raman spectroscopy (used by Botcha et al.) is an indirect method that can overestimate κ due to assumptions about the phonon decay process whereas Scanning thermal microscopy (SThM) (used by Buckley et al., 2021) directly probes local heat transport and can be more sensitive to boundary scattering, leading to lower κ values. These findings emphasize the importance of carefully considering experimental conditions when

evaluating the intrinsic thermal properties of 2D InSe. Hence, the focus of this study is mainly on understanding the effects of temperature and doping on γ-InSe flakes of similar thicknesses. I have also investigated the gate-dependent Seebeck coefficient at room temperature and electrical conductivity to estimate the thermoelectric figure of merit zT.

3.2.2 Devices and Methods

Single Crystal Growth and Characterization

InSe single crystals were grown using the vertical Bridgman-Stockbarger method. Initially, polycrystalline InSe was synthesized by reacting high-purity In (99.99%) and Se (99.99%) in a 52 at.% In to 48 at. % Se ratio inside vacuum-sealed quartz ampoules at 720°C for 8 hours. The ampoules were graphitized through acetone pyrolysis to prevent selenium from reacting with the quartz. A non-stoichiometric mixture was used based on previous literature, which indicated that an In-rich charge enhances the yield of the InSe phase by avoiding peritectic decomposition during the melt cooling process [126]. The resulting poly-InSe was milled and loaded into a new ampoule, which was then sealed under vacuum and placed in a vertical Bridgman furnace. Prior to crystal growth, the InSe charge was maintained at 720°C for 3 hours to achieve melt homogenization. The molten charge was then moved through a thermal gradient at a rate of 0.5 mm/h. To obtain n-type doped InSe crystals, Sn (5 at. %) was added to the In:Se mixture during polycrystalline InSe synthesis. This resulted in the production of InSe ingots with a length of 3.5 cm and a diameter of 1 cm. The crystal structure was identified using X-ray diffraction and annular dark-field scanning transmission electron microscopy (ADF-STEM), with both techniques confirming the presence of the γ phase of InSe [127–129]. Room-temperature electron concentration and mobility, determined from Hall effect measurements, were 4×10^{13} cm^{-3} (534 cm^2/V·s) for undoped InSe and 3.5×10^{16} cm^{-3} (782 cm^2/V·s) for Sn-doped InSe.

2D Device Fabrication and Measurement Method

Small InSe flakes from the crystals were exfoliated by the scotch tape method on a pre-cleaned 300 nm SiO_2/p^+-doped Si substrate. The substrates were pre-cleaned by

following a series of sonication in acetone, isopropyl alcohol, N_2 blowing, and finally by cleaning with UV-ozone. For thermal transport investigations in 2D flakes, γ -InSe flakes with an area greater than 15μm x 20μm were chosen. Figure 3.10a shows an optical microscopy image of a representative flake at a magnification of 20X. The uniform distribution of the elemental composition of the samples was confirmed with scanning electron microscopy with energy dispersive X-ray spectroscopy (SEM-EDX). In the next

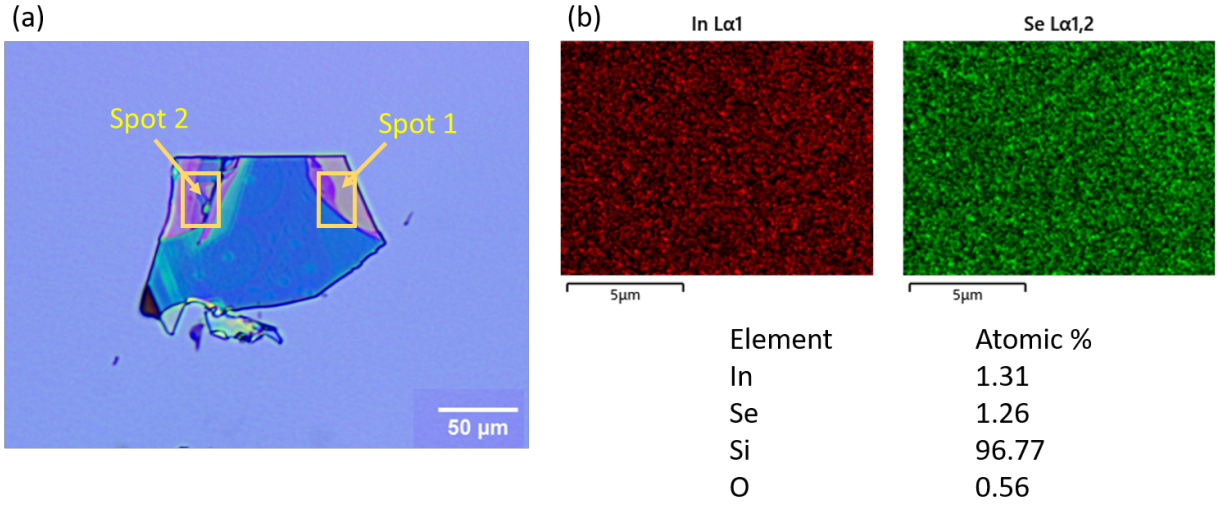

Figure 3.9: (a) Optical image of a representative InSe flake with spots 1 and 2 marked over which SEM analysis was done. (b) SEM-EDX results of spot 1, demonstrate the uniform distribution of In and Se atoms. Silicon and oxygen signals are from the substrate.

step, 2D devices were prepared by depositing metal lines (heater) on the sample for in-plane thermal conductivity measurements. Initially, the heater/electrode pattern was prepared using Quantum Design MicroWriter ML3 Pro direct-write laser lithography (385 nm). 10 nm Ti and 190 nm Ni were evaporated as contact metals (base pressure < 10^{-5} Torr,) at a deposition rate 0.5 Å s^{-1} for Ti and 1.0 Å s^{-1} for Ni. Optical pictures of the final two devices for thermal transport measurements are shown in Figure 3.11a and b. The samples were annealed under high vacuum ($\sim 10^{-6}$ Torr) at 300°C for 30 min in the cryostat immediately before measurements to minimize the effects of environmental contamination during the fabrication processes. Two different setups have been used to measure (a) the thermal conductivity, and (b) the Seebeck coefficient and electrical conductivity.

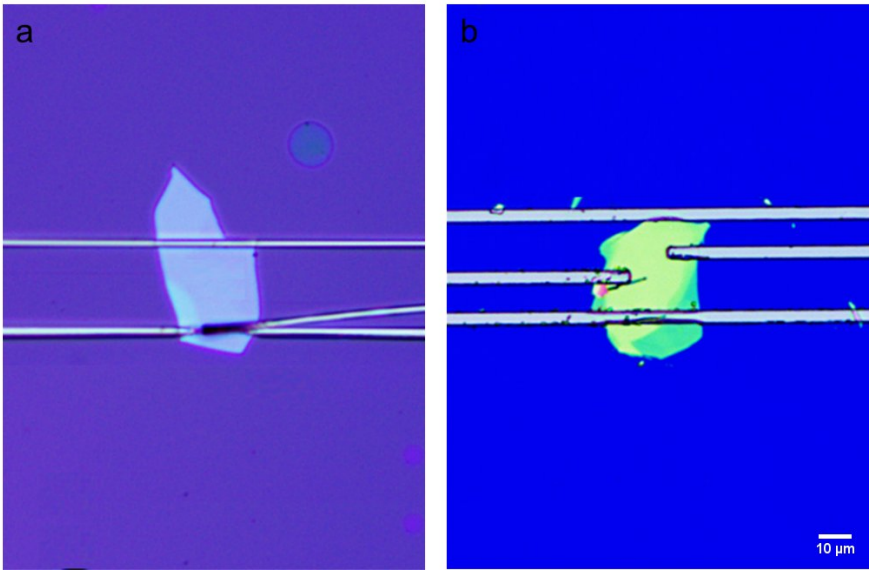

Figure 3.10: (a) Optical image of γ-InSe devices (a) S1-intrinsic and (b) S2- n-doped.

Thermal Conductivity Measurements

In-plane thermal conductivities in the 2D flakes were studied using the thermoreflectance-based HDI method, which captures the temperature decay along the sample after a heat flow injection and extracts the thermal conductivity using the heat spreader model. In this thermoreflectance imaging system, we used a 470 nm blue LED as a light source. Electrical pulses of 3 V and 5 ms duration were sent to the heater with a 20% duty cycle. Details of the measurements are described in Chapter 2.

Seebeck Coefficient Measurement

The wire-bonded DIP package was loaded onto the sample stage of a JANIS cryostat. The samples were annealed under high vacuum ($\sim 10^{-6}$ Torr) at 30°C min in the cryostat immediately before measurements to minimize the effects of environmental contamination during the fabrication processes. To measure the Seebeck coefficient, a temperature gradient was created along the sample by passing a current through the heater. The two thermometers' resistance changes determine the resulting temperature changes. The temperature coefficients of the resistances at each measurement temperature should be calibrated before the Seebeck measurement. The thermometer resistances were measured with AC signals by lock-in amplifiers in 4-wire sensing mode to minimize the noise in the temperature measurements. Finally, the Seebeck coefficient can be deter-

mined by repeating the measurements at various back-gate voltages.

Electrical Conductivity Measurement

A standard 4-point probe configuration was used for electrical resistance measurements. Electrical currents were sent through the contacts at the two ends of the samples, and electrical voltages were measured by the two contacts on the side of the samples, between the current leads.

Finally, the thicknesses of the samples were measured after the thermal conductivity measurements using the Tencor P-7 Stylus Profiler.

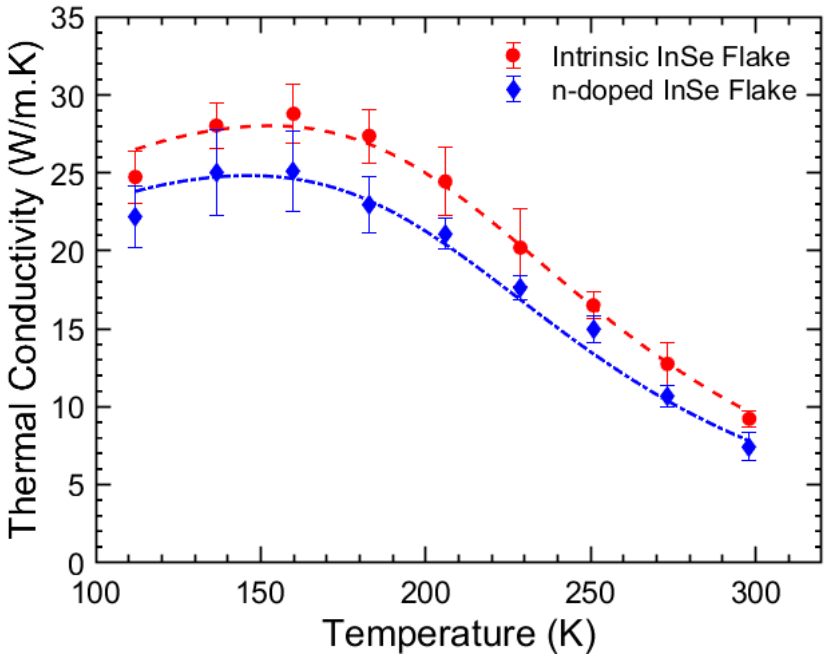

Figure 3.11: Temperature dependent in-plane thermal conductivity of 2D flakes of γ-InSe.

Figure 3.10 illustrates the temperature-dependent thermal conductivity of two distinct flakes of intrinsic and n-doped InSe, with thicknesses of 29.8 nm and 37.53 nm, respectively. In both cases, the thermal conductivity peaks around 150 K before declining, indicating a phonon-dominated transport mechanism. Beyond 200 K, the thermal conductivity follows a T^{-1} trend. At room temperature, we obtained in-plane thermal conductivity for 29.8 nm intrinsic γ-InSe flake 9.2 $Wm^{-1}K^{-1}$ and for 37.53 nm n-type flakes 7.4 $Wm^{-1}K^{-1}$. These values are comparable with the measured κ of exfoliated

β-InSe flakes on Si substrate with aluminum oxide over layer, using beam offset time-domain thermoreflectance (TDTR) [130]. In their study, Rai et al. observed that for 2D β-InSe with a thickness larger than 100 nm, its in-plane κ is essentially independent of the flake thickness. The κ of the thick InSe layer was measured to be only about 8.5 $Wm^{-1}K^{-1}$ along the in-plane direction. We observed that the thermal conductivity of the n-doped flake is slightly lower than that of the undoped flake, despite the minimal difference in thickness. This reduction can be attributed to increased impurity scattering in the doped sample. We also calculated the theoretical thermal conductivity of the n-type γ-InSe flake, utilizing the Callaway model to compare the experimental results.

Theoretical calculation of the thermal conductivities

For the theoretical calculation of thermal conductivity, we used the modified Callaway's model for thin film lattice thermal conductivity with considerations of boundary, point defects, Umklapp and normal scattering processes. It is important to note that the electronic thermal conductivities (κ_e) of the intrinsic and n-doped InSe according to the Wiedemann-Franz law at room temperature (300 K) are approximately 2.50×10^{-6} W/m·K and 3.20×10^{-3} W/m·K. These values are significantly lower than the total thermal conductivity, confirming that heat transport in γ-InSe is dominated by phonons rather than electrons. The calculated data from the Callaway model using the average sound velocity from previous studies fit the experimental values very well. The fitting parameters show that the thermal conductivity difference in the n-doped sample from the intrinsic one comes from the impurity scattering or point defect scattering parameter, with the same phonon scattering parameter for both cases. The modified Callaway model for thin films has the following expression:

$$\kappa = \frac{k_B}{2\pi^2 v_s}\left(\frac{k_B T}{\hbar}\right)^3 \int_0^{\theta_D/T} \tau_c \frac{x^4 e^x}{(e^x-1)^2}\, dx \tag{3.1}$$

where k_B is the Boltzmann constant, v_s is the speed of sound in the material, $\hbar$ is the reduced Planck's constant, T is the absolute temperature, θ_D is the Debye temperature, τ_c is the combined phonon relaxation time.

The combined relaxation time τ_c can be expressed as:

$$\frac{1}{\tau_c} = \frac{1}{\tau_B} + \frac{1}{\tau_I} + \frac{1}{\tau_U} + \frac{1}{\tau_N} \tag{3.2}$$

or

$$\frac{1}{\tau_c} = \frac{v_s}{L} + A\omega^4 + B_U\omega^2 T e^{-\theta_D/\alpha T} + B_N\omega^2 T \tag{3.3}$$

where τ_B is the boundary scattering time, τ_I is the impurity scattering time, τ_U is the Umklapp scattering time with α being the vibrational constant, τ_N is the normal phonon-phonon scattering time, L is the flake thickness, v_s is the average sound velocity, $\Theta_D = v_s \frac{\hbar}{k_B}\left(\frac{6\pi^2 N}{V}\right)^{1/3}$. From the work of Pandey et al [131] the longitudinal and transverse sound velocities are in γ-InSe are $v_l = 3272$ m/s and $v_t = 1853$ m/s, respectively from which the average sound velocity is calculated to be 2060.58 m/s and the Debye temperature for the best fit was found to be 205K. The fitting parameters that resulted in the best fit to the experimental data were A, B_U, B_N, and α for which the resulting fit is shown in Figure 3.10 with dashed lines.

Material (γ-InSe)	A (s^3)	$B_U(sdeg^{-3})$	$B_N(sdeg^{-3})$	α
Intrinsic (29.8 nm flake)	5.095e-45	1.3337e-16	1.1347e-26	0.152
n-doped (37.53 nm flake)	1.3241e-43	1.3337e-16	1.1347e-26	0.165

Table 3.2: Fitting parameters used for Callaway's model

Electrical Conductivity

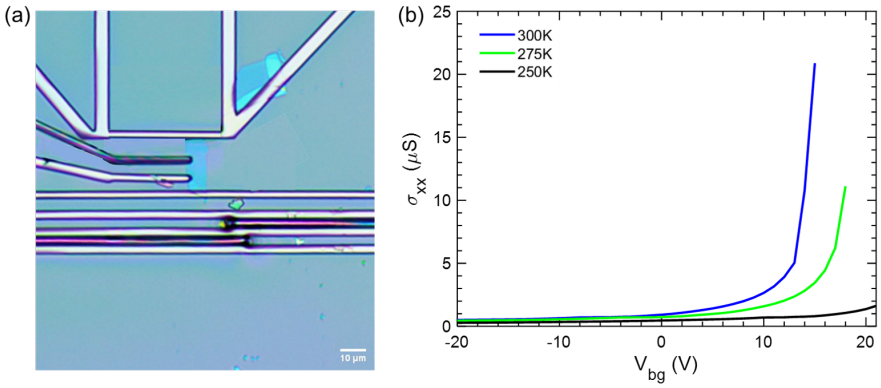

Figure 3.12: (a) n-doped γ-InSe flake with contacts, (b) electrical conductivity measured as a function of V_g at room temperature.

The four-terminal resistance R_{xx} measurements were carried out via an AC lock-in technique, with the corresponding four-terminal conductivity σ_{xx} shown in Figure 3.11 ($\sigma_{xx} = (L/W)(1/R_{xx})$, L, W is the length and width of the sample, respectively). The electrical conductivity in the thinner InSe sample at room temperature is much higher than the values of the bulk sample. The bulk electrical conductivity for the n-doped sample is calculated from the carrier concentration and mobility value to be 4.379 Sm^{-1} whereas for the 7.9 nm thin flake the conductivity under zero applied bias is 116.593 Sm^{-1}. To compare this result with the available literature, it is found that the electrical conductivity of a 10 nm n-type γ-InSe with carrier concentration one order of magnitude higher than that of the sample used in this work was measured to be 1127.7 Sm^{-1} for 25 V back-gate voltage according to [132]. This enhancement can be attributed to the sharper edge of the conduction-band DOS onset due to quantum confinement as shown on the basis of ab initio calculations and Boltzmann transport theory reported in [133, 134] and experimentally verified in [132]. The quantum confinement effect occurs when the material is reduced to a size comparable to the de Broglie wavelength of the carriers (electrons or holes) as shown in their article by [132] for different thicknesses. This confinement alters the electronic structure of the material by creating discrete energy levels. Increased sharpness of the conduction-band DOS at the Fermi level can result from quantum confinement, which means there are more available states for electrons to occupy near the Fermi energy leading to enhanced electron density near the Fermi level. At room temperature, as V_g is swept from -20 V to 15 V, its electrical conductivity is enhanced from 64.31 Sm^{-1} to 2643.38 Sm^{-1}. The conductivity goes up with increasing gate voltages. Since V_g is connected to the highly doped Si, increasing the back-gate V_g means increasing electron density in the n-doped sample. By applying a gate voltage, this modulation of carrier concentration can directly affect the conductivity. More carriers in the conduction band (increased electron density) means higher electrical conductivity. As we go lower in temperature, the lower conductivity confirms the semiconducting behavior.

Seebeck Coefficient

The Seebeck coefficient S was measured in an intrinsic sample of 50 nm thickness at different V_g as shown in Figure 3.12 (b). The negative S value confirms the n-type conduction of the sample. At Vg = 0 V, the sample shows a Seebeck coefficient of $\sim$70 μVK^{-1} at room- temperature. This room-temperature value is about a quarter of that of the bulk single crystal [135]. However, as V_g is swept from 20 V to -20 V, the Seeback Coefficient, S was enhanced from $\sim$70 μVK^{-1} to $\sim$155 μVK^{-1}. The gate-dependent electrical conductivity trend observed in the previous section for an n-type sample demonstrates that increasing the back-gate voltage leads to enhanced conductivity, indicating a higher carrier concentration in the material. Hence, a lower Seebeck coefficient with a higher electrical conductivity is expected due to the inverse relationship between the Seebeck coefficient and carrier concentration.

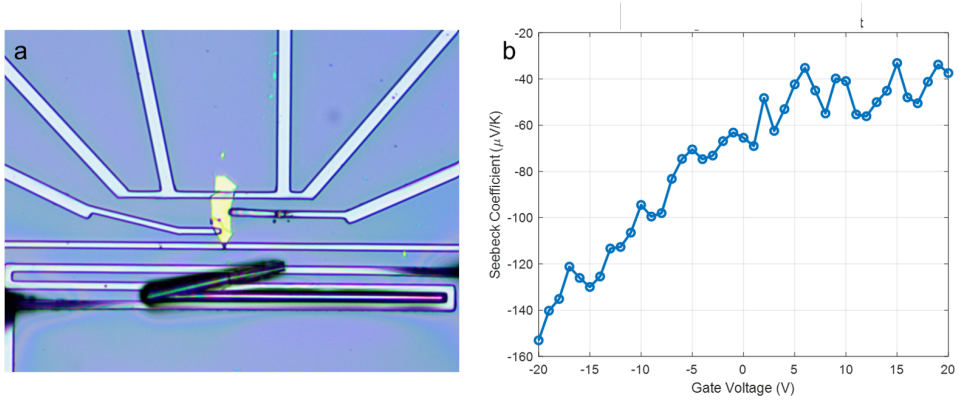

Figure 3.13: (a) Intrinsic γ-InSe flake with contacts, (b) Seebeck Coefficient, S measured as a function of V_g at room temperature.

In conclusion, this study provides valuable insights into the thermoelectric and thermal transport properties of 2D γ-InSe flakes, advancing their potential application in nanoelectronics and thermoelectric energy harvesting. Electrical conductivity measurements on a 7.9 nm γ-InSe flake confirm the quantum confinement effect, aligning with first-principles predictions and demonstrating its role in enhancing thermoelectric performance. However, due to sample-to-sample variations in thickness, a direct comparison of the power factor across different flakes remains challenging. In addition, through heat diffusion imaging, I present the first experimental measurements of the thermal conductivity of γ-InSe flakes over a temperature range of 100 K to 300 K. These results

can deepen our understanding of temperature-dependent phonon transport, which is crucial for optimizing thermal management in nanoscale devices.

Chapter 4

Monte Carlo Simulation of Transient Electron Gas Energy Conversion Thermodynamic Cycle in GaAs

4.1 Background and Motivation

Solid-state modules are environmentally friendly since they do not rely on chemical products, are quiet and maintenance-free as they do not have mechanical components or moving parts, have a long operating life, and can be integrated into microscale semiconductor circuit chips and flexible devices [136–139]. However, the thermal-to-electrical energy conversion efficiency of conventional thermoelectric modules is limited to about 5–15% [140]. The thermoelectric module's efficiency is limited by the material thermoelectric figure-of-merit, zT. The zT of infinity takes us to the Carnot limit while the current commercial zT values are around 1 and the best-reported pick zT values are between 2 and 3, which provides the conversion efficiency still lower than many internal combustion heat engines. Recently a new study showed that a volumetric change in non-equilibrium electron gas in a solid could yield high power conversion efficiency ($\sim 53\%$) by using electronic analogs of an internal combustion gas engine, the Otto cycle [141]. This cycle contains four processes. First, electrons are compressed adiabatically using an electrostatic field and gating. Next, a heat pulse input is applied and it increases the electrons' energy beyond that of the lattice to create a non-equilibrium electron gas. The

heat input is a constant volume process that can be obtained for instance using a light pulse. Electrons retain the gained energy for a very short time, i.e., on the order of a picosecond, before releasing it to the lattice [142]. Next, the high-energy electron gas is released and expands in the larger space in the solid where the electrons perform useful work on a connected load to generate electrical power and reject some of their heat to the lattice. The cycle is then repeated to generate periodic current pulses. The cycle operates at large frequencies and the electrons are out-of-equilibrium with the lattice. Instead of using two steady heat reservoirs, a heat pulse input is used. Therefore, in principle, this cycle is not limited by the Carnot efficiency, which is defined in the case of a quasi-steady-state cycle operating between two constant-temperature reservoirs. Inspired by this, I present here a Monte Carlo simulation of non-equilibrium electron transport in a GaAs-based device by solving the Boltzmann transport equation (BTE) and studying the electron dynamics in a power-generating process when the electrons are confined and heated locally. Here, a 1-D device simulator based on the MC method, which was developed by our group, is modified and adapted for the simulation of heated electronic gas expansion. The bulk MC transport solver for n-type carriers has been evaluated and validated in the past [143, 144]. For this study, I have modified the code to compute the power and the energy delivered to the load.

4.2 Methodology

An ensemble MC code has been used to simulate the electron gas transport in the time domain. In MC simulation, carriers move with Newtonian motion (assuming a classic particle picture) according to the local electric field, referred to as the free-flight step. A random lifetime is assigned to each particle which is weighted by the inverse of total scattering rates. At the end of its lifetime, each electron goes through a scattering process to determine its new wave vector and energy. The cycle is repeated for all electrons and they are synchronized at each simulation time step. At this time, a 1D Poisson equation is solved using the position of all electrons (charge density) and the imposed boundary conditions to include both internal and external forces. The electric field is then obtained and updated locally in the device for the later free-flight steps. The model

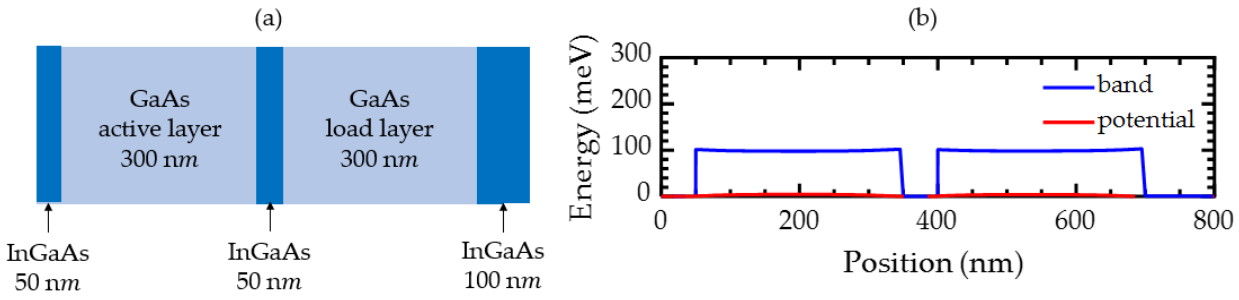

Figure 4.1: a) Schematic of the device structure, b) Conduction band profile and potential.

is simulated in three dimensions, both in real space and k-space. The non-parabolic multivalley band structure is used for each material [145]. The scattering mechanisms include acoustic and polar optical phonon scattering, and ionized impurity scattering, which is calculated using a quantum mechanical approach [35]. The acoustic phonons are assumed to be elastic, however, we have also tested non-elastic acoustic phonons and we have not observed any difference in the device performance. The ionized impurity scattering is calculated using the Brooks-Herring equation [146]. Polar optical phonons are the main inelastic source of electron energy relaxation in the GaAs family. A flat optical band is assumed for these phonons with the energy of 35 meV for GaAs layers. MC is a semiclassical approach since electrons are considered classical particles during their Newtonian motion (free-flight time) and are considered quantum particles at the time of scattering. The code is coupled with a 1D heat conduction equation which tracks the electron-phonon energy exchange to update the lattice temperature. The Fermi statistics are enforced using a shifted Fermi sphere with modified electronic temperature [144]. The boundary conditions in lateral directions (x and y) are reflective and periodic in the z-direction through the contact-electrodes junction. The code is written in Fortran and several tests were made previously to reproduce the experimental data and in particular the carrier mobility [143, 144].

4.3 Results and Discussion

The simulation structure of the proposed 1D device is illustrated in Figure 4.1a with the longitudinal z-axis going from left to right. The device structure consists of InGaAs/GaAs/InGaAs/GaAs/InGaAs. Here, heavily doped (1×10^{17} cm^{-3}) interfacial InGaAs layers serve as semi-metallic contact layers. The first (left-hand side) GaAs is the active device and the second (right-hand side) GaAs layer serves as a load. The simulation is done in four steps replicating the energy conversion or power generation from the non-equilibrium hot electrons undergoing an analogous Otto thermodynamic cycle process presented below. The lattice temperature was kept at 50 K, as at lower temperatures the electron-phonon scattering rates decrease significantly. The device's cross-sectional area is $0.3\times0.3\mu$m^2. Contact layers are 0.05 μm long, the active layer is 0.3 μm long, and the load layer length is 0.3 μm to match the active layer, see Fig. 1a. The GaAs active layer is lightly doped (1×10^{15} cm^{-3}) where the electrothermal energy conversion is happening and power is generated. The second GaAs load layer is also lightly doped (1×10^{15} cm^{-3}) to match with the active layer which is the part where power is delivered. In the first step, the proposed structure (Fig. 1a) is simulated using zero voltages at the right and left contact as the boundary conditions. The doping levels are adjusted so that the final band diagram (Fig. 1b) shows minimum bending and flat bands. Electrons are allowed to reach a steady state under this zero-bias condition. In the second step, the previous steady-state distribution of the carriers is manipulated using the following process. Within the active layer (left-hand side GaAs), a random selection of electrons is moved to the GaAs/InGaAs interface right before the load. The code is set to confine these electrons on the right side, a pre-defined confinement length (120 nm, 40% of the active layer length) within the active layer. The resulting example distribution is shown in Fig. 4.2a, where a higher carrier concentration of electrons can be observed on the right side of the active layer (the interface of the GaAs active layer and the middle InGaAs contact). This process represents the confining of the electrons at the interface and the formation of a compressed electron gas and it is the analogy of applying pressure in mechanical pistons. In a practical device, this step can be accomplished by electrostatic gating in 3D device geometry. The third step is to heat the confined electrons to create hot electrons, which is similar to ignition in gas engines. This can be done in sev-

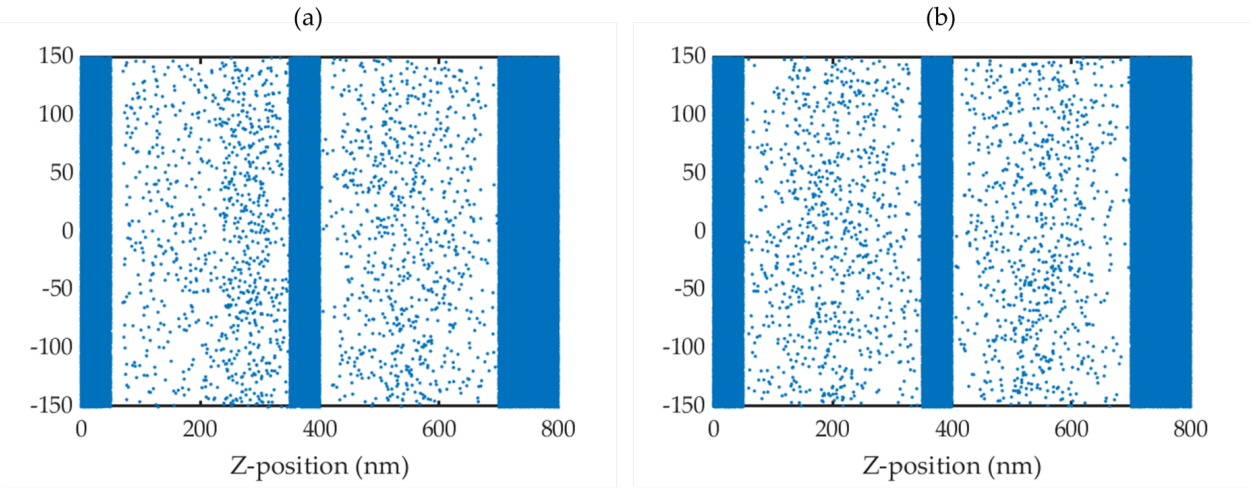

Figure 4.2: a) Electron distribution after compression, b) final electron distribution after releasing them.

eral ways, i.e., by giving energy to the electrons using a Fermi-Dirac distribution with a higher temperature or giving fixed energy to each confined electron which collectively results in the heating of the electrons by gaining sufficient kinetic energy. We use the second method in this simulation as it is closer to the incident light heating condition. As a result of compression in the second step and heating in the third step, the electrons in the confined region are out of equilibrium with the rest of the electrons and the lattice, and they are referred to as 'hot electrons'. Here, we do not consider the time needed for compression and heating and these two steps are performed instantaneously. Finally, in the last step, upon removal of pressure and heat, we allow the hot electron gas to expand. To do so, we assume periodic boundary conditions along the z direction and zero applied bias. The expansion, therefore, is only the result of diffusion. While expanding, they initially perform work at the load, but eventually, the interaction with phonons starts and electrons release their extra energy to the lattice (heat rejection). The electrons lose their energy during a short time in picoseconds in this study case. Hot electrons release their energy via long-range coulomb interactions as they travel and reach the load region i.e., deliver power to the load. This is considered the output work of the thermodynamic cycle. Eventually, they reach equilibrium with other electrons and the lattice. The part of the energy released to the phonons is considered waste energy and lowers the efficiency. During the electron expansion, we monitor the power and

the energy delivered to the load to evaluate the efficiency of this proposed device. The current, j, is calculated by summing over all electrons in each given layer as

$$j_{z-load} = \frac{q}{A}(\frac{n_{tot}}{n_{sim}}) \sum_{i \in load} v_{zi} \tag{4.1}$$

Power in each layer is calculated by summing over the z mesh points along the layer. For instance, the power in the load is given by:

$$P_{load} = \sum_{z \in load} j_z E_z \Delta z \tag{4.2}$$

Finally, the total energy delivered in the load, ϵ_{load}, is calculated by integrating the load power versus time.

$$\epsilon_{load} = \sum_{t} P_{load} \Delta t \tag{4.3}$$

Here v_{zi} is the ith electron velocity in the z-direction, n_{tot} is the actual number of electrons in the device, n_{sim} is the number of electrons used for the simulation, and E_z is the electric field in the z-direction, calculated from the Poisson equation. The thermal conversion efficiency of the device from the compressed electrons at different input energies is calculated using the following equation:

$$\eta_{th} = \frac{\epsilon - \epsilon_0}{\epsilon_{thermal-in}} \tag{4.4}$$

Here, ϵ_0 is the output electrical energy generated inside the load under compression and no heating conditions, and ϵ is the output electrical energy inside the load under compression and heating. Fig 4.3a and b represent the instantaneous current in the active layer and the load layer respectively. As expected, when there is no external potential difference in the device, the current eventually dies out and fluctuates around zero, but we observe instantaneous current in the device in the non-equilibrium condition. Some damped oscillations in the current are observed which are due to the reflectance from the boundaries and energy exchange back and forth between the active region and the load. The average velocity of hot electrons, depending on the input energy, reaches several hundred nm/ps. Given the device length of 300 nm, this corresponds to sub-picosecond transit times, resulting in rapid charge redistribution. These transient effects lead to an inherent inductive-like behavior, as the system temporarily stores and releases energy

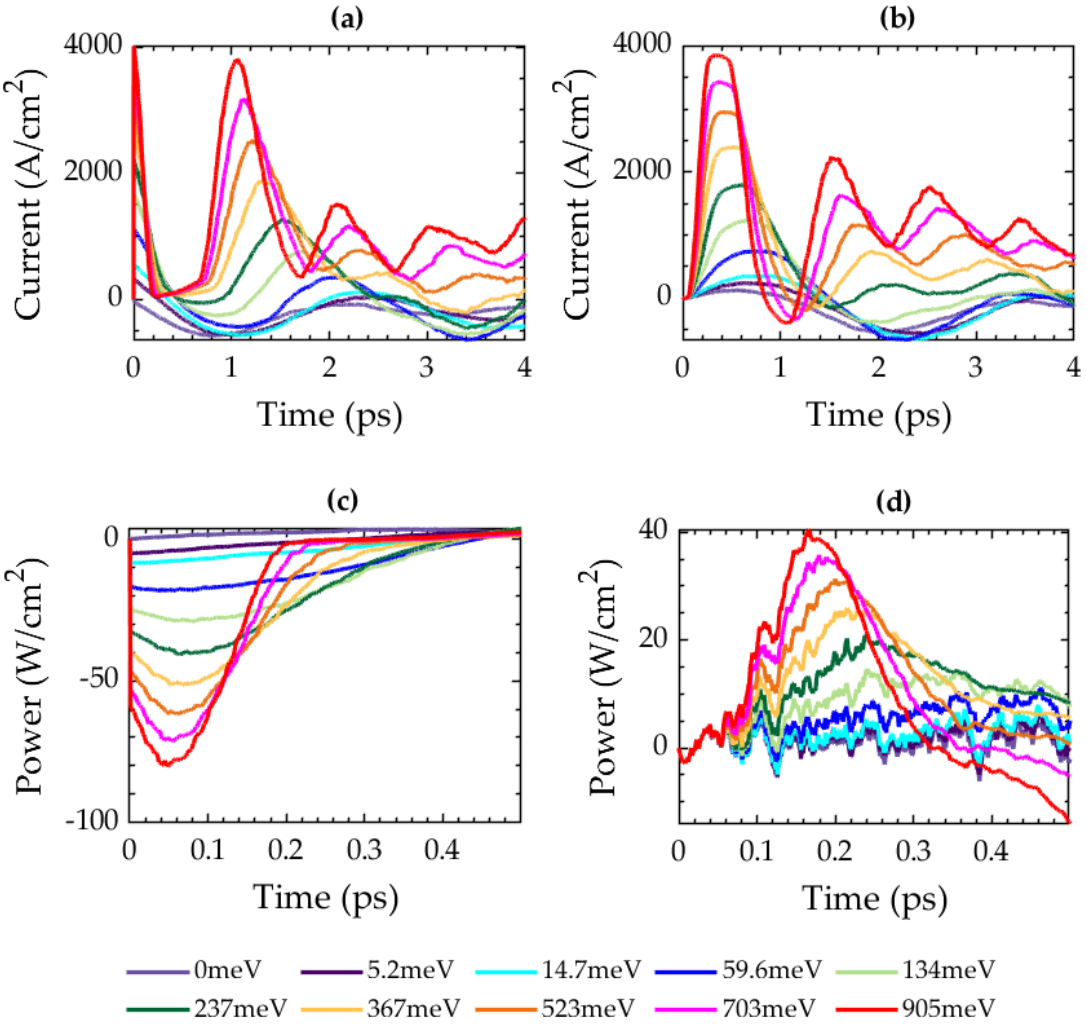

Figure 4.3: Instantaneous current in a) active layer, and b) load layer, instantaneous power c) generated in the active layer, and d) dissipated in the load layer. All curves are calculated for different input energies to the confined electrons.

in response to the evolving carrier dynamics. The confined hot electrons are out of equilibrium with the lattice at the beginning of the release step. Upon release, the power is generated in the active layer in this non-equilibrium transient process within half a picosecond and is transmitted to the load layer via long-range Coulomb interactions. We can observe the power generated in the active layer and the power dissipated in

the load in Fig 4.3c and d respectively. It is expected that the generated power should go to zero as the heat pulse dies out and the resulting current vanishes. However, we observe that the current does not die out completely but rather fluctuates around zero due to reflectances from the boundaries. Hence, we can see that the power curve also fluctuates at large time scales. It reaches a peak value, drops to zero, and then fluctuates around zero following the trend of the current curve when we wait for a longer time. The energy plots in Figure 4(a) and 4(b) show the total energy generated in the active

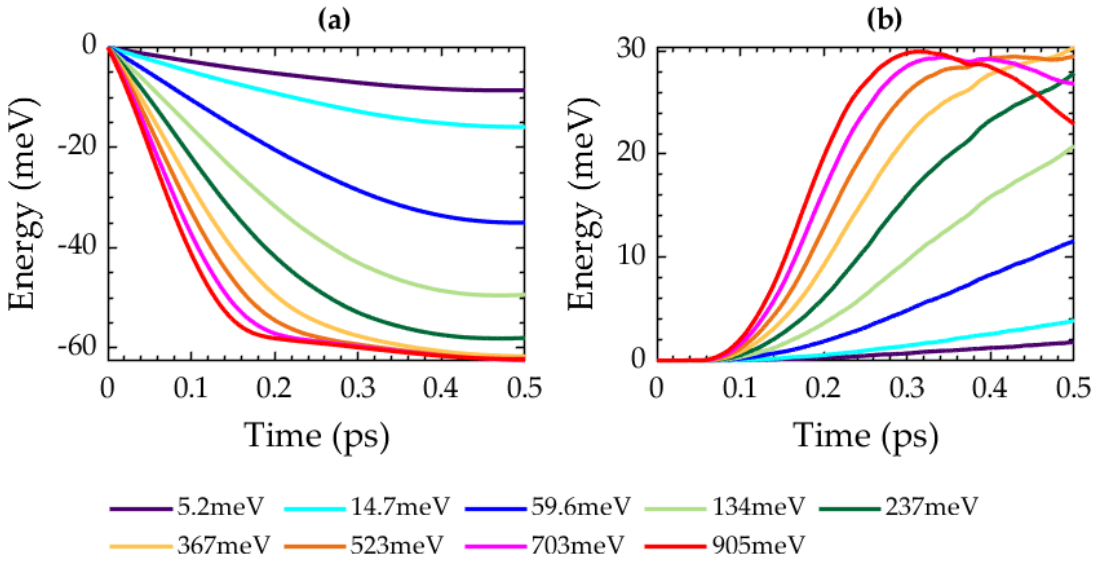

Figure 4.4: Energy a) generated in the active layer, and b) supplied to the load as a function of current. This is used to calculate thermal-to-electrical energy conversion efficiency for different input heating to the electrons.

layer and the total energy delivered in the load which is calculated by integrating the load power versus time (see Eq. 3.3). From the plots with higher input energies we see a shift of the maximum output energies towards earlier times as the electrons travel faster with higher velocities and deliver larger power at shorter time scales. However, the electron-phonon scattering rate also increases with higher electron energies. Hence, with higher input energies, power dissipation dies out faster and energy curves saturate

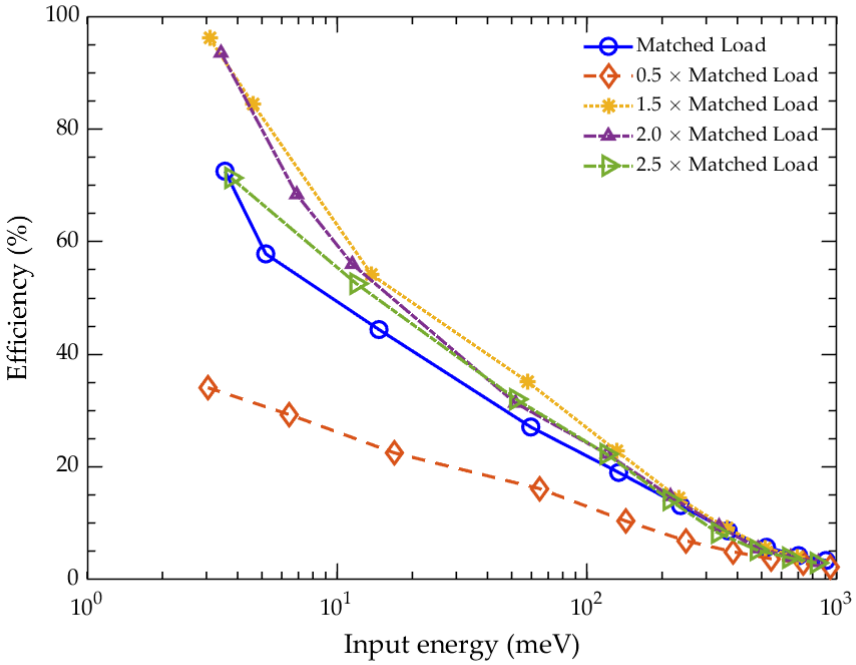

Figure 4.5: Thermal efficiency vs. the input heat energy.

at shorter time scales. The negative power/energy observed in the active region indicates the power/energy generation and the positive power/energy in the load indicates the power/energy consumption in the load. In all cases, we observe saturation of energy at time scales less than 0.5 ps. The saturation is at smaller time scales in the active region compared to the load region which is due to the delay in energy transfer from the active layer to the load. When looking at the load, we observe a drop in the energy at higher energies in Fig 4b. We note that this is not really a drop but a fluctuation, as will be evident if we plot this curve on a larger time scale. The device conversion efficiency is not limited by Carnot efficiency due to its highly transient nature and a single cold reservoir (lattice). Since we only artificially simulated the gating step, we cannot report the total efficiency. Here, we only focus on thermal efficiency. Electrostatic confinement can be reversible and it is not inherently limited by thermodynamic efficiencies. On the other hand, complex optimization of 3D device geometry (e.g. a non-equilibrium metal-oxide-semiconductor CMOS transistor) including a gate electrode will make it harder to

study the fundamental limitation for conversion of heat into electricity. The maximum (ϵ_{load}) is shown in Fig 4.4 and calculated using Eq. 4.2. We used the same amount of compression consistently in all simulations to allow subtraction of the compression energy. $\epsilon_{thermal-in}$ is the input thermal energy and is the sum of the small kinetic energy values given to electrons in the confined region in the heating step. We can observe from the energy plots in Fig 4.4 that as the input energy increases, the output energy also increases and its maximum shifts to lower times. However, the increase in the output energy is much less than the increase in the input energy, resulting in lower efficiency values as the input energy increases. This is shown quantitatively in Fig. 4.5. Here, the results are reported for multiple loads. In all cases, we kept the number of confined electrons the same and only increased the load length. When increasing the load length, the efficiency increases. However, after matched load conditions are achieved (load matching the active layer in terms of its length, 300nm in this case), a further increase in the load length does not affect the efficiency significantly. In a power generation device, it is expected to have an optimal load. Here, the results are transient and calculated on each mesh point inside the load. The saturation of power with load length indicates that the power is dissipated only in the first 300 nm of the load. One should note that energy conversion efficiency of more than 50% is achieved when the input energy is less than 10meV (per electron this is about 12K increase in the temperature, that is from 50K to 62K).

Chapter 5

Conclusion and Outlook

Effective thermal management is a fundamental challenge in modern electronics as device densities continue to rise, necessitating innovative solutions for efficient heat dissipation and energy conversion. This dissertation has explored thermal and thermoelectric transport in two-dimensional thin-film materials, providing valuable insights into phonon transport mechanisms and strategies for improving thermoelectric efficiency.

Silicon-based thermoelectric materials are appealing due to their affordability, compatibility with existing industrial processes, and high power factor. A promising approach to enhancing their performance involves nanostructuring, where periodic nanosized holes are patterned with spacings smaller than the mean free path (MFP) of phonons but larger than that of charge carriers. This strategy effectively reduces the thermal conductivity of silicon thin films while preserving their electrical transport properties. The in-plane thermal conductivity of the holey silicon thin film depends on the neck size between the periodic holes. The room temperature thermal conductivity decreased from 26.4 $Wm^{-1}K^{-1}$ to 4.7 $Wm^{-1}K^{-1}$, nearly 5 times. Smaller neck size suppressed phonon transport more, leading to smaller thermal conductivity values.

Through systematic investigations of in-plane thermal transport in layered transition-metal dichalcogenides ($NbSe_2$, 2H-$MoTe_2$, and $PtSe_2$), this work expands the limited knowledge base on nanoscale heat conduction, contributing to the development of materials optimized for thermal management applications. Being the first in-plane thermal conductivity measurement of few-layer $NbSe_2$, and 2H-$MoTe_2$ samples in the reported temperature range, this work contributed to the research in a significant way by pro-

viding valuable insights into its thermal transport properties of 2D TMDs, aiding in the development of efficient thermal management strategies for nanoelectronic and optoelectronic applications. Likewise the thermal transport study in single $PtSe_2$ and vertically stacked 2D/2D $PtSe_2/PtSe_2$ thin films homostructure indirectly confirms interface formation and decrease in thermal conductivity demonstrating feasibility of utilizing them in TE energy-saving and energy-generating devices.

Additionally, the study of thermoelectric performance in BiSb thin films on patterned nanostructured substrates sheds light on how the patterning can affect their thermoelectric properties. All the flat and patterned films exhibited behavior characteristics of n-type semiconductors and surface states' contribution was detected. The ratio of surface state contribution was consistently higher in the patterned samples, but the total conductance was higher in the flat samples, owing to the different thickness structures and morphology. The Seebeck coefficient increased with temperature for all of the patterned samples, but peaked at 250 K for the flat samples, with a high power factor value (6 mW/mK^2). At the same temperature, the figure of merit was estimated to reach a high value, zT = 0.67 for the flat (003) oriented sample. The thermal transport study was not feasible because the Microsanj setup employs the thermoreflectance method, which is sensitive to surface reflectivity and roughness and was unable to capture thermal images from these rough samples with nanostructured substrates. To fully assess the impact of the nano-patterning on zT, a thermal conductivity study is required for the samples with an appropriate setup.

A complete study on all the thermoelectric properties (thermal conductivity, Seebcek coefficient, and electrical conductivity) of two-dimensional γ-InSe has been done. The findings from electrical conductivity measurement in a 7.9 nm γ-InSe flake confirm the theory of quantum confinement for enhancing the thermoelectric performance of 2D InSe thin films through experimental measurements and first-principles calculations from literature. Through heat diffusion imaging, the thermal conductivity of γ-InSe flakes was measured for the first time in the 100 K to 300 K temperature range. This study contributes to the understanding of 2D thermoelectric materials by offering valuable insights into the temperature-dependent thermal transport properties of γ-InSe. These findings are essential for improving heat management and advancing the perfor-

mance of next-generation thermoelectric and nanoelectronic devices.

A significant outcome of this research is the conceptualization and demonstration of a novel solid-state energy conversion device based on a thermodynamic cycle inspired by the Otto cycle. Unlike conventional thermoelectric and thermionic generators, this approach leverages electron gas dynamics for energy conversion, presenting a pathway to surpass Carnot efficiency. This breakthrough opens new avenues for thermal-to-electrical energy conversion, redefining the efficiency limits of solid-state energy devices.

Looking ahead, future work could focus on refining fabrication techniques for nanostructured thermoelectric materials, further optimizing phonon-electron interactions, and experimentally validating the proposed thermodynamic cycle under various operating conditions. Additionally, integrating these findings into practical device architectures could bridge the gap between fundamental research and real-world applications, advancing next-generation energy-efficient electronics and sustainable power generation technologies.

Bibliography

[1] G. E. Moore, *Cramming More Components onto Integrated Circuits*, Electronics **38**, 114–117 (1965).

[2] C. Bailey. *Thermal management technologies for electronic packaging: current capabilities and future challenges for modelling tools*. In *10th Electronics Packaging Technology Conference*, pages 527–532, (2008).

[3] G. Laguna, M. Vilarrubí, M. Ibañez, et al., *Numerical parametric study of a hotspot-targeted microfluidic cooling array for microelectronics*, Applied Thermal Engineering **144**, 71–80 (2018).

[4] Z. Khattak and H. M. Ali, *Air cooled heat sink geometries subjected to forced flow: a critical review*, International Journal of Heat and Mass Transfer **130**, 141–161 (2019).

[5] W. Liu and M. Asheghi, *Thermal Conductivity Measurements of Ultra-Thin Single Crystal Silicon Layers*, Journal of Heat Transfer **128**, 75–83 (2005).

[6] C. Dames, *MEASURING THE THERMAL CONDUCTIVITY OF THIN FILMS: 3 OMEGA AND RELATED ELECTROTHERMAL METHODS*, Annual Review of Heat Transfer **16**, 7–49 (2013).

[7] A. J. Schmidt, X. Chen, and G. Chen, *Pulse accumulation, radial heat conduction, and anisotropic thermal conductivity in pump-probe transient thermoreflectance*, Review of Scientific Instruments **79**, 114902 (2008).

[8] W. Liu and M. Asheghi, *Phonon–boundary scattering in ultrathin single-crystal silicon layers*, Applied Physics Letters **84**, 3819–3821 (2004).

[9] M. Asheghi, K. Kurabayashi, R. Kasnavi, and K. E. Goodson, *Thermal conduction in doped single-crystal silicon films*, Journal of Applied Physics **91**, 5079–5088 (2002).

[10] Y. C. Tai, C. H. Mastrangelo, and R. S. Muller, *Thermal conductivity of heavily doped low-pressure chemical vapor deposited polycrystalline silicon films*, Journal of Applied Physics **63**, 1442–1447 (1988).

[11] D. G. Cahill, *Thermal conductivity measurement from 30 to 750 K: the 3ω method*, Review of Scientific Instruments **61**, 802–808 (1990).

[12] D. G. Cahill, *Analysis of heat flow in layered structures for time-domain thermoreflectance*, Review of Scientific Instruments **75**, 5119–5122 (2004).

[13] P. Kim, L. Shi, A. Majumdar, and P. L. McEuen, *Thermal Transport Measurements of Individual Multiwalled Nanotubes*, Physical Review Letters **87**, 215502 (2001).

[14] A. A. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao, and C. N. Lau, *Superior Thermal Conductivity of Single-Layer Graphene*, Nano Letters **8**, 902–907 (2008).

[15] K. Kurabayashi, M. Asheghi, M. Touzelbaev, and K. E. Goodson, *Measurement of the thermal conductivity anisotropy in polyimide films*, Journal of Microelectromechanical Systems **8**, 180–191 (1999).

[16] Y. S. Ju, K. Kurabayashi, and K. E. Goodson, *Thermal characterization of anisotropic thin dielectric films using harmonic Joule heating*, Thin Solid Films **339**, 160–164 (1999).

[17] W. Jang, Z. Chen, W. Bao, C. N. Lau, and C. Dames, *Thickness-Dependent Thermal Conductivity of Encased Graphene and Ultrathin Graphite*, Nano Letters **10**, 3909–3913 (2010).

[18] T. Zhu, D. H. Olson, P. E. Hopkins, and M. Zebarjadi, *Heat diffusion imaging: In-plane thermal conductivity measurement of thin films in a broad temperature range*, Review of Scientific Instruments **91** (2020).

[19] Y. S. Touloukian, R. W. Powel, C. Y. Ho, and P. G. Klemens, *Thermal conductivity of nonmetallic solids*, Thermophysical Properties of Matter **2**, 1389 (1970).

[20] W. Jang, Z. Chen, W. Bao, C. N. Lau, and C. Dames, *Thickness-Dependent Thermal Conductivity of Encased Graphene and Ultrathin Graphite*, Nano Letters **8**, 4123–4128 (2008).

[21] G. D. Mahan and J. O. Sofo, *The best thermoelectric*, Proceedings of the National Academy of Sciences of the United States of America **93**, 7436–7439 (1996).

[22] G. J. Snyder and E. S. Toberer, *Complex thermoelectric materials*, Nature Materials **7**, 105–114 (2008).

[23] K. Tyagi, B. Gahtori, S. Bathula, M. Jayasimhadri, N. K. Singh, S. Sharma, D. Haranath, A. Srivastava, and A. Dhar, *Enhanced thermoelectric performance of spark plasma sintered copper-deficient nanostructured copper selenide*, Journal of Physics and Chemistry of Solids **81**, 100–105 (2015).

[24] X.-L. Shi, J. Zou, and Z.-G. Chen, *Advanced thermoelectric design: from materials and structures to devices*, Chemical reviews **120**, 7399–7515 (2020).

[25] L. Yang, Z.-G. Chen, M. S. Dargusch, and J. Zou, *High performance thermoelectric materials: progress and their applications*, Advanced Energy Materials **8**, 1701797 (2018).

[26] L. D. Hicks and M. S. Dresselhaus, *Effect of quantum-well structures on the thermoelectric Bgure of merit*, PHYSICAL REVIEW **8**, 15–1993.

[27] L. D. Hicks and M. S. Dresselhaus, *Thermoelectric figure of merit of a one-dimensional conductor*, Physical Review B **47**, 16631 (1993).

[28] M. S. Dresselhaus, G. Chen, M. Y. Tang, R. Yang, H. Lee, D. Wang, Z. Ren, J.-P. Fleurial, and P. Gogna, *New Directions for Low-Dimensional Thermoelectric Materials***, (2007).

[29] M. Lundstrom and C. Jeong, *Near-equilibrium transport : fundamentals and applications*, (2013).

[30] K. I. Bolotin, K. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Hone, P. Kim, and H. L. Stormer, *Ultrahigh electron mobility in suspended graphene*, Solid state communications **146**, 351–355 (2008).

[31] A. A. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao, and C. N. Lau, *Superior thermal conductivity of single-layer graphene*, Nano letters **8**, 902–907 (2008).

[32] T. Feng, J. He, A. Rai, D. Hun, J. Liu, and S. S. Shrestha, *Size Effects in the Thermal Conductivity of Amorphous Polymers*, Physical Review Applied **14**, 1 (2020).

[33] D. Akinwande, N. Petrone, and J. Hone, *Two-dimensional flexible nanoelectronics*, Nature communications **5**, 5678 (2014).

[34] J. Singh, *Electronic and optoelectronic properties of semiconductor structures*, Cambridge University Press (2007).

[35] M. Lundstrom, *Fundamentals of Carrier Transport*, Cambridge University Press, second edi edition (2000).

[36] C. Jacoboni and L. Reggiani, *The Monte Carlo method for the solution of charge transport in semiconductors with applications to covalent materials*, Reviews of Modern Physics **55**, 645–705 (1983).

[37] K. Tomizawa, *Numerical Simulation of Submicron Semiconductor Devices*, Artech House, Boston (1993).

[38] D. Vasileska, K. Raleva, and S. M. Goodnick. *Monte Carlo Device Simulations*. In S. Mordechai, editor, *Applications of Monte Carlo Method in Science and Engineering*, chapter 15. IntechOpen, Rijeka, (2011).

[39] S. Park, Y. H. Lee, J.-S. Wi, and J. Oh, *A Semitransparent and Flexible Single Crystal Si Thin Film: Silicon on Nothing (SON) Revisited*, ACS Applied Materials Interfaces **8**, 18962–18968 (2016).

[40] A. Stranz, J. Kähler, A. Waag, and E. Peiner, *Thermoelectric Properties of High-Doped Silicon from Room Temperature to 900 K*, Journal of Electronic Materials **42**, 2381–2387 (2013).

[41] M. Zebarjadi, *Electronic cooling using thermoelectric devices*, Applied Physics Letters **106**, 203506 (2015).

[42] M. J. Adams, M. Verosky, M. Zebarjadi, and J. P. Heremans, *Active Peltier Coolers Based on Correlated and Magnon-Drag Metals*, Physical Review Applied **11**, 54008 (2019).

[43] J. Tang, H.-T. Wang, D. H. Lee, M. Fardy, Z. Huo, T. P. Russell, and P. Yang, *Holey Silicon as an Efficient Thermoelectric Material*, Nano Letters **10**, 4279–4283 (2010).

[44] P. E. Hopkins, C. M. Reinke, M. F. Su, R. H. I. I. I. Olsson, E. A. Shaner, Z. C. Leseman, J. R. Serrano, L. M. Phinney, and I. El-Kady, *Reduction in the Thermal Conductivity of Single Crystalline Silicon by Phononic Crystal Patterning*, Nano Letters **11**, 107–112 (2011).

[45] J. Lim, H.-T. Wang, J. Tang, S. C. Andrews, H. So, J. Lee, D. H. Lee, T. P. Russell, and P. Yang, *Simultaneous Thermoelectric Property Measurement and Incoherent Phonon Transport in Holey Silicon*, ACS Nano **10**, 124–132 (2016).

[46] M. Nomura, R. Anufriev, Z. Zhang, J. Maire, Y. Guo, R. Yanagisawa, and S. Volz, *Review of thermal transport in phononic crystals*, Materials Today Physics **22**, 100613 (2022).

[47] N. Liu, T. Zhu, M. G. Rosul, J. Peters, J. E. Bowers, and M. Zebarjadi, *Thermoelectric properties of holey silicon at elevated temperatures*, Materials Today Physics **14**, 100224 (2020).

[48] M. Nomura, Y. Kage, D. Müller, D. Moser, and O. Paul, *Electrical and thermal properties of polycrystalline Si thin films with phononic crystal nanopatterning for thermoelectric applications*, Applied Physics Letters **106**, 223106 (2015).

[49] J. Maire, E. Chávez-Ángel, G. Arregui, M. F. Colombano, N. E. Capuj, A. Griol, A. Martínez, D. Navarro-Urrios, J. Ahopelto, and C. M. Sotomayor-Torres, *Thermal Properties of Nanocrystalline Silicon Nanobeams*, Advanced Functional Materials **32**, 2105767 (2022).

[50] N. W. Ashcroft and N. D. Mermin, *Solid State Physics*, Saunders College Publishing (1976).

[51] G. Fiori, F. Bonaccorso, G. Iannaccone, T. Palacios, D. Neumaier, A. Seabaugh, S. K. Banerjee, and L. Colombo, *Electronics based on two-dimensional materials*, Nature Nanotechnology **9**, 768–779 (2014).

[52] M. Bernardi, C. Ataca, M. Palummo, and J. C. Grossman, *Optical and Electronic Properties of Two-Dimensional Layered Materials*, **6**, 479–493 (2017).

[53] M. H. Kalantari and X. Zhang, *Thermal Transport in 2D Materials*, Nanomaterials **13** (2023).

[54] X. Xi, L. Zhao, Z. Wang, H. Berger, L. Forró, J. Shan, and K. F. Mak, *Strongly enhanced charge-density-wave order in monolayer NbSe2*, Nature Nanotechnology **10**, 765–769 (2015).

[55] X. Xi, Z. Wang, W. Zhao, J.-H. Park, K. T. Law, H. Berger, L. Forró, J. Shan, and K. F. Mak, *Ising pairing in superconducting NbSe2 atomic layers*, Nature Physics **12**, 139–143 (2016).

[56] M. M. Ugeda, A. J. Bradley, Y. Zhang, S. Onishi, Y. Chen, W. Ruan, C. Ojeda-Aristizabal, H. Ryu, M. T. Edmonds, H.-Z. Tsai, A. Riss, S.-K. Mo, D. Lee, A. Zettl, Z. Hussain, Z.-X. Shen, and M. F. Crommie, *Characterization of collective ground states in single-layer NbSe2*, Nature Physics **12**, 92–97 (2016).

[57] U. Chatterjee, J. Zhao, M. Iavarone, R. Di Capua, J. P. Castellan, G. Karapetrov, C. D. Malliakas, M. G. Kanatzidis, H. Claus, J. P. C. Ruff, F. Weber, J. van Wezel, J. C. Campuzano, R. Osborn, M. Randeria, N. Trivedi, M. R. Norman, and S. Rosenkranz, *Emergence of coherence in the charge-density wave state of 2H-NbSe2*, Nature Communications **6**, 6313 (2015).

[58] J. Á. Silva-Guillén, P. Ordejón, F. Guinea, and E. Canadell, *Electronic structure of 2H-NbSe2 single-layers in the CDW state*, 2D Materials **3**, 35028 (2016).

[59] L. B. Lei, C. Zhang, A. B. Yu, Y. F. Wu, W. Peng, H. Xiao, S. Qiao, and T. Hu, *The transport properties of ultrathin 2H–NbSe2*, Superconductor Science and Technology **34**, 25019 (2021).

[60] A. Hamill, B. Heischmidt, E. Sohn, D. Shaffer, K.-T. Tsai, X. Zhang, X. Xi, A. Suslov, H. Berger, L. Forró, F. J. Burnell, J. Shan, K. F. Mak, R. M. Fernandes, K. Wang, and V. S. Pribiag, *Two-fold symmetric superconductivity in few-layer NbSe2*, Nature Physics **17**, 949–954 (2021).

[61] E. Zhang, X. Xu, Y.-C. Zou, L. Ai, X. Dong, C. Huang, P. Leng, S. Liu, Y. Zhang, Z. Jia, X. Peng, M. Zhao, Y. Yang, Z. Li, H. Guo, S. J. Haigh, N. Nagaosa, J. Shen, and F. Xiu, *Nonreciprocal superconducting NbSe2 antenna*, Nature Communications **11**, 5634 (2020).

[62] J. Y. Oh, J. H. Lee, S. W. Han, S. S. Chae, E. J. Bae, Y. H. Kang, W. J. Choi, S. Y. Cho, J.-O. Lee, H. K. Baik, and T. I. Lee, *Chemically exfoliated transition metal dichalcogenide nanosheet-based wearable thermoelectric generators*, Energy Environ. Sci. **9**, 1696–1705 (2016).

[63] H. Park, J. Y. Kim, J. Y. Oh, and T. I. Lee, *Long-term stable NbSe2 nanosheet aqueous ink for printable electronics*, Applied Surface Science **504**, 144342 (2020).

[64] V. I. Beletskii, O. A. Gavrenko, B. A. Merisov, M. A. Obolenskii, A. V. Sologubenko, G. Y. Khadjai, and K. B. Chashka, *Thermal conductivity and electrical resistivity of the layered compound Nb1-xSnxSe2*, Low Temperature Physics **24**, 273–277 (1998).

[65] I. Jo, M. T. Pettes, E. Ou, W. Wu, and L. Shi, *Basal-plane thermal conductivity of few-layer molybdenum disulfide*, Applied Physics Letters **104**, 201902 (2014).

[66] H.-H. Lien. *THERMAL CONDUCTIVITY OF THIN FILM NIOBIUM DISELENIDE FROM TEMPERATURE-DEPENDENT RAMAN*. PhD thesis, Cornell University, (2017).

[67] C. Ruppert, B. Aslan, and T. F. Heinz, *Optical Properties and Band Gap of Single- and Few-Layer MoTe2 Crystals*, Nano Letters **14**, 6231–6236 (2014).

[68] I. G. Lezama, A. Arora, A. Ubaldini, C. Barreteau, E. Giannini, M. Potemski, and A. F. Morpurgo, *Indirect-to-Direct Band Gap Crossover in Few-Layer MoTe2*, Nano Letters **15**, 2336–2342 (2015).

[69] Y. Yang, X. Zhu, K. Zhang, H. Zhu, L. Chen, and Q. Sun, *Observation of different transport behaviors in a two-dimensional MoTe2 field-effect transistor with engineered gate stack*, Microelectronic Engineering **237**, 111497 (2021).

[70] C. Gong, Y. Zhang, W. Chen, J. Chu, T. Lei, J. Pu, L. Dai, C. Wu, Y. Cheng, T. Zhai, L. Li, and J. Xiong, *Electronic and Optoelectronic Applications Based on 2D Novel Anisotropic Transition Metal Dichalcogenides*, Advanced Science **4**, 1700231 (2017).

[71] Y.-F. Lin, Y. Xu, S.-T. Wang, S.-L. Li, M. Yamamoto, A. Aparecido-Ferreira, W. Li, H. Sun, S. Nakaharai, W.-B. Jian, K. Ueno, and K. Tsukagoshi, *Ambipolar MoTe2 Transistors and Their Applications in Logic Circuits*, Advanced Materials **26**, 3263–3269 (2014).

[72] Y. M. Chang, C. Y. Lin, Y. F. Lin, and K. Tsukagoshi, *Two-dimensional MoTe2 materials: From synthesis, identification, and charge transport to electronics applications*, Japanese Journal of Applied Physics **55**, 1102A1 (2016).

[73] Y.-Q. Bie, G. Grosso, M. Heuck, M. M. Furchi, Y. Cao, J. Zheng, D. Bunandar, E. Navarro-Moratalla, L. Zhou, D. K. Efetov, T. Taniguchi, K. Watanabe, J. Kong, D. Englund, and P. Jarillo-Herrero, *A MoTe2-based light-emitting diode and photodetector for silicon photonic integrated circuits*, Nature Nanotechnology **12**, 1124–1129 (2017).

[74] A. Conan, D. Delaunay, A. Bonnet, A. G. Moustafa, and M. Spiesser, *Temperature dependence of the electrical conductivity and thermoelectric power in MoTe2 single crystals*, physica status solidi (b) **94**, 279–286 (1979).

[75] D. Shi, G. Wang, C. Li, X. Shen, and Q. Nie, *Preparation and thermoelectric properties of MoTe2 thin films by magnetron co-sputtering*, Vacuum **138**, 101–104 (2017).

[76] X.-J. Yan, Y.-Y. Lv, L. Li, X. Li, S.-H. Yao, Y.-B. Chen, X.-P. Liu, H. Lu, M.-H. Lu, and Y.-F. Chen, *Investigation on the phase-transition-induced hysteresis in the thermal transport along the c-axis of MoTe2*, npj Quantum Materials **2**, 31 (2017).

[77] A. Shafique and Y.-H. Shin, *Strain engineering of phonon thermal transport properties in monolayer 2H-MoTe2*, Physical Chemistry Chemical Physics **19**, 32072–32078 (2017).

[78] H. Li, T. Pandey, Y. Jiang, X. Gu, L. Lindsay, and Y. K. Koh, *Origins of heat transport anisotropy in MoTe2 and other bulk van der Waals materials*, Materials Today Physics **37**, 101196 (2023).

[79] C. Rodriguez-Fernandez, A. Nieminen, F. Ahmed, J. Pietila, H. Lipsanen, and H. Caglayan, *Unraveling Thermal Transport Properties of MoTe2 Thin Films Using the Optothermal Raman Technique*, ACS Applied Materials Interfaces **15**, 35692–35700 (2023).

[80] C. Kittel, *Introduction to Solid State Physics*, Wiley, 8th edition (2005).

[81] Y. Wang, L. Li, W. Yao, S. Song, J. T. Sun, J. Pan, X. Ren, C. Li, E. Okunishi, Y.-Q. Wang, E. Wang, Y. Shao, Y. Y. Zhang, H.-t. Yang, E. F. Schwier, H. Iwasawa, K. Shimada, M. Taniguchi, Z. Cheng, S. Zhou, S. Du, S. J. Pennycook, S. T. Pantelides, and H.-J. Gao, *Monolayer PtSe2, a New Semiconducting Transition-Metal-Dichalcogenide, Epitaxially Grown by Direct Selenization of Pt*, Nano Letters **15**, 4013–4018 (2015).

[82] R. A. B. Villaos, C. P. Crisostomo, Z.-Q. Huang, S.-M. Huang, A. A. B. Padama, M. A. Albao, H. Lin, and F.-C. Chuang, *Thickness dependent electronic properties of Pt dichalcogenides*, npj 2D Materials and Applications **3**, 2 (2019).

[83] J. Heremans and C. M. Thrush, *Thermoelectric power of bismuth nanowires*, Physical Review B **59**, 12579–12583 (1999).

[84] H. Usui, K. Kuroki, S. Nakano, K. Kudo, and M. Nohara, *Pudding-Mold-Type Band as an Origin of the Large Seebeck Coefficient Coexisting with Metallic Conductivity in Carrier-Doped FeAs2 and PtSe2*, Journal of Electronic Materials **43**, 1656–1661 (2014).

[85] T.-Y. Su, T.-H. Wang, D. P. Wong, Y.-C. Wang, A. Huang, Y.-C. Sheng, S.-Y. Tang, T.-C. Chou, T.-L. Chou, H.-T. Jeng, L.-C. Chen, K.-H. Chen, and Y.-L. Chueh, *Thermally Strain-Induced Band Gap Opening on Platinum Diselenide-Layered Films: A Promising Two-Dimensional Material with Excellent Thermoelectric Performance*, Chemistry of Materials **33**, 3490–3498 (2021).

[86] W. Y. Lee, M. S. Kang, G. S. Kim, J. W. Choi, N. W. Park, Y. Sim, Y. H. Kim,

M. J. Seong, Y. G. Yoon, E. Saitoh, and S. K. Lee, *Interface-Induced Seebeck Effect in PtSe2/PtSe2 van der Waals Homostructures*, ACS nano **16**, 3404–3416 (2022).

[87] D. Hsieh, D. Qian, L. Wray, Y. Xia, Y. S. Hor, R. J. Cava, and M. Z. Hasan, *A topological dirac insulator in a quantum spin Hall Phase*, Nature **452**, 970–974 (2008).

[88] L. Fu and C. L. Kane, *Topological insulators with inversion symmetry*, Phys. Rev. B **76**, 045302 (2007).

[89] W. Tian, W. Yu, J. Shi, and Y. Wang, *The Property, Preparation and Application of Topological Insulators: A Review*, Materials **10** (2017).

[90] H. Beidenkopf, P. Roushan, J. Seo, L. Gorman, I. Drozdov, Y. S. Hor, R. J. Cava, and A. Yazdani, *Spatial Fluctuations of Helical Dirac Fermions on the Surface of Topological Insulators*, Nature Physics **7**, 939–943 (2011).

[91] P. Bonderson, C. Nayak, and X.-L. Qi, *A Time-Reversal Invariant Topological Phase at the Surface of a 3D Topological Insulator*, Journal of Statistical Mechanics: Theory and Experiment **2013**, P09016 (2013).

[92] Y. Xu and J. Zhu, *Topological insulators for thermoelectrics*, npj Quantum Materials **2**, 51 (2017).

[93] J. J. Cha, K. J. Koski, and Y. Cui, *Topological insulator nanostructures*, Physica Status Solidi (RRL) – Rapid Research Letters **7**, 15–25 (2013).

[94] O. A. Tretiakov, A. Abanov, and J. Sinova, *Appl. Phys. Lett.*, Applied Physics Letters **99**, 113110 (2011).

[95] E. S. Walker, S. Muschinske, C. J. Brennan, S. R. Na, T. Trivedi, S. D. March, Y. Sun, T. Yang, A. Yau, D. Jung, A. F. Briggs, E. M. Krivoy, M. L. Lee, K. M. Liechti, E. T. Yu, D. Akinwande, and S. R. Bank, *Composition-dependent structural transition in epitaxial $Bi_{1-x}Sb_x$ thin films on Si(111)*, Physical Review Materials **3**, 064201 (2019).

[96] S. Gao, J. Gaskins, X. Hu, et al., *Enhanced Figure of Merit in Bismuth-Antimony Fine-Grained Alloys at Cryogenic Temperatures*, Scientific Reports **9**, 14892 (2019).

[97] M. P. Siegal, A. L. Lima-Sharma, P. A. Sharma, and C. Rochford, *Correlating thermoelectric properties with microstructure in $Bi_{0.8}Sb_{0.2}$ thin films*, Applied Physics Letters **110**, 141905 (2017).

[98] Y. Ueda, N. H. D. Khang, K. Yao, and P. N. Hai, *Epitaxial growth and characterization of $Bi_{1-x}Sb_x$ spin Hall thin films on GaAs(111)A substrates*, Applied Physics Letters **110**, 062401 (2017).

[99] A. Ibrahim and D. Thompson, *Thermoelectric properties of BiSb alloys*, Materials Chemistry and Physics **12**, 29–36 (1985).

[100] D. Sadek. *Integration of the BiSb topological insulator on industrial substrate: from structural to electrical characterizations*. Ph.d. thesis, Université Paul Sabatier - Toulouse III, (2022).

[101] E. Güneş, B. Landschreiber, G. Homm, et al., *Structure and Thermoelectric Properties of Nanostructured $Bi_{1-x}Sb_x$ Alloys Synthesized by Mechanical Alloying*, Journal of Electronic Materials **47**, 6007–6015 (2018).

[102] S. Gates-Rector and T. Blanton, *The Powder Diffraction File: a quality materials characterization database*, Powder Diffraction **34**, 352–360 (2019).

[103] H. Yadav, *Relation between the thermal activation energy of conduction and the first excited singlet state energy—a case of photo-conducting organic materials*, Thin Solid Films **477**, 222–226 (2005).

[104] N. F. Mott and E. A. Davis, *Electronic processes in non-crystalline materials*, Oxford University Press, Oxford (2012).

[105] A. Jain, S. P. Ong, G. Hautier, W. Chen, W. D. Richards, S. Dacek, S. Cholia, D. Gunter, D. Skinner, G. Ceder, and K. A. Persson, *Commentary: The materials project: A materials genome approach to accelerating materials innovation*, APL Materials **1**, 011002 (2013).

[106] K. Ueda, Y. Hadate, K. Suzuki, and H. Asano, *Fabrication of high-quality epitaxial $Bi_{1-x}Sb_x$ films by two-step growth using molecular beam epitaxy*, Thin Solid Films **713**, 138361 (2020).

[107] J. C. Y. Teo, L. Fu, and C. L. Kane, *Surface states and topological invariants in three-dimensional topological insulators: Application to $Bi_{1-x}Sb_x$*, Physical Review B **78**, 045426 (2008).

[108] P. Fan, W. fang Fan, Z. hao Zheng, Y. Zhang, J. ting Luo, G. Liang, and D. ping Zhang, *Thermoelectric properties of zinc antimonide thin film deposited on flexible polyimide substrate by RF magnetron sputtering*, Journal of Materials Science: Materials in Electronics **25**, 5060–5065 (2014).

[109] F. Völklein and E. Kessler, *Thermal Conductivity and Thermoelectric Figure of Merit of $Bi_{1-x}Sb_x$ Films With $0 < x \leq 0.3$*, physica status solidi (b) **143**, 121–130 (1987).

[110] Z. hao Zheng, F. Li, J. ting Luo, G. xing Liang, H. li Ma, X. hua Zhang, and P. Fan, *Enhancement of power factor in zinc antimonide thermoelectric thin film doped with titanium*, Materials Letters **209**, 455–458 (2017).

[111] G. J. Snyder, M. Christensen, E. Nishibori, T. Caillat, and B. B. Iversen, *Disordered zinc in Zn_4Sb_3 with phonon-glass and electron-crystal thermoelectric properties*, Nature Materials **3**, 458–463 (2004).

[112] Z. hao Zheng, P. Fan, J. ting Luo, and G. xing Liang, *Enhanced thermoelectric properties of In-doped ZnSb thin film with surface nanocrystallization*, Journal of Electronic Materials **46**, 1319–1323 (2017).

[113] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, *Electric field in atomically thin carbon films*, Science **306**, 666–669 (2004).

[114] Y. Cai, M. Faizan, H. Mu, Y. Zhang, H. Zou, H. J. Zhao, Y. Fu, and L. Zhang, *Anisotropic phonon thermal transport in two-dimensional layered materials*, Frontiers of Physics **18**, 43303 (2023).

[115] W. Feng, W. Zheng, W. Cao, P. Hu, W. Feng, W. Zheng, P. A. Hu, W. W. Cao, and H. W. W Cao, *Back Gated Multilayer InSe Transistors with Enhanced Carrier Mobilities via the Suppression of Carrier Scattering from a Dielectric Interface*, (2014).

[116] S. Sucharitakul, N. J. Goble, U. R. Kumar, R. Sankar, Z. A. Bogorad, F.-C. Chou, Y.-T. Chen, and X. P. A. Gao, *Intrinsic Electron Mobility Exceeding 103 cm2/(V s) in Multilayer InSe FETs*, Nano Letters **15**, 3815–3819 (2015).

[117] G. W. Mudd, S. A. Svatek, T. Ren, A. Patanè, O. Makarovsky, L. Eaves, P. H. Beton, Z. D. Kovalyuk, G. V. Lashkarev, Z. R. Kudrynskyi, A. I. Dmitriev G W Mudd, S. A. Svatek, T. H. Ren, A. Patanè, O. Makarovsky, L. Eaves, P. H. Beton, Z. D. Kovalyuk, G. V. Lashkarev, Z. R. Kudrynskyi, and A. I. Dmitriev, *Tuning the Bandgap of Exfoliated InSe Nanosheets by Quantum Confi nement*, Adv. Mater **25**, 5714–5718 (2013).

[118] J. Kang, S. A. Wells, V. K. Sangwan, D. Lam, X. Liu, J. Luxa, Z. Sofer, M. C. Hersam, J. Kang, S. A. Wells, V. K. Sangwan, D. Lam, M. C. Hersam, X. Liu, J. Luxa, and Z. Sofer, *Solution-Based Processing of Optoelectronically Active Indium Selenide*, Advanced Materials **30**, 1802990 (2018).

[119] M. Alidoosti, D. N. Esfahani, and R. Asgari, *Charge density wave and superconducting phase in monolayer InSe*, Physical Review B **103**, 035411 (2021).

[120] G. D. Guseinov, A. I. Rasulov, E. M. Kerimova, and M. Z. Ismailov, *On Heat Conductivity of AIIIBVI-Type Semiconductors*, physica status solidi (b) **19**, K87–K90 (1967).

[121] S. M. Atakishiev, D. S. Abdinov, and G. A. Akhundov, *Heat Conductivity of Indium Selenide*, physica status solidi (b) **28**, K47–K50 (1968).

[122] D. Spitzer, *Lattice thermal conductivity of semiconductors: A chemical bond approach*, Journal of Physics and Chemistry of Solids **31**, 19–40 (1970).

[123] V. D. Botcha, M. Zhang, K. Li, H. Gu, Z. Huang, J. Cai, Y. Lu, W. Yu, and X. Liu, *High-K substrate effect on thermal properties of 2D InSe few layer*, Journal of Alloys and Compounds **735**, 594–599 (2018).

[124] K. Li, Y. Hong, Z. Li, and X. Liu, *Thermal property engineering of InSe layer by a thin Al2O3 stress liner*, Applied Physics Letters **113**, 21903 (2018).

[125] D. Buckley, Z. R. Kudrynskyi, N. Balakrishnan, T. Vincent, D. Mazumder, E. Castanon, Z. D. Kovalyuk, O. Kolosov, O. Kazakova, A. Tzalenchuk, and A. Patanè,

Anomalous Low Thermal Conductivity of Atomically Thin InSe Probed by Scanning Thermal Microscopy, Advanced Functional Materials **31**, 1–10 (2021).

[126] A. Chevy, A. Kuhn, and M.-S. Martin, *Large InSe monocrystals grown from a non-stoichiometric melt*, J. Cryst. Growth **38**, 118 (1977).

[127] J. Miao, C. Leblanc, J. Wang, Y. Gu, X. Liu, B. Song, H. Zhang, S. Krylyuk, W. Hu, A. V. Davydov, T. Back, N. Glavin, and D. Jariwala, *Heterojunction tunnel triodes based on two-dimensional metal selenide and three-dimensional silicon*, Nature Electronics **5**, 744 (2022).

[128] C. Patil, C. Dong, H. Wang, B. M. Nouri, S. Krylyuk, H. Zhang, A. V. Davydov, H. Dalir, and V. J. Sorger, *Self-driven highly responsive p-n junction InSe heterostructure near-infrared light detector*, Photonics Res. **10**, A97 (2022).

[129] N. A. Pike, R. Pachter, M. A. Altvater, C. E. Stevens, M. Klein, J. R. Hendrickson, H. Zhang, S. Krylyuk, A. V. Davydov, and N. R. Glavin, *Understanding the Origin and Implication of the Indirect-to-Direct Bandgap Transition in Multilayer InSe*, J. Phys. Chem. C **128**, 7957 (2024).

[130] A. Rai, V. K. Sangwan, J. T. Gish, M. C. Hersam, and D. G. Cahill, *Anisotropic thermal conductivity of layered indium selenide*, Applied Physics Letters **118** (2021).

[131] T. Pandey, D. S. Parker, and L. Lindsay, *Ab initio phonon thermal transport in monolayer InSe, GaSe, GaS, and alloys*, Nanotechnology **28**, 455706 (2017).

[132] J. Zeng, X. He, S.-J. Liang, E. Liu, Y. Sun, C. Pan, Y. Wang, T. Cao, X. Liu, C. Wang, L. Zhang, S. Yan, G. Su, Z. Wang, K. Watanabe, T. Taniguchi, D. J. Singh, L. Zhang, and F. Miao, *Experimental Identification of Critical Condition for Drastically Enhancing Thermoelectric Power Factor of Two-Dimensional Layered Materials*, Nano Letters **18**, 7538–7545 (2018).

[133] N. T. Hung, E. H. Hasdeo, A. R. T. Nugraha, M. S. Dresselhaus, and R. Saito, *Quantum Effects in the Thermoelectric Power Factor of Low-Dimensional Semiconductors*, Phys. Rev. Lett. **117**, 036602 (2016).

[134] N. T. Hung, A. R. Nugraha, and R. Saito, *Two-dimensional InSe as a potential thermoelectric material*, Applied Physics Letters **111** (2017).

[135] B. Zhang and et al., *Super deformability and thermoelectricity of bulk -InSe single crystals*, Chinese Physics B **30**, 078101 (2021).

[136] N. Jaziri, A. Boughamoura, J. Müller, B. Mezghani, F. Tounsi, and M. Ismail, *A comprehensive review of Thermoelectric Generators: Technologies and common applications*, Energy Reports **6**, 264–287 (2020).

[137] M. Haras and T. Skotnicki, *Thermoelectricity for IoT – A review*, Nano Energy **54**, 461–476 (2018).

[138] M. Zebarjadi, K. Esfarjani, M. S. Dresselhaus, Z. F. Ren, and G. Chen, *Perspectives on thermoelectrics: from fundamentals to device applications*, Energy Environmental Science **5**, 5147–5162 (2012).

[139] G. S. Nolas, J. Sharp, and H. J. Goldsmid, *Thermoelectrics : basic principles and new materials developments*, Science And Technology **45**, VIII, 292 S. (2001).

[140] D. Enescu and D. Enescu, *Thermoelectric Energy Harvesting: Basic Principles and Applications*, Green Energy Advances (2019).

[141] K. Yazawa and A. Shakouri, *Electrothermal energy conversion using electron gas volumetric change inside semiconductors*, Applied Physics Letters **109**, 3–7 (2016).

[142] K. Yazawa and A. Shakouri. *Non-Equilibrium Electron Gas Thermodynamic Cycle with Nano Features*. In *Proceedings of the 15th International Heat Transfer Conference*, pages 1–13, Connecticut, (2014). Begellhouse.

[143] M. Zebarjadi, A. Shakouri, and K. Esfarjani, *Thermoelectric transport perpendicular to thin-film heterostructures calculated using the Monte Carlo technique*, Physical Review B - Condensed Matter and Materials Physics **74**, 1–6 (2006).

[144] M. Zebarjadi, C. Bulutay, K. Esfarjani, and A. Shakouri, *View Online Export Citation CrossMark Monte Carlo simulation of electron transport in degenerate and inhomogeneous semiconductors* , (2007).

[145] *Physical properties of Gallium Arsenide (GaAs)*, (2018).

[146] H. Brooks and C. Herring. *Scattering by Ionized Impurities in Semiconductors*. In *Proceedings of the American Physical Society*, pages 879–887, (1951).