Highly Reconfigurable and High Sensitivity Wake-upReceivers with Aggressive Duty-Cycling Techniques

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Abstract

Ultra-low power sensor nodes are vital for large scale Internet-of-Things (IoT) sensing applications. A typical IoT sensor node may consist of a micro-controller, wireless transceivers, sensor interfaces, and a power-management unit. The continuous operation with high instantaneous power node components can quickly overwhelm the available energy sources, which limits the operational lifetime. Low activity factor IoT networks can adopt periodic duty-cycling to reduce the average node power consumption at the cost of latency. However, periodic duty-cycling can be inefficient if the node information is accessed in an infrequent event-driven manner. A wireless wake-up receiver with negligible power consumption was proposed as an optimal solution to improve the node lifetime by providing event-driven duty cycling capability instead of a local wake-up timer based approach.

The prior wake-up receiver work has largely investigated the envelope-detector first (ED-1st) topology. The sub-GHz operation can enable wide area networks due to the low path loss, even though the optimum operation requires a large antenna and reliance on off-chip components. The ED-1st topology at sub-GHz range demonstrated sub micro-watt dc-power beneficial for longer node lifetime, but the maximum sensitivity was limited near -81dBm. However, the industrial IoT applications spanning several kilo-meters scale networks, such as agriculture, farming, and forest monitoring, require sensitivities near -100dBm, which cannot be achieved by the ED-1st topology. As the frequency is scaled to multi-GHz range to benefit from a smaller antenna and high integration, the sensitivity of the ED-1st quickly diminishes due to the lack of available high-quality factor components. Moreover, the reconfigurability with respect to the sensitivity, dc-power, and latency, is highly impactful due to the diverse

application space of the IoT and numerous unforeseen post-deployment variations. However, the ED-1st does not readily lend to the reconfigurability aspect, and the inherent sensitivity limitation and frequency scaling difficulties call for alternate solutions.

Addressing above issues, this dissertation presents highly reconfigurable and high sensitivity wakeup receiver design techniques. The research in this dissertation explores two architectures, the tuned-RF (T-RF) and the uncertain-IF (U-IF) as alternate solutions beyond the ED-1st topology. Both the T-RF and U-IF require high power active components and requires duty-cycling to maintain low power. This dissertation explores the limitations of two asynchronous duty-cycling techniques, the bit-level duty cycling and packet-level duty cycling, to reduce the dc-power to sub-microwatt levels while maintaining desirably low latencies.

The bit-level duty cycling technique has been demonstrated with sub-GHz T-RF topology in three separate proof of concept CMOS prototypes and the trade-offs between the sensitivity, power, and latency are explored. This dissertation demonstrates that heterogenous integration of the T-RF with a noise limiting narrowband micro-electromechanical system (MEMS) based filter can boost the wake-up receiver sensitivity beyond -100dBm while maintaining sub-microwatt level power at hundreds of milli-seconds latencies. When the noise limiting filter is omitted, the T-RF suffers from a high dc-offset at the rectifier output due to the noise self-mixing effect. This work demonstrates that an envelope modulated signaling scheme capable of IF channelization can alleviate the dc-offset issues. An IF channelization method without the need of a complex multi-tone transmission is used to demonstrate the multi-channel operation in a nano-watt scale T-RF wakeup receiver.

The packet-level duty cycling technique has been investigated with a highly integrated U-IF wake-up receiver operating at the 2.4GHz ISM band. This work demonstrates that an integrated PLL based event-driven calibrated RF oscillator in a U-IF front-end can enable a sensitivity of -93.5dBm without external calibration. The work also demonstrates that in a low-activity factor network, the received signal strength-based within-packet duty cycling can be used achieve dc-power as low as 2μW at 100ms latency with a 540μW instantaneous power of the U-IF receiver. These contributions can enable 2.4GHz ISM band wake-up receiver solutions suitable for low-throughput event-driven IoT applications.

Overall, the prior wake-up receiver research has produced an abundance of literature but found limited commercial applications. This can be attributed to the fact that each IoT application requiring a dedicated wake-up receiver due to the unique user constraints. This

dissertation attempts to address the above issue by providing insightful guidelines on selecting the best possible wake-up receiver topology for a given set of application constraints. This is done by 1) relating various user specifications to the WuRX performance metrics, 2) identifying the various trade-offs associated with several popular WuRX topologies and duty-cycling schemes, and 3) selecting the topology closest to the requirements with the aid of a design space analysis of reported wake-up receiver performance. The method proposed in this dissertation can serve as a tool for IoT system planning with respect to selecting the optimum wake-up receiver topology.

This research was funded in part by Defense Advanced Research Projects Agency (DARPA) Near Zero Power RF and Sensor Operations (N-ZERO) program, National Science Foundation (NSF) ASSIST Center, and Viasat Virginia-Beach Program.

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have always challenged me to think deeper and more meaningfully into electronics as a passion rather than a profession. I would also like to thank Sherry Moody for her delicious meals and tolerating us nerding out.

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"Seek perfection of character, Be faithful, Endeavor, Respect others, Refrain from violent behavior."

to my heart.

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This work is dedicated to my parents.

Anjana Dissanayake.

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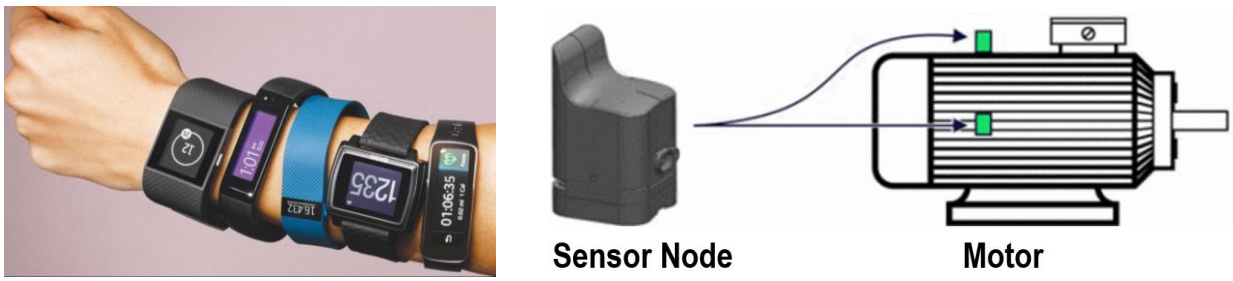
Chapter 1

1. Introduction

1.1 Background

Internet of things (IoT) refers to the concept of connecting sensor embedded physical objects into a network for the purpose of collecting, exchanging, and controlling of information over the internet [1]. The application space of IoT may spans from several interconnected sensors in an object for personal usage to thousands of connected nodes in an industrial setting. The personal healthcare monitoring wristbands that take measurements of heartbeat, breathing, and sleep-cycle (such as fitbit™) [2] are an example of a popular wearable IoT application (Fig. 1.1-a), while monitoring machine-health information to predict motor failure for the reduction of downtime [3] is an example of an industrial application (Fig. 1.1-b).

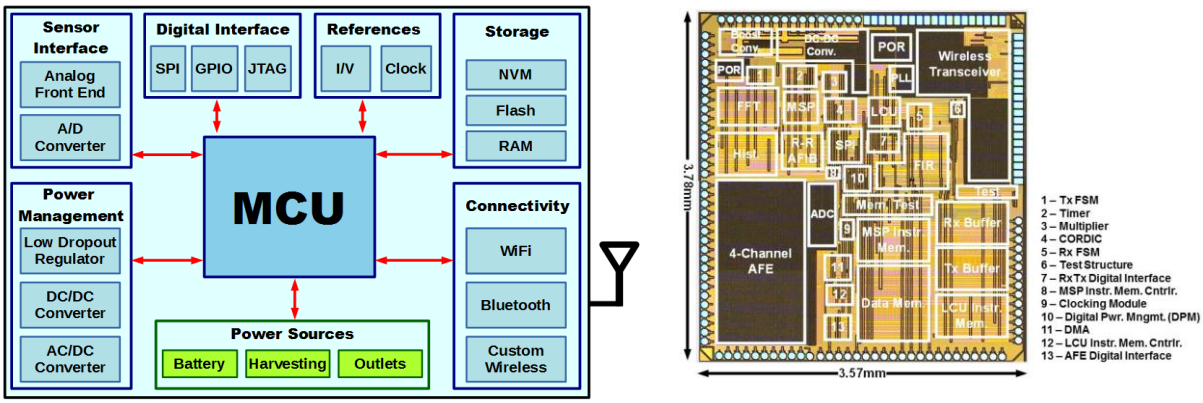


(a) Wearable Fitness Trackers[1] (b) Sensor nodes for Machine health monitoring[2]

Fig. 1.1. Examples of Internet of Things Applications; (a) personal; (b) industrial.

[1] Image credit: https://www.sundried.com/blogs/training/are-you-addicted-to-your-fitness-tracker
[2] Image credit: [3]

An IoT sensor node requires several hardware components for sensing the desired information, data processing, regulating proper operating conditions (ex: power supply), and maintaining network connectivity. Most of these functionalities can be realized with integrated-circuits (IC) as either a system-on-chip (SoC) or system-in-package (SiP), owing to the advancements of complementary metal-oxide semiconductor (CMOS) technology [4], which in turn enables robust mass-production. Fig. 1.2 shows a block diagram of an example SoC with associated hardware components which forms the 'soul' of an IoT sensor node and an actual CMOS implementation [5]. A high-level of monolithic integration can reduce the overall component cost of an IoT node by leveraging high yield large volume production. This is further aided by easy adoption of built-in self testing techniques (BIST) and desgin for testability (DFT) of integrated circuits compared with discrete implementations [6,7]. The contributions of this thesis are set in the above context of IC realization of an IoT sensor node.



(a) Block diagram of an IoT node IC

(b) CMOS implementation of an IoT SoC from [5]

Fig. 1.2. Example of an IoT system-on-chip; (a) Block level breakdown; (b) Actual CMOS implementation

Early predictions of the number of nodes associated with IoT were on the order of one trillion nodes by year 2015 [8], later revised to 50 billion nodes by year 2020 [9], and 25 billion nodes by year 2025 [10] by the industry experts and analysts. The negative speculation for the growth of IoT is a worthwhile consideration to understand what barriers exist. Three largest bottlenecks were named by [9] and they are:

1) Slow deployment of IPv6 and security features to support unique address to each new IoT device.

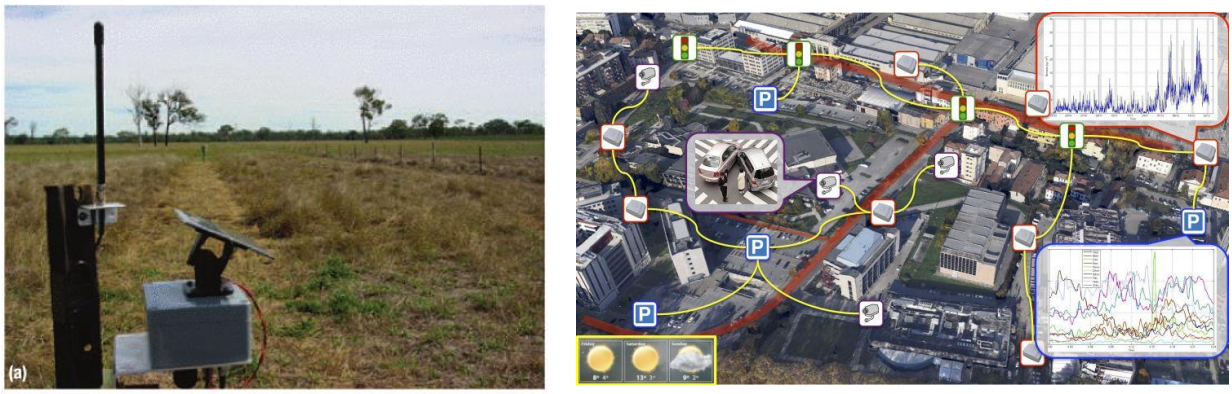
2) Lack of agreements and slow progress on new standards to support IoT related technology.

3) Sensor energy consumption.

The first two points relate to the development of network protocols and standardization agencies such as Institute of Electrical and Electronics Engineers (IEEE) and International Organization for Standardization (ISO), while the third point is directly related to the IoT node hardware power consumption and available energy resources.

For example, 50 billion IoT nodes worldwide, and assuming each node is powered by a battery with 1-year lifetime, would result in a large number of battery replacements per day given by A 137 million, which can cause a large overhead in IoT network maintenance and a huge environmental impact. This number becomes increasingly impractical if the number of devices reach towards 1 trillion nodes and with decreasing battery life [11].

Therefore, **it is imperative to produce device and system level solutions that consume less energy, which enables longer battery lives or ambient energy harvesting for mass deployment of IoT.**



(a) Agriculture: Soil moisture sensing [12] (b) Padova Smart-city project [14]

Fig. 1.3. Examples of low-activity factor industrial IoT applications.

Given the vast application space of IoT, unique features of certain application classes can be leveraged towards reducing the sensor energy consumption. One such feature is the amount of actual useful on-time of the sensor node. In the case of industrial IoT (iIoT) applications, the required sensor information may only be required only a few times per day while the sensor may spend most of the time in an idle state. Such networks are known as low activity factor networks. In the agricultural IoT application of [12], a combination of solar powered battery charging unit, a wireless transceiver, a microcontroller, and a set of integrated sensors, successfully harvested energy from sun-light and took soil moisture measurements typically at one-minute intervals (Fig. 1.3-a). A precision micro-climate control application for cattle farms demonstrated regulating the temperature-humidity index to improve the milk production with the aid of a misting fan and an exhaust fan with an event period of

approximately 4 minutes [13]. In the Padova smart-city project performed in collaboration with the city municipality of Padova, Italy, the sensors recorded 10 readings of temperature, humidity, and light, and 120 recordings of benzene over a one-hour window, which respectively yields activity intervals of 6 minutes and 30 seconds [14].

1.2 Wake-up Receiver as a Key Enabling Technology

The average power consumption of low-activity factor networks can be reduced by periodically turning the node off, also known as duty-cycling. The dc-power of a duty cycled component ($P_{DC,Avg}$) is given by:

$$P_{DC,Avg} = D \cdot P_{on} + (1 - D_{on}) \cdot P_{off} \quad (1)$$

$$D = \frac{T_{on}}{T_{per}} \quad (2)$$

where D is the duty-cycle of the device given by the ratio of on time T_{on} to duty-period T_{per}, the power of the device at on-state is P_{on}, the leakage power of the device at off-state is P_{off}.

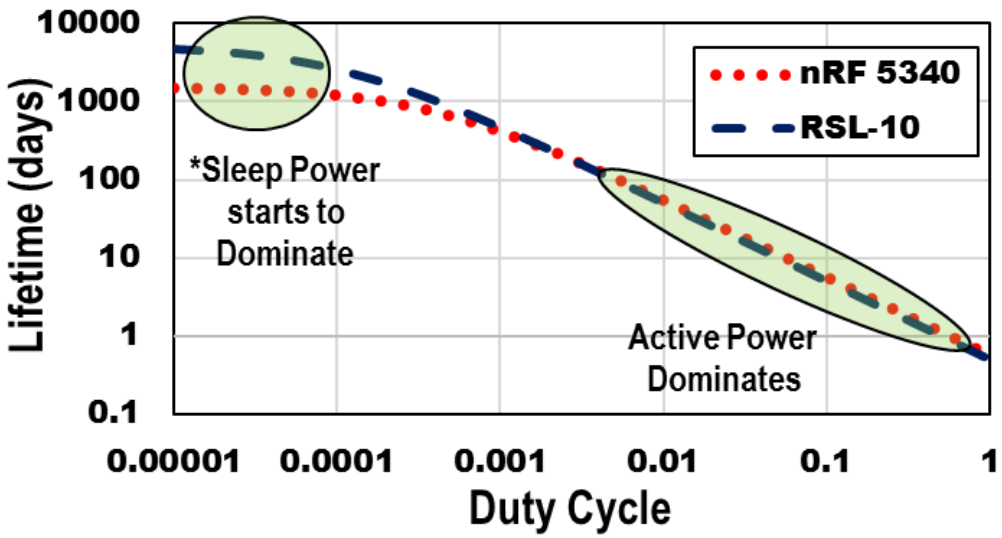


Fig. 1.4. Node lifetime as a function of duty-cycle with a commercially available components (nRF5340 and RSL-10 SoCs) and energy source (CR-1220 coin-cell battery).

An example operational node lifetime profile as a function of the duty-cycle for two commercially available low power SoCs including a micro controller, power management, and wireless transceiver unit is shown in Fig. 1.4 for nRF-5340 [15] and RSL-10 [16]. A CR-1220 coin-cell battery with 37mAh capacity is used as the energy source and zero self-discharge is assumed. Both SoCs drain the battery within approximately 13 hours at an always-on state

corresponding to a duty-cycle of 1. As the duty-cycle approaches smaller and smaller values the off power of each SoC starts to dominate and duty-cycling provides no further power benefits.

The behavior shown in Fig. 1.4 exemplifies two problems associated with conventional duty-cycling for low activity factor networks.

1. In the absence of high-capacity batteries and low active and leakage powers, the duty-cycle required to achieve years long life time can be prohibitively small and become impractical due to reasons such as finite turn-on time associated with hardware and low accuracy of duty cycling timers.

2. If the node activity rate is low but occurs infrequently or at random, then periodic duty-cycling is an inefficient method to reduce power.

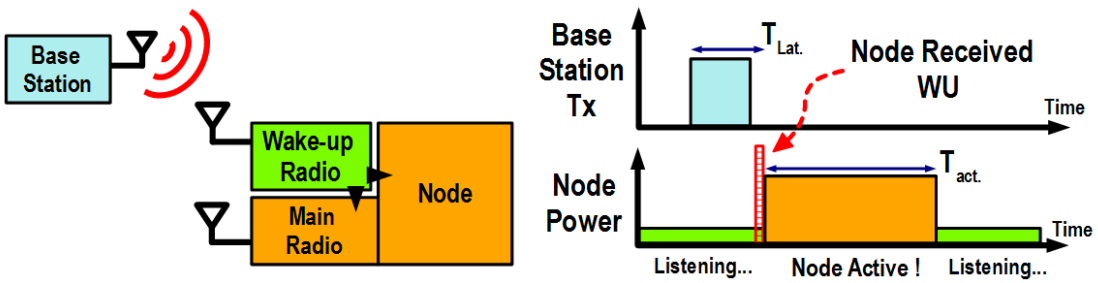


Fig. 1.5. Wake-up receiver operation; Received signal and node-power profile

The concept of an event-driven wake-up receiver (WuRX) was proposed as a solution addressing both of the above concerns and to efficiently manage the node power [17,18]. Shown in Fig. 1.5, a dedicated ultra-low power receiver is added to the IoT node, which constantly scans the wireless medium for a trigger command, while the rest of the node is in sleep state. The base-station transmits a wake-up signature to a desired node when the sensor information is required. After a finite latency given by $T_{Lat.}$, the node is powered up and operates as intended for a duration of T_{act} and reverts back to the sleep-state. The node power consumption with a wake-up receiver is given by:

$$P_{DC,Avg} = P_{WuRX} + AF \cdot \frac{T_{Act}}{3600} \cdot P_{on} + (1 - AF) \cdot P_{off} \qquad (3)$$

where P_{WuRX} is the power of the wake-up receiver and AF is the number of activities (sensing or processing event) per hour (aka activity factor). Assuming AF ≈ 0 for low activity networks, the node power is now dominated by the wake-up receiver power consumption and the leakage power.

The node lifetime is plotted in Fig. 1.6 as function of AF for the same battery example in Fig. 1.4 assuming the wake-up receiver current to be 1µA, event duration (T_{Act}) of 10ms, and an active event current of 5mA, and a leakage current of 100nA.

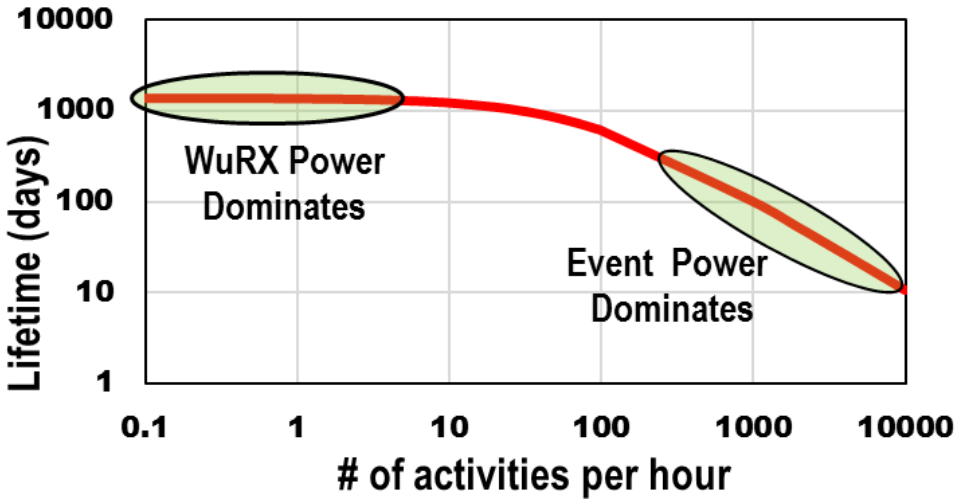


Fig. 1.6. Node power as a function of activity factor according to eq. (3). (WuRX current draw of 1µA, active time of 10ms, active event current draw of 5mA, and leakage of 100nA is used)

The results of the Fig. 1.6 show that for low activity factors of less than 1 per hour, a node-life time of approximately 3.3 years can be realized with the example wake-up receiver + leakage current and assuming no battery self-discharge, proving the usefulness of the concept. A much more optimistic current draw of 100nA for the wake-up receiver can extend the battery life to well beyond a decade (~20.5 years) with all other conditions being equal.

Given the potential impact of wake-up receiver as an enabling technology for solving the sensor energy problem in route to mass deployment of distributed sensor networks, this thesis presents **analyses and design techniques of sub-microwatt wake-up receiver s suitable for low activity factor and long-range industrial IoT applications.** Furthermore, given the highly application specific nature of IoT, where it is impractical to produce a generalized '*one-fits-all*' solution, this thesis provides **a constrain-driven design guide and insights which relate the user-needs to wake-up receiver metrics to select the best wake-up receiver topology satisfying the design trade-offs.**

1.3 Design Space analysis for Wake-up receivers

Before delving into prior-work and design space analysis, it is useful to clarify several major evaluation metrics used in this thesis for wake-up receivers.

- **Sensitivity:** Sensitivity is defined as the minimum required input radio-frequency (RF) signal power (available power) provided by a driving impedance (such as a 50-ohm antenna), which produces a certain bit-error ratio, packet-error ratio, missed-detection ratio or a wake-up error ratio (ex. 0.001 or 0.1%). Sensitivity is a metric of maximum communication distance.

- **Latency:** The latency is defined as the average time it takes the wake-up receiver to successfully detect and demodulate a wake-up packet starting from the beginning of the intended transmission. Latency can be extrapolated by the average bit-rate of the wake-up receiver and address length. Latency generally does not include any pair-up time delays associated with any other transceivers in the system.

- **Signal to interference ratio (SIR):** SIR is defined as the input power of unwanted (generally called interference) RF signals that causes 3dB degradation of signal to noise ratio (or equivalently sensitivity). SIR is commonly measured by injecting both the desired signal and interference signal (at a certain offset frequency) while setting the desired signal 3dB above the sensitivity level, and gradually increasing the interference power until the error-ratio corresponding to the sensitivity level is reached. This is a metric of the robustness where high SIR levels for various modulations indicate that the wake-up receiver may robustly operate in a crowded medium with strong and diverse background signals.

- **False alarm rate:** False alarm rate is defined as the number of wakeups that are issued in error for a given time period when there is no RF input signal present. Input signal in this case consists entirely of the thermal noise of the source impedance (antenna) and does not include the effect of any background signals that may exist in the same medium. False alarm rate constrains the minimum power consumption of a node.

A plethora of ultra-low power (ULP) receivers suitable for wake-up receiver applications have been reported since the inception of the concept. Fig. 1.7 to 1.9 illustrate two major performance metrics; sensitivity, and SIR against dc-power for the sub-10mW region of

the design space, based on the operating frequency for the reported ULP work during 2000-2020 [19] (The data does not include the contributions of this thesis to better emphasize the design space gaps). Fig. 1.7 shows the sensitivity versus dc-power while Fig. 1.8 shows the normalized sensitivity defined as:

$$Normalized\ Sensitivity_{ED} = Sensitivity - 5\log_{10}(Bit\ rate) \quad (1.4)$$

$$Normalized\ Sensitivity_{Het} = Sensitivity - 10\log_{10}(Bit\ rate) \quad (1.5)$$

where eq. (1.4) is used for the case of direct RF envelope detection and eq. (1.5) is used for heterodyne case [20] (*discussed in chapter 4*). The normalized sensitivity provides a better comparison of receivers since it remaps the sensitivity to the hypothetical case of 1-bps (or ~1Hz BW) while accounting for sensitivity scaling factors associated with various topologies and bit rates.

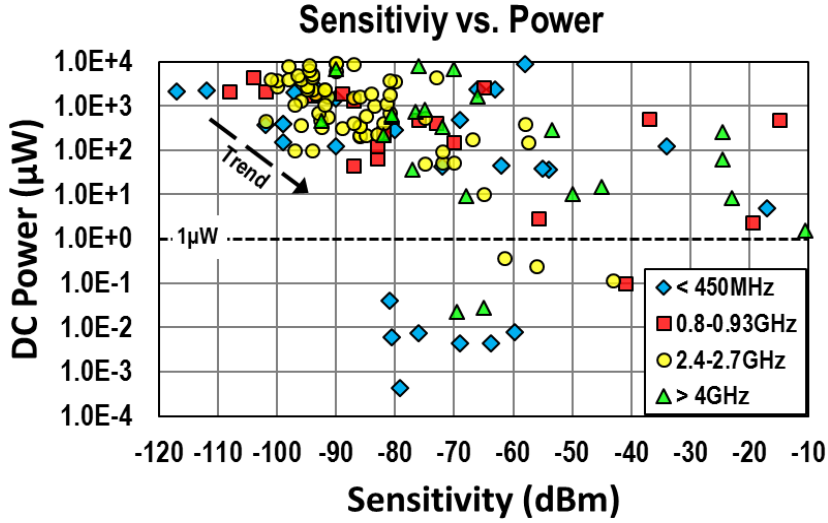


Fig. 1.7. Sensitivity vs. DC power for sub-10mW receivers (2000-2020).

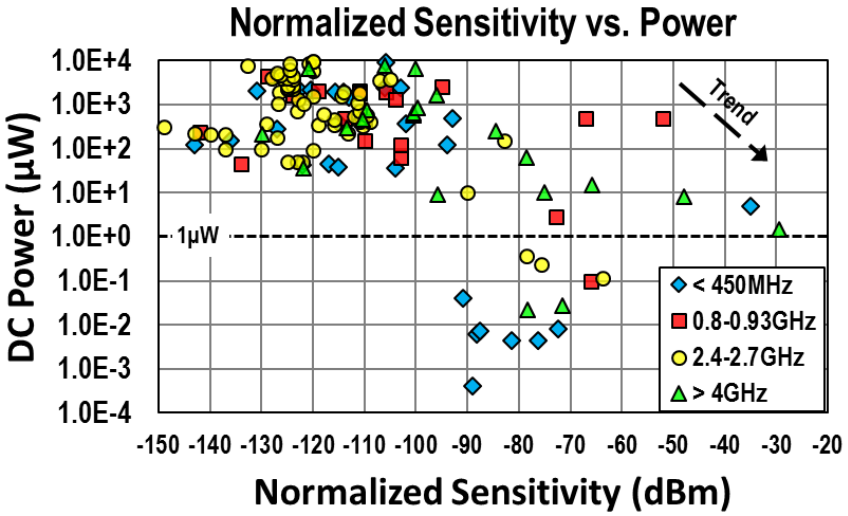


Fig. 1.8. Normalized Sensitivity vs. DC power for sub-10mW receivers (2000-2020). Normalized sensitivity is defined as: "Sensitivity-5log$_{10}$(bit-rate)" for the case of RF envelope detection and "Sensitivity-10log$_{10}$(bit-rate)" for other cases.

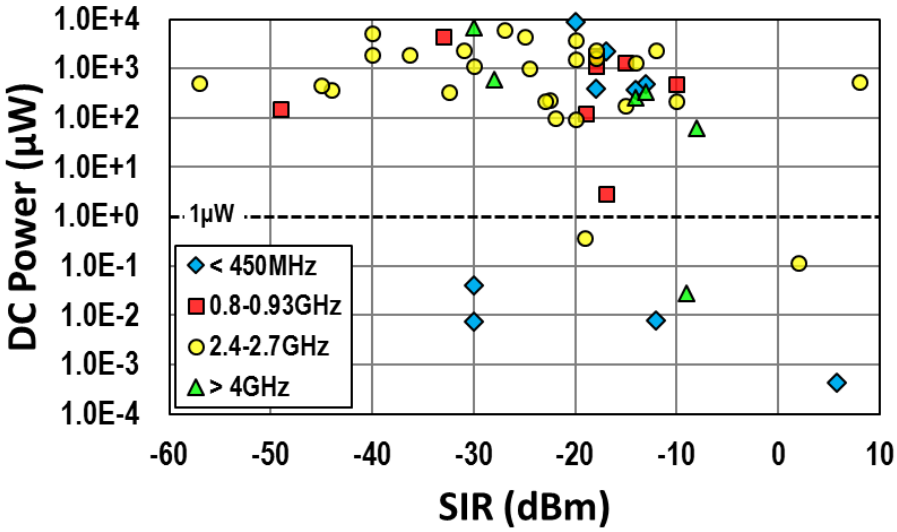


Fig. 1.9. Signal to Interference Ratio (SIR) vs. DC power for sub-10mW receivers (2000-2020). Not all receivers reported SIR hence it is difficult to discern a trend.

Both Fig. 1.7 and 1.8 show that a high sensitivity is generally associated with high instantaneous dc-power, a discouraging trend for wake-up receiver design for long range applications. This suggests that simultaneous high sensitivity and low-power operation either requires revolutionary new breakthroughs in architecture and technology or forces the designers to adopt duty-cycling techniques in the wake-up receiver design itself. However, this is a different scenario than duty-cycling the main transceiver, which is typically designed to provide high data-rates with complex modulation schemes, which in turn lead to high amount of active power. Hypothetically, a wake-up receiver does not need such complex demodulation schemes, hence a low instantaneous active power which allows for practical levels of duty cycling to reach sub-µW can be realized. One conclusion drawn here is that **wake-up should favor signaling schemes such as amplitude modulation to leverage low power non-coherent demodulation.**

Another important observation from Fig. 1.7 is that there exists a large gap in the region where sensitivity is better than -80dBm and power less than 1µW (almost up to <100µW). High sensitivity is extremely desirable for long-range operation since a large propagation path loss can then be tolerated. Path loss can be calculated using the well-known Friis path loss equation:

$$Path\ Loss(dB) = 10n\log(d) + 20\log(f) + 20\log\left(\frac{4\pi}{C}\right) - G_T - G_R \qquad (6)$$

where n is an empirical loss exponent, d is the distance, f is the carrier frequency, C is the speed of light, and G_T and G_R are transmitter and receiver gains, respectively. Assuming a -80dBm sensitivity and transmit power of 10dBm, table 1 summarizes the communication range for various values of n [21,22] for various frequency bands.

Table 1.1. Communication distance at various frequencies assuming -80dBm sensitivity and 10dBm TX power

	Loss Exponent (n)	Range w/ -80dBm Sensitivity and 10dBm TX power		
		434MHz	915MHz	2.4GHz
Free Space	2	1.7km	850m	320m
Urban	2.7	250m	150m	75m
Obstructed in Factories	3	150m	90m	45m
Obstructed in Building	5	20m	15m	10m

The results in table 1 indicate that in the absence of high-transmit powers (regulated by authorities of individual countries), sensitivities beyond -80dBm are required to cover a several kilo meters of range and low frequency operation is generally favorable. Hence, the first major design objective of this thesis is **to produce wake-up receiver solutions capable of achieving sensitivities near or better than -100dBm at sub-GHz range while still dissipating sub-µW level power to enable long range communications.**

Interestingly, table 1 also indicates that due to extremely high path loss, lower carrier frequencies do not provide as much of a benefit compared to the free space case. For example, the 434MHz operation provides more than 5x the range compared to 2.4GHz in free space, but only provides 2x benefit in the 'obstructed in building' case. Given that the antenna area is inversely proportional to the operating frequency [23], this means that a 434MHz antenna is considerably larger in area than a 2.4GHz one. This trade-off indicates that one may readily adopt **lower frequency operation for long range and large area applications** such as agricultural and wild-life monitoring where the node area is not a burden, while **area constrained in-door applications** such as factories and office environments **may benefit from high frequency operation** such as 2.4GHz band, leveraging small antenna area without a large degradation in communication range. Therefore, this thesis provides **wake-up receiver design methodology for achieving sensitivity better than -90dBm at 2.4GHz band while simultaneously realizing sub-µW operation**.

Although not every work listed in [19] reports the SIR metric, the plotted values in Fig. 1.9 show a clear lack of solutions below 100µW region indicating a potential bottleneck. Interference tolerance is vital for robust operation, especially in the context of trillion node IoT, since every sensor node becomes a potential interference source for other nodes. Since the

wake-up receiver is generally expected to operate in combination with a main data receiver, an argument could be made that the wake-up receiver should also demonstrate expected interference tolerance levels of the main receiver, although this argument may not hold for the case of low activity factor networks. However, even in a low activity factor network, interference tolerance is crucial for coexisting with other background networks such as cellular, WiFi, and Bluetooth, especially for indoor applications. Hence, **this thesis investigates methods for improving interference tolerance in the ultra-low power context.**

1.4 Prior Work in Low Power Receiver Design

The existing ultra-low power receiver solutions can be grouped into two main categories based on the position where the actual demodulation occurs in the signal chain. The bit detection can be done at the RF carrier frequency or in a baseband (BB) frequency after employing a frequency shifting operation commonly called down-conversion or heterodyning. Each category has several widely used topologies with merits and demerits warranting careful attention, hence this section briefly introduces several popular RX topologies suitable for wake-up receivers.

Popular receiver topologies that fall into the category of energy detection at RF are shown in Fig. 1.10. Not surprisingly, these topologies are much similar to the earliest reported work dating back to the first world war era [24], where receiver design was constrained by the availability of semiconductor components rather than dc-power.

Due to the omission of power-hungry RF gain circuitry, the envelope detector first (ED-1st) topology shown in Fig.10-(a) achieves the lowest instantaneous power consumption, hence has found immense popularity as candidate wake-up receiver topology in both industrial [25, 26] as well as academic [27-37] research. The envelope detector produces an output dc signal proportional to the RF signal's envelope, and can be realized entirely in passive (zero dc-bias current) implementation with modern CMOS technology.

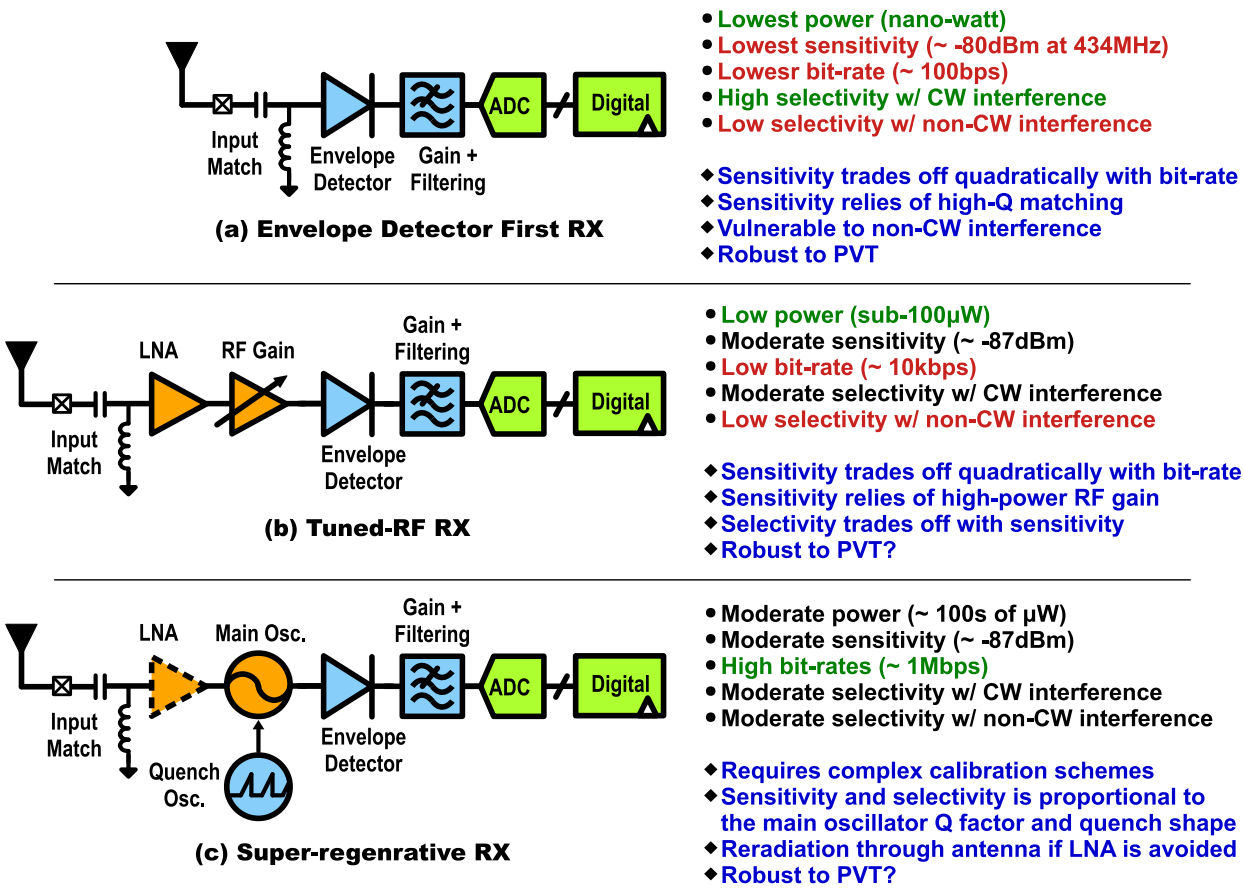


Fig. 1.10. Common receiver topologies employing direct RF detection w/ pros and cons and design considerations; (a) Envelope detector first, (b) Tuned-RF, (c) super-regenerative. PVT stands for process, variation and temperature variation.

The sensitivity of ED-1st RX demonstrates a quadratic relationship to the baseband bandwidth, which corresponds to the data-rate [30]. The sensitivity is improved by adopting a passive voltage-boosting type matching networks with high quality-factor (Q-factor) components prior to the detector. Data-rates of approximately 100s of bits per second, corresponding to latencies of hundreds of milli-seconds, have been demonstrated with the maximum sensitivity near -80dBm at sub-GHz frequency range. However, the sensitivity close to -100dBm suitable for long range applications (even at sub-GHz) has yet to be demonstrated, while scaling from -80dBm to such high sensitivity is not entirely trivial due to the quadratic trade-off between sensitivity and data-rate. However, even with the limited sensitivity, the ability to realize nano-watt level power is an attractive feature, and robust operation up to several GHz has been demonstrated [27, 28]. ED-1st topology can adopt baseband ac-coupling techniques, which can help with continuous-wave (CW) interference, while non-CW interference can affect the detection.

The limited sensitivity of the ED-1st topology can be improved by addition of a low-noise RF gain stage prior to the detector. Shown in Fig. 1.10-(b), this topology is known as tuned-RF (T-RF) architecture and may consume significant amounts of dc-power (several tens of micro-watts) in the active RF gain stages. Moderate sensitivities of about -87dBm have been demonstrated by several prototype wake-up receiver implementations, while maintaining low to moderate data rates of several kilobits per second [38-40]. Since the active gain can be realized at higher frequencies by dissipating more power, sensitivity can theoretically be maintained as the frequency is scaled. Since the detection is still performed at RF, the quadratic relationship between sensitivity and baseband data-rate similar to ED-1st case remains unchanged. The selectivity performance is affected by the amount of RF gain, where high gain can lead to compression due to interference even for CW signals.

The super-regenerative topology shown in Fig. 1.10-(c) adopts an RF oscillator (super-regenerative oscillator or SRO) that is periodically refreshed (turn on-and-off) by another time varying signal, which is generated by another low frequency oscillator called the quench oscillator. The injection of RF signal causes the oscillation in SRO to build up faster and the time domain waveform is rectified with an envelope detector, creating a signal dependent dc level at the out of the rectifier. High data rates of several megabits per second have been demonstrated with moderate sensitivities, while the power consumption can be several hundreds of micro-watts [41-45]. The robust operation requires calibration circuitry in the SRO and quench oscillator, while the sensitivity depends on the Q-factor of SRO and shape of the quench waveform. In the case where the pre-amplifier prior to SRO is avoided for low power, the reradiation of the SRO signal through the antenna interface can cause periodic background interference. Although desirably high data rates can be achieved, due to the required calibration efforts and vulnerability to PVT [43], this topology has yet to be explored in depth in the context of wake-up receivers.

The second main category of ultra-low power receivers employing the heterodyne principle is shown in Fig. 1.11. These receivers employ an RF oscillator similar to the case of super-regenerative architecture, but instead of directly injecting the RF signal to the oscillator, a down-conversion to a baseband frequency is performed by a device called a mixer. The mixer implements time-domain multiplication of RF signal and the local-oscillator (LO) signal, which down-converts the information to a frequency corresponding to the difference of RF and LO frequencies. Heterodyne receivers are arguably the most popular receiver topology due to the ease of selectivity and multi-channel communication capabilities.

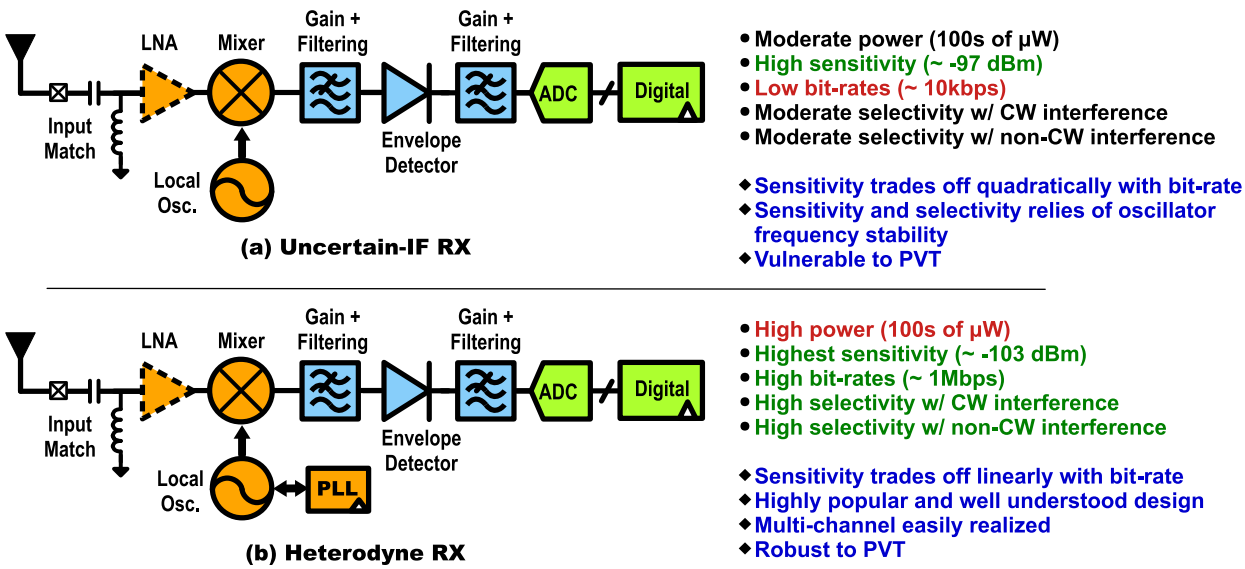


Fig. 1.11. Common receiver topologies employing heterodyne principal w/ pros and cons and design considerations; (a) Uncertain-IF RX, (b) Conventional Heterodyne RX

The uncertain-IF (U-IF) topology shown in Fig. 11-(a) adopts a free running oscillator to perform down-conversion, hence the exact down-converted intermediate frequency (IF) is uncertain [46, 50]. The uncertainty can be reduced by the addition of calibration techniques as well as adopting high-Q oscillator design methodologies. A high sensitivity closer to -100dBm has been demonstrated while maintaining moderate powers near 100s of micro-watts. The sensitivity of a U-IF receiver depends on the level of baseband filtering that can be allowed prior to envelope detector, and the sensitivity trades-off quadratically with bandwidth prior to ED and post ED similar to T-RF.

The conventional heterodyne topology shown in Fig. 11-(b) adopts a control unit called a phase-locked loop (PLL) or a frequency-locked loop (FLL) to perform accurate LO synthesis with the aid of a stable baseband reference frequency [51-62]. The heterodyne topology benefits from extremely accurate frequency selectivity and has demonstrated sensitivities surpassing -100dBm while power required to operate the PLL and LO contributes to several hundreds of micro-watts in addition to the power dissipated in active RF gain circuitry, while the total power can reach up to milli-watts. However, since high-Q filtering can easily be realized at baseband frequencies, this topology exhibits extremely high selectivity and interference tolerance, hence the popular choice for high through-put applications.

With the above overview of the popular low power receiver topologies, several observations and conclusions can be made regarding required further research. First, the ED-1st topology provides the lowest power, but a drastic sensitivity improvement beyond -100dBm

while maintaining reasonable latency is a challenging task requiring careful architectural changes to be adopted in the design. **The addition of low noise RF gain (T-RF and heterodyne topologies) can enable better sensitivity, but comes at the cost of high dc-power dissipation, which calls for efficient duty-cycling techniques at system and component level to realize sub-microwatt average power**.

1.5 Dissertation Contributions and Organization

1.5.1 Research Questions

The research for this thesis was conducted to answer the following research questions.

Research Question 1:

"What trade-offs are enabled by bit-level duty cycling and packet-level duty cycling for tuned-RF and heterodyne receiver architectures with respect to sensitivity, latency, dc power consumption, and interference tolerance?"

Research Question 2:

"What RF signaling methods can be leveraged to improve robustness and spectrum efficiency in the context of an energy-detection to enable baseband channelization?"

Research Question 3:

"What are the RF oscillator design considerations for aggressively duty-cycled energy detection down-conversion receivers, and how to improve the frequency stability of a duty-cycled RF oscillator without a dedicated power-hungry phase/frequency locking circuitry?"

Research Question 3:

"Given the highly application specific nature of IoT, what is the best wake-up receiver topology satisfying a given set of user-constraints?"

1.5.2 Thesis Statement

Industrial IoT applications can benefit from high sensitivity wake-up receivers with near or below microwatt level dc-power to address the sensor energy problem in low activity factor networks. The prior work in ED-1st topology achieved nano-watt level power but it is challenging to reach sensitivities beyond -90dBm without suffering a substantial latency penalty, which calls for alternate solutions.

This dissertation presents analysis and design techniques that demonstrate the feasibility of implementing aggressive duty-cycling to simultaneously enable near micro-watt average power, high sensitivity, scalability, interference tolerance, and low latency wake-up receivers employing tuned-RF and uncertain-IF topologies at sub-GHz and multi-GHz RF frequencies.

Various combinations of bit-level duty-cycling, packet level duty-cycling, sophisticated RF signaling, adoption of tuned-RF and uncertain-IF frontend, local-oscillator stabilization, statistics of wake-up receiver wireless channel activity, and careful circuit design has been employed to produce several proof-of-concept CMOS ICs to demonstrate the ultra-low power operation, which can enable prolonged lifetime for power constrained long range IoT networks.

1.5.3 Research Contributions

This dissertation presents design-oriented analysis and techniques for improving the sensitivity of wake-up receivers while maintaining low average dc-power and latency at sub-GHz and multi-GHz operation frequency.

The highlights of the thesis contributions are listed below:

1. Analysis of bit-level duty cycling and packet-level duty-cycling methods and associated dynamic range trade-offs on the sensitivity, dc-power, latency.
2. Analysis of dc-offset up-conversion and spectrum-regrowth issues of bit-level duty-cycling and propose mitigation methods.
3. Analysis of proposed channel-embedded on-off-keying (CE-OOK) signaling method for emulating a multi-tone signal to create IF content in a energy detection receivers such as ED-1st and T-RF.
4. Design techniques for improving RF oscillator stability by embedding an energy-efficient self-calibration technique to uncertain-IF architecture for reduce calibration overhead.
5. Design techniques for achieving sub-microwatt power wake-up receivers at 434MHz and 2.4GHz unlicensed frequency bands.
6. Design techniques for highly integrated heterodyne receiver front-ends at 2.4GHz frequency.

The research in this dissertation advances the state-of-art by:

1. Practical demonstration of sensitivity better than -100dBm with co-designed micro-electro mechanical system (MEMS) and CMOS wake-up receiver at nano-watt level power for the first time in literature.

2. Practical demonstration of sensitivity at -99dBm with a CMOS T-RF architecture at 434MHz frequency with sub-microwatt power.

3. Practical demonstration of high dynamic range of sensitivity, latency, and dc-power by adopting bit-level duty cycling in a T-RF receiver.

4. Practical demonstration of -91.5dBm sensitivity and -47.5dB interference tolerance with sub-microwatt dc-power at 1s latency, and 2μW dc-power at 100ms latency at 2.4GHz frequency band with a CMOS highly integrated U-IF wake-up receiver.

Fig. 1.12 shows a comparison of normalized sensitivity (*eq. (4)*) versus power of prior state-of-art including the contributions of this thesis. This work achieves a sensitivity better than -27dB with MEMS integration and -13 dB without MEMS integration over prior sub-GHz nano-watt wake-up receivers.

Fig. 1.13 shows a comparison of sensitivity versus power of prior state-of-art including the contributions of this thesis at 2.4GHz frequency. This work achieves a comparable sensitivity to prior state-of-art while drastically reducing the power consumption, especially at low latencies.

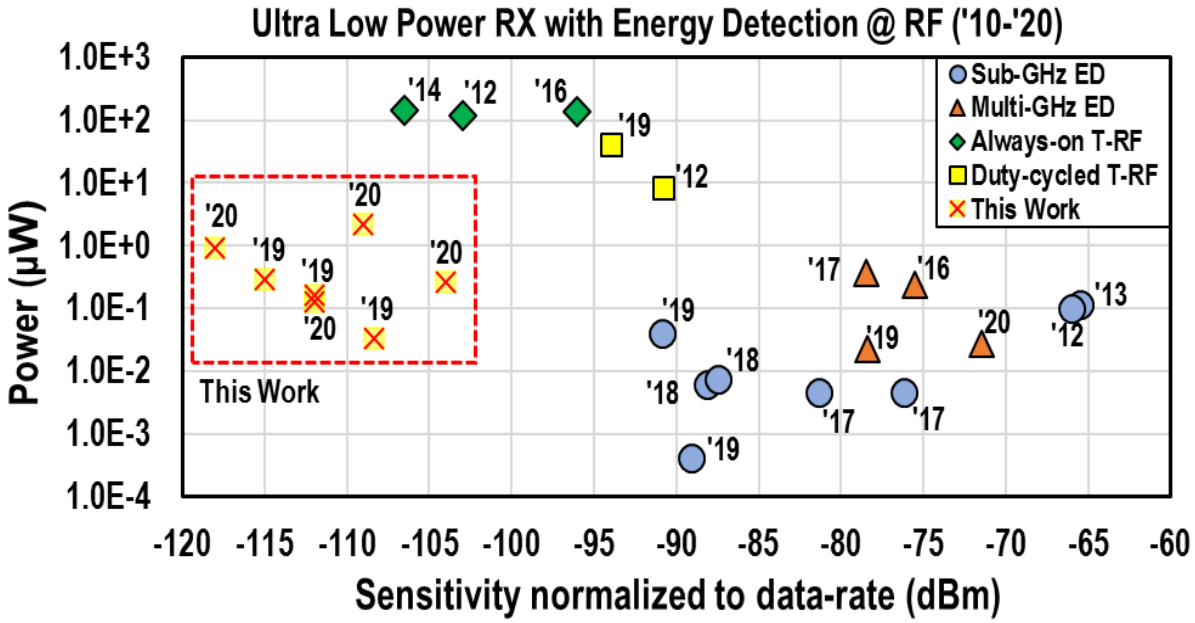


Fig. 1.12. Normalized sensitivity versus power of prior state-of-art including the contributions of this thesis at sub-GHz range. (T-RF are all sub-GHz)

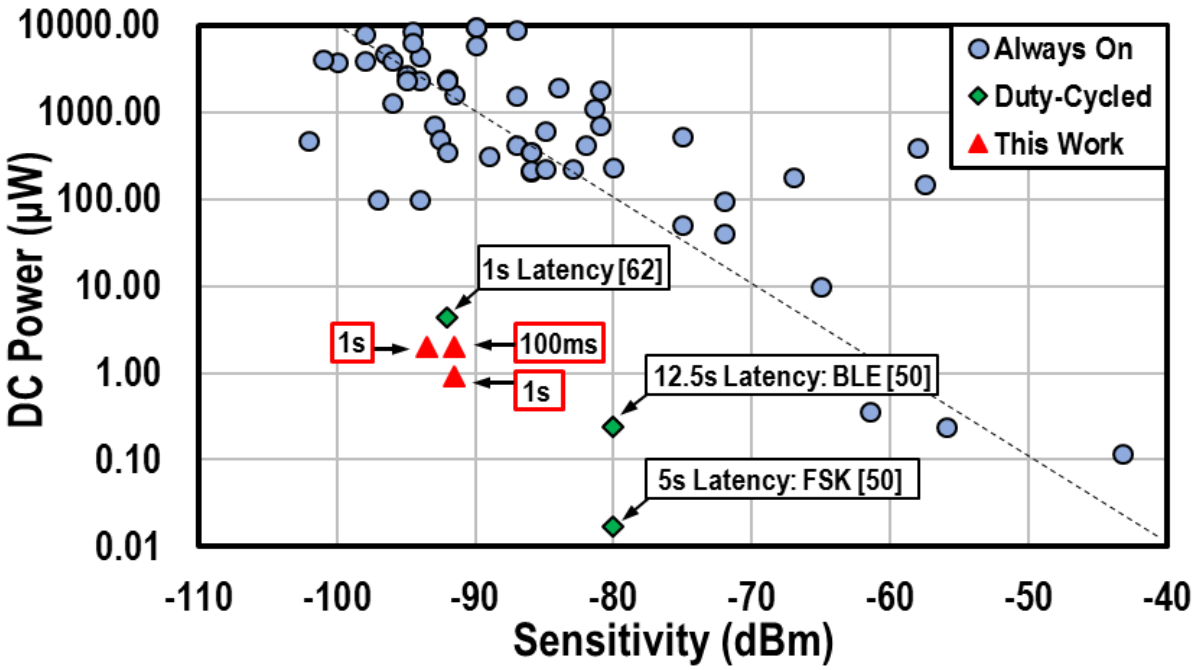


Fig. 1.13. Sensitivity versus power of prior state-of-art 2.4GHz receivers from 2010-2020 including the contributions of this thesis.

1.5.4 Dissertation Organization

The remainder of this thesis is organized as follows:

Chapter 2:

This chapter qualitatively presents the sensitivity limitations of envelope-detector 1st topology and tuned-RF topology and propose a sensitivity improvement by limiting the equivalent noise bandwidth prior to the envelope detector with high-Q band-pass filtering. The bit-level duty cycling concept is introduced as the chosen power saving method and the effects are qualitatively analyzed for sensitivity and selectivity considerations. A prototype CMOS wake-up receiver operating at 428MHz achieving a sensitivity of -106dBm with 33nW dc-power is presented to validate the proposed improvements.

Chapter 3:

This chapter further explores the merits of bit-level duty cycling and the trade-off space associated with sensitivity, dc-power, and latency. A major bottleneck associated with bit-level duty cycling (CW interference up-conversion) is analyzed and envelope modulated signaling scheme with two-tone RF on-off-keying (OOK) is adopted as a mitigation method. Results from a proof-of-concept prototype CMOS wake-up receiver are also presented employing the proposed techniques. Digitally reconfigurable dynamic ranges of 11dB in sensitivity, 410X in power, and 672X in latency is achieved to demonstrate the trade-off space.

Chapter 4:

This chapter presents the issues associated with the off-chip component integration as well as adopting purely multi-tone signaling schemes. To mitigate these issues, a CMOS only bit-level duty-cycled wake-up receiver with the proposed channel-embedded OOK (CE-OOK) signaling is presented. The CE-OOK signaling creates IF content at the output of an ED without requiring a multi-tone transmission and this concept is used to demonstrate a T-RF receiver with multi-channel communication capabilities at nano-watt power level.

Chapter 5:

This chapter focuses on the analysis and design of uncertain-IF wake-up topology with built-in self-calibration to improve the robustness over prior one-time initial calibration methods. Limitations of the packet-level duty cycling are investigated. Using the statistics of wake-up channel, a carrier sense-based improvement method is employed to further reduce the average power. A highly integrated and scalable 2.4GHz CMOS proof-of-concept wake-up receiver prototype achieving sub-microwatt power at -91.5dBm sensitivity, 100ms latency, and -47.5dB selectivity with zero off-chip RF components is presented.

Chapter 6:

This chapter provides an insightful guide for constrain-driven wake-up receiver design for general RF/analog designers. Various user needs are related to the common wake-up receiver metrics and design space trade-offs are summarized for better selection of topology.

Chapter 7:

This chapter presents the conclusions of this dissertation. A discussion towards future work and identified bottlenecks which warrants further attention is also included.

1.6 Exhaustive List of publications

The publication list is arranged chronologically including the work prior to joining the University of Virginia.

1.6.1 Published as a member of institutions other than University of Virginia

[AD1] **A. Dissanayake**, H. Seok, O. Jung, S. Han and S. Lee, "A 64 µW, 23 dB gain, 8 dB NF, 2.4 GHz RF front-end for ultra-low power Internet-of-Things transceivers," *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Honolulu, HI, 2017, pp. 184-187.

[AD2] H. Seok, O. Jung, **A. Dissanayake** and S. Lee, "A 2.4GHz, −102dBm-sensitivity, 25kb/s, 0.466mW interference resistant BFSK multi-channel sliding-IF ULP receiver," *2017 Symposium on VLSI Circuits*, Kyoto, 2017, pp. C70-C71.

[AD3] J. Kim, D. R. Utomo, **A. Dissanayake**, S. Han and S. Lee, "The Evolution of Channelization Receiver Architecture: Principles and Design Challenges," in *IEEE Access*, vol. 5, pp. 25385-25395, 2017.

[AD4] O. Jung, H. Seok, **A. Dissanayake** and S. Lee, "A 45- µW, 162.1-dBc/Hz FoM, 490-MHz Two-Stage Differential Ring VCO Without a Cross-Coupled Latch," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 11, pp. 1579-1583, Nov. 2018.

1.6.2 Published as a member University of Virginia

[AD5] N. Liu, R. Agarwala, **A. Dissanayake**, D. S. Truesdell, S. Kamineni and B.H. Calhoun,"A 2.5 ppm/°C 1.05 MHz Relaxation Oscillator with Dynamic Frequency-Error Compensation and 8 µs Start-up Time," ESSCIRC 2018 - IEEE 44th European Solid State Circuits Conference (ESSCIRC), Dresden, 2018, pp. 150-153.

[AD6] N. Liu, R. Agarwala, **A. Dissanayake**, D. S. Truesdell, S. Kamineni and B.H. Calhoun,, "A 2.5 ppm/°C 1.05-MHz Relaxation Oscillator With Dynamic Frequency-Error

Compensation and Fast Start-Up Time," in IEEE Journal of Solid-State Circuits, vol. 54, no. 7, pp. 1952-1959, July 2019.

[AD7] Jesse Moody, **Anjana Dissanayake**, Henry Bishop, Ruochen Lu, Ningxi Liu, Divya Duvvuri, Anming Gao, Daniel Truesdell, N. Scott Barker, Songbin Gong, Benton H. Calhoun, and Steven M. Bowers, "A -106dBm 33nW Bit-Level Duty-Cycled Tuned RF Wakeup Receiver," 2019 Symposium on VLSI Circuits, Kyoto, Japan, 2019, pp. C86-C87.

[AD8] Jesse Moody, **Anjana Dissanayake**, Henry Bishop, Ruochen Lu, Ningxi Liu, Divya Duvvuri, Anming Gao, Daniel Truesdell, N. Scott Barker, Songbin Gong, Benton H. Calhoun, and Steven M. Bowers, "A Highly Reconfigurable Bit-Level Duty-Cycled TRF Receiver Achieving −106-dBm Sensitivity and 33-nW Average Power Consumption," in IEEE Solid-State Circuits Letters, vol. 2, no. 12, pp. 309-312, Dec. 2019.

[AD9] D. S. Truesdell, **A. Dissanayake** and B. H. Calhoun, "A 0.6-V 44.6-fJ/Cycle Energy-Optimized Frequency-Locked Loop in 65-nm CMOS with 20.3-ppm/°C Stability," in IEEE Solid-State Circuits Letters, vol. 2, no. 10, pp. 223-226, Oct. 2019.

[AD10] **Anjana Dissanayake**, Jesse Moody, Henry L. Bishop, Daniel Truesdell, Henry Muhlbauer, Ruochen Lu, Anming Gao, Songbin Gong, Benton H. Calhoun, and Steven M. Bowers, "A -108dBm Sensitivity, -28dB SIR, 130nW to 41µW, Digitally Reconfigurable Bit-Level Duty-Cycled Wakeup and Data Receiver," 2020 IEEE Custom Integrated Circuits Conference (CICC), Boston, MA, USA, 2020, pp. 1-4.

[AD11] P. Wang, R. Agarwala, H. L. Bishop, **A. Dissanayake** and B. H. Calhoun, "A 785nW Multimodal (V/I/R) Sensor Interface IC for Ozone Pollutant Sensing and Correlated Cardiovascular Disease Monitoring," *2020 IEEE Symposium on VLSI Circuits*, Honolulu, HI, USA, 2020, pp. 1-2.

[AD12] **A. Dissanayake**, H. L. Bishop, J. Moody, H. Muhlbauer, B. H. Calhoun and S. M. Bowers, "A Multichannel, MEMS-Less −99dBm 260nW Bit-Level Duty Cycled Wakeup Receiver," 2020 IEEE Symposium on VLSI Circuits, Honolulu, HI, USA, 2020, pp. 1-2.

[AD13] S. Link, R. Lu, S. Zhang, S. Gong, **A. Dissanayake** and S. M. Bowers, "Enabling Channelizing Filters for High Impedance Nodes with Temperature Compensated Lamb-Wave Resonators," 2020 Joint Conference of the IEEE International Frequency Control Symposium and International Symposium on Applications of Ferroelectrics (IFCS-ISAF), Keystone, CO, USA, 2020, pp. 1-4.

[AD14] R. Agarwala, P. Wang, H. L. Bishop, **A. Dissanayake** and B. H. Calhoun, "A 0.6V 785-nW Multimodal Sensor Interface IC for Ozone Pollutant Sensing and Correlated Cardiovascular Disease Monitoring," in *IEEE Journal of Solid-State Circuits.*

[AD15] H. L. Bishop*, **A. Dissanayake***, S. M. Bowers and B. H. Calhoun, ***equally credited authors (ECAs)** "21.5 An Integrated 2.4GHz -91.5dBm-Sensitivity Within-Packet Duty-Cycled Wake-Up Receiver Achieving 2µ W at 100ms Latency," *2021 IEEE International Solid- State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2021, pp. 310-312.

[AD16] **Anjana Dissanayake**, Steven Bowers, Benton H. Calhoun, "Stacked Transconductance Boosting for Ultra-Low Power 2.4GHz RF Front-End Design" 2022 IEEE International Symposium on Circuits and Systems (ISCAS), Daegu, South Korea, 2021, pp. 1-4

[AD17] Divya Duvvuri, Xiaochaun Shen, Pouyan Bassirian Jahromi, Henry Bishop, Xinjian Liu, Chien-Hen Chen, **Anjana Dissanayake**, Yaobin Zhang ,Travis Blalock, Benton Calhoun, and Steven Bowers, "A 366 nW, -74.5 dBm Sensitivity Antenna-Coupled Wakeup Receiver at 4.9 GHz with Integrated Voltage Regulation and References", 2021 IEEE/MTT-S International Microwave Symposium (IMS), Atlanta, GA, USA, 2021

Chapter 2

2. Sub-GHz T-RF Wake-up Receiver Phase 1: High-Sensitivity

2.1 Limitations of Envelope-Detector First Architecture

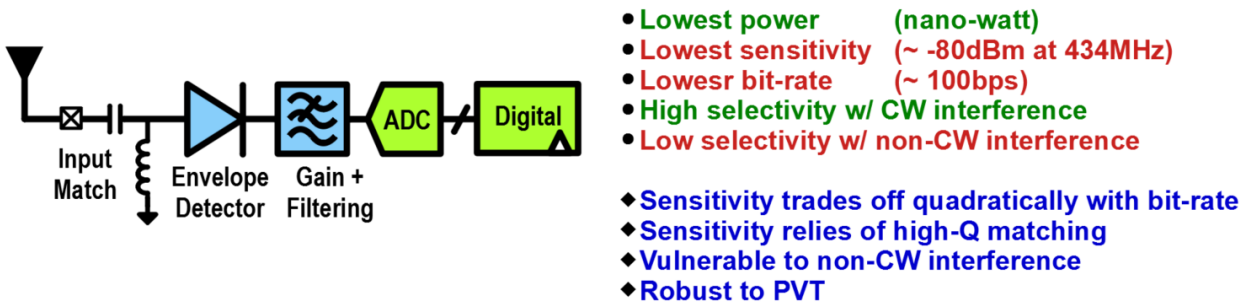


Fig. 2.1. Envelope Detector First Wake-up Receiver topology

Simultaneous nano-watt scale power and high sensitivity is challenging due to the high-power consumption of active RF circuitry required for low noise amplification prior to the detection circuitry. The ED-1st architecture shown in Fig. 2.1 can achieve low active power due to the omission of such RF gain components but trades-off in data rate. The limitations of the ED-1st architecture in the context of co-designed discrete matching networks have been presented in [63], and the sensitivity (P_{MDS}) in decibel-milliwatt can be expressed as:

$$P_{MDS}(dBm) = 5log_{10}(16 \cdot K_B T) + 5log_{10}(BW_{BB}) + 5log_{10}(SNR_{min}) - 5log(R_s) - 10log_{10}(\mu_{det}) + 30dB \quad (2.1)$$

where K_B is the Boltzmann constant, T is the temperature in kelvin, BW_{BB} is the baseband bandwidth corresponding to required data rate, SNR_{min} is the minimum required signal to noise ratio prior to the bit decision circuitry, R_S is the source resistance presented to the envelope detector, μ_{det} is the open circuit voltage of a single rectifier stage, and 30dB accounts for the watt to milli-watt conversion factor. The expression above suggests that the sensitivity can be improved if the envelope detector is driven by an arbitrarily large source resistance as long as an impedance match can be achieved. Fig. 2.2 shows the sensitivity as a function of source resistance for baseband bandwidths of 100Hz, 1KHz, and 10KHz assuming a SNR_{min} of 11dB.

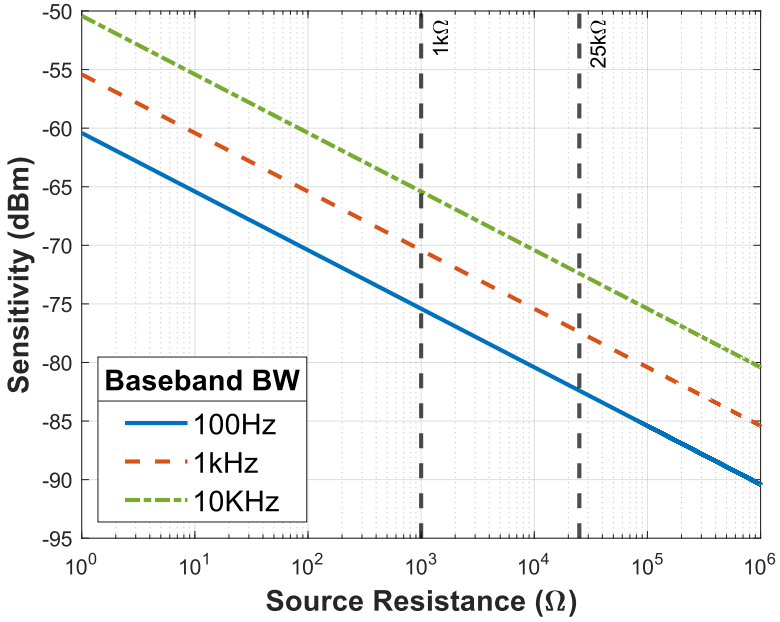


Fig. 2.2. Sensitivity of ED-1st WuRX with respect to source impedance

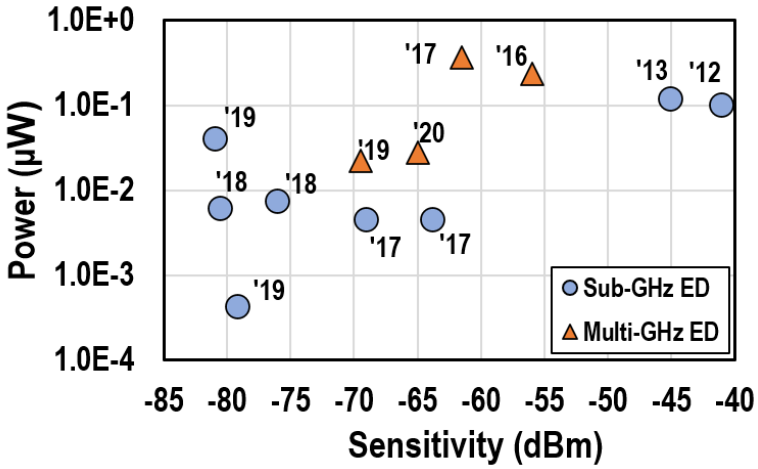


Fig. 2.3. Sensitivity of prior state-of-the-art ED-1st Work

The dashed vertical lines in Fig. 2.2 correspond to the resistance values of 1kΩ and 25kΩ representing available realistic inductor quality factors of on-chip (at 2.4GHz) and off-chip (at sub-GHz). The results indicate that moving towards high quality factor and low

baseband bandwidths can enable high sensitivity. This limits the ED-1st feasibility to sub-GHz range, where sufficiently high-Q off-chip inductors are readily available. These conclusions are evident from the prior state-of-the-art ED-1st wake-up receiver sensitivity shown in Fig. 2.3.

The prior work of Fig. 2.3 also emphasizes a sensitivity limitation of about -80dBm due to the maximum available quality factors of off-chip components. This limitations corresponds to the vertical dashed line at 25kΩ. The communication range corresponding to this sensitivity can be calculated with the Friis path loss equation (1.6) and provides a range of 1.7km in free-space and 250m in urban areas. Since the industrial IoT applications such as agricultural and live-stock monitoring can span several kilometers of range, wake-up receiver architectures capable of achieving sensitivity well beyond -80dBm are highly desirable.

2.2 Insights for Moving Beyond the Limitations of ED-1st

2.2.1 Tuned-RF Architecture for High-Sensitivity:

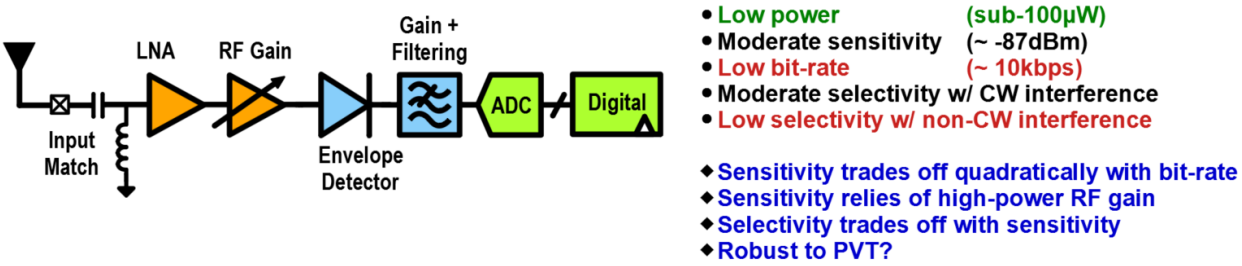


Fig. 2.4. Tuned-RF topology

The limitations of the ED-1st topology call for different architectures to improve the sensitivity beyond -80dBm. Among the prior-work, the Tuned-RF (T-RF) receiver shown in Fig. 2.4 has achieved a sensitivity near -90dBm at 915MHz with 1kHz data rate [40]. The theoretical sensitivity of the T-RF architecture has been derived in [64] for the case of RF bandwidth much larger than the baseband bandwidth, a noiseless baseband chain, and given by:

$$P_{MDS} = -171dBm + NF + 5\log_{10}(SNR_{min}) + 5\log_{10} BW_{RF} + 5\log_{10} BW_{BB} \quad (2.2)$$

where NF is the front-end noise figure and BW_{RF} is the bandwidth prior to the envelope detector. Assuming a front-end noise figure of 10dB, an SNR_{min} of 11dB, a RF bandwidth of

100MHz, and a baseband bandwidth of 1KHz results in a sensitivity of -95dBm, which indicates the feasibility of T-RF architecture as a high-sensitivity wake-up receiver candidate.

The above results also suggest that adopting noise limiting filters prior to the envelope detector at RF, the sensitivity can be further improved. In the numerical example above, reducing the RF bandwidth to 1MHz can improve the sensitivity to -105dBm, a 10dB improvement. This however requires a bandpass filter with much larger quality factors than passive off-chip inductors can provide at high frequencies. For example, considering an RF bandwidth of 1MHz, operating frequencies of 434MHz and 915MHz respectively requires loaded quality factors of 434 and 915.

2.2.2 Duty-Cycling for Low Average Power Consumption

Although T-RF achieves high-sensitivity, the use of low-noise RF gain leads to dissipation of substantial dc-power (146μW in [40]). Thus, reducing the average power to reach sub-μW levels requires adopting a duty cycling scheme. The power due to duty-cycling is given by eq. (1.1) with the duty-factor given by eq. (1.2) for a general component.

For the case of asynchronous data reception, the duty-cycling can be implemented in two different methods:

1. Bit-Level Duty-Cycling (BLDC): The wake-up receiver stays on for a duration of $T_{on,B}$ of a transmitted bit, where the duration of an entire bit is $T_{per,B}$. The best-case duty-factor (D_{BLDC}) is then given by:

$$D_{BLDC} = \frac{T_{on,B}}{T_{Per,B}} \tag{2.3}$$

2. Packet-level Duty (PLDC): The wake-up receiver stays on for a duration of two wake-up packets $T_{on,P}$ and transmission lasts for a duration of $T_{per,P}$ which comprises of multiple packets. The duty-factor (D_{PLDC}) is then given by:

$$D_{PLDC} = \frac{T_{on,P}}{T_{Per,P}} \tag{2.4}$$

The above two methods are illustrated graphically in Fig. 2.5.

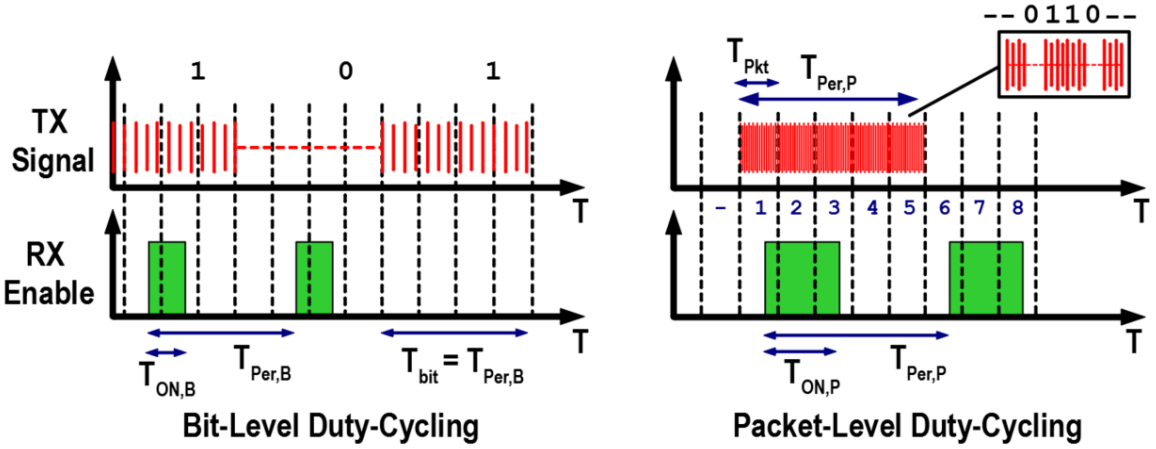


Fig. 2.5. Two Duty-cycling concepts for asynchronous receivers.

Both duty-cycling schemes can achieve low power by appropriately scaling the on-to-off time (duty-factor). Therefore, a qualitative analysis of the two methods with respect to sensitivity is necessary for selecting the most appropriate scheme in the context of T-RF architecture. Assuming a T-RF receiver with zero leakage, instantaneous start-up, and equal power dissipation in both BLDC and PLDC operation, yields the following latency and baseband bandwidths:

$$BLDC\ Latency: \boldsymbol{Lat_{BLDC}} = \boldsymbol{N}.\boldsymbol{T_{per,B}} \tag{2.5}$$

$$PLDC\ Latency: \boldsymbol{Lat_{PLDC}} = \boldsymbol{T_{per,P}} = \frac{\boldsymbol{T_{per,B}}\cdot\boldsymbol{T_{on,P}}}{\boldsymbol{T_{on,B}}} \tag{2.6}$$

$$BLDC\ Bandwidth: \boldsymbol{BW_{BLDC}} = \frac{\boldsymbol{0.35}}{\boldsymbol{T_{on,B}}} \tag{2.7}$$

$$PLDC\ Bandwidth: \boldsymbol{BW_{PLDC}} = \frac{\boldsymbol{N}}{\boldsymbol{T_{on,P}}} = \frac{\boldsymbol{N}\cdot\boldsymbol{T_{per,B}}}{\boldsymbol{T_{on,B}}\cdot\boldsymbol{T_{per,P}}} \tag{2.8}$$

where N is the number of bits in a single wake-up message. Assuming both BLDC and PLDC modes are limited by the same minimum achievable on-time, the BLDC latency is N times larger than the PLDC latency. However, the same case leads to a 0.35/N times smaller baseband bandwidth in BLDC. This is because PLDC requires Nyquist criteria to avoid inter-symbol-interference. That is, during the on-time, PLDC needs to accurately decode multiple sequential bits instead of performing a pure energy detection operation as BLDC does. And this sequential bit detection requires a larger bandwidth than inherent rise time requirement of a single bit. Larger bandwidth translates to more baseband noise which reduces the signal to noise ratio.

BLDC experience a reset phase between two successive bits, while the required bandwidth is related to the rise time. Assuming a wake-up message length of 32 bits, BLDC

can achieve approximately 10dB better sensitivity than PLDC in the case of (2.2) where both power and sensitivity are optimized while sacrificing latency. Hence the Tuned-RF architecture in this work adopts packet-level duty-cycling as the preferred power reduction method. Additionally, since the transmitted length of a bit is comparatively much longer with BLDC, an ED-1st receiver in the same network can also operate at the maximum sensitivity, which allows for optimized co-existence of both topologies.

2.3 Receiver Implementation

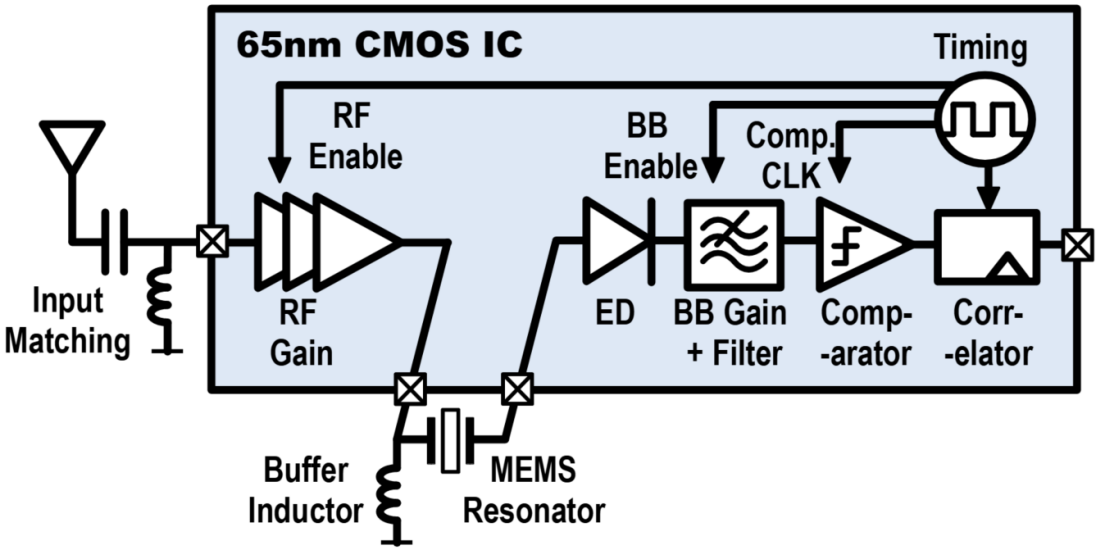


Fig. 2.6. Block diagram of the implemented receiver

The block diagram of the implemented tuned-RF receiver is shown in Fig. 2.6 and includes co-designed 65nm CMOS IC, off-chip matching network, and external MEMS resonator [65, 66]. The input RF OOK signal at 428MHz carrier frequency is fed to the CMOS IC through an impedance boosting matching network providing passive voltage gain. The RF signal is further boosted by a low-noise RF amplifier chain and filtered by an off-chip Aluminum-Nitride based MEMS resonator for noise-limiting to improve the sensitivity. An off-chip inductor at the resonator driving interface is used to mitigate the parasitic capacitance. The filtered signal is then fed to an envelope detector for rectification. Then, the rectified signal corresponding to the baseband bit-stream is further filtered and amplified prior to bit detection with a comparator. The digital bit stream is used for wake-up packet detection using a digitally synthesized address correlator. An integrated clock generator is used for duty-cycling and digital circuits. The tunable parameters in various circuit blocks can be digitally programmed by an integrated serial-to-parallel (SPI) interface. The CMOS portion of the receiver was

implemented using Taiwan semiconductor manufacturing company (TSMC) 65nm low-power (LP) process to benefit from the multiple threshold voltage devices and low leakage.

2.3.1 Timing and Synchronization

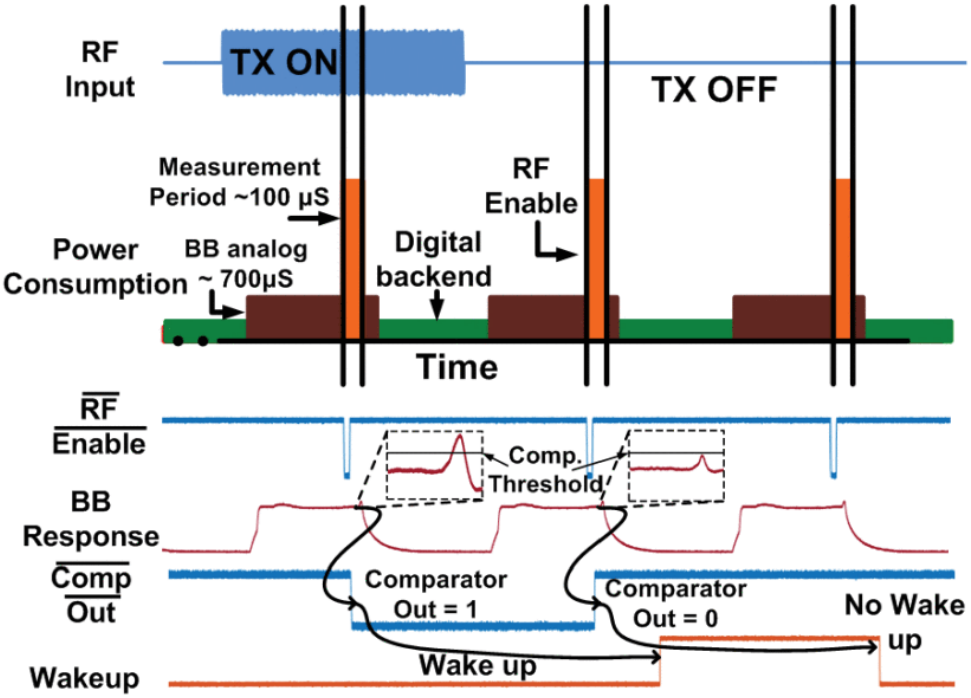


Fig. 2.7. Illustration of duty-cycling pulses and measured time domain waveforms

The bit-level duty-cycling is adopted as the preferred power reduction method. Dedicated supply enable signals are provided to the RF and baseband circuitry as shown in Fig. 2.7. The RF-circuitry consumes substantially high dc-power to operate at 428MHz and achieve much smaller time constants than the slow baseband circuitry. If a single enable signal is used for both the RF and baseband, then the start-up time is dominated by the slow baseband while power consumption is dominated by RF. Therefore, an optimized solution is to distribute the enable signal, such that the slow but low-power baseband circuitry are enabled first (~0.7ms start-up time), followed by the fast but high-power RF circuitry (< 100µs start-up time). At the end of the RF enable time, the comparator issues a bit-decision based on a programmable threshold value and latched to the digital correlator for wake-up detection. The measured time domain behavior during wake-up reception is also plotted in Fig. 2.7.

The nature of BLDC is to sample a small portion of a bit and has the benefit of low overhead in synchronization. The probability of the sampling window occurring at the edge of a transmitted bit, such that a portion of '1' and '0' is captured, is equal to the duty factor. This

allows for omission of over-sampling as required by the ED-1st wake-up receiver to properly align the optimum comparator sampling edge. The programmable main clock (fast-clock) operates at tens of kilohertz and a divided version (slow-clock) sets the duty period, which in turn sets the bit period. The pulse width of the fast-lock limits the minimum achievable duty-cycling pulse length for each circuit block. The timing signals are controlled by 16-bit counters and dynamic range of 1 to 65535 can be achieved with respect to the system clock used for duty-cycling.

2.3.2 Circuit Level Implementation Details

RF front-end

The RF frontend design plays a critical part in optimizing the sensitivity of a tuned-RF wake-up receiver. As an outcome of this research, the SNR at the output of the ED for a Tuned-RF wake-up receiver was previously derived in [67] as,

$$SNR_{Out} = \frac{V_{RF}^2}{16BW_{BB}}\left(\frac{V_{RF}^2+16K_BT_{Sys}B_{RF}R_S}{2V_{RF}^2T_{sys}K_BR_S+BW_{RF}\left(T_{sys}K_BR_S\right)^2}\right) \quad (2.9)$$

where, V_{RF} is input RF signal voltage at ED input, B_{RF} is RF noise equivalent bandwidth (NEB), BW_{BB} is the BB noise equivalent bandwidth, and T_{sys} is the system noise temperature at the input to ED. Given that the BB bandwidth is determined by the RF sampling time, optimizing for the RF NEB and system noise figure yield the highest sensitivity achievable, which agrees with the work of [64]. To this end, a high-Q MEMS resonator was placed before the ED to maximize the SNR. The resonator filters out both the source noise and the wideband output thermal noise of the RF gain stages, and this prevents the wideband noise self-mixing effect.

The required minimum RF gain prior to baseband can be approximated from [64] and given by the following expression:

$$A_V \geq \sqrt{\frac{10}{K_BT\cdot F\cdot\mu_D}\sqrt{\frac{v_{in,bb}^2}{BW_{RF}\cdot BW_{BB}}}} \quad (2.10)$$

where μ_D is the detector total OCVS, $v^2_{in,bb}$ corresponds to the input referred noise of the baseband chain. Any RF gain beyond this value does not provide any sensitivity benefit and can negatively affect the receiver linearity.

The implemented RF gain stages comprise a low-noise amplifier, a regenerative ring amplifier, and an off-chip inductor loaded buffer amplifier [66]. The envelope detector is a ten stage pseudo-differential triode mode Dixon rectifier [68]. The simulated input matching Q-factor is approximately 43 with a bandwidth of 10MHz at 430MHz. The full RF amplifier chain provides a voltage gain of 68dB. The simulated open circuit voltage sensitivity of rectifier is 100V/V^2.

Baseband Circuitry

The output signal of the RF envelope detector carries the desired rectified signal, the rectified thermal noise of the source impedance, and the noise of the active RF circuitry, spread across a wider bandwidth. Therefore, the ED output signal requires additional baseband filtering and amplification prior to the bit decision circuitry. This is captured by the "$5\log_{10}(BW_{BB})$" term of eq. (2.2). Ultra-low power baseband gain cells are required for the proper amplification and filtering for a minimum system dc-power overhead.

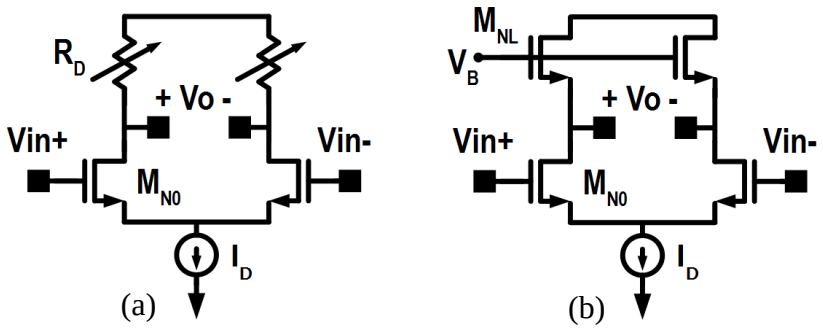


Fig. 2.8. Conventional baseband gain cells

The conventional variable gain cell shown in Fig. 2.8-(a) has the advantage of simple and compact design, where the gain can be set by tuning the load resistor R_D. The gain for this amplifier is given by the product of transconductance of M_{N0} and load resistance R_D, where the output common mode level trades off with the dc-power consumption. Assuming deep sub-threshold operation to maintain low dc-power and high g_m/I_D efficiency, the required load resistor size for voltage gain > 1 can be calculated as

$$R_D > \frac{2nU_T}{I_D} \tag{2.11}$$

where U_T is the thermal voltage, n is the sub-vt slope factor, and I_D is the total bias current of differential amp. For a bias current = 200nA and n = 1.5, the required R_D needs to be larger than 780kΩ, which would occupy a large chip area and suffer from high process variation.

The gain cell shown in Fig. 2.8-(b) adopts a transconductance load to alleviate the resistive loading issue. This topology also performs better with process variation, which is evident by the voltage gain expression, which can be derived using device transconductances as:

$$Voltage\ Gain \propto \frac{g_{m_{N0}}}{g_{m_{NL}}} \tag{2.12}$$

The transconductance is purely a function of the bias current in sub-vt region, which limits the maximum achievable voltage gain of this topology to unity. To overcome the unity gain threshold, this work adopts the current bleeding transconductance loading shown in Fig. 2.9. The proposed technique allows for independent scaling of the transconductance in sub-vt regime.

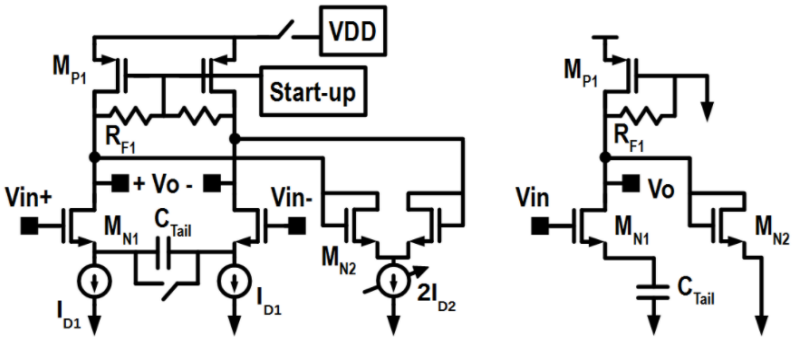


Fig. 2.9. Proposed sub-vt transconductance loaded differential gain cell and half circuit

In sub-vt operation, nearly all transistors demonstrate rectification properties owing to even order non-linearity, which contribute dc offsets along the signal chain. Such offsets can saturate the succeeding stage amplifiers in baseband chain. The differential amplifier shown in Fig. 2.9 is therefore designed as a pseudo differential cell with a transmission zero inserted set by C_{Tail}. The transfer function for this cell can be derived using the half circuit shown in Fig. 2.9:

$$H(s) \approx -\frac{g_{mN1}}{g_{mN2}}\left[\frac{\frac{sC_{Tail}}{g_{mN1}}}{\left(1+s\left(\frac{C_{Tail}+C_{gs1}}{g_{mN1}}\right)\right)\cdot\left(1+\frac{sC_L}{g_{mN2}}\right)}\right] \tag{2.13}$$

where g_{mN1} and g_{mN2} are the transconductance of M_{N1} and M_{N2}, C_{gs} is the gate source capacitance of M_{N1}, C_L is the total output capacitance, and R_F is a self-bias resistor assumed to be large. The overall transfer function demonstrates an ideal bandpass behavior with the transmission zero. The first pole, which determines the low side of passband, is set by C_{Tail},

while total load capacitance determines the high side of passband. The Passband gain can be approximated by setting $C_L = 0$, C_{Tail} = infinite, which yields a voltage gain $A_V \approx -\frac{g_{mN1}}{g_{mN2}}$.

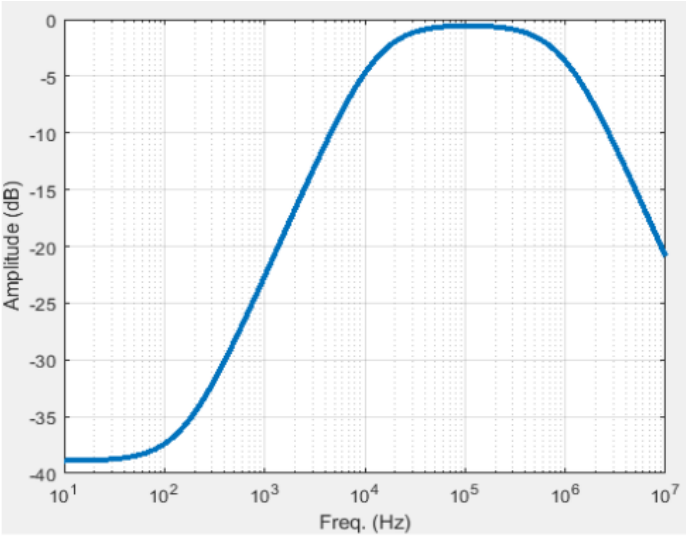


Fig. 2.10. Simulated transfer function of baseband amplifier in unity gain configuration.

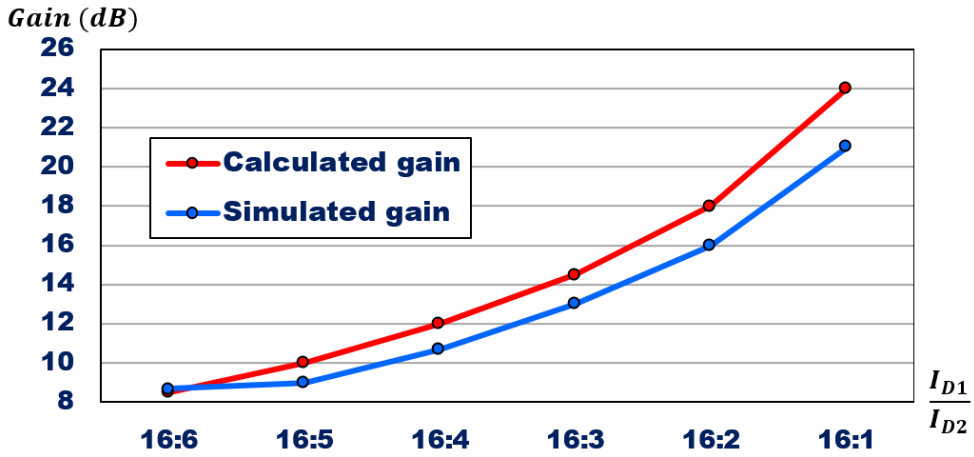


Fig. 2.11. Simulated vs. Calculated passband gain of the proposed amplifier.

The simulated behavior for a passband unity gain with a bias current of 20nA is shown in Fig. 2.10. The results indicate that the finite impedance of the tail current source of M_{N1} deviates the transmission zero from the origin. The topology provides the benefit of gain control robust to process variation as well as feedback-less bandpass response without having to add series capacitors to the signal path. Moreover, C_{Tail} can be realized with an off-chip capacitor providing higher tunability of the passband. The bandpass nature also aids with flicker noise reduction. The calculated and simulated passband gains for various current ratio for I_{D1}/I_{D2} are shown in fig 2.11.

The startup time of the amplifier is of great concern since long startup can waste energy in a bit level duty cycled implementation (more on this is presented in chapter 5). Due to the high time constants associated with baseband circuits, a fast startup plan should be incorporated into any baseband circuitry. To improve the startup time, this work utilizes a critical node pre-charging scheme to momentarily change the time constants to low during startup. The PMOS gate node in the proposed cell has the longest time constant due to the large feedback resistance, which slows the gate charge build up in a diode connected configuration. Therefore, this critical node is pre-charged to the ground voltage during the startup, such that the instantaneous current through the PMOS is large enough to charge its gate node faster.

The input referred noise voltage of the proposed baseband VGA can be derived as,

$$v_{in}^2 = \frac{4K_B T\gamma}{g_{mN1}^2}(g_{mN1} + g_{mN2} + g_{mP1}) + \frac{K_f}{g_{mN1}^2 C_{ox}}\left(\frac{g_{mN1}^2}{(WL)_{N1}} + \frac{g_{mN2}^2}{(WL)_{N2}} + \frac{g_{mP1}^2}{(WL)_{P1}}\right) \quad (2.14)$$

where γ is the channel thermal noise coefficient, K_f is the process dependent flicker noise coefficient, C_{ox} is the unit oxide capacitance, and $(WL)_i$ represents the total area of i^{th} transistor. The feedback resistor and current source noises have been neglected and flicker noise in both NMOS and PMOS are treated equally in the above calculation. The noise contribution demonstrates a direct trade off with dc-power and the flicker noise can be further attenuated by selecting a large device size.

Fig. 2.12 shows the block diagram of the implemented Gm-C type baseband filter. The Gm-C architecture is chosen due to the low power constraints, where active-RC implementation generally requires high power for op-amp cells.

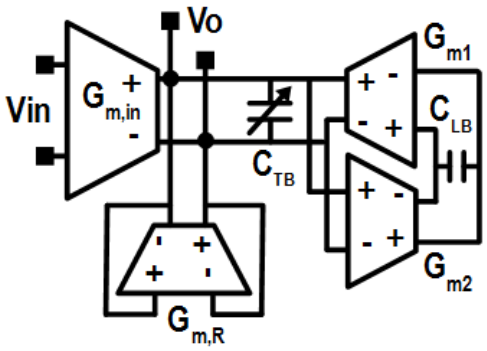


Fig. 2.12. Schematic of the bandpass filter

The center frequency ($f_{C,BP}$) and the Q-factor (Q_{BP}) of the implemented bandpass filter can be derived as,

$$f_{C,BP} = \frac{1}{2\pi}\sqrt{\frac{G_{m1}G_{m2}}{C_{TB}C_{LB}}} \tag{2.15}$$

$$Q_{BP} = \sqrt{\frac{C_{TB}}{C_{LB}}\frac{G_{m1}G_{m2}}{G_{m,R}^2}} \tag{2.16}$$

where G_{mi} is the transconductance of i^{th} gain cell made of conventional five-transistor differential OTA. The output impedances of the $G_{m,R}$, G_{m1}, and G_{m2} are assumed to be infinitely large.

Fig. 2.13 shows the complete baseband signal chain, including the comparator bank and the digital circuitry used for automatic gain and offset correction. Three comparators are used to determine the dc-value of the rectified signal and the baseband is increased or decreased depending on the signal level.

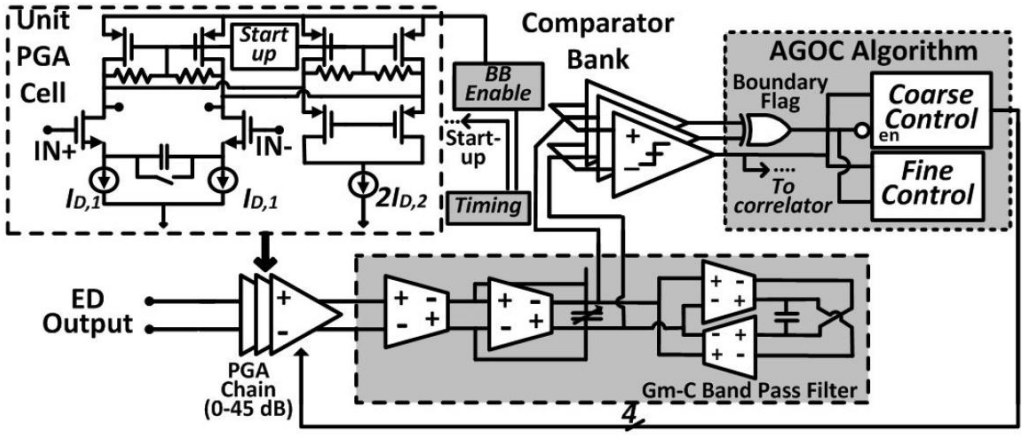


Fig. 2.13. Complete baseband signal chain

2.4 Measurement Results

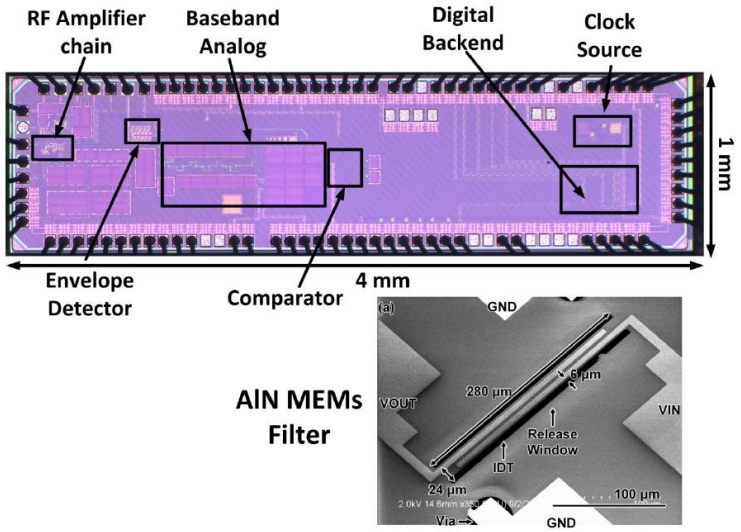


Fig. 2.14. Die photos of CMOS IC and Aluminum Nitride MEMS resonator

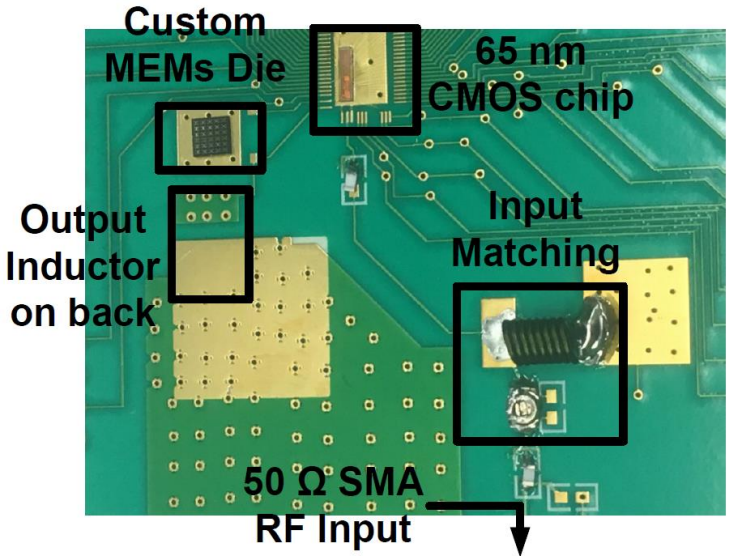


Fig. 2.15. Photograph of the test PCB implementation on Rogers 4350 Material

The wake-up receiver was implemented in TSMC-65nm CMOS process and the MEMS resonator is fabricated using a custom process (Fig. 2.14). The wake-up receiver system is assembled using a Rogers 4350 RF material based printed circuit board (PCB) and chip-on-board (COB) assembly for maintaining high input matching Q-factor (Fig. 2.15). The input matching is realized with a CoilCraft™ air core inductor and a variable capacitor at the input. The MEMS resonator is wire-bonded to the PCB and the buffer inductor is placed on the opposite side to reduce the electro-magnetic coupling between input and output sides of the RF amplification chain. The CMOS IC operates with a 0.75V power supply.

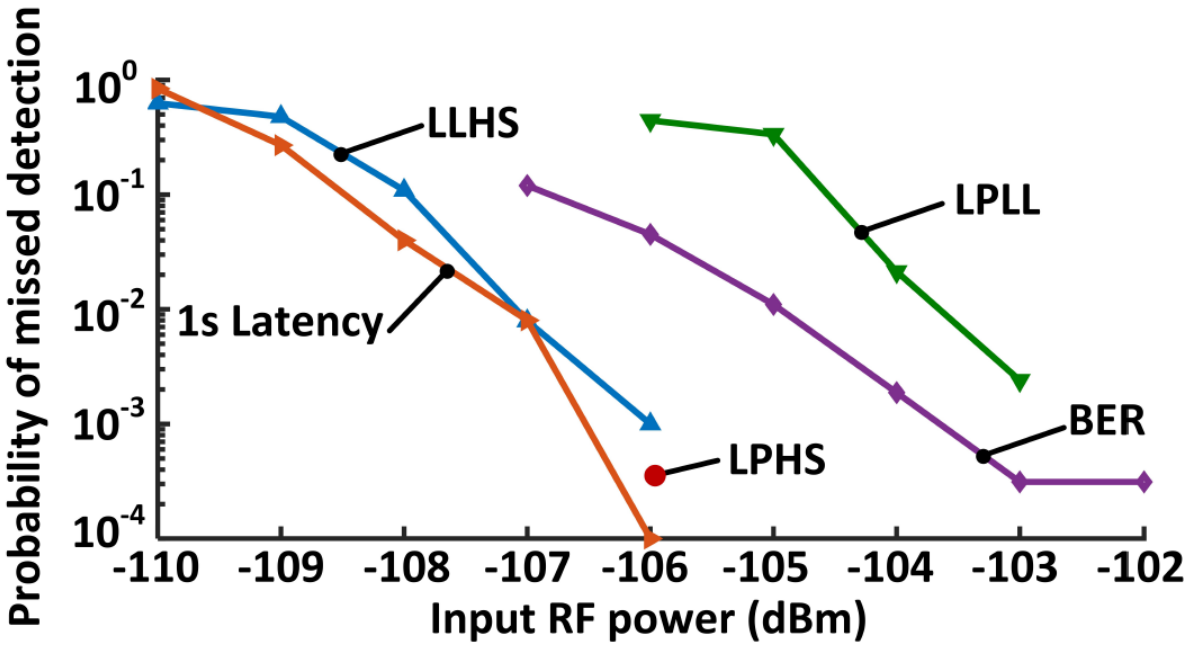


Fig. 2.16. Measured wake-up receiver sensitivity for various operation modes

Since bit-level duty-cycling lends to high degree of sensitivity, power, and latency trade-off, the wake-up receiver sensitivity is captured by measuring the bit-error ratio (BER) and missed detection ratio (MDR) for various operating modes. The low-power high-sensitivity (LPHS) mode operates at 5s latency with highest integration time while sacrificing latency to maintain low power. Both the low-latency high-sensitivity (LLHS) and low-power low-latency (LPLL) modes operate at 240ms latency. The LLHS mode sacrifices power to attain lower latency by operating at a faster bit rate with longer integration time while the LPLL mode sacrifices sensitivity to attain low power with a shorter RF integration time. Additionally, a 1 second latency measurement is also carried out to characterize the operation of mid-scale latencies. The modes are selected by programming the slow-clock frequency, which sets the overall latency. The RF integration time sets the maximum sensitivity. Since the active power consumption is largely dominated by the RF circuitry, the receiver demonstrates a strong sensitivity and dc-power trade-off.

The measured bit-error rate in the high-sensitivity mode is 0.1% for an input RF power of -103dBm. This sensitivity value is improved to -106dBm in the wake-up detection with several errors tolerated in the 15-bit correlator. The measured false positive rate is less than one per hour. The LPHS mode achieves the best sensitivity and power combination of 32.7nW at -106dBm for 5s latency, while the power is increased to 288nW in LLHS mode for a latency of 240ms. For the same 240ms latency, the power can be reduced by trading off-sensitivity with shorter RF sampling time, which achieved -103dBm sensitivity for 161nW. Overall, the wake-up receiver demonstrates tunability dynamic ranges of 8.7X in power, 20.8X in latency, and 3dB in sensitivity, which can be used for a wide variety of applications.

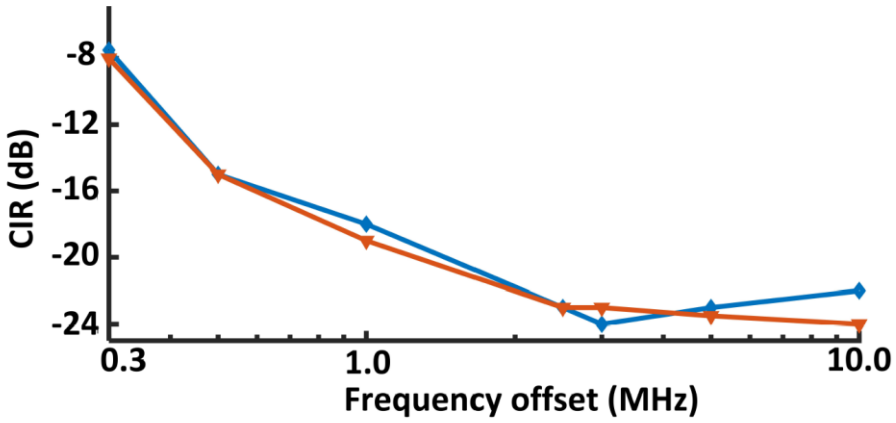


Fig. 2.17. Measured Signal-to-Interference ratio (SIR)

Fig. 2.17 shows the measured signal to interference ratio (SIR) of the receiver for varying interference offset on high side and low side of the carrier signal. The desired RF signal is set to a -102dBm (1dB above the BER) and the interference signal power is increased until a BER of 1% is observed. The measured results show that a worst-case SIR of -16dB at 1MHz offset and -20dB at 10MHz. This interference performance is largely due to the shape of the input matching network and selectivity of the MEMS resonator.

Table 2.2. Performance summary and comparison to state-of-the-art work.

	This Work			[31]	[29]	[50]	[51]	[25]
	LPHS	LLHS	LPLL					
Technology	65 nm			130 nm	65 nm	65 nm	65 nm	65 nm
Carrier Frequency	428.3 MHz			151.8 MHz	113 MHz	2.4 GHz	433 MHz	2.4 GHz
Sensitivity	-106 dBm	-106 dBm	-103 dBm*	-76 dBm	-80.5 dBm	-80 dBm	-102.5 dBm	N/A
Power Consumption	33 nW	288 nW	161 nW	7.4 nW	6.1 nW	17 nW	378 µW	236 nW
Latency/Data Rate	5 s	240 ms	240 ms	92.5 ms	180 ms	5 s	1kbps	12.8 ms
Interferer Rejection	AGOC/MEMS			Offset Comp	N/A	N/A	N/A	N/A
CIR @ 0.1% Offset	-16 dB			-27 dB	N/A	N/A	N/A	N/A
Sensitivity BER	-103			-75	N/A	N/A	N/A	-56.5
Die Area	3.95 mm^2			1.95 mm^2	6 mm^2	4 mm^2	2.25 mm^2	1.1 mm^2

* Measured at 99.7% Probability of detection

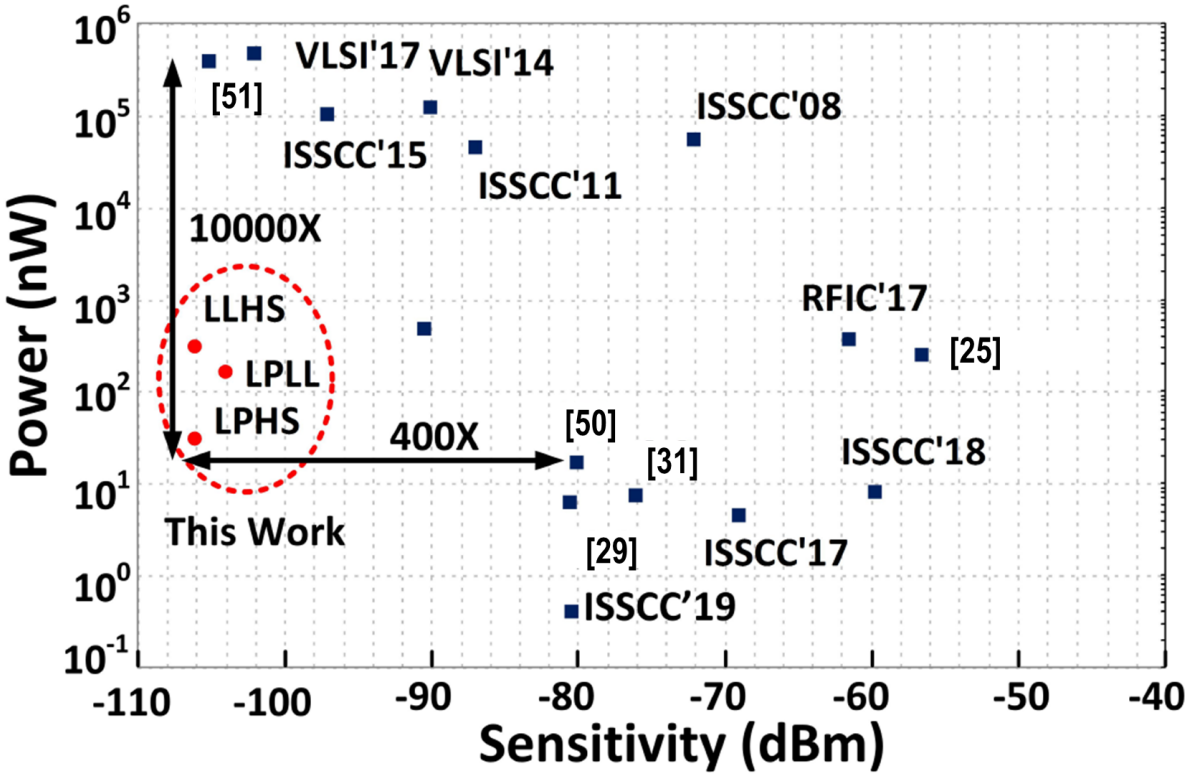


Fig. 2.18. Power and sensitivity comparison to prior wake-up receivers.

Table 2.1 shows the comparison of the measured performance of this work to prior state-of-the-art work. Fig. 2.18 shows the sensitivity and power scatter plot of wake-up

receivers highlighting the contributions of this work. To the best of our knowledge, this work was the first wake-up receiver demonstration with better than -100dBm sensitivity while simultaneously achieving nano-watt power. An improvement of 1000X in dc-power due to aggressive duty-cycling and 26dB in sensitivity due to noise-filtered T-RF architecture is achieved, while maintaining similar latency to prior ED-1st demonstrations.

2.5 Conclusions

The envelope detector first topology provides excellent power savings but scaling the sensitivity requires high quality factor input matching inductors and high open circuit voltage sensitivity. Prior ED-1st work achieved a maximum sensitivity near -80dBm for several hundreds of milli-second latency at sub-GHz operation. Tuned-RF architecture can surpass this sensitivity limitation by adopting low-noise RF gain prior to rectification but requires duty-cycling to reduce the average power to nano-watt scale. This work demonstrates a bit-level duty-cycled T-RF receiver with a high-Q MEMS resonator prior to the envelope detector for further sensitivity boosting by noise filtering. A maximum sensitivity of -106dBm was demonstrated for a low average power of 33nW at 5s latency and 288nW at 240ms latency at 428MHz. This work is suitable for a wide variety of long range IoT applications and paves a way to reach beyond the limitations of ED-1st topology.

2.6 Personal Contributions

- Programmable gain baseband amplifier and bandpass filter design efforts, including schematic, layout, and post-layout extraction level verification.
- Assisted the RF LNA design in schematic level.
- Co-lead the baseband testing efforts and assisted the full system characterization.
- Contributed to the manuscript writing process of conference [65] and journal paper [66].

Acknowledgements

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University of Illinois Urbana Champaign: Ruochen Lu, Anming Gao, Songbin Gong.

Chapter 3

3. Sub-GHz T-RF Wake-up Receiver Phase 2: High-Dynamic Range

The first phase wake-up receiver demonstrated that better than -100dBm sensitivities can be achieved for sub-μW power levels. However, the prior phase demonstrated a limited reconfigurability level. Digital reconfigurability of the wake-up receiver is highly desirable to compensate for environmental uncertainties such as fading and multipath by enabling trade-offs between the latency, dc power, and sensitivity. Therefore, this phase prioritizes the high reconfigurability aspect and interference suppression improvements with MEMS integration. To this end, special care has been given to start-up improvements in both RF and IF/BB implementations.

The implemented bit-level duty-cycled T-RF wake-up receiver achieved -108dBm sensitivity while consuming 130nW dc-power, achieving -25dB close-in Signal-to-Interferer Ratio (SIR) (0.12% frequency offset from carrier) and -28dB far-out SIR (0.7% frequency offset from carrier) at 430MHz frequency. Digitally programmable dynamic ranges of 11dB in sensitivity, 410X in power, and 672X in latency are achieved to demonstrate the trade-off space. This was possible due to the adoption of:

1) Two-tone RF OOK modulation to enable IF bandpass filtering for interference suppression without the use of a power hungry LO.
2) Multi-stage sequential Bit-Level Duty Cycling (BLDC) with tunable RF sampling time and baseband filter bandwidth with fast startup circuitry.

3) High gain tuned-RF architecture with high-Q RF filtering via co-design of active CMOS and an Al-N MEMS filter.

4) 6-bit SAR ADC-aided automatic offset and gain control (AGOC) for dynamic threshold correction.

Table 3.1. Trade-offs enabled by BLDC.

Parameter	Increase	Decrease	Upper Limit	Lower Limit
RF sample time (RF on)	High sensitivity. High dc-power. Low dc-offsets.	Low sensitivity. Low dc- power. High dc-offset.	Full bit period.	Pulse width of reference clocks. Digital Leakage.
Bit rate	Low latency	High latency.	Clock freq. Stability. Max clock freq. ED risetime. ADC sampling rate	Clock freq. Stability. Digital Leakage.

Table 3.1 summarizes the trade-offs enabled by the bit-level duty cycling including the upper and lower limits. The sensitivity is increased by expanding the RF enable time, but this comes at the cost of increased dc-power. Expanding the RF sampling time also reduces the dc-offset and interference up-conversion effects due to spectrum shaping explained later. Conversely, reducing the RF sample time reduces the power but at the cost of sensitivity and increased effects of dc-offsets. The maximum duration of the RF sample time is a full bit, but once the on time is sufficiently large, the probability of sampling occurring near an edge also increases. Oversampling is required to mitigate this issue. The lower limit of the sampling time is given by the pulse width of the clock pulse that regulated the timing circuitry. The bit-rate and therefore the latency can be modified by employing a larger counter length as well as a higher frequency system clock. The highest bit-rate would be limited by the minimum rise time of the envelope detector. It should also be noted that increasing the latency beyond a certain point does not provide a dc-power benefit when the system power is dominated by leakage.

3.1 Receiver Architecture

The receiver architecture and the signal propagation at various nodes are shown in Fig. 3.1 [69]. The RF OOK signal made of two-tones is fed to a low noise and high gain RF amplifier chain through an off-chip input match. The amplified signal is then filtered with an off-chip MEMS filter and fed to the RF triode mode Dixon ED. Due to the signaling method, the ED generates dc as well as IF content. The IF content is further amplified and filtered for detection. The BB signal is digitized with a 6-bit SAR ADC as opposed to a bit decision with an analog comparator for faster offset convergence in the digital domain.

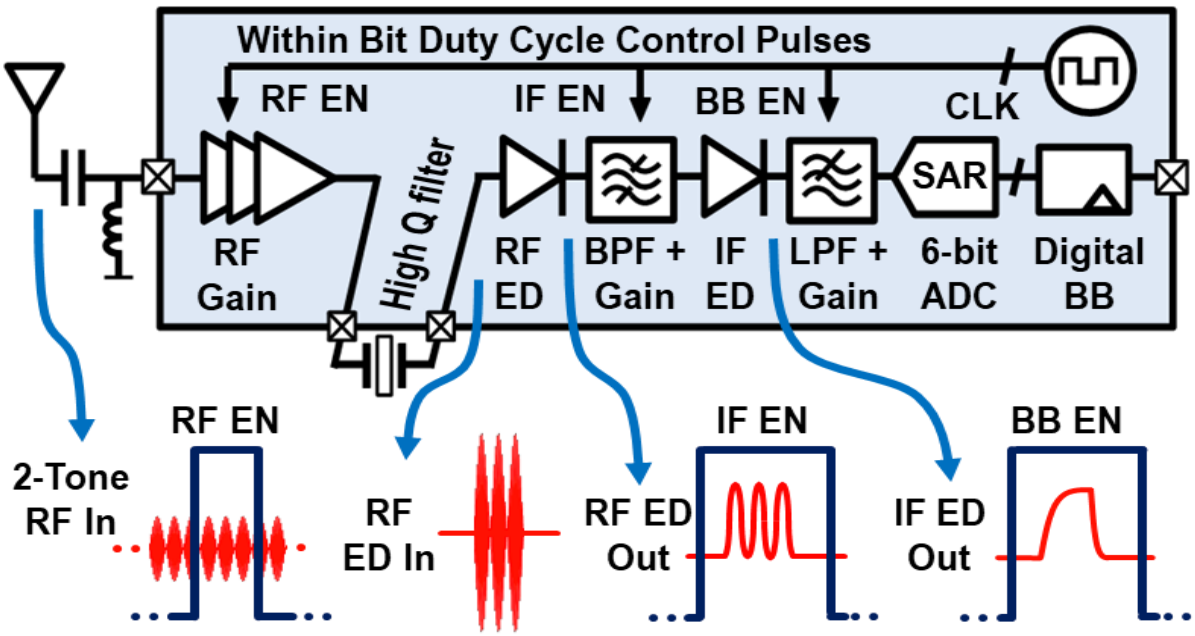


Fig. 3.1. Proposed Gen-2 bit-level duty cycled WuRX block diagram of showing time domain signal at each node

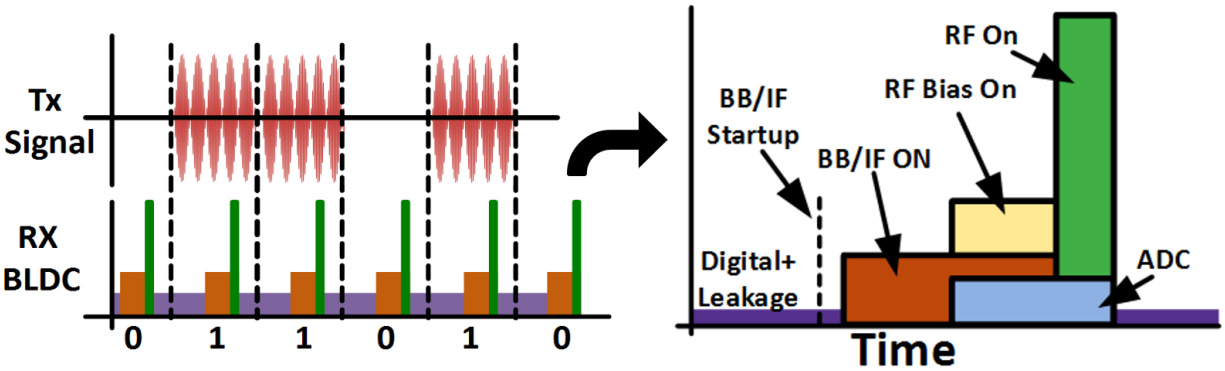


Fig. 3.2. Bit Level Duty Cycling (left) and zoomed in multi-stage turn on sequence (right)

The BLDC scheme in this work adopts a multi-stage turn-on scheme with dedicated timing pulses to the RF, IF/BB, and ADC as shown in Fig. 3.2. This enables aggressive per-

block-optimized duty cycling of both high-current fast RF blocks and low-current slow baseband analog circuits to realize higher reconfigurability as opposed to a single startup of the full RF and baseband path. With the implemented enhancements, the RF sampling time can be reduced to as low as 20µs, achieving lower average RF dc power.

3.2 An Unwanted Effect: Spectrum Shaping Due to BLDC

An ED-1st wake-up receiver experiencing a continuous wave (CW) interferer produces a constant dc offset at the output of the ED. Such offsets can be removed by either ac-coupling or an analog/digital offset compensation mechanism and can achieve sufficiently large interference tolerance. Non-CW signals however cannot be suppressed by simple ac-coupling and act as blockers. A T-RF receiver behaves similarly to and ED-1st in the case in steady state operation. However, with bit-level duty-cycled conditions, the input to the ED undergoes a windowing operation. This can be mathematically represented as:

$$v_{IF}(t) = v_{RF}^2(t) \cdot Rect\left(\frac{t}{\tau}\right) \tag{3.1}$$

where $v_{IF}(t)$ is the rectified output of envelope detector, $v_{RF}(t)$ is the input RF signal, and $Rect(t/\tau)$ is a rectangular pulse approximating the abrupt turn on of the receiver. The frequency content of the envelope detector output can be obtained by the Fourier transform of (3.1) and is given by:

$$V(f) = F\{v_{RF}^2(t)\} * sinc(\tau f) \tag{3.2}$$

This spectrum shaping due to the rectangular windowing is graphically plotted in Fig. 3.3 for a desired signal and a CW interferer for an RF enable time duration of 200µs.

Fig. 3.3 shows that the rectified CW-interference is indistinguishable from the wanted signal spectrum. Since the baseband spectrum of the interferer now has energy at non-dc, a simple ac-coupling can no longer suppress the dc-offsets suggesting poor interference tolerance. However, it can be noted that CW interference causes a deterministic spectrum at the output of the ED such that it causes a deterministic offset on the ideal bit decision threshold.

Hence, theoretically, such deterministic offsets can be corrected by addition or subtraction from the decision threshold.

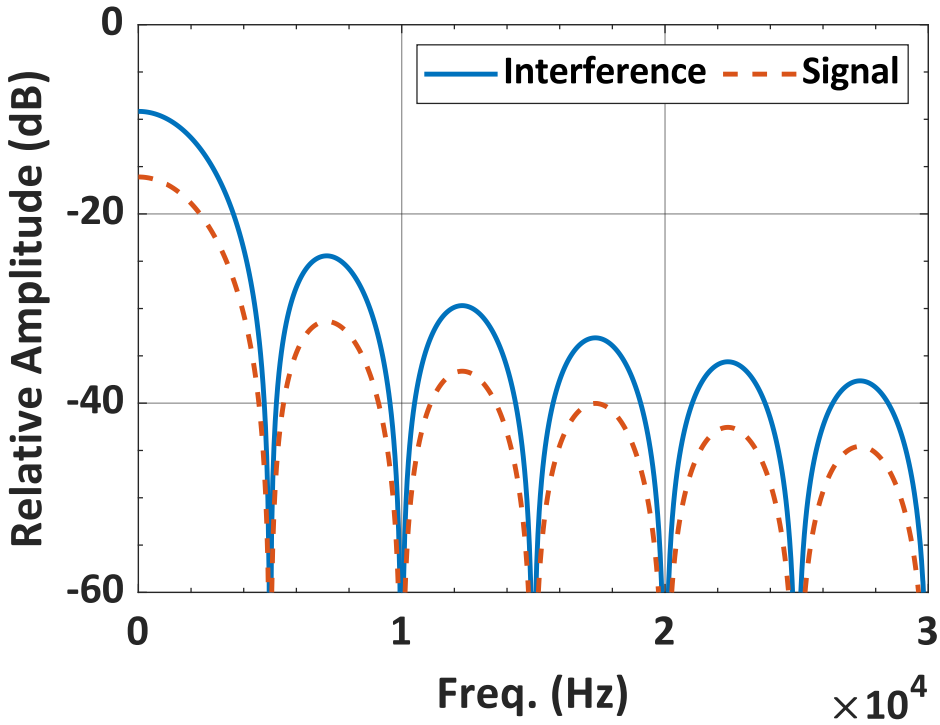


Fig. 3.3. The spectrum shaping of the rectified signal due to bit-level duty cycling for a sampling time of 200us. Both CW-interference and desired signals are shown.

Thus, one method of alleviating the interference dependent offsets is to enable a high dynamic range in the circuitry following the envelope detector, and then add the required offset value to the decision threshold in the comparator stage. Assuming the circuitry following the ED has a sufficiently large dynamic range and neglecting the additional down-converted noise due to interference (out of band interferer case), the ideal maximum possible signal to interference ratio (SIR_{max}) at the input of the ED is given by:

$$SIR_{max} = 5\log(2^{-ENOB}) \tag{3.3}$$

where ENOB is the effective number of bits that represent the comparators decision threshold range. The factor of 5 accounts for the square law detection nature. It should also be noted that the dc offset at the output of the ED can be caused by both CW interference as well as inherent noise self-mixing effects and startup transients, which further contribute to dynamic range degradation.

3.3 IF Channelization in Energy Detection Receivers

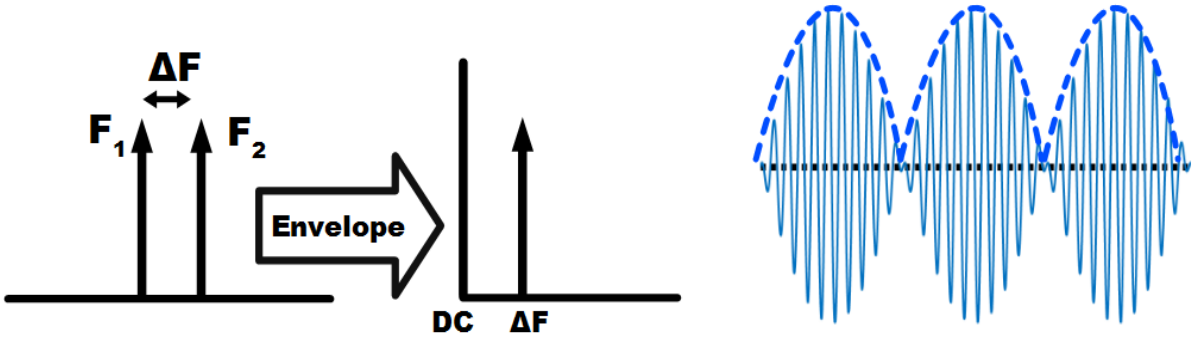


Fig. 3.4. Envelope information of a two-tone RF signal shown in frequency (left) and time domain (right).

The conventional envelope detection rectifies the RF signal directly to dc, where most of the desired signal is concentrated in the vicinity of 0Hz for low bit rates. Direct dc-coupling can suffer from unwanted dc-offsets induced by baseband non-idealities, RF noise self-mixing, and baseband flicker noise. Capacitive coupling can remove dc offsets as mentioned earlier but the required capacitor values can be prohibitively large for low data rate applications. IF channelization provides the flexibility to encode information in various IF channels, and perform bandpass IF filtering to reduce the effects of the rectified interference signals mentioned in section 3.2 as well as systematic dc-offsets and flicker noise issues. To mitigate these issues, this work adopts a multi-tone signaling scheme similar to [38].

The transmitted signal ($v_{RF,2-tone}(t)$) in this scheme comprises of two RF tones spaced by Δf as shown in Fig. 3.4, which can be explained mathematically as the sum of two sinusoids:

$$v_{RF,2-tone}(t) = \frac{A_{RF}}{\sqrt{2}}(cos\,(2\pi f_C t + \varphi_1)\; + cos\,(2\pi(f_C + \Delta f)t + \varphi_2)\,) \qquad (3.4)$$

where the peak-to-peak amplitude is A_{RF}, the carrier frequency is f_C, and φ_1 and φ_2 represent the random phase offsets for mathematical convenience. The resulting output signal upon entering a square law envelope detector can be expressed as:

$$v_{IF,2-tone}(t) = kV_{RF}^2(t) \qquad (3.5)$$

Neglecting the high frequency content at F_{RF} owing to the attenuation at IF with lowpass filtering, the resulting IF tone is expressed as:

$$v_{IF,2-tone}(t) = \frac{kA_{RF}^2}{2}(1 + cos\,(2\pi\Delta f t + \varphi_2 - \varphi_1\,)\,) \qquad (3.6)$$

The transmitted two tones result in rectified energy at DC and intermixing that produces a tone at Δf. The analysis above applies to the non-duty cycled case and a modification is necessary for bit-level duty cycling case. Approximating an instantaneous on-off transition of the RF signal due to duty cycling, eq. (3.6) can be modified as:

$$v_{RF_{BLDC}}(t) = v_{RF}(t)Rect\left(\frac{t}{\tau}\right) \tag{3.7}$$

Using the identity $\mathrm{Rect}^2(X) = \mathrm{Rect}(X)$, we can obtain the low frequency output content of the ED as:

$$v_{IF}(t) = \frac{kA_{RF}^2}{2}(1 + cos\,(2\pi\Delta f t + \varphi_2 - \varphi_1)\,)\,Rect\left(\frac{t}{\tau}\right) \tag{3.8}$$

The frequency domain behavior of (10) can be obtained by the Fourier transform:

$$V_{IF}(f) = \frac{kA_{RF}^2}{2}[\,\delta\,(f) + 0.5 * \delta(f - \Delta f) + 0.5 * \delta(f + \Delta f)] \;*\; \tau sinc(f\tau) \tag{3.9}$$

$$V_{IF}(f) = \frac{\tau kA_{RF}^2}{2} * \left[\, sinc(f\tau) + sinc\big((f - \Delta f)\tau\big)\right] \text{(one sided)} \tag{3.10}$$

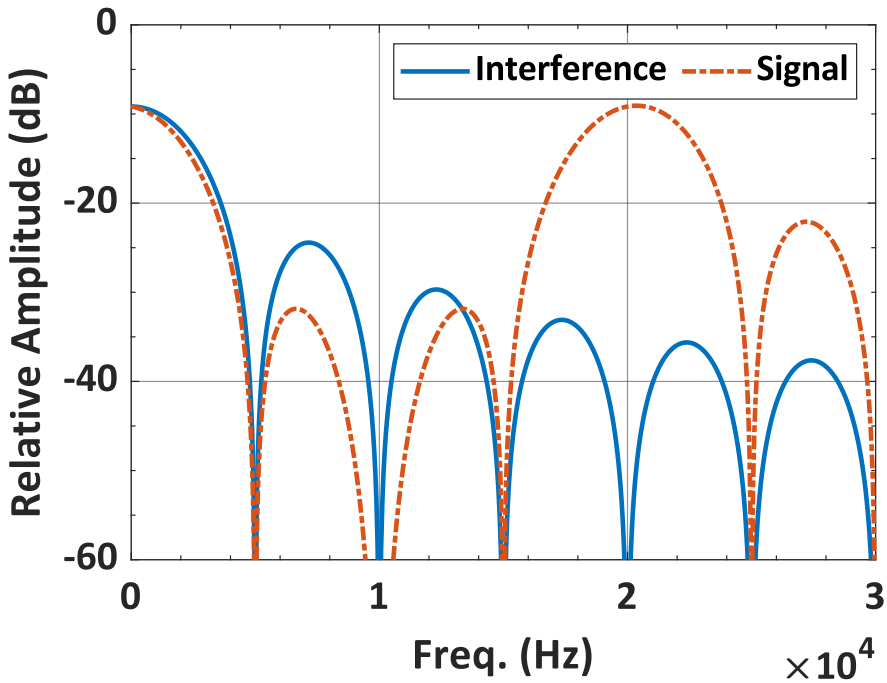
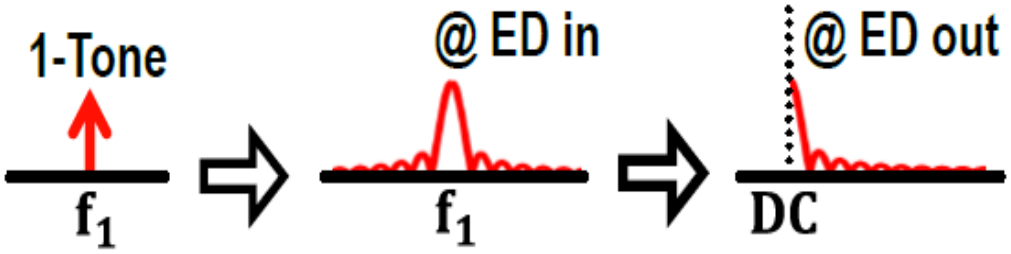


Fig. 3.5. Rectified Signal and Interference spectrum at ED output for BLDC RF sampling time of 200us for a channelized signaling scheme.

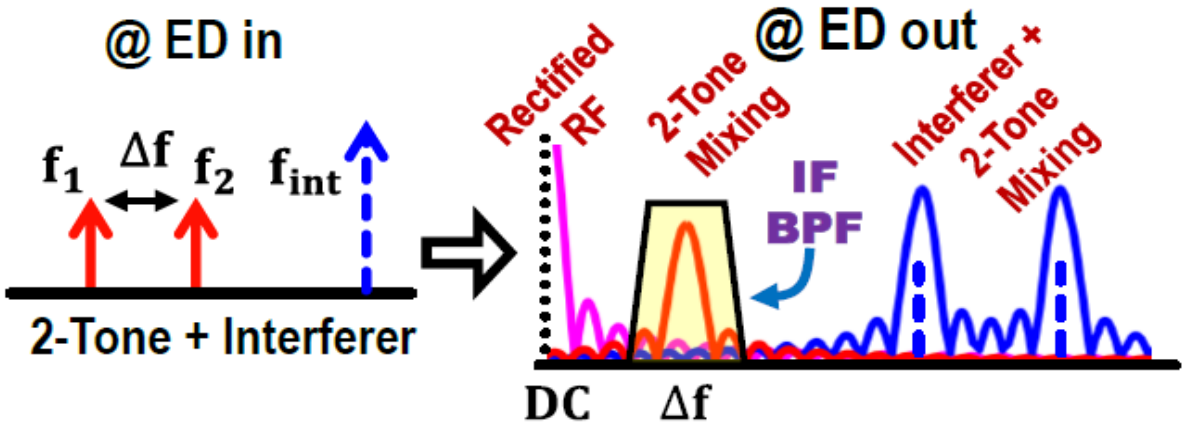
Fig. 3.5 shows the interference spectrum at the ED output for an RF sampling time of 200us for a two-tone signaling scheme. Assuming the multi-tone RF signal is downconverted to 20KHz (tone spacing at RF) in a baseband OOK scheme, the relative interference offset

effect is reduced by a factor of 7.5dB. This is calculated by the area under the main lobe to the 3rd and 4th sidelobes.

Since the wanted signal now lies at an IF, a bandpass filter centered at 20KHz can be used to extract the desired information while suppressing the large offsets near dc. It can also be noted that elongating the RF sampling time to the always-on case is same as the non-duty cycled operation identical to the ED-1st case, where the desired signal at IF, interference, and dc-offset spectrum become impulses. Therefore, further improvement of the SIR can be achieved by either placing the IF signal further from dc, or by selecting a longer RF sampling time to reduce the energy under the sidelobes corresponding to the interference spectrum. An illustration of the single tone case and two-tone case under bit-level duty-cycling is shown in Fig. 3.6 for further clarity.



(a) Single tone case



(b) Two tone case

Fig. 3.6. Single tone and two-tone behavior with bit-level duty cycling

3.4 Circuit Description

3.4.1 RF Frontend

The RF front-end (RFFE) employs active RF gain for high sensitivity and a passive pseudo-differential ED for rectification. The RFFE achieves 64dB measured voltage gain at 40.5μW active power through a combination of a high impedance interface at the CMOS RF ports and a power-efficient regenerative amplifier. The co-designed-impedance interfaces effectively decrease the filter bandwidth from roughly 1MHz to less than 100kHz by utilizing asymmetric capacitive loading on the AlN MEMS filter. This allows for superior close-in interference rejection at RF.

3.4.2 IF and Baseband

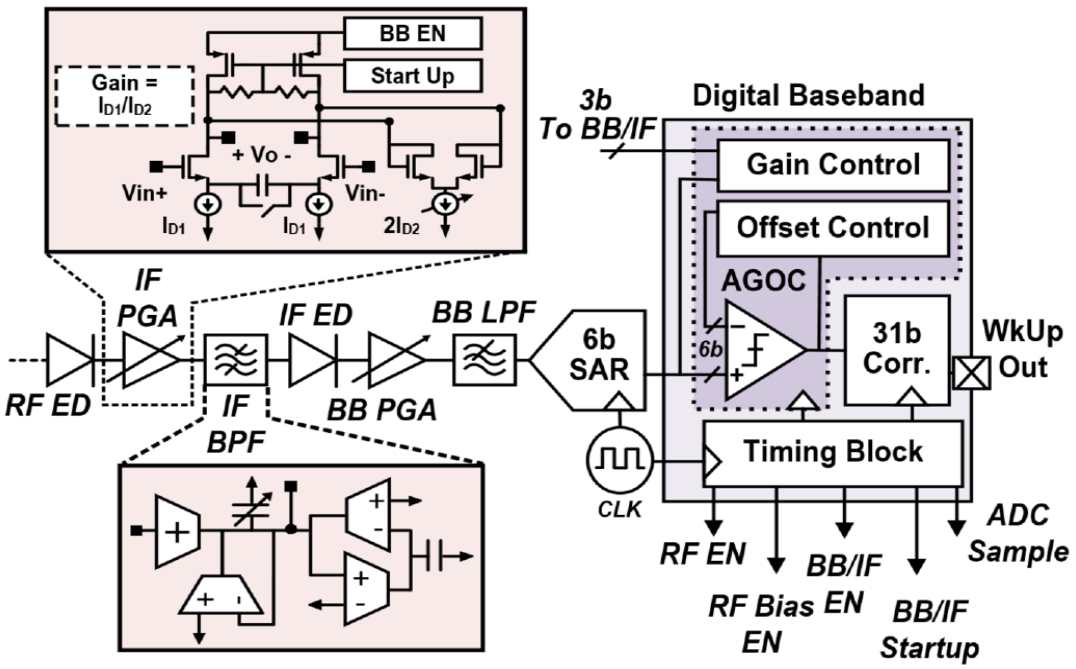


Fig. 3.7. IF and BB chain (left) with digital baseband including comparator, AGOC and timing circuitry (right).

The IF and BB chain (Fig. 3.7) is designed to isolate the resulting post RF-ED intermixing product of the 2-tone signal. The IF signal at the output of the RF ED is amplified with a modified version of the VGA in the prior phase with programmable gain from 24-42dB. The PMOS current sources of the transconductance loading stage are merged with the gain transconductor stage's PMOS headers, which improves the design simplicity as well as the overall noise contribution. The load transconductor have also been switched from a diode

connected PMOS to a diode connected NMOS, and the gain is identical to the design in prior phase.

The amplified IF signal is then filtered with a Gm-C bandpass filter tunable from 55kHz-70kHz with a Q factor of 5, and rectified with a source follower ED. The measured startup time of the IF/BB is ~350us with an active non-duty cycled power consumption of 1μW. The rectified signal is further amplified, filtered, and digitized with 6-bit SAR ADC. The bit decision and automatic offset correction are realized in the digital domain, and the wakeup is detected using a 31-bit correlator. The wakeup receiver is clocked with an on-frequency locked loop-based relaxation oscillator [70].

A 6-bit differential SAR ADC quantizes the baseband output during the RF sampling time. In the digital baseband, the ADC result is compared against a target threshold level to generate a bit decision. An AGOC algorithm is used to adjust the IF/BB gain to keep the threshold level within the ADC's full range. The decision threshold is tuned when observing a desirably low quantity of false positives out of the comparator. Under high interference conditions, the decision threshold can be rapidly adjusted by monitoring the 6-b ADC code and switching to a new threshold based on the ADC value. Similarly, a 1-b ADC requires a longer compensating interval to approach the new threshold. The AGOC ideally can compensate up to 15dB of SIR with the 6-bit SAR ADC and achieves steady-state in five clock cycles. Bit decisions are fed into a 31-bit binary correlator with 5-bit of error tolerance to detect the wakeup signal.

A frequency locked loop (FLL) based 50kHz system clock adopted from [70] using a gate-leakage based current source is integrated on-chip and consumes 20nW. A timing block generated duty-cycling enable signals for the RF, IF/BB, and digital baseband with 12-bits of timing resolution. The bit rates, sampling time, IF center frequency, and baseband bandwidth are all digitally programmable with a SPI interface. The measured dc power of the digital baseband is 38nW at 100bps.

3.5 Measurement Results

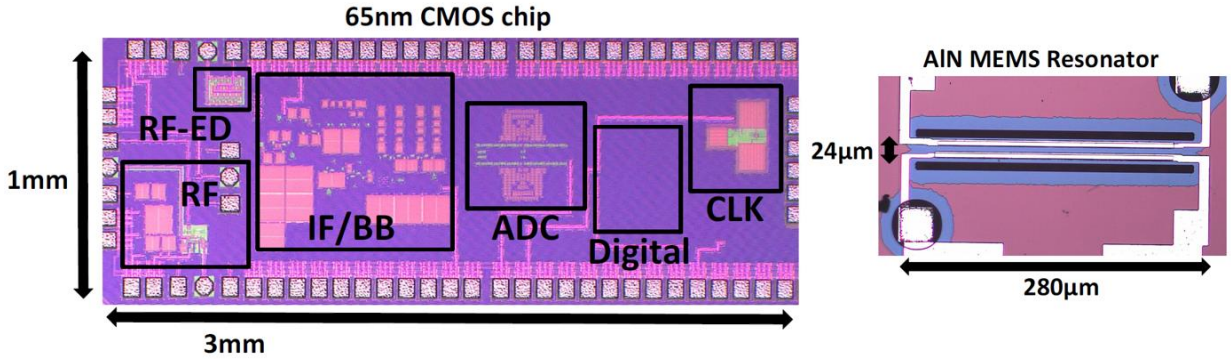


Fig. 3.8. Chip photographs of 65nm CMOS and MEMS resonator

The wake-up receiver is fabricated in TSMC 65nm LP CMOS process, and the Al-N MEMS resonator is fabricated through a custom process. Fig. 3.8 shows die photos of the CMOS and MEMS chips.

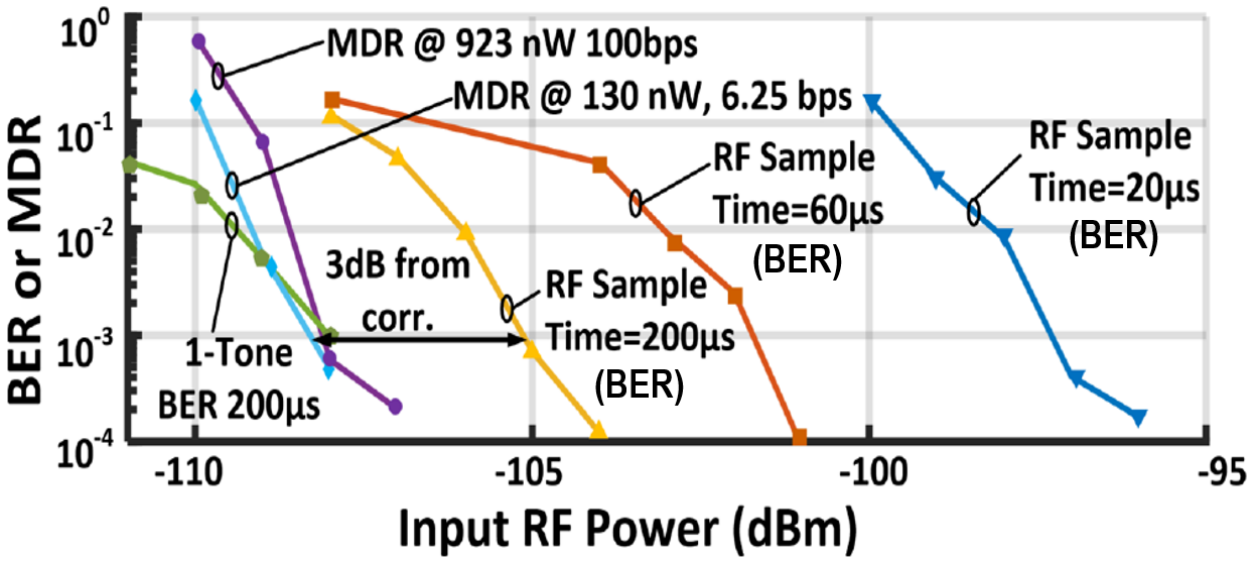


Fig. 3.9. Measured MDR and BER performance. Increasing the RF sampling time improves the sensitivity and lowering the data rate reduces average WuRx power

Fig. 3.9 shows the measured receiver performance 0.1% Missed-Detection-Ratio (MDR) and Bit-Error-Ratio (BER) using a PRBS9 sequence. The measured false alarm rate was less than 1 per hour.

The wake-up receiver achieves the best case MDR sensitivity of -108dBm and bit-error ratio (BER) sensitivity of -105dBm at 130nW dc power with RF sampling time of 200µs for 6.25bps in 2-tone mode. The BER sensitivity is unchanged when the data rate is increased from 6.25bps to 100bps, for an increment in dc-power from 130nW to 923nW. To show the

sensitivity and dc power trade off, the data rate is kept at 100bps, while the sample time is reduced from 200µs down to 60µs and 20µs, resulting in a reduction in dc power from 923nW, 363nW, and 243nW, respectively. This results in a BER sensitivity degradation from -105dBm to -102dBm and -97dBm respectively.

The broad operating space of the receiver is supported by measuring the tradeoffs of data rate, sensitivity, and dc power in 2-tone RF OOK mode for 3 different bit rates (10,100,1000 bps) and 3 different RF sampling times (20,60,200 µs). A plot of the measured 3-dimensional tradeoff space is shown in Fig. 3.10.

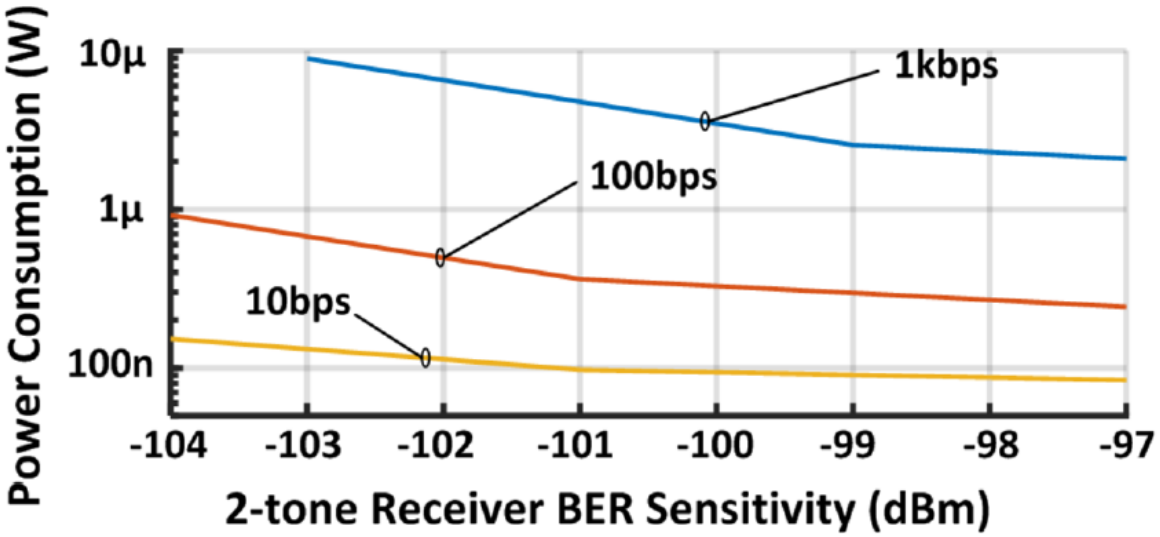


Fig. 3.10. Measured sensitivity, dc power, and data rate trade space.

In the 2-tone mode, the wake-up receiver demonstrates tunability of 11dB in sensitivity (-108dBm to -97dBm), 410x in dc power (100nW to 41µW), and 672x in data rate (6.25bps to 4.2kbps). Alternatively, using the receiver in a conventional single tone OOK mode for data reception shows a maximum data rate of 4.2kbps at a BER sensitivity of -108dBm and 41µW dc-power consumption. This indicates that the receiver can function as either a wake-up receiver or a low-data rate receiver.

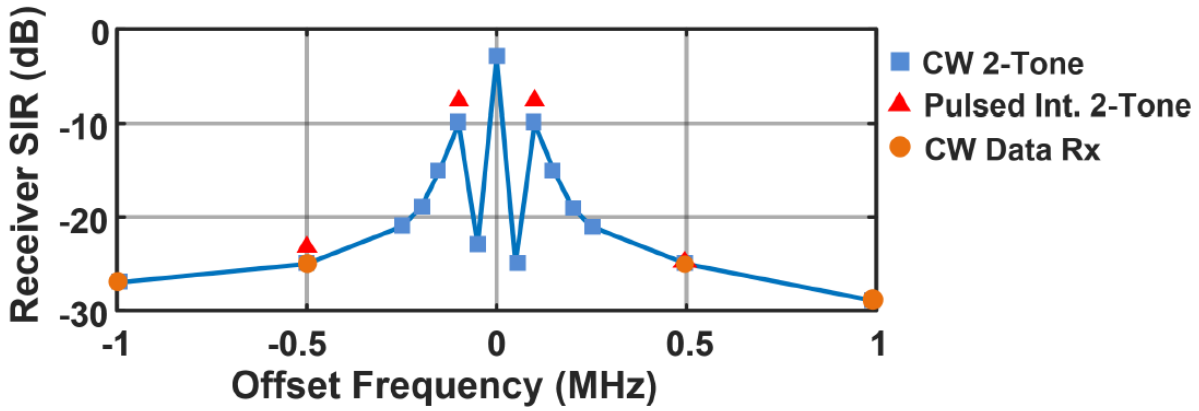


Fig. 3.11. Measured signal to interference ratio (SIR) with multiple interferer types as well as single tone mode with duty cycling disabled for reference.

The measured interference performance of the wake-up receiver is shown in Fig. 3.11. Owing to the combination of two-tone method and high Q MEMS filter, a signal to interference ratio (SIR) of -28dB at 1MHz offset is achieved. The overall wake-up receiver performance is summarized in table 3.2 along with previous state-of-the-art work. Fig. 3.12 shows the wake-up receiver Figure of merit versus the CW-SIR to highlight the improvements of this work.

Table 3.2. Comparison Table of this work with prior state-of-the-art

		This Work			Phase 1	RFIC '19	ISSCC '18	ISSCC '17	ISSCC '16
Key Techniques		2-Tone/MEMS/ADC			Bit-lvl TRF	An. Corr.	ED First	TRF/Ant	2-Tone TRF
Wake-up/Data		Wake-up + Data			Wake-up	Wake-up	Wake-up	Data	Data
Dyn. Range	Sensitivity (dBm)	-97→ -108 (11dB)			-103→ -106	N/A	N/A	N/A	N/A
	Data Rate (bps)	6.25→ 4.2k (672x)			3→ 62.5	N/A	N/A	N/A	N/A
	DC Power (nW)	100→ 41,000 (410x)			33→ 288	N/A	N/A	N/A	N/A
	Samp. Time (µs)	20→ 200 (10x)			N/A	N/A	N/A	N/A	N/A
Close-In: CW SIR (dB)		-25 dB @ 0.12%			N/A	N/A	-27 @ 0.1%	-18 @ 0.3%	-2.5 @ 0.1%
Far-Out: CW SIR(dB)		-28 dB @ 0.7%			-16 @ 0.7%	-30 @ 0.7%	-30 @ 2.0%	-27 @ 1.1%	-2.5 @ 0.3%
Close-In: NCE SIR (dB)[1]		-25 dB @ 0.12%			N/A	1.1 @ 0.7%	-4 @ 2.0%	N/A	N/A
Carrier Freq. (MHz)		430			428.6	450	151.8	915	915
Technology (nm)		65			65	65	130	180	65
Die Area (mm^2)		3			3.95	0.6	1.95	2.67	0.225
Mode		Low P_{DC} (2-Tone)	Low Lat. (2-Tone)	Data Rx (1-Tone)					
Sensitivity (dBm)		-108[2]	-108[2]	-108[3]	-106[2]	-80.9[2]	-76[2]	-93[3]	-76[3]
Power (nW)		130	923	41,000	33	40	7.4	1,850,000	135,000
Data Rate (bps)		6.25	100	4,200	3	100	200	62,500	10,000
Sampling Time (µs)		200	200	240	100	10,000	5,000	16	100
FOM (dB)		170[4]	173[4]	188[5]	173.8[4]	160[4]	165[4]	168[5]	154[5]

1: Non-Constant Envelope (NCE) OOK Modulated Interferer 2: 10^{-3} Missed Detection Ratio (MDR)
3: 10^{-3} Bit Error Ratio (BER) 4: MDR FOM 5: BER FOM

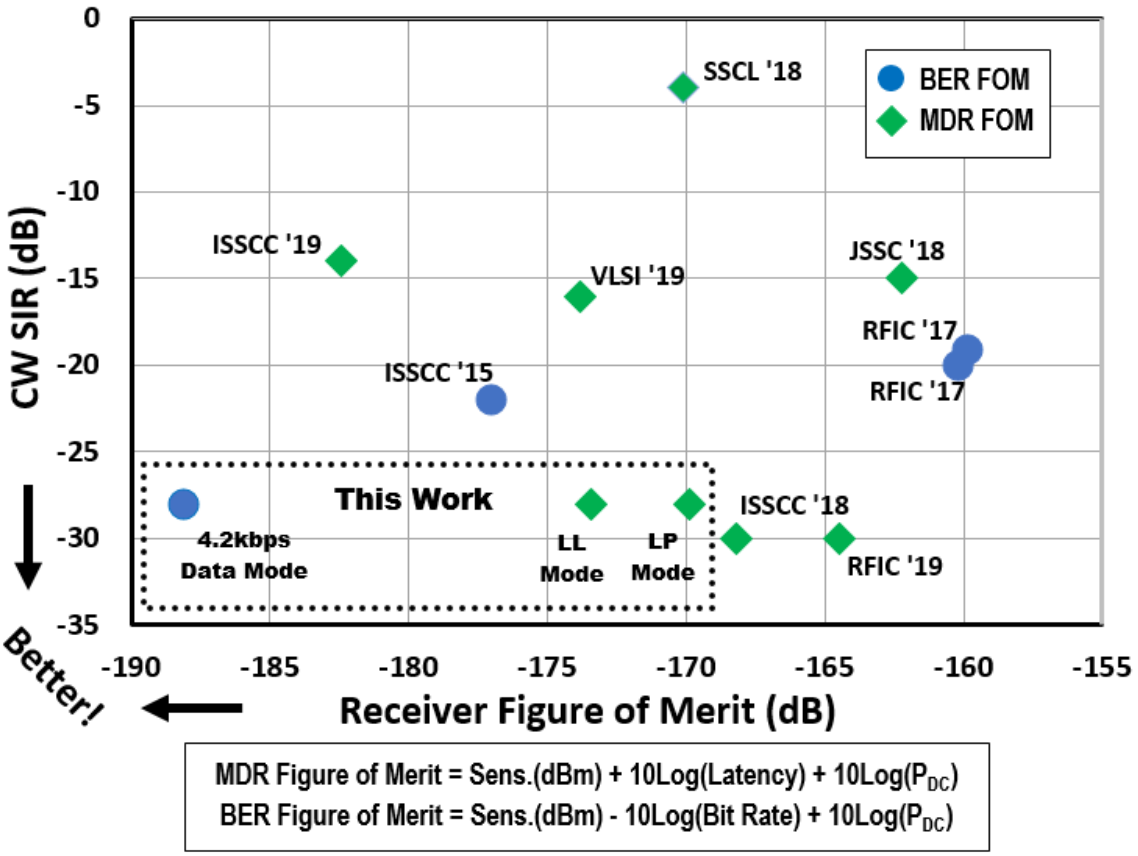


Fig. 3.12. Comparison of WuRX Figure of merit vs. CW SIR with existing sub 100µW receivers.

3.6 Conclusion

The first phase of the bit-level duty-cycled T-RF architecture achieved high sensitivity and nano-watt power but was limited in the dynamic range afforded by the bit-level duty-cycling. The second phase of the research improves upon these limitations by demonstrating a highly scalable 430MHz 65nm CMOS Al-N MEMS co-integrated wake-up receiver prototype employing bit-level duty cycling and 2-tone OOK RF signaling. A -108dBm of maximum sensitivity is achieved for a 130nW minimum dc-power at 6.25bps, which is ideal for low power wide area networks (LPWAN) spanning several kilometers with relaxed latency requirements. The wake-up receiver is fully digitally programmable between 130nW to 41µW dc power and 6.25bps to 4.2kbps. Close-in SIR of -25dB and far-out SIR of -28dB allows for robust operation in a spectrum crowded environment. Dynamic ranges of 11dB, 410X, 672X are achieved for sensitivity, power, and latency, which enable high post-fabricated tunability and firmware programmability after deployment in a network.

3.7 Personal Contributions

- Co-lead the system architecture and RF signaling method selection efforts.
- Lead the baseband design efforts including the programmable gain amplifier chain, IF envelope detector, and bandpass filter.
- Assisted the ADC design efforts.
- Co-Lead the full system testing and characterization efforts.
- Co-lead the conference manuscript preparation.

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University of Illinois Urbana Champaign: Ruochen Lu, Anming Gao, Songbin Gong.

Chapter 4

4. Sub-GHz T-RF Wake-up Receiver Phase 3: High Integration Factor and Multi-Channel

The prior two generations of the bit-level duty cycled T-RF wake-up receivers demonstrated that better than -106dBm sensitivity can be achieved for tens to hundreds of nano-watt level power levels. However, this required the adoption of bulky off-chip MEMS, which raise the integration size and cost for the overall sensor node. Furthermore, prior wake-up receiver solutions (including the ED-1st) have been unable to provide multichannel operation, which limits the spectrum efficiency and node density. Multi-channel operation typically requires either a power hungry PLL or a multi-tone transmission scheme. Moreover, the high Q-factor of the front-end MEMS required for improved sensitivity can limit the multi-channel operation due to limited bandwidth and center frequency tunability. The third phase of sub-GHz T-RF research addresses these issues and demonstrates a prototype wake-up receiver with -99dBm sensitivity at 260nW without MEMS. This work also demonstrates multichannel operation with a single-tone based channel-embedded OOK (CE-OOK) signaling method.

4.1 Channel Embedded On-Off-Keying (CE-OOK)

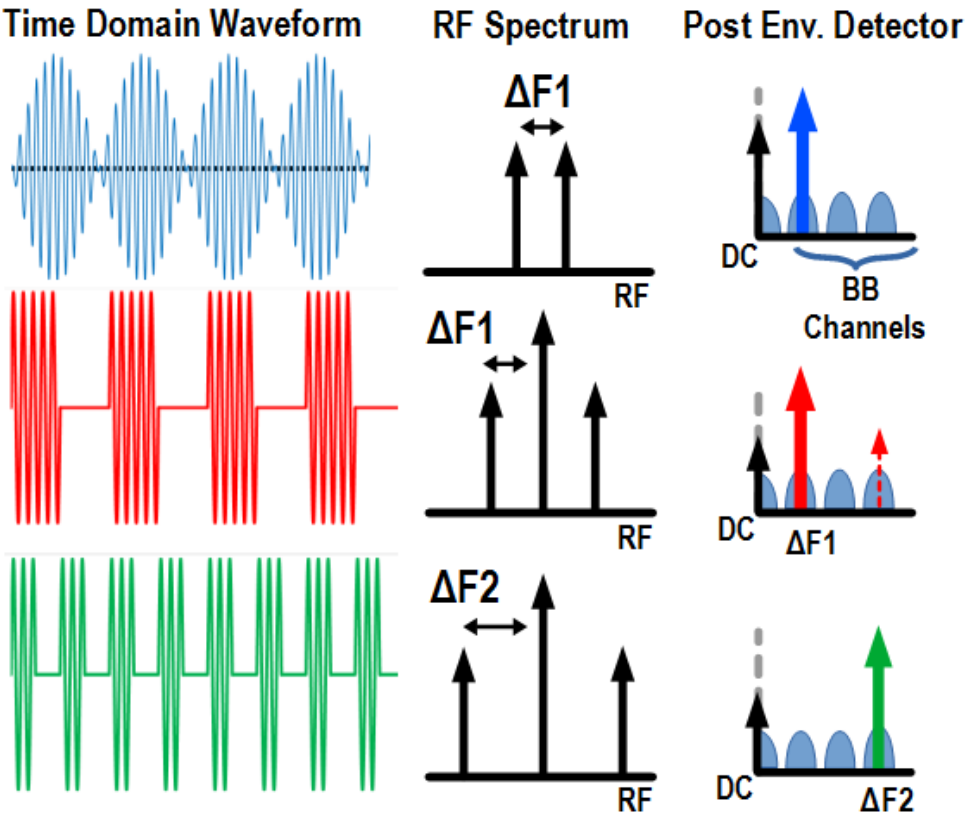


Fig. 4.1. Two tones rectification (top). CE-OOK: Slow OOK rates produce lower IF content (middle) and faster OOK rates produce higher IF content (bottom).

The multi-tone method explained in the chapter 3 can generate an IF signal, but this requires some complexity to be added to the transmitter due to the non-constant wave (NCW) output. An alternate method termed "Channel-Embedded On-Off-Keying" (CE-OOK) to generate an IF tone with a transmitter capable of the conventional single tone OOK signaling is shown in Fig. 4.1. The CE-OOK utilizes an OOK modulated single tone to represent the IF symbol. This can be mathematically modelled as below:

$$v_{RF,CE-OOK} = A_{RF}\, cos\,(2\pi f_C t)[Sq(t) + 1] \tag{4.1}$$

$$Sq(t) = \frac{\pi}{4}(sin\,(2\pi f_\Delta t)\; + \frac{1}{3} sin\,(3 \cdot 2\pi f_\Delta t)\; + \frac{1}{5} sin\,(5 \cdot 2\pi f_\Delta t)\; + \cdots] \tag{4.2}$$

where Sq(t) is the mathematical representation of a square signal with an amplitude of 1 and f_Δ being the frequency of the square wave. Note that the expression above also assumes an infinitely long symbol sequence for the convenience of computation. This condition approximates the case where symbol rate is much slower than the modulation rate.

Replacing variables $2\pi f_C t = \omega_1$ and $2\pi f_\Delta t = \omega_2$, expanding the terms in Sq(t), cross multiplying with $\cos(2\pi f_C t)$, and simplifying to sinusoids using trigonometric identities produces:

$$v_{RF,CE-OOK} = A_{RF}\left(cos(\omega_1) + \frac{2}{\pi}sin(\omega_2 + \omega_1) + \frac{2}{\pi}sin(\omega_2 - \omega_1) + \frac{2}{3\pi}sin(3\omega_2 + \omega_1) + \cdots\right)^2 \quad (4.3)$$

Rectification of the above signal with an ideal square law envelope detector and filtering out the high frequency terms due to the band-limited baseband produces the following result in eq. (4.4),

$$v_{IF,CE-OOK} = A_{RF}^2\left(\frac{4}{\pi}sin\,(2\pi f_\Delta t) + \frac{4}{3\pi}sin\,(3\cdot 2\pi f_\Delta t) + \cdots\right) \quad (4.4)$$

where the odd order harmonic content beyond the 3rd harmonic are not shown. Note that these harmonic contents attenuate as the frequency extends from dc.

The result above in eq. (4.4) can also be intuitively derived by considering that an ideal envelope detector fed with a square envelope modulated signal must produce the corresponding baseband square wave. (Assume the bandwidth of the envelope detector is large enough to capture the harmonic content making up the square wave, but small enough to suppress the RF content.) The Fig. 4.1 illustrates a two-tone signal and CE-OOK signal with two different modulation rates producing differing IF content.

The eq. (4.4) for a CE-OOK baseband signal shows that it can provide a $\frac{4}{\pi}$ times (or +2dB) higher voltage conversion gain compared to the eq. (3.6) for a two-tone modulated case for the same peak amplitude of the input RF signal. This is advantageous if the transmitter is limited by the peak output power due to local regulations or power amplifier constrains. The penalty paid for adopting the CE-OOK method over a two-tone method is that CE-OOK requires sharper bandpass filters at the IF to suppress the higher odd order harmonic content of the square baseband envelope. Since this filtering occurs at the IF, it can be easily achieved with low dc-power.

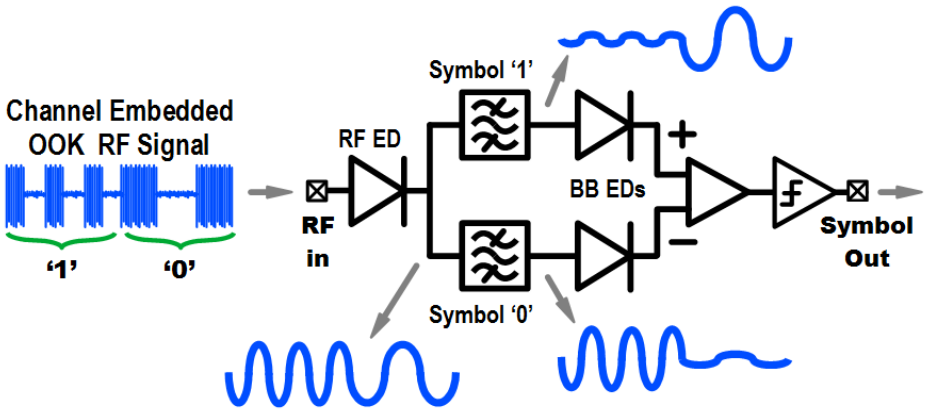


Fig. 4.2. Demodulation method for CE-OOK encoded with baseband 2-FSK scheme.

Given the versatility of CE-OOK for the IF channelization purposes, the SIR advantage can be further improved by adopting a baseband binary frequency shift keying (BFSK) scheme where both 0 and 1 symbols are transmitted and down-converted to different IF as shown in Fig. 4.2.

The spectrum shaping effect due to BLDC warrants attention in the BFSK case to accurately determine the channel selection filter requirements. The behavior of the BFSK case can be plotted using the expressions derived in chapter 3 using the two-tone approximation for mathematical convenience.

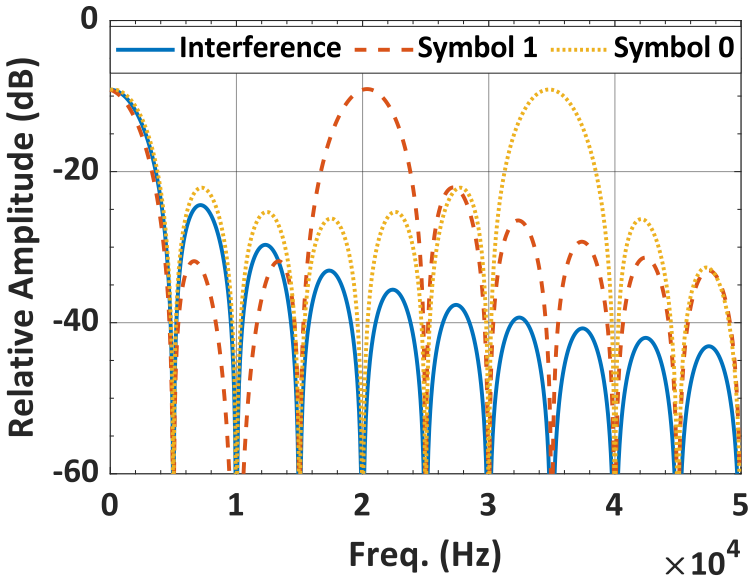


Fig. 4.3. Rectified Signal and Interference spectrum at the ED output for a BLDC sampling time of 200us for a baseband 2-FSK scheme

The output spectrum is plotted in Fig. 4.3 for IFs of 20K and 35KHz. A certain amount of interference energy now becomes common mode to both symbols and can be suppressed by

taking the difference of relative power. The integrated interference power corrupting the 20KHz IF tone is only 2.5dB stronger than that of the 35KHz IF tone. This means tht the interference would cause a 2.5dB higher dc-offset in 20KHz IF path compared to 30KH IF path. A relative power comparison scheme, such as the one shown in Fig. 4.2, can reject the majority of common mode interference energy assuming a sufficiently linear baseband following the RF envelope detector.

4.2 Wake-up Receiver Architecture and Measured Results

The proposed wake-up receiver shown in Fig. 4.4 uses a bit-level duty cycled T-RF topology similar to the prior two phases for high sensitivity at low average dc power [71]. The CE-OOK modulated RF signal is used to encode the wakeup message with both '1' and '0' symbols, creating an IF BFSK waveform as explained before.

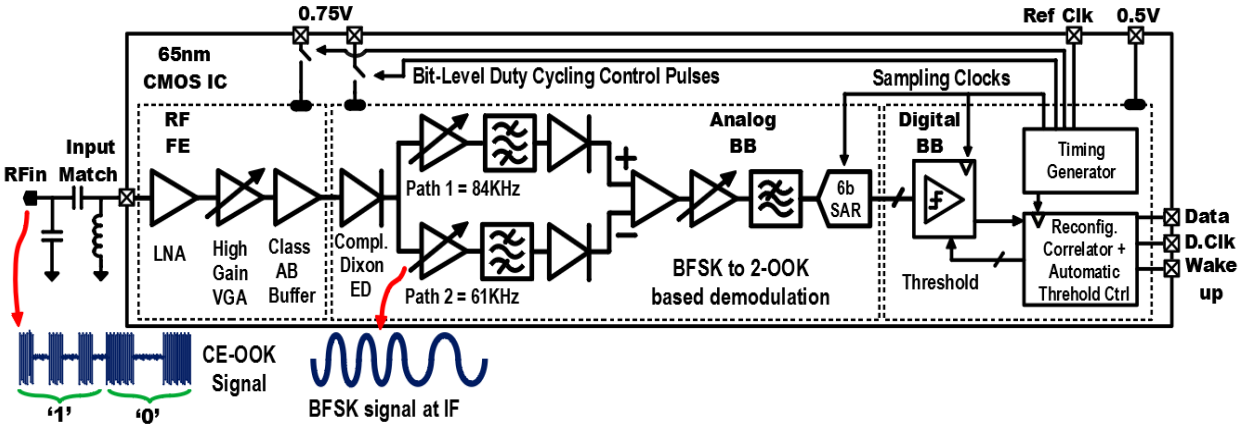


Fig. 4.4. Block diagram of the MEMS-less wake-up receiver

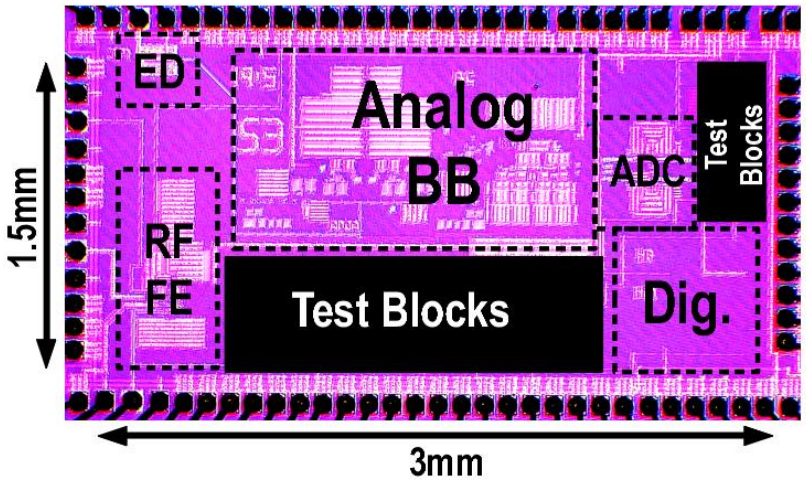


Fig. 4.5. Chip Photograph

The CE-OOK RF signal is first amplified with a high gain RF frontend (RFFE) consuming 50.3µW of instantaneous power for a 61dB simulated gain using a cascade of regenerative ring amplifiers adopted from [69]. The CE-OOK RF signal is then down-converted with a passive triode mode Dickson envelope detector, where both the symbols '0' and '1' are down-converted to their respective IFs. This IF BFSK signal is then fed to a symbol detecting IF block consuming 2.1µW dc-power with two parallel bandpass filters tuned to each of the sub-carrier channel. The symbol filters are digitally tunable and implemented using the Gm-C bandpass topology. The measured results show 9dB suppression for the opposite symbol channel. The rectified voltage in each of the IF paths is then compared against each other and digitized with a 6-bit SAR ADC. The resulting 6-bit value is digitally compared against a target threshold to issue a bit decision. A 64-bit reconfigurable correlator with programmable error tolerance is used to detect the wakeup code. A programmable timing generator provides dedicated duty cycling pulses to both RFFE and analog BB for optimum power saving.

The WuRX was fabricated in the TSMC CMOS 65nm LP process occupying 4.5mm^2 as shown in Fig. 4.5. The measured dc-power consumption of various circuit blocks are shown in table 4.1. The power consumption for a 400µs RF sampling time and various bit rates are also shown to highlight the dynamic range in latency and power.

Table 4.1. Measured dc-power consumption for various bit rates at RF sampling time of 400µs

	RF (nW)	BB (nW)	Dig. (nW)	Total (nW)
Always on	50325	2138	40	52503
1kbps	19973	1050	40	21063
500bps	10080	578	40	10698
100bps	2003	129	40	2172
10bps	201	19	40	260

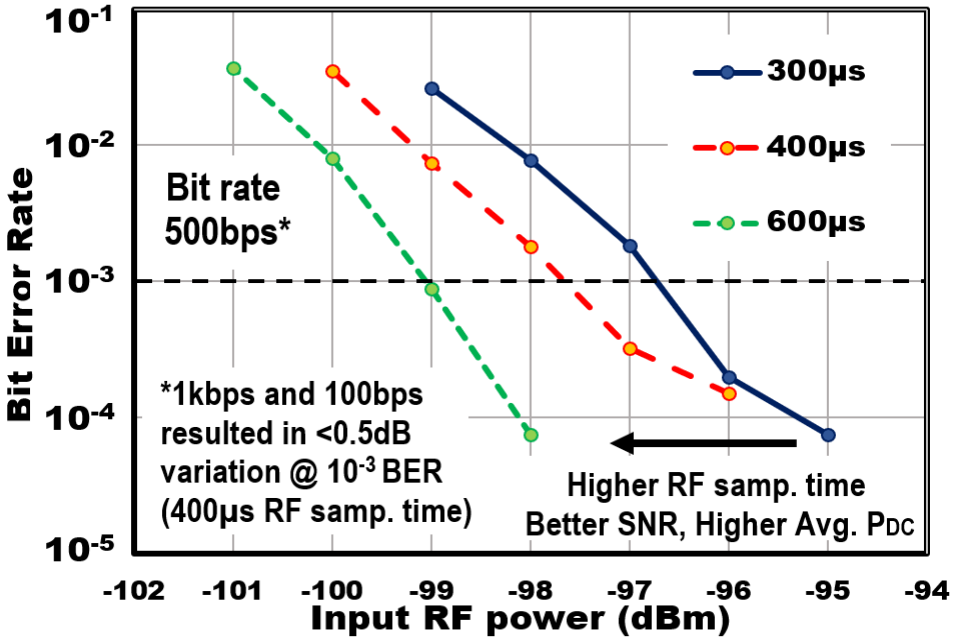


Fig. 4.6 Measured bit error ratios for various RF sampling times

Fig. 4.6 shows the measured bit error ratios (BER) for three RF sampling times at 500bps using a PRBS9 sequence with the automatic threshold control setting the optimum decision threshold. Measurements at 1kbps and 100bps show BER curves within 0.5dB variation at a 400µs RF-sampling time, all at better than -97dBm BER sensitivity.

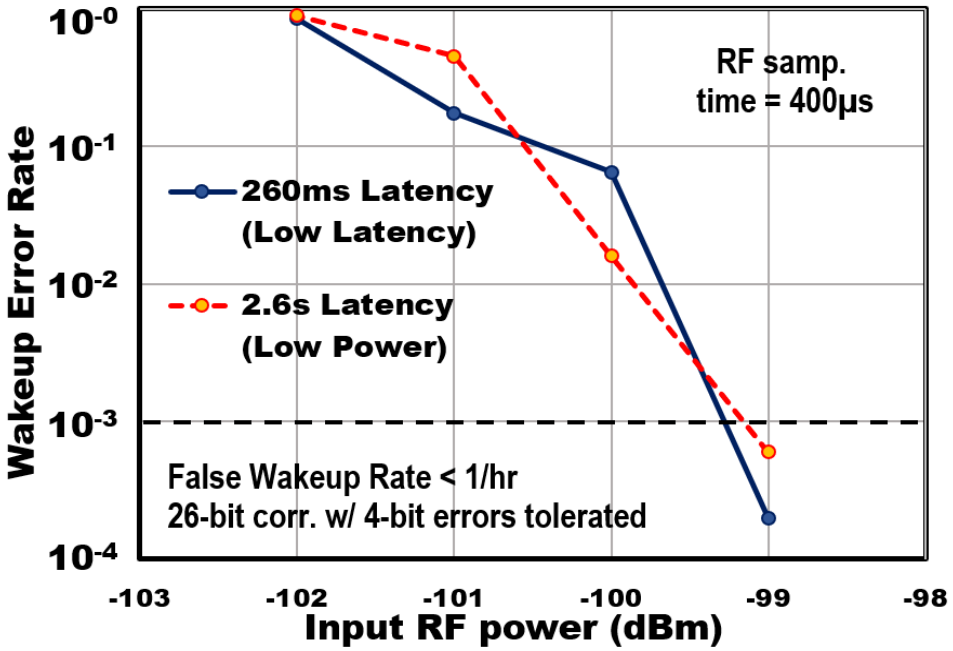


Fig. 4.7. Measured wakeup error ratios for low power and low latency modes

Fig. 4.7 shows the measured wakeup error rates (WER) at a 0.1% missed detection rate with less than 1 false positive per hour, using a 26-bit wakeup code made of cascaded 13-bit Barker codes. The wake-up receiver achieves a wakeup sensitivity of -99 dBm for 260ms and 2.6s latency, at total average dc power of 2.17uW and 260nw respectively.

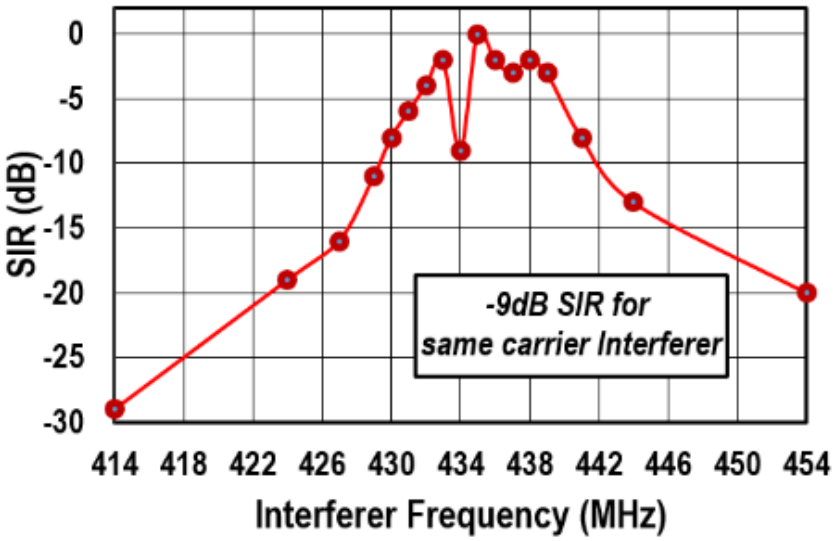


Fig. 4.8. Measured signal to interference ratio

The signal to interference ratio (SIR) shown in Fig. 4.8 is measured with the desired signal 3dB above the sensitivity level at 500bps and 400µs sampling time. The same carrier-frequency interference yield a -9dB SIR due to the virtue of CE-OOK signaling method.

Multichannel Wakeup test w/ 5000 wakeups

Wakeup message embedded on	Percentage wakeups when RX is configured to listen on: Ch. pair A	Ch. pair B
Ch. pair A	100%	0.2%
Ch. pair B	0%	100%

Test Settings
- Same correlator code for all 4 tests
- RF signal: 434MHz, -98dBm
- Ch. pair A = 61kHz , 84KHz
- Ch. pair B = 88kHz , 113KHz

Fig. 4.9. Measured multichannel performance with 5000 wakeups using different CE-OOK channel pairs.

Multichannel operation is demonstrated in the low latency mode by first defining channel-pair A (61/84 kHz) and B (88/113 kHz) and a shared wakeup code. The wake-up receiver is tuned to the channel-pair A and 5000 wakeups are sent over channel-pair A followed by B. Next, the wake-up receiver is tuned to the channel-pair B followed by the same test. A maximum false wakeup rate of 0.2% is observed when the receiver listens with the alternate channel pair, while receiving 100% of intended wakeups in both cases as shown in Fig. 4.9.

Table 4.2. Comparison with other duty cycled TRF work. This WuRX achieves comparable Sens. to w/ MEMS WuRX while providing multichannel operation.

	This Work		2019 VLSI			2019 JSSC		2020 CICC	
Multichannel	Yes		No			No		No	
MEMS	No		Yes			No		Yes	
Carrier Freq.	434MHz ISM		428.3MHz			413-419MHz		430 MHz	
Mode	Low power	Low Latency	LPHS	LLHS	LPLL	1k	10k	Low power	Low Latency
Sensitivity (dBm)	-99		-106		-103	-79	-74	-108	
Data rate	10bps	100 bps	-	-	-	1kbps	10kbps	6.25 bps	100 bps
Latency	2.6s	260ms	5s	240ms	240ms	-	-	5s	310ms
DC power	260nW	2.17µW	33nW	288nW	161nW	42µW	92µW	130nW	923nW
SIR	-9dB @ 0MHz, -3dB @ 3MHz		-16 dB @ 3MHz			-20dBm @ 1m far from RX ant.		-28 dB @ 3MHz	
Technology	65nm		65nm			180nm		65nm	
Area (mm2)	4.5		3.95			5.29		3	

Table 4.2 shows the performance summary of the prototype wake-up receiver against prior the phases as well as another MEMS-less bit-level duty cycled T-RF receiver. Fig. 4.8 shows a comparison of the sensitivity with state of art sub-µW work showing an 18dB sensitivity improvement compared to prior MEMS-less wake-up receivers.

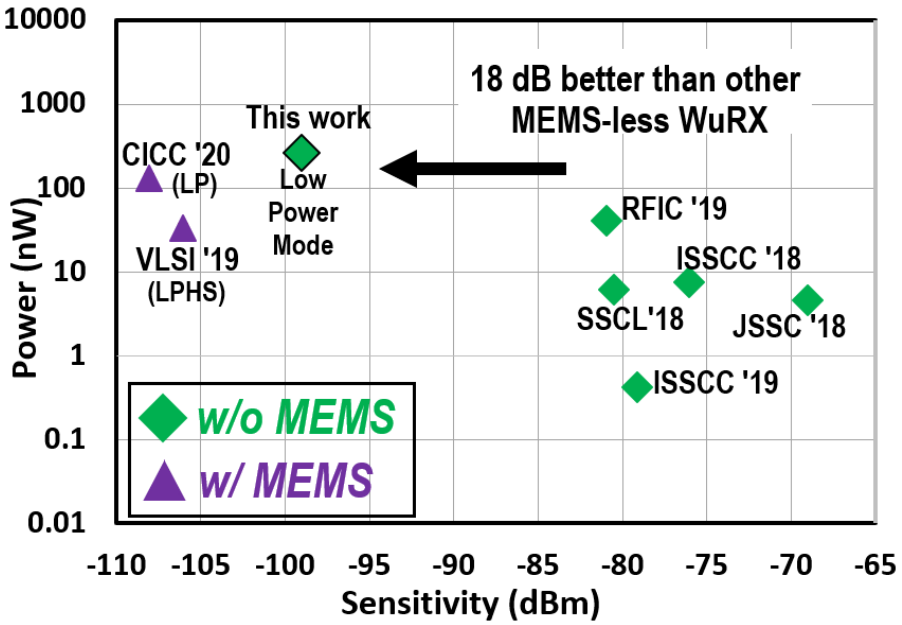


Fig. 4.10 Comparison with state of art shows an 18 dB improvement over MEMS-less WuRX

4.3 Conclusion

Prior two phases of the bit-level duty cycled T-RF research work demonstrated high sensitivity of better than -106dBm with high dynamic range of the sensitivity, power, and latency. But these prior phases adopt custom MEMS resonators, which adds to the integration complexity and impose limitations on the spectrum efficiency due to the high Q factor. The third phase of T-RF work demonstrates that the T-RF architecture can operate with sensitivities near -100dBm (-99dBm in this work) by trading off dc-power required for high RF gain while maintaining stability.

However, the omission of the MEMS resonator prior to the envelope detector results in a high dc-offset due to the RF noise self-mixing effect. To alleviate this, an envelope modulated RF signal scheme called Channel Embedded On-Off-Keying (CE-OOK) is adopted to create IF content at the output of ED. This allows bandpass filtering at IF/baseband stages to overcome dc-offset issues due to the noise self-mixing. The fabricated prototype of MEMS-less wake-up receiver achieves -99dBm sensitivity at 260nW with multichannel operation using the proposed CE-OOK signaling at 2.6s latency, an 18dB improvement over prior MEMS-less work.

4.4 Personal Contributions

- Lead the system architecture and design integration efforts.
- Proposed the CE-OOK signaling method as an IF channelization technique.
- Lead the baseband design efforts.
- Lead the system testing efforts.
- Lead the conference manuscript writing efforts.

Acknowledgements

University of Virginia: Henry Bishop, Daniel Truesdell, Shuo-Li, Benton H. Calhoun, Steven M. Bowers.

Chapter 5

5. 2.4GHz Near and Sub-μW Wake-up Receivers

5.1 Introduction

Ultra-low power receivers at 2.4GHz industrial scientific and medical (ISM) band has gained wide attention in the recent literature. This can be attributed to the widespread popularity of the free to use standards such as Wi-Fi, Bluetooth, Bluetooth Low-Energy (BLE), and Zigbee. One major advantage of the multi-GHz operation is that the physical antenna area can be made considerably smaller [23], which reduces the node volume. Moreover, the path-loss given in Table 1.1 (Chapter 1) shows that the range difference between 434MHz and 2.4GHz in severely obstructed in-building case is much lower compared to the free-space case. Considering these reasons, the 2.4GHz band has found wide applicability in short to mid-range networks spanning several meters to hundreds of meters in obstructed areas such as home and office networks.

A design space analysis of the published work from 2010 to 2020 shows several interesting trends [19]. The dc-power versus sensitivity distribution shown in Fig. 5.1 shows that most high-sensitivity receivers near -100dBm consume hundreds of micro-watt dc-power. The sub-micro watt work in the same Fig. has achieved either poor sensitivity or poor latency (data rate) performance. Regardless of the operating frequency, maintaining operational lifetime of several years require sub-μW receiver solutions, if the available dc-power is limited by the battery replacement cost or the energy harvester area.

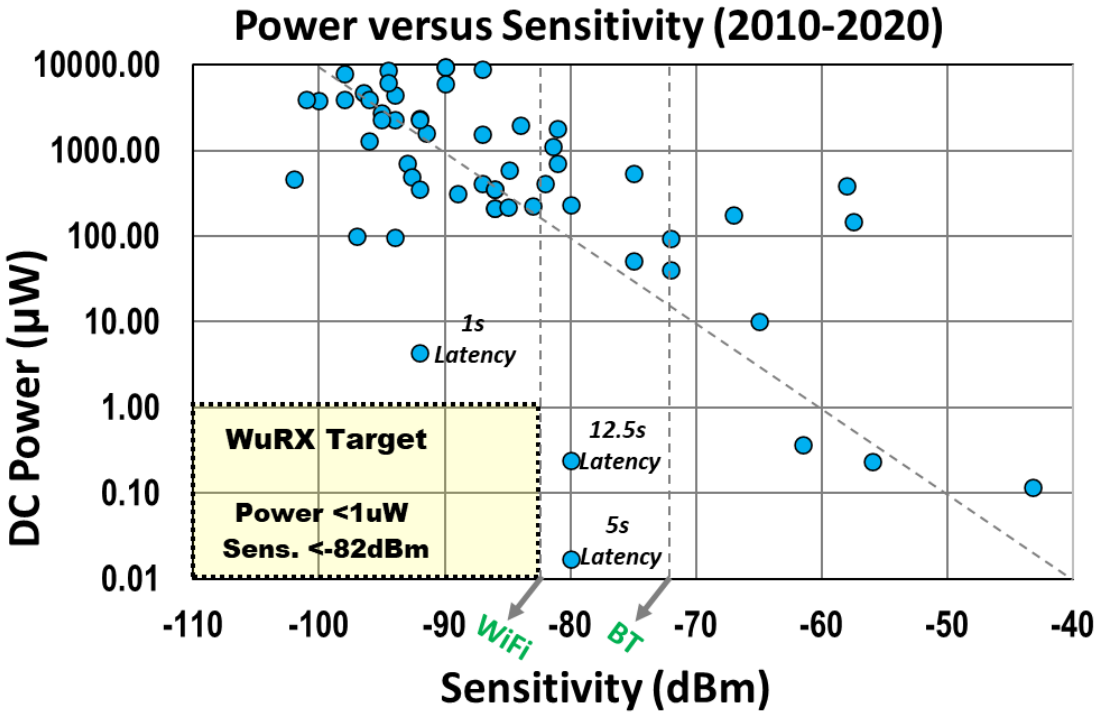


Fig. 5.1. Power versus Sensitivity of 2.4GHz receivers between (2010-2020)

The Bluetooth standard operate with sensitivities between -70dBm to -82dBm but the commercial receivers achieve sensitivities near -95dBm or better [15, 16, 72]. Similarly, Wi-Fi standards also require a maximum sensitivity of -82dBm [52], but the industrial solutions demonstrate better than -90dBm sensitivity [57, 58]. One recent 2.4GHz academic wake-up receiver solution achieved both BLE/WiFi compliant -92/-90dBm sensitivity operation at 4.4µW, but at 1 second latency [62]. Given the crowded nature of the spectrum at the 2.4GHz band, it is highly desirable to realize sub-µW operation at sub-second scale latency for an efficient spectrum usage. Another wake-up receiver achieved an impressive dc-power consumption of 17nW, but this also came at a longer latency of 5s [50]. Considering the stringent sensitivity, power, and latency requirements, designing for a **sub-µW dc-power, sub-1s latency, and better than -90dBm wake-up receiver at the 2.4GHz ISM band** provides a reasonable design target for short to mid-range wake-up receivers. However, the results in Fig. 5.1 shows clear lack of solutions in this space.

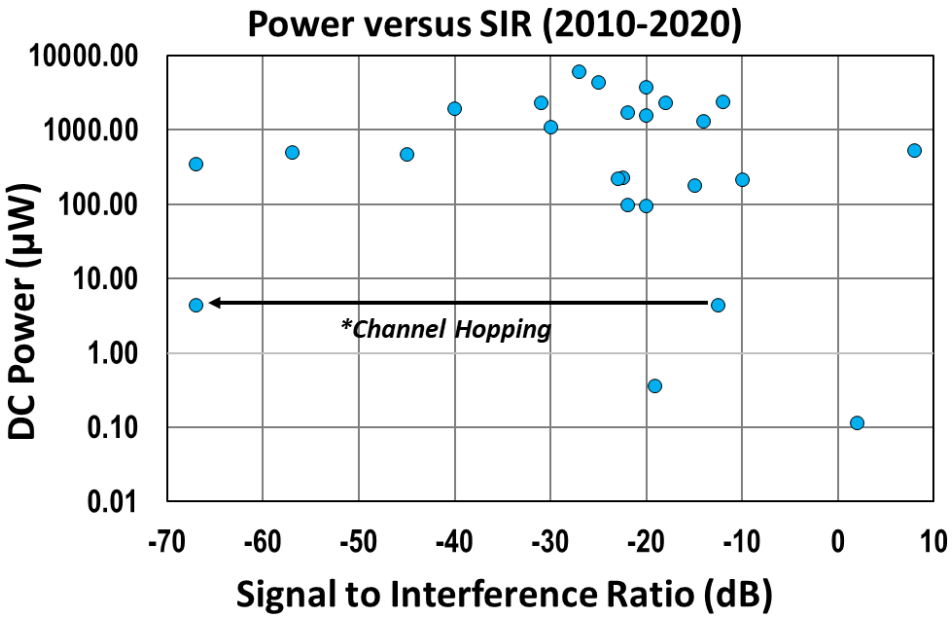


Fig. 5.2. Power versus SIR of 2.4GHz receivers during past decade.
(Not all the work in 5.1 reported SIR)

The reported signal to interference ratio (SIR) is shown in Fig. 5.2. The SIR does not show any directly discernable trends other than that the simultaneous low power and high SIR seems a challenging task to achieve. The lack of reporting can loosely be attributed to the fact that the recent low-power research has largely prioritized sensitivity improvements. However, given the extreme channel crowded nature due to the multiple coexisting standards and unlicensed usage at 2.4GHz, the interference tolerance is equally important as achieving higher sensitivity for robust operation in the increasingly crowded ISM bands. This has motivated the wake-up receiver work of [57, 58, 62, and 73] pursue superior high interference tolerance of better than a -50dB SIR. **Similarly, this work aims to achieve interference specifications near -50dB SIR.**

Short-range networks deployed inside of buildings or factory areas can greatly benefit from a smaller node volume. Area constraining components that are sensitive to placement, routing, and assembly such as off-chip RF inductors and bulky MEMS components contribute negatively to this aspect. The work in [57] operated entirely with integrated CMOS components where the only off-chip component is a 32KHz reference crystal used for the system clock. Contributing to this integration merit, **the goal of this work is to forego any off-chip and sensitive RF components.**

5.2 Prior Art Analysis and Insights

5.2.1 Uncertain IF as Preferred Wake-up Receiver Architecture

The ED-1st topology provides the lowest power due to the omission of any active RF gain and has demonstrated sub-μW operation at 2.4GHz [25, 37] as well as 9GHz [27, 28]. However, the sensitivity at low latency has failed to surpass -82dBm owing to inherent limitations explained in chapter 2. The duty-cycled Tuned-RF wake-up receivers of prior research phases achieved power near-μW for low latencies but require substantial RF gain and high-Q off-chip MEMS, which increase the integration cost. The driving of high impedance off-chip components at multi-GHz requires high dc-power if the inductively loaded buffers are avoided to reduce the system area. Furthermore, high gain in high-impedance environments can lead to instability and poor selectivity as demonstrated by the third phase of the T-RF work in chapter 4. These difficulties call for a more robust approach, such as low power heterodyne topologies, including the mixer-first [52, 56] and the uncertain-IF (U-IF) [46-48] in conjunction with a duty-cycling scheme [50, 62].

High sensitivity with the mixer-first architecture requires a low on-resistance of mixer switches [57] and a high voltage boost from the matching network, which respectively requires high LO power and high-Q components. The inclusion of a PLL can further increase the power due to long lock-times associated with lower frequency crystals [52]. Therefore, **this work adopts the U-IF topology with an event-driven calibrated RF oscillator to limit the IF uncertainty**. The channel-embedded OOK (CE-OOK) scheme proposed in the chapter 4 is also adopted to provide precise channel selection at the baseband even with the U-IF architecture, which can enable sub-carrier detection schemes in baseband.

5.2.2 Packet Level Duty Cycling as Preferred Duty-Cycling Scheme

As mentioned in the chapter 1, the asynchronous operation is beneficial since it enables mesh networks without the need for a dedicated base-station transmitter (TX), such as the synchronous ‘target wake-up time’ method preferred by the prior work at 2.4GHz band [52, 57]. The prior phase sub-GHz T-RF work demonstrated asynchronous operation with bit-level duty cycling, while the asynchronous packet level duty cycling has been demonstrated in the works of [50, 62] showing that either method is capable of operating without any synchronization overhead.

The prior sub-GHz phase work prioritized achieving maximum sensitivity while minimizing the dc-power. It was proven in Chapter 2 that BLDC provides a much better sensitivity advantage over PLDC **for the same power consumption and on-time**. The penalty paid for this is that the BLDC latency is N times longer than the PLDC case, where N is the wake-up message length. Given the highly crowded nature of the 2.4GHz ISM band, one major motivation for this work is to achieve a lower latency of several tens or hundreds of milli-seconds. Therefore, the BLDC latency penalty is no longer a negligible component. Moreover, the wake-up receiver sensitivity target for this work is near -90dBm, which is about 10dB below the MEMS-less T-RF case. Thus, the sensitivity advantage of BLDC alone does not provide a strong justification as the duty-cycling scheme, especially when the latency is a critical parameter.

Thus, a question naturally arises as to what trade-offs are enabled by the packet-level duty-cycling method if one were to tolerate a relaxed sensitivity target. To this end**, the trade-off between the sensitivity and latency for the case of same power between the two duty-cycling methods** warrants further attention.

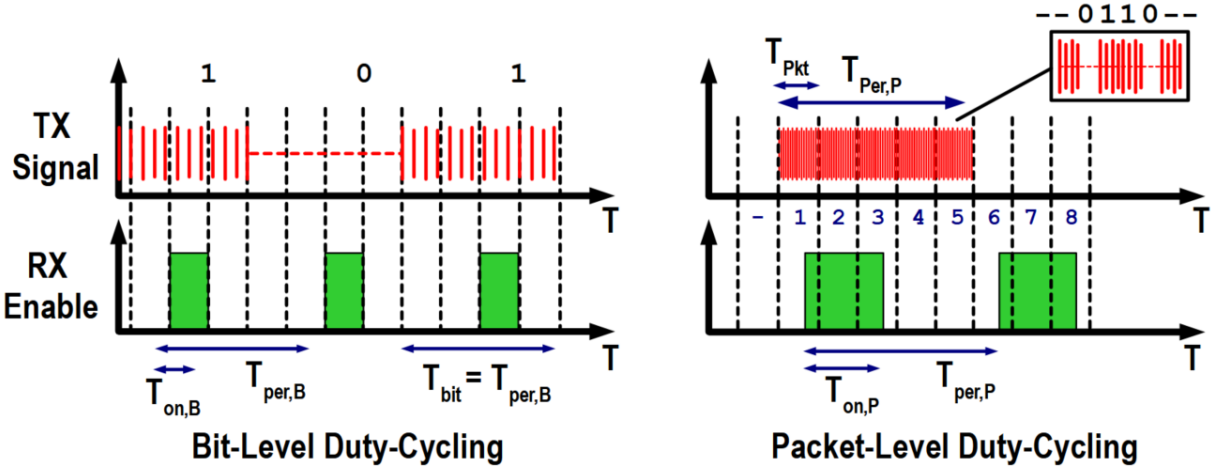


Fig. 5.3. BLDC (left) vs. PLDC (right) for general case.

The qualitative analysis for this case can be started with the aid of Fig. 5.3, where the BLDC and PLDC operations are shown side-by-side. BLDC operates identical to the implementation in the prior T-RF phases, where a portion of each transmitted bit ($T_{on,B}$) is sampled over a full bit duration of $T_{per,B}$. The minimum baseband bandwidth required to capture the rectified energy is given by the rise-time to bandwidth relationship:

$$BW_{BLDC} = \frac{0.35}{T_{on,B}} \tag{5.1}$$

The PLDC method requires back-to-back wake-up packet transmission such that a shorter on-time of the receiver can be adopted. This is because in a back-to-back message transmission, the receiver only needs N number of bits (one packet duration) to be captured instead of 2N due to repetition of the code. The captured N bits can then be rotated one bit at a time and compared against the wake-up address associated with the node to successfully detect a wake-up interrupt.

The baseband bandwidth of the PLDC case needs to satisfy Nyquist criterion and given by:

$$BW_{PLDC} = \frac{1}{T_{on,P}} \tag{5.2}$$

The power dissipation with the BLDC (P_{BLDC}) and PLDC (P_{PLDC}) methods are related to the instantaneous power (P_{inst}) by:

$$P_{BLDC} = P_{inst} \cdot \frac{T_{on,B}}{T_{per,B}} \tag{5.3}$$

$$P_{PLDC} = P_{inst} \cdot \frac{T_{on,P}}{T_{per,P}} \tag{5.4}$$

The above expressions (5.1) through (5.4) describe general case of the BLDC and PLDC operation. The same latency condition requires the period of PLDC ($T_{per,P}$) to be equal to the total number of bit duration in the BLDC case:

$$T_{per,P} = N \cdot T_{per,B} \tag{5.5}$$

Considering the special case where **both the latency and power are same**, the following relationship can be obtained:

$$\frac{T_{on,B}}{T_{per,B}} = \frac{T_{on,P}}{T_{per,P}} \tag{5.6}$$

Combining the expression (5.5) and (5.6) provide:

$$T_{on,P} = N \cdot T_{on,B}, \tag{5.7}$$

and Fig. 5.2 illustrate the above case.

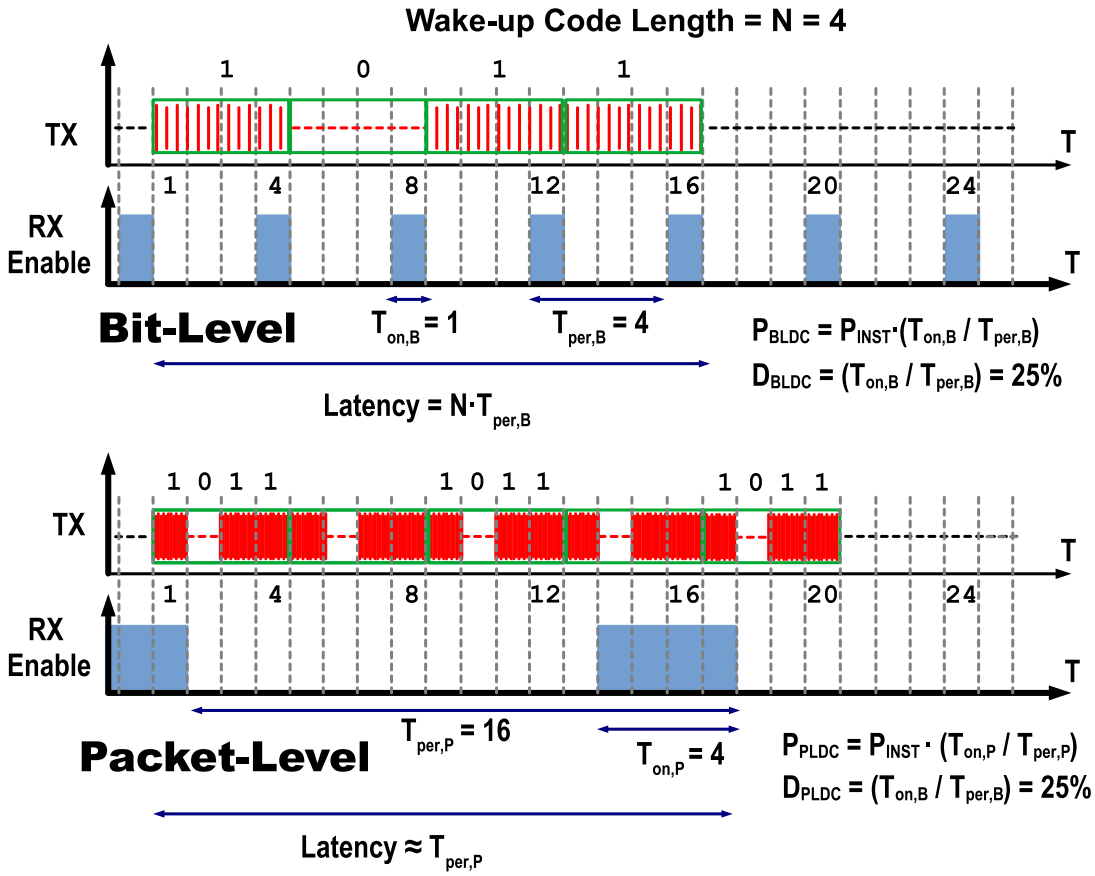


Fig. 5.4. Illustration of BLDC and PLDC for same latency and power

The unit time interval shown is the transmitted bit duration for the PLDC case, where the wake-up message length (N) is 4 bits. The bit duration of the BLDC case then corresponds to 4 unit-intervals and the duty-factor corresponding to both cases is 25%. The relative baseband bandwidth difference between the two cases is:

$$\frac{BW_{BLDC}}{BW_{PLDC}} = 0.35 \tag{5.8}$$

The result in equation (5.8) concludes that in the case of a **heterodyne receiver** with same power and latency, the sensitivity difference between PLDC and BLDC is $|\mathbf{10Log_{10}(0.35)}|$ = **4.6dB**, i.e. a BLDC receiver is 4.6dB better in sensitivity compared to a PLDC receiver of the same power and latency. However, the bandwidth of PLDC may be reduced below the requirement given by eq. (5.2) if certain statistics of the packet structure is known, such as the consecutive number of 1's and 0's allowed in a message and baseband pulse-shaping, which relaxes the ISI requirements. Hence, realistically, the sensitivity difference may approach ~3dB. For case of a T-RF or a U-IF with RF bandwidth much larger than baseband bandwidth, this leads to $|\mathbf{5Log_{10}(0.35)}|$ = **2.28dB < 3dB,** which is an acceptable reduction.

The analysis so far has assumed an instantaneous startup time. However, all analog circuits have finite time-constants associated with each node and require a certain startup and settling time. If the associated quality factors are high enough, then a node may exhibit significant ringing before reaching the steady state for bandpass circuits. The power overhead due to the startup can be analyzed with the aid of Fig. 5.5.

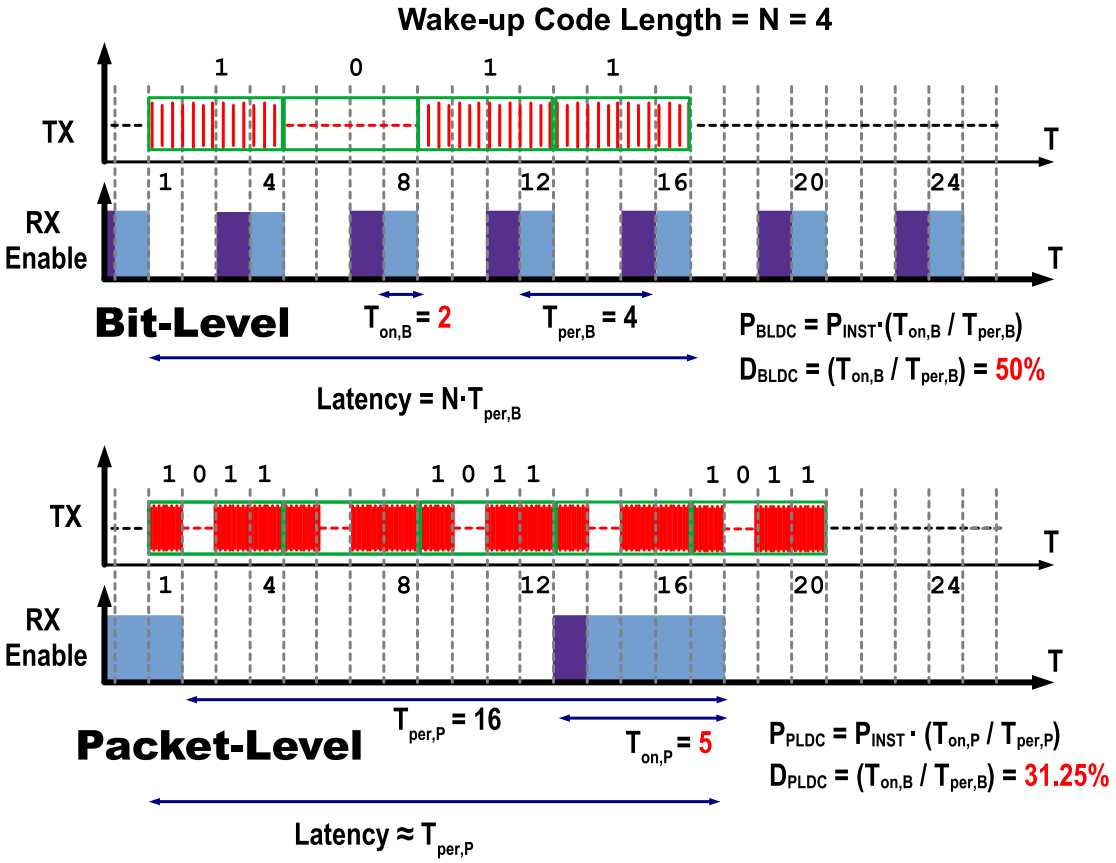


Fig. 5.5. Effect of startup time in BLDC and PLDC for same latency and power as in Fig. 5.4.

Fig. 5.5 shows the effect of a non-ideal startup for the same example shown in Fig. 5.4. A startup time of one additional bit of the PLDC case is used. This leads to a power increment of 25% in the BLDC case but only 6.25% in the PLDC case. In other words, the BLDC method achieves poor 'energy-per-bit' metric for the case of the same latency and power as the PLDC receiver. Note that in the case of an integrated PLL with a low frequency reference (32KHz) such as the work in [52], PLL settling time can be several milliseconds, such that a heavy power penalty may be paid in a BLDC scheme.

Another disadvantage of BLDC is the dc-offset and interference up-conversion due to the spectrum shaping effect, as discussed in the section 3.2. Given that a PLDC receiver operates mostly in its steady state operating conditions, such spectrum shaping does not occur for a sufficiently large $T_{on,P}$. Moreover, for a fixed transmitter bit rate, PLDC needs to trade-

off sensitivity to achieve a lower power, while PLDC can trade-off latency for power while maintaining the maximum sensitivity. This is assuming that the transmitter continues the back-to-back wake-up transmission for a maximum pre-determined latency period. *Note that a similar scheme in BLDC cannot exist since maintaining maximum sensitivity while lowering the power requires a fixed on-time and reducing the bit-rate.*

Given the above-mentioned reasons of:

1) Better energy per bit metric due to startup delays,
2) Robustness against dc-offset and interference up-conversion through spectrum shaping,
3) Latency and power trade-off while maintaining maximum sensitivity for constant TX bitrate,

this work adopts the PLDC scheme as the preferred duty-cycling method.

Given that the wake-up events are infrequent, and the receiver spends majority of the time listening to an idle channel, a modification to the previously explained PLDC scheme can be adopted as shown in Fig. 5.6. Called the 'within-packed duty-cycling' (WPDC), at the beginning of each duty period, the receiver first determines if the wake-up channel is active by sensing the carrier energy level. If the energy in the first several bit periods are above a certain threshold, then the channel is deemed active, and the wake-up receiver stays on for a duration of a full packet. Conversely, if the energy level is too low and the channel is deemed inactive, the receiver turns off early. This results in a dynamic duty-factor where the receiver operates at a much lower duty-cycle if the wake-up channel is inactive, which in turn contributes to power savings.

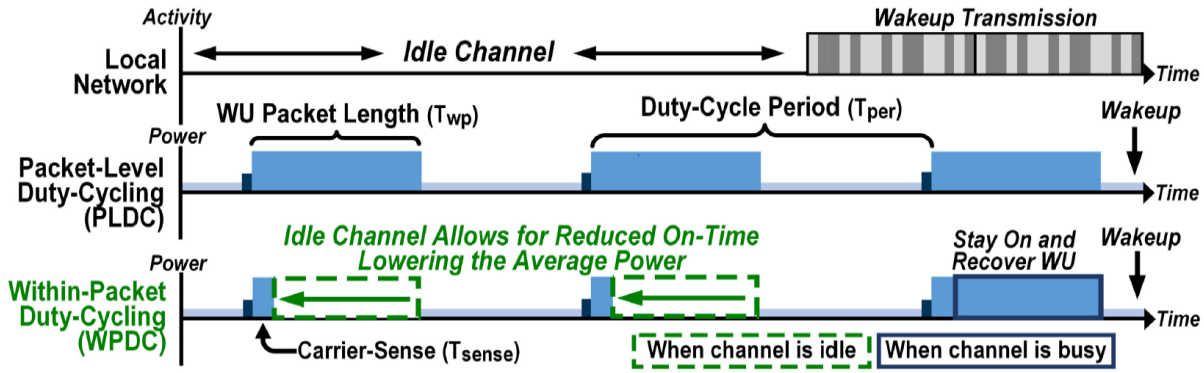


Fig. 5.6. Within-Packet Duty-Cycling to Further Reduce Power

5.3 Wake-up Receiver Architecture

5.3.1 Near-μW Heterodyne Topology Overview

A recent uncertain-IF (U-IF) wake-up receiver achieved -80dBm sensitivity for an extreme low dc-power of 17nW, but at a higher latency of 5s [50]. As discussed before, such high latency can be problematic in a crowded frequency band due to interference as well as hindering node-to-node wake-ups due to the higher required TX on-time. However, the extracted dc-power from the presented plots approximate 370nW for a latency of 100ms with a custom FSK, which is highly desirable for low latency applications. Such low power is possible due to the omission of an RF PLL, an approach that shows up in non-duty cycled work as well [46, 47]. The RF oscillators used in these U-IF wake-up receivers require external calibration, which may need to be performed per chip basis, since an approximate 2fF variation can cause a 1MHz frequency drift at 2.4GHz with a 10nH inductor in the resonant tank. Furthermore, such calibration schemes perform poorly against the temperature and voltage variations. Thus, low-cost and built-in self-calibration methods to maintain high sensitivity by avoiding a large IF uncertainty are a highly desired feature [46, 48].

5.3.2 Proposed Wake-up Receiver

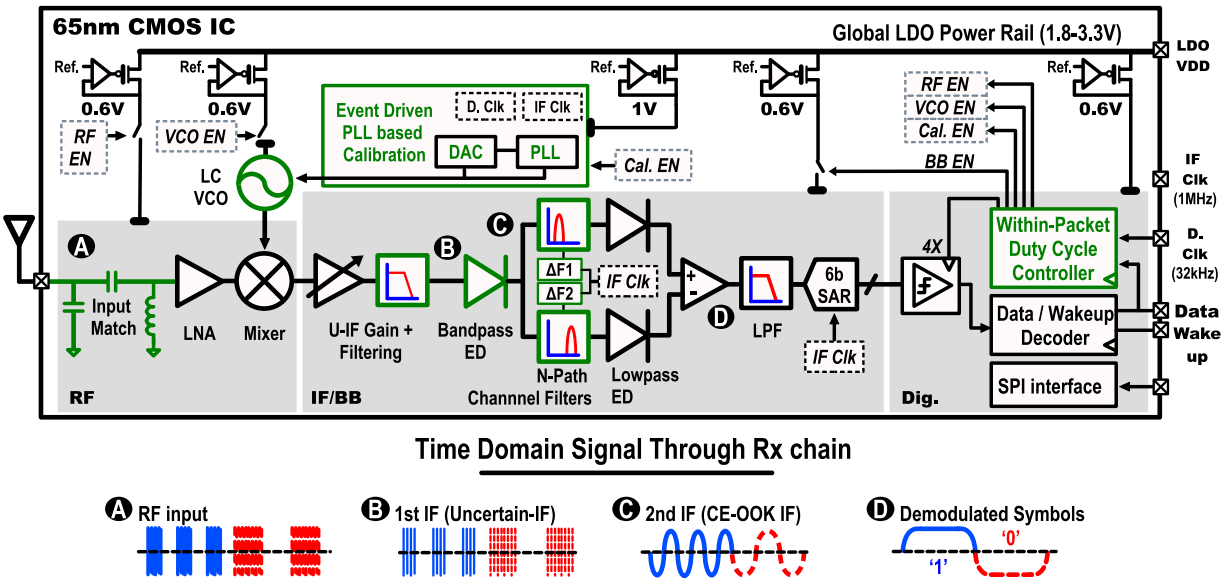


Fig. 5.7. Block Diagram of event driven calibrated U-IF receiver. Time domain signals at various points are also shown.

The proposed wake-up receiver solution is shown in Fig. 5.6 and adopts the U-IF topology with an event-driven integrated PLL based frequency calibration. The PLDC/WPDC methods and rotating correlators are adopted for power savings, where the wake-up receiver needs to stay on for one packet duration. Since the U-IF architecture cannot inherently achieve precise channelization, the channel-embedded OOK (CE-OOK) signaling is adopted to provide deterministic sub-carrier channel filtering at the baseband. The wake-up receiver is implemented in a CMOS low-power (LP) process with access to multiple V_{th} devices to further minimize the leakage.

The CE-OOK RF input signal is sensed through an on-chip matching network, amplified by an LNA, and downconverted to an uncertain-IF using an active mixer driven by a free-running VCO. The U-IF signal is further amplified and filtered by a programmable 4^{th} order Gm-C low pass filter (LPF). The bandwidth of this LPF limits the allowable frequency drift of the LO and ultimately limits the maximum sensitivity and SIR as explained later. The filtered signal is rectified by an envelope detector with a bandpass output for dc-offset mitigation. The output of the rectifier produces the CE-OOK embedded channels in a BFSK format. Then, a tuned-filter based energy comparison is performed to demodulate and produce an analog bit stream. An n-path (n=4) based bandpass filter (BPF) followed by an envelope detector and a difference amplifier implements the energy comparison for '0' and '1' sub-carrier channels. The difference is amplified and lowpass filtered prior to digitizing with a 6-bit SAR ADC. The ADC output is used in a quadruple (4X) oversampled comparator for bit decision. The demodulated oversampled bit stream is used for the detection of wake-up signature with 4 parallel correlator banks and within-packet duty cycle control. The local power supplies are regulated by dedicated low-dropout regulators (LDO) and the reference clocks of 1MHz and 32KHz are provided externally.

The LDO is of conventional design with thick-gate I/O transistors and intended to be directly operated with a 1.8-3.3V battery supply for the convivence in a system-in-package (SiP) integration in a larger system including an MCU and a sensor front-end. Although the LDOs do not provide any power benefit when referred to the battery voltage, it is meant to be used as a proof of concept demonstrating the effects of LDOs on wake-up receiver performance metrics with aggressive duty-cycling. The LDOs can be redesigned for a lower global supply voltage with ease.

Although the mixer first topology has been favored in low power receivers, such RX typically demonstrates poor sensitivity due to high mixer noise figures. The power saved by the omission of an LNA, and an active mixer needs to be compensated in the VCO and LO driving circuitry to maintain high sensitivity, which leads to diminishing returns. Hence, this work adopts the LNA first topology. The LNA also provides improved shielding to the LO leakage through the RF input port.

5.3.3 LO considerations

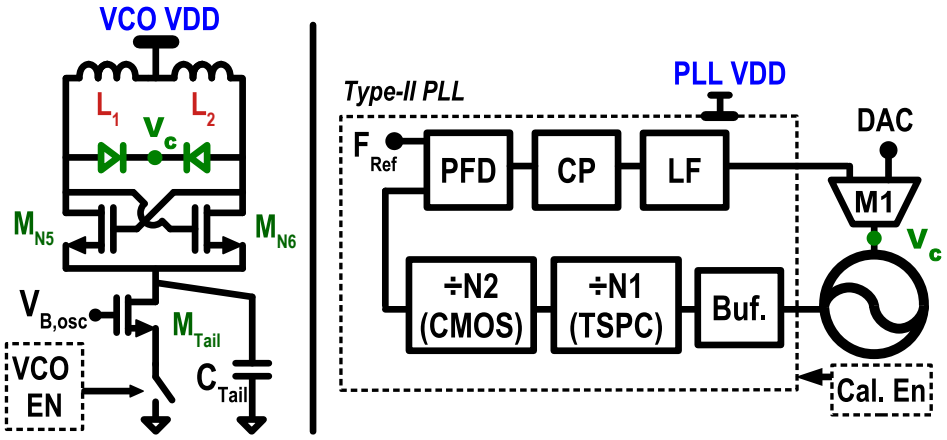


Fig. 5.8.VCO (left). PLL used for frequency calibration (right).

An on-chip inductor-based LC-VCO (Fig. 5.8) with low frequency gain is adopted for improved frequency stability. Although low-Q on-chip inductors lead to an increase in dc-power, this is still a desirable trade-off since it avoids off-chip RF component integration. The VCO can be calibrated with the aid of an integrated type-II PLL using the procedure shown in Fig. 5.9 and stores the control voltage in a 7-bit capacitor DAC. The calibration process is shown in Fig. 5.9.

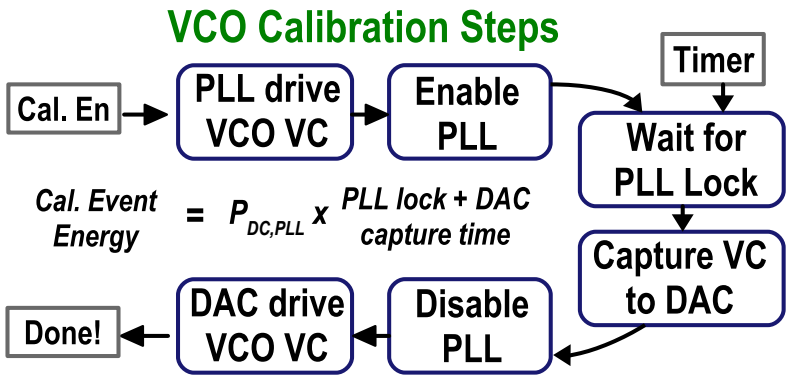


Fig. 5.9. Event driven VCO calibration steps

Frequency variations due to small capacitive process variations are corrected by the PLL with ease. Assuming the supply voltages of the VCO and the control voltage storage DAC are well regulated and have adequate decoupling capacitors, the frequency variation due to the temperature becomes the dominant instability source. A temperature sensor IP block [74] is included in the wake-up receiver, whose value can be read through a SPI interface. The temperature information can then be used to re-calibrate the VCO in an event-driven basis depending on the desired IF bandwidth. The tolerable temperature drift before a re-calibration event depends on the temperature coefficients of the VCO [76], largely the capacitive components. The PLL can also be set to periodically re-calibrate the VCO, but at a slower duty rate than rest of the circuitry to reduce the power overhead. The simulated settling time of the PLL is about 70us. With a calibration event time of 2ms to account for the DAC capture time and a duty-rate of once per 10s lead to an average power of 52nW for the PLL (with a measured active chip dc-power of 260μW).

5.3.4 Sensitivity Estimation and CE-OOK Extraction

The sensitivity of a conventional heterodyne RX can be derived using the definition of noise figure and given by the following expression:

$$P_{MDS} = -174dBm + NF + 10\log(S_{BW}) + SNR_{min} \quad (5.9)$$

where P_{MDS} is the minimum detectable signal power in dBm, NF is the system noise-Fig., S_{BW} is the occupied signal bandwidth, and SNR_{min} is the minimum required signal to noise ratio for the desired bit error rate. However, the IF bandwidth does not correspond to the bit rate in U-IF topology, and the sensitivity in this case is analogues to the Tuned-RF RX [64]. The sensitivity of the U-IF wake-up receiver is then approximated by the following expression:

$$P_{MDS} = -171dBm + NF_{SSB} + 5\log(BW_{RF}) + 5\log(BW_{BB}) + SNR_{min} \quad (5.10)$$

where NF_{SSB} is the single side band noise figure at the input of the envelope detector, BW_{RF} is the bandwidth prior to envelope detector, BW_{BB} is the bandwidth after the envelope detector. The NF_{SSB} term (2nd term of eq. (5.9)) accounts for the signal to noise ratio degradation prior to the rectification while the 3rd and 4th terms accounts for the wideband input noise rectification and post-envelope-detector noise integration.

Above expression was modified from the original context of a T-RF RX with the data rate much larger than the RF bandwidth case, and observing that the U-IF RX is identical to a T-RF RX with a frequency shifting operation prior to the ED. In this work, BW_{RF} corresponds to the bandwidth after the mixer and BW_{BB} is related to the instantaneous (or always-on) bit rate. Assuming the IF uncertainty is 4MHz (=BW_{RF}), a data rate corresponding to 8.192KHz (=BW_{BB}), a NF of 12dB prior to ED, and a 11dB $SNR_{min,}$ yield an approximate sensitivity of -94.5dBm, which is comparable to the current state-of-the-art standard compliant wake-up receivers.

The IF downconversion does not alter the embedded channels in the CE-OOK regardless of the LO uncertainty. Approximating the CE-OOK symbol with an RF carrier (ω_{RF}) multiplied by a square signal limited to the 1st and 3rd harmonics for simplicity, the rectified output of the 1st ED ($V_{out,ED}$) is:

$$V_{out,ED} \propto \left(1 + {}^{4}/_{\pi}\left(\sin(\omega_d t) + \frac{1}{3}\sin(3\omega_d t)\right) \cdot \cos(\omega_{RF} t) \cdot \cos(\omega_{LO} t)\right)^2 \qquad (5.11)$$

where ω_d corresponds to the desired CE-OOK encoded baseband channel and ω_{LO} is the LO frequency. The low frequency terms of (3) can be isolated as:

$$V_{out,ED} \propto \frac{2}{\pi}\sin(\omega_d t) + \frac{2}{3\pi}\sin(3\omega_d t) \; - \frac{2}{3\pi^2}\cos(2\omega_d t) - \frac{4}{3\pi^2}\cos(4\omega_d t) - \cdots \qquad 5.12)$$

The first two terms of eq. (5.12) correspond to the rectified square signal, and the next two terms corresponds to error due to approximation of a square wave with the 1st and 3rd harmonics. These errors diminish as the number of harmonics are increased. The embedded channel frequency ω_d corresponding to transmitted symbol can be filtered and isolated with a BPF after the ED.

5.4 Circuit Implementation

5.4.1 RF Frontend

An LNA first RF frontend is adopted for low power down-conversion and the building blocks are shown in Fig. 5.10, including the duty cycling switches. The input RF signal is sensed through a tapped-capacitor matching network comprising C_{M1}, C_{M2}, and L_M ($Q \approx 10$) where all components are realized on-chip for the integration merit. The required component values for matched condition are approximated by solving the relationships below:

$$\frac{C_{M1}C_{M2}}{C_{M1}+C_{M2}} = \frac{1}{(2\pi f_C)^2 L_M} \tag{5.13}$$

$$R_S \cdot (1 + C_{M2}/C_{M1})^2 = R_M, \tag{5.14}$$

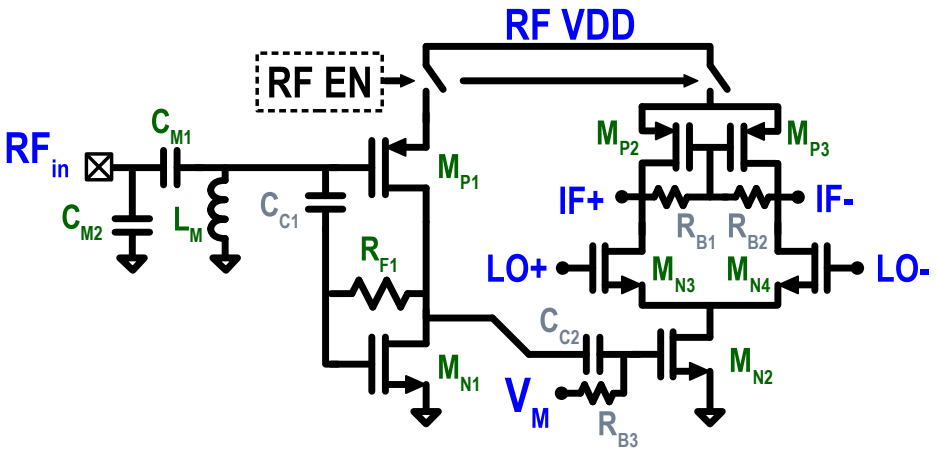


Fig. 5.10. Schematic of LNA and mixer

where, R_M is the equivalent parallel resistance of the inductor, f_C is the center frequency, and R_S is the 50Ω antenna resistance. Any real resistance from the LNA appearing in parallel to the inductor can be lumped into R_M. Since R_S is 50 ohm and R_M can be realized in the order of kilo ohms at 2.4GHz, C_{M2} is smaller than C_{M1} and the center frequency varies weakly with C_{M2}. This is advantageous since C_{M2} can now readily absorb any unaccounted parasitic pad, ESD, transmission line, and PCB capacitances without a significant variation of the matching frequency, which improves the robustness. Simulated values for L_M = 11.1nH, C_{M1} = 0.38pF, and C_{M2} = 0.6pF including pad and ESD capacitance.

The LNA is a complementary current-reuse topology made of M_{P1} and M_{N1} for doubled gm with a supply voltage of 0.6V. The gate of M_{P1} is dc-grounded via the matching inductor L_M and M_{N1} is self-biased with the feedback resistor R_{F1} (=110kΩ). Assuming an equal transconductance for both M_{P1} and M_{N1}, the feedback resistor R_{F1} acts as an ac open circuit due to large size. Neglecting the flicker noise, the gain and noise figure of LNA can be approximated by (5.15) and (5.16) as:

$$A_V \approx 2g_m \cdot (r_{o,n}||r_{o,p}) \cdot \sqrt{\frac{R_M}{R_S}} \tag{5.15}$$

$$NF \approx 2 + \frac{\gamma}{g_m R_M} \tag{5.16}$$

where, $r_{o,n}$ and $r_{o,p}$, are the output resistance of M_{N1} and M_{N2}, γ is the channel thermal noise coefficient. The simulated gain for the LNA is 26dB including a 13dB gain from the

matching network. Due to the relatively low bias current and low-Q inductor, the noise figure is approximately 5dB in simulation, 2dB higher than the ideal minimum value.

The output of the LNA is ac-coupled to a conventional single balanced active mixer, which performs the 1st downconversion to an uncertain IF band. The current source of the mixer is merged with the voltage to current conversion stage in M_{N2} for low headroom operation and biased via R_{B3}. The switching pair comprises of M_{N3} and M_{N}, and loaded with the self-biased PMOS pair M_{P2} and M_{P3} . The PMOS pair's body terminals are shorted to the gate to lower the threshold voltage. All bias resistors are 110kΩ and the simulated conversion gain is 7dB. The startup time for both the frontend is less than 2µs leading to a negligible wasted power.

5.4.2 Local Oscillator and Frequency Stability

Since the VCO is mostly expected to be in the free-running condition for the proposed wakeup architecture, the frequency stability is of utmost importance. Since LC based oscillators with sufficiently high Q factors are superior ring oscillators with respect to stability and phase-noise [76], we adopt a cross-coupled LC oscillator as shown in Fig. 5.8. The NMOS based topology comprised of M_{N5} and M_{N6} is preferred for low voltage operation and the tank inductors (L_1, L_2) are realized with a symmetric center-tapped inductor. Since any resistance appearing at the resonant tank interface can degrade the Q-factor, the duty cycling switch is inserted at the tail current side.

Several factors can adversely affect the frequency stability of the VCO and warrants attention, which are:

a) Phase noise,

b) Supply voltage noise,

c) Control voltage noise,

d) Temperature variation.

The phase noise of an LC oscillator is inversely proportional to the tank Q factor [76] and therefore it is beneficial to choose an inductor with the largest Q possible, which trades-off with the area occupied and frequency sensitivity to tank capacitance. A tail capacitor (C_{tail}) is also added to further attenuate the phase noise. The value of C_{tail} was determined through simulations.

The supply noise appears directly across the varactor diodes, which in turn affects the frequency. Any noise appearing at the control voltage node similarly modulates the VCO frequency. The supply voltage noise is suppressed using a dedicated LDO for the VCO and employing both RF and low frequency decoupling capacitors. The gain of the VCO is intentionally kept low (100kHz/mV) to desensitize to variations in the supply and control voltage.

An LC VCO is typically less affected by temperature compared to a ring oscillator and the variations are mainly due to the resonant tank capacitance changes. With a 7.5nH inductor and a resonant frequency of 2440MHz, a variation in 1fF leads to a frequency deviation of approximately 2.1MHz. A lower sensitivity to capacitance can be achieved by selecting a smaller inductor, but this comes at the cost of dc-power to maintain reasonable voltage swings. Simulation results achieve a 300mV peak swing for a 140uA bias current with the selected inductor size. The type-II PLL shown in Fig. 5.8 is used for the event driven calibration of the VCO. Output of the VCO is buffered and divided down to the reference frequency range by a cascade of true single phase clocking (TSPC) and CMOS digital divider chain. The Charge pump current is selected at 10uA and the loop filter is implemented externally for tuning convenience.

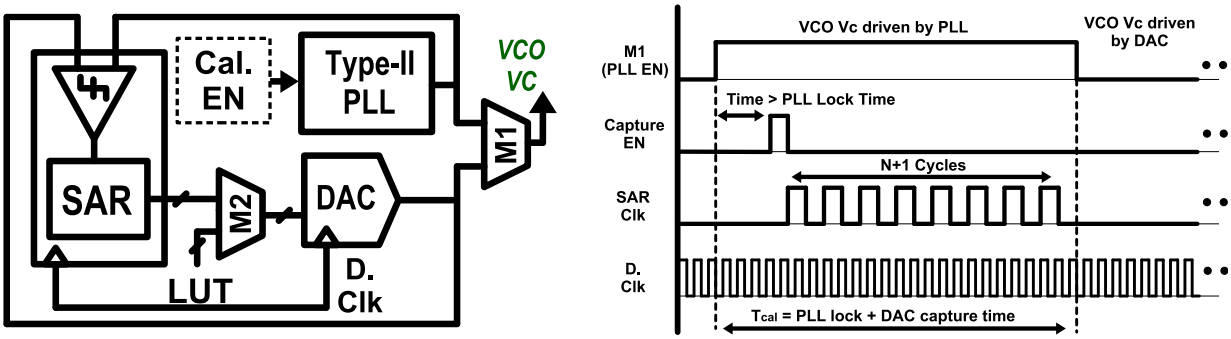


Fig. 5.11. VCO calibration circuitry and the timing diagram.

The block diagram of the VCO calibration circuitry and corresponding timing diagram are shown in Fig. 5.11. Upon receiving the "Cal. EN" signal, the PLL VDD is enabled and the multiplexer M1 selects the PLL to drive the control voltage of the VCO. After a set amount of time required for the PLL to acquire the lock condition, the "Capture EN" signal is issued. This enables the clock signal for the SAR based logic to resolve the control voltage into an N-bit DAC (N=7). Finally, the multiplexer M1 sets the VCO to be driven by the output of the DAC and disables the PLL VDD, which completes the calibration event. The DAC is driven with the 32KHz clock and the SAR clock signal is generated by the capture logic block internally.

The DAC LSB needs to be kept low to maintain frequency variation due to quantization error. Additionally, the multiplexer M2 can be used to set an external DAC code word through the SPI interface.

Note that an all-digital PLL (ADPLL) with a digitally controlled oscillator (DCO) could potentially replace the operation of VCO, PLL, and DAC loop. This however requires low on resistance switches to be realized in the used LP technology at reasonable sizes, that does not significantly cause deviations in the frequency or the Q-factor.

5.4.3 Signal processing at Uncertain-IF (1st IF)

The down-converted RF signal needs further amplification and noise-limiting filtering before the 1st rectification. The IF signal chain includes a programmable gain amplifier (PGA) based on prior T-RF phases (chapter 3) followed by a tunable 4th order Gm-C lowpass filter. Higher order filters provide strong out-of-band interference suppression. The filter is digitally tunable up to 4MHz of bandwidth.

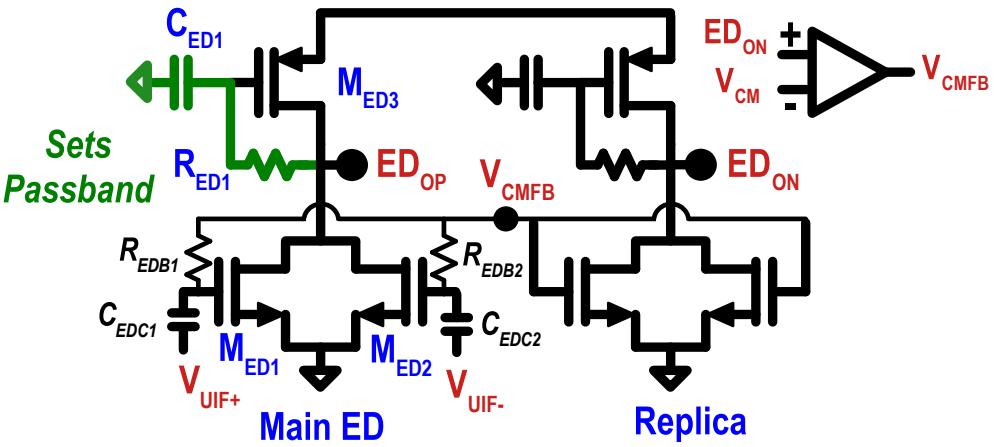


Fig. 5.12. IF envelope detector for demodulation CE-OOK symbols

The IF-ED shown in Fig. 5.12 acts as a down-converter from the uncertain-IF signal to known IFs embedded in CE-OOK signals and needs further processing in the baseband. The open-circuit voltage sensitivity (OVCS) of this ED is equivalent to the IF conversion gain, and can be derived with the aid of sub-V_{th} drain current (I_{DS}) current model [77, 78]:

$$I_{DS} = I_{dc} \exp\left(\frac{V_{in,ac}}{nU_T}\right) \tag{5.17}$$

$$I_{dc} = I_0 \exp\left(\frac{V_{CMFB}-V_{th}}{nU_T}\right)\left(1-\exp\left(\frac{V_{DS}}{U_T}\right)\right) \quad (5.18)$$

where I_0 is technology current proportional to device parameters; V_{GS}, V_{DS}, and V_{th} are the gate source, drain-source, and threshold voltage of input NMOS of main EDm V_{CMFB} is the gate bias voltage provided with the aid of replica ED, U_T is the thermal voltage, and n is the sub-Vt factor typically about 1.5. Applying Taylor series expansion up to the 2nd order terms produces:

$$I_{DS} = I_{dc}\left(1+\left(\frac{V_{in,ac}}{nU_T}\right)+\frac{V_{in,ac}^2}{2(nU_T)^2}\right) \quad (5.19)$$

The constant term in eq. (5.19) represents the dc bias current and the 2nd term is the small signal ac-gain term. The 3rd term provides the CE-OOK demodulation via square-law operation. The differential input can double the dc current while cancelling the ac-gain at the drain node. This is extremely beneficial since the ac-gain can suppress the rectified CE-OOK signals due to the much lower frequency operation compared to prior T-RF phases, where the input of the ED was at the vicinity of 434MHz.

For simplicity, approximating the CE-OOK as a two-tone modulated signal with channel separation of $\Delta\omega_{IF}$, and substituting $V_{in,ac} = \frac{V_{IF}}{\sqrt{2}}\left(cos\,(\omega_{IF}t) + cos\,(\omega_{IF}t + \Delta\omega_{IF}t)\right)$ in to 3rd term and neglecting the terms above $2\omega_{IF}$ due to BPF, yields the low frequency rectified current given by:

$$i_O = \frac{I_{dc}V_{IF}^2}{4(nU_T)^2}(1+\cos(\Delta\omega_{IF}t)) \quad (5.20)$$

The sinusoidal term in eq. (5.20) carries the channel information embedded in the CE-OOK RF signal. Thus, the 2nd IF is certain, and can be used for channelization.

The 1st term in eq. (5.20) represents the dc-offset due to input, which can saturate the baseband for large input signals. The capacitive coupling can alleviate the input compression of the baseband but it does not fix the ED output node compression. The ED output compression is suppressed by adopting an inductive load to provide a bandpass response. Assuming the drain node is capacitively loaded with C_L, the output impedance at ED_{OP} is:

$$Z_{O,ED} = \frac{1+sR_{ED1}C_{ED1}}{s^2R_{ED1}C_{ED1}C_L+s(C_{ED1}+C_L)+g_{m,ED3}} \quad (5.21)$$

which provides a bandpass behavior suppressing the dc-offset, provided that $1/g_{m,ED3} \ll R_{ED1}$.

The output signal of the 1st ED contains the demodulated channel information of the CE-OOK signal in a BFSK format. We adopt tuned-filter based energy detection to detect the embedded symbols. The PGA cell following the 1st ED provides additional gain, and the FSK channel filters are realized as n-path filters (n=4) since the required Q factor is greater than 10 (center frequency > 100kHz and instantaneous bandwidth ≈ 8kHz). The filtered signals are rectified with an active common source type ED and differentially amplified to produce a demodulated analog symbol stream. The symbols are then low pass-filtered and digitized with a 6-bit SAR ADC.

5.4.4 Digital Baseband

The wake-up receiver can operate with either the standard packet-level duty cycling or carrier sense within packet duty cycling (WPDC). The necessary functionality and logic are implemented in the digital baseband as shown in Fig. 5.13. At the beginning of the duty period for a given number samples, the WPDC controller decides if sufficient energy is present based on the number of samples crossing a given threshold value. If a certain number of samples cross the threshold, then the channel is deemed active, and the receiver continues to collect enough samples to demodulate a wakeup. The integrated timing block requires the 32KHz digital clocks to regulate duty-cycle behavior for all components. The data collection process for the carrier-sense mechanism and the rotating correlator are controlled from the same timing block.

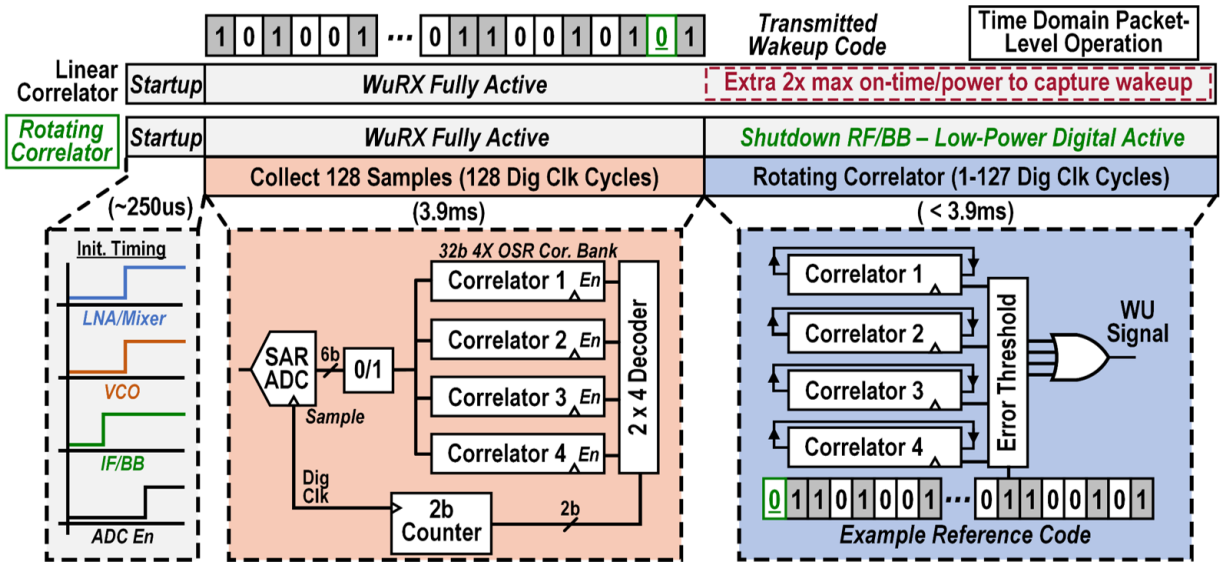


Fig. 5.13. Digital baseband including timing control, WPDC, and Correlators.

5.5 Measurement Results and Discussion

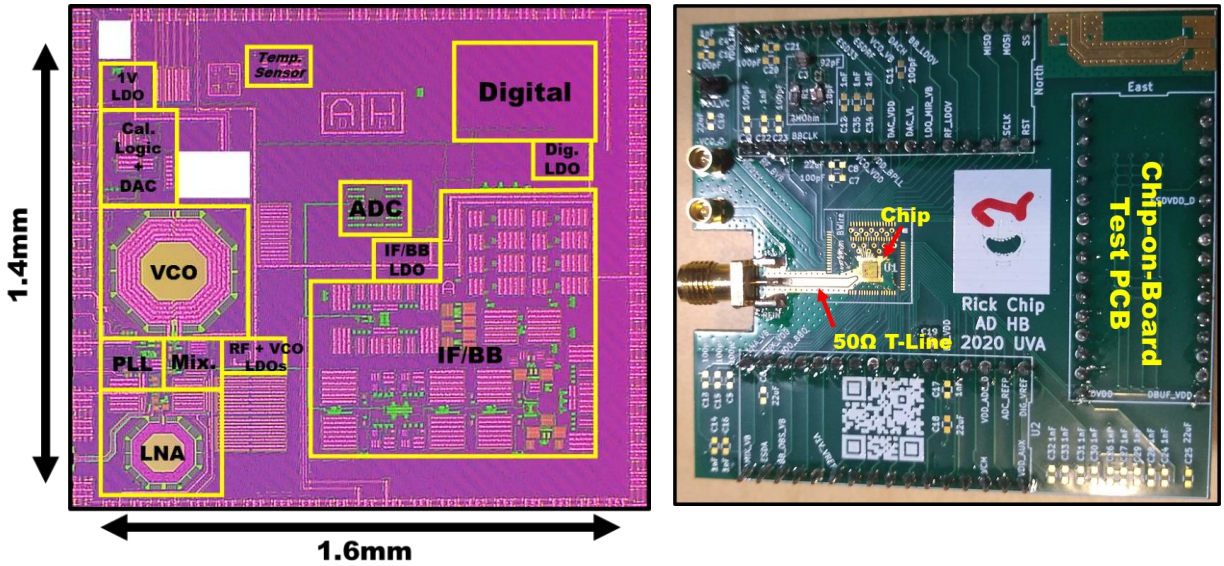


Fig. 5.14. Chip photograph and the chip on board test PCB

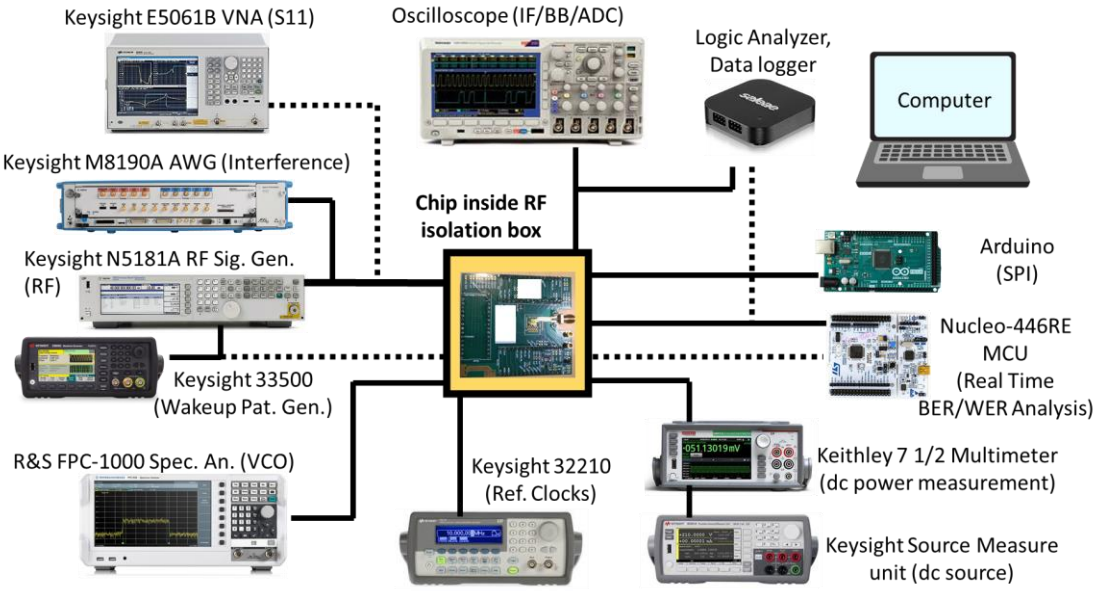
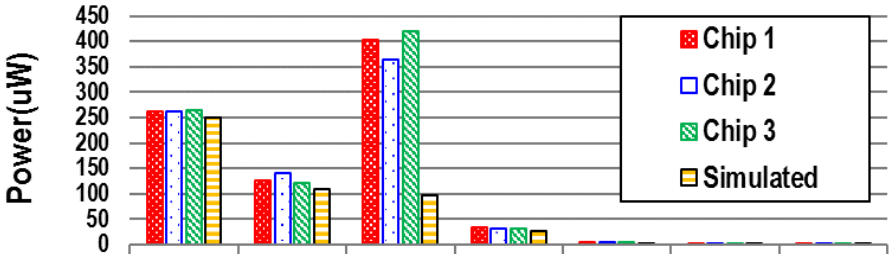


Fig. 5.15. Measurement setup

The prototype wake-up receiver was implemented using the TSMC 65nm CMOS LP process. The chip photograph including key circuit blocks are shown in Fig. 5.14 and a chip on board test PCB used for evaluation. The input RF trace for the PCB is a 50Ω co-planar waveguide with ground plane transmission line. The prototype is characterized by taking measurements from three separate samples and the setup shown in Fig. 5.15 is used for chip characterization.



	PLL	RF	VCO	IF/BB	ADC	DIG	Leakage
Chip 1	260.8	126.9	403.1	32.7	3.6	0.6	0.3
Chip 2	261.5	140.3	363.5	31.7	3.6	0.5	0.4
Chip 3	265.1	122.0	420.7	30.8	3.6	0.6	0.4
Simulated	250.0	108.0	96.0	27.0	3.0	0.3	0.3

Fig. 5.16 Measured and simulated active power of the blocks.

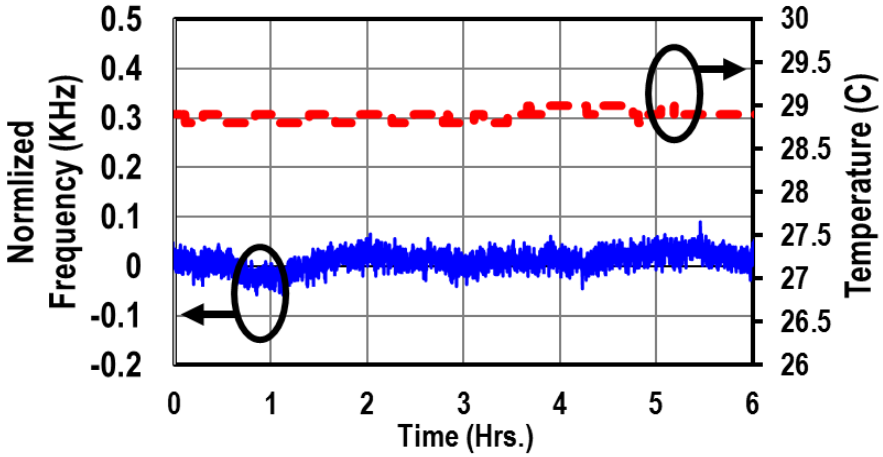


Fig. 5.17. Measured long term stability of the VCO.

The active power consumption with respect to the block level supply voltage of various components are shown in Fig. 5.16 along with the simulated values for better comparison. The measured dc-power of the VCO in Fig. 5.16 shows a four-fold increase over the simulated value. The nominal frequency of the VCO was set at 2.44GHz in simulation, but the measured frequency was near 2.54GHz, an approximately100MHz shift towards high frequency. We suspect this was due to an incorrectly extracted varactor capacitance and inductance at the post layout level. Unfortunately, no tuning capacitors were added in the VCO for this prototype. Thus, the nominal frequency was shifted back to the desired 2.4GHz range by increasing the bias current, which resulted in the power increase. This can be reduced to the intended power with the required capacitance corrected in the resonant tank in a future chip implementation.

The long-term stability of the free-running VCO was measured for 6 hours at the nominal lab temperature with a Rhode & Schwarz FPC-1000 spectrum analyzer with 5MHz span and 10kHz resolution bandwidth (Fig. 5.17). The VCO demonstrates about 150KHz variation at nominal lab temperature and the measured gain is approximately 110kHz/mV, slightly increased due to the re-tuning. The measured deviation between the PLL based calibration to free-running case was less than 500KHz, and the allowed IF bandwidth after the mixer is 2MHz, which corresponds to twice the frequency variation required for 500kHz case.

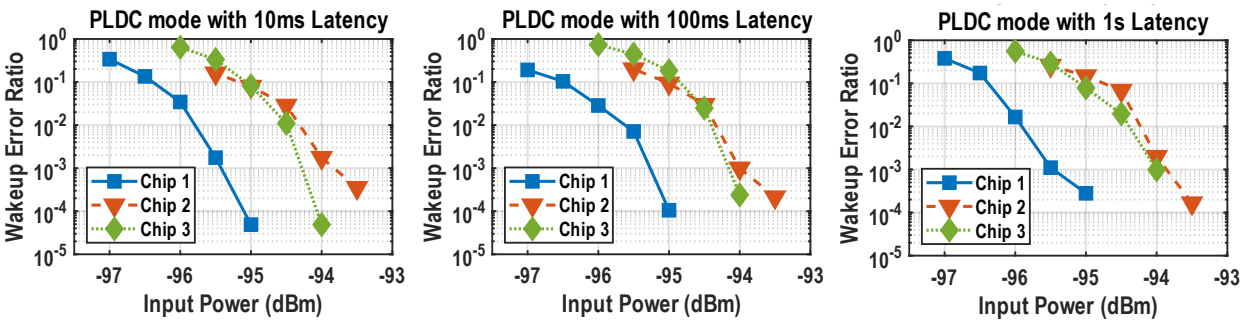


Fig. 5.18. Measured wake-up error ratio in PLDC mode.

The wake-up error ratio (WER) is characterized for the conventional PLDC mode first. The input is set to transmit the wake-up code back-to-back, while the wake-up receiver operates asynchronously to the transmitter. Measured results shown in Fig. 5.18 are taken for the latency periods of 10ms, 100ms, and 1s to characterize the scalability. A sensitivity near -94dBm is measured for 0.1% WER for a false alarm rate below <1/hr with 6 errors tolerated in the correlator.

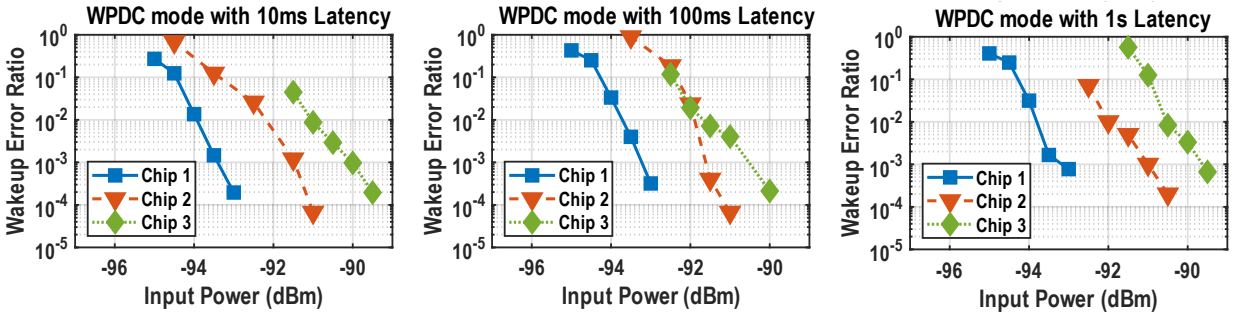


Fig. 5.19 Measured wake-up error ratio in WLDC mode.

Next, the WER in the WPDC mode is measured as shown in Fig. 5.19 for the same latencies. A sample size of 5 at the beginning of each period with a threshold crossing count of 3 is used to determine whether a carrier is present as per the WPDC operation. This inevitably causes a sensitivity loss compared to PLDC case as observed by several decibel degradation for the respective latencies.

Table 5.1. PLDC power

PLDC Power			
	Chip 1	Chip 2	Chip 3
10ms	193.62	188.80	204.60
100ms	12.75	12.02	13.18
1s	1.96	1.97	1.93

Table 5.2. WPDC power

WPDC Power			
	Chip 1	Chip 2	Chip 3
10ms	24.77	20.90	24.48
100ms	2.23	2.02	2.18
1s	0.98	0.90	0.91

The power consumption corresponding to the PLDC and WPDC modes are shown side by side in tables 5.1 and 5.2. The observed dc-power reduction is about 8X for the 10ms (low latency) and 2X for the 1s (high latency) proving the advantage of the WPDC method. The reduced power advantage at high latency is due to the dominating power of the digital and leakage components, that cannot be further reduced with duty-cycling.

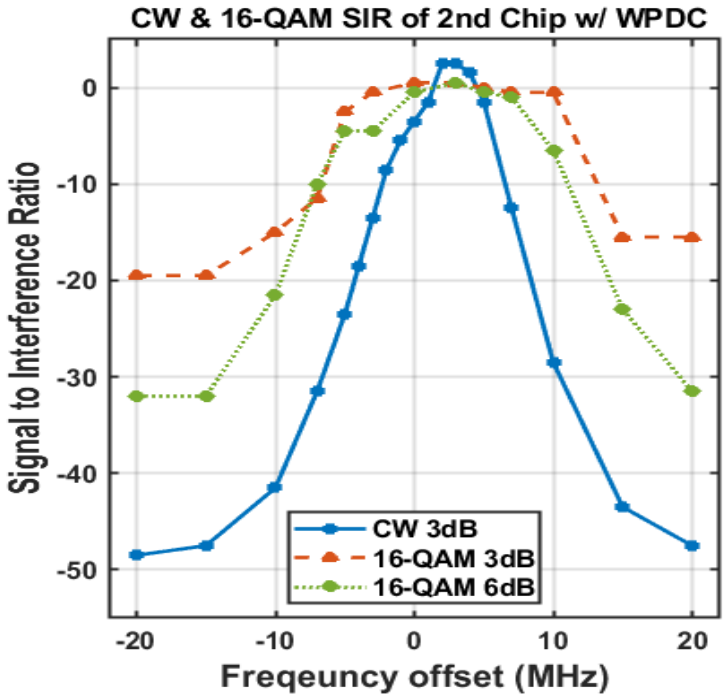


Fig. 5.20. Measured interference tolerance to CW and 16-QAM (10Mbaud) in WPDC mode

The measured signal to interference (SIR) for CW and 10Mbaud PRBS7 16-QAM signals are shown in Fig. 5.20 for the 2nd sample in the WPDC mode for 10ms latency mode. The CW interference is measured with the desired signal kept 3dB above the sensitivity level. The 16-QAM is measured for both 3dB and 6dB desensitization levels. WPDC performs well against CW interference with -47.5dB SIR at 20MHz offset. The SIR corresponding 16-QAM improves nonlinearly from -19.5dB for 3dB desensitization to -32dB for 6dB desensitization due to the carrier sense operation.

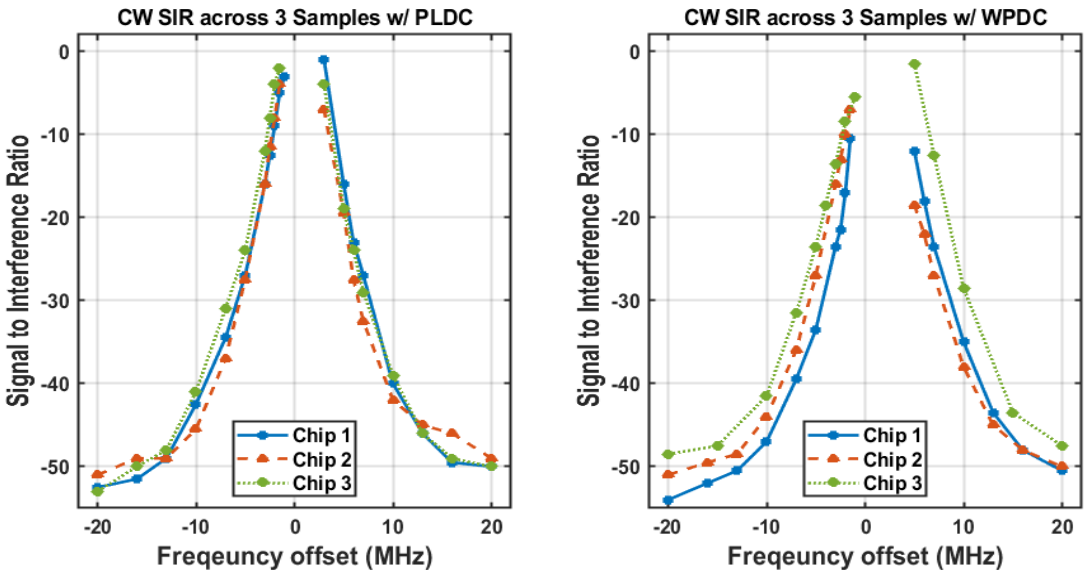


Fig. 5.21. Measured interference tolerance to CW for PLDC and WPDC modes

Fig. 5.21 shows the 3dB desensitization SIR for CW interference for both the PLDC and WPDC modes for comparison. All three samples achieve near -50dB SIR at 20MHz offset in the PLDC mode while the SIR somewhat fluctuate in the WPDC mode due to guard-band size. These results indicate that improving the frequency stability of the VCO can in-turn improve SIR by enabling a smaller the IF LPF bandwidth.

The performance of the 2nd sample is compared against the prior state-of-art 2.4GHz work in table 5.3. The presented work achieves a state-of-art combination of sensitivity, latency, and dc-power. The dc-power versus sensitivity plot of prior state-of-the-art work including the contributions of this work shows that this work achieves the lowest power among better than -90dBm sensitivity receivers at low latency.

Finally, Fig. 5.23 shows the power versus latency with respect to the PLL duty factor for the within packet duty-cycled case. When the PLL is rarely used as explained in the wake-up receiver architecture section (10s period with 2ms on time leading to 50nW of power), the total estimated power is close to the 0% duty cycle of the PLL. Due to the sparse calibration of the VCO, the sensitivity corresponding to this case is the minimum value. However, as the PLL duty cycle is increased, the uncertainty of the IF is reduced. The actual uncertainty must be calculated based of factors such as the temperature variation between the calibration periods as well as the inherent short-term instability of the VCO, and hence can be challenging to derive numerically.

Table 5.3. Performance comparison with prior state-of-the-art wakeup receivers at 2.4GHz

	Heterodyne												ED-First	
	This Work						[2] JSSC '21		[14] JSSC '16	[3] CICC '18		[11] JSSC'18	[15] JSSC'19	[5] ISSCC '16	[6] RFIC '17
Sensitivity (dBm)	-91.5*			-93.5*			-92*		-97**	-80**	-74**	-72**	-92.6***	-56.5**	-61.5**
Power (µW)	20.9	2.0	0.9	189	12	2.0	352	4.4	99	0.24	0.185	95	495	0.236	0.365
Latency (ms)	10	100	1k	10	100	1k	1.47	1k	n/a	12.5k		n/a	n/a	3.9[1]	12.8[1]
SIR (dB @ offset)	CW[2]: -2/-28.5/-47.5 @ 5/10/20MHz 16-QAM: -19.5[2] / -32[3] @ 20MHz						-12.5/-21.7 @ 2/24MHz -67.5[4] @ 2 to 24MHz		-25/-31 @ 3/5MHz	n/a		-20dB @ 20MHz	CW: -57 @ 20MHz WiFi: -49 @ 25MHz	n/a	CW: -19.1dB @ 3MHz offset
RX Bit-Rate (kbps)	8.192						n/a		10	83		62.5	62.5	8.192	2.5
RF Signal	OOK (CE-OOK)						MC-OOK (WiFi) + Back-channel BLE		OOK	GFSK (BLE)		MC-OOK (WiFi)	MC-OOK (WiFi)	Back-channel BLE	OOK
Power Saving Method	Within-Packet Duty-Cycled			Duty-Cycled			Duty-Cycled		High-Q Off-chip comp.	Duty-Cycled	Bit-Level	Duty-Cycled[5]	Duty-Cycled[5]	Passive RF	Passive RF
Off-chip RF Components	None						Matching Network[6]		Matching + LO Inductors	Matching Network		None	None	Matching Network	Antenna Match
LDO integration	Yes						No		No	No		No	Yes	Yes	No
Core Voltages (V)	0.6 / 1						0.5		0.5	0.75		0.95	0.9 / 0.6	0.5 / 1 / 2.5	1 / 0.8 / 0.5
Tech. (nm)	65						65		65	65		14	28	65	65
Chip Area (mm²)	2.24						0.6		0.0576	4		0.19	0.13	2.25	1.1

* Wakeup error ratio (= Missed detection ratio) at 0.1% ** Bit error ratio at 0.1% *** Packet error ratio at 10% [1] Calculated from the correlator length
[2] 3dB desensitization [3] 6dB desensitization [4] With frequency hopping enabled [5] Not demonstrated in the publication [6] According to the shown schematic

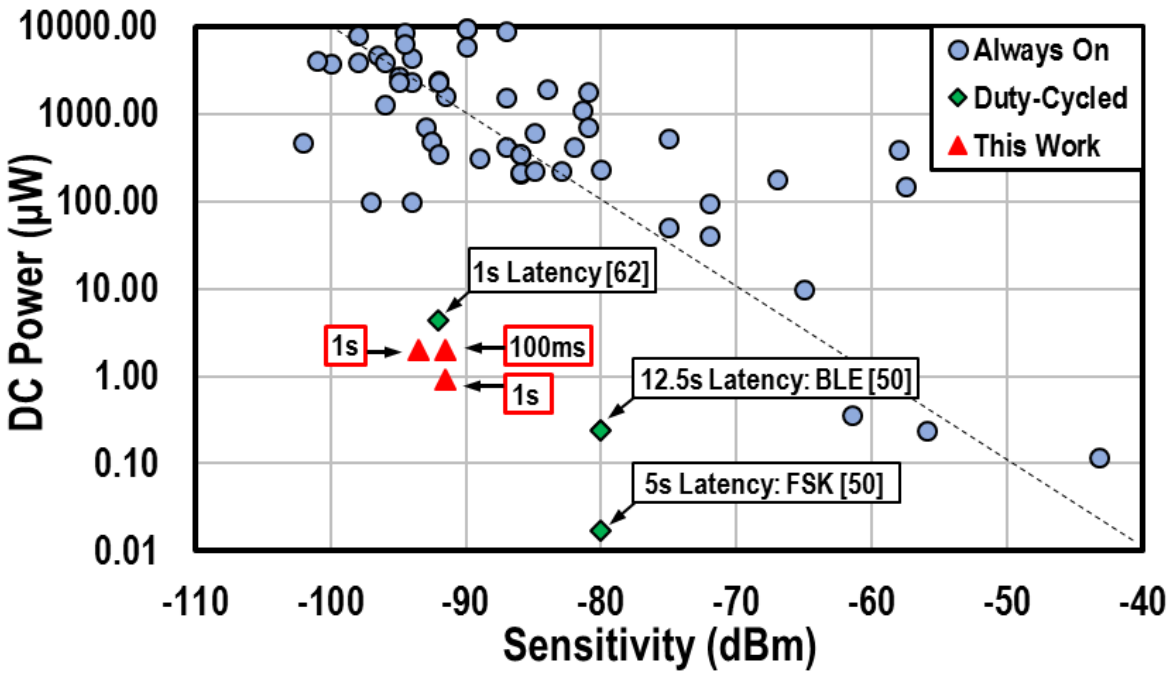


Fig. 5.22. DC power versus sensitivity for 2.4GHz work including contributions of this work.

However, as the PLL duty factor increases and reaches the maximum value given by the receiver duty factor, the architecture changes from an uncertain-IF to a heterodyne. The sensitivity corresponding to this case can be numerically. The sensitivity improvement comes at the cost of dc-power increment and this trade-off is captured in Fig. 5.23 where the two curves corresponding to the duty-cycle of 0 and 100% of the PLL.

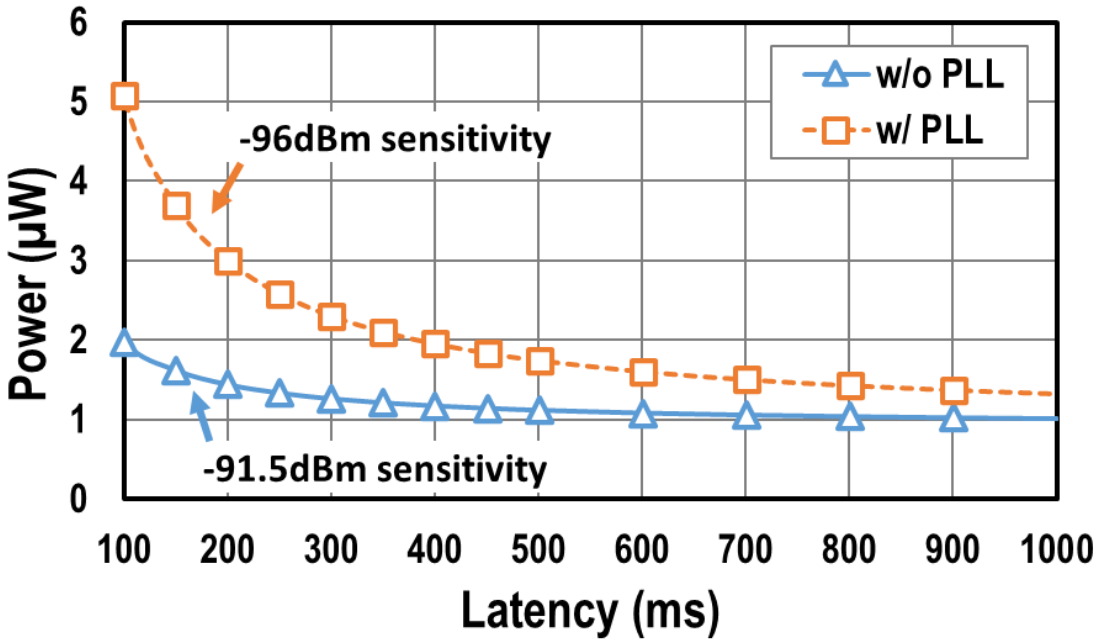


Fig. 5.23. DC power versus latency for 0% and 100% duty cycle of the PLL with respect to the rest of the wakeup receiver duty-cycle in WPDC mode. PLL settling time of 2ms assumed.

5.6 Conclusion

A design space overview of the popular 2.4GHz ISM band shows that sub-μW power desirable for wake-up receivers and sensitivity near -90dBm required for long range operation has been largely unexplored. Such wake-up receivers combined with low latency operation can enable short to mid-range networks in area constraining home, office, and factory IoT applications. The prior reported state-of-the-art near-μW wake-up receivers operate at high latency of equal to or larger than 1s, which can constrain certain applications. Simultaneously realizing high sensitivity, low latency, and near-μW operation, while withstanding similar levels of interference comparable to the main data receiver (RX) is highly desirable.

Addressing these issues, this work presents a highly integrated wake-up receiver operating at 2.4GHz with -91.5dBm sensitivity, 2μW dc-power, and 100ms latency through: 1) within-packet duty-cycling to improve power and latency up to 9x and 10x, respectively, compared to conventional packet-level duty-cycling (PLDC); 2) U-IF front-end with an on-chip VCO for low-power downconversion to an uncertain 1st IF for improved selectivity; 3) Channel-Embedded OOK (CE-OOK) signaling with BFSK symbol encoding to create a known 2nd IF for channel selective filtering; 4) event-triggered, PLL-based VCO calibration for improved RF oscillator stability; 5) Integrated supply regulators (LDOs) and zero dedicated off-chip RF components for low-volume integration. The contributions of this work can enable

2.4GHz wake-up receiver solutions suitable for low-throughput event-driven mid-range IoT applications.

5.7 Personal Contributions

- Lead the system architecture and design integration efforts.
- Proposed the PLL based event-driven calibration technique for stabilizing U-IF topology.
- Proposed the adoption of CE-OOK for deterministic sub-carrier creation with U-IF.
- Lead the RF and Analog baseband design efforts.
- Co-lead the system testing efforts including PCB design and test setup preparation.
- Co-lead the conference and journal manuscript writing efforts.

Acknowledgements

University of Virginia: Henry Bishop, Steven Bowers, Benton Calhoun, Terry Tigner

Chapter 6

6. Sub-μw Wake-Up Receivers for IoT: A Review and Design Guide[3]

6.1 Introduction

The number of connected devices is rapidly increasing due to the Internet-of-things (IoT). In a post COVID-19 environment, distributed remote sensing can benefit areas such as healthcare, agricultural, infrastructure monitoring, and industrial automation. The CMOS technology scaling helped the design of the low power sensor node circuitry, but it is not trivial to achieve years long operational lifetimes while maintaining high performance and robustness. As an example, a small CR-1227 button-cell battery (0.25 cm^3 volume, 0.8g weight) with 37mAh capacity powering a commercially available two different Bluetooth SoCs (nRF5340 [15] and RSL-10 [16]) with approximately 3mA active current in receive mode will drain the said battery within half a day.

Periodically turning the node on-and-off (also known as duty-cycling) can improve the lifetime but the required duty-cycle can reach prohibitively small values that comes at the cost of increased latency and reduced access time [79]. The lifetime as a function of duty-cycling is shown in Fig. 6.1 for the same example above. Although duty-cycling can reduce the dc-power, it is still a sub-optimum solution for the case where a sensor's information is accessed in an infrequent and on-demand manner. This realization resulted in the concept of wake-up

[3] This chapter includes content from previous chapters

receiver (WuRX) [17] shown in Fig. 6.2, where a dedicated ultra-low power wireless receiver constantly listens for an over the air wake-up trigger command.

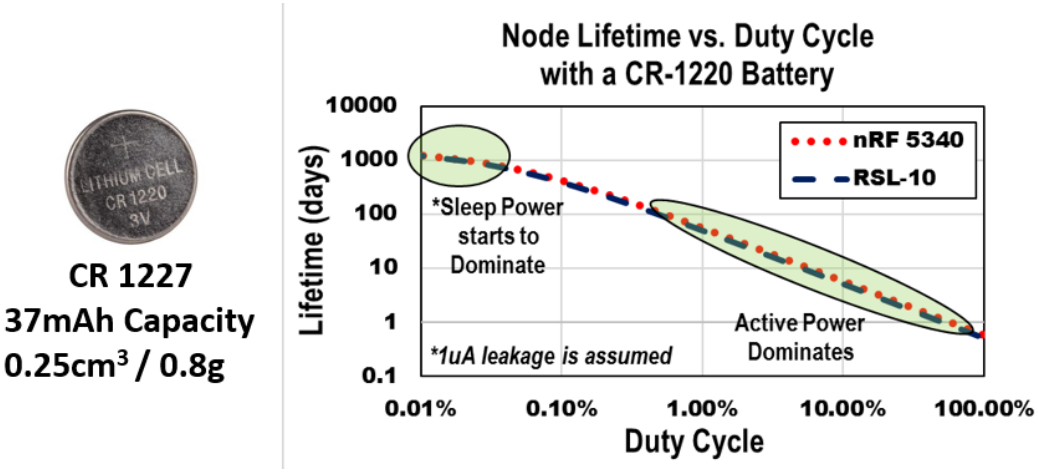


Fig. 6.1. Duty Cycled power of a commercial SoC with a CR-1227 battery

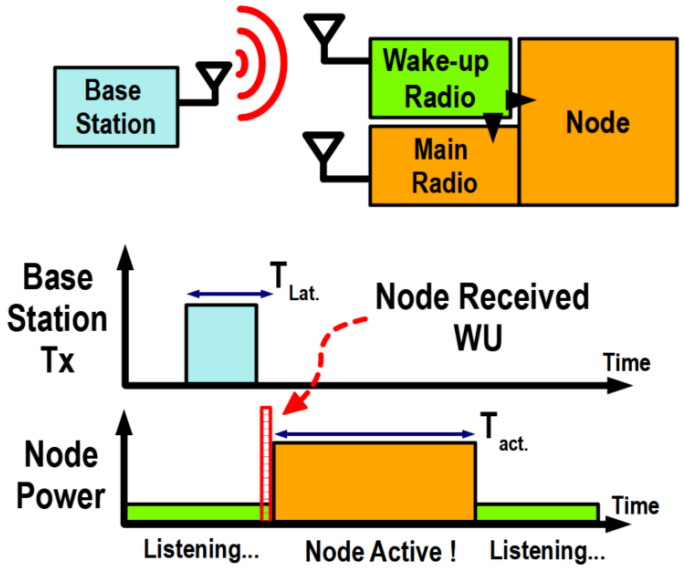


Fig. 6.2. Illustration of the WuRX operation

Compared to the typical data RX, a WuRX is an extremely low power device favoring simple signaling schemes and circuitry leveraging low complexity in demodulation. On-off-keying (OOK) has emerged as the candidate signaling method and included in the IEEE 802.11.ba standard [52]. WuRXs have gained wide attention over the last two decades, producing a multitude of publications. The reported work spans across short-range to ultra-long range, sub-GHz to multi-GHz, and pico-watts to hundreds of microwatts. This is mainly because the IoT design space is highly application specific, thus making it hard to come up with a generalized ‘one-size-fits-all’ solution.

Given the diversity of the IoT application space, a question then arises: **"which WuRX topology would be the best candidate for a given set of user constraints?"**. An answer to this can be formulated by:

1. Categorizing different user needs and relating them to the WuRX design metrics,
2. Identifying the metrics trade-offs and bounds associated with the reported WuRX topologies,
3. Presenting insights and guidelines to select the best topology to satisfy the tradeoffs and user needs.

Rest of this chapter is organized as follows. Section 6.2 introduces common user needs and relates them to the WuRX metrics known to circuit designers. Section 6.3 briefly introduces popular WuRX topologies and identifies the trade-offs and bounds associated with each various design choice. Section 6.4 provides a mathematical analysis and comparison between two simple duty-cycling schemes capable of asynchronous operation. Section 6.5 revisits the user needs in the context of identified WuRX metric trade-offs and reported work. Section 6.6 presents an example demonstrating the selection method presented in this paper with the aid of design space plots. The chapter is concluded in section 7.

6.2 User Needs and Wake-Up Receiver Metrics

Table 6.1. Common user needs and related WuRX metrics.

High Level Spec.	Related WuRX Metrics
Communication distance	Sensitivity
Access time	Latency, Data rate
Lifetime	Average power consumption False alarm rate
Robustness	Signal to Interference ratio Process, voltage, and temperature variations
Form factor	Antenna size Off-chip components Battery or harvester size

Since there can be a wide variety of use cases and each with a set of unique constraints, most common user needs are selected to limit the scope of this work. Table 6.1 indicates these needs and relates them to the performance metrics known to circuit designers. A brief discussion on each need is presented next.

The communication distance (d) is proportional to the sensitivity and the operational frequency as given by the following relationship:

$$\boldsymbol{d} = \sqrt[n]{\frac{P_T G_T G_R \lambda^2}{16\pi^2 \cdot FD_{MG} \cdot P_{MDS}}} \tag{6.1}$$

where n is the path loss exponent, P_T is the transmitted power, G_T is the transmit antenna gain, G_R is the receiver antenna gain, λ is the wavelength of the signal, FD_{MG} is the fade margin, and P_{MDS} is the minimum detectable signal or the sensitivity of the receiver. The calculated communication distance assuming an ideal fade margin of 1, a transmit power of 10dBm, isotropic transmit and receiver antennas, and sensitivity of -80dBm, is shown in table 6.2 for several popular industrial, scientific, and medical (ISM) bands for various loss exponents.

Table 6.2. Communication range example

	Loss Exponent (n)	Range w/ -80dBm Sensitivity and 10dBm TX power		
		434MHz	915MHz	2.4GHz
Free Space	2	1.7km	850m	320m
Urban	2.7	250m	150m	75m
Obstructed in Factories	3	150m	90m	45m
Obstructed in Building	5	20m	15m	10m

According to the table 6.2, the low frequency operation benefits long range communication in free space. For example, the 434MHz operation shows 5 times the range compared to 2.4GHz band operation. However, as the loss exponent increases, the range difference quickly diminish, reaching only twice the distance for heavily obstructed case. This is an important trade-off to keep in mind since the antenna area and thereby the node form-factor inversely trades-off with the frequency. For example, the length of a dipole antenna at 2.4GHz is ~6cm while a 434MHz dipole length is ~33cm. Shrinking the antenna size may cause weaker received signals due to low efficiency, which degrades the communication distance [23].

The wake-up latency is proportional to the average data rate and the address length (correlator code length). Depending on the duty-cycling scheme, the latency either trades-off with the sensitivity or the dc-power. The node lifetime is inversely proportional to the WuRX dc-power and false alarm rate. The false alarm rate is defined as the number of unintended wakeups per unit time due to the antenna thermal noise when channel is quiet. The false alarm rate trades-off with the correlator code-length and therefore, the dc-power shows an indirect trade-off with the latency.

Robustness against the process, voltage, and temperature (PVT) is of great importance for IoT nodes, since industrial applications such as agriculture, mining, and city infrastructure monitoring, may experience harsh operating conditions. The PVT robustness is generally improved by circuit design techniques and is out of the scope for the purposes of this chapter.

The background interference tolerance is a loosely defined metric for WuRXs. It can be argued that a WuRX should tolerate similar interference levels as the main receiver. However, wake-up transmissions are infrequent and may not have a dedicated channel. This can lead to collisions as well as in-band or same channel interference. For the scope of this work, only the adjacent channel and out-of-band interference is considered. The interference tolerance may trade-off with the dc-power consumption due to architecture choice, and node-volume due to off-chip MEMS filtering elements.

The form factor of the WuRX is related to the antenna size, the number of off-chip components, and the battery or harvester size. The antenna size is related to the operation frequency as explained before. The number of off-chip components depends on the architecture choice due to the input matching requirements, interference filtering, LC oscillator inductors, decoupling capacitors, and crystal references etc. Moreover, certain off-chip components may impose limitations on selecting the thickness and the substrate material for the printed circuit board (PCB) used for the system assembly. The battery size trades-off with the power consumption and battery replacement cost, while the harvester area trades-off with available energy sources, storage capacitor size.

6.3 Overview of Wake-Up Receiver Architectures

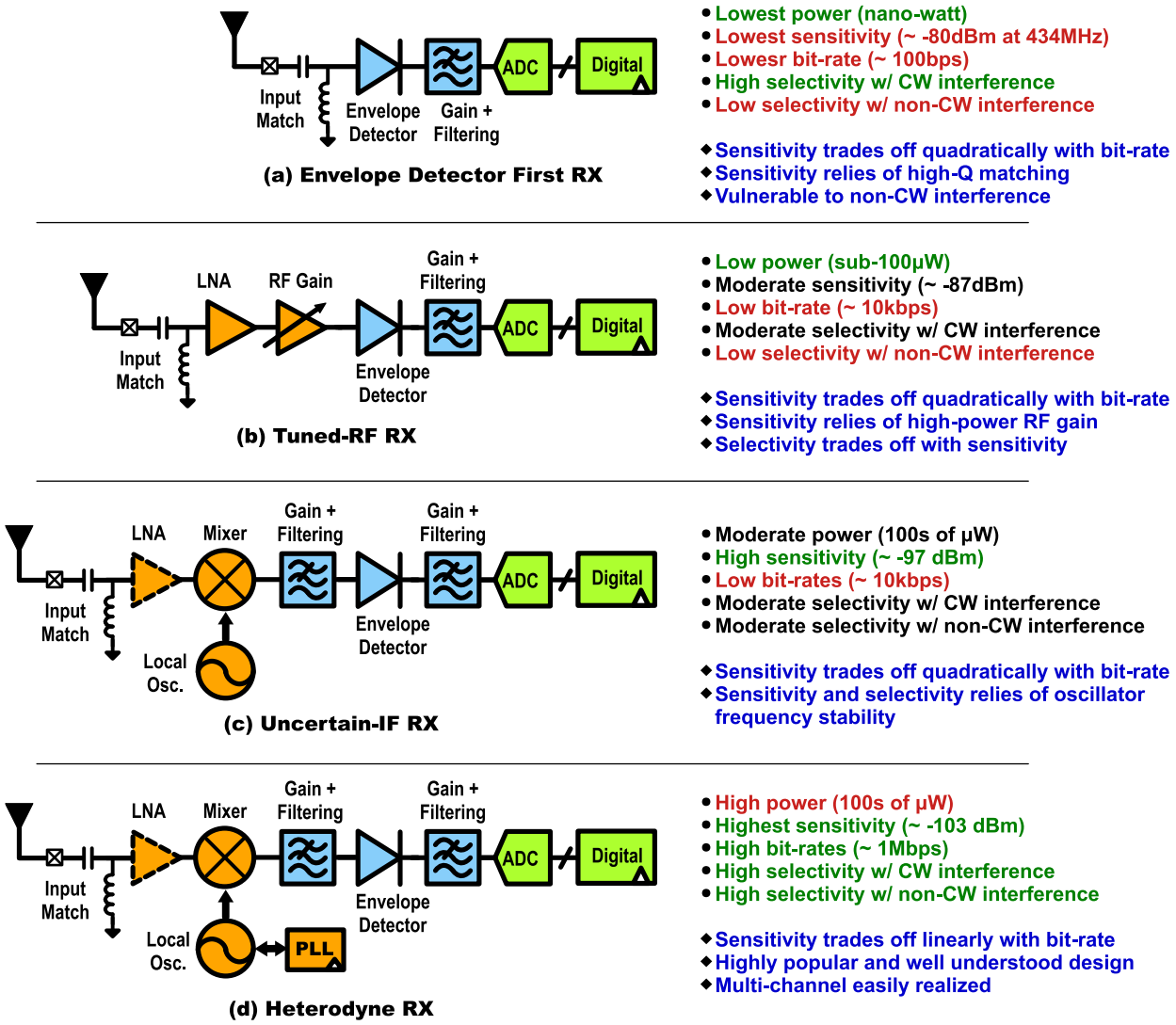


Fig. 6.3. Commonly used WuRX architectures including pros and cons.

Any receiver can potentially operate as a WuRX if the average power consumption can be low. A comprehensive list of such low power receivers can be found in [19]. This article limits the scope to 4 commonly used architectures in recent literature, namely:

1) Envelope Detector 1st (ED-1st)
2) Tuned-RF (T-RF),
3) Uncertain-IF (U-IF),
4) Heterodyne (Het),

in the context of energy detection or non-coherent type detection for low power design feasibility. Fig. 3 shows typical block diagrams of each architecture including pros and cons.

6.3.1 Envelope Detector-First (ED-1st)

The ED-1st topology comprises of an input matching network followed by an RF envelope detector. The rectified output corresponding to the input RF signal can then be further amplified and filtered in the baseband, followed by a thresholding circuit for analog to digital conversion. A digital correlator can be used to detect the wake-up address. Due to the omission of any active RF gain circuits and feasibility of passive diode-based square-law rectification, the ED-1st topology achieves the lowest dc-power among the reported WuRXs, as low as pico-watts [34]. Given the high output spot noise of rectifiers, the sensitivity needs to be traded-off for latency. The sensitivity is further improved by adopting passive voltage boosting input matching network, but this requires high-quality factor inductive elements. The sensitivity (P_{MDS}) of an optimally input matched Dixon ED-1st WuRX can be approximated by [63]:

$$P_{MDS}(dBm) = 5log_{10}(16 \cdot K_B T) + 5log_{10}(BW_{BB}) + 5log_{10}(SNR_{min}) + 5\log_{10}(NF_{BB}) - 5log(R_s) - 10log_{10}(\mu_{det}) + 30dB \quad (6.2)$$

where K_B is the Boltzmann constant, T is the physical temperature in kelvin, BW_{BB} is the baseband bandwidth corresponding to the data rate, NF_{BB} is the baseband noise-factor, SNR_{min} is the desired signal to noise ratio, R_S is the transformed resistance of the antenna through the matching network, and μ_{det} is the open circuit voltage sensitivity (OCVS) of a single diode stage in the ED. Although the above expression is derived in the context of a Dixon charge-pump type ED, it provides a good approximation for the triode-mode Dixon [68] and passive gate-biased self-mixer [63] based EDs as well. Assuming a required SNR of 12, baseband noise-factor of 2, source resistance of 25kΩ, OCVS per stage of $10V/V^2$, and 1 bit per second provides a maximum sensitivity of -91dBm.

The condition for the optimum input matching requires the input impedance of the ED to be equal to the parallel equivalent resistance of the inductor at resonance [31, 63]. For a given rectifier topology and the inductor Q-factor, the sensitivity can be traded-off for latency as shown by the $5\log_{10}(BW_{BB})$ term of eq. (6.2). The sensitivity also trades-off with the dc-power loosely due to the NF_{BB} term, which relates to the baseband circuits. The baseband dc-power consumption can be somewhat adjusted by adopting a large number of rectifying stages, which leads to a high output impedance. But the penalty paid is the slow rise time of the ED, which may lead to low data rates. These trade-offs are shown in Fig. 6.4.

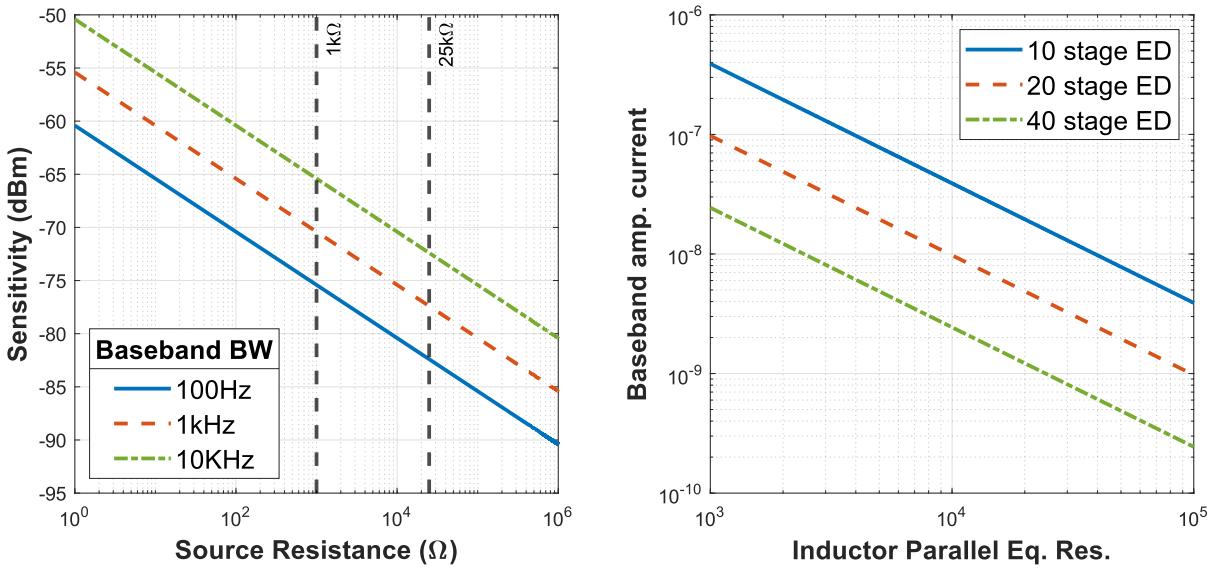


Fig. 6.4. (a) Sensitivity as a function of source resistance for various data rates, (b) baseband current as a function of source resistance for various numbered EDs.

The vertical dashed lines in the Fig. 6.4-(a) are typical Q-factors corresponding to an on-chip inductor at 2.4GHz (1kΩ) and off-chip inductor at 434MHz (25kΩ). The state-of-the-art work in ED-1st WuRXs have demonstrated near -80dBm sensitivity while maintaining several nano-watts of power at near 100Hz baseband bandwidth, which agrees well with the above plots.

Due to the inherent envelope detection operation, the ED-1st WuRXs are strongly vulnerable to non-constant-wave (NCW) type interference. The constant-wave (CW) interference can be filtered out by capacitive coupling or adopting an automatic threshold recovery scheme [31]. The Interference suppression may be improved by adopting an envelope modulated signaling scheme to enable baseband channel filtering. Several examples are the two-tone OOK [38], the wide-band 2-tone OOK [39], and the single tone channel-embedded OOK [71] signaling schemes.

6.3.2 Tuned-RF (T-RF)

The tuned-RF topology adopts active-RF gain prior to the rectifier. The added gain can extend the sensitivity beyond the limitations of ED-1st at the cost of dc-power. However, high RF-gain also contributes to a phenomenon called ‘noise-self mixing’, due to the high-gain seen by wideband thermal noise of the antenna and the amplifiers prior to the ED. Assuming a noiseless baseband, the sensitivity of a T-RF RX can be approximated by [64]:

$$P_{MDS}(dBm) = 10\log_{10}(2K_BT) + 10\log_{10}(NF_{RF}) + 5\log_{10}(BW_{RF}) + 5\log_{10}(BW_{BB}) + 5\log_{10}(SNR_{min}) \quad (6.3)$$

where NF_{RF} is the frontend noise-factor and BW_{RF} is the noise equivalent bandwidth prior to ED. Above expression also assumes that the BW_{RF} is much wider than the BW_{BB} term.

Assuming a front-end noise figure of 20dB, a front-end bandwidth of 100MHz, a baseband bandwidth of 1Hz, and a required SNR of 12.5 leads to a -115dBm sensitivity, a value 15dB better than the ED-1st case. The prior art T-RF at higher baseband bandwidths (~0.5-1kHz) have demonstrated sensitivities near -100dBm [71] with only a matching network, and as high as -108dBm [69] at the cost of off-chip high-Q MEMS resonators to limit the BW_{RF} at sub-GHz frequencies. However, the adoption of active gain requires a duty-cycling scheme to reduce the average power to sub-μW scale. Addition of high RF gain also negatively affects the interference tolerance [38, 39]. Adopting an envelope modulated signaling scheme may alleviate this issue to a certain degree similar to the ED-1st case.

6.3.3 Uncertain-IF (U-IF)

The uncertain-IF architecture adopts a free-running oscillator to down-convert the high-frequency input signal to a relatively low (but uncertain) intermediate frequency. In Essence, the U-IF can be thought of as a T-RF receiver with a frequency shifting operation prior to the ED. The main advantage of the U-IF is that high-gain can be realized at the uncertain IF region for relatively low dc-power. The penalty paid is the dc-power dissipation of the RF oscillator. Moreover, since the high-gain occurs at low frequencies where the coupling effects are relatively weaker, the U-IF topology can be more stable than the T-RF, where high RF gains can lead to front-end instability. Due to the similarity to T-RF, the sensitivity of the U-IF can also be approximated by eq. (6.3) when double sideband noise-factor is used for the complete RF signal chain prior to the ED. For the same example case as T-RF above, limiting the RF bandwidth to 1MHz can provide a sensitivity of -125dBm, a 10dB improvement over the T-RF.

The U-IF RX can realize superior interference tolerance over the T-RF, if the uncertainty of the free-running local oscillator (FR-LO) can be lowered. This can be accomplished by opting for a robust oscillator topology, such as LC with high-Q components [47], initial calibration [48], or built-in run time calibration methods [80]. For the example above, the T-RF receiver would be vulnerable to interference within a 100MHz bandwidth, while the U-IF receiver is only vulnerable within a 2MHz (considering the image). High FR-

LO stability of the U-IF also reduces the BW_{RF} component and enables a smaller bandwidth for the low-pass filter after the mixer.

6.3.4 Heterodyne (HET)

Permanently stabilizing the FR-LO of the U-IF leads to the heterodyne receiver topology. Since the IF frequency is now deterministic, the BW_{RF} portion of eq. (3) can be equal to BW_{BB}. The precise sensitivity in this case can be derived by using the definition of noise-Fig. for a coherent receiver and given by:

$$P_{MDS} = 10\log_{10}(K_B T) + 10\log_{10}(NF_{sys}) + 10\log_{10}(BW_{BB}) + 10\log_{10}(SNR_{\min}) \qquad (4)$$

where NF_{sys} is the system noise figure prior to the bit decision circuit. Adopting a phase or frequency locked loop (PLL of FLL) with a programmable synthesizer can enable RF channel selection. Thus, the heterodyne topology is arguably the most popular choice due to the superior selectivity and sensitivity. However, due to the complexity, the heterodyne architecture tends to consume a high amount of dc-power while offering vastly superior sensitivity, selectivity, and interference tolerance to any of the prior discussed architectures.

For the same example above, the sensitivity of heterodyne RX is -153dBm, 38dB better than the T-RF and 28dB better than U-IF.

6.4 Duty-Cycling Analysis

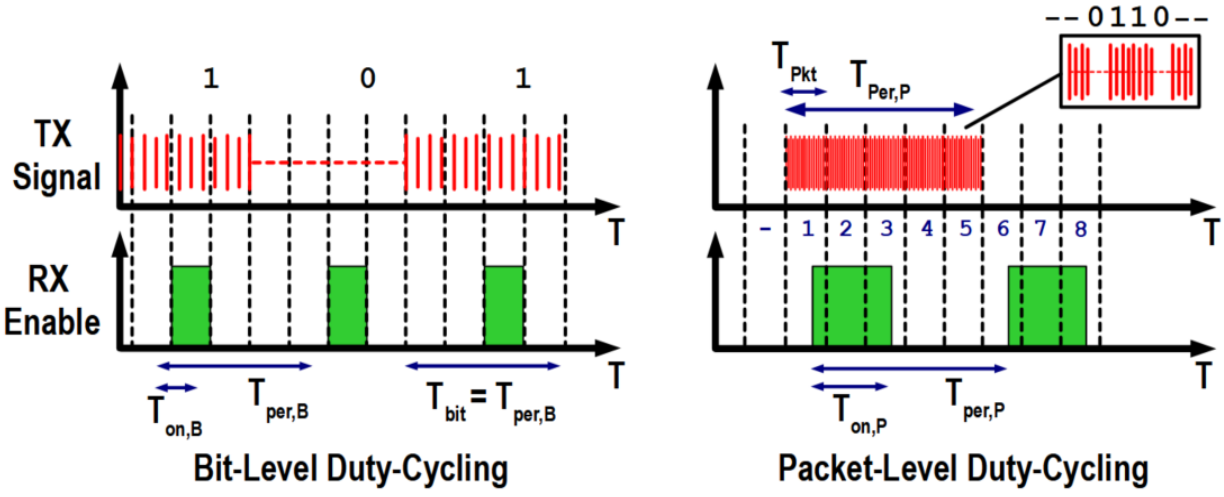


Fig. 6.5. Bit-level and Packet-level duty-cycling. BLDC senses a portion of each bit, while PLDC senses a portion of a transmitted packet.

Given the high dc-power associated with the T-RF, U-IF, and HET architectures, a duty-cycling scheme must be adopted if sub or near-μW operation is desired. Although

numerous complicated duty-cycling methods have been considered in the literature [52], this chapter focuses on two simple duty-cycling schemes, the bit-level duty-cycling (BLDC) and packet-level duty-cycling (PLDC), to limit the scope. Both these methods can be easily used in an asynchronous operation, where the receiver has no prior information about the transmitter. The Fig. 6.5 shows both schemes for comparison.

Bit-level duty-cycling senses a small portion of the transmitted bit while packet-level duty-cycling attempts to capture a full packet in a repeated *M* number of transmitted packets. Average power, latency, and baseband bandwidth are affected by each duty cycling method and warrants attention when various metrics are equalized. The table 6.3 illustrates various cases when instantaneous power is P_{inst}, abrupt start-up with no delays, and wakeup message is N bit long.

Table 6.3. Analysis of BLDC vs. PLDC

	BLDC	PLDC	Comments
Same DC Power and On time:		$\frac{T_{on,B}}{T_{per,B}} = \frac{T_{on,P}}{T_{per,P}}$, $T_{on,B} = T_{on,P}$	
Power	$P_{inst}\frac{T_{on,B}}{T_{per,B}}$	$P_{inst}\frac{T_{on,P}}{T_{per,P}} = P_{inst}\frac{T_{on,B}}{T_{per,B}}$	=
Latency	$N.T_{per,B}$	$T_{per,P} = \frac{T_{per,B} \cdot T_{on,P}}{T_{on,B}}$	PLDC: Better Latency
Baseband BW	$\frac{0.35}{T_{on,B}}$	$\frac{N}{T_{on,P}} = \frac{N \cdot T_{per,B}}{T_{on,B} \cdot T_{per,P}}$	PLDC: 3N Higher BW
Same DC Power and Latency:		$T_{per,P} = N \cdot T_{per,B}$	
Power	$P_{inst}\frac{T_{on,B}}{T_{per,B}}$	$P_{inst}\frac{T_{on,P}}{T_{per,P}} \Rightarrow P_{inst}\frac{T_{on,P}}{N \cdot T_{per,B}}$	PLDC: N times longer on-time
Latency	$N \cdot T_{per,B}$	$T_{per,P} = N \cdot T_{per,B}$	=
Baseband BW	$\frac{0.35}{T_{on,B}}$	$\frac{N}{T_{on,P}} \Rightarrow \frac{1}{T_{on,B}}$	PLDC: 3X higher BW
Same Sensitivity:		$T_{on,P} = \frac{N \cdot T_{on,B}}{0.35}$	
Power	$P_{inst}\frac{T_{on,B}}{T_{per,B}}$	$P_{inst}\frac{T_{on,P}}{T_{per,P}} \Rightarrow \frac{1}{0.35} \cdot P_{inst}\frac{T_{on,B}}{T_{per,B}}$	PLDC: 3X worse power for same Latency
Latency	$N \cdot T_{per,B}$	$T_{per,P} \Rightarrow T_{per,B} \cdot \frac{N}{0.35}$	PLDC: 3x worse latency for same power
Baseband BW	$\frac{0.35}{T_{on,B}}$	$\frac{N}{T_{on,P}}$	=

Generally, the PLDC requires a larger bandwidth to satisfy the Nyquist sampling criterion. The factor of 0.35 associated with the BLDC is the rise time to bandwidth relationship of a low pass system. When the duty-cycling is limited by the minimum on-time, the PLDC can achieve better latency at the cost of reduced sensitivity. If both the average power and latency is made the same, then the BLDC achieves better sensitivity, but the PLDC maintains a longer on-time, which allows the WuRX to achieve a better energy per bit metric. This is

crucial when the non-ideal startup energy effects are considered. The longer on-times also help with the dc-offset settling issues. Conversely, when the baseband bandwidth is held constant, the PLDC achieves either 3X worse dc-power (for the same latency) or latency (for the same power).

This indicates that in a sensitivity and dc-power critical scenario, adoption of the BLDC is preferrable at the cost of a higher latency. The PLDC achieves better latency (or a longer on-time for same latency) at the cost of lower sensitivity, which is useful for latency critical applications. This also benefits systems with start-up or settling times, such as high-Q bandpass filters or PLLs with low frequency references.

Several identified trade-offs for hypothetical duty-cycling parameters are plotted in appendix A.

6.5 Trade-Off Space

The WuRX design is complicated by the highly inter-dependent nature of the metrics presented in the table 6.1. Hence, this section attempts to simplify the process by providing insightful guidelines overviewed in sections 3 and 4, combined with a design space analysis of prior reported work.

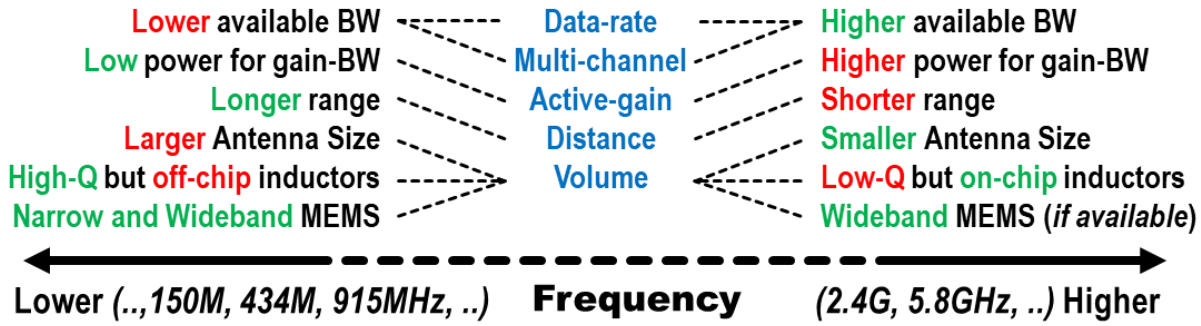


Fig. 6.6. Trade-offs enabled by the choice of operating frequency.

One of the major decisions constraining the available design choices is the RF carrier frequency. Various trade-offs enabled by high or low frequency operation is shown in Fig. 6.6. A lower carrier frequency generally helps with the low power circuit design and a longer communication range. However, the required antenna size can be bigger, which negatively affects the node volume. The inductors required for the input matching and LC oscillators at lower RFs are also area consuming and generally restricted to the off-chip domain. In

conclusion, the low frequency operation leads to a large communication range while requiring considerably large footprint. This is ideally suited for large-scale distributed and out-door networks such as agriculture and farming.

Conversely, higher carrier frequencies require high active power but benefit from smaller antenna area and on-chip inductors, which enable integrated low volume systems. High bandwidths can support a high number of simultaneously accessible nodes by employing multi-channel communications and efficient spectrum management. Due to high-integration factor, higher path-loss, and availability of larger bandwidths, high frequency operation is ideally suited for short or mid-range indoor networks with large number of node density.

Fig. 6.7 shows the dc-power versus normalized sensitivity of several prior state-of-the-art literature for both sub-GHz and multi-GHz regions [19]. The normalized sensitivity metric is defined below and captures the dependency of sensitivity due to baseband bandwidth. i.e., the normalized sensitivity corresponds to the hypothetical case of 1Hz data-rate of 1s latency, and much similar to the classical noise-Fig. definition.

$$Norm\_Sens._{1.} = Sens. - 10\log_{10}(data\_rate) \tag{6.5}$$

(for Heterodyne RX)

$$Norm\_Sens._{2A} = Sensitivity - 5\log_{10}(data\_rate) \tag{6.6}$$

(for ED-1st, T-RF, & U-IF)

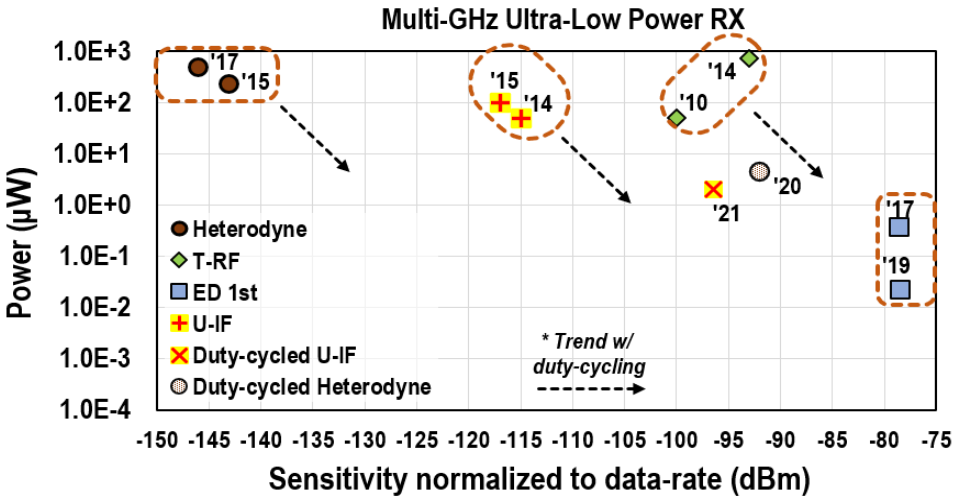
or

$$Norm\_Sens._{2B} = Sensitivity + 5\log_{10}(latency) \tag{6.7}$$

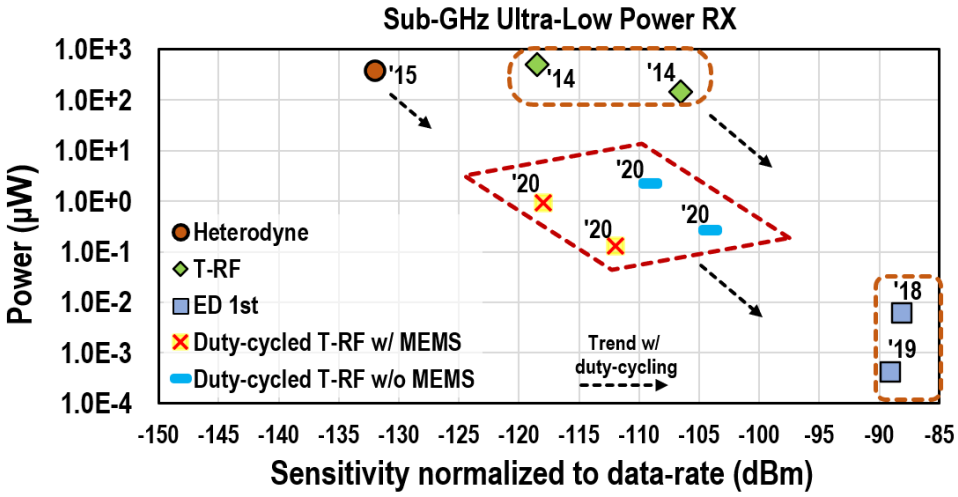
(for ED-1st, T-RF, & U-IF)

The factor of 5 or 10 associated in the *data_rate* term corresponds to the square root or linear dependency of sensitivity to baseband bandwidth in eqs. (6.3) and (6.4).

Two bounds on the design space shown in the Fig. 6.7 can immediately be identified at the top-left (high power, high sensitivity) and the bottom right (low power, low sensitivity) edges. The heterodyne topology achieves the best sensitivity but also consumes the highest amount of power, while the ED-1st consumes the lowest power but achieves the lowest sensitivity. Higher frequency ED-1st suffers from a lower sensitivity since voltage boosting from the input matching is reduced due to the low-quality factor of inductive components at multi-GHz range.



(a)



(b)

Fig. 6.7. Power vs. normalized sensitivity trends of (a) sub-GHz and (b) multi-GHz WuRX.

The T-RF topology achieves moderate dc-power for moderate sensitivity and the power can be reduced to sub-µW levels with duty-cycling. This moves the receiver operating points diagonally downwards and the duty-cycling trends are shown in dotted-lines. Sensitivity can be improved by adopting high-Q narrowband MEMS components to achieve a lower noise equivalent bandwidth (ENB) prior to the rectifier [69]. But the MEMS components result in a large-node area as well as a higher integration cost.

The U-IF topology achieves better sensitivity than the T-RF in multi-GHz range since higher frequency T-RF suffers from a larger ENB. The U-IF can reduce the ENB with better lowpass filtering after the mixer stage, if the LO frequency stability can be improved. Hence, techniques such as high-Q off-chip inductors for the LC oscillator [47] and built-in calibration methods [80] have been adopted in reported literature. The U-IF also lends more easily to duty-cycling than heterodyne due to the omission of a PLL and high-power crystal references.

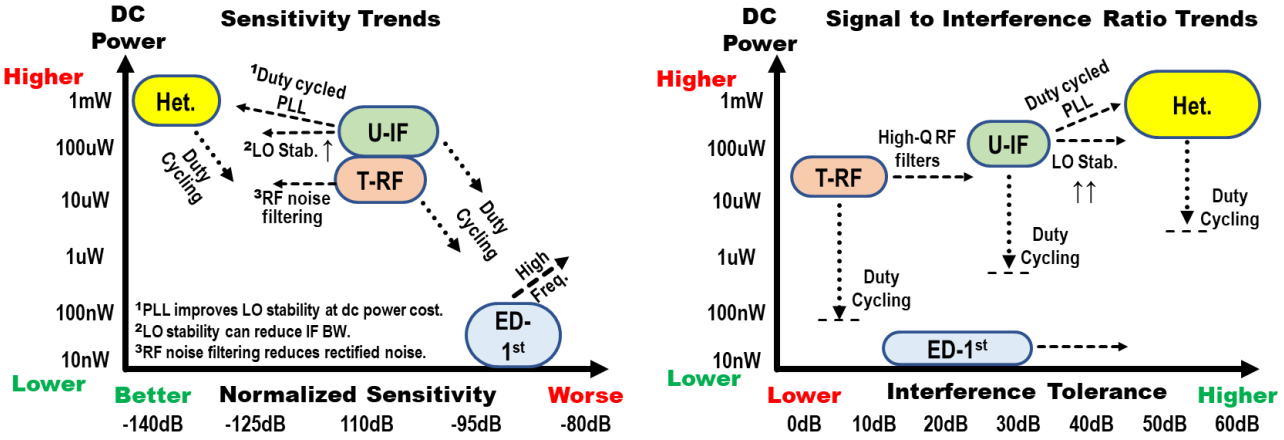


Fig. 6.8. Trade-off space for Power vs. (a) Normalized Sensitivity and (b) Signal to Interference ratio.

The summary of the identified operating space trade-offs are shown in Fig. 6.8-(a). The ED-1st and heterodyne occupies the edges of the operating space with respect to sensitivity and power. The in-between regions can be realized with heterodyne, U-IF, or T-RF combined with duty-cycling. Sensitivity of the T-RF can be improved with MEMS based ENB limiting filters. Similarly, the sensitivity of the U-IF is improved with calibration techniques.

The signal to interference ratio (SIR) trends are shown in Fig. 6.8-(b) for a side-by-side comparison with sensitivity trends. The prior ULP work shows a lack of reporting of SIR metric due to the emphasis on sensitivity improvements. However, the SIR becomes highly important if the WuRX is expected to operate in a crowded area with increased number of potential interference sources. Among the interference trends, the Heterodyne achieves the best performance due to the ease of high-Q filtering at the baseband. Both the ED-1st and T-RF cannot achieve any baseband filtering without incorporating a channelized signaling scheme.

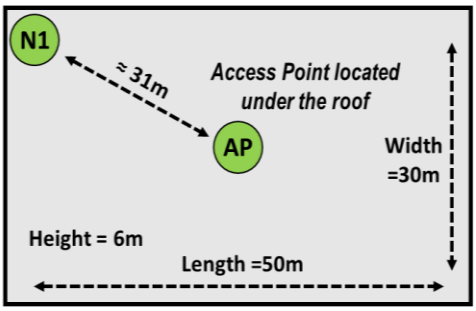
Even with a channelized signaling scheme, the reported T-RF work have achieved poor SIR [38, 39, 71], which can be attributed to front-end non-linearity due to the high RF gain required for maximizing the sensitivity. The benefit of channelized signaling methods seems

to be the capability of ac-coupling the ED output to the baseband, which alleviates large dc-offsets due to the noise-self mixing effect [71]. The prior work adopting channelized signaling schemes lowered the front-end gain to achieve a better SIR, but this also lowered the maximum sensitivity [38, 39]. Hence, further proof-of-concepts are required to conclude that the channelized signaling can provide reasonable SIR while maintaining the maximum sensitivity.

A straightforward way to improve the SIR metric of the ED-1st and T-RF is to either adopt a high-Q input matching or a front-end MEMS filter. Both the choices lead to off-chip component integration and sub-GHz operation. The U-IF topology can realize better SIR even with a wideband input match due to the selectivity offered by the downconversion and filtering operation. Similar to the sensitivity improvement of the U-IF, the SIR is also enhanced by a higher LO stability. The Fig. 6.8 captures the insights related to the SIR trends as well as the approximated minimum power floor with duty-cycling. Minimum power floor is approximated from the values reported from prior art as well as considering the complexity of the system.

6.6 A Design Example

A simple step by step design example to illustrate the applicability of the information covered in this article is shown in this section. The selected example is a warehouse tracking application, and the dimension of the required serviceable area is shown in Fig. 6.9, along with the other desired user specifications. A single access point located in the middle of the warehouse at roof height is assumed for simplicity. This leads to a maximum required communication distance of ~ 31 meters. The path loss exponent corresponding to obstructed in-building case (n=3), a fade margin of 15dB, and a maximum transmit power of 10dBm is assumed for this exercise.



High Level Spec.	Related WuRX Metrics
Distance	Max 32m
Latency	< 1s
Lifetime	1 year
Signal to Interference Ratio	-20 dB
Other requirements	Miniature node attachable to goods. Omni directional antenna. CR-1220 battery (36mAh capacity).

Fig. 6.9. Simplified example case for a warehouse IoT application.

First, the average power available to the WuRX needs to be calculated. The lifetime of 1 year with a 36mAh battery translates to approximately a 4µA of average current assuming the WuRX dominates the total power. A safer power margin can be established if the power consumption is purposefully limited to 3µA, i.e., 25% lower than required. With a battery voltage of 3V, and a local supply voltage of 1V, and an ideal power converter, this translates to a 9µW dc power available for the WuRX. This requirement is well within the reachable power with any of the discussed topologies. If this requirement cannot be met, then either the battery or the harvester size must be increased.

Table 6.4. Sensitivity with a miniature antenna.

Carrier Freq.	Sensitivity w/ ideal ant.	Antenna	Mean Ant. gain	Required Sensitivity
434 MHz	-70 dBm	12x4 mm^2 (Yageo ANT1204LL20R0433A)	-5 dBi	-75 dBm
915 MHz	-76 dBm	12x4 mm^2 (Yageo ANT1204F005R0915A)	-4 dBi	-80 dBm
2.4 GHz	-85 dBm	3.2x1.6 mm^2 (Yageo ANT3216LL00R2400A)	-1 dBi	-86 dBm
5.5 GHz	-92 dBm	1.6x0.8 mm^2 (ANT1608LL14R2455A)	-3 dBi	-95 dBm

Latency of 1 second makes the normalized sensitivity to be identical to the sensitivity of the WuRX. The table 6.4 shows the required sensitivity values for four different ISM bands assuming a typical miniature chip scale antenna. The calculation first assumes an ideal antenna, and then incorporates the effect of antenna gain or loss. As expected, the 434MHz operation leads to the lowest required sensitivity but the antenna size is considerably large. Moreover, the 434MHz operation will also requires a bulky off-chip inductor for input matching purposes. For the ED-1st example sensitivity case in the section 6.3.1, selecting a baseband bandwidth of 32 bps (1 second latency with a 32 bit correlator code) provides a sensitivity of -83dBm, which can satisfy both the 434MHz and 915MHz. The extra sensitivity margin of 8dB for 434MHz and 3dB for 915MHz means that there is room for inductor Q factor (thereby area) trade-off with the sensitivity.

The 5.5GHz antenna occupies a much smaller footprint as well as benefitting from integrated on-chip inductors, but the required sensitivity (-95dBm) to cover the distance can be challenging. Hence, the 5.5GHz operation can be discarded from the list.

To decide which topology leads to the best-case design with least number of trade-offs, Fig 6.7 and Fig. 6.8 can be used. The identified operating region is shown in Fig. 6.10. Since the required normalized sensitivity is below -86dBm (i.e., a moderate to low value), and dc-

power is near 3uW, the heterodyne architecture can be omitted as a choice. A Sub-GHz ED-1st WuRX may easily satisfy the normalized sensitivity, dc-power, and SIR constraints, but leads to a large node volume due to the use of a larger antenna and an off-chip matching network. The multi-GHz ED-1st can provide a highly integrated solution, but the required sensitivity cannot be realized according to fig. 8 for the desired normalized sensitivity, hence ED-1st at multi-GHz can also be discarded as a choice.

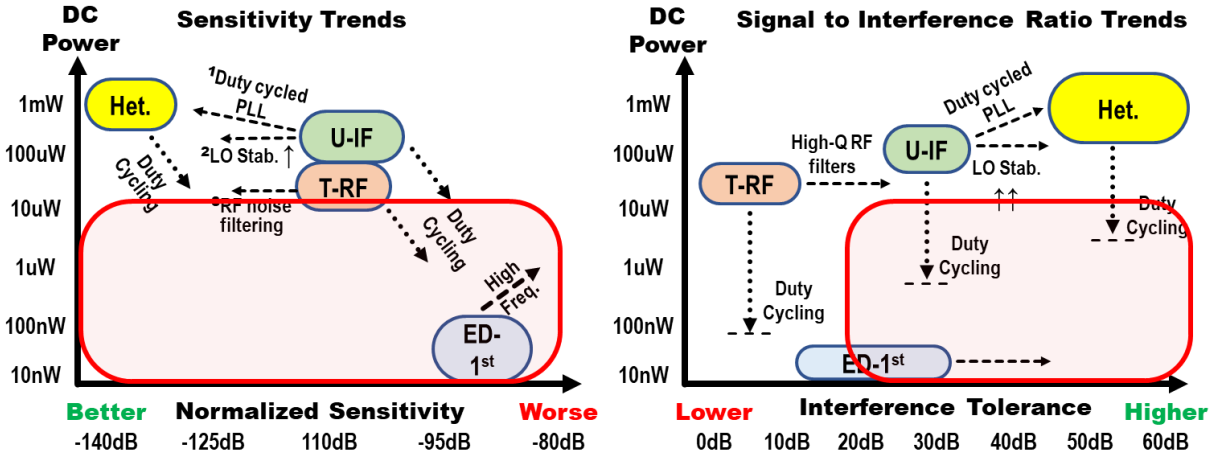


fig. 6.10. Identified operation regions in the trade-off space plots

From a duty-cycling standpoint, either of the BLDC or the PLDC schemes can be adopted due to the relaxed sensitivity and latency requirements. However, BLDC may impact the SIR requirement of 20dB due to the interference up-conversion effect and requires careful analysis depending on the resulting on-time. Thus, for the sake of simplicity, the PLDC can be selected as the possible duty-cycling method.

The actual calculation of the duty cycling parameters requires the knowledge of T-RF and U-IF receivers available to the designer. For this exercise, let us assume the instantaneous dc-power of the T-RF consumes 100uW and the U-IF consumes 400uW. This means that the maximum on-time per second for the T-RF is 90ms and the U-IF is 22.5ms to meet the 9uW duty-cycled power. Assuming the on duration is two packets long and the correlator length is 32 bits, the bit duration for T-RF is 1.40625ms while the U-IF is 0.3515625ms. Then, the baseband bandwidths corresponding to T-RF is 0.712kHz and U-IF is 2.845kHz. For the same example cases in section 6.3, the maximum achievable sensitivity for T-RF is -91.3dBm and U-IF is -98.2dBm, both of which are well within the requirements for 434MHz, 915MHz, and 2.4GHz bands. If desired, this additional sensitivity can be traded-off for lower average power or better latency.

The T-RF can satisfy the sensitivity requirement but the 20dB SIR calls for a bulky off-chip front-end filter-based solution. If the bandwidth of the front-end filter is chosen to be narrow to provide better in-band SIR, then this also limits operation to sub-GHz regime, where high-Q MEMS filters are readily available. Comparing this with sub-GHz ED-1st, where only a matching network is required, the choice of T-RF can be discarded as a potential topology.

The uncertain-IF architecture can satisfy the specifications including the low footprint requirement. However, this necessitates a calibration scheme to be adopted if better in-band SIR is desired.

Thus, the calibration overhead of a 2.4GHz U-IF topology against the volume trade-off of sub-GHz ED-1st topology must be compared next. Given that the normalized sensitivity required by the ED-1st is more relaxed than the maximum achievable values for the topology, a miniature low-Q off-chip inductor may be adopted to satisfy the low footprint requirement. The ED-1st also consumes much less power than the allocated 3uW budget, so the battery area may be traded-off for the antenna or the matching network area.

Similarly, if the node area is an inflexible decision factor, an embedded PLL based periodic calibration of a multi-GHz U-IF, or an initial one-time calibration scheme can be considered as well. Note that one-time calibration methods may require careful circuit level design to maintain robustness against PVT variations, especially for the LO, while a PLL based on-chip calibration method requires an off-chip crystal to be included in the system.

6.7 Conclusion

The rising popularity of IoT calls for innovative solutions to lower the overall sensor energy consumption and enable long lifetime of wireless sensor nodes. The concept of the wake-up receiver was proposed as an optimum duty-cycling method for latency critical low activity factor applications. The research into WuRXs have produced an abundance of literature but found limited commercial applications. This is likely because the IoT application space is highly user specific, thus, ‘one-size-fits-all’ WuRX does not exist. Each IoT application requires a carefully designed WuRX by considering the various user constraints. Thus, this article provides practical guidelines on selecting the best possible WuRX topology for a given set of application constraints. This is done by 1) relating various user specifications to WuRX performance metrics, 2) identifying the various trade-offs associated with several popular

WuRX topologies and duty-cycling schemes, and 3) selecting the topology closet to requirements with the aid of design space analysis of reported WuRX performance. It is often the case that no topology can simultaneously satisfy all the requirements. In which case, the above procedure can be used to select the topology with least number of trade-offs required or a system level specification adjustment. The selection process is demonstrated with a simple IoT application. The content of this chapter can serve as a tool for IoT system planning with respect to selecting the WuRX architecture.

Acknowledgements

University of Virginia: Steven Bowers, Benton Calhoun

Chapter 7

7. Conclusion and Future Directions

7.1 Conclusions

This dissertation presented analysis and techniques for the design of aggressively duty-cycled wake-up receivers to simultaneously achieve high-sensitivity and sub-µW power levels as required for the mass deployment of the IoT. Starting with an overview of the sensitivity limitations associated with the envelope-detector 1st wake-up receiver topology, this work proposed the adoption of two alternative architectures, the tune-RF and the uncertain-IF, to extend the sensitivity to enable low-power wide area networks. Both the above architectures require duty-cycling to achieve power levels similar to the ED-1st wake-up receivers. Hence, this work investigated two feasible duty-cycling candidates capable of asynchronous operation to alleviate the synchronization overhead. Several prototype wake-up receivers were implemented using a standard 65nm CMOS technology as proof-of-concept demonstrations to validate the proposed improvements. The high-level summary of the proposed design techniques is as follows:

Related to the sub-GHz T-RF research phase:

1) The quality factor of available off-chip and on-chip inductors limit the normalized sensitivity of CMOS envelope detector 1st topology to near -90dBm as shown in the Fig. 2.2. This is evident by the reported work capturing the sub and above 1GHz ED-1st work of the prior decade as shown in the Fig. 2.3.

2) The tuned-RF architecture is a viable candidate for improving the normalized sensitivity beyond the -80dBm limit of the ED-1st topology. But the adoption of active-RF gain leads to high dc-power consumption and a duty-cycling method needs to be adopted. In extreme power constrained applications, the overall power is limited by the minimum on-time for a given latency, and the bit-level duty cycling method can achieve a higher sensitivity than the packet-level case as shown in the section 2.2.2.

3) Bit-level duty-cycling allows for longer bit duration than packet level-duty cycling for a given dc-power, and this leads to the best-case sensitivity of an ED-1st topology as well. Therefore, bit-level duty cycling provides an optimum co-existence of the duty-cycled T-RF with respect to the dc-power, and ED-1st with respect to the sensitivity in the same network.

4) The prior T-RF work was unable to demonstrate sensitivities surpassing -90dBm due to the wide input RF bandwidth prior to the rectification. The rectified noise is not only of the source impedance, but also of the active RF gain stages prior to the detector. Hence, this work adopted a high-Q MEMS resonator prior to the rectifier to boost the sensitivity of the T-RF as shown in Fig. 2.6. With the addition of MEMS filter, a -106dBm sensitivity for 288nW at 240ms latency was demonstrated in the first phase of T-RF research. The 2nd phase research achieves a maximum sensitivity of -108dBm for 0.92µW at 310ms latency. Overall, a 26dB sensitivity improvement over the ED-1st topology is demonstrated while maintaining sub-µW operation and hundreds of milliseconds latency.

5) In addition to the dc-power versus latency, the bit-level duty-cycling method also allows for the unique trade-off of sensitivity versus power by varying the RF sampling time. By exploiting this three-dimensional trade-off space, dynamic ranges of 11dB in sensitivity, 410X in power, and 672X in latency was demonstrated as shown in the Fig. 3.10.

6) Bit-level duty-cycling results in an unwanted spectrum shaping effect as explained in the section 3.2, which caused the dc-offsets and CW interference to propagate through the receiver chain even with ac-coupling. Moreover, the omission of a MEMS resonator causes large dc-offsets at the rectifier output due to the noise self-mixing effect. Envelope modulated signaling schemes such as the two-tone RF OOK can alleviate both these issues by creating information at a higher frequency after the rectification,

such that bandpass selection can be enabled in the baseband. By exploiting this concept, this work demonstrated a bit-level duty-cycled T-RF receiver achieving a -99dBm sensitivity for 260nW at 2.6s latency, which is 18dB better than the prior MEMS-less work as shown in the Fig. 4.10.

7) The channel embedded OOK (CE-OOK) signaling scheme utilizing a Manchester-coded single-tone OOK signal is proposed as an envelope modulated signaling scheme. This enabled binary-FSK type baseband signals after the envelope detector as shown in the Fig. 4.2. It is also proven that the CE-OOK can achieve a 2dB higher conversion gain compared to a two-tone OOK signal of same peak amplitude. This is beneficial for the case where the maximum transmitted power is limited by the peak amplitude either due to local regulations or power amplifier constraints. Given the versatility of the CE-OOK for creating multiple IFs after an ED, the multichannel operation of a nano-watt scale energy detection type wake-up receiver was demonstrated for the first time as shown in the Fig. 4.9.

Related to 2.4-GHz U-IF research phase:

8) For the case of the same dc-power and latency, the sensitivity degradation due to packet-level duty-cycling is shown to be less than 3dB for the case of U-IF architecture, and less than 5dB for the heterodyne architecture as shown in the section 5.2.2. This allows for adoption of the packet-level duty cycling method for latency constrained applications while marginally sacrificing the sensitivity.

9) Bit-level duty-cycling was shown to perform worse than packet level duty-cycling when the non-ideal start-up delays are considered as visualized by the Fig. 5.5.

10) Packet-level duty cycling allows for carrier-sensing operations as shown in Fig. 5.6. This allows for the ‘within-packet’ duty-cycling, where depending on the energy level corresponding to the first several bits in a duty-period, the receiver can opt to turn off early instead of staying on for a full packet duration. Given the wakeups are expected to be infrequent for low-activity factor networks, the within-packet duty-cycling concept can be adopted for drastic power reductions as shown by the side-by-side measured power consumption of the standard packet-level method versus the within-packet duty-cycling method as shown in tables 5.1 and 5.2.

11) The duty-cycling of a conventional heterodyne receiver suffer from a high-startup delay due to the phase locked-loop's (PLL) settling time. This can be alleviated by opting for a uncertain-IF topology, but the large uncertainty of IF leads to a worsened sensitivity performance. This work mitigated the said issue by adopting an event-driven calibrating oscillator with the aid of an integrated PLL as shown in the Fig. 5.11.

12) The uncertainty of IF can be alleviated by adopting an envelope modulated signaling scheme such as the CE-OOK to enable deterministic sub-carrier channel selection as mathematically proven in the section 5.3.4.

13) The combination of a calibrated U-IF and within-packet duty-cycling can enable a wake-up receiver dc-power level as low as 2µW for a sensitivity of -91.5dBm at 100ms latency as shown in the table 5.3. The power can be reduced to 900nW while sacrificing the latency up to 1s.

Related to the constrain driven wake-up receiver design method:

14) A side-by-side analysis of the bit-level duty-cycling and the packet-level duty-cycling for the same dc-power and on-time, same dc-power and latency, same sensitivity and power, and same sensitivity and latency is presented in the table 6.3. The content in this table can be used as a tool for determining which duty-cycling method would be the ideal choice for a given application.

15) A trade-off space analysis with the aid of reported work is shown for the dc-power versus sensitivity at sub and multi-GHz ranges in the Fig. 6.7. The insights are captured in the Fig. 6.8 along with the signal to interference ratio trends. These trade-off space plots can be used as a tool for selecting the wake-up receiver topology for a given set of constraints.

16) A step-by-step design example to illustrate the optimum wake-up receiver topology selection for a given set of user needs is shown in the section 6.6.

7.2 Future directions and open problems

Concerning the T-RF phases

The T-RF phase of this work achieved high sensitivity, but this came at the cost of bulky off-chip MEMS resonators. The omission of a MEMS resonator led to the sensitivity degradation of 9dB while the dc-power was increased to compensate for the sensitivity loss. One of the much-needed open ended future directions for high sensitivity T-RF is to realize on-chip high quality factor RF filtering. The advantage of this is twofold; 1) The cost of the node may drastically reduce by enabling monolithic solutions due to the high integration factor, and 2) High spectrum efficiency by allowing channel or band selection at RF as opposed to the fixed frequency MEMS.

The T-RF architecture also suffers from poor tolerance to interference as evident by the prior work as well as the 3rd phase T-RF work of this dissertation. However, as the sensitivity increases, the interference tolerance should similarly increase to maintain robust operation. This is especially crucial for densely deployed sensor networks where each individual node may now act as an interference source to others. Therefore, the future research should strive to achieve high interference tolerance while maintaining the high sensitivity and low power afforded by the T-RF architecture.

Concerning the U-IF phase

The maximum achievable sensitivity of a U-IF receiver is directly proportional to the frequency stability of the employed RF reference oscillator. This work adopted simple cross-coupled LC oscillator topology for a better stability, but LC oscillators dissipate higher power than ring-oscillators. Moreover, majority of the active power of the implemented receiver is limited by the power consumption of the said LC VCO. Therefore, one straightforward method to reduce the dc-power even further would be to implement a highly stable ring oscillator at 2.4GHz frequency.

The frequency calibrating mechanism used in this work adopted a type-II charge pump PLL and storing the control voltage on a digital-to-analog converter (DAC). This can suffer from the unwanted ripple on the DAC output due to refreshing clock and inherent DAC + voltage buffer offsets. This can be further improved by adopting an ultra-low power ADPLL [81] or a subharmonic injection locked ring oscillator [82].

The proposed work in both phases adopt OOK or variants of OOK as the RF signal. Until recently, OOK was not a supported modulation format in either BLE or Wi-Fi. The Wi-Fi standard has adopted multi-carrier based emulated on-off-keying to enable wake-up receiver functionality [52]. Therefore, enabling multi-tone or direct-OOK schemes at a network scale can enable low power wake-up receivers as proposed in this work.

Appendix A: Trade-offs space of BLDC and PLDC

This section provides additional information about identified bounds and trade-offs for the packet level and bit-level duty cycling schemes. Table 6.3 is shown again for the convenience.

Table 6.5. Analysis of BLDC vs. PLDC

	BLDC	PLDC	Comments
Same DC Power and On time:		$\frac{T_{on,B}}{T_{per,B}} = \frac{T_{on,P}}{T_{per,P}}$, $T_{on,B} = T_{on,P}$	
Power	$P_{inst}\frac{T_{on,B}}{T_{per,B}}$	$P_{inst}\frac{T_{on,P}}{T_{per,P}} = P_{inst}\frac{T_{on,B}}{T_{per,B}}$	=
Latency	$N.T_{per,B}$	$T_{per,P} = \frac{T_{per,B}\cdot T_{on,P}}{T_{on,B}}$	PLDC: Better Latency
Baseband BW	$\frac{0.35}{T_{on,B}}$	$\frac{N}{T_{on,P}} = \frac{N\cdot T_{per,B}}{T_{on,B}\cdot T_{per,P}}$	PLDC: 3N Higher BW
Same DC Power and Latency:		$T_{per,P} = N \cdot T_{per,B}$	
Power	$P_{inst}\frac{T_{on,B}}{T_{per,B}}$	$P_{inst}\frac{T_{on,P}}{T_{per,P}} \Rightarrow P_{inst}\frac{T_{on,P}}{N\cdot T_{per,B}}$	PLDC: N times longer on-time
Latency	$N \cdot T_{per,B}$	$T_{per,P} = N \cdot T_{per,B}$	=
Baseband BW	$\frac{0.35}{T_{on,B}}$	$\frac{N}{T_{on,P}} \Rightarrow \frac{1}{T_{on,B}}$	PLDC: 3X higher BW
Same Sensitivity:		$T_{on,P} = \frac{N\cdot T_{on,B}}{0.35}$	
Power	$P_{inst}\frac{T_{on,B}}{T_{per,B}}$	$P_{inst}\frac{T_{on,P}}{T_{per,P}} \Rightarrow \frac{1}{0.35}\cdot P_{inst}\frac{T_{on,B}}{T_{per,B}}$	PLDC: 3X worse power for same Latency
Latency	$N \cdot T_{per,B}$	$T_{per,P} \Rightarrow T_{per,B}\cdot\frac{N}{0.35}$	PLDC: 3x worse latency for same power
Baseband BW	$\frac{0.35}{T_{on,B}}$	$\frac{N}{T_{on,P}}$	=

Case 1: For the same DC power and on time between BLDC and PLDC:

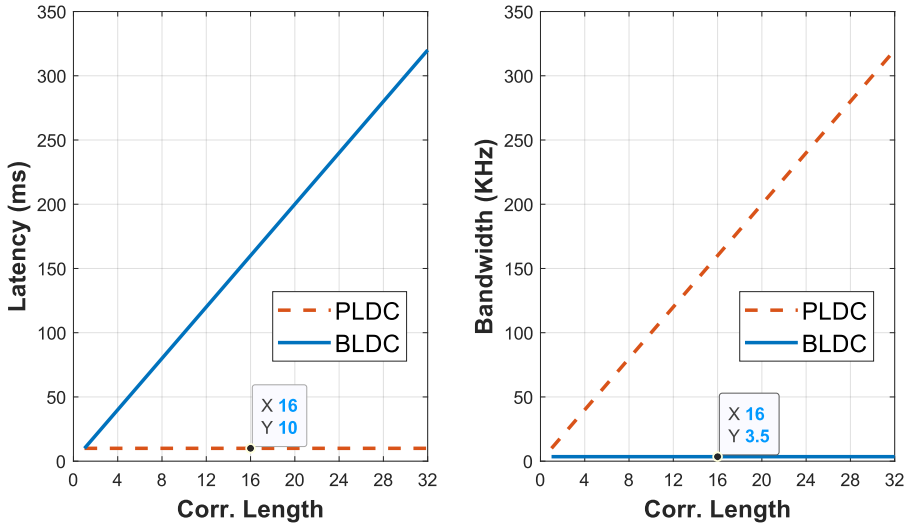


Fig. A.11. Latency and baseband BW as a function of correlator length for the case of same dc power and on-time between PLDC and BLDC. Assume the following. P_{inst} = 100µW, $T_{on,B}$ = $T_{on,P}$ = 100µs, $T_{per,B}$ = $T_{per,P}$ = 10ms. This results in an ideal duty-cycled power of 1µW.

Case 2: For the same DC power and latency between BLDC and PLDC:

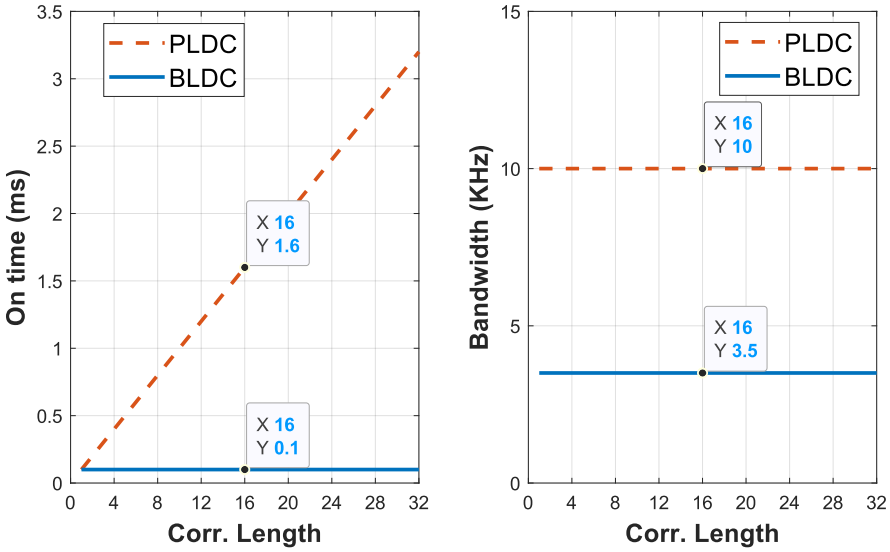


Fig. A.12. On-time and baseband BW as a function of correlator length for the case of same dc power and latency between PLDC and BLDC. $T_{on,B}$ = 100μs.

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