Integrated Millimeter-Wave Signal Amplification and Frequency Multiplication for Phase Conjugation

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A Dissertation
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APPROVAL SHEET

This

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Abstract

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The terahertz range is generally accepted as the spectrum between 300 GHz and 3 THz to distinguish it from its millimeter-wave counterpart (30–300 GHz). The first documented demonstration of a terahertz system was in 1923. Since then, there has been a significant amount of research in understanding the fundamental nature of the spectrum that exists between heat and electric waves. Almost a century later, this space has not been fully conquered, and the terahertz gap still exists. On the other hand, the significant challenges in devising hardware to enable the generation, detection, manipulation and modulation of terahertz waves make this an area rich with opportunities to explore. Numerous approaches including vacuum tube amplifiers, Schottky diodes, CMOS and BiCMOS transistors, HBT and HEMT have been pursued and it is generally accepted that all these methods complement each other in their capabilities. Terahertz radiation has applications in imaging, communications and spectroscopy among many others.

This research fundamentally focuses on techniques for terahertz wave front manipulation, and more specifically for phase conjugation, while building on wideband amplifier design and characterization techniques. Phase conjugation has been primarily used in the optical regimes for aberration correction, and in the microwave regime in automatic point and track systems and communications including radar.

The phase conjugated beam bears a unique relation with regards to the signal beam - the wavefront is reversed and any distortions in the signal beam as it passes through an non-homogeneous medium can be removed as the reverse beam passes through the same medium. There are interesting applications for this behavior in imaging at the diffraction limited regime enabled by time-reversal among others, and there has been some success in realizing these results. Nevertheless, challenges with demonstrating phase conjugation itself exist, and transistor and material-based approaches coexist in this space.

In the transistor realm, Indium Phosphide (InP) Heterojunction Bipolar Transistors have demonstrated capabilities with f_{max} in excess of 1 THz (130 nm). InP HBTs are therefore well positioned to be designed into terahertz applications. Commercial foundries are also able to integrate these devices with other circuit components and multiple levels of metallization, enabling an extensive design space of devices and antenna elements. This research has two thrusts. The first part of the research details the design and measurement of wideband and high output power amplifiers for emerging 6G applications. Techniques for modulation measurements and power combining are detailed and the work is demonstrated by proof-of-concept realization using the 130nm InP HBT node from Teledyne Scientific.

The next part of the research focuses on the design and characterization of a phase conjugating system operating at 300 GHz in the 250 nm InP HBT node from Teledyne Scientific. Additionally, tests structures are also designed and implemented in the same technology to correlate the behavior of the system with the individual circuit blocks. The research demonstrates the capabilities of InP HBT transistor technology in devising novel methods for wavefront and signal modulation at terahertz, and opens up new frontiers to expand on this in conjunction with other device technologies like Schottky diodes. As part of the design of the individual circuit blocks, the research also details techniques that can be used to improve performance in mmwave circuits at frequencies approaching the limits of operation

of the device.

One critical aspect to enabling massive terahertz electronic systems at scale is the holistic integration of electromagnetic and circuit simulator based co-design of circuits, with packaging techniques. These are specifically of immense importance in circuits that have a soft dielectric underneath the pad metallization, like the demonstrations in this thesis are. A custom interposer capable of being used to supply DC bias to the pads on the integrated circuit, and of being wire bonded to a printed circuit board, was used to characterize the behavior of the test structures in the latter part of the thesis. This opens up a potentially interesting space for developing mmwave systems that can be deployed at scale while being resilient to foundry and pad specific adhesion and other packaging issues. The interposer was comprehensively designed and fabricated in-house in the UVA cleanroom while making use of modern fabrication and etch techniques.

This research also expands on earlier work that used phased LO signals to relax the frequency requirements on the Local Oscillator (LO) for phase conjugate mixing. A prototype subharmonic phase conjugate mixer that uses the 4th harmonic of the LO is implemented on a FR4 4 layer PCB, and is the first demonstration of a phase conjugate mixer using subharmonic mixing of the 4th harmonic of the LO with the RF, while incorporating a quadrature hybrid to intrinsically separate the input RF and output IF. Although the use of subharmonic mixers to achieve phase conjugation is not novel, this particular design that is able to separate the RF and IF to different ports unlike prior art that used the same antenna to radiate both is new in itself. Prior art also relied on an arbitrarily low frequency separation to demonstrate the potential for retrodirection. While optical techniques have been used to demonstrate phase conjugation using three and four way mixing, a unified theory to establish this behavior using conventional RF measurement techniques is absent in the literature. This thesis establishes one such technique using the aforementioned mixer. This method has the potential to be used in specific applications like net-

work synthesis for example, and provides a quantitative method to infer the quality of the phase conjugate signal versus the other signals in the system.

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Finally, thank you to the Bhagavad Gita - for providing me succor in the darkest times and for keeping me grounded in the good times. The learnings of the Gita are timeless and a source of eternal spiritual light for all humanity.

This work is dedicated to my parents and wife.

Vinay Iyer

"Seek refuge in the attitude of detachment and you will amass the wealth of spiritual awareness. The one who is motivated only by the desire for the fruits of their action, and anxious about the results, is miserable indeed."

- **The Bhagavad Gita**

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Chapter 1

Introduction

1.1 Research Overview

Advances in transistor technology have driven tremendous improvements in connectivity and in enabling new applications. The number of connected devices is rapidly increasing and access to new spectrum at the lower frequency ranges is scarce. 5G systems are already in commercial deployment, and there is increasing emphasis on bringing beyond-5G and 6G applications to fruition in sensing, imaging and communication systems. The upper millimeter wave and sub-terahertz frequency range (100 - 300 GHz) is expected to be a major source of spectrum as systems move closer to achieving 1Tb/s of wireless throughput. These beyond 5G/6G applications [7, 8] are expected to be deployed as very large scale arrays to make up for the high-frequency path loss [9, 10].

Power amplifiers are crucial building blocks in such systems. At lower mmwave and RF frequencies, silicon based technologies enable extensive levels of integration and design space optimizations leading to wideband, energy-efficient power amplifiers. At mmwave frequencies and above, the lower fundamental transistor gain in silicon means that peak efficiency is low especially at D band and above. The average efficiency when amplifying high dynamic range signals is even lower. InP

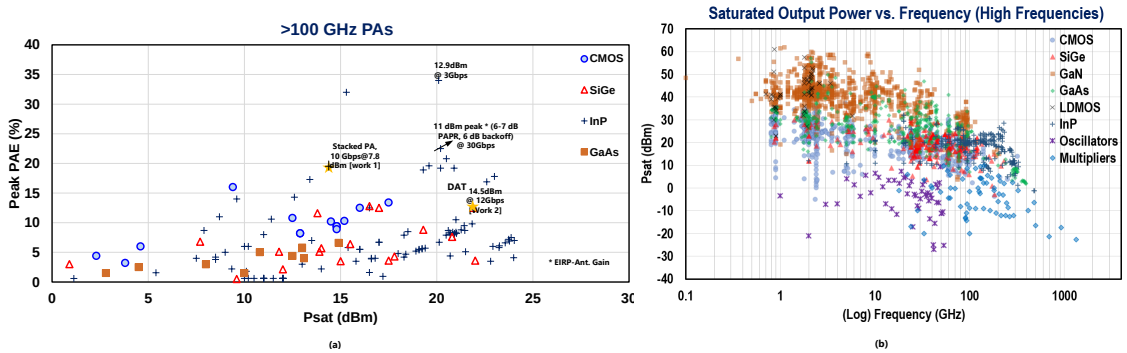

Figure 1.1: Georgia Tech PA survey on silicon and III-V PAs at 100–190 GHz. (a) PAE vs. Psat. (b) Psat vs. frequency. The work in this thesis is clearly labeled [1]

PA offer higher fundamental gain and efficiency [11] [12, 13] at the higher end of the mmwave spectrum. These trends are plotted in Fig. 1.1 across frequency and saturated output power levels [1].

Table 1.1: Detailed comparisons of 2G to 6G communications [7]

features	2G	3G	4G	5G	6G
Period	1990–2000	2000–2010	2010–2020	2020–2030	2030–2040
Max. rate	144 kb s^{-1}	2 Mb s^{-1}	1 Gb s^{-1}	35.46 Gb s^{-1}	100 Gb s^{-1}
Max. freq.	1.9 GHz	2.1 GHz	6 GHz	90 GHz	10 THz

The first part of this research focuses on D band PAs that demonstrate high 3dB bandwidth and high output power. A stacked PA is designed in the 130 nm InP HBT technology node from Teledyne Scientific. This PA is demonstrated to have high peak efficiency and wideband characteristics. Previous work on modulated power amplifier measurements at W band have included custom modulators on chip and multi-chip solutions [14, 15]. We propose a signal lineup using commercial equipment that enables us to measure the performance of the standalone PA across power levels upto P1dB. The measurement is done once by equalizing the setup without the PA and then measuring the PA. Next, this wideband stacked PA is used as the unit cell in a millimeter wave DAT power amplifier and exhibits an excellent design space tradeoff between bandwidth, gain flatness and power levels. These two works have been listed in Fig.1.1 (a) and contribute vital data points - to

the best of our knowledge, these are the highest data rates achieved on InP power amplifiers at these frequencies at close to Psat levels. While other work displayed does show a greater data rate (30 Gbps), this was done at 6 dB back off. With this custom modulation chain, there is greater exercising of the modulating stimuli at ever increasing power levels and this can provide important information to PA designers as 6G proliferates, especially at the intersection of transistor and amplifier performance.

The earliest documented endeavor a century ago to demonstrate achieving terahertz radiation consisted of spark-gap oscillators and Boltzmann interferometers. Advances in technology have improved the range of frequencies, and output power levels and sensitivities since then but significant research is needed to be able to conclusively fill the Terahertz Gap. The synthesis and control of terahertz radiation, on the other hand has tremendous implications in a wide range of applications. [16–19] . At these frequencies, solid state III-V and Si-based technologies coexist with vacuum tubes, backward wave oscillators, far infrared lasers and quantum cascade lasers, among many others to enable true terahertz operation. Solid-state solutions enable extensive and fast reconfigurability and are critical building blocks for such systems.

More specifically, phase conjugation is the reversal of a wavefront as it travels through a non-homogeneous medium while being distorted. The phase conjugated beam is thus retro-directed and has none of the distortions that the original signal beam underwent. At optical frequencies, phase conjugation finds applications in aberration correction, four wave degenerate mixing and stimulated Brioullin scattering among others [20, 21]. Phase conjugation also has applications in sub-wavelength diffraction limited imaging [22, 23], and there has been some success in demonstrating this use-case at terahertz frequencies using plasmonic nanoantennas loaded with non-linear elements [24]. At microwave frequencies, Fusco et. al demonstrated an active phase conjugating lens With sub-wavelength resolution

capability at 2.4 GHz [25, 26]. Retrodirective arrays can also provide additional security in highly directional, high gain array systems [27, 28] and this has implications for future communication links that can exploit multipath effects to enhance the capacity of communications networks and achieve super-resolution using time reversal techniques [29, 30]. To the author's best knowledge, there have been no demonstrations of phase conjugate mixing at terahertz frequencies using transistor technologies.

The InP HBTs used in this latter part of the research have f_{max} in excess of 600 GHz [2, 13]. This coupled with the high breakdown voltage can enable myriad building blocks necessary for a system.The multilayer BEOL (back end of the line) wiring and backside metal processing also present interesting opportunities to synthesize novel EM structures. Fig. 1.2 details the layers in the process used in the first part of the thesis. The results from the first part of the research, combined with the integration and fabrication capabilities afforded by the foundry enable interesting co-design between circuit elements and antenna structures. The second part of this research focuses on the design, implementation and measurement of one such architecture for phase conjugation at terahertz frequencies. Quasi-optical methods are proposed to test the retro-directive action the setup. The design and characterization of a quadrupler in the 250nm InP HBT Teledyne process is also detailed. Next, a PCB implementation of a subharmonic mixer based phase conjugator using COTS diodes is also detailed.

1.2 Background of the research

Advances in technology scaling in silicon have enabled exceptional systems that integrate a wide range of functionality. Silicon based PAs however suffer from low gain and PAE (power added efficiency) at W band and higher. Given the lack of gain, it has been difficult to implement many of the techniques (digital power amplifiers,

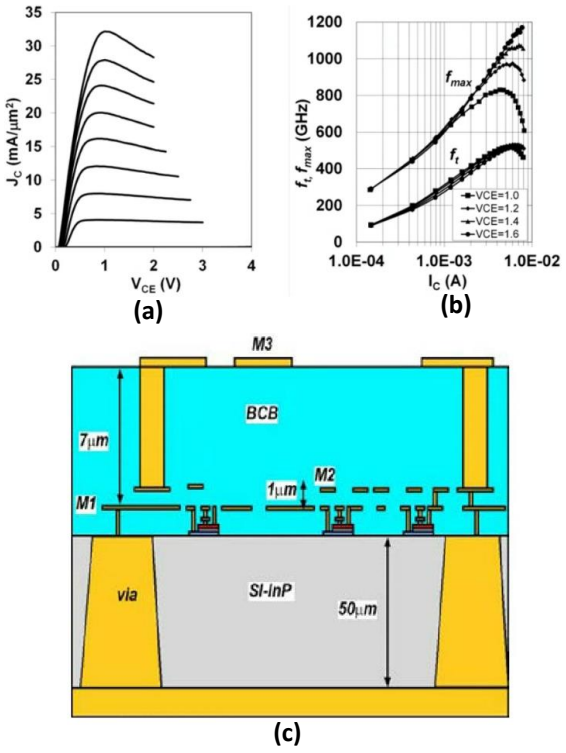

Figure 1.2: (a)CE IV characteristics of a 0.13um HBT normalized to emitter area (b)Extrapolated ft, fmax vs Ic for 0.13x2um^2 for varying Vce (c) Thin film wiring environment [2]

switched passive networks etc.) [31, 32] that are possible at RF and lower mmwave frequencies [11].

InP provides excellent energy efficiency at these frequencies and higher. Prior art proposes using the CB to improve gain however, the need for a bias-tee and negative power supplies makes system integration more difficult [33, 34]. Prior and current art also looks at using classical power combining techniques using Wilkinson dividers and combiners [35]. Transistor scaling enables large-scale integration, but is also accompanied by an attendant lowering of breakdown voltages. The stacked PA is an excellent candidate for wideband power combining especially in scaled technologies. Cascode (and stacked topologies) have therefore been widely used in the design of single stages, and in distributed amplifiers [34, 36, 37].

As beyond 5G/6G systems proliferate, there is increasing emphasis on demonstrating the performance of such systems to real-world modulated signals. There is a plethora of research on mmwave and THz transmitters, receivers and transceivers that can achieve this [38, 39]. Power amplifiers (PA) are crucial building blocks in such systems and the response of the PA to modulated signals is a critical measure of the performance. Techniques to characterize this performance conventionally involve a high-bandwidth arbitrary waveform generator. We propose a different signal chain that obviates this need. This signal chain has the capability to be arbitrarily extended to higher frequencies, well into the true terahertz (> 300 GHz) while being extremely linear and supporting a wide variety of formats. A wideband stacked power amplifier is designed and implemented in the 130 nm InP HBT process from Teledyne Scientific [2, 40]. The proposed signal lineup is then used to characterize the performance of the amplifier.

There is also an ever persistent thrust to design higher output power amplifiers. Higher power can work to extend the detection range for imaging and radar applications. Previous work has focused on n-way power combining on chip, primarily 2-way and 4-way [41]. There are broad avenues for research into newer areas that

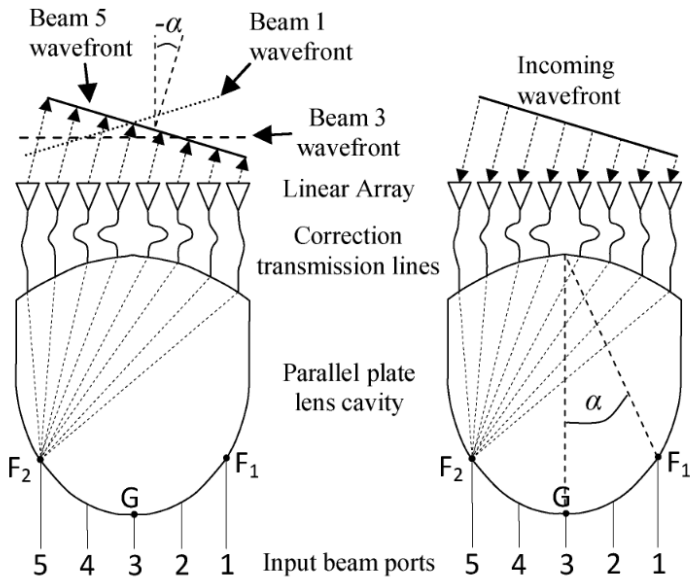

Figure 1.3: Schematic of the Rotman Lens [3]

can improve the efficiency and bandwidth of the combining network. A range of innovative power combining techniques have been developed at lower frequencies, spurred by advances in passive component fabrication that accompany the scaling of devices - including the Distributed Active Transformer (DAT) and broadband transformer based methods among many others [42, 43]. At upper mmwave frequencies, Wilkinson power combiners have been used as in [44, 45]. Transmission lone based combiners have also been used to implement 8:1 way combining as in [46]. These methods however suffer from narrow bandwidths. This work extends the DAT network to millimeter wave frequencies, using the stacked PA as the unit cell for the combining. The PA is a two-stage 8 way power combined design, and the compact geometry minimizes the imbalance from the inter-winding capacitance. The output is capacitively tuned for performance. The design achieves high output power, efficiency and bandwidth.

The research then builds on the results in the first part to develop an architecture for terahertz phase conjugation using the 250 nm InP HBT technology node from Teledyne Scientific Co. Retrodirective arrays have been demonstrated at C band upto Ka-band [47–50]. The self-phasing function of a retrodirective antenna

gives it the ability to automatically track moving targets, and in eliminating the fading effects of multipath propagation [3, 51]. The simplest microwave retrodirective system is a corner cube reflector. However, these are non-conformal and do not integrate the complex electronics that can be used to process the impinging signal. The Van-attay array [52] is a conformal passive solution that makes use of array spacing to redirect the incoming signal with the appropriate phasing - but the incoming waves are restricted to be plane waves [49]. Phase conjugating circuits have been demonstrated up to 20 GHz using the Rotman Lens architecture [3, 53]. The terahertz spectrum provides interesting opportunities for the development of phase conjugating systems especially in sub-wavelength diffraction limited imaging, and in future terahertz communication links with additional security [27, 28].

This research proposes an architecture for active phase conjugation using a low-frequency LO [6], on-chip quadrupler, and a fundamental micromixer. The system also integrates an on-chip frequency selective surface that enables spatial separation of the LO and interrogating RF beams into opposing hemispheres. The architecture has 4 "pixels" and each pixel is capable of simultaneously receiving and transmitting separated by polarization. Each pixel is hence a multifunctional T/R (transmit/receive) element. The architecture lends itself to natural extension to an array and is limited only by device performance and frequencies. The important issues that concern the architecture are space to implement electronics and mutual coupling between adjacent elements. The research also details the design of a quadrupler capable of being used for phase conjugation. The output of the quadrupler is close to the fmax of the devices used, and this opens up an interesting design space. This design space is explored using coupled lines, to improve the amplitude balance of an active balun used as one of the blocks, and to optimize the performance of the quadrupler mentioned above.

The research also details the design space for extracting maximal performance from circuits at frequencies close to the fmax of the transistors using coupled lines

[54]. These design techniques are used in the design of a mixer and quadrupler in the 250nm InP HBT process. Further, a custom interposer is designed in house in the UVA cleanroom and is used to supply DC bias to the circuits mentioned.

Next, an RF demonstration of phase conjugation using appropriately phased LO and RF signals on a PCB is detailed - including design considerations for subharmonic mixer based phase conjugators that utilize the 4th-harmonic of the LO for mixing. A novel metrology technique is used to quantify the phase conjugate signal itself as opposed to prior art that used frequency separation. There are previous demonstrations of art that use a LO at twice the RF frequency like [48–50, 55]. However as operating frequencies increase, the requirement of a high power source at twice the RF frequency can be difficult to meet. Subharmonic mixers operate at a fraction of the LO, based on the design and hence are easier to characterize. However, they typically also suffer from higher conversion loss (in the case of diode mixers specifically). In systems where this is not a critical drawback, this relaxed requirement can be used to the benefit of the overall system. Liu's work [56] detailed the use of an arbitrary number of phases of the LO to obtain the required order of mixing. [57] detailed work that used a LO at the same frequency as the RF. Frequency separation can be an issue in such designs if not accounted for appropriately. [58] detailed an array that operated at a fourth of the RF frequency. However, no design considerations were listed for obtaining an optimal conversion gain. [59] details an array with the LO at one half the frequency of the RF like our design, but these are integrated with antennas and no design decisions to minimize the conversion loss are enumerated. In essence, none of the previous work provide for a systematic design that idles the various "unwanted" frequencies at the various nodes, while providing an intrinsic separation between the RF and IF like we demonstrate.

1.3 Thesis Statement

This thesis aims to demonstrate that the building blocks necessary to implement phase conjugation at the upper millimeter wave frequencies can be implemented in InP HBT technology. Techniques for wide-band power amplifier design and modulation characterization at D-band are also introduced. The design techniques used in this research include the use of multi-functional EM blocks, circuit design methods that enable optimal performance at THz frequencies, the use of a frequency selective surface on chip, the development of a phase conjugating system architecture that is easily extensible to an array, the development of packaging tools that make interfacing to devices built on soft substrates more reliable, and the design of a PCB based phase conjugator using COTS (commercial off the shelf) diodes.

1.4 Research Questions

Research Question 1. How can a multi-frequency electromagnetic structure be co-designed with recently developed HBT-based circuit electronics to implement phase conjugation at sub-mmwave frequencies?

Research Question 2. How can dual-polarized antenna structures be employed to perform wavefront diplexing in simultaneous phase conjugating transmit/receive systems?

Research Question 3. Can coupled line structures be used to improve signal balance in active baluns at frequencies close to the transistor f_{max}?

Research Question 4. How can the distributed active transformer method be extended to millimeter-wave frequencies for efficient power combining?

Research Question 5. How can MMICs that suffer from low pad adhesion to the substrates be reliably biased and characterized?

Research Question 6. How can the amount of phase conjugate signal present

in the system be quantitatively characterized using conventional RF measurement techniques

1.5 Research Contributions

This dissertation provides design analysis, characterization techniques and insight into newer methods of packaging that will enable the realm of terahertz systems and their deployment at scale. Specifically, the highlights of the thesis are listed below -

1. New techniques for characterization of the modulation performance of PAs above 100 GHz, and design and characterization aspects that influence the modulation performance.

2. Power combined PA amplifier topologies for emerging applications above 100 GHz, specifically an extension of the Distributed Active Transformer technique for PAs above 100 GHz.

3. Design of architectures using integrated circuit fundamental mixers and harmonic generators for retro-reflective/phase-conjugation applications.

4. Demonstration of phase conjugation using subharmonic diode mixers on a RF printed circuit board using a quadrature hybrid.

5. An innovative metrology technique for the quantitative characterization of the phase conjugate signal using conventional RF measurement methods.

6. Co-design and fabrication of custom interposers/probe-cards that eliminate the need for wirebonding on pads that are supported by soft substrates that cannot be wirebonded to reliably.

1.6 Dissertation Organization

The remainder of this thesis is organized as follows:

- ***Chapter 2***

  This chapter presents the design of a stacked PA in the 130nm InP Teledyne process node. Small signal S parameter and large signal measurements are also detailed. The design decisions made, including the visualization and use of the intrinsic current generator as a useful design tool is presented. Modulation measurements are performed using commercial equipment, and the PA is measured with the modulation peak reaching saturated power numbers. A qualitative analysis of the factors impacting the modulation performance is detailed as are areas for future lines of inquiry.

- ***Chapter 3***

  This chapter presents the design of a distributed active transformer based PA reusing the stacked PA unit cell from the previous chapter. A theoretical framework to design a DAT PA at higher frequencies using asymmetric coupled lines is explored and a schematic model compares favorably with EM simulated results. The PA performs exceedingly well on various fronts, including small signal bandwidth and modulation results. Certain directions for future research are also detailed.

- ***Chapter 4***

  This chapter details the design and characterization of a phase conjugation capable system in the Teledyne InP 250nm node at 300 GHz. The chapter details the architecture of the antennas, the driving mechanisms, the schematic and design decisions underlying the various blocks, the characterization results and areas of learning. The array integrates 6 antennas and a multitude of circuit structures.

- ***Chapter 5***

  This chapter details the design and characterization of an on wafer quadrupler, and the design of a mixer at terahertz frequencies. This quadrupler is a component in the previous system and is vital in correlating the behavior of the system to the behavior of the individual circuit blocks. The chapter also details the design and fabrication of an on-chip interposer with beamleads used to supply DC bias.

- ***Chapter 6***

  This chapter details the design of a subharmonic phase conjugator using COTS diodes on a 2 layer FR4 PCB at RF frequencies, and the analysis and characterization efforts. A metrology technique and analysis is introduced and can serve as a vital tool for comprehensive chracterization of the behavior of the circuit as a phase conjugator instead of using separation in frequencies as a distinction tool.

- ***Chapter 7***

  This chapter includes some conclusions that connect these threads together, and some recommendations for areas of future research.

1.7 Exhaustive List of publications (published and submitted)

- **V. Iyer**, J. Sheth, L. Zhang, R. M. Weikle and S. M. Bowers, "A 15.3-dBm, 18.3% PAE F-Band Power Amplifier in 130-nm InP HBT With Modulation Measurements," in IEEE Microwave and Wireless Technology Letters, vol. 33, no. 5, pp. 547-550, May 2023.

- L. Zhang, **V. Iyer**, J. Sheth, L. Xie, R. M. Weikle and S. M. Bowers, "A 117.5-130 GHz 22.1 dBm 11.5% PAE DAT Based Power Amplifier in InP 130 nm HBT

Technology," 2021 16th European Microwave Integrated Circuits Conference (EuMIC), London, United Kingdom, 2022, pp. 229-232, doi: 10.23919/EuMIC50153.2022.9783740.

- **V. Iyer**, J. Sheth, L. Zhang, R. M. Weikle and S. Bowers, "A 90-125 GHz Stacked PA in 130 nm InP HBT with 18.3 % peak PAE at 15.3 dBm Output Power," 2022 United States National Committee of URSI National Radio Science Meeting (USNC-URSI NRSM), Boulder, CO, USA, 2022, pp. 224-225.

- L. Zhang, **V. Iyer**, J. Sheth, L. Xie, R. M. Weikle and S. M. Bowers, "F Band Distributed Active Transformer Power Amplifier Achieving 12 Gbps in InP 130 nm HBT" submitted to the IEEE Transactions on Microwave Theory and Techniques, May 2023.

- J. Sheth, L. Zhang, X. Shen, **V. Iyer**, S.M. Bowers, "A Current-Mode Multi-Phase Digital Transmitter With a Single Footprint Transformer-Based Asymmetric Doherty Output Network" submitted to IEEE Open Journal of the Solid-State Circuits Society, May 2023.

Chapter 2

Efficient wideband medium power amplifiers for beyond 100 GHz operation - Design and characterization techniques

2.1 Introduction

Power amplifiers (PA) are crucial building blocks in a variety of applications and influence system efficiency and performance metrics. F and D-band power amplifiers (90 to 140 GHz and 110 to 170 GHz respectively) specifically have use in short range applications such as inter-chip communications, and in millimeter wave front-haul and back-haul for communication systems [60]. The stacked PA topology is an attractive candidate to simultaneously optimize gain, output power and power added efficiency (PAE) in scaled technologies [37, 61]. Advances in silicon and III-V technologies have also enabled the realisation of complete transmitter chains capable of high data rates at moderate to high effective isotropic radiated power (EIRP). There have been previous demonstrations of complete transmitters at D-band, but these

systems used custom integrated circuits to perform modulation [62–66]. There is value in being able to characterize the performance of individual circuit blocks using commercial equipment as millimeterwave systems proliferate.

This work presents a custom-built modulation chain using commercial equipment as shown in Fig. 2.1, that is used to characterize the behavior of stand-alone circuit blocks like PA at 121 GHz, across a range of power levels. Next, the design and characterization of an example wideband stacked PA in a 130nm InP process is detailed. The stacked power amplifier [67] has a peak $|S21|$ of 11.7 dB, peak PAE of 18.3%, a 3-dB bandwidth from 90-135 GHz and gain greater than 8.8 dB from 90-140 GHz. The PA has at least 10 dB of gain from 95-130 GHz. The PA stages and interstage network are designed so as to have a loadline match close to 50 Ω. The amplifier is capable of data rates of 500 MSPS 16 QAM with an RMS EVM (Error Vector Magnitude) of 5.8% and average PAE of 5.2% at an average output power level of 8.2 dBm, and 5 GSPS QPSK with an RMS EVM of 14.3% at an average output power of 7.8 dBm with a PAPR (peak to average power ratio) of 6.3 dB. Using a low frequency Arbitrary Waveform Generator (AWG), this chain is also capable of being extended to higher frequencies and higher modulation bandwidths like 64-QAM, at higher Psat than the Tx module used in[68].

2.2 Modulation chain

This demonstration was designed at a center frequency of 121 GHz. On the transmitter side, a Keysight E8257D signal generator is used to produce a LO for a WR8 VDI Signal Extender (SGX) at 37 GHz. The SGX (x3) multiplies the signal up to the WR8 band. A Keysight M8190A AWG is used to generate baseband I/Q data which is then used to drive a Marki IQ mixer (MMIQ 0520HS). The LO input to the IQ mixer is powered by an E8257D at 10 GHz. The signal multiplied up by the WR8 extender is mixed with the RF output of the Marki IQ mixer using a VDI

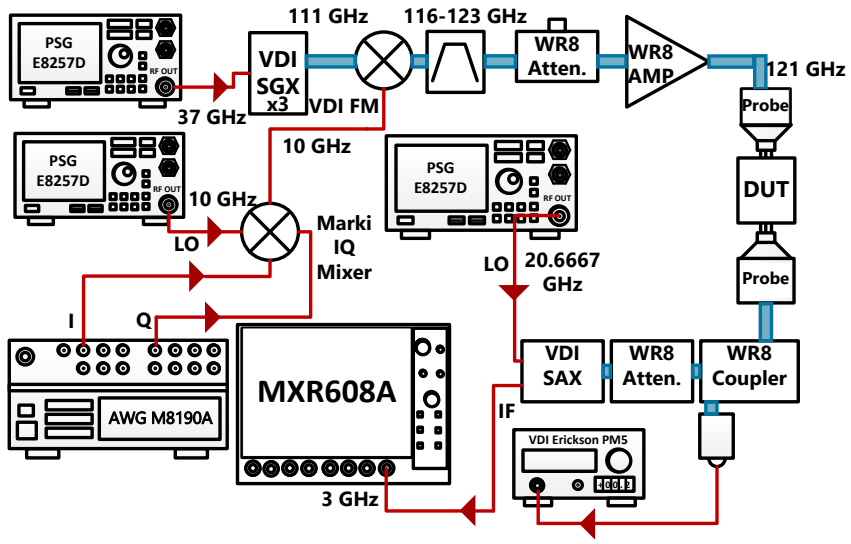

Figure 2.1: 121 GHz modulation measurement setup depicting the flow of various signals and components. Waveguide connections are colored blue.

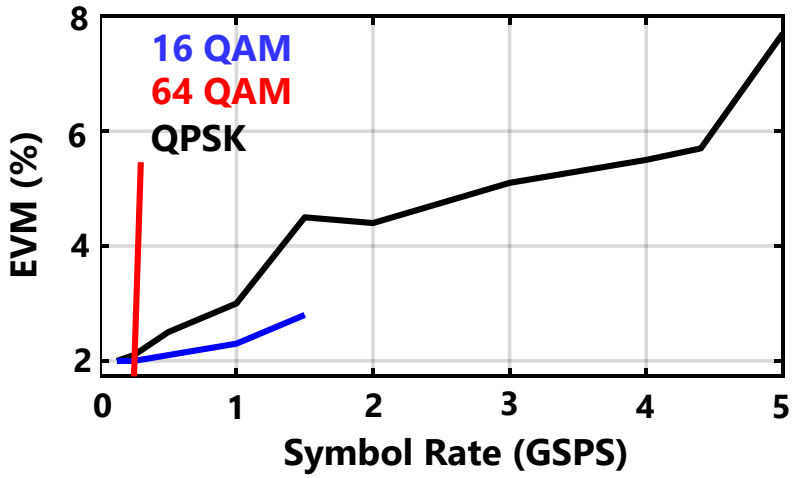

Figure 2.2: EVM performance of the chain without the DUT across modulation formats. The measured EVM at 5 GHz QPSK is 7.7%.

Fundamental Mixer. The output of the mixer is connected to a VDI bandpass mesh filter that passes the 121 GHz modulated signal. The image at 101 GHz is rejected by more than 50 dB. The modulated signal at 121 GHz passes through a waveguide attenuator, and is then amplified using a VDI WR8 amplifier to ensure the PA DUT (device under test) can be saturated to peak output power. The P1dB of the VDI amplifier is 13 dBm. The combination of the attenuator and VDI amplifier enables measurements for the DUT at various back-off power levels. On the receiver side,

the signal from the probe is sent to a waveguide 10 dB directional coupler. The coupled output is connected to a PM5 power meter. The IF output of the SAX (centered at 3 GHz) is connected to a Keysight MXR608A 6 GHz scope. The scope runs the Vector Signal Analyzer (VSA) software and is used to analyse the waveform and look at the RMS EVM numbers. The 10 MHz reference clock on all Keysight equipment is connected together, with the oscilloscope clock output acting as the master. The chain is characterized without the probes and DUT to understand the effects on the measurements of the DUT's EVM performance. As shown in Fig 2.2, this wideband chain is capable of up and down-converting a low power 1500 MSPS 16 QAM signal with an EVM of 2.8%, a 300 MSPS 64QAM signal with an EVM of 5.5% and a 5 GSPS QPSK signal with an EVM of 7.7%. An adaptive equalization generated by the Keysight VSA is applied to this chain (without the PA).

2.3 Power Amplifier design

2.3.1 Transistor Characterization and intrinsic loadline analysis

The single stage large signal power gain at frequencies greater than 100 GHz is typically low and amplifiers usually have multiple stages [11]. The stacked amplifier topology[69–72] is an excellent design choice for increasing output power and gain while ensuring all devices stay within their safe operating area (SOA) limit. This power amplifier was fabricated in the Teledyne 130 nm InP HBT process (f_t/f_{max} in excess of 500 GHz/1 THz) [73, 74]. The $BVCE_O$ is 3.5 V. The technology has 3 metal layers and Metal-Insulator-Metal (MIM) capacitors. Fig. 2.6 (b) compares the Maximum Stable Gain (the maximum stable gain that can be achieved by a potentially unstable device) for the cascode, CE, CB and stacked topologies for a unit transistor with an emitter length of 6 µm. In the stacked PA, a common emitter (CE) stage drives a common base (CB) stage, with an interstage matching network in between so the voltage across the two stages swing in phase. The capacitance at the base

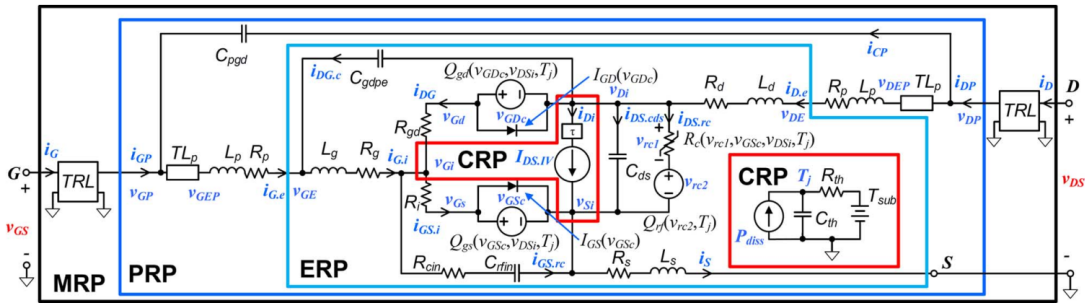

Figure 2.3: Packaged large-signal equivalent circuit. The red, light blue, dark blue, and black boxes define the current reference plane (CRP), extrinsic reference plane (ERP), package reference plane (PRP), and measurement reference plane(MRP), respectively [4].

of the CB stage is designed in conjunction with the interstage transmission line to ensure optimal phasing as shown in Fig. 2.6 (d).

Most transistor PDK (process design kit) are usually physics based and need extensive simulations to fit the parameters to a model. Power amplifier designers benefit from a first fit and from looking at the intrinsic loadline [4, 75, 76]. The intrinsic loadline can be complicated to simulate, especially in a packaged transistor with multiple parasitic components leading from the package reference plane to the internal transistor reference plane [4]. Fig. 2.3 details the various layers in a typical packaged part and the extensive parasitic accompanying the component. In a typical design, the waveforms at the intrinsic current generator plane are simulated, analysed and modified using the matching network and terminations until the overlap between the voltage and current is minimized - this guarantees minimal power dissipation in the transistor itself. It is notable that for the purposes of the designs in this and the succeeding chapter, a single or multi-tone Harmonic Balance simulation was used. The multi-tone simulation was used to check for oscillations as detailed in the section on stability 2.3.3. This means that the circuit was solved under a quasi-static assumption and this is comprehensive enough to get convergence on a design to a significant level.

Fig. 2.4 from [4] details these waveforms at the various planes and how the par-

asitic at each layer modifies the waveform, thus masking useful information about the operation of the device. This device modelling is a huge area of research in itself including the use of artificial neural networks [77]. A simpler approach is adopted in this design. A transistor biased at class A was simulated using Keysight ADS and the S parameters were fit to arrive at values for the capacitance between the various nodes as shown in 2.5 (a). A simple model consisting of purely the intrinsic part was used for this purpose as is detailed in 2.5 (b). It is notable that the change in the average value of the capacitance with input power levels is not reflected in this analysis. However, to the first order, this suffices to arrive at the waveforms at the intrinsic current generator reference plane and to look at the distortion from the intended loadline at the terminal of the device. It is upto the designer to ensure that none of the breakdown limits are exceeded - as these are nominally specified at the terminals of the device, and the optimized waveform can sometimes exceed these limits at the terminals. A voltage bias is used for the purpose of this analysis.

The equations used to arrive at the capacitance are detailed here, where f represents the frequency of operation [78]. For the sake of brevity, the metric most commonly used to characterize power amplifiers, and quite possibly for any block that consumes DC power and provides fundamental gain - the Power Added Efficiency (PAE) in % is also detailed here (where P_{out},P_{in} and P_{dc} are the output and available input power, and the DC power consumed at that level of excitation.

$$Cbc = -im(Y(1,2))/(2\pi * f) \tag{2.1}$$

$$Cbe = (im(Y(1,1))/2\pi * f) - Cbc \tag{2.2}$$

$$Cce = (im(Y(2,2))/2\pi * f) - Cbc \tag{2.3}$$

$$Cce = (im(Y(2,2))/2\pi * f) - Cbc \tag{2.4}$$

$$Cce = (im(Y(2,2))/2\pi * f) - Cbc \tag{2.5}$$

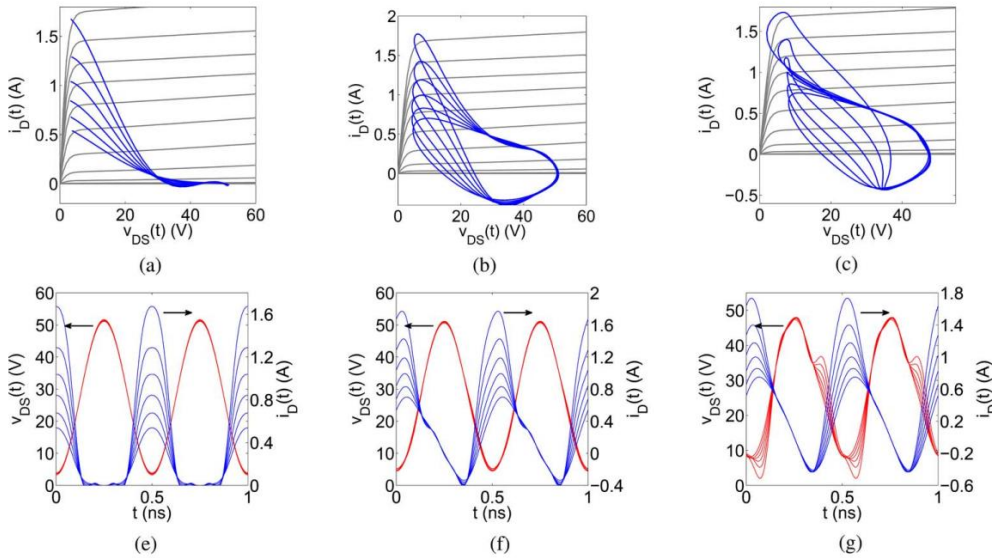

Figure 2.4: Simulated 2-GHz load lines and waveforms at the CRPs (a) and (e), respectively, are embedded to the ERPs in (b) and (f), the PRPs in (c) and (g). [4].

$$PAE = (P_{\text{out}} - P_{\text{in}})/P_{\text{dc}} \tag{2.6}$$

2.3.2 Loadpull analysis and EM simulations

The design proceeds by using the model to present the required loadline impedance at the current generator plane. This is then transformed to 50 *Omega* at the center frequency. The impedance derived from the loadline analysis does not account for the significant efficiency gain from clipping and the highly non-linear nature of the capacitances at high drive levels. This first pass design is then refined using a loadpull simulation to refine results. Next, a second stage is added to the CE transistor with an appropriate interstage matching network. There are multiple design space options to effectively and efficiently phase the signals at the various nodes - a series microstrip transmission line was used in this case. This was found to be efficient at the center frequency but this changes as the frequency of operation changes. All electromagnetic simulations are performed in the Ansys HFSS (High frequency structure simulator). Fig. 2.6 (a) compares the simulated load pull contour between

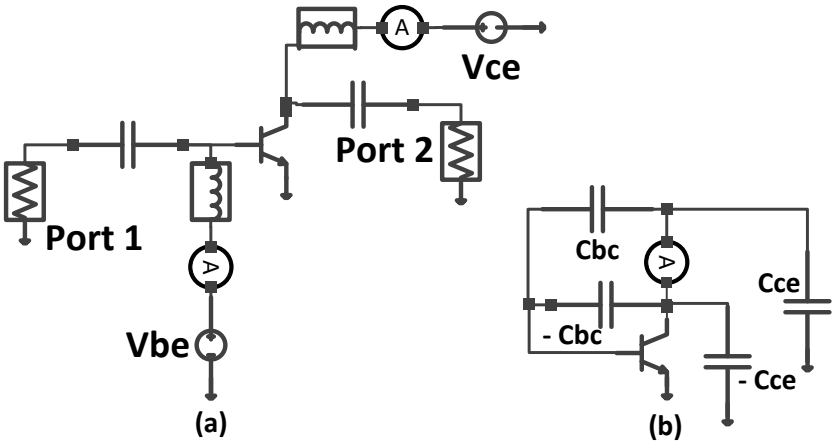

Figure 2.5: (a) Simulation set up used to arrive at the de-embedding capacitances (b) Model used to simulate the current at the intrinsic waveform generator plane.

a class A CE (i) and the stacked power amplifier (ii) at 125 GHz at various levels of compression. Fig. 2.6 (c) shows the architecture of the design. Radial stubs are used in this design for broadband bias insensitivity. The transistors in the CB stage are laid out with the bases in proximity so as to minimize stray inductance and prevent instability. The series capacitors are EM simulated in isolation before insertion into the matching networks. Each stage in the CE and stacked PA consists of four transistors, with an emitter length of 6 µm each. The optimum load impedance for the CE amplifier is 10+j15 Ω for peak efficiency. Matching this impedance to 50 Ω requires high-Q components, and is difficult to design with broad bandwidth. The optimum load impedance for the stacked PA design is 60+j40 Ω, making a broadband match easier to implement. The simulated output network passive efficiency exceeds 80% for the WR8 band. The simulated interstage and output matching network loss are 0.9 dB and 0.7 dB at 125 GHz. A 65 fF capacitor was used at the base of the cascode stage and a 150 Ω resistor (Rb) was used to both thermally ballast and electrically stabilize the PA, as shown in Fig. 2.6(c).

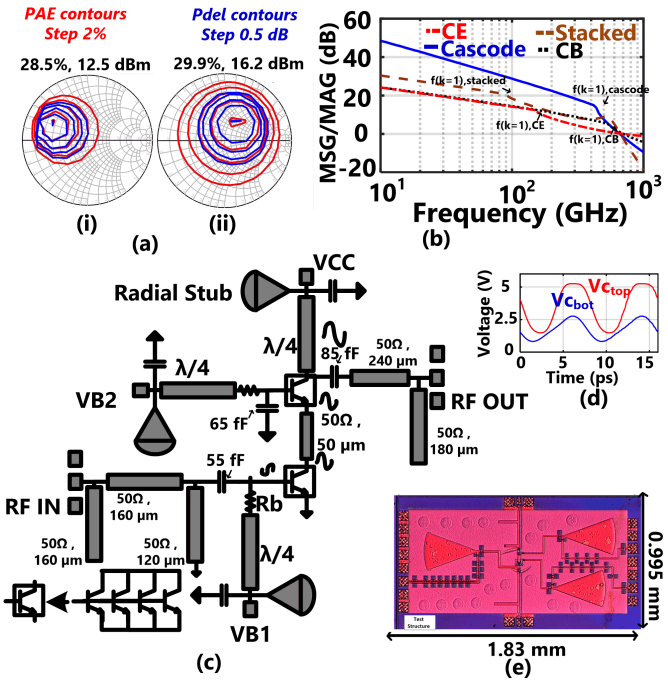

Figure 2.6: (a) Loadpull contours for class A (i) CE (Common Emitter) (ii) Stacked PA (Power amplifier). Each stage in the CE and stacked PA was comprised of 4 transistors, each 6 µm long (b) MSG (Maximum Stable Gain) comparison for the CE, CB and stacked topology. (c) Schematic of the stacked PA (d) Collector voltage waveform at the two nodes (e) Die photo of the stacked PA.

2.3.3 Stability analysis

The K and Rollet factor analsyses are unable to capture instability in amplifiers that have more than just a single input and output node, i.e in amplifiers that have multiple stages or ones that have intermediate nodes. This is because an instability at the intermediate node Amplifiers operating at power levels that vary significantly in operation can also suffer from parametric oscillations and bifurcations, especially at $f_0/2$. There is also a potential for an onset of instability without the amplifier being excited while at quiescent bias. In this work, stability is checked using the small signal method mentioned above, and by using a large signal auxiliary generator method [79, 80]. A 150 Ω resistor is seen to guarantee stability in all the analyses, and is used in the design.

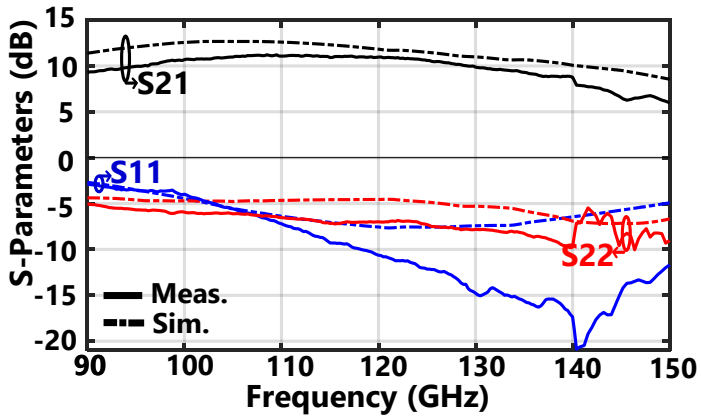

Figure 2.7: Simulated and measured S-parameters of the PA showing a 3 dB gain bandwidth of 45 GHz.

2.4 Measurements and results

2.4.1 CW measurements

A die photo is shown in Fig. 2.6 (e). The small signal S parameters were measured across two bands - WR8 and WR5, using Virginia Diode Inc. (VDI) Vector Network Analyzer Extenders (VNAx) interfaced to a Keysight PXA Vector Network Analyzer (VNA). The small signal S parameters (simulated and measured) are shown in Fig. 2.7 (c). The peak measured gain is 11.7 dB at 112.5 GHz and exceeds 10 dB from 95 to 130 GHz.

Large signal measurements were performed from 90 GHz to 140 GHz. A Keysight signal generator connected to a VDI WR8 tripler (WR8.0X3) followed by a VDI amplifier is used to drive the input of the power amplifier. The output power is measured using a VDI PM5 power meter. The PA saturates at 8.5 dBm available input power. Fig. 2.8 (a) plots the measured and simulated peak PAE (%), and output power at peak PAE (dBm) across frequency. The measured peak PAE is 18.3%, and the peak output power is 15.3 dBm, at 112.5 GHz. Fig. 2.8 (b) plots the the simulated and measured gain (dB), output power (dBm) and PAE (%) at 112.5 GHz against available input power, showing 7 dB of gain at peak PAE.

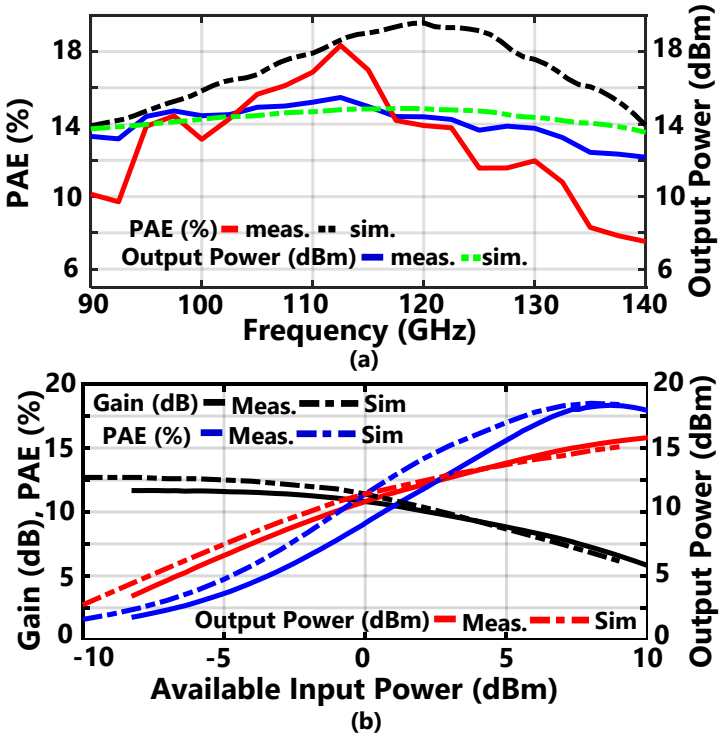

Figure 2.8: Large signal (a) Measured and simulated output power at maximum PAE (%), and maximum PAE (%) (b) Measured and simulated gain (dB), output Power (dBm) and PAE (%) at 112.5 GHz - with a peak PAE and output power at peak PAE, of 18.3 % and 15.3 dBm.

2.4.2 Modulation measurements

Modulation measurements are performed at 121 GHz using the setup in Fig. 2.1. The complete signal chain, without the DUT is equalized across power levels using the VSA software and input power numbers are noted. The stimulus generated is then applied to the chain with the PA. The PA performance is measured up to 5 GSPS QPSK, limited by the equipment - specifically the sampling speed of the AWG. The PA output power and modulation performance are simultaneously measured to arrive at PAE numbers. Demonstrative results are plotted in Fig. 2.9 (a) and (b) for 500 MSPS 16QAM and 5 GSPS QPSK respectively. The trends across average output power level are plotted in Fig. 2.9 (c). The EVM is 14.3% for 5 GSPS QPSK (PAPR of 6.3 dB), operating at an average power of 7.8 dBm - the output power at maximum PAE at 120 GHz is 14.2 dBm. Table 2.1 compares the performance of the PA with prior stand-alone power amplifiers operating at frequencies greater than 100 GHz.

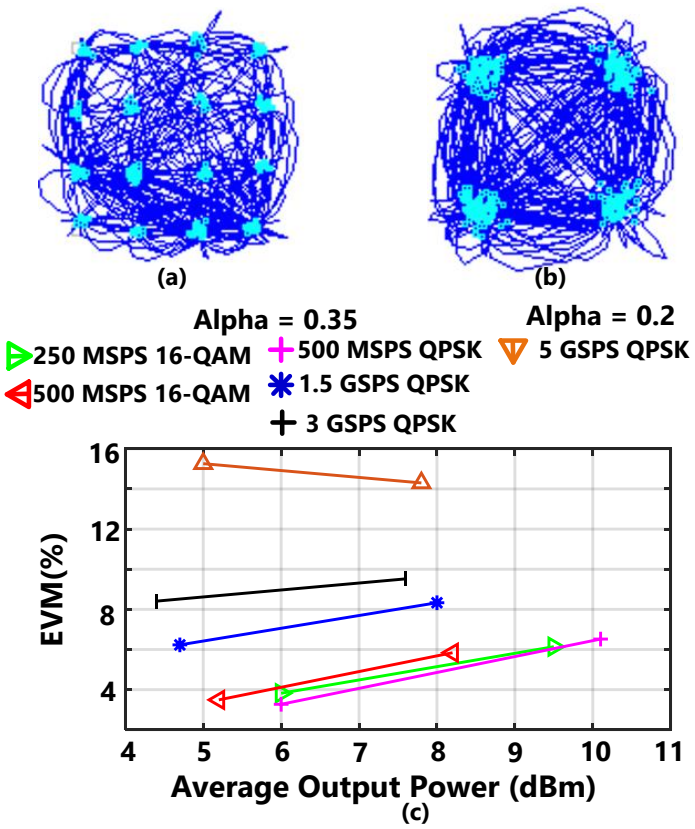

Figure 2.9: Constellations for (a) 500 MSPS 16 QAM and (b) 5 GSPS QPSK. (c) Performance across average output power (dBm), depicting 14 % EVM for 5 GSPS QPSK.

The PA achieves a maximum data rate at state-of-the-art levels while at a higher output power.

2.5 Conclusion and areas for further research

This work presents a scalable modulation chain built using commercial equipment at 121 GHz and its demonstration using a 130nm InP HBT PA. This chain is capable of being extended to higher frequencies, and coupled with the excellent small signal linearity of the VDI frequency translation blocks can open a path to standardizing modulation performance characterization for both transmitter and receiver modules. The PA has a 3 dB small signal gain BW from 90 GHz to 135 GHz with a peak gain of 11.7 dB, peak PAE of 18.3% and peak power of 15.3 dBm at 112.5 GHz. These results demonstrate the highest data rate for stand alone power amplifiers

operating at frequencies greater than 100 GHz, at peak output power greater than 10 dBm using commercially available equipment.

One of the key aspects of a good design starts with a holistic fitting of the transistor parameters to a model, and specifically for power amplifiers - a good thermal model. This was not provided by the foundry and an estimate based on past designs was used for the ballast resistor. The ballast resistor has a significant impact on the poles at the base of the two stages, and hence by extension on the performance at large signal especially when modulated using a wideband signal like this design was. A future line of inquiry could also concentrate on using a simulator like ADS to run a two tone harmonic balance to understand memory effects [78], and to also simulate a wide band modulation excitation to correlate measurement results with the expected results. A future design could benefit from the development of a thermal model with parameters that are coupled with the electrical model like many other foundries provide.

One of the key challenges in obtaining good wideband performance is in maintaining excellent thermal stability across the periphery of the device. This design was characterized on a PCB made from FR4. Although the copper ground plane on the second layer is flooded, the FR4 performs worse as a thermal conductor compared to other ceramic substrates. Future work could also benefit from an analysis of better packaging mechanisms that are able to dissipate the heat generated in the device more efficiently.

2.6 Personal Contributions

- Led the design effort for the PA block including small and large signal instability analyses.
- Led the characterization effort at small signal and CW large signal.
- Led the design of the modulation chain and characterization of the PA using

Table 2.1: Table of comparison for stand-alone PAs/Front-Ends at greater than 100GHz

Ref.	**This Work**		**[68]**	**[81]**	**[62] /[82]**	
Pout 1dB BW (GHz)	97.5-122.5		107-135**	147-153.5**	125-145**	
Technology	130nm InP		130nm SiGe	45nm CMOS SOI	250nm InP +CMOS	
PA Topology	1 stg. stacked		8 way slotline comb. Doherty	Tx FE.	4 way combined	
Psat (dBm)	**15.3**		22.7	1.9	17	
Peak PAE (%)	18.3		18.7	11**	20	
@ (GHz)	112.5		110	149.9		
Peak S21 (dB)	11.7		21.8	22.5**	20	
Mod. Freq.	**121 GHz**		131.5 GHz	150.7 GHz	135 GHz	
Mod. Format	**16 QAM**	**QPSK**	16 QAM	64 QAM	64QAM	16QAM
Data rate (Gb/s)	2	**10**	8	10.56	6	4
EVM	**5.8%**	**14.3%**	11.6%	9.5%	12%**	12%**
PAE_{avg}	**5.2%**		7.9%			
$Pout_{avg}$	**8.2 dBm**	**7.8 dBm**	13.7 dBm	0.1 dBm		
$Pout_{peak}$					11 dBm	11 dBm

****Estimated from plots**

this chain.

- Led the manuscript writing and review response efforts.

2.6.1 Acknowledgements

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Chapter 3

DAT - A millimeterwave extension : Analysis and characterization

3.1 Introduction

This chapter details the design and analysis of an extension of the Distributed Active Transformer power amplifier to millimeter wave frequencies using asymmetric coupled lines. An exhaustive level of detail of all the design decisions made are explored in this chapter. The DAT PA uses the stacked PA from the previous chapter as the unit cells for the driver and power stages.

Several PAs have been implemented using InP technology above 100 GHz with peak output power up to 24 dBm [83–88]. On-chip power combiners are used to further increase the output power from a single stage PA. [84, 86] use Wilkinson based power combiners for reasons of stability and low loss performance. Tline based one like and [85, 87] typically have even lower loss since the lines are shorter than a quarter of a wavelength. However, they typically suffer from a lower operating bandwidth. The Distributed Active Transformer (DAT) is a compact and low-loss power combining technique [89] and has been developed up to 77 GHz [90, 91]. However, further use of this technique is limited by the parasitics at higher frequen-

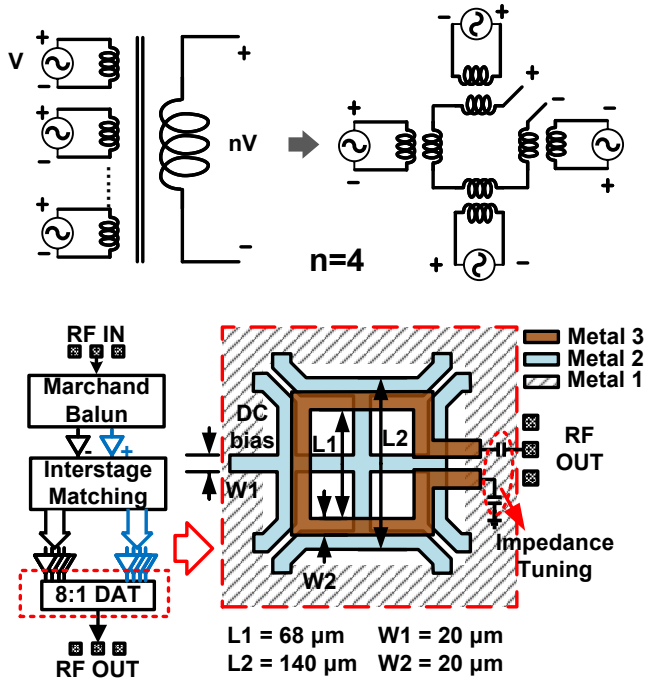


Figure 3.1: Coupled inductors model of the DAT power combining topology (top), and proposed 2-stage DAT PA with single-ended output (bottom).

cies. This paper extends the DAT operation frequency up to 120 GHz with efficient 8-to-1 power combining with the help of the proposed asymmetrical coupled transmission line (Cline) model. This chapter details the design and characterization of a DAT bsed PA capable of a peak 22.1 dBm output power and 11.5% PAE [92].

The chapter is organized as described below. Section 3.2, introduces the design, analysis of the limitations of the DAT architecture, and proposes a high-frequency model. Further, the block-level design details and analysis are shown in Sections 3.3, 3.4, and 3.5 . The measurement setup and the results are shown in section 3.6. Section 3.7 concludes this work.

3.2 DAT design and model

As is evident in Fig. 3.1, the DAT is primarily modeled with coupled inductors. A number of n individual primary inductors are voltage combined to achieve n times voltage and power on the secondary side. Due to the differential operation on the

primary input, the center of the inductor acts as a virtual short at the fundamental and all odd harmonics. Thus the DC supply can connect directly to this point without a bias tee or quarter-wave transmission line to improve efficiency. This is of course under the caveat that the bias line does not impact the behavior at even harmonics significantly - something that the designer needs to keep in mind. The traditional transformer-based model is only valid at RF frequencies, because the size of the transformer should be considerably smaller than a wavelength to avoid any distributed effects. In addition, the inter-winding capacitance between primary and secondary can be neglected only at lower frequencies. As frequencies increase, these factors become increasingly important. Certain capacitance and self-inductance can be added to the model to improve its accuracy up to 100 GHz [93]. However, this requires a complex model with many parameters, and decreases in accuracy for large bandwidth applications [93].

Fig. 3.1 shows the block diagram of the proposed power amplifier. The input signal is converted into differential signals by a balun and fed to the driver stage. The output power of each driver is divided equally into four parts by a Tline-based power splitter to drive four power units that also serves as the impedance matching network. An 8-to-1 DAT is implemented as an output matching network to combine power and output a single-ended signal to make the configuration a single ended input to single ended output amplifier.

3.2.1 Fully differential configuration

To further extend the DAT to higher frequencies, a Cline model and the proposed fully differential 8-to-1 DAT (n=4) are introduced in Fig. 3.2. Each side is modeled as two coupled lines. Certain simplifications are introduced to make the model easier to work with. Asymmetric coupled lines are used in the model since the primary and secondary windings are not symmetric in our implementation - these are on different metal layers. [5] introduced theory for asymmetrical coupled line and its

lumped-element equivalent. Resistors are inserted to model metal losses in the lines as shown in Fig. 3.2. $C1$, $C2$, and $L1$, $L2$ represent the self-capacitance and inductance of each line. C_m and L_m are the mutual capacitance and inductance between the two lines. The impedance presented to the PA can be realized by choosing the proper parameters within certain constraints owing to DRC (design rule check) limits. The primary winding is between port 3 (P3) and port 4 (P4) and the secondary winding is between port 1(P1) and port 2 (P2). The primary capacitance $C_2 - C_m$ is 1.8x of the $C_1 - C_m$ as expected because the primary is closer to the ground. Thus, this cannot be simply modeled with a symmetrical coupled line requiring $C1 = C2$ and $L1 = L2$ and requires the use of this asymmetric model.

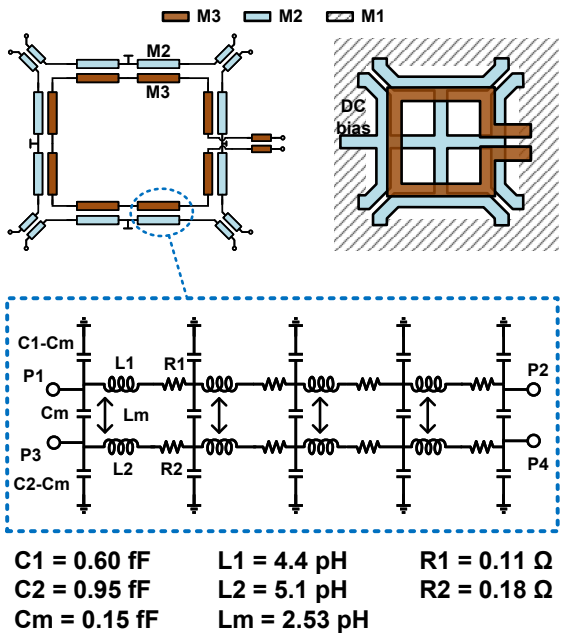


Figure 3.2: Asymmetric coupled line model[5] applied in the DAT and its corresponding layout.

There are typically two dominant mechanisms for coupling in coupled lines - broadside and edge based coupling. Considering that capacitive coupling contributes to the inter-winding capacitance, the broadside coupled lines are offset in this design. To evaluate the tradeoffs between these two configurations, a 68 μm long, 20 μm wide edge-coupled couple line on M3 with the minimum spacing al-

lowed by the technology, and an identically sized broadside coupled line on M2 and M3 with 16 μm offset are simulated using HFSS. While the area of the edge coupled lines are 22% higher than the broadside coupled lines, the loss is only 0.3 dB lower. In this implementation, broadside coupled laterally-offset traces on M2 and M3 are chosen for a compact layout for the actual DAT itself. M1 is chosen as the global ground and the ground underneath the DAT is carved out. The Cline model with a 4 μm overlap is used to match the C_m in the lumped-element model. The center of each primary is used to introduce DC bias. At the differential output of the DAT, two series load capacitors each with a capacitance of 17 fF are used for matching. The full DAT structure is simulated in Ansys HFSS and the S-parameter results are compared to the proposed Cline model in Fig. 3.3. The model and the EM simulated structure agree exceedingly well showing the efficacy of the model while being simple enough to use and intuitively understand.

3.2.2 Conversion to single-ended output

A Marchand balun would be area intensive and contribute to loss at the output. Unlike at the input, a balun at the output has a direct bearing on the performance of the PA since this is after the gain stages and before the output, and hence cannot be accounted for merely by an increase in input power. In simulations of the differential output configuration, the efficiency of the DAT including the input impedance mismatch, is found to be 88%. However, if a balun were to be used and if a perfect match was achieved between the DAT and the balun, the maximum achievable efficiency would be drop to 55.5%. The DAT's operation relies on the input and output operating in a differential fashion to maintain symmetry. Merely keeping one of the secondary terminals open or shorting would have increased the imbalance seen by the various stages at the various points. A small shunt capacitor is used at the output to replace the combination of the series capacitance and a 50 Ω load resistor to achieve better performance, while avoiding power dissipation in the dummy load.

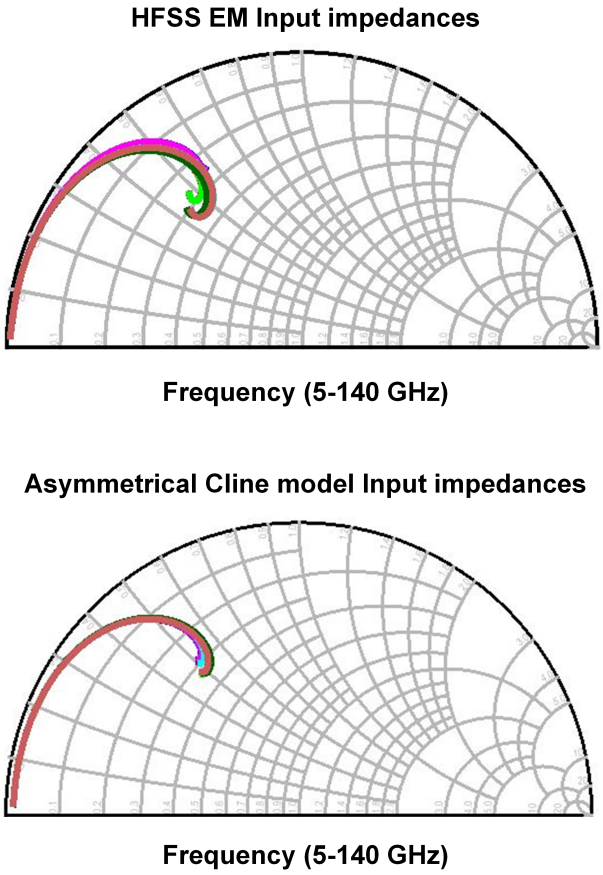


Figure 3.3: Comparison of simulated input impedance of the differential DAT between the Asymmetrical Cline model and the EM model.

The simulated passive efficiency and total efficiency versus the value of the shunt capacitor are plotted in Fig. 3.4. The simulation is conducted using an available power of 0 dBm for each input, with the power source impedance set to the conjugate of the simulated load-pull input impedance of the PA unit. Three different models are compared, including the Ansys HFSS EM simulated model, asymmetrical Cline model, and symmetrical Cline model. The symmetrical Cline model parameter chooses the average value of asymmetrical parameters - here, $L = (L1 + L2)/2$. The asymmetrical Cline model presents similar results as the EM simulated model, while the symmetrical Cline model yields a peak efficiency at 2 fF, which is primarily from the inaccuracy due to the assumption of $C1$ being equal to $C2$. With the asymmetrical Cline model, the single-ended DAT achieves 72% peak total efficiency with an 8 fF shunt capacitor and is 1 dB better than using an area-expensive balun.

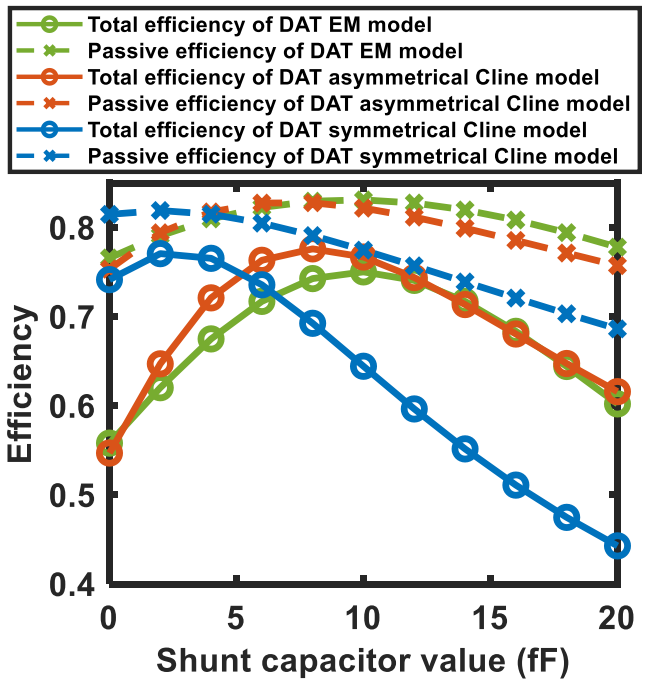


Figure 3.4: The passive efficiency and total efficiency vs the shunt capacitor value of DAT EM model, asymmetrical Cline model, and symmetrical Cline model.

The total efficiency changes more significantly than the passive efficiency change when the shunt capacitor value increases. This confirms that the shunt capacitor primarily helps with impedance matching as expected. Using this capacitive termination technique, the DAT in differential operation can be converted to the single-ended operation while maintaining high efficiency with minimal area overhead.

After the final design, the entire DAT PA is simulated in the Ansys HFSS FEM simulator, including the bias networks and interstage matching. A customized 8 fF parallel plate capacitor between M2 and M1 is used to terminate one of the outputs as shown in Fig. 3.1. The DAT achieved a simulated loss of 1.16 dB at 135 GHz as shown in Fig. 3.5. In addition, the simulated loss including metal loss and impedance mismatch is less than 1.3 dB from 120 GHz to 140 GHz.

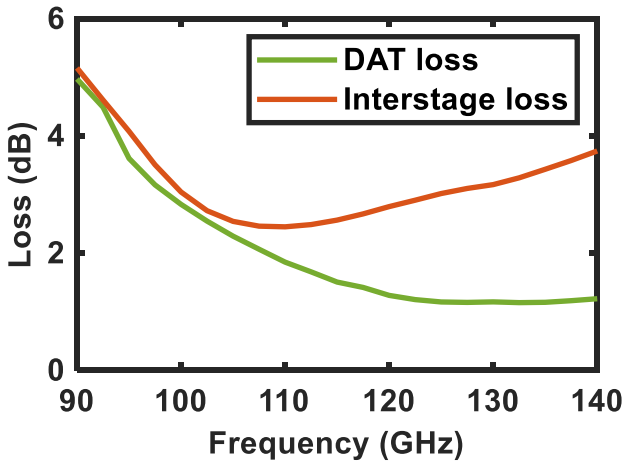


Figure 3.5: HFSS EM Simulated DAT loss and interstage loss including the metal loss and impedance mismatch.

3.3 Single stage PA design

The PA is implemented in the Teledyne InP 130 nm HBT technology with a breakdown voltage BV_CEO of 3.5 V, and a typical DC beta ~18. Simulated f_t/f_{max} is 521 GHz/1.15 THz[94]. Each HBT symbol in the schematic represents four HBTs in parallel, each 6 μm wide. The transistor embedding structures and Tlines are simulated in the Keysight Momentum EM simulator and include all the effects from the metal connection to the HBT, base capacitor, and quarter wavelength bias line. The load-pull impedance is 22+23j Ω as shown in Fig. 3.6 and the source impedance is 4+5j Ω. The peak achievable PAE is 25.9% with 14.7 dBm output power at 120 GHz. The differential driver unit adopts the same stacked structure, but the input impedance is matched to 50 Ω with the additional input matching network. Each driver unit drives four power units. A 5 Ω resistor is added to the emitter in the driver stage to quash potential common mode oscillations that were seen from a stability analsys in Keysight ADS. The additional DC power from the drop across the 5 Ω resistor lowers the PAE by less than 1 % in this specific implementation.

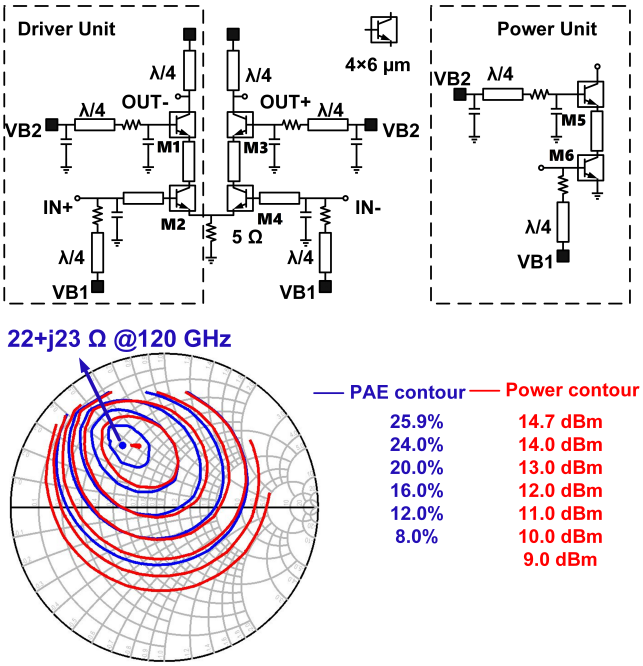


Figure 3.6: Schematic of the proposed stacked PA unit and the load pull simulation of the power unit.

3.4 Power splitter design

A Tline-based structure is adopted for the power splitter, and the output of the driver unit is directly matched to the input of the power unit as shown in Fig. 3.7. The adopted geometry is fully symmetric along the x-axis in the figure, to ensure that all of the differential signal paths are delayed equally. In addition, the electrical length of each Tline section are designed to be the same irrespective of asymmetry across the y-axis.

The InP 130 nm technology used in this design only offers three metal layers. The distance from M3 to M1 is much larger than the distance from M2 to M1. A Microstrip transmission line (Tline) with M1 ground shows substantially different characteristic impedance for an identically sized signal line on M2 compared to M3. Reducing the width of the M2 traces helps but is limited by the design rule checking (DRC) in this design. The crossover of M2 and M3 would cause impedance and phase imbalance and degrade the PA output power and efficiency if they are not

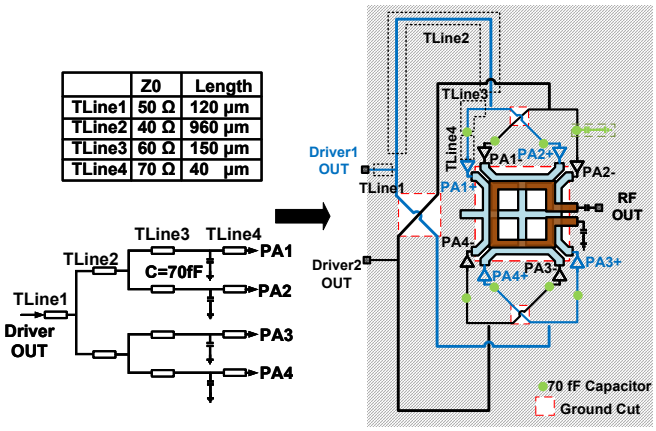


Figure 3.7: Proposed 2-to-8 power splitter co-designed with PA.

taken into account. Therefore, ground cuts are implemented at the crossover region to reduce the mismatch. The waveforms of each power splitter output, when inputs are driven differentially, are shown in Fig. 3.8. The ground-cut version has a higher amplitude and has improved phase balance proving the efficacy of the methodology adopted. Since the power splitter is AC coupled to the output of the driver stage and DC coupled to the input of the power unit, the base bias of the CE HBT in the power stage is injected at the low impedance locations on the power splitter with a quarter-wave Tline to the DC pad. This eliminates the need to design a complex bias network near the active region. The EM simulated loss is ~2.5 dB to 4 dB and includes the metal loss and impedance mismatch, as shown in Fig. 3.5.

3.5 Input Balun Design

The single-ended input signal is converted to a differential signal by a Marchand balun and fed to the driver. In order to increase coupling, the balun is designed with signals on M1 and M2 while using M3 as ground. Since the remainder of the circuit uses M1 as ground, the ground plane is transitioned from M3 to M1 as shown in Fig. 3.9a, and this is included in the EM simulation of the balun. The simulated balun has less than 0.49 dB amplitude imbalance and less than 3.7 degree phase imbalance across 120 GHz to 140 GHz as shown in Fig. 3.9b. The excess loss at each

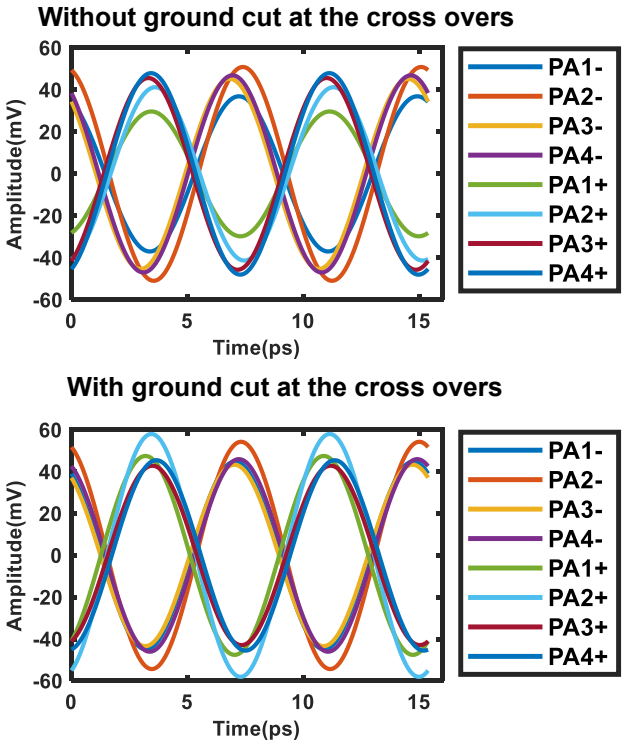


Figure 3.8: A comparison of the splitter output without and with the ground cut applied.

output at 130 GHz is 1.9 dB and 1.7 dB for the two output ports respectively, and is less than 3 dB across 120 GHz to 140 GHz. All the ports are matched to 50 Ω and the simulated |S11| is less than -10 dB |S11| across from 125 GHz to 140 GHz.

3.6 Measurement Results

3.6.1 Small signal measurements

The design is fabricated in Teledyne's InP 130nm technology is shown in Fig. 3.10. The chip occupies 1.86 mm * 1.56 mm including pads. The core DAT only occupies 0.5 mm * 0.36 mm, and most of the chip area is occupied by the power splitter. Thru substrate vias are systematically placed over the entire chip to eliminate possible substrate modes. All the measurements are performed on a MPI TS150-THZ probe station. The chip is biased through MPI Multi-Contact Probes. Formfactor

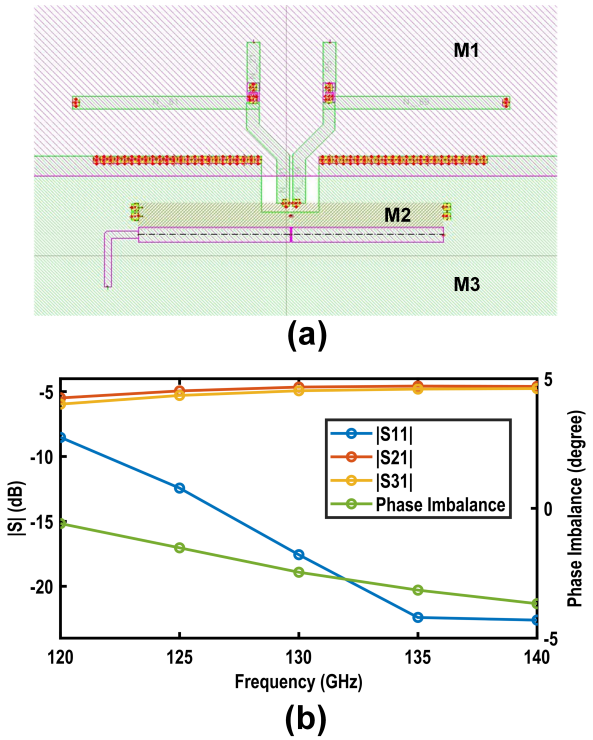


Figure 3.9: (a) Marchand balun layout showing the ground plane change. (b) EM simulated |S| parameter and phase imbalance of the balun.

WR-8 Infinity GSG probes are used at the RF input and output pads. The power stage consumes 215 mA DC current at 3.55 V VCC. Due to the additional emitter resistance at the driver stage, the driver stage has a higher base bias and supply voltage. It consumes 63 mA current at 4.1 V supply.

S-parameters are measured by using the Keysight PNA-X Vector Network Analyzer and WR8 VDI VNA extenders. The signal is attenuated by a waveguide attenuator at the input to ensure small signal operation. An on-die TRL cal standard set was used for calibration. The measured S-parameter is shown in Fig. 3.11. The implemented PA achieves 40 GHz 3dB small signal bandwidth from 100 GHz to 140 GHz and 17.77 dB peak |S21|at 133.75 GHz. Furthermore, the PA is unconditionally stable across the entire F band in measurements.

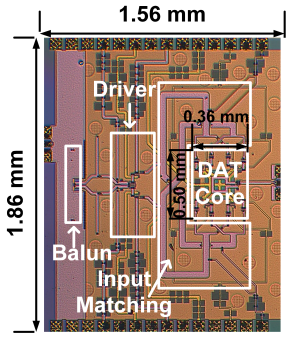


Figure 3.10: Die photo of the proposed DAT-based PA.

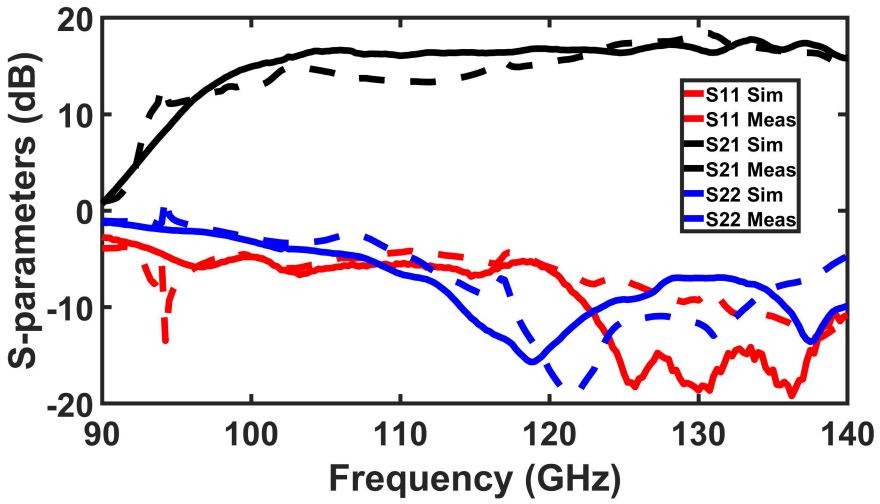


Figure 3.11: Measured and simulated S-parameter from 90 GHz to 140 GHz.

3.6.2 Large signal measurements

The measurement setup is shown in Fig. 3.12a. The input signal from the Keysight signal generator is upconverted to the F band with a VDI tripler. A VDI WR9 amplifier is inserted to drive the PA to saturation. A VDI PM5 power meter is used to measure the output power. The probe loss is calibrated out by landing probes on a short through. The measured output power, gain, and PAE versus available input power at 120 GHz are shown in Fig. 3.12b. The measurement matches the HFSS simulation within 0.6 dB. The PA achieves 22.1 dBm peak output power with 11.5% PAE and 8.6 dB large signal gain at 120 GHz. The measured saturated output power (Psat) and PAE vs frequency is shown in Fig. 3.12c. The prototype PA achieves 117.5 - 130 GHz Psat 1-dB bandwidth. The output 1 dB compression is

20.3 dBm with 8.7% PAE and 13.8 dB gain. The upper frequency limit of the measurement is limited by the bandwidth of the WR9 amplifier. The PA has larger than 20 dBm saturated output power from 115 GHz to 130 GHz with PAE higher than 7%.

3.6.3 Modulation results

The modulation measurement setup is shown in Fig. 3.13[95]. The baseband I/Q signals are connected to the mixer with a pair of phase-matched cables to the Marki IQ mixer (MMIQ 0520HS), and up-converted to 10 GHz first. 111 GHz carrier is generated by a VDI SGX as a frequency tripler with a 37 GHz signal source. An attenuator is inserted after the SGX to provide appropriate LO power to the input of the mixer. Then the 10 GHz signal is upconverted to 121 GHz by the VDI WR8.0 BAM mixer. The VDI WR6.5BPF filters out the image for linearity consideration. After the signal is amplified by the device under test (DUT), 1/10 of the power is coupled to the PM5 power meter to measure the output power. The rest of the signal is further down-converted to 4 GHz to fully utilize the 8 GHz bandwidth of Keysight's DSO804A oscilloscope, where the signal is demodulated by using Keysight Vector Signal Analysis (VSA). Finally, PSG E8257D's 10 MHz reference is connected to the rest of the signal generators, M8190 arbitrary waveform generator (AWG), and the oscilloscope's external clock to sync the system.

The measurement setup without DUT is equalized to eliminate the channel distortion from the setup itself. Due to the output power limitation of the equipment, the modulation is measured at the backoff region of the PA. The measured 16 QAM, 64 QAM, and QPSK modulation results are shown in Fig. 3.14. The root-raised-cosine (RRC) filter used in all setups had a value of roll-off factor $\alpha = 0.35$. The results showed that at a data rate of 12 Gbps and 16 QAM modulation, an 8.0% root-mean-square error vector magnitude (rms EVM) was achieved, with an average output power of 14.5 dBm and 3.3% PAE. Additionally, the DUT was also measured

with 64 QAM/QPSK at a max data rate of 1.5/8 Gbps resulting in 3.8%/11.4% rms EVM.

3.7 Conclusion

This work first presents a Cline model of DAT to accurately predict input impedance and passive efficiency. Then, a 22.1 dBm output power PA with 11.5% PAE at 120 GHz is implemented by using a compact DAT as output matching and power combining network. This is the first work to demonstrate the DAT topology beyond 100 GHz to the author's best knowledge. This work doubles the small signal bandwidth compared to [85] with comparable output power. In addition, it presents a 14.5 dBm average output power at a 12 Gbps data rate in 16 QAM to show the potential of high-speed wireless communication in the F band. This chapter of the thesis specifically addresses the research question on how the DAT method could be extended to millimeter wave frequencies, and especially to technologies where the vertical separation between metal layers introduces complex asymmetries.

3.8 Personal Contributions

- Co-Led the design effort for the unit cell.
- Contributed to the stability analysis efforts.
- Contributed to small signal, large signal CW and modulation characterization efforts.
- Contributed to the manuscript writing efforts.

3.8.1 Acknowledgements

Linsheng Zhang, Jay Sheth, Robert M. Weikle, Steven M. Bowers, Travis Blalock, Jeffrey Hesler.

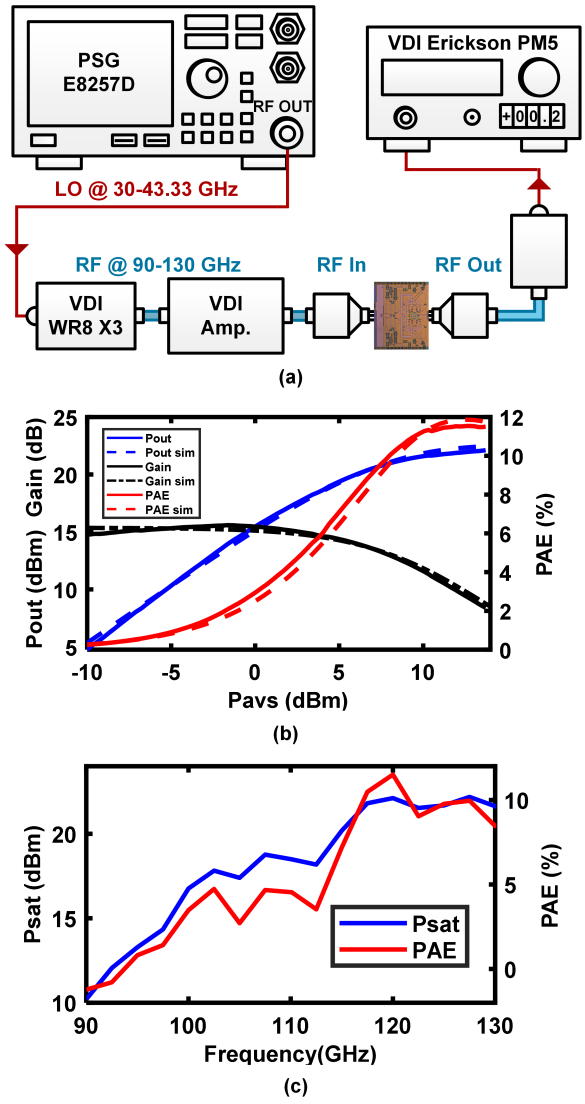


Figure 3.12: (a) Large signal measurement setup. (b) Measured and simulated output power, gain, and PAE versus available input power at 120 GHz. (c) Measured saturated output power and PAE versus frequency.

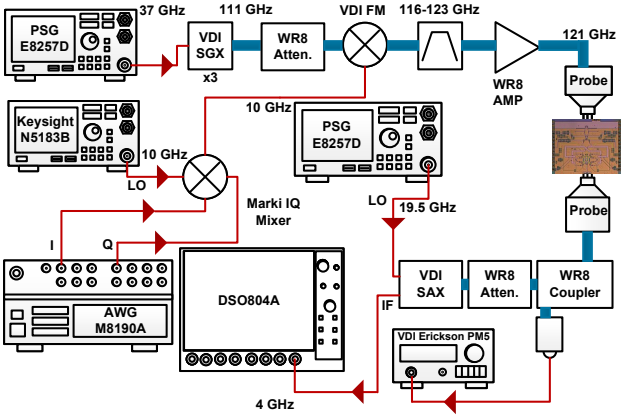


Figure 3.13: Modulation measurement setup and measured rms EVM vs symbol rate.

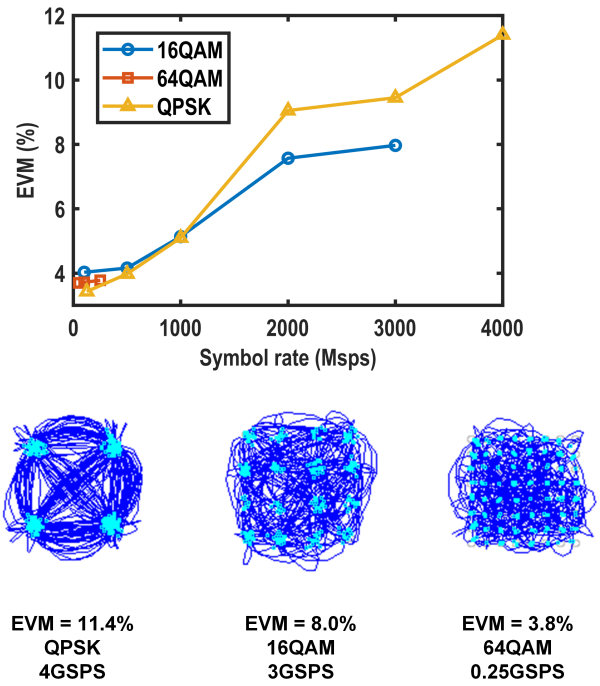


Figure 3.14: Measured rms EVM vs symbol rate in QPSK, 16 QAM, and 64 QAM modulation formats.

Chapter 4

Circuits for terahertz phase conjugation

The terahertz spectrum is generally accepted to be radiation with a frequency in the range of 300 GHz to 3 THz. Terahertz radiation has interesting properties - they combine many of the advantages of microwave and visible light. The radiation has small wavelengths and extremely wide bandwidths. This can allow very high spatial resolution images even with less complex systems. THz radiation also displays specular and diffuse scattering - all extremely attractive in imaging around obstacles and maintaining narrow "pencil"beams [8, 96].

There is a rich plethora of research in co-designing transistor arrays with multi-functional EM elements to realise radiators [97–99], power-combined arrays [100], holographic metasurfaces [101] and many more applications. Phase conjugation at THz has its own challenges, primarily limited by the lower f_{max} of transistors, the design complexity involved in antenna integration and the ability to detect low power levels. In what follows, we propose a novel architecture that achieves phase conjugation at 300 GHz using 4 "pixels" in the 250nm InP HBT Teledyne node (with a f_t/f_{max} of 350 GHz/650 GHz).

4.1 Conceptual description of the process

In this section, we define and detail the features of phase conjugate waves (PCWs) [102].

Suppose we have an input plane-monochromatic wave given by

$$\mathbf{E}(z,x,y,\omega) = \mathbf{E}(z,x,y,\omega)e^{-i\omega t} = \mathbf{A}_0 e^{i[kz]}e^{-i\omega t} \tag{4.1}$$

In this equation, z is the longitudinal variable in the direction of propagation,x and y are the radial variables, ω is the angular frequency of the wave, k is the wave vector and A_0 is the real amplitude function. After this wave passes through a distorting medium, it becomes

$$\mathbf{E}^{'}(z,x,y,\omega) = \mathbf{E}^{'}(z,x,y,\omega)e^{-i\omega t} = \mathbf{A}_0 e^{i[kz+\phi(z,x,y)]}e^{-i\omega t} \tag{4.2}$$

If there is a plane mirror, the reflected wave will be of the form

$$\mathbf{E}^{''}(z,x,y,\omega) = \bar{R}.\mathbf{A}_0 e^{i[-kz+\phi(z,x,y)]}e^{-i\omega t} \tag{4.3}$$

After passing through the same medium, this becomes

$$\mathbf{E}^{'''}(z,x,y,\omega) = \bar{R}.\mathbf{A}_0 e^{i[-kz+2\phi(z,x,y)]}e^{-i\omega t} \tag{4.4}$$

where $\bar{R}$ is the amplitude reflectivity of the mirror.

However, if this mirror was replaced by a phase conjugating surface,

$$\mathbf{E}^{''}(z,x,y,\omega) = \bar{R}^{'}.\mathbf{A}_0 e^{i[-kz-\phi(z,x,y)]}e^{-i\omega t} \tag{4.5}$$

where $\bar{R}^{'}$ is the effective amplitude reflectivity of the phase conjugating surface.

After passing back through the distorting medium, this becomes

$$\mathbf{E}'''(z,x,y,\omega) = \bar{R}'.\mathbf{A}_0 e^{i[-kz-\phi(z,x,y)]} e^{-i\omega t} e^{i[\phi(z,x,y)]} = \bar{R}'.\mathbf{A}_0 e^{i[-kz]} e^{-i\omega t} \tag{4.6}$$

Thus an ideal plane wave is obtained again, and the aberration influences from the medium are entirely obviated.

The popular architectures for implementing phase conjugation using RF/microwave circuits involves some form of mixing. Next, we detail the mathematics that underlie this operation.

Consider the typical fundamental mixing operation where a signal at frequency RF is mixed with a signal at frequency LO as below.

$$\begin{aligned} V_{IF} &= V_{RF} cos(\omega_{\mathrm{RF}} t + \phi) V_{LO} cos(\omega_{\mathrm{LO}} t) \\ &= \frac{1}{2} V_{RF} V_{LO} [cos((\omega_{\mathrm{LO}} - \omega_{\mathrm{RF}})t - \phi) + cos((\omega_{\mathrm{LO}} + \omega_{\mathrm{RF}})t + \phi)] \end{aligned} \tag{4.7}$$

If the LO frequency is double the RF, the phase of the output IF at the RF frequency is now reversed with respect to the input.

4.2 Overview of the architecture

Traditional phase conjugating architectures use a LO at double the RF frequency [103], or at the RF or half the RF frequency in the case of subharmonic mixers [58, 104]. The subharmonic mixers rely on appropriate phasing of the signals to cancel certain output products while performing the mixing operation. However architectures that have been used at lower frequencies do not lend themselves easily to extension at the higher mmwave, and do not readily exist. This is therefore an interesting areas for exploration.

Extending the subharmonic mixer technique to the upper mmwave comes with additional challenges - the need to generate multiple phases on-chip or to use circularly polarized LO waves. In the latter case, the challenges involved in the imple-

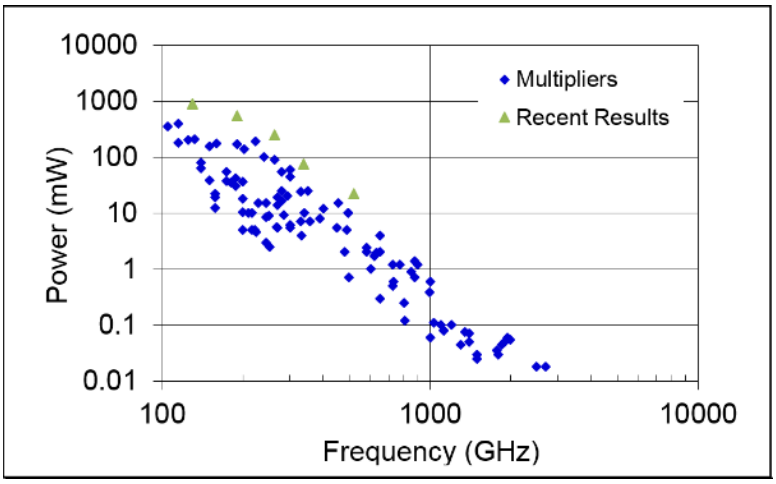


Figure 4.1: Measured output power vs frequency for frequency multiplier based sources produced by VDI. [6]

mentation of antennas, measurements and isolation between various frequencies for the array can become prohibitive. In the former case, on-chip passive phase shifters are lossy especially at the frequencies involved and consume chip area. Generating the amount of power needed at the LO frequency can be challenging especially as frequencies move up. For comparison, Fig. 4.1 plots the output power (mW) vs frequency for millimeter wave sources produced by VDI. The available power decreases drastically as frequency goes up.

The architecture we propose 1) Uses a lower frequency LO off chip (150 GHz) and quadruples it on chip 2) Separates the input RF signal (301 GHz) (RF_{in}) and the phase conjugated beam (RF_{out}) by polarization 3) Uses a Frequency Selective Surface to separate the two input (LO and RF) signals in two opposing hemispheres with respect to the chip 4) Uses a double folded slot for the LO 5) Uses the annular slot as a multi-port structure/ "pixel" for both reception of the RF and transmission of the phase conjugated signal 6)The RF_{in} input on each antenna is single ended. This supports the RF_{in} coming in at any angle. The mixer is an adaptation of the Gilbert Cell micromixer - the desired RF_{out} is differential, while the leakage at the output at the RF_{in} frequency is common mode/in-phase. The input node is also at a virtual short for the output given the differential operation - making the isolation

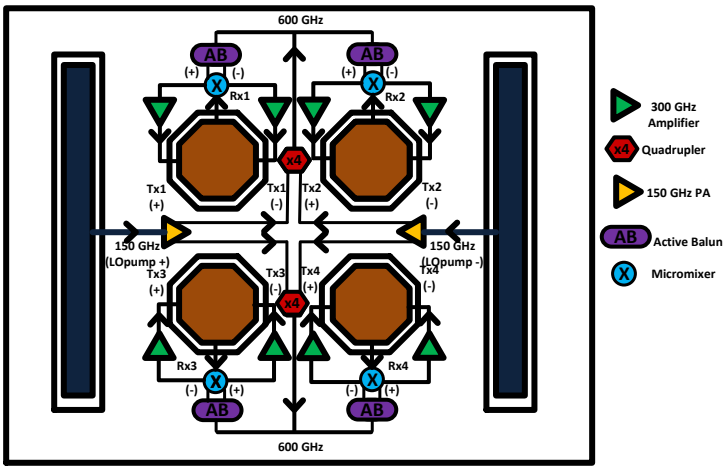


Figure 4.2: Architecture of the proposed array depicting the positions of antennas and various circuit building blocks.

of the input to output more robust.

Antennas on substrates radiate preferentially through the substrate [105]. The ratio of the two powers is $\epsilon_r^{(3/2)}$. The proposed chip will be suspended on a lens for measurements [106]. The lens is included in all simulations to obtain accurate results. All matching components are implemented using microstrip transmission lines with the first layer as the metal ground. The antennas are also built on the same layer.

Fig. 4.2 details the architecture and the various circuit building blocks along with the flow of various signals. The folded slots and annular slots are outlined in purple and brown respectively. By virtue of the placement of the folded slots, a linearly polarized LO signal will produce signals out of phase at the inputs to the two 150 GHz power amplifiers. The 150 GHz signal is quadrupled in each of the upper and lower half-planes, and routed to two active baluns to generate differential signals at 600 GHz. These are then routed to a mmwave Gilbert cell micromixer [107]. The micromixer is well suited for this application, having a single ended input and differential outputs. The single ended input accommodates input plane waves at arbitrary angles, not only broadside to the chip. The differential outputs work with

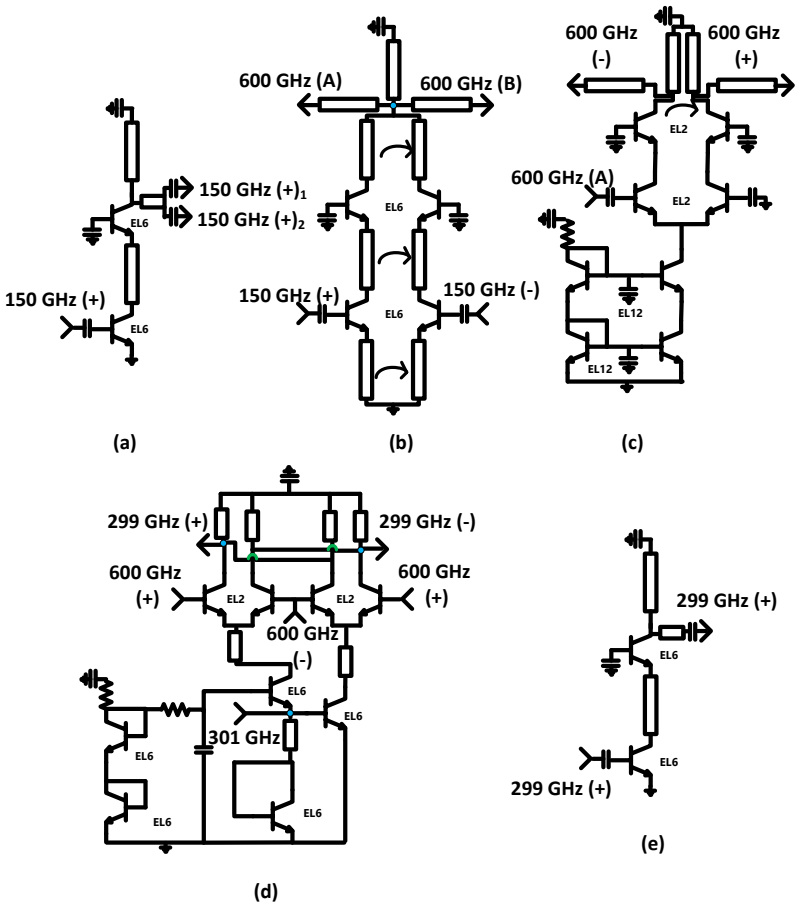


Figure 4.3: Topology of the circuits and primary operating frequencies (a) 150 GHz PA (b) Quadrupler (c) 600 GHz Active Balun (d) Fundamental mixer (e) 300 GHz amplifier. Connections are emphasized with blue dots, and jump-overs with green arcs. Bias connections are not shown explicitly. Curved arrows indicate coupled lines. Emitter lengths are listed. All circuits use two collector contact transistors.

the positioning of the ports enabling only the mixed up/down signal to radiate - the input signal leaking out is common-mode and does not radiate efficiently. The "pixels" are spaced more than half-wavelength (with respect to the RF frequency) in this design to accommodate the electronic signal conditioning circuits, and to decrease mutual coupling issues.

Fig. 4.3 details the architecture of the various circuit building blocks used in the design. The PA is a stacked amplifier adapted to have two outputs as required by the system. The quadrupler is a cascode stage designed for increased isolation between input and output. The active balun provides improved common mode re-

jection ratio (CMRR) at 600 GHz and also provides improved phase and amplitude balance between the two outputs.The micromixer is modified for improved conversion gain, and phase balance between the common-emitter and common-base paths. The small signal amplifier at 300 GHz is a cascode design conjugately matched to the antenna output for optimum performance.

4.3 Description of the antenna building blocks

4.3.1 Frequency selective surface

One of the key issues in designing a phase conjugating array is the stimulation and measurement of such systems. In a typical lens based antenna system, most of the energy radiates through the substrate [105]. A thicker substrate also means loss of power to substrate modes [108]. This makes measurement of the monostatic and bistatic patterns difficult if all of the LO, RF_{out} and RF_{in} antennas have to be co-located. To surmount this issue, we implement a frequeny selective surface (FSS) on the chip. The FSS behaves as a band-pass filter, allowing signals at the RF_{in} and RF_{out} frequencies to transmit through while behaving as a reflector to the LO frequency. The FSS is adapted from previous work [109] in the far-infrared and uses crossed metal dipoles [110] as the unit element. This makes the FSS relatively insensitive to the polarization of the incident wave. Fig. 4.4 (a) depicts the geometry of the unit cell. The cell is designed embedded in InP to emulate the behavior of the circuit when suspended on a lens. Fig. 4.4 (b) depicts the insertion and return loss of the unit cell in a Floquet-mode simulation. The 300 GHz signal sees a low insertion loss whereas the 150 GHz LO is reflected. The Frequency Selective Surface (FSS) is patterned using the Backside Metal (BSM) option provided by the foundry.

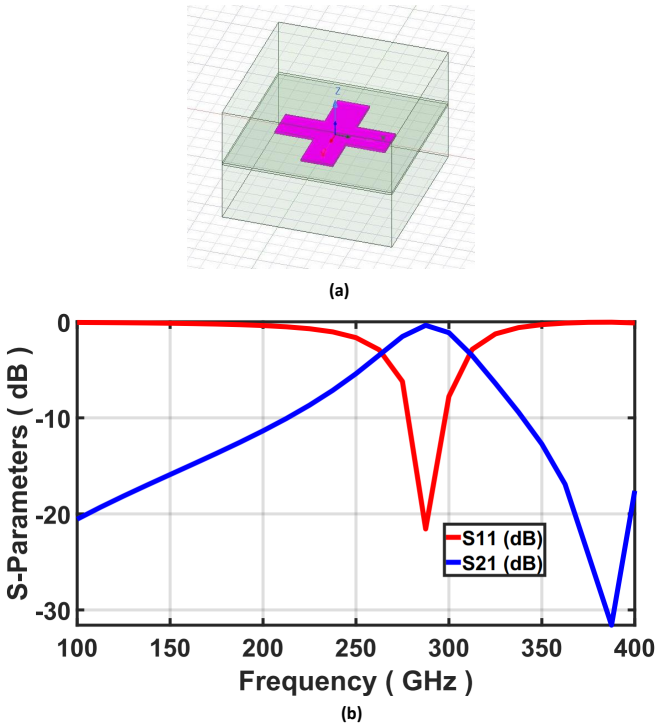


Figure 4.4: (a) Geometry of the FSS unit cell (b) Floquet mode results of the insertion and return loss of the unit cell.

4.3.2 Double folded slot

The double folded slot [111] lends itself to integration with microwave circuits since the signal and ground planes are isolated at DC. The geometry also makes it easier to access differential signals from a linearly polarized incident wave. SIW cavity backed slots can make excellent unidirectional antennas [112]. This process does afford the possibility of through-substrate vias [113] but the dimensions of the vias was electrically large, and their RF performance was unknown. It was also not straight-forward to integrate this with the FSS, so it was decided to use the FSS as a stand-alone reflector. This makes the folded slot antenna's performance a function of the reflections from the sidewalls, the FSS and the lens-air interface. The differential double folded slot antenna suspended on a InP lens is shown in Fig. 4.5 (a). The variation in the gain in the broadside direction as a function of frequency is shown in Fig. 4.5 (c). The gain at a representative point in the frequency response around

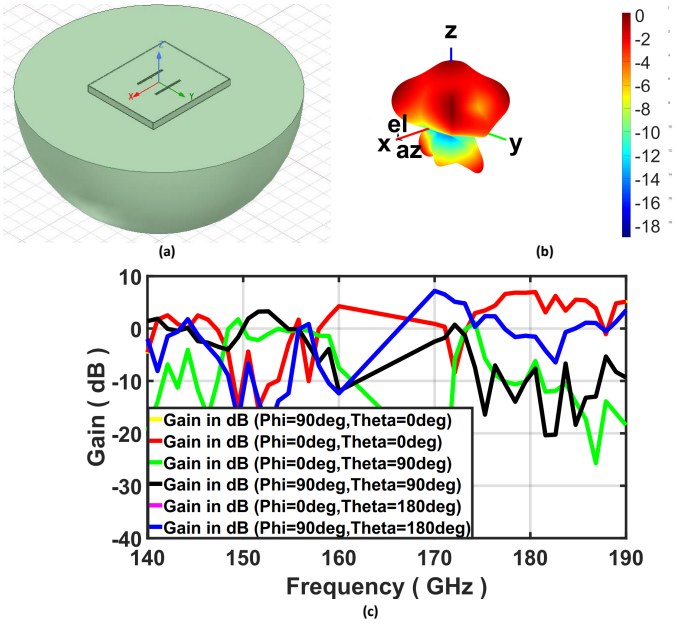


Figure 4.5: (a) Elements of the double folded slot simulation including the lens (b) Gain of the system at 146 GHz (dB) (c) Variation of the gain in various directions as a function of frequency (broadside in bold red).

the LO frequency is shown in Fig. 4.5 (b). The response is primarily broadside (+z) as desired.

4.3.3 Annular Slot

The annular slot is a well-known antenna with properties that have been extensively studied [114]. In the past, work at UVa has focussed on using this structure in the design of HEB mixers [115]. We propose using the annular slot in an array in this design. The geometry of the array with the FSS backing is shown in Fig. 4.6 (a). The gain at 310 GHz is shown in Fig. 4.6 (b) depicting that the FSS is transparent to the RF frequencies as desired. In this particular simulation, all annular slots are each driven at one port and phased for the appropriate polarization.

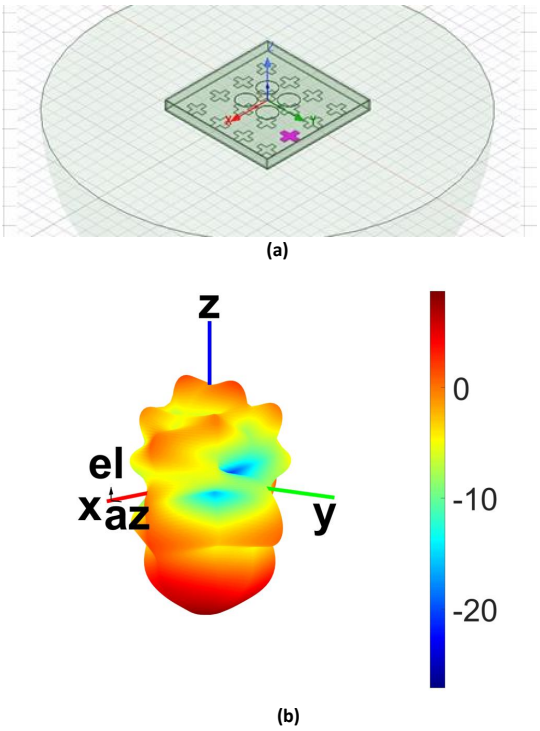


Figure 4.6: (a) Elements of the annular slot array simulation including the lens (b) Gain of the system at 310 GHz (dB).

4.4 System Level Antenna Simulations

Next we detail the performance of the comprehensive antenna system backed by the metal FSS suspended on an InP lens. The separation between various elements are determined by coupling effects and the space required for routing and the placement of the associated circuitry. Fig. 4.7 (a) describes pictorially the geometry of the system, including the various individual antenna elements. Fig. 4.7 (b) shows the gain of the annular slot (RF) system at 303 GHz. The LO double folded slot antennas are terminated by an impedance that represents the input impedance of the circuit connected to the LO antenna when this pattern is simulated. Fig. 4.7 (c) shows the gain of the RF system across frequency for this simulation. Fig. 4.7 (d) shows the gain of the double folded slot system at 153 GHz. The annular slot antennas are terminated by an impedance that represents the input impedance of the circuit connected to the annular slot antenna when this pattern is simulated. Fig.

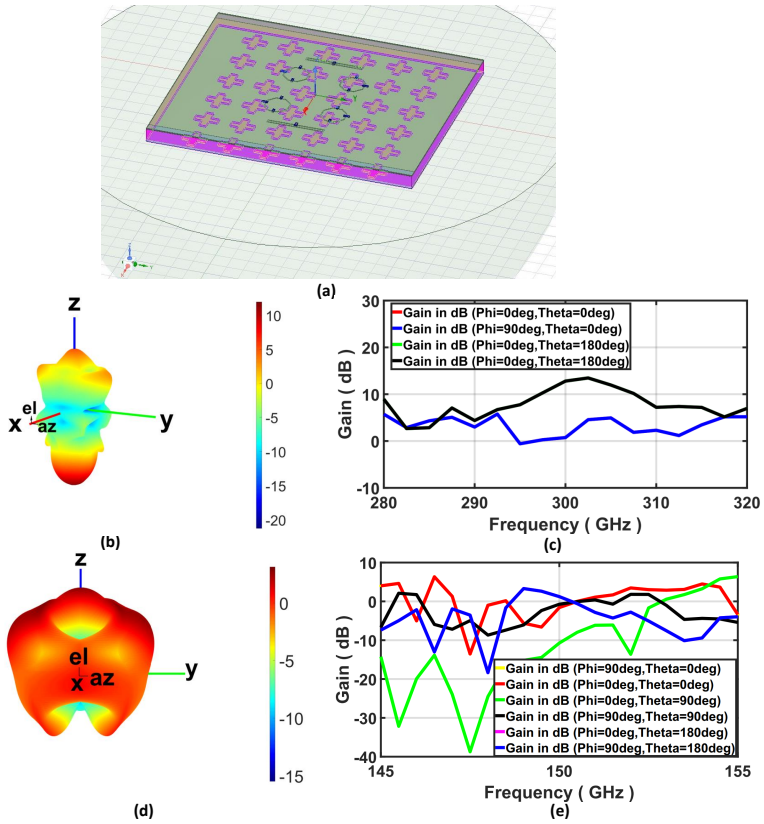


Figure 4.7: (a) Geometry of the final antenna system showing the two double folded slots, four annular slots, the FSS and lens. (b) The gain of the annular slot (RF) system at 303 GHz (dB). (c) The gain of the annular slot (RF) system across frequency (d) The gain of the double folded slot (LO) system at 153 GHz (dB). (d) The gain of the folded slot (LO) system across frequency.

4.7 (e) shows the gain of the LO system across frequency for this simulation. This image provides a complete picture of the full system across the two frequencies. As seen before, the LO system is more sensitive to the thickness and extents of the substrate, and the FSS and lens.

4.5 Circuit descriptions and simulation results

The performance of the system depends on careful co-design between the various antenna blocks and the circuit elements. The performance is also limited by the capabilities of the transistor itself - the published transistor f_{max} is 650 GHz. One of

the most significant challenges is in generating power at 600 GHz and higher without damaging the transistors - the higher input powers lead to higher peak currents in the transistor. The 150 GHz PA is very similar in design to the one implemented previously in chapters 2 and 3 of this thesis, and is hence not expounded here again.

The next subsections go over the design constraints and choices made for each block. The design choices are governed by the necessity to integrate these into the system developed above. The design uses coupled lines extensively to achieve a compact layout, and where possible to keep fields constrained between the coupled lines, given the complexity of the system, and the multitude of frequencies involved. Fig. 4.3 details the schematic of these various blocks. Where necessary, coupled lines are indicated explicitly with a symbol. All circuits are provided with bias using diode connected maximum emitter length transistors and resistor legs. The sizing is shown to not impact the noise of the transistor at relatively low frequencies [116] but the complex interaction at higher frequencies is not simulated and could be a further line of enquiry.

4.5.1 Quadrupler

The quadrupler schematic is shown in Fig. 4.3 (a). The design starts with a large signal simulation for optimization of the harmonics. A differential design is adopted so odd harmonics are idled by virtue of symmetry. Ref. [117] is used to design the quadrupler with some changes based on our design constraints. Coupled lines serve two purposes here - they serve to keep the differential signal tightly coupled and prevent leakage to neighboring circuits. They also help optimize the harmonic generation. The coupled line parameters are swept within certain bounds to obtain the optimum. Since is this is a strictly large signal design, small signal concepts do not apply readily and emphasis is on an empirical approach. The design is biased in deep class-AB since this is seen to maximize the harmonic generation at higher power levels, presumably from the loadline hitting the knee voltage. The leakage

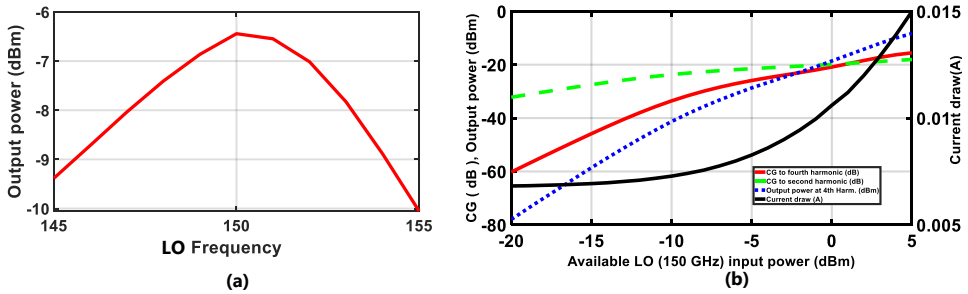


Figure 4.8: (a) Simulated behavior of the quadrupler versus frequency and (b) Behavior of the quadrupler versus available LO power at 150 GHz.

of the second harmonic was minimized to the extent possible within the constraints of area, the quality factor of the components and compromise between leakage and conversion gain to the fourth harmonic. Fig. 4.8 details the (a) Simulated behavior of the quadrupler versus frequency and (b) Behavior of the quadrupler versus available LO power at 150 GHz. As can be seen, the design is optimized to have a peak at around 150 GHz and a sweet spot in terms of simulated generation of the fourth harmonic compared to the second at about 2 dBm Pavs. The quadrupler generates -10 dBm of simulated 4th harmonic power at 4 dBm Pavs at a current draw of 14 mA from a 4.9 V supply. Please note that the power numbers shown on the X axis in Fig. 4.8 reflect single ended output power at each differential input. The total available power would be 3 dB higher by extension. The design is also simulated with the port impedance being the conjugate of the input impedance looking in, as is common in system simulations.

4.5.2 Active Balun (AB)

It is extremely challenging to design a functional balun at these frequencies as required by the mixer - a passive balun would have been extremely lossy and considerably expensive in terms of area on the chip. The active balun on the other hand suffers from amplitude and phase imbalance because of the uneven gains in the two

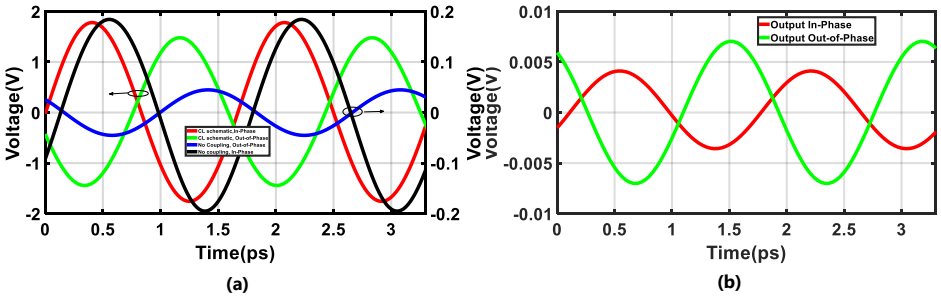


Figure 4.9: (a) Simulated behavior of the AB with and without a coupled line output network in schematic (b) EM simulated outputs of the designed active balun.

signal paths from the input to the two outputs at 600 GHz. There has been some work on mmwave active baluns in HBT that improve the performance of the circuit using coupled inductors [54]. We propose using a coupled line in lieu of coupled inductors. Fig. 4.9 (a) compares the performance of an active balun with a coupled line matching network to one without. Both of these are simulated at the schematic level when terminated at each output with the conjugate of the impedance looking in. As is evident, the amplitude balance is greatly improved in the coupled line version versus the one which does not have coupling at the output. The common-mode rejection is improved by introducing a transmission line to resonate out the capacitance and increase the impedance looking into the current tail. The behavior of the circuit with these modifications is shown. The phase imbalance is within 20 degrees for the stand-alone circuit. The amplitude imbalance is within 5 dB. The simulated common mode rejection ratio is 2 dB and is defined as the ratio of the difference in the single ended voltage outputs divided by the average of the outputs. The mixer behavior is simulated with these numbers. Fig. 4.9 (b) details the behavior of each of the nodes after simulating at the electromagnetic level and accounting for most parasitic.

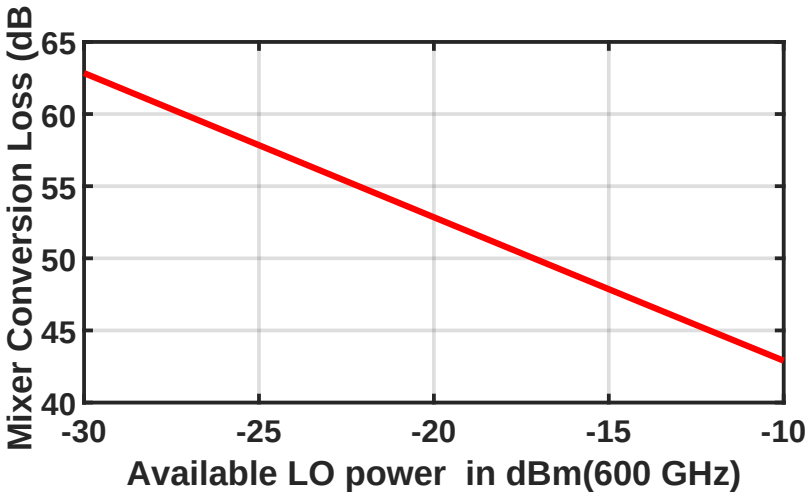


Figure 4.10: Plot of the conversion loss of the micromixer as a function of the available LO power at 600 GHz, in dB.

4.5.3 Micromixer

Fig. 4.10 plots the conversion loss of the micromixer as a function of the available LO power at 600 GHz. The micromixer layout was complicated by the need to integrate with the annular slot antenna. Given the limitations on the number of metal layer available to route signals, emphasis was placed on doing the best possible design with the best conversion loss. The isolation between the input and output frequencies is also crucial - but given that the leakage of the input signal is common-mode, the antenna does not support efficient re-radiation of the input signal. The output is connected to the orthogonal polarization ports on the same antenna.

4.5.4 300 GHz small signal amplifier

The small signal amplifier operating at 300 GHz is a typical cascode design. Care is taken to ensure that there are no propensity for low frequency oscillations. The design is driven by system constraints especially with respect to layout. The gain (S21) is plotted in Fig.

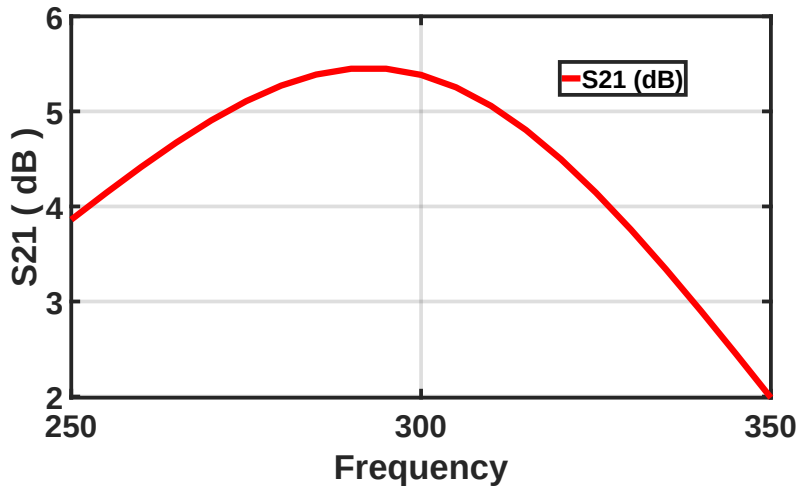


Figure 4.11: S21 (dB) of the 300 GHz amplifier vs frequency.

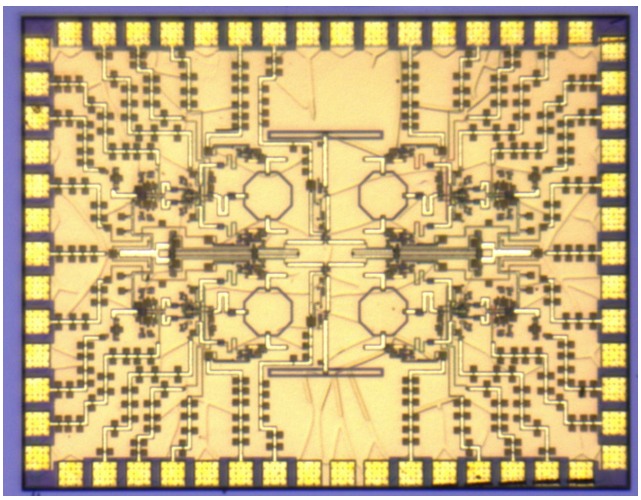


Figure 4.12: Die photo of the phase conjugating array chip.

4.6 Implementation and chip photograph

The chip was fabricated in the 250 nm InP HBT node from Teledyne Scientific. DC pads on the periphery are used to introduce bias as shown in Fig. 4.12. The annular slots are approximated by octagons owing to the design rule limitations in the kit. The overall chip occupies a compact area of 1.9 mm x 1.5 mm.

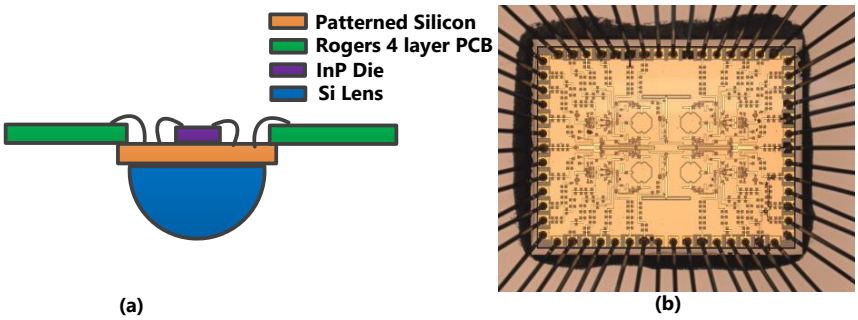


Figure 4.13: (a) Cartoon of the cross section of the packaging scheme used (b) Image of the wirebonded InP die.

4.7 Die packaging scheme

The die was epoxied to a high resistivity silicon substrate using non-conductive epoxy, and wirebonded to a Rogers 4 layer printed circuit board with a cavity cut out at the center. The PCB does affect the behavior of the patterns at various frequencies as expected and the design is simulated to reduce the impact of the various elements of the physical setup. The printed circuit board uses the second layer as the ground layer. All traces on the PCB carry DC bias - all RF input and output are quasi-optically coupled. The silicon substrate is patterned to carry DC bias from the chip to the PCB.

The cross section shown above is simplified and simulated in HFSS to ensure the patterns do not show significant deviation from what was intended. The cutout is patterned with metal, and the dimensions of the cavity are a crucial design choice. Bondwires are also added to the simulation to characterize their effect on the radiation. As expected, the results are no longer uniform as before, especially for the 150 GHz LO antenna. The gain of the 150 GHz antenna system (dB) is shown in Fig. 4.14 and Fig. 4.15. A variety of grating lobes are seen.

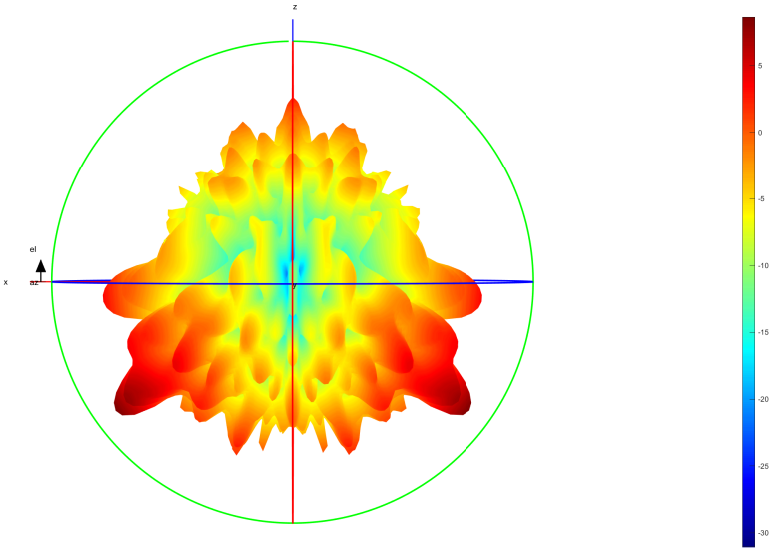


Figure 4.14: 3D radiation pattern (Gain in dB) of the simulated cross section at 150 GHz. The maxima in the broadside direction (+z) is evidently seen as are grating lobes from the introduction of the complex geometry.

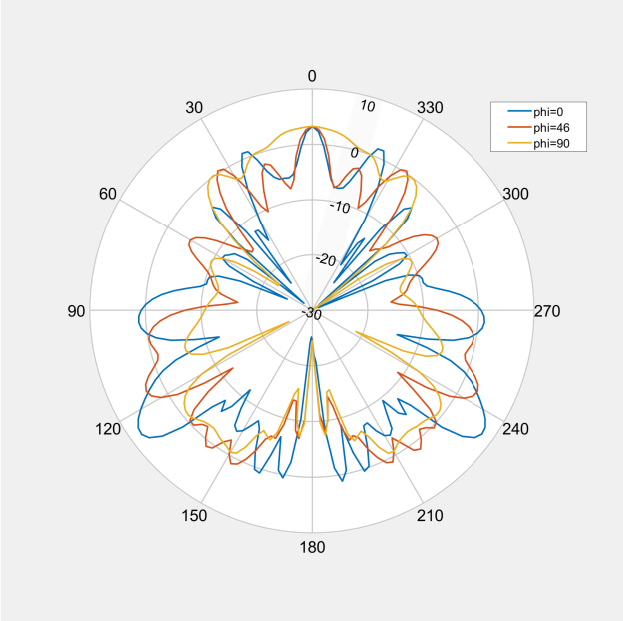


Figure 4.15: 2D radiation pattern (Gain in dB) of the simulated cross section at 150 GHz at various slices of Phi.

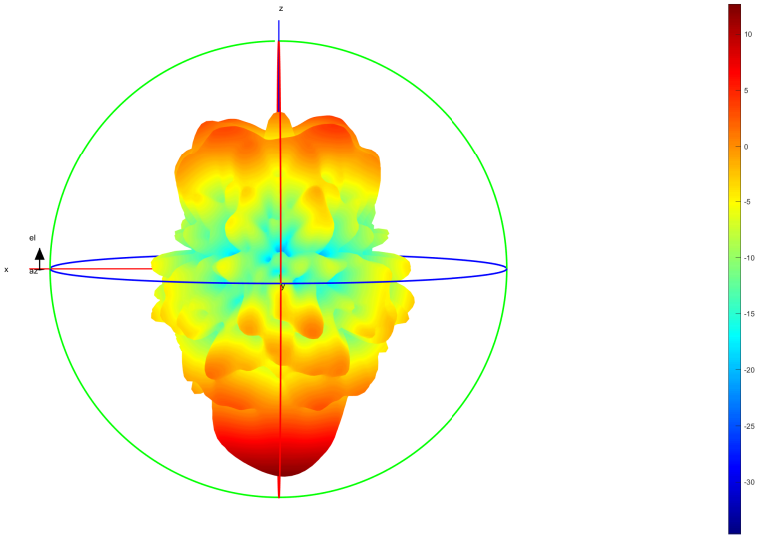


Figure 4.16: 3D radiation pattern (Gain in dB) of the simulated cross section at 300 GHz. The maxima in the broadside direction (-z) is evidently seen as are grating lobes from the introduction of the complex geometry.

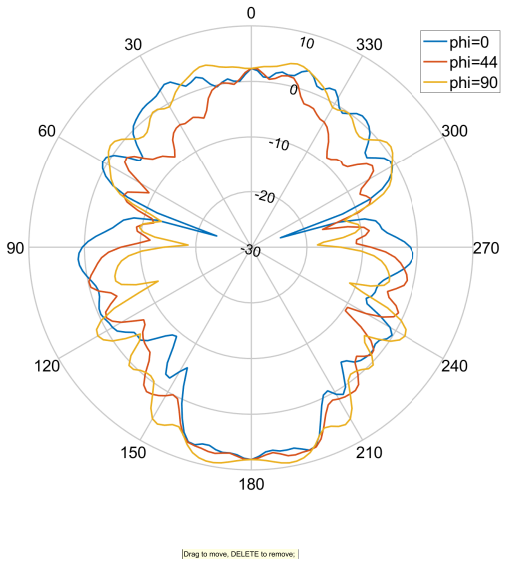


Figure 4.17: 2D radiation pattern (gain in dB) of the simulated cross section at 300 GHz at various slices of Phi.

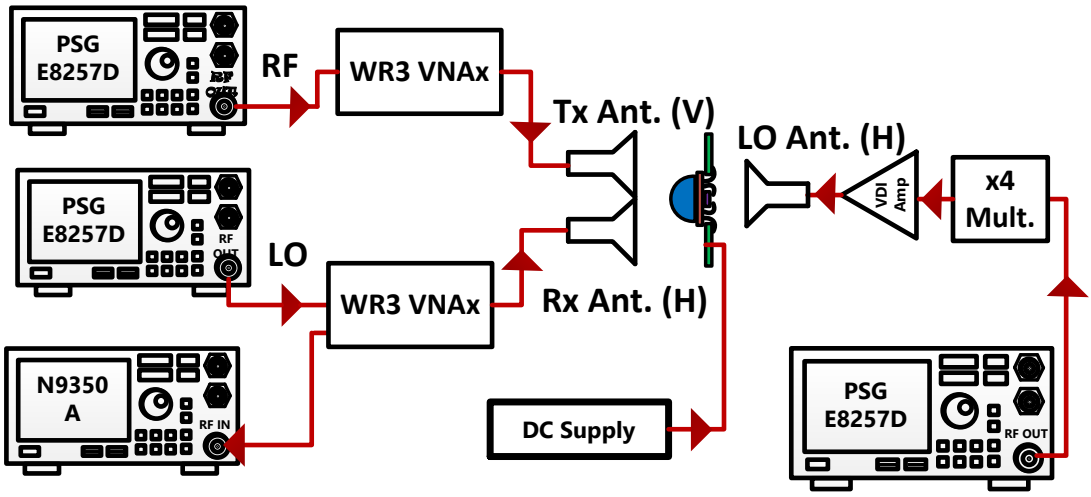
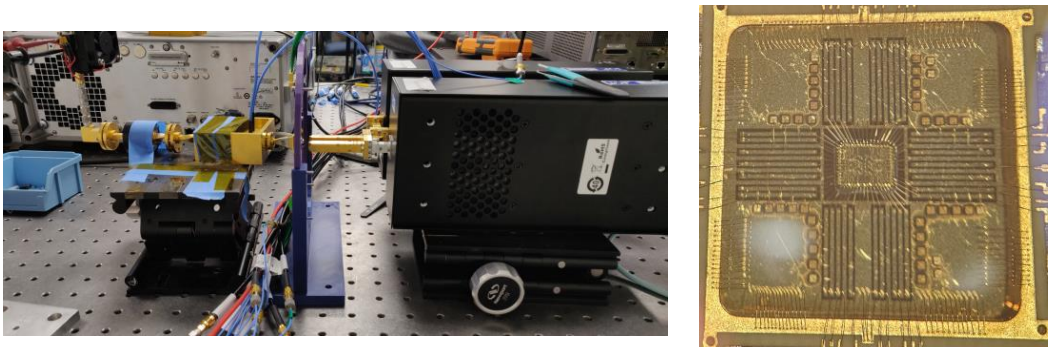


Figure 4.18: Measurement setup used to characterize the InP PC array.

4.8 Measurement apparatus and results

The chip as packaged is mounted on a plastic PCB holder that enables ready access to the actual DUT area while positioning all bias wires leading from the source meter away from the central area that dominates the radiation patterns. The architecture of the measurement setup is shown in Fig. 4.18, and a photograph is in Fig. 4.19. A multiplier built at UVA is used to excite the LO horn antenna. The design and characterization of the multiplier (quadrupler) are detailed in [118]. This quadrupler is followed by a VDI WR5 amplifier that then drives the WR5 horn antenna which is polarization matched to that of the LO antenna on the chip. in the WR3 band, a VNAx each is used to upconvert and downconvert the desired signals when driven by the Keysight Signal Generator. Again, each of these VNAx are followed by horn antennas with polarization matching that on the DUT. The Meas. port on the receiving WR3 VNAx is connected to a Keysight Spectrum Analyzer. The spectrum analyzer is used to look for the mixed down signal emanating from the DUT. Sourcemeters are used to supply DC bias to the chip.



(a) (b)

Figure 4.19: (a) Photograph of the measurement setup showing all antennas and measurement/excitation sources (b) Image of the die epoxied to the high resistivity silicon substrate and wirebonded to PCB bias lines.

4.8.1 SNR calculations

The VNAx used as the transmitter is characterized to have an output power of -5 dBm at its waveguide flange. Using Friis' path loss equation at 300 GHz at an estimated distance of 1 inch between the transmitting horn and on-chip receiving antenna, and with the gain of the on-chip receiving antenna set to 10 dB from simulations (Fig. 4.16), a received power of -20 dBm is estimated at the chip.

The conversion loss of the chain consisting of the mixer followed by the small signal amp is estimated to be 50 dB (Fig. 4.10 and Fig. 4.11). Therefore, the power transmitted from the chip is approximately -75 dBm.

Again, using Friis' path loss equation with the same parameters as before, the power received at the WR3 flange of the receiving VNAx is estimated to be -95 dBm. The VNAx mixer sensitivity is -135 dBm/Hz based on discussions with VDI. With a RBW of 1 Hz on the spectrum analyzer, we have an estimated SNR of **40 dB** for the measurement setup pictured in Fig. 4.18.

4.8.2 Observations

A variety of quasi-optical focusing techniques are used to illuminate the 150 GHz LO antenna on chip. The bias line on the PA and quadrupler are monitored to ob-

serve a response. The quesicent currents on both biases, and especially the quadrupler increases as the LO antenna on-chip is progressively illuminated with power proving that the concept of separating the two antennas using a FSS is feasible and demonstrable. The leakage of the Tx horn to the Rx horn antenna is also observed, as is the 8th harmonic of the quadrupler used to excite the LO (that falls in the WR3) band. However, the on-chip mixer response is not observed over a range of experiments that varied biases, frequencies and power levels. It is hence decided to characterize the quadrupler test structure that was also taped out as part of this project to be able to correlate the simulated behavior at 600 GHz versus what is actually measured.

4.9 Conclusions

The design analysis and characterization results (including the test structure in the next chapter) provide a framework to develop these ideas further and to implement them in a process and technology than can support the frequencies involved, perhaps where the maximum frequency of operation does not exceed $f_{max}/2$. The design also provides a foundation for a new class of ICs that are able to simultaneously efficiently radiate both from the top and the bottom of the chip, and this can be a useful tool in implementing use cases where the chip might need to be free standing and be able to interact with fields impinging from both hemispheres. The design analysis using coupled lines can also be extended further to demonstrate some critical circuit ideas.

Specifically, by extending on previous work that uses coupled transformers and demonstrating an improvement in the signal balance when using a coupled line at the output in simulation, this chapter provides an interesting design space exploration for future work. By intelligently using phases of the Tx and Rx antennas

and by creating virtual shorts, a degree of isolation between the input and output ports is enforced in systems that need to be used in STAR (simultaneous transmit and receive) form. By integrating the transistor electronics and various drive signals with the passive antennas on chip, this chapter further answers the question on integrating HBT electronics to build a phase conjugating system.

4.10 Personal Contributions

- Designed and laid out every circuit block.
- Designed and simulated all the antennas and accompanying physical structures.
- Designed the PCB and mounting structures.
- Designed the measurement setup and conducted experiments.
- Co-designed the silicon substrate interposer with Chris Moore.
- Assisted in the fabrication of said interposer in the UVA cleanroom.
- Leading effort to document observations and manuscript writing.

4.10.1 Acknowledgements

Chris Moore, Jay Sheth, Michael Cyberey, Matthew Bauwens, Robert M. Weikle, Steven M. Bowers, Travis Blalock, Jeffrey Hesler, Scott Barker.

Chapter 5

Design and characterization of a 250nm InP HBT frequency quadrupler using custom DC interposers

In order to understand the behavior of the individual circuits on the array described in the previous chapter, on-wafer test structures were characterized. The project had two on-chip test structures but only one could be characterized effectively - owing to an error in the layout that prevented the mixer from being completely biased up. This chapter also addresses a crucial issue that was encountered when these chips were attempted to be wirebonded to. The soft BCB dielectric and adhesion issues prevented a series of succesful wirebonds from being made which made characterization extremely difficult. To overcome this issue, it was decided to use a custom in-house beamlead frame that would act as a reliable means of supplying DC bias. One crucial difference between the wirebond and the DC interposer approach was in the reliability of contact with the InP die. Additionally, the beamleads are tacked down and are not pulled back by the bonder head like a traditional

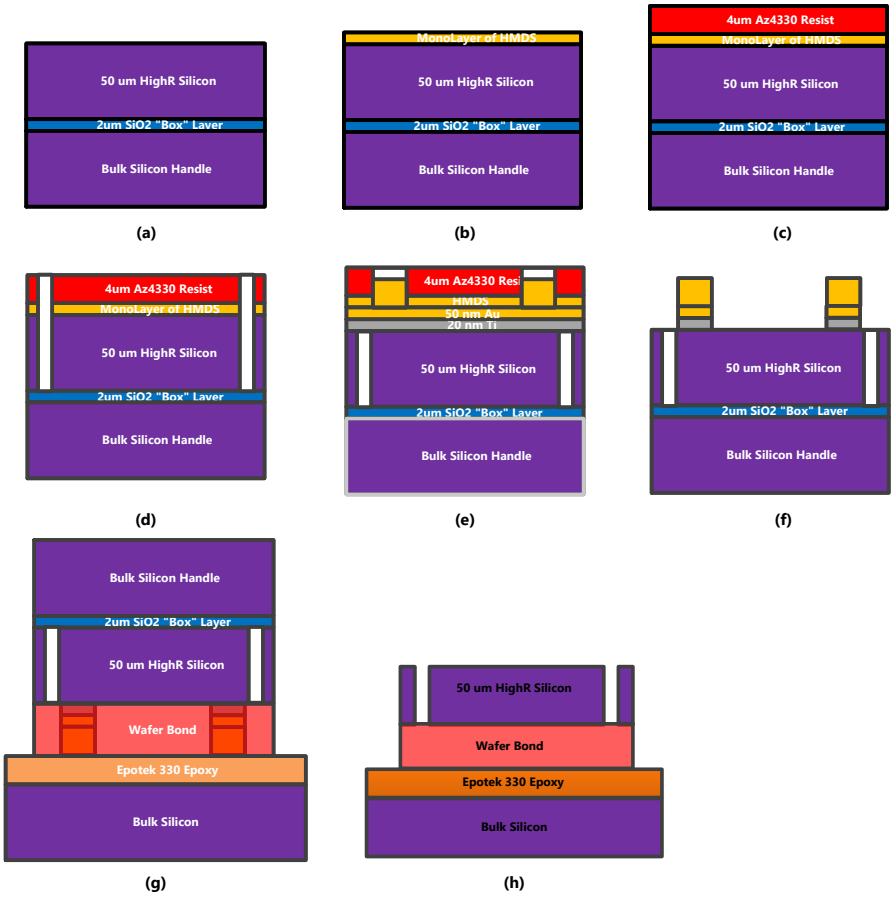


Figure 5.1: Pictorial depiction of the fabrication process outlined in Section 5.1.

wirebond would. This meant that the pads no longer peeled off. The remainder of this chapter is arranged as three primary sections - one expanding on the fabrication details of this interposer, one on the design of the quadrupler test structure, and one on characterization results.

5.1 Beamlead frame/Interposer design and fabrication

5.1.1 Wafer preparation and front side processing

The beamlead frame was designed in Keysight ADS to accomodate the pad pitch on the on-wafer test structures. This was then translated to a format that the machines used in the cleanroom could understand.The process begins with a pre-cut 50.8mm

diameter 635um thick wafer comprising three layers as shown in Fig. 5.1 (a).

1. A top device layer, >10k Ohm cm (high resistivity) 50 µm thick Silicon

2. A 2 µm thick Silicon Oxide ("Box") layer which separates the device layer from the

3. Bulk Silicon Handle (low resistivity).

The silicon is grown using the float zone method, and is optimal for producing low-defect silicon [Si] (low oxygen and carbon impurities). All solvent cleaning is done by placing the wafer on a spinner. The next step is to use a buffered oxide etch (BOE - 10% Hydrofluoric Acid and 90% Water H_2O) to remove any oxide from the surface of the wafer. The wafer is placed into a Teflon dish, and BOE is poured onto only the wafer, while ensuring that it is not entirely submerged - to be able to observe when the surface becomes hydrophobic.

The next step in the wafer processing is applying a monolayer of Hexamethyldisilane (HMDS) to promote photoresist adhesion as shown in Fig. 5.1 (b). The wafer is loaded into a vacuum oven preheated to 150°C on Aluminum surface, and a dry-scroll vacuum pump is used to pump to <10 millitorrs [mT]. The chamber is then purged by flowing N2 until the pressure is 300 mT. This pump-purge process is repeated three times. After the third iteration of the pump purge, the chamber is pumped until the pressure is <5 mT. HMDS is then bubbled into the chamber using an Erlenmeyer flask configured as a bubbler, and a needle gauge is used to increase the flow out of the bubbler until the partial pressure measurement is between 10-12 mT. The HMDS flows for approximately 10 minutes, and then the chamber is pumped and purged with N_2. The photoresist is then applied to the wafer by using a Spin Coater. AZ4330-RS is spun at 3000 RPM (revolutions per minute) to apply a 4 µm film of photoresist as shown in Fig. 5.1 (c). Edgebead is removed using a swab and reagent alcohol. The Resist is soft-baked at 110° C for 1 minute.

The ML3 Microwriter (projection lithography) is used to pattern the photoresist using a photomask taking into account fabrication tolerances using Autodesk's AutoCAD software. Features representing beam leads were added to perform tab bonding between a mounted chip and a printed circuit board. For this work, an aspect ratio of 5 to 1 was chosen for the beam lead; that is, the beam lead could hang off the side of the silicon five times longer than the width of the beam lead. Additional blocks were made, resembling the various microchips being tested for the assembly procedure and other parts.

The via layer is loaded onto the micro-writer software, and a 1 µm beam, using normal settings with a 10 mm focusing mesh, is used to pattern the photoresist. After patterning the photoresist AZ400K:H_2O 1:4 is used to develop the exposed Resist. A hardbake was performed in preparation for etching at 110° C for 60 seconds and 130° C for 3 minutes. After hardbake, the wafer is loaded into a vacuum chamber and an O_2 plasma to clear any residual resist in the developed features.This is done to ensure that no remaining resist could mask etching. A mechanical profiler is used to measure the step of the Resist, which corresponded to around 3.9 µm .

An Oxford plasma Inductively Coupled Plasma–Reactive Ion etcher (ICPRIE) machine was used to etch through the silicon to define alignment markers for the top side and backside processing. The wafer is loaded into the vacuum chamber and pumped to approximately 1E-6 torr. The next etch is the Bosch process, which balances deposition (or passivation) and etching to create an anisotropic etch optimal for vias. The Bosch process deposits by flowing Octafluorocyclobutane (C_4F_8), which leaves a fluorocarbon film on the surface and the walls where the etching is taking place. The Sulfur hexafluoride (SF_6) etches faster on the top and bottom surfaces "anisotropic-like" therefore, it clears the fluorocarbons on the top and bottom faster than it does the sidewalls, therefore allowing us to define holes through the wafer. After This was completed, the wafer was loaded into an O_2 plasma etcher for

30 minutes before stripping the Resist with Acetone and Isopropanol as shown in Fig. 5.1 (d).

5.1.2 Beamlead processing

The next step of the process is to define the topside metalization layer for the transmission lines and the beam leads. Resist from the previous processing steps was removed by using an O_2 Plasma. After the wafer is cleaned, the wafer is loaded into the electron beam physical vapor deposition EBPVD (evaporator) to deposit a seed layer of metal. The metal seed layer was masked with photoresist and electroplated to define the microchip's transmission lines and beam leads. Electroplating is performed using a Technigold solution. A magnetic stir bar was used at approximately 200 RPM, along with slight ultrasonic agitation. The plating voltage and current were 0.6 Volts and 0.68 mA, respectively. The plating bath was heated to 50° C. HMDS and Resist are applied to the surface to define plating features. The total thickness was checked every 30 minutes until we reached a thickness greater than 2.5 µm as shown in Fig. 5.1 (e). The next step is to remove the seed layer from the wafer. This is done by using HG800 gold etchant and BOE. The wafer is held with tweezers, wafted for 10-second increments, and then soaked in multiple DI water beakers until the gold layer is visually gone as shown in Fig. 5.1 (f). The wafer is then placed into a Teflon dish, and BOE is poured onto only the wafer.

A separate bulk silicon piece is prepared. Epotek 330 Epoxy is applied to the top of the surface and the two wafers are brought in contact with each other with a wafer press and cured at 100°C for >4 hours as shown in Fig. 5.1 (g). After bonding these two wafers together, the Bulk Silicon handle is removed through mechanical and plasma etching. The mechanical etching procedure involves using a Disco Dicing saw and making approximately 400 cuts- a kerf width from each other through 90% of the thickness of the wafer. The next step is to use a buffered oxide etch (BOE - 10% Hydrofluoric Acid and 90% Water H_2O) to remove the Silicon oxide from the

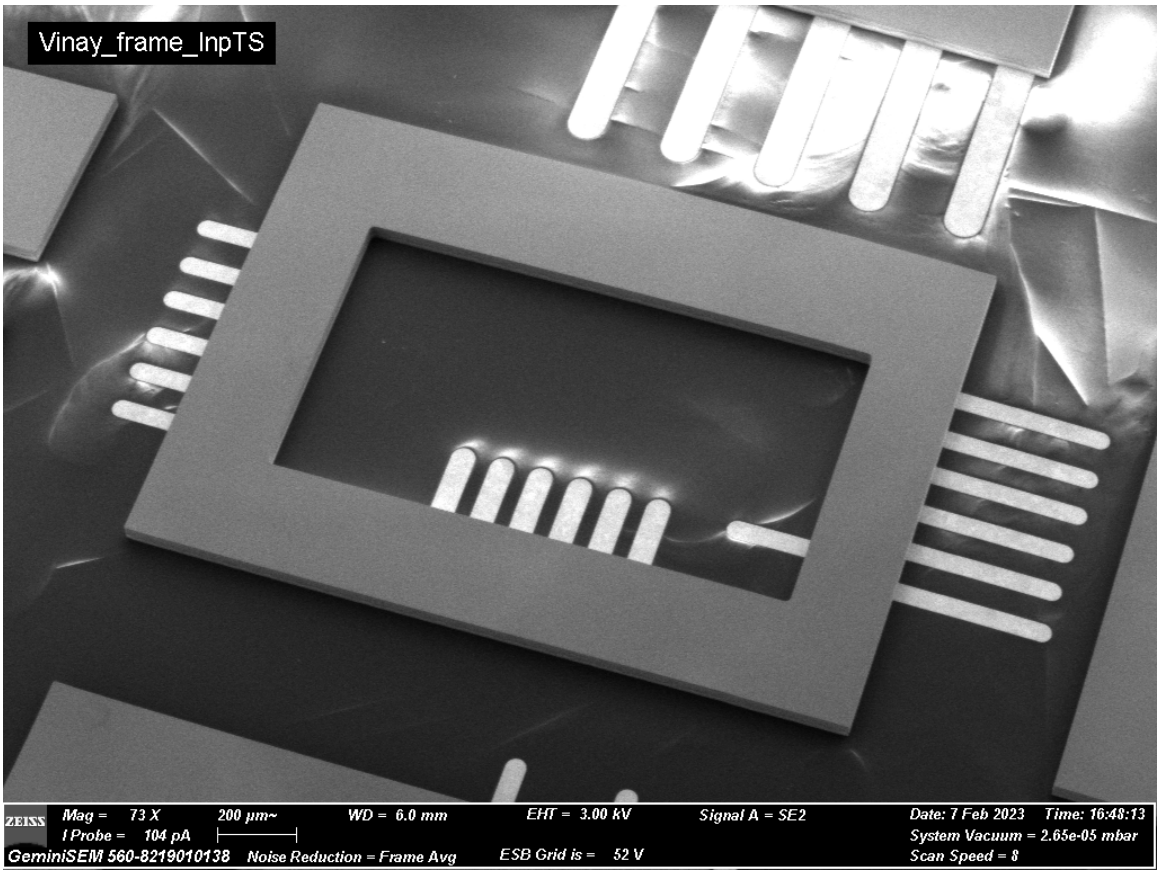


Figure 5.2: Beamlead frame fabricated in the UVA cleanroom using steps outlined in Section 5.1. This image shows beamleads on both the PCB and the InP die sides.

surface of the wafer as shown in Fig. 5.1 (h). The wafer is placed into a Teflon dish, and BOE is poured onto only the wafer, ensuring that it is not entirely submerged. Since this surface is thick, this takes around 30 minutes. After plasma cleaning the wafer is submerged into wafer bond remover. Heated to 100° C, the wafer is left in this solution for approximately 4 hours and Isopropyl and Trichloroethylene is sprayed on the surface of the wafer to release the chips onto filter-paper.

5.2 Quadrupler Test Structure Design

The test structure is designed to replicate the positioning of various nodes in the actual array as shown in Fig. 4.3. A dummy 50 Ω on chip termination is connected to a dummy pad on one side. On the other side, a CPW pad is used to probe the

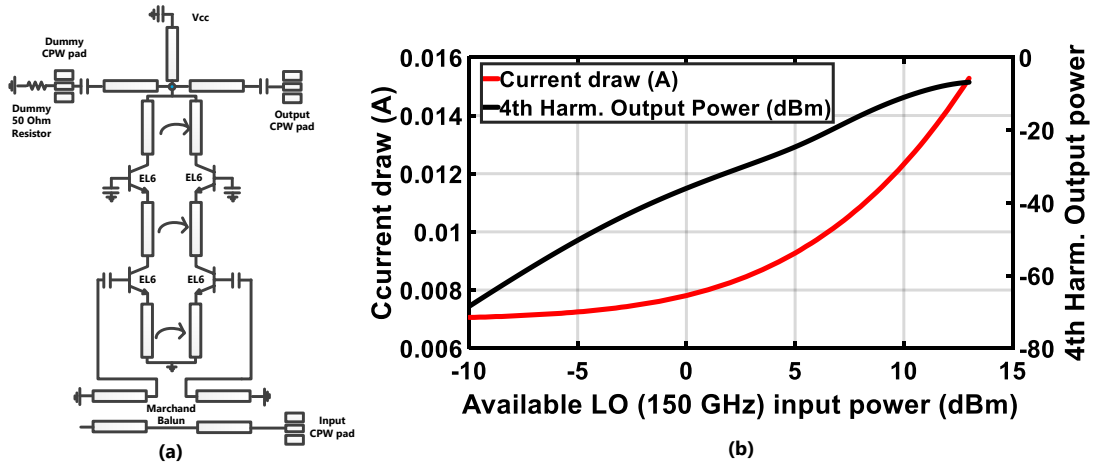


Figure 5.3: (a) Schematic of the quadrupler test structure showing the positions of the CPW pads and dummy resistor. Biasing details are not shown explicitly. (b) Simulated performance of the quadrupler test structure vs available LO power.

output. The design details are exactly as described in 4.5.1. Wide emitter length transistors are used to bias each side from the Vcc bias pad. The schematic is shown in Fig. 5.3 (a). Small and large signal simulations are shown in conjunction with measurements in section 5.3. Fig. 5.3 (b) plots the simulated current draw and 4th harmonic output power as a function of available power at 150 GHz. Fig. 5.4 depicts an image of the die layout. The pads and other structures mentioned above are clearly visible. A dummy load replicates the division of power into two legs as it would be in the actual array. The dummy load consists of a 50 Ω resistor on-chip termination preceded by a 25 µm pitch CPW pad. On the output side, an identical pad is used to probe the output. At the design stage, idlers are used to desensitize the output node at the second harmonic at both sides and this combined with the on chip dummy pad was thought to suffice to enable the maintenance of symmetry at all frequencies. However it was later realized that the probe presents a different impedance out of band and this does create additional asymmetry. However, the probe is simulated out of band and these results are shown in 5.3.

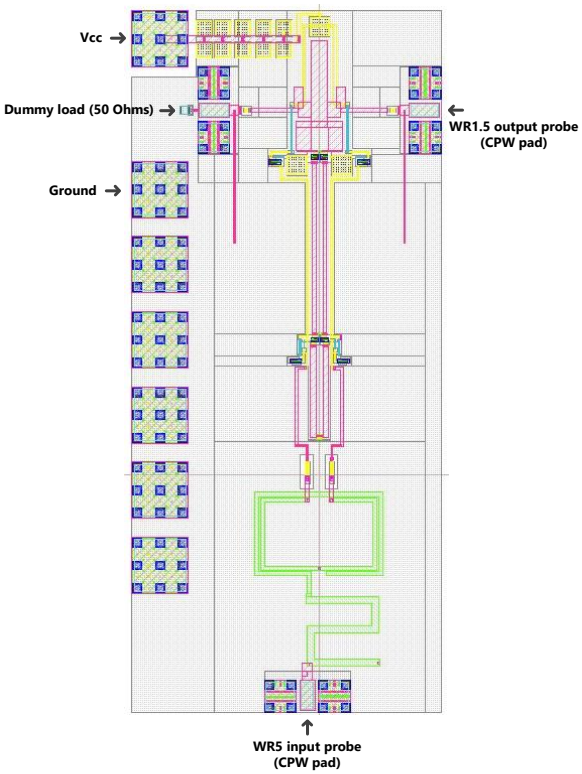


Figure 5.4: Layout of the fabricated quadrupler test structure. The DC and RF CPW pads are indicated.

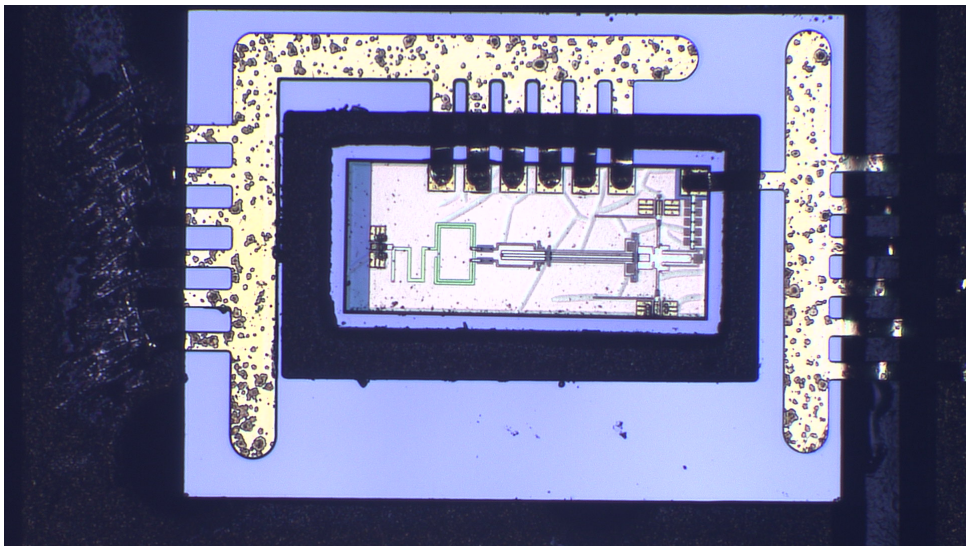


Figure 5.5: Die picture of the fabricated quadrupler test structure in conjunction with the DC interposer. The DC interposer beamleads and traces are colored bright yello. The cavity accomodating the die is seen as a black outline.

5.3 Packaging and measurements

The die is first epoxied to a PCB. The beamlead frame from Fig. 5.2 is next epoxied to the PCB with the cavity fitting the die. After the epoxy has cured, a wirebonder head (without the wire) is used to gently tack down the beamleads on both the PCB and die side. This is then tested for DC bias to ensure a functional chip and package. Please note that all probe pitches are 25 µm on this test structure.

5.3.1 S-parameter measurements

An input S parameter measurement is performed in the WR5 band. A DMPI WR5.1 probe is landed on the input CPW pad. A WR1.5 probe with a section of WR1.5 through and a WR1.2 to 10 transition is attached to a PM5 Erickson Calorimeter and landed on the output side to act as a load. The input chain leading to the WR5.1 probe tip is calibrated using a custom DMPI calibration substrate. It is noteworthy that the pads on-wafer are not calibrated and are part of the network measured. The chip is biased at 4.9 V for a quiescent of 6.1 mA. Fig. 5.6 plots the simulated and measured S parameters at the input of the quadrupler test structure with the output terminated. The results agree exceedingly well indicating that both the transistor and passive structure have been well modeled at these frequencies, atleast on the input side.

Next, a S parameters measurement is performed at the output, with the input terminated. On the input, a WR5 VNAx connected to a WR5 probe is landed to ensure a good 50 Ohm termination in band. At the output, the WR1.5 VNA extender with the test port attached is first calibrated upto the flange. Next, the probe is attached and an on-wafer 1 port calibration is performed utilising a DMPI calibration substrate that incorporates five delay short elements. The chip is biased at 4.9 V for a quiescent of 6.1 mA. The setup now calibrated to the probe tips is used to test the S parameters at the output of the HBT quadrupler from 500 to 675 GHz. A section

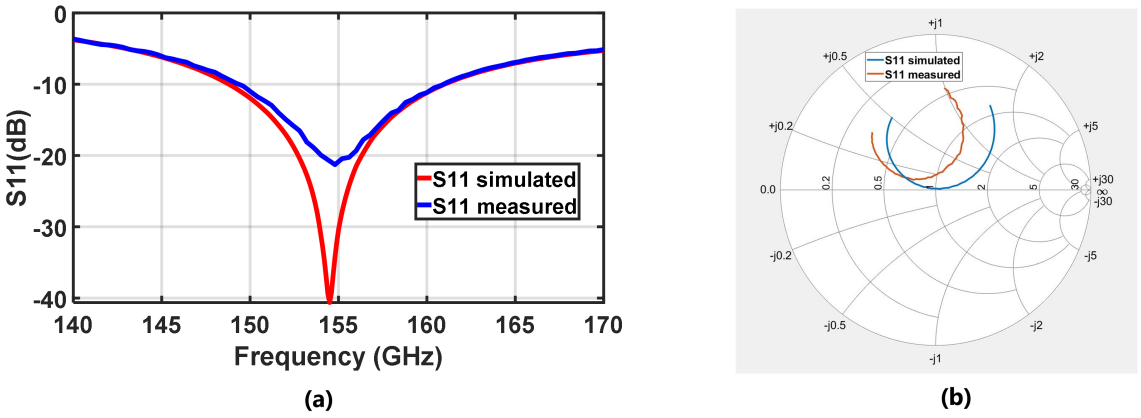


Figure 5.6: One port S parameter results for the quadrupler, with the output terminated.

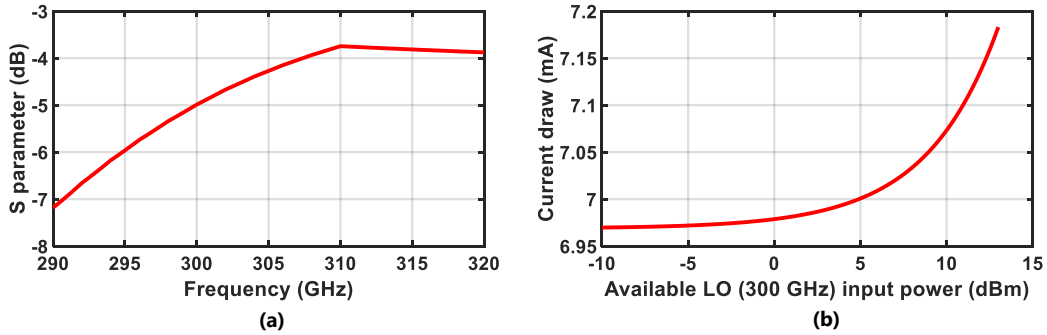


Figure 5.7: (a) Simulated one port S parameter at the input for the quadrupler, with the output terminated. (b) Current draw from supply when excited significantly by a WR3 input power source.

of the measurements in the band of interest is plotted in Fig. 5.8. The simulated and measured results do not match well and this is thought to be from the poor modeling of the transistors at these frequencies along with a combination of metal and dielectric losses and any excited substrate modes.

The setup calibrated at the test flange, is also used to measure the mismatch loss of the WR1.2 to WR10 taper connected to the PM5, that is used in the large signal measurement elaborated on next.

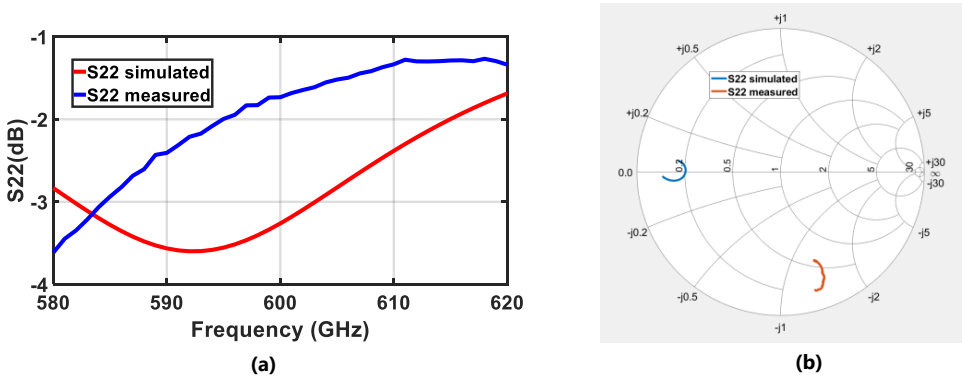


Figure 5.8: One port S parameter results for the quadrupler, with the input terminated from 580 to 620 GHz

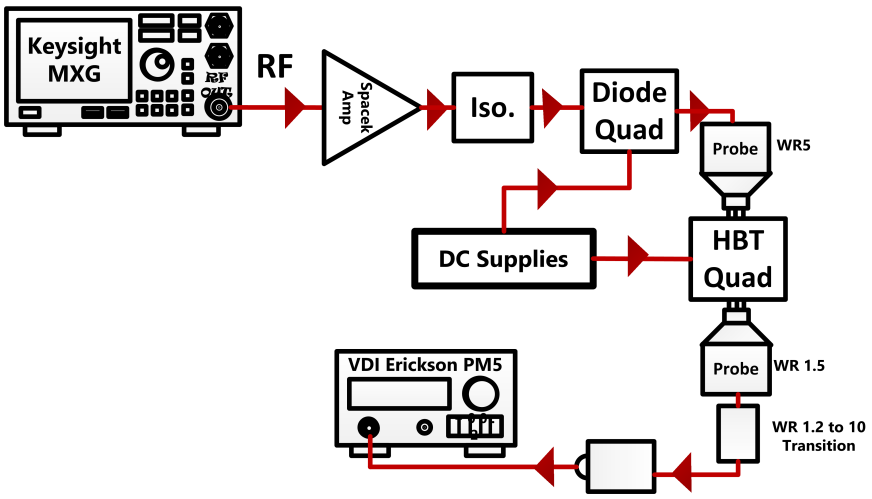


Figure 5.9: Large signal measurement setup. The Spacek amp drives an isolator followed by the diode quadrupler.

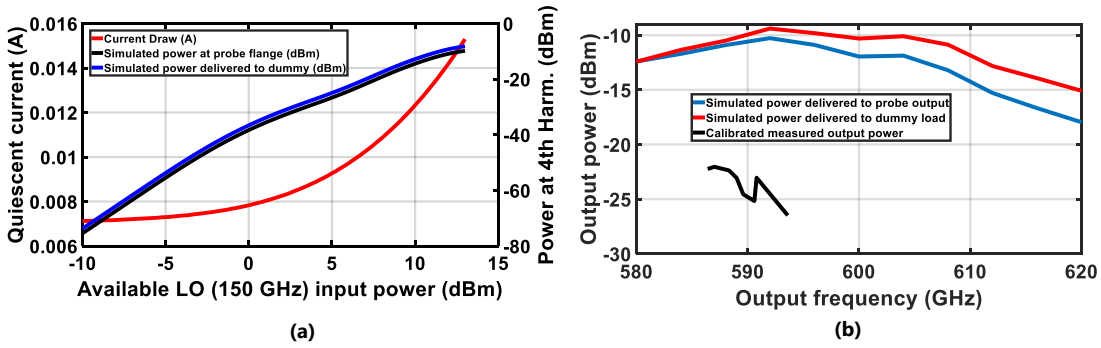


Figure 5.10: Saturated output power at peak current draw - Simulations vs measurements. The lower end is limited by the performance of the driving source. The black and blue traces in (b) are relevant for comparison.

5.3.2 Large signal measurements

The test structure is then tested for large signal performance. At the input, a Spacek amplifier drives the quadrupler detailed in [118] with an isolator in between. The output of the quadrupler (with the dump port terminated in a load) is connected to a WR5.1 probe (with a twist). The setup is pictorially depicted in Fig. /ref (a). The eighth harmonic of the quadrupler in the vicinity of the WR3 band is expected to be lower than 15 dBc and hence most of the power going into the HBT quadrupler is expected to be in the WR5 band. It is difficult to measure the eighth harmonic from the diode quadrupler directly by attaching the output flange to a mixer since this alters the behavior of the quadrupler significantly. The simulation of the test structure gives us a degree of confidence about the signal going into the probe on the input pad. Fig. 5.7 (a) and (b) plot the simulated S parameters at the input (with output terminated) and the current draw when excited by a WR3 input. As can be seen, with a return loss of 5 dB, 32% of the power is expected to be reflected. The current draw is also not as significant and this is because of a highly tuned design at 150 GHz.

At the output, a WR1.5 probe is connected to a Wr1.2 to WR10 taper. The WR10 taper is connected to a VDI PM5 power meter. The WR1.2 probe cuts on at a higher frequency compared to the WR1.5 waveguide (492 GHz vs 393 GHz), and this is done to ensure that the power read at the PM5 is at the 4th harmonic (> 493 GHz). The HBT quadrupler is excited by the input chain and readings are taken on the power meter at a range of frequencies when the current draw on the HBT quadrupler exceeds 14 mA. This is expected to be the safe range from simulations using the model kit provided by the foundry. Between each frequency point, the PM5 is zeroed to ensure maximal accuracy in the readings. The lower end of the frequency range in measurements is constrained by the lower cutoff in the exciting diode quadrupler [118]. Next, the measured S parameters of the probe are used to

account for the insertion loss of the probe in band. This is nominally 3.5 dB in the band of operation. The mismatch loss taken from the measurement of the S parameters of the WR1.2 to WR10 taper is added to the loss of the PM5 upto the flange, and the insertion loss of the taper. This is then added to the loss of the probe and the raw measured output power. This cumulative number is the actual measured output power in the WR1.2 band.

As is expected, the behavior of the WR1.5 probe out of band does violate the symmetry assumptions inherent in the design and the usage of a dummy load on chip. In order to account for this, the simulated S parameters of the WR1.5 probe in all the frequencies of interest (150 GHz and all harmonics) is used in the simulation to account for the effects of the termination out of band. As expected, there is a delta in the power delivered between the dummy on chip-load and the other leg that drives the actual measured output on chip. Fig. 5.10 plots the simulated and measured results across frequencies and power levels. Fig. 5.10 (a) plots the simulated output power across power levels at 150 GHz. The delta between the two output powers is about 1.6 dB at 150 GHz input, with the output power supplied to the on-chip load being higher. Fig. 5.10 (b) plots the simulated output power across frequencies. Again, the output power supplied to the on-chip load is higher across the band.

Fig. 5.10 (b) also plots the calibrated measured output power referenced in the paragraph above. As can be seen there is a large delta in the simulated and measured power. This is attributed to a combination of dielectric and metal losses, and significant difference between modeling and behavior of the transistors at these frequencies, although it is harder to conclude which of these factors contribute significantly or in what proportion. All simulations include realistic estimates for dielectric loss tangent and metallic conductivity, at the lower frequencies and to the best of the author's knowledge, a reasonable loss model for the higher frequencies. [119] details an oscillator built using this same technology at comparable frequencies. The

authors report a 8 dB delta between simulated and measured output powers. Their design uses no series capacitors and does not have an on chip load resistor and is hence significantly different from our design. Moreover, it is unclear if the authors used their own models or the foundry provided models for the transistors.

5.4 Conclusions

The results from this chapter provide a significant insight into the behavior of the array in simulations versus measurements. If the actual output of the quadrupler is lower by 15 dB, the conversion loss of the mixer is almost lower than simulated by that amount if not more. The SNR of the setup that was measured to be roughly 40 dB in 4.8.1 suddenly falls down to 5 dB or even lesser. This would help explain the fact that no signal is seen at the WR3 receiving antenna in the measurement to observe the mixed signal. This chapter answers the research question that pertains to interfacing with electronics that suffer from low pad adhesion by implementing an interposer that while being used here only at DC, is capable of being used at RF frequencies as well.

5.5 Personal Contributions

- Design and layout of the HBT quadrupler test structure.
- Designed the beamlead interposer in ADS.
- Assisted in the fabrication of said interposer.
- Designed the measurement setup.
- Leading effort to document observations and manuscript writing.

5.5.1 Acknowledgements

Chris Moore, Matthew Bauwens, Michael Cyberey, Robert M. Weikle, Steven M. Bowers, Travis Blalock, Jeffrey Hesler, Scott Barker.

Chapter 6

Design and characterization of a phase conjugator using subharmonic diode mixers

As detailed in the background, traditional phase conjugating architectures typically use a LO at twice the radio frequency (RF). Architectures based on this approach, however, are problematic at millimeter and sub-millimeterwave bands where high-power local oscillators are costly and scarce. In this chapter, a new phase conjugator architecture based on 4th-order subharmonically pumped mixers that use an LO with frequency at approximately half the RF is described. Analysis and design of the phase conjugator are discussed and a prototype version operating at 1.7 GHz is demonstrated. This chapter also details a technique to quantitatively measure the degree of phase conjugate signal versus all the other signal sources at the RF frequency that leak out at the IF port. Qualitatively, this provides the benefit of not having to rely on an arbitrarily small separation in frequencies to prove the existence of a phase conjugate signal. In a larger terahertz systems consisting of various ICs and packages, it may become prohibitively computationally expensive to simulate the pattern at a number of frequencies. Using a conventional RF technique

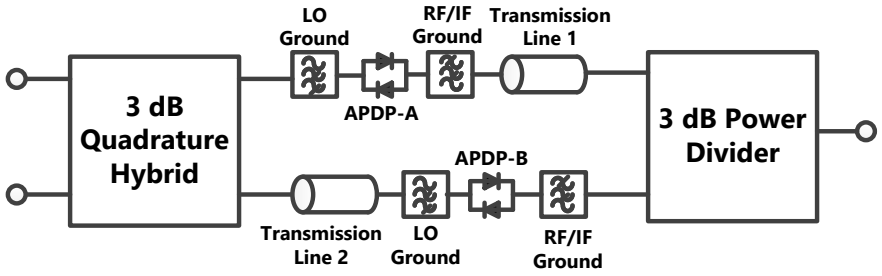


Figure 6.1: Circuit architecture of the phase conjugator based on 4th order subharmonically pumped mixers. The transmission lines 1 and 2 are 90 degree at the RF frequency

(S parameters) to quantify this behavior thus has interesting implications. This circuit also lends itself to this interferometry based characterization by virtue of its intrinsically separate input and output ports.

6.1 Circuit Analysis and Design

Fig. 6.1 shows the basic circuit topology of the phase conjugator. Two anti-parallel diode pairs (labeled APDP-A and APDPB) are employed for subharmonic mixing. The LO signal ($\omega_P \approx \omega_{RF}/2$) is divided and applied to drive the APDP's with equal amplitudes and 45° phase offset corresponding to the electrical length of transmission line 1 at the LO frequency). The RF signal is fed to the APDP's using a 3-dB quadrature hybrid with a 90° delay line (transmission line 2) connecting the hybrid's quadrature port to APDP-2. This effectively provides two equal-amplitude RF signals to the APDP's with a 180° phase-offset.

It is well-established that the sideband currents present at the terminals of the anti-parallel diode pairs can be expressed in terms of the small-signal sideband voltages, Vn, and a conversion admittance matrix [120, 121]. The elements of the conversion admittance matrix, $Y_{m,n}$, are functions of the Fourier components of the conductance (G_k) and capacitance (C_k) waveforms of the pumped diodes,

$$Y_{\mathrm{m,n}} = G_{\mathrm{m\text{-}n}} + j(\omega_0 + m\omega_{\mathrm{p}})C_{\mathrm{m\text{-}n}} \tag{6.1}$$

where ω_0 and ω_{p} are the IF and LO frequencies respectively. The LO phase offset applied to APDP-A through delay line 1 results in a linear (with frequency) phase shift of each Fourier component of the diode pair's conductance and capacitance waveforms [56]. Thus, the sideband currents flowing through APDP-A and APDP-B can be expressed as,

$$I_{\mathrm{m}}^{\mathrm{A}} = \sum_{n=-\infty}^{\infty} Y_{\mathrm{m,n}} exp\frac{(-j(m-n)\pi)}{4})V_{\mathrm{n}} \tag{6.2}$$

and

$$I_{\mathrm{m}}^{\mathrm{B}} = \sum_{n=-\infty}^{\infty} Y_{\mathrm{m,n}} V_{\mathrm{n}} \tag{6.3}$$

In expressions 6.2 and 6.3, superscripts A and B refer to the APDP's, m is the current sideband index, n is the voltage sideband index, and $\mathrm{Y_{m,n}}$ is the $\mathrm{mn^{th}}$ element of the conversion admittance matrix. Consistent with the literature, the radial frequency corresponding to sideband n is defined as $\omega_0 + n\omega_{\mathrm{p}}$. Thus, a sideband index of m = 0 corresponds to the IF current. The negative sign in equation 6.3 arises from the 180– phase difference between the RF signals at the output of the hybrid. Examination of equations 6.2 and 6.3 readily shows that the IF currents at the terminals of the anti-parallel diode pairs that are associated with the input RF signal (at sideband n = -4, corresponding to $\omega_{\mathrm{RF}} \approx 2\omega_{\mathrm{p}}$) are in phase. As a result, the IF signals (which are at approximately the same frequency as the RF input signal) cancel at the RF input (port 1) of the quadrature hybrid and sum at the IF output (port 4). Conversely, the RF currents (with sideband indices of m = -4) are 180° out of phase, resulting in cancellation at the IF output (port 4). In addition, because the RF input is applied and the IF output is taken at mutually-isolated ports of the hybrid, coupling between the input RF and its phase-conjugate replica at the IF output is minimized. Isolation between these signals is examined further through measure-

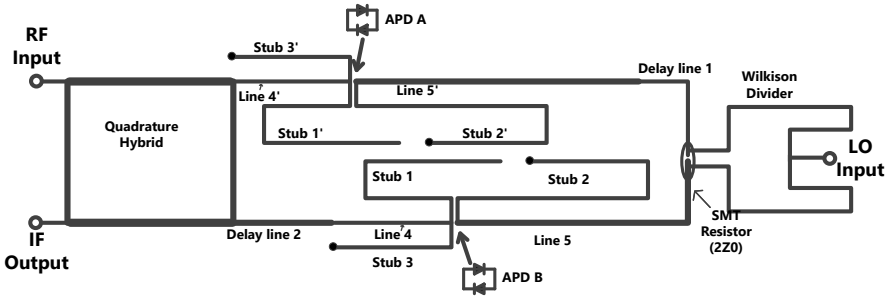


Figure 6.2: Microstrip layout of the 4th order subharmonic phase conjugator.

Parameter	Value
Total Capacitance at 0V, 1 MHz	45 fF
Series Resistance	4 Ohms
SSB NF	6.5 dB

Table 6.1: Parameters of the Anti-Parallel Diode pair from Macom

ments on a prototype phase-conjugator based on the architecture of fig. 6.1.

6.2 Implementation

A prototype phase conjugator based on the architecture of fig. 6.1 has been implemented as a microstrip circuit fabricated on a FR4 4 layer substrate (with dielectric constant of 3.61, substrate thickness of approximately 55 mils and top conductor thickness of approximately 1.7 mils). The transmission lines and circuit components are designed with the ground being on the second metal layer for optimal RF performance. The circuit is designed to operate at an RF of 3.47 GHz, an LO frequency of 1.76 GHz and an IF of 3.53 GHz. The circuit layout is shown in Fig. 6.2 and consists of a branchline coupler as the 3-dB quadrature hybrid and a meandered Wilkinson coupler as the LO power divider. Two pairs of beamlead GaAs Schottky anti parallel diode pairs (Model MA4E1318 from Macom) are soldered onto the circuit. Electrical parameters (obtained from the datasheet) for these devices are provided in Table I6.1.

In addition to the two delay lines required for proper phasing of the RF and

LO signals, several microstrip lines and stubs are included as idlers and impedance matching networks. Referring to fig. 2, microstrip stubs 1 and 1' (with electrical lengths of 90°at the LO frequency) are open-circuited and serve as ground to the LO signal. Similarly, stubs 2 and 2' (with electrical lengths of 180°at the RF) are short-circuited through via holes and act as RF/IF grounds.

Stubs 3 and 3' (with electrical lengths of 90°at the RF) are also shortcircuited and these are used as idlers for mixing products at the frequencies $\omega_{RF} + 2\omega_p = 6.99$ GHz, $-(\omega_{RF} - 2\omega_p) = 50$ MHz, and $\omega_{RF} + 6\omega_p = 14.03$ GHz. Because the RF and IF are approximately the same frequency, the RF input and IF output are matched using the same impedance transformer design (microstrip lines 4 and 4'), with line width of 50 mil and length of 450 mil. The microstrip transformers labeled 5 and 5' are chosen to optimize the LO impedance for conversion loss and are designed using the harmonic balance simulator of Agilent's Advanced Design System software. The width and length of these LO transformers are 50 mil and 170 mil, respectively. A meandered Wilkinson power divider is used to feed equal amplitude and equal-phase LO's to the diode pairs. Final design of the meandered power divider made use of Agilent's electromagnetic solver Momentum to account for physical discontinuities such as the hairpin turns used in the structure. Fig. 6.3 plots the simulated S parameters of the tapered Wilkinson divider with 1 being the input port and 2 and 3 being the 3-dB split ports. As expected, the divider performs exceedingly well in the vicinity of the LO frequency.

6.3 Measurements

The RF/IF matching and isolation of the phase conjugator were measured using an Keysight PNA vector network analyzer. During this measurement, a 1.693 GHz source with available power of 10.1 dBm was applied to the LO port of the circuit. The measured S-parameters are shown in Fig. 6.5 where S11, S22, and S21 repre-

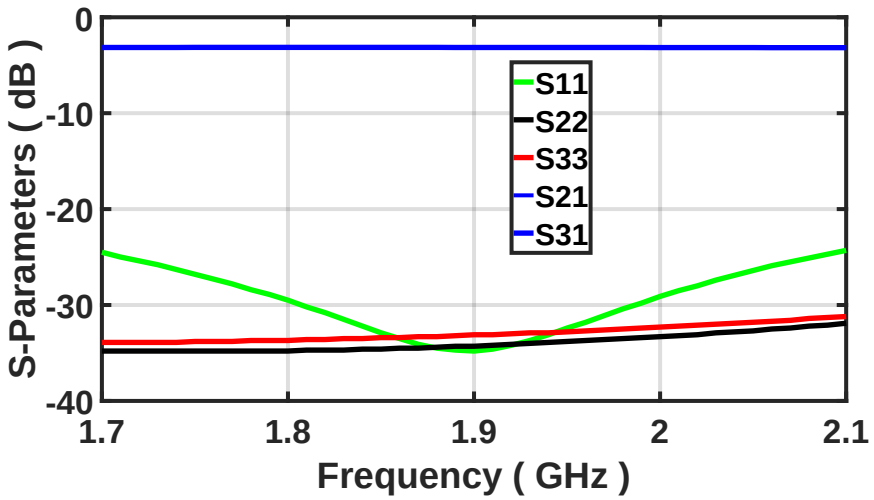


Figure 6.3: Simulated S parameters of the Wilkinson Divider with 1 being the input port and 2 and 3 being the 3-dB split ports. The EM simulation was performed in the Keysight ADS Momentum simulator.

sent the RF input matching, IF output matching and RF-to-IF isolation, respectively. The input and return loss do not match simulations well, and this is thought to be from a combination from a highly dispersive lossy FR4 substrate and poor modeling of the diode parameters. Measurements of RF-to-IF conversion loss and 2 LO-to IF isolation were done using swept-frequency sources applied to the LO and RF ports with a spectrum analyzer at the IF port. The LO, RF, and IF are fixed at 1.693, 3.416 and 3.386 GHz, respectively, with available LO power of 10.1 dBm. The 2 LO-to-IF isolation (ratio of the available LO power to the LO second-harmonic power at the IF port) was measured because the 2nd harmonic of the LO is at approximately the same frequency as the IF signal, thus presenting a potential interference at the output. The measured RF-to-IF conversion loss is 21.4 dB and the 2 LO-to-IF isolation is better than 50 dB. The leakage from the RF to IF port when pumped at the LO port, is 26 dB. The phase conjugate signal is thus stronger than the leakage. Table 6.2 summarizes the simulated and measured performance of the prototype phase conjugator at the given design frequencies. A design on a high frequency Rogers Substrate with a better characterization of the diode parasitic is expected to yield a better conversion loss, and have improved matching.

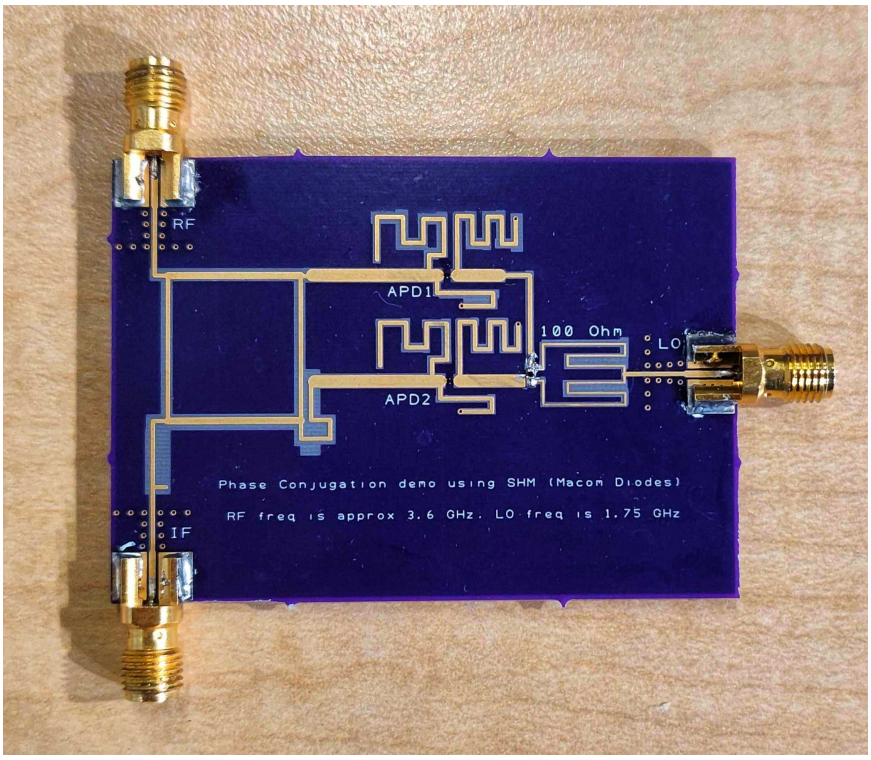


Figure 6.4: Photograph of the phase conjugate mixer. The APDs are labeled. The LO port is at the right, and the RF and IF ports are on the top and bottom of the image

Parameter	Simulation	Measurement
Conversion Loss(dB)	26	21.4
RF to IF isolation (dB)	29	26.5
2 LO to IF isolation (dB)	Inf	60
Avail. LO power (dBm)	13.5	10.1

Table 6.2: Comparison of the measured and simulated performance of the phase conjugator.

It is worth examining the possibility of quantifying the quality of the phase conjugate signal using conventional RF characterization methodology as opposed to using a retrodirective method that differentiates with respect to frequency. A S parameter measurement is most suited to this purpose given the measurement of phase and amplitude at each sweep point. It is critical to understand the concept of phase here - this is the relative phase between the RF and LO paths going into the mixer. Consider the scheme in Fig. 6.6. All measurements are performed at CW unlike a conventional frequency sweep. The signal from Port 1 is divided using a

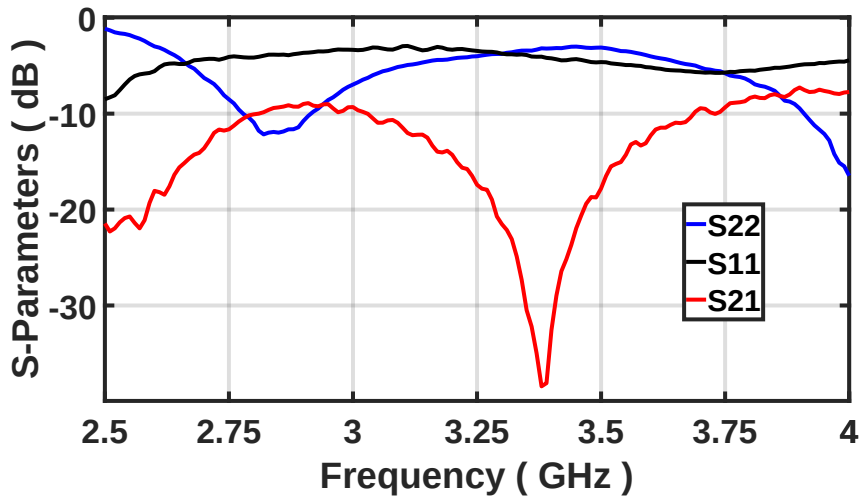


Figure 6.5: Measured S parameters of the Phase Conjugator. RF input is at port 1, and IF output is at port 2.

3 dB power splitter and one of the ports is connected to a circulator followed by a Pasternack Divider, a bandpass filter and an amplifier in that sequence. This signal supplies the LO to the DUT mixer examined above. The bandpass filter is needed to condition the signal such that the second harmonic of the LO (at the RF frequency) is not significantly strong. This is needed since the DUT mixer performs poorly if the LO signal has significant second harmonic content (close to the RF frequency). This is also borne out by the fact that the mixer is inherently subharmonic in design. Next, the signal from the other port of the 3 dB splitter is supplied to an attenuator followed by a phase shifter. The phase shifter is a delay line that operates over the band of the RF signal. This signal is connected to the RF port of the DUT mixer. The IF port is connected to Port 2 of the VNA.

The reference planes for the two port S parameter calibration are shown in the scheme as well. The phase shifter enables introducing a phase shift in the RF path relative to the LO path. It is noteworthy that there is purely one frequency that is being stimulated and interrogated here and all the various terms fold on this single frequency. Consider the various complex wave amplitudes as detailed in Fig. 6.6.

$$b_2 = a_1 e^{(j\phi)} \tag{6.4}$$

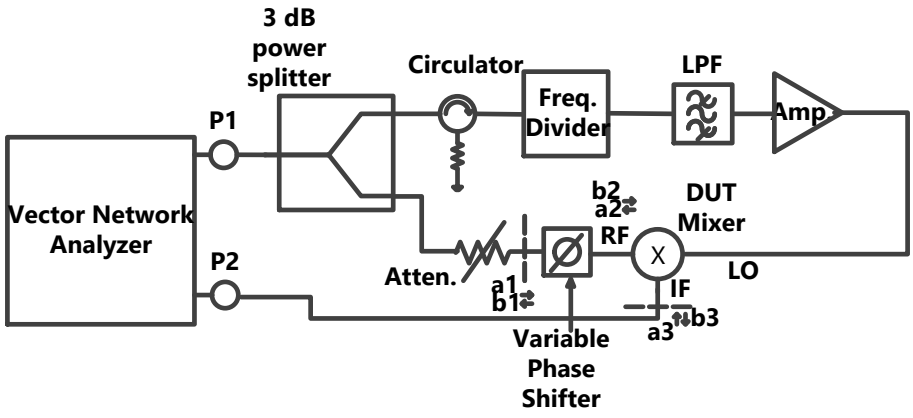


Figure 6.6: Metrology scheme for demonstrating phase conjugation using the DUT mixer and a COTS frequency divider.

$$b_3 = \alpha b_2 + \beta \bar{b}_2 + \gamma = \epsilon a_1 e^{(j\phi)} + \delta \bar{a}_1 e^{(-j\phi)} + \gamma \tag{6.5}$$

where ϵ, δ and γ are complex constants that represent the leakage of the RF, the phase conjugate signal and the leakage of the LO signal - all at the IF port.

$$S_{21} = b_3/a_1 = \epsilon e^{(j\phi)} + \nu e^{(-j\phi)} + \mu \tag{6.6}$$

where ν and μ are complex constants that indicate the quantities of the phase conjugate signal and LO leakage normalized to the input wave. This contour sketches out an ellipse in the ϕ plane. The eccentricty and the focii are dictated by the various terms in equation 6.6. The behavior of equation 6.6 is plotted for various values of the phase conjugate signal and LO leakage in Fig. 6.7. As expected, the LO leakage drives the offset from the origin of the contour, and the strength of the phase conjugate signal versus the RF leakage drives what direction the contour is traced out in. For equal parts RF leakage and phase conjugate signal, the contour is a line as expected. It is instructive to consider the behavior of the DUT mixer under these measurement conditions. In order to characterize the behavior of the phase shifter, a two port S parameter measurement is performed as the phase setting is altered. As is evident, the phase shifter has uniform insertion loss over all of the phase range

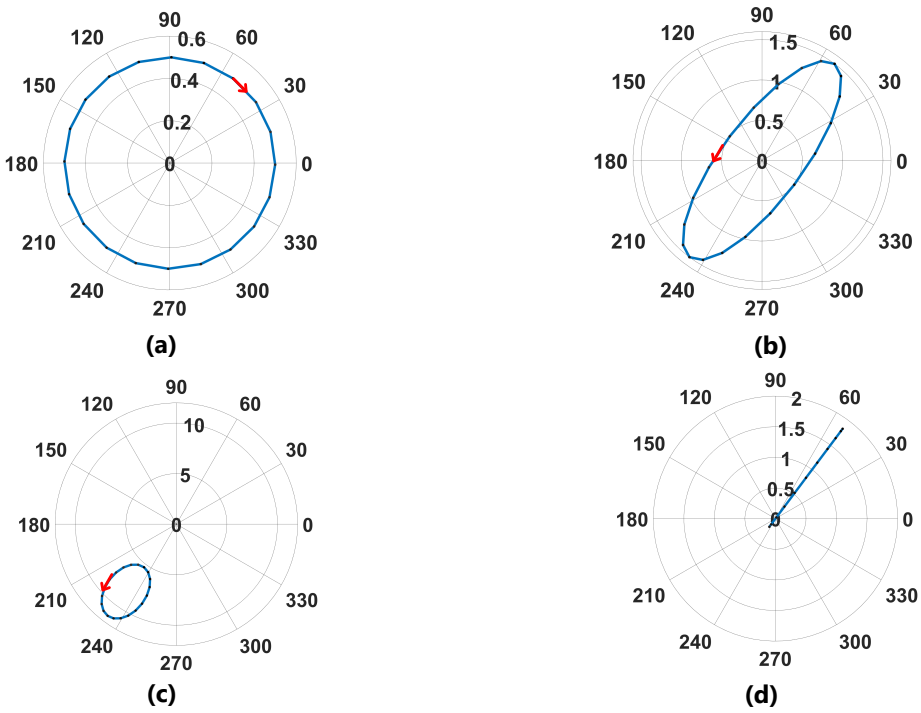


Figure 6.7: Eqn 6.6 plotted for various values of the coefficients. (a) No phase conjugate signal and no LO leakage. (b) Strong phase conjugate signal, no LO leakage. (c) Strong phase conjugate signal, with LO leakage. (d) Equally strong phase conjugate signal and RF leakage with LO leakage.

with close to 0 dB insertion loss as expected. The arrow indicates the direction of increasing delay on the delay line.

Next, the VNA is calibrated at the reference planes indicated in the scheme with the amplifier and frequency divider biased at quiescent. These two ports are then connected as shown in the scheme and S21 measured with first the divider and amplifier being turned off, and then with them on. As is shown in Fig. 6.10, the contour is offset from the center of the ϕ plane owing to the leakage of the LO at the same frequency. However, the points now trace an ellipse in the counter clockwise direction as expected if the phase conjugate signal dominates. This also leads to an interesting class of network behavior that could be exploited in certain applications like matching networks for example. For more context, Fig. 6.11 details

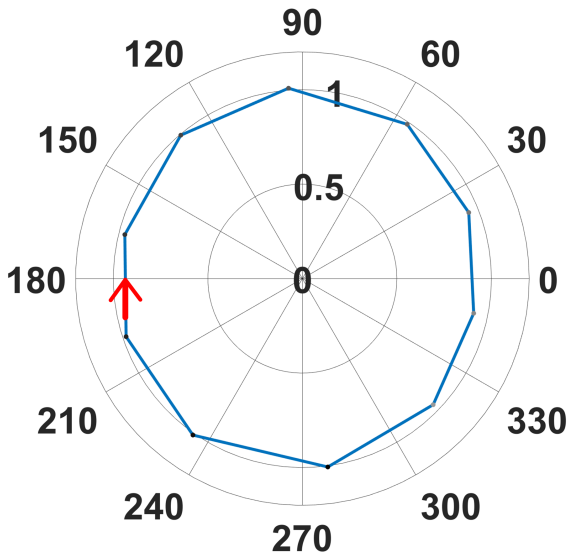


Figure 6.8: S21 of the phase shifter on a polar plot as the phase settings are altered (increasing phase delay, in steps of 10 degrees per gigacycles).

these contours on the same polar plot. Each point is color coded, and similarly coded colors correspond to the same physical setting on the phase shifter in both cases. As is evident, the directions traced by both these are opposite of one another like stated above. The geometrical nature of the contour can be used to quantify the various expected terms as noted above.

It is instructive to attempt to fit the contour shown in Fig. 6.10 to Eqn. 6.6 to quantify the various components. This is done in Fig. 6.12. The quantities ϵ, μ and ν are listed in the table below. As can be interpreted based on the contour and confirmed by the analysis, the LO leakage dominates. The phase conjugate term is stronger than the leakage as expected as well. Since the terms in 6.3 are normalized to the input amplitude, these are directly an indication of each term at the output. This method thus provides both a qualitative and quantitative method to characterize the amount of phase conjugate signal. The powers normalized in dB correlate exceedingly well with the large signal measurements in Table 6.2 in terms of the approximately 5 dB difference between the RF leakage and the conversion loss. This provides additional confirmation about the validity of this methodology.

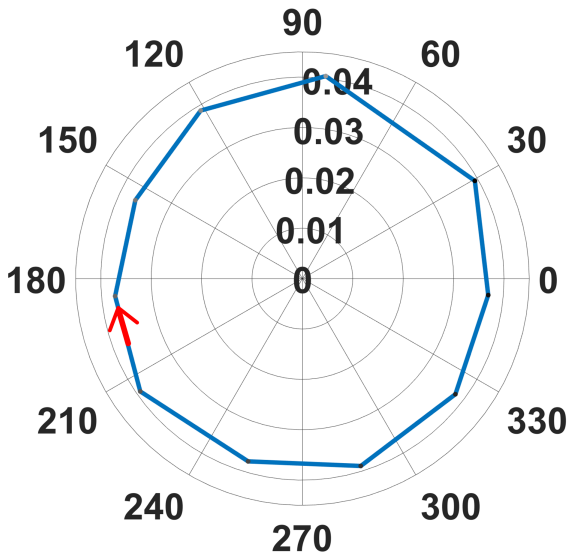


Figure 6.9: S21 of the scheme shown above on a polar plot as the phase settings are altered, with the LO amp and frequency divider turned off(increasing phase delay, in steps of 10 degrees per gigacycles). More points would add more granularity.

Parameter	Complex	Magnitude (linear)	dB norm.
ϵ	-0.01345+0.01565i	0.0206	-9.03
ν	0.03 + 0.0553i	0.0629	-4.19
μ	-0.1555 - 0.05506i	0.1650	0

Table 6.3: Values of the various complex quantities from curvefitting to an ellipse using Equation. 6.6. The values are normalized to the LO leakage in the last column. The analysis shows that the phase conjugate signal is 4.8 dB stronger than the leakage.

6.4 Conclusion and future work

A phase conjugator architecture suitable for extension to mm-wave bands is demonstrated at RF frequencies on a low frequency prototype PCB. The circuit uses a 4th harmonic mixer relaxing the frequency requirement on the LO considerably. Next, a metrology technique to characterize the actual degree of phase conjugation is demonstrated. This has interesting implications for network synthesis resulting from the parametric nature of this operation, and could be an area of future research. The latter part of the chapter and analysis therein also answers the research question about quantifying the amount of phase conjugate signal versus the other components using cogent complex analysis and curve fitting.

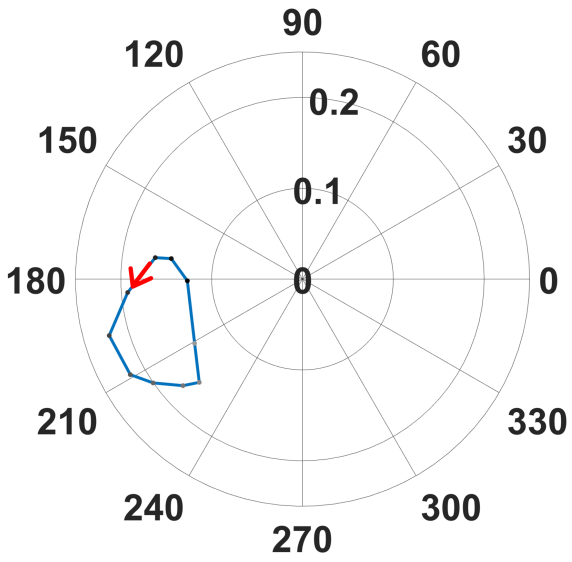


Figure 6.10: S21 of the scheme shown above on a polar plot as the phase settings are altered, with the LO amp and frequency divider turned on(increasing phase delay, in steps of 10 degrees per gigacycles).

6.5 Personal Contributions

- Co-designed the conjugator architecture with Zhiyang Liu
- Designed and simulated the specific implementation on FR4 at 3.4 GHz.
- Characterized the PCB after fabrication at small signal and large signal CW.
- Designed the metrology technique to prove and quantify phase conjugation.
- Led the analysis of the results and the development of the theory detailed above.
- Leading effort to document observations and manuscript writing.

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Matthew Bauwens, Chris Moore, Steven M. Bowers, Robert M. Weikle, Scott Barker, Travis Blalock, Jeffrey Hesler.

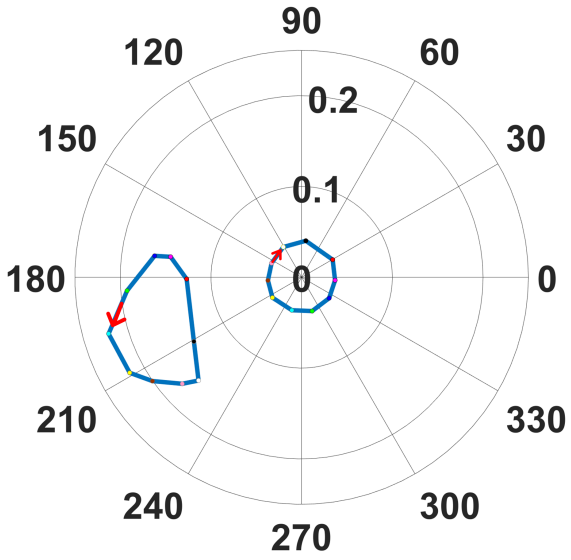

Figure 6.11: S21 of the scheme shown above on a polar plot as the phase settings are altered, with the LO amp and frequency divider turned on(increasing phase delay, in steps of 10 degrees per gigacycles). The contour centered at the origin is traced with the frequency divider and LO amplifier turned off. Each point is color coded and corresponds to exactly the same point on the phase shifter on both plots.

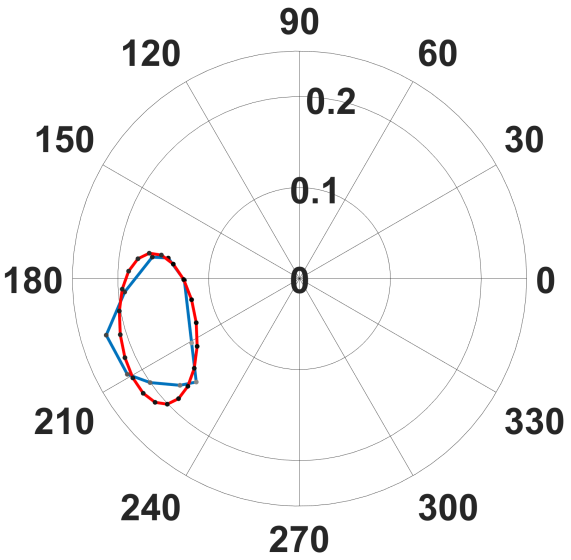

Figure 6.12: S21 on a polar plot with the LO path on, overlaid with an ellipse with parameters determined using Eqn. 6.6 and Table 6.3.

Chapter 7

Conclusion and Future work

This chapter attempts to summarise the conclusions from the individual chapters in one cogent synthesis and details possible directions for future work.

The underlying theme that recurs in the first five the chapters is the need for improved modeling of the InP HBT devices (specifically from Teledyne) under varying amounts of RF and thermal stress. PA designers will also increasingly benefit from a thermal model that is coupled to the electrical model and that converges reasonably easily, to be able to run two tone and modulated stimulus simulations to see the effects on the core devices and its performance. There has been a plethora of work on modeling GaAs devices, but to the best of the author's knowledge, there is a gap in literature for the InP devices used in most of this thesis. A unified framework that combines the thermal and electrical simulations in a unified framework would be the hoy grail for large signal circuit (and specifically PA) designers. As InP devices show increasing potential at the THz frequencies, the need for better modeling in every sense will only become paramount.

As mmwave systems proliferate, there will be an increasing need to be able to build complex subsystems that include antennas on the chip, and research on numerical solutions to reduce simulation time (in addition to the usage of virtual shorts and opens) will be extremely beneficial.Finally, the use of artificial intelligence (AI) as a tool cannot be discounted. There has been research on AI assisted

power amplifier design, and the output matching network (perhaps the most critical part of the design) of such an endeavor does not look like anything that a PA designer would envision. A potential area of research could be using AI/Reinforcement learning to either simulate complex electromagnetic structures exceedingly easily or in generating a network (perhaps an antenna) that behaves the way we would like at different frequencies- that in itself is not new and has been around for a while. What would be truly useful would be in capturing the complex models for these transistors and the antenna/output networks in a single encapsulation that can interact and learn on the go. This would be especially useful in something like the phase conjugating array that was designed, especially since each of these pieces were simulated separately and then put together in a simulation increasing the chances of error etc.

A third area of research could be the unique opportunity to heterogeneously integrate the diodes and other devices built at UVA with these transistor devices. A synergy between the two technologies could enable increasing amounts of signal processing, and functionality that was previously unimaginable, especially something akin to putting amplifiers/conditioning circuits close to the probe tip on a waveguide probe, or in building a hybrid system that could subsume the SpaceK amplifier and the quadrupler used in [118] into one single device.

A fourth area of research could be the genesis of non-traditional matching networks using the methods outlined in Chapter 6 on phase conjugation. While foster networks are strictly defined as having a certain behavior with respect to frequency, these networks have a certain behavior with respect to phase and this could perhaps somehow be exploited. The fact that this is a parametric phenomenon gives it certain qualities that would otherwise not exist in a traditional network.

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