In-sensor Synaptic Computing in a Curved Image Sensor via three-dimensional Heterogeneous integration

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Doeon Lee

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This Dissertation is submitted in partial fulfillment of the requirements for the degree

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Authored by:

Doeon Lee

This Dissertation has been read and approved by the examining committee:

Kyusang Lee, PhD
Advisor

Andreas Beling, PhD
Committee Chair

Mona Zebarjadi, PhD
Committee Member

Nikhil Shukla, PhD
Committee Member

Seongkook Heo, PhD
Committee Member

Accepted for the School of Engineering and Applied Science:

Jennifer L. West, School of Engineering and Applied Science
May 2022

Abstract

Image sensor technology provides a bridge between the physical world of analogue image/light signals and virtual digital data by converting light signals to electrical signals. There has been a dramatic improvement in silicon-based image sensor technology, in which the number of pixels and nodes has been exponentially increased in virtue of the rapid development of semiconductor fabrication technology. When a large amount of raw data generated in the photodetectors are transported to the computing system through limited sensory nodes, the conventional image sensors, however, suffer from a data bottleneck effect at the sensor/processor interface as well as within the processor with the von Neumann computing architecture, resulting in data transportation and computation delay. This delay can be a critical issue to image sensor applications that require fast image processing and strict delay requirements, such as autonomous driving and real-time video analysis. Furthermore, a planar geometry of the typical image sensors still needs bulky and complex optics lenses to minimize spherical aberration. The bulky lens system is the main obstacle in further miniaturization of the planar image sensors. In this proposal, I will develop a curved computational image sensor with the capability of in-sensor computing via heterogeneous integration and thin-film III-V compound semiconductor fabrication techniques. This entirely novel image sensor system will effectively overcome the abovementioned limitations in conventional image sensors by adopting the hemispherical geometry of the imager and in-sensor computing architecture.

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Epitaxial growth and heterogeneous integration

1.1 Introduction

Epitaxy, which is the art of growing single-crystalline materials on a crystallographically oriented wafer, is an essential technology to develop modern high-performance electronic and optoelectronic devices overcoming inherent limitation of silicon such as fixed and indirect bandgap nature and low electron/hole mobility. Thus, various epitaxial growth methods enable growths of a wide variety of III-V and III-N compound semiconductors and complex oxide materials for post-silicon electronic and photonic devices with an operation wavelength from infrared (IR) to ultraviolet (UV). Epitaxial growth process can be basically classified into two types: 1) homoepitaxy, which is a growth of an identical material on a substrate, and 2) heteroepitaxy, which is a growth of a dissimilar material on a substrate. Homoepitaxial growth generally provides a high-quality single-crystalline epitaxial film copying the materials composition and crystal structure of the substrate. On the other hand, heteroepitaxial growth is typically limited by the lattice matching requirement between an epilayer and a substrate material. For example, monolithic integration of III–V and III–N compound semiconductors on

silicon has been of great interest in electronic and photonic communities to compensate for the poor carrier mobility and light-emitting efficiency of silicon-based integrated circuits. However, such approaches have been restricted by the generation of a high density of defects in the epitaxial heterostructure on silicon due to the large lattice and thermal expansion coefficient mismatch between the two materials.

Various epitaxial growth techniques have been developed for heteroepitaxy of highly lattice-mismatched material systems by reducing epitaxial defects and threading dislocations: low-temperature buffer layer, lattice-engineered buffer layer, metamorphic buffer layer, domain-matched epitaxy and epitaxial lateral overgrowth. By controlling the density of defects and threading dislocations, these epitaxial growth methods allow a wide variety of compound semiconductors to be grown on lattice-mismatched substrates broadening the spectrum of their applications.

However, obtaining a high crystalline quality of heteroepitaxial grown films comparable to that of homoepitaxial films is still challenging in large lattice mismatched material systems while homoepitaxy often requires extremely expensive substrates. This limits wide adoption of such electronic/photonic materials in major commercial markets. While advanced heteroepitaxy techniques can accommodate relatively large lattice mismatch between the device (active) layer and substrate (often mismatch greater than 10%), direct heteroepitaxy without any form of strain/domain engineering typically forms extremely defective or polycrystalline device layers if the mismatch is more than a few per cent. Thus, monolithic integration of high-efficiency devices via heteroepitaxy becomes complex, expensive and time consuming.

An elegant solution is to lift-off and transfer the grown epitaxial layer from the substrate, which enables a heterogeneous integration of highly mismatched material systems. The lift-off approach gives the freedom to transfer the released epilayer onto any arbitrary substrate of interest, and also allows the expensive substrates to be reused if the substrate is undamaged during the lift-off process, reducing the overall cost of device production. Various lift-off technologies have been developed, including epitaxial lift-off (ELO), mechanical spalling, laser lift-off and two-dimensional (2D) material-assisted layer transfer (2DLT), in accordance with the growing need for heterogeneous integration of dissimilar materials. In particular, 2DLT requires unique epitaxial techniques such as remote epitaxy or van der Waals (vdW) epitaxy, allowing growth of single-crystalline thin films on 2D materials, which can be easily exfoliated from the weak vdW interface.

In this chapter, I first summarize conventional epitaxial growth methods to form epitaxial heterostructures with low defect densities. Then, I give an overview of advanced heteroepitaxy techniques for monolithic integration of high quality device layers to lattice mismatching substrates, and ELO technique for heterogeneous integration of highly lattice mismatched systems. Furthermore, I introduce emerging epitaxial growth techniques that involve 2D materials as an epitaxial release layer. Finally, I suggest desirable direction for future integrated computing systems harnessing advanced epitaxial growth and lift-off approaches.

1.2 Epitaxial Growth Tools

In this section I introduce three commonly used growth techniques: molecular beam epitaxy (MBE), metal-organic chemical vapor deposition (MOCVD), and pulsed

laser deposition (PLD). These three tools mainly differ in the type of sources used, growth conditions, and growth dynamics. However, all three methods produce high-quality single crystalline films.[1,2]

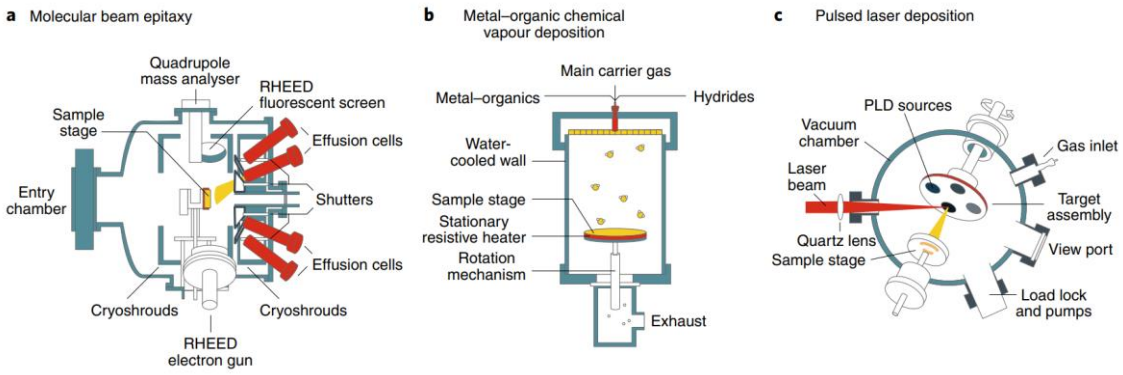

Figure 1.1 Epitaxial growth tools. Schematic illustrations of **a,** molecular beam epitaxy (MBE) **b,** metal-organic chemical vapor deposition (MOCVD) **c,** and pulsed laser deposition (PLD) tools for epitaxial growth of elementary crystalline group IV elements, as well as compound semiconductors (III-V and III-N) and complex functional oxides of perovskite, spinel, and garnet crystal family.

MBE is ultrahigh-vacuum (UHV, $<10^{-10}$ Torr) evaporation techniques for the growth of epitaxial layers on a heated crystalline substrate by atomic or molecular beams from constituent ultra-pure source materials. It is possible to precisely control the layer thickness in monolayer resolution, material purity, doping concentration, and alloy composition. The general MBE system (Fig. 1.1a) consists of effusion cells with constituent elements are pointing and arranged around the substrate to ensure epitaxial surface uniformity. The epitaxial growth process occurs when a flux of molecular beams generated from the heated sources impinge on the heated crystalline substrate, giving rise

to chemical reaction of constituent elements on the surface of the wafer. Growth in the MBE largely depends on a kinetic process such as adsorption, desorption, incorporation, migration, and reaction. As a result, growth rate, doping profile, and alloy composition are predominantly governed by the arrival rate of constituent elements on the substrate surface. The MBE system possesses a robust *in-situ* growth monitor, reflection high-energy electron diffraction (RHEED). RHEED is a very sensitive diagnostic tool for the analysis of the surface structures of crystalline semiconductor. As only few monolayers at the substrate surface contribute to the diffraction pattern due to the near-horizontal incident angle of electrons, RHEED allows real-time monitoring and analysis of epitaxially grown crystalline layers. With this *in-situ* monitoring tool combined with UHV and relatively low temperature growth environment, the MBE system is a powerful epitaxial growth tool for studying fundamental science and production of extremely high-quality single-crystalline compound semiconductors for high performance electronic/optoelectronic devices.

MOCVD, on the other hand, is the preferred epitaxial equipment for large-volume manufacturing owing to its relatively fast growth rate (> 2-5 μm/h) and uniformity for large wafer sizes. The MOCVD (Fig. 1.1b) often utilizes hydrides for group V elements and organometallic compounds for group III elements (such as trimethylgallium, trimethylaluminum, trimethylindium). These organometallic compounds are chosen as source materials since relatively low temperatures are required for their complete pyrolysis (typical growth temperature of 550-750 ℃ for III-V compounds and 500-1000 ℃ for III-N compounds). Similarly, less thermally stable chemical species for N source is used, such as hydrazine, which demonstrates pyrolysis as low as 220 ℃[3]. The

decomposition of N at high temperatures can also be greatly mitigated by high partial pressure of N source with III/V gas ratios as high as 2000. The use of the MOCVD for compound semiconductor growth have dominated the market in the recent decade, especially with the continuing surge of light emitting diode (LED) demands for backlighting and solid-state lighting application. In the MOCVD, real time diagnosis of epitaxial films is allowed by emissivity corrected pyrometry with various wavelength LEDs to monitor the growth rate and surface roughness.

PLD (Fig. 1.1c) has also emerged in recent decades as a means of growing epitaxial films of oxide materials. Its popularity has grown shortly after its inception when the PLD was used to epitaxially grow high temperature superconductor (HTS)[4]. The PLD requires a low pressure system in the presence of precursor gases such as O_2, N_2 and H_2, pulses of lasers are 'shot' to ablate a target with the desired source material and deposit the ablated material onto the substrate opposite of the target. During the ablation process, hot dense plasma is formed which react with the background gasses to form oxides, nitrides or hydrides that deposit onto the substrate to create stoichiometric high-quality films. While the ablation is a complex process, with many factors and physical phenomena that closely interplay with each other[5–8], irrespective of the ablation process, the stoichiometric composition of the epitaxial film exactly matches the composition of the target, enabling single crystalline epitaxial growth of complex alloys. The deposition rate can be precisely controlled by the rate of laser shots and number of shots, with a growth rate comparable to MOCVD at ~2-5 μm/h[9] as well as an accommodation of 6-inch wafers for production. Thus, PLD offers an attractive means of creating artificially layered oxides for fabrication of oxide electronic and magnetic materials and is a versatile

tool for fabricating films of ferroelectric, piezoelectric, pyroelectric, and magnetic materials.

1.3 Epitaxial Growth Techniques

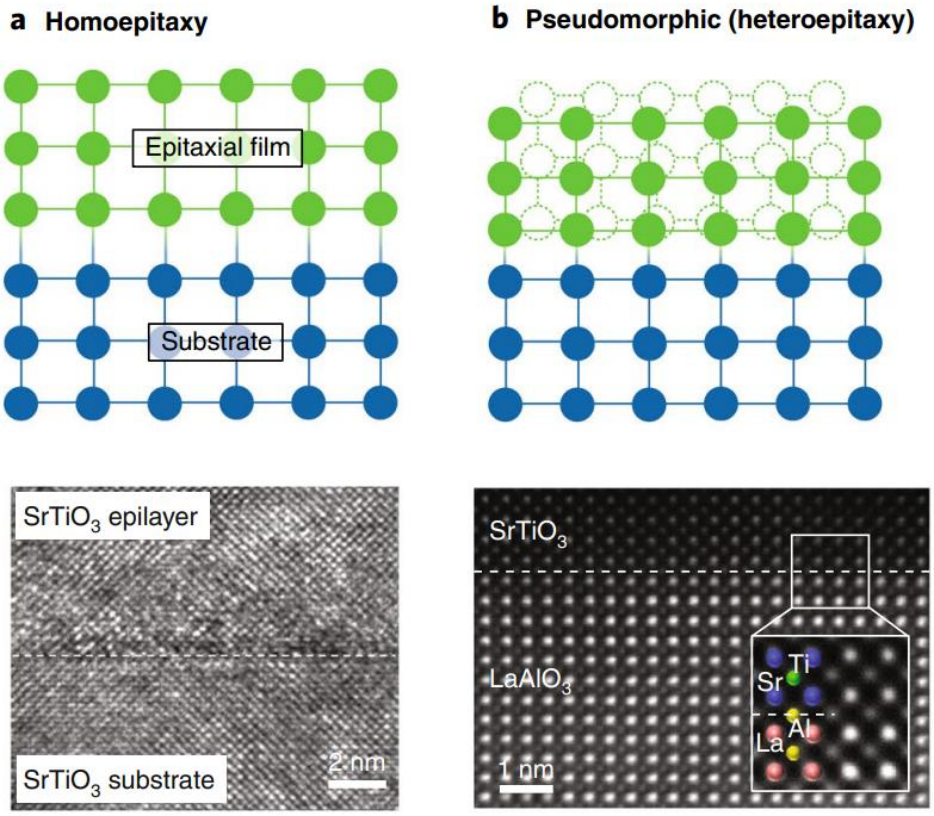

Figure 1.2 Conventional epitaxy techniques. **a**, Illustration of a homoepitaxial growth, where the lattice constant of the epitaxial film is matched to the lattice constant of the substrate. The SEM image below shows $SrTiO_3$ on $SrTiO_3$ homoepitaxy, where the interface between the substrate and epilayer is impossible to distinguish due to the lattice constant being the same. **b**, Illustration of Pseudomorphic epitaxial growth. The epilayer has a different lattice constant than the substrate. The epilayer has to conform to the lattice of the substrate to grow without defects. The original lattice of the epilayer is shown in

dotted line and the strained epilayer is shown in solid lines. If the epilayer thickness increases beyond the "critical thickness", the strain at the interface will relax and cause threading dislocations. The SEM below shows $SrTiO_3$ on $LaAlO_3$ that is pseudomorphically grown. The lattice constant of $SrTiO_3$ is 3.905 Å , whereas the $LaAlO_3$ lattice constant is 3.787 Å .

While epitaxial growth of homogenous materials (Fig. 1.2a) pose no challenge, heteroepitaxy is unavoidable for device structures and applications that lack lattice matched substrates or involve multiple materials of different lattice constants[10–12]. Heteroepitaxy is the epitaxial growth of an epilayer on a substrate with different lattice constants. At the initial stage, the lattices of the epilayer are deformed elastically to comply with the substrate, i.e. pseudomorphically strained. Pseudomorphic heterostructures (Fig. 1.2b) can only sustain up to a certain thickness before the strain is relaxed and dislocations are generated within the epilayer. The thickness at which relaxation occurs is called the critical thickness, which is inversely proportional to the magnitude of lattice mismatch between the epilayer and the substrate[13–16]. The resulting misfit dislocations act as carrier scattering centers, leading to substantial carrier mobility degradation which is detrimental to electronic applications. The difficulty is also in part due to the difference in thermal expansion coefficient between the epilayer and substrate. Upon more shrinkage of films, cracks are generated during the cooldown process after growth, leading to device failure. Therefore, epitaxial growth of complex heterostructures with large lattice mismatch requires ingenious techniques to achieve controllable relaxation with low defect densities.

Low temperature (LT) buffer layers are the most popular technique bridging the substrate and final epilayers. By deposition at relatively low temperature, the LT buffer layer develops as crystals with fine grains, relaxation and flat surface can be obtained in the early stage, which is beneficial to the subsequent growth of high-quality target epitaxial layer at elevated temperatures. As an example, LT-AlN buffer layer was used prior the growth of GaN on sapphire substrate, which has 16% lattice mismatch with GaN[17]. Such invention directly resulted in the consecutive successes in GaN based device development as the device quality GaN was obtained for the first time on sapphire substrates.

For more controllable strain release at the lattice, lattice-engineered buffers based on the bending or gliding of dislocations, such as superlattices and graded composition layers, have been developed while minimizing the generation of dislocations in lattice-mismatched heterostructures. With superlattice buffers such as InGaAs/GaAs and InGaP/InP with alternating compositions, it was shown that the threading dislocation density can be reduced by one to two orders of magnitude by facilitating the bending of dislocations.

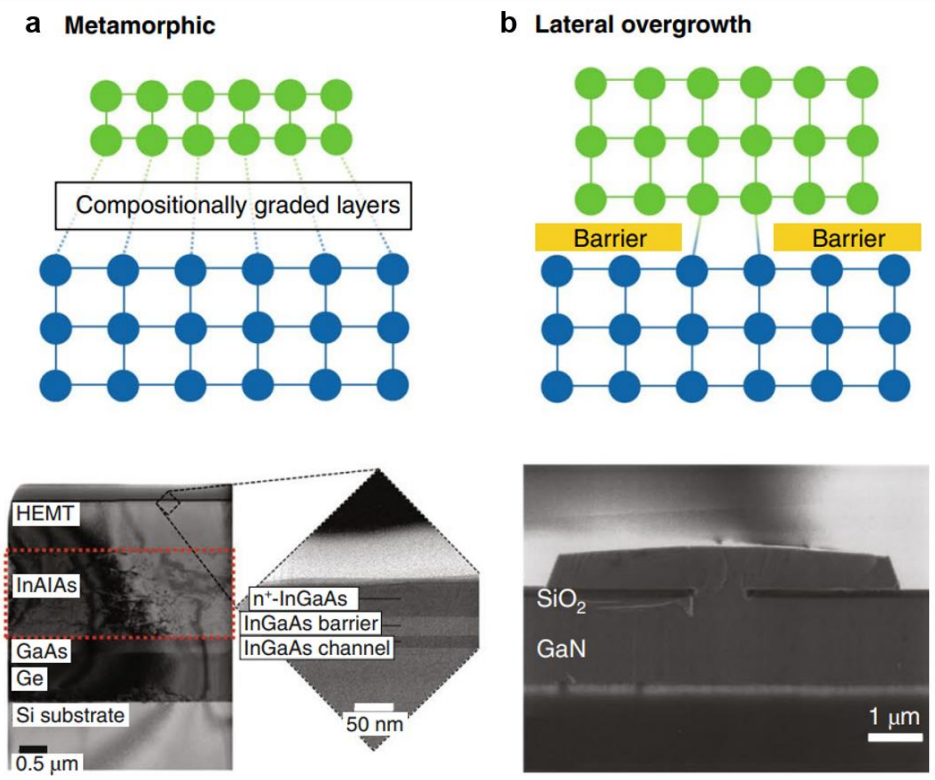

Figure 1.3 **a**, Illustration of metamorphic growth technique, in which a thick buffer consisting of compositionally graded heterostructure is used to gradually change the lattice closer to match the active epilayer. In the SEM below, an InAlAs metamorphic buffer is used to grow low defect InGaAs HEMT on a Si substrate. **b**, Schematic of lateral overgrowth (or selective area epitaxy), where an inert oxide mask is used to define small areas where heteroepitaxy occurs. The epilayer grows laterally outside the mask and merges into a complete film, leaving the defects localized in the area of the holes. The SEM below shows lateral overgrowth of GaN on a sapphire substrate using SiO_2 as the mask.

It has been also known that step graded composition layers (also known as metamorphic buffer layers) can substantially reduce the dislocation density by facilitating

dislocation glide due to the higher surface residual strain compared to that with an abrupt change of composition (Fig. 1.3a). Graded composition buffer layers have been proven to achieve significantly improved material quality at the active device layer for III-V and Si-Ge material systems, by localizing the dislocation at the electrically inactive metamorphic buffer layer. For example, a metamorphic $Si_{(1-x)}Ge_x$ buffer layer with linear grading of Ge composition from 0% to 30% enhanced the electron mobility by two folds, in comparison to an abrupt $Si_{0.7}Ge_{0.3}$/Si heterostructure[18]. Metamorphic buffer layer has also been utilized to achieve triple junction solar cell with efficiency more than 41%. In this case, a 1.4 μm thick $Ga_{(1-x)}In_xAs$ layer with stepwise grading of indium content from 1% to 17% was inserted between a Ge bottom cell and a $Ga_{0.83}In_{0.17}As$ mid cell to bridging the lattice mismatch of 1.1%[19].

Last but not least, epitaxial lateral overgrowth is another lattice engineering technique to realize drastic dislocation reduction (Fig. 1.3b). In this case, the substrate surface is covered by a patterned mask (usually a dielectric film such as SiO_2 or SiN_x), which has negligible sticking coefficient to the target material, revealing only small parts of the substrate. The target material grows on the exposed substrate areas and subsequently expands laterally on top of the mask to create a planar film. The lateral growth portion is dislocation free, hence drastically reducing the dislocation density in the epitaxial film. Epitaxial lateral overgrowth has been the only viable option of achieving GaN-based green laser with reasonable lifetime so far due to the lack of high-quality substrates. Similarly using the lateral growth technique, monolithic integration of single crystalline III-V on a Si substrate has also been demonstrated, which is compatible with current complementary metal-oxide-semiconductor (CMOS) processing[20].

1.4 Advanced Epitaxial Growth Approaches

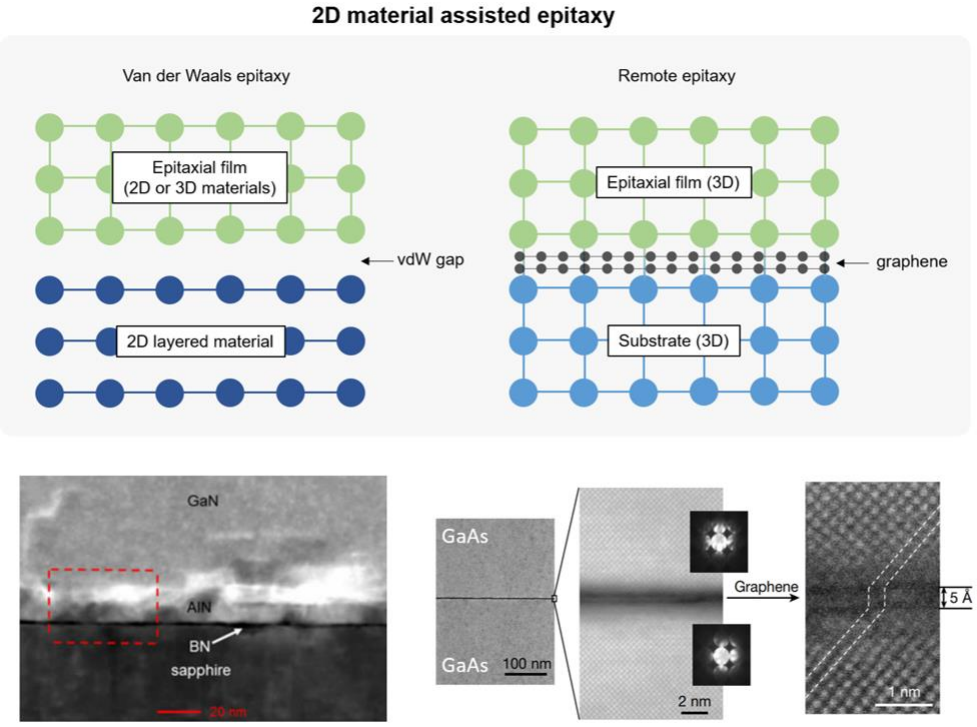

Figure 1.4 Illustration of epitaxy on 2D materials. For vdWE, the epitaxial layer grows without any interaction with the host substrate. The vdW layer becomes the seed for growth. In contrast, for remote epitaxy, a couple monolayers of graphene is transferred or directly grown on the substrate and the epilayer grown directly on top of it. Because graphene is so thin, the polarity of the substrate penetrates the graphene and the adatoms interact with the substrate as if graphene is not present. However, once the growth is finished, the epilayer can be exfoliated and transferred to any arbitrary substrate since the graphene acts as a sacrificial layer for exfoliation.

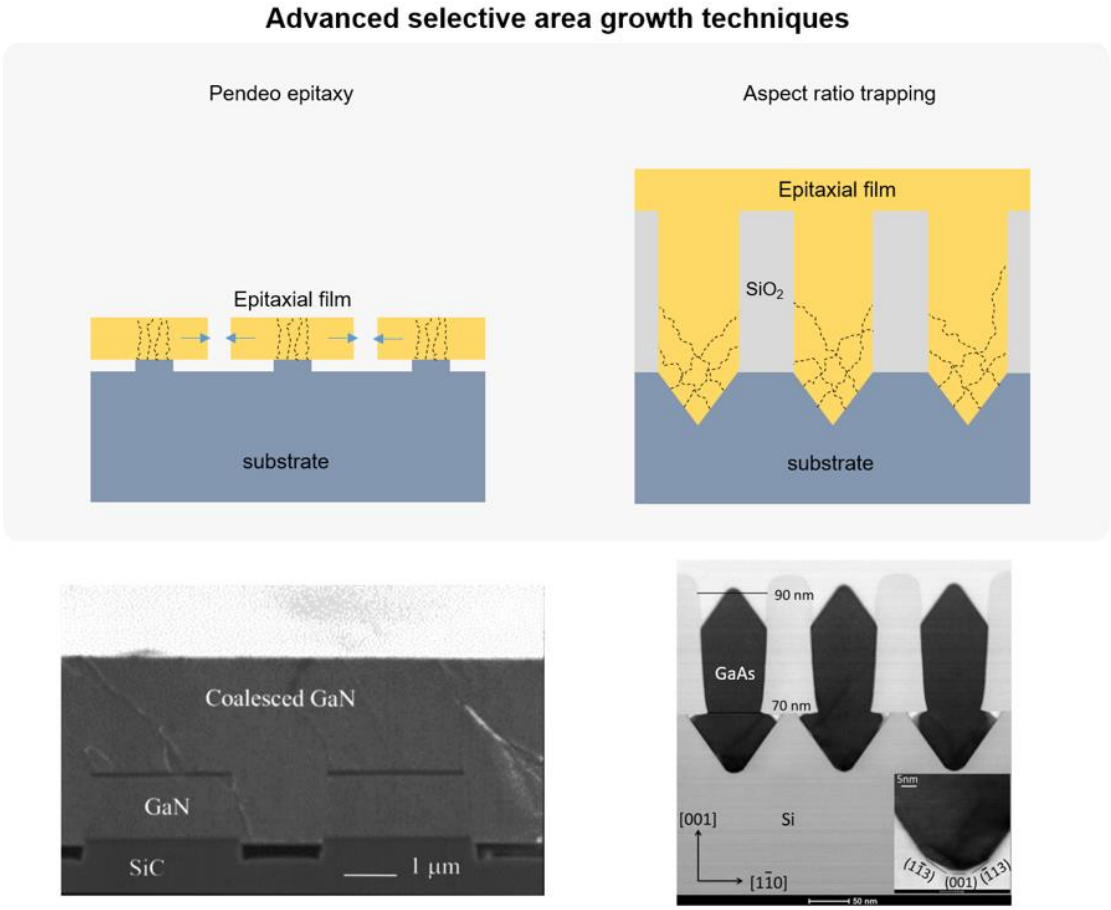

Figure 1.5 Schematic illustration of geometrical confined epitaxy. Pendeo epitaxy is similar to lateral overgrowth, but does not use a mask. Instead, small seed pillars are initially grown on the substrate, and the growth condition is modified such that the growth only occurs laterally. Aspect ratio trapping uses an inert SiO_2 mask similar to lateral overgrowth, but with much deeper trench. However, the substrate is etched such that during growth, the extended defects are confined in the trench and the resulting film outside the trench is mostly defect free.

For highly lattice mismatched systems, conventional epitaxy methods presented above cannot be applied for growing high-quality epitaxial films. Additionally, use of

thick buffer layers are undesirable as it consumes growth sources as well as decreasing production throughput, a major negative for industry focused on mass production. Thus, innovative approaches are required not only to overcome this strict lattice matching rules of epitaxy, but also to enhance manufacturability and adoption. In this section, I give an overview of several novel epitaxy techniques dissimilar from conventional buffer techniques discussed in the previous section to produce large-area single-crystalline epitaxial films. I categorized them into 2D material-assisted epitaxy (Fig 1.4) and geometrically defined epitaxy techniques (Fig. 1.5).[6,21,22]. The former utilizes slippery surfaces of 2D material substrates that can help relax the films before dislocations are introduce into the crystals, and the latter enables geometrical filtering of dislocations in its 3D architectures.

As one of the 2D material-assisted epitaxy technique, van der Waals epitaxy (vdWE) has recently gained an explosive amount of attention owing to the possibility to grow heteroepitaxial films with lattice mismatch greater than 60% (Fig. 1.4). First, discovered by Koma et al.[21,23], vdWE is a method of performing epitaxy of 2D and 3D materials on top of 2D materials or on top of 3D materials with passivated dangling bonds on the surface. Bulk 2D materials exhibit zero dangling bonds at the surface and is held together by a very weak vdW force. Thus, epitaxial strain can be immediately relaxed on slippery 2D surfaces, allowing growth of largely lattice-mismatched materials on top. Because most 2D materials have a hexagonal lattice, bulk materials with similar lattice structure such as III-N have shown robust and high quality growth. For example, the growth of single-crystalline InGaN/GaN blue LEDs on single-crystal h-BN layers have been successfully demonstrated even with substantially high lattice mismatch between

GaN and h-BN (>25%) by adding a thin AlN layer as a buffer between the h-BN and GaN. In addition, the same technique allowed AlGaN/GaN heterostructures grown on h-BN to exhibit an electron mobility of 1,100 $cm^2V^{-1}s^{-1}$[24], which verifies device quality GaN growth on h-BN. Moreover, due to the weak vdW interaction of the h-BN film, the III-N films could be easily released from the substrate using an indium sheet, which opens up further opportunities for heterointegration. Even with > 25% lattice mismatch between GaN and h-BN, the dislocation density in grown-GaN was estimated to be $8.6x10^9$ cm^{-2}. Since further reduction of lattice mismatch between 2D material substrates and epitaxial films can reduce the dislocation density, it is crucial to explore 2D materials whose lattice is closer to conventional III-V or III-N semiconductors for reduced defects in highly lattice mismatched systems.

Remote epitaxy has been recently discovered where epitaxy occurs through ultrathin graphene layers between the epilayer and the substrate due to graphene being transparent to the Coulombic interaction between the adatoms and the substrate surface. (Fig. 1.4)[6,25]. In this method, one to two layers of graphene are transferred or directly grown on the surface of the substrate, followed by epitaxial growth of single-crystalline film seeded by the underlying host substrate through graphene. Remote epitaxy of single-crystalline compound materials such as III-V, III-N, and I-VII have been successfully demonstrated, whereas remote epitaxy cannot be applied for elemental semiconductors such as Si or Ge owing to the lack of surface polarity of these materials. Compared to vdWE, remote epitaxy can occur in lattice-matched systems, preventing dislocation formation in the epitaxial films. As in vdWE, remote epitaxial films can also be easily released from the graphene-coated substrate, which can then be hetero-integrated with

other materials via layer transfer. Moreover, due to the modified surface energy of the substrate surface by adding graphene, it may be possible that remote epitaxy may promote spontaneous relaxation of heteroepitaxial films without generating defects. However, such effects have not been studied in detail and is an open opportunity for investigation.

Compared to 2D material-assisted epitaxy, geometrically defined epitaxy is a more straightforward method to reduce dislocation density by filtering dislocations inside 3-dimensionally fabricated micro-structures. One popular geometrical methods is called pendeo-epitaxy (PE) (Fig. 1.5). This method is conceptually similar to lateral epitaxial overgrowth (LEO); however, several key factors differentiates it from LEO. First, the substrate is patterned such that a seed "post" can be grown on selective areas of the substrate. Due to the lattice mismatch between the "post" material and the substrate, dislocations are formed in the posts. Once the growth of the "post" is complete, the growth condition is changed such that lateral growth happens almost exclusively on the sidewalls of the "post" (there are some variations, but this is the most general description of PE). The material continues to growth laterally from the sidewalls until it meets with material grown from another "post", converging into a full film similar to LEO. This method is most frequently used to grow low defect GaN films. For example, Davis et al. showed PE of GaN with low dislocation density on SiC deposited on Si, with GaN seed posts grown on patterned thin AlN buffer layers[26]. The growth temperature prevents nucleation on the 3C-SiC surface while allowing lateral growth from the sidewall of the GaN seed post without any support or contact with a mask layer. A drastic reduction of threading dislocation was achieved, from dislocation density of 10^9-10^{10} cm^{-2} down to

approximately 10^4-10^5 cm^{-2}, as well as a ten times reduction in leakage currents of a Schottky contact with an ideality factor of nearly one.

Aspect ratio trapping (ART) growth is another representative process to geometrically confine dislocations, studied vigorously for III-V films on Si (Fig. 1.5)[27,28]. So far, ART of single-crystalline GaAs, InAs, and GaSb on Si has been demonstrated, paving the way for monolithic integration of III-V channels with higher mobility on Si substrates. In this method, a V-shaped trench is etched into the substrate while a large aspect ratio mask (typically SiO_2) is fabricated on top to trap and confine the epitaxial layer into a trench. The idea is to confine any extended defects at the bottom of the trench or terminate it at the sidewalls of the SiO_2 mask, allowing a defect free film to be grown at the upper region of the epilayer where it coalesces into a film. This method was shown to significantly reduce anti-phase boundaries and threading dislocations of GaAs or Ge on Si to also zero. However, this method is reported to still produce twin planes at a density of 10^8 cm^{-2} which cannot be confined within the trench, and remains a challenge to be solved[28].

One major drawback of geometrically defined epitaxial methods is that it involves a time consuming and expensive pre-epitaxy process of patterning the substrate, which involves mask deposition, photolithography, etch processes, and extra cleaning steps. So far, the benefits of better material quality using these methods do not justify the extra time and cost required to implement them at an industrial scale. However, I speculate that as heterointegration of vastly dissimilar materials on Si is becoming increasingly important, these methods will be revisited and improved for faster throughput and cheaper cost, such as utilizing roll-to-roll imprint lithography techniques and such.

1.5 Heterointegration via epitaxial lift-off and layer transfer

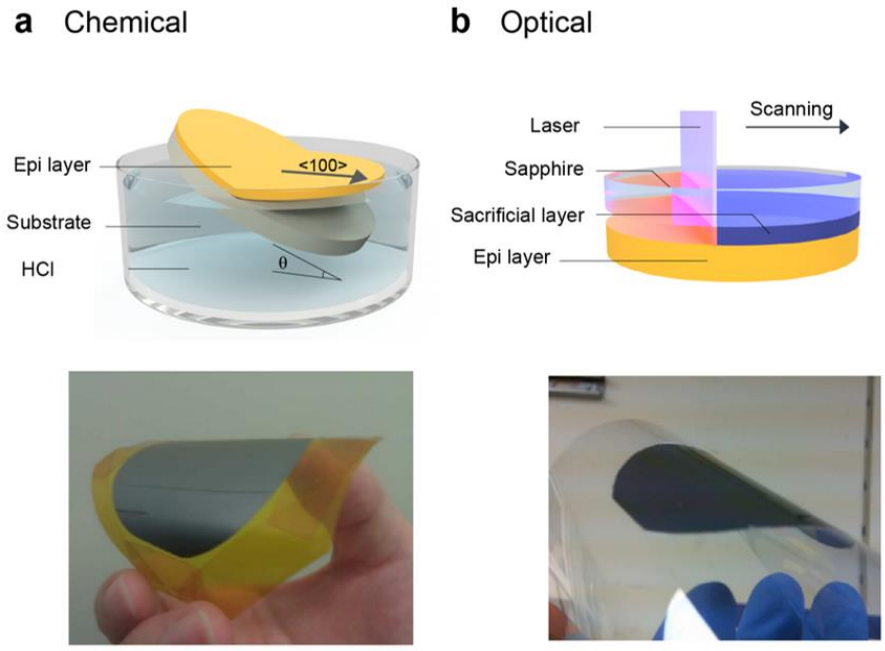

Figure 1.6 Schematic illustrations of epitaxial lift-off techniques using **a**, chemically etched sacrificial layer, **b**, optically induced separation between the epilayer and substrate.

Epitaxial lift-off techniques are becoming increasingly important as thin, flexible, light-weight and 3D-integrated structures. The major benefits of epitaxial lift-off techniques are two-fold, (1) it allows heterogeneous integration of dissimilar materials which cannot be otherwise integrated together for expanded functionality, and (2) reuse of the host substrate which dramatically reduces the fabrication cost of devices.[6,29–31]

Several lift-off technologies have been developed so far in industrial scale. Chemical lift-off is a method of creating freestanding epitaxial films by inserting a sacrificial layer that can be selectively etched before growing the active device (Fig. 1.6a)[32,33,42–50,34–41]. For example, Al(Ga)As can be etched by hydrofluoric acid (HF)

whereas (In)GaAs based materials is resistant to HF, allowing Al(Ga)As to be used as a sacrificial layer to create freestanding GaAs-based devices such as solar cells, LEDs, and detectors[32,33,56–65,34,66–72,35,48,51–55]. Complex perovskite oxides use acid[73,74] or water-soluble layers[75] to produce freestanding single-crystalline films. For example, $La_{0.7}Sr_{0.3}MnO_3$ (LSMO) was used as a sacrificial layer to release centimeter scale perovskite films in KOH, whereas Lu et al. demonstrated synthesis of freestanding thin-film heterostructures by engineering a water soluble $Sr_3Al_2O_6$ buffer layer[76–81]. Although chemical lift-off of centimeter scale coupon wafers is relatively quick, wafer scale release typically takes several hours to even days[59,82–84], which limits throughput and detrimental for high volume production. Several groups have devised creative ways to accelerate the lift-off process by inducing epitaxial strain[85,86] and adding physical weights to the exfoliated film to maximize the area of the sacrificial layer exposed to the etchant solution[36,38,39,41–43,45,85–87]. The surface roughness of the host substrate after the chemical etch is also an issue, preventing immediate reuse of the substrate and requiring chemical and mechanical polishing to reconstruct an epi-ready surface. Although few groups have demonstrated atomically smooth etching morphology, significant reusability of the substrate (> 50 times) has not been demonstrated to date. Chemical lift-off has seen the most success in the photovoltaic industry, where world record efficiencies have been demonstrated via photon recycling effect by integrating the photovoltaic cell with rear surface mirror.

Laser lift-off is a technique of separating epitaxial layers from transparent substrates such as sapphire or SiC using excimer lasers (Fig. 1.6b). This method uses short wavelength lasers which is absorbed by the GaN film, decomposing the

substrate/GaN interface into metallic Ga and N_2 gas, which can then be heated above the melting point of Ga (30° C) to separate the epilayer from the substrate. Damage free separation of GaN from sapphire was demonstrated using 248 nm laser at 400-600 mJ/cm^2 fluences[88]. However, because of the induced plasma at the interface during laser excitation, the substrate surface is roughened, with roughness ranging from 60-90 nm[89,90] such that subsequent epitaxy cannot be done unless the substrate is chemically and mechanically polished. This technique is fast and robust for epitaxial films that are grown on high band-gap substrates, but therefore limited in terms of the scope of materials possible. Nevertheless, high bandgap materials have been gaining increasing attention over the past few years for applications in quantum computing[91], power electronics[92,93,102–104,94–101], and high efficiency laser diodes[105–107] which may potentially allow vertical integration of high band gap electronics and optoelectronics on a single platform.

Mechanical spalling is a brute force method of creating thin films in the microns-thick range, where a metal stressor layer (typically thick Ni films) is used to initiate a crack running parallel to the substrate (Fig. 1.7a). Mechanical spalling has been demonstrated for Si, Ge, GaAs, and GaN substrates at IBM to generate thin film CMOS circuits[2,108–110], solar cells[111–115], and LEDs[116,117]. As can be deduced from the process description, mechanical spalling is a brute force process which produces films with thicknesses in the hundreds of nanometers to several microns and the roughness of the substrate surface is the roughest of all the epitaxial lift-off techniques as well as depending on the surface orientation. Moreover, the spalling propagation depth cannot be precisely controlled as well as depending on the surface orientation. Thus, this method could be

used for vertical integration of electronic circuit stacks (e.g. 3DVLSI) where physical coupling between each layer is not required[118].

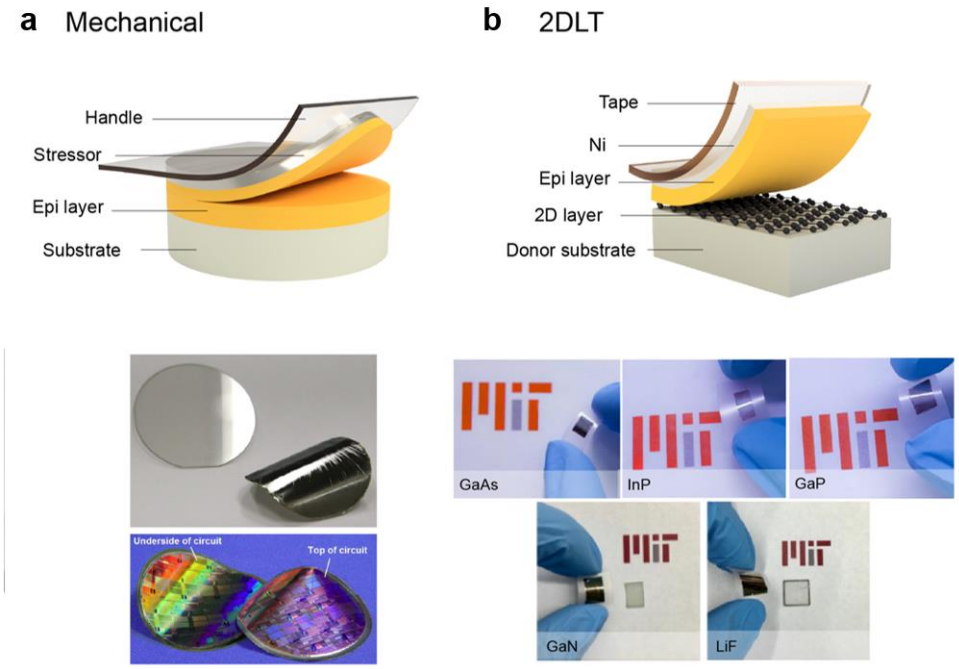

Figure 1.7 **a**, brute-force mechanical exfoliation using a metal stressor layer, and **b**, two-dimensional material assisted layer transfer. The resulting single-crystalline epitaxial membrane is shown below each illustration. Each method has its own advantages and disadvantages, with key parameters being the release-rate, universality of the technique, need for post-release refurbishment of the substrate, and controllability of the exfoliated film thickness.

2D-material assisted layer transfer (2DLT) utilizes the benefits of vdWE and remote epitaxy to generate freestanding single crystalline membranes (Fig. 1.7b). This method is enabled by vdW and remote epitaxy in unison with 2D material transfer techniques, where the weak vdW bonding of 2D materials facilitates exfoliation of

epitaxially grown films from the substrate, leaving a pristine surface after exfoliation. This process is analogous to mechanical spalling but has several advantages. First, the spalling depth is determined by the position of the 2D material rather than the stress of the metal stressor film and thus more controllable. Third, it requires much less stress for the metal stressor compared to spalling and easier to remove the metal after exfoliation. Third, the separation interface is atomically sharp due to the 2D buffer layer not allowing covalent bonds between the epilayer and the substrate. Thus, potentially no wafer refurbish process is necessary such as chemical and mechanical polishing. However, some challenges do still remain for industrial adoption of this technique. For example, elemental semiconductors such as Si and Ge cannot be grown remote epitaxially due to it having no ionicity of their bonds[6]. Also, the area yield of exfoliation depends on the quality of graphene transfer. If there are significant tears, holes, or wrinkles after transferring graphene, the epi uniformity will suffer. The next step is, therefore, is to figure out ways to directly grow mono- or bi-layer graphene on the material of interest, which will significantly improve the quality and yield of 2DLT process by eliminating any transfer defects as well as reduce the vdW gap between the graphene and substrate.

1.6 Applications of advanced epitaxy and lift-off technology

In this section, I provide various applications that is enabled by advanced epitaxial growth and lift-off approaches discussed in previous sections. Additionally, my perspective on the need and desirable direction for epitaxial growth techniques and approaches to further advance the electronics/optoelectronics field will be given[57,119].

One of the early demonstrations of heterointegration of epitaxial thin-films was demonstrated by Yablonovitch et al. through vdW bonding. The authors showed thin semi-transparent GaAs membranes created by chemical lift-off and transferred onto various substrates such as Si, glass, sapphire, $LiNbO_3$, InP, and diamond substrates[29,120]. A thin layer (< 100 Å) of amorphous oxide was seen at the GaAs/substrate interface, showing the potential of heterogenous integration of thin epitaxial films in the early 1990's. Following the research, the epitaxial thin-films have yielded many creative applications for functional electronic and optoelectronic devices such as photodetectors, solar cell, laser, and LED.

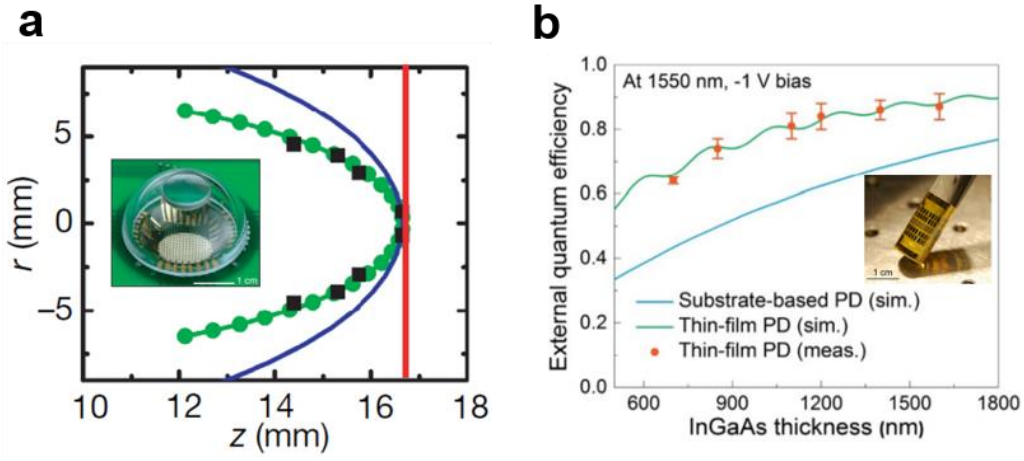

Figure 1.8 **a,** Ray tracing simulation of the curvature of the focal plane of single lens (green circles) and parabolic fit (green curve), the detector surface profile of the hemispherical camera (blue curve), and a planar camera (red curve).[121] Inset: image of the fabricated hemispherical electronic camera. **b,** Comparison of simulated and measured external quantum efficiencies (EQE) as function of intrinsic InGaAs thickness at −1 V bias and 1550 nm wavelength for thin-film (green line) and substrate-based devices (blue line). Measured EQE of fabricated device with bilayer anti-reflection

coating are shown (orange points). Inset: the fabricated 8x100 photodiodes array deformed into a convex form.[122]

Photodetectors on a thin-film substrate can be transformed into a conformal architecture, which allows to achieve a wide field of view and obtain low aberration image with simple optical elements, mimicking biological imaging systems such as human and insect eyes[121–123]. Ko et al. demonstrated a hemispherical conformal imager based on compressible silicon photodiodes array with a single-element lens system[121]. Although the imager has only one lens to focus an image onto the focal plane array, high quality images were obtained without the off-axis optical aberration by matching the surface of the focal plane array to the calculated Petzval surface of the lens (Fig. 1.8a). For a more general approach to offer various wavelength detection with epitaxially grown active materials, a thin-film InGaAs photodetector array was fabricated through the chemical epitaxial lift-off process (inset of Fig. 1.8b)[122]. The flexible array sensitive to near-infrared wavelength was deformed into a convex cylindrically curved imager to achieve 2π field of view, and exhibited high performance even with a thin InGaAs active layer by virtue of having back-side metal mirrors (Fig. 1.8b). While the conformal imager demonstrated was in a cylindrical shape, the epitaxial thin film has potential to be deformed into the hemispherical shape via a concave mesh structure or a kirigami with a proper design of cutting patterns.

A similar kirigami approach can be applied to a solar cell fabricated out of a thin epitaxial film to realize a simple and low-cost solar tracking system, maximizing solar power generation over the course of a day without additional heavy, bulky components

and structural supports[124]. Figure 1.9a shows the integrated thin-film, crystalline GaAs solar cells fabricated by using chemical epitaxial lift-off and kirigami line cut patterning, and the output electrical power densities as function of time of day for flat panel, various kirigami cut designs, and single-axis tracking system. The result indicates that the solar tracking system with the dynamic kirigami structure are capable of near single-axis performance. Meanwhile, the epitaxial lift-off has been used to achieve cost-competitive solar energy conversion via a wafer recycling process[42,57,65], and to fabricate high efficiency solar cell by mechanically stacking of separately grown active materials[114,125–127].

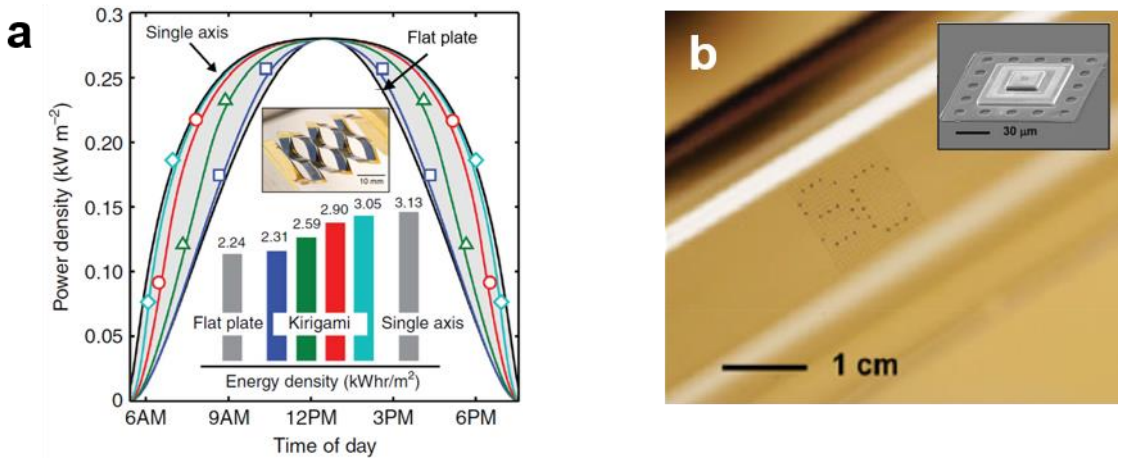

Figure 1.9 **a**, Output electrical power density incident on the solar cell versus time of day for several kirigami cut structures, stationary panel and single-axis tracking systems in Phoenix, AZ (33.45 N, 112.07 W) during the summer solstice. Inset: Integration of the curves yields the associated energy densities, where kirigami-enabled tracking systems are capable of near single-axis performance.[124] **b**, Images of micro-VCSELs on polyethylene terephthalate (PET) substrate with GaAs quantum well active layer. Inset: SEM image of a single micro-VCSEL.[128]

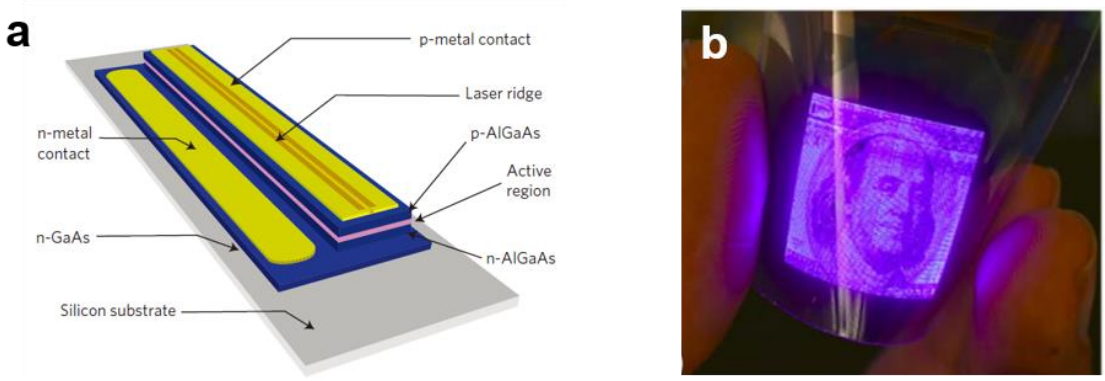

Figure 1.10. **a,** Schematic of a laser on the silicon substrate. **b,** Image of the plastic, flexible, passive-matrix RGB color LED display with 100 RGB × 100 pixels and 254 pixels per inch.

For laser applications, several driving forces has existed to let researchers use epitaxial lift-off to overcome limitations in current laser technology. The two main motivations for use of epitaxial lift-off for laser systems are (i) flexible architectures to allow the laser to be integrated onto low-modulus and curvilinear surfaces such as biological tissues and skins for bio-medical applications[128,129], and (ii) heterogeneous integration with unusual combinations of materials and device structures such as integration of III-V photonic materials onto silicon-based conventional electronic backplane circuits or waveguides[130–132]. An example of the former is a vertical cavity surface emitting laser (VCSEL) transferred on a flexible plastic substrate by employing epitaxial lift-off and transfer printing process (Fig. 1.9b)[128]; an example of the latter is heterogeneous integration of edge emitting lasers based on GaAs onto a silicon substrate for continuous wave operation, representing the potential pathway to low-cost integration of III-V photonic devices and circuits on foreign substrates (Fig. 1.10a)[131]. Eliminating

the native substrates also enable novel applications of LEDs, conceptually similar to the laser applications[133–137]. Figures 1.10b and g show examples of inorganic LEDs on flexible and stretchable substrates: a flexible RGB display based on III-V materials on plastic substrate (Fig. 1.11a)[135] and a stretchable InAlGaP red LEDs with non-coplanar serpentine bridges on a thin PDMS substrate (Fig. 1.11b)[133], which has demonstrated its capability in robotics and clinical medicine applications.

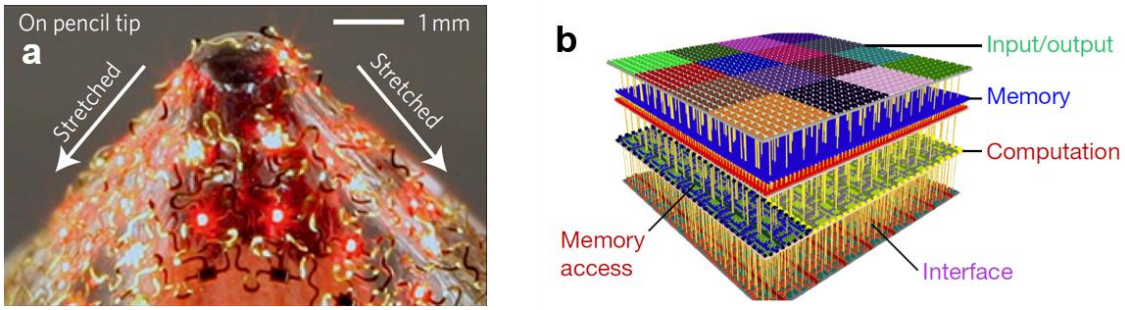

Figure 1.11.**a,** Optical images of an array of AlInGaP red LEDs (6 x 6), tightly stretching onto the sharp tip of a pencil.[135] **b,** Illustration of heterogeneously integrated nanosystem. Bottom layer is silicon FET logic, second layer consists of CNFET logic for the CNFET row decoders and CNFET classification accelerator. Third layer has 1 Mbit RRAM, and CNFET sensors are on top layer. The layers are connected through dense vertical inter-connects.[133]

In addition to optoelectronic device applications, epitaxial growth and lift-off have potential to be exploited to realize non-von Neumann computing systems on a single chip by heterogeneously integrating the required components[119,138,139]. Computational complexity and memory consumption are continuously increasing along with advance of machine learning and artificial intelligence, while traditional CMOS scaling has reached

the end of its technological limit. Subsequently, the demands of alternative computing architecture, circuit, device, and material surge to improve computation performance and energy efficiency of the computing system. One promising approach to mitigate the von Neumann bottleneck is by moving to on-chip memory-based computing system instead of dynamic random access memory (DRAM)-based off-chip computing system[119]. Figure. 5h shows a prototype of heterogeneously integrated on-chip memory computing system for sensing and classifying gases, consisting of input/output layer (carbon nanotube field effect transistors, CNFETs), memory layer (resistive random access memory, RRAM), and computation layer (Si-FETs and CNFETs). The integrated system can capture massive amounts of gases (data) in real time, store the data directly in RRAM, and perform *in-situ* classification of the gases in the computation layer. On the other hand, using advanced epitaxial growth and lift-off processes, various epitaxial layers can be directly integrated onto the on-chip memory computing system to develop the device architecture for a wide variety of applications. Diverse optoelectronic devices based on the epitaxial layer which previously discussed, for example, can be served as the input and output layer for *in-situ* cognitive computing such as image processing, recognition, and classification. Furthermore, phase change memory (e.g., Ge-Sb-Te)[140] and epitaxial random access memory (epiRAM, e.g., SiGe)[141] are applicable for non-volatile on-chip memory, allowing high-capacity data storage with improved speed, spatial density, and energy efficiency compared to DRAM.

1.7 Conclusion

In the short term, growing device quality epitaxial layers on Si wafers for monolithic integration of vertically stacked multifunctional integrated circuits will significantly reduce integrated circuit footprints and allow unprecedented all-in-one chip platforms that couple photonic circuitry with state-of-the-art sensors, transistors, and memory elements being actively processed by neuromorphic chips. Such a platform can be used as a universal processor for internet-of-things (IoT) and the recently emerging AI-of-things (AIoT) applications, significantly impacting the way we live. For this to happen, however, several other technological advancements must be made in parallel.

While monolithic integration with advanced epitaxy techniques can be the simplest way of coupling different materials, grown epitaxial films are defective and heteroepitaxy is only allowed for limited lattice mismatched system. Thus, various lift-off techniques for heterointegration have been invented and developed to produce defect-free epitaxial layers on lattice matching substrates followed by release of the layers from the substrate. In order to secure cost-effective heterointegration of various freestanding membranes, at least, the cost required for lift-off must be lower than that for substrates by maximizing substrate reusability. While various lift-off techniques developed so far have shown promising preliminary devices, they have not satisfied requirements needed to match the large volume manufacturing at a scale seen for current IC industries. However, various companies such as SolAero and Microlink are seriously developing chemical lift-off techniques used in small-scale manufacturing of solar cells, and optical lift-off techniques are being used in InGaN/GaN based LED industry for flip-chip architectures. I believe that high throughput lift-off process may be secured by further

development of the 2DLT technique as it secures fast release of epilayers at controllable interfaces. However, the quality of epitaxy on graphene is not as matured compared to that obtained by conventional direct epitaxy, which must be addressed for the future work.

Owing to its capability of producing thin single-crystalline freestanding flexible membranes, further development of epitaxial lift-off techniques will meet current needs for flexible, conformal, and multifunctional electronics in the system for IoT, smart city, smart vehicles, and wearable electronics. Together with monolithic integration by heteroepitaxy, heterointergration by lift-off can eventually allow mix-and-match various thin film membranes and stack them up for advanced heterointegrated system. While 2D material-based heterostructures have been receiving great deal of attention so far owing to its stackability, electrical and optical properties of 2D materials are substantially inferior compared to conventional semiconductor materials (3D materials). Thus, stackability of various 3D materials enabled by the advanced lift-off technique will open up completely new opportunities for future electronics. Current advancement of 2D heterostructures can also play together as 2D materials can expand the material system that can be stacked with 3D material freestanding membranes.

Another intriguing ability via epitaxy is creating low dimensional structures, which can generate single crystalline structures with 0-D (quantum dots), 1-D (nanowires), and 2-D (quantum wells) confinement of charged carriers, allowing for novel applications not possible using bulk 3D materials. Quantum dots (QDs) confine carriers within itself and does not allow any movement in all directions. Due to this high confinement capability, carriers captured in the QDs tend to be shielded from external perturbations, leading to long carrier lifetimes inside the QD. Epitaxially, QDs are grown

inside a 2D or 3D matrix by utilizing the Stranski-Krastanov (SK) growth mode. For some material systems, the size, density, and placement of the QDs can be deterministically controlled143–147, which have been proposed to be used for quantum computing. Quantum dots are also useful for laser and photovoltaic applications, allowing lasers that are insensitive to temperature with enhanced threshold voltage and modulation bandwidth, and the discrete energy level of QDs allows formation of intermediate bands for two-step photon absorption to artificially broaden the absorption spectrum of a single junction solar cell beyond its bulk limit148,149. Single crystalline nanowires with 1D quantum confinement, on the other hand, can be grown by using metal droplets as a catalyst via VLS, MBE, or MOCVD. Due to its large surface to volume ratio, the nanowires form with absence of extended defects even on substrates with large lattice mismatch. Because of its extremely small dimensions and bottom-up process, a defining advantage is that scaling is facile compared to current lithographical techniques. Also, since the nanowires are defect free, the carrier mobilities are very high and the electrostatic potential can be modulated by a gate-all-around structure which has several advantages over conventional FinFET structures150. However, one challenge to be solved using nanowires for electrical and optoelectrical devices is to find a robust and high-yield method of growing, placing, and integrating individual nanowires in a deterministic fashion onto conventional CMOS platforms. QWs with 2D confinement is made by cladding a thin lower bandgap material layer (usually between 1-5 nm) between two high bandgap material, forming a potential well with discrete energy levels. This type of structure is predominantly used for high-electron mobility transistors (HEMTS) and light-emitting diodes.M[119].

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Chapter 2

β-Ga_2O_3/MgO heterostructure-based UV phototransistor for in-sensor computing

2.1 Introduction

The optoelectronic properties of ultra-wide-bandgap materials such as AlGaN, $Mg_xZn_{1-x}O$, $Zn_xGa_{1-x}O$, BN, and diamond have enabled the implementation of solar-blind deep ultraviolet (DUV) photodetectors for unique applications such as flame detection, missile tracking, pollution monitoring, and inter-satellite communication systems.[1–3] The high thermal stability, high chemical stability, and superior radiation hardness of these materials also enable them to be deployed in harsh conditions, such as high-temperature environments and space. Despite substantial progress in crystal growth technologies over the past few decades, obtaining high-quality ultra-wide-bandgap alloys is still challenging because of their demanding growth conditions and poor crystalline quality.[4–6] For instance, a lattice-mismatched heteroepitaxial growth of AlGaN, and a phase mixing in a high-Mg-content MgZnO, resulted in a large defect density, degrading detecting performance.[6,7] As alternatives to these materials for DUV photodetection, monoclinic β-Ga_2O_3, the most stable phase in the polymorphism of Ga_2O_3, holds promise. Its well-developed melt growth methods, such as the Czochralski method, edge-defined film-fed growth, and the floating zone technique, allow the production of single-crystal β-Ga_2O_3 wafers with superior material quality.[8] In addition, β-Ga_2O_3 active layers obtained by

mechanical exfoliation or homoepitaxy from single-crystal bulk substrates have demonstrated high crystal quality, making them promising contenders for solar-blind high-performance DUV photodetectors.

The figure of merit for DUV photodetectors in particular is responsivity (in A/W), which is inversely proportional to the energy of a detected photon and proportional to the quantum efficiency.[9] The responsivity can be improved by maximizing the absorption of incident light and/or by extracting more carriers per photon. The former strategy was pursued by employing UV-transparent electrodes such as semi-transparent Ni/Au, IZO, and graphene[10–13]; nevertheless, this approach by itself cannot overcome the maximum imposed by the intrinsic material responsivity. The latter strategy achieves higher responsivity by means of avalanche carrier multiplication or unbalanced channel-charge-induced photocurrent gain.[14] In this context, various types of β-Ga_2O_3 photodetector configurations with a photocurrent gain mechanism have been investigated, including metal-semiconductor-metal devices, heterojunctions, and phototransistors. Still, the highest responsivity achieved for the β-Ga_2O_3 photodetector has been ~10^5 A/W.[15]

In this work, I demonstrate a β-Ga_2O_3/MgO heterostructure DUV phototransistor with ultrahigh sensitivity by using the photogating effect to significantly amplify the photocurrent. MgO and Al_2O_3 layers are sputtered by a RF magnetron on top of a β-Ga_2O_3 phototransistor on a Si/SiO_2 substrate, where the heavily doped Si (p^{++}-Si) substrate is used to control a gate. The material properties of the β-Ga_2O_3/MgO/Al_2O_3 layers were characterized by high-resolution transmission electron microscopy (HR-TEM) and energy-dispersive X-ray spectroscopy (EDX). Furthermore, the optoelectronic properties of the β-Ga_2O_3 and β-Ga_2O_3/MgO phototransistors were characterized under illumination

with DUV light and dark condition. A comparison between the β-Ga_2O_3 and β-Ga_2O_3/MgO heterostructure phototransistors shows that the MgO layer efficiently limit the photoconductive effect, such that the photogating effect predominantly governs the β-Ga_2O_3/MgO heterostructure-based phototransistor operation. I ascribe this phenomenon to defect-assisted charge transfer at the β-Ga_2O_3/MgO interface, where the charge transfer process could be described by electronic band diagrams. As the photogating effect is solely responsible for the significant photocurrents due to the restricted photoconduction, the β-Ga_2O_3/MgO phototransistor showed an ultrahigh responsivity of 2.4×10^7 A/W and a specific detectivity of 1.7×10^{15} Jones at the wavelength of 260 nm. These unprecedentedly high DUV responsivity and specific detectivity values confirm that the β-Ga_2O_3/MgO heterostructure-based phototransistor outperforms previously reported β-Ga_2O_3-based DUV photodetectors.

2.2 Fabrication of β-Ga2O3/MgO heterojunction phototransistor

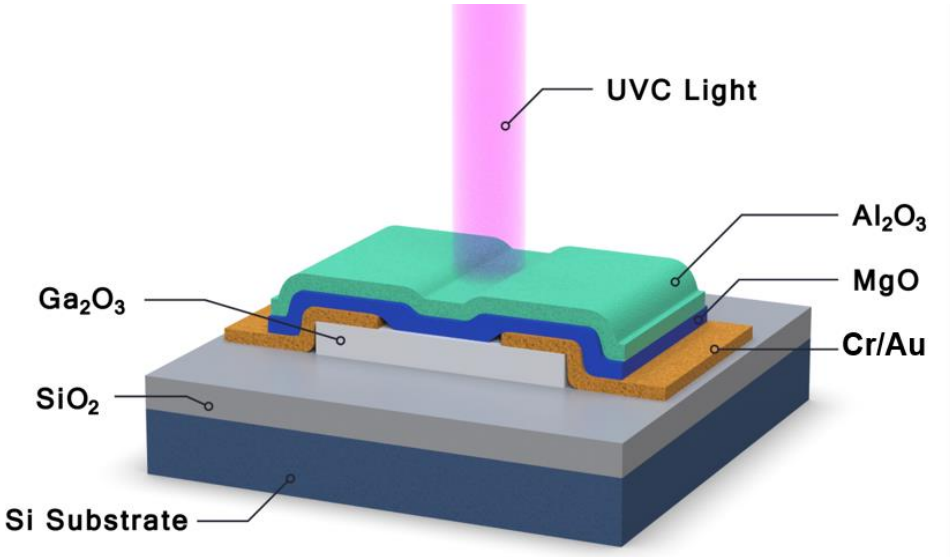

Figure 2.1 Schematic illustration of the bilayer passivated β-Ga_2O_3 phototransistor.

Figure 2.1 shows the configuration of the β-Ga_2O_3 phototransistor, which included a charge transfer layer (MgO) and an encapsulation layer (Al_2O_3). Here, the β-Ga_2O_3 films were mechanically exfoliated from a single-crystal (−201) bulk β-Ga_2O_3 substrate (Tamura Corp., Japan) and transferred onto a Si/SiO_2 substrate. The highly-doped Si substrate was used to apply the gate voltage to the β-Ga_2O_3 channel through the SiO_2 dielectric layer. The source (*S*) and drain (*D*) electrodes (Cr/Au 20/80 nm) were deposited and patterned by thermal evaporation following a photolithography process. Then, MgO (30 nm) and Al_2O_3 (20 nm) were deposited by RF magnetron sputtering at room temperature. The Al_2O_3 encapsulation layer prevents a degradation of the MgO layer by water molecules due to a hygroscopic nature of the MgO layer.[16,17] Figure 2.2a shows a scanning electron microscope (SEM) image of the fabricated β-Ga_2O_3/MgO

phototransistor. I also fabricated a reference β-Ga_2O_3 phototransistor with nearly identical dimensions and channel thickness to investigate the effects of the MgO layer.

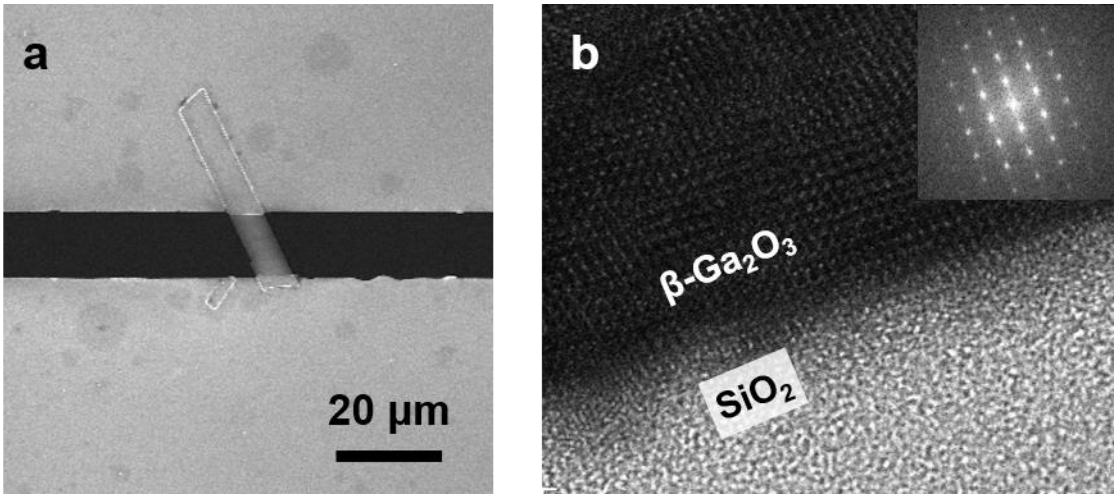

Figure 2.2 **a** Optical microscope image of the fabricated β-Ga_2O_3 phototransistor. Scale bar: 20 µm. **b** High resolution TEM image of the β-Ga_2O_3/SiO_2 interface. Scale bar: 5 nm Inset: Corresponding FFT patterns of β-Ga_2O_3 region.

Material properties of the exfoliated β-Ga_2O_3 and MgO/Al_2O_3 layers in the fabricated device were studied by using HR-TEM and an EDX mapping. Cross-sectional HR-TEM images were obtained over the SiO_2/β-Ga_2O_3/MgO/Al_2O_3 cross-sectional interface (Figure 2.2b; see Figure 2.3 for MgO). A fast Fourier transform (FFT) micrograph of the β-Ga_2O_3 HR-TEM image indicates the high crystal quality of the exfoliated β-Ga_2O_3 film (inset of Figure 2.2b). Moreover, Figure 2.4a shows a cross-sectional TEM image and the corresponding TEM-EDX maps of the device, where four elemental species (Al, Mg, Ga, and O) are displayed as four different colors (green, cyan,

magenta, and red). The TEM-EDX maps clearly reveal that the MgO and Al_2O_3 layers were uniformly deposited on top of the β-Ga_2O_3 layer.

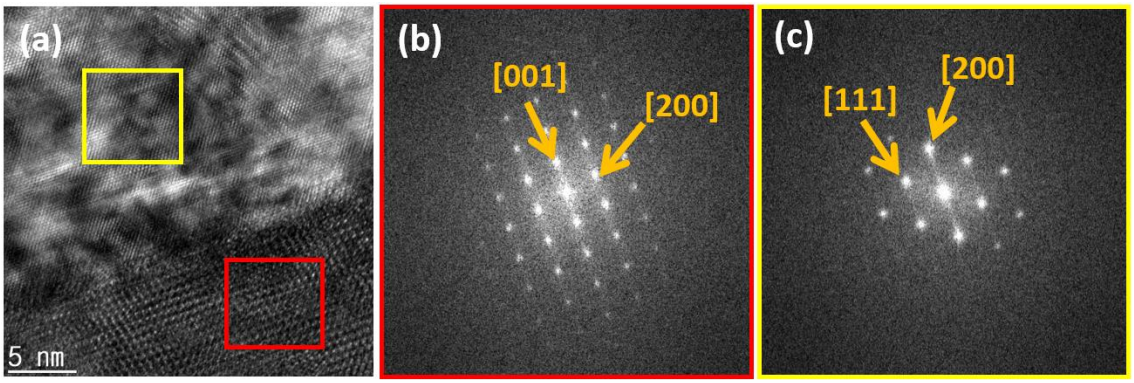

Figure 2.3 **a** A cross-sectional HR-TEM image of the β-Ga_2O_3/MgO channel. **b** FFT of the red square area (β-Ga_2O_3) in the HR-TEM image shows periodicity value d = 0.58 nm and 0.61 (=1.22/2) nm, confirming the (100) surface orientation. **c** FFT of the yellow highlighted area (MgO) showing periodicity value d = 0.21 nm and 0.24 nm.

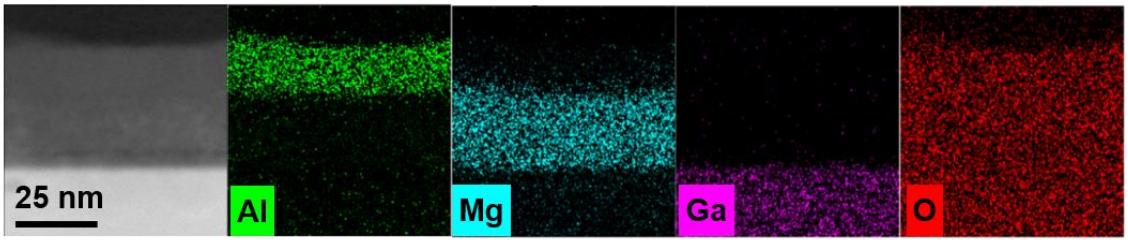

Figure 2.4 EDX elemental mapping of four chemical species (Al, Mg, Ga, and O). Scale bar: 25 nm

2.3 Characterization of β-Ga_2O_3/MgO heterojunction phototransistor

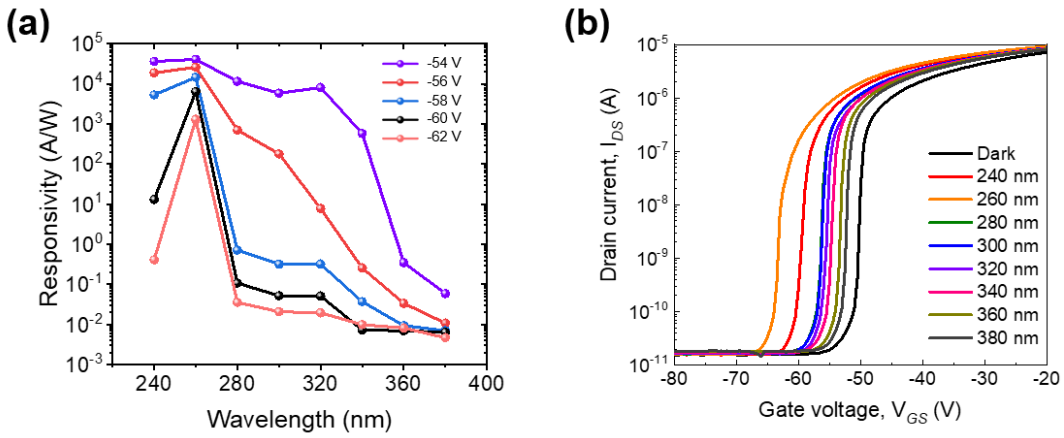

Figure 2.5. Spectral responsivity of the β-Ga_2O_3-based phototransistors at V_{DS} = 1 V. (a) Responsivity spectra at various applied gate voltages from -54 V to -62 V. (b) The transfer characteristics under light illumination at various wavelengths from 240 nm to 380 nm.

The β-Ga_2O_3 phototransistor exhibits various spectral responses depending on the applied gate bias. Figure 2.5a presents the responsivity spectra in the β-Ga_2O_3 phototransistor with various applied gate biases. This phenomenon occurs because the photogating effect, which shifts the threshold voltage under light illumination, plays an important role in both β-Ga_2O_3 and β-Ga_2O_3/MgO devices. Depending on the wavelength of light, the amount of V_{TH} shift is different as shown in Fig. 2.5b. When the shifted V_{TH} of phototransistor under illumination is higher than the applied gate voltage (V_{GS}) ($V_{TH,\ light} > V_{GS,}$ where $V_{TH,\ light}$ means a shifted V_{TH} under light illumination), the responsivity is very low because there is no huge difference between $I_{light}(V_{GS})$ and $I_{dark}(V_{GS,})$. On the other hand, When the shifted V_{TH} of phototransistor under illumination becomes lower

than an applied gate voltage ($V_{TH,\ light} < V_{GS}$), the responsivity exceptionally increases since the difference between I_{light} ($V_{GS,\ applied}$) and I_{dark} ($V_{GS,\ applied}$) corresponds to ($I_{ON,\ dark}$ - $I_{OFF,\ dark}$) of the phototransistor, where $I_{ON,\ dark}$ and $I_{OFF,\ dark}$ are on-state current and off-state current of phototransistor under dark, respectively. Therefore, the phototransistors can be used for either broadband UV photodetector of 240-340 nm or solar-blind UV-C light photodetector (260 nm).

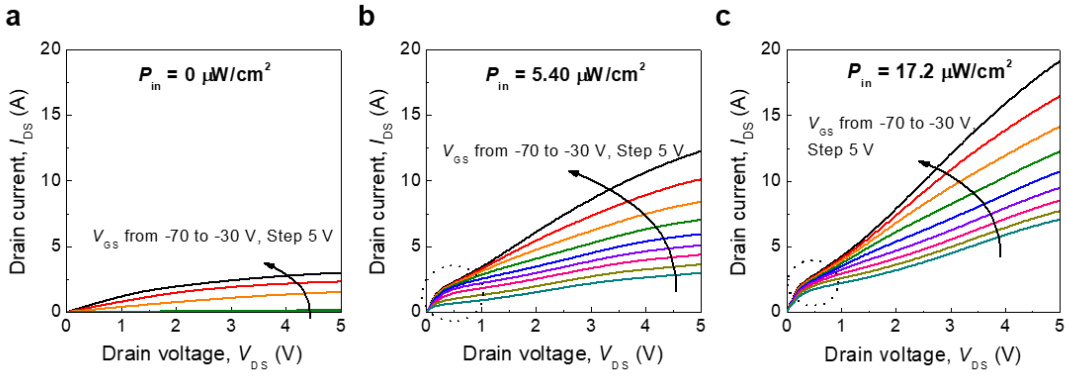

Figure 2.6 **a-c** I_{DS}-V_{DS} characteristics of the β-Ga_2O_3 phototransistor without a passivation layer with various VGS ranging from -70 V to -30 V in step of 5 V under (**a**) dark and 260 nm DUV light illumination of (**b**) 5.40 μW/cm^2 and (**c**) 17.2 μW/cm^2.

Figure 2.6a-c shows the output characteristics (I_{DS}-V_{DS}) of the reference β-Ga_2O_3 device for gate biases (V_{GS}) ranging from −70 V to −30 V at steps of 5 V, under dark conditions and 260 nm DUV light illumination of 5.4 μW/cm^2 or 17.2 μW/cm^2. I set the wavelength of DUV light at 260 nm, in which the photon energy is slightly larger than bandgap of β-Ga_2O_3, in this work for simplicity of experiment. The I_{DS}-V_{DS} curves of the β-Ga_2O_3 device under dark conditions exhibit the typical linear and saturation

characteristics of thin-film transistors (TFTs) (Fig. 2.6a). However, the output curves of the reference device under DUV light deviate from this behavior, exhibiting a hump in the low V_{DS} region (V_{DS} < 1 V) (black dotted circles in Fig. 2.6b,c).[18] The hump implies that two distinct charge transport mechanisms in the β-Ga_2O_3 channel concurrently contribute to the conduction of carriers. It has been known that the back-channel surface of metal-oxide semiconductor-based TFTs provides an additional conduction channel that is not controlled by a gate bias, thereby increasing dark current and reducing photoresponsivity.[19,20] This back-channel conduction possibly originates from photo-adsorption/desorption of oxygen species from the atmosphere,[20] as the back-channel effect is only observed in the reference β-Ga_2O_3 device in which the surface is exposed to the ambient air.

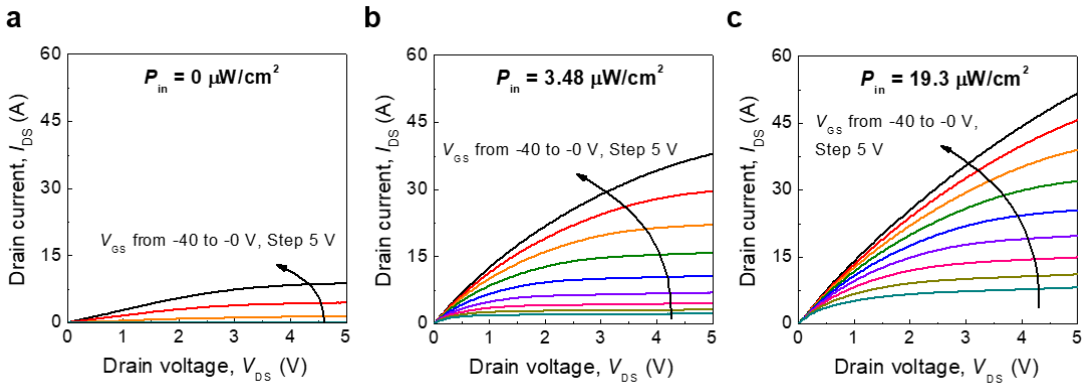

Figure 2.7 **a-c** I_{DS}-V_{DS} characteristics of the β-Ga_2O_3 phototransistor with a passivation layer with various V_{GS} ranging from -40 V to 0 V in step of 5 V under (**a**) dark and 260 nm DUV light illumination of (**b**) 3.48 μW/cm^2 and (**c**) 19.3 μW/cm^2

To suppress the back-channel surface effects, I introduce the β-Ga_2O_3/MgO heterostructure-based phototransistor with a Al_2O_3 encapsulation layer. Figure 2.7a-c presents the linear and saturation output characteristics of the β-Ga_2O_3/MgO phototransistor under dark conditions, as well as under 3.48 μW/cm^2 and 19.3 μW/cm^2 light illumination. I attribute the suppression of the back-channel conduction in the β-Ga_2O_3/MgO device to defect-assisted charge transfer, which will be discussed in more detail in a later section.

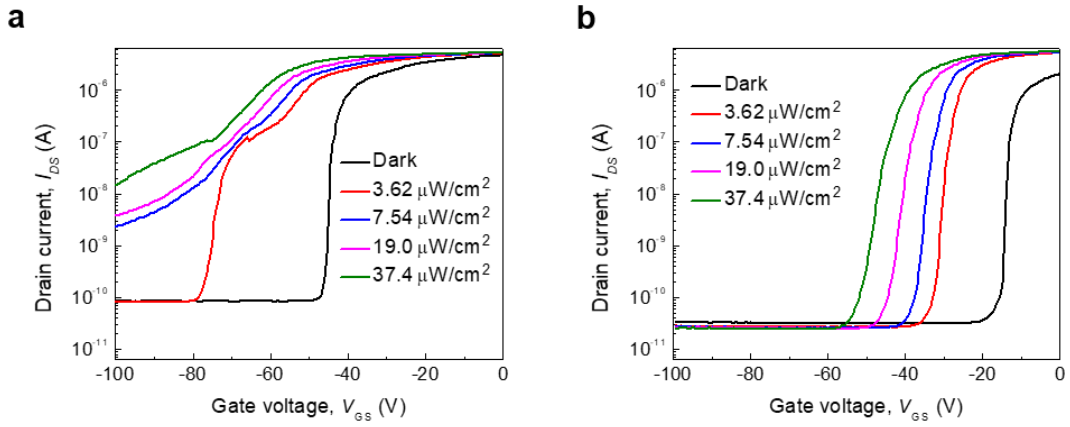

Figure 2.8 **a,b** Transfer characteristics of (**a**) the β-Ga_2O_3 and (**b**) β-Ga_2O_3/MgO phototransistor. V_{DS} was fixed at 1 V.

Figure 2.8a,b shows transfer characteristics of the β-Ga_2O_3 and β-Ga_2O_3/MgO phototransistors, respectively, at V_{DS} = 1 V under DUV light illumination. The threshold voltage (V_{TH}) difference of ~ 30 V between the β-Ga_2O_3 and β-Ga_2O_3/MgO devices is attributed to a slight thickness difference of β-Ga_2O_3 layers in those devices since a V_{TH} of β-Ga_2O_3 transistors sensitively depends on a thickness of β-Ga_2O_3 layer.[21] In the β-Ga_2O_3 phototransistor, a light-induced hump appears when the gate bias is lower than V_{TH}.

This hump is observed because the photoconductive and photogating effects concurrently occur in the β-Ga_2O_3 phototransistors under light illumination. Although a weak photoconductive effect is measured at highly negative gate biases ($V_{GS} < -80$ V) under weak light illumination ($P = 3.48$ μW/cm^2) due to oxygen vacancy defect trapping, the coexistence of the photoconductive and photogating effects is evidenced by the two different rising slopes that exist in the transfer curves. On the other hand, only the photogating effect contributes to photocurrent generation in the β-Ga_2O_3/MgO phototransistor, which means no photocurrent arises from photoconduction when $V_{GS} < V_{TH}$. By eliminating the photoconductive effect, the recombination of photogenerated electron–hole pairs is effectively suppressed, enabling ultrahigh photoresponsivity solely by means of the photogating effect.[9,22,23]

2.4 β-Ga_2O_3/MgO phototransistor operation mechanism

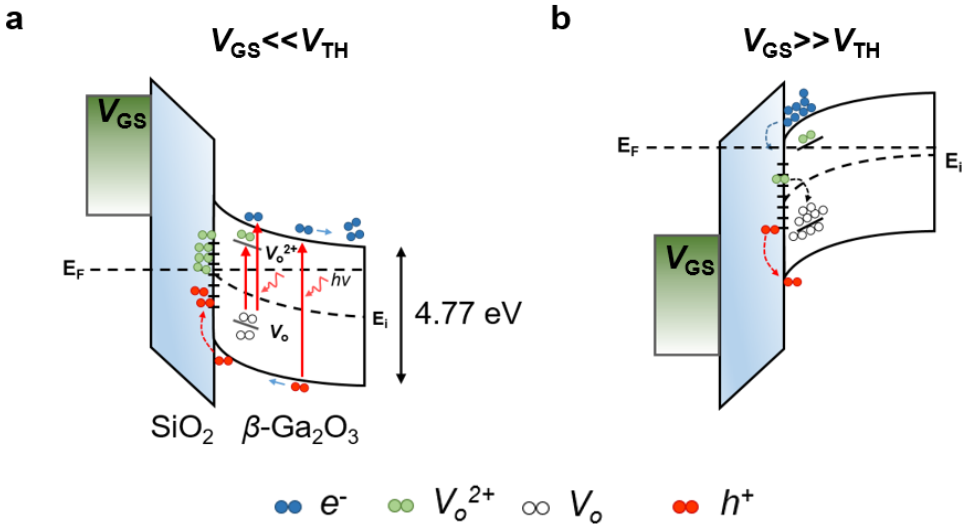

Figure 2.9 **a,b** Schematic illustration of the mechanism of the unpassivated β-Ga_2O_3 phototransistor. (**a**) When the DUV light is illuminated on the device under a negative gate bias, holes and ionized oxygen vacancies are trapped in the SiO_2/β-Ga_2O_3 interface while photogenerated electrons remain on the back-channel surface. (**b**) When a positive bias is applied to the β-Ga_2O_3 unpassivated phototransistor, the electrons are injected to the SiO_2/ β-Ga_2O_3 interface, releasing the trapped holes and oxygen vacancies.

To explain the suppression of the photoconductive effect in the β-Ga_2O_3/MgO heterostructure device, I propose a defect-assisted charge transfer model. Figure 2.9a,b displays a schematic illustration of processes involving photogenerated charge carriers for the β-Ga_2O_3 and the β-Ga_2O_3/MgO devices, respectively, when the applied gate bias voltage is either much lower or much higher than the threshold voltage (V_{GS}<<V_{TH} or V_{GS}>>V_{TH}). The drawn band diagram is based on literature values.[24–26] When photons

with above-bandgap energies illuminate the phototransistor, an absorbed photon causes the creation of a free electron-hole pair as well as the ionization of an oxygen vacancy (V_o), generating two free electrons in the conduction band ($V_o + h\nu \rightarrow V_o^{2+} + 2e^-$).[27] In the β-Ga_2O_3 phototransistor, when V_{GS} is less than V_{TH}, photogenerated holes and ionized oxygen vacancies are attracted to the SiO_2/β-Ga_2O_3 interface, while photogenerated electrons are attracted to the back-channel surface (Fig. 2.9a). The drifting photogenerated holes and oxygen vacancies become localized by deep interfacial trap states, inducing a negative V_{TH} shift (i.e., the photogating effect).[9,22,23] At the same time, the remaining photogenerated electrons in the conduction band flow to the drain electrode, resulting in photocurrent at the below-threshold gate voltage (i.e., the photoconducting effect),[9,22,23] while some of the electrons recombine with holes, reducing the photoresponsivity. When $V_{GS}>>V_{TH}$, electrons are injected at the SiO_2/β-Ga_2O_3 interface, and the injected electrons deionize the ionized oxygen vacancies and combine with the trapped holes (Fig. 2.9b). Subsequently, the shift in threshold voltage is recovered. This conceptual mechanism also explains the evolution of the β-Ga_2O_3 phototransistor operation under light illumination and varying gate bias voltage, which will be discussed in Fig. 2.11.

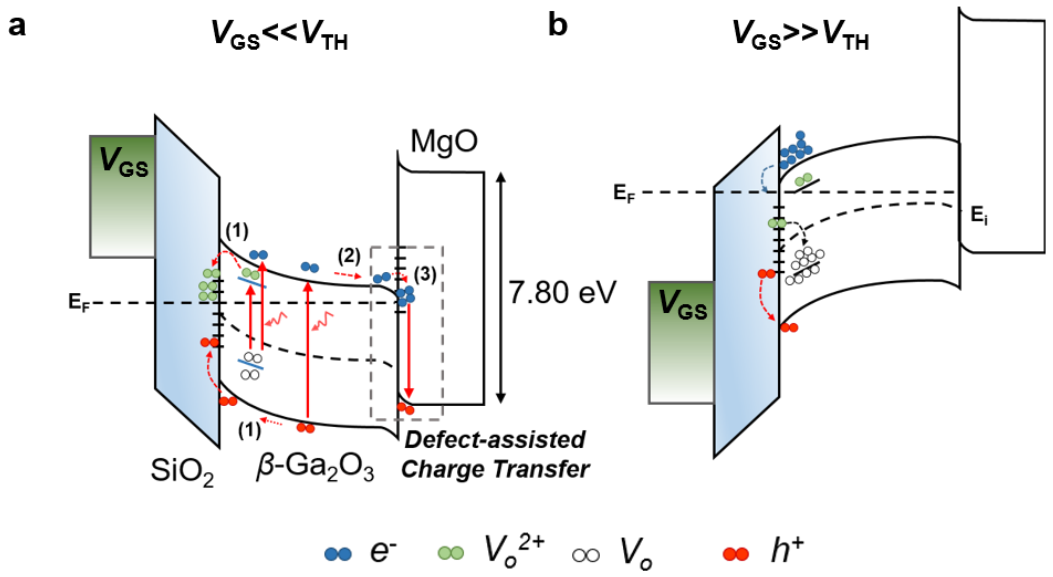

Figure 2.10 **a,b** Schematic illustration of the mechanism of the passivated β-Ga_2O_3 phototransistor. (**a**) When the DUV light is illuminated on the passivated β-Ga_2O_3 phototransistor, When the DUV light is illuminated on the device under a negative gate bias, holes and ionized oxygen vacancies are trapped in the SiO_2/β-Ga_2O_3 interface, but the photogenerated electrons are transferred to the MgO layer by a defect-assisted charge transfer process. (**b**) When a positive bias is applied to the β-Ga_2O_3 passivated phototransistor, the trapped positive charges are released as same as the unpassivated device.

While the overall mechanism for the β-Ga_2O_3/MgO heterostructure phototransistor is similar to that of the β-Ga_2O_3 phototransistor, I assume that the defect-assisted charge transfer takes place at the β-Ga_2O_3/MgO interface under light illumination (Fig. 2.10a), which increases the photoresponsivity by suppressing electron-hole recombination and back-channel conduction at the off state of the phototransistor. When

V_{GS} is less than V_{TH}, the photogenerated holes and ionized oxygen vacancies migrate to the SiO_2/β-Ga_2O_3 interface (process (1) in Fig. 2.10a) and the photogenerated electrons drift toward the β-Ga_2O_3 back-channel surface (process (2) in Fig. 2.10a), where they are trapped by interfacial oxygen defect states at the SiO_2/β-Ga_2O_3 and β-Ga_2O_3/MgO junctions, respectively. Meanwhile, the trapped electrons are recombined with holes in MgO layer by defect-assisted non-radiative recombination process (process (3) in Fig. 2.10a), resulting in the transfer of the photogenerated electrons in β-Ga_2O_3 to the MgO layer (defect-assisted charge transfer).[28] Consequently, the β-Ga_2O_3/MgO device functionally mitigates photogenerated electron-hole pair recombination and back-channel conduction in the β-Ga_2O_3 channel layer at the transistor off state, enabling the observed ultrahigh responsivity and high specific detectivity (to be discussed in Section 2.5). When V_{GS} is greater than V_{TH} (Fig. 2.10b), the operation mechanism is nearly identical with the β-Ga_2O_3 device without the MgO layer.

2.5 β-Ga_2O_3/MgO phototransistor memory operation

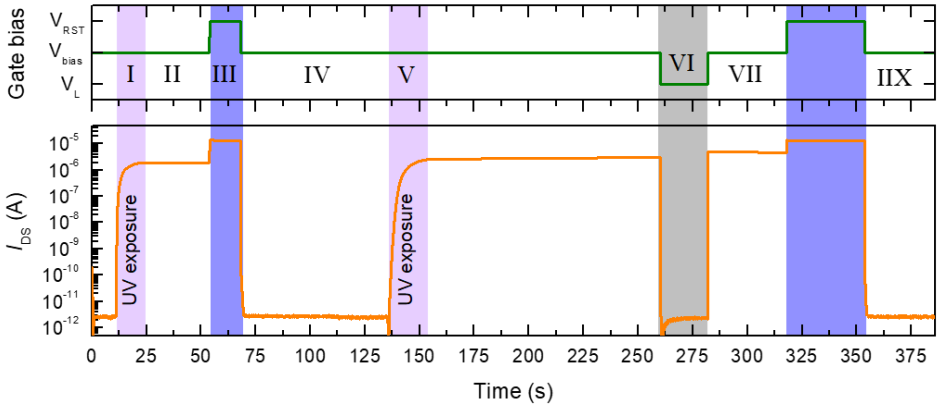

Figure 2.11**.** Comprehensive transient response of the passivated β-Ga_2O_3 phototransistor applying various gate voltage pulses. The measurement is conducted under fixed V_{DS}= 1 V, Irradiance = 5 .4 μW/cm^2. V_{RST}=33 V, V_{bias} = -36 V, and V_L = -69 V.

Figure 2.11 shows the time-resolved photoresponse of the β-Ga_2O_3/MgO phototransistor under a drain bias of 1 V, in which DUV light of an irradiance of 5.4 $\mu W/cm^2$ is used for the light-on state during the measurement. When the light is on for 10 s under a gate bias of V_{bias} = −36 V (= V_{TH} −17 V), I_{DS} increases as the holes and ionized oxygen vacancies are trapped at the SiO_2/β-Ga_2O_3 interface, leading to the observed negative V_{TH} shift (I). After the light is turned off, the photocurrent is stable during the extremely slow recovery time, which is the so-called persistent photocurrent (PPC) (II).[27,29] PPC is commonly observed in oxide TFTs under UV light illumination due to the slow decay time of the oxygen vacancy defect states, and it prohibits a photodetector from exhibiting fast photocurrent response. Hence, PPC is usually very desirable to implement optoelectronic memory.[30,31] To circumvent the restriction of the slow photoresponse, a positive gate bias voltage pulse (PBP, V_{RST} = 33 V = V_{TH} + 50 V) is applied to quickly suppress the PPC (III). When the PBP is applied, electrons in the channel are injected at the SiO_2/β-Ga_2O_3 interface, recombining the trapped holes and ionized oxygen vacancies with the electrons and returning the shifted V_{TH} to the initial value (IV). On the other hand, when a negative gate bias of −69 V (= V_L = V_{TH} − 50 V) is applied to the phototransistor (VI), photogenerated holes and ionized oxygen vacancies from another 10 s DUV light illumination (V_{GS} = V_{bias}) (V) remained trapped. Although the phototransistor appears to recover to the initial state while the negative gate bias is being applied, the removal of the negative gate bias restores the device to the on state (VII) since the trapped positive charges have not been released (Figs. 2.9a and 2.10a). In fact, the drain current slightly increases after the negative gate bias is applied because extra positive charges are injected at the SiO_2/β-Ga_2O_3 interface. After these phenomena,

the application of another PBP completely recovers the shift in V_{TH} (IIX). The comprehensive transient responses detailed here support the model, which is depicted in Figs. 2.9a and 2.10a.

2.6 Ultrahigh responsivity in the β-Ga_2O_3 phototransistor

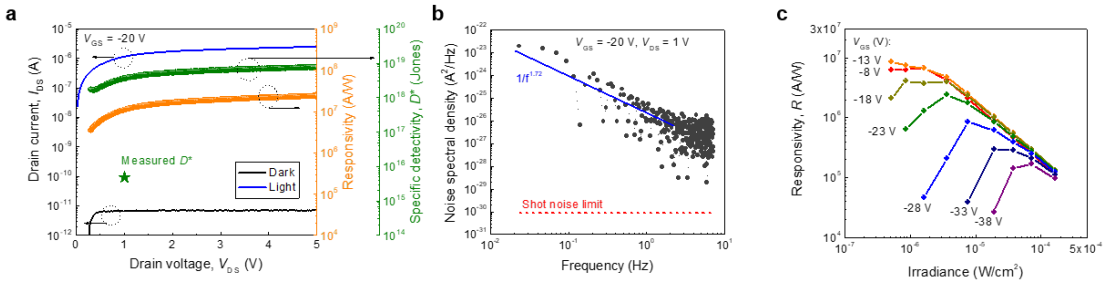

Figure 2.12 **a** Dependence of responsivity and specific detectivity on drain voltage (at V_{GS} = -20 V) under light illumination of 0.51 μW/cm^2. The I_{DS} curves under the dark and the light illumination are also plotted to aid understanding. **b** The noise spectral density of dark current at V_{GS} = −20 V and V_{DS} = 1 V. **c** Responsivity as a function of incident irradiance under different applied gate voltages (V_{DS} =1 V).

Based on the above discussion, the β-Ga_2O_3/MgO phototransistor is expected to exhibit outstanding performance with high photosensitivity. The responsivity (R) and the specific detectivity (D^*) of phototransistors are key parameters for evaluating the photosensitivity and detection capability, respectively, toward low-level light in a photodetector. For further characterization of the phototransistor, the responsivity and the specific detectivity are characterized under various V_{DS}, V_{GS}, and irradiance conditions. The responsivity is given by $R = I_{ph}/(PA)$, where P and A are the incident light power and

the effective illuminated area of the device, respectively, and the specific detectivity can be expressed as $D^* = (A \cdot BW)^{1/2}/NEP$, where BW is the bandwidth and NEP is the noise-equivalent power. When I assume the major factor of the noise of the phototransistor is dominated by the shot noise, the specific detectivity can be expressed ad $D^* = R \cdot A^{1/2}/(2eI_{dark})^{1/2}$, where e is the electron charge. Therefore, the responsivity and the specific detectivity can be calculated using the measured I_{ph} and I_{dark}. Figure 2.12a shows the responsivity and specific detectivity as a function of V_{DS} (at $V_{GS} = -20$ V) under 0.51 μW/cm^2 light illumination. The I_{DS} curves under dark conditions and light illumination are also plotted to aid understanding. Both R and D^* obviously increase with increasing V_{DS} due to the increase of I_{ph}, and they saturate at high V_{DS}, where R and D^* are 2.1×10^7 A/W and 1.8×10^{15} Jones, respectively, at $V_{DS} = 5$ V (Fig. 2.12a). The shot noise limited D^* is prone to overestimate the performance because other noise components are not considered. Thus, a noise analysis of dark current is beneficial to precisely predict a specific detectivity. Figure 2.12b shows the noise spectral density of dark current at $V_{GS} = -20$ V and $V_{DS} = 1$ V. It turns out that the flicker noise proportional to $1/f^{1.72}$ prevails in the noise spectrum. The rms (root mean squared) value of the noise current up to $BW = 1$ Hz was 1.11 pA, corresponding to D^* of 4.9×10^{15} Jones. The measured D^* determined by the noise analysis was three order magnitude lower than the shot noise limited D^* as shown in Fig. 2.12a. Nevertheless, the measured D^* of ~ 10^{15} is still unprecedentedly high value. Figure 2.12c shows the responsivity as a function of the irradiance under different applied gate voltages. Since the photogating effect is predominantly attributed to the generation of photocurrent by the shift in V_{TH}, the responsivity increases with increasing irradiance until the effective threshold voltage

($V_{TH,eff} = V_{TH} + \Delta V_{TH}$) is equal to the applied gate voltage. When $V_{TH,eff}$ is higher than the applied gate voltage, the responsivity decreases with increasing light intensity. This decrease could be caused by absorption saturation, as well as by enhanced scattering and/or recombination rates associated with high irradiance.

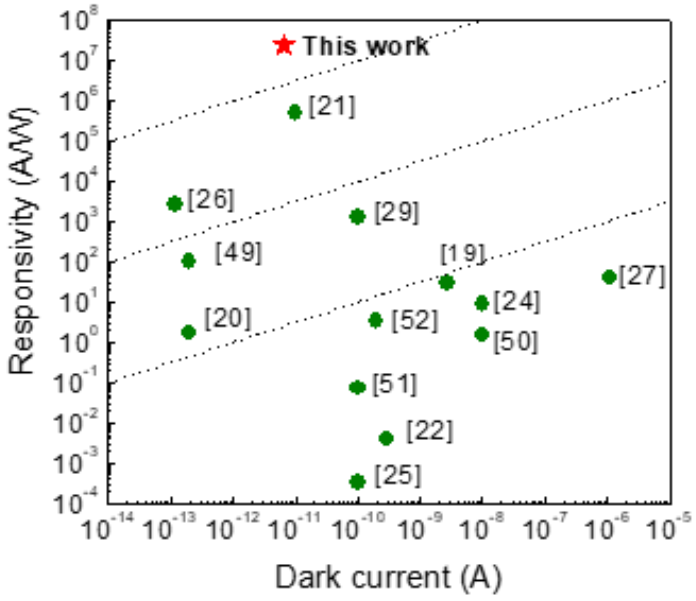

Figure 2.13 Responsivity and dark current of several state-of-the-art of β-Ga_2O_3-based phototransistors.[10,11,37–39,13–15,32–36]

On the basis of the analyzed characteristics of the β-Ga_2O_3/MgO phototransistor, I obtain ultrahigh values of $R = 2.4 \times 10^7$ A/W and $D^* = 1.7 \times 10^{15}$ Jones at $V_{DS} = 5$ V, $V_{GS} = -20$ V, and $P = 0.51$ μW/cm^2 in the β-Ga_2O_3/MgO device. It should be noted that, to the best of my knowledge, these achieved values are almost two orders of magnitude higher than the best previously reported values for β-Ga_2O_3-based photodetectors.[15] To provide a clear comparison, I have summarized the responsivities and dark current values

for several previously reported β-Ga_2O_3 photodetectors based on exfoliated β-Ga_2O_3, MBE- or MOCVD-grown β-Ga_2O_3, and graphene/β-Ga_2O_3 heterostructures (Figure 2.13 and Table 2.1).[10,11,37–39,13–15,32–36]

Table 2.1. Reported values for dark current, responsivity, and specific detectivity in β-Ga_2O_3-based photodetectors

Materials	Dark current (A)	Responsivity (A/W)	Detectivity (Jones)	Ref.
β-Ga_2O_3 flakes	6.7×10^{-12}	2.3×10^{7}	1.7×10^{15}	This work
β-Ga_2O_3 flakes	2.77×10^{-9}	29.8	1.45×10^{12}	[19]
β-Ga_2O_3 flakes	2×10^{-13}	1.68	3.73×10^{10}	[20]
β-Ga_2O_3 flakes	9.91×10^{-12}	4.79×10^{5}	6.69×10^{14}	[21]
MBE-grown β-Ga_2O_3	3×10^{-10}	4×10^{-3}	-	[22]
β-Ga_2O_3 substrate	1×10^{-8}	8.7	-	[24]
MOCVD-grown β-Ga_2O_3	1×10^{-10}	3.2×10^{-4}	2.8×10^{10}	[25]
Graphene/β-Ga_2O_3 flakes	1.2×10^{-13}	2.6×10^{3}	9.7×10^{13}	[26]
Graphene/β-Ga_2O_3 wafer	1.1×10^{-6}	39.3	2.24×10^{12}	[27]
ZnO-Ga_2O_3 core-shell	1×10^{-10}	1.3×10^{3}	9.91×10^{14}	[29]
Ga_2O_3 nanobelt	2×10^{-13}	$\sim10^{2}$	-	[49]
MBE grown β-Ga_2O_3	1×10^{-8}	1.5	-	[50]
β-Ga_2O_3/SiC	1×10^{-10}	7×10^{-2}	-	[51]
2D β-Ga_2O_3nano sheet	2×10^{-10}	3.3	4.0×10^{12}	[52]

2.7 Conclusions

In summary, I have demonstrated a β-Ga_2O_3/MgO heterostructure-based DUV phototransistor with an Al_2O_3 encapsulation layer, exhibiting ultrahigh light sensitivity. The material properties were characterized by HR-TEM and TEM-EDX mapping, confirming the highly crystalline quality of the β-Ga_2O_3. I studied the β-Ga_2O_3 and β-

Ga_2O_3/MgO phototransistors under 260 nm light illumination and compared the β-Ga_2O_3/MgO device to the β-Ga_2O_3 device to clarify the role of the MgO layer. The MgO layer effectively suppressed the photoconductive current in the subthreshold region and enhanced a photogating effect by defect-assisted charge transfer at the β-Ga_2O_3/MgO interface. Due to this charge transfer, the recombination of photogenerated electrons and holes is inhibited, contributing to the enhancement of the photogating effect and the photocurrent. As a result, I are able to achieve the highest responsivity (2.3×10^7 A/W) and specific detectivity (1.7×10^{15} Jones) of any reported β-Ga_2O_3 photodetection device. This β-Ga_2O_3/MgO heterostructure configuration in the demonstrated β-Ga_2O_3/MgO heterostructure phototransistor will provide a promising way for the development of ultrasensitive DUV photodetectors utilizing oxide-based wide-bandgap materials.

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Chapter 3

In-sensor image memorization and encoding for visual cognitive processing

3.1 Introduction

Machine vision technology provides the capability to inspect and analyze the surrounding environment using image sensors integrated with processing units.[1–4] Recent advances of various image sensing and artificial intelligence (AI) technology have enabled to efficiently generate digital images from the physical world and to interpret the acquired images, respectively. A key feature of machine vision is real-time object recognition and/or classification via machine learning using an artificial neural network (ANN) inspired by the visual reasoning process of mammalian.[5] Therefore, machine vision has been widely employed in applications that require in-situ sensing, environment analysis and interpretation of visual images such as autonomous vehicles, robotics, smart production systems etc.[1,6–8]

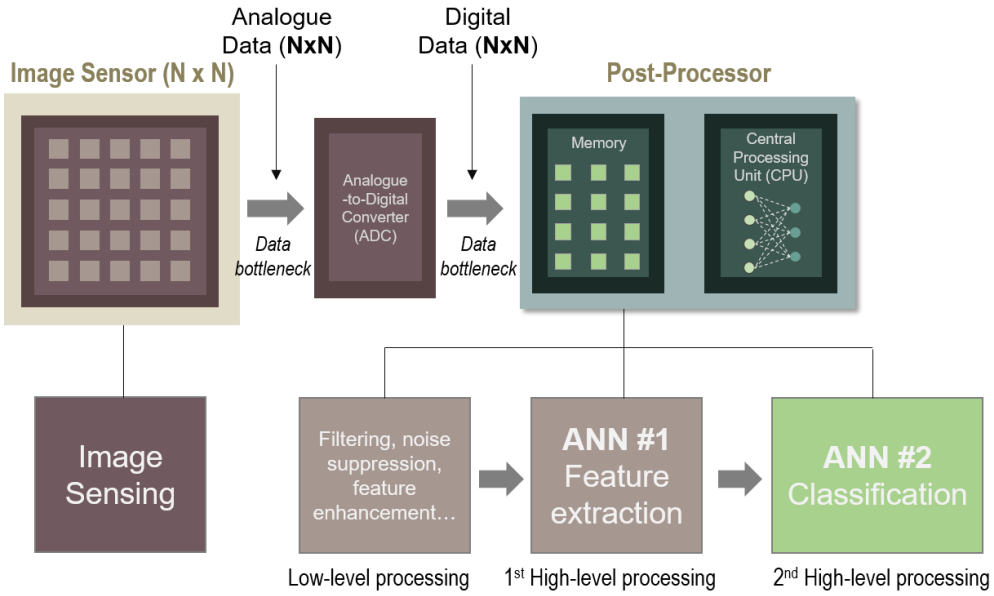
In conventional machine vision systems, the image sensors are externally connected with the memory and processing units by adapting von Neumann computing architectures (Fig. 3.1). Sensing occurs in the analogue domain that usually leads to generate vast amounts of raw data at the image sensor. The huge amounts of redundant analogue data including unnecessary background information have to be converted to digital data via analogue-digital-converter (ADC), then transferred to processing units or

cloud-based computing systems[6,9], in which the image processing and analysis are conducted for machine vision applications. Thus, this sensory data processing requires energy-hungry long-distance data communication from the sensors to memories and processing units with a limited data transfer rate.[1,6,10] These massive amounts of data conversion/transportation cause significant issues in terms of energy consumption, delayed response-time, and communication bandwidth, all of which are particularly important for machine vision applications with strict delay and power-consumption requirements. Therefore, this data transportation bottleneck issue in the integrated sensor and processor system should be mitigated for fast and efficient machine vision processes.

In contrast, the human vision system outperforms conventional imager and machine vision systems especially with regard to unstructured image classification and recognition, low-latency, and energy efficiency[6]. The human retina detects images with rod and cone photoreceptors and conveys the images through the optic nerve to the brain, then the cortex processes the collected information for visual perception. Interestingly, much of the image process already begins in a neural circuit within the retina[11–13]. The retina compresses the large volume of visual signals detected by approximately 100 million photoreceptor cells, and then transmits the encoded data to the brain without latency and significant energy consumption via the optic nerve. This in-retina computation mechanism can be effectively applied to machine vision systems to alleviate the data transportation bottleneck issues at the sensor/processor interface due to the big data acquisition at the sensor nodes as well as heavy computation burden and reliance on the post-processor.

Analogous to the neural circuit and photoreceptor cells in the retina, photodetectors in the image sensors can be directly integrated with artificial synapse (e.g., oxide memristors, phase change memories, etc.), constructing an artificial neural circuit.[14–16] Integrated analog computing units can store image information as resistance states simultaneously performing the computational tasks to implement an ANN for a cognitive algorithm. Thereby so-called "in-sensor computing," the image information can be processed within the sensors, largely reducing data movement by processing it at the edge of the system in a similar way to mammalian vision (Fig. 3.1).[1,6] There have been efforts to demonstrate in-sensor computing systems for analogue machine vision by using optoelectronic memory devices. However, the previously demonstrated in-sensor machine vision systems mostly conducted an image memorization and an image pre-processing (e.g. image enhancement) within the sensors.[2,3,25,17–24] Thus, the entire image data still needed to be transferred to a back-end post-processor for the high-level image processing, such as feature extraction, image encoding, and image classification. However, minimizing unnecessary data transportation between the sensor, memory, and computation unit is the key features and the ultimate goals of in-sensor computing to achieve an energy efficient and latency-free sensor/processor system. As such, advanced in-sensor computing systems require capabilities to memorize images and to directly perform high-level image processing within the sensor.

Conventional architecture



Computational optoelectronic synaptic memory

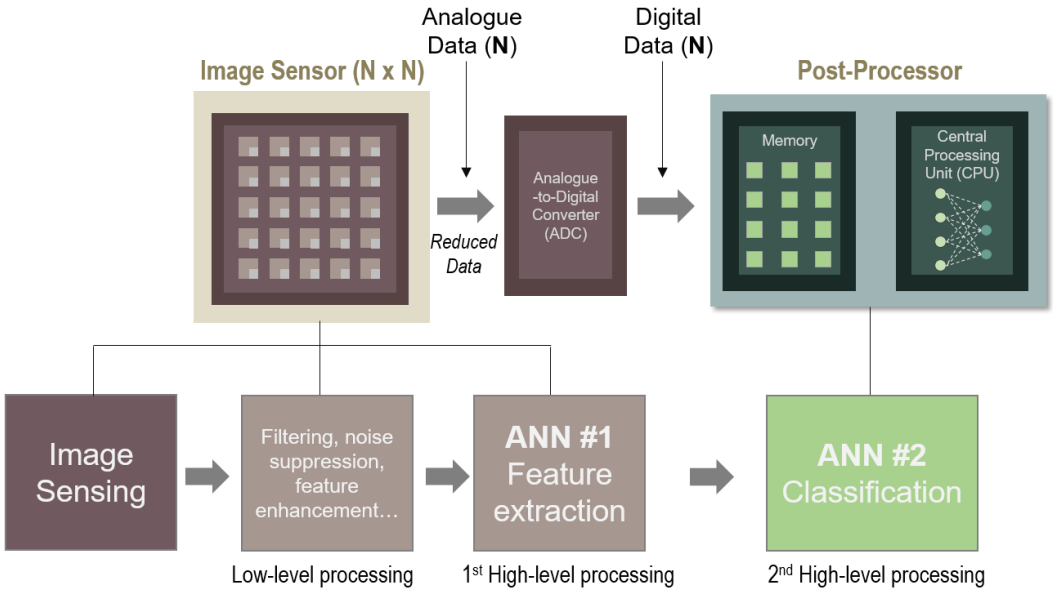


Figure 3.1. Image data collection and processing architecture in a conventional image sensor and a proposed computational optoelectronic synaptic memory.

In this work, I have developed an advanced in-sensor computing system with neuromorphic image memorization and encoding capabilities within the pixel for visual cognitive processing emulating the biological visual processing system of the mammalian retina. This in-pixel computing system efficiently computes and conveys visual information to minimize a data transportation bottleneck. In the single sensor, a photodiode is directly integrated with a resistive random access memory (ReRAM) to construct 1-photodiode 1-resistive random access memory (1P-1R) pixels, where HfO_2-based ReRAMs are fabricated on InGaAs-based p-i-n photodiodes. I first fabricated the 1P-1R single pixel with an InGaAs photodetector and a HfO_2-based ReRAM, and characterized the electrical and optoelectrical properties for the image memorization and data processing of visual information within the sensor. Then, a 16×16 1P-1R crossbar array with InGaAs photodiode and HfO_2-based ReRAM was fabricated and characterized. Subsequently, imaging of MNIST handwritten digits was performed, where the visual stimuli of the images were effectively stored in the pixels. Then, using the fabricated 1P-1R array, bio-mimicking image encoding process was performed by in-memory vector-matrix-multiplication without data transfer. Contrary to typical in-memory computing manners, input image data were stored in ReRAMs and weights were applied to the crossbar array as input voltages, in which 2D-1D vectorization was no longer needed and the size of the crossbar array was significantly reduced. Then, the encoded images were conveyed to a central processor for the image classification process. My process dramatically reduces redundant data movement between the sensor, memory, and processor by performing in-pixel encoding, possibly alleviating a data transportation bottleneck and energy overconsumption issues.

3.2 In-sensor computing system emulating human vision system

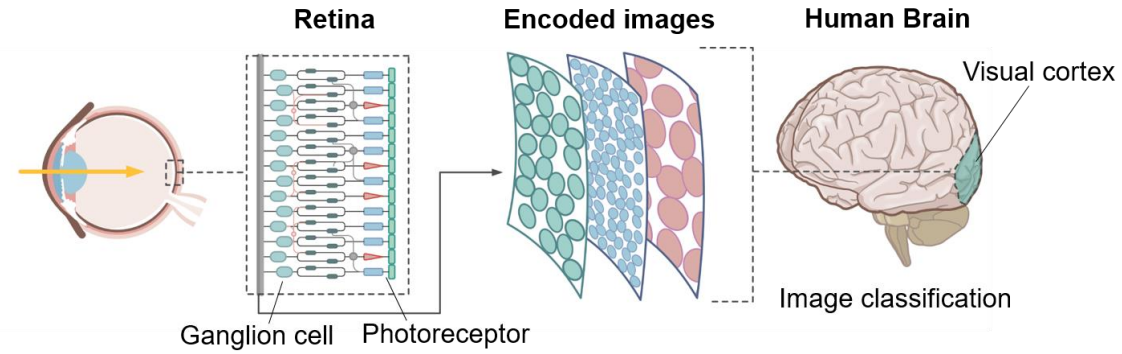


Figure 3.2 Schematic illustration of human vision system from the retina to the brain, and its visual cognitive processing with in-retina image encoding process

Figure 3.2a shows a schematic illustration of image encoding and classification process in the mammalian retina and brain system. The outputs of the rod and cone photoreceptors are decomposed into approximately 12 parallel information streams, and then these streams are connected to the retinal ganglion cells. Bipolar and amacrine cell activity is combined in a ganglion cell to create the diverse encodings of features extracted from the visual world such as edges, direction, and color, and then the retina transmits this pre-processed data to the brain[11–13]. By reducing redundant information, the retina can effectively convey the image data to the central processor with minimal transport delay. In the visual cortex, higher level visual cognitive processes are conducted using the encoded images from the retina[11–13].

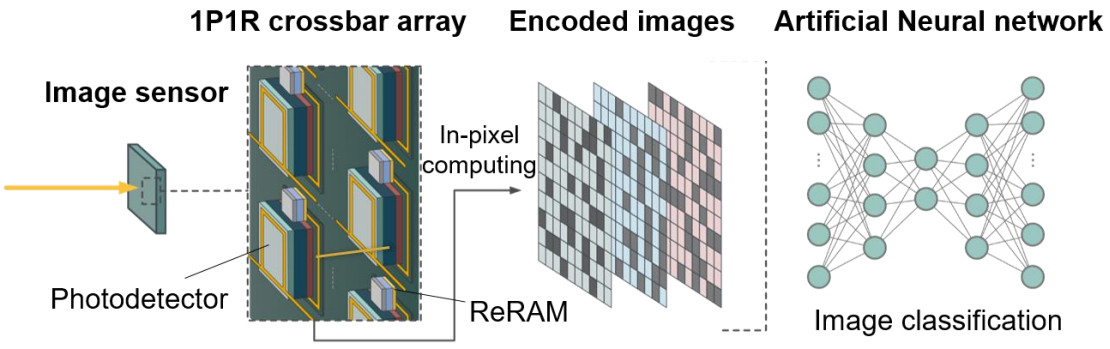


Figure 3.3 Schematic illustration of a process flow of the 1P-1R in-sensor computing system, which emulates the human vision system.

Here, I have designed and demonstrated the in-sensor neuromorphic machine vision system with functionalities of image memorization and processing by mimicking the above-mentioned neural circuit and the visual classification system in the human eyes as shown in Fig. 3.3. The the image sensor consists of a crossbar array of photodetectors and resistive memory cells, which correspond to the photoreceptors and the ganglion cells in the retina, respectively. In the retina, the ganglion cells operate as a pre-computing processor unit while the ReRAM in my system serves as a memory and computation unit simultaneously depending on a polarity and magnitude of an applied bias to each pixel. When a reversed bias with respect to the photodiode is applied to the 1P-1R pixels, the sensor operates in a memorization mode in which incident light stimuli are converted to electrical signals in the photodetectors and the photocurrents subsequently are stored in the memory cells by changing the conductance of the memory. Under a forward biased voltage with respect to the photodiode (lower than a threshold voltage for the erase operation), the sensor operates as a computing mode to process the stored image at the pixels via analogue in-memory computing for vector-matrix multiplication. Since the

vector-matrix multiplication is a key operation in the ANN algorithm, I have utilized the 1P-1R crossbar array to execute the in-sensor image encoding which extracts critical features from the original image to alleviate data transfer burden at the sensor and processor interface, paralleling biological process at the human retina. Finally, image classification is conducted in the post-processing unit with the delivered encoded images through a ANN. While the encoded images possess compressed information than original images, the ANN successfully classify the object with less computation load.

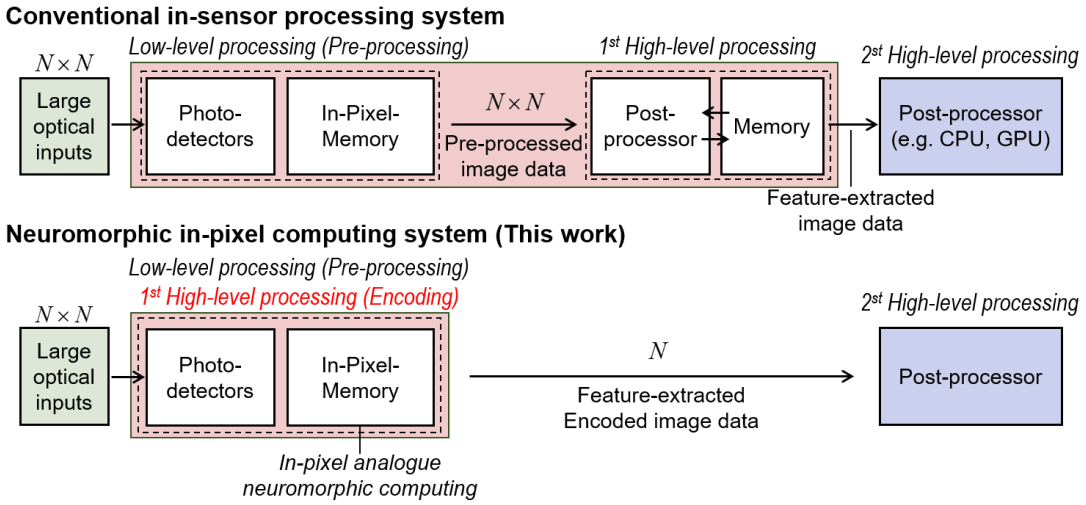


Figure 3.4 Block diagrams of image process flows with N×N input images in conventional in-sensor processing systems and 1P-1R in-pixel computing system.

Fig. 3.4 shows block diagrams of image processing sequence in conventional in-sensor processing systems and my neuromorphic in-pixel computing system.[6,20,22,23] Most of previously reported conventional in-sensor processing systems only performed image memorization and pre-processing (low-level processing) within the sensors, such as

image contrast enhancement and noise reduction. Meanwhile, the size of the pre-processed-images from the sensors ($N \times N$) is still the same as the size of the original images ($N \times N$), and high-level image processing took place in a post-processor. Therefore, the conventional systems barely reduce a data traffic load at a sensor/processor interface as well as a computational burden in a post-processor. Contrarily, fabricated neuromorphic in-pixel computing system in this work memorizes images in each pixel, and subsequently conducts image encoding by analogue in-memory multiply-accumulate operation (1^{st} high-level processing) by combining the sensing and computing functions. Therefore, the size of the output data from the sensor (N) is effectively reduced to square-root of the $N \times N$ original image by the in-sensor image encoding process, minimizing transportation of redundant data and simultaneously, reducing the computation load in a post-processor. Therefore, this advanced in-sensor computing architecture will significantly reduce inefficient energy usage and high data latency of smart imaging system.

3.3 Synaptic resistive memory on various substrates

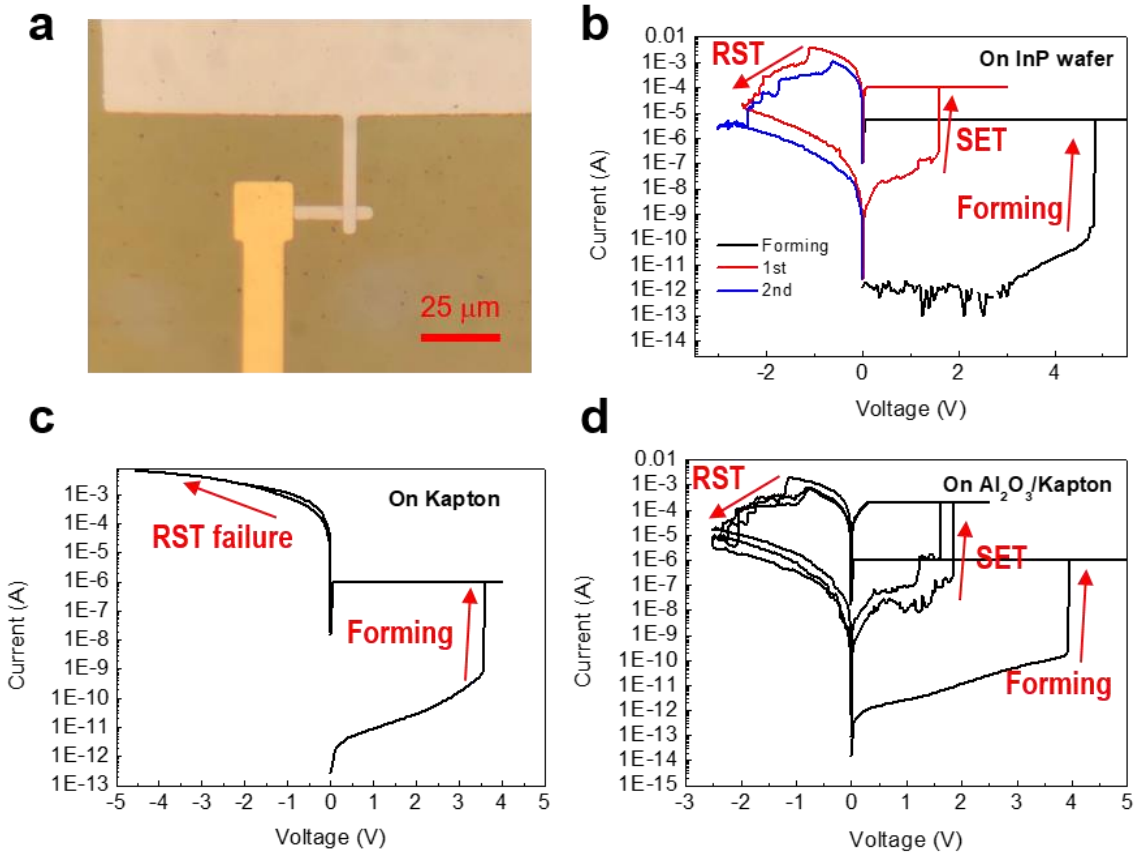


Figure 3.5. **a.** An optical image of a fabricated HfO_2-based ReRAM on a InP wafer. **b-d.** An electrical characteristics of the ReRAM on (**b**) the InP substrate, (**c**) a Kapton film, and (**d**) Al_2O_3-coated Kapton film.

HfO_2-based ReRAM is designed, fabricated, and characterized, which will be integrated with a photodetector. The structure of the ReRAM is thin-HfO_2 (5.5 nm) layer is sandwiched by top (Ta/Pt: 50/25 nm) and bottom (Ti/Pt: 5/25 nm) metal layers, in which the metal line width is 8 μm. The ReRAM fabrication begins with patterning photoresist for the bottom metal layer followed by Ti/Pt metal deposition by electron-

beam evaporation. Then, 5.5 nm of HfO_2 layer is deposited by using plasma enhanced atomic layer deposition (PEALD), and photoresist is patterned for the top metal layer and 50 nm of Ta is deposited by direct current (DC)-magneton sputtering and 20 nm of Pt layer is deposited by electron beam evaporation. Figure 3.5a shows an optical microscope image of the fabricated ReRAM on a InP wafer. The electrical characteristics of the ReRAM was characterized by a semiconductor analyzer (Fig. 3.5b). A conducting filament channel of the ReRAM should be firstly formed by applying high positive voltage (5 V) to the top metal electrode grounding the bottom metal electrode. After forming process, the resistance of the ReRAM set to a low resistance state (LRS) due to the formed conductive filament in the HfO_2 layer. When a negative biased voltage is applied to the top metal electrode of the ReRAM with LRS over a reset threshold voltage, the resistance is switched to a high resistance state (HRS), dissociating the filament channel. When a positive biased voltage is applied to the ReRAM with HRS over a set threshold voltage, the ReRAM state is turned to LRS, constructing the conductive filament again. These characteristic behaviors are clearly shown in the measured DC voltage sweep curves in Fig. 3.5b.

For further application of this ReRAM to a conformal image sensor in the future work, the ReRAM has to operate in the flexible substrate (Kapton), where the surface is rough and hydrogen atom is diffusing from the surface hindering proper operation of electronic devices. Meanwhile, the ReRAM is very vulnerable to the interface environment due to the extremely thin device structure. Figure 3.5c shows a ReRAM fabricated on a Kapton substrate with the exactly same device structure. After an initial forming process, the reset state is not recovered by an applied reset voltage. To mitigate

this problem, the ReRAM is protected from the Kapton substrate by coating the film with 50 nm of Al_2O_3 layer by PEALD before the ReRAM fabrication process. The Al_2O_3 protection layer is expected to protect ReRAM from a chemical attack from the hydrogen atoms on the Kapton as well as make the surface uniform and smooth. A characteristics of a ReRAM fabricated on Al_2O_3-coated Kapton substrate reveals a stable resistive switching behavior same as the ReRAM on the InP wafer. This Al_2O_3 coating method enables a universal application of the HfO_2-based ReRAM to various electronic devices with almost zero limitation.

3.4 Fabrication of 1P-1R single and crossbar array

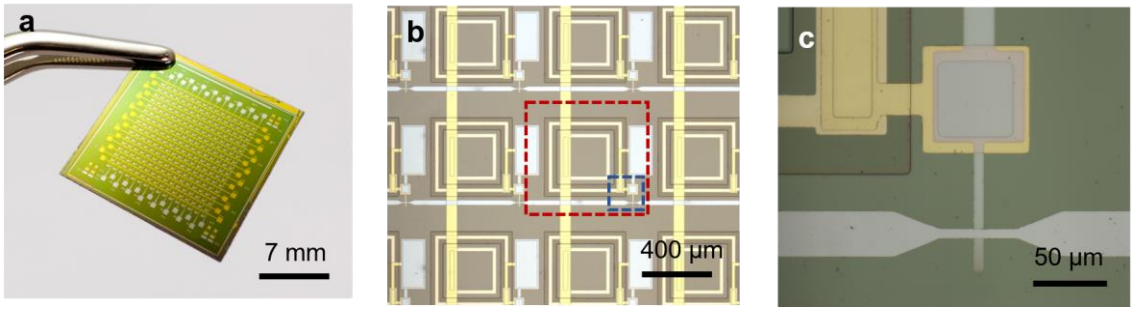


Figure 3.6 **a** Optical image of the fabricated 1P-1R focal plane array. Scale bar: 7 mm. **b,c** Optical microscope images of the fabricated 1P-1R array. Dashed red (blue) box shows a 1P-1R pixel (ReRAM) in the array. Scale bar: 400 µm. **c** An enlarged optical microscope image of the dashed blue box area in (**b**). Scale bar: 50 µm.

First, the 16×16 1P-1R in-pixel computing chip was fabricated with p-i-n InGaAs photodiodes and HfO_2-based ReRAM. InGaAs p-i-n layers were grown on a InP substrate by general molecular beam epitaxy (MBE).[26] The 1P-1R crossbar array fabrication starts

with a mesa etching of p-InGaAs/Uid-InGaAs layers. The mesa areas were protected with a bilayer photoresist (PR; LOR3A/AZ5214) by photolithography, and the unprotected InGaAs area was etched using inductively coupled plasma-reactive ion etching (ICP-RIE; BCl_3 20 sccm, 600 W ICP power, 150 W forward power, 7 mTorr, 20 ℃ stage temperature for 6 min), followed by wet etching for 1 min in a solution of H_3PO_4:H_2O_2:H_2O = 3:1:25, which stopped at the n-InP layer. The PR mask was then removed in the Remover PG (Kayaku Advanced Materials) at 60 ℃. With a single PR (AZ5214) patterning, n-InP mesa for the bottom metal electrodes was defined, followed by a wet etch process for the n-InP/InP buffer layer using a solution of HCl:H_3PO_4 = 3:1 (30 s). Next, a dielectric insulator layer of 150 nm Al_2O_3 was deposited by plasma-enhanced atomic layer deposition (PE-ALD). The via holes were etched with a bilayer PR mask using ICP-RIE (BCl_3 20 sccm, 50 W ICP power, 200 W forward power, 5 mTorr, 20 ℃ stage temperature for 6 min). The top and bottom electrodes of the photodiodes were simultaneously deposited by photolithography with bilayer PR and e-beam evaporation of Ti/Pt/Au (5/10/50 nm), which was lifted off in the Remover PG at 60 ℃. Another dielectric insulator of 150 nm Al_2O_3 was deposited by PE-ALD, and through holes were opened on the bottom electrodes of the photodiodes. Subsequently, the bottom electrodes of the ReRAMs, which are connected to the bottom electrodes of the photodiodes, were deposited using bilayer photolithography, e-beam evaporation of Ti/Pt (5/25 nm), and a lift-off process with the Remover PG. 5.5 nm of a HfO_2 layer was deposited by PE-ALD, followed by metal deposition of Ta/Pt (50/25 nm) on the top electrodes of the ReRAMs using DC magnetron sputtering of Ta (25 W RF power, 5

mTorr, Ar 20 sccm, room temperature for 18 min) and e-beam evaporation of Pt. Finally, the HfO_2 mesa areas were defined by dry etching with ICP-RIE with a bilayer PR mask.

The optical image of the fabricated chip and the optical microscope images of the 1P-1R crossbar array are shown in Fig. 3.6a and Figs 3.6e,f, respectively. Each pixel consists of a InGaAs photodiode and a ReRAM. The row lines share the top electrodes of the ReRAMs (Ta/Pt electrodes), and the column lines share the top electrode of the InGaAs photodiodes (p+ electrodes).

3.5 Characterization of Single 1P-1R Pixel

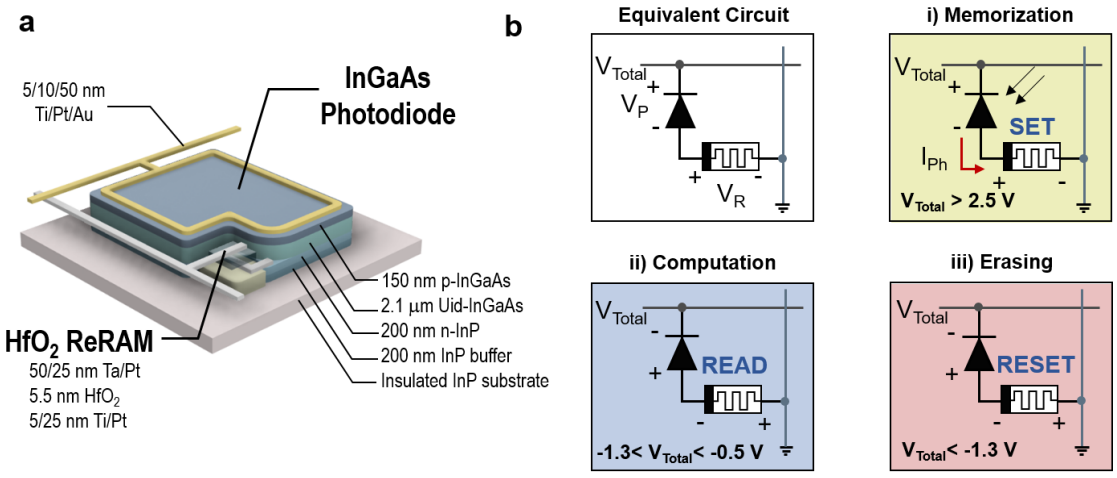


Figure 3.7 **a** Schematic illustration of the fabricated InGaAs 1P-1R device. **b** Equivalent circuit diagram of the 1P-1R structure, and three key operations in the 1P-1R device depending on applied bias voltage: i) memorization, ii) computation, and iii) erasing operations.

Prior to operating the 1P-1R array, I first study optical and electrical characteristics of a single 1P-1R pixel. Figure 3.7a shows a schematic illustration of the single 1P-1R pixel, and its equivalent circuit diagram is shown in Fig. 3.7b, where V_P and V_R are applied voltages of the photodiode and the ReRAM, respectively and $V_{total}=V_P + V_R$. The 1P-1R pixel is composed of a InGaAs p-i-n photodiode and a HfO_2-based ReRAM, which converts incoming optical signals to electrical signals and memorizes the optical information as its resistance, respectively. In addition, the ReRAM is utilized as an in-memory computation unit when it operates as a computation mode. The three primary operations of the 1P-1R device depending on applied biased voltage (V_{Total}) are depicted in Fig. 3.7b: i) Memorization, ii) Computation and iii) Erasing operations. When V_{Total}>2.5 V under light illumination, photodiode is reverse-biased so that an incident optical signal generates a photocurrent to modulate a resistance of the ReRAM by forming a conductive filament (Memorization operation). Thus, the optical signal can be stored as a form of resistance in a synaptic device. Then, the stored image data in the ReRAM can be directly used for a high-level in-sensor processing (Computation operation). When -1.3 V<V_{Total}<-0.5 V, photodiode operates under Ohmic regime with relatively low resistance (<50 Ω) compared to a resistance range of the ReRAM (> $1 \cdot 10^3$ Ω); thereby the 1P-1R circuit can be approximated to a single ReRAM circuit. Thus, the 1P-1R crossbar array can be used for a synaptic in-memory computing based on Ohm's law and Kirchhoff 's law. [6,10,27] Therefore, the ReRAM serves as a cross-functional device both for a memory unit and a processing unit towards high-level in-sensory image processing. When a high negative bias voltage over RESET threshold voltage (V_{Total}<-1.3 V) is applied across the 1P-1R device, the memorized data in the ReRAM is erased

(Erase operation). These three operations will be key functions to realize neuromorphic in-pixel image processing with the 1P-1R crossbar array.

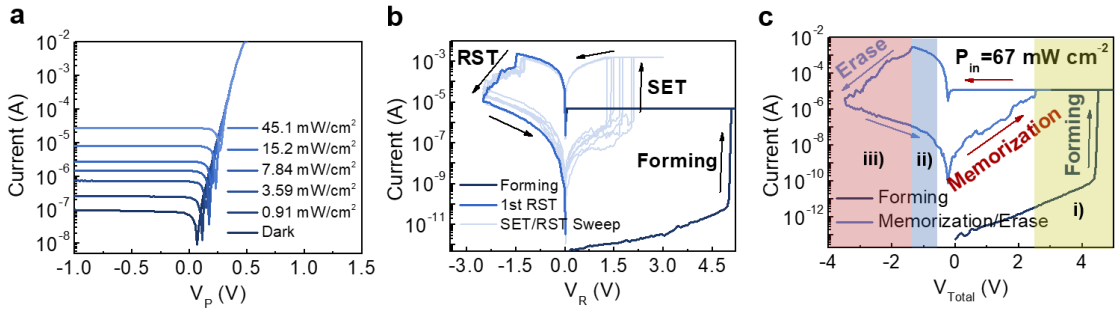


Figure 3.8 **a** I-V curves of the single InGaAs photodiode in the 1P-1R unit under dark and various light illuminations with a wavelength of 532 nm. **b** I-V characteristic of single ReRAM in the 1P-1R unit, sweeping the applied voltage along with the indicated loops in the graph. **c** I-V characteristics of the single 1P-1R integrated device under light illumination with an incident power density of 67 mW/cm^2 and wavelength of 532 nm. The colored regions indicate operation ranges for three main processes shown in (Fig. 3.7b).

Figure 3.8a shows current-voltage (I-V) characteristics of the fabricated InGaAs photodiode in the single 1P-1R device under light illumination (λ = 532 nm) with various light intensities, where V = V_P and the bottom electrode on the n-InP layer is grounded. The generated photocurrents from the photodiode under reverse bias modulate the resistance states of the connected ReRAM depending on the incident light intensity. The fabricated HfO_2-based ReRAM in the single 1P-1R device is also characterized by applying the repetitive positive and negative voltage sweeps for SET and RESET

processes, respectively, while the bottom electrode (Ti/Pt) of the ReRAM is grounded (Fig. 3.8b). Initially, to form a conductive filament, a positive d.c. voltage sweep is employed by increasing voltage from 0 V to 5 V and then decreasing voltage from 5 V to 0 V with 2 μA of a compliance current. After the initial channel forming process, repeated SET/RESET operations are performed by applying the positive and negative sweeps of 3 V (SET) and -2.5 V (RESET), respectively along the sweep paths indicated in the graph to switch the state of the ReRAM between high resistance state (HRS) and low resistance state (LRS). The I-V curves show a stable bipolar switching behavior with abrupt SET and gradual RESET, which is ideal for binary data storage.

Then, the optoelectronic switching behavior of the integrated 1P-1R pixel is characterized by an I-V measurement under light illumination (λ = 532 nm and P = 67 W/cm^2) as shown in Fig. 3.8c. The voltage is applied to the top electrode of the ReRAM (Ta/Pt contact) while the top electrode of the photodiode (p-InGaAs contact) is grounded as shown in the equivalent circuit diagram in Fig. 3.7b. Ranges of the corresponding three operations, which were explained in Fig. 3.7b, depending on the applied bias voltage are indicated by colored area in the graph. Unlike the electrical field driven switching process of the single ReRAM device, the conductive filament channel of the ReRAM in the 1P-1R pixel is grown by means of a photogenerated current from the connected photodiode (Memorization operation), whereas the RESET switching is still performed by an application of electrical field. The conductive filament is formed by the first positive voltage sweep under the light illumination, corresponding to the forming loop in Fig. 3.8c. After the forming process, the ReRAM is switched to the OFF state by applying a negative voltage sweep, where the light illumination has no effect on the Erase operation.

Subsequently, a positive voltage sweep is conducted on the 1P-1R device under light illumination, switching the ReRAM to the ON state, memorizing the light information (see memorization loop in Fig. 3.8b). Under dark conditions, the ReRAM in the 1P-1R device cannot be switched from OFF to ON via a positive voltage sweep due to a lack of sufficient driving current to build the conductive filament as shown in Fig. 3.9 since the current flow is limited by a reverse-biased dark current of the photodiode. This result clearly represents a capability of the 1P-1R device as a binary optoelectronic memory.

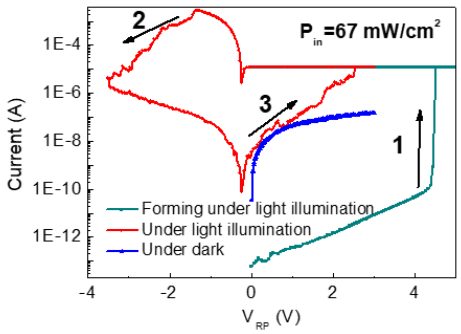


Figure 3.9 I-V characteristic of the single 1P-1R unit from forming to SET and RESET process under light illumination, sweeping the applied voltage along with the indicated loops in the graph. Red (blue) graph shows a positive voltage loop under light illumination (dark) condition.

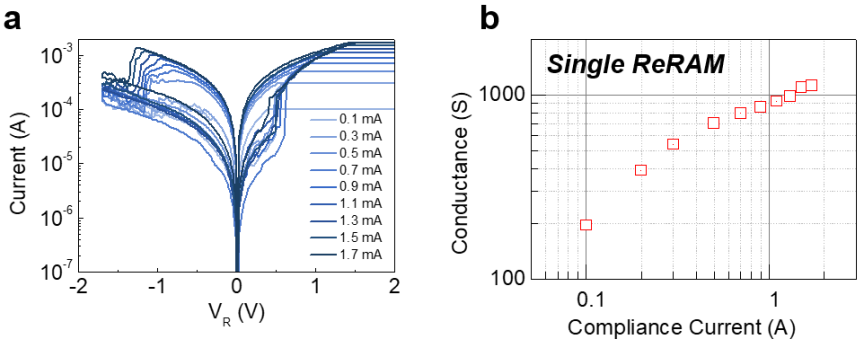


Figure 3.10 **a** I-V characteristics of a single ReRAM in a 1P-1R unit under various compliance currents. **b** extracted SET conductance depending on the compliance current during SET process.

Moreover, I have demonstrated the functionality of the 1P-1R cell as a multi-state optoelectronic memory. The memory effect of the 1P-1R unit is predominantly determined by the characteristics of the ReRAM in the pixel. Hence, a multi-state capability of the ReRAM enables the 1P-1R pixel to function as a multi-state optoelectronic memory device for in-sensor computing applications. Multiple resistance states in the HfO_2-based ReRAM is usually achieved by an application of various compliance currents during the SET operation.[28,29] Figure 3.10a presents I-V curves of the multiple resistance states in the ReRAM by controlling the compliance currents during the SET operations. When the higher compliance current is applied to the ReRAM during the SET operation, the lower resistance state is formed due to the continuous growth of the oxygen vacancy (V_o) based filament with a higher charge injection into the oxide layer.[28,29] Multiple conductance states achieved in Fig. 3.10a are plotted in Fig. 3.10b depending on the applied compliance. This behavior is consistent with characterization results from previously reported oxide-based ReRAMs.[28–30] Inspired by

above described resistance modulation method in the HfO_2-based ReRAMs, here, the photogenerated currents from the photodiode in the 1P-1R system are used as the driving currents to perform a SET operation to the ReRAM during the memorization process. Therefore, the multiple resistance states in the 1P-1R system can be enabled by light illumination with different intensities on the photodiode, generating diverse magnitudes of the driving photocurrent during the memorization process.

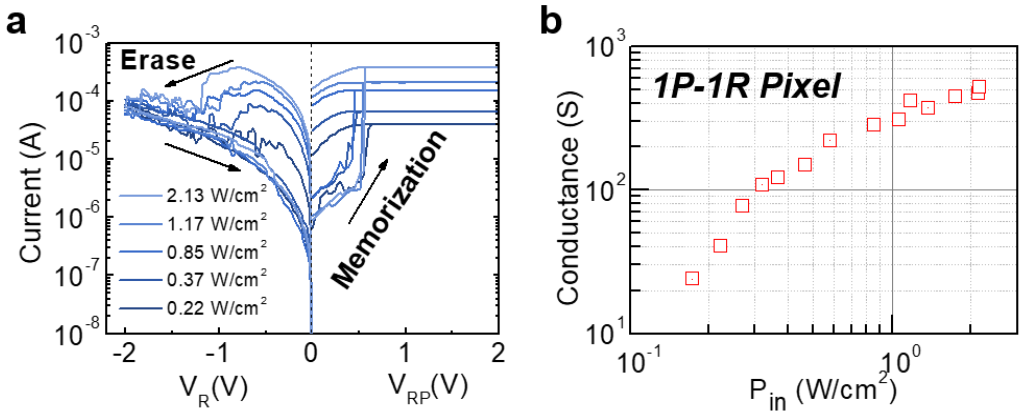


Figure 3.11 **a** Multi-state memorization process in the single 1P-1R device under light illuminations with various intensities. Each memorization process is followed by an erase process. **b** Conductance of the ReRAM in the 1P-1R unit as a function of the incident light power density during the memorization process.

Figure 3.11a shows multiple memorization and erase processes to demonstrate the analog resistance states in the 1P-1R device by employing double-voltage sweep I-V measurements under the illumination of 532 nm wavelength light. The positive voltage sweeps were applied across the photodiode-memristor (V_{RP}) to perform a light-driven

SET operation, while the negative voltage sweeps were applied only to memristor (V_R) for a RESET operation. The I-V curves in Fig. 3.11a clearly display the multiple resistance behaviors depending on the incident light intensity, where the higher intensity light results in a formation of the filament channel with higher conductance. Figure 3.11b shows conductance of multiple states depending on the incident light power density in the memorization process, nearly identical to the multi-state characteristic of the single ReRAM.

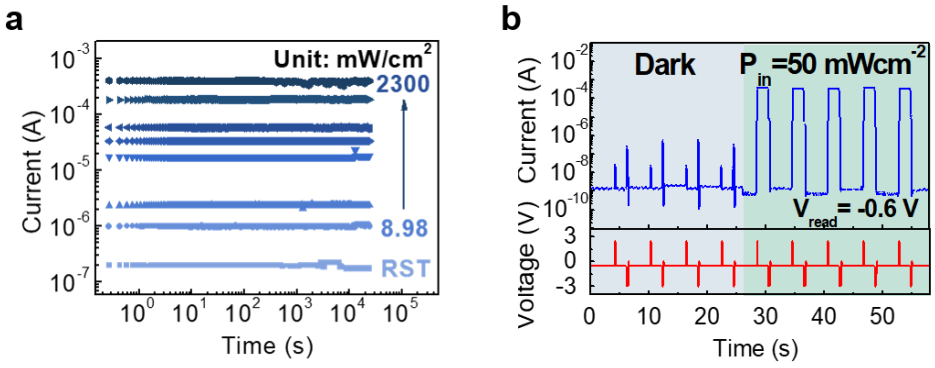


Figure 3.12. **a** Endurance test of 1P-1R optoelectronic memory depending on light intensity during memorization process. **b** Sequential memorization process in the single 1P-1R device with voltage pulse inputs. Light with P_{in}=50 mW/cm^2 is turned on at 26 s. Input voltage pulses of 2 V and -3 V were used for memorization and erase operation, respectively. Otherwise, a voltage of -0.6 V was applied to the device to readout the resistance state of the ReRAM over time.

An endurance characteristic of the 1P-1R optoelectronic memory is measured after setting the resistance of the ReRAM by illuminating lights with 7 different intensities (Fig. 3.12a). The measurement result confirms that the 1P-1R device has a

stable and reliable endurance property over 10^4 s for memory functionality. Then, to validate the continuous image detection and memorization capability using the 1P-1R system, the sequential memorization/erase operations has been demonstrated in Fig. 3.12b. Voltage pulses (V_{RP}) for memorization (2 V), erase (-3 V), and read (-0.6 V) operations are applied to the 1P-1R device under dark or light conditions with a power density of 50 mW/cm^2. Without light illumination, no data was stored in the memory even with the SET pulses, and only leakage currents were observed. On the other hand, imaging data was stored in the memory once the light is illuminated on the device with the application of memorization voltage pulse, and the memory is maintained as a form of LRS until the application of an erasing voltage pulse. When the erasing voltage pulse is applied to the ReRAM, the device is switched back to HRS. The repeated memorization/erase processes are successfully completed in the 1P-1R system. This transient switching characteristic can be utilized to perform a continuous image memorization/erase processes via an application of a voltage pulse train to the 1P-1R focal plane array without data transfer to the external memory.

3.6 Characterization of 1P-1R Crossbar Array

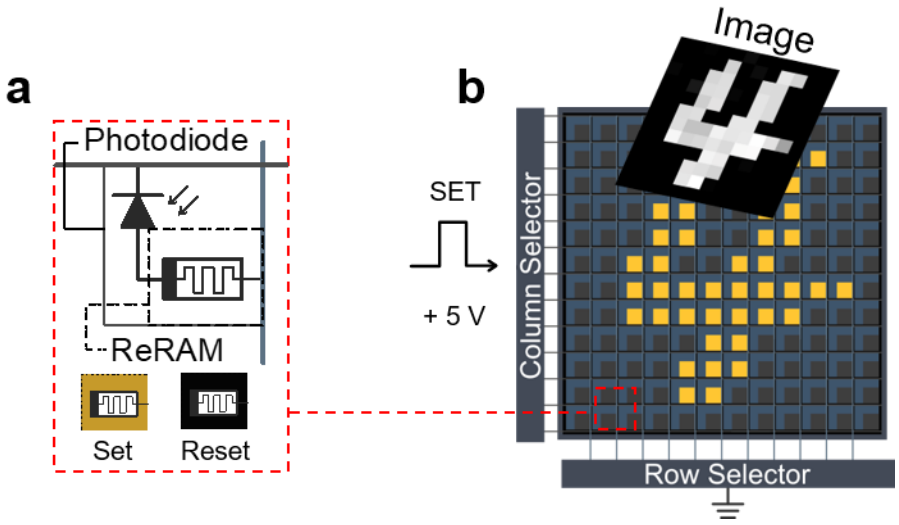


Figure 3.13 **a** Circuit diagram for a pixel in the 16×16 1P-1R crossbar array. The pixels are colored in yellow (blue) when the ReRAMs are in a SET (RESET) state in (**b**). **b** Schematic illustration of image memorization process in the 1P-1R crossbar array.

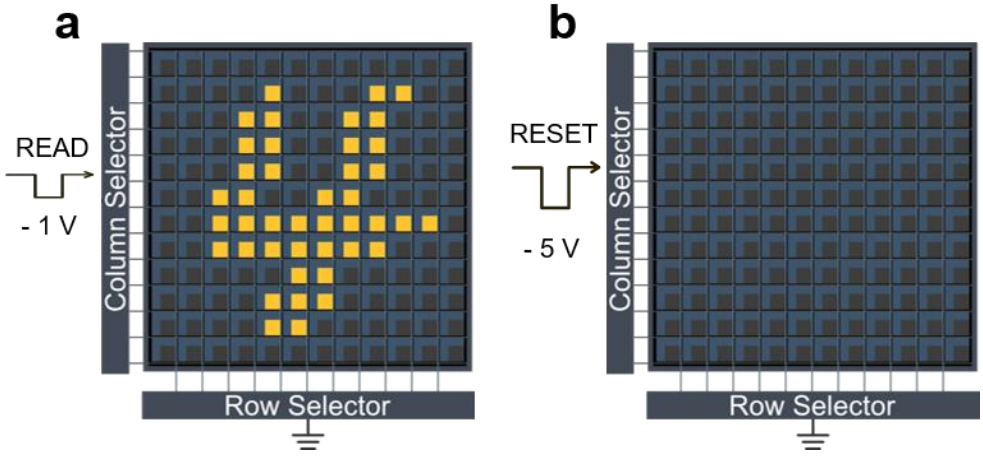


Figure 3.14 **a,b** Schematic illustration of image readout (**a**), and erasing (**b**) processes in the 1P-1R crossbar array.

With the fabricated 1P-1R array, I have demonstrated in-sensor image storage, encoding, and classification. Prior to image encoding and classification, an image storage operation is first demonstrated. Figures 3d-g show schematic illustrations of the image memorization, read and erasing processes with the 16×16 1P-1R focal plane array. A circuit diagram of the pixels is depicted in Fig. 3.13a, where a ReRAM in a yellow (dark blue)-colored pixel is in LRS (HRS) state. To control the 1P-1R array, memorization, read, and erase operations (described in Fig. 3.7b) have been utilized. For the image memorization process, voltage pulses of +5 V are applied across the individual 1P-1R pixels, where the photodiodes are reverse-biased, to store incident image information in the ReRAMs as shown in Fig. 3.13b (see Methods for more experimental details). Then, the stored image is read by applying voltage pulses of -1 V to each 1P-1R pixel, where the photodiode is forward biased, to read resistance states of the ReRAMs (Fig. 3.14a). To erase the saved image in the sensor, voltage pulses of -5 V are applied to each 1P-1R pixel to switch all pixels to HRS state, enabling the sensor to be ready to capture the next images (Fig. 3.14b).

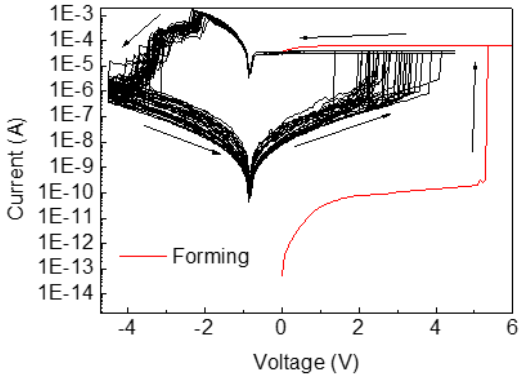


Figure 3.15 I-V characteristics of a 1P-1R pixel in the 1P-1R crossbar array under light illumination.

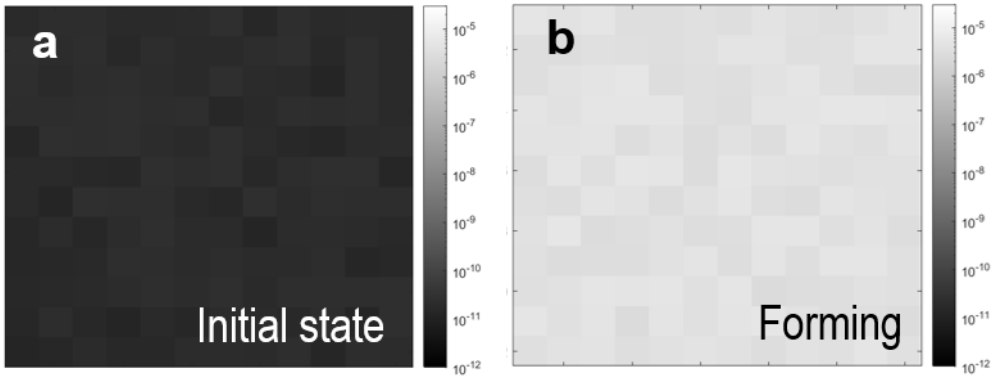


Figure 3.16 **a,b** Read current maps before (**a**) and after (**b**) a forming process in the fabricated 1P-1R array. The read voltage is –1 V.

Here, I have characterized and have operated the fabricated 16×16 1P-1R crossbar array for image memorization under light illumination with a wavelength of 532 nm. First, the I-V characteristic of an individual pixel in the array has been measured under 532 nm light illumination (Fig. 3.15). The forming voltage pulses of +6 V were applied to all 256 pixels under global light illumination (P =70 mJ/cm^2) to form the conductive filament channels in active medium of ReRAMs. Then, READ voltage pulses of -1 V are applied to each pixel to read the conductance state of each ReRAM in the pixels, followed by an application of RESET voltage pulses of -5 V to switch all pixels to HRS state for a next image memorization process. Figures 3.16a,b show 12×12 conductance maps of the InGaAs 1P-1R array before and after the forming process, respectively, in a logarithmic scale. After the forming process, all pixels are effectively switched from the initial HRS state (Fig. 3.16a) to the LRS state (Fig. 3.16b).

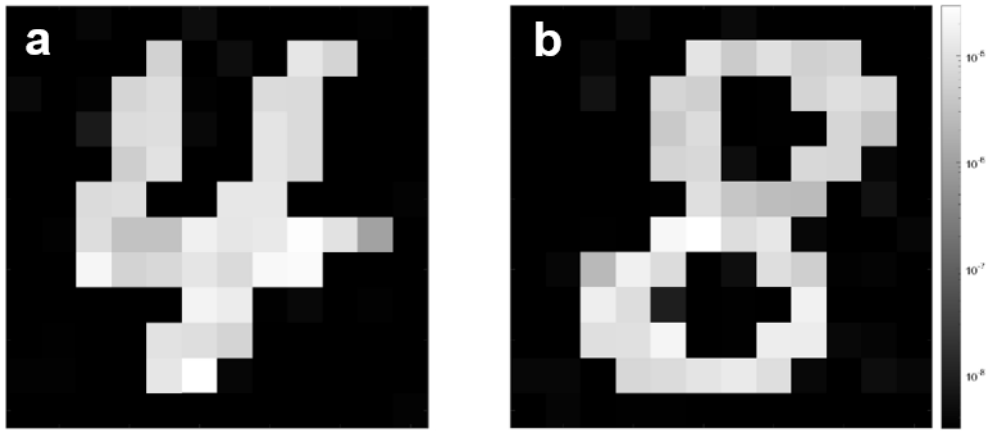


Figure 3.17 **a,b** Readout image maps after image memorization of MNIST handwritten number '4' (**a**) and '8' (**b**). The read voltage is –1 V.

Then, with the operation-ready 1P-1R array, the memorization function has been demonstrated by imaging the handwritten digit images of '4' and 8' from the MNIST dataset.[31] First, the '4' handwritten digit image is illuminated on the 1P-1R array, and +5 V (SET) voltage pulses are applied to each pixel to memorize the exposed image in the sensor as shown in Fig. 3.13b. MNIST handwritten digit images of '4' and '8' are printed out on photomasks using a direct write lithography tool (MicroWriter ML3, Durham Magneto Optics Ltd), and the diode laser light with a wavelength of 532 nm (P =50 mJ/cm^2) is illuminated on the 1P-1R device by passing through the printed digit images. The projected image ('4' or '8') on the sensor is memorized by applying a +5 V voltage pulse to each pixel using a semiconductor analyzer. After the image memorization process, -1 V (READ) voltage pulses are applied to all pixels to readout the saved image from the sensor. Figure 3.17a shows the corresponding current map of the 1P-1R array after the memorization process with the digit '4' image, indicating that the captured image is successfully memorized in the sensor. Then, the saved image in the sensor array is

erased by applying voltage pulses of -5 V (RESET) to all pixels, and second image memorization and readout processes were performed under the image exposure of the MNIST handwritten digit of '8' using the identical procedure described above (Fig. 3.17b).

The 1P-1R crossbar array can be approximated to 1R crossbar array under a forward bias condition for the photodiodes since the resistance of the forward biased p-i-n InGaAs photodiode is relatively low compared to that of the ReRAM. Thus, analogue neuromorphic computing can be directly performed in the 1P-1R crossbar array using the stored image data in the ReRAMs in the same way as 1R based crossbar arrays.[10,16,27,32] Therefore, image processing and encoding based on ANNs can be conducted within the sensor by directly implementing an vector-matrix multiplication. This in-sensor vector-matrix multiplication enables an efficient higher-level computation without data transport between the sensor, memory, and processor reducing significant amounts of energy consumption and processing time.[6,10]

3.7 In-sensor Image Encoding and Classification

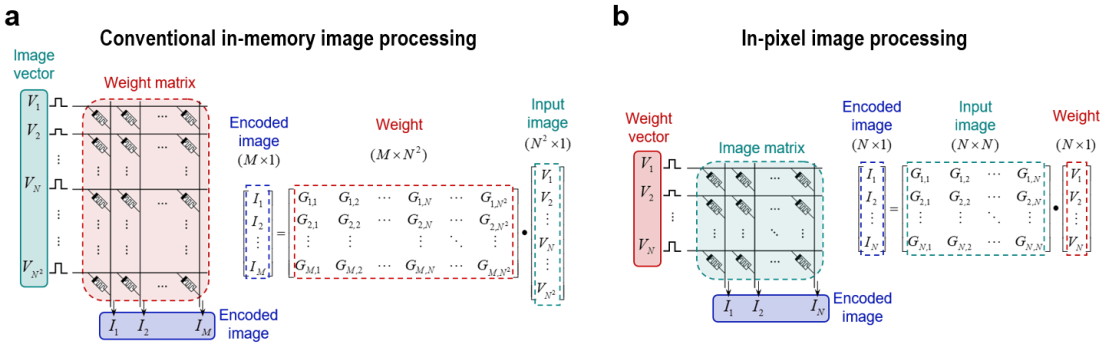


Figure 3.18 **a,b** Schematic illustration of multiply–accumulate operation for an image encoding process in conventional ReRAM crossbar array (**a**) and 1P-1R crossbar array (**b**). Corresponding matrix-vector multiplication is depicted with parameters of the input voltage (V_j), conductance of ReRAM ($G_{,i,j}$), and output current (I_j).

The fabricated 1P-1R crossbar focal plane array fuses the function of sensing, learning, and computing capabilities similar to that of biological retinas. To realize a neuromorphic vision system, I have stored the vision information in each 1P-1R cell as a matrix geometry and simultaneously harnessed the data as emulated vision encoding. Previously demonstrated conventional crossbar geometries of the neuromorphic in-memory computing systems for image processing are associated with pre-trained weight value in the matrices of ANNs, and input image data is applied to the column of the crossbar as a vectorized electrical signal (Fig. 3.18a)[6,10,14]. Since a format of image data is usually 2-dimensional (2D) $N \times N$ array, 2D-to-1D conversion (vectorization) is required to be applied as a vector input, which is $N^2 \times 1$ vector, to the column of the ReRAM crossbar array. In that case, extra complex circuit components (e.g. ADCs, DACs, and multiplexers) have to be added to a peripheral circuit to control a large number

of input signals, increasing energy consumption and operation complexity.[1,6,10] However, my in-pixel image processing system transposes image data to the weights of an ANN, in which input image is applied and is stored to the crossbar array as an weigh vector matrix form as shown in Fig. 3.18b. Thereby, the 2D-to-1D conversion of image data is no longer necessary for this configuration, tremendously reducing the circuit complexity and improving the operation efficiency. Moreover, data transportations from image memorization to image encoding process are extremely diminished because the image information is directly processed in the pixels without any data transfer.

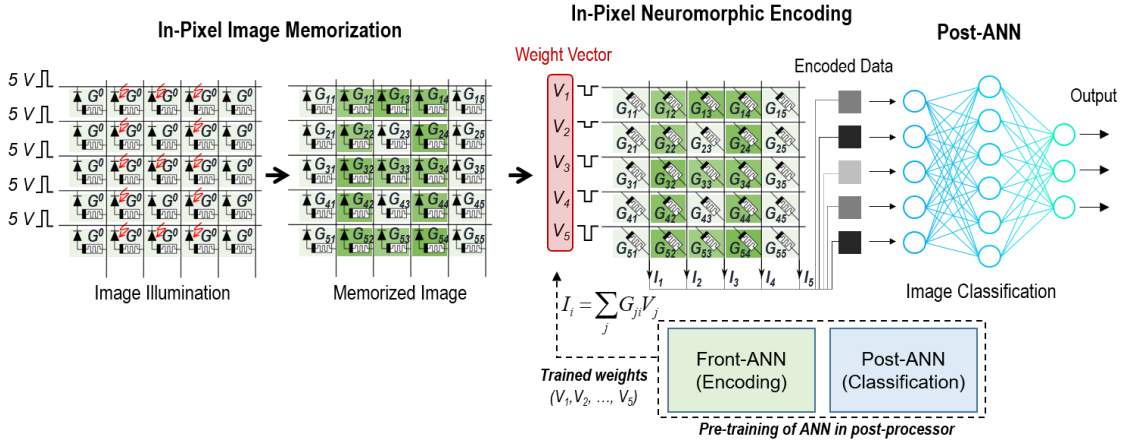


Figure 3.19 Schematic illustration of an example of in-pixel image memorization, encoding, and classification process with a 5×5 1P-1R array. At the initial state, conductance of ReRAMs is G^0. After image memorization, conductance of each ReRAM is indicated as G_{ij}. Once an image is memorized in the sensor, pre-trained weight voltages (-1.3 V<V_i<-0.5 V) are applied to the rows of the crossbar to perform a multiply–accumulate operation in the sensor for the encoding process. The encoded data are transferred to a post-ANN to classify the image.

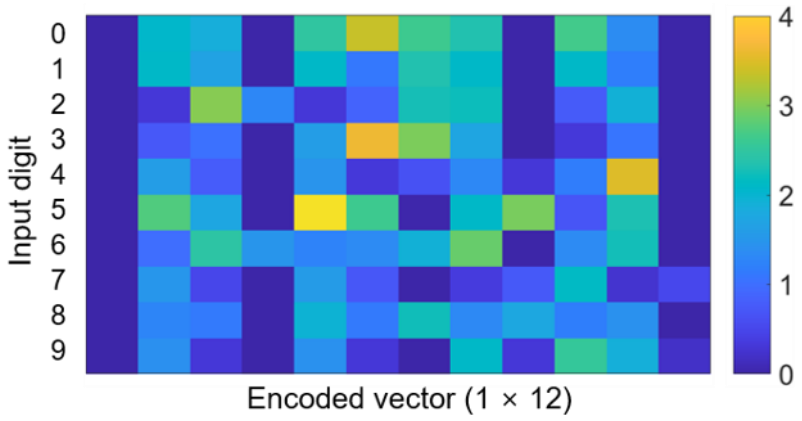


Figure 3.20 Examples of encoded images of MNIST handwritten numbers from 0 to 9.

Figure 3.19 shows the in-pixel computing process by using the fabricated 1P-1R array. The 12×12 image of '8' is optically mapped onto the 1P-1R array (sensing) and preserved as the conductance of the ReRAMs (learning). Meanwhile, the front-ANN and post-ANN has been pre-trained with 10,000 datasets of MNIST handwritten numbers in post-processor to extract the optimum weight vector.[31] The pre-trained 1D weight vector is then converted to electrical signals and applied to the 1P-1R array, enabling the physical matrix multiplication for the in-pixel ANN computation via Ohm's and Kirchhoff 's law (computing). The output current signals from the voltage-conductance multiplication thus represent the encoded vector of the image '8,' achieved without the data transportation by emulating biological encoding capability. Figure 3.20 shows the 10 encoded vectors (vector size: 1 × 12) for input digits from '0' to '9', and each digit exhibits the distinguishable encoded vector. The encoded vector is then fed to the next hidden layers to perform the classification of image in the post-ANN.

The encoder and classifier models were implemented using Python. I combined a matrix-to-vector encoder (12×12-12) and a fully connected layer classifier with two hidden layers (12-20-16-10) on the Modified National Institute of Standards and Technology (MNIST) dataset. Each original MNIST image was resized to 12×12 pixels, and I trained and tested 10,000 images (with 64 batch sizes for 100 epochs) and 100 MNIST images. For the backpropagation learning process, I employed an RMSprop optimizer, rectifier (softmax for the last output) nonlinearity activations, and an initial time-decaying learning rate (0.001).

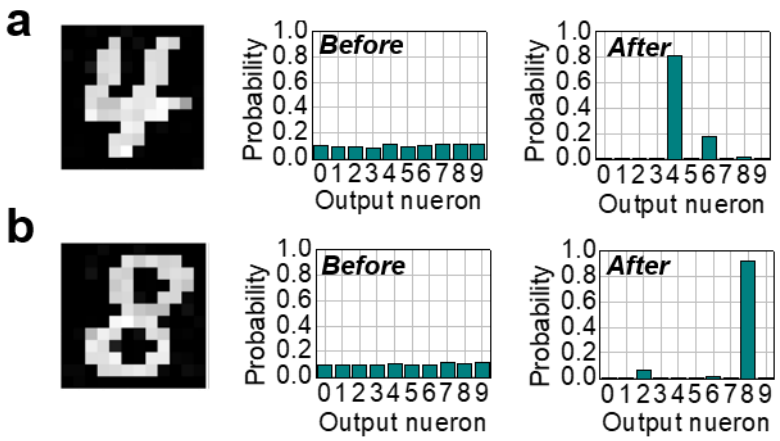


Figure 3.21 **a,b** Classification results from the memorized '4' (**a**) and '8' (**b**) digit images before and after training the ANN.

Figures 3.21a,b show the classification results from the measured and memorized '4' and '8' digit images. Before the training, the activation level of each digit is randomly distributed. However, the activation level of the output neurons of the ANN is concentrated on a single digit after the training. A digit with the highest activation level is adopted as a classified 'answer'. Figures 3.22a and b show the results of image

classification before and after 100 training epochs for the full precision of 10,000 test digit images, exhibiting that the classification performance of the ANN is significantly improved after training ANN. Although the proposed device has the *N* times smaller number of weight values compared to the conventional in-memory computing methods, the classification accuracy is up to 82% with the 100 training epochs (Fig. 3.22c). Further accuracy improvement could be possible by employing a dual encoding neural layer to the ANN, conserving both row- and column-wise features of images which can be realized by employing the bi-directional peripheral circuitry.[33]

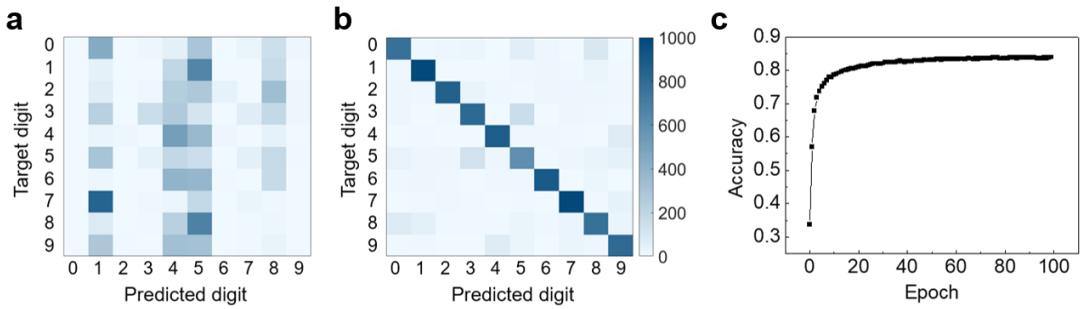


Figure 3.22 **a,b** Confusion matrices for a classification result from the 10,000 MNIST handwritten digit images before (**a**) and after (**b**) 100 training epochs. **c** Classification accuracy as a function of the number of training epochs. The classification accuracy is up to 82% with the 100 training epochs.

3.8 Conclusion

I have demonstrated a neuromorphic machine vision system with in-sensor encoding process, inspired by mammalian vision. The focal plane array is based on InGaAs photodiode directly integrated with the HfO_2 ReRAM, constructing the 1P-1R

optoelectronic memory and computing pixel. Optoelectronic and memory functionality of the fabricated 1P-1R pixel under light illumination shows the reliable digital and multibit memory operations and endurance performance. Furthermore, developed 16×16 1P-1R crossbar array with InGaAs photodiode and HfO_2-based ReRAM was characterized to perform the edge computing of handwritten numbers. Finally, I demonstrated biological image encoding with the developed 1P-1R crossbar array, utilizing direct image memorization and in-memory vector-matrix-multiplication. The encoded images are conveyed to the ANN for the image classification process, which reveals an accuracy of 82% with the 100 training epochs. This slightly low classification accuracy is attributed to the structure of the encoding neural network which consists of 12 of a 12×1 fully-connected layer. This architecture of the neural network is inevitably determined by the hardware circuit structure of the 1P-1R crossbar array. The classification accuracy of my sensor system can be further improved with a dual encoding neural layer to the ANN.

This in-sensor encoding method can be benchmarked against the compressed sensing technology. The compressed sensing is a new data acquisition way to directly sense data in compressed form at lower sampling rate.[34] Then, the sparse and compressed data is transferred to a main processor with a low energy consumption and fast transfer time because of the smaller size of the image data. Then, the compressed images are reconstructed in the main processor with a reconstruction algorithm. In this way, for example, the compressed sensing method has enabled speedups by a factor of seven in pediatric magnetic resonance imaging (MRI) while preserving diagnostic quality by reducing measurement and image transfer times.[34,35] While the compressed sensing

method only focuses on alleviating the data bottleneck issue between sensors and processors, my in-sensor encoding system not only compresses image data to minimize the bottleneck but also efficiently shares the computation burden for the image classification task with the post-processor by extracting features of the images with in-memory computing method. Therefore, this new in-sensor computing system enables an efficient image classification by directly extracting features of images within the sensor and transferring compresses images to the post-processor. The introduced in-sensor computing concept in this work provides a novel method to store and process image information directly within the pixels that is seamlessly scalable with the conventional semiconductor fabrication technology.

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Chapter 4

Curved Image sensors

4.1 Introduction to curved imagers

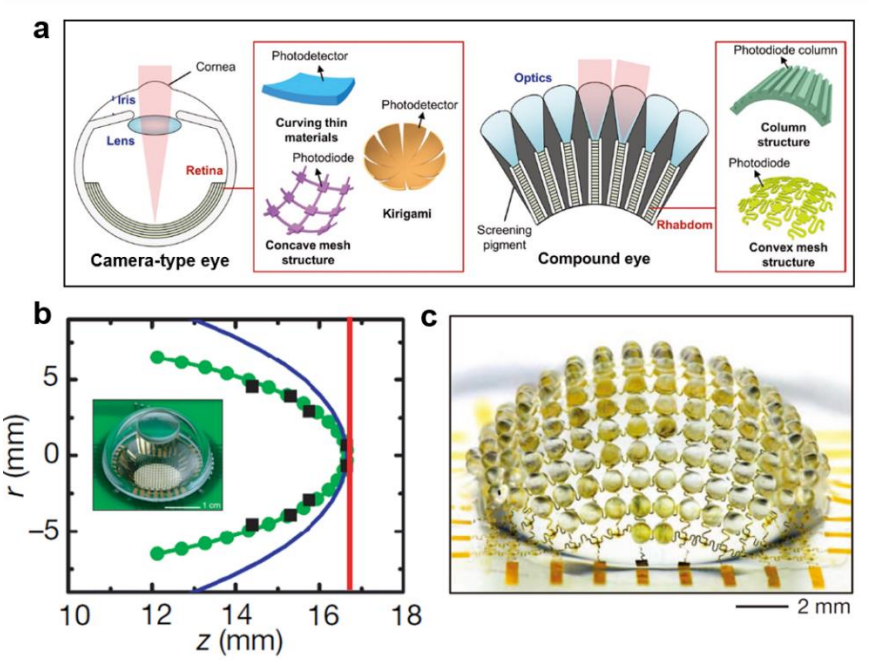

Figure 4.1 **a,** Schematic illustrations of the major components of bioinspired imaging systems: camera-type eye (left) and compound eye (right). **b,** Ray tracing simulation of the curvature of the focal plane of single lens (green circles) and parabolic fit (green curve), the detector surface profile of the hemispherical camera (blue curve), and a planar camera (red curve). Inset: image of the fabricated hemispherical electronic camera. **c,** Image of the compound eye camera with 16x16 microlens array integrated with thin silicon photodetectors.

Typical image sensors consist of a focal plane array of light-sensing pixels, a set of light focusing optics, and a back-plane readout circuit. Most of conventional focal plane arrays have a planar geometry because of a planar semiconductor-fabrication technology/process and non-flexibility of their solid substrates such as a silicon, GaAs, and InP. Unfortunately, the planar focal plane array, inevitably, requires extra bulky and complex optics components to focus light on the planar focal plane array minimizing optic aberrations (e.g. chromatic aberration, spherical aberration etc.) since the focal plane of a single lens system is naturally a hemisphere or paraboloid surface (Fig 4.1). This complex optic system is a main obstacle to the development of compact and light weight imagers without optic aberrations, which is of interest in various applications including smartphone and drone as well as robot eyes and visual prostheses [1–6].

To overcome the limitation of planar detection geometry, researchers have developed several methods to fabricate conformal focal plane arrays on flexible substrates. Fig. 4.1a shows two different types of conformal imagers, which are a retina-type imager and a compound eye-type imager. The retina-type imager enables a high-resolution and wide field-of-view imaging with simple optic lenses. Ko et al. demonstrated a retina-type hemispherical conformal imager based on compressible silicon photodiodes array with a single-element lens system. Although the imager has only one lens to focus an image onto the focal plane array, high quality images are obtained without the off-axis optic aberration by matching the surface of focal plane array to the calculated Petzval surface of the lens (Fig 4.1b)[2].

The compound eyes usually can be found in insects, crustaceans, and other arthropods, the individual facets are optically isolated from one another, with each

providing part of the total scene (right panel of Fig 4.1a)[1,4,7]. Compound eyes exhibit various remarkable advantages such as a 180 degree of field of view, fast motion detection, and infinite depth of field[1,2,4–11]. Thus, the compound eye-type imager enables an extreme wide-field of view imaging (~ 180°) with the infinite depth of field sacrificing the resolution of the image sensor. Figure 4.1c shows a compound eye-type image sensor. Elastomeric compound microlens array is combined with a deformable array of thin silicon photodetectors, and then they are deformed into a hemispherical shape. This artificial compound eye camera achieved fascinating imaging features of the biological compound eye, such as individual imaging, a wide field of view (160°), a nearly infinite depth of field, and low off-axis aberrations[2].

4.2 Introduction to curved infrared image sensor

Image sensors and their technology are increasingly important as demands for efficient imaging and surrounding environments analysis have surged in machine vision, the internet of things (IoT), medical imaging, and astronomy applications. Conventional image sensors are typically composed of a set of complex optical components, a planar focal plane array (FPA), and a readout backplane circuit. The high complexity in the optic systems originates from the fact that single-lens systems focus an object plane onto a curved focal plane (Petzval plane), resulting in a significant mismatch between the Petzval plane and the planar FPA, particularly on the off-axis surface. Thus, this curved nature of the Petzval surface of simple optic systems requires adding bulky field flattening lens elements to the design to minimize the optical aberrations. Nowadays, high-resolution and high-quality imaging even with planar FPAs has been enabled by rapid developments in design and manufacturing technologies for complex lens systems along with a matured semiconductor fabrication technology. The bulky and complex lens systems, however, contribute to increased volume and weight of image sensors while needs for miniaturization have constantly increased for applications such as drones, virtual reality/augmented reality (VR/AR), medical imaging, and military imaging. Also, adding extra lenses typically gives rise to other aberrations on an off-axial focal surface, reducing the quality of captured images. As scaling and simplification of optical systems have reached their physical limit, it is desired to develop totally different approaches to considerably simplify complex optical components for further minimization and lightening of image sensors.

Recently, curved FPAs have emerged as a potential promising candidate to mitigate the disparity between the curved focal plane and FPAs with planar geometry even with simple optic components. Instead of adding numerous lenses to generate a flat focal plane, the geometry of the FPA is directly manipulated so as to exactly match it to a hemispherical Petzval surface, dramatically decreasing the complexity of optic elements in the image sensor. Thereby, the volume and weight of the curved image sensors are significantly reduced, while the performance of the optic system is even improved in terms of field of view, modulation transfer function and relative light illumination especially off-axis. There have been several demonstrations of curved (cylindrical or hemispherical shape) FPAs with various active materials (e.g. silicon, III-V compound semiconductors, two-dimensional (2D) materials, and perovskite) by typically employing transfer printing, epitaxial lift-off (ELO), and Kirigami/Origami techniques.[2,12] Their curved imagers successfully presented a capability of high-quality imaging with simple lens elements without a spherical aberration. However, their imaging systems mainly lack a readout integrated circuit (ROIC) and further design and method to integrate a ROIC on their curved FPAs to construct a complete curved image sensor. Moreover, it is hard to develop a manufacture process to produce high-pixel-density curved imagers comparable to the state-of-the-art planar image sensor by utilizing the previously demonstrated fabrication methods.

Contrarily, Sony and Microsoft have demonstrated mass-producible silicon CMOS curved image sensors with an integrated silicon ROIC by thinning and curving commercially-available silicon CMOS sensors.[13,14] Since these fabrication methods can be applied to any planar commercial silicon CMOS sensors, practical curved imagers for

a visible light detection can be achievable by utilizing the developed methods. However, curved image sensors for non-visible light applications are still unattainable with these manufacture techniques because the range of detection wavelength of silicon is only limited to the visible regime due to an absence of its bandgap modulation method. For non-visible imagers, III-V compound semiconductors have been widely used by virtue of seamless bandgap modulation from far-infrared (IR) to ultraviolet (UV) by tuning atomic compositions of compounds with well-developed epitaxial growth techniques. There have been several demonstrations of a curved IR FPA based on III-V semiconductors by employing an epitaxial lift-off (ELO) technique. Nevertheless, these methods still lack a methodology to integrate a ROIC with the FPAs since there has been no demonstration of an integration of a curved epitaxial film with a ROIC, to the best my knowledge.

In this work, I will demonstrate an entirely new approach to achieve a retina-type infrared (IR) image sensor by hybridizing a curved GaAs FPA with a curved readout integrated circuit (c-ROIC), which will enable to realize an extreme radius of curvature (RoC) for extreme size, weight, and power (SWaP) reduction compared to conventional imagers. The free-standing single crystalline GaAs epitaxial layer will be grown and lifted-off by remote epitaxy and 2-dimensional material-based layer transfer (2DLT), respectively.[15,16] Remote epitaxy is a epitaxy technique that has proven their ability to grow single crystalline compound semiconductors on graphene coated substrate and allows to lift-off it from the substrate by taking advantage of weak van der Waals bonding between graphene and epitaxial film. Remote epitaxy and 2DLT process allows the 3D heterogeneous integration with dissimilar materials[15,16]. Therefore, lifted-off active

absorbing materials via 2DLT can be applied on top of fabricated CMOS readout-circuits on thin-film silicon.

4.3 Remote epitaxy and 2D Layer Transfer (2DLT)

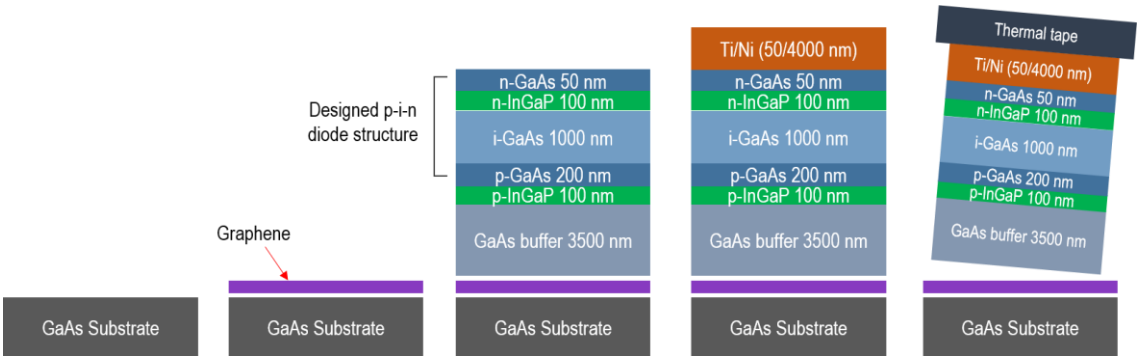

Figure 4.2 Schematic illustration of remote epitaxy and 2DLT process to growth and exfoliation of p-i-n GaAs structure

To utilize exotic compound semiconductor materials for the conformal focal plane array, I have developed a method to grow III-V compound semiconductors on a graphene coated-substrate by the remote epitaxy and exfoliate/transfer the epitaxial layers by the 2DLT process. Figure 4.2 shows the process flow of preparing free-standing epitaxial films by employing the remote epitaxy and the 2DLT process. The remote epitaxy starts with a transfer of graphene on an GaAs wafer by means of layer resolved splitting (LRS) process of monolayer graphene from few-layer graphene[17]. Then, a thick buffer GaAs layer is directly grown on the graphene-coated GaAs wafer to reduce the defect sites and increase uniformity of the epitaxial layer, and the designed inverted active epitaxial layers (pin GaAs active layers) are subsequently grown on top of the buffer layer. The two

InGaP layers are inserted in the designed growth structure for etch-stop in the device fabrication process. After the epitaxial growth, Nickel (Ni) metal stressor is deposited on the epilayer by using a DC magneton sputter. The tensile-stressed metal film imparts strain energy to the graphene/epilayer interface causing the epilayer to delaminate from the graphene surface when the strain energy surpasses the bonding energy between the epilayer and graphene. The epilayer is exfoliated by applying a thermally release tape, which releases the attached film when the temperature increases above the releasing temperature (e.g. 150 ^{o}C), on Ni as a temporal handler.

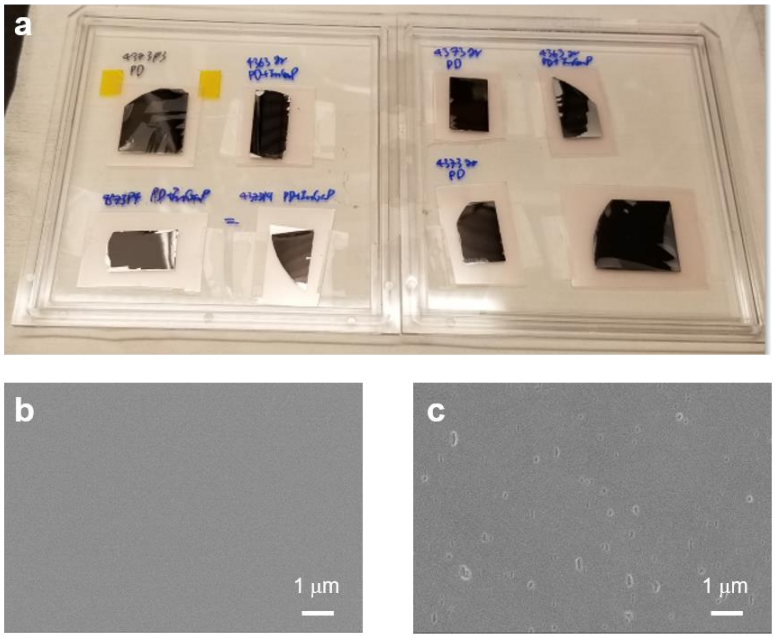

Figure 4.3. **a.** an optical image of the exfoliated epitaxial films on the thermal release tapes. **b,c.** SEM image of GaAs grown on (**b**) a GaAs bare substrate and (**c**) a graphene-coated GaAs substrate.

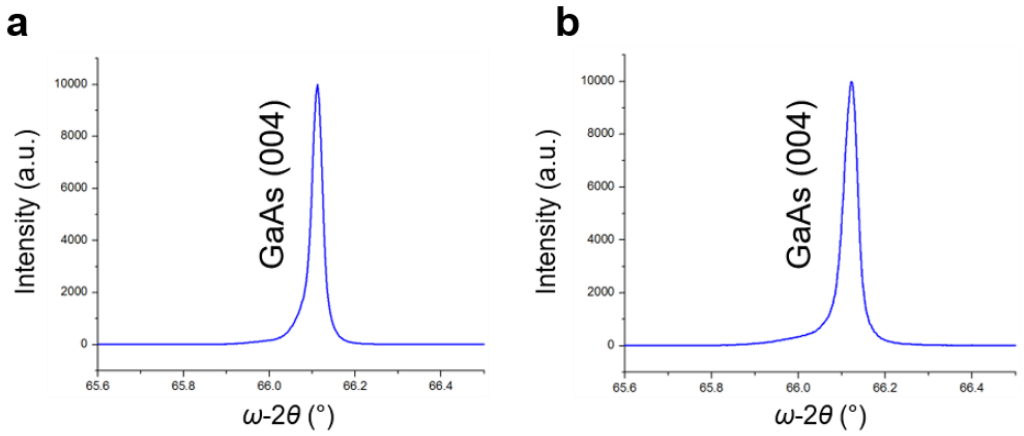

Figure 4.4. **a,b** XRD measurement data from GaAs grown on (**a**) a GaAs bare substrate and (**b**) a graphene-coated GaAs substrate.

Figure 4.3a shows the successfully exfoliated epitaxial films on the thermal release tapes. The 2" GaAs wafer was clipped into small pieces before the exfoliation step to produce more pieces of samples to test the fabrication process and fabricate test devices. The surface and crystallinity characterizations of films were performed using scanning electron microscopy (SEM) and x-ray diffraction (XRD) measurement. Figures 4.3b and 4.3c show the SEM images of the GaAs epitaxial films grown on a bare GaAs substrate and a graphene-coated GaAs substrate, respectively. Although the epilayer grown by the remote epitaxy exhibits several defect sites which may be originating from defects on the graphene layer, the uniform GaAs is remotely grown on the graphene-coated substrate. The growth condition and/or graphene transfer process (LRS process) should be further optimized to reduce the defects on the surface of the epitaxial layer. The single-crystal nature of the grown films is still confirmed by characterizations based on the XRD measurement as shown in Figs. 4.4a and 4.4b which are measured from the

GaAs films grown on the bare GaAs substrate and the graphene-coated GaAs substrate, respectively. The full width half maximums (FWHM) of the GaAs(004) peaks are 115 arc-second for the GaAs on the bare GaAs substrate and 144 arc-second for GaAs on the graphene-coated substrate. These free-standing films are ready to be fabricated into photodiodes for the conformal focal plane array. Figure 4.5 shows SEM images of as-grown epitaxial layer on a graphene-coated GaAs substrate.

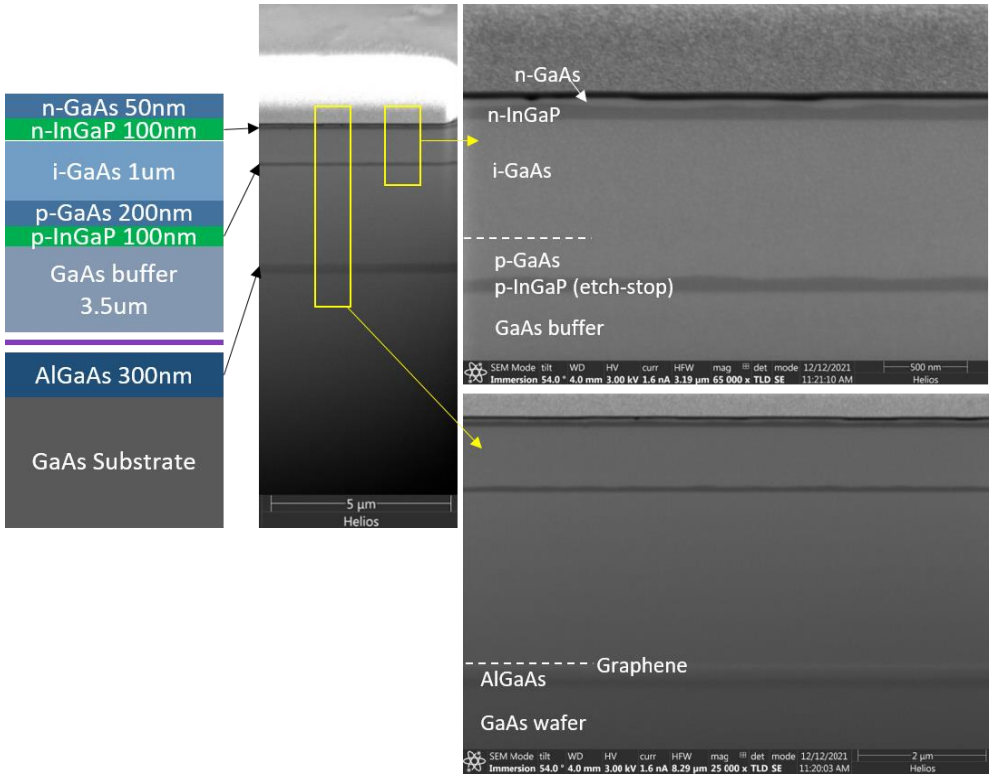

Figure 4.5. Cross-sectional scanning electron microscopy (SEM) image of as grown epitaxial layer on graphene-coated GaAs substrate.

4.4 Single photodiode fabrication and characterization

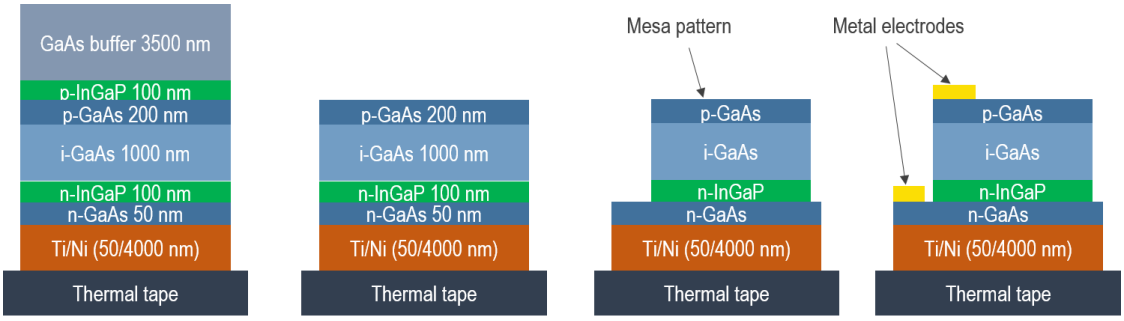

Figure 4.6. Schematic illustration of a fabrication process flow of a GaAs photodiode from the exfoliated epitaxial film.

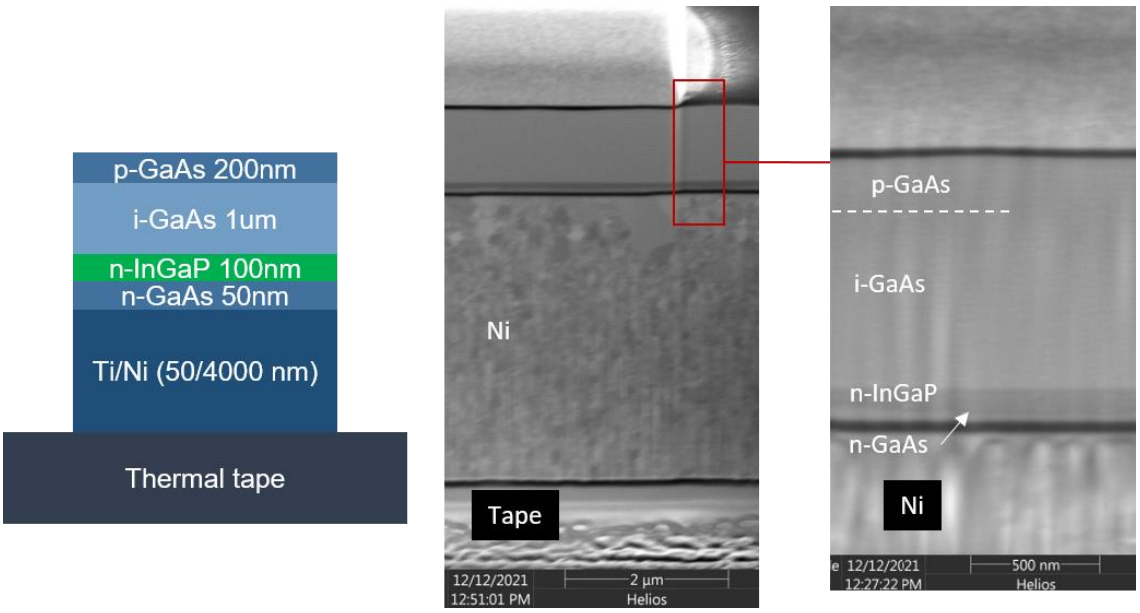

Figure 4.7. Cross-sectional scanning electron microscopy (SEM) image of the exfoliated film from the graphene-coated GaAs substrate after selectively etching the GaAs buffer layer.

Single p-i-n photodiodes are fabricated to characterize the exfoliated free-standing GaAs films and the electrical and optoelectrical properties of the GaAs photodiode. The fabrication process (Fig. 4.6) starts with etching buffer GaAs and p-InGaP etch stop layer by using a selective wet etching process where a solution of H_3PO_4:H_2O_2:H_2O (3:1:25) and a solution of H_3PO_4:HCl (1:4) are used as selective etchants for GaAs and InGaP, respectively. Then, photoresist is spin-coated on the film, and mesa patterns for active areas are defined by a general photolithography process. The opened p-i GaAs layer is firstly etched by Inductively Coupled Plasma-Reactive Ion Etching (ICP-RIE) under BCl_3 gas injection followed by wet etching process with the GaAs etchant, where the etch stops at the n-InGaP layer. The n-InGaP etch stop layer is selectively etched by the InGaP etchant, and accordingly, photoresist mask is removed in an acetone solution (rinsed with 2-propanol and deionized water). After the GaAs mesa patterning, another photolithography process is performed to define top and bottom electrode areas, followed by electron beam evaporation of Ti/Au (5/50 nm) and metal lift-off process in an acetone solution. Figure 4.7 shows cross-sectional SEM images of the exfoliated film after selectively removing the GaAs buffer layer.

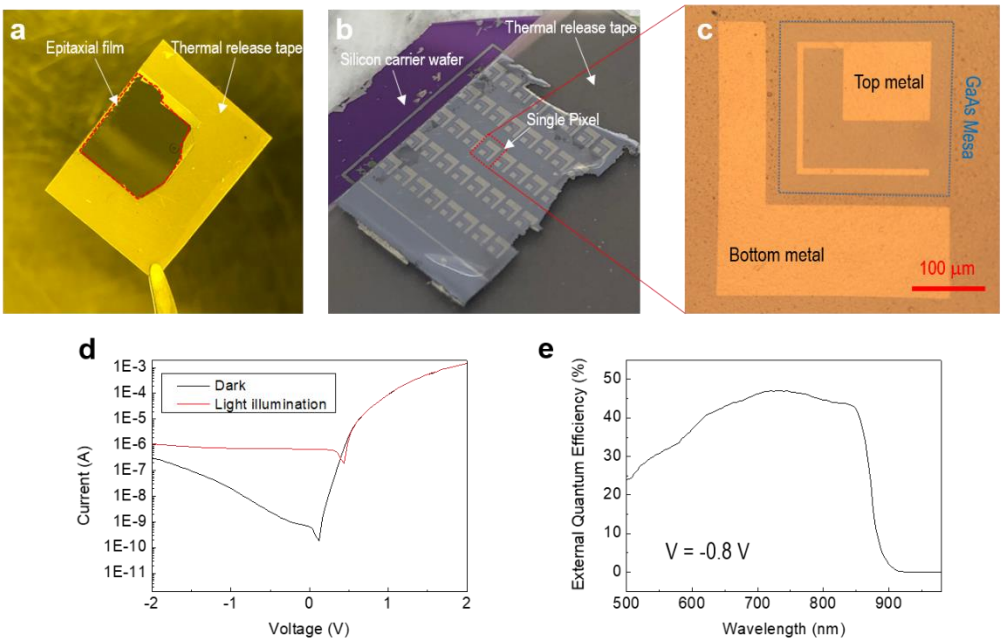

Figure 4.8. **a.** an optical image of the exfoliated epitaxial film on the thermal release tape. **b.** an optical image of the fabricated single pixel GaAs p-i-n photodiodes on the exfoliated epitaxial film. **c.** an optical microscope image of the single pixel GaAs photodiode. The scale bar is 100 μm. **d.** Measured I-V curves of the GaAs photodiode under dark and light illumination. **e.** EQE spectrum of the GaAs photodiode under an application of negative voltage bias (-0.8 V).

Figures 4.8a,b show optical images of the GaAs epitaxial film on a thermal release tape before (Fig. 4.8a) and after (Fig. 4.8b) the fabrication process of the single photodiodes, respectively. The optical microscope image of the single pixel of the photodiode is shown in Fig. 4.8c. The fabricated devices were characterized by current-voltage (I-V) curve measurements under dark and light illumination as well as a spectral measurement of an external quantum efficiency (EQE) (Figs. 4.8d,e). Figure 4.8d shows the I-V curves of a photodiode under dark and white light illumination. The device

exhibits low dark current at a low negative bias, but relatively higher dark current is measured at a larger negative bias voltage, which may be attributed to a leakage current through detect sites observed in the SEM image (Fig. 4.3c). Figure 4.8e shows the measured EQE spectrum under an application of a negative bias voltage (-0.8 V). The EQE spectrum shows that the GaAs photodiode responses to photons whose energy is above ~1.42 eV. This energy is well matched with the bandgap energy of GaAs (1.44 eV). However, the highest EQE is only ~ 47 % at λ = 732 nm. This low EQE is mainly ascribed to an absence of anti-reflection coating ($R = [(n_1-n_2)/(n_1+n_2)]^2$ = ~31 %, where n_1=1 (air) and n_2= 3.5 (GaAs)), an absorption of the incident light in the 200 nm p-GaAs layer, and thin thickness of the i-GaAs layer. Therefore, the EQE can be further improved in the next batch by increasing the thickness of the i-GaAs layer and decreasing the thickness of the p-GaAs layer, and applying anti-reflection coating.

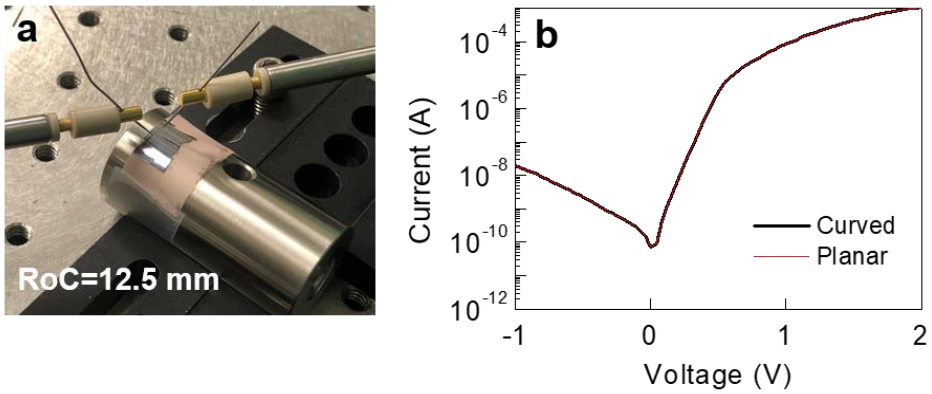

Figure 4.9. **a.** an optical image of the curved photodiode attached on a cylinder with 12.5 mm RoC. **b.** I-V characteristics of the photodiode under dark condition in planar and curved geometries.

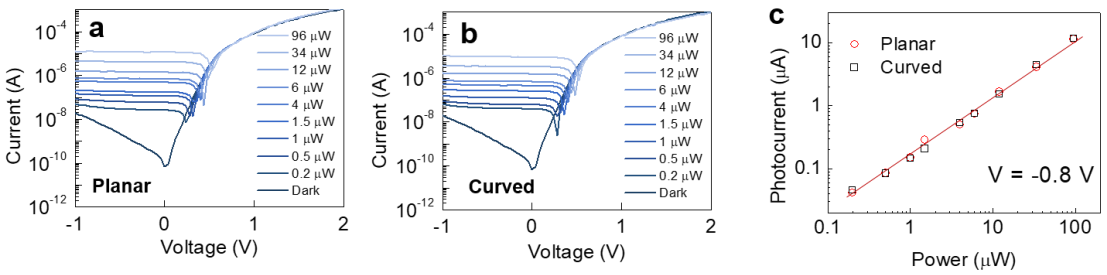

Figure 4.10. **a,b.** I-V characteristics of the photodiode under various light illumination in (**a**) planar and (**b**) curved geometries. **c.** Photocurrent plot as function of illumination power under an applied voltage of -0.8 V.

The GaAs photodiodes should properly operate in curved geometry since the exfoliated epitaxial film will be integrated with a curved ROIC for future curved imager applications. Thus, the electrical and optoelectrical characteristics of the photodiodes were measured in a planar form as well as in a curved geometry by curving the film with a radius of curvature (RoC) of 12.5 mm (Fig. 4.9a). Figure 4.9b shows current-voltage (I-V) curves of the photodiode under dark condition for planar and curved geometries, in which the bottom electrode (n-contact) was grounded. The measured dark current characteristics exhibit diode-like behavior and indicate that a mechanical deformation on the film and the devices hardly deteriorates and/or influences on its electrical characteristics. In addition, I also characterized photo-responses of the photodiode in planar and curved forms to light illumination with a wavelength of 532 nm as shown in Figs. 4.10a,b. The photodiodes in planar and curved geometries reveal nearly identical optoelectrical characteristics, which is clearly displayed in a graph of photocurrents as function of incident light power (Fig. 4.10c). As such, the mechanical deformation even with an extreme RoC of my exfoliated films barely change their electrical and

optoelectrical properties; thereby prepared films can be utilized to fabricate curved imagers by integrating with a curved ROIC.

4.5 Integration of active layer with ROIC and sensor deformation

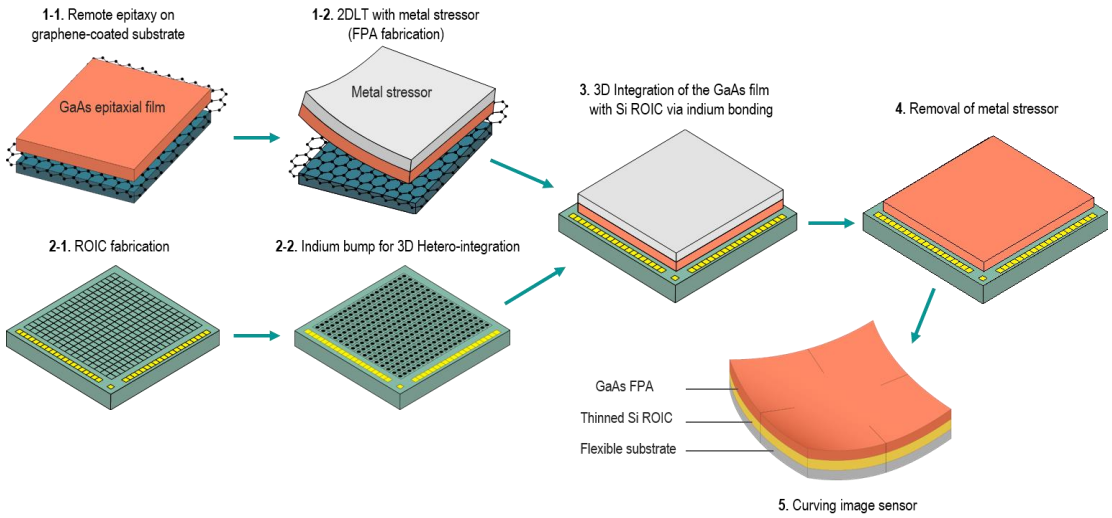

Figure 4.11. Schematic illustration of a fabrication process flow of the heterogeneous integration of a thin-film GaAs FPA with a thinned Si ROIC for an IR conformal image sensor.

The process flow for the heterogeneous integration of GaAs focal plane array (FPA) with readout circuit integrated circuit (ROIC) is described in Fig. 4.11. The designed GaAs active layer is grown by the remote epitaxy on a graphene-coated GaAs substrate followed by deposition of a metal stressor, and the grown film is exfoliated with a thermal release tape. The exfoliated film is fabricated into the focal plane array by using the previously developed process. Meanwhile, a ROIC is fabricated by a 90-nm FDSOI

poly-gate process with an ultra-shallow trench isolation, both low-and mid-threshold-voltage transistors designed for use in digital and analog applications. Next, the thickness of the ROIC is thinned down to a few tens of micrometers to efficiently curve the ROIC. Then, indium bump is patterned and deposited on the ROIC. The prepared focal plane array and ROIC are hybridized via an indium bumps bonding process aligning the focal plane array onto the indium bumps on the ROIC. After the hybridization, the thermal release tape and metal stressor are respectively removed by increasing temperature above critical temperature of the tape and Nickel/Titanium etchant. Finally, the integrated image sensor is curved into a hemispherical shape.

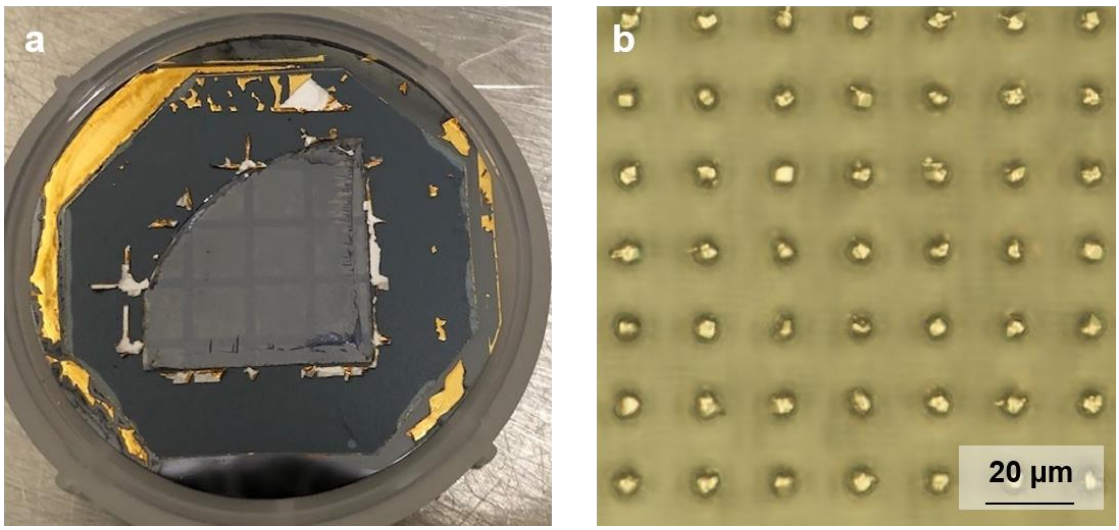

Figure 4.12. **a**. Optical image of indium bump pattering on a GaAs photodetector film on a thermal release tape. **b.** Optical microscope image of indium bump patterns on the GaAs photodetector film.

With the remotely grown and exfoliated epitaxial photodetector films, I first patterned indium bumps. Since the release temperature of the thermal release tape is 140 C, I develop indium bump patterning process with a low process temperature (<100 C) to avoid release of thermal tape during the process. Photolithography was performed with a Futurrex NR9 8000 photoresist in which baking temperature is 100 C. Ti/Au/Pt/Au (2/200/50/50 nm) was deposited as the under bump metallurgy (UBM) layer followed by deposition of 6 µm indium layer. Then, acetone spray with the air brush guns to lift-off metals starting in the epi and angle outward to minimize undercutting the epi-tape interface which would delaminate the epi. Figures 4.12a,b show an optical image and microscope image of a GaAs photodetector film with indium bump patterns. After the indium bump patterning process, the film was diced out into 8 mm by 8 mm pieces for the indium bump bonding process (Fig. 4.13).

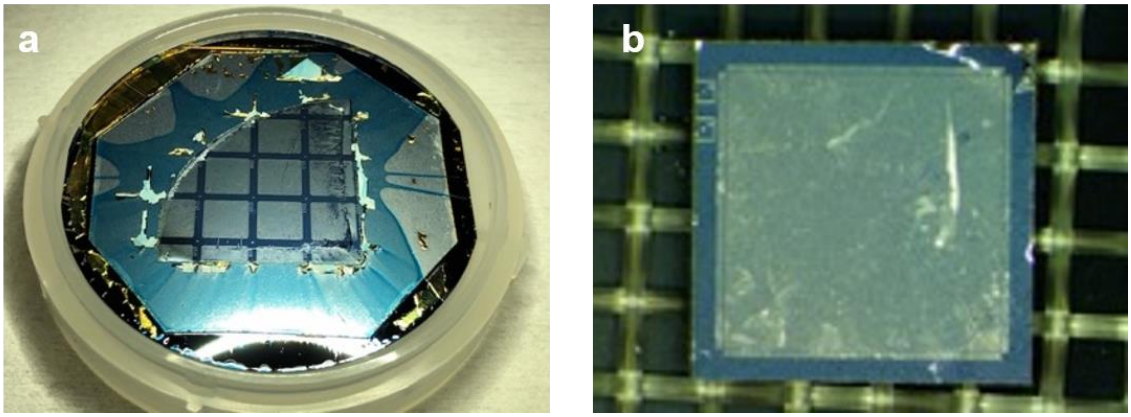

Figure 4.13. **a**. Optical image of the diced GaAs film with indium bump patterns. **b.** Optical image of an 8 mm by 8 mm piece of the diced GaAs film with indium bump patterns.

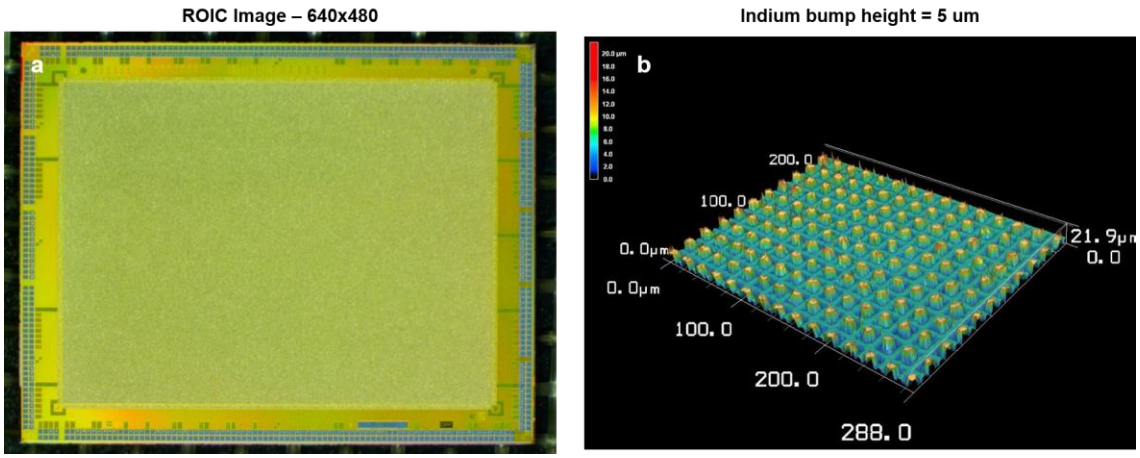

Figure 4.14. **a** 640 x 480 20 µm-pitch ROIC with indium bump patterns. **b.** 3D optical profile image of indium bump patterns on the ROIC.

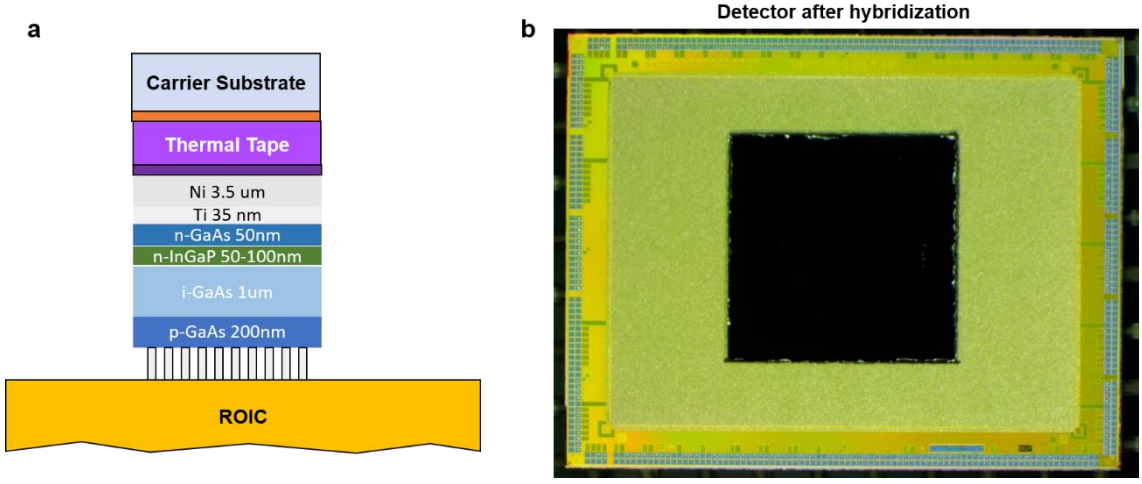

Figure 4.15. **a** Schematic illustration of the integrated photodetector film with the ROIC by indium bump bonding. **b** Optical image of the ROIC integrated GaAs photodetector film.

Next, I prepared 640 x 480 20 µm-pitch ROIC by Lincoln lab ROIC fabrication process, and deposited 5 µm height indium bumps on the ROIC with same

photolithography and metal lift-off processes. (Fig. 4.14). Subsequently, the photodetector film was hybridized with the ROIC employing an indium bump bonder where the film and ROIC were precisely aligned and then 10 kg force was applied to the sample heating to 90 C. Figures 4.15a,b, respectively, show a schematic illustration and optical image of the integrated photodetector film with the ROIC by the indium bump bonding. After the bonding process, a carrier Si wafer was removed by releasing thermal tape at 140 C. Then, ROIC was under-filled with an epoxy to strongly hold the film and simultaneously encapsulate the indium bumps, and Ti/Ni metal stressor was etched by wet etch process (Fig. 4.16a). The GaAs imager was packaged for characterizations (Fig. 4.16b).

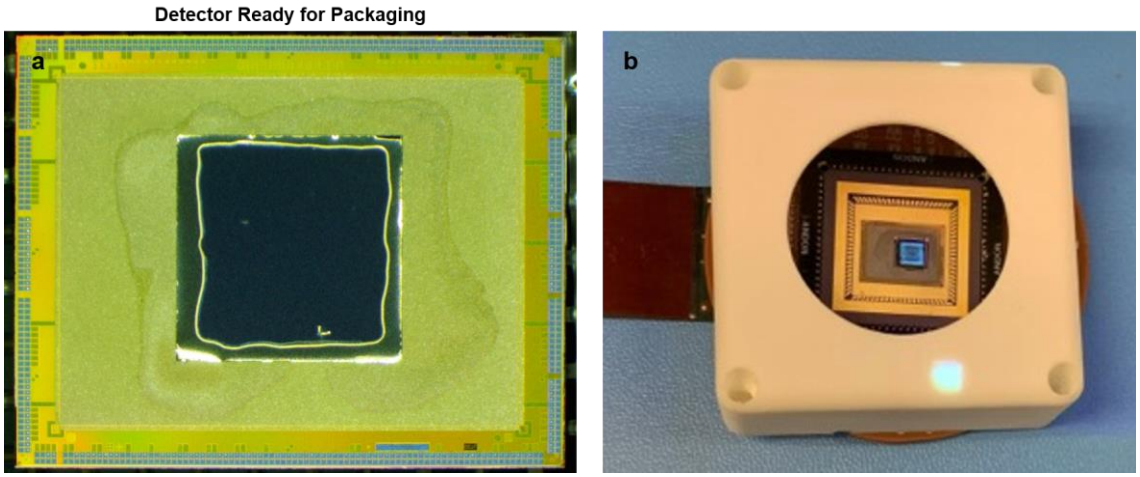

Figure 4.16. **a** Optical image of packaging-ready imager after under-filling ROIC with an epoxy, and removing Ti/Ni/Thermal tape. **b** Optical image of the packaged GaAs imager.

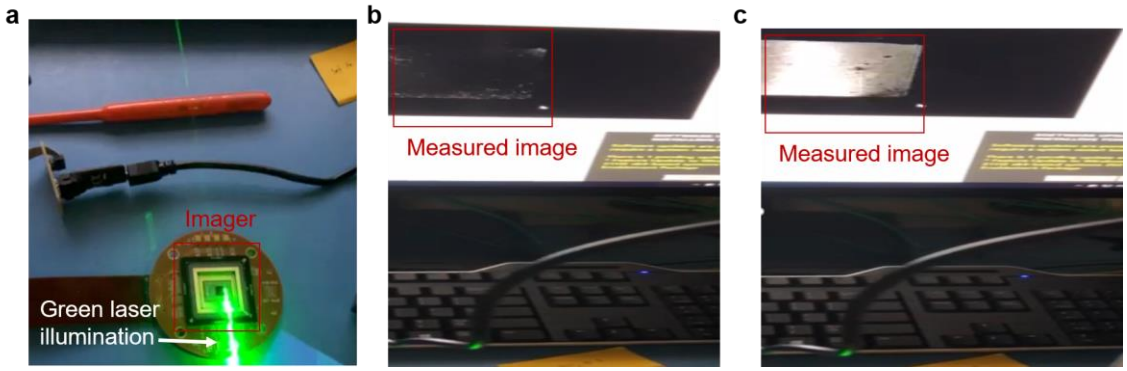

Figure 4.17. **a** Optical image of experimental setup for characterization of the packaged imager. 532 nm of diode laser was illuminated on the imager. **b,c** Measured images on a computer screen under (**b**) dark and (**c**) green laser illumination.

With the packaged GaAs imager, I demonstrate imaging capability by operating ROIC to readout photocurrent from the GaAs film under illumination of 532 nm diode laser. Figure 4.17a shows experimental setup for characterization of the packaged imager, where laser light was swiped over the image sensors. Under dark condition, no image was measured by the imager (Fig. 4.17b). Meanwhile, bright image was measured under 532 laser illumination condition as shown in Fig. 4.17c.

4.6 Future plans

I have developed methods for i) remote epitaxy growth and exfoliation of III-V thin film for a focal plane array, ii) fabrication of photodiodes using the exfoliated film, and iii) thinning and curving the ROIC. Then, I will combine all developed methods to integrate the thin film focal plane array with the thinned ROIC, and demonstrate

aberration-free IR imaging with less optic components taking advantage of the curved geometry.

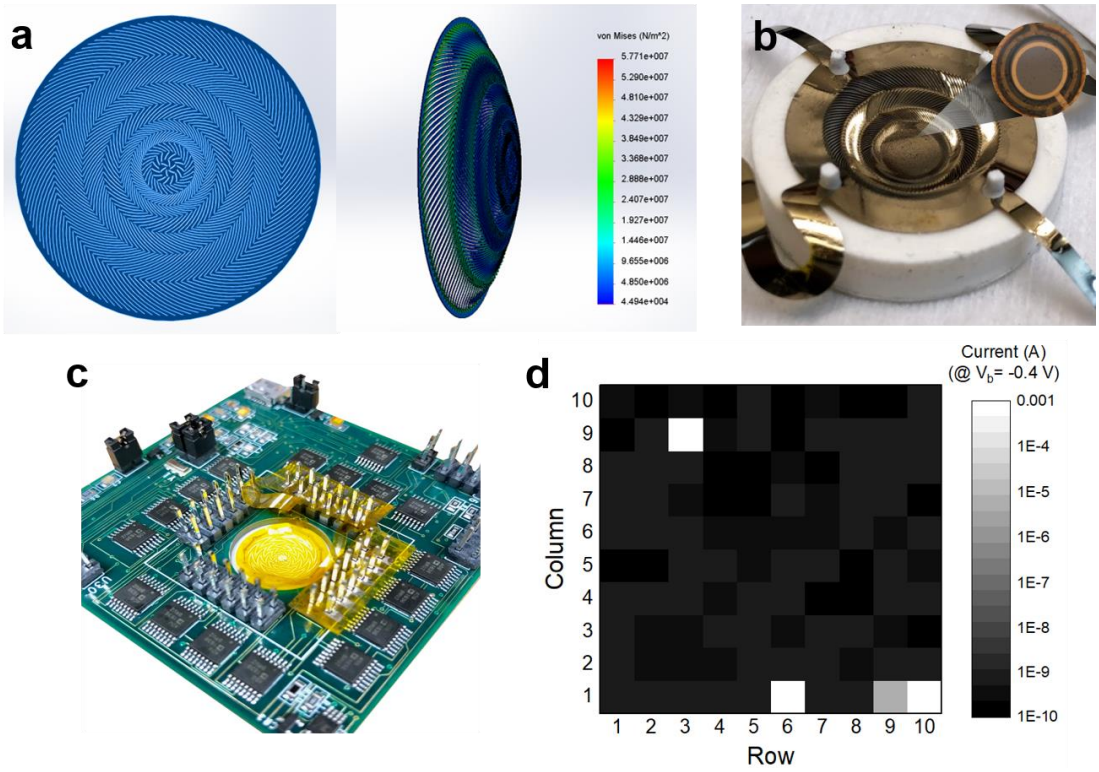

Figure 4.18. **a.** Mechanical deformation simulation of the designed kirigami cut pattern (Left: top view; Right: side view). **b**. Kirigami patterned Kapton substrates on a concave hemispherical sample holder, demonstrating effective deformation of the thin film with Kirigami cuttings. **c.** Customized PCB measurement system with a mounted Kapton dummy device on a concave hemispherical sample mount. **d.** Dark current and photocurrent mapping of fabricated 10x10 GaAs focal plane array on a Kapton substrate. (log scale, V_b= -0.4 V). Yield is over 95 %.

Furthermore, I will employ the Kirigami technique to demonstrate hemispherical 1P-1R focal plane array with an extreme small RoC. Figure 4.18a shows a mechanical simulation for the expected hemispherical shape of the deformed substrate with the my designed unique Kirigami cutting lines where the curvature of the hemispherical structure is enough to be used as the focal array with extreme RoC of 12.5 mm. With the simulated Kirigami design, the Kapton substrate with the fabricated 10x10 GaAs photodetector array was etched along with the Kirigami cut pattern as a preliminary work (Fig. 4.18b**),** where the photodetectors in the focal plane array had a p-i-n photodiode structure and the active layers were transferred via cold-weld bonding and ELO process. The etched and deformed hemispherical focal plane array was mounted on a customized printed circuit board (PCB) measurement system with a concave hemispherical sample mount (Fig. 4.18c) to characterize the GaAs focal plane array without a backplane readout circuit. Fig. 4.18d shows a contour plot of the measured dark current of the 10x10 array at V_b = -0.4 V, where the fabrication yield is over 95 %. This hemispherical FPA will be integrated with ReRAMs as the similar way developed in Chapter 3 to realize a light-weight, compact smart image sensor with in-sensor computing functionality.

4.7 References

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