Low-Phase Noise RF and Microwave Circuits for Hybrid Electronic-Photonic Microwave Frequency Synthesis

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(ABSTRACT)

Microwave signals with low phase and timing noise are critical for multiple fields of wide scientific, technological, and societal impact. This includes the areas of precision timekeeping, navigation, communications and radar-based sensing. Conventional high-performance electrical oscillators rely on a resonator to achieve low-phase noise performance; however, the quality factor of the resonator limits the purity of the signal generated by these oscillators.

On the other hand, photonic-based microwave generation approaches such as Optical Frequency Division (OFD) have drawn significant attention due to their unique ability to overcome some of the conventional oscillator's limitations and outperform their traditional counterparts, state-of-the-art electronic oscillators by several orders of magnitude. However, this superior performance comes with restricted tunability that is often in the range of a few percent. As a result, frequency synthesis faces a trade-off between achieving low noise, broad, and fast tunability.

To leverage the benefits of low-phase noise photonic techniques while maintaining the low additive noise characteristics of the generated microwave signal, a low phase noise electronic frequency synthesizer driven by a photonic oscillator is essential, which ensures the extension of the frequency range of the generated microwave signal to several frequency bands.

A conventional electronic frequency synthesizer is based on the Phase Lock Loop (PLLs) technique, which face limitations on bandwidth and frequency tuning resolution. On the other hand, Direct Digital Synthesizers (DDSs) are widely used for their tuning range and phase noise performance, yet they suffer from the drawback of limited bandwidth. Therefore, this dissertation aims to explore the challenges associated with low-phase-noise microwave signal generation and introduce multiple effective techniques to achieve ultra-low phase noise performance across a wide frequency range.

High-performance radar and communication systems rely highly on the phase noise performance of the microwave signal, and the additive noise of the amplifier limits the purity of the signal generated by electronic oscillators. Moreover, power amplifiers are essential components in the transmitter chain of a broad range of systems with applications covering wireless and mobile communication, and their phase noise can affect the error vector magnitude (EVM) of the signal and the bit error rate (BER) of a communication system. To achieve low additive phase noise and high efficiency across a wide frequency range, ultra-low-phase-noise and efficient amplifiers are essential. Consequently, this dissertation explores trade offs associated with low-phase-noise amplification and provides a detailed discussion of effective approaches to minimizing the phase noise in electrical amplifiers.

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Every journey has an end, and this dissertation marks the conclusion of one of the most transformative chapters of my life. I close one of the most challenging yet rewarding part of my life. This PhD has been more than just research—it has been a test of resilience, a lesson in collaboration, and a journey of growth. From designing circuits to navigating the electrical-photonic co-design, every challenge was met with the support of incredible mentors, colleagues, friends, and family. This dissertation represents not just years of research and hard work, but also the unwavering support of those who believed in me and I would like to take a moment to express my gratitude to those who made this journey possible.

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Chapter 1

Research Overview

1.1 Motivation

An oscillator is a fundamental circuit that generates a periodic sinusoidal signal without requiring an external input. As a critical component of various communication systems [3], oscillators play a key role in applications such as radar [4], navigation [5], modern wireless communication and their primary function is to provide a reference signal for synchronization and wave propagation [6].

There are several key parameters to characterize the performance of an oscillator, including power consumption, frequency tunability, and output power. However, the most crucial parameter in determining the performance of oscillators is frequency stability. Frequency stability represents the ability of oscillators to provide consistent frequency over time and is expressed in both the short-term and long-term domains.

Long-term stability refers to the frequency shift of an oscillator over a long period of time, typically a few days span. This gradual drift can result from several factors, such as aging, temperature variation, and long-term degradation, and it is expressed in parts per million or ppm [7]. Although long-term drift or instability can cause challenges for communication systems, usually it is compensated by using software adjustment and frequency recalibration.

Short-term stability, on the other hand, refers to frequency fluctuation over a short period of time ranging from a millisecond to a day. It is usually due to the noise within the oscillator output and expressed as phase modulation of the output signal [8]. Short-term stability can be expressed in both the time domain and the frequency domain. In the time domain, it appears as a shift in zero crossing point from an ideal case or "time jitter". In the frequency domain, it is characterized and described as phase noise, which describes the shape of the output waveform and purity of the generated signal. In general, the output voltage of the ideal oscillator can be expressed as:

$$V_{out}(t) = Acos[\omega_0(t) + \phi] \tag{1.1}$$

However, if we consider the fluctuation of the amplitude and phase the equation for the output voltage of the oscillator would describe as [8]:

$$V_{out}(t) = A(t)cos[\omega_0(t) + \phi(t)] \tag{1.2}$$

where the amplitude and phase fluctuation are functions of time and create a sideband close to the frequency of the oscillation in the frequency domain and create time jitter in the time domain as illustrated in Fig. 1.1 in both the time domain and frequency domain.

Phase noise is defined as the ratio of the noise power at a specific offset frequency to carrier power. It plays an important role in modern communication systems as high phase noise can degrade the overall system performance. This degradation can manifest in various ways, including degrading signal integrity, increasing timing errors, and synchronization errors in high-speed communication. As a result, the development of low-noise microwave signals are of significant importance and have attracted lots of attention in recent decades for their wide spectrum of applications such as radar and navigation systems [3].

In order to illustrate the impact of phase noise on a communication system a conventional RF receiver chain is shown in Fig. 1.2. The receiver chain consists of a Low Noise Amplifier (LNA), a RF mixer, a local oscillator (LO), and a low pass filter. The high-frequency RF signal is received

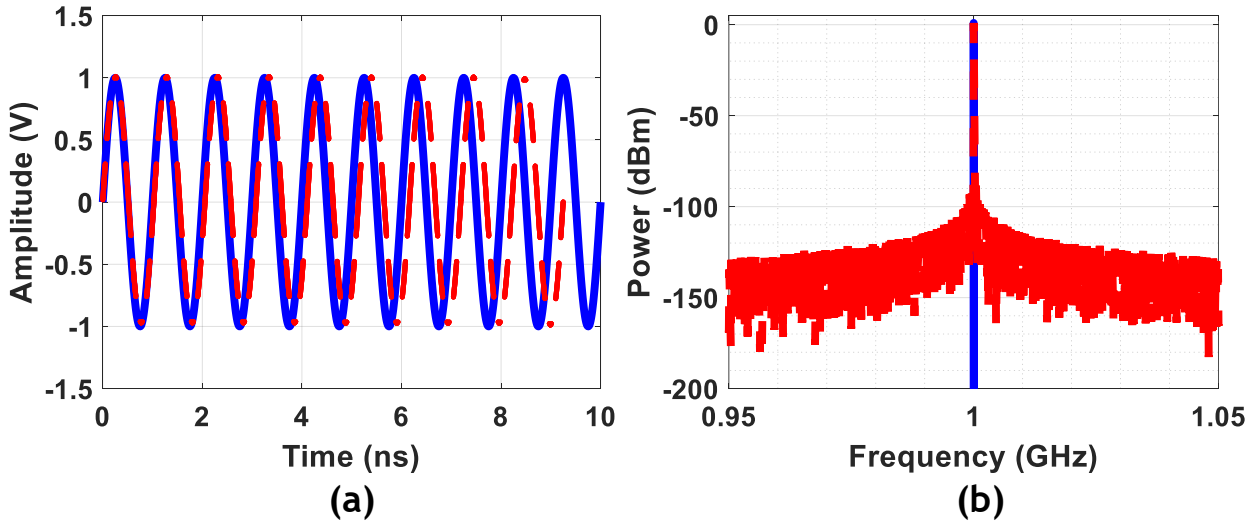


Figure 1.1: (a) Effect of short-term stability on sine wave in time domain represented by time jitter (σ_t). (b) Effect of phase noise on sine wave in the frequency domain.

through an antenna and amplified by the LNA, followed by frequency down conversion using a mixer, where the LO signal provided by the local oscillator is used to shift the signal to a lower frequency. The downconverted low-frequency signal then passes through a low-pass filter to remove unwanted harmonics, ensuring that only the desired baseband signal remains. This baseband signal can be digitized using an Analog-to-Digital Converter (ADC).

In an ideal scenario where the LO signal is noise-free or its noise is negligible, the intermediate frequency (IF) signal can still be detected even in the presence of a strong interferer at the RF input, as illustrated in Fig. 1.2(a). However, if the LO suffers from phase noise, the skirts generated by this noise can mix with both the RF input signal and interference, leading to corruption of the IF signal. In severe cases, phase noise can degrade the signal quality to the extent that the IF signal is lost entirely [9], as shown in Fig.1.2(b).

The degradation of a communication system due to phase noise can manifest on both the transmitter and receiver sides. The effect of additive phase noise from the local oscillator (LO) on the transmitter is illustrated in Fig. 1.3. Due to the phase noise of the local oscillator, their signals are corrupted, causing interference in adjacent channels on the receiver side.

Furthermore, data traffic transmission has experienced exponential growth over the past decade

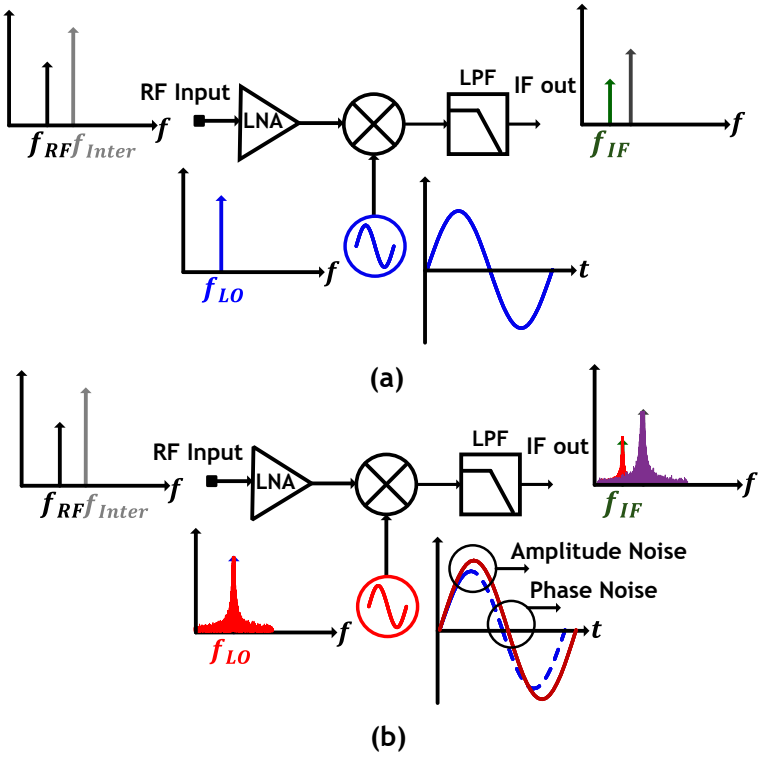


Figure 1.2: Down conversion of RF to IF with a large interference in (a) Noise free oscillator (b) Noisy oscillator.

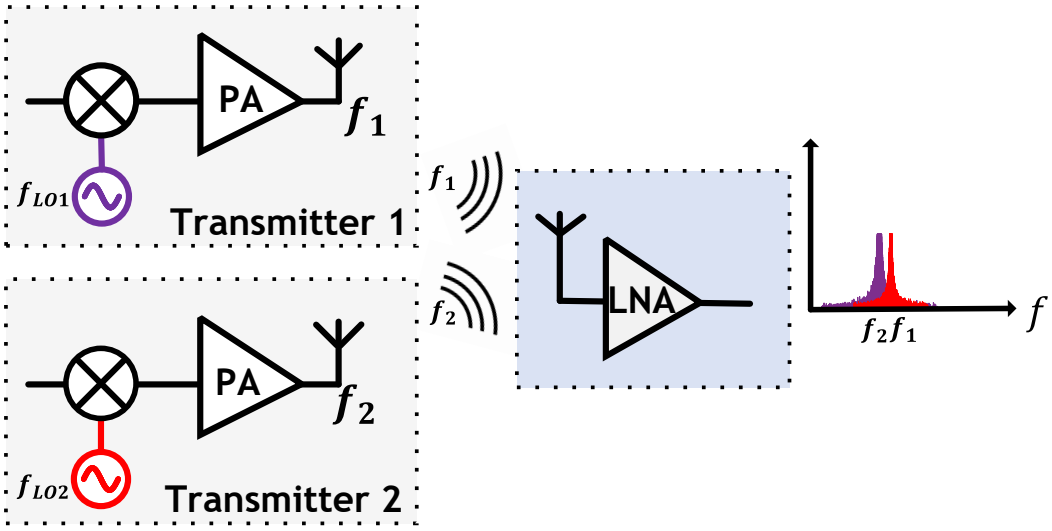


Figure 1.3: Effect of Phase noise in transmitter (TX) chain.

[10], as illustrated in Fig. 1.4(a). Meanwhile, with increasing interest in 5G / 6G communication systems and the increasing demand for high-bandwidth applications, such as virtual reality (VR) [11] and connected autonomous systems [12], data rates have grown accordingly [13] as shown in

Fig. 1.4(b). Consequently, improving spectrum efficiency has become a critical challenge that must be addressed. To address the aforementioned challenge, various approaches have been proposed in the literature. These include Orthogonal Frequency Division Multiplexing (OFDM) [14], which maximizes bandwidth utilization [15], the adoption of massive Multiple Input Multiple Output (MIMO) systems [16], and the transition to advanced digital modulation schemes such as 256-QAM or 512-QAM [9, 17].

Moving toward advanced modulation schemes improves spectral efficiency by enabling the transmission of more bits per symbol, effectively increasing the data rate without requiring additional bandwidth. However, this comes at the cost of increased noise sensitivity, making higher-order modulation schemes more susceptible to signal degradation and requiring a higher signal-to-noise ratio (SNR) for reliable communication [9].

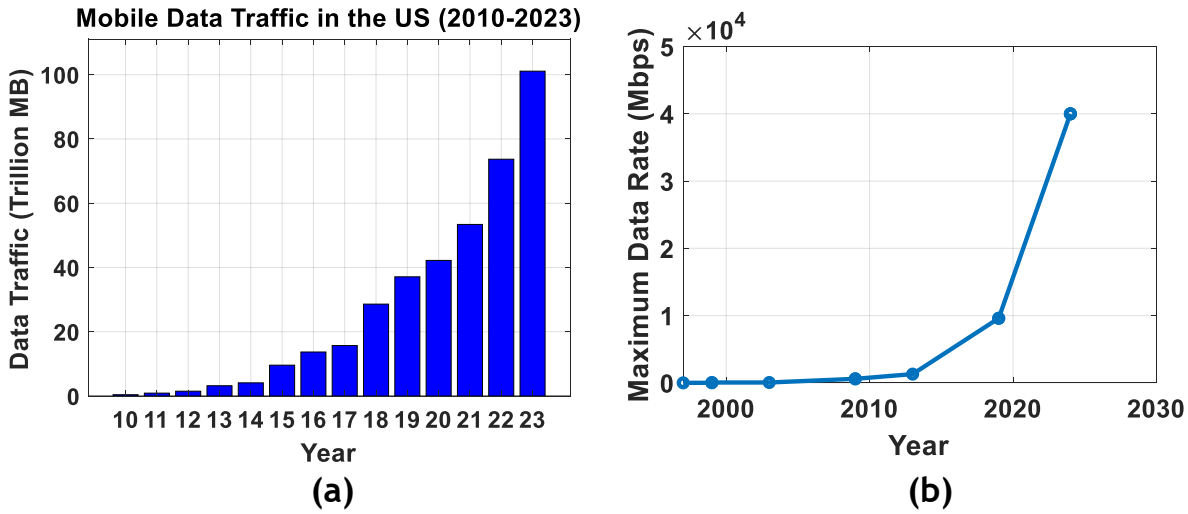


Figure 1.4: (a) Exponential growth of mobile data traffic over the past decades in USA (b) Maximum data rate for communication system.

One effective way to measure the sensitivity of communication system to noise is through Bit Error Rate or BER which quantifies the number of errors in compare with the total number of bits transmitted over a transmission channel. To illustrate the impact of noise on different modulation schemes, the BER and requirements for various communication systems are shown in Fig. 1.5(a). For instance, BER of (10^{-6}) is required for smooth video streaming. Achieving this level of BER required additional 13 dB more SNR in 256 QAM in comared with 16 QAM which required only

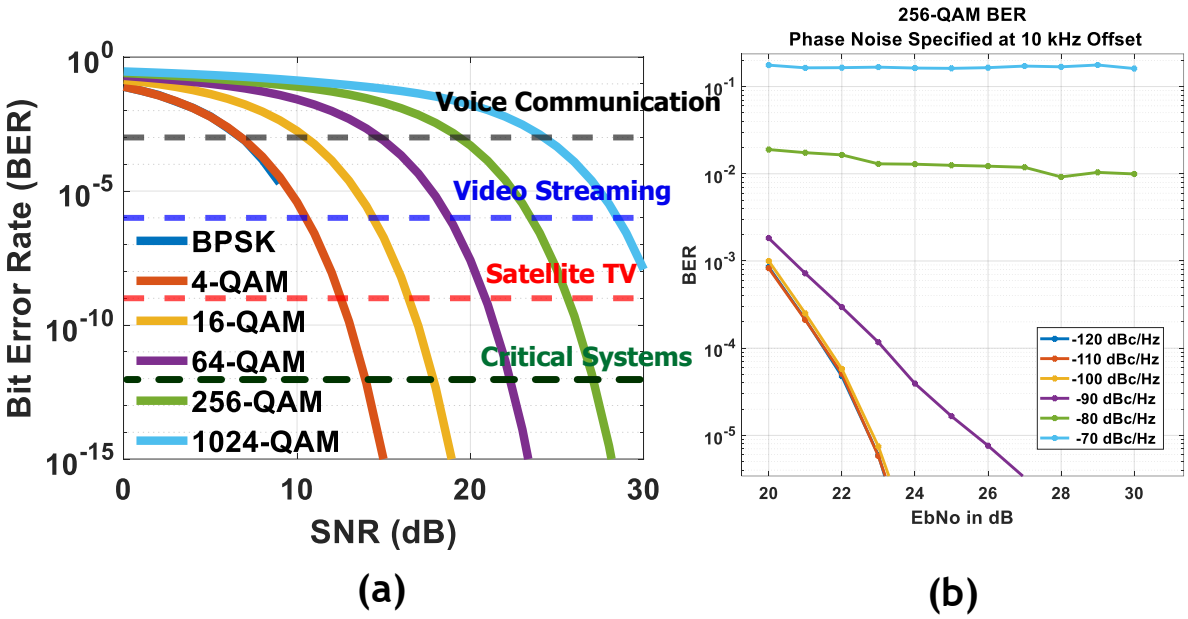


Figure 1.5: (a) Bit error rate (BER) versus E/N for different digital modulation schemes. (b) Effect of the phase noise on 256 QAM scheme modulation versus E/N.

11 dB of signal to noise ratio, highlighting the increased sensitivity of higher-order modulation schemes to noise.

Furthermore, in order to fully evaluate the effect of phase noise on BER and its potential degradation in digital communication systems, the additive phase noise was introduced to LO of such system. The resulting BER and SNR are plotted for 256 QAM in Fig. 1.5(b). The simulation results indicate that if the phase noise of LO is sufficiently high, even with improvements in SNR, the BER remains constant since phase noise becomes the dominant noise source, resulting in limiting performance regardless of SNR improvements.

Furthermore, Frequency Modulated Continuous Wave (FMCW) radar is widely utilized in autonomous vehicles [12], drone and UAV navigation [18], and medical applications [19] due to its capability to provide high-resolution range measurements and precise target and motion detection. FMCW radar operates by continuously transmitting a wave while varying its frequency over time.

The block diagram of an FMCW radar system is illustrated in Fig. 1.6, where a chirp oscillator generates a frequency-modulated signal that is transmitted toward the target. The transmitted signal

can be mathematically expressed as:

$$f_{TX}(t) = f_c + \frac{B}{T_C}t \tag{1.3}$$

where:

- f_c is the carrier frequency,
- B is the bandwidth of the chirp, and
- T_C is the chirp duration (transmission time).

Since the signal propagates to the target and reflects back to the receiver, there is a time delay due to the round-trip travel time. As a result, the received signal is a delayed version of the transmitted signal and is given by:

$$f_{RX}(t) = f_c + \frac{B}{T_C}\left(t - \frac{2R}{c}\right) \tag{1.4}$$

where as R is the range to the target. Finally, after down conversion and filtering, the resulting IF frequency is expressed as:

$$f_{IF} = \frac{2BR}{cT_C} \tag{1.5}$$

The time-domain and frequency-domain representations of the TX and RX signals along with IF frequency are plotted in Fig.1.6.

Additive phase noise of the LO can significantly impact the performance of an FMCW radar system, degrading overall radar precision [20]. Additionally, it can introduce side lobes, making object detection difficult or even nearly impossible [21]. As a result, reducing the additive phase noise of oscillators is a critical challenge that must be addressed appropriately to enhance radar accuracy and reliability.

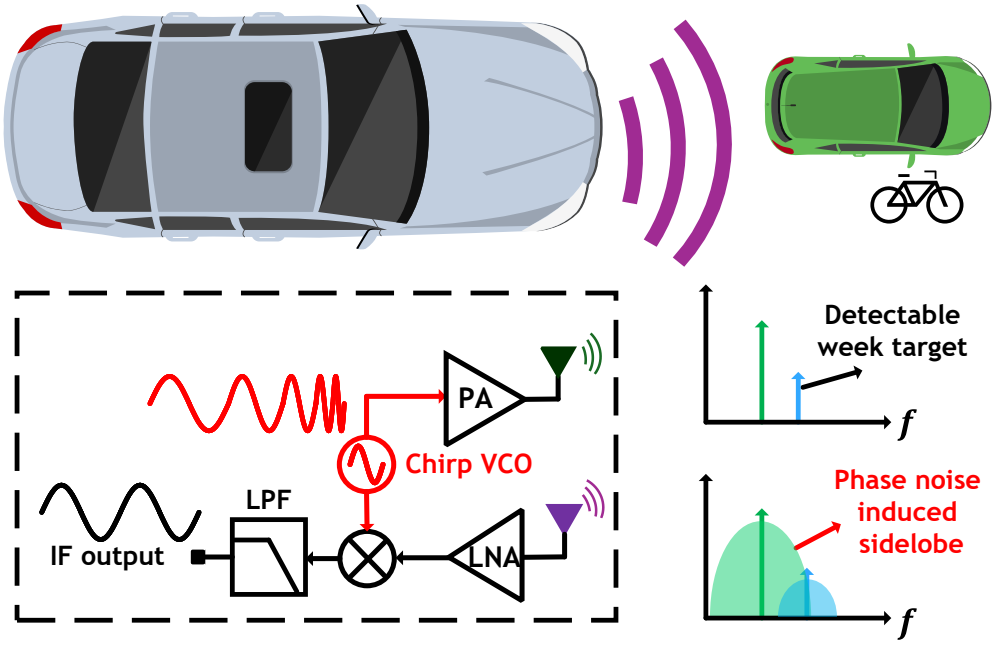


Figure 1.6: Transceiver architecture of an FMCW radar system, along with the time-domain and frequency-domain representations of both the TX and RX signals.

As a result, this dissertation aims to address the challenges associated with low-phase-noise microwave signal generation and introduce multiple effective techniques to achieve ultra-low phase noise performance over a wide frequency range. Furthermore, given the impact of additive phase noise from electrical components such as amplifiers and frequency dividers on microwave signal generation—and their critical role in communication systems—this dissertation explores various methods in detail to suppress the additive noise of these components while maintaining low power consumption and a compact form factor.

1.2 Prior Art

1.2.1 RF and Microwave Frequency Synthesizer

The operation principle of a frequency synthesizer is to generate any range of frequencies(f_{out}) from a fixed single-tone frequency (f_{in}). Multiple ways have been introduced in the literature to frequency tunability, each offering its own advantages and trade-offs.

One of the simplest methods for generating microwave signals is through fully electrical oscillators, such as Colpitts oscillators, cross-coupled oscillators, or ring oscillators [22]. These oscillators are commonly used to generate microwave and millimeter-wave signals. In order to achieve tunability in fully electrical oscillators, a control voltage is usually applied to the circuit, shifting the oscillation frequency. Typically, a capacitor bank or varactor is incorporated into the resonant tank of cross-coupled or Colpitts oscillators. This setup effectively changes the capacitance in response to the applied control voltage, resulting in a shift in the operating frequency, which is highly dependent on the control voltage. In order to expand the tuning range, a larger varactor is required; however, this approach comes with a higher noise trade-off, which can degrade signal quality and negatively affect oscillator phase noise [22, 23]. A simplified model of a traditional free-running oscillator, consisting of a gain medium and a resonator with positive feedback, is illustrated in Fig. 1.7(a).

While fully electrical oscillators provide benefits such as low power consumption and fast response time, they usually suffer from low-frequency resolution, and long-term drift [9, 24]. Additionally, their phase noise is limited to the phase noise of their active gain stage and the quality factor of the resonator as described in equation .1.6. Consequently, free-running oscillators typically exhibit high short-term stability and phase noise [25] as depicted in Fig .1.7(b).

$$\mathcal{L}(f_m) = \frac{F k_B T}{2P_s}\left(1+\frac{f_L}{f_m}\right)\left(1+\frac{f_c^2}{f_m^2}\right), \tag{1.6}$$

where:

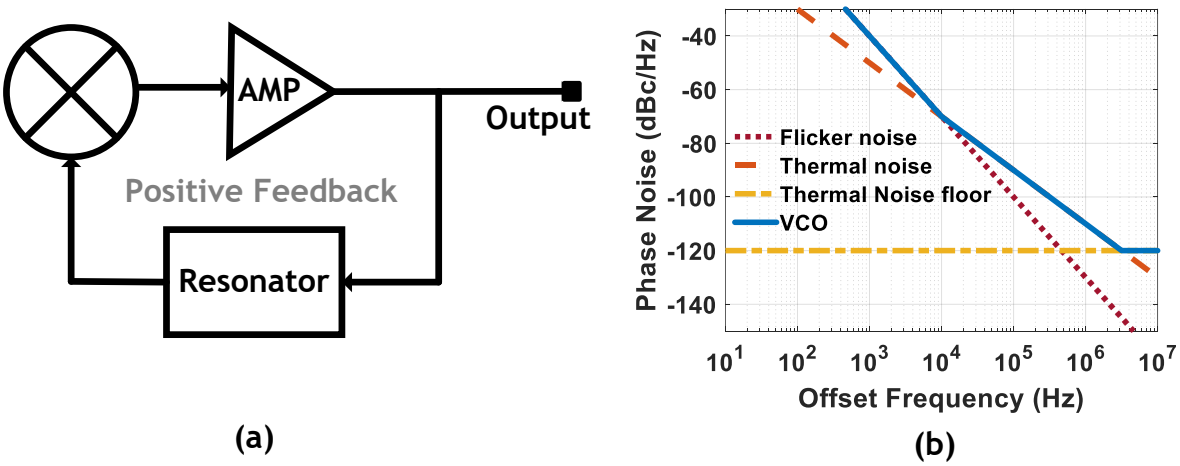


Figure 1.7: (a) A simplified model of free-running oscillator including a gain stage and positive feedback system (b) General model of VCO phase noise including $\frac{1}{f^3}$ and $\frac{1}{f^2}$ behaviors.

- f_m is the frequency offset from the carrier,
- F is the noise factor of the active device,
- k_B is Boltzmann's constant,
- T is the temperature in Kelvin,
- P_s is the signal power,
- f_L is the flicker noise corner frequency,
- f_c is the oscillator's resonant frequency divided by the loaded quality factor Q_L.

In order to overcome some of the above-mentioned limitations associated with free-running VCOs, frequency, and phase-locked systems have been extensively studied and implemented in the literature [26,27]. The block diagram of a Phase Locked Loop (PLL) system is illustrated in Fig. 1.8(a), whereas a high-frequency free-running VCO is locked to a lower frequency cleaner reference signal by using a frequency divider and phase frequency detector. In the PLL, the phase detector compares two input signals and calculates the phase difference between the reference signal and

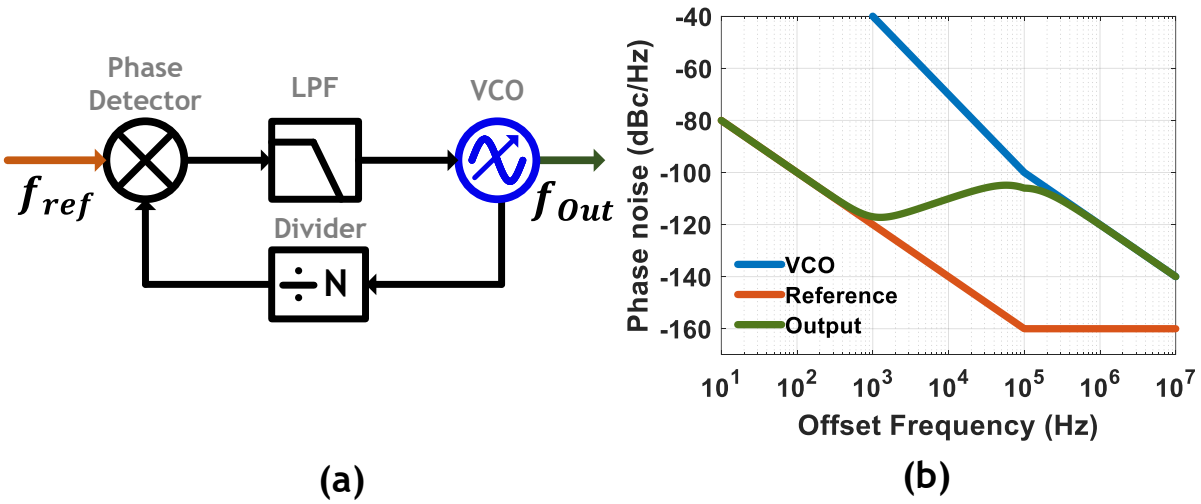


Figure 1.8: (a) PLL architecture. (b) Output Phase noise of PLL assuming noisy VCO and clean reference.

output loop signal. The feedback loop in the system causes one signal to track another one, and keeps the reference signal phase and frequency synchronized with the output signal.

Although PLL can suppress the additive phase noise of free-running VCOs and mitigate frequency drift of such systems, they introduce constraints such as setting time and low frequency resolution [28] while they substantially increase the power consumption and system complexity. The achievable locking bandwidth of a PLL, which is typically determined by the loop filter design, typically ranges from a few hundred Hz to several kHz. The bandwidth defines the ability of the locking loop to suppress the additive phase noise of VCO and align it with reference phase noise as illustrated in Fig.1.8(b). The additive phase noise of a PLL system versus offset is plotted in Fig .1.8(b) where as within the loop bandwidth, the phase noise of the VCO is effectively reduced; however, outside this bandwidth, the total phase noise of the PLL follows the original phase noise of the VCO.

Although most state-of-the-art low-noise electronic frequency synthesizers are based on PLLs [26, 27], frequency synthesizers based on Direct Digital Synthesis (DDS) are attracting more and more attention due to their ability to achieve low phase noise, precise frequency resolution, and fast switching time [29, 30]. The DDS architecture, which is shown in Fig. 1.9, has four key components: phase accumulator, phase-amplitude converter, Digital Analog converter (DAC), and

reference source, At each clock the phase accumulator computes a new phase-based on the referenced signal and tuning word and look up table or phase to amplitude converted, converted the phase to digital amplitude which finally would be converted to analog voltage or current through DAC [31].

DDS functions as a variable frequency divider, where the input frequency is divided down to the desired output frequency based on the tuning word. Thus, the additive phase noise of a DDS can be approximated as by a frequency divider until it reaches the phase noise limitations of the DAC. Additionally, due to DDS's digital nature, the output frequency of a DDS is limited by the Nyquist theorem and is susceptible to high spurs levels.

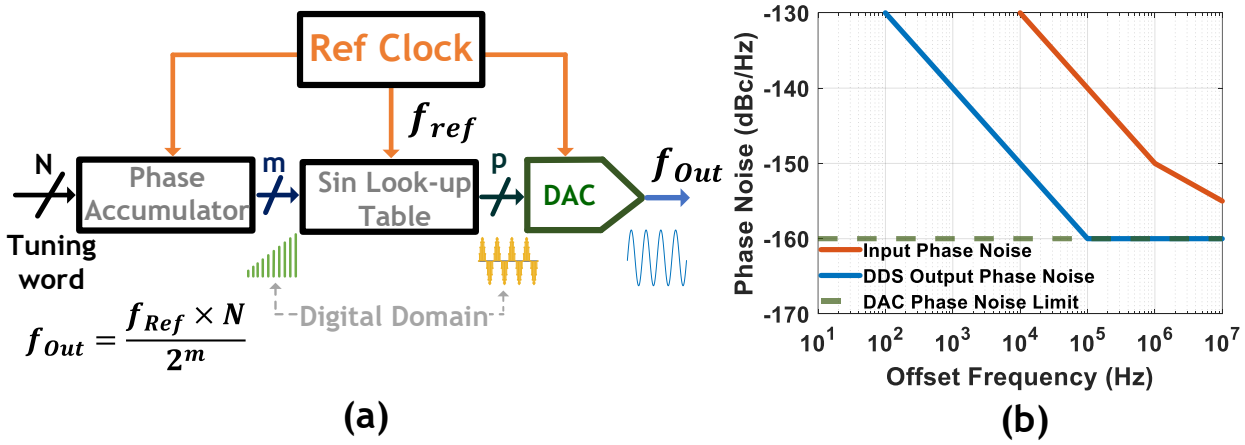


Figure 1.9: (a) DDS architecture. (b) Output phase noise of DDS.

Meanwhile, generating ultra-low phase noise microwave and mm-wave signals through optical methods has been gaining increasing attention due to the unique advantages they offer. Photonic lightwave systems provide significant benefits over more conventional electronic approaches for generating low-noise microwaves. In particular, the extremely low loss and high-quality factors of photonic resonators are fundamental to achieve the lowest noise and highest spectral purity [32]. Furthermore, the introduction and rapid development of frequency combs in the last few decades enable seamless coherent synthesis across the full EM spectrum [33]. Among various optical techniques, Optical Frequency Division (OFD) has demonstrated the highest potential for achieving ultra-low phase noise performance. OFD effectively translates the frequency stability of 200-500

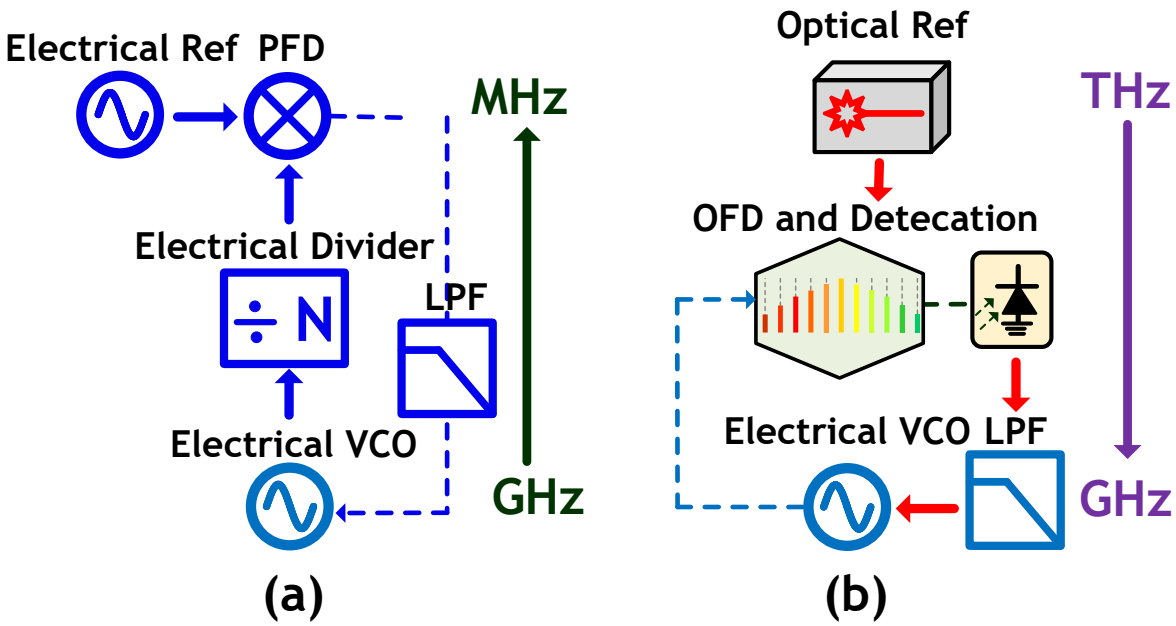


Figure 1.10: (a) PLL system (GHz VCO divide down to be compared with MHz reference). (b) OFD system (THz reference divide down to be compared with GHz VCO).

THz optical carrier frequency down to a 10 GHz microwave, enabling long- and short-term stability [34]. This technique demonstrates exceptionally low noise performance, reaching approximately -160 dBC/Hz at 10 KHz offset from 8 GHz carrier [35].

A comparison between traditional fully electrical PLL systems and OFD systems is illustrated in Fig.1.10. In the PLL system, the VCO signal is divided down to be compared with low-frequency electronic reference. In contrast, in the OFD system, the microwave signal from a VCO is multiplied up to be compared with an optical frequency reference [36].

Most of OFD systems rely on a stable optical frequency reference, typically a laboratory fiber or solid state laser that is frequency-stabilized to a Fabry-Pérot (F-P) cavity [32]. A detailed block diagram of OFD system is shown in Fig .1.11. Two semiconductor lasers are self-injection locked (SIL) to spiral resonators whose optical modes are aligned, using temperature control, to the modes of the high-finesse F-P cavity for PDH locking. A microcomb is generated in a coupled dual-ring resonator and is heterodyned with the two stabilized lasers. The resulting beat-notes are mixed to produce an IF. The IF is phase-locked by feedback to the current supply of the microcomb

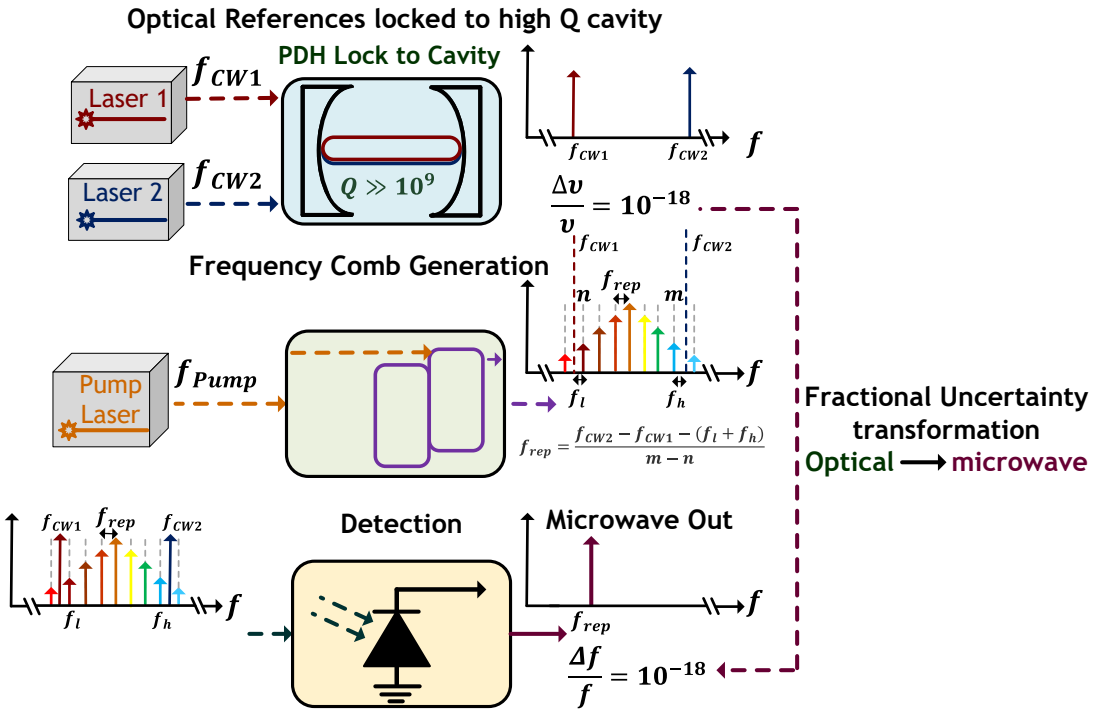


Figure 1.11: Deatiled block diagram of OFD system

seed laser, and finally, a photodetector is used to convert the microcomb's optical output into a microwave signal.

Although low noise microwave signal generation through optical methods offers high potential and outperforms the electrical methods by several orders of magnitude in terms of phase noise, they are constrained by their frequency tunability [37]. Additionally, high power consumption and large physical size are big limiting factors for their widespread adoption. Consequently, the ability to generate a widely tunable microwave frequency signal with low additive phase noise, while maintaining low DC power consumption and a compact footprint, is crucial. Addressing these challenges is the primary focus of the DARPA-sponsored CHROME project, described below.

The Coherent Heterodyne Robust Optical Microwave Emitter (CHROME) project aimed to promote a technical revolution for electrical optical systems to improve the conventional method of microwave frequency synthesis. Optical-driven microwave synthesizer is not a new area of research however the cost, size, and power consumption of components restricted the usage of these

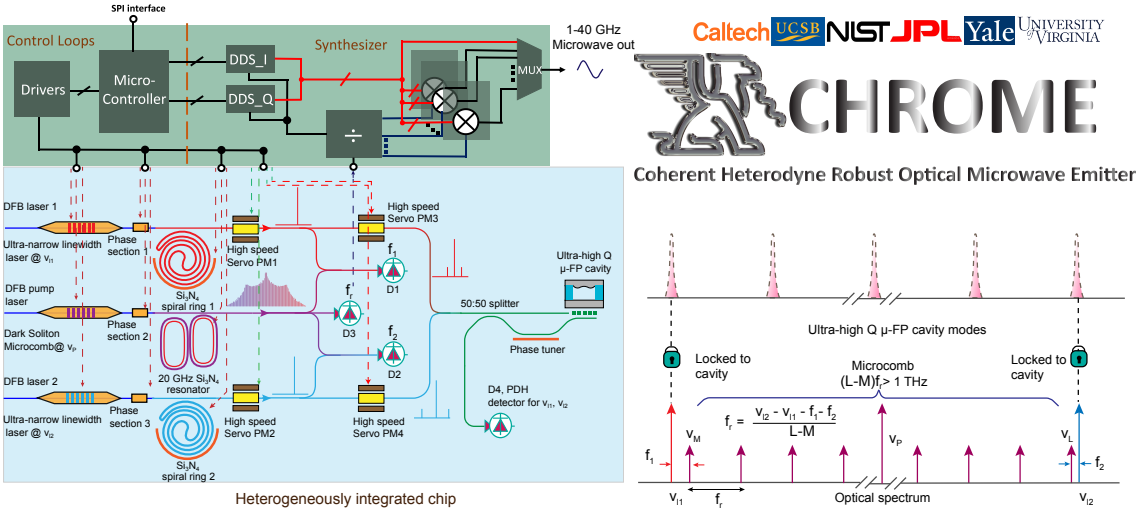


Figure 1.12: CHROME architecture for microwave generation.

systems [38]. The primary goal of the project is to combine all the optical components, including tunable lasers, optical combs, micro-Fabry-Perot (μ-FP) cavity, photodiode along with all of the electronic synthesizer, and control loop into a small package on the order of 10 cm^3 while consuming under 10 W of DC power to generate a clean, highly tunable microwave signal.

As much of the work in this proposal was pursued in direct relation to the CHROME project as part of a multi-organization team, the overall system is discussed here briefly to describe the motivation behind the work. Prior OFD system uses solid-state lasers and bulky evacuated Fabry-Perot (FP) cavity. To address these drawbacks, an effort to integrate high-performance III-V materials and silicon and a new F-P concept that can be chip-integrated without the need for high-vacuum enclosure was made [39, 40], Additionally, the frequency noise of two semiconductor laser is reduced by self-injection locking (SIL) to high-Q Si_3N_4 spiral resonators [41]. The overall architecture of the CHROME system is shown in Fig. 1.12. The system utilizes three low-noise continuous wave laser self-injection locked to ultra-high Q spiral ring resonators [42, 43].

The third DFB laser enables the generation of solution microcomb in order to achieve ODF. After two lasers locked at ν_{l1} and ν_{l2}, modes m and n of the microcomb would be phased locked to ν_{l1} and ν_{l2} by small RF offset beats f_1 and f_2. The beat note between the microcomb and each of CW laser are given by: $f_{\mathrm{b1}} = \nu_0 - n \cdot f_{\mathrm{rep}} - \nu_{\mathrm{CW1}}$ and $f_{\mathrm{b2}} = \nu_{\mathrm{CW2}} - \nu_0 - m \cdot f_{\mathrm{rep}}$ as a result, these beat

notes mix together to generate the intermediate frequency and as a result, microwave generation through the 2-point OFD can be realized and can be expressed using the following equation:

$$f_{\text{rep}} = \frac{\nu_{\text{CW2}} - \nu_{\text{CW1}} - f_{\text{IF}}}{n+m}. \tag{1.7}$$

Finally, the f_{rep} will be fed into a compact, broad-band frequency synthesizer through a photodiode to achieve low additive phase noise, highly tunable output tone.

Therefore, there is a need for an ultra-wide band frequency synthesizer that exhibits low phase noise performance, ensuring that the purity of the generated signal through optical methods does not degrade.

1.2.2 Low Additive Phase Noise Power Amplifier

As discussed above, the phase noise performance of the oscillator plays an important role in a wide spectrum of applications such as radar systems, communication, and navigation systems and the additional noise from an amplifier along with the quality factor of the oscillator tank will cause phase noise reduction. Moreover, the additive phase noise of the amplifier can affect the error vector magnitude (EVM) of the signal and the bit error rate (BER) of a communication system.

Multiple approaches can be used to achieve low residual phase noise in amplifiers.One such approach is to use technologies that inherently have a low flicker (1/f) noise [44, 45]. Heterojunction bipolar transistors benefit from low-frequency noise in comparison with field effect transistors (FETs) [44] and thus are a good choice for low-phase noise applications. The second approach to reduce the additive phase noise of the amplifier is to suppress the upconverted near carrier frequency noise due to the nonlinearities effect of the amplifier itself [44, 46–48] which can be achieved using feedforward, feedback, and parallel techniques [44, 46], however, most of discuss technique highly suffers from large physical size and efficiency,

As a result, the need for a compact and efficient power amplifier with low additive phase

noise over a broad spectrum range is necessary.

1.3 Dissertation Organization

1.3.1 Thesis Statement

The cointegration and co-packaged of electrical and optical components provide significant advantages across various applications, including wireline and wireless communication, GPS and navigation, and radar systems. By leveraging the strengths of both domains, an ultra-low phase noise frequency synthesizer is achievable. Specifically, the low phase noise characteristics of optical components, combined with the fine tunability and wide bandwidth offered by electrical components, enable these systems to meet the stringent noise performance and high-speed requirement demanded by emerging applications such as high-speed optical communication systems, light detection and ranging (LiDAR), navigation, and advanced detection systems.

This dissertation addresses the conventional limitations and challenges of low-phase-noise microwave signal generation by introducing multiple effective techniques to achieve ultra-low phase noise over a wide range of frequencies. By employing several stages of frequency dividers and leveraging a DDS-based system, the proposed synthesizer achieves ultra-low phase noise performance and covers a frequency range spanning over four octaves in a SiGe BiCMOS process. Additionally, this dissertation proposed and implemented several ultra-low-phase-noise, high-bandwidth InP HBT circuits, including frequency dividers, to push the boundaries of divider performance. These advancements challenge the status quo by achieving lower phase noise and reduced DC power consumption, ultimately enhancing the performance of phase-locked loops and electro-optic circuits and systems.

In addition, a low additive phase noise power amplifier with high efficiency and linearity will improve the error vector magnitude (EVM) of the signal and bit error rate (BER) of a communication system.

The design technique to be utilized in this research for achieving the state goal is mentioned as follows: A modified version of feed-forward low noise amplifier is designed to further reduce the additive phase noise of the amplifier with a highly compact form factor to reduce the cost of the chip and improve the BER of the communication system, A wideband power combined parallel power amplifier with a compact form factor is designed to achieve high efficiency and low additive phase noise in both InP and SiGe processes.

1.3.2 Research Questions

The dissertation proposal will focus on the following research questions:

- **Research Question 1.** What are the current tradeoffs and bottlenecks limiting tuning range, phase noise, and form factor within electronic and electro-optic systems and circuits used for wideband microwave synthesizers?
- **Research Question 2.** What co-design methodology and tradeoff is employed to effectively integrate photonic integrated circuits and electronic synthesizers, to take advantage of low-phase noise photonics? Furthermore, what are the fundamental constraints in achieving highly adaptable, low-phase noise microwave signal generation?
- **Research Question 3.** What are the underlying mechanisms responsible for the introduction of up-conversion of low-frequency noise into phase noise in both active and passive components? Furthermore, what are the effective strategies to reduce additive phase noise of the circuit and overcome design bottlenecks?
- **Research Question 4.** What are the comparative trade-offs, in terms of additive phase noise, power consumption, output power, and efficiency, when considering the InP and SiGe HBT processes for designing linear power amplifiers?

To address the above-mentioned research questions, the following research thrusts are proposed.

Research Thrust 1: Broadband Ultra-Low Phase Noise Frequency Synthesizer.

This research thrust aims to demonstrate the effectiveness of DDS-based systems for generating ultra-low phase noise microwave signals while addressing the inherent bandwidth limitations associated with DDS systems. Additionally, this thrust outlines the essential steps and co-design considerations required for successful co-integration and co-packaging of electro-optical systems, leveraging advantages provided by both electrical and optical domains.

Research Thrust 2: Low Phase Noise Power Combined Power Amplifier.

The objective of this research thrust is to conduct a comparative study identifying the key contributors to the additive phase noise in amplifiers and explore effective strategies for the mitigation of additive noise. Additionally this trust conducts a detailed comparison study between SiGe and InP HBT devices for low phase noise amplification and highlights the benefits and drawbacks associated with each process by illustrating the performance of an X-band power combined power amplifier.

Research Thrust 3: Feed Forward Amplifier with Noise and Distortion Cancellation Technique.

This research thrust aims to explore effective methods for reducing amplifier additive phase noise beyond conventional design limits, emphasizing the potential of feed-forward techniques for additive phase noise cancellation. Furthermore, this thrust investigates the limitations associated with traditional feed-forward designs and proposes advanced solutions to achieve even lower amplifier phase noise, carefully considering bandwidth and chip area.

Research Thrust 4: Broadband Low Additive Phase Noise Regenerative Divider.

The objective of this research thrust is to explore the limitations associated with microwave frequency dividers, emphasizing the boundaries and shortcomings inherent to conventional regenerative divider designs. Furthermore, this thrust addresses the drawbacks of traditional approaches by proposing a novel method that effectively minimizes the amplifier's additive phase noise contribution to the total noise of regenerative frequency dividers while simultaneously addressing their excessive power consumption.

1.3.3 Research Contributions

The research presented in this dissertation has contributed to the field of electronics and photonics through co-design and co-packaging techniques, leveraging the advantages of both electrical and optical domains. This has led to the development of advanced systems and circuits that offer innovative solutions for emerging applications.

The highlights of the dissertation contribution are listed as follows:

- **Ultra-Low Phase Noise DDS-Based frequency Synthesizer:** Traditional low phase noise frequency synthesizers are typically based on PLL systems, suffer from limited tuning range, restricted tuning resolution and narrow locking bandwidth due to gain bandwidth trades offs. On the other hand, DDS-based synthesizers offer improvement in terms of frequency tunability, resolution, and phase noise performance. However, their tuning bandwidth remains limited. This dissertation proposes a DDS-based frequency synthesizer designed to overcome bandwidth limitations while preserving ultra-low additive phase noise performance. By employing multiple stages of frequency division and carefully optimizing each component's bandwidth, the synthesizer can effectively cover multiple frequency bands. An implementation of the proposed method in a SiGe BiCMOS process demonstrates a frequency tuning range spanning four octaves (exceeding 170% tunability), while achieving an additive phase noise better than -130 dBc/Hz across the entire tuning range.

- **Dual Mode Regenerative Dividers:** Regenerative frequency dividers offer significant advantages, including ultra-low phase noise and high-frequency operation, making them a preferred choice for low-phase-noise applications. However, these dividers typically come with the cost of high power consumption and large chip area. To address these challenges, this dissertation proposes a regenerative frequency divider employing a configurable division ratio. By employing a dual mode multiplier capable of operating both as a doubler and an amplifier in the feedback loop of regenerative divider, both divide by two and three is feasible. This design effectively minimizes the power consumption and optimizes the chip area

of such dividers, while simultaneously enabling rapid switching between division ratios.

- **Single Inductor Footprint Transformer Based Quadrature Signal Generation:** DDS-based synthesizer offers ultra-low phase noise performance but faces bandwidth limitation. Utilizing mixers to extend the bandwidth of DDS-based systems can be a practical solution; however, mixer nonlinearities and the digital characteristics of DDS inherently produce unwanted spurious signals. To mitigate these unwanted spurs and generate an ideal sine wave at synthesizer output, a single-side-band mixer is beneficial. SSB mixing requires accurate quadrature phase generation of the LO signal, which is critical for performance. However, achieving on-chip broadband quadrature phase generation presents challenges, including phase and amplitude mismatches as well as conversion loss. This dissertation proposes and implements a technique for achieving ultra-broadband quadrature phase generation using a passive transformer-based architecture.

- **Design Strategy For Additive Phase Noise Reduction of RF and Microwave Amplifiers:** The low-frequency noise of transistors can be effectively upconverted to phase noise due to amplifier nonlinearities, resulting in increased noise at the amplifier output. This excess phase noise adversely impacts the Bit Error Rate (BER) and Error Vector Magnitude (EVM) of communication systems. To address this issue, this dissertation investigates design strategies to minimize amplifier additive phase noise, both by reducing the low-frequency noise and mitigating its upconversion mechanism. Furthermore, the dissertation explores the impact of different amplifier operation classes on additive phase noise, examining the trade-offs between output power and noise performance.

- **Feedforward Low Phase Noise Noise Canceling Amplifier:** Feedforward techniques are widely used to reduce the additive phase noise and distortion of amplifiers by employing an auxiliary amplifier to cancel out the noise and distortion generated by the main amplifier. While these techniques effectively mitigate additive noise, they face challenges such as reduced efficiency and large area requirements due to the extensive use of phase shifters and passive structures. To address these limitations, this dissertation proposes and implements

a novel design that minimizes the form factor and associated losses of passive components. The proposed schematic achieves more than 15 dB of large-signal gain, delivers over 16 dBm of output power, and simultaneously cancels the main amplifier's phase noise by more than 7 dB.

1.3.4 Dissertation Organization

The rest of the dissertation is organized as follows:

Chapter 2: Optical Driven Low Phase Noise DDS-Based Frequency Synthesizer

This chapter demonstrates the advantages of optical-based microwave signal generation for achieving ultra-low phase noise compared to fully electrical signal generation methods. Additionally, this chapter explores the design considerations of the hybrid electro-optical synthesizer and proposes an effective method to enhance the limited tunability of optical systems while maintaining the low-noise characteristics of the generated microwave signal through a two-point Optical Frequency Division (OFD) approach.

Chapter 3: Low Additive Phase Noise Microwave Power Amplifier

This chapter investigates how amplifier nonlinearities affect the upconversion of low-frequency noise into additive-phase noise and proposes effective methods to minimize flicker noise upconversion. This chapter also examines low phase noise amplification strategies, highlighting techniques to effectively mitigate the additive noise of the amplifier by trading off the output power. Finally, it presents a modified feedforward noise canceling amplifier to address the drawbacks associated with conventional feedforward amplifiers in terms of efficiency, power consumption, and large chip area.

Chapter 4: Ultra Low Phase Noise Microwave Frequency Dividers

This chapter explores the limitations of microwave frequency dividers, examining trade-offs among power consumption, bandwidth, sensitivity, and additive phase noise, particularly in regenerative

divider architectures. It also presents effective strategies for reducing the additive phase noise of these dividers by minimizing the amplifier's contribution to overall noise performance.

Chapter 5: Ultra-Broadband Low Phase Noise DDS-Based Frequency Synthesizers

This chapter presents the design of multi-band DDS-based frequency synthesizer to overcome the limitation of synthesis bandwidth associated with DDS-based architectures. Additionally, the chapter illustrates design techniques to effectively switch the division ratio of regenerative dividers, effectively addressing the phase noise and DC power consumption trade-offs. Finally, it demonstrates the transformer-within-transformer approach for on-chip multiphase generation, significantly reducing design complexity and enabling a compact, area-efficient solution.

Chapter 6: Conclusion and Future Work

This chapter concludes the dissertation and describes other work that was not part of this dissertation. It also includes a discussion of a future direction related to this work.

1.4 Complete List of Publication

[PS1] **P. Shirmohammadi**, S. Hanifi, S. Sarpong, T.N. Blalock and S.M. Bowers "A Broadband 0.66 -10 GHz Low Phase Noise DDS-Based Frequency Synthesizer," to be submitted to *IEEE Transactions on Microwave Theory and Techniques (TMTT)*.

[PS2] S. Hanifi, **P. Shirmohammadi** and S.M. Bowers "Additive Phase-Noise Reduction in Microwave Regenerative Dividers" in *IEEE Transactions on Microwave Theory and Techniques (TMTT)*, under review.

[PS3] S. Hanifi, **P. Shirmohammadi** and S.M. Bowers "Low Phase Noise mm-wave Regenerative frequency Divider" to be submitted to *IEEE Transactions on Microwave Theory and Techniques (TMTT)*.

[PS4] S. Hanifi, **P. Shirmohammadi**, S. Sarpong and S.M. Bowers "Ultra-Low Phase Noise Mi-

crowave Frequency Divider for Low Noise Photonic-based Signal Generation" to be submitted to *IEEE Transactions on Microwave Theory and Techniques (TMTT)*.

[PS5] I. Kudelin, G. William, Q. Ji, J. Que, M. Kelleher, D. Lee, T. Nakamura, C. McLemore, **P. Shirmohammadi** et al., "Photonic chip-based low-noise microwave oscillator" *Nature, 627(8004), 534-539*.

[PS6] I. Kudelin, **P. Shirmohammadi** et al., "An optoelectronic microwave synthesizer with frequency tunability and low phase noise" *Nature Electronics, 7(12), 1170-1175*.

[PS7] **P. Shirmohammadi**, S.M. Bowers "A Wideband 2.18-13.51 GHz Ultra-Low Additive Phase Noise Power Amplifier in InP 250nm HBT" In *2024 IEEE Radio and Wireless Symposium (RWS) (pp. 16-18). IEEE*.

[PS8] **P. Shirmohammadi**, S. Hanifi, S.M. Bowers "An X-Band Phase Noise Canceling Feedforward Amplifier in InP 250 nm HBT Process" In *2024 IEEE/MTT-S International Microwave Symposium-IMS 2024 (pp. 682-685). IEEE*.

[PS9] **P. Shirmohammadi**, S.M. Bowers "Reduction of Additive Phase Noise of Electrical Amplifiers for Electronic-Photonic Low Noise Signal Generation" In *CLEO: Science and Innovations (pp. JTu2A-113). Optica Publishing Group*.

[PS10] I. Kudelin, **P. Shirmohammadi** et al., "Tunable opto-electronic synthesizer at 10 GHz with ultralow phase noise" In *2023 Conference on Lasers and Electro-Optics (CLEO) (pp. 1-2). IEEE*.

[PS11] I. Kudelin, **P. Shirmohammadi** et al., "Tunable X-band opto-electronic synthesizer for low noise microwave generation" In *CLEO: Science and Innovations (pp. SF3N-4). Optica Publishing Group*.

[PS12] I. Kudelin, G. William, Q. Ji, J. Que, M. Kelleher, D. Lee, T. Nakamura, C. McLemore, **P. Shirmohammadi** et al, "Integrated Photonic Platform for Low Noise Microwave Generation " In *CLEO: Science and Innovations (pp. SF3N-4). Optica Publishing Group*.

Chapter 2

Optically Driven Low Phase Noise DDS-Based Frequency Synthesizer

2.1 Introduction, Motivation and Prior Art

As mentioned in Chapter 1, one of the key components of any wireless communication system both on the receiver and transmitter side is its local oscillator which will be used to up-convert and down-convert the signal for processing [9]. however, the random fluctuation of phase and amplitude of these oscillators are usually limiting factors for many applications [49].

Furthermore, microwave signals with low phase and timing noise are critical for multiple fields of wide scientific, technological, and societal impact. This includes the areas of precision time-keeping, navigation, communications and radar-based sensing. Increasing demands for improved performance in these applications drive the need for microwave frequency synthesis that provides both low timing jitter and broad tunability while keeping the area and DC power consumption low. Applications such as microwave spectroscopy at the core of atomic clocks [50], as well as radio astronomy [51] require precise and low-noise signals, but with minimal frequency tuning. On the other hand, communication systems often require fast frequency hopping, where the phase noise

on the microwave carrier affects the error vector magnitude of the signal and bit error rate [3, 9]. Radar is another prominent application that relies on both frequency agility and low noise [52, 53]. Here, low phase noise improves the detection probability as well as the imaging accuracy and quality [54]. Beyond these examples, low-noise and frequency-agile synthesis is indispensable in other technical and scientific fields including metrology, sensors, and navigation systems. The extent of the application space elevates the importance of robust and low noise microwave synthesis that covers a broad frequency range.

Conventional electronic synthesizers introduce tunability with multiple electronic up-converters and local oscillators. These tuning elements provide an avenue to introduce noise that is multiplicative as the frequency increases. Most of the state-of-the-art PLL ICs and Signal Generator (Sig- Gen) typically offer wide tuning ranges but face trade-offs involving phase noise, power consumption, and physical area. The relationship among these parameters is depicted in Fig. 2.1, highlighting the trade-offs between power consumption, physical size, and phase noise performance observed in current commercial PLL ICs and signal generators.

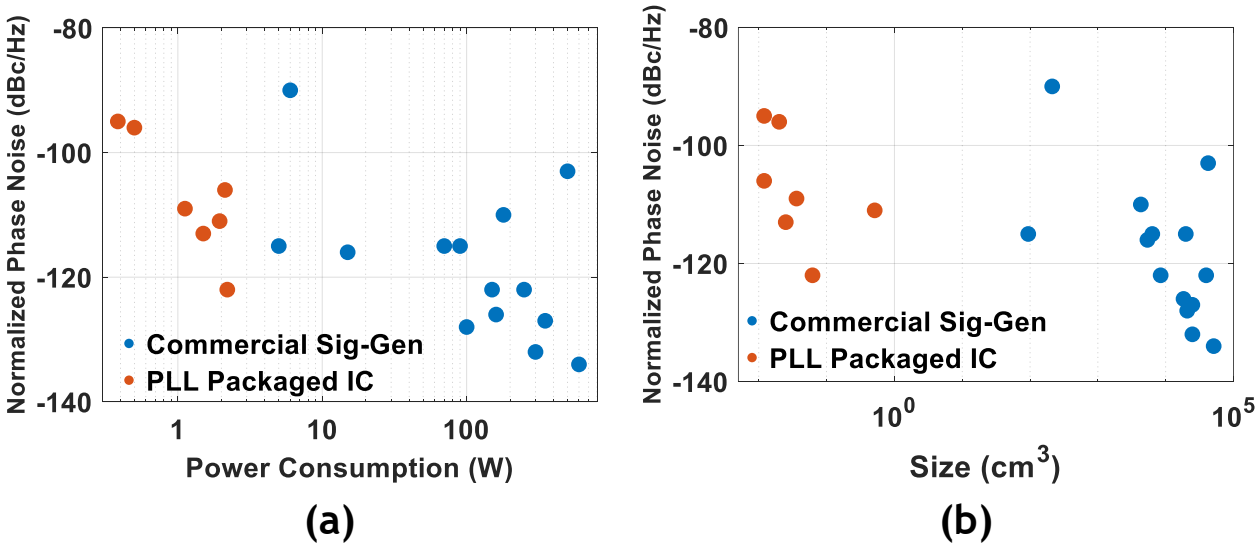


Figure 2.1: Phase noise versus (a) Power consumption (b) Size of commercial signal generators and PLLs.

On the other hand, photonic-based microwave generation approaches such as Optical Frequency Division (OFD) have drawn significant attention due to their unique ability to overcome some of the

conventional oscillator's limitations and outperform their traditional counterparts, state-of-the-art electronic oscillators by several orders of magnitude. However, this superior performance comes with restricted tunability that is often in the range of a few percent and significantly increased physical size [55–57].

One commercially available state-of-the-art solution for ultra-low phase noise microwave signal generation via optical methods is offered by Menlo Systems with their UMS compact and mini. These synthesizers achieve phase noise performance more than 20 dB better than traditional approaches, but at the expense of very limited tunability and increased size.

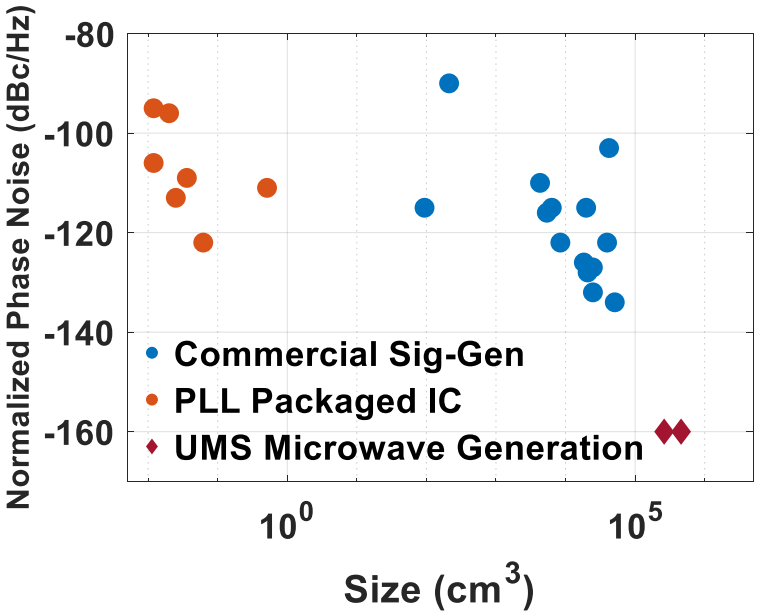


Figure 2.2: Comparison between phase noise of UMS with state of the art siggen and PLL ICs.

The phase noise performance of the UMS is compared with commercial signal generators and PLLs in Fig. 2.2 illustrating the existing trade-off between achieving ultra-low phase noise and providing broad, rapid frequency tunability in frequency synthesizer design.

In order to address the inherent trade-offs and challenge this paradigm, this dissertation proposes leveraging the advantages of co-integrating and co-packaging electronic and photonic systems. In contrast to previous works [58, 59] and UMS system, this dissertation proposed a plan of co-integration and co-packaging of electronic and photonic systems that implement significant sim-

plifications to ultra-low phase noise microwave signal generation. This co-integration strategy is designed to align with recent advancements in chip-level integration technologies, enabling compact, high-performance, and widely tunable frequency synthesizers [57, 60, 61].

This chapter addresses the limitations of traditional microwave synthesizers by introducing a hybrid electro-optical approach, combining simplified OFD with DDS to generate tunable, ultra-low phase noise microwave signals across the entire X-band. Additionally, the chapter investigates key design considerations for integrating photonic and electronic components, discusses effective co-packaging strategies, and outlines a pathway toward fully integrated, on-chip, low-phase-noise microwave signal generation.

The implemented hybrid electrical synthesizer was driven by the photonic system with a fixed 10 GHz input with phase noise of -156 dBc/Hz at 10 kHz offset and fractional frequency instability of 1×10^{-13}. This low-noise signal then serves as the reference clock for a direct digital synthesizer (DDS), the output of which is mixed with the clock itself to provide tunable low-noise microwaves across the entire X-band (8-12 GHz). This yields microwaves with phase noise at 10 kHz offset of -150 dBc/Hz, -146 dBc/Hz, and -140 dBc/Hz in the tuning range of $\pm$500 MHz, $\pm$1 GHz, and $\pm$2 GHz from the 10 GHz, respectively. At the same time, the DDS allows tuning with μHz resolution and speeds of tens of ns. Compared to previous works [58, 59], we increase the continuous tuning range by up to a factor of 4, with an improvement in the phase noise of 10 dB.

The synthesizer architecture is fully compatible with integrated photonic implementations that will enable a versatile microwave source in a chip-scale package. Together, these advances illustrate an impactful and practical synthesis technique that shares the combined benefits of low-timing noise provided by photonics and the frequency agility of established digital synthesis.

2.2 Tunable X-band Opto-Electronic Synthesizer with Ultralow Phase Noise

The key contributor to the architecture of hybrid electro-optical synthesizer is a low-noise photonic oscillator at 10 GHz that is generated using 2-point optical frequency division (2P-OFD) [60, 61]. Compared to traditional OFD approaches [55,56,58], 2P-OFD results in a lower division factor, but enables a significant reduction in the size and power requirements. Additionally, carefully designed 2P-OFD allows further noise reduction due to common mode rejection, which can bring it on par with conventional OFD systems [62]. In our system, the frequency division is implemented with an injection-locked laser that generates a microcomb by using an Electro-Optical modulator (EO-comb). 2P-OFD is then implemented by heterodyning the two SIL lasers with the closest comb teeth to produce two beat notes.

The following subsections explain the two primary aspects of the synthesizer design: the generation of ultra-low phase noise microwave signals and strategies for achieving broad frequency tunability.

2.2.1 Low-Noise Microwave Generation Through OFD

In our realization of 2P-OFD, the low phase noise of continuous wave (CW) lasers is transferred to an optical frequency comb and its microwave-rate mode spacing. This is achieved by first narrowing the linewidth of the CW lasers through active stabilization of their frequencies to a high quality (Q) factor Fabry-Pérot (FP) cavity [63, 64]. The FP cavity plays a crucial role in low-noise microwave generation with 2P-OFD by providing the phase and frequency reference of the generated microwave signal. The lowest noise can be achieved with a long FP cavity length [63, 64].

However, to reduce the system size, we take advantage of recent advances in miniature FP cavities [65] and employ an FP with 6.3 mm cavity length and 23.6 GHz free-spectral range (FSR).

Ultralow loss cavity mirrors yield a cavity with Q∼5 billion and the fractional frequency stability as low as 3×10^{-14} with 1 s of averaging [65]. The phase noise of the lasers that are stabilized to the cavity inherits the thermal-limited cavity length stability for offset frequencies below 10 kHz.

As shown in the experimental setup in Fig. 2.3, two lasers with frequencies ν_{1555} and ν_{1545} and a frequency separation of 1.3 THz are stabilized to different modes of the FP cavity. This gap, which is $55\times$ the cavity FSR, is then divided down with an electro-optic (EO) frequency comb. The EO comb is generated by phase modulating a 1550 nm CW laser (ν_{1550}) with the amplified output of a voltage-controlled oscillator (VCO) at $f_m = 10$ GHz [66].

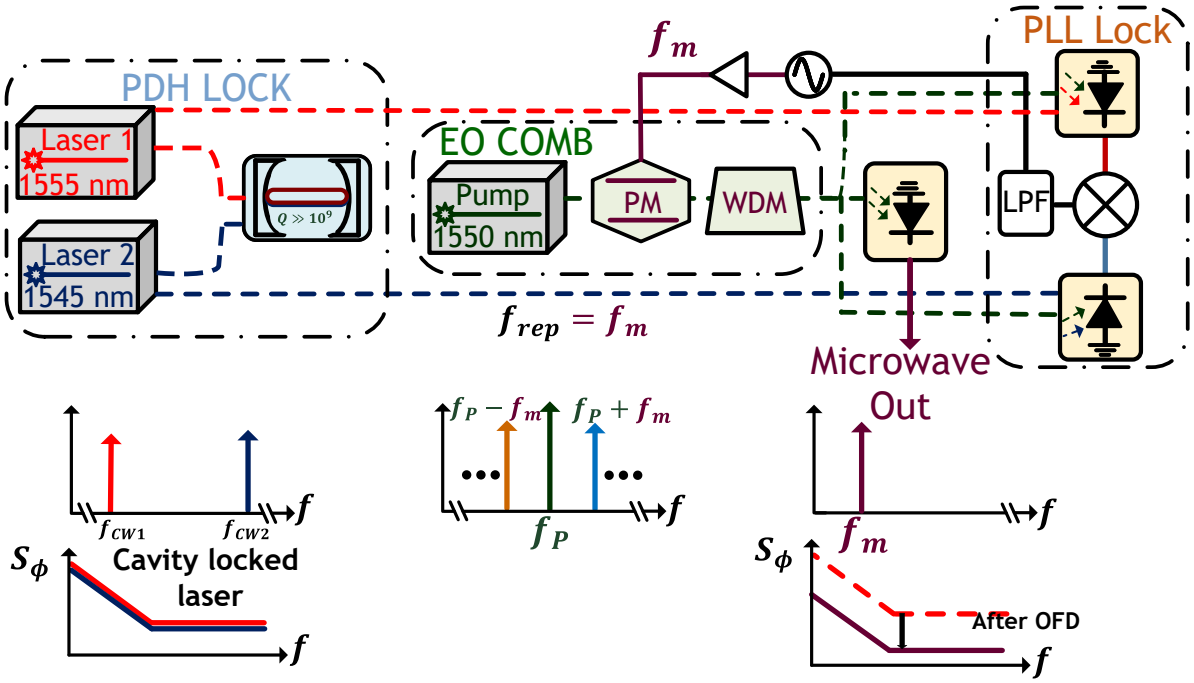


Figure 2.3: Two CW at 1545 nm and 1555 nm are locked to a millimeter-scale (FP) cavity with the Pound-Drever-Hall (PDH) technique. The EO comb is split in a WDM to provide the beat notes (f_{b1} and f_{b2}) with the reference lasers. Part of the EO comb is detected in a modified uni-traveling carrier (MUTC) detector to provide a low-noise microwave at f_{rep}. The beat frequencies between the CW lasers and the EO comb are mixed together to provide the error signal that is conditioned with a loop filter (LF) and used to stabilize the VCO and the EO comb mode spacing.

The comb frequency spacing is given by $f_{rep} = f_m$ and the optical spectrum of the comb along with the two CW lasers is shown in Fig. 2.4. 2P-OFD is implemented by heterodyning the cavity-

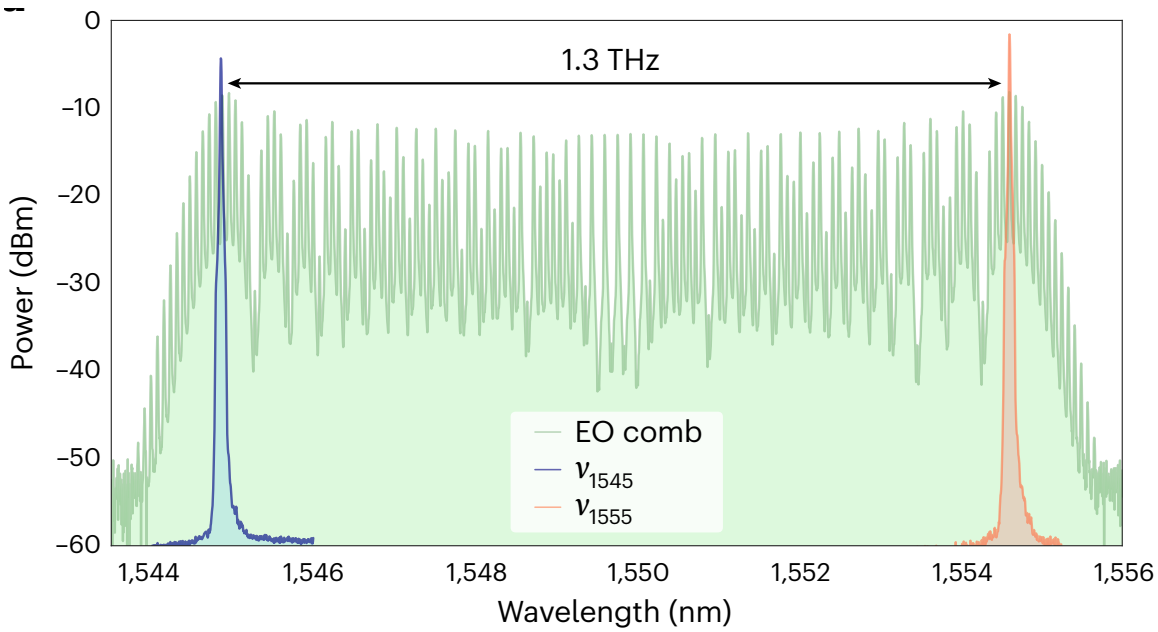


Figure 2.4: Optical spectra of the EO comb and reference CW lasers.

stabilized optical references ν_{1555} and ν_{1545} with the closest comb lines $\nu_{1550} - nf_{rep}$ and $\nu_{1550} + mf_{rep}$, where n and m are positive integers. This yields two beat-notes $f_{b1} = \nu_{1555} - \nu_{1550} + nf_{rep}$ and $f_{b2} = \nu_{1545} - \nu_{1550} - mf_{rep}$, which are further mixed to provide an intermediate frequency (IF) $f_{IF} = f_{b2} - f_{b1} = \nu_{1545} - \nu_{1555} - (n+m)f_{rep}$. The correct choice of the sum or difference between f_{b1} and f_{b2} depends on the frequency positions of the CW lasers relative to the comb lines. Conveniently, f_{IF} does not depend on the center frequency of the EO comb, allowing for the use of a free-running laser for ν_{1550}. To complete the comb stabilization, the intermediate frequency is compared to a reference oscillator f_{ref} to generate an error signal that is conditioned and fed to the 10 GHz VCO.

Once the servo loop is closed, the frequency of f_{rep} is given by:

$$f_{\text{rep}} = \frac{(\nu_{1545} - \nu_{1555}) + f_{\text{IF}}}{(n+m)}. \tag{2.1}$$

The denominator $(n + m)$ is the number of comb modes between the CW lasers and is responsible for the frequency division and corresponding noise reduction due to OFD. In terms of the phase noise power spectral density, this reduction is equal to $20\log[(\nu_{1545} - \nu_{1555})/f_{rep}] =$

$20\log[1.3\ \mathrm{THz}/10\ \mathrm{GHz}] = 42$ dB. This division reduces the noise contributions of the relative stability of the reference lasers, $(\nu_{1545} - \nu_{1555})$, and f_{IF}. Since both lasers are locked to the same cavity, their noise is highly correlated which leads to improved relative phase noise due to the common mode rejection [62, 67].This common mode rejection of the cavity noise reduces the phase noise below the thermal noise of the cavity to the limit imposed by residual noise of the individual laser locking circuits. The output of the servo-controlled VCO provides direct access to the 10 GHz signal and the output is detected through a high-power and high-linearity modified uni-traveling carrier (MUTC) photodiode [68]. Fiber dispersion and optical filtering of the spectrum in the WDM transforms the phase modulation that creates the EO comb into an amplitude modulated signal that can be photodetected with sufficient signal-to-noise ratio.

As shown in Fig. 2.5, in this configuration we achieve phase noise of -156 dBc/Hz at 10 kHz offset frequency. At higher offset frequencies, the microwave performance is limited by the phase locking of f_{IF}. Reducing the noise in this frequency range would require broader bandwidth servo control of f_{IF}. At offset frequencies below 100 kHz, the phase noise is limited by the relative stability of the CW lasers, as shown by the red curve of Fig. 2.5. Further improvement of the relative phase noise of the reference CW lasers, and the generated 10 GHz as well, can be made by custom designed servo controls to reduce the residual noise of the PDH locking and allow higher common mode rejection.

To demonstrate the low additive phase noise performance of a 10 GHz signal generated using the EO comb system and to compare it against state-of-the-art photonic and electronic systems, the phase noise versus size is plotted in Fig. 2.6. This plot shows that the EO comb achieves superior phase noise performance relative to Siggen and comparable performance when compared with UMS systems while significantly reducing size and area. However, tunability remains a challenge that must be addressed.

As indicated in Eq.2.1, f_{rep} can be tuned via f_{IF}, which assumes a maximum value of f_{rep} through coarse stepwise tuning of the VCO. Nonetheless, when divided by $(n+m) \approx 130$ the tunability is reduced to a small fraction of f_{rep}. This limitation is a common drawback in all OFD systems, but

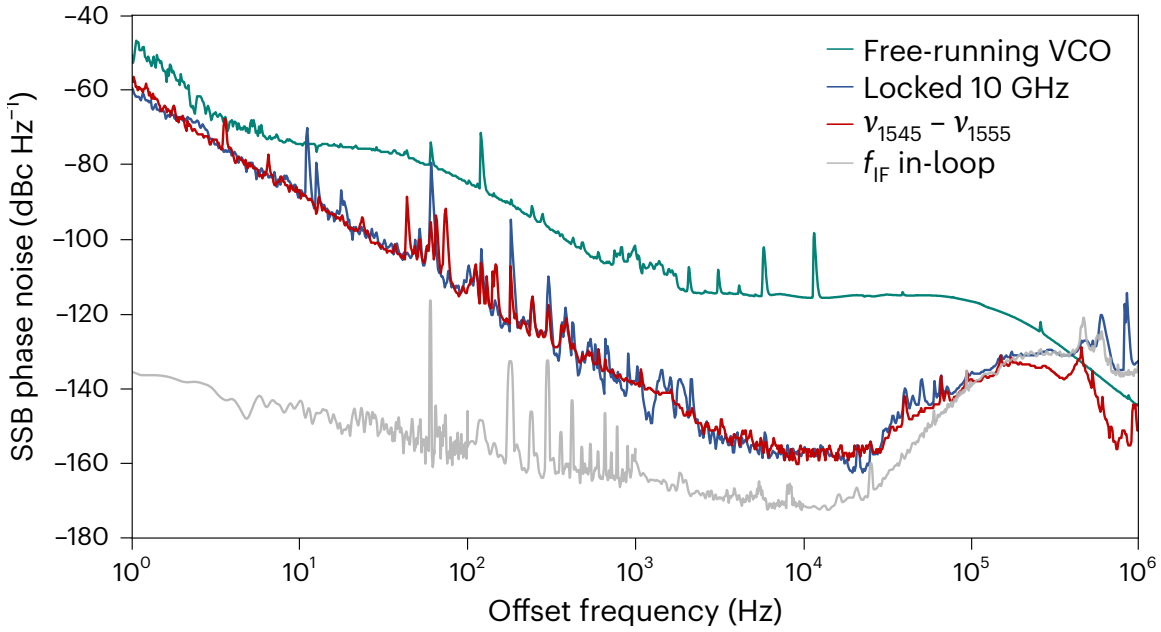


Figure 2.5: The phase noise of the free-running VCO, photodetected stabilized 10 GHz, in-loop phase noise of the intermediate frequency locking, and the relative phase noise of the reference CW lasers ($\nu_{1545} - \nu_{1555}$) spaced by 1.3 THz.

in what follows we show how the tuning range can be significantly increased.

2.2.2 Broadband Tunability with Low Phase Noise

Broad bandwidth tunability of the low-noise 10 GHz microwave is achieved by mixing this signal with the output of a direct digital synthesizer. With reference to Fig. 2.7, the low noise microwave at 10 GHz is frequency divided by 2 and serves as a reference (clock) for the DDS. The DDS output is then added to (or subtracted from) the original 10 GHz reference using an IQ mixer. Since the DDS initially creates the output waveform only at discrete time intervals, its generated output frequency can not exceed the Nyquist–Shannon sampling theorem limit. In the case of the DDS employed here, the maximum output frequency is 2 GHz, which is ∼40% of the reference input $f_{rep}/2$.

The two main contributions to the phase noise of the DDS output are: (1) the input clock noise that

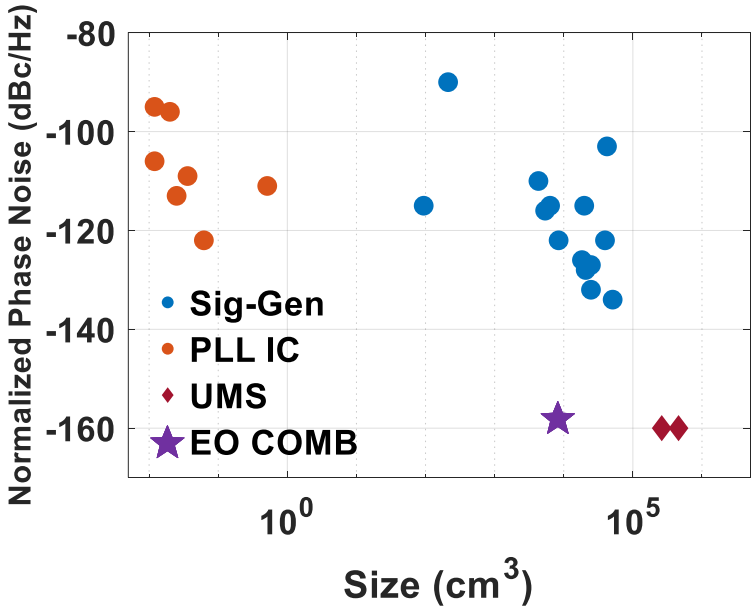


Figure 2.6: Comparison between phase noise of best electronic and photonic systems and EO comb results.

is reduced by the ratio $(f_{clock}/f_{out})^2$, and (2) the intrinsic noise originating within the DDS itself, which arises from quantization noise, truncation noise and nonlinearity in the DAC [69].

In Fig. 2.8, we show sample phase noise when the DDS is clocked by the low-noise 5 GHz and its output is set at frequencies between 100 MHz and 2 GHz. For the 100 MHz output, the output noise is limited by the DDS intrinsic noise, reaching -152 dBc/Hz at 10 kHz offset frequency. As the DDS frequency increases, the noise of the clock signal starts to dominate at offset frequencies

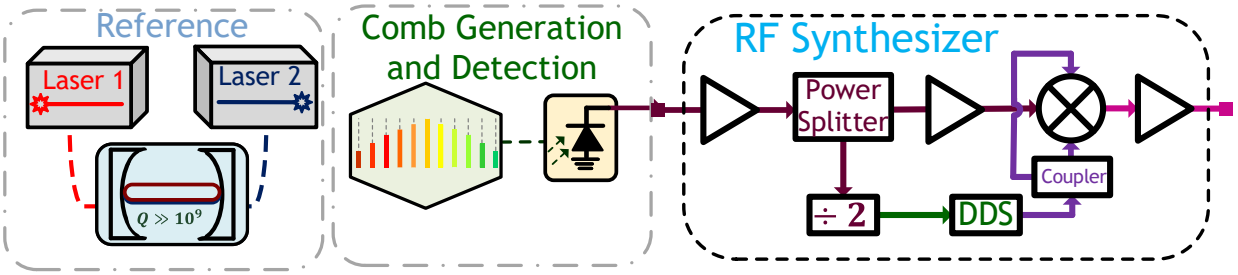


Figure 2.7: The stabilized 10 GHz is frequency-divided by two and serves as the clock signal for a direct digital synthesizer (DDS). The DDS output is split in the hybrid coupler to provide two signals with 90° relative phase shift. These signals are mixed with the original 10 GHz in an IQ mixer for single-sideband generation. By tuning the DDS frequency, the synthesizer output covers the entire X-band (8 - 12 GHz).

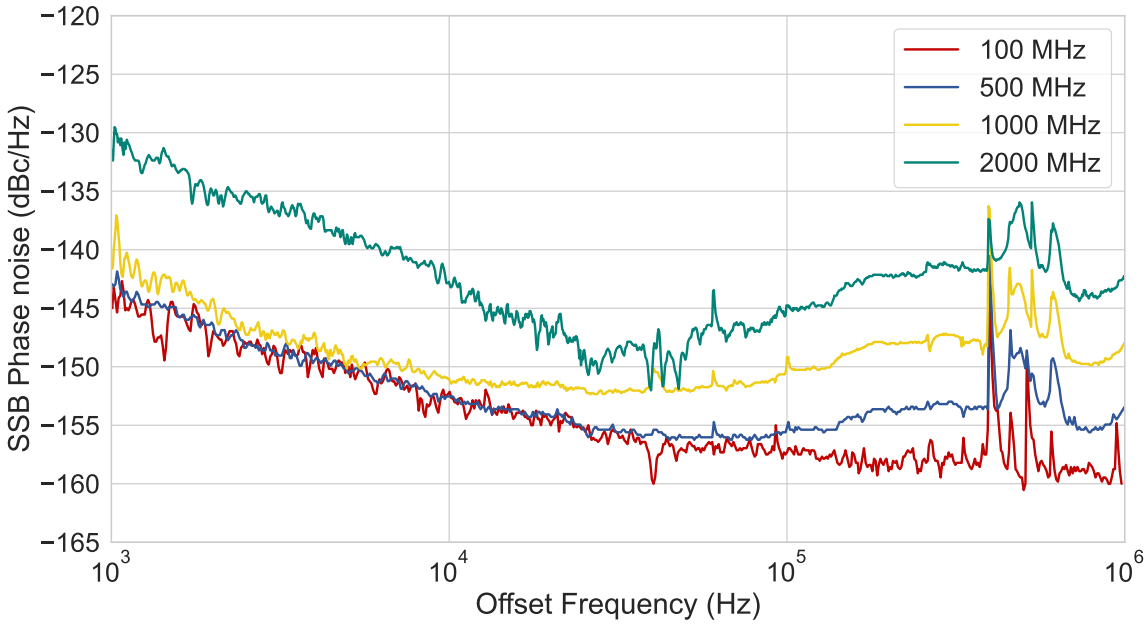


Figure 2.8: Single side-band (SSB) phase noise of DDS output in the range from 100 MHz to 2 GHz, while the stabilized 10 GHz serves as an external clock.

above 100 kHz.

The DDS output is summed or differenced with original 10 GHz microwave in an IQ mixer. The low noise 10 GHz at f_{rep} is amplified to saturate the mixer, while the DDS output is split in a hybrid coupler to provide a 90° phase shift between the I and Q ports of the mixer. The phase shift of 90° is necessary to achieve single sideband operation with high image rejection. Output in the range of 8-10 GHz or 10-12 GHz is determined by the relative sign of the phase shift between the I and Q ports.

Power spectra of synthesized frequencies in the 10-12 GHz band are shown in Fig. 2.9. The rejection of the synthesized frequencies relative to the original 10 GHz carrier is more than 16 dB across all tuning frequencies. This rejection can be increased with higher power driving the I and Q inputs of the mixer. At the same time, the image rejection exceeds 21 dB across all generated frequencies. This rejection can be improved with more precise amplitude balance and phase control between the I and Q ports. Alternatively, one could use two DDSs clocked by the same microwave input, with precise digital tuning of the amplitude and respective phases adjusted to 90°.

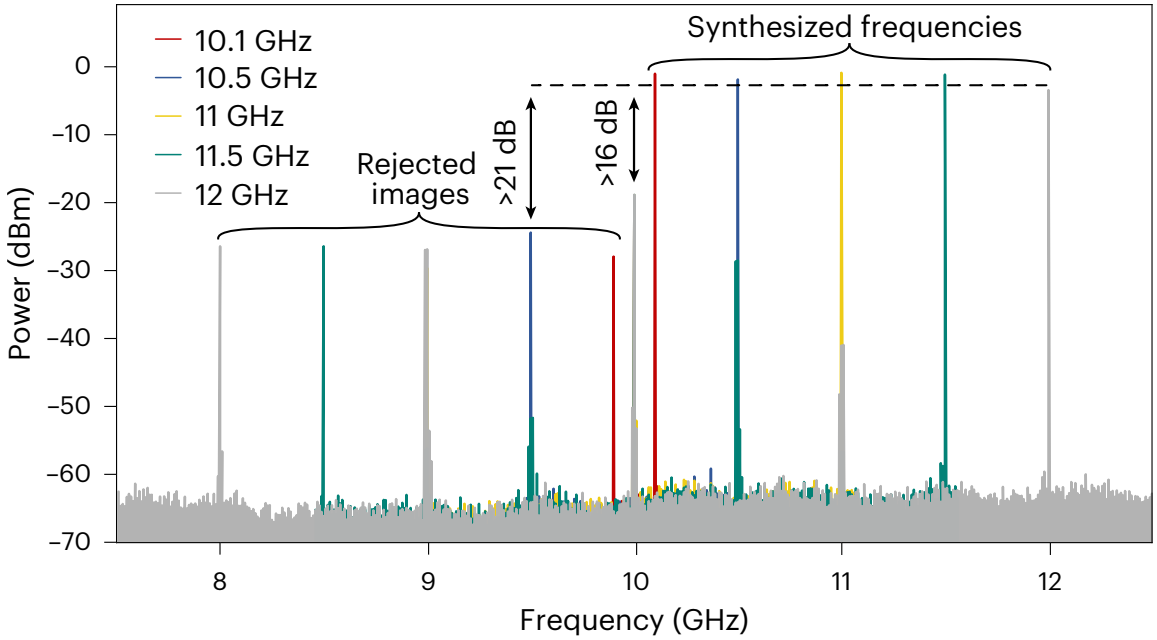


Figure 2.9: RF spectra of the synthesized frequencies. The spectra with lower syntehesized frequencies is exactly symmetric to the presented one.

Figure 2.10 shows our measurements of the phase noise of the synthesized frequencies at discrete values across the entire X-band. At offsets above 80 kHz, the phase noise is limited by that of the 10 GHz signal itself, while at lower offset frequencies, the noise from the DDS dominates, which correlates well with the phase noise measurements of the DDS itself. The noise on the synthesized frequencies in the range of 9.5 to 10.5 GHz falls below -150 dBc/Hz at 10 kHz offset, while the phase noise increases to near -140 dBc/Hz at 8 and 12 GHz. Note, that down-scaled clock noise does not affect the synthesizer output noise since the noise of the original 10 GHz is higher then its down-scaled replica. However, the flicker noise in the analog circuitry, along with quantization noise and DAC nonlinearity of the DDS, limit the reduction of clock noise.

This increase versus carrier frequency (f_c) is summarized in the inset in Fig. 2.10. The phase noise contribution of the DDS to the entire synthesizer can be categorized into two regions. In the range of 9.5 to 10.5 GHz, the phase noise does not depend on carrier frequency. However, at carrier frequencies offset by more than 500 MHz from 10 GHz, the phase noise increases approximately as $20\log(N)$, where N is the frequency multiplication factor. Considering the noise sources de-

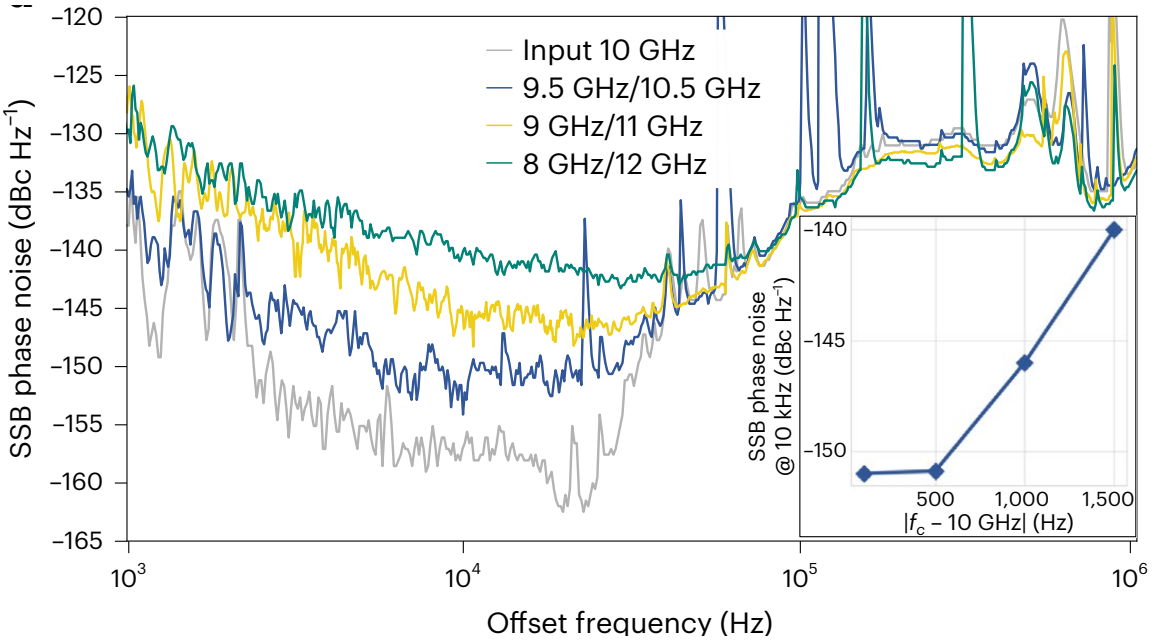


Figure 2.10: Single side-band (SSB) phase noise of the synthesized frequencies from 8 GHz to 12 GHz. Inset: Phase noise at 10 kHz offset against the synthesized frequency.

scribed earlier, we assume that the dominant noise source at carrier frequencies closer to 10 GHz is quantization noise in the digital-to-analog conversion. This noise results from the quantized number of DAC bits and the symbol rate of the DAC, which exhibits the white noise power spectral density independently of the generated output frequency. Meanwhile, the noise originating within the final output stage of DAC is likely the limitation at higher synthesized frequencies. This noise arises from both the DAC switching mechanism and the flicker noise of the output stages. The flicker noise from the analog output stages exhibits a 1/f characteristic and scales with the generated output frequency. Switching noise occurs when the digital circuitry within the DAC changes state, leading to additional noise and spurs, particularly at high clock and output frequencies. We note that since the DDS primarily limits the noise, there is no need for a reference microwave source with noise lower than the internal noise of DDS, making 2P-OFD an ideal technique for such a synthesis approach.

An advantage of our approach is its versatility that overcomes the obstacle of the limited tunability of photonic-based microwave generators. We expect similar phase noise performance can be

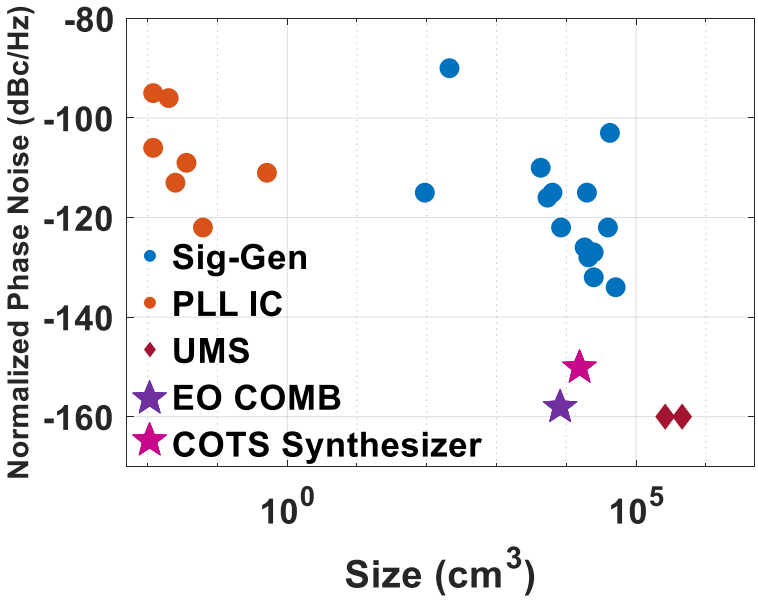


Figure 2.11: Comparison between phase noise of best electronic and photonic systems and the hybrid electro-optical synthesizer.

readily achieved in other microwave bands. For example, by using the 20 GHz harmonic from the photodetected EO comb, it is possible to partially cover the K-band while maintaining low noise, similar to that of Figure 2.10. The tuning resolution of the DDS is in the μHz range, and that can be controlled at the speeds of tens of ns [59]. Compared to previous work on tunable microwave generation with frequency comb [58, 59], we demonstrate a 4-fold improvement in tunability with an improvement of up to 10 dB in phase noise.

The phase noise performance of the implemented hybrid electro-optical synthesizer, compared to other state-of-the-art systems, is illustrated in Fig. 2.11. The plot shows that while the phase noise performance is slightly impacted by a few dB and the physical size increases due to the use of COTS components, the synthesizer achieves over 40% tunability for the ultra-low-phase-noise 10 GHz signal, with microhertz-level resolution and sub-nanosecond tuning speed. Moreover, our hybrid synthesizer outperforms state-of-the-art signal generators while maintaining a significantly smaller footprint and surpasses commercially available PLL chips by several orders of magnitude in terms of phase noise performance.

2.3 Chip-Scaled Solution for Broadband Tunability

The implemented hybrid synthesizer represents a significant advancement in low-phase-noise microwave signal generation, addressing key trade-offs between noise performance, power consumption, tunability, and bandwidth. It has made a notable impact on DDS-based synthesizers and presents a promising solution for the next generation of hybrid synthesizers. However, several challenges remain in pushing the boundaries of microwave signal generation, including expanding tunability and bandwidth, further reducing spurs generated in the final mixing stage, and, most importantly, transitioning to a more compact, custom chip-based solution. Achieving this goal requires advancements in both optical and electronic domains, which are explored in detail in the following subchapter.

2.3.1 Photonic Chip-Based Low Noise Microwave Oscillator

As discussed earlier in this chapter, achieving low-phase-noise tunability relies on utilizing ultra-low-phase-noise sources, such as Optical Frequency Division (OFD) and injection-locked lasers. All OFD systems begin with a highly stable optical frequency reference, typically a fiber-based or solid-state laser that is frequency-stabilized to a large evacuated Fabry-Pérot (F-P) cavity [32, 70]. However, recent advancements have focused on transitioning from bulky, laboratory-scale components to compact, on-chip solutions [57, 60, 61, 71], which are summarized below.

Miniature Fabry-Pérot cavity: The phase and frequency stability of the generated microwave signal is ultimately derived from that of the ultrastable optical reference. The lowest noise optical references are lasers locked to vacuum-gap F-P cavities, where fractional frequency stability as low as $4\times\ 10^{-17}$ has been demonstrated with 212 mm long, cryogenic cavity systems [32]. Extensive research has been conducted to minimize cavity size and transition toward integrable cavity designs. One approach involves a compact, rigidly held cylindrical Fabry-Pérot compact, that supports fractional frequency stability at the 10^{-14} level [65]. Ultra-low expansion glass with 1 m radius of curvature and an ultra-low expansion glass spacer compose the 6.3 mm long cavity

with finesse of ∼900,000 (Q∼5 billion) and overall volume of less than 9 cm^3.

Self-injection locked lasers: To achieve high stability performance in a hybrid systems, it is crucial to use narrow-linewidth and frequency-stable lasers. This is because electrical noise from the individual laser locking circuits does not experience Common Mode Rejection (CMR), and this noise is reduced only by the 2P-OFD. To address this issue and reach the thermal noise floor of the F-P cavity, several research employs SIL lasers that are both integrable and have noise performance equivalent to much larger laboratory fiber lasers [72–74].

Microcomb: Robust and low-noise optical frequency comb generation with 10-20 GHz repetition rate and broad optical coverage is challenging. Considerable research has focused on utilizing microcombs instead of electro-optic (EO) combs, highlighting a trend toward integrated resonator solutions. Such approaches include employing Si_3N_4 microresonator fabricated at a CMOS foundry to generate mode-locked microcombs [72]. To produce dark soliton microcombs with higher bandwidth, a dual coupled-ring resonator with FSR of 20 GHz [75] can be used, where the zero GVD wavelength is tuned using integrated heaters [76].

Achieving fully integrated, ultra-low-phase-noise signal generation on-chip is becoming increasingly feasible, as discussed in [60]. The block diagram and on-chip components of the proposed integrated solution are illustrated in Fig. 2.12, demonstrating the potential for a compact and highly stable photonic-electronic system.

2.3.2 Electronic Chip Design for Low Phase Noise Tunability

The second key aspect of low-phase-noise microwave signal generation is achieving both low noise and broadband tunability. While the proposed COTS synthesizer advances electronic synthesizer technology and pushes the limits of DDS-based architectures, it still faces challenges such as limited bandwidth, high spur levels, and large physical size. As a reuslt, developing a custom IC version of the synthesizer is preferable, as it would significantly expand the system's bandwidth while reducing its size by several orders of magnitude.

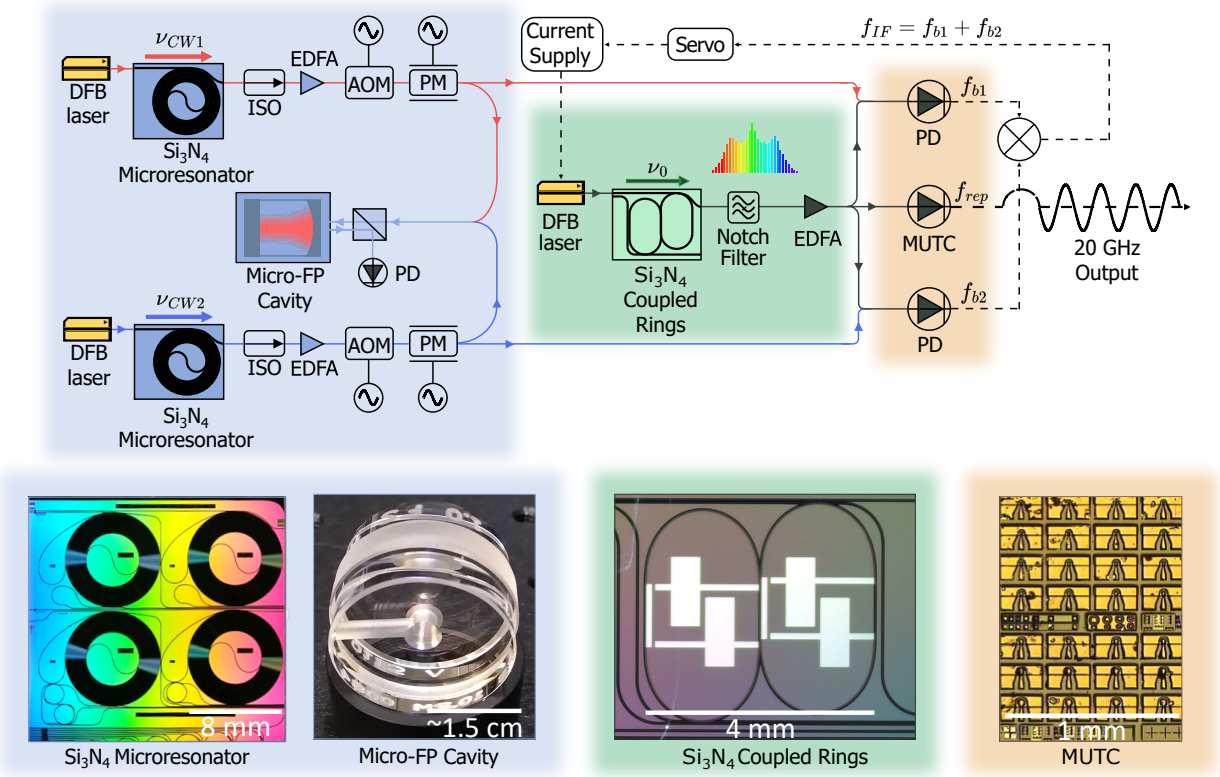


Figure 2.12: Two distributed feedback (DFB) lasers self-injection locked to Si_3N_4 microresonator chips, amplified and locked to the same miniature Fabry-Pérot cavity. A broad frequency comb with a 20 GHz repetition rate is parametrically generated in a coupled-rings resonator. **Bottom row:** Photographs of the key components for low noise microwave generation.

Furthermore, moving to chip-scale solutions such as microcombs and SIL lasers, instead of bulky EO combs and fiber lasers, offers significant advantages. Microcombs with higher repetition rates are particularly preferable, as they enable smaller resonators, leading to higher integration density [77] and lower phase noise [78]. Meanwhile, the generated microwave frequency often exceeds the acceptable clock frequency limits of DDS synthesizer, as a result, a frequency divider is required to divide down the high-frequency generated signal to a level acceptable for the input of the synthesizer.

To address the aforementioned challenges, a custom broadband frequency synthesizer capable of operating in the higher end of the Ku-band and the lower end of the K-band is highly desirable.

The high-performance HBT transistor of the SiGe process, along with the 90 nm CMOS transistor, provides an advantage, making the 9HP process an ideal choice for high-frequency, low-noise mixed-signal architecture. Consequently, an integrated synthesizer has been designed and fabricated using the SiGe BiCMOS 9HP process. The block diagram of this IC synthesizer is illustrated in Fig. 2.13.

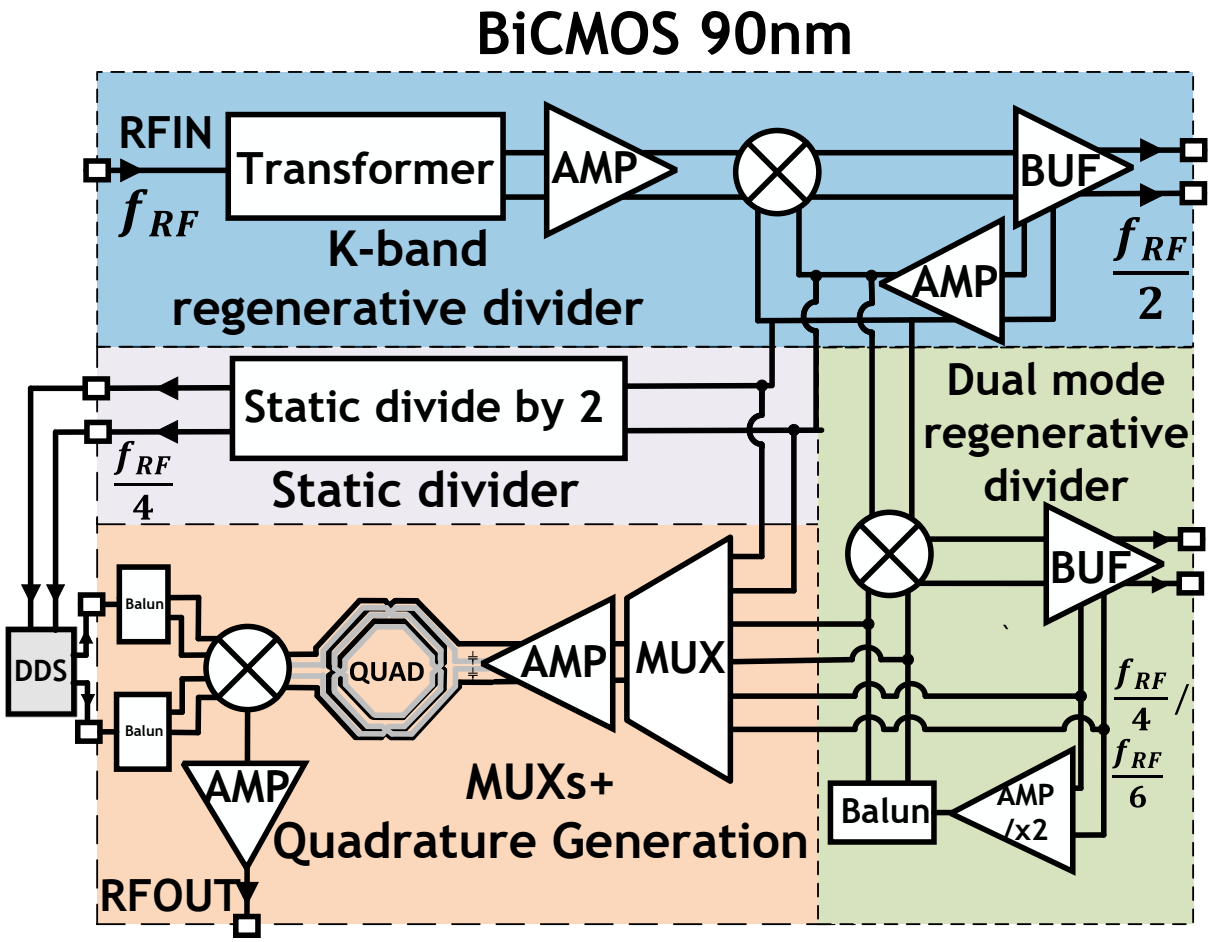


Figure 2.13: Detailed block diagram of the implemented IC synthesizer.

The system includes a K band divide-by-two frequency divider to generate the first LO tone for the final stage of the mixing. The output of divider drives two different frequency dividers: a static and a dual mode regenerative divider. The dual mode divider can be configured as either divide-by-two or divide-by-three. Since the input signal has already undergone a divide-by-two operation, the final output of the divider can be either a divide-by-four or divide-by-six.

In order to select the desired frequency band and minimize leakage from unwanted LO tones to the output, multiplexers (MUXs) are employed to isolate and select the wanted tone. To further suppress the unwanted harmonic, quadrature phase generation followed by a single sideband mixer is required. Thus, an on-chip passive transformer-based quadrature generator is implemented to provide all four phases required for single-sideband mixing. The output of a static divider is used to provide the clock signal for a Commercial Off-The-Shelf (COTS) Analog Device DDS. The output of DDS goes through a broadband COTS hybrid coupler followed by on-chip active baluns to generate all four phases required for IF port of the mixer. The final single-ended output of the mixer is amplified using a broadband single-ended amplifier to boost the output power.

Chapter 5 provides a detailed description of synthesizer performance and design considerations for each main section of the design.

2.4 Conclusion

In this chapter, a tunable low noise microwave generation using 2P-OFD in combination with DDS was demonstrated. This work provides the first 10 GHz microwave generation via 2P-OFD with low noise on both short and longer timescales. This is demonstrated via frequency instability of 1×10^{-13} at 0.1 s and the phase noise of -156 dBc/Hz at 10 kHz offset. This milestone is significant because it is realized with components amenable to low-SWaP on-chip microwave generation, where 2P-OFD is the ideal approach in terms of simplicity and performance. In the past years, significant progress has been made in the hybrid and heterogeneous chip-scale integration of all photonic components of the system in this design. As a result, it now appears realistic to realize a complete microwave synthesizer on a chip [57, 60, 61, 71, 79].

Another significant milestone of the work is the first demonstration of broad frequency tunability with 2P-OFD, while maintaining low phase noise. The key to this is using the stabilized 10 GHz signal as the clock of the DDS. For the synthesized frequencies in the range of 8 GHz to 12 GHz, the system supports the phase noise of -140 dBc/Hz at 10 kHz offset. And in the range of 9.5 GHz

to 10.5 GHz, the phase noise is below -150 dBc/Hz. In comparison to other similar works [58, 59], this work showed a substantial improvement in the tuning range with up to 10 dB improvement in the phase noise. While this work demonstrated the advantages of combining 2P-OFD with DDS-based synthesis, the performance still can be improved by optimizing the system with lower noise DDS and lasers, larger OFD factors, and improved servo systems. Additionally, with lower noise RF amplifiers it is possible to access low noise microwave with power above +30 dBm. These insights provide a roadmap for low-SWaP photonic microwave generation with low-noise and broad tunability, as will be important for multiple applications in navigation, communications and sensing.

2.5 Contribution

This work was done in collaboration with Igor Kudelin, Samin Hanifi and William Groman. I would like to thank them for following contributions:

- Igor Kudling and William Groman for building the photonic system setup and performing the hybrid measurements.
- Samin Hanifi for helpful technical discussion.

2.5.1 Publications

- I. Kudelin, **P. Shirmohammadi** et al., ”An optoelectronic microwave synthesizer with frequency tunability and low phase noise” *Nature Electronics, 7(12), 1170-1175*.
- I. Kudelin, **P. Shirmohammadi** et al., ”Tunable opto-electronic synthesizer at 10 GHz with ultralow phase noise” In *2023 Conference on Lasers and Electro-Optics (CLEO) (pp. 1-2). IEEE*.

- I. Kudelin, **P. Shirmohammadi** et al., ”Tunable X-band opto-electronic synthesizer for low noise microwave generation” In *CLEO: Science and Innovations (pp. SF3N-4). Optica Publishing Group*.

Chapter 3

Low Additive Phase noise Microwave Power Amplifier

3.1 Introduction, Prior Art

The rapid increase of emerging applications such as Virtual Reality (VR) [11], coupled with the increasing need for higher precision of advanced positioning [4], navigation, and radar systems [80] has accelerated research on the stable and precise clock and oscillators [81]. As stated earlier in Chapter 1, One of the key factors in determining the overall performance of such systems is phase noise, potentially serving as a limiting factor for the above-mentioned applications [8,82,83]. Thus generating ultra-stable low-phase noise microwave using optical methods is getting more and more attention and optical frequency division (OFD) [84] has demonstrated excellent capabilities to overcome some of the traditional limitations associated with state-of-the-art electrical oscillators in terms of phase noise.

The operating principle of OFD is illustrated in Fig. 3.1. It involves two lasers as optical references, self-injection locked to a high-quality factor (Q) cavity. A third ultra-stable laser enables the generation of a soliton microcomb to achieve OFD and lock the output of each laser to different

lines of the microcomb for phase noise reduction. The optical output of the microcomb undergoes through a photodetector (PD) to generate a low-noise electrical signal followed by an amplifier for amplification [85, 86]. Some of the state-of-the-art optical oscillators demonstrate outstanding phase noise performances, such as -163 and -153 dBc/Hz at 10 kHz offset from 8 and 40 GHz carrier frequencies, respectively [87, 88]. A significant concern associated with optical oscillators originates from additive phase noise and linearity of the electrical amplifier, and the phase noise introduced by the electrical amplifier has the potential to limit the purity of microwave signal originating through optical methods and disturb the low noise profile of generated signals as illustrated in Fig. 3.1.

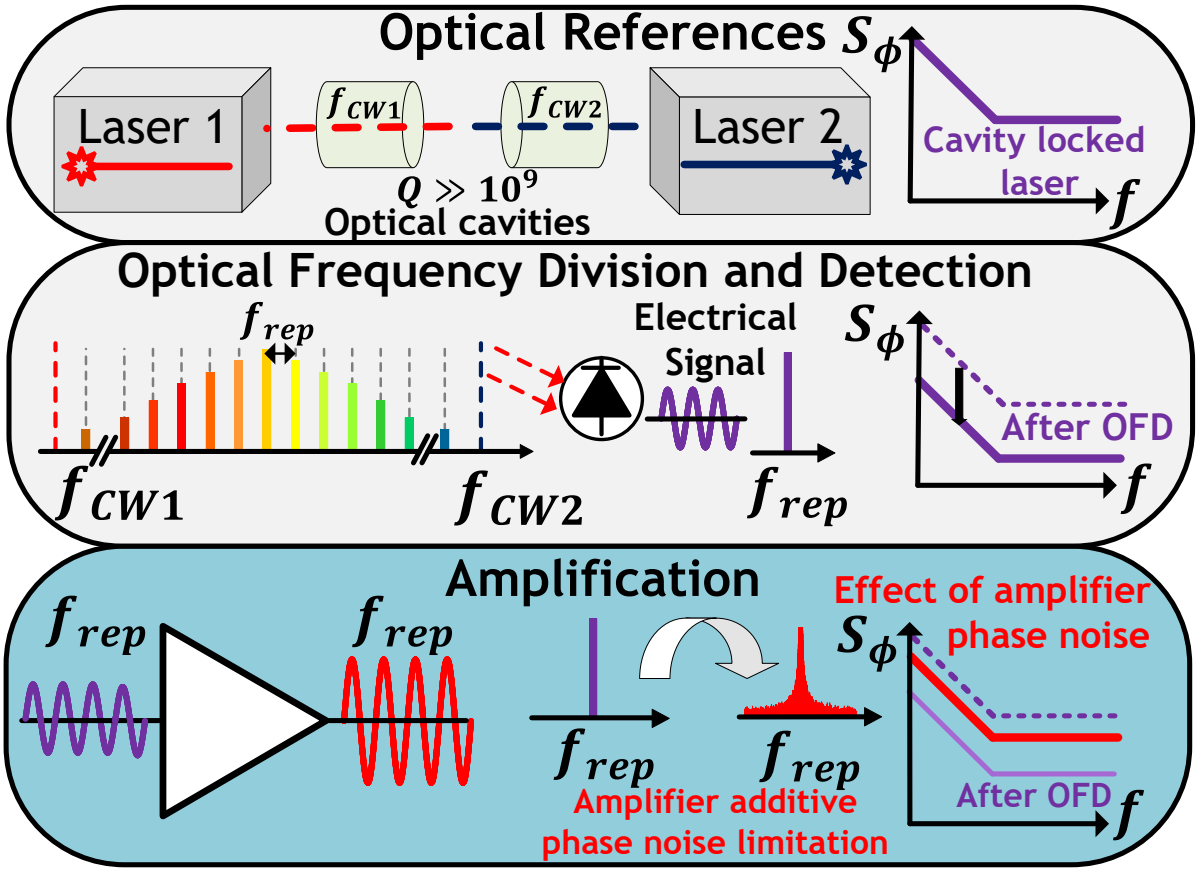


Figure 3.1: Demonstration of 2-point optical frequency division and effect of amplifier additive phase noise on low noise microwave signal. Two lasers are self-injected and locked to a cavity. A microcomb is used to generate beat notes for locking, followed by a photodetector for the detection and an amplifier for amplification.

Additive noise reduction technique has always been a topic of interest, and multiple papers have

been introducing methods to achieve phase noise reduction; the first approach involves using inherently low near DC flicker noise, which translates to phase noise and Heterojunction bipolar transistors benefit from it in compared with Field Effect Transistors [44, 45]. On the other hand, reducing the upconversion of flicker noise caused by nonliterary has been a topic of research for several decades [44, 46–48], and feedforward, feedback, and parallel architecture have been explored in detail.

Thus, this chapter is dedicated to investigating methods to enhance the frequency range of the power amplifier while simultaneously minimizing its additive phase noise and reducing both the form factor and power consumption of the amplifier.

3.2 Additive Noise in Amplifiers: Mechanisms and Effects

3.2.1 Additive White Noise

There are different sources of noise involved in the additive phase noise of the amplifier as plotted in Fig. 3.2. However, the most dominant parameters involved in the additive phase noise of the amplifier are the white noise and up-converted near DC noise. The additive phase noise of the amplifier can be described by the following equation [46]:

$$S_\phi(f) = b_0 + \frac{b_{-1}}{f} \quad [\frac{rad^2}{Hz}] \tag{3.1}$$

The white noise b_0 is based on random noise with power spectral density $N = FKT_0$ added to the carrier's input power (P_{in}) and be calculated using $b_0 = \frac{FKT_0}{P_{in}}$ where K and T_0 are Boltzmann constant and reference temperature respectively and F is amplifier noise figure.

3.2.2 Flicker Noise Up-Conversion

The origin of the 1/f noise is due to random fluctuation [89]; although the 1/f noise has a low-pass nature, due to nonlinearities of the transistor, the 1/f noise will upconvert to frequencies of interest

and create a sideband at frequencies close to the carrier [48]. The major 1/f noise in an HBT device originates in the base, with both the base and collector currents significantly influencing the baseband noise characteristics of HBTs [90]. Due to the amplifier's nonlinearity, these noise components are ultimately upconverted to the carrier frequency, contributing to additive phase noise.

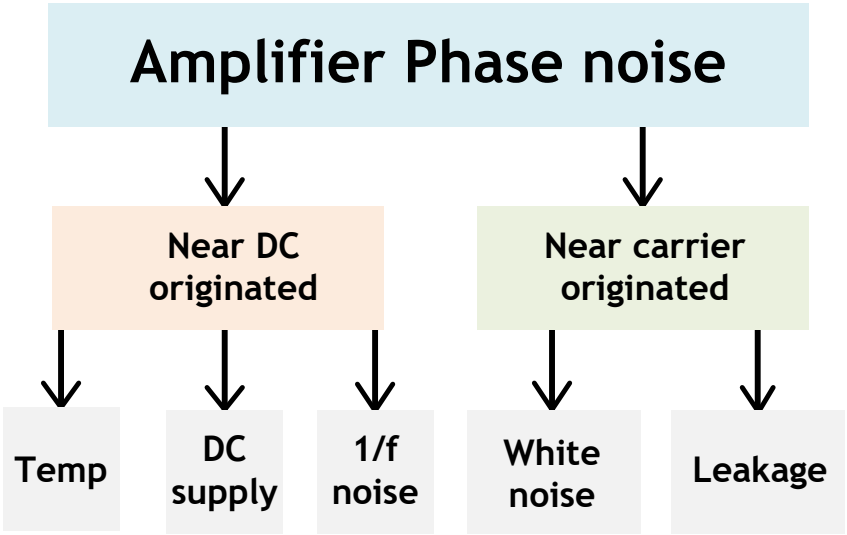


Figure 3.2: Amplifier Phase noise mechanism.

One potential and effective way to minimize the additive phase noise of the amplifier in the flicker noise region is parallel architecture. By considering that each noise source of any given amplifier is independent of the other amplifiers, the noises added in RMS value while each transistor contributes directly to the total output power [44, 46] as a result, the total signal-to-noise ratio of each pair of parallel amplifiers achieves around 3 dB better phase noise performance in compared to one single amplifier generating the same output power.

Furthermore, when multiple amplifiers are cascaded, the Friis equation [91] applies:

$$F_{\text{total}} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}} \tag{3.2}$$

where

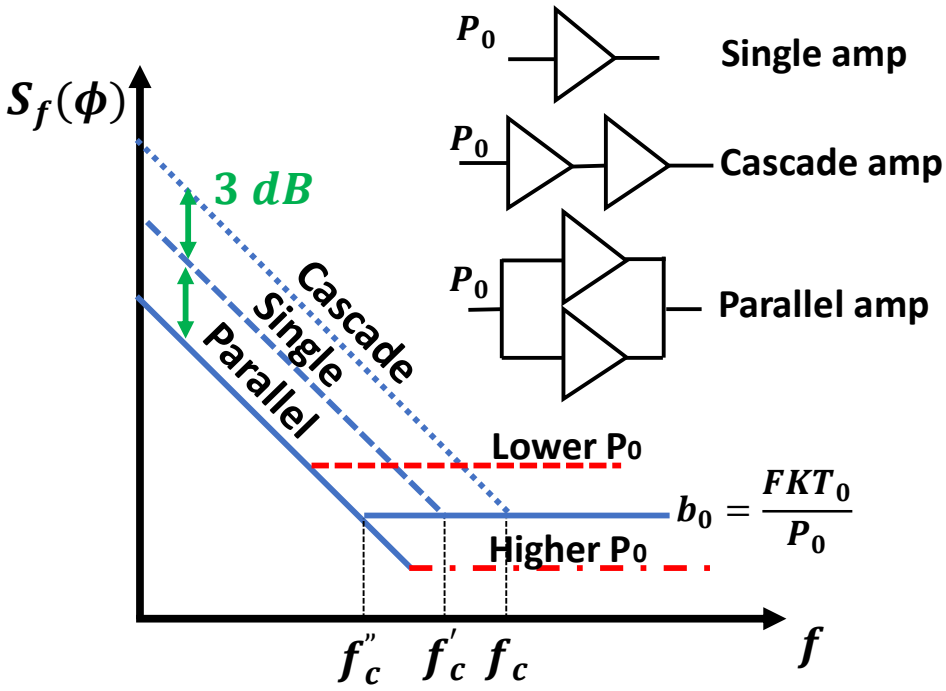


Figure 3.3: Phase noise comparison between single, parallel and cascade amplifiers.

- F_{total} is the total noise figure of the cascaded system
- F_1, F_2,..., F_n are the noise figures of individual stages
- G_1,G_2,...,G_{n-1} are the gain of individual stages

Since the 1/f noise of each amplifier is independent of the others, both flicker noise and white noise in a two-stage cascaded amplifier configuration are 3 dB higher than those of a single amplifier, as illustrated in Fig. 3.3.

The rest of this chapter explores effective methods to further minimize the additive phase noise in amplifiers, with a particular emphasis on the upconversion of flicker noise.

3.3 A Wideband Power Combined Power Amplifier in 250 nm InP HBT

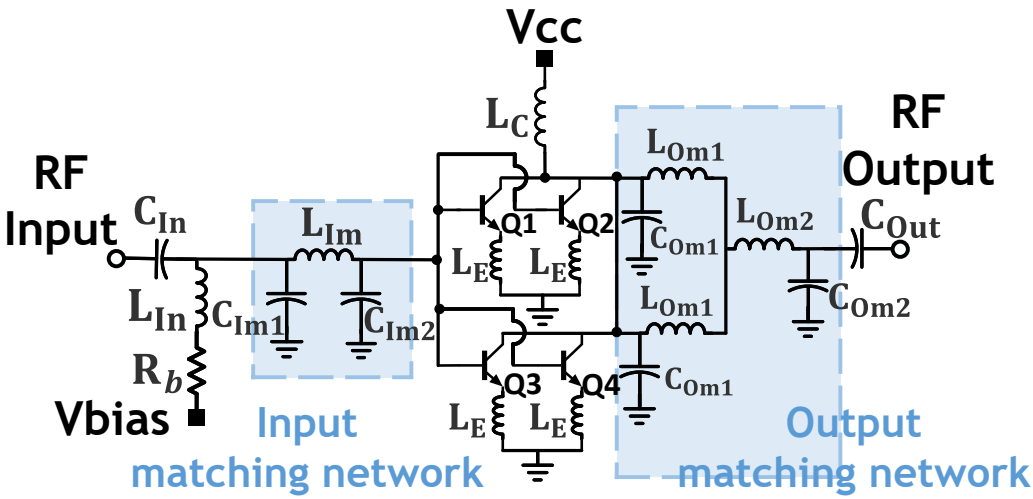
3.3.1 Design Consideration and Implementation

As mentioned earlier, the additive phase noise of the amplifier is highly dependent on both nonlinearities of the amplifier and low-frequency 1/f noise. For pushing the additive phase noise of the designed amplifier lower, the InP process is a more suitable choice over FET processes. The InP HBT transistors offer high breakdown voltage due to wide bandgap InP collectors and, as a result, are the appropriate choice for high-power applications. moreover, they have an advantage over Si and GaAs technologies due to high frequency and low noise performance [92].

This section presents a broadband parallel HBT InP amplifier for C and X-band applications. By taking advantage of both low near DC flicker noise offered by InP HBT and the power splitting and combining technique for parallel amplifiers, low additive phase noise is achieved in a wide range of frequencies. Both simulation and measurements result shows more than 18 dBm saturated output power and 20% Power Added Efficiency (PAE) at 10 GHz carrier frequency.

Two main common typologies for X band HBT amplifiers are common emitter (CE) and cascade topologies. Cascade topologies offer several advantages, such as high gain, good reverse isolation, higher stability, and simplified input and output matching network. However, they encounter several drawbacks, such as their higher noise figure due to the noise contribution of the common-base stage. higher DC power consumption [93], large parasitic capacitance on the shared node. The reduction of shared node capacitance can be done by introducing an interstage inductor or transmission line to resonate out the capacitance. However, it is critical to note this additional inductor can cause large physical size and additional losses to the circuit. As a result, a common emitter configuration is chosen over the cascade structure.

The proposed power amplifier is based on parallel architecture to benefit from power splitting input and power combining output. Fig. 3.4. shows the schematic of the proposed power amplifier.



C_{In}=1080 fF	C_{Im2}=165 fF	C_{Om1}=108 fF	R_b=100	C_{Om2}=132 fF
L_{In}=0.97 nH	L_E=0.18 nH	L_{Om2}=0.4 nH	L_C=1.7 nH	L_{Im}=0.52 nH
L_{Om1}=0.6 nH	C_{Out}=1080 fF	C_{Im1}=81 fF	Q1-Q4=8*250 nm	

Figure 3.4: Schematic of the power amplifier.

The design includes four gain units sharing a Pi-shaped input-matching network to achieve minimal noise levels across a broad operational range. The series base inductor L_{In} is used to cancel out the input reactance of the base-emitter capacitor of transistors, C_{In2}, and also provide the minimum noise figure input impedance for a wide range of frequencies. Furthermore, L_{In} needs to experience high quality factor to sustain high output power and minimize noise. In the direction of mitigating this concern and reducing the shunt capacitors associated with inductors, the spacing between inductors and the ground cut was increased from 10 µm to 20 µm and the quality factor and inductance value of L_{In} improved by 8.2% and 11% as illustrated in Fig. 3.5. The input impedance of the designed amplifier and the full EM simulated minimum and actual noise figure are demonstrated in Fig. 3.6(a) and Fig. 3.6(b), respectively while the amplifier is biased in class A operation mode.

As mentioned earlier, more than the power generated by a single unit gain may be required for applications requiring high output power. Moreover, parallel architecture can enhance the amplifier's

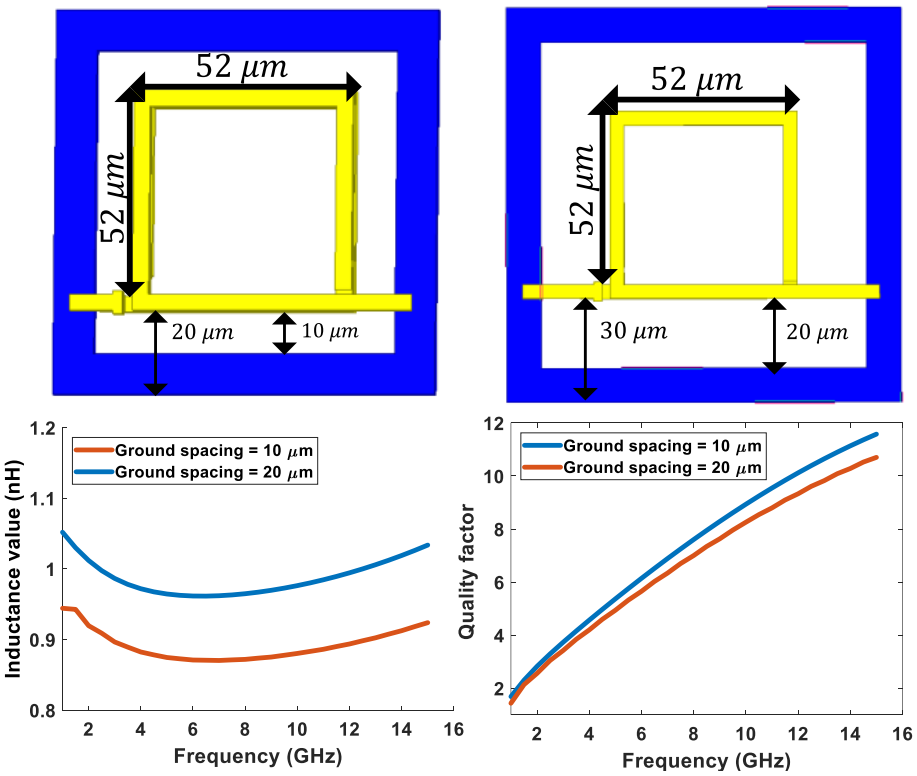


Figure 3.5: The effect of the ground spacing on inductor value and quality factor.

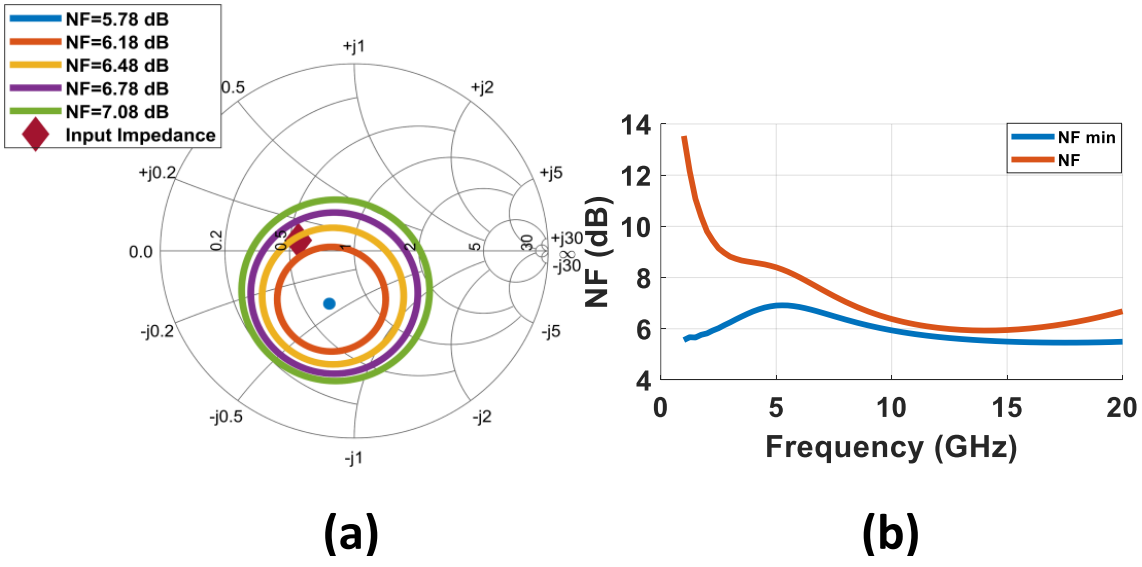


Figure 3.6: (a) Constant noise figure (NF) contours under class A operation region and input impedance of the low phase noise amplifier (center frequency=10 GHz). (b) Simulated minimum and actual NF of the amplifier.

additive phase noise. Consequently, a power combining technique needs to be deployed in design to improve the generated output power and additive phase noise with the cost of higher DC power consumption. An output matching network is designed to minimize the drawbacks associated with large and bulky traditional power combiners and still take advantage of the benefits of parallel architecture. Two stages of the L-shaped output matching network are designed to increase the power generated by each power cell, as demonstrated in Fig. 3.7(a). The quality factor of the inductors, particularly L_C, significantly influences the amplifier's capabilities to sustain high-output power for a wide range of frequencies. Thus, a custom cascaded inductor with a value of 1.7 nH and a quality factor of 10 was designed. Given the high number of inductors in the output-matching network, potential coupling may become a major concern. Therefore, a minimum spacing of 25 µm was chosen between the inductors to minimize the coupling effect.

The flicker noise contributes to the additive phase noise of the amplifier and has a low-frequency profile. However, due to nonlinearities inherent in the amplifier, this flicker noise undergoes upconversion to the carrier frequency. One of the main factors in this upconversion process is the ratio between the second harmonic and fundamental tone [46]. Therefore, the output matching network deployed in the design targets explicitly second harmonic suppression for reducing the additive phase noise of the amplifier in the 8-12 GHz frequency range, as shown in Fig.3.7(b). The second harmonic suppression, even at -5 dBm input power, is more than 25 dB, highlighting a notable reduction in up-converted flicker noise.

A 100 Ω ballast resistor was added to the base of the amplifiers to mitigate the thermal runaway and help with the stability of the circuit. Furthermore, a 180 pH inductor was added to the emitter of each unit cell to increase the linearity and stability of the amplifier with the cost of gain reduction.

By considering that each noise source of any given amplifier is independent of the other amplifiers, the noises added in RMS value while each transistor contributes directly to the total output power [44, 46] as a result, the total signal-to-noise ratio of the four parallel amplifiers achieves around 6 dB better phase noise performance in compared to one single amplifier generating the same output power. The quiescent base and collector currents are chosen to achieve more than 15 dB gain and

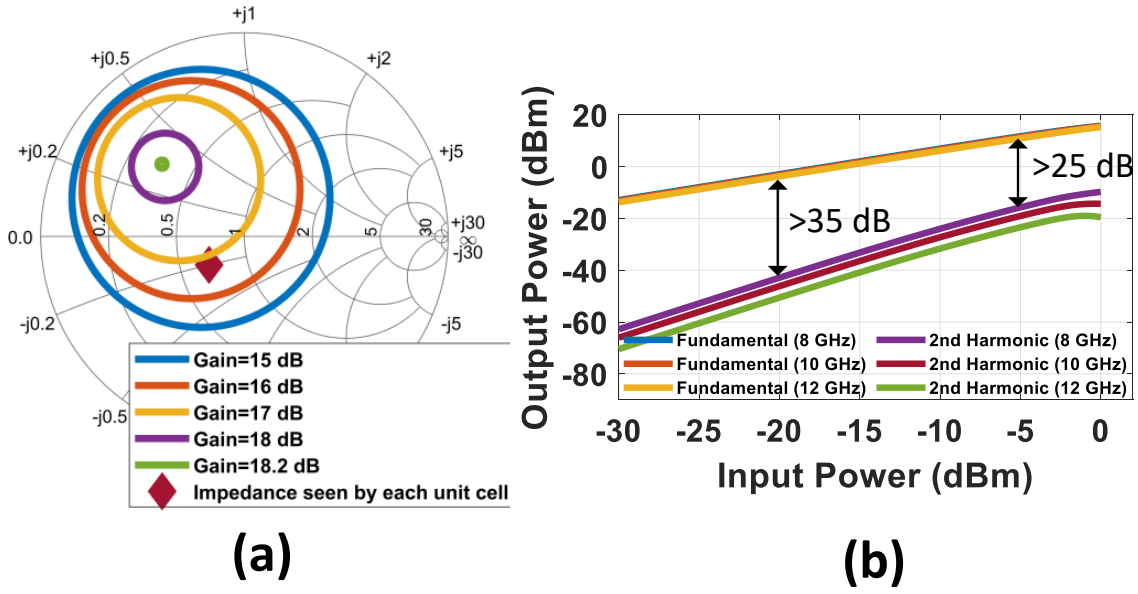


Figure 3.7: (a) MSG (Maximum Stable Gain) contours and impedance seen by low phase noise amplifier in class A operation mode (center frequency=10 GHz). (b) Simulated fundamental and second harmonic output powers versus input power for different center frequencies.

lower than -150 dBc/Hz additive phase noise at 10 kHz offset frequency in the frequency range of operation.

3.3.2 Measurement Results

The low-phase noise amplifier was fabricated in Teledyne InP 250 nm HBT process with more than 300 GHz and 600 GHz unity current gain frequency Ft and maximum oscillation frequency $Fmax$ and 4.5 V break down voltage, which make it an ideal candidate for X band applications. The die photograph of the fabricated amplifier is shown in Fig. 3.8, and the amplifier is biased in class A operation mode with a collector current and Vcc of 42.5 mA and 3.1 V, respectively. MPI GSG probes with 100 µm pitch are served for RF measurements; DC biases were provided using MPI multi-contact probes.

Small signal characterization is measured using a Keysight PNA-X Vector Network Analyzer and an on-die TRL calibration standard set is used to calibrate the measurements and set the reference

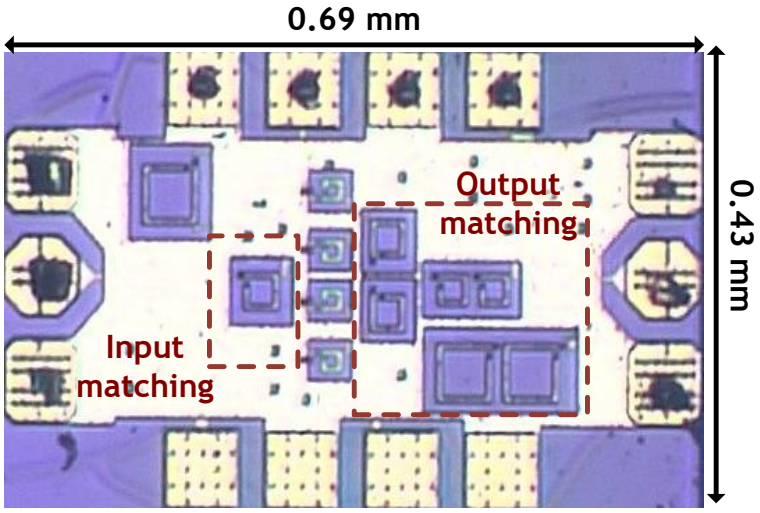


Figure 3.8: Die photograph of the fabricated low phase noise amplifier.

plane to where the pads connect to transmission lines. The simulated and measured S parameters are shown in Fig. 3.9. The peak S_{21} is 18.1 dB at 2.76 GHz and the PA achieves a fractional 3 dB bandwidth of 2.18 to 13.51 GHz (144%).

A Rohde and Schwarz FSWP phase noise analyzer is used for large signal characterization and measurement. The measurement setup involves generating an input signal with the PNA and measuring the output power with the same phase noise analyzer. Large signal gain and output power are plotted against available input power at multiple output frequencies in Fig.3.10. The saturated output power is 18.2 dBm with a 11.1 dB large signal gain at 10 GHz frequency. The output 1 dB compression point is 15.8 dBm with 21.0 % PAE and 15.8 dB large signal gain, with matched correlation with full- EM post layout simulation using HFSS. The 1_{dB} compression point and Psat of the fabricated amplifier is plotted against input frequency in Fig. 3.11.

Additive phase noise measurements are performed using Rohde and Schwarz FSWP phase noise analyzer. The PNA employs digital cross-correlation for phase noise measurement, with capabilities of separate measurement for both amplitude and phase noise. The accuracy of the phase noise measurements was improved by increasing the number of correlation factors, and the instrument noise floor did not limit the phase noise measurement. The setup showed capabilities to character-

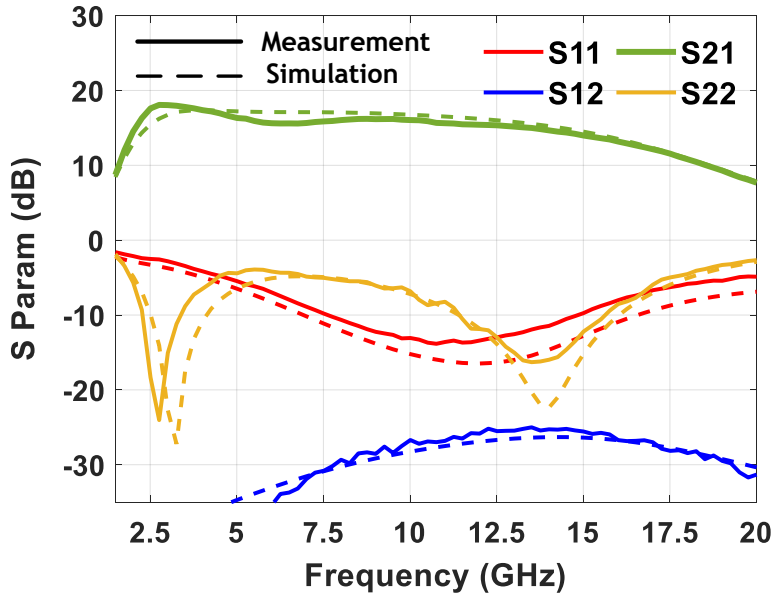


Figure 3.9: S Param simulation and measurement results of the fabricated amplifier.

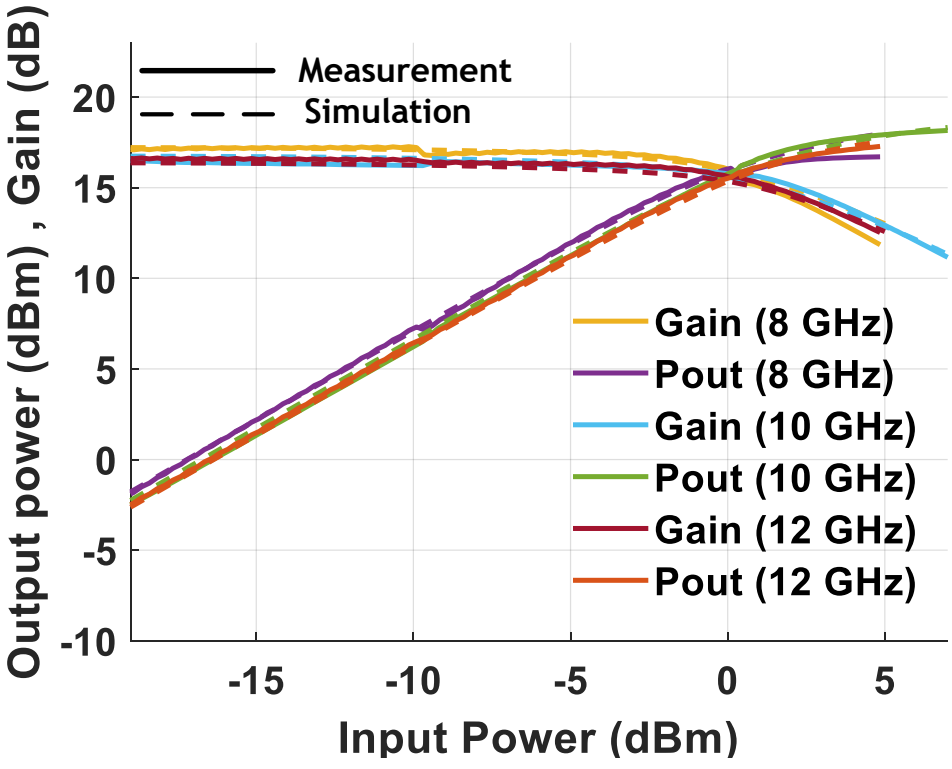


Figure 3.10: Large signal simulation and measurement results of the fabricated amplifier.

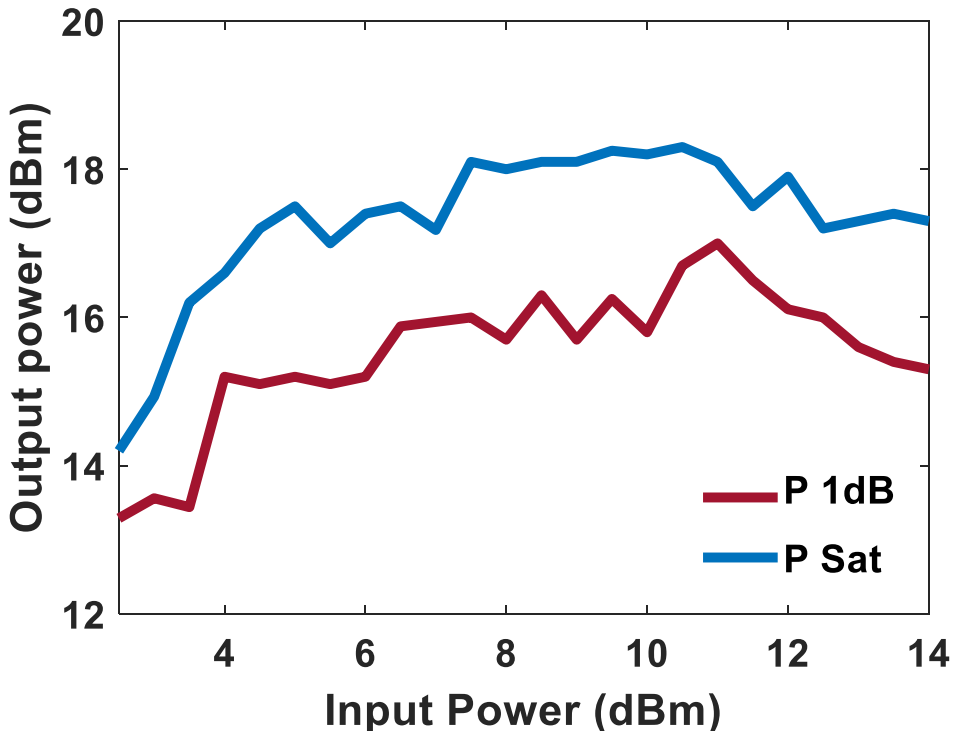


Figure 3.11: Measured 1_{dB} compression point and Psat of the fabricated amplifier versus input frequency.

ize an additive phase fluctuation down to -165 dBc/Hz at 10 kHz offset from 10 GHz; however, the time of the measurements increased ($\approx \times 2.4$).

The additive phase noise measurement results are demonstrated in Fig. 3.12(a). for different carrier frequencies versus offset frequency, the amplifier exhibits less than 5 dB variation in additive phase noise and less than 0.9 dB variation in 1_{dB} compression point along the measured frequencies while biased in the class A operation as summarized in table3.1.

Furthermore, to examine the effect of different classes of operation, the class of operation is switched from class A to class B/C, and the phase noise measurement result also illustrated in Fig.3.12(b) the additive phase noise decreases by more than 7 dB, reaching -157.3 dBc/Hz at 10 kHz offset. In comparison, the highest large signal gain of the amplifier drops significantly to 6.5 dB at 10 GHz carrier frequency.

Finally, a single-transistor amplifier was designed for comparative analysis. Additionally, two

Center Frequency (GHz)	Phase noise @10 kHz (dBc/Hz)	Phase noise @ 1 MHz (dBc/Hz)	P 1_dB (dBm)	P sat (dBm)
4	-151.5	-161.3	15.2	16.6
8	-148.6	-157.7	15.7	18
10	-150	-156.1	15.8	18.2
12	-150.1	-159.3	16.1	17.9
14	-153.5	-160.1	15.3	17.3

Table 3.1: 1_{dB} compression point, saturation output power, and additive phase noise at 10 kHz and 1 MHz offset from different carrier frequencies (Pin=-2.2 dBm).

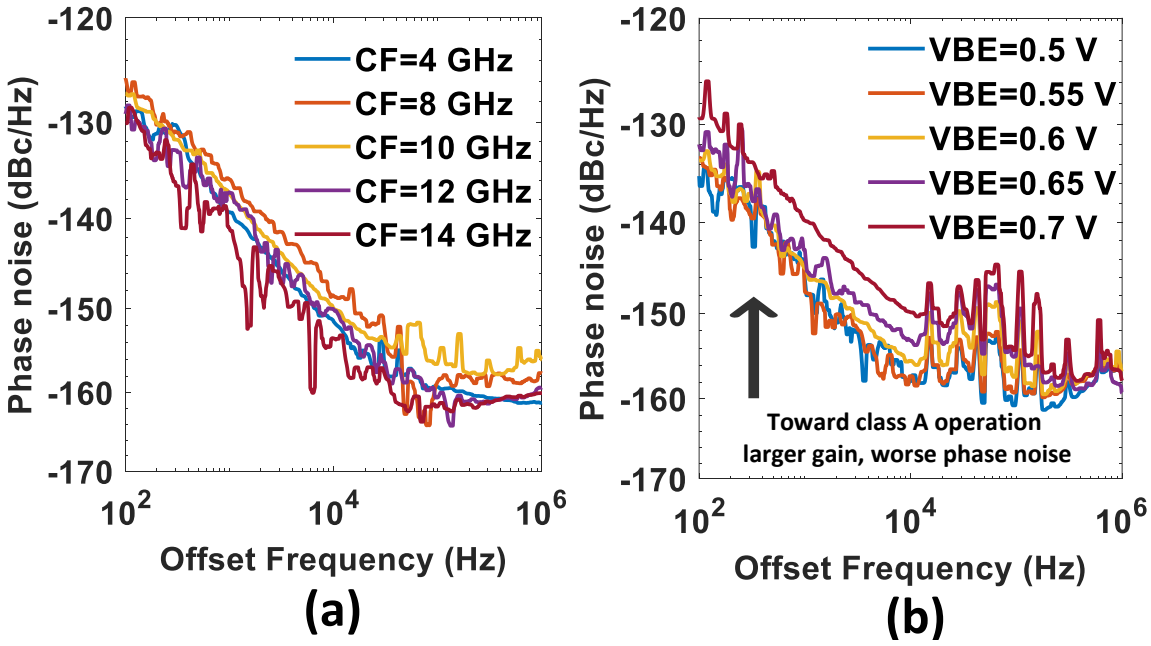


Figure 3.12: (a) Additive phase noise measurement of the amplifier for different carrier frequencies while the amplifier is biased in class A operation range (Pin=-2.2 dBm) . (b) Additive phase noise measurement of the amplifier while the amplifier is biased in class B/C operation range (CF=10 GHz).

parallel amplifiers were cascaded, and the additive phase noise performance of the cascaded configuration was evaluated. The measured additive phase noise results for the single, cascaded, and parallel amplifier setups at a 10 GHz carrier frequency with a -10 dBm input power are presented

in Fig. 3.13. As expected, the parallel amplifier demonstrates approximately 6 dB lower flicker noise compared to the single amplifier, while the cascaded amplifier exhibits 3 dB higher phase noise.

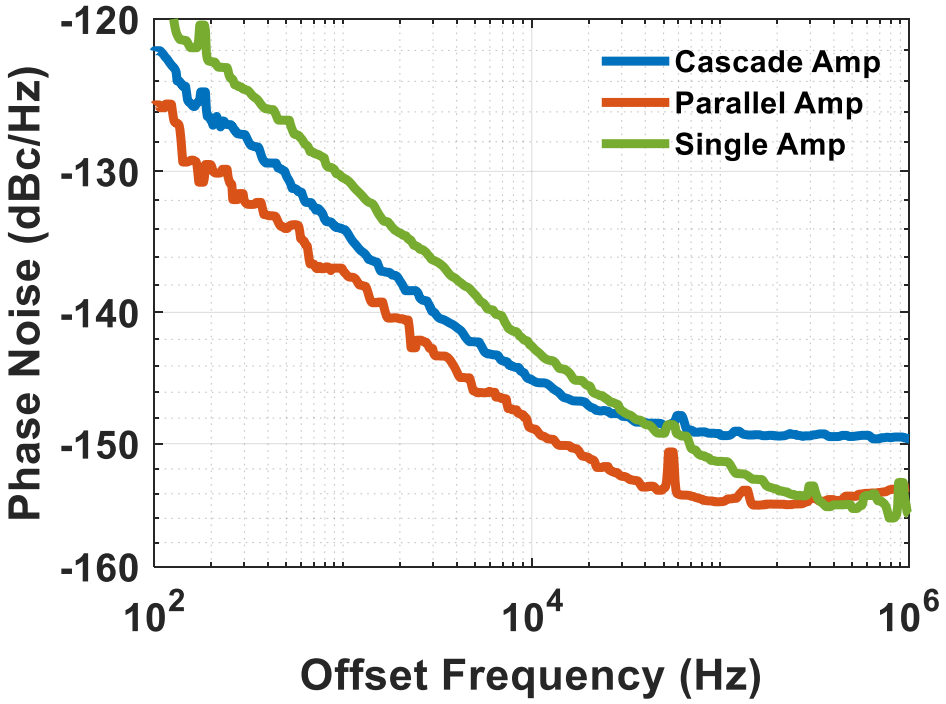


Figure 3.13: Phase noise comparison between single, cascade and parallel amplifiers

Table 3.2 summarizes the proposed broadband PA in comparison with commercialized low-phase noise amplifiers measured in [44, 46]. As can be seen, the proposed PA maintains a phase noise performance of -150 dBc/Hz at a 10 kHz offset, with comparable or better performance in gain and output power compared to others, while consuming significantly lower DC power.

3.3.3 Conclusion

A wideband low-phase noise PA in the InP 250 nm HBT process has been demonstrated in this subchapter. The small signal gain has a 3 dB bandwidth greater than 11.3 GHz from 2.18 to 13.51 GHz with a peak gain of 18.0 dB, a saturation output power of 18.1 dBm, and additive phase noise of -150.0 dBc/Hz at 10 kHz offset from 10 GHz while occupying only 0.296 mm^2. This

Table 3.2: Table of comparison of broadband InP amplifier

Power Amplifier	AML812PNB1901,Ref [46]	AFS6, Ref [46]	JS2, Ref [46]	HMCC-5618, Ref [44]	This Work
BW_3dB (GHz)	8-12	8-12	8-12	6-20$^{\$}$	**2.18-13.51**
P_{1dB} (dBm)	17	16	13.5	18$^{\$}$	**15.7**
Peak S_{21} (dB)	22	44	17.5	14$^{\$}$	**18.07**
Phase noise at 10 kHz (dBc/Hz)	-158*	-142*	-142*	-151*	**-150**
DC power consumption(mW)	6375	2565	1380	575$^{\$}$	**136**

$*$ Graphically estimated at 10 GHz. $ Based on device datasheet.

performance and consistency over a wide frequency range enables low phase noise, high output power, and compact design and improves the EVM and BER of the communication systems.

3.4 X-band Feed Forward Low Phase Noise Amplifier in 250 nm InP HBT

While the implemented low-phase-noise amplifier represents a significant advancement in low-phase-noise amplification and introduces an effective method to reduce additive phase noise beyond conventional designs, further efforts are needed to push the boundaries of low-phase-noise amplification even further and to mitigate the upconversion of flicker noise into phase noise.

An effective approach to reducing the additive noise of amplifiers and minimizing Intermodulation Distortion (IMD) is the utilization of feedforward and feedback amplifier techniques.

The utilization of feedforward amplifiers to reduce phase noise has been a subject of continuous research and traditional feedforward scheme has gained interest due to its capability for phase and

amplitude noise reduction [46, 94, 95]. However, the physical size and chip-scale integration of such systems are big limiting factors. This sub chapter presents a new modified schematic for a feedforward amplifier to further push down the additive noise of amplifier and by employing a noise canceling scheme 7.5 dB phase noise reduction is achieved at 10.5 GHz carrier frequency and the amplifier shows a small signal peak gain of 15.9 dB.

3.4.1 Phase Noise Analysis and Circuit Design

The utilization of feedforward and feedback amplifiers to mitigate Intermodulation Distortion (IMD) has been a subject of continuous research over the past several decades [96, 97]. The feedforward scheme has gained extensive popularity due to its capability to provide a wide linearization bandwidth and excellent capabilities for phase and amplitude noise reduction [98].

The principle operation of the feedforward noise cancellation can be described as follows: the input signal, after being amplified by the main amplifier, is compared and subtracted from the original input signal, and as a result, the input of the Aux amplifier mainly contains noise and distortion originating from the main amplifier and ideally devoid of any carrier signal. The noise and distortion would be amplified and then subtracted from the input at the output of the coupler by proper phase and amplitude adjustment as illustrated in Fig. 3.14. The efficacy of phase and amplitude noise cancellation largely are dependent on proper carrier suppression and noise suppression in two interferometers, carrier cancellation loop, and noise cancellation loop, and the phase noise equation for the feedforward amplifier is shown in Equation.3.3 and a deeply detailed derivation of the equation can be found in [98]. Equation. 3.3 illustrated that with the close-to-ideal carrier suppression, the phase noise of the output signal is subjected to the noise figure of the AUX amplifier and noise suppression in the second interferometry.

$$S_{\phi}^{FFA}(f) = \frac{S_{\phi}^{Main}(f)}{NS} + \frac{k_B F_{aux} T_0 L_{T1}}{P_{in}(1-\eta_1^2)(1-\eta_2^2)} + \frac{S_{\phi}^{Aux}(f)}{CS} \tag{3.3}$$

However, feedforward amplifier highly suffers from a large form factor primarily attributed to

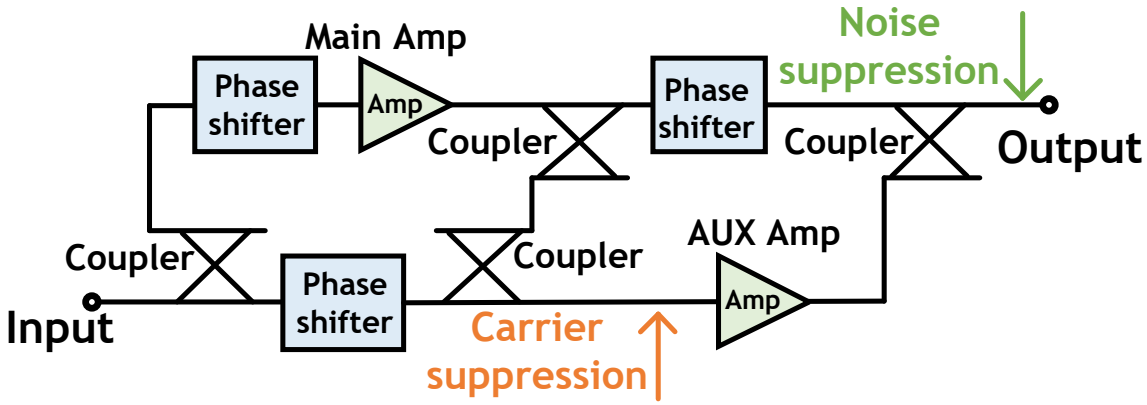


Figure 3.14: Traditional feedforward scheme required several phase shifters and couplers for carrier and noise suppression at the input of AUX amp and the output.

the presence of numerous couplers and inductors, and high DC power consumption. As a result, implementing a broadband, efficient feedforward scheme in the X-band frequency range on a single chip is challenging. Moreover, the noise figure of the proposed feedforward amplifier is relatively higher than the traditional low noise amplifier in X-band and C-band frequency ranges due to a high number of losses associated with the number of couplers along the way.

In order to address the above-mentioned challenges and still benefit from the noise and distortion cancellation offered by the feedforward amplifier, a new modified schematic of the amplifier has been proposed as illustrated in Fig. 3.15. In this new schematic, the input signal goes through an unbalanced to balanced conversion using a passive balun, followed by a differential class A power amplifier serving as the main amplifier. The output of the differential amplifier is connected to a rat-race coupler, whereas in one output arm, the interferometry between the inputs is conservative and on the other is destructive. Consequently, carrier suppression occurs in one arm, while carrier addition takes place in the other arm. The carrier-suppressed output goes through another unbalanced to balanced transformation using a passive balun, followed by an AUX amplifier utilizing the identical schematic as the main amplifier.

The AUX amplifier output is also connected to a rat race coupler, and the carrier-suppressed arm of the rat race coupler is terminated with a 50 Ω on-chip resistor. Subsequently, the carrier-added

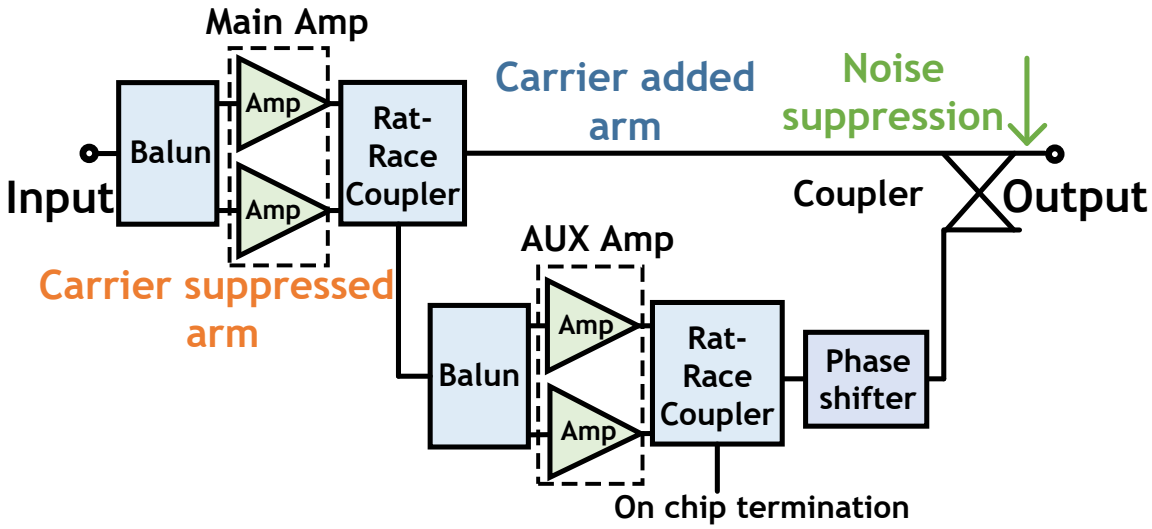


Figure 3.15: New implemented schematic for feedforward amplifier aim to decrease the number of couplers and phase shifter by utilizing rat-race couplers which potentially have the capability to add and subtract the carrier at each arm.

output of both rat-race couplers is directed through a coupler to suppress the noise and distortion of the main amplifier through appropriate amplitude and phase adjustments. By reducing the number of couplers utilized in the new modified schematic, the number of required inductors has significantly decreased from 30 to 11, thereby rendering the on-chip implementation of the feedforward amplifier more feasible in the realm of integrated circuits.

3.4.2 Main and AUX Amplifier Design

One of the key components in the feedforward schematic is the core amplifier which serves as both main and AUX amplifier and the noise and gain generated by it would highly affect the whole performance of the noise cancellation schematic.

In order to achieve low additive phase noise in a broad range of operations, a power-combined scheme is required, however as stated earlier in this chapter Wilkinson and DAT-based power combiners suffer from large physical size, as a result, the transistor-level power combined schematic is chosen. Furthermore, to push the additive phase noise of the proposed low-phase noise amplifier even lower and benefit from the differential output and common mode noise rejection, differential

topology is implemented in the design. The schematic of the core amplifier is shown in Fig. 3.16.

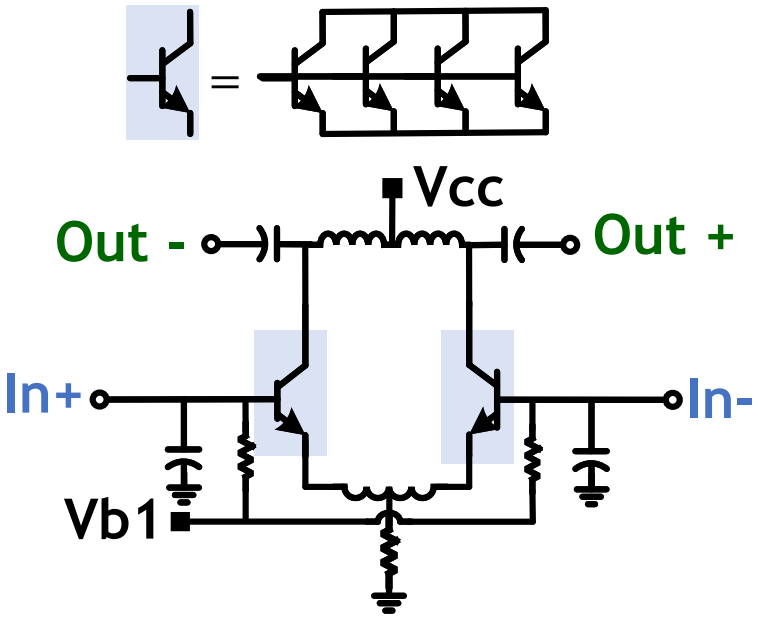


Figure 3.16: Schematic of core and AUX amplifiers.

A single-to-differential transformation for input is required to attain compatibility with a single output from a photodetector while still leveraging the benefits of a differential design. Thus, a passive balun is implemented in the design serving a dual purpose: to match the input impedance of the entire system to 50 Ω and also to match the noise figure of the amplifier to the minimum achievable noise figure, as illustrated in Fig. 3.17. The flicker noise upconversion from near DC to the carrier highly relies on the ratio between the second harmonic and fundamental [44, 46]. To suppress the upconversion of flicker noise, an output matching network, and the differential topology are coupled together to minimize the second harmonic to fundamental ratio as illustrated in Fig. 3.18.

The amplifier was fabricated in the Teledyne InP 250 nm HBT process and is biased with 3.2V V_{cc} and 60.5 mA DC current for class A operation. The amplifier's small-signal simulation and measurement results are shown in Fig. 3.19. The amplifier demonstrates a small signal peak gain of 17.2 dB and more than 4 GHz 3_{dB} bandwidth (7.75-11.75 GHz).

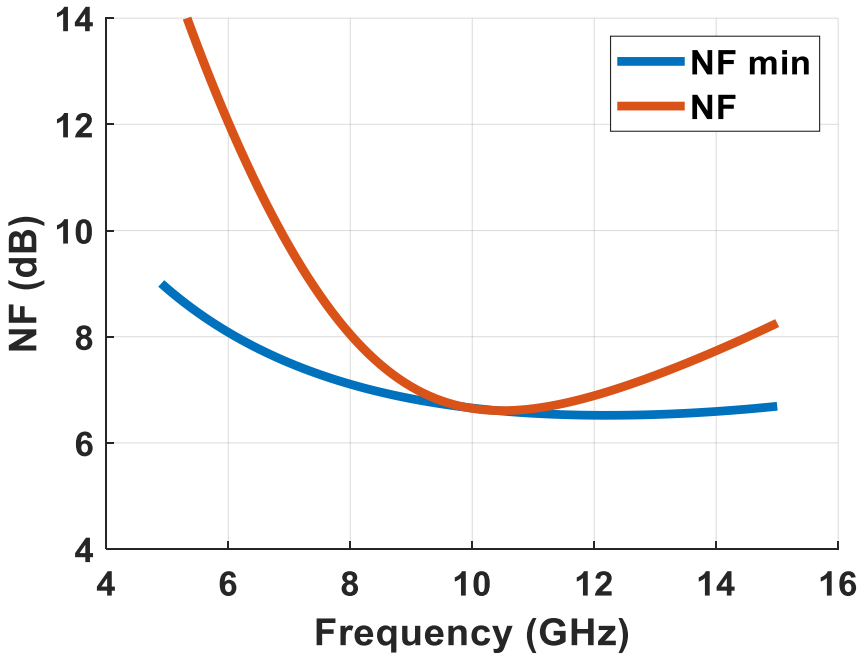


Figure 3.17: Simulated minimum and actual noise figure of the amplifier.

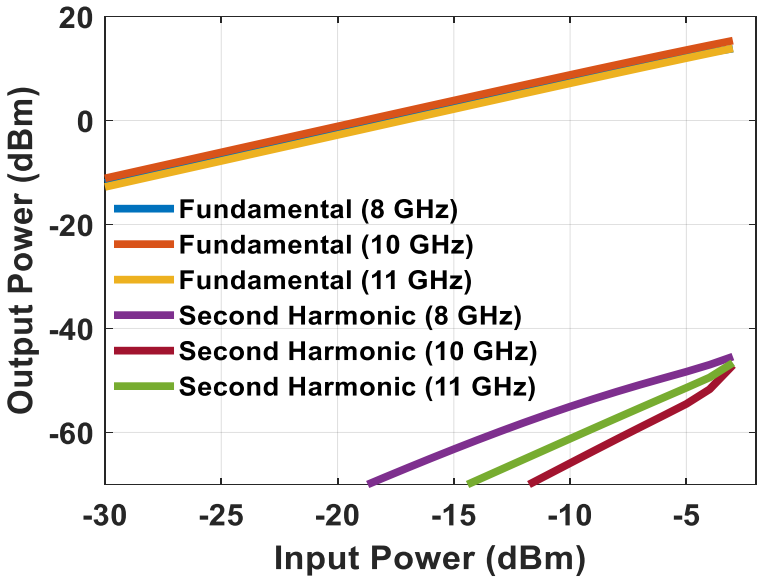


Figure 3.18: Simulated fundamental and second harmonic output powers for different center frequencies.

A Rohde and Schwarz FSWP phase noise analyzer is used to capture large-signal measurements. In Fig. 3.20. Output power and the large signal gain for various output frequencies are plotted versus available input power. The amplifier can generate more than 18 dBm output power at 10

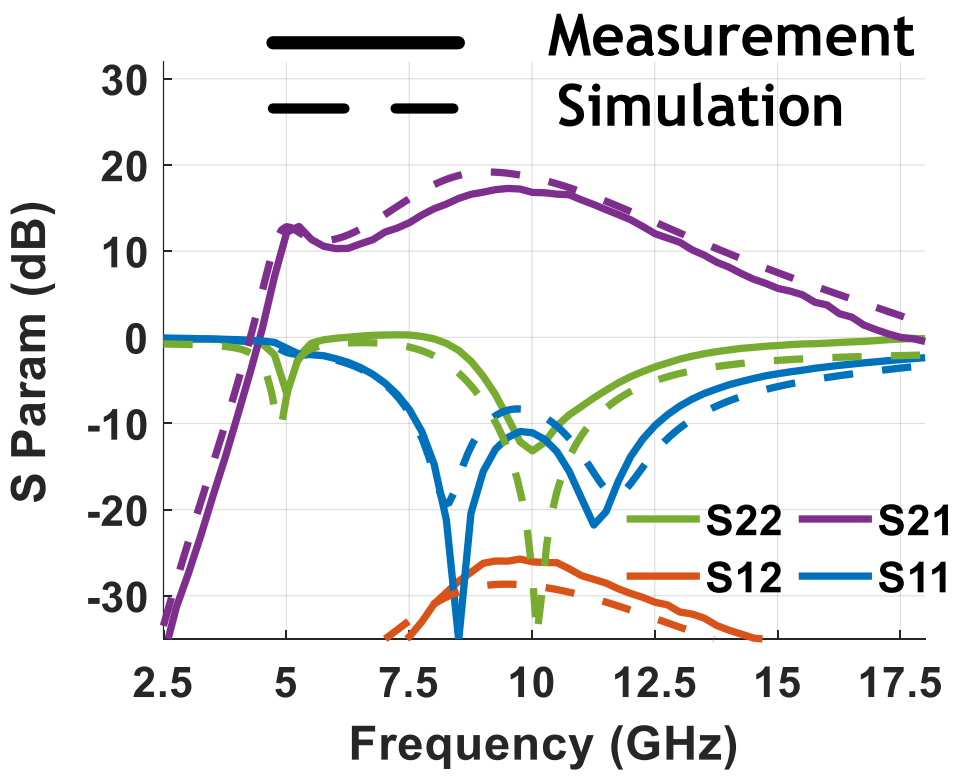


Figure 3.19: Small signal simulation and measurements results.

GHz carrier frequency. The additive phase noise measurements utilizing the same phase noise analyzer are conducted, and the additive phase noise measurements for different power at 10 GHz carrier frequency are plotted in Fig. 3.21. The amplifier could achieve an additive phase noise lower than -152 dBc/Hz at 10 kHz carrier frequency while the input power is 0 dBm.

3.4.3 Passive Balun and Rat Race Coupler

The input signal undergoes an unbalanced-balanced transformation using a passive balun as illustrated in Fig. 3.15. In order to mitigate the up-conversion of the flicker noise in an active device and improve the power handling capabilities of the balun, a passive transformer-based structure is utilized in the design both for the input of the main amplifier and the aux amplifier with the cost of higher conversion loss compared with active baluns. The input impedance of the proposed balun is matched to, and the output impedance is matched to the optimum source impedance for

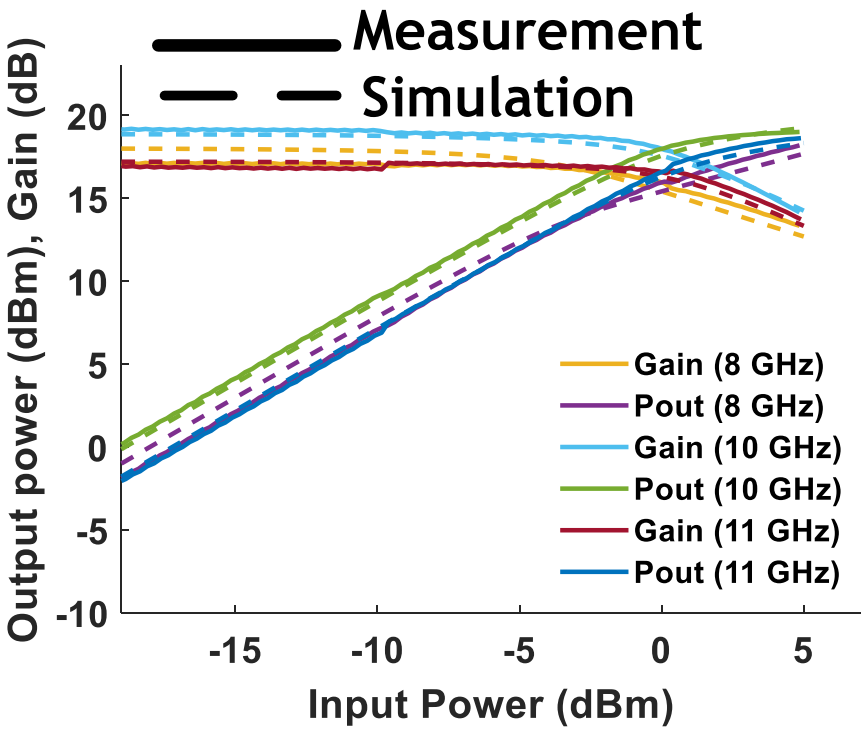


Figure 3.20: Large signal simulation and measurement results.

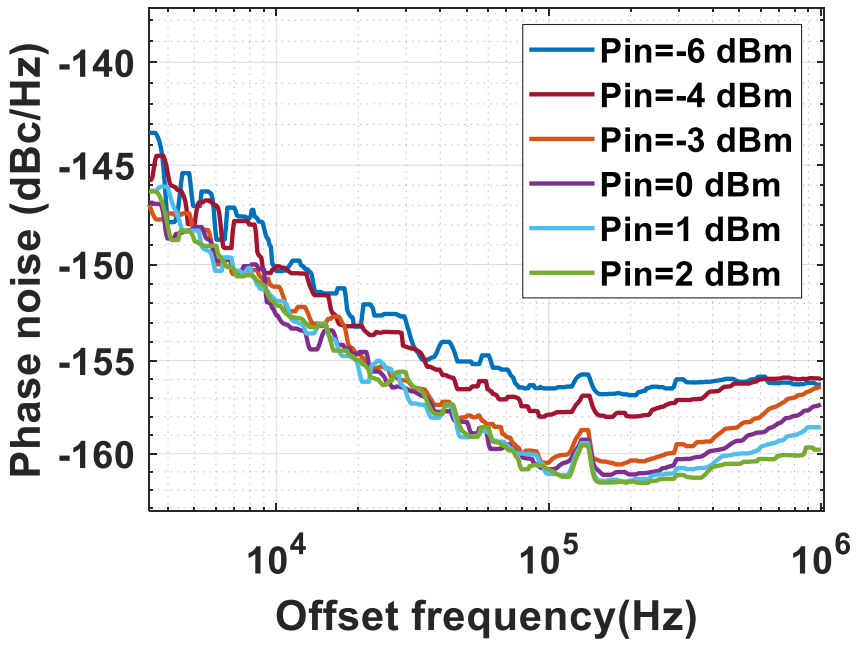


Figure 3.21: Phase noise measurement results of the low phase noise amplifier (CF=10 GHz).

noise figure matching. The balun time domain response and simulated small signal response are displayed in Fig. 3.22(a) and (b) respectively.

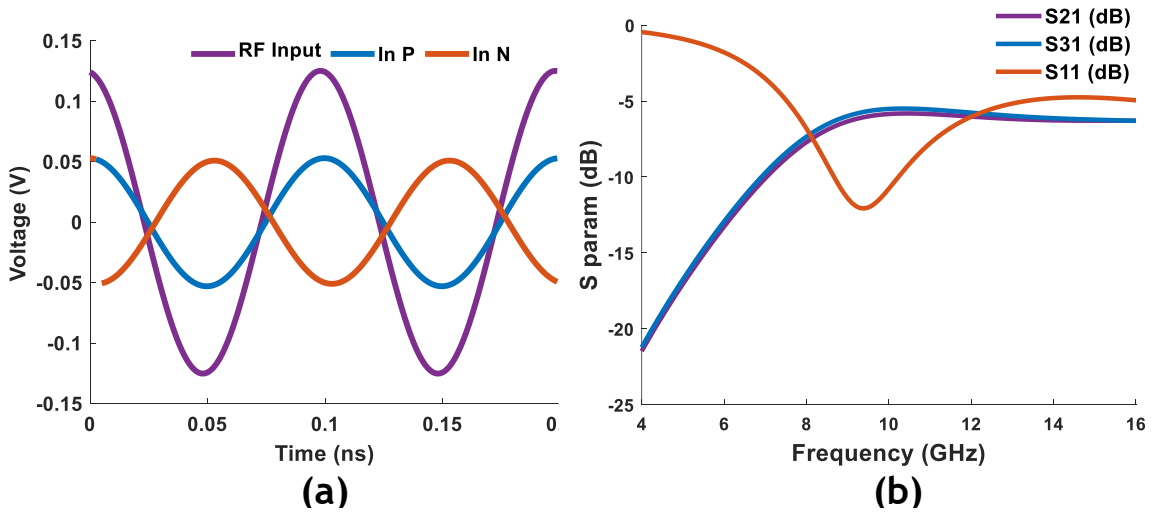


Figure 3.22: (a) Time domain and (b) Small signal simulations result of the implemented balun.

The rat-race coupler is required in the design to suppress the carrier in one arm and add up the carrier in the other arm, however, microstrip based rat-race couplers required $\lambda/4$ and $3\lambda/4$ transmission line to achieve 180-degree phase shift for the two outputs, which constitutes a significant limitation of rat-race couplers in the C and X-band frequency ranges. In order to achieve the required phase-shifted output and minimize the required space for the rat-race coupler, an LC-CL-based schematic is used to model the rat-race coupler at 10 GHz frequency. Time domain, Insertion loss, and amplitude imbalance of the proposed model are plotted in Fig. 3.23(a). and Fig. 3.23(b) respectively.

3.4.4 Measurement Results

The proposed feedforward amplifier is fabricated in Teledyne InP 250 nm process and both main and AUX amplifier collector voltage is set at 3.2 V with a base current of 2.2 mA and a collector current of 60.5 mA for each main and AUX amplifier to ensure class A operation mode. A Keysight Vector Network Analyzer is used for S-param measurement and an on-die TRL calibra-

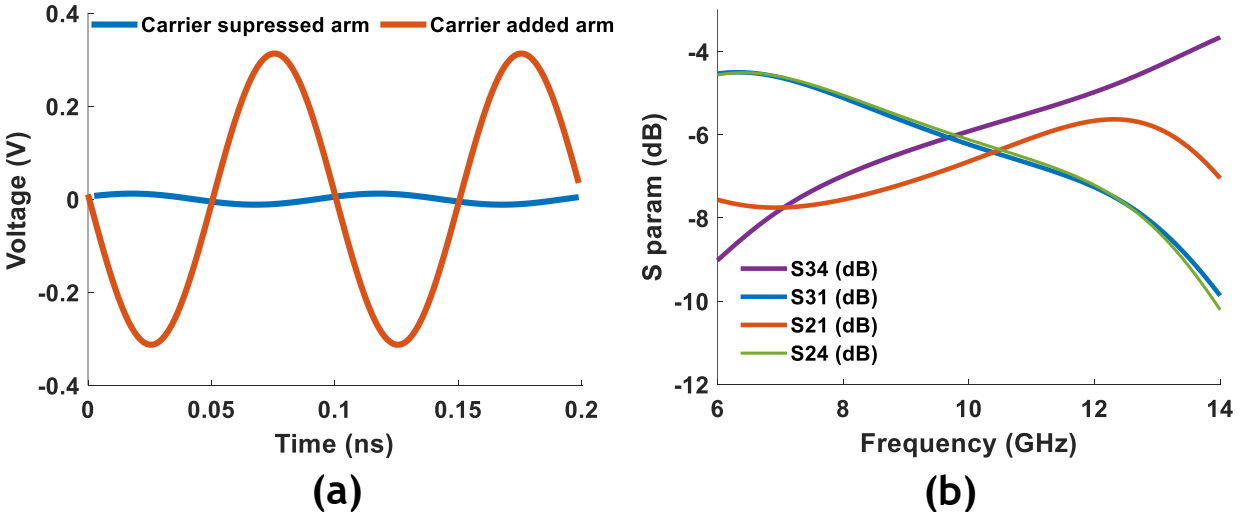


Figure 3.23: (a) Time domain and (b) Small signal simulations result of the implemented rat-race coupler.

tion calibrated the measurements. The simulated and measured S parameters are plotted in Fig. 3.24, and measurement of the fabricated amplifier indicates a peak gain of 15.9 dB and more than 4.4 GHz bandwidth (8.1-12.5 GHz).

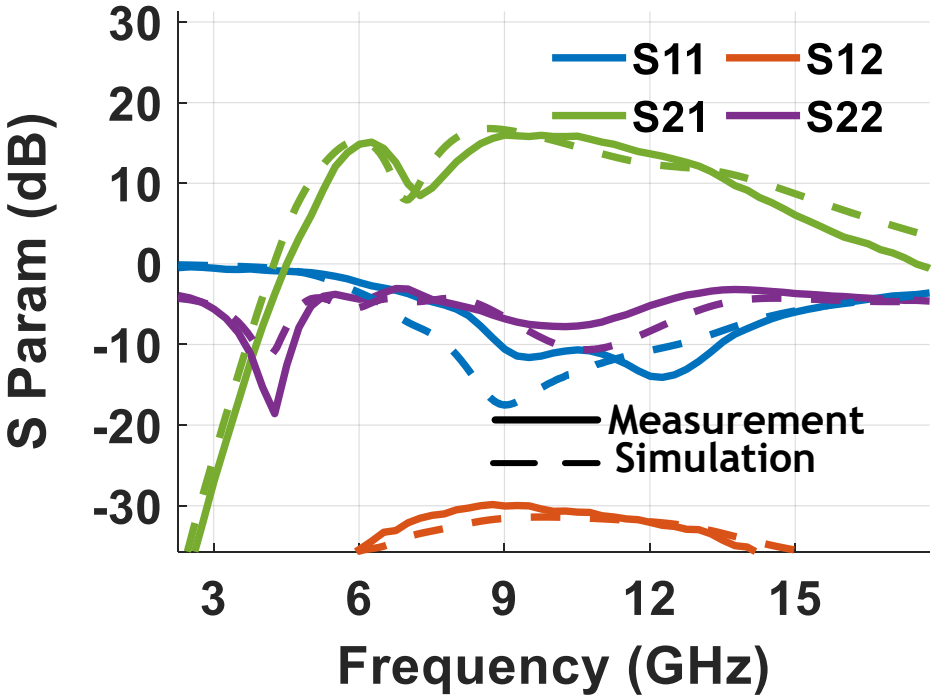


Figure 3.24: Simulated and measured S-param of the proposed amplifier.

A Rohde and Schwarz phase noise analyzer is used for large signal measurements serving as both an input source for the amplifier and as a signal analyzer. Large signal gain and output power for different carrier frequencies are demonstrated in Fig. 3.25. Both measurements and simulation show more than 15 dB large signal gain and 16.1 dBm P_{1dB} at 10 GHz.

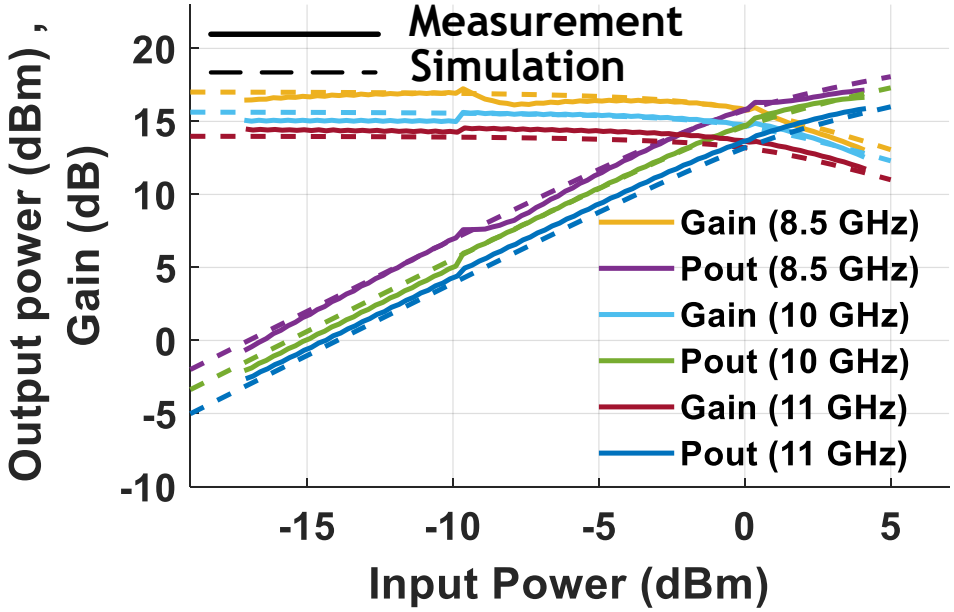


Figure 3.25: Large signal gain and output power of the fabricated amplifier.

The phase noise measurements are conducted using the same phase noise analyzer and the measurement setup enables the characterization of additive phase noise down to -165 dBc/Hz at a 10 kHz offset from a 10 GHz carrier. The additive phase noise plot of the feedforward amplifier is demonstrated in Fig. 3.26(a) for multiple carrier frequencies in class A operation mode and the amplifier could achieve lower than -155 dBc/Hz at 10 kHz offset from 9.5 GHz. The additive phase noise of the feedforward amplifier improves significantly while biased in class B/C and reaches -160 and -156 dBc/Hz while the large signal gain drops to 2 and 5.5 dB respectively as plotted in Fig. 3.26(b).

The comparison of additive phase noise of the core and feedforward amplifier is plotted in Fig. 3.27(a) for 10 GHz carrier frequency. The feedforward amplifier demonstrates more than 4 dB phase noise reduction in small signal regions while biased in class A operation mode. Furthermore,

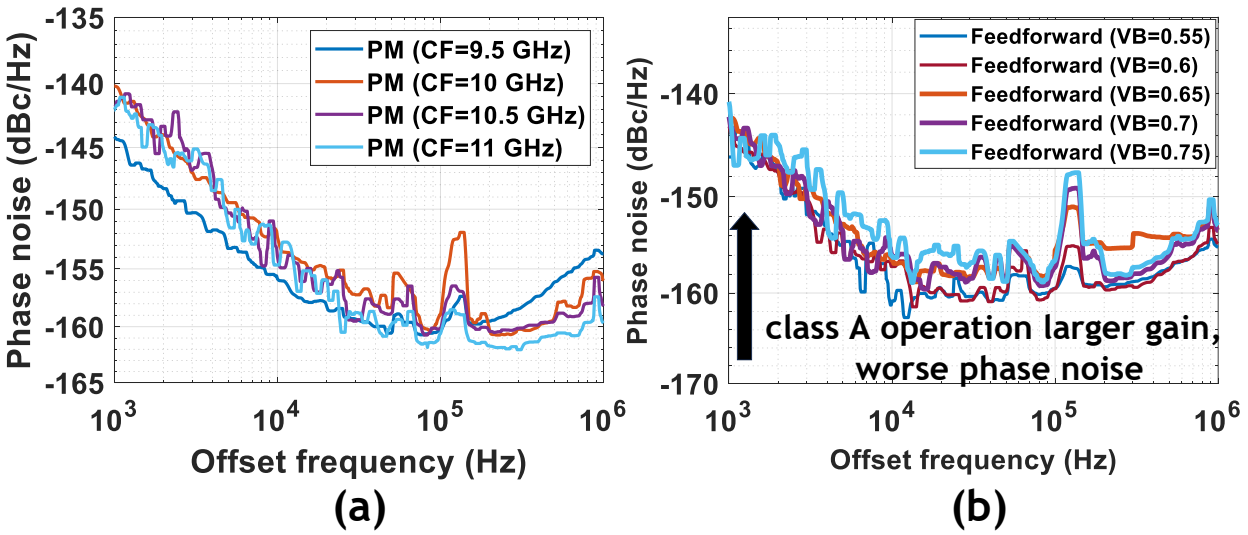


Figure 3.26: (a) Additive phase noise of amplifier at different carrier frequencies (Pin=0 dBm). (b) Additive phase noise of amplifier in class B/C operation mode (CF=10 GHz).

the additive phase noise of both the feedforward and core amplifier is graphed in Fig. 3.27(b) for 10 kHz offset versus input power at various carrier frequencies, and the feedforward amplifier attains a maximum of 6 and 7.5 dB phase noise reduction at 9.5 GHz and 10.5 GHz respectively.

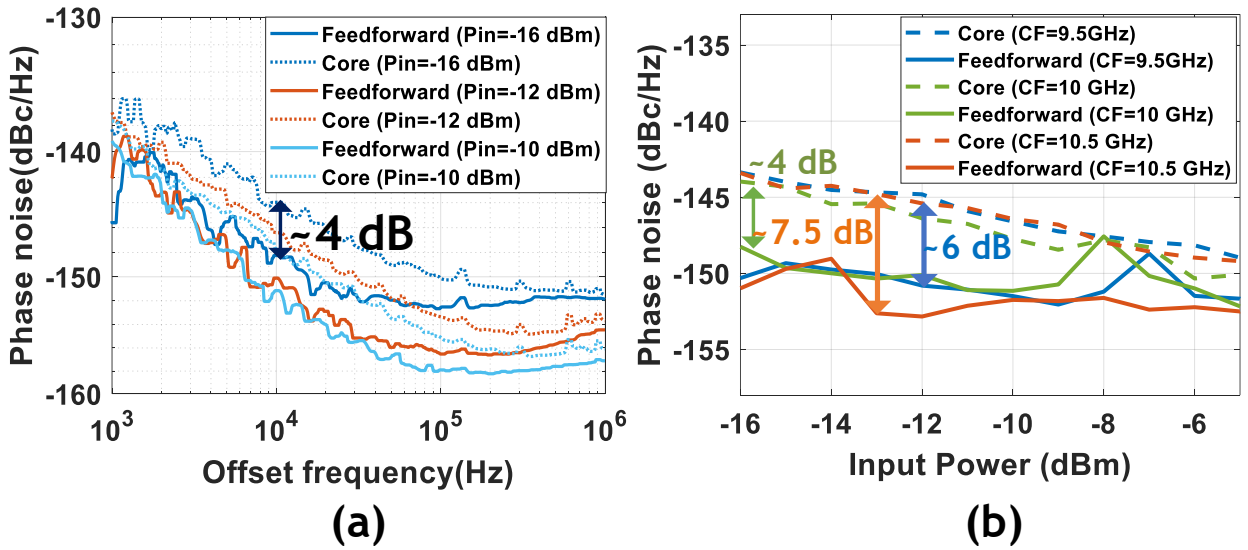


Figure 3.27: (a) The feedforward and core amplifier additive phase noise for different input powers (CF=10 GHz). (b) The feedforward and core amplifier additive phase noise versus input power at 10 kHz offset.

The comparison of the fabricated feedforward amplifier with commercially available low noise amplifier measured in [44, 46] is presented in the Table. 3.3. The new proposed noise-canceling scheme demonstrates better or the same phase noise performance and 1_{dB} compression point while exhibiting a significant decrease in DC power consumption and the die photo of the fabricated amplifier is graphed in Fig. 3.28.

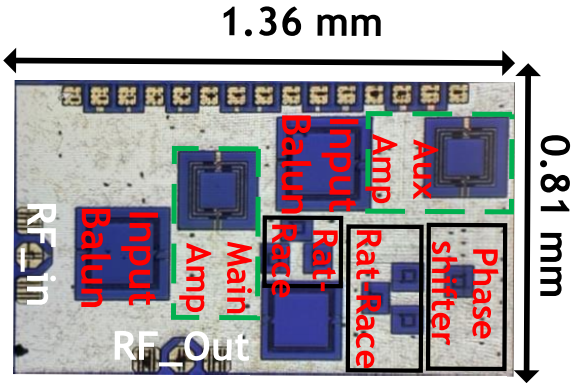


Figure 3.28: Die photo of designed feedforward amplifier.

Table 3.3: Table of comparison of Feedforward amplifeir

Amplifier	AML812PNB1901,Ref [46]	AML412L2001, Ref [46]	AML612L2201, Ref [46]	HMCC-5618, Ref [44]	This Work
BW_3dB (GHz)	8-12	4-12	6-12	6-20$^{\$}$	**8.1-12.5**
P_{1dB} (dBm)	17	10	10	18$^{\$}$	**16.1**
Peak S_{21} (dB)	22	20	22	14$^{\$}$	**15.9**
Phase noise at 10 kHz (dBc/Hz)	-158*	-151$^{€}$	-148$^{\#}$	-151*	**-155**
DC power consumption(mW)	6375	1500	1500	575$^{\$}$	**393**

$*$ Graphically estimated at 10 GHz. $ Based on device datasheet. # Graphically estimated at 9.2 GHz. €Graphically estimated at 9.192 GHz.

3.4.5 Conclusion

A low additive phase noise low power noise canceling feedforward amplifier is demonstrated in this work. By modifying the traditional scheme for the feedforward amplifier a new approach for carrier and noise suppression is proposed which decreases the physical size and form factor of the amplifier by reducing the number of couplers and phase shifters. The amplifier demonstrated a peak gain of 15.9 dB and a maximum of 7.5 dB phase noise reduction. This performance and form factor reduction facilitates on-chip implementation of the feedforward amplifier, for both phase and amplitude noise reduction.

3.5 Low Phase Noise Amplifier in SiGe BiCMOS Process

As discussed in Chapter 2, many modern technologies depend on the low-phase noise and exceptional timing stability of microwave signals. One effective method for generating low-phase noise microwave signals is through the down-conversion of ultra-stable optical references using a frequency comb. Toward the end of Chapter 2, a pathway to a chip-scale microwave frequency synthesizer was demonstrated, where SIL lasers replace fiber lasers, microcombs replace EO combs, and micro-FP cavities replace bulky cavities.

Furthermore, transitioning from COTS synthesizers to IC-based synthesizers makes the low-phase noise design of various components, such as amplifiers, increasingly critical. Amplifiers, being fundamental building blocks of IC synthesizers as highlighted in Fig. 3.29 and can potentially limit overall system performance.

After investigating multiple factors affecting low-phase noise amplification and strategies to minimize low-frequency to phase noise upconversion in amplifiers using the InP HBT process, applying these techniques to the SiGe BiCMOS process becomes even more critical. Moreover, both InP HBT and SiGe BiCMOS processes offer advantages over Si and GaAs technologies due to their high-frequency operation and low noise performance [92]. However, to make informed design

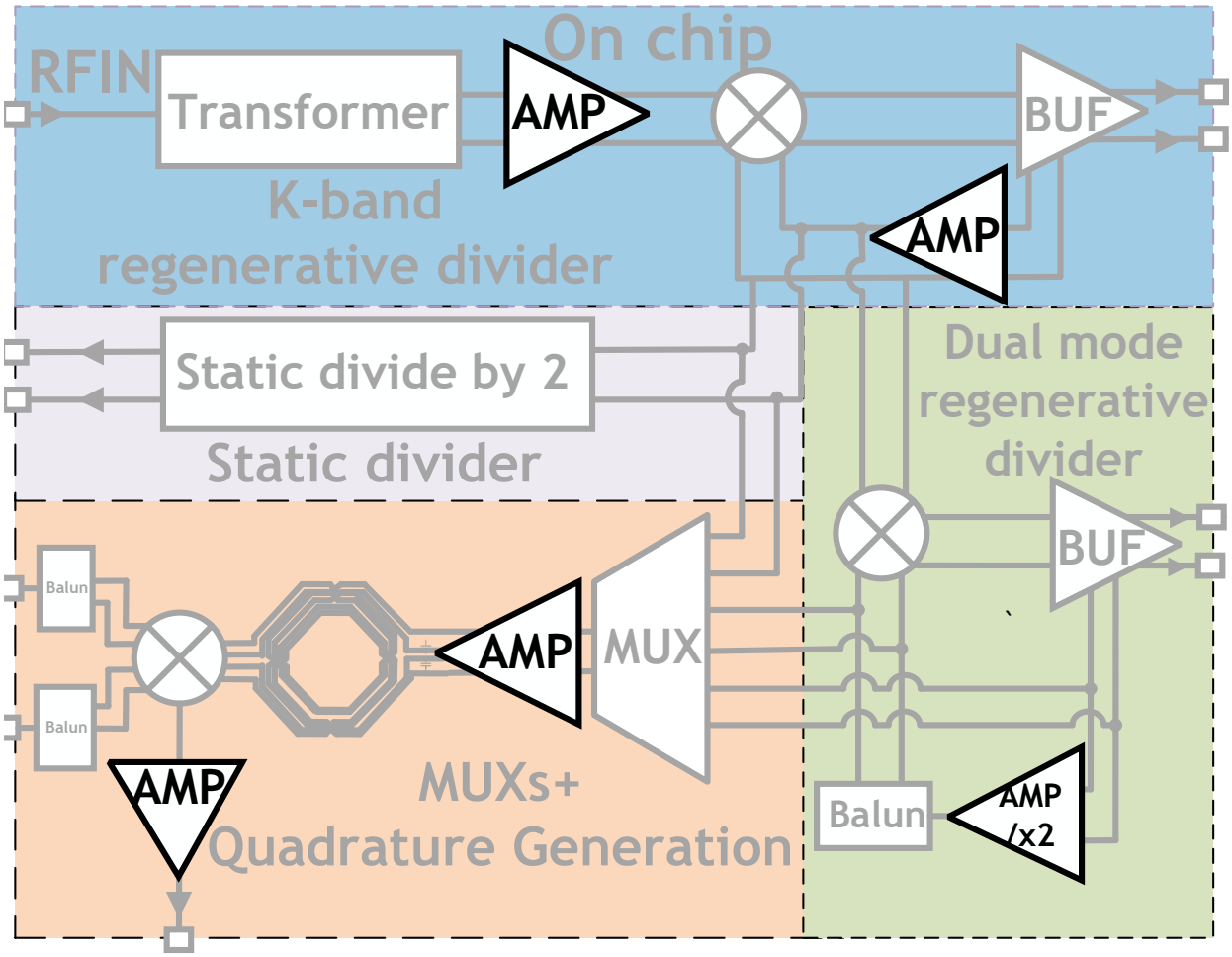


Figure 3.29: The critical role of low phase noise amplifier in synthesizer design.

choices and balance trade-offs between gain, additive phase noise, and power consumption, a thorough comparison of these technologies is necessary.

This subchapter explores the benefits of the SiGe BiCMOS process and compares low-phase noise amplifier designs in both processes to further reduce additive noise.

3.5.1 SiGe HBT Low Phase Noise Power Amplifier

SiGe HBT has a smaller bandgap compared to InP, leading to lower generated output power with the same number of transistors, however, due to high DC current gain and low base resistance, they

experience large benefits from low-frequency noise performance and power consumption [99]. In order to examine the additive phase noise of the SiGe PA especially due to nonlinearities of the transistor, a power-combined parallel amplifier is designed.

Four parallel transistors were used to improve the gain, deliverable output power, and 1 dB compression point and additive phase noise, without significantly degrading the noise figure (NF). The schematic and die photo of the fabricated amplifier are plotted in Fig. 3.30 and Fig. 3.31, respectively.

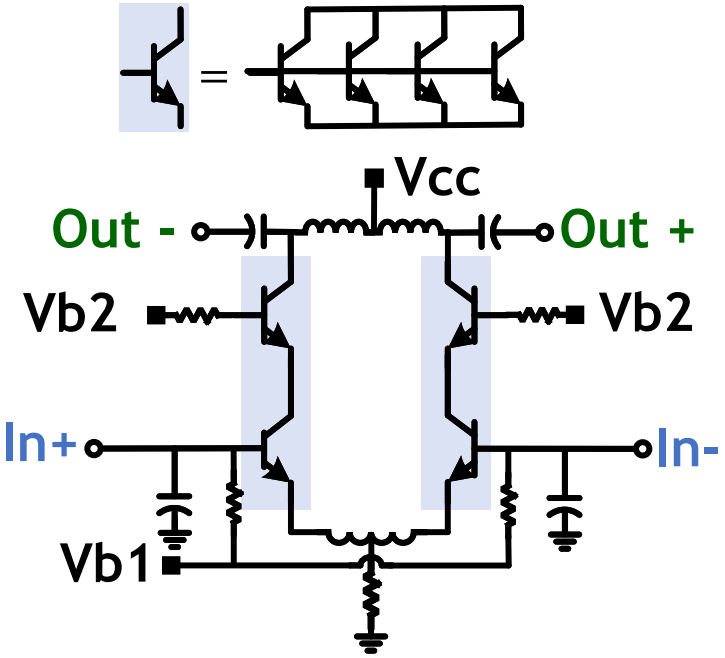


Figure 3.30: Schematic view of the Fabricated SiGe Amplifier.

In order to push the additive phase noise of the designed amplifier lower and take advantage of optical mode such as OFD, a differential design is preferable and utilized in the design to further minimize the phase noise added by the electrical amplifier and increase the common mode rejection with the cost of additional unbalanced to balanced transformation. As a result, a custom passive structure is deployed in the design to attain compatibility with a single output from a photodetector and minimize the achievable noise figure of the designed amplifier as plotted in Fig.3.32. In order

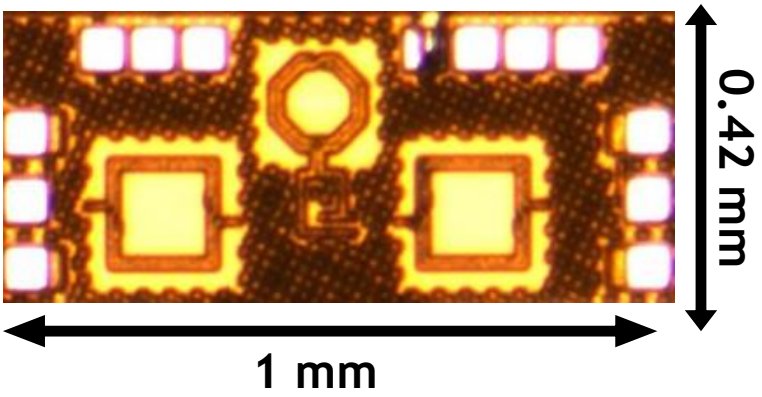


Figure 3.31: Die photo of the implemented SiGe Amplifier.

to increase the common mode noise rejection, a 5 Ω resistor is used, which further improves the stability of the circuit. The output impedance of the proposed amplifier goes through a balun which matches using load pull simulation to enhance the deliverable output power.

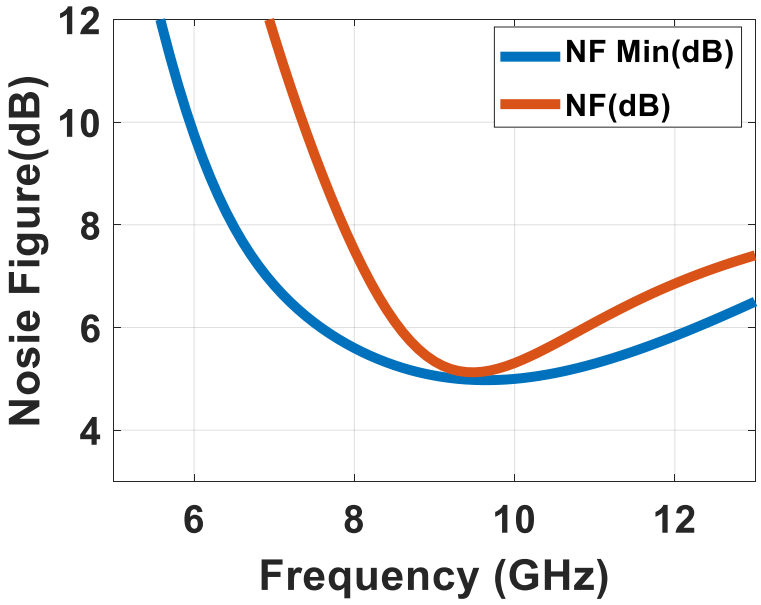


Figure 3.32: Simulated minimum and actual noise figure of the amplifier.

3.5.2 Measurement Results

The low-phase noise amplifier was fabricated in the Global Foundry SiGe BiCMOS process and is biased in the linear region to achieve the maximum available gain, with DC collector currents and voltages set to 9 mA and 2 V, respectively. The large signal measurement result of the fabricated amplifier is plotted in Fig. 3.33 and the amplifier can deliver more than 5 dBm at 9 GHz frequency.

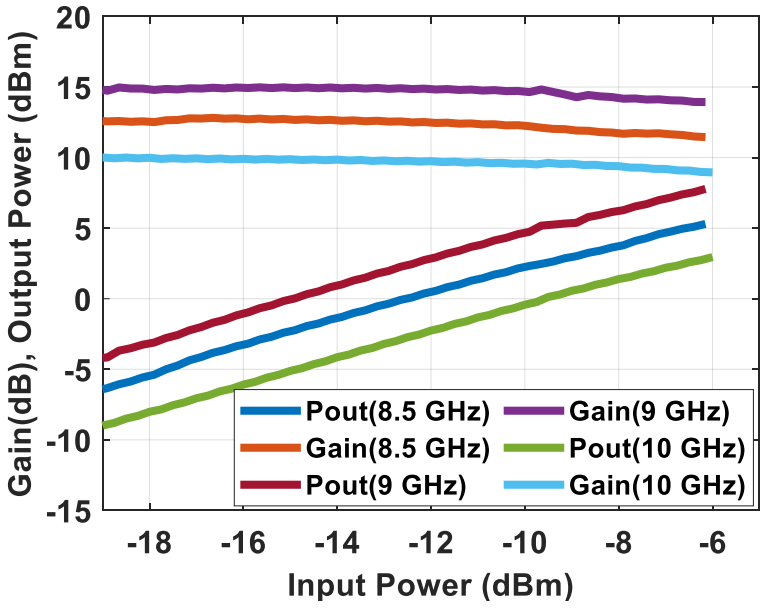


Figure 3.33: Large signal measurement results of BiCMOS amplifier.

Additive phase noise measurements are performed using Rohde and Schwarz FSWP phase noise analyzer and the measurement results are demonstrated in Fig. 3.34(a) for a 10 GHz carrier while the amplifier could achieve lower than -157 dBc/Hz at 10 KHz offset. Amplifier exhibits less than 7 dB variation in additive phase noise while biased in the class A operation as plotted in Fig. 3.34(b) for different carrier frequencies. The designed and implemented amplifier surpasses the performance of state-of-the-art low phase noise amplifiers in [86] achieving significant reduction in DC power consumption.

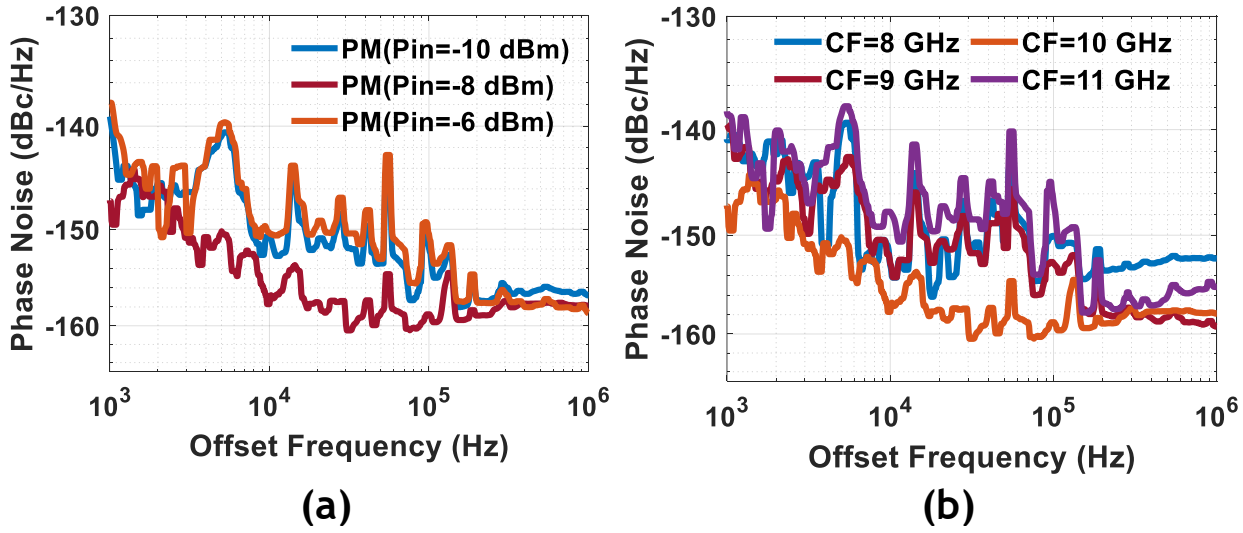


Figure 3.34: (a) Phase noise measurement results of the low phase noise amplifier (CF=10 GHz). (b) Amplifier phase noise measurement results versus different center frequencies.

3.6 Conclusion

This chapter explores a key component in low-phase noise microwave signal generation using electro-optical methods and presents multiple approaches to minimizing the additive phase noise of amplifiers across different processes. A noise canceling amplifier was proposed and measured to push the boundaries of low-phase noise amplification even further. Additionally, a comparative analysis of output power, phase noise, and DC power consumption across different processes was conducted.

The measurement result demonstrates InP amplifier offers higher gain and greater output power due to its larger bandgap and higher breakdown voltages. While InP amplifiers have the limits of low-phase noise amplification and demonstrated an effective approach for achieving it, they are outperformed by the SiGe BiCMOS process. This is primarily due to InP's higher base resistance, which directly contributes to thermal noise, increased generation-recombination noise affecting flicker noise, and lower DC current gain.

The presented result of SiGe amplifier combined with the proposed phase noise reduction methods,

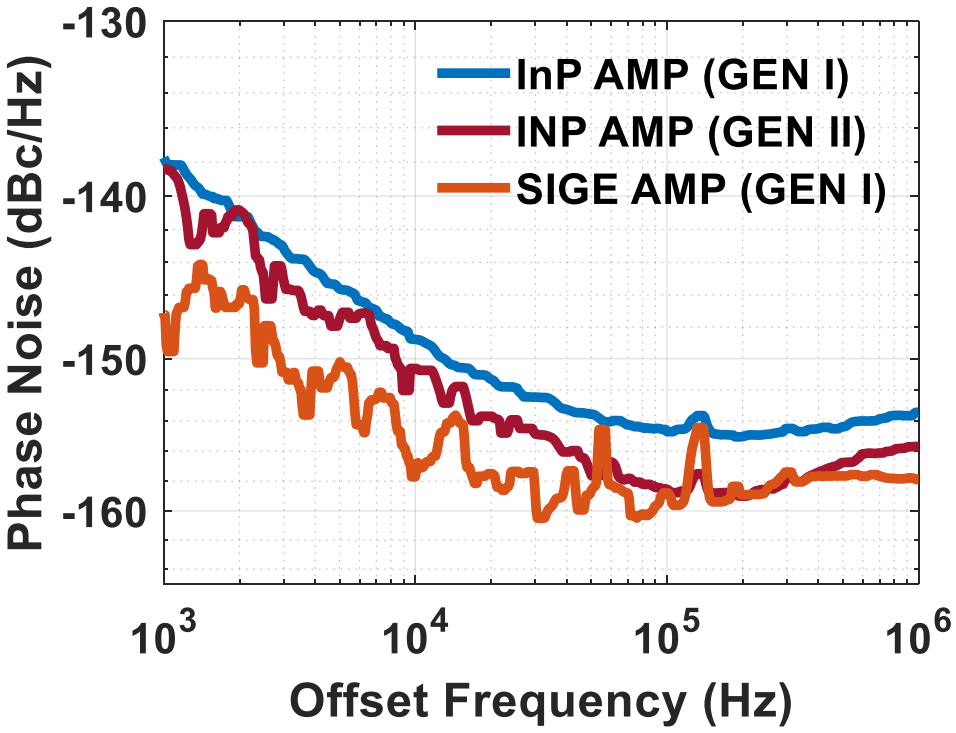


Figure 3.35: Low phase noise amplifier comparisons between different generations.

is expected to support the development of electronic-photonic integrated circuits for chip-scale OFDs capable of generating low-noise microwave signals and provide a pathway for chip-scale hybrid synthesizers.

The summary of low-phase-noise amplifiers across different generations is illustrated in Fig. 3.35.

3.7 Contributions

This work was done in collaboration with Samin Hanifi. I would like to thank her for her contribution:

- For the design and layout of passive baluns in both InP and SiGe amplifiers, assist with measurement setup and with helpful technical discussion.

3.7.1 Publication

- **P. Shirmohammadi**, S.M. Bowers "A Wideband 2.18-13.51 GHz Ultra-Low Additive Phase Noise Power Amplifier in InP 250nm HBT" In *2024 IEEE Radio and Wireless Symposium (RWS) (pp. 16-18). IEEE*.

- **P. Shirmohammadi**, S. Hanifi, S.M. Bowers "An X-Band Phase Noise Canceling Feedforward Amplifier in InP 250 nm HBT Process" In *2024 IEEE/MTT-S International Microwave Symposium-IMS 2024 (pp. 682-685). IEEE*.

- **P. Shirmohammadi**, S.M. Bowers "Reduction of Additive Phase Noise of Electrical Amplifiers for Electronic-Photonic Low Noise Signal Generation" In *CLEO: Science and Innovations (pp. JTu2A-113). Optica Publishing Group*.

Chapter 4

Ultra Low Phase Noise Microwave Frequency Dividers

4.1 Introduction, Motivation and Prior Art

As mentioned earlier in Chapter 2, an effective approach to extending the bandwidth of a DDS-based synthesizer is to develop multiple stages of frequency dividers. These dividers divide down the high-frequency output generated through optical methods, which can then be mixed with the DDS output to achieve the desired frequency range.

Multiple approaches have been introduced for high-performance frequency dividers such as static dividers, and regenerative dividers [100]. Static D-latch-based frequency dividers are known for their low input power requirements and ability to operate across a broad range of frequencies. However, their phase noise performance remains one of their primary limitations. On the other hand, a regenerative divider offers low additive phase noise performance, with the cost of higher input power and limited bandwidth [101].

This chapter introduces an integrated regenerative divide by two designed to improve the traditional regenerative divider's sensitivity and reduce startup issues while keeping the additive phase noise

low. Given the amplifier's and buffer's critical role in the divider's additive phase noise, integrated low-phase-noise amplifiers and buffers are designed and implemented in the divider. Integrating all components on a single die and utilizing a passive mixer instead of a conventional Gilbert cell mixer reduces the form factor and minimizes the divider's additive phase noise. Additionally, this chapter explores the impact of various biasing points on the divider's phase noise performance, demonstrating the effectiveness of proper biasing in achieving optimal phase noise.

Finally this chapter is dedicated to investigating methods to enhance the frequency range of the regenerative divider while simultaneously minimizing its additive phase noise and reducing both the form factor and power consumption of these dividers, since they play a key role in determining the performance of the synthesizer, and can also act as a limiting factor in terms of phase noise. as shown in Fig.4.1.

The measurement of the fabricated divider indicates more than 12 dB fundamental rejection and more than -10 dBm output power across various frequencies.

4.2 Regenerative Divider Operation

Fig. 4.2(a) illustrates the traditional block diagram of regenerative dividers. The conventional design of regenerative dividers consists of four main components: an amplifier, a filter, a power splitter, and a mixer. In a conventional regenerative divider, the output of the mixer is fed back to the LO port of the mixer after being filtered and amplified. Assuming the amplifier's nonlinearity is negligible and the frequency of LO port and IF port are the same ($f_{IF} = f_{LO}$), the mixer output consists of both ($f_{IF} = \frac{f_{RF}}{2}$) and ($f_{IF} = \frac{3f_{RF}}{2}$) frequencies. However, by proper bandwidth engineering of each component and implementing appropriate filter along the chain, only $\frac{f_{RF}}{2}$ passes through the loop, resulting in a divide by two at the output [102–104]. A power splitter is typically used at the output in traditional regenerative divider designs. The loss associated with the passive structure may prevent the LO port of the mixer from being properly saturated and prevent the proper division process. To mitigate start-up challenges and minimize power losses associated

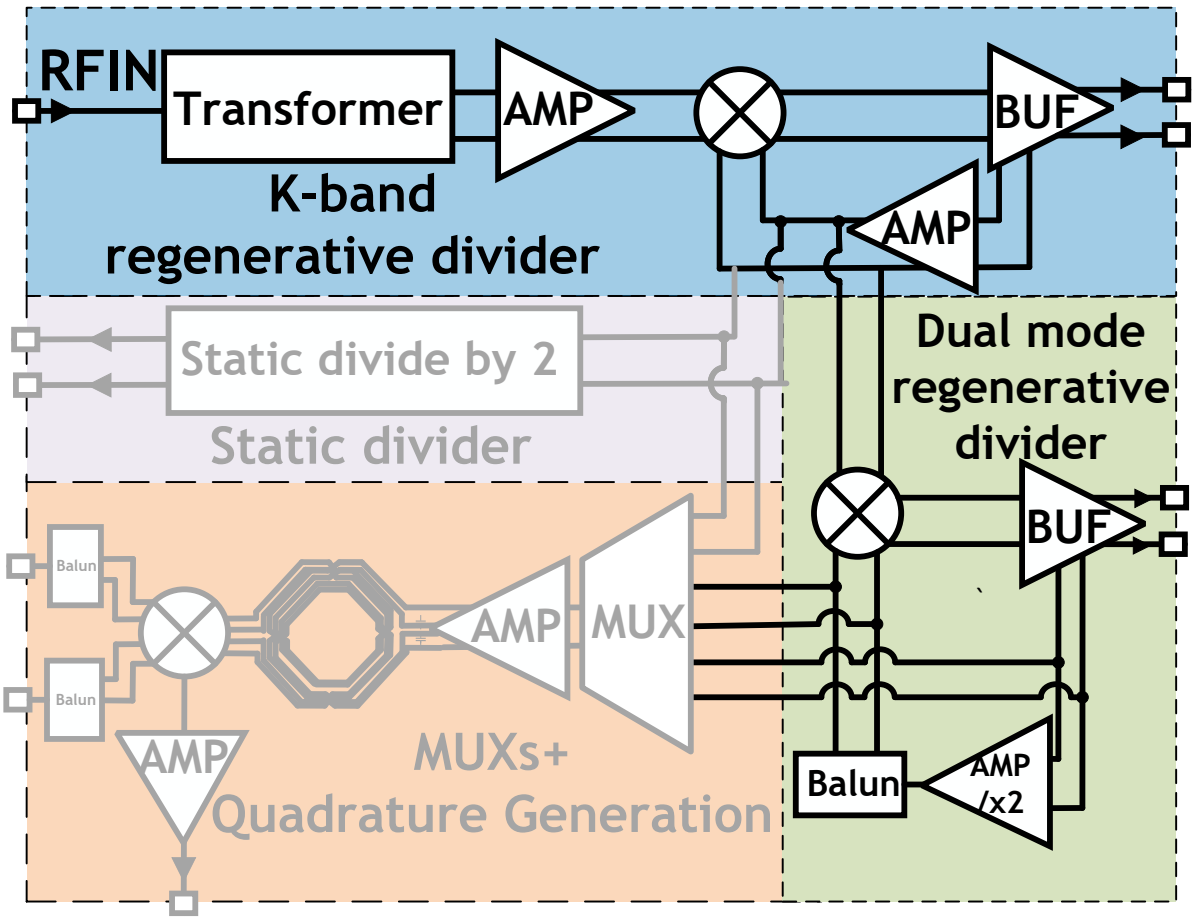


Figure 4.1: Impact of regenerative dividers in BiCMOS synthesizer.

with power splitting while maintaining low-phase noise performance, an active high-impedance buffer is implemented at the output instead of the conventional power splitter, as shown in Fig. 4.2(b). The high-impedance buffer is chosen to minimize the voltage drop across the amplifier, facilitating an easier startup condition.

In the conventional regenerative divider, the amplifier is implemented in the forward path before the splitter; in the proposed design, the amplifier is relocated from the forward path to the feedback path to reduce its phase noise contribution while still delivering sufficient power for LO saturation.In addition, a phase shifter is integrated into the feedback loop to improve phase noise performance further, allowing for phase fine-tuning and ultra-low phase noise operation.

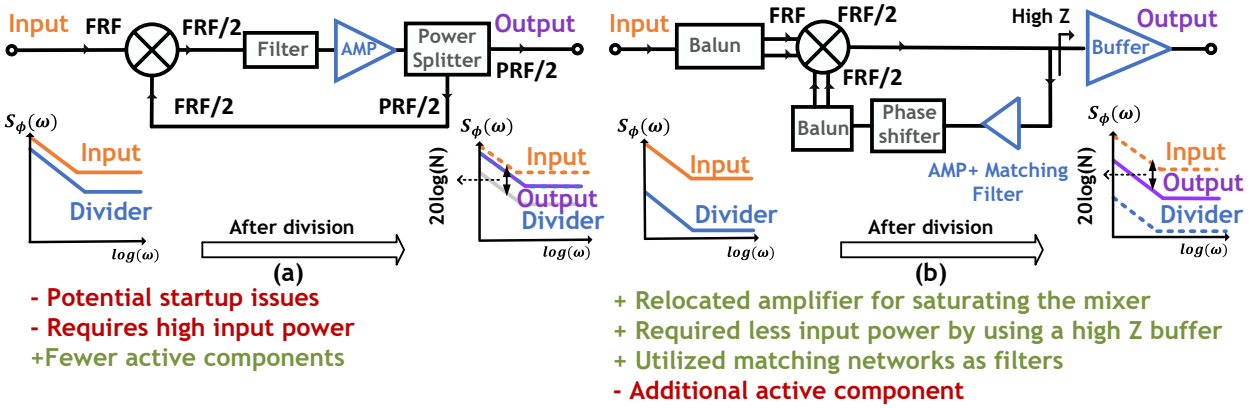


Figure 4.2: (a) Traditional regenerative divider's block diagram utilizing amplifier in the forward path in the combination of power splitter at the output. (b) The block diagram of the proposed regenerative divider uses a high-impedance buffer instead of a power splitter. Additionally, an amplifier is implemented into the feedback path to ensure sufficient power is delivered to the mixer's LO port. The $20log(2)$ reduction in phase noise will be observed if the additive phase noise of the divider is below the expected phase noise.

4.3 Low-Additive Phase Noise Regenerative Divider by 2

4.3.1 Amplifier Design

One of the critical components in the entire system chain is the amplifier in the feedback path. The performance of the regenerative divider primarily depends on the saturation of the mixer's LO port. Additionally, the amplifier phase noise is one of the dominant noise sources that contributes to the additive phase noise of the regenerative divider [101]. Taking all these factors into account, the amplifier in the chain is not only required to cover a wide range of operations, but it also needs to exhibit very low-additive phase noise while being capable of saturating the LO port of the mixer across a broad range of frequencies [44, 46].

The low phase noise InP amplifier described in Chapter 2 is used in the integrated regenerative divider which can provide more than 18.2 dBm saturated output power, peak S_{21} of 18.1 dB over 11 GHz bandwidth.

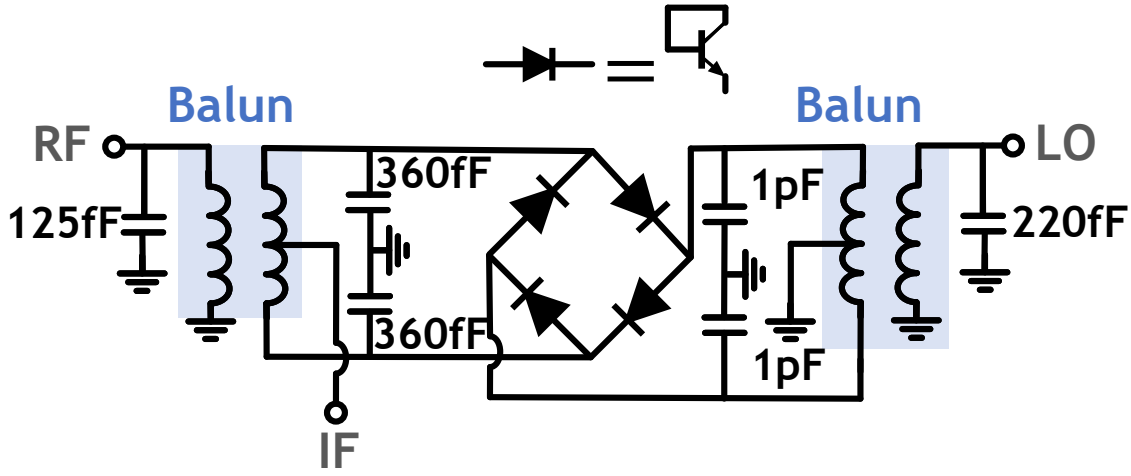


Figure 4.3: Passive double-balanced mixer schematic with custom passive baluns. A passive structure has been chosen over an active one for lower noise with the cost of lower conversion gain.

4.3.2 Mixer Design

Saturating the mixer's LO port is crucial for the regenerative divider's operation. The mixer has been designed with a low LO power requirement to minimize start-up issues and lower the required input power. A passive double-balanced diode ring mixer is chosen over the traditional Gilbert cell mixer to minimize the up conversion 1/f noise at the cost of lower conversion gain. However, due to the single-ended nature of the RF and LO ports, unbalanced to balanced transformation is required. A passive balun structure is used for the LO and RF ports to mitigate the up-conversion of flicker noise in an active device and improve the balun's power handling capabilities at the cost of lower conversion gain compared to active baluns and the schematic of the mixer is shown in Fig.4.3.

The large signal simulation results of the mixer, along with its RF and LO baluns, are demonstrated in Fig. 4.4(a). In conjunction with baluns, the mixer simulation achieves a conversion gain of less than -8.5 dB and more than -2.5 dBm output power at RF and LO frequencies of 14 GHz and 7.5 GHz, respectively. Furthermore, the effect of different LO powers on conversion gain is illustrated in Fig. 4.4(b).

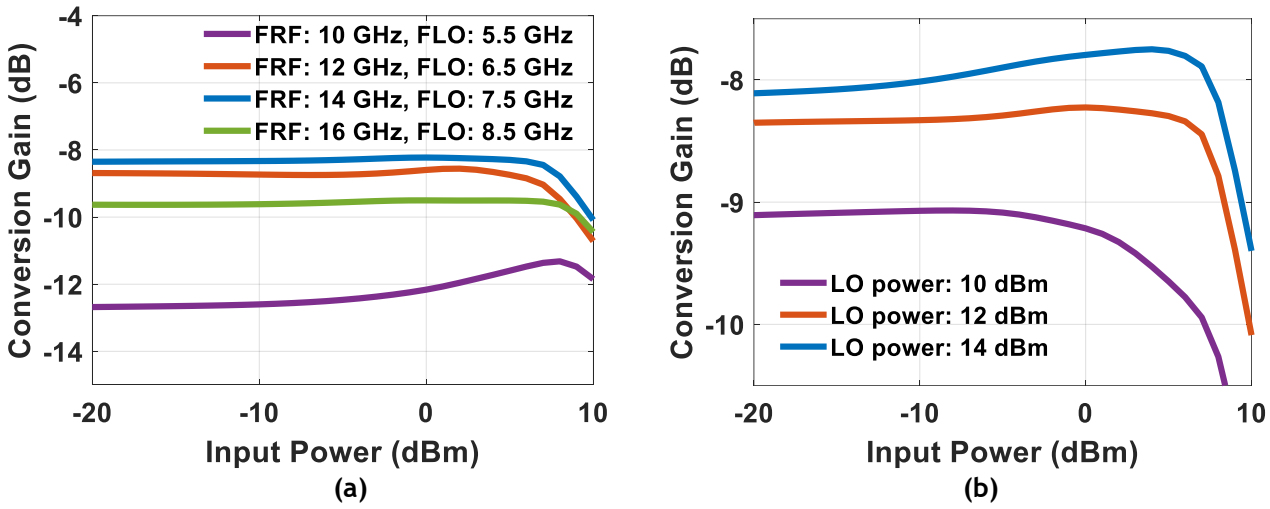


Figure 4.4: (a) Conversion gain of the mixer across various RF frequencies (PLO=12 dBm, FLO=$\frac{FRF}{2}$+0.5 GHz) with the highest conversion gain occurs at 14 GHz RF frequency, which aligns with the measured data. (b) conversion gain versus input power for different LO powers when FRF=14 GHz and FLO=7.5 GHz.

4.3.3 Buffer Design

The conventional regenerative divider employs a power splitter following the amplifier to monitor the output and provide feedback for LO port saturation [101]. However, using a power splitter reduces the output power by half, which may lead to start-up issues due to insufficient power being delivered to the LO port and prevent from proper dividing. Additionally, it may increase the required input power to meet the necessary gain conditions for stable operation, resulting in lower sensitivity which traditional regenerative dividers usually suffers from.

A high input impedance buffer is introduced into the forward path to mitigate risks associated with LO saturation and start-up conditions while minimizing the input power required for LO saturation. The buffer is designed to have a large input impedance to minimize the voltage swing drop at the LO port of the mixer while tolerating a large swing at the input port and still providing the necessary drive power for external 50 Ω loads, such as a signal analyzer or oscilloscope.

4.3.4 Phase Shifter Design

Achieving accurate phase control in the loop is essential to satisfy the loop's gain and phase requirements, especially for proper frequency division across a wide operating range. An active phase shifter, such as the vector sum phase shifter, offers advantages such as a full 360-degree phase shift and superior phase and gain resolution, which can be crucial for systems with low phase noise requirements [105].

Due to the active nature of the vector sum phase shifter, its additive phase noise may affect the low-phase noise design and can be a limiting factor.

To minimize the need for a full 360-degree phase shifter, a full EM simulation of the on-chip transmission line is performed to ensure the phase condition is met. However, for improved control over the phase, and enhanced phase noise performance particularly by minimizing the noise contribution from $\frac{3f_0}{2}$ at $\frac{f_0}{2}$ a passive loaded transmission line is designed and implemented, as illustrated in Fig. 4.5(a).

The simulation results of insertion loss versus phase shift, normalized to the phase shifter's off state, are shown in Fig 4.5(b). When the phase shifter is off, insertion loss is 2 dB, and the loaded transmission line provides an 11.7-degree phase shift. Adding the phase shift helps adjust the phase, but it comes at the cost of introducing additional loss. This can impact sensitivity, potentially preventing division when the phase shift increases and requires higher input power to achieve proper division.

4.3.5 Measurement Results

The proposed divider is designed in the Teledyne InP 250nm HBT process with V_{CC} of amplifier and buffer set to 3.2 V and 2.6 V accordingly with quiescent collector currents of 17 mA and 0.2 mA when the amplifier and buffers are biased for the best phase noise performance, respectively. In order to measure the sensitivity and spectrum of the frequency divider a Keysight E8257D signal

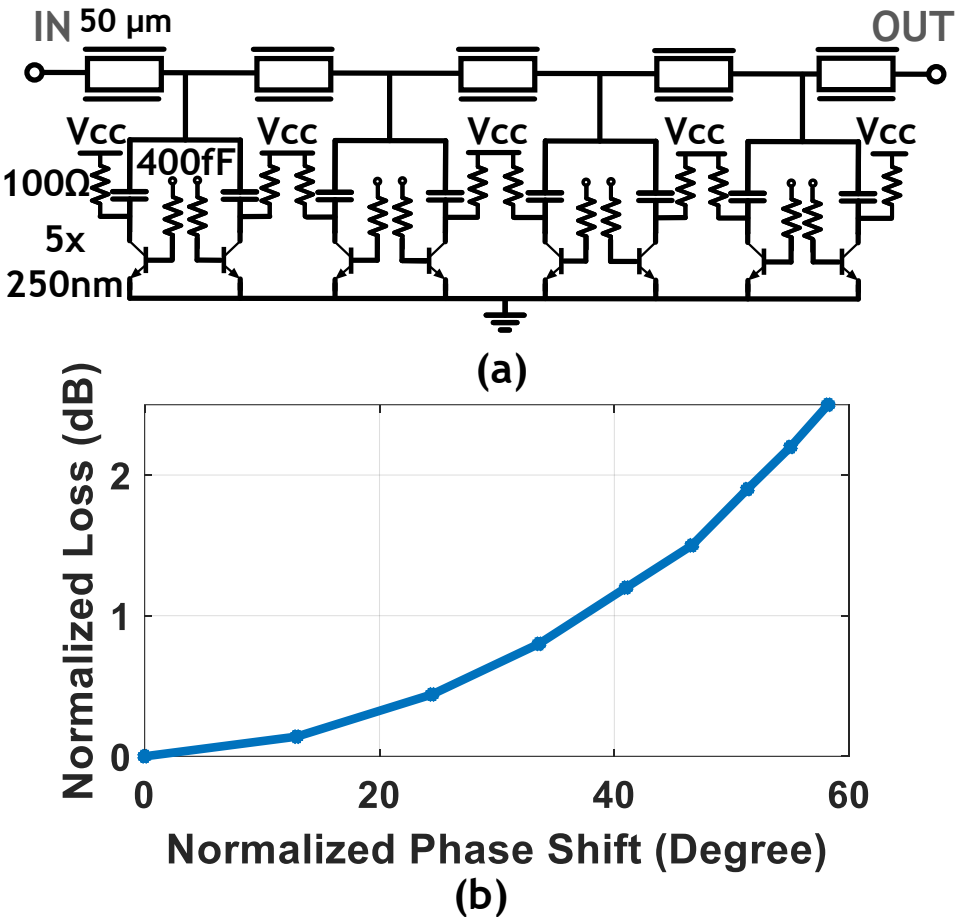


Figure 4.5: (a) The loaded transmission line phase shifter schematic with a capacitor bank (b) Simulation results of loss versus phase shift normalized when all switching transistors are in the off state at 7 GHz input frequency. When the phase shifter is off, the loss and phase shifts are 2 dB and 11.7 degrees, respectively.

generator is used. The sensitivity of the divider is plotted in Fig. 4.6(a), which shows the broad range of operation from 9-22 GHz, with the minimum input power required at 14 GHz. This frequency corresponds to the best RF and LO baluns matching conditions. Fig. 4.6 (b) shows the frequency spectrum of the divider for input frequencies of 14, 16, 18, and 20 GHz, demonstrating a consistent suppression of more than 12 dB of the fundamental tone across the plotted frequency range.

The die photograph of the fabricated divider and absolute phase noise measurement setup are shown in Fig. 4.7(a) and (b), respectively, where a phase noise analyzer (PNA) is used to measure

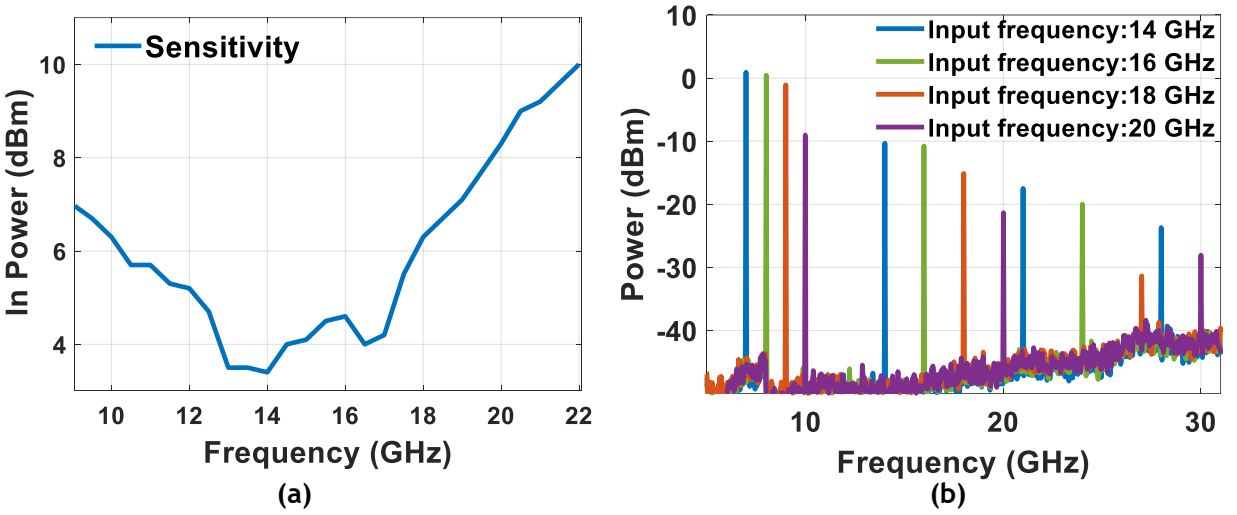


Figure 4.6: (a) The minimum input power across different input frequencies, showing that the best sensitivity occurs at 14 GHz due to the optimized matching of the EM structures, mixer, and amplifier. (b) Output spectrum at various frequencies, demonstrating over 12 dB fundamental rejection throughout the operating range.

phase noise.The PNA provides the input signal and simultaneously measures the divider's output. The absolute phase noise of dividers is around -135 and -134 dBc/Hz at 10 kHz offset from 8 and 9 GHz output frequencies as shown in Fig. 4.8(a) and (b), respectively. The output phase noise has almost 6 dB phase noise reduction from the input signal aligning with $20 * log(N)$ where N is the division ratio. The 6 dB reduction in phase noise after division indicates that the additive phase noise of the divider is lower than the measured output phase noise. The additive phase noise of the divider will be further discussed in the following section. To measure the additive phase noise of any frequency-converting component, at least two identical components are required. Therefore, two dividers need to operate simultaneously with the same input signal to measure the additive phase noise of dividers. By comparing the output signals of these two dividers, the common phase noise from the input source is canceled out, and the measured phase noise is only divider additive phase noise isolated from noise generated by the input source. The keysight N5183B, followed by a power splitter, provides the same input signal for the input of the dividers, and DC supplies are shared between the two dividers. The output from the first divider is split into two signals, and both outputs from the first divider and the output of the second divider are sent to the PNA to measure the additive phase noise as illustrated in Fig. 4.9.

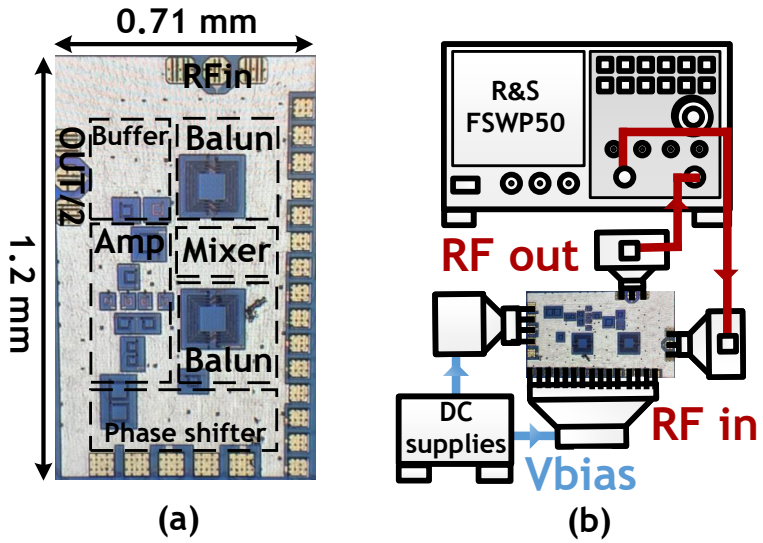


Figure 4.7: (a) Die photograph of fabricated InP 250nm regenerative divider (b) Absolute phase noise measurement setup where phase noise analyzer provided the input signal and measured the output phase noise.

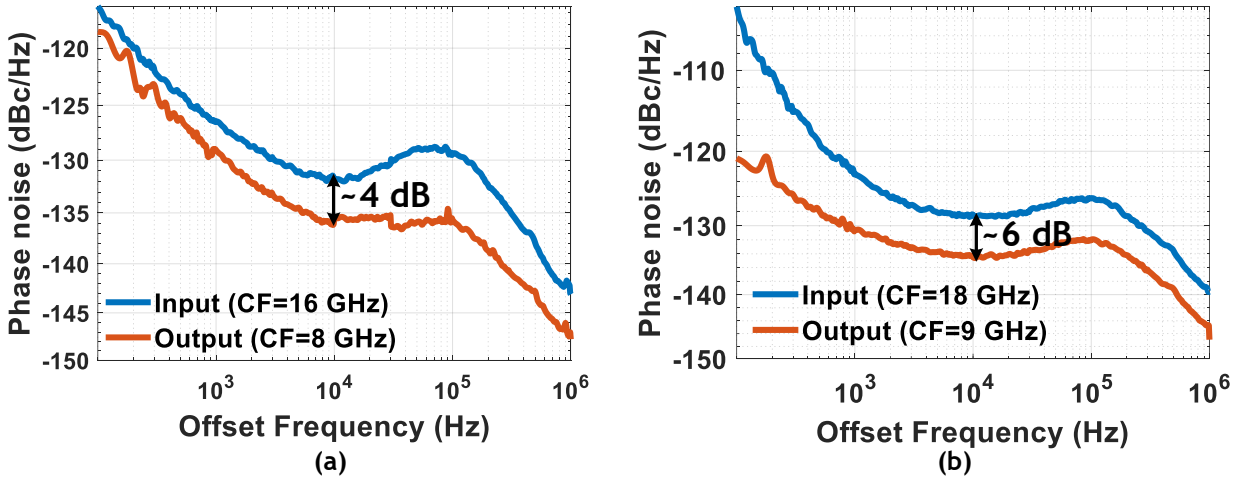


Figure 4.8: Absolute phase noise measurement results for (a) 8 GHz output frequency (b) 9 GHz output frequency where 6 dB phase noise reduction pattern shows additive phase noise of divider is below the phase noise of source.

Fig. 4.10(a) shows the additive phase noise of the 14 GHz input frequency when the V_{BEAmp}, V_{BEBuff} and input power is set to 0.85 V, 0.625 V, and 8.5 dBm respectively. Fig. 4.10(b) shows the additive phase noise at 15 GHz input frequency when the V_{BEAmp}, V_{BEBuff} and input power

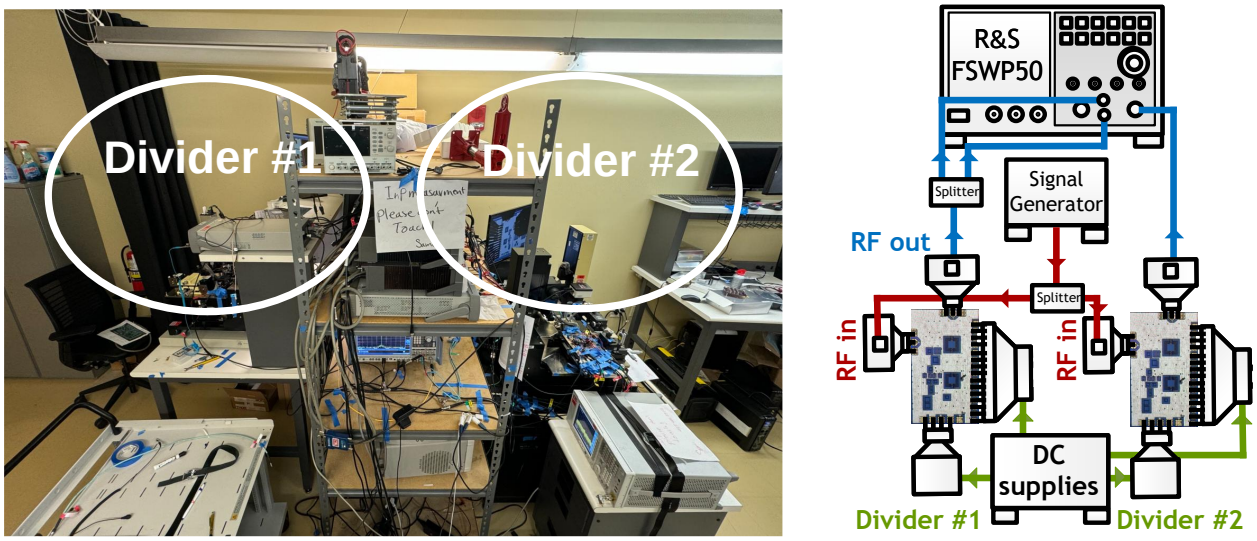


Figure 4.9: The additive phase noise measurement setup, with two dividers operating simultaneously with the same RF input and DC supplies.

are set to 0.85 V, 0.725 V, and 8 dBm respectively. The divider's additive phase noise at 7 GHz and 7.5 GHz output frequencies are around -163 and -157 dBc/Hz at 10 kHz offset, respectively.

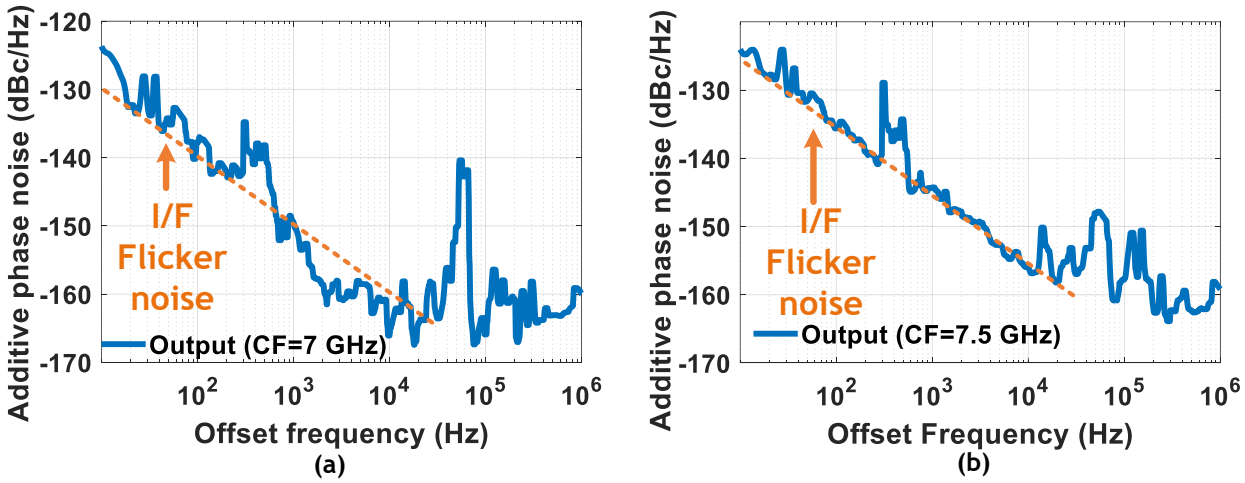


Figure 4.10: Additive phase noise measurement (a) at 7 GHz output frequency (optimum matching of passive structures, mixer, and amplifier) (b) at 7.5 GHz output frequency, emphasizing the 1/f noise (flicker noise) performance.

The divider's additive phase noise highly depends on the amplifier and buffer's additive phase

noise. By changing the amplifier's bias and buffer, the divider's overall additive phase noise will also change. In the following section, the effect of different biases for the amplifier, buffer, and phase shifters on the divider's overall additive phase noise is investigated.

Fig. 4.11(a) illustrates the impact of buffer's bias on additive phase noise at 10 kHz offset frequency when V_{BEAmp} is fixed to 0.85 V, and the input power is swept from 6 to 10 dBm at 7 GHz output frequency. As shown in the Figure, the additive phase noise of the entire divider can vary up to 29 dB depending on the input power level and buffer bias. It can shift from -134 dBc/Hz (V_{BEBuff}: 0.575 V, input power: 6 dBm) to -163 dBc/Hz (V_{BEBuff}: 0.625 V, input power: 8.5 dBm). Additionally, for a fixed buffer bias point, the variation in phase noise can be as high as 28 dB (at V_{BEBuff}: 0.575 V) or as low as a few dB (at V_{BEBuff}: 0.75 V).

To minimize the impact of biasing and phase noise variation caused by power sweeps, an optimal biasing point was identified from the minimum phase noise values in Fig. 4.11(a). By controlling the buffer's bias voltage at this optimal point, additive phase noise lower than -158 dBc/Hz can be achieved across the entire input power, as shown in Fig. 4.11(a) and (b).

To realize the relationship between the input power and buffer bias, an exponential fit between input power and buffer bias was applied to the optimal phase noise points in Fig. 4.11(a), with V_{BEAmp} fixed at 0.85 V. Eq. 4.1 is described the relationship between input power and buffer's bias in order to achieve the minimum phase noise.

$$V_{BEBuff(P_{RF}(dBm))} = Ae^{(BP_{RF}(dBm))} \tag{4.1}$$

4.3.6 Effect of Amplifier's Bias

The effect of the amplifier's bias is investigated in two scenarios when buffer bias is fixed at 0.6 and 0.7 V, as shown in Fig. 4.12(a) and (b), respectively. When the amplifier is biased at a lower voltage, the entire regenerative divider requires more input power to provide sufficient gain for saturating the LO of the mixer.Once the input power exceeds the level that required to achieve the best phase noise, the mixer operates in a nonlinear region, introducing additional noise into the

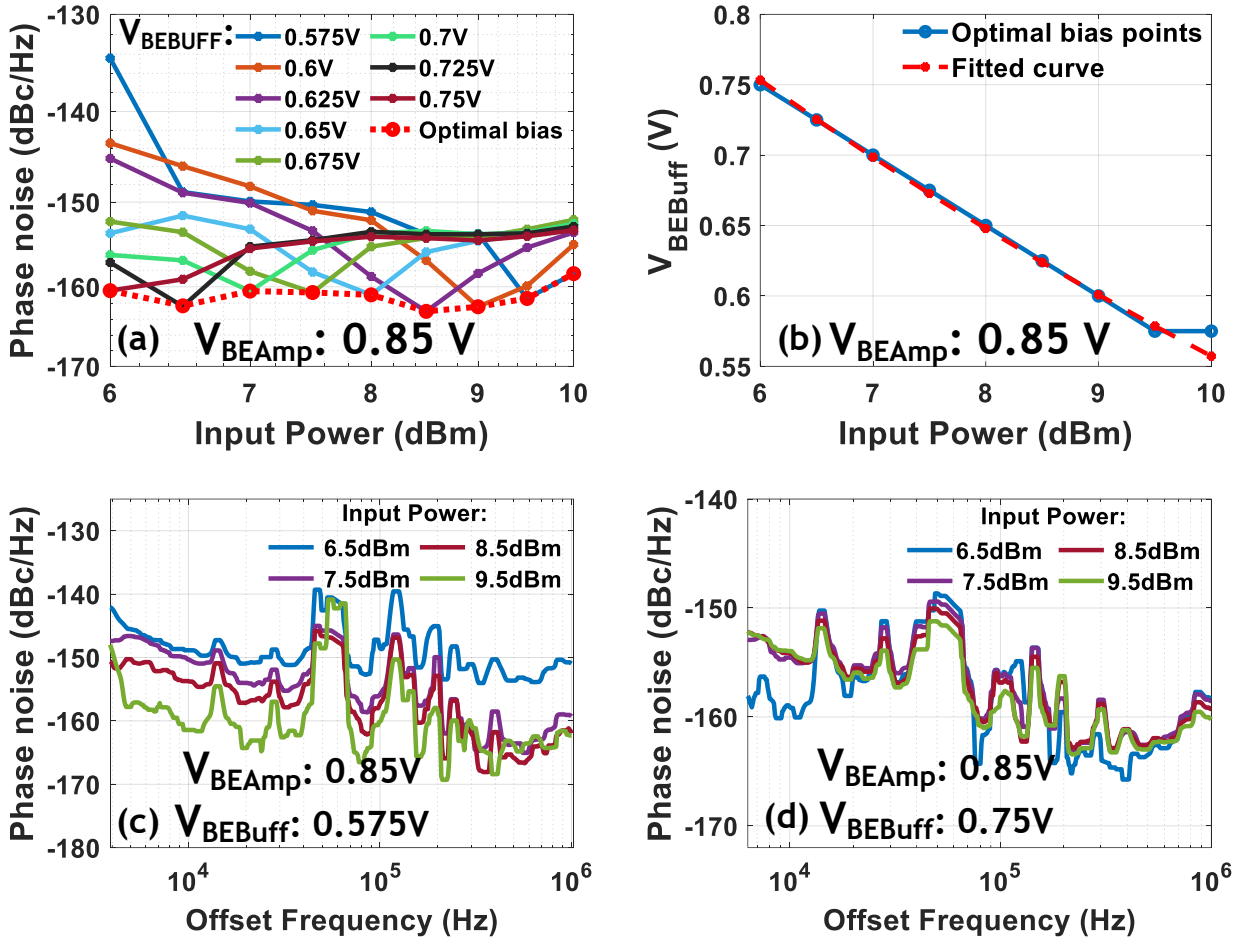


Figure 4.11: Additive phase noise at 14 GHz input frequency (a) versus input power at 10 kHz offset: To achieve the best phase noise at each given input power, applying an optimal bias point for the buffer is necessary. (b) optimal biases for buffer versus different input power for achieving minimum phase at 10 kHz offset (c) for different input power while V_{BEBuff} and V_{BEAmp} fix to 0.575 V and 0.85 V (d) for different input power while V_{BEBuff} and V_{BEAmp} set to 0.75 V and 0.85 V

system. In comparison to Fig. 4.12(a), the buffer bias is increased by 0.1 V in Fig. 4.12(b), which effectively demonstrates that lower input power is required to reach the optimal biasing point for phase noise.

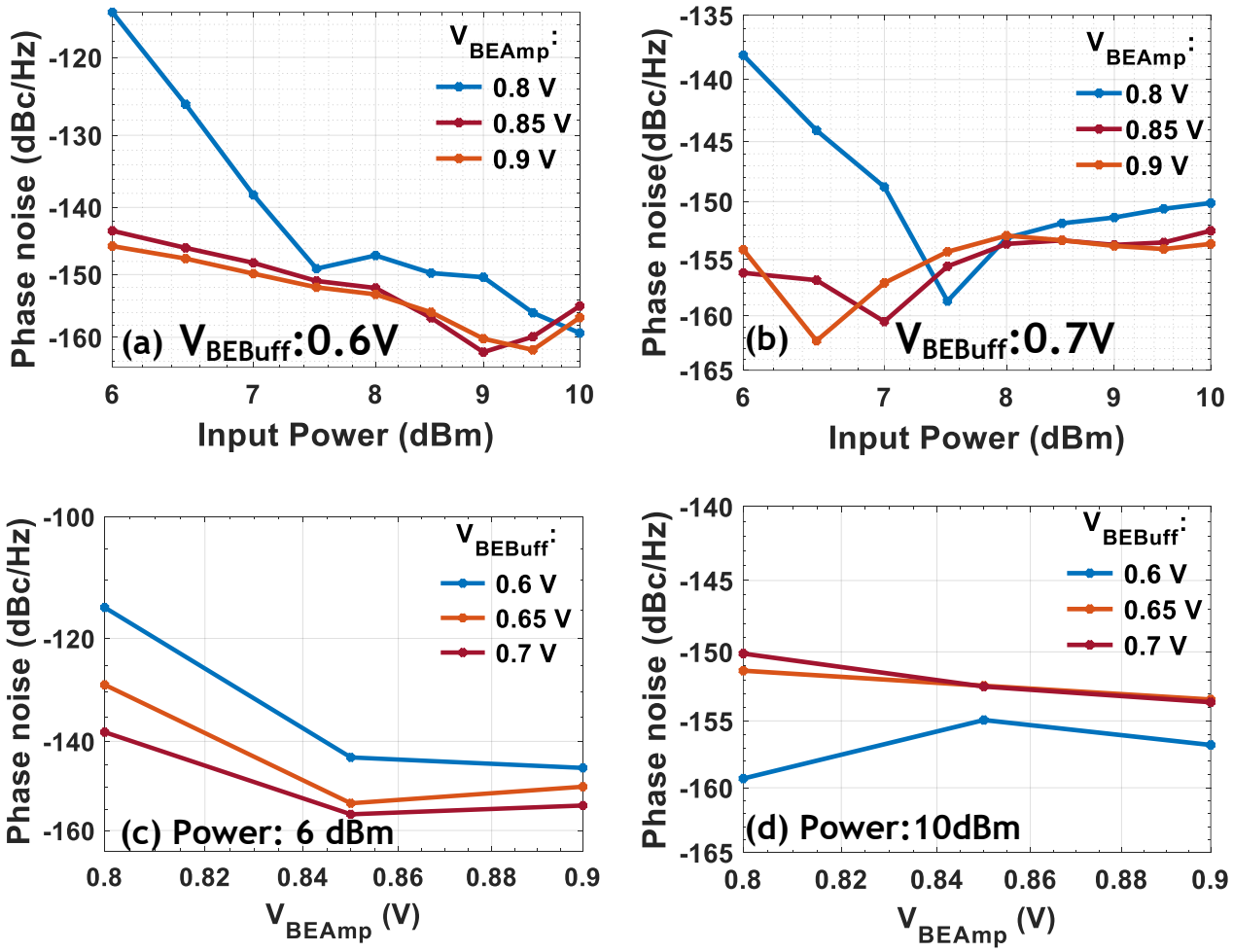


Figure 4.12: Additive phase noise at 14 GHz input frequency (a) versus input power for different bias points for amplifier at 10 kHz offset while V_{BEBuff}: 0.6 V (b) versus input power for different bias points for amplifier at 10 kHz offset while V_{BEBuff}: 0.7 V (c) versus V_{BEAmp} while input power is fixed at 6 dBm at 10 kHz offset (d) versus V_{BEAmp} while input power is fixed at 10 dBm at 10 kHz offset.

4.3.7 Effect of Phase Shifter

The loaded line phase shifter is implemented on the chip to provide the proper division at the output while affecting the other harmonics that exist in the loop. The proper divide by two happens when the signal generated in the loop could satisfy the loop's phase and gain condition ($mf_{RF} + nf_{LO} = f_{IF}$). The strongest harmonic that results in dividing by two, assuming the phase and gain conditions are met, is when $m = 1$ and $n = -1$, leading to $f_{RF}/2$ being generated

in the loop [101]. However, other harmonics within the loop can also satisfy the phase and gain conditions, resulting in a divide by two at the output, such as $m = -1$ and $n = 3$. The phase shift introduced by the phase shifter directly affects the other harmonics in the chain, causing them to either constructively or destructively combine and directly change the phase gain of the mixer (G). Fig. 4.13 (a) and (b) illustrate the effect of the phase shift on phase noise for 14 and 16 GHz input frequencies for different phase shifts, respectively. Table 4.1 compares the performance of

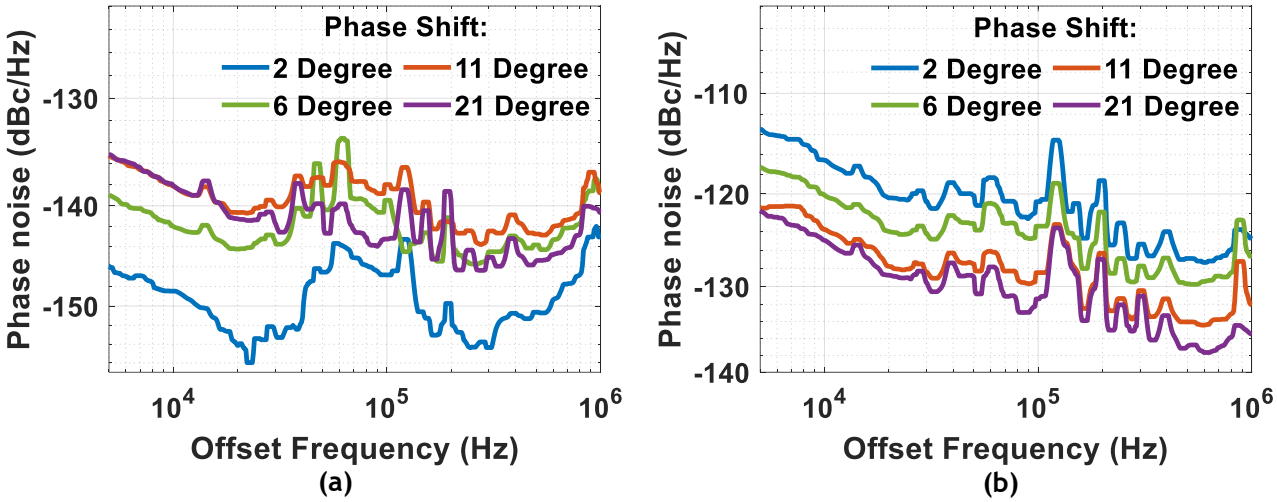


Figure 4.13: Effect of phase shifter on phase noise at (a) 14 GHz input frequency (b) 16 GHz input frequency for V_{BEAmp}: 0.9 V and V_{BEBuff}: 0.55 V. Since at 14 GHz input frequency optimal matching for all passive and active components provides, the best phase alignment was achieved without using the phase shifter.

the implemented divider with other static and regenerative custom ICs and commercial off-the-shelf (COTS) low-phase noise frequency dividers. As shown in Table 4.1, the proposed divider has comparable phase noise performance compared to other dividers while having an octave range of operation with power consumption of less than 60 mW.

Phase noise normalized to a 10 GHz output frequency for various state-of-the-art static and regenerative frequency dividers, with power consumption below 600 mW and phase noise below -100 dBc/Hz at a 10 kHz offset, is presented in Fig. 4.14(a) and (b). The Phase noise is normalized to

Table 4.1: Divide by Two Divider Table of Comparison

Ref	[115]	[130]	[131]	[132]	[102]	[133]	This work
Process /FT(GHz)	InP 0.25um /370	SiGe 0.35um/ 70	AlGaAs/ InGaAs 0.15um /85	AlGaAs/ InGaAs 0.15um	COTS	CMOS 65nm/ 42.7	InP 0.25um /370
Structure	Static	Regen	Regen	Regen	Regen	Static	Regen
Chip size (mm^2)	0.49 x 0.56	3.2 × 3.2	1.8 × 1.9	1.3 × 1.6	NA	0.42 x0.29	0.71×1.2
DC power# (mW)	137	247*	199*	106	NA	21	55
Sensitivity (dBm)	-62	5	9 *	2.7	NA	-46	4
Frequency range (GHz)	1-32	3.2-6.4	22-26	32-36	30	1-39	9-22
Output power (dBm)	>-13	0	-21@ 14GHz	-12@ 17.5GHz	NA	-17 @13GHz	>-10
Fundamental rejection(dB) @Fin	NA	>20	5@ 28GHz	15@ 35GHz	NA	NA	>12
Additive phase noise@ 10 kHz offset(dBcHz) @Fout	-138 5 GHz	-162 2.2 GHz	NA	NA	-162 10 GHz	NA	-163 7 GHz
Absolute Phase noise@ 10 kHz offset(dBc/Hz) @Fout	-120 5 GHz	NA	-114 * 12.5 GHz	-105 * 17.5 GHz	NA	-110 * 10 GHz	-135 8 GHz
Normalized Additive Phase noise@ 10 kHz offset(dBc/Hz) @Fout	-132 10GHz	-149 10GHz	NA	NA	-162 10 GHz	NA	-160 10 GHz

$*$ Estimated from plots. # Total DC power consumption including buffer.

10 GHz carrier frequency at 10 kHz offset by using the equation below [57, 84]:

$$PN_{N(dBc/Hz)} = PN_{(dBc/Hz)} - 20log(f_{(GHz)}/10) \tag{4.2}$$

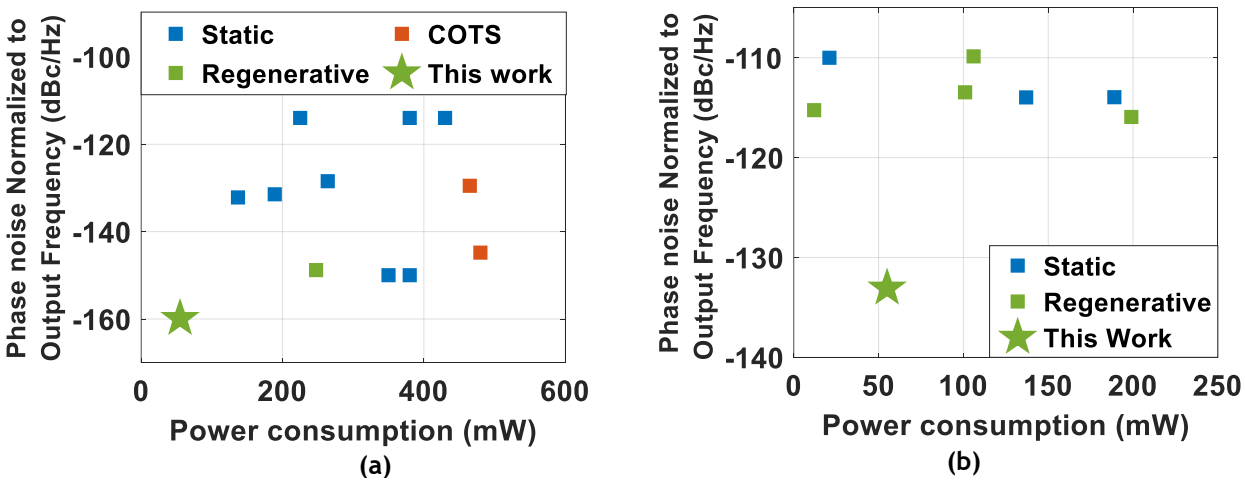


Figure 4.14: The proposed regenerative divider consumes less power than other regenerative, static, and commercial dividers with low-additive phase noise. Phase noise normalized to output frequency (10 GHz) at 10 kHz offset (a) Additive phase noise (b) Absolute phase noise.

4.3.8 Conclusion

This chapter demonstrates an octave-spanning low-additive phase noise dynamic frequency divider in InP 250 nm technology with additive phase noise lower than -163 dBc/Hz from a 7 GHz carrier frequency at 10 kHz offset while consuming less than 60 mW power, 12 dB fundamental rejection, and higher than -10 dBm output power across various measured frequencies. Furthermore, the integration of all components on a single die enables low-phase division and enlightens a pathway for full synthesizer realization.

4.4 Sub-mm wave Low-Additive Phase Noise Regenerative Divide by 2/4

4.4.1 Circuit Design and Analysis

Although achieving ultra-low phase noise division is appealing and enables frequency extension of DDS-based synthesizers, a divider with a division ratio greater than two is required to further push the bandwidth of the synthesizer. Multiple approaches have been demonstrated to enable different dividing ratios for regenerative dividers [106]. One such approach involves leveraging a frequency multiplier to multiply the LO frequency compared with the IF frequency ($f_{LO} = m \times f_{IF}$) which resulted in $m + 1$ diving ratio ($f_{IF} = f_{RF}/(m + 1)$). However, the additive phase noise of the multiplier will impact the noise performance of the system. In order to attain simultaneous divide by two and four outputs, two regenerative dividers are utilized in a cascade manner, one working within the X-band to K-band frequency range and the other one working in the C-band range as shown in Fig. 4.15.

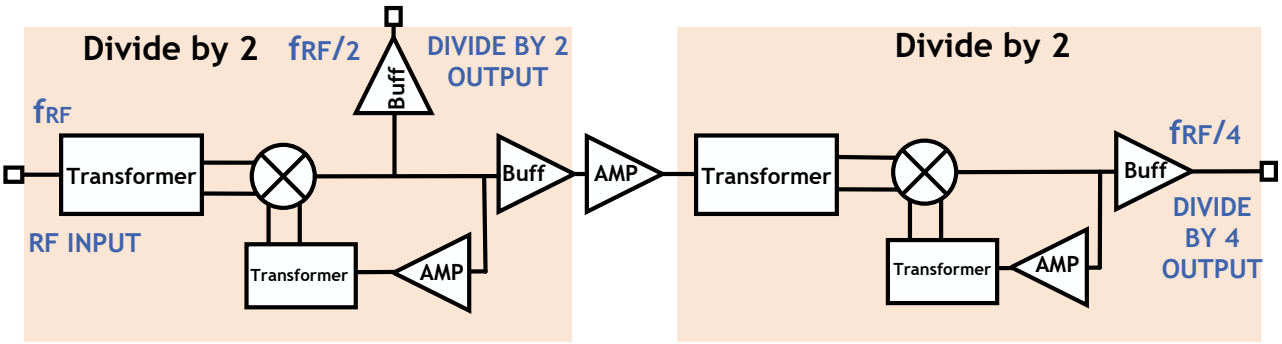


Figure 4.15: Simultaneously divide by two and four schematic

4.4.2 Measurement Results of divide by 2

The regenerative divider is fabricated in InP 250 nm HBT process with collector current and voltage of the amplifier set to 30.1 mA and 3.1 V, respectively.The die photograph of the fabricated divider is shown in Fig.4.16. The sensitivity measurement of divider is plotted in Fig.4.17 (a), illustrating lower than 1 dBm input power required at a 10 GHz input frequency for proper division. The output spectrum of the divider is plotted in Fig. 4.17(b) with 7 GHz Bandwidth. The

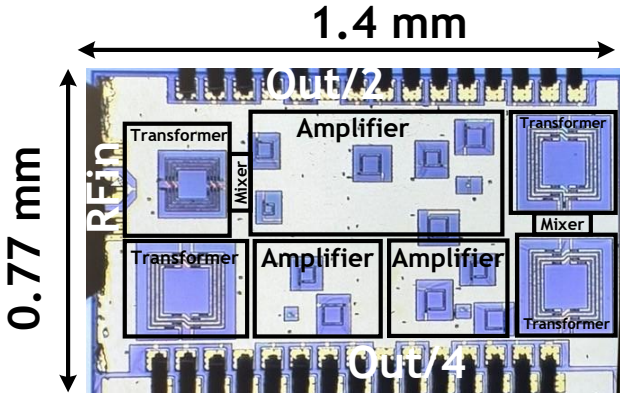


Figure 4.16: Die photograph of fabricated divider

absolute phase noise measurement plot is conducted using a phase noise analyzer. The phase noise performance of the fabricated divider for two different input frequencies is plotted in Fig.4.18, demonstrating 6 dB phase noise reduction from the source, which emphasizes that the additive phase noise of the divider is lower than the measured phase noise.

4.4.3 Simulation Results divide by 4

Fig.4.19 shows the output spectrum and time domain simulation results of divider by 4 at 12 GHz input frequencies with more than 20 dB fundamental suppression over the range of operation. The designed divide by 4 can provide more than 0 dBm output power with a broad range of operation from 8 to 15 GHz.

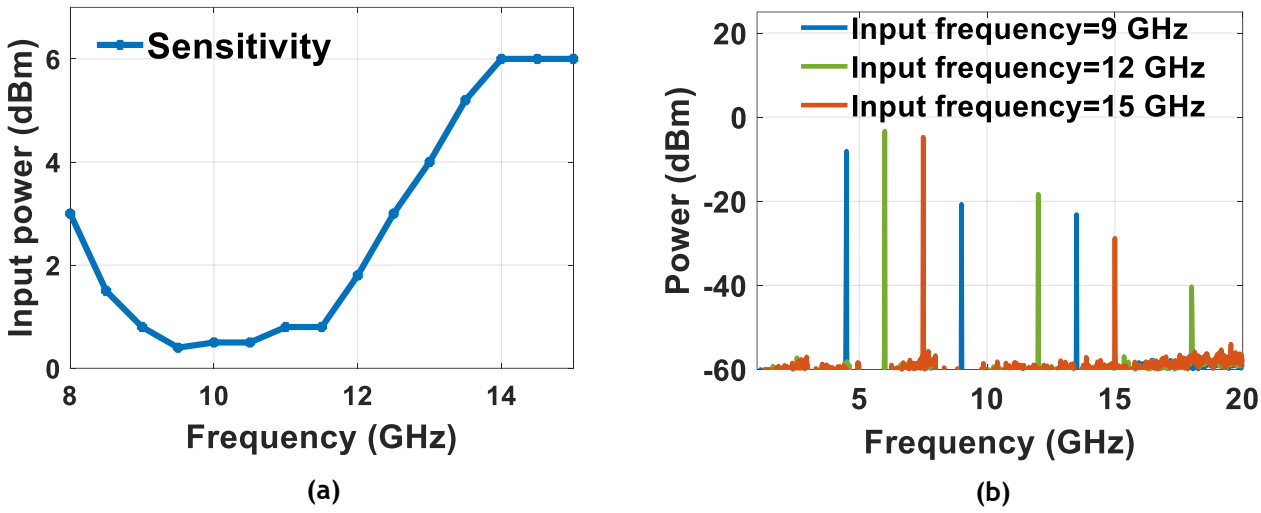


Figure 4.17: (a) Minimum input power required for proper division (Sensitivity).(b) Frequency spectrum for different input frequencies.

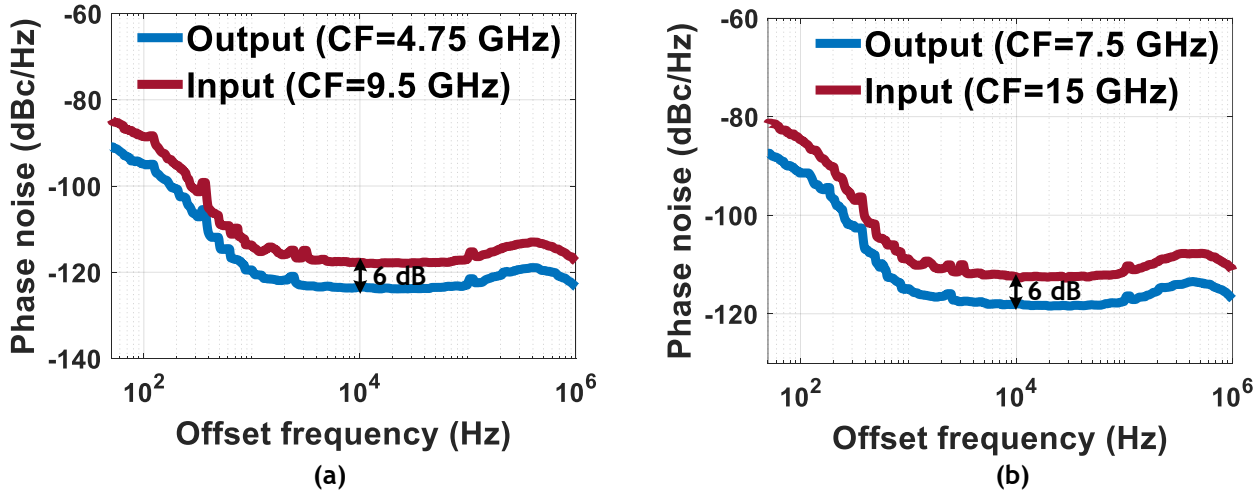


Figure 4.18: (a) Absolute phase noise at 4.75 GHz output frequency. (b) Absolute phase noise at 7.5 GHz output frequency matches with a 20 log (2) reduction in source phase noise.

4.5 Conclusion

This chapter discusses the challenges and limitations of regenerative dividers, one of the key building blocks in DDS-based frequency synthesizers. Regenerative dividers are widely utilized to achieve ultra-low phase noise performance but face several inherent limitations, such as restricted

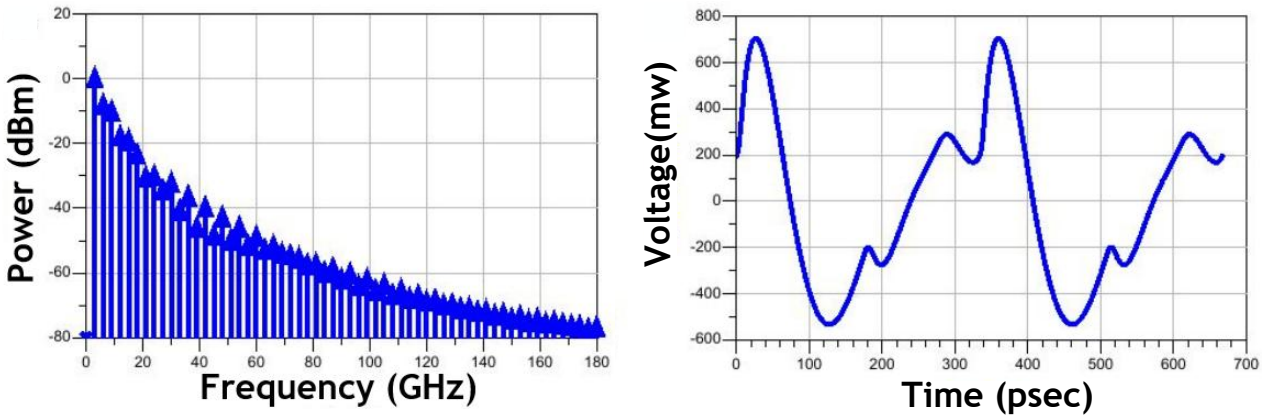


Figure 4.19: The output spectrum and time domain simulation results of divide by four at 12 GHz input frequency.

frequency range and a large form factor. To make regenerative dividers practical for on-chip integration and broadband applications, overcoming these limitations is essential.

This chapter introduces multiple approaches to achieving ultra-low phase noise performance while simultaneously optimizing DC power consumption and minimizing form factor. Additionally, it examines the impact of output buffers and amplifiers within the feedback loop on overall phase noise performance.

The proposed divider enhances the capabilities of integrating low-phase noise components on-chip, enabling broadband frequency synthesizers with low additive phase noise. It also addresses and mitigates several conventional drawbacks associated with traditional regenerative dividers.

4.6 Contribution

This work was done in collaboration with Samin Hanifi and Shadrach Sarpong. I would like to thank them for following contribution:

- Samin Hanifi contributed to the system-level schematic and layout design of divide-by-two and four, passive balun in divide by two and divide by two and four, as well as conducted measurements for the divide-by-two circuit. Additionally, she performed theoretical calcu-

lations to evaluate phase noise considerations in low-phase noise dividers.

- Shadrach Sarpong for schematic and layout design of high input impedance buffer in divide by two and four divider.

4.6.1 Publications

- S. Hanifi, **P. Shirmohammadi** and S.M. Bowers "Additive Phase-Noise Reduction in Microwave Regenerative Dividers" in *IEEE Transactions on Microwave Theory and Techniques (TMTT)*, under review.

- S. Hanifi, **P. Shirmohammadi**, S. Sarpong and S.M. Bowers "Ultra-Low Phase Noise Microwave Frequency Divider for Low Noise Photonic-based Signal Generation" to be submitted to *IEEE Transactions on Microwave Theory and Techniques (TMTT)*.

Chapter 5

Ultra-Broadband Low Phase Noise DDS-Based Frequency Synthesizers

5.1 Introduction and Prior Art

As mentioned earlier in Chapter 1, photonic-based microwave and mm-wave signal generation techniques such as Optical Frequency Division (OFD) have demonstrated ultra-low phase noise performance and surpassing the conventional electrical oscillators [57]. Although OFD and other photonics-based techniques demonstrated extraordinary ultra-low phase noise performance achieving -154 and -153 dBc/Hz at 10 kHz offset from 10 and 40 GHz carriers respectively, they usually suffer from limitations such as fixed output frequency and lack of tunability [107]. To address this concern, Chapter 2 presents a COTS synthesizer designed to achieve broader tunability while preserving the low-noise profile of the generated signal.

To extend the generated output frequency beyond the limitations of DDS, Chapter 2 explores the use of a mixer to combine the tunable DDS output signal with a fixed input tone. This process results in a shift at the center frequency of the synthesized signal from DC to the input frequency, as shown in Fig.5.1. Although mixing a single tone with DDS output can extend the synthesized tone

to a higher center frequency, this approach suffers from limitations such as unwanted harmonics and restricted tunability [1, 108].

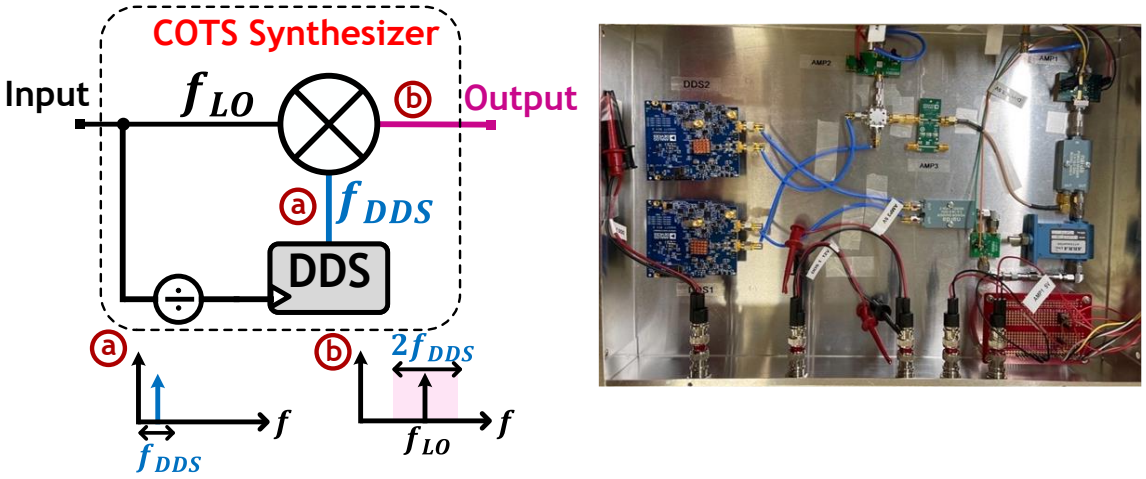


Figure 5.1: Low-phase-noise signal generation using COTS DDS reported in [1, 2] along with COTS synthesizer picture

In order to achieve higher frequency tunability, cover multiple frequency bands and reduce unwanted harmonics generated by the mixer, a new scheme has been proposed in this paper, as shown in Fig.5.2. In this approach, the input signal would go through cascaded frequency dividers to generate multiple tones for the final mixing stage, effectively transferring the tunability of DDS to different LO tones of the mixer as illustrated in Fig.5.2.

To supply different LO frequencies for the mixer, multiple frequency dividers are required. Regenerative dividers offer low-phase-noise performance; however, they are constrained by their large physical size and high power consumption [100, 101]. To overcome these limitations while still benefiting from low-phase-noise division, a dual-mode regenerative divider is implemented in this design, enabling both divide-by-two and divide-by-three operations. Dual-mode dividers leverage a frequency multiplier that can also function as an amplifier. By switching the operating mode of this block, the entire divider transitions between different division modes, allowing for both divide-by-four and divide-by-six operations.

Moreover, the output of a frequency synthesizer must be free of spurs; however, the nonlinearity

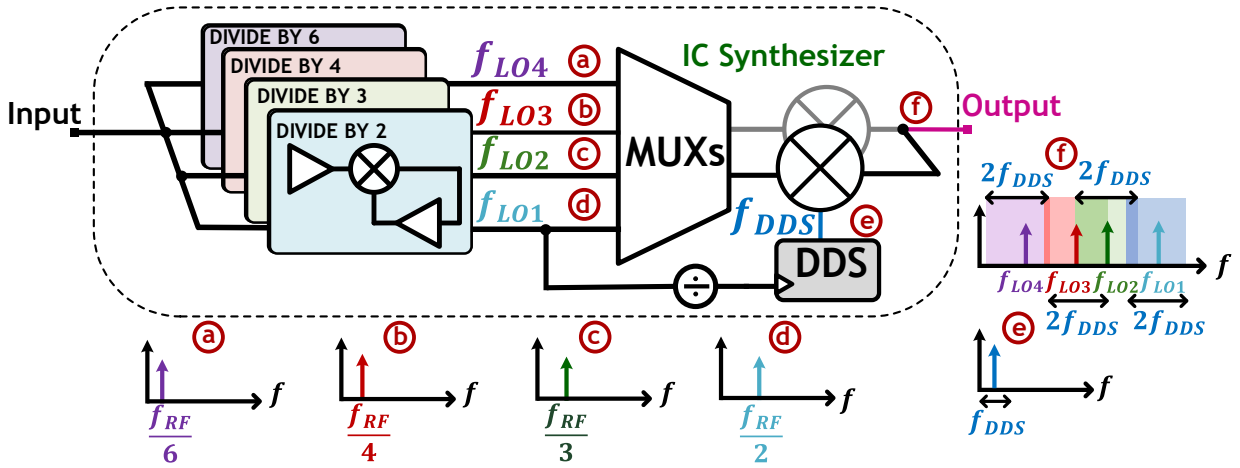


Figure 5.2: The proposed synthesizer uses multiple frequency dividers to cover a broad range of operations and achieve low-phase-noise signal generation.

of different components in the signal chain, particularly mixers, significantly affects the output, generating unwanted harmonics. To mitigate this issue, single-sideband (SSB) mixing is a viable solution, which requires quadrature signal generation over a broad frequency range [109, 110]. Achieving quadrature signal generation across a wide range of frequencies can be accomplished using ring oscillators [111], static frequency dividers [112], or multiple stages of polyphase filters [109, 110]. However, each of these approaches comes with its own limitations [113]. Ring oscillator provides quadrature signal but suffers from additive phase noise and limited tunability [114]. Static frequency dividers can provide I and Q signals over a wide frequency range [115], but they require an input frequency twice the desired frequency, adding design complexity and impacting phase noise. Polyphase filters, while useful, are constrained by limited bandwidth, sensitivity to load and source impedance, and high losses [113]. As a result, achieving broadband multi-phase signal generation on-chip remains a significant challenge [116]. To address these limitations, this dissertation implements a broadband transformer-based architecture that enables low conversion loss and high bandwidth while maintaining a compact form factor.

To highlight the effectiveness of the proposed technique, an ultra-wide band frequency synthesizer is implemented in SiGe BiCMOS 9HP process. The measurement of the designed system achieves a frequency range more than 9.3 GHz, spanning from 0.66 GHz to 10 GHz, using a fixed 16 GHz

input tone. he measured phase noise performance of the synthesizer ranges between -131 dBc/Hz to -139 dBc/Hz, while power consumption is between 1075 and 949 mW based on the mode of operation.. This performance is currently limited by the phase noise of the 16 GHz input source and could be further improved by using a lower-phase-noise input signal.

The rest of this chapter is divided into the following sections. Section 5.2 provides a discussion of circuit design and implementation for various components along the chain, system level measurement results are shown in Chapter 5.3 and finally the conclusion are drawn in Chapter 5.4.

5.2 Circuit Design and Implementation

As discussed earlier, multiple frequency dividers are employed to generate the necessary tones for a single-sideband mixer in the final stage. A detailed block diagram of the designed synthesizer is presented in Fig.5.3. The input signal goes through single to differential conversion using a passive balun. This transformation provides differential signals through the entire chip and leverages the inherent advantages of differential design including common mode noise rejection and even harmonic suppression. The differential signals pass through a K-Ku band divide-by-two Frequency divider to generate the first LO tone for the final stage of the mixing. The output of divide by two also drives two different Frequency dividers: A static D-latch-based Frequency divider and an X-C variable regenerative divider. The X-C band divider can be configured as either divide by two or divide by three. Given that the input signal has already undergone a divide-by-two operation, the final output of the X-C band divider can be configured to provide either a divide-by-four or divide-by-six, relative to the original input signal.

In order to select the desired Frequency band and minimize the leakage from unwanted LO tones to the output, multiplexers (MUXs) are employed to isolate and route the wanted tone. To further suppress the unwanted harmonic, quadrature phase generation followed by single a sideband mixer is required. Thus an on-chip passive transformer-based quadrature generator is implemented to provide all four phases required for single side band mixing.

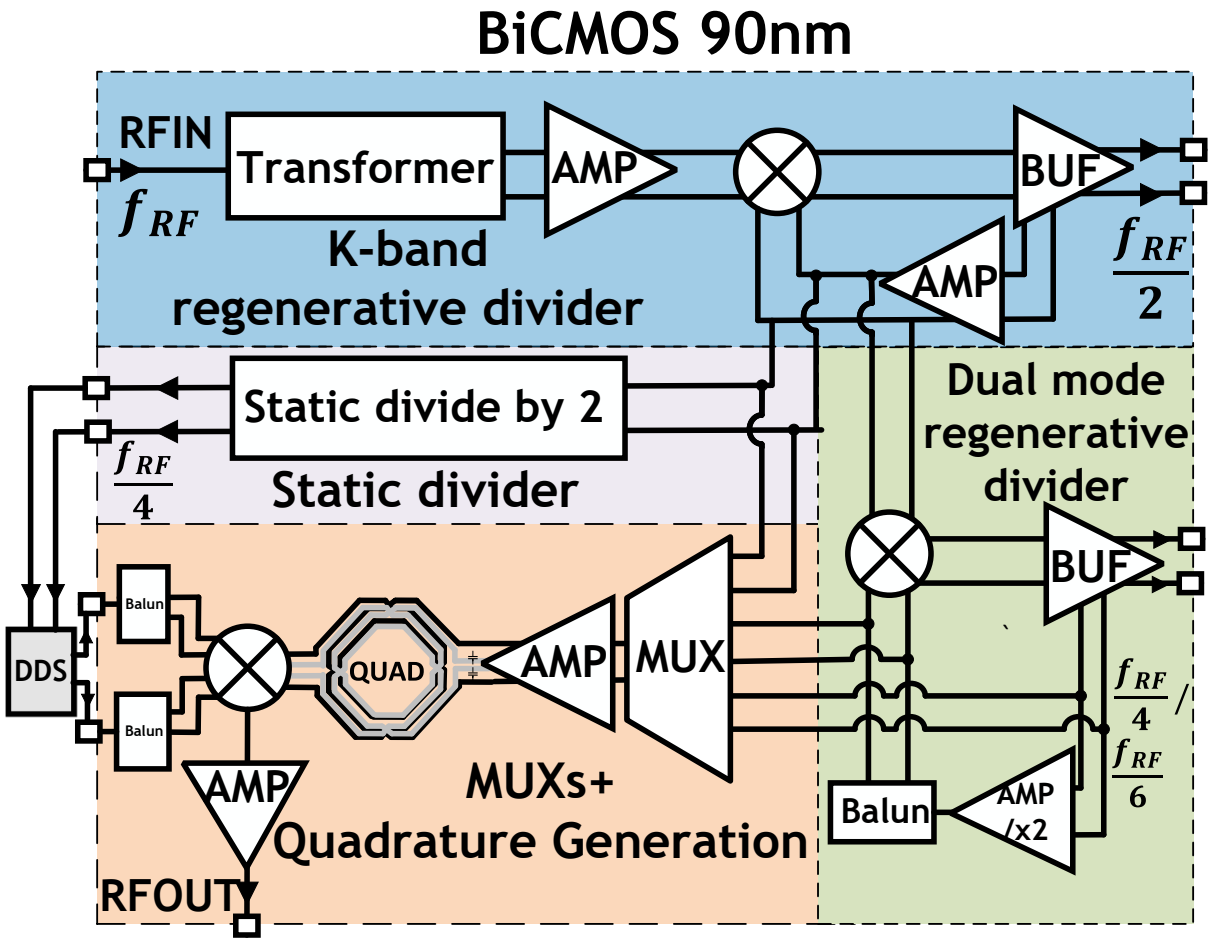


Figure 5.3: Detailed block diagram of the implemented IC synthesizer.

The output of the static divider is used to provide the clock signal for a Commercial Off-The-Shelf (COTS) Analog Device DDS. The output of DDS would go through a broadband COTS hybrid coupler followed by on-chip active baluns to provide all four phases for intermediate frequency (IF) port of the mixer. The final single-ended output of the mixer is amplified using a broadband single-ended amplifier to boost the output power and drive the 50-ohm input impedance of spectrum analyzers. The following subsections provide a detailed description of the main sections of the design.

5.2.1 Low Phase Noise Amplifier

As mentioned in Chapter 3, one of the key components of the entire synthesizer is the amplifiers. As illustrated in Fig. 5.4, a significant number of amplifiers are used throughout the design to boost power levels along the signal chain, ensure sufficient gain to meet the gain requirements of regenerative dividers and provide enough output power at the final port to ensures that the IC synthesizer is a practical candidate for communication and radar systems [4, 117].

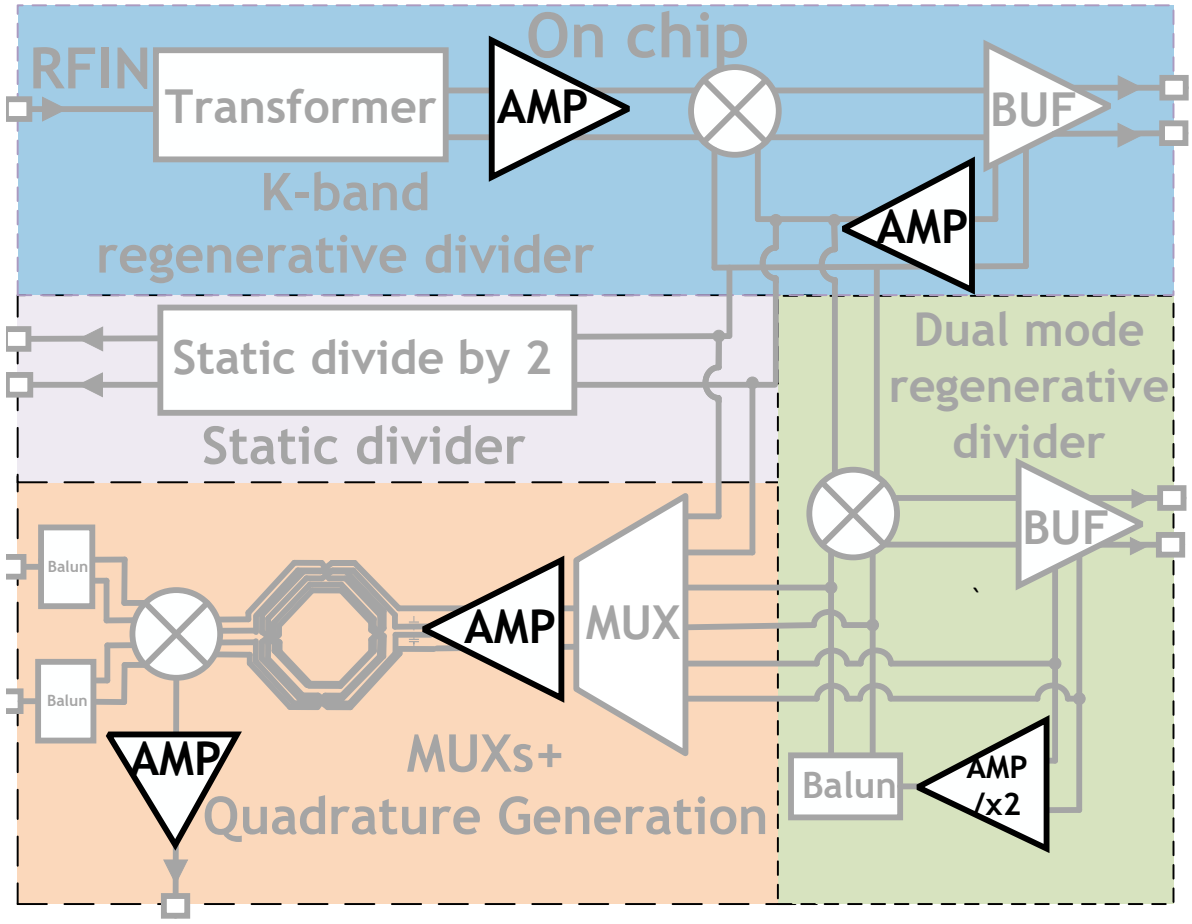


Figure 5.4: Impact of amplifiers in BiCMOS synthesizer and their critical role in design.

Although amplifiers are key building blocks of the synthesizer and facilitate low-phase-noise tunability by providing both small- and large-signal gain, their phase noise performance can ultimately limit the overall system performance and act as a bottleneck for the entire synthesizer loop. There-

fore, the amplifiers designed and implemented within the loop must achieve high gain and high saturation output power while exhibiting exceptionally low residual phase noise over a wide range of frequencies.

As mentioned earlier in chapter 3, one of the effective methods to push the additive phase noise of amplifier lower is power combining techniques [44, 46]. Different power combining techniques have been introduced such as the Wilkinson and Distributive Active Transformer (DAT) power combiner, however, both of these techniques suffer from the large physical size. In order to keep the form factor of the chip small and still benefit from the power combining technique, transistor-level power combing is chosen in the entire design.

In order to provide the required power for the LO port of regenerative divider and maintain enough power for static divider, a differential X-band amplifier is designed which utilizes the power combining scheme along with advantages that common-mode noise rejection can offer. The small signal gain and phase noise performance of the amplifier is plotted in Fig. 5.5(a). The simulated peak small-signal gain of the amplifier is 15.1 dB, with a 3 dB bandwidth exceeding 8 GHz.The simulated additive phase noise of the amplifier for various input power levels, illustrated in Fig.5.5(b), demonstrates that the amplifier can achieve a phase noise lower than -154 dBc/Hz at a 10 kHz offset.

5.2.2 K Band Regenerative Frequency Divider

In order to generate the first LO frequency for the single sideband mixer and cover the high end of C band and low end of the X-band frequency range for the output of the frequency synthesizer, a divide by two frequency dividers is employed to divide down the 16 GHz input frequency to 8 GHz.

As mentioned earlier, frequency dividers can be classified into three categories: static, regenerative, and injection-locked dividers [118]. Static frequency dividers have the advantage of higher sensitivity and large bandwidth, however, the operation range of this divider is restricted based on

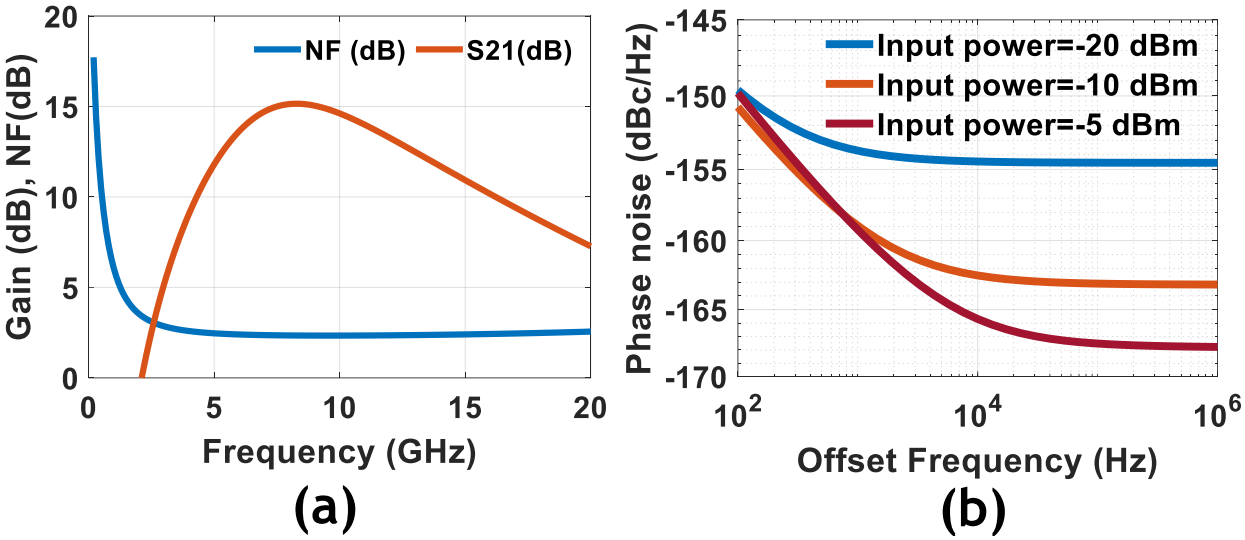


Figure 5.5: (a) Small signal simulation results. (b) Phase noise simulation results of X band amplifier (CF=8 GHz).

the Self Oscillation Frequency (SOF) and their additive phase noise is limited [115]. Regenerative dividers on the other hand offer low additive phase noise with a high operation frequency, making them a more suitable choice for the first divider as shown in Fig.5.6. Nonetheless, the regenerative dividers usually come at the cost of higher input power for proper dividing [101].

To reduce the required input power and compensate for the insertion loss associated with the passive balun, a differential K-Ku band amplifier is designed and implemented. Furthermore, an active Gilber cell mixer is utilized to replace the diode ring mixer to provide more gain and minimize the required input power, with the expense of higher noise.

The additive phase noise of the regenerative divider depends on the additive phase noise of the amplifier. Consequently, an ultra-low phase noise amplifier was designed in the feedback chain to provide enough swing for LO saturation of the mixer and maintain the low additive noise profile. The small signal gain and phase noise performance of the amplifier are plotted in Fig. 5.5.

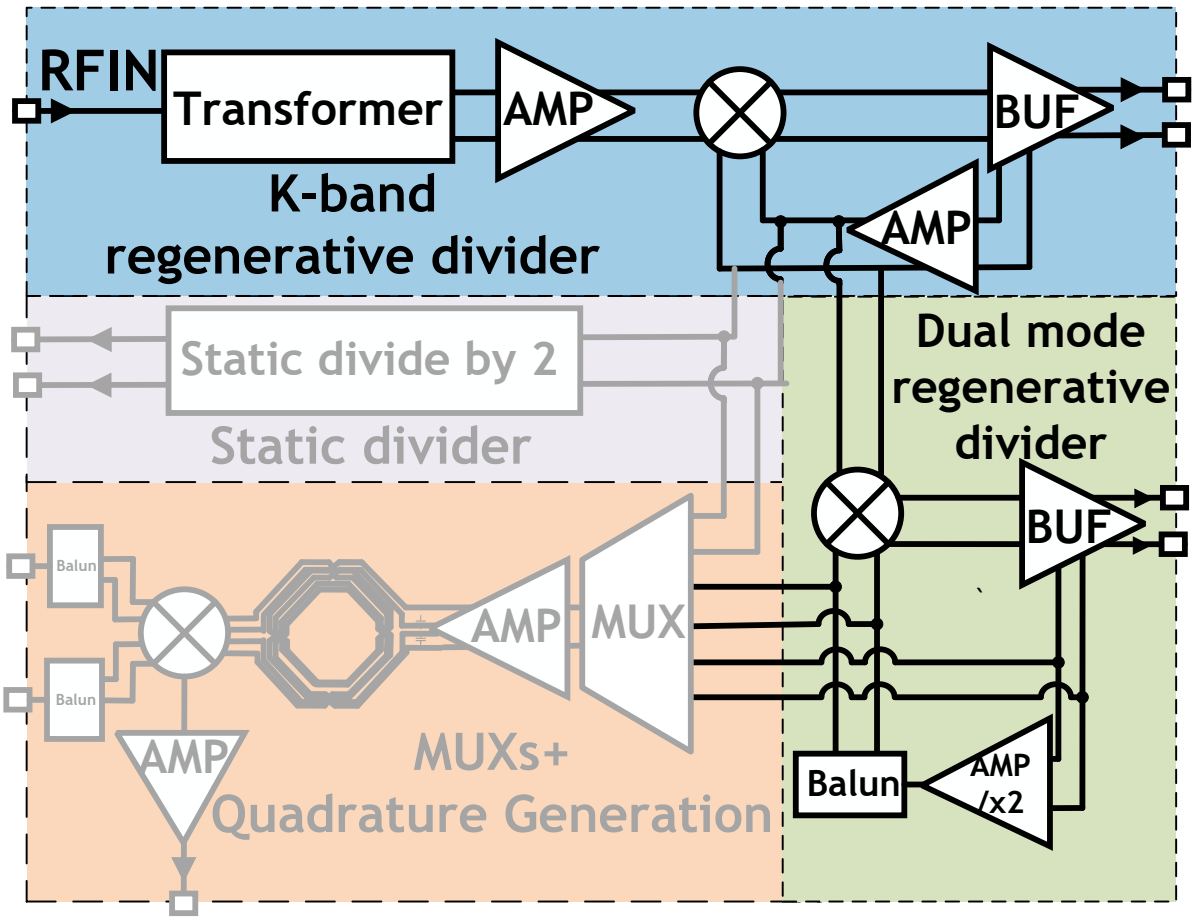


Figure 5.6: Impact of regenerative dividers in BiCMOS synthesizer.

5.2.3 Dual Mode Regenerative Frequency Divider

To generate additional LO tones for the final stage of mixing and extend the bandwidth of the synthesizer, multiple cascaded regenerative dividers are necessary. However, since each regenerative divider incorporates components such as mixers, amplifiers, multipliers, and buffers, integrating multiple dividers on a single chip is suboptimal due to their high power consumption and large physical size. Consequently implementing a Dual Mode regenerative divider is a more practical and efficient solution.

If there is no frequency-converting component in the feedback chain of the regenerative divider, the condition $f_{LO} = f_{IF}$ holds, leading to $f_{IF} = f_{RF}/2$.Under this configuration, the divide-by-

two output propagates along the chain if the phase and gain conditions are met and satisfied [101]. However, if a multiplier, such as a frequency doubler, is present in the chain, the condition $f_{LO} = 2 \times f_{IF}$ is established, resulting in $f_{IF} = f_{RF}/3$ at the output. The block diagrams of divide by two and three are illustrated in Fig. 5.7

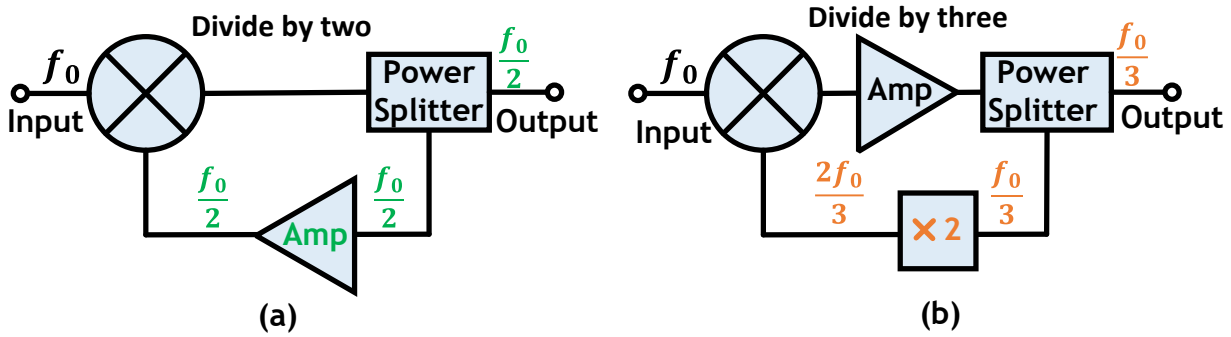


Figure 5.7: (a) Divide by two block diagram (b) Divide by three block diagram.

By implementing a variable doubler that can also function as an amplifier depending on the configuration, both divide-by-two and divide-by-three operations become feasible within the chain as shown in Fig.5.8. Since the input signal initially undergoes a divide-by-two operation, the final output of the Dual Mode divider can be either a divide-by-four or divide-by-six ratio. Furthermore, when the Dual Mode regenerative divider operates in divide-by-three mode, the condition $f_{LO} = 2 \times f_{IF}$ holds, effectively enabling access to a divide-by-two-thirds ratio at the multiplier's output or a divide-by-three ratio relative to the input signal. Thus, by implementing a Dual Mode divider, divide-by-three, divide-by-four, and divide-by-six operations can be achieved with the appropriate configuration.

The schematic of the variable amplifier/doubler is shown in Fig. 5.9. It features a differential common-emitter pair followed by a cascode stage while collectors of the cascode transistors are tied together. A controlling transistor has its emitter connected to one arm of the cascode stage's emitter and its collector connected to the supply voltage. When the base controlling voltage is significantly lower than the base voltage of the cascode stage, the controlling transistor does not draw any current, allowing all the current to flow through the cascode arm, resulting in multiplication at the output, as the fundamental tones in each arm are out of phase and cancel each other out. This

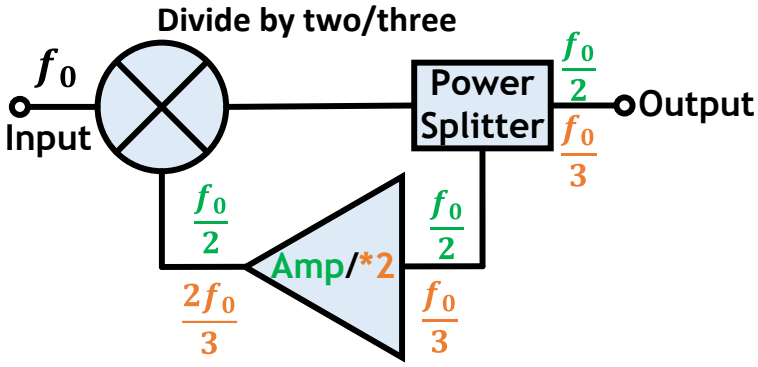


Figure 5.8: Dual mode divider block diagram.

configuration has the fundamental frequency at the collector since the first harmonic components of each arm are out of phase and the second harmonics are in phase.

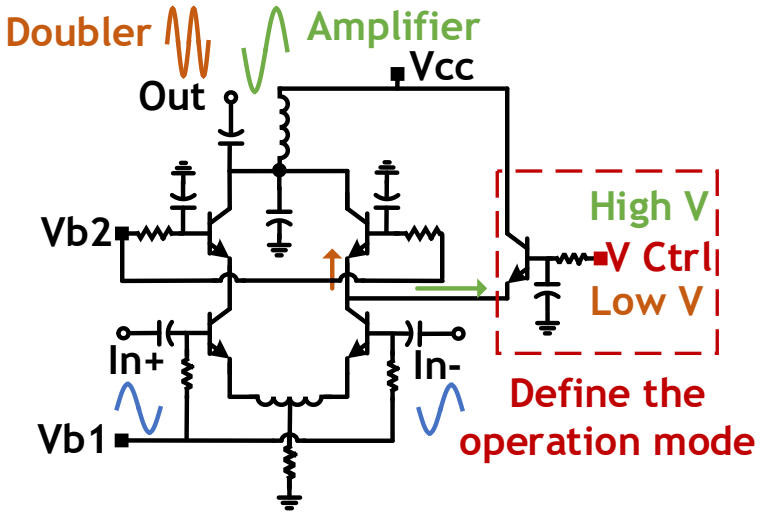


Figure 5.9: Schematic of doubler/amplifier demonstrating the impact of control voltage on the dual mode regenerative divider.

However, when the controlling voltage is much higher than the base voltage of the cascode stage, all the current generated by the common-emitter stage flows through the controlling transistor. In this case, the fundamental frequency becomes the dominant harmonic at the output, as no out-of-phase components are present to cancel it. The large signal simulation results of the doubler/amplifier in each mode are illustrated in Fig. 5.10(a) and (b) respectively.

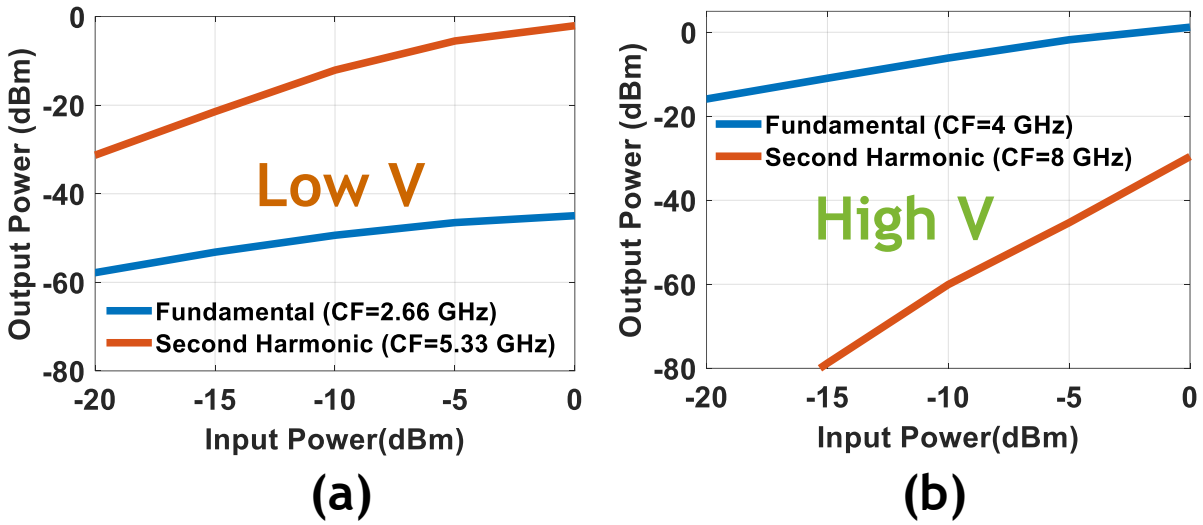


Figure 5.10: large-signal simulation results, demonstrating the impact of control voltage on the variable regenerative divider (high voltage results in a divide-by-four output, while low voltage results in a divide-by-six output)

Due to the inherent nature of the variable doubler/amplifier, a single-ended output and differential input, another single-to-differential conversion is required. However, the gain in the amplifier mode and conversion gain in double mode are insufficient to provide the necessary swing for LO port of the mixer to ensure proper operation. Consequently, an active balun is employed to provide additional gain and saturate the mixer effectively. The simulated small signal performance of the balun along with phase and amplitude mismatch is plotted in Fig.5.11. The simulated peak gain of the balun exceeds 8.4 dB, with a bandwidth greater than 6.5 GHz. It achieves phase and amplitude imbalances of less than 3 degrees and 1 dB, respectively.

5.2.4 Static Frequency Divider and DDS

As mentioned at the beginning of Chapter 2, a DDS is a sampled data system, indicating that it requires a reference signal to function as the clock of the system to generate m-Hz resolution tuneable output. In a simplified model of the phase noise of the DDS, it behaves like a variable frequency divider and would track the input source phase noise with the division factor until it got limited by the internal noise of DAC and up-conversion of near DC flicker noise to the frequency

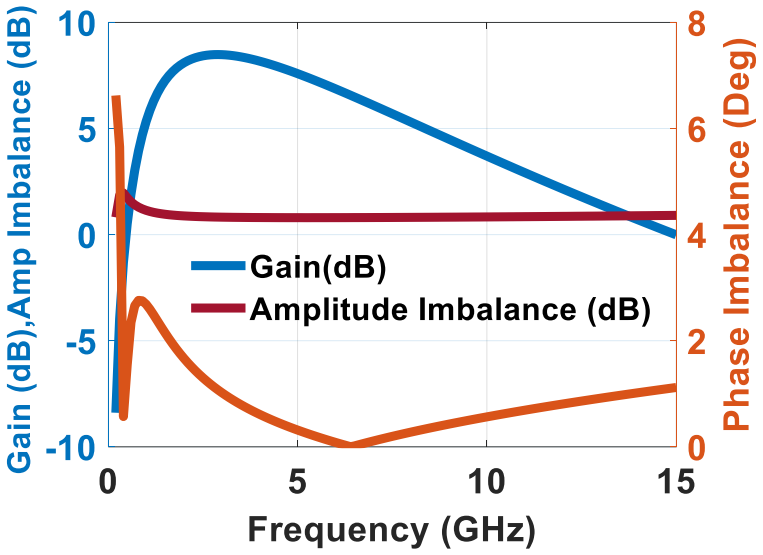


Figure 5.11: Active balun simulation results including the gain and phase and amplitude mismatches.

of interest [69]. In order to benefit from low phase noise signal at the output of the DDS, it is critical for the input reference signal to be low phase noise itself.

An Analog Device AD9164 DDS is used to achieve the desired tunability, which can work with internal reference as well as external reference, while the optimum performance is achieved with a low-jitter external single feed into the DDS. The maximum input frequency of the DDS is 6 GHz, as a result, an additional frequency divider is needed to further divide down the 8 GHz output of the first regenerative divider down to 4 GHz. Although the regenerative frequency divider shows superior performance in terms of additive phase noise, the required input power, the need for an additional low-phase noise amplifier, and the form factor of the regenerative divider at lower frequencies is a practical restriction. On the other hand, the static frequency divider shows better performance in terms of power consumption and lower input power, and a smaller physical dimension at the lower input frequency [119]. Therefore, a low-phase noise static frequency divider is devised to further divide the input frequency all the way down to 4 GHz.

The static frequency divider utilizes a current-mode logic (CML) design based on a leader-follower D-latch architecture. In this configuration, the outputs of the second (follower) D-latch are fed back to the inputs of the first (leader) D-latch through negative feedback. By cascading the two

D-latches, the desired frequency division is achieved at the output.

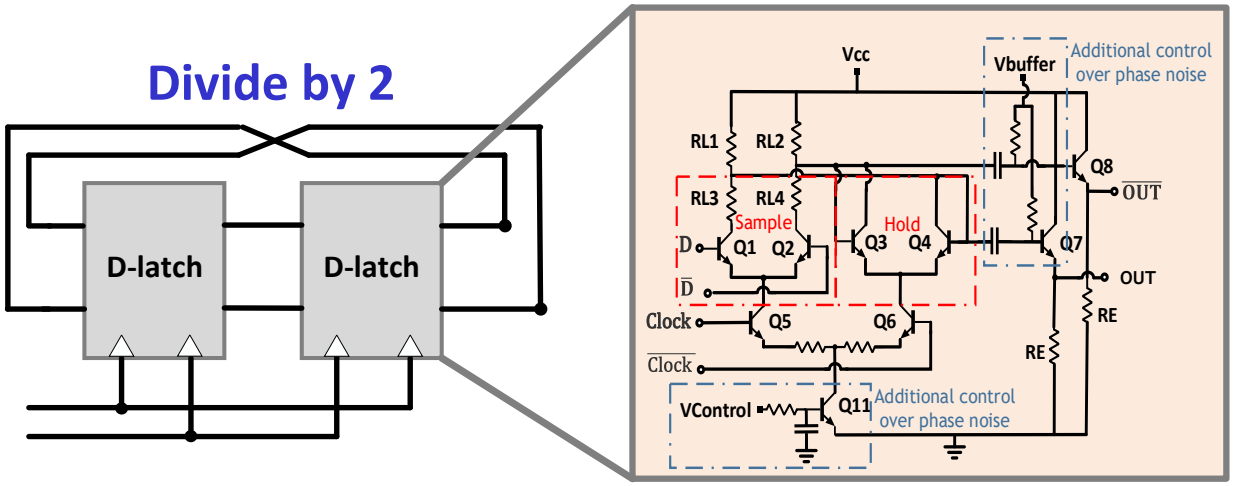


Figure 5.12: Schematic of the implemented static frequency divider.

In order to provide enough swing for the follower D-latch, two emitter followers stages are used at the output of each D-latch. Fig. 5.12 shows the block diagram of leader and follower D-latch and divide by 2 respectively.

In order to provide enough voltage swing for the DDS input clock, the output power of the divider needs to be greater than -20 dBm on a 50 Ω resistor. Consequently, to ensure enough swing to generate the required power and keep the transistor away from the saturation region, a two-stage load resistor is incorporated into this design. The time domain response along with the phase noise performance of the frequency divider is plotted in Fig. 5.13

The output of the static divider is fed into the input of the DDS to enable sub m-Hz frequency tuning. The output of the DDS passes through a COTS RF-Lambda hybrid coupler to generate 0 and 90 degrees outputs. These signals are then connected to two on-chip active baluns to produce the four-phase signals required for single-sideband mixing at the IF port of the mixer.

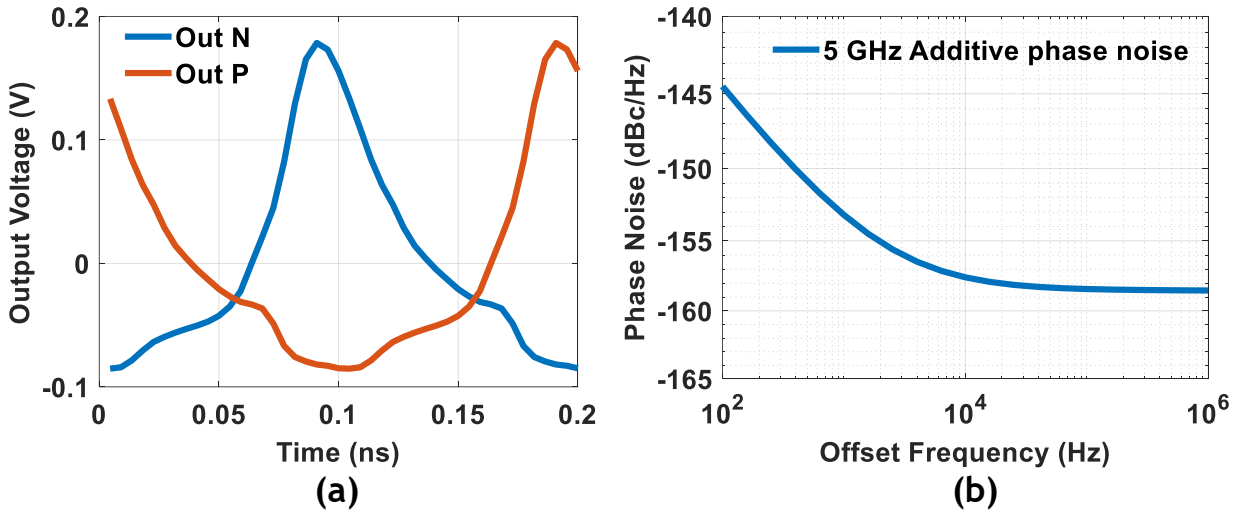


Figure 5.13: (a) Time domain simulation result of divider. (b) Phase noise simulation result of the divider.

5.2.5 Multiplexing And Single Side Band Mixing

Ideally, the output of the frequency synthesizer needs to be a clean single-tone without the unwanted harmonics. However, the multiple LO tones generated through multiple stages of frequency division, combined with the final stage of mixing, can degrade the purity of the output signal.

To mitigate the impact of unwanted harmonics, two key design efforts are required. The first involves low-phase-noise multiplexing, which selects the desired frequency range while eliminating unwanted harmonics. The second is single-sideband (SSB) mixing, which minimizes spurs generated in the final stage of the mixing process. Spur rejection and spur-free dynamic range are critical parameters in frequency synthesizers and can potentially serve as limiting factors in applications such as radar and phased array systems [120]. As a result, MUXs and SSB mixing play a crucial role as key building blocks in the synthesizer, as highlighted in Fig. 5.14.

Due to the presence of multiple LO tones, an analog multiplexer (A-MUX) is required to select the desired frequency band [121]. The operation of a 2:1 A-MUX is based on a modified Gilbert cell architecture [121] as illustrated in Fig.5.15.

The design includes a linearized common emitter stage for data inputs and cascode stages for

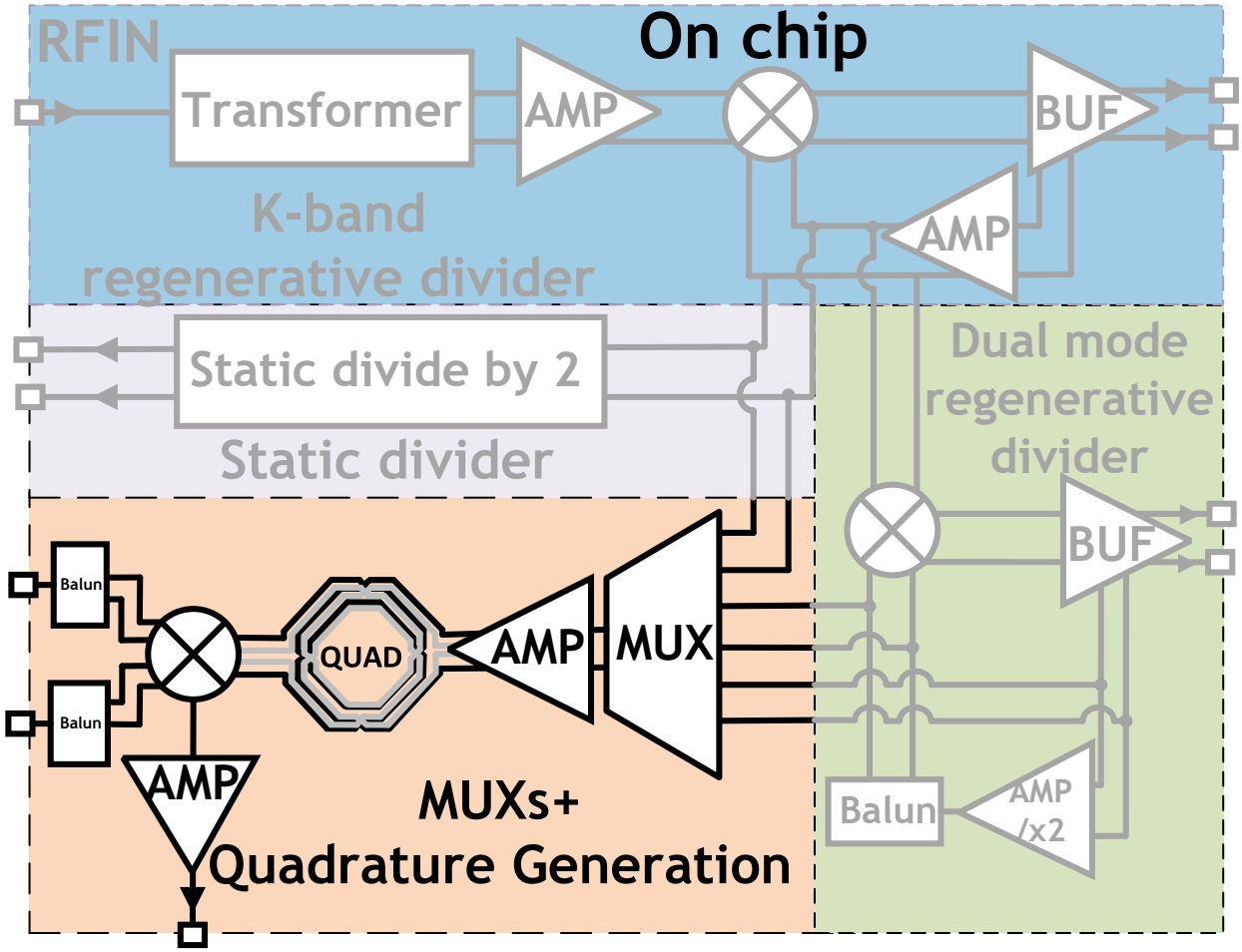


Figure 5.14: The critical role of MUXs and SSB mixing in BiCMOS synthesizer

current switching. Depending on the base voltage applied to the cascode stage, one of the inputs is connected to the output. The small signal and large signal simulation result of the MUX is plotted in Fig.5.16. The small-signal and large-signal simulation results of the MUX are shown in Fig. 5.16. As illustrated in the plot, the small-signal simulation demonstrates a gain of over 2.6 dB across a 9 GHz bandwidth with 18 dB rejection. Furthermore, the large-signal simulation results indicate a P_{1dB} greater than -3 dBm.

Furthermore, the time-domain and phase-noise simulation results of the MUX are shown in Fig. 5.17, where the selected input frequencies are 4 GHz and 8 GHz, respectively. In both the time

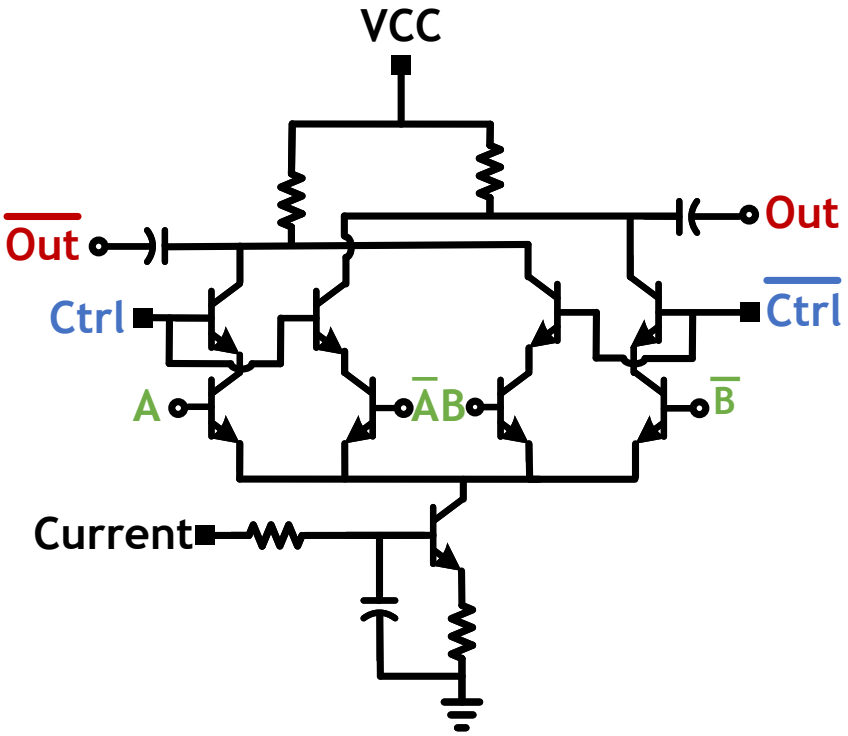


Figure 5.15: Schematic of the designed analog MUX.

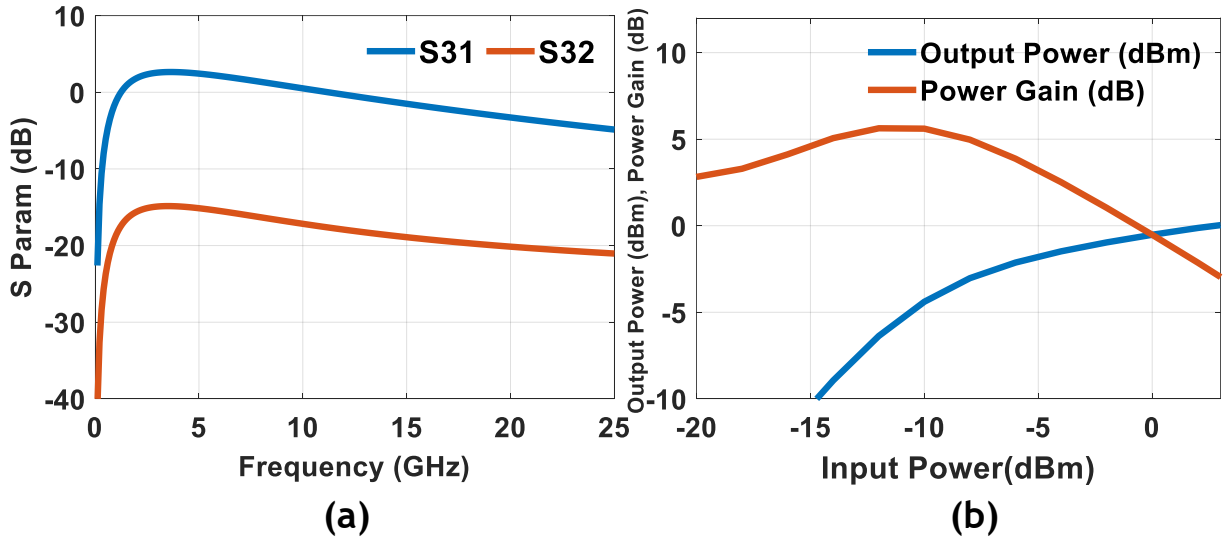


Figure 5.16: (a) Small signal and (b) large signal (CF=4 GHz) simulation result of MUX.

and phase-noise domains, the MUX successfully passed the desired frequency while rejecting the unwanted tone.

Additionally, the phase noise of the output closely follows the phase noise of the selected input, indicating that the additive phase noise of the MUX is significantly lower than the phase noise of both inputs. This demonstrates that the MUX effectively isolates the output from the other input, as the higher phase noise of input 2 does not affect the output phase noise.

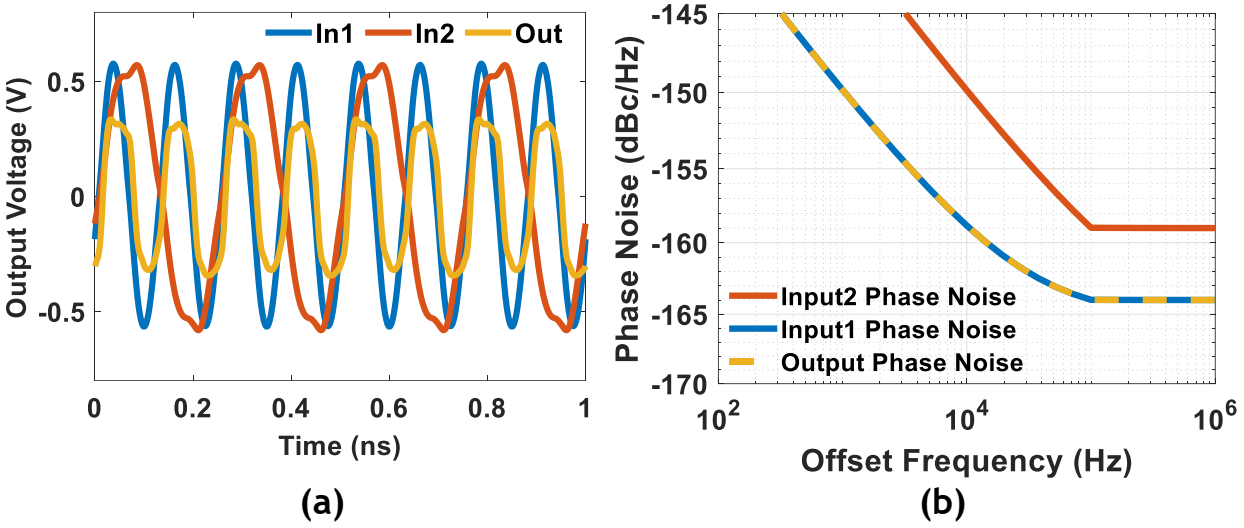


Figure 5.17: (a) Time domain (b) Phase noise simulation result of proposed MUX (CF1=8 GHz, CF2=4 GHz).

The transient response of the MUX when transitioning from Input 1 to Input 2 is shown in Fig. 5.18. The figure illustrates how the output smoothly switches from the first input frequency to the second, demonstrating the MUX's ability to effectively select the desired signal while minimizing distortion.

Furthermore, since the last stage of the designed frequency synthesizer is a mixer, the leakage from the IF and LO ports to the RF port, the image of the mixing product, along with the third and fifth mixing products, are going to be presented in the output of the synthesizer. One potential option to eliminate the unwanted harmonics is to develop a sharp filter, however, the selectivity of these filters along with the desired sub-Hz tunability is going to be a practical limitation [109]. In order to address the abovementioned issues related to unwanted harmonics, a single sideband or image reject mixer is implemented in the design. In order to achieve better image rejection and minimize the sensitivity to phase and amplitude imbalances, double quadrature architecture is employed.

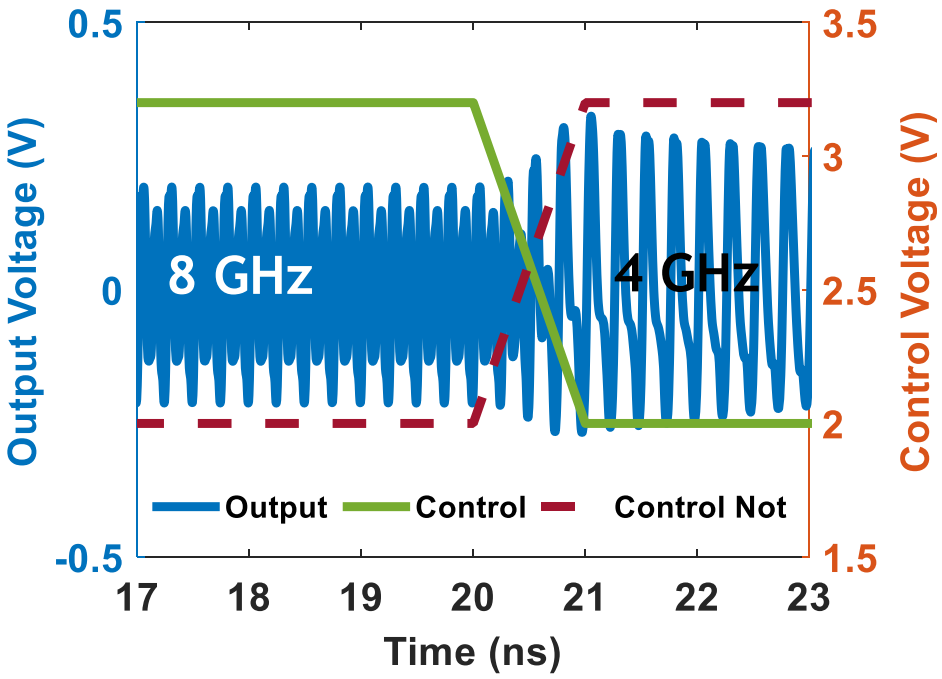


Figure 5.18: Time domain simulation result of the MUX.

This approach ensures that both the IF and LO signals are in quadrature phases, improving the unwanted image along with the third and fifth harmonic.

Passive structures are widely used for quadrature generation due to their superior advantages such as power consumption and linearity [122]. among the passive structures, RC-CR polyphase filters are frequently employed due to their simple and compact architecture, however, their drawbacks include and not limited to conversion loss, narrow bandwidth, and sensitivity to load termination [109, 122]. Another alternative approach involves using transmission line couplers to generate I and Q signals, however, it is highly from large form factor due to their $\lambda/4$ transmission line specifically in the X-band frequency range [123]. On the other hand, using transformer-based quadrature generation is getting more and more interest due to their small form factor and lower insertion loss [122].

In this design, a transformer-based quadrature generation schematic is deployed with the form factor of a single inductor to generate the I and Q signal for the LO port of the single sideband mixer as show in Fig.5.19(a). The time simulation results have been plotted in Fig.5.19(b) for

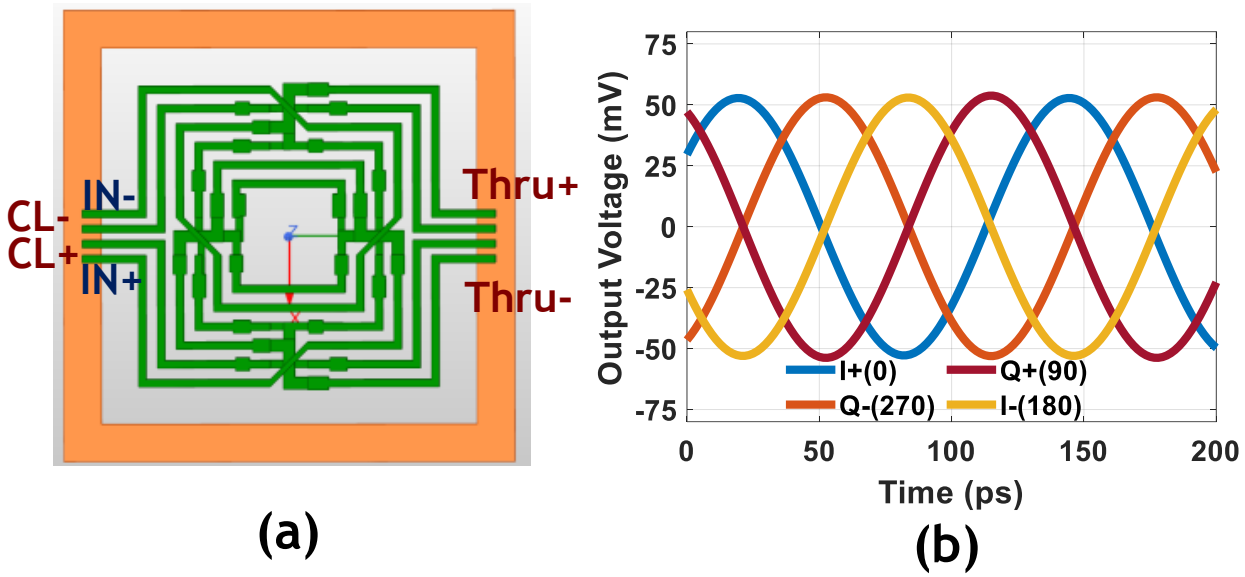


Figure 5.19: (a) 3D image of transformer based quadrature generation. (b) Time domain simulation results (CF=8 GHz, Pin=-10 dBm).

an 8 GHz differential input signal with -10 dBm power. The quadrature could achieve phase and amplitude imbalances of less than 1.5 degrees and 0.2 dB, respectively. When the input frequency is switched to 4 GHz, the phase and amplitude imbalances increase to 3 degrees and 2.4 dB. At an input frequency of 2.66 GHz, the imbalances further increase to 1.7 degrees and 4.7 dB.

In order to remove unwanted image products of the mixer, generating quadrature phases for both IF and LO is required, the quadrature generation of the LO port is achieved using differential output from the regenerative divider and using transformer quadrature generation, however, the sub-m-Hz targeted frequency resolution of the output of frequency synthesizer, simply implies that the IF frequency needs to go all the way down to almost DC. Generating the quadrature phase from DC up to 2 GHz is challenging, one potential option involves using a D-Latch-based static divide by two frequency dividers to generate all four phases [112].

Nevertheless, the divider phase noise and phase and amplitude mismatch of the generated four phases signal, make it less attractive for low phase noise frequency synthesizer especially at lower input frequency (e.g. below 100 MHz, when the additive phase noise of the DDS is well below

-160 dBC at 10 kHz offset). Additionally, the static dividers required a differential input for proper latching and frequency dividing, This requirement entails either additional DDS or designing a balun to generate all four phases.

On the other hand, DDS output frequency and phase can be tuned based on the resolution bits, thus one possible solution is to use 4 DDSs to generate all four phases, nevertheless, the power consumption, form factor, and heat generated by these DDSs render this solution suboptimal. Yet, utilization of multiple DDSs remains an appealing alternative due to fine resolution tuning capabilities for both phase and frequency, as well as their phase noise performance. Furthermore generating broadband low-frequency differential outputs is easier compared to generating broadband quadrature outputs from a single input, As a result, deploying two baluns along with two DDS is preferable. Conventional passive LC-CL balun or transformer-based balun benefited from several advantages such as DC power consumption, linearity, and noise performance, nonetheless, their physical dimension and limited bandwidth make them impractical for wideband, low-frequency applications [124], as a result utilizing a wide band active balun is more advantageous.

The combined schematic of the DDS along with active balun is plotted in Fig. 5.20. Each DDS can be fine-tuned to generate either I or Q, and the generated signal will go through an active balun to generate $\pm$ Q and $\pm$ I and feed into the single side band mixer, depending on whether a DDS is lagging or leading a single tune in upper or lower sideband would be generated.

The active balun can be implemented in a single transistor configuration or common base common collector configuration [125], however, their limitation such as bandwidth and the frequency range of operation renders them unsuitable for broadband operation range, consequently, a differential amplifier-based configuration employed in this design to address these challenges. In order to keep the noise performance of the DDS, the active balun needs to exhibit very low residual phase noise as a result a power combined schematic has been implemented to take advantage of lower flicker noise. The small signal simulation result and amplitude and phase imbalance of the implemented active balun are plotted in Fig.5.21(a). The active balun can reach a peak gain of 9.8 dB with more than 5.85 GHz bandwidth and less than 0.5 dB and 3 degrees amplitude and phase imbalance

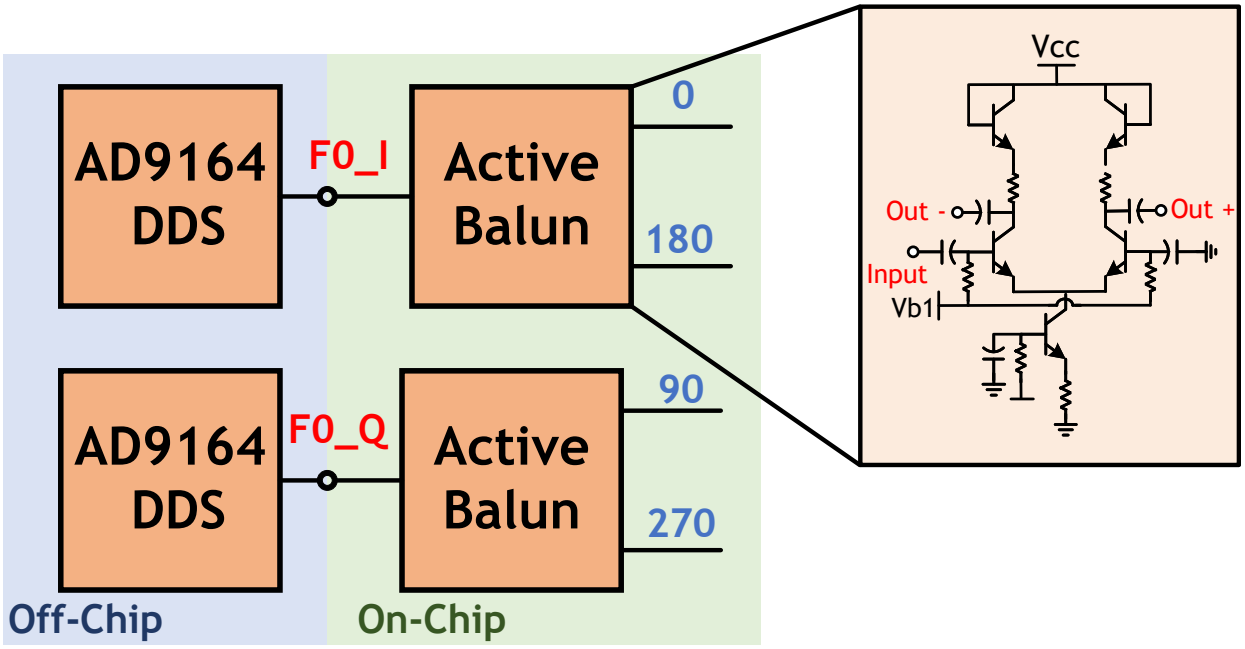


Figure 5.20: Block diagram of two DDSs and two active baluns for quadrature phase generation.

receptively and the balun can achieve lower than -158 dBc/Hz additive phase noise at 10 kHz offset from a broad range of carrier frequencies as demonstrated in Fig.5.21(b).

5.3 Measurement Results

The proposed synthesizer is designed and fabricated in Global Foundry BiCMOS 9HP process. The fabricated IC and measurement setup are plotted in Fig.5.22(a) and (b) respectively. The fabricated synthesizer was tested using a fully wire-bonded package. The packaging Printed Circuit Board (PCB) is a 4-layer board with a controlled dielectric, comprising a combination of Rogers 4350 and FR4 materials.

The Coplanar Waveguide (CPWG) on the PCB is implemented on the top metal layer as the signal path, with the second metal layer serving as the ground plane, utilizing Rogers 4350 as the dielectric. To minimize wire-bond height, the silicon substrate was back-grinded to a thickness of 75

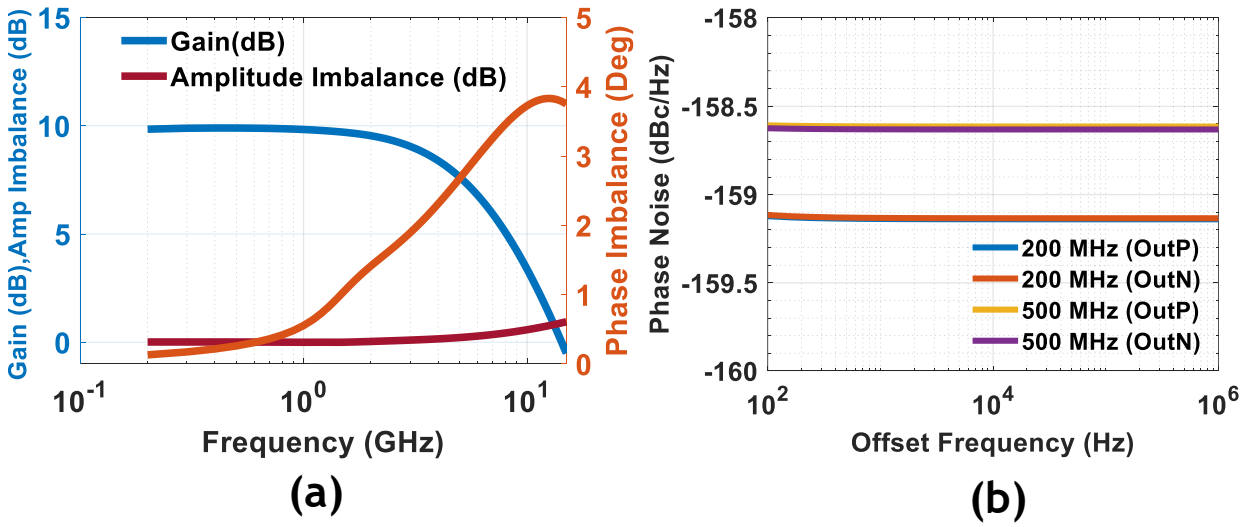


Figure 5.21: (a) Low frequency balun small signal simulation result (b) Phase noise simulation result

μm. All measurement results were calibrated, with the calibration plane set at the PCB connector interface.

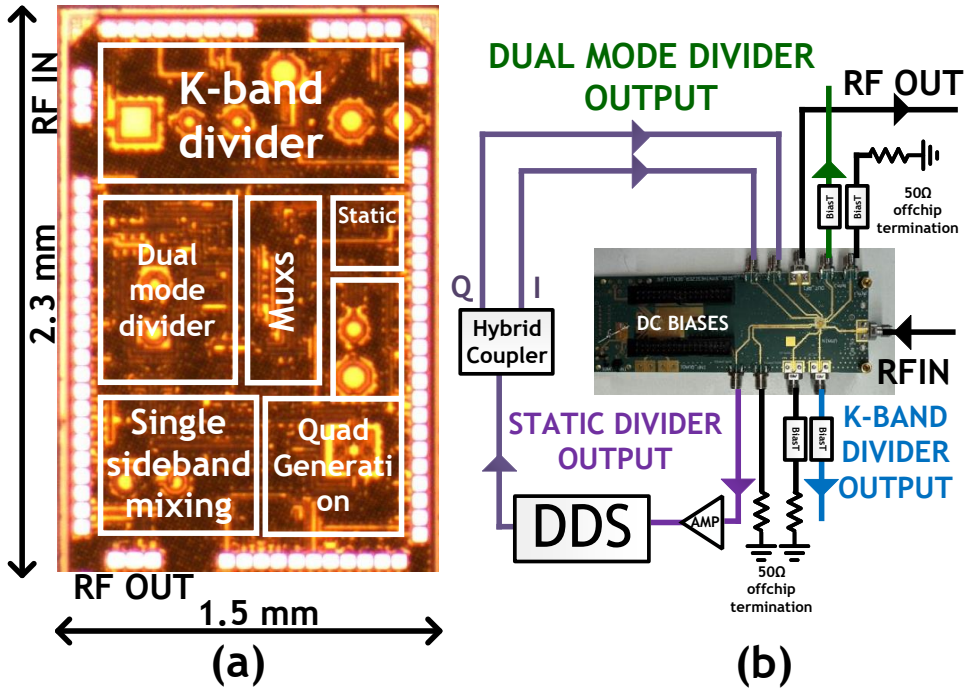


Figure 5.22: (a) Die photo of the fabricated synthesizer. (b) Measurement setup along with packaged PCB.

To fully assess the impact of wire bonding on system performance, a full EM simulation was

conducted using HFSS, as illustrated in Fig. 5.23. To minimize the inductive effects of wire bonds, mimic the CPWG effect, and reduce loss and reflection, three wire bonds were used for RF performance. A single signal wire bond was employed for signal transmission, while two ground wire bonds provided RF shielding.

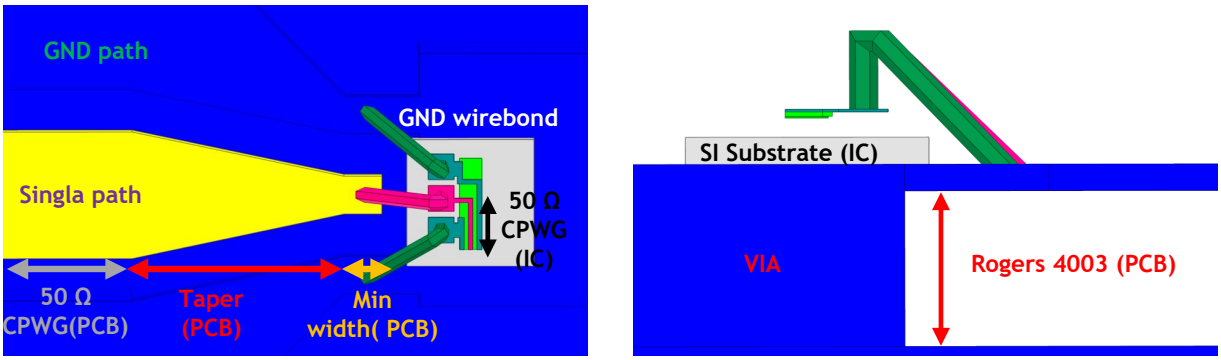


Figure 5.23: Full EM Simulation Setup for Wire Bond Analysis.

The full EM simulation of the wire bond effect, including the CPWG and taper transition from the PCB side to the RF pad, is shown in Fig. 5.24. The simulation results indicate that the losses associated with the wire bond and CPWG on the PCB remain below 4 dB across the entire frequency range from DC to 20 GHz.

The remainder of this section presents the measurement results for various blocks within the system.

5.3.1 K Band Regenerative Divider Measurement Results

Two different input sources were used to evaluate the performance of the first frequency divider. The first was a continuous-wave RF signal generated using a Keysight E8257D signal generator. Additionally, a Rohde and Schwarz FSWP50 signal source was used due to its superior phase noise performance. One output was terminated with an off-chip 50 Ω load, while the other was connected to a Keysight N9030A PXA spectrum analyzer for signal analysis and a Rohde and Schwarz FSWP50 for phase noise measurement.

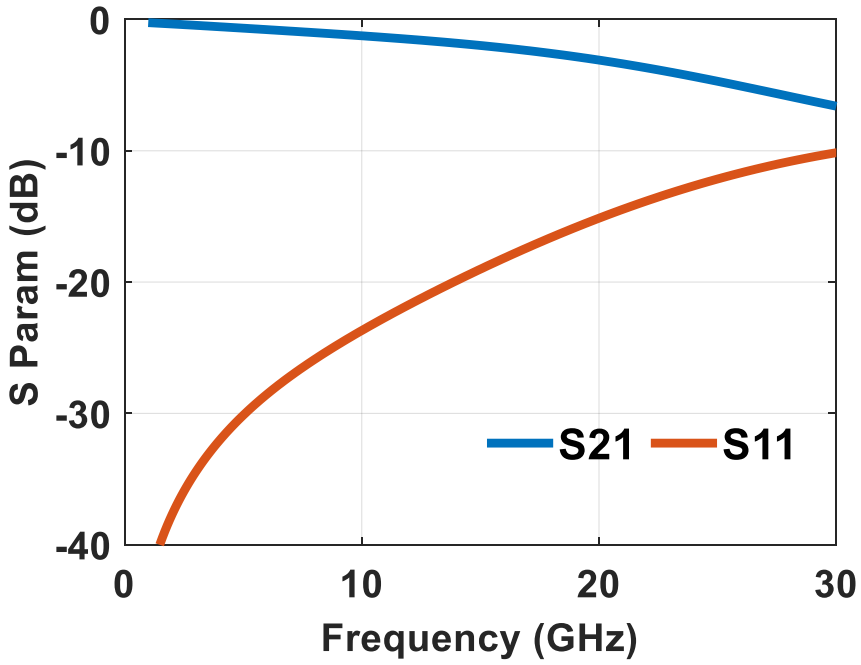


Figure 5.24: Full EM Simulation Results of Wire Bonds and CPWG Transmission Line on PCB, Including RF Pads in IC side.

The output spectrum of the K-band frequency divider is shown in Fig. 5.25(a), measured at an input power of -6 dBm for various center frequencies. The measurement results of the fabricated divider demonstrate an output power exceeding -17 dBm and a fundamental rejection greater than 9 dB. In order to increase the output power of regenerative divider, one approach is to increase the current tail of the mixer or raise the bias voltage of the output buffer, as demonstrated in Fig. 5.25(b). However, higher output power comes with trade-offs, including increased power consumption and phase noise.

The output phase noise of the frequency divider at different carrier frequencies, using a Keysight signal source as the input, is shown in Fig. 5.26. As illustrated in the plot, the frequency divider follows an approximate 6 dB phase noise reduction across various center frequencies, demonstrating that the additive phase noise of the divider remains well below the noise of the input source.

Furthermore, to validate the phase noise performance, an R and S signal source was used to drive the synthesizer and evaluate phase noise across different center frequencies. As shown in Fig.

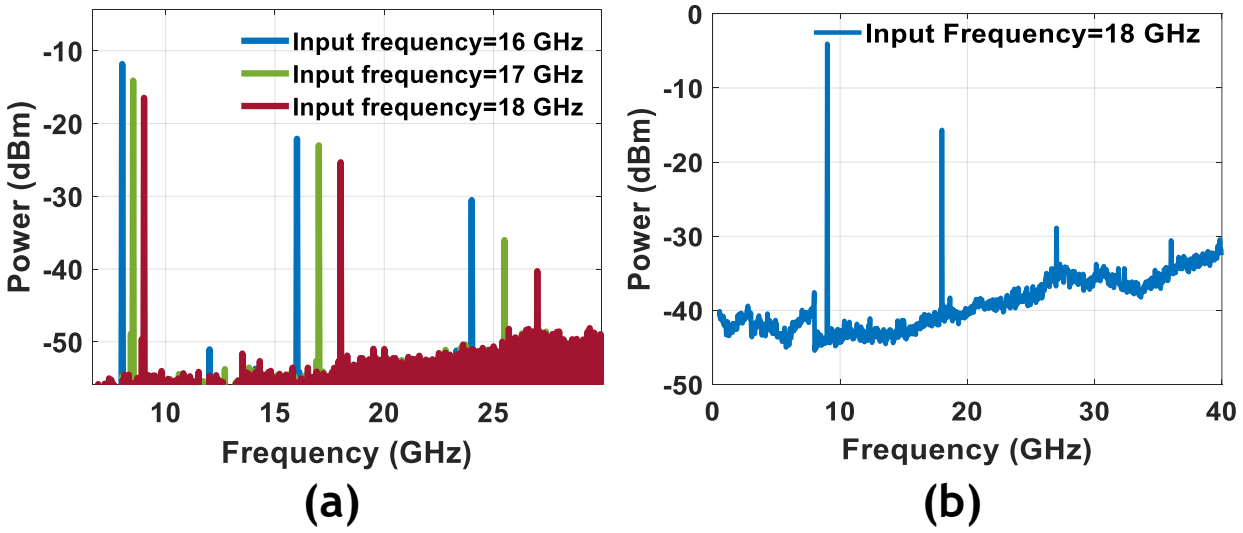


Figure 5.25: (a) The output spectrum of K band frequencydivider versus different frequency(b) Effect of Increasing Bias Voltage on Buffer and Mixer for High Output Power Generation.

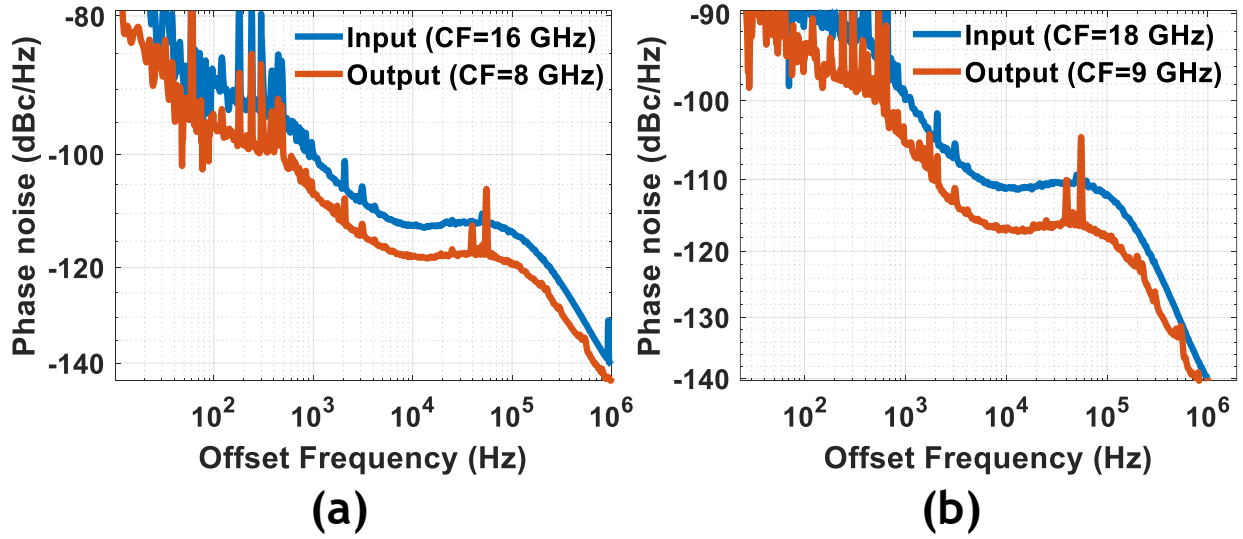


Figure 5.26: The input and output phase noise of the regenerative divider when using a Keysight signal source for 16 and 18 GHz input frequencies.

5.27, the divider maintains an 6 dB phase noise reduction for offset frequencies above 1 kHz, confirming its effective noise performance.

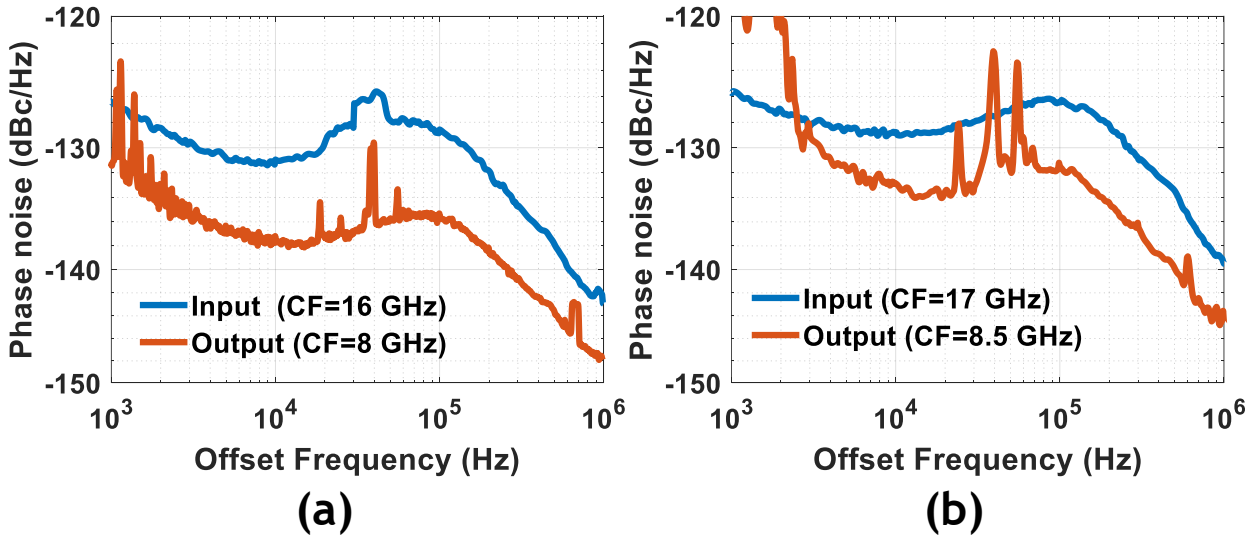


Figure 5.27: The input and output phase noise of the regenerative divider when using R and S signal source for 16 and 17 GHz input frequencies.

5.3.2 Dual Mode Regenerative Divider Measurement Results

The differential outputs of the variable regenerative divider were similarly connected to Mini-Circuits Bias-Tees. One output was terminated with a 50 Ω load, while the other was connected to the Keysight N9030A PXA spectrum analyzer for signal analysis and the Rohde and Schwarz FSWP50 for phase noise measurement.

The output spectrum of the variable divider configured in the divide-by-four mode is presented in Fig. 5.28(a) for different carrier frequencies. In this mode, the divider achieves an output power greater than -18 dBm and spurious rejection of more than 9 dB. Similarly, the output spectrum of the variable divider in the divide-by-six mode is depicted in Fig. 5.28(b), demonstrating an output power of more than -7 dBm and a spurious rejection exceeding 10 dB.

The measurement result for the output spectrum at 16 GHz input frequency is presented in Fig. 5.29. The results confirm effective division, with output powers of -7.3 dBm and -3.4 dBm, respectively.

To further evaluate the effectiveness of the proposed method for varying the dividing ratio of the

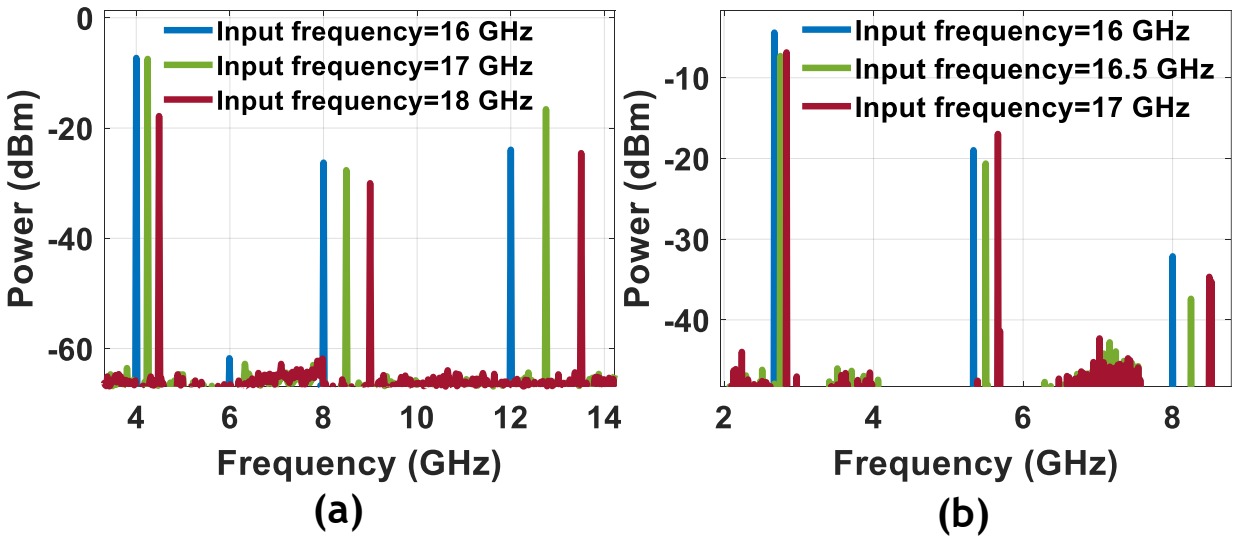


Figure 5.28: The output spectrum of dual band frequencydivider versus different frequencyin (a) Divide by four mode (b) Divide by Six mode.

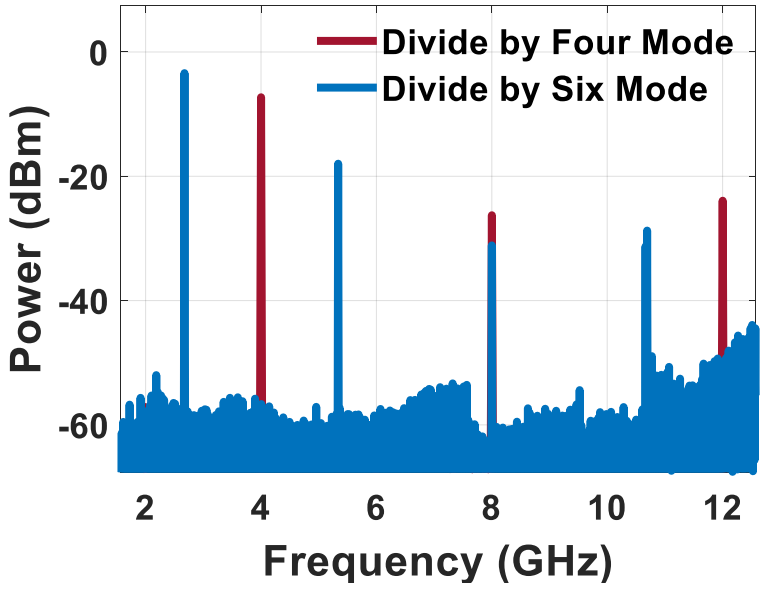
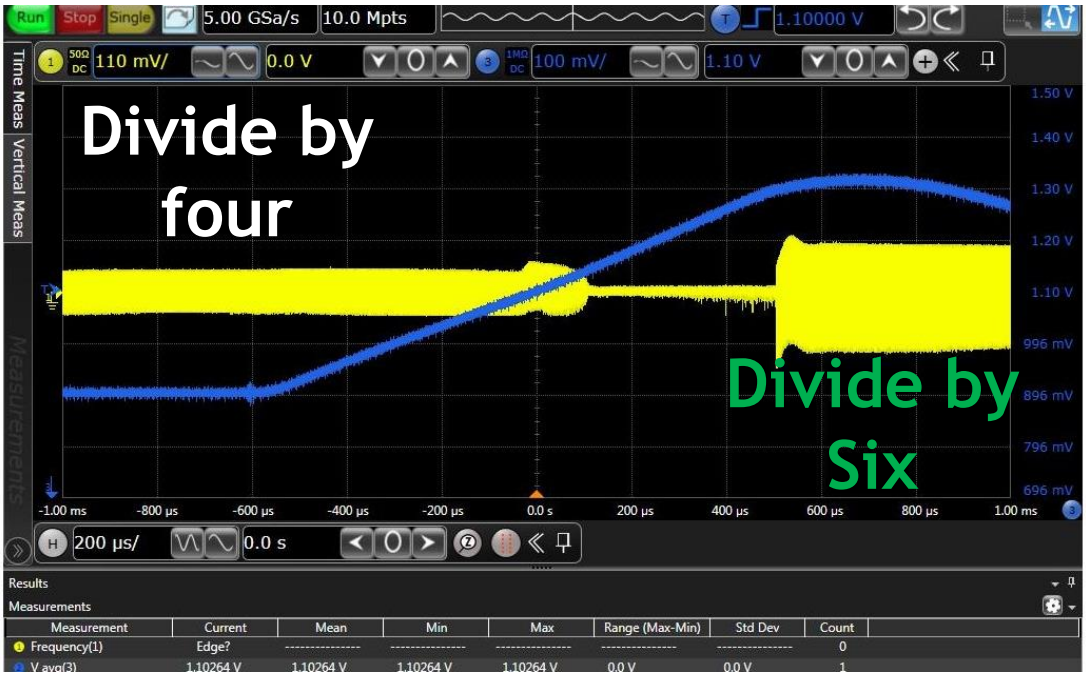


Figure 5.29: Output spectrum measurement results of dual-mode divider.

divider, transient measurements are presented in Fig.5.30. The results illustrate the conversion between divide-by-six and divide-by-four modes, and vice versa, demonstrating the divider's capability to switch between different division ratios.



(a)

(b)

Figure 5.30: Transient response of divider while switching the voltage.

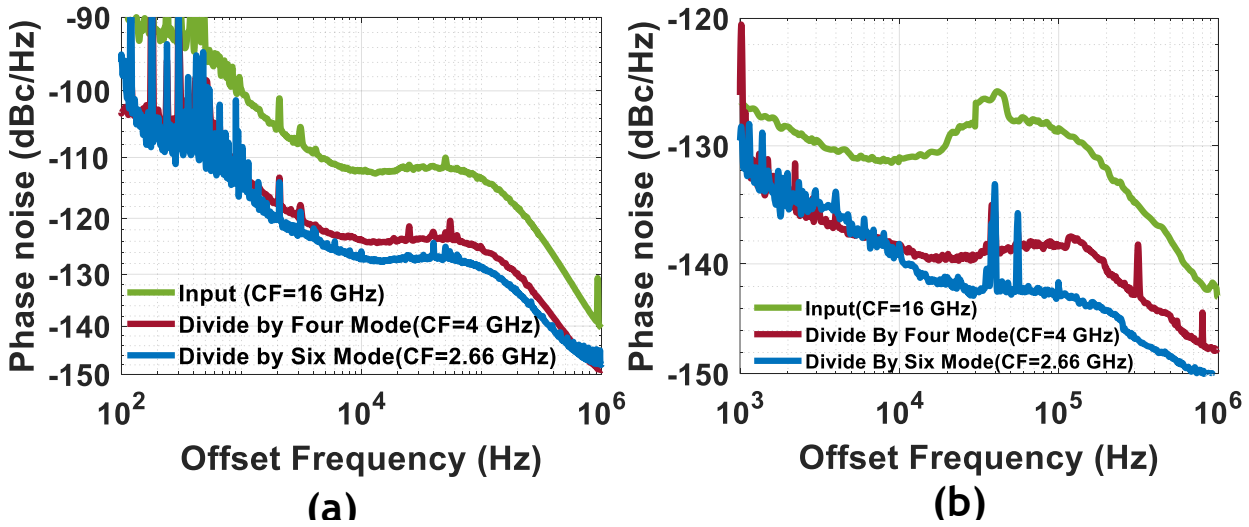


Figure 5.31: Phase noise results of dual mode divide using (a) Keysight source. (b) PNA signal source.

The measurement results for phase noise of the dual-mode divider using Keysight and R & S as input sources are presented in Fig. 5.31(a) and (b), respectively (Input= 16 GHz). The results show phase noise reductions of approximately 12 dB and 15.6 dB for the divide-by-four and divide-by-six modes compared to the input while using Keysight and approximately 10 dB and 14 dB for the divide-by-four and six compared to the input at 100 kHz offset while using R &S signal source.

5.3.3 Static Divider and DDS Measurement Results

The output of the static dividers was connected to an off-chip Mini-Circuits amplifier to boost the signal power for driving the Analog Devices DDS, with the other output terminated to an off-chip 50 Ω load. The Analog Devices DDS output was used to drive an RF Lambda COTS hybrid coupler, generating 0 and 90 degree phase signals required for IF quadrature signal generation.

The output spectrum of the static divider and the DDS driven by static divider is shown in Fig. 5.32(a) and (b) respectively.

The measured phase noise performance of the static divider and DDS is plotted in Fig. 5.33(a) and (b). The results show that the static divider achieves a phase noise lower than -139 dBc/Hz, while

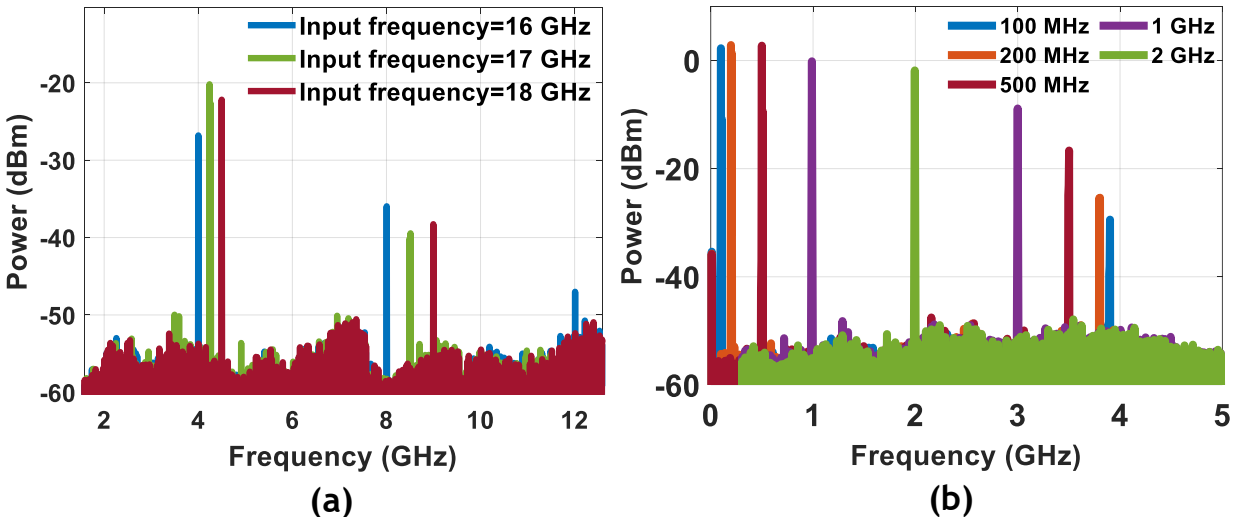


Figure 5.32: (a) Output Spectrum of static divider for various input frequencies (b) Output spectrum of DDS while driven by static divider

the DDS achieves a phase noise lower than -146 dBc/Hz at a 10 kHz offset from 4 GHz and 0.5 GHz carrier frequencies, respectively.

5.3.4 MUX Measurement Results

As mentioned earlier in this chapter, an effective way to extend the synthesizer's bandwidth is by generating different LO frequencies for the final mixing stage with the DDS output. However, the presence of multiple LO frequencies introduces spurious signals at the mixer output. As a result, the role of the MUX becomes even more critical in effectively suppressing unwanted LO frequencies and ensuring a clean output signal. To evaluate the effectiveness of the MUX in suppressing unwanted LO signals, the synthesizer's output was measured with the DDS frequency set to DC. This configuration ensures that the final output does not contain any mixing products or generated image signals, allowing for a clear assessment of the MUX's suppression capabilities.

The output spectrum for all four different cases is plotted in Fig. 5.34(a) and (b), respectively, where the MUX is set to pass divide-by-two and divide-by-four modes.

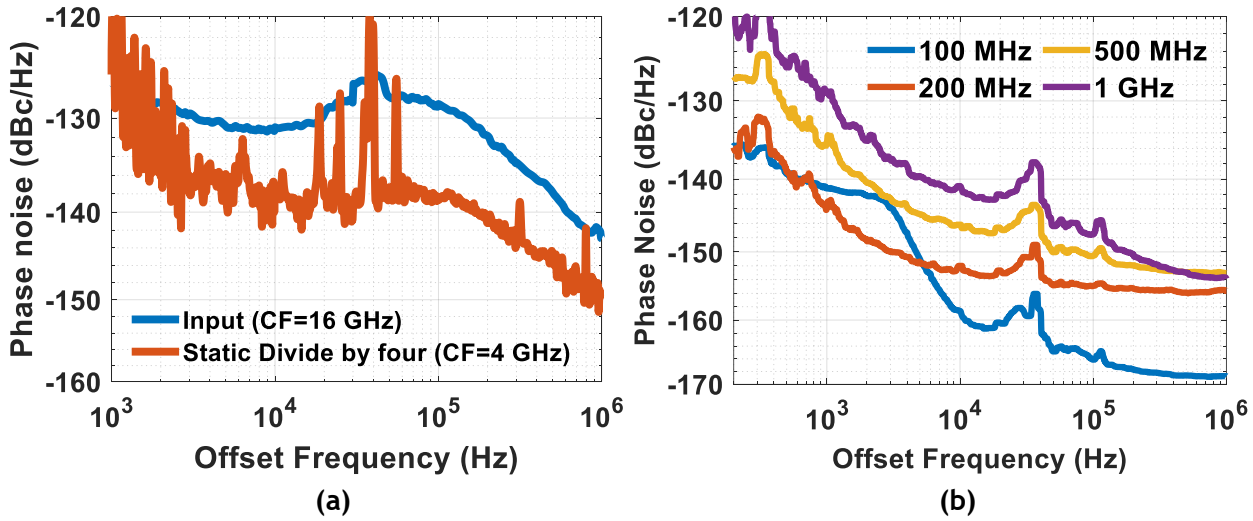


Figure 5.33: (a) Phase noise result of static divider while driven by PNA source when the input frequency is set to 16 GHz. (b) Phase noise result of DDS while driven by static divider input frequency is set to 16 GHz.

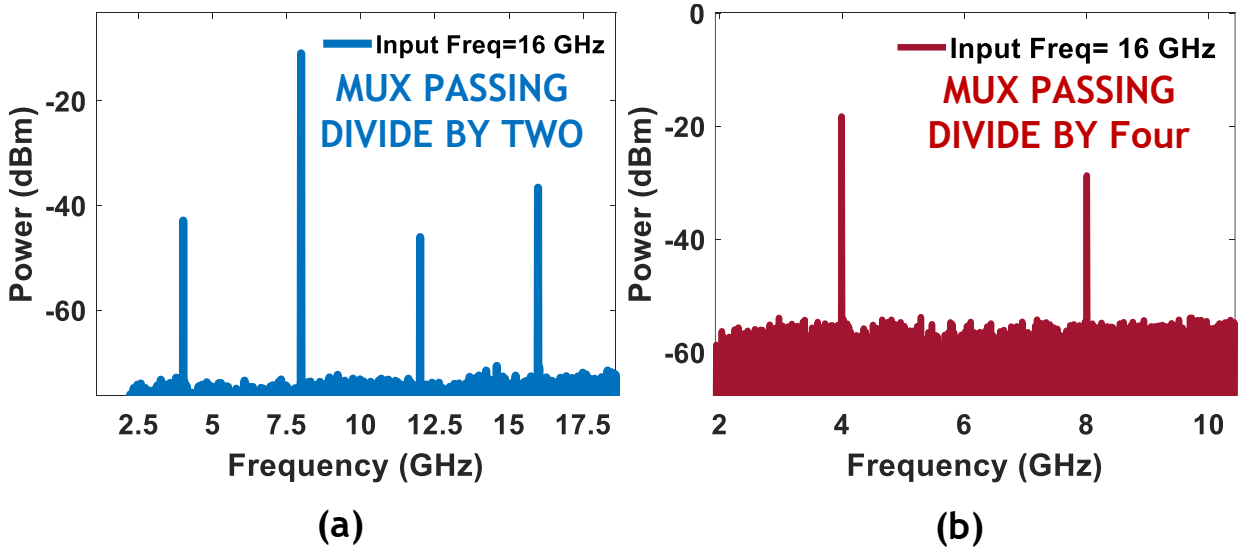


Figure 5.34: The final output spectrum when the IF frequencyis set to zero in: (a) MUX passing divide by two (b) MUX passing divide by four

5.3.5 Final Output Measurement Results of the Synthesizer

The measurement results of final synthesized output spectrum for various LO frequencies are shown in Fig. 5.35(a) to (d), with an input frequency of 16 GHz and an input power of -6 dBm. The Analog Devices DDS, followed by a hybrid coupler, generates the IF frequencies required for single-sideband mixing. Each figure represents a specific LO frequency with two different IF frequencies: one for the upper sideband and the other showing the lower sideband, showcasing the effectiveness of single sideband mixing on surpassing the unwanted image.

The synthesizer's final output is shown in Fig.5.35(a), with the MUXs passing the divide-by-two signal (8 GHz) to the output for mixing with the DDS output, and the variable divider configured in divide-by-four mode. When the IF frequency is set to 1.25 GHz and the upper sideband is selected, the output power is -4.3 dBm, with unwanted image rejection and LO feedthrough measured at -14.1 dBc and -25.2 dBc, respectively. Alternatively, when the IF frequency is set to 0.6 GHz and the lower sideband is selected, the output power increases to -2.5 dBm, while the unwanted image rejection and LO feedthrough improve to -21.2 dBc and -27.2 dBc, respectively.

The synthesizer's final output, with the variable divider operating in divide-by-six mode and the divide-by-three output (CF = 5.33 GHz) selected through the MUX, is shown in Fig.5.35(b). When the IF is 0.3 GHz and the lower sideband is selected the output power is -15.1 dBm while the unwanted image rejection, LO feedthrough are measured at -12.5 dBc and -26.5 dBc, respectively. Meanwhile, when the IF is 0.75 GHz and the upper sideband is selected, the output power is -16.4 dBm, with unwanted image rejection and LO feedthrough at -13 and -22.1 dBc, respectively.

When the variable divider is configured to divide by four and the LO output is set to 4 GHz, the output spectrum is shown in Fig.5.35(c). For an IF frequency of 1 GHz and upper sideband, the output power is -6.8 dBm and image rejection and Lo feedthrough are -23.9 dBc and -27.6, respectively. For the lower side band and an IF frequency of 0.6 GHz the output power drops to -8.6 dBm, while the image rejection and LO feedthrough are measured at -6.3 and -34.1 dBc.

Fig. 5.35(d) illustrates the output spectrum when the divide-by-six mode is selected for the LO

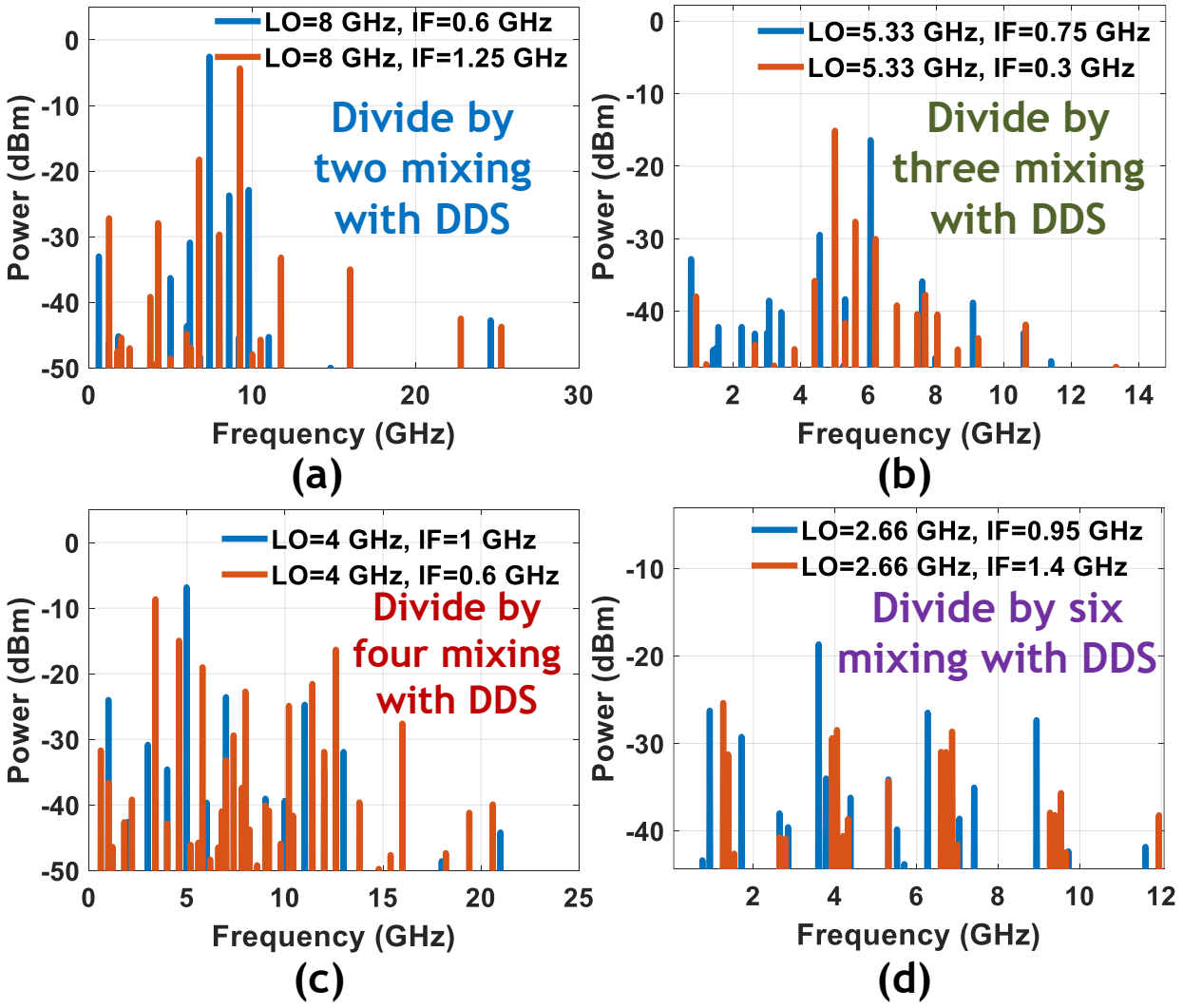


Figure 5.35: The measured spectrum for various LO Frequency for both lower and upper sideband. LO Freq: (a) 8 GHz (b) 5.33 GHz (c) 4 GHz (d) 2.66 GHz.

(CF=2.66 GHz). When the IF is 0.95 GHz and the higher side band is selected the output power is -18.6 dBm while the unwanted image rejection, LO feedthrough are measured at -10.6 dBc and -19.4 dBc, respectively. Meanwhile, when the IF is 1.4 GHz and the lower sideband is selected, the output power is -24.9 dBm, with unwanted image rejection and LO feedthrough at -4.8 and -15 dBc, respectively. respectively.

The synthesizer output power is shown in Fig.5.36. The output power for a specific LO frequency

exhibits less than 10.3 dB variation, with the minimum occurring near the lowest and highest frequencies generated by the DDS. The lower cutoff is attributed to the limitations of the on-chip active balun and COTS hybrid coupler, while the reduction at the higher end is due to the limited output power of the DDS near the Nyquist limit.

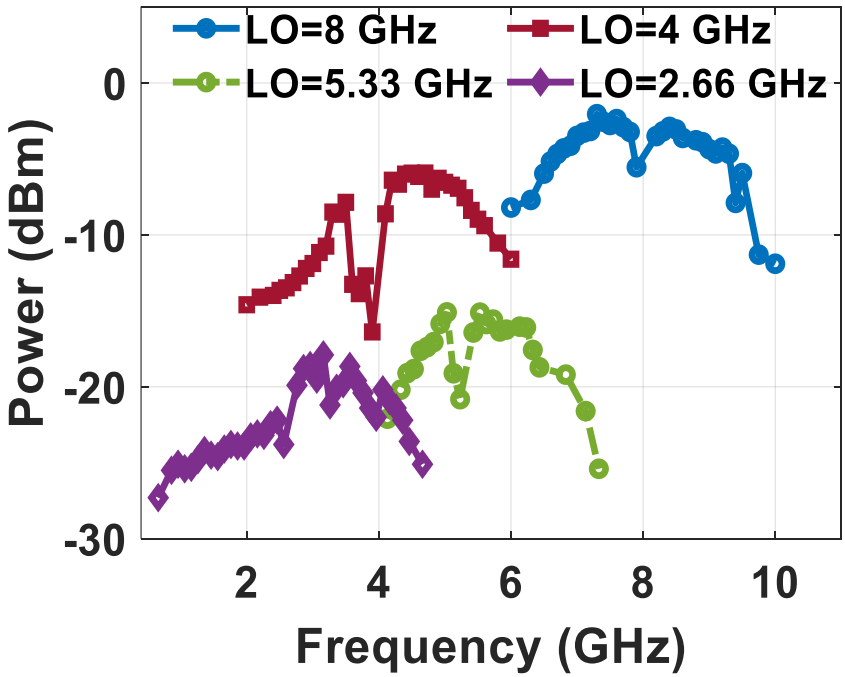


Figure 5.36: Power versus different synthesis frequencies. The power, along with a specific LO, exhibit the same performance. The minimum of the power happens at the maximum and minimum of the DDS output Frequency, which corresponds to the output power of the DDS drops at near Nyquist limit, and the other one due to the lower limit of the Hybrid Coupler.

The synthesizer's phase noise performance is shown in Fig.5.37(a) and (b) for LO frequencies of 8 GHz and 2.66 GHz, respectively, across multiple IF frequencies where the Keysight signal generator is used. The plots include the absolute phase noise of the divide-by-two and divide-by-six stages, as well as the input stage. The phase noise performance of the divide-by-two and divide-by-six stages demonstrate approximately 6 dB and 15.5 dB reductions relative to the input source, respectively.

Furthermore, the phase noise performance of the synthesizer output across multiple IF frequencies,

closely follows the phase noise of dividers across a wide range of offset frequencies, highlighting that the primary limitation in both cases originates from the input source. In both cases, the final synthesized output phase noise remains limited by the phase noise of the input source.

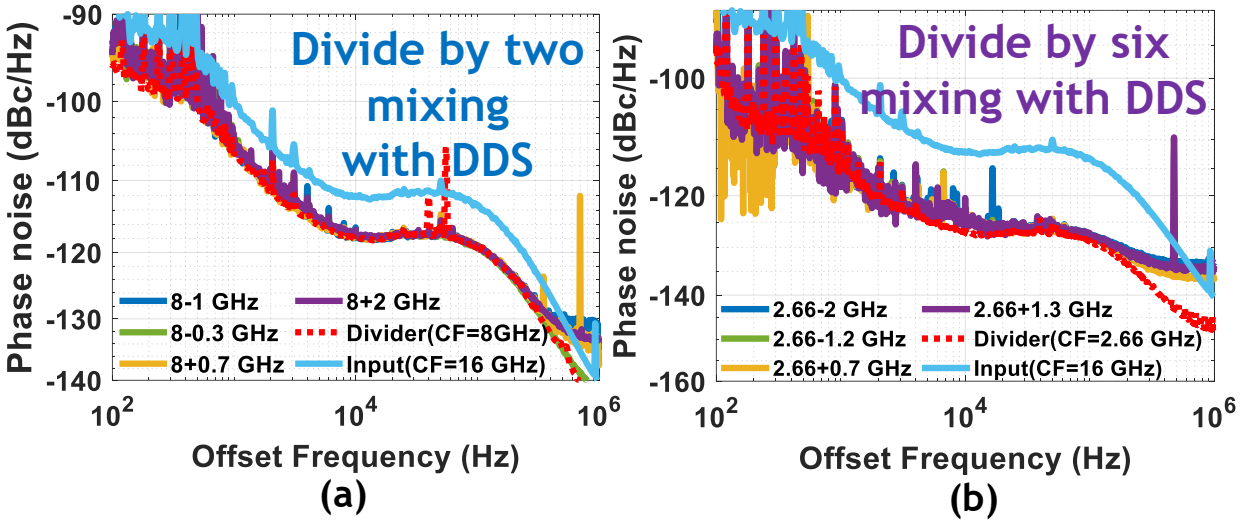


Figure 5.37: Phase noise performance of the synthesized output while LO frequency of: (a) 8 GHz and (b)2.66 GHz for multiple IF frequencies along with absolute phase noise of divide by two and sixth and input stage.

The synthesizer's phase noise performance is shown in Fig. 5.38(a) and (b) for LO frequencies of 8 GHz and 4 GHz across multiple IF frequencies. The plots include the absolute phase noise of the divide-by-two and divide-by-four dividers, along with the input signal. The phase noise performance of the dividers demonstrates an approximate 6 dB reduction for the divide-by-two divider and a 10 dB reduction for the divide-by-four divider at a 100 kHz offset frequency.

The phase noise performance of the synthesizer using a Keysight source across different synthesized frequencies is plotted in Fig. 5.39(a). The results show that for the same LO frequency, the phase noise remains consistent, with variations of less than 3.5 dB. The worst phase noise occurs at the maximum frequency generated by the DDS, as it approaches the Nyquist limit. Moreover, the phase noise of the synthesizer while using the PNA source is plotted in Fig.5.39(b) and the synthesizer shows almost similar performance with a few dB variation at a set LO frequency.

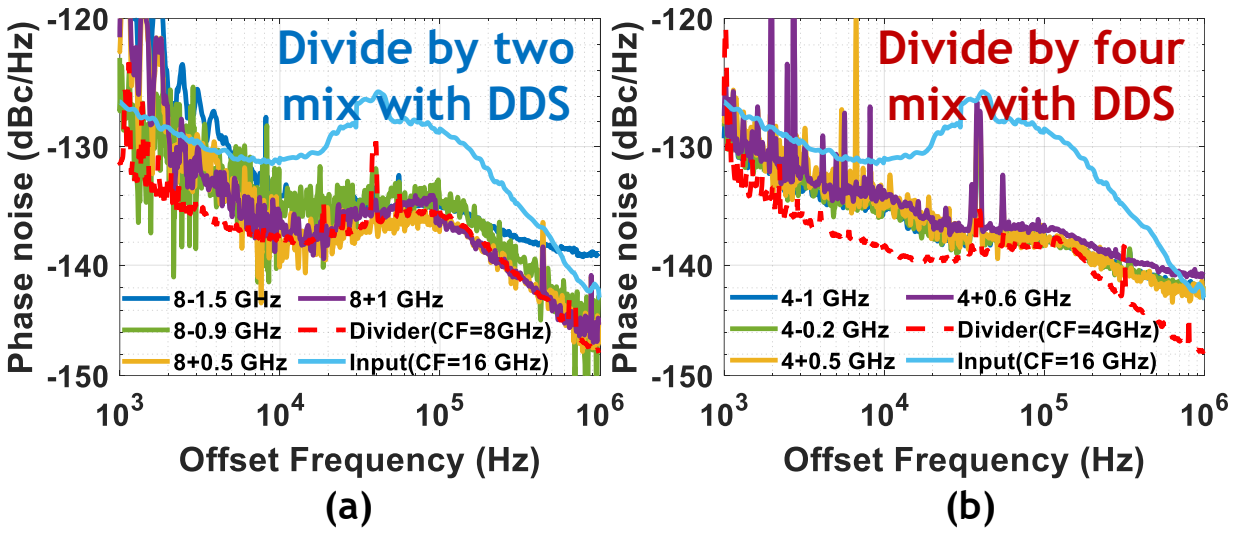


Figure 5.38: Phase noise measurement of the synthesized output with LO frequency of: (a) 8 GHz and (b) 4 GHz for multiple IF frequencies along with absolute phase noise of divide by two and four and input.

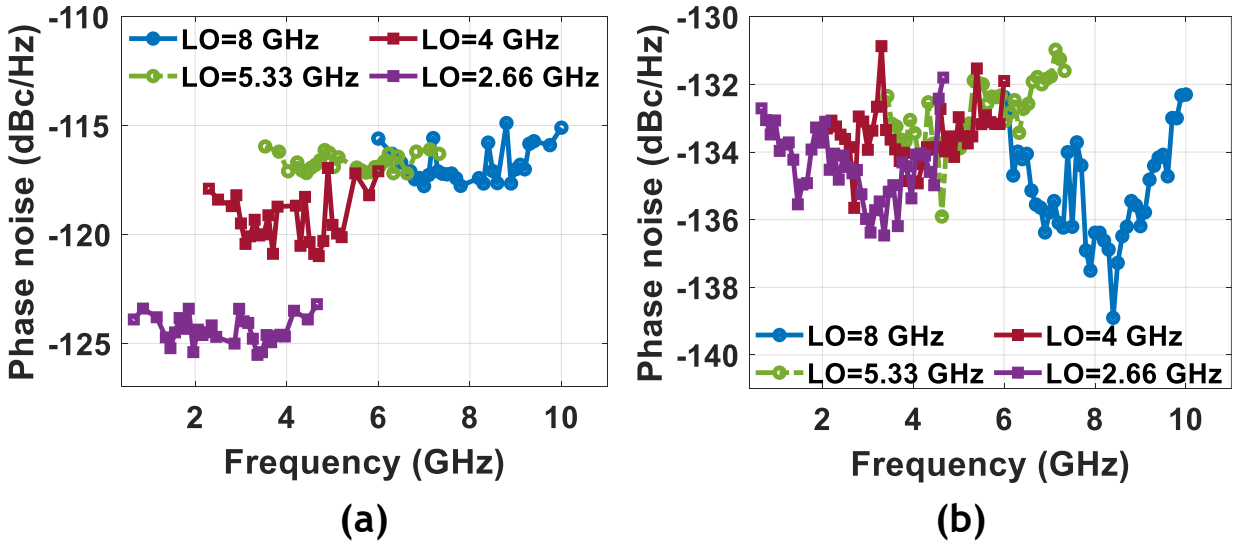


Figure 5.39: Measurement of phase noise at 10 kHz offset versus different synthesis frequencies. (a) Using Keysight Siggen (b) Using Rohde and Schwarz PNA

5.3.6 Measurement Results for Dual DDS Implementation

Although the proposed method of using a single DDS coupled with a hybrid coupler offers the advantage of lower DC power consumption, it comes with trade-offs, including bandwidth limita-

tions of the coupler and phase imbalance between its two outputs. Furthermore, since the input of the on-chip active balun is wire-bonded to the PCB, asymmetries in the wire bonds, on-chip transmission lines, and PCB traces, along with the phase imbalance of the active balun, may introduce variations in the 90-degree phase difference. These deviations can lead to reduced image rejection in the system.

To address this issue and enable frequency synthesis down to the kHz level, one approach is to use two DDS systems simultaneously clocked by the output of a static divider. This method allows for ultra-low-frequency synthesis at each LO frequency while providing accurate phase adjustment, at the cost of higher DC power consumption.

To investigate the sensitivity of image rejection to input phase variations, measurements were conducted using two DDS systems while continuously shifting their phases for a fixed LO frequency of 8 GHz and an IF frequency of 1.1 GHz, as shown in Fig.5.40(a) and (b).

The upper sideband image rejection varies between 14 dB and 26 dB across a 30-degree phase shift, reaching a maximum of 26.2 dB at an 85-degree phase shift between the two inputs. Similarly, the lower sideband image rejection ranges from 9 dB to 19 dB across a 25-degree phase shift, achieving a maximum rejection of 19.1 dB at 273 degrees.

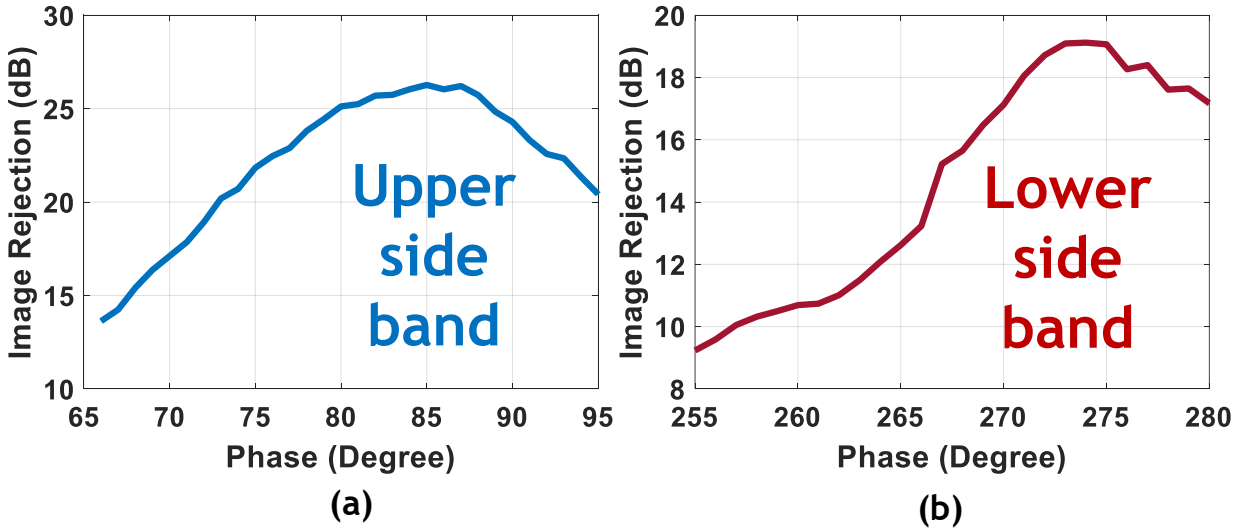


Figure 5.40: Measurement of dual DDS with fixed LO and IF frequencies for (a) Upper side band (b) Lower side band.

Table 5.1: Table of comparison of IC synthesizer

	Nature Electronic 24[2]	CLEO23[1]	MPW14 [126]	CICC23[128]	ISSCC24[129]	This Work
Type	DDS	DDS	DDS	PLL	PLL	DDS
Technology(nm)	COTS	COTS	COTS	65	65	BiCMOS 90 (COTS DDS)
Reference Frequency (GHz)	10	10	10	0.1	0.1	16
Frequency Range (GHz)	8-12	8-12	9.5-10.5	10.3-11.1	5.6-7.8	0.66-10
Output Frequency (GHz)	10.5	8-12	9.5	10.6	6.6	8.5
DC Power Consumption(mW)	NA	NA	NA	242	16.4	949#
Output Power (dBm)	-2$	NA	-11€	-13$	1$	-3
Phase noise @10kHz (dBc/Hz)	-150	-140*$	-140$	-108$	-109	-139*

∗ Limited by input source. $ Graphically estimated from plot. # Core power consumption (Excluding COTS). €Graphically estimated at 9.7 GHz.

5.3.7 Phase Noise Comparison

A comparison of the fabricated synthesizer with other DDS and PLL frequency synthesizers [126–129], is presented in Table 5.1. The synthesizer demonstrates a broader operation range and generates comparable or better output power. Additionally, the measured phase noise performance of the synthesizer outperforms other PLL-based and integrated synthesizers. The phase noise performance of the implemented synthesizer, compared to state-of-the-art systems, is illustrated in Fig. 5.41(a). While its phase noise is slightly higher by a few dB, the synthesizer still outperforms commercially available PLL chips by several orders of magnitude in phase noise performance.

However, its overall performance is limited by the input source, and further improvements could be achieved using a hybrid synthesizer.

Additionally, a comparison with other academic synthesizers in terms of phase noise and tunability is shown in Fig. 5.41(b). The results demonstrate that the proposed synthesizer achieves over 170% tunability while maintaining ultra-low phase noise performance.

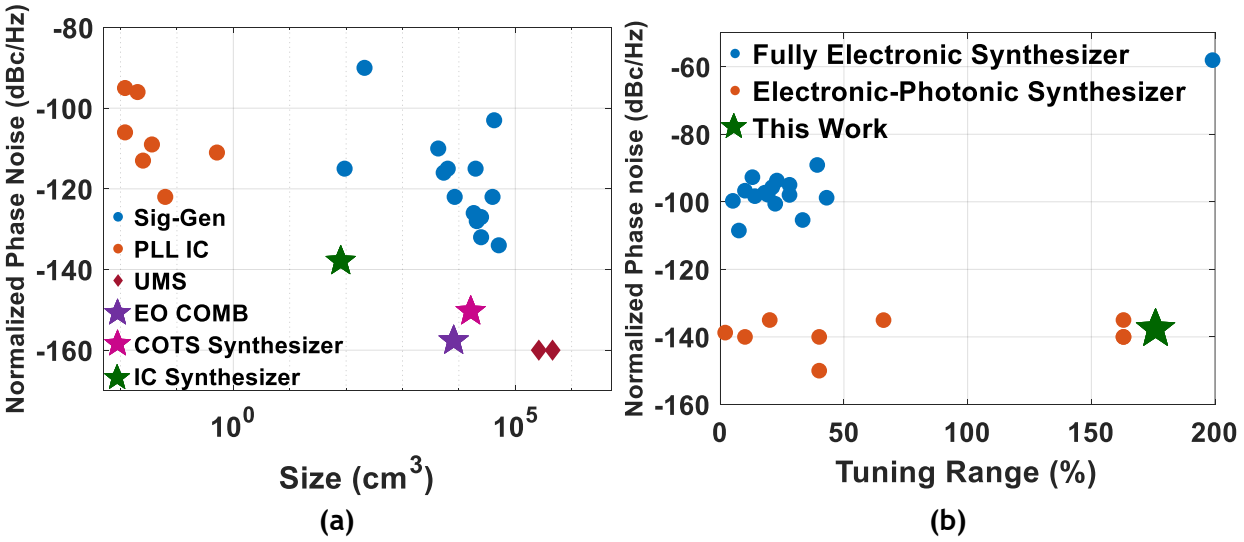


Figure 5.41: (a) Comparison between phase noise of best electronic and photonic systems and IC synthesizer. (b) Comparison between tunability and phase noise of best electronic and photonic synthesizer.

5.4 Conclusion

This chapter presents a broadband, low-phase-noise frequency synthesizer implemented in a SiGe BiCMOS 9HP process. The fabricated synthesizer integrates multiple techniques for LO generation to achieve a broad operational range, along with a DDS for ultra-low-phase-noise performance. The synthesizer achieves a phase noise of -139 dBc/Hz at a 10 kHz offset from an 8.5 GHz carrier, delivers an output power of -3 dBm, and consumes 949 mW of DC power.

As mentioned before the primary limitation in phase noise arises from the input source, showcasing improvement by employing a source with lower phase noise. The presented results with

integration of all blocks on a single chip facilitates advancements in low-phase-noise, broadband signal generation.

5.5 Contribution

This work was done in collaboration with Samin Hanifi and Shadrach Sarpong. I would like to thank them for following contribution:

- Samin Hanifi contributed to the schematic and layout design of the static divider and transformer, provided system-level schematic and layout support, and offered valuable technical insights.
- Shadrach Sarpong for schematic and layout design of final mixer and helpful technical discussion.

5.5.1 Publications

- **P. Shirmohammadi**, S. Hanifi, S. Sarpong, T.N. Blalock and S.M. Bowers "A Broadband 0.66 -10 GHz Low Phase Noise DDS-Based Frequency Synthesizer," to be submitted to *IEEE Transactions on Microwave Theory and Techniques (TMTT)*.

Chapter 6

Conclusion and Future Work

6.1 Dissertation Conclusions

Oscillators are at the heart of every radar and communication system, and their spectral purity sets the limit for achievable system performance. As a result, low noise microwave signals with high timing stability are a critical enabler of modern science and multiple technologies of broad impact. Positioning and navigation, advanced communications, high-fidelity radar and sensing, and high-performance atomic clocks are all dependent upon low-phase noise microwave signals. Currently, photonically derived microwave signals can achieve phase noise and timing stability superior to electronic sources. However, many applications require precise microwave frequency tuning, and the absence of this capability in photonic systems restricts their applicability. On the other hand, a fully electronic approach is not capable of delivering a widely and continuously tunable and low phase noise source, which is essential for many emerging applications requiring a broad frequency range (e.g., wideband radars and wideband communication systems) while maintaining low phase noise. Fully electronic synthesizers typically rely on a phase-locked loop (PLL) architecture, which inherently limits the achievable phase noise using this approach.

This dissertation focuses on the challenges of generating low-phase-noise microwave signals

and proposes and implements design techniques to achieve ultra-low-phase-noise, widely tunable signals.

- A DDS-based optically driven synthesizer is proposed and implemented to achieve ultra-low phase noise performance in the X-band frequency range. While typical photonic systems offer ultra-low phase noise, they are limited in tunability. Conversely, DDS-based frequency synthesizers generate low-phase-noise signals but suffer from low output frequency, limited tuning bandwidth, and high spurious signals. This dissertation proposes a hybrid frequency synthesizer in which the DDS is clocked using a clean, photonic-generated signal, leading to a significant improvement in tunable phase noise generation. The implementation of the proposed method demonstrated a substantial enhancement in tuning range, with up to a 10 dB improvement in phase noise compared to previous works.

- A chip-scale solution for ultra-broadband tunability is proposed to reduce the size of the tunable system and achieve an ultra-compact form factor while increasing tunability by more than 200 $\%$ compared to COTs synthesizers. To extend the bandwidth of the generated signal, multiple cascaded frequency dividers were designed and implemented, providing additional LO frequencies for single-sideband mixing with the DDS, thereby achieving a broader operational range. An implementation of the proposed idea is shown in Chapter 5, where a wide band frequency synthesizer is designed to achieve more than 9.3 GHz tuning range with lower than -130 dBc/Hz phase noise in the entire range of operation.

- A dual-mode regenerative divider is proposed and implemented to minimize the need for multiple frequency dividers in the loop, reduce DC power consumption, and achieve a compact form factor. The proposed divider usees an amplifier that can also function as a multiplier, enabling both divide-by-two and divide-by-three operations. An implementation of this technique is presented in Chapter 5, demonstrating divide-by-four and divide-by-six modes with more than -10 dBm output power at each mode and a phase noise reduction proportional to the division ratio.

- A single-inductor footprint transformer-based quadrature signal generation technique is proposed to enhance spur rejection in DDS-based systems. While DDS-based synthesizers can achieve ultra-low phase noise, their bandwidth is inherently limited. To extend the bandwidth, mixers are commonly used; however, they introduce high spurs due to their inherent non-linearity. To mitigate these unwanted spurs, single-sideband mixing is required, which necessitates on-chip quadrature-phase signal generation. This dissertation proposes and implements a wideband quadrature signal generation technique, as presented in Chapter 5, demonstrating over 9 GHz bandwidth and achieving more than 20 dBc image rejection after mixing.

- Multiple design techniques were explored in this dissertation to reduce the additive phase noise of amplifiers. Parallel amplifiers and feedforward amplifiers are preferred for low-phase-noise amplification; however, they typically suffer from large form factors and poor efficiency. This dissertation proposes and implements a novel feedforward amplifier architecture to minimize the additive noise of amplifiers. A proof-of-concept implementation of this design is presented in Chapter 3, demonstrating that the feedforward scheme reduces the additive phase noise of the core amplifier by more than 7 dB while maintaining an ultra-compact form factor.

Furthermore, an in-depth study of low-phase-noise frequency dividers is presented in Chapter 4, detailing effective methods to reduce power consumption, mitigate startup issues, and enhance phase noise performance. This study provides a foundation for designing low-phase-noise regenerative dividers and explores how different classes of operation impact the additive phase noise of these dividers.

6.2 Future Directions

This dissertation showcases advancements in multiple aspects of low-phase-noise signal generation and tunability. However, challenges and limitations remain that must be addressed to further push

the boundaries of communication systems, radar, and navigation.

6.2.1 Broadening the Tunability of the Synthesizer

Most applications benefit from a broader operational range of low-phase-noise microwave signals. As demonstrated in Chapter 5, multiple frequency dividers can be used to extend the synthesizer's frequency range; however, integrating multiple dividers onto a single chip presents significant challenges. One potential solution is to add additional modes into a dual-mode regenerative divider, though this approach also has its own limitations. Furthermore, extending the operational bandwidth requires increasing the bandwidth of each individual component within the synthesizer, which may introduce greater complexity, higher DC power consumption, and increased noise. Therefore, innovative solutions are needed to achieve a wider operational range while mitigating these trade-offs.

6.2.2 Suppressing Spur Power in Frequency Synthesis

In an ideal world, the output of a frequency synthesizer would be a pure sine wave, free from unwanted harmonics. However, in real-world applications, the non-linearity of components, particularly mixers, generates unwanted spurs, especially in DDS-based frequency synthesizers. Therefore, effective techniques are required to further reduce spur levels.

One possible approach involves on-chip quadrature-phase signal generation with minimal phase and amplitude imbalances. However, achieving a wide frequency range while maintaining low phase imbalance, amplitude imbalance, and conversion loss is highly challenging. Ring oscillators and static dividers are common methods for quadrature signal generation, but each has drawbacks—ring oscillators suffer from additive phase noise, while static dividers require an input frequency twice the desired range. Cascaded passive structures can also be used, but they often introduce high conversion loss, large form factors, or sensitivity to source and load impedance. Consequently, solutions are required to effectively reduce spur levels while overcoming these lim-

itations.

6.3 Other Work

In addition to the work presented in this dissertation, contributions were made to other projects. Specifically, efforts were directed toward developing a low-phase-noise mm-wave regenerative divider. As previously mentioned, the demand for chip-scale solutions for low-phase-noise mm-wave and microwave signal generation has grown, which result in increased research into integrating microcombs, resonators, and SIL lasers on photonic integrated circuits (PICs). This shift enables smaller cavity sizes, leading to higher output frequencies. However, to make these low-phase-noise signals more practical for communication systems, a low-phase-noise frequency divider is necessary to scale down the generated signals to levels suitable for electronic systems. As a result, a low phase noise mm-wave regenerative frequency divider was designed in SiGe BiCMOS process to divide down a clean low phase noise signal generated through optical source.

Personal contribution involves designing a transformer-based balun at D-band with less than 1.5 dB conversion loss and more than 35 GHz bandwidth and an active balun with more than 10 dB gain with more than 70 GHz bandwidth.

The expected publications are listed below:

- S. Hanifi, **P. Shirmohammadi** and S.M. Bowers "Low Phase Noise mm-wave Regenerative Frequency Divider" to be submitted to *IEEE Transactions on Microwave Theory and Techniques (TMTT)*.
- S. Hanifi, **P. Shirmohammadi** and S.M. Bowers "Low Phase Noise Divide by 5 Regenerative Frequency Divider" *Currently being measured*.

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