THERMOELECTRIC TRANSPORT IN TWO DIMENSIONS

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Abstract

As modern electronics shift towards nanoscale, the device performance becomes limited by the increasing dissipated power density. Proper heat management is one of the major challenges in the design of nanoelectronic devices. Thermoelectric devices can pump heat using electrical energy and can be used to cool the chips. They are also used to convert thermal energy into electrical energy and can be used to recycle industrial waste heat into electric power or power wearable electronics.

This dissertation focuses on the characterization of thermoelectric transport in two-dimensional (2D) systems, including Si-based thin films and few-layer 2D materials, and evaluates the strategies to optimize their performance. A thermoreflectance-based method, heat diffusion imaging, is developed to measure the in-plane thermal conductivity of thin films or even few-layer samples supported on a substrate. Enhanced thermoelectric performance has been achieved by adding periodic nano-sized holes to suppress the phonon transport and by doping via surface charge transfer to improve carrier mobility. The thermal conductivity of a holey Si thin film reduces by almost 20 times compared to a high-doped bulk Si sample or Si thin film without holes. P-type doping has been realized in holey Si thin films with organic surface dopants F_4TCNQ, which improves the thermoelectric power factor by two orders of magnitude.

2D transitional metal dichalcogenides (TMDs) are the other material system of interest. They possess a wide range of electronic properties, from insulating to superconducting, depending on their crystalline structures and the topology of their electronic

structure. Their electronic properties are usually superior to their bulk counterparts and can be modified, for instance, by applying an electrostatic back gate bias. In this dissertation, we study the in-plane thermoelectric transport of 4-layer $NbSe_2$ grown by molecular beam epitaxy. It includes the first thermal conductivity measurement in the low-temperature range (below room temperature) reported for a few-layer $NbSe_2$. The charge carriers added by back gate doping are not enough to alter the behavior of the metallic $NbSe_2$, but they can change the resistance of a semiconducting 2H-$MoTe_2$ by one order of magnitude and improve its thermoelectric power factor by up to 89% compared to the intrinsic value. The effects of different metal contacts, i.e., Ti and TiO_x, have been evaluated for WSe_2 in a cross-plane geometry. In general, thermal and electrical contact resistances are particularly important in the design of 2D devices and can change the efficiency of these devices significantly.

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Chapter 1

Introduction

As the development in modern electronics moves towards micro and nanoscales, the dissipated power density keeps increasing, which limits device performance. Heat management is therefore a major challenge in device designs [1]. Thermoelectric devices can pump heat using electrical energy and can be used to take the heat away from the chips. These modules are also used to convert thermal energy into electrical energy and can be used to recycle waste heat into electric power, which is attractive for powering Internet-of-Things (IoT) or wearable electronics [2]. This introduction aims to provide basic background knowledge on thermoelectric materials and discuss strategies to improve their performance, as well as the potential of the two systems of interest – thin films and two-dimensional (2D) transition metal dichalcogenides (TMDs) materials in terms of thermoelectric applications.

1.1 Basics of Thermoelectrics

A thermoelectric device achieves its functions mainly via two effects: the Seebeck effect and the Peltier effect. The Seebeck effect states that if a temperature difference (ΔT) is applied between two points on an electrically-conductive sample, an

open voltage (ΔV) develops between them as charge carriers diffuse from the hot side to the cold side. It is the basis of thermoelectric heat-to-electricity power generators. The Seebeck coefficient S (sometimes referred to as thermopower) is defined as $S = -\Delta V/\Delta T$. The sign of the built-up voltage depends on the majority of charge carriers. The Seebeck coefficient is positive for p-type materials and negative for n-type materials. Thermoelectric modules usually consist of pairs of n-type and p-type thermoelectric elements connected electrically in series and thermally in parallel. The Peltier effect is the reverse of the Seebeck effect: when an electrical current flows through a junction connecting two dissimilar conductors, one material will be cooled and the other will be heated. It is the basis of thermoelectric refrigerators.

The performance of a thermoelectric device is often characterized by its materials' power factor and figure of merit. The thermoelectric power factor is defined as

$$PF = \sigma S^2, \tag{1.1}$$

where σ is the electrical conductivity. Power factor times temperature (PFT) is also often used since it shares the same unit as thermal conductivity. Dividing PFT by the thermal conductivity, k, yields the dimensionless thermoelectric figure of merit,

$$zT = \frac{PF \times T}{k} = \frac{\sigma S^2 T}{k}. \tag{1.2}$$

The efficiency of the thermoelectric power generators and the coefficient of performance of the Peltier refrigerators are increasing functions of zT. High power factor and low thermal conductivity are desirable in high-performance thermoelectric materials.

Thermoelectric devices are solid-state devices with no moving parts, so they are quiet and can operate over an extended period of time. For example, the radioisotope

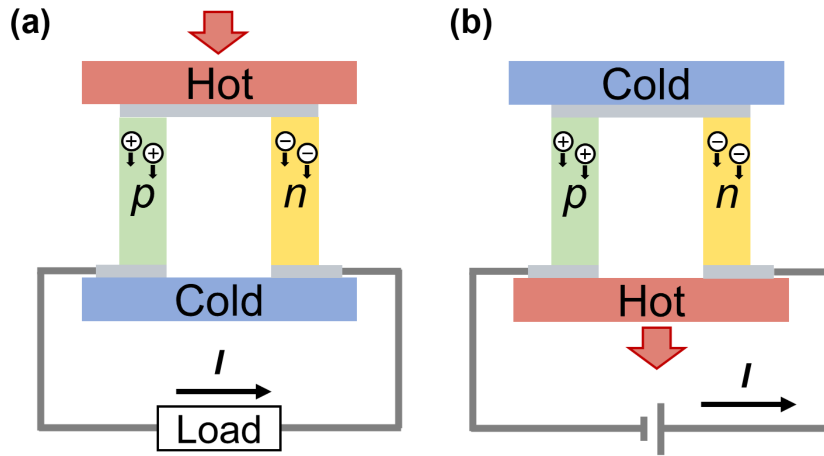

Figure 1.1: Schematics of a thermoelectric module made of p-type and n-type thermoelectric materials, operating in (a) power generation (Seebeck effect) and (b) refrigeration (Peltier effect) modes. In (a), a temperature difference causes the charge carriers to diffuse from the hot side to the cold side, generating a current. In (b), a current is supplied to the circuit and when the charge carriers move under the electric field, they carry the heat energy with them.

thermoelectric generators on the Voyager space crafts have been in service for over 40 years. Thermoelectric modules can be used at extremely small scales (micro size) and at moderately large scales (meters). By controlling the size of each component and the total number of components, they can be used to output kilowatts of power in industrial facilities or mW for nanoelectronics. The limiting factor that prevents thermoelectric devices from more general applications is their efficiency, with the highest obtained value currently at 15% [3]. The maximum efficiency of a thermoelectric generator can be expressed as a function of zT:

$$\eta_{\text{max}} = \frac{\sqrt{1 - zT} - 1}{\sqrt{1 + zT} + \frac{T_C}{T_H}} \cdot \frac{T_H - T_C}{T_H}, \tag{1.3}$$

where T_C and T_H are the cold and the hot side temepratures. Therefore, finding ways to improve zT of existing material systems and evaluating new and promising materials for their thermoelectric performance is of great significance.

1.2 Engineering Towards Better Thermoelectric Performance

Interplay between Transport Parameters

As is suggested by the definition of zT in Eqn. 1.2, enhanced thermoelectric performance comes from two aspects: one is to suppress phonon transport without significantly affecting electrical transport, the other is to obtain higher electrical conductivity or Seebeck coefficient for a higher PF. The former is usually done by structure engineering while the latter is by band engineering. Ideally, the two strategies should be employed in parallel for maximum improvement. The difficulty in designing high-efficiency thermoelectric systems is that these transport properties are interrelated. Tuning one parameter often leads to change in another and oftentimes the changes oppose each other. Efforts have to be made to decouple these properties and to find the balance for the optimized performance.

The electrical conductivity is proportional to the carrier concentration and the mobility and is expressed as

$$\sigma = e(n\mu_e + p\mu_h), \tag{1.4}$$

where e is the elementary charge, n and p are electron and hole concentrations, and μ_e and μ_h are electron and hole mobilities, respectively. Both types of carriers add to the conductivity. However, if both carriers conduct in a material, they will both move to the cold end, canceling out the induced Seebeck voltages. This is the so-called bipolar effect. Only one dominant type of carrier should exist to ensure a large Seebeck coefficient.

High carrier concentrations lead to high electrical conductivity and, at the same time, low Seebeck coefficient, as the Seebeck coefficient is related to the carrier concentration by $S \propto n^{-2/3}$ in metals or degenerate semiconductors. Additionally, the

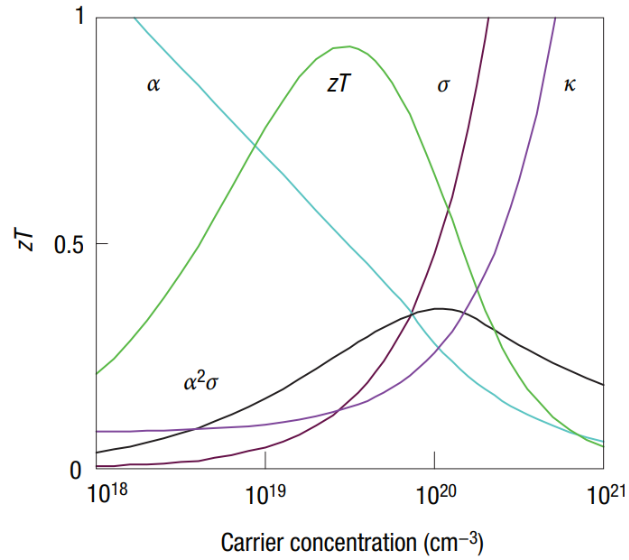

Figure 1.2: zT optimization through comprises from Seebeck coefficient (noted by α in figure), electrical conductivity and thermal conductivity, in the example of Bi_2Te_3 [4]. Good thermoelectrics typically have a carrier concentration of $10^{19} - 10^{21}$ cm^{-3}.

charge carriers also transport heat. The electronic contribution to thermal conductivity in metals and heavily doped semiconductors is governed by the Wiedemann-Franz law and becomes significant at very large carrier concentrations, i.e., at the metallic range. Despite having large electrical conductivities, metals have small Seebeck coefficients, usually on the order of a few μV/K, and large thermal conductivities. Therefore, they are not desirable for thermoelectric applications. Heavily-doped semiconductors [4] or possibly semimetals [5] are the candidates for the best thermoelectric materials. As shown in Fig. 1.2, maximizing zT involves an intricate balance between large Seebeck coefficient, high electrical conductivity, and low thermal conductivity [4]. The complexity of optimizing the interrelated thermoelectric parameters has been discussed extensively in several review papers [4, 6].

Nanostructuring

It has been demonstrated that by using nanostructure features in a material system, it

is possible to manipulate the thermal conductivity without significantly affecting the electrical transport properties. Hence, nanostructuring provides a pathway to manipulate S, σ, and k separately for zT enhancement. The idea is to induce frequent phonon scattering with the added boundaries or interfaces in order to suppress lattice thermal conductivity. Charge carriers usually have mean free paths (MFPs) much shorter than phonons, so they are less affected and the electrical transport properties are mostly preserved. In addition, using lower dimensional samples (e.g. 2D films, 1D nanowires, and 0D quantum dots) results in electron confinement and sharp features in the density of states (DOS) [7–9]. Therefore, it is also possible to alter the band structure to enhance the Seebeck coefficient and thus the power factor [7–9]. Several examples of different nanostructured thermoelectric systems are given in Fig. 1.3.

For bulk materials, one can ball-mill ingots of good thermoelectric materials into nanopowders and then hot-press the powders back into ingots. One of the first demonstrations of this method was the case of nanostructured $Bi_xSb_{2-x}Te_3$ [10]. The thermal conductivity of the nanostructured ingot was reduced by about 20% and its zT increased from 1 to 1.2 at 300 K and 1.4 at 373 K compared to its bulk ingot. The nanograins were on average about $10-50$ nm in size, with some Sb-rich nanodots of below 10 nm. The grain boundaries were randomly distributed and effectively scattered the phonons. The key is to ensure that the grain boundaries do not impede the carrier mobility more than the phonon transport. A previous study on nanostructured Si-Ge alloys showed that the decrease in electrical conductivity could offset the increased phonon scattering depending on the sample quality [11].

Thin films and nanowires are attractive platforms for nanostructuring, considering their already reduced length scales. Besides random structures, periodic structures can also help accomplish the goal. Forming superlattices of dissimilar materials creates periodic structures for phonon scattering and band structure modifications. Creating 3D superlattices, including Bi_2Te_3/Sb_2Te_3 [12], PbTe/PbSe [13], and

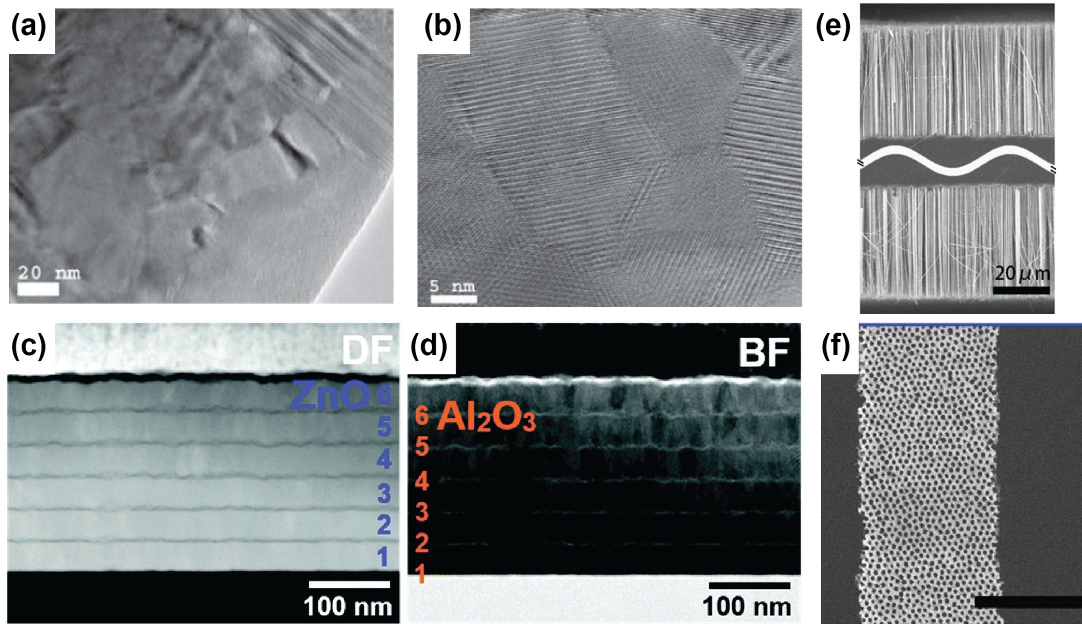

Figure 1.3: Examples of nanostructured thermoelectric materials. Transmission electron microscope (TEM) images of (a) the $Bi_xSb_{2-x}Te_3$ nanograins and (b) a close-up showing high crystallinity and clean grain boundaries [10]. Cross-sectional (c) dark field and (d) bright-field scanning TEM (STEM) images of the 6-cycled Al_2O_3/ZnO thin film [14]. (e) Cross-sectional scanning electron microscope (SEM) images of the Si nanowire arrays with Si substrate sandwiched in the middle [15]. (f) SEM images of holey Si thin film with 55 nm pitch and 23 nm neck size. The scale bar here is 1 μm.

ZnO/Al_2O_3 [14], is effective in reducing the lattice thermal conductivity to values as low as 0.2 $Wm^{-1}K^{-1}$and significantly improves zT to up to 2. High-density and large-area vertically aligned porous silicon nanowire arrays possess a thermal conductivity as low as 1.7 $Wm^{-1}K^{-1}$and a high room temperature zT value of 0.49 [15]. Another concept is to pattern arrays of nano-pores using advanced lithography and etching techniques. By varying the porous configuration in Si membranes, a high room temperature zT of 0.4 was reported [16]. This will be discussed in more details in Section 1.3, when we look at Si-based thermoelectrics.

Alternative Doping Schemes

Most thermoelectric materials are made out of heavily doped semiconductors. Conventional doping techniques insert dopant atoms into the host materials. These dopants introduce strong Coulomb repulsion and reduce carrier mobility.

Modulation doping has been proposed to combat these issues. A typical modulation-doped structure consists of an undoped channel for the mobile carriers, an undoped spacer layer that separates the ionized dopants from the conducting channel, and a doping layer [17]. The carriers then travel along the channel parallel to the interface with high mobility. This idea was first used in transistors. The electron mobility in GaAs, for instance, has been enhanced by 4 orders of magnitudes using AlGaAs at below 10 K [18]. However, in terms of thermoelectric applications, while the thermoelectric power factor can be extremely large [19], one has to deal with an electron gas with a large thermal conductivity. Modulation doping was successfully extended to 3D in nanostructured SiGe bulk samples and improved zT has been shown [17, 20]. The improvement, in that case, was limited due to scattering from irregular grain boundaries and impurities.

Similarly, in surface charge transfer doping, charges exchange across the interface between the surface dopants and the host material due to energy bands misalignment and form space charge layer with high mobility [21, 22]. This concept was first presented to explain the high surface conductivity of intrinsic diamond [23, 24] and was later expanded to dope other materials. Fig. 1.4 shows the band diagrams of p-type surface charge transfer doping on the right-hand side [21]. The surface dopants have unoccupied molecular orbitals (UMOs). Electrons from the valence band maximum (VBM) of the host material are energetically favorable to transfer to the lowest unoccupied molecular orbitals (LUMOs) of the dopants. As a result, the surface dopants become negatively charged and equal numbers of holes accumulate in the valence band

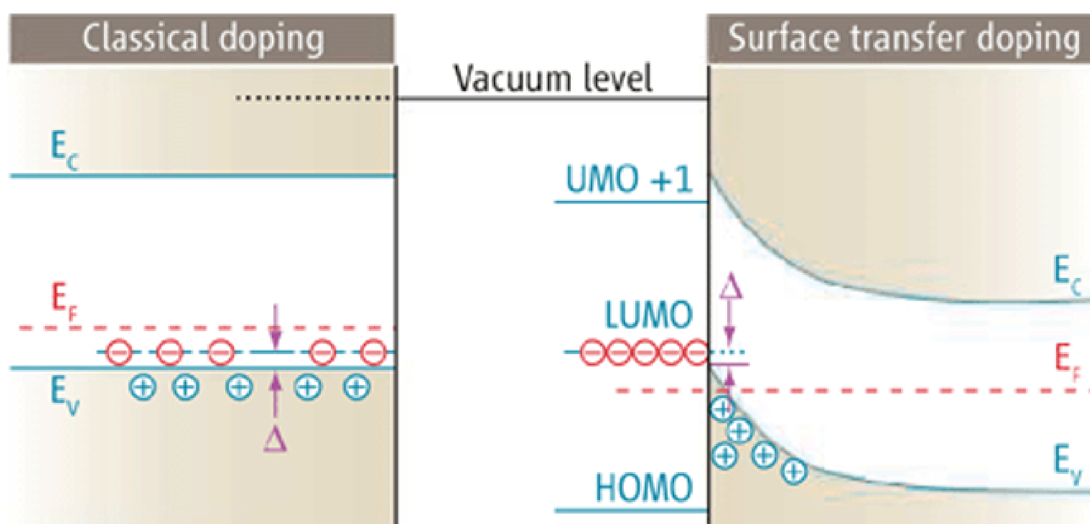

Figure 1.4: Band diagrams for conventional p-type doping (left) and p-type surface transfer doping (right) [21]. The Fermi level is labeled with E_F. Conduction band minimum and valence band maximum have energies E_C and E_V, respectively. LUMO and HOMO are the lowest unoccupied and highest occupied molecular orbitals of the surface dopants.

of the host material. The free charge carriers are confined in the direction perpendicular to the surface due to the electrostatic potential built by charge separation and are only mobile in the parallel direction. The thin space charge layer is usually on the order of nm. Effective charge transfer doping requires the LUMO of the surface dopants to lie below the VBM of the host material for p-type doping, and the highest occupied molecular orbital (HOMO) of the surface adsorbates to lie above the conduction band minimum (CBM) of the host material for n-type doping.

These alternative doping schemes are especially beneficial in low-dimensional materials, such as thin films, few-layer 2D materials, and nanowires, where impurity doping is not feasible. They have been utilized in intrinsic silicon nanowires to achieve p-type conduction [25]. They also attracted increasing research interests in the field of 2D materials, from graphene [26–28] to MoS_2 [29, 30] to other van der Waals (vdW) materials and heterostructures [31, 32]. Previous work from our group showed that thermally evaporated organic molecules, F_4TCNQ (2,3,5,6-tetrafluoro-7,7,8,8-

tetracyanoquinodimethane), could effectively p-dope Si thin film via charge transfer and improve the power factor by 75% [33]. In Chapter 3, we apply the F_4TCNQ surface transfer doping scheme to holey Si thin films and extend the effect to 3D in this hybrid organic-inorganic system.

New Material Systems

Apart from improving upon existing thermoelectric material systems, researchers are constantly searching for promising new materials. Standards-based on material chemistry have been established to efficiently filter through complex materials for promising thermoelectric properties [34]. For example, low lattice thermal conductivity can be expected for a complex unit cell with heavy atoms and strong anharmonicity.

In the past 10 years or so, several new bulk material systems have emerged as potential candidates for the next generation thermoelectric devices. BiCuSeO oxyselenides were discovered as promising thermoelectric materials in 2010 [35] and their zT was quickly improved from 0.5 to 1.4 [36]. $Mg_3Sb_{2-x}Bi_x$ in the Zintl phase compound family was recently recognized as an effective n-type thermoelectric material, with zT of about 0.8 at room temperature and of above 1.5 at 700 K [37–39]. The abundance of Mg means that $Mg_3Sb_{2-x}Bi_x$ could potentially become a low-cost alternative to commercial n-type material $Bi_2Te_{3-x}Se_x$. zT values of over 2 at high temperatures (700 K to 1000 K) have been reported for n-type SnSe in the out-of-plane direction [40–42], which motivated subsequent research to design and fabricate SnSe-based thermoelectric generators [43, 44]. Polycrystalline bulk $Sb_2Si_2Te_6$ exhibited an intrinsically high thermoelectric figure of merit zT of 1.1 at 800 K and by covering the nanograins with a cellular nanostructure of ultrathin Si_2Te_3 nanosheets its zT increased to 1.65 at the same temperature [45].

Significant advances have been made in low-dimensional materials as well. Few-layer 2D materials can be exfoliated from bulk crystals or grown epitaxially. They

often exhibit properties superior to their bulk counterpart and provide additional opportunities for tuning thermoelectric properties via band engineering. A sharp DOS profile at the band edge and a better electron mobility in many 2D materials are desirable traits for high power factor. They can be stacked together to form homo- or hetero-structures to engineer for desired properties. The attractiveness of 2D materials will be introduced in depth in Section 1.4.

1.3 Silicon-Based Thermoelectrics

Common materials used in conventional thermoelectrics can be relatively expensive. For example, BiSbTe alloys are above $100/kg and SiGe can be over $300/kg [46]. In comparison, Si is only about $3/kg. Additionally, Si is the centerpiece of the semiconductor industry. The industrial process compatibility plus the cost-effectiveness give Si-based materials great value as chip-integrated Peltier coolers and thermoelectric power generators.

Highly-doped single crystal bulk Si has a room temperature PFT of around $2.24\,\mathrm{Wm^{-1}K^{-1}}$ [47], which doubles the PFT of $\sim 1.1\,\mathrm{Wm^{-1}K^{-1}}$for commercially used thermoelectric material p-type Bi_2Te_3. This shows the potential of Si as an efficient thermoelectric material. At the same time, Si also has a large thermal conductivity, which is about $100\,\mathrm{Wm^{-1}K^{-1}}$for the doped single crystal [47]. As a result, zT of highly-doped Si is only 0.02 which is significantly lower compared to that of 1.1 for Bi_2Te_3.

Various attempts have been made by researchers to use nanostructures to suppress the thermal conduction in Si. Kessler et al. synthesized Si nanoparticles and then sintered them into nanostructured bulk Si samples, which had a room temperature zT of 0.1 and the highest zT of 0.3 at over 1000 K [48]. A series of polycrystalline Si thin films with thicknesses between 100 nm and 500 nm was grown by low-pressure

chemical vapor deposition [49]. It was found that the thinnest 100 nm sample exhibited the highest zT of 0.033 due to small grain size. High-density porous Si nanowire arrays were fabricated from Si substrates using metal-assisted chemical etching and the sample with the largest surface area demonstrated the highest zT of 0.49 at room temperature [15].

Another approach is to pattern high-density nano-sized holes onto single crystalline Si thin films. The structure is more robust compared to Si nanowires and is more compatible with silicon semiconducting industrial production. Single crystals usually have better electrical performance than polycrystalline samples because of fewer impurities and boundaries. The holey structure needs to be carefully designed so that the neck between adjacent holes is smaller than the phonon MFP but larger than the charge carrier MFP. With the right hole configuration, the holey Si thin film is expected to preserve most of its electrical transport properties while its thermal conductivity is significantly reduced. In a 100 nm thick thin film with 55 nm pitch distance and 23 nm neck between holes, the thermal conductivity reached below 2 $\mathrm{Wm^{-1}K^{-1}}$, which was suppressed by almost 85 times compared to bulk Si and by about 30 times compared to non-holey thin film of the same thickness [16]. Although its power factor was smaller by a factor of 1.5, it was overcome by the large k suppression, and a high room temperature zT of 0.4 was achieved [16]. This research proves the effectiveness of the holey Si concept. It should be noted that the performance depends highly on the sample quality and the fabrication process. The following research conducted by the same group with a similar holey configuration did not achieve such large zT because defects caused by ion implantation restricted the sample electrical conductivity [50].

Literature data of boron-doped nanostructured [15, 16, 48–50, 52] and single crystal bulk [47, 51] Si samples are plotted in Fig. 1.5 for comparison. The single crystal bulk samples have some of the best PFT values, as less scattering leads to high carrier mobility. Among the polycrystalline samples, the nanostructured bulk sample is the

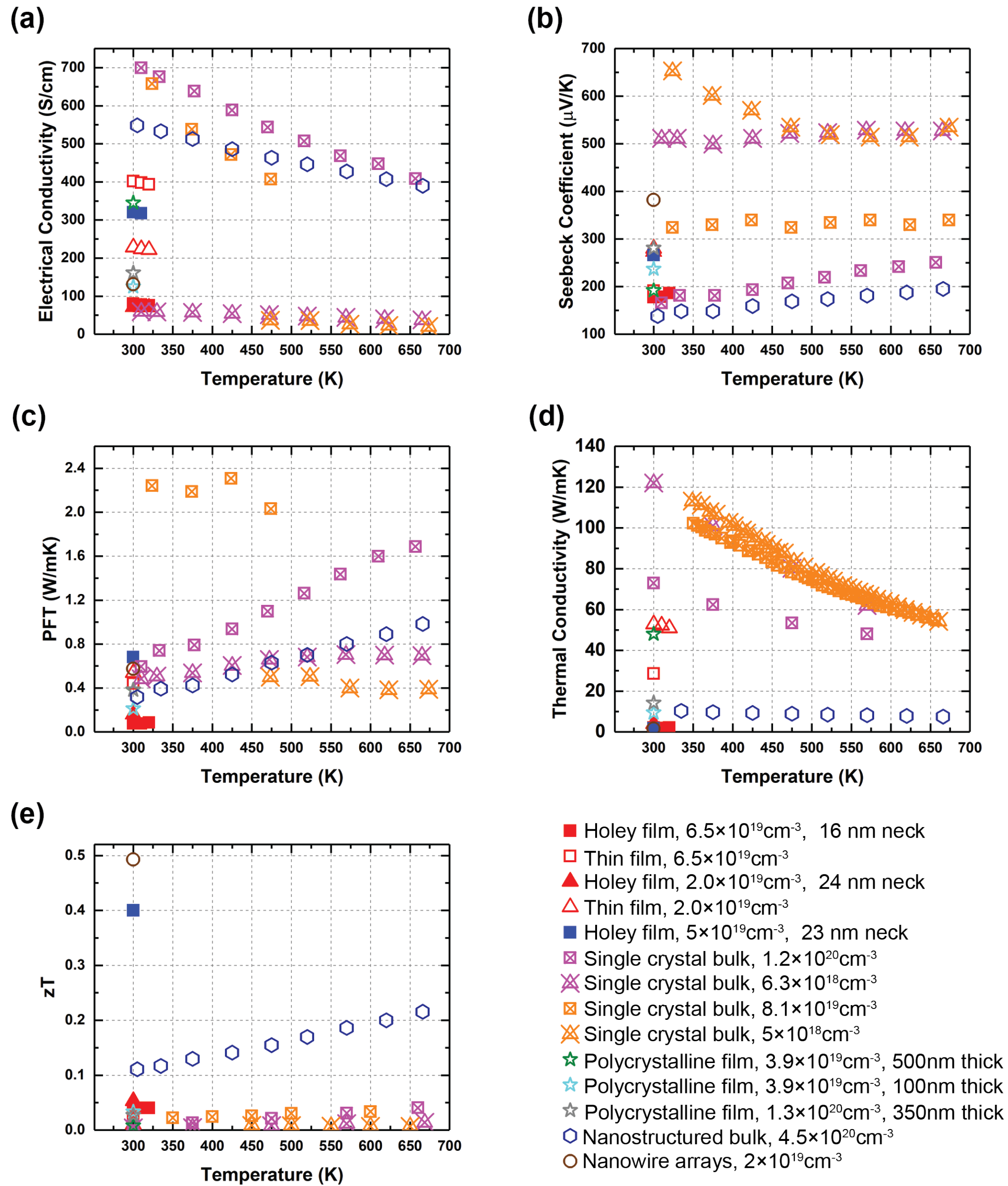

Figure 1.5: Literature data for Si-based thermoelectrics, including (a) electrical conductivity, (b) Seebeck coefficient, (c) PFT, (d) thermal conductivity and (e) zT. The closed symbols are for holey Si thin films [16, 50]. The open symbols are for plain Si thin films [16, 50]. The crossed symbols are for single crystal bulk Si [47, 51]. The star symbols are for polycrystalline thin films [49, 52]. The hexagonal symbols are for nanostructured bulk [48]. The circular symbols are for nanowire arrays [15]. All samples are boron-doped with carrier concentrations noted in the legend. The thin films are 100 nm thick unless noted otherwise.

best with a zT of above 0.1, with a moderate PFT and relatively low k. The ultra-low thermal conductivity of the holey Si thin films makes them surpass the zT of most of the other Si-based thermoelectrics, even when the electrical transport properties of some samples were on the lower side. The highest room temperature zT out of the select samples is 0.49 and was attained by the porous Si nanowire arrays, thanks to a high Seebeck coefficient and low thermal conductivity. Thermal and thermoelectric transport in Si thin films will be the main topics of Chapter 2 and 3.

1.4 2D Materials for Thermoelectric Applications

The first experimental discovery of graphene [53] has attracted attention from numerous research fields and sparked interest in many other families of 2D materials, e.g., Xenes, chalcogenides, and oxides. Here, we refer to 2D materials as a stack of a few atomic layers, with a thickness of a few nanometers or less. The layers are weakly bound by vdW interactions while the atoms are held by strong covalent or ionic bondings within each layer. They possess unique chemical, mechanical and physical properties compared to bulk materials [54, 55]. Due to the small thickness, it is possible to modulate the Fermi level and the charge carrier concentrations with electrostatic gating by use of the electric field effect [53].

2D materials are proposed for a number of potential next-generation electronic applications, such as scaling of field effect transistors down to 1 nm channel length [56], valleytronics [57], logic gates [58], memory [59] and wearable electronics [60]. 2D thermoelectric materials are proposed for nanoscale power generation and cooling. Great flexibility in band gap engineering is one of the many advantages of exploring 2D materials for thermoelectric applications. High power factors have been reported in a few 2D materials [61]. However, due to difficulty in measuring the thermal conductivity, most research reports only PF and has to rely on others' findings or theoretical

calculations to estimate k and zT.

Monolayer graphene is a gapless semimetal. It has ambipolar transport properties, record-high electron mobility of $2 \times 10^5\,\mathrm{cm^2V^{-1}s^{-1}}$ [62] and superior thermal conductivity of above $3000\,\mathrm{Wm^{-1}K^{-1}}$suspended [63, 64] and about $600\,\mathrm{Wm^{-1}K^{-1}}$on a substrate [65]. The experimental Seebeck coefficient of graphene was first reported in 2009 with a peak value of around 80 μV/K at 300 K [66], which is consistent with other reports [65, 67–69]. The sign of the Seebeck coefficient changes as the back gate voltage sweeps across the charge neutrality point. The SiO_2 substrate causes electron-hole puddles to occur near the charge neutrality point, which prevents access to lower charge carrier concentrations [70]. Duan et al. found that by placing graphene onto hexagonal boron nitride (hBN) flakes, which are relatively inert and free of surface charge traps, instead of SiO_2 substrates, the maximum Seebeck coefficient could be doubled to reach 182 μV/K and the optimized PFT was as high as $10.35\,\mathrm{Wm^{-1}K^{-1}}$ [69]. This PFT value is an order of magnitude higher than a commercial bulk Bi_2Te_3. While the ultra-high thermal conductivity makes graphene less preferable for thermoelectric energy conversions, it is great for active cooling purposes [71–73], where passive cooling by phonon transport works together with active cooling by Peltier effect to conduct heat away from the hot spots.

Besides graphene, TMDs are another family of highly appealing 2D materials for both studies of fundamental physics phenomena and emergent applications [74]. TMDs are mostly air-stable. They possess a wide range of electronic properties, from insulating to superconducting, depending on their crystalline structures and the topology of their electronic structure. These properties can be tuned by factors including the number of layers [75, 76], strain [77–79] and applied field [80]. 2D confined states can lead to a larger Seebeck coefficient, in comparison to their bulk counterparts [9]. Their thermal conductivity is moderate (much smaller than graphene) in the in-plane direction and can be extremely low in the cross-plane direction, for instance,

0.05 $\mathrm{Wm^{-1}K^{-1}}$for WSe_2 [81].

The thermoelectric performance of few-layer MoS_2 has been studied extensively. MoS_2 is an n-type material. Seebeck coefficient of monolayer MoS_2 was probed via photo-thermoelectric response [82] as well as standard transport measurements [83], which reveals a large value of -30 mV/K at 280 K. This value is 4 times higher than the 7 mV/K value of bulk MoS_2 [84] and 2 orders of magnitude higher than that of graphene [66, 69]. However, the power factor was low as a result of low conductance [83]. Following research investigated the thickness dependence of MoS_2 from a single layer up to 23 layers with the objective of optimizing PF and found that the largest PF occurred in the bilayer sample with a value above 50 $\mu\mathrm{Wcm^{-1}K^{-2}}$ [85], which is about the same as that of Bi_2Te_3 [4]. Theoretical research based on Boltzmann Transport Equation confirmed that the largely enhanced power factor in bilayer MoS_2 originated from dimensional confinement [86]. Further tuning of bilayer MoS_2 increased its room temperature PF to 8.5 $\mathrm{mWm^{-1}K^{-2}}$ or 85 $\mu\mathrm{Wcm^{-1}K^{-2}}$, almost doubling the previous maximum PF [87]. Anomalous high PF of 50 $\mathrm{mWm^{-1}K^{-2}}$ (500 $\mu\mathrm{Wcm^{-1}K^{-2}}$) has been observed in sulfur vacancy-enriched 6-layer MoS_2 on hBN at 30 K to 50 K [88]. While this PF is the highest among 2D materials measured across all temperature ranges and outperforms most bulk samples in a similar temperature range, its PFT is about 2.5 $\mathrm{Wm^{-1}K^{-1}}$because of the low temperature.

In the past two years, more exotic thin layered materials have been explored for thermoelectric applications. Single crystals of Nb_3SiTe_6 were grown by the chemical vapor transport method and exfoliated to thin samples between 7 to 70 nm thick [89]. Their Seebeck coefficient had a strong dependence on the hole density. The peak Seebeck coefficient reached 230 μV/K at 370 K resulting in a PF of 36 $\mu\mathrm{Wcm^{-1}K^{-2}}$ [89], which is comparable to materials known for high thermoelectric performance – hole-doped single crystal bulk SnSe [90] and nanostructured bulk $Bi_xSb_{2-x}Te_3$ [10]. 8 nm thick Bi_2O_2Se was grown by chemical vapor deposition and measured from low

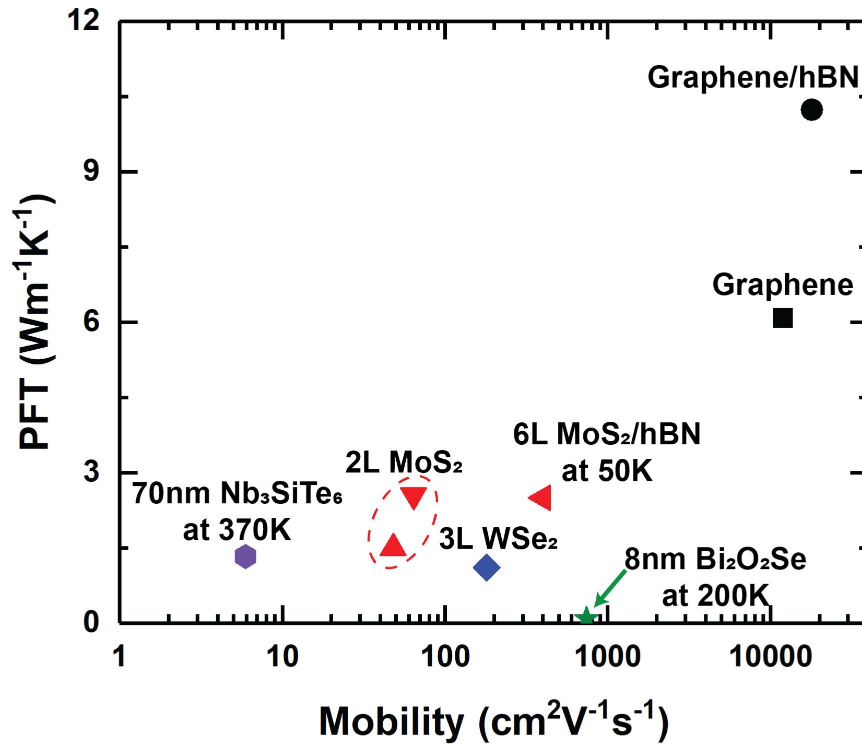

Figure 1.6: Highest experimental PFT versus mobility for 2D samples, including monolayer graphene [69], bilayer (2L) MoS_2 [85, 87], 6L vacancy-enriched MoS_2 on hBN [88], 3L WSe_2 [92], 70 nm thick Nb_3SiTe_6 [89] and 8 nm thick Bi_2O_2Se [91]. The samples are on SiO_2 substrates and measured at room temperature unless noted otherwise.

to room temperature [91]. A PF of above 4 μWcm^{-1}K^{-2} was maintained over a large temperature range from 80 K to 200 K, due to the persistently high mobility. This is potentially useful when a thermoelectric device with a large working temperature range is called for.

Figure 1.6 summarizes the highest measured PFT versus the corresponding mobility of some 2D samples mentioned above [69, 85, 87–89, 91] plus a few-layer WSe_2 sample [92]. The two graphene samples had PFT higher than all other samples with the graphene/hBN sample having the largest value. The lowest PFT belongs to Bi_2O_2Se and is about 0.1 Wm^{-1}K^{-1}. At the same time, 8 nm thick Bi_2O_2Se has

been shown to have in-plane thermal conductivity as low as $1\,\mathrm{Wm^{-1}K^{-1}}$using Raman spectroscopy [93], which means it can have a zT on the order of 0.1 and is a promising thermoelectric material for the low temperatures. The other samples have PFT values between 1 and $3\,\mathrm{Wm^{-1}K^{-1}}$. Although the mobility is relatively low in the Nb_3SiTe_6 sample, it has been compensated by its high carrier concentration and relatively large Seebeck coefficient.

These examples have demonstrated the potential of using 2D materials for high performance thermoelectric devices. However, there have been limited experimental studies on 2D thermoelectric materials to date, due to difficulties in device fabrication and measurement. In Chapter 4, I present my works on the thermoelectric transport measurements of 2D materials, in an attempt to further our understanding of the materials and the factors that might affect their performance.

1.5 Dissertation Outline

This dissertation studies material systems of thin films and 2D TMD materials. Following the background and motivation provided in the preceding sections of Chapter 1, the remaining chapters of this dissertation are organized as stated below. Chapter 2 is dedicated to a hybrid thermoreflectance-based method to measure the in-plane thermal conductivity of supported thin films, where Si and holey Si thin films were used as verification of the approach. Chapter 3 covers enhancement of the thermoelectric performance of holey silicon thin film with surface dopants organic molecules F_4TCNQ. By extending the surface doping scheme to 3D, orders of magnitude improvement in zT has been observed. Chapter 4 is centered around measuring the thermoelectric performance of few-layer 2D materials and contains both cross-plane and in-plane measurements. Chapter 5 summarizes my dissertation work and presents an outlook on future studies.

Chapter 2

Heat Diffusion Imaging for In-Plane Thermal Transport

2.1 Introduction

Measuring the in-plane thermal conductivity of thin film samples often requires film suspension [94–96] and is demanding in terms of the micro-fabrication processes needed. In the case of thin films supported on a substrate, which is typical in devices, the options are limited. If the samples are isotropic, a cross-plane measurement can be taken instead, using the 3ω method [97] or the time-domain thermoreflectance (TDTR) method [98]. In the case of anisotropic samples, two established in-plane measurement techniques are the variable-linewidth 3ω method [99, 100] and the heat spreader method [101, 102]. Both methods require extensive fabrication work and can be difficult to implement. In addition, the variable-linewidth 3ω method requires knowledge of the cross-plane thermal conductivity to obtain the in-plane one.

There has been an attempt to combine thermoreflectance (TR) imaging with finite element modeling for measurement of the in-plane thermal conductivity of Si

thin films at room temperature [103], but it requires intensive modeling and is considered as an indirect method to extract thermal conductivity. Similar combinations of thermoreflectance imaging and finite element modeling have been used by many groups to study heat transport in devices and extract various parameters, such as thermal boundary resistance between the layers and thermal conductivity of each layer of the device [104–108]. While additional opportunities for measuring in-plane thermal conductivities can be provided using TDTR, typical measurements of the technique are utilized for the extraction of the cross-plane thermal conductivity of a material.

In order to fill this void in the in-plane thermal conductivity measurement of supported thin films, *heat diffusion imaging* (HDI) is proposed, which combines the principles of the heat spreader method and the imaging capability of the thermoreflectance technique. A heater is first deposited on top of one end of the film and subsequently Joule heated. When heat flow reaches the thin film of interest, the film, supported by a low thermal conductivity substrate, spreads the heat laterally. Therefore, it is possible to extract its in-plane thermal conductivity by measuring the temperature decay profile along the film. This is known as the heat spreader method. Conventional heat spreader method requires patterning of a series of metallic lines along the sample. These metallic lines are used as resistance thermometers (thermistors) to detect the local temperatures. To measure temperature, one needs to pass current and measure resistance of the thermistors, hence, deposition of an insulating layer between a conductive sample and these thermistors is needed to avoid a current leak. This indicates that a limited number of data points (equal to the number of thermistors deposited) is available for thermal conductivity extraction, and inaccuracy exists because the temperature is not measured directly on sample.

With a TR imaging system, the thermistor fabrication processes are no longer necessary. The temperature can be measured directly on the sample and continuously along the film with a spatial resolution on the order of 100 nm. A temperature map of

the sample surface is acquired based on how surface reflectivity changes with respect to temperature variations. With HDI, one only needs a metallic heater line deposited on top of the thin film to provide the initial heat flow by Joule heating.

The detailed principles of operation, the experimental setup, the validation of HDI and a summary of the results are provided in the following sections.

2.2 Principles of Operation

2.2.1 Thermoreflectance Imaging

The TR imaging system utilizes the fact that the refractive index and therefore the reflectivity R of a material depends on its temperature T. A so-called thermoreflectance coefficient, C_{TR}, is defined to describe this relation: $C_{\mathrm{TR}} = \frac{1}{R_0}\frac{\Delta R}{\Delta T}$, where R_0 is the initial reflectivity without thermal excitation. C_{TR} mainly depends on the material surface, the incident light wavelength, and the ambient temperature. Typical C_{TR} values are in the range of 10^{-2} to $10^{-5}\,\mathrm{K}^{-1}$. When C_{TR} is known, an absolute temperature map of the sample can be obtained based on how the reflectivity changes. It is possible to calibrate for C_{TR} of an unkown material by repeatly measuring the changes in the reflectivity in response to a controlled temperature change.

A working diagram of our TR imaging system from Microsanj, LLC [110] is shown in Fig. 2.1 (a). The function generator generates a voltage pulse to excite the device under study, which is synchronized with a light pulse emitted from the LED light source by the control unit. The illumination options include 470 nm blue light, 532 nm green light and 780 nm near infrared red light, which can be selected depending on the optimal C_{TR} for the test sample. The 532 nm green light is often chosen for the best TR response, and is also used in this case. The incident light then travels through a beam splitter: half of the light goes to the sample and reflects back; the other half

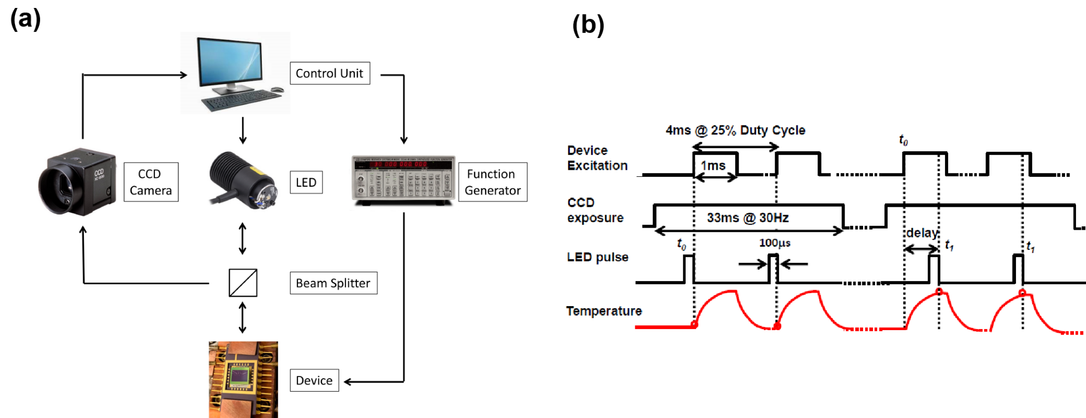

Figure 2.1: (a) The working diagram of our thermoreflectance imaging system from Microsanj, LLC. (b) Signal synchronization during measurements [109].

goes to a charge-coupled device (CCD) camera to serve as the reference signal. The CCD camera captures the changes in the reflected light off the sample when the LED is activated and deactivated to determine the temperature change, ΔT, at a certain delay time. The magnification of the microscope objective can be selected based on sample size. The spatial resolution of the temperature map is limited by optical diffraction and has values of around 300 to 400 nm depending on the wavelength and the objective numerical aperature.

Fig. 2.1(b) shows how the electrical and the optical signals are synchronized during looping measurement cycles. The duty cycle of the excitation is usually set below 30%. The captured reflectivity information is averaged over many thermal excitation cycles to provide a complete temperature map of the area of interest with minimum noise. The delay time can be choosen to look at the status of the sample surface at a specific time instant, from the beginning to the end of a entire cycle. The temporal resolution of the system is 50 ns. By sweeping the delay time, it is possible to obtain a heating or cooling curve for the device under test. For HDI measurements, the delay time is set to the end of the electrical pulse. The pulse length is long enough so that we can observe the sample in steady state.

2.2.2 Heat Spreader Model

The in-plane thermal conductivity can be extracted by analyzing how heat propagates along the thin films. When current passes though the metallic heater line on top of the thin film of interest, the generated heat from Joule heating results in a temperature gradient, which gradually decays with increasing distance away from the heater line. This temperature decay can be described by the classical fin equation [111] and is expected to be exponential in the lateral direction. Temperature, T, as a function of distance away from the heater, x, is:

$$T(x) - T(\infty) \propto e^{-\sqrt{h_i/(k_x d)}x} = e^{-\beta x}, \tag{2.1}$$

where the parameter $\beta = \sqrt{h_i/\left(k_x d\right)}$ is defined for simplicity, h_i is the cross-plane thermal conductance of the the underlying insulating layer, k_x is the in-plane thermal conductivity of the thin film of interest and d is its thickness. Dividing the cross-plane thermal conductivity of the insulator, $k_{i,z}$, by the layer thickness, d_i, gives us h_i, i.e., $h_i = k_{i,z}/d_i$. k_x can be extracted from the temperature profile as long as the thin film thickness and the substrate parameters are known. This theoretical model has been discussed extensively in the heat spreader method [102] and has been verified for Si thin films on SiO_2/Si substrate [112] and for few layer graphene on SiO_2 [101].

The thin film of interest should have a large in-plane thermal conductance relative to the cross-plane thermal conductance of the substrate insulating layer. In order to satisfy the conditions of the fin equation, it has been proposed that the healing length, defined as $\beta^{-1} = \sqrt{k_x d d_i/k_{i,z}}$, should be much larger than the combined thickness of the thin film and the substrate insulating layer, $d + d_i$ [112]. Jang et al. studied the heat transfer in a few layers of graphene on SiO_2. Even though the healing length was on the same order of magnitude as the SiO_2 substrate thickness, they have shown that the heat spreader model is still valid [101], which should be the limiting condition

to justify the application of this model. The bulk substrate at the bottom needs to be highly thermally conductive to maintain the isothermal condition.

2.3 Experimental Setup and Device Configuration

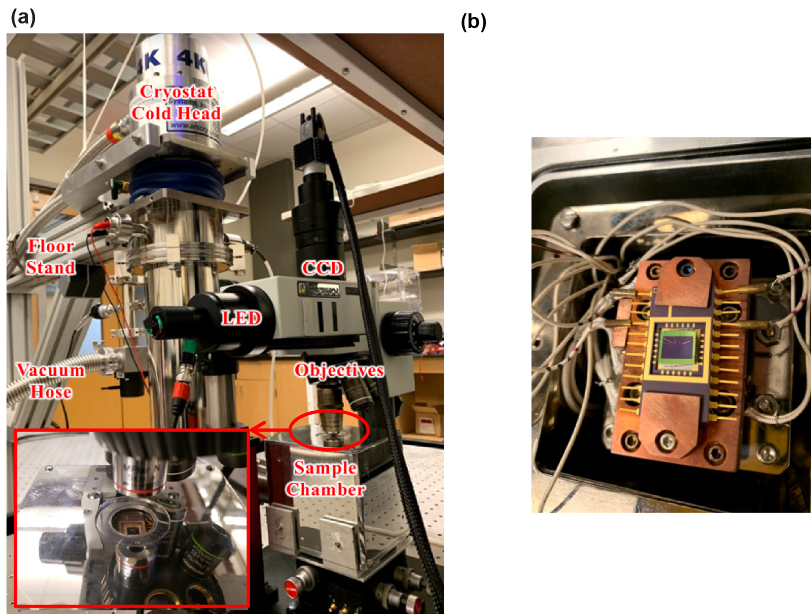

Figure 2.2: (a) Our thermoreflectance imaging system coupled with a cyrostat. The inset shows a close-up of the optical window. (b) Sample is mounted to a DIP and then to the sample stage the inside of the sample chamber.

Experimental Setup Fig. 2.2(a) shows the entire setup. The cryostat from Advanced Research Systems (ARS) has been specially engineered so that the sample chamber has an optical window on top for imaging. The window is made of 1 mm thick N-BK7 glass with Vis 0° anti-reflective coating from Edmund Optics, which provides $> 99.5\%$ transmissivity for wavelength between 425 and 675 nm and has a transformation temperature above 800 K. The thickness of the window glass needs to be corrected for by the correction collar of the objective, in order to avoid blurry images caused by changes in the refractive index. We use the $60\times$ magnification objective from Nikon

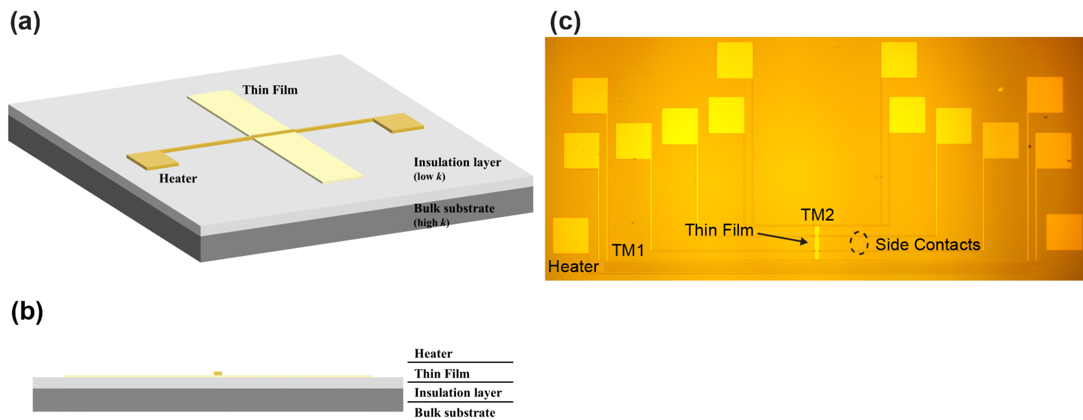

Figure 2.3: (a) Schematic of device configuration for heat diffusion imaging measurements with (b) side view. (c) Typical electrode configuration for thermoelectric transport measurements, which includes two metal lines (thermometers, namely TM 1 and 2) placed on top of the thin film.

for temperature-dependent measurements, which can correct for cover glass thickness up to 1.3 mm and offers a relatively long working distance up to 2.6 mm. The sample is wire-bonded to a ceramic dual in-line package (DIP) for electrical connections inside the chamber and is shown in Fig. 2.2(b). A heater is embedded in the sample stage to set the temperature. Vibrations caused by the vacuum pump and the helium compressor have been minimized by using low-vibration design from ARS, securing the setup on an optical table, having a floor stand and sandbags to support the cold head, and a stand to support the TR imaging camera system.

Device Configuration In order to employ the heat spreader model, we need a heater line deposited directly on top of the thin film of interest to electrically generate the heat flows. The thin film should be supported by an insulating substrate layer with low thermal conductivity, which is on a bulk substrate with high thermal conductivity as the heat sink. A simple schematic of the necessary device configuration is shown in Fig. 2.3(a) and (b).

As is often the case, the thermoelectric properties of the thin film are to be investigated together with the thermal conductivity. Typically, electrodes are configured as shown in Fig. 2.3(c) for thermoelectric measurements, which includes a heater, two thermometers and four side contacts. The two thermometer lines are deposited on top of the thin film to read local temperatures in Seebeck coefficient measurements and they can be conveniently used as heaters for HDI here. This means all measurements can be completed with one set of electrodes on the same sample and significantly lowers the required work for device fabrication.

Silicon thin films are selected as the test bed for our method, since Si is one of the most studied materials and can serve as a good reference. Two samples have been measured: one is a plain Si thin film, and the other is a holey Si thin film with periodic holes of fixed spacing. In-plane thermal conductivity of the holey Si sample is expected to greatly reduce compared to that of the in-plane silicon film, as phonons with mean free paths longer than the neck size are suppressed [16, 50, 113–116].

The devices are fabricated by our collaborators from Prof. Jon Bowers group at University of Santa Barbara from silicon-on-insulator (SOI) wafers. They have a 100 nm thick active Si layer of area $30\times200\,\mu\mathrm{m}^2$, sitting on a $2\,\mu$m thick buried oxide (BOX). The holey Si device is boron-doped ($3 - 10 \times 10^{19}\,\mathrm{cm}^{-3}$). The arrays of holes of 55 nm in diameter are spaced with a center-to-center distance of 100 nm or, in other words, a neck size of 45 nm. The plain Si thin film is lightly doped (boron, $\sim 10^{16}\,\mathrm{cm}^{-3}$) and has the same dimensions as the holey silicon film but without the holes. The Al/Au contact ($1\,\mu$m/50 nm) deposited on top of one end of the thin film is used as the heater for our measurements.

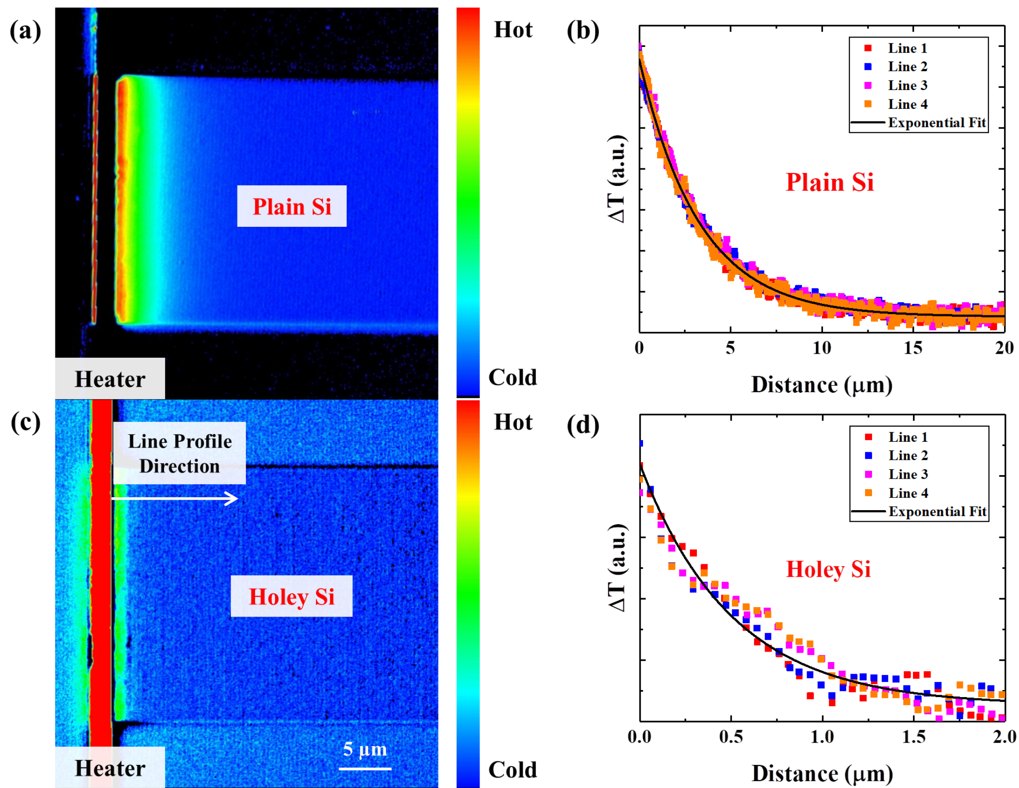

Figure 2.4: Example temperature maps of (a) the plain Si sample and (c) the holey Si sample under 100× magnification at room temperature. The same thermoreflectance coeffcient is assumed for both maps and an arbitrary unit for temperature is adopted. Note that the heater in (a) is shown in dark color as its thermoreflectance coefficient has an opposite sign to the coefficient assumed. Typically more than ten temperature line profiles are taken from each temperature map for averaging. A few representative temperature decay curves and their corresponding exponential fitting curves are shown for (b) the plain Si and (d) the holey Si thin films.

2.4 Results and Discussion

Pulses of 5 ms in duration, up to 5 V in voltage and 20% duty cycle were applied to the heater line at one end of the thin film to generate Joule heating. An example of the temperature decay map of the plain Si thin film in steady state, averaged over a few hundred thermal excitation cycles and taken under 100× magnification, is shown in Fig. 2.4(a). A representative map of the holey Si sample is provided by its side in Fig. 2.4(c) for comparison.

The same C_{TR} is used for all temperature maps across all materials, which means that an arbitrary unit is adopted for temperature. Calibrating for C_{TR} to get the absolute temperatures on the thin films is not necessary here, because the parameter β is determined by an exponential fit of the temperature profile and depends only on how fast the temperature drops. Nevertheless, since C_{TR} of Au for our green light wavelength is known [117], the temperature rise of the heater (less than 50 K) was closely monitored throughout measurements to ensure that it is reasonable to assume a single thermoreflectance coefficient. The distance that the temperature gradient extends over is much shorter on the holey Si thin film than on the plain Si one, because of a greatly suppressed thermal conductivity.

Knowing that the Si thin film thickness $d = 100\,\text{nm}$ and that the insulating SiO_2 layer thickness $d_i = 2\,\mu\text{m}$, the in-plane thermal conductivity calculation is reduced to

$$k_x = \frac{h_i}{\beta^2 d} = 5 \times 10^{12} \times \frac{k_{i,z}}{\beta^2}. \tag{2.2}$$

We use the recommended values of fused SiO_2 [118] for $k_{i,z}$ in our calculations, as it has been shown that the temperature dependence of the thermal conductivity of micrometer-thick SiO_2 matches well with the bulk values [112]. h_i is typically on the order of $10^5 - 10^6$ W/(m^{2}K), which means that the air convection to the surroundings [111] and the thermal contact resistance between the Si layer and the SiO_2 layer [119–121] are negligible in comparison. An exponential fit to the temperature line profile taken along the thin film yields β and then k_x is obtained. A few representative temperature profiles of both films and their corresponding exponential fitting curves at room temperature are shown in Fig. 2.4(b) and (d). As expected, β is smaller for plain Si based on a more gradual temperature decay, which results in a larger k_x. In order to reduce the uncertainty, for each measurement, multiple temperature line profiles that start from the edge of the heater and continue along the length of the thin

films have been taken into account and an averaged thermal conductivity is reported.

Temperature dependent data were acquired by repeating the measurements at different sample stage temperatures. The highest magnification offered for objective with correction collar and adequate working distance is 60$\times$, so the temperature map resolution is reduced to about 300 nm per pixel at temperatures other than room temperature. Limited by the working distance of this microscope objective, the mounted sample had to be brought to within 1 mm of the optical window. This led to a discrepancy between the sample stage temperature and the sample surface temperature. This temperature difference was measured using a silicon diode temperature sensor inside the cryostat, by mounting the sensor onto the DIP, where the sample was mounted. The error in the measured sample temperature is estimated to be within 1 K and has been taken into account in the thermal conductivity calculation.

2.4.1 Validation: Plain Silicon Thin Film

The temperature dependence of the in-plane thermal conductivity of the plain Si film is plotted in Fig. 2.5 and is compared with data from literature [16, 122]. Phonon-boundary scattering dominates phonon-impurity scattering in micrometer-thick plain Si thin films with carrier concentration less than $10^{17}\,\mathrm{cm}^{-3}$, and their thermal conductivities are nearly identical against temperature, independent of the exact concentrations [95]. Therefore, it is justifiable to compare the results of our 100 nm thick, slightly-doped ($10^{16}\,\mathrm{cm}^{-3}$) plain Si thin film with thermal conductivities of intrinsic silicon thin films of the same thickness [16, 122]. Our values agree with literature data for suspended samples in the temperature range from 40 K to 400 K with reasonable errors. While the uncertainty in our TDTR measurements are large, there is generally good agreement found with values extracted from heat diffusion imaging. These comparisons show the feasibility and reliability of the heat diffusion imaging method.

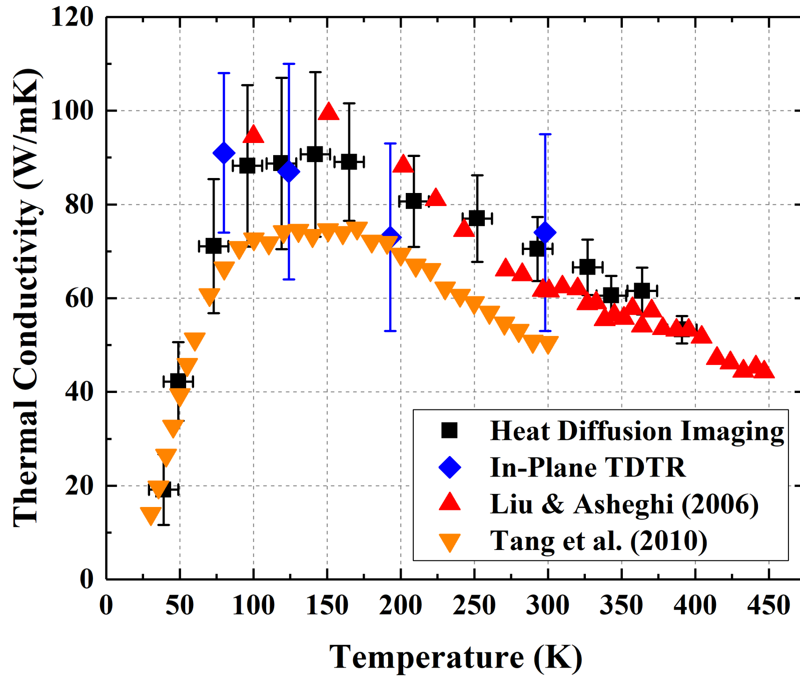

Figure 2.5: Temperature dependence of the in-plane thermal conductivity of the plain Si thin film measured by heat diffusion imaging, compared with in-plane TDTR measurement on the same sample and data from literature on suspended samples of the same thickness (100 nm) [16, 122].

2.4.2 Validation: Holey Silicon Thin Film

Data for the holey Si sample are presented in Fig. 2.6. The values are much lower than those of the plain Si sample, as the higher doping concentrations and the periodic holes introduce more frequent phonon scattering events. We were not able to perform TDTR measurements on the in-plane thermal conductivity of the holey Si film due to its low thermal conductivity. As the neck size between holes is the major deciding factor in the suppression of the in-plane thermal conductivity [16, 50, 113–115], we compared our results with suspended holey Si samples of the same thickness but different neck sizes [16, 50]. Our values for 45 nm neck size are lower than the data for 59 nm neck size and higher than those with smaller neck sizes [16, 50], as expected.

Based on a simple estimation of phonon mean free path in Si at room temperature using phonon dispersion relations, the mean free path is above 200 nm. The holey Si

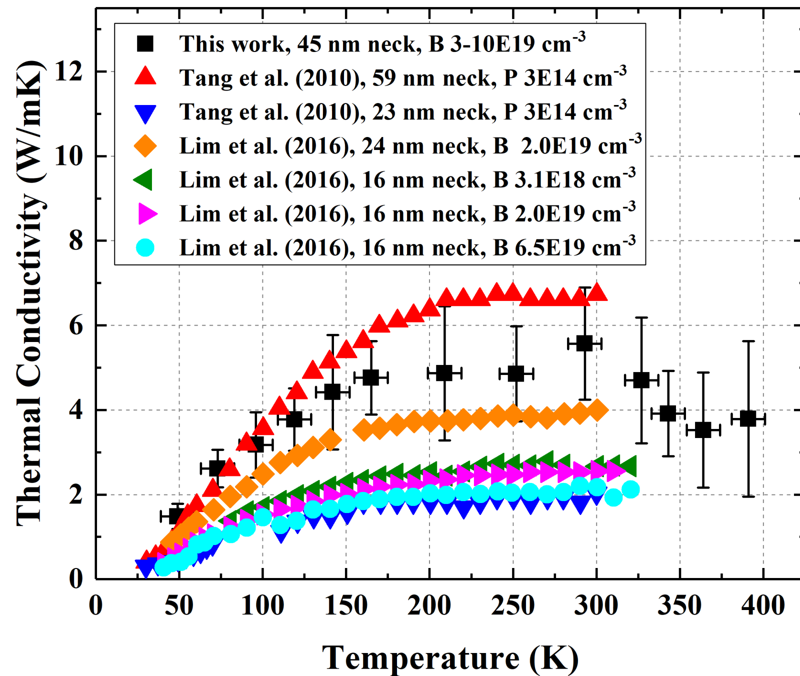

Figure 2.6: Temperature dependence of the in-plane thermal conductivity of the holey Si thin film measured by heat diffusion imaging, compared with holey Si thin films with the same thickness (100 nm) but different neck sizes from literature [16, 50]. The carrier concentration of each sample is noted in the legend, with B for boron-doped and P for phosphorus doped.

thin film is 100 nm thick and the neck size is 55 nm, which is the limiting dimension here. This leads to increased phonon scattering and suppression of the thermal conductivity. The error bars are large in our thermal conductivity measurement, so the decrease in the thermal conductivity above 300 K is not conclusive and it is possible that the thermal conductivity flats out. The existence of the periodic holes changes phonon behaviors and might backscatter them. There is one report on decreasing thermal conductivity above 300 K in holey Si thin films, which was attributed to phonon-boundary scattering [123]. Although higher temperatures usually result in increased phonon-phonon scattering, there is not enough research to conclude how that will manifest in the temperature-dependent thermal conductivity of holey Si with the already increased phonon-boundary scattering. Phonon behavior in holey Si at high temperatures could be an interesting topic for future studies.

2.4.3 Note on Determination of Steady State

Before performing the systematic temperature dependent study, we ran a short experiment to check the time needed for the system to reach steady state, by applying a 10 ms voltage pulse and measuring at delay times of 4 ms, 6 ms, 8 ms and 10 ms after the start of the pulse. Although the overall temperature of the sample is slightly higher with longer delay time, the shape of the temperature decay profiles stayed constant and there was no noticeable difference in the measured β parameter.

2.4.4 Note on Thermoreflectance Signals from Substrate Layers

The optical penetration depth of our LED wavelength in Si is more than 100 nm so we might receive reflectance signal off the SiO_2. The SiO_2 layer under the Si thin film is 2 μm thick and therefore the light should not be able to penetrate through or reach the bulk Si substrate. At room temperature, the refractive index of Si at 530 nm is about 4.3 and that of SiO_2 is about 1.45 [124]. Assuming that the normal incident light has an intensity of I_0, the reflected light intensity off the Si surface is $R_{air/Si}I_0 = \left|\frac{n_{air}-n_{Si}}{n_{air}+n_{Si}}\right|^2 I_0 = 0.39I_0$, where R is the reflectance; and the received light intensity off the SiO_2 surface after travelling through the Si thin film is $R_{air/Si}\left(1-A_{Si}\right)R_{Si/SiO_2}\left(1-A_{Si}\right)R_{air/Si}I_0 = 0.03I_0$, where A_{Si} is the light absorbed by the 100 nm thick Si layer and is about 0.1 in our case.

Additionally, the thermoreflectance signal is proportional to the thermoreflectance coefficient (C_{TR}) and hence is proportional to the derivative of the refractive index to the temperature ($\mathrm{d}n/\mathrm{d}T$). Larger $\mathrm{d}n/\mathrm{d}T$ indicates larger change in the reflectivity signal with the same temperature change. $\mathrm{d}n/\mathrm{d}T$ of SiO_2 around 500 nm wavelength has values smaller than 1×10^{-5} K^{-1} in our measurement temperature range [124], while that of Si one order of magnitude larger: it is around 5×10^{-4} K^{-1} at room temperature and stays on this order of magnitude as temperature changes [125, 126].

Considering these two factors, the TR signal from the SiO_2 layer should be negligible in comparison.

2.5 Conclusion

We have measured the in-plane thermal conductivity of holey Si and plain Si thin films from 40 K to 400 K using heat diffusion imaging, which combines the thermoreflectance imaging technique with the heat spreader model. By comparing the obtained data for plain Si with values measured by in-plane TDTR and from literature, we have demonstrated the reliability of our method.

Compared to existing methods, HDI holds several advantages. Firstly, it works for anisotropic thin films supported on a substrate without the need for film suspension. Secondly, it is an electrical-pump opitcal-probe method and brings minimum disturbance to the sample. Thirdly, the local temperatures are measured directly at the sample surface without resistive thermometers or top insulation layer for conductive samples. The temperature readings are more accurate and the fabrication processes are much simplified. Lastly, it has submicron spatial resolution of around 300 nm, limited by optical diffraction.

In summary, HDI provides fast and accurate in-plane thermal conductivity readings of supported thin films with minimum required micro-fabrication processes and is of great importance in the study of heat transport in thin films. In the next two chapters, we apply the heat diffusion imaging method for neck size dependence of holey Si thin films as well as few-layer 2D samples including $NbSe_2$.

The work in this chapter has been published in *Review of Scientific Instruments* [127].

Chapter 3

Enhancing Thermoelectric Performance of Holey Silicon Thin Films using F_4TCNQ Surface Doping

3.1 Introduction

3.1.1 Thermoelectric Transport of Conventionally Doped Holey Silicon Thin Films

With the thermal conductivity measurements on holey silicon thin films in Section 2.4.2, a thorough study of its thermoelectric transport properties could be completed. The samples were boron-doped to $3 \times 10^{19} - 1 \times 10^{20}$ cm^{-3}. zT of the holey silicon sample is plotted in Fig. 3.1 and compared to literature data of Si-based thermoelectric materials. As the temperature increases, the rate of change in its thermal conductivity gradually decreases. We expect minor changes in the thermal conductivity of holey Si above 400 K and we can estimate the lower limit of its zT at higher temperatures by assuming a constant thermal conductivity 3.8 ± 0.3 W/mK. At room temperature, zT

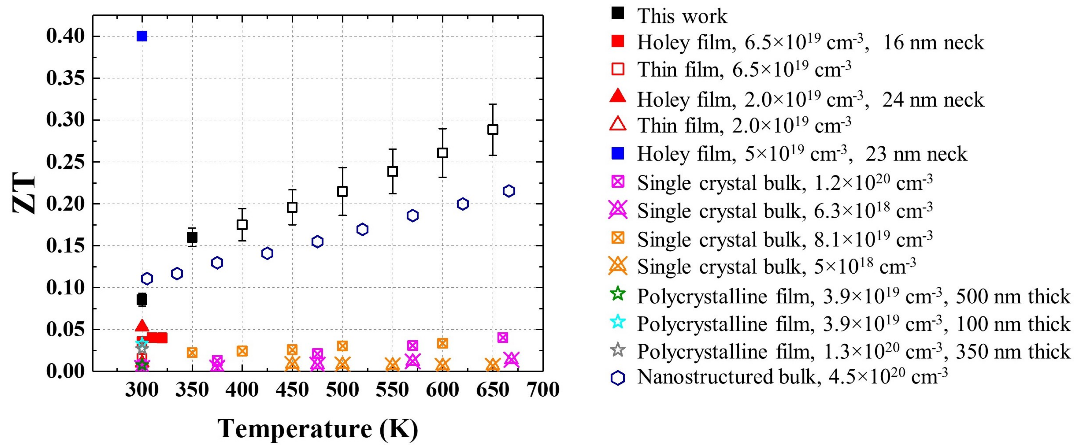

Figure 3.1: Figure of merit, zT, of the highly-doped holey Si thin film versus temperature. The closed black symbol represents our experimental data and the open black symbols give our projected zT by assuming a constant thermal conductivity against temperature higher than 391 K. The results are compared with data from literature [16, 47–52]. All samples are boron-doped with carrier concentrations noted in the legend. The thin films are 100 nm thick unless otherwise noted.

is approximately 0.09. The holey Si device becomes more efficient at elevated temperatures, with its ZT exceeding 0.29 at 650 K. Our room temperature zT shows more than four times improvement over the highly-doped bulk Si sample [47], because of the 16-fold reduction in thermal conductivity. This demonstrates that the holey geometry is an effective approach to limit phonon transport and increase the thermoelectric performance.

3.1.2 Surface Charge Transfer Doping

Similar to the holey silicon samples we studied, most thermoelectric materials are made out of heavily doped semiconductors. Bulk silicon demonstrates the maximum thermoelectric power factor at high doping levels (around $10^{20}\,\mathrm{cm}^{-3}$) [47]. Conventional doping techniques insert dopant atoms into the host materials. These dopants introduce strong Coulomb repulsion and reduce the carrier mobility. In comparison,

surface charge transfer doping is a clean and effective alternative, where charges exchange across the interface between the surface dopants and the host material due to energy bands misalignment [21]. The ionized atoms are therefore distanced from the mobile charge carriers and a space-charge layer is formed at the interface. As the dopants are outside the host material, the extra space between the dopants and the carriers lowers the ionized impurity interactions significantly. This is similar to the modulation doping idea used in transistors. The electron mobility in GaAs, for instance, has been enhanced by 4 orders of magnitudes using modulation doping strategy at below 10 K [18].

Organic molecule, F_4TCNQ, is a strong electron acceptor with an electron affinity as high as $E_a = 5.24\,\mathrm{eV}$ [128] and is often used as a p-type surface dopant for organic [129, 130] and inorganic [26, 27, 131] materials. First-principles calculations predict that physisorbed F_4TCNQ monolayer can efficiently dope Si [132], achieving a surface hole concentration as high as $10^{13}\,\mathrm{cm}^{-2}$. Experimental study on the transport properties at F_4TCNQ-Si interface demonstrated a resistance reduction by a factor of 10 compared to undoped film and a thermoelectric PF enhancement by 75% [33].

In this work, we extend the surface doping to 3D. In a 2D geometry, while the thermoelectric power factor can be extremely large [19], one has to deal with an electron gas with a large thermal conductivity. The modulation doping concept has

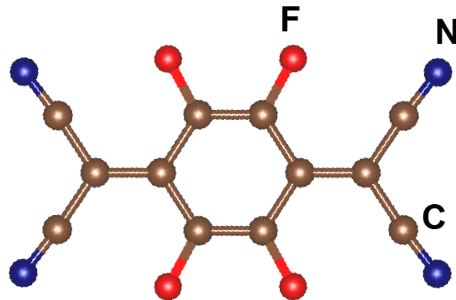

Figure 3.2: Molecular structure of F_4TCNQ, with unit cell $a = 7.51\,\text{Å}$, $b = 11.68\,\text{Å}$, $c = 5.93\,\text{Å}$.

been extended to 3D in the past and improved zT has been shown in SiGe nanostructures [17, 20]. The improvement, in that case, was limited due to the grain-boundary scattering. Here, we propose the usage of holey silicon thin films to demonstrate 3D surface doping in organic-inorganic structures. The holey silicon films are clean with minimal scattering due to the periodic nature of holes and clean thin-film fabrication process, compared to the nanostructured bulk samples [17, 20] with irregular grain boundaries and impurities. They provide a possible geometry for a 3D network of organic dopants and an effective doping not only from the top surface but also from within the film.

Figure 3.3: (a) Schematic and (b) optical image of the holey silicon device, which includes one heater, two thermometers (TMs) and four side contacts. (c) Scanning electron microscope image of the hole configuration, for sample with 120 nm neck size. The scale bar is 300 nm.

3.2 Device and Methods

Device Fabrication

The holey silicon thin-film devices were fabricated from SOI wafers by our collaborators from Prof. Masahiro Nomura's group at the University of Tokyo, Japan. The wafers had an active Si layer of 220 nm thickness on top of a 3-μm-thick SiO_2 layer. We used laser lithography and reactive ion etching (RIE) to define device areas of $200\times30\,\mu m^2$. Subsequently, e-beam lithography and RIE patterned the nano-sized hole arrays onto each device. The holes were kept at a fixed pitch distance of $a = 300$ nm, and the neck size n of each device varied from 80 nm to 190 nm. Lastly, electrodes (500 nm Al and 50 nm Au) were evaporated onto the sample to serve as thermometers, heaters and voltage probes. The Si layer was mildly boron-doped with a resistivity of $10\,\Omega\cdot$cm, which corresponds to a hole concentration of $\sim 10^{15}\,\mathrm{cm}^{-3}$. The regions under the contacts were doped to $10^{20}\,\mathrm{cm}^{-3}$ to ensure Ohmic contacts. Schematics of the hole configuration, as well as the device configuration, are shown in Fig. 3.3.

F_4TCNQ Deposition

F_4TCNQ crystal powder was thermally evaporated in a home-built vacuum chamber with a base pressure of $< 10^{-6}$ Torr. The deposition temperature was maintained at about 140 °C, following the methods described in a previous work [33]. The samples were dipped in 10% HF for a few seconds right before being loaded to the evaporation chamber, in order to remove the native oxide and passivate the Si surface.

Transport Measurements

The electrical resistance was measured by the standard 4-point probe method and the

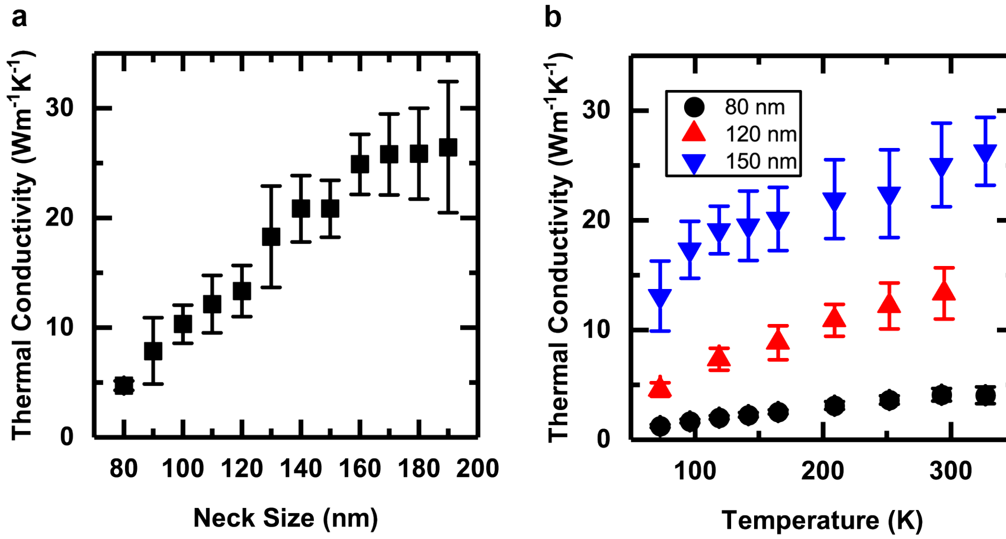

Figure 3.4: (a) Room temperature in-plane thermal conductivity for neck sizes from 80 nm to 190 nm and (b) temperature-dependent thermal conductivity from 50 K to 350 K for neck sizes 80 nm, 120 nm and 150 nm.

conductivity was calculated assuming a solid thin film. The Seebeck voltage was measured by a Keithley 2182A nanovoltmeter and the temperature difference was interpreted from the resistance changes of the two gold thermistors at the two ends of the thin film. Heat diffusion imaging was used to measure the in-plane thermal conductivity.

3.3 Results and Discussion

The in-plane thermal conductivity of the holey silicon thin film depends on the neck size. Figure 3.4 shows that as the neck size goes down from 190 nm to 80 nm, the room temperature thermal conductivity decreases from 26.4 $\mathrm{Wm^{-1}K^{-1}}$ to 4.7 $\mathrm{Wm^{-1}K^{-1}}$. Smaller neck size suppresses the phonon transport more and leads to smaller thermal conductivity values. The trend is consistent with those summarized in literature [115, 116]. In comparison, the room temperature thermal conductivity of a silicon thin film of the same thickness without any holes is about 90 $\mathrm{Wm^{-1}K^{-1}}$ [133]. The reduction

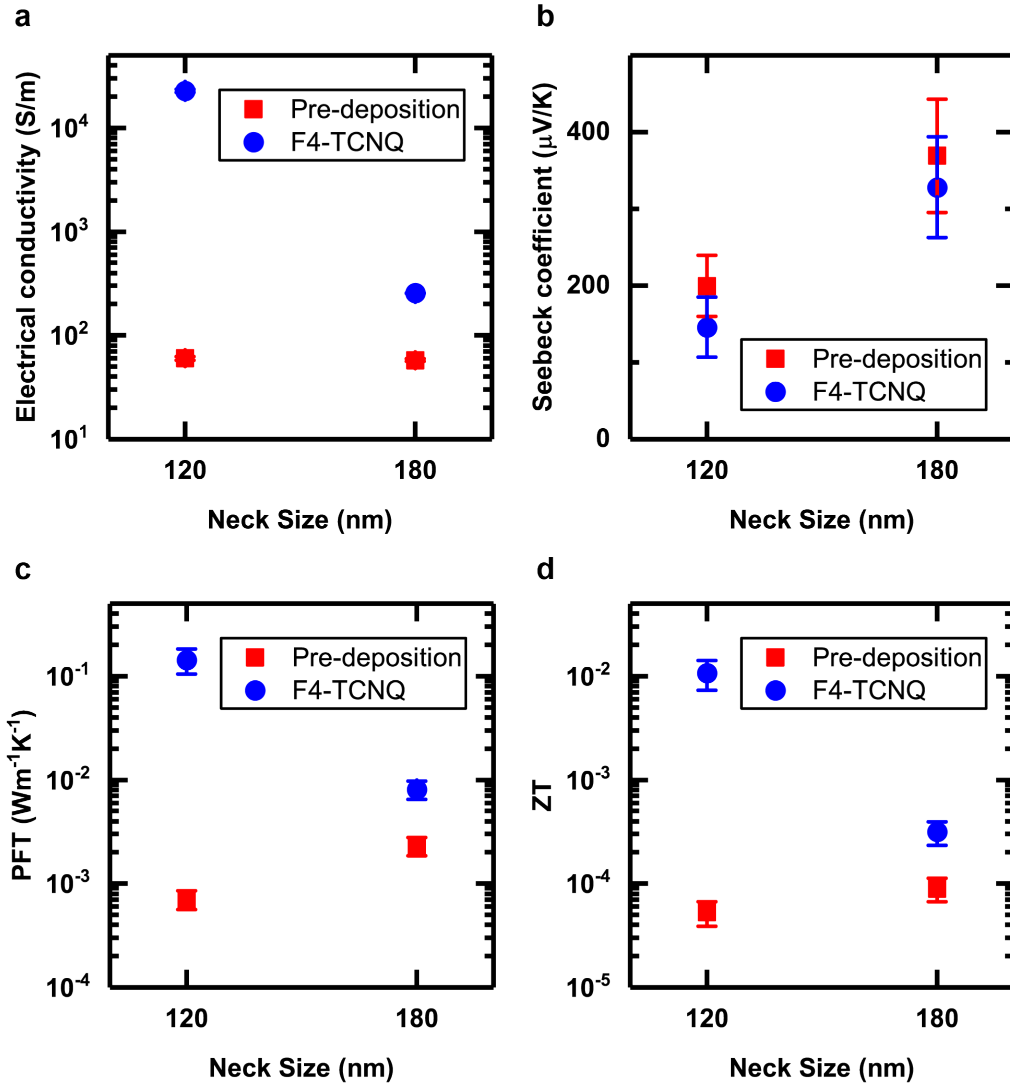

Figure 3.5: Comparison of the thermoelectric performance of the 120 nm neck and 180 nm neck devices before and after F_4TCNQ deposition at room temperature, in terms of (a) electrical conductivity, (b) Seebeck coefficient, (c) PFT and (d) zT.

in thermal conductivity with periodic holes is as high as 19 fold.

The thermal conductivity of three different neck sizes as a function of temperature was also obtained and is plotted in Fig. 3.4. Their temperature-dependent trends are consistent: as the temperature increases from 75 K to above room temperature, the thermal conductivity increases and the rate of change becomes smaller at higher temperatures. The overall change in this range is about 2 to 3 times.

The electrical transport of the thin film with neck sizes of 120 nm and 180 nm before and after the F_4TCNQ deposition was measured at room temperature. For both samples, their electrical conductivity started at around 60 S/m. With F_4TCNQ, the conductivity of the 120 nm sample increased by 2 orders of magnitude and reached 2.28×10^4 S/m, while that of the 180 nm sample increased to 255 S/m, slightly over 4 times higher. As expected, the Seebeck coefficients of both samples dropped after doping, by about $10 - 20\%$. As a result, the power factor times temperature (PFT) was improved by 4 times for the 180 nm neck sample and by 200 times for the 120 nm one. The doping by F_4TCNQ here is more effective compared to the case of silicon thin film without holes [33]. A PFT as high as 0.14 $\mathrm{Wm^{-1}K^{-1}}$ was achieved for the doped 120 nm sample, which is on the same order of magnitude compared to highly-doped Si thin film samples from literature [16, 49].

There are several factors deciding the effectiveness of the F_4TCNQ doping. First is the orientation of the molecules. It has been shown that when the molecules lay parallel to the surface, the charge transfer is small [132]. F_4TCNQ doping is only effective when the molecular long axis is normal to the silicon surface. Second, because these are relatively large molecules (see Fig. 3.2), the holes have to be large enough for them to enter properly and attach to the inner cylindrical walls effectively. Finally, F_4TCNQ has a low sticking probability on H-Si(100) [134] and limited wettability making the deposition processes only successful when high flux and long time deposition are used [33]. Considering that the 180 nm neck size sample (corresponding to 120 nm hole diameter) only demonstrates 4 times conductivity improvement compared to the 200 times improvement observed in the 120 nm neck size sample (180 nm hole diameter), we can infer that in the latter sample, more F_4TCNQ molecules entered the holes and attached normal to the walls. In other words, the 120 nm neck size sample has a larger overall surface coverage. However, we note that the difference in the surface area coverage is only a factor of 2.4 and is not enough to explain the large benefit here.

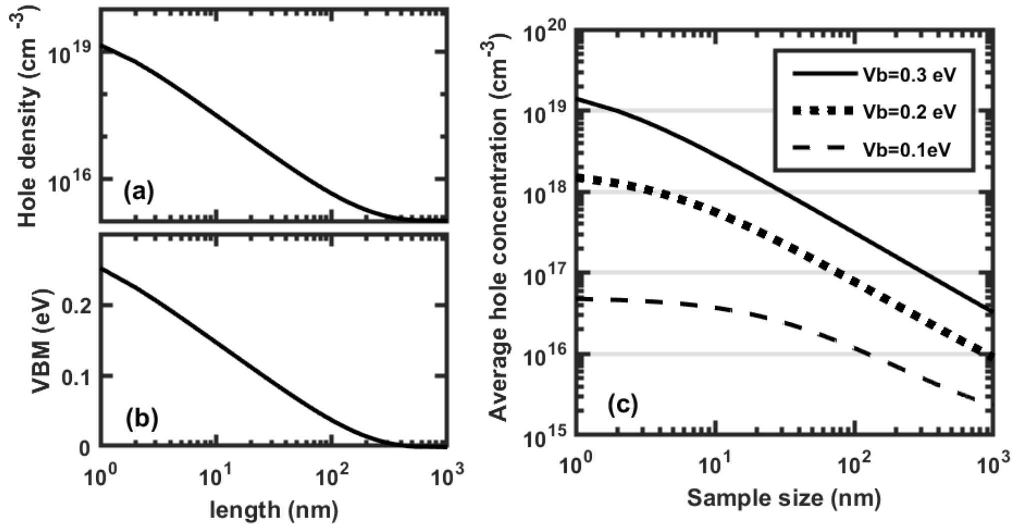

Figure 3.6: 1D Possion solver for charge transfer between F_4TCNQ and silicon. (a) Hole density and (b) valence band maximum as a function of the length into the silicon from the surface. (c) Average total hole concentration versus effective sample size, where V_b is the built-in potential.

To understand the effect better, we have developed a 1D Poisson solver. The model considers F_4TCNQ as metal-like source of hole carriers and calculates the charge transfer and the band bending inside the silicon structure, assuming that the Fermi level is pinned by the F_4TCNQ molecules. Parameters of Si, including its effective mass (0.81 for hole and 1.81 for electron density of states effective masses respectively), bandgap (1.12 eV), work function, and dielectric constant (11.7), are well known [135]. The position of the chemical potential of silicon before F_4TCNQ deposition can be calculated knowing the initial doping density of silicon (10^{15} cm^{-3}) and it is 0.3 eV below the middle of the gap. Besides the silicon parameters, the relative alignment of the F_4TCNQ energy levels to the bands of silicon determines the amount of charge transfer.

Wang et al. [132] calculated the charge transfer energy of a single F_4TCNQ molecule on silicon surface using first-principles calculations. They reported that the difference

between the electron affinity of the F_4TCNQ molecule and the valence band maxima of silicon is about -0.01 eV and 0.17 eV using PBE and GW calculations respectively. We also note that the levels are modified when studying a single molecule compared to bulk. The electron affinity of F_4TCNQ is reported to be between $5.08 - 5.24$ eV [136] and the work function of Si(100) is reported to be around 4.91 eV [137]. The difference results in a built-in potential of 0.1 to 0.3 eV between silicon and F_4TCNQ surface. Charge transfer occurs primarily at the surface and drops rapidly perpendicular to the surface. Hence, we expect a strong size dependence. Figure 3.6 shows the potential profile (valence band maxima) and the charge carrier density along a 1D sample. As expected, at the interface the charge density is maximum, and far from the interface it is the same as the initial value of 10^{15} cm^{-3}.

Figure 3.6(c) shows the effect of Fermi level pinning. As the Fermi level is pinned deeper in the valence band, the built-in potential is larger and the charge transfer is also larger. Let us now map this 1D model onto the 3D geometry. Assuming that in the 120 nm hole diameter case the dopants either did not enter the holes or if they did, they did not effectively align inside, then only the top surface is doped. The effective size of the sample is the thickness of the film, 220nm. Figure 3.6c shows that in the case of 220 nm, the carrier concentration can be improved to between 5×10^{15} to 1.1×10^{17} cm^{-3} depending on the the built-in potential. In the 180 nm diameter case, and assuming effective doping from the inner walls, the size is now half of the neck size, 60 nm. At this length, the carrier concentration improves to between 2×10^{16} to 5×10^{17} cm^{-3}, corresponding to a 20 to 500 times improvement of the conductivity after F_4TCNQ deposition. The overlap of the charges from the top and side surfaces can further increase these numbers.

We conclude that small neck sizes correspond to significantly larger carrier concentrations and enhanced power factors after doping. Smaller neck size also means smaller thermal conductivity, which is advantageous for better zT. In the current

study, zT of the 120 nm sample reached 0.01 after F_4TCNQ doping, demonstrating 2 orders of magnitude improvement. We therefore believe that even smaller neck sizes can further improve the zT.

Here we compare the obtained zT with conventionally doped samples at room temperature. zT of 0.01 in this work is one order of magnitude smaller than that of highly-doped nanocrystalline bulk Si samples ($4 \times 10^{20}\,\mathrm{cm}^{-3}$) [48] but is comparable to highly-doped single crystal bulk Si ($10^{20}\,\mathrm{cm}^{-3}$) [47] and higher than single crystal with mid-level doping ($10^{18} - 10^{19}\,\mathrm{cm}^{-3}$) [47, 51]. While our zT is lower than some reported values for highly-doped holey Si thin films with smaller thicknesses and neck sizes [16, 138], it is comparable to others [50]. This shows that surface charge transfer doping via F_4TCNQ deposition is an effective approach to introduce additional charge carriers into Si thin films. The improvement in the thermoelectric performance of holey Si thin films can be further optimized by considering factors including film thickness, neck sizes and surface dopants.

3.4 Conclusion

In conclusion, we fabricated Si thin films with periodic nm-sized holes from SOI wafers for thermoelectric applications. We first evaluated the zT of holey Si thin films conventionally doped by boron ion implantation and showed that the holey structure effectively suppressed the thermal conductivity and improved the zT to over 0.29 at 650 K. Then we performed surface charge transfer doping with F_4TCNQ organic molecules to holey Si thin films with different hole configurations. The in-plane thermal conductivity depends on the neck size and changed from $26\,\mathrm{Wm^{-1}K^{-1}}$ to $5\,\mathrm{Wm^{-1}K^{-1}}$ as the neck size decreased from 190 nm to 80 nm. The F_4TCNQ molecules were deposited via thermal evaporation. The sample with larger hole diameter allowed more space for the F_4TCNQ molecules and the surface doping was

more effective. PF and zT of the 120 nm neck sample improved by 2 orders of magnitude. The large improvement was possible because the holey structure extended the surface doping effect to 3D. This study demonstrates the possibility of building high-performance thermoelectric devices out of organic-holey Si hybrid structure. Further evaluation of the holey Si geometry, the dopant materials and the manipulation of dopant molecule orientation is expected to bring even more enhancement in the thermoelectric properties. Systems with larger surface-to-volume ratios, such as nanowires, should also benefit from this doping scheme.

The results in this section have been published in *Materials Today Physics* [139].

Chapter 4

Thermoelectric Transport in 2D Materials

4.1 Overview

2D materials are being considered in many next-generation electronic devices as conventional silicon-based electronics approach their limits of scaling [132,140]. This also calls for next-generation heat management devices. In order to select suitable materials for cooling and energy conversion applications, we need to have adequate knowledge of their thermoelectric properties, as well as the factors affecting their performance in a device.

4.1.1 Thermoelectric Transport in 2D Materials Under Gating

The thermoelectric transport properties of graphene and several 2D materials, such as MoS_2 and WSe_2, have been discussed in detail in Section 1.4. In their pristine form, by changing the carrier concentration with a back gate voltage, high PF of 85 μWcm^{-1}K^{-2} was reported in bilayer MoS_2 [87] and the highest PFT of 6.16 Wm^{-1}K^{-1} was achieved by monolayer graphene on SiO_2 [69]. However, their in-plane thermal

conductivities are also high. Up to now, the zT values of pristine graphene and TMDs have only reached the order of 10^{-2}.

Few-layer black phosphorus (BP) is a narrow bandgap semiconductor, with a high mobility of 1×10^{3} $cm^{2}V^{-1}s^{-1}$ [141]. First-principles calculations show that the zT of monolayer BP can reach 1 by either raising the temperature to 500 K or moderate doping [142]. The challenge in experimental studies of BP comes from its air stability. Mono- or bi-layer devices have to be encased to retain their properties [143]. 10 nm to 30 nm thick BP flakes were characterized, showing a room temperature Seebeck coefficient of about 400 μV/K and a power factor of 5 $\mu Wcm^{-1}K^{-2}$ at 245 K [144]. The experimental zT is only on the order of 10^{-3}, far from the theoretically predicted values.

Table 4.1 summarizes the maximum experimental PFT and the corresponding Seebeck coefficient achieved in intrinsic 2D materials on SiO_2 substrates with back gate optimization. Graphene and TMD samples are the most promising, with PFT comparable to or larger than 1.1 $Wm^{-1}K^{-1}$, which is the PFT value of commercial Bi_2Te_3. We turn to heterostructures and other nanostructures in hope of a better zT.

Material	Seebeck (μV/K)	PFT ($Wm^{-1}K^{-1}$)	Reference	Year
1L graphene	109	6.16	[69]	2016
1L MoS_2	-3×10^{4}	low	[83]	2014
2L MoS_2	-375	1.5	[85]	2016
2L MoS_2	-320	2.55	[87]	2017
3L WSe_2	100	1.1	[92]	2016
	-150	0.96		
10$-$30 nm BP	300 @245 K	0.12 @245 K	[144]	2016
70 nm Nb_3SiTe_6	230 @370 K	1.33 @370 K	[89]	2020
8 nm Bi_2O_2Se	-100 @200 K	0.05 @200 K	[91]	2021

Table 4.1: Summary of maximum experimental PFT and the corresponding Seebeck coefficient achieved in thin intrinsic 2D materials on SiO_2 substrate with gate optimization. The data were obtained at room temperature unless noted otherwise.

4.1.2 Thermoelectric Transport in van der Waals Heterostructures and Other Nanostructures

Few-layer 2D materials can be stacked on top of one another like LEGO bricks to form van der Waals heterostructures [145, 146]. Although the interlayer vdW forces are relatively weak compared to the covalent bonds in plane, they are sufficient to keep the stack together. The layer-by-layer dry transfer technique is frequently used to assemble these heterostructures. It uses heated polymers – polypropylene carbonate (PPC) mounted on polydimethylsiloxane (PDMS) – to pick up the desired flake and drops down the stack to its destination by adjusting the polymer temperature [147].

Atomically smooth insulator hBN is mostly free of surface dangling bonds and charge traps and thus is often used to improve the electrical performance or protect the sample from air exposure in the vdW heterostructures [148]. Graphene was distanced from the surface charges on SiO_2 substrate by stacking it on top of hBN and its PFT almost doubled [69]. Similarly, in the case of 6L MoS_2/hBN heterostructure, it exhibited PF higher than all other 2D materials measured to date [88]. Twisted bilayer graphene, which is two monolayer graphene stacked and twisted relative to each other by a small angle, on hBN had a cross-plane effective PFT of 0.3 $Wm^{-1}K^{-1}$at room temperature [149]. Although this value is smaller than in-plane graphene samples [69], the cross-plane thermal conductivity of this structure is expected to be lower due to phonon scattering and might lead to high zT. A complicated heterostructure of bilayer graphene/20 nm hBN/bilayer graphene demonstrated a maximum PF of 700 $\mu Wcm^{-1}K^{-2}$ at room temperature due to Coulomb drag and counterflow Seebeck effect [150], corresponding to a high PFT of 21 $Wm^{-1}K^{-1}$.

The nanostructuring strategies introduced in Section 1.2 for thin films can also be implemented for 2D materials. Wan et al. [151] constructed n-type hybrid superlattices of alternating inorganic TiS_2 monolayers and organic cations and obtained a

PF of 4.5 μWcm^{-1}K^{-2} at room temperature. With an ultra-low in-plane thermal conductivity at 0.7 Wm^{-1}K^{-1}, its zT reached 0.28 at 373 K. Oxygen plasma treatment in few-layer graphene can randomly introduce defects and was able to raise the Seebeck coefficient to 700 μV/K [152]. Unfortunately, the electrical conductivity of the plasma-treated graphene was lowered by 2 orders of magnitude and the PF was 45 μWcm^{-1}K^{-2} [152], only 20% of the value for pristine graphene on SiO_2 [69]. Suspended graphene nanoribbons of 237 nm long by 43 nm wide successfully increased the zT to 0.1 at below room tempratures [153], which is orders of magnitude improvement from pristine graphene.

This short literature review suggests that 2D materials generally have superior electrical performance and high power factors. However, the realization of high zT in 2D materials requires more sophisticated phonon transport engineering. Thermoelectric studies in the cross-plane direction might provide some answers, as the cross-plane thermal conductivity can be much lower than the in-plane one [81]. Heterostructures and nanostructures provide additional knobs for tuning the thermoelectric performance but can be demanding in terms of the required fabrication work. While theoretical calculations can offer insights to materials that have not been measured experimentally, experimental characterization of more 2D materials will expand the database and point out the discrepancy between theory and reality so that a more accurate prediction of useful materials can be made.

4.2 In-Plane Thermoelectric Transport of 4-Layer $NbSe_2$

Among TMDs, $NbSe_2$ is of particular interest. In its 2H phase, charge density waves (CDWs) and superconductivity occur and coexist at low temperatures (below 7 K for bulk crystals), with the superconducting state and the CDW transition temperature depending on thickness [154–156]. 2H-$NbSe_2$ has been studied extensively as an exemplary system for highly correlated electronic states both experimentally and theoretically [154–158]. Its electrical and magneto-transport properties have been used at low temperatures to identify the superconducting or the CDW phase of the sample [154, 155, 159]. It has been found that when an in-plane magnetic field is applied to a few-layer $NbSe_2$, it exhibits two-fold rotational symmetry in the superconducting state as opposed to the three-fold lattice symmetry [160]. Due to its non-centrosymmetric superconductivity, few-layer $NbSe_2$ can be fabricated into superconducting antenna devices, which have shown a reversible nonreciprocal sensitivity to electromagnetic waves with a wide range of frequencies [161].

In recent years, it was discovered that islands of the 1T polymorph of $NbSe_2$, which is thermodynamically unfavorable as a bulk material [162–165], could be grown by molecular beam epitaxy (MBE) [166]. Monolayer 1T-$NbSe_2$ is believed to be a Mott insulator in its CDW state according to several scanning tunneling microscopy (STM) studies [166–168]; while one study finds it to be a charge-transfer insulator [169]. Although not a focus of this study, this stable 1T phase in the few-layer limit has sparked renewed interest in $NbSe_2$ and adds to its application potential.

Here, we conduct a study on few-layer $Nb_{1+x}Se_2$ grown by MBE on SiO_2/Si substrates. A single crystal bulk 2H-$NbSe_2$ sample grown by chemical vapor transport (CVT) was used as a reference. The MBE-grown material was characterized by X-ray

photoelectron spectroscopy (XPS) and STM. In-plane thermoelectric transport measurements of the thin film samples, including normalized electrical resistance, electrical conductivity, and Seebeck coefficient were performed over a broad temperature range and compared with the bulk sample. The understanding of the transport properties was aided by first-principles calculations as well as STM probing. Finally, the in-plane thermal conductivity of few-layer $NbSe_2$ was measured using heat diffusion imaging from 50 K to 200 K.

This project is a collaboration between several groups. The MBE samples were grown and characterized with XPS by Dr. McDonnell's group at UVa. The CVT bulk sample was provided by Dr. Davydov and Dr. Krylyuk at the National Institute of Standards and Technology (NIST). The STM measurement was performed by Dr. Reinke's group at UVa. The first-principles calculations were completed by my colleague Md Golam Rosul. I fabricated the devices and characterized their thermoelectric properties.

4.2.1 Methods

Sample Fabrication

Two batches of $NbSe_2$ samples were grown to satisfy the different measurement setup requirements. One batch was grown on 285 nm thick SiO_2/highly p-doped Si (samples S1 to S4). This substrate was chosen for optimal optical contrast. Samples S1-S4 were grown on the same piece of SiO_2 substrate, which was later diced for different measurements. Another batch of samples was on chemically grown SiO_2/intrinsic Si substrate (sample S5). The intrinsic Si substrate was required to eliminate the substrate's contribution to the Seebeck measurements as contacts are attached to the sides of the sample.

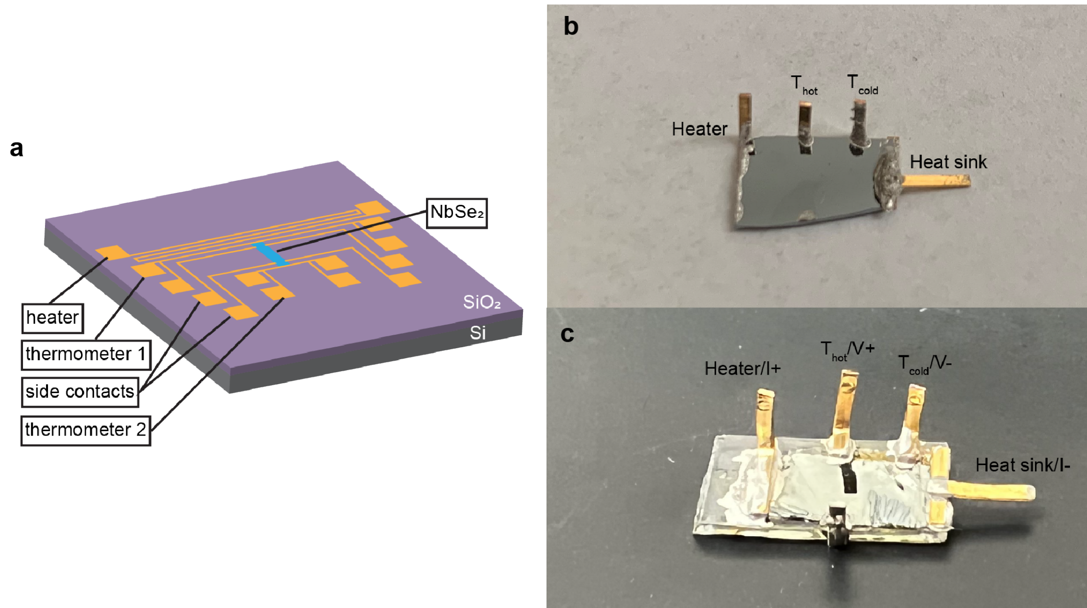

Figure 4.1: (a) Schematic of electrode configuration of devices S1-S4. Device configuration of (b) S5 (Seebeck measurement) and (c) CVT single crystal for VERSALAB thermal transport option (TTO) with each electrode noted.

Devices S1-S4 were fabricated following the same procedures with photolithography: the full coverage thin film was first etched by CF_4 plasma (30 W, 120 s) to a well-defined rectangular area, then the electrodes (5 nm Ti/50 nm Au) were deposited using e-beam evaporation (base pressure of 10^{-6} Torr, deposition rate of 0.4 Å/s for Ti and 2.0 Å/s for Au). A schematic of the device configuration is provided in Fig. 4.1(a), which includes one heater close to one end of the thin film, two thermometers on top of the ends of the film, and four side contacts. During the Seebeck coefficient measurement, the heater provides a temperature gradient, and the temperature and voltage responses are measured by the two thermometers. For 4-probe resistance measurement, current is supplied through the two thermometers and voltage is measured by the two side contacts on the same side of the sample. It is assumed that the possibly remaining Se capping layer between the contact and the $NbSe_2$ has minimum effect on the sample, since 4 probe resistance measurement should eliminate contact resistance and Seebeck coefficient is open voltage measurement.

Device S5 was fabricated to fit the measurement setup for Quantum Design VERSALAB Thermal Transport Option (TTO). A picture of the electrode configuration is provided in Fig. 4.1(b). A two-component silver-filled epoxy was used to attach the 0.5 mm wide gold-coated Cu wire contacts.

The CVT bulk device was also measured inside the VERSALAB setup using similar configuration, shown in Fig. 4.1(c). The thin NbSe2 flake was mounted on a glass substrate as added support for the electrodes.

Electrical Resistance Measurement

Standard 4-point probe configuration was used for all electrical resistance measurements. Electrical currents were sent through the contacts at the two ends of the samples, and electrical voltages were measured by the two contacts on the side of the samples, between the current leads.

Seebeck Coefficient Measurement

For S1, up to 30 mA current was supplied to the resistive heater for the temperature gradient. Temperature and voltage responses at the two ends of the sample were recorded by the two thermometers. The temperature response was acquired in form of changes in the thermometer resistances, which were then calibrated by changing the sample stage temperatures from 295 K to 310 K in a separate measurement.

For S5, the temperature dependence of the Seebeck coefficient was measured in the one-heater two-thermometer configuration employing the single-mode measurement technique of the TTO mode. One end of the sample was connected to a resistive heater while the other end was connected to the coldfoot of the sample puck. Two Cernox sensors placed along the length of the sample were used to measure the voltage and temperature difference simultaneously. An uncertainty of about 5% is estimated.

In-Plane Thermal Conductivity Measurement

In-plane thermal conductivity was measured following the HDI method [127]. A 60× Nikon objective with numerical aperture = 0.7 was used with the thermoreflectance imaging setup from Microsanj LLC. LEDs of 530 nm wavelength served as the light source. Electrical pulses of 5 ms duration, 30% duty cycle and 5 V to 10 V voltages were supplied during measurements. The temperature maps were taken at a delay time of 5 ms, which was the end of the pulse.

There is negligible change in the thermoreflectance coefficient of 2H-$NbSe_2$ in our measured temperature range with 530 nm wavelength incident light [170, 171]. It is safe to assume that the reflectivity signal changes linearly with temperature and the temperature maps obtained from thermoreflectance imaging reflect the temperature decay trends accurately. The heater temperature was closely monitored to make sure the heating was moderate and would not affect the overall sample temperature.

The reported uncertainties in the thermal conductivity values are based on an estimated uncertainty of 2% in the sample temperature and thus the referenced SiO_2 thermal conductivity value, as well as variations in the extracted β values. The standard deviation of β values was extracted from the temperature decay profiles for each temperature map. It was then combined with and averaged over values from other temperature maps at the same sample temperature, to derive the uncertainty in β. At least ten curves were taken from each map to reduce the random errors.

4.2.2 Results and Discussion

Characterization of Sample Growth

Single crystal 2H-$NbSe_2$ flakes were grown using CVT as reference samples. 4-layer thick $NbSe_2$ were grown on SiO_2 by MBE. The growth of 4L-$NbSe_2$ was characterized by in-situ XPS. The core-level spectra of the Nb 3*d* and Se 3*d* core levels can be

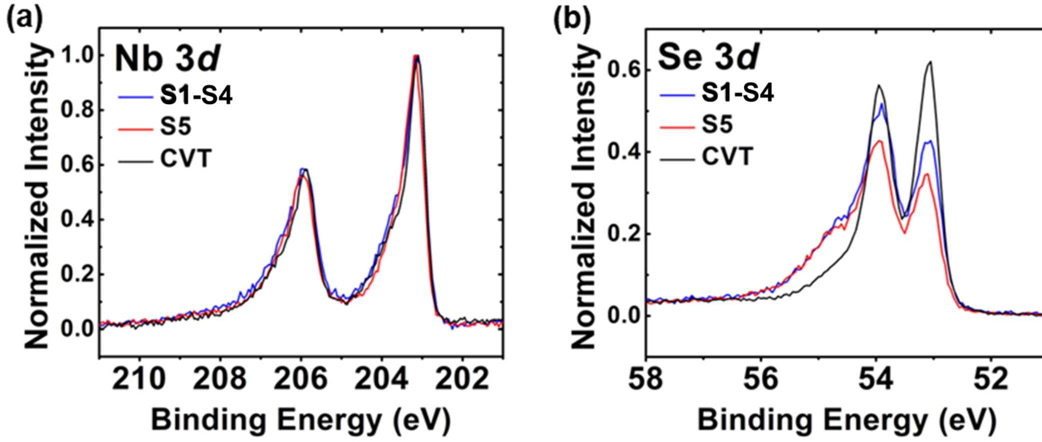

Figure 4.2: (a) Nb 3*d* and (b) Se 3*d* core levels of $NbSe_2$ in samples S1-S4 (grown on 285 nm thick SiO_2/highly p-doped Si), S5 (grown on chemically grown SiO_2/intrinsic Si substrate) and a CVT grown reference sample. Spectra are normalized to the maximum Nb 3*d* intensity for each sample.

seen in Fig. 4.2 for S1–S4 on on 285 nm thick SiO_2/highly p-doped Si substrate and S5 on chemically grown SiO_2/intrinsic Si substrate. The lineshapes of the Nb 3*d* core level as observed in XPS of the MBE-grown 4L samples are consistent with the reference CVT-grown 2H-$NbSe_2$. The Se 3*d* core level however differs from the expected lineshape of 2H-$NbSe_2$. This deviation of the Se 3*d* spectra is thought to be a consequence of intercalated Nb atoms which would change the coordination of adjacent Se atoms. In contrast, the coordination of all Nb atoms is identical, thus the deviations in the Nb 3*d* spectra are subtle. The coordination of Nb and Se atoms in the $Nb_{1+x}Se_2$ structure has been discussed previously by Selte and Kjekshus [172]. Angle-resolved photoelectron spectroscopy (ARPES) measurements were carried out on MBE thin films grown on single-crystal graphene substrates using identical growth conditions to the samples discussed here. No evidence of the expected dispersion associated with 1T-$NbSe_2$ was found, suggesting that the chemical variability in these samples is not associated with the 1T phase of $NbSe_2$ [166, 173]. The stoichiometry of the films in this work was determined to be Nb-rich when compared to our CVT reference sample

with stoichiometries of samples S1 and S5 approximating $NbSe_{1.93}$ ($Nb_{1.04}Se_2$) and $NbSe_{1.91}$ ($Nb_{1.05}Se_2$), respectively. This value was calculated using the total measured Nb 3d and Se 3d areas from XPS analysis and assuming a 2:1 Se to Nb stoichiometry for our CVT reference sample. X-ray diffraction of thicker MBE $NbSe_2$ samples grown under similar conditions suggest an expansion of the c-axis lattice parameter in our MBE grown films to 13.21 Å, 5% increase when compared to our bulk CVT grown 2H-$NbSe_2$ crystal. The expanded lattice constant along the c-axis supports the theory of Nb-intercalation suggested by the stoichiometry calculations [174]. However, the nature of the chemical variability associated with these samples is not fully understood at this time and requires further investigation.

Figure 4.3(a) is a typical surface morphology for the $NbSe_2$ surface of S5 and is observed across the entire sample. It shows a relatively large corrugation and the islands are frequently fused, growing into one another rather than in a wedding cake type structure [175] often observed for TMDs. The island size is highly variable and is between 30 nm and 90 nm albeit the complex growth does not allow to properly assess the size distribution. Additionally, there are undulations imprinted across all the layers, manifesting as brighter and darker patches within all islands independent of layer or size. The origin of these undulations is most likely related to inhomogeneities at the $NbSe_2$ – SiO_2 interface either in electronic structure or topography. The red circle in Fig. 4.3(b) highlights a screw dislocation [176], which is a feature found frequently across the entire sample surface. Fig. 4.3(d) includes at the center of the image also a screw dislocation which involves several islands. Screw dislocations have been reported previously for MoS_2 [176] and are caused by the specific initial orientation of merging islands with competing growth fronts and located on different sides of a terraces step.

The blue lines in Fig. 4.3(b) mark the position of line scans as profiles of apparent height on the surface summarized in Fig. 4.3(c). Profiles 1 and 2 are measured across

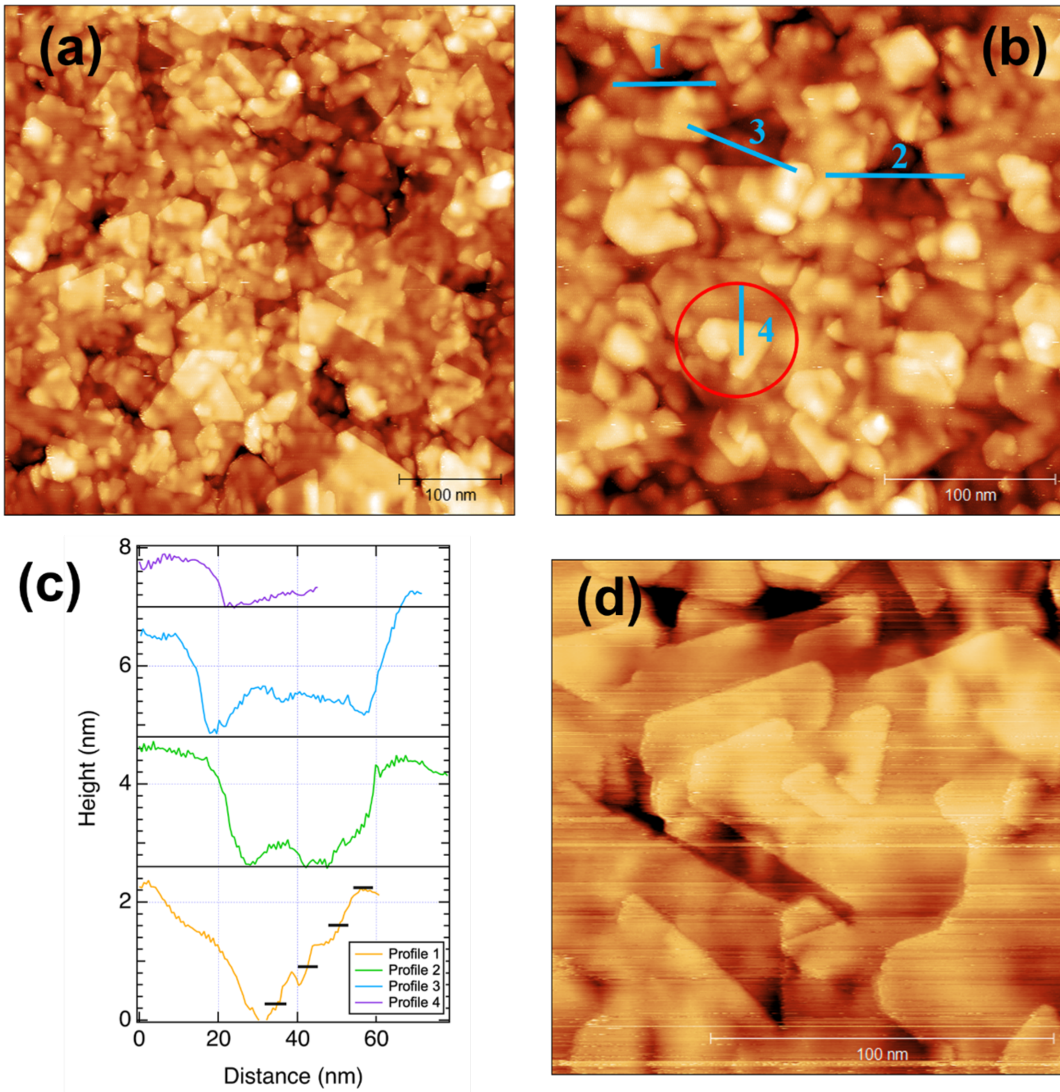

Figure 4.3: Collection of representative topography images, which capture the layer structure, and growth mode of the $NbSe_2$ on chemically grown SiO_2/intrinsic Si sample. (a) Topography image with a size of 500 nm×500 nm image, and (b) shows a topography image covering 300 nm×300 nm imaged with $V_{\text{bias}} = -0.8$ V and $I_t = 0.2$ nA. The red circle indicates a screw dislocation, and the blue lines mark line scans summarized in (c). The height of a single $NbSe_2$ layer (0.62 nm) is indicated in profile 1 with black lines for guidance. The linescans are vertically offset for illustration. (d) is a topography image with a size of 150 nm×150 nm, which also includes a screw dislocation at the center of the image.

the deepest depressions seen in the images to assess the number of layers. The depressions in profiles 1 and 2 capture the lowest-lying features in the images and are about 2.0 nm, which is commensurate with a stack of four $NbSe_2$ layers if the bottom of the

profile is assumed to be the first layer, whereas a single layer of $NbSe_2$ has a height of 0.63 nm [177]. The islands with the largest apparent height, such as the one included on the right-hand edge of profile 3, might be the onset of the fifth layer. XPS and growth data support this assignment. Additional topography images of $NbSe_2$ are included in Section 4.2.3, and visualize the contribution of the exposed first layer, which is about 10% of the surface area. Profile 4 shows an apparent height of about 0.8 nm commensurate with a single layer step. The corrugation of the layer surface and incomplete closure of the lower layers pose a significant challenge in the fabrication of few- or single-layer devices.

Electronic Structure

We used density functional theory (DFT) to study the band structure of $NbSe_2$. The band structures of bulk and monolayer 2H-$NbSe_2$ have been discussed extensively in the literature [158, 178, 179]. The band structure of these two cases and their corresponding Seebeck coefficients are shown in Section 4.2.3. As shown in Fig. 4.8, both bulk and monolayer 2H-$NbSe_2$ are metallic with Fermi levels inside the band and a small Seebeck coefficient. As expected, in the case of a monolayer, the sample is overall less metallic as a result of the shift in the band levels. It is then anticipated that regardless of the number of layers, 2H-$NbSe_2$ preserves its metallic behavior.

Figure 4.4 shows the obtained band structure and the corresponding Seebeck coefficient for 4L-$NbSe_2$. The number of layers is set to four to represent the MBE grown samples accurately. The 4L-$NbSe_2$ remains metallic and the Fermi level (zero of the energy scale) is deep inside the band. Due to the metallic nature of the sample, the absolute Seebeck values are expected to be small. As shown in Fig. 4.4, our DFT calculations predict absolute values of less than 60 μV/K for chemical potentials smaller than 0.25 eV (relative to the intrinsic Fermi level) and less than 20 μV/K for intrinsic

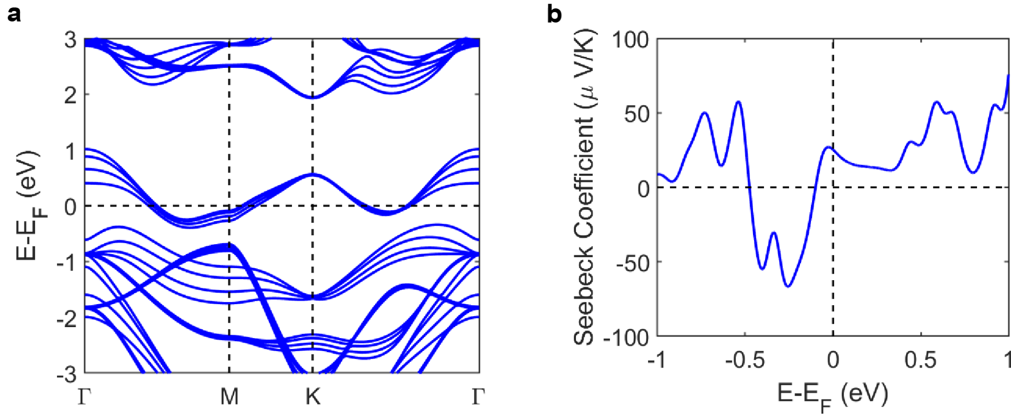

Figure 4.4: (a) Band structure and (b) room temperature Seebeck coefficient versus the chemical potential for 4L-NbSe$_2$, calculated with DFT.

samples. The exact position of the chemical potential in our MBE-grown samples is not known, since the samples are Nb rich as discussed previously. The intercalation of the Nb atoms in between the layers [180] can result in a change in the chemical potential level and consequently a change in the Seebeck coefficient. Comparing the obtained results from DFT with measured room temperature Seebeck coefficient, we conclude that the chemical potential at room temperature is slightly less than 0.1 eV below the intrinsic Fermi level. We note that the measured Seebeck coefficients for both the CVT sample and MBE grown layers are negative at this temperature.

In the DFT calculations and within the reported Fermi window, the chemical potential stays within the same band. Although the chemical potential does not move to a different band, the measured Seebeck changes sign, which is an indication that the slope of the density of states with respect to energy changes sign within the reported window. Since the samples are metallic, we can assume that the number of free carriers do not change with temperature. Our calculation shows that the carrier concentration of these samples is $4.3 \times 10^{21}\,\mathrm{cm}^{-3}$. Fixing the carrier concentration, we can calculate the Seebeck coefficient of the samples with respect to temperature. The calculated Seebeck coefficient values are shown in Fig. 4.5 and are in close agreement with the

experimentally measured values. The slight differences could be associated with the constant relaxation approximation used in these calculations and slight changes in the carrier concentrations which were not included. Overall, the DFT results agree with the experiments, in terms of the values and the trend with respect to temperature.

The metallic nature of the samples is further confirmed using STM and measurements of the dI/dV, which is an indirect measure of the local density of states (LDOS). As shown in Section 4.2.3, dI/dV values are finite at various locations around the Fermi level. However, the lower islands (closer to the substrate) of the sample have smaller LDOS values compared to higher islands (closer to the top surface) and appear less metallic which is consistent with layer-dependent modifications of the LDOS.

Finally, the resistance of these samples cannot be obtained using constant relaxation time approximation. The relaxation times change significantly with temperature and while these changes do not affect the Seebeck coefficient, the resistance is inversely proportional to the mobility and is heavily influenced by the changes in the temperature. The major electron scattering for metals is due to acoustic phonons. The elecron-phonon scattering rate in this case increases linearly with temperature, and can be modeled as $S_{e-ph} \propto g(E)$ [181], where $g(E)$ is the density of states at energy E. Using this assumption and our privous assumption of constant carrier concentration with respect to the temperature, we can calculate the changes in the normalized resistance with respect to temperature. The results are shown in Fig. 4.5 and are in close agreement with experiment. In the next two sections, we discuss the experimental results in more details.

Normalized electrical resistance and electrical conductivity

The temperature dependence of the normalized four-point resistance, $R(T)/R(300\,\mathrm{K})$, is shown in Fig. 4.5(a) for device S1 and the CVT single crystal reference sample.

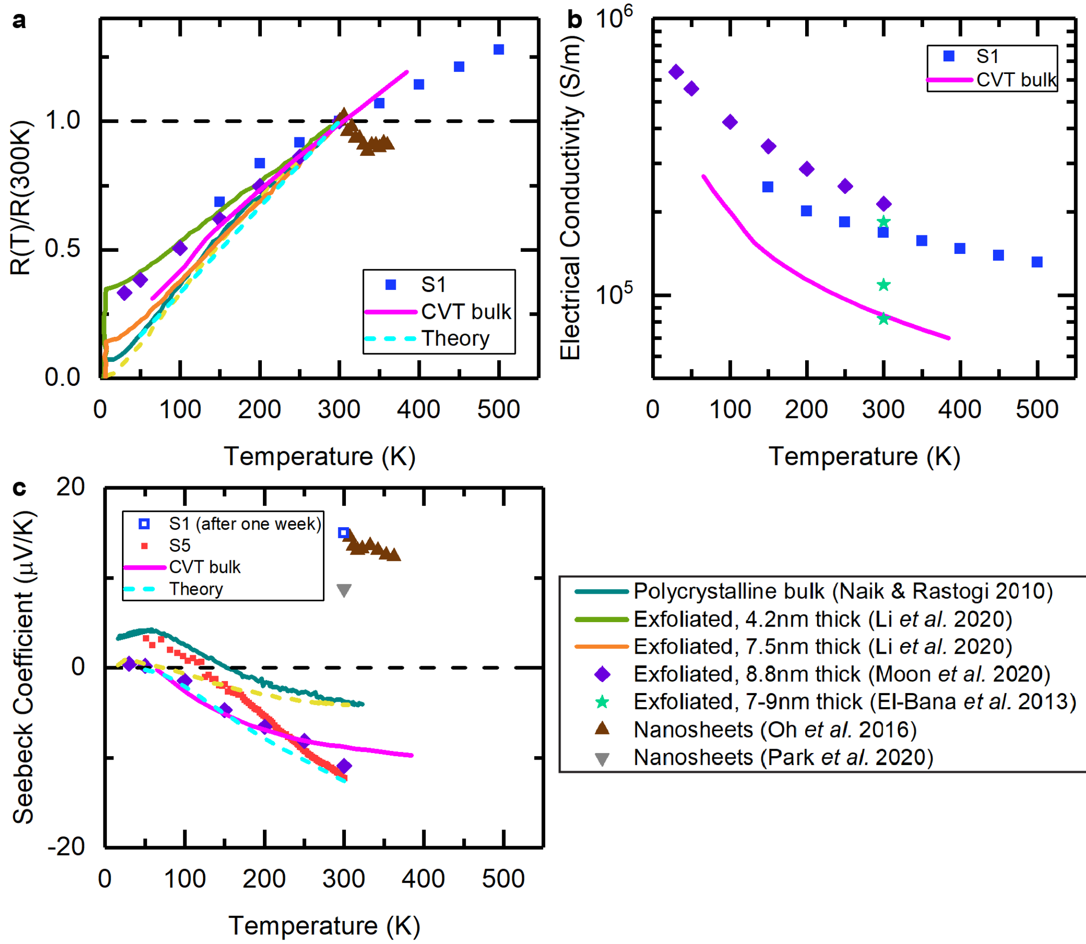

Figure 4.5: Temperature-dependent electrical resistance and conductivity measurements, as well as Seebeck coefficient. (a) Normalized resistance of samples S1 and the CVT bulk reference sample, (b) electrical conductivity of S1 and the CVT sample, and (c) Seebeck coefficient of S1 (after one-week exposure to air) and S5, compared with the CVT sample, theoretical calculations and literature data [182–186]. Note that oxides were detected in the nanosheet samples and they were showing insulating behavior and a positive room temperature Seebeck coefficient [183, 185].

S1 was fabricated from $NbSe_2$ film grown on 285 nm thick SiO_2/highly p-doped Si substrate, using photolithography and e-beam evaporation for electrodes. It had a thickness of 2.93 nm, corresponding to 4 layers estimated from XPS data. This device was measured inside a home-built JANIS cryostat system. The Se capping layer used to protect the samples in the atmosphere was removed at 500 K under vacuum

($\sim 10^{-6}$ Torr), prior to measurements. Data on more devices (S2 and S3) can be found in Section 4.2.3.

Theoretical calculations for 4L-$NbSe_2$, literature data for bulk [182] and few-layer $NbSe_2$ samples [183–186] are plotted alongside data from this work for comparison in Fig. 4.5. The thin film sample S1 was measured from 150 K to 500 K, while the single crystal bulk sample was measured from 50 K to 400 K. The samples are purely metallic, and their resistances are an increasing function of temperature. Their rates of change with respect to temperature match well with theory and those from the literature (except the heavily oxidized nanosheet samples made by chemical exfoliation).

Fig. 4.5(b) shows the temperature-dependent electrical conductivity. At room temperature, S1 has a conductivity of around 1.68×10^5 S/m, which is slightly smaller than that of the thicker exfoliated flake [187]. In comparison, the CVT single crystal sample has an electrical conductivity that is about half of that value.

The electrical properties of $NbSe_2$ are highly sensitive to the growth method, to the device fabrication protocols and to the ambient conditions. As illustrated in the case of the $7 - 9$ nm thick exfoliated flakes [186], even when they were fabricated following the same procedures, their room temperature conductivity varied from 8.2×10^4 to 1.8×10^5 S/m. The electrical conductivities of S1 and the CVT sample are within the range of the reported values. In order to better understand the samples, we performed Hall measurements on the CVT bulk sample. Its Hall carrier concentration was measured to be around 4.1×10^{21} cm^{-3} at room temperature, which is very close to the theoretically estimated value of the 4L sample. The exfoliated flakes reported in literature [186, 187] were made from high quality single crystals and thus we assume they had a high structural quality similar to the CVT sample and a similar carrier concentration. The main difference between the samples is most likely their mobility. Bulk and few layer $NbSe_2$ are reported to have room temperature mobility in the range of $0.5 - 3$ cm^2/V·s [188, 189] and there is no clear thickness dependence. The Hall

mobility of the CVT sample was calculated as 1.7 cm^2/V·s, within this reported range. The 8.8 nm thick flake [187] is expected to have a high mobility of close to 3 cm^2/V·s based on its high electrical conductivity. Although S1 is comprised of many islands, it shows higher mobility than the CVT single crystal. The carrier mean free path in 4L $NbSe_2$ was estimated to be about 20 nm at 50 K limited by the thickness [190], and should drop significantly at higher temperatures due to electron-phonon scattering. In comparison, the islands of S1 are between 30 and 90 nm in size. Their impact on carrier mobility is minimal and the mobility of S1 remains high.

Seebeck coefficient

The temperature dependent Seebeck coefficient for device S5 and room temperature value for S1 (which was exposed to air for one week after electrical conductivity measurements) are presented in Fig. 4.5(c), together with the CVT reference. Device S5 was fabricated from $NbSe_2$ grown on a few-nm-thick chemically grown SiO_2/intrinsic Si substrate and gold-copper electrodes were attached to the sides of the sample for measurements inside a commercial VERSALAB system. Its Se capping layer was removed at 400 K under vacuum before measurements.

The Seebeck coefficient of S5 starts from around $-12\,\mu$V/K at room temperature, gradually increases as the temperature goes down, eventually crosses over to a positive value around 120 K, and continues to increase to about $+3\,\mu$V/K at 50 K. The values and the overall trend agree well with the CVT bulk sample, as well as reference data for 2H bulk and exfoliated thin flake samples [182, 187]. For single-crystal samples, whether as a bulk crystal or as a few-nm thick exfoliate flake, the negative-to-positive crossover temperature is around 50 K [182, 187]. However, this temperature increases to about 120 K for the polycrystalline thin film S5 and about 150 K for the referenced polycrystalline bulk sample [182]. The grain sizes and boundaries might have some effect on this crossover temperature, which could be of value for further investigation.

The theoretical Seebeck coefficient of 4L-$NbSe_2$ follows a similar trend and approaches zero as the temperature goes to 50 K. The behavior matches the single crystal data well, since a perfect crystal has been assumed in the calculations. This provides further evidence to our speculation that grain boundaries can modulate the Seebeck cross-over temperature.

It is interesting to note that a positive room temperature value of around +15 μV/K was obtained for S1 after being exposed to air (kept in a desiccator after Se cap removal) for roughly a week, while the S5 sample, which was not exposed, has a negative Seebeck coefficient at room temperature. The observed positive Seebeck coefficient matches the reported values for $NbSe_2$ nanosheet samples [183, 185], in which the existence of oxide Nb_2O_5 has been confirmed by XPS measurements. Although the exact oxide content of S1 at the time of the measurement was not known, its resistance was orders of magnitude higher than before and other samples (S2 and S3) measured in the same week showed insulating behavior. The temperature-dependent normalized resistance of S3 matches that of the oxidized nanosheet [183] above room temperature. Oxidation seems to be a major factor leading to these positive values.

Thermal Conductivity

The thermal conductivity of device S4 (fabricated in the same batch as S1) was measured using heat diffusion imaging method at low temperatures. Heat diffusion imaging is an electrical-pump optical-probe method based on the thermoreflectance technique. In-plane thermal conductivity of a supported thin film is extracted by fitting the temperature decay in the longitudinal direction to an exponential function according to the heat spreader model.

As shown in Fig. 4.6, the thermal conductivity rises to a maximum of about $(53 \pm$

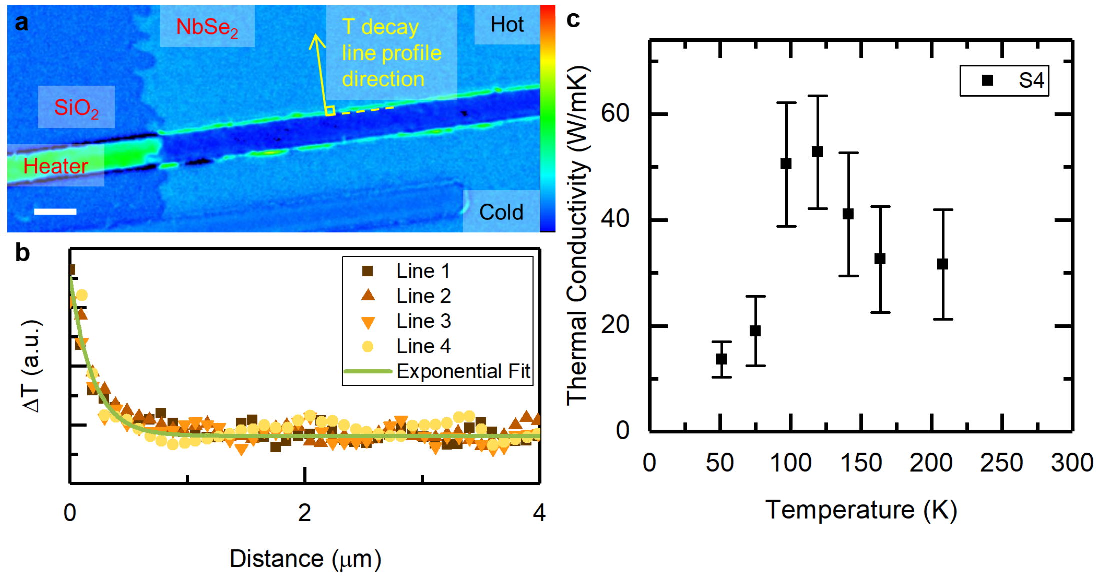

Figure 4.6: (a) Example temperature map at 50 K, (b) example temperature decay curves taken from (a) and their corresponding exponential fitting curve, and (c) temperature-dependent in-plane thermal conductivity from 50 K to 210 K for device S4. The scale bar in (a) is 5 μm. The same thermoreflectance coefficient is assumed for the entire sample surface, since only how the temperature decays with distance affects the extracted thermal conductivity, not the absolute temperature values.

$11)\,\mathrm{Wm^{-1}K^{-1}}$as the temperature increases from 50 K to 120 K, then gradually decreases and almost reaches a plateau of $(32 \pm 10)\,\mathrm{Wm^{-1}K^{-1}}$as the temperature gets closer to room temperature at 200 K. Although the sample was metallic, Wiedemann-Franz law estimated the electronic thermal conductivity to be about $1.5\,\mathrm{Wm^{-1}K^{-1}}$at 200 K, comprising less than 5% of the total value. The thermal transport was dominated by phonons. More phonon-phonon scattering is expected with increasing temperature and therefore leads to shorter temperature decay length. Our measurement at higher temperatures was limited by optical resolution. This increasing then decreasing trend in thermal conductivity with respect to increasing temperature resembles that in a previous report on bulk $NbSe_2$ [191], although the maxima occur at different temperatures and the overall thermal conductivity is surprisingly larger than the bulk

equivalent. The largest thermal conductivity is reached at 120 K for the 4L $Nb_{1+x}Se_2$. In another few-layer TMD, 4L-MoS_2, the largest thermal conductivity also occurs at around 120 K, where the behavior below 120 K is attributed to phonon-boundary scattering and that above 120 K is attributed to phonon-phonon scattering [192]. To the best of our knowledge, this is the first in-plane thermal conductivity measurement of few-layer $NbSe_2$ samples in this temperature range. However, a room temperature value of $(15 \pm 4)\,\mathrm{Wm^{-1}K^{-1}}$for exfoliated 2H-$NbSe_2$ flakes (about 20 nm to 25 nm thick) using the Raman method was reported in a recent master's thesis [193].

Power factor, PF, and thermoelectric figure of merit, zT

A discussion on the two parameters used to characterize a material's thermoelectric performance, PF (σS^2) and zT ($\sigma S^2 T/k$), is called for since the temperature-dependent measurements of their constituents, i.e., electrical conductivity σ, Seebeck coefficient S and thermal conductivity k, have been performed. Although a thermal conductivity value could not be obtained at room temperature, PF and zT values of the few-layer samples are expected to be small due to the small Seebeck value (about $-12.3\,\mu$V/K). The room temperature PF is slightly smaller than that of the oxidized $NbSe_2$ nanosheets reported by Oh et al. [183]; but is 3 times as high as that from Park et al. [185] and 4 times that of the CVT reference sample. If we take the thermal conductivity value at 200 K as the room temperature value, zT is estimated to be on the order of 10^{-4}. As temperature decreases, although the electrical conductivity gets higher, the absolute Seebeck coefficient becomes too close to zero to yield better PF or zT.

4.2.3 Additional Data

Electrical Conductivity of More Devices

Devices S1-S3 were fabricated in the same batch, however, measured some time apart. S2 was measured right after S1 in the same week and S3 was measured the following week. Unmeasured devices were kept inside a vacuum desiccator with the Se capping layer. As the resistance and the conductivity data show, S1 is metallic while S2 and S3 became more semiconducting. This suggests that although the Se cap was enough to protect the samples, especially during the fabrication process, the few nm thick protection layer was not impenetrable and oxidation began to happen after some time.

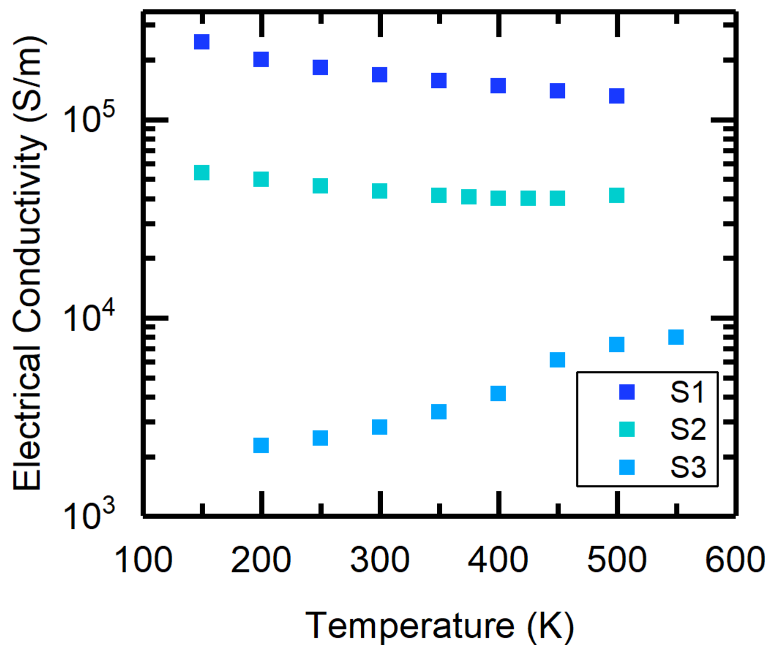

Figure 4.7: Electrical conductivity of devices S1, S2 and S3, plotted against temperature.

Electronic structures and Seebeck coefficients of bulk and monolayer $NbSe_2$

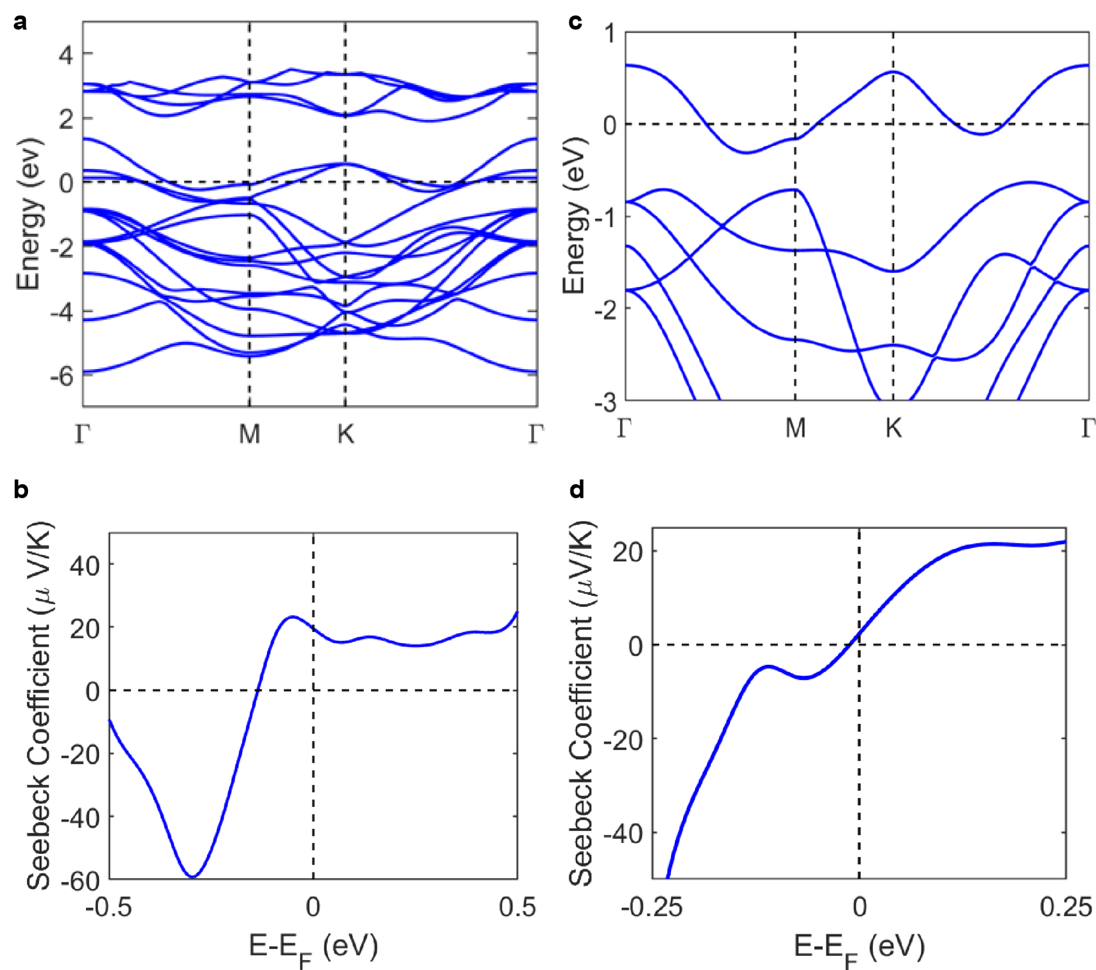

Figure 4.8: Band structures and room temperature Seebeck coefficient versus the chemical potential for $NbSe_2$, calculated with DFT. (a) Band structure and (b) Seebeck coefficient of bulk 2H-$NbSe_2$. (c) Band structure and (d) Seebeck coefficient of monolayer 2H-$NbSe_2$.

Scanning Tunneling Spectroscopy Analysis

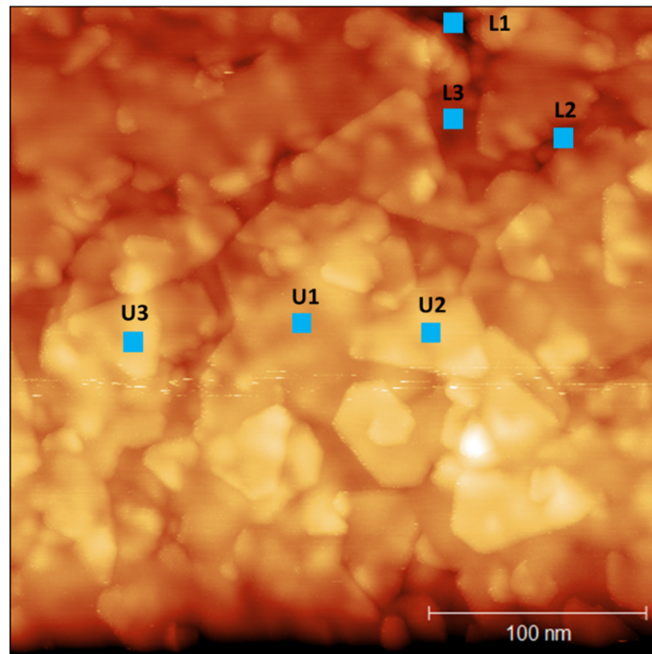

Figure 4.9: A 300 x 300 nm STM image taken at $V_{\text{bias}} = 0.45\,\text{V}$ and $I_{\text{t}} = 0.2\,\text{nA}$. The blue boxes represent the approximate area in which STS curves were taken from the overall grid. "U" refers to "upper" islands, while "L" refers to "lower" islands. Blue boxes are not to size.

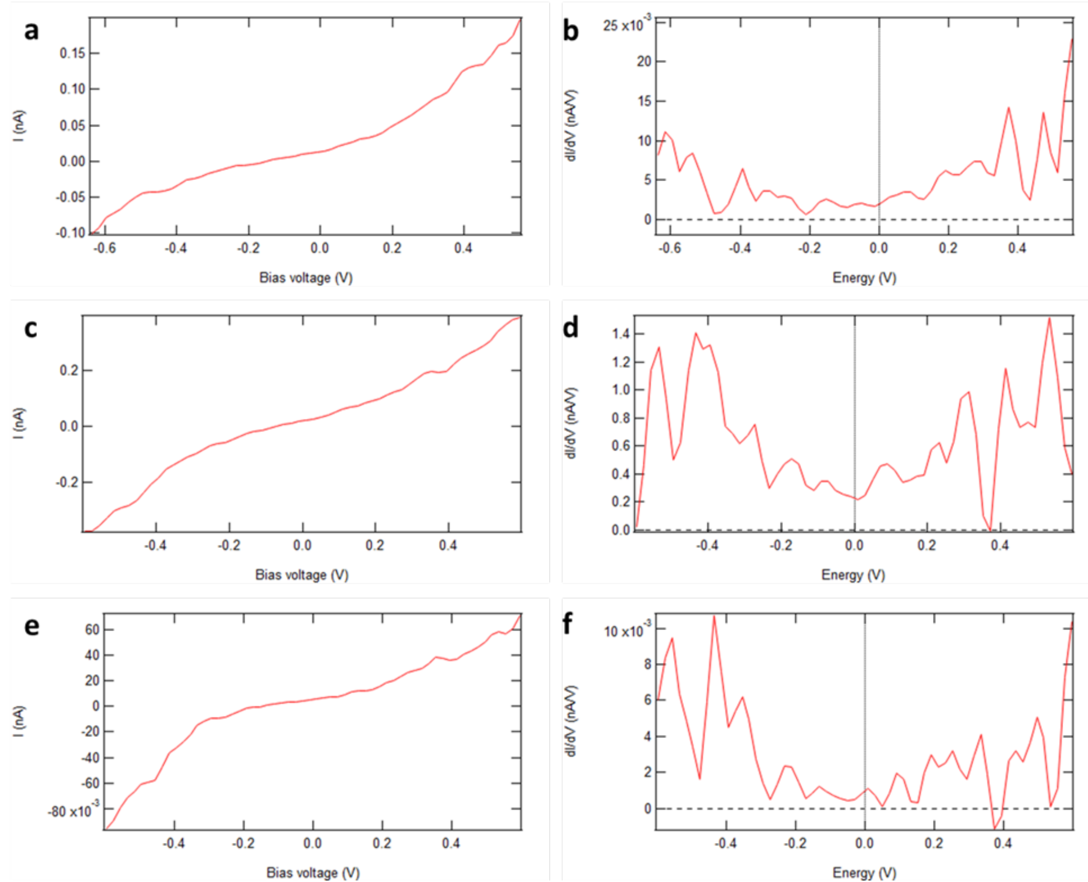

Figure 4.10: I/V and dI/dV curves for spectroscopy data from "islands" taken closer to the "highest" surface of the sample. (a), (c), and (e) show the averaged I/V curves taken at three different upper islands, while (b), (d), and (f) show the averaged derivatives. The dI/dV curves in this case are proportional to the density of states at those locations on the sample. The Fermi level has been marked on graphs (b), (d), and (f). From these graphs one can see that the sample is largely metallic in character, as in (b). In (d) and (f) the sample has a smaller local density of states at E_F. STS data was acquired by sweeping V_{bias} from 1 to -1 V at image size 300 $\times$ 300 nm, acquiring curves at every second pixel. The area probed with STS is then about 300/512 nm/pixel.

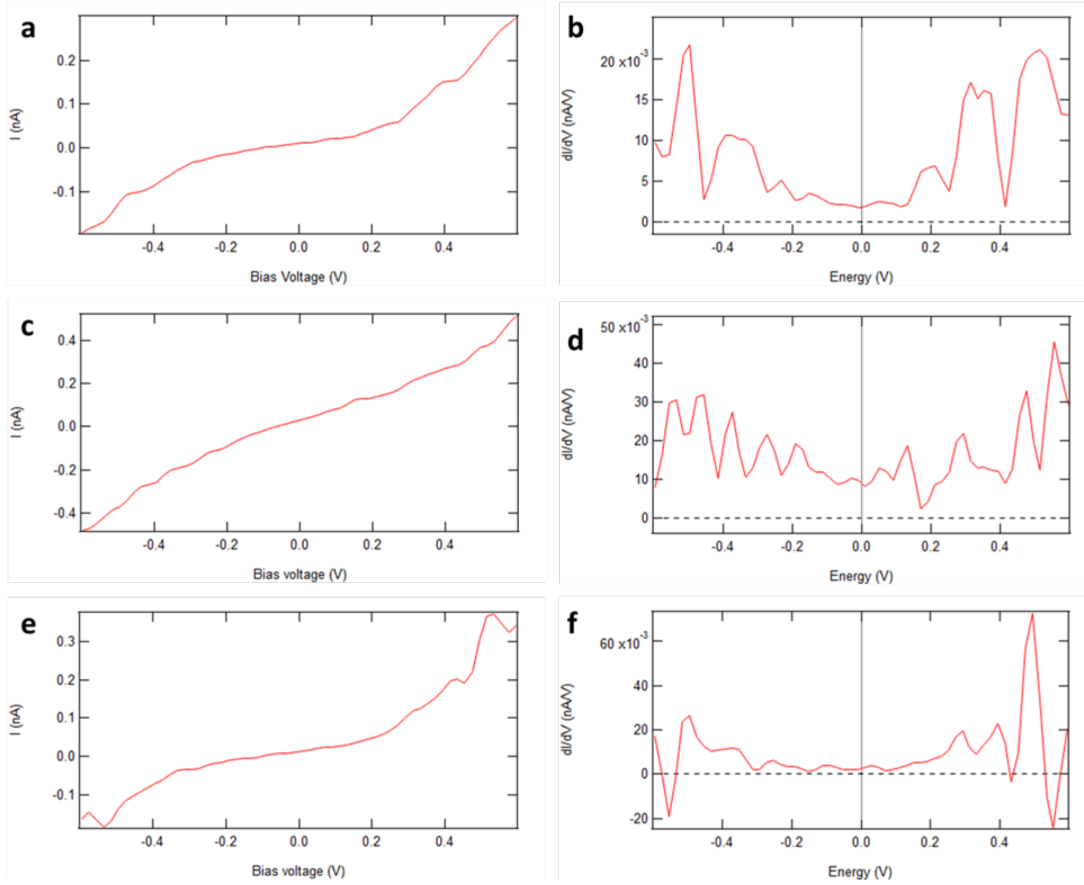

Figure 4.11: I/V and dI/dV curves for spectroscopy data from “islands” (topography image sections) which are the lowest lying sections and hence closer to the substrate of the sample. We assigned these as the 1st layer in the topography image write-up. (a), (c), and (e) again show the I/V curves of the three lower islands, while (b), (d), and (f) show the derivatives of these curves. Again, the Fermi level has been marked where relevant. (b) and (d) show fully metallic characteristics, while (f) has a somewhat lower density of states at E_F. Note that because these areas are rather small, and with a steeper sidewall, we might have some contributions from the $1 + n$ islands to the STS characteristics (side of tip interacts).

4.2.4 Conclusion

In summary, we have demonstrated the growth of few-layer $NbSe_2$ by MBE on SiO_2. Using In-situ XPS we showed these thin films were Nb-rich $Nb_{1+x}Se_2$. The extra Nb atoms were possibly intercalated between the layers resulting in a larger separation of the layers. The STM confirmed the metallic nature of the samples, however, it also showed that the samples were inhomogeneous and had lower LDOS closer to the substrate. The metallic nature of the four layer sample was also confirmed with DFT calculations. Theoretical Seebeck coefficients as well as the normalized resistance were calculated with respect to temperature, and agreed well with experiments.

Several devices were fabricated from full-coverage $NbSe_2$ thin films for measurements of their in-plane thermoelectric properties across a wide temperature range. It was observed that exposure to air and oxidization changed the Seebeck coefficient from a small negative number to a positive number with a larger absolute value. However, it resulted in a significant drop in electrical conductivity. The Seebeck coefficient of the few-layer $NbSe_2$ (prior to oxidization) had a very similar trend as that of the single crystal CVT sample. However, the transition temperature wherein the sign of the Seebeck changes was different. Despite the Se deficiency and the many islands which introduce extra scattering, the MBE-grown samples show higher electrical and thermal conductivity values compared to single-crystal 2H bulk samples. While the larger electrical conductivity could be attributed to larger carrier concentrations, it is difficult to explain the larger thermal conductivity and the latter should be the subject of future investigations. These measurements open up dialogues about the transport properties of few-layer $NbSe_2$ and should be considered a step towards the optimization of $NbSe_2$ for device applications.

The results in this section have been published in *Materials Today Physics* [194].

4.3 In-Plane Thermoelectric Transport of 2H-MoTe$_2$

As presented in Section 1.4, extensive research efforts have been made towards 2D MoS_2 for thermoelectric applications. $MoTe_2$ is another molybdenum-based TMD material that is air-stable. So far, the research interests on 2D $MoTe_2$ have mostly come from electronics [91, 124, 195, 196] and optoelectronics [124, 197] considerations but not from a thermoelectric perspective.

$MoTe_2$ has a semiconducting 2H phase, where the band gap changes from an indirect gap of 0.83 eV in the bulk form to a direct gap of 1.1 eV in the monolayer form [198, 199]. Seebeck coefficient of n-type single crystal bulk $MoTe_2$ was measured to be around $-400\,\mu$V/K from 77 K to 300 K [200]. 330 nm thick 2H-$MoTe_2$ thin films were prepared by magnetron co-sputtering and showed a maximum power factor of 0.33 mWm^{-1}K^{-2} (3.3 μWcm^{-1}K^{-2}) at 460 K for p-type and 0.82 mWm^{-1}K^{-2} (8.2 μWcm^{-1}K^{-2}) at 670 K for n-type samples. These studies indicate that 2H-$MoTe_2$ can be a potential candidate for good thermoelectric materials, especially in the few layer limit when band structures change due to quantum confinement.

In this section, I fabricate exfoliated 2H-$MoTe_2$ samples on SiO_2/Si substrate that are about 10 nm thick and measure their in-plane thermoelectric transport properties.

4.3.1 Methods

Thin 2H-$MoTe_2$ flakes were exfoliated onto 300 nm SiO_2/highly-doped Si substrates by the Scotch tape method. The substrates were pre-cleaned by acetone and isopropanol sonication, followed by annealing at 400 °C in forming gas (5% H/95%Ar). $MoTe_2$ single-crystalline bulks were grown by CVT method by Dr. Davydov and Dr. Krylyuk at NIST. The standard thermoelectric electrode patterns were prepared using laser lithography (385 nm), and flakes with a uniform thickness of about 10 nm were chosen according to optical contrast. Individual design patterns were prepared for each

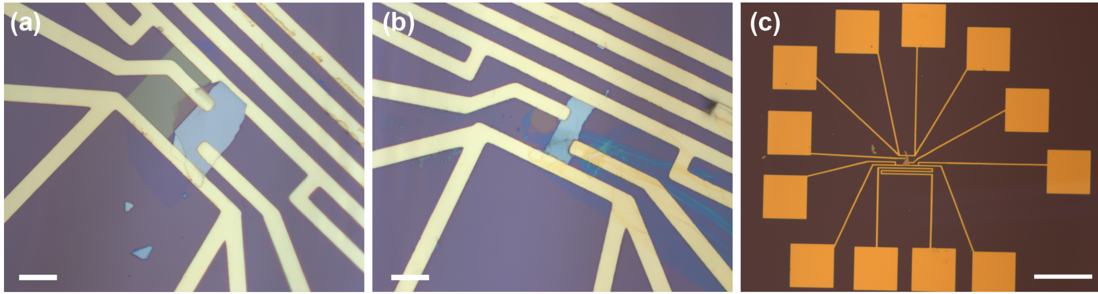

Figure 4.12: Optical images of two $MoTe_2$ samples, (a) S1 and (b) S2, after etching and (c) the electrode design. The scale bars in (a) and (b) indicate 10 μm and that in (c) is 200 μm.

flake to accommodate the different sizes and shapes. Both positive (AZ 5209) and negative (nLOF 2020) resists were tested for optimizing lithography and lift-off processes. Dosage tests were performed to find the operating parameters for each resist. The minimum feature size that can be reliably produced is 4 μm.

5 nm Ti and 100 nm Au were evaporated as contact metals (base pressure below 10^{-5} Torr, 1 Å/s). The electrodes were lifted off by overnight acetone soak for the positive resist or by heated propylene glycol/N-Methyl-2-pyrrolidone (NMP) bath for the negative resist. The shape of each flake was identified under a microscope and subsequently etched to a rectangular shape by opening etch windows with laser lithography and then reactive ion etching (RIE) with SF_6 (30W) for up to a minute. Optical images of two samples are shown in Fig. 4.12(a) and (b). Exposure to air during the fabrication process might cause some surface oxidation, but the oxidation is expected to only occur in the top two or three layers on the surface and the bulk of the 10 nm thick flake remains intact [201]. The samples were kept inside an Ar-filled glovebox and annealed in high vacuum ($\sim 10^{-6}$ Torr) at 600 K prior to measurements to minimize effects from environmental contamination.

As shown in Fig. 4.12(c), the electrode configuration is similar to the one used in Section 4.2 for the $NbSe_2$ samples, which includes one heater close to one end of the flake and two thermometers on top of the ends of the flake for the Seebeck coefficient

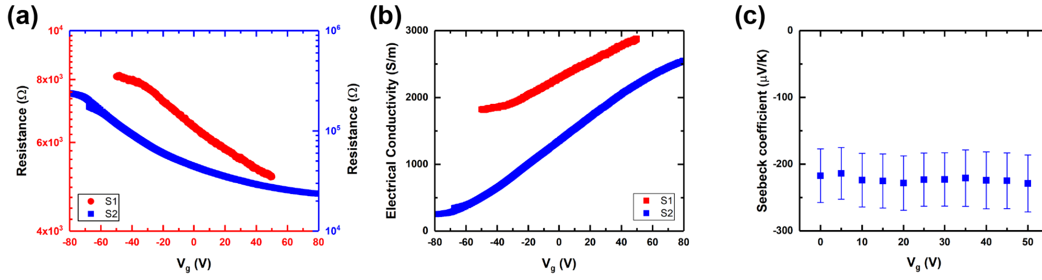

Figure 4.13: (a) Resistance, (b) electrical conductivity and (c) Seebeck coefficient of thin 2H-MoTe$_2$ samples measured as a function of V_g at room temperature.

measurement. However, limited by the sample size and the minimum feature size of the lithography technique, only two side contacts could be patterned, with one on each side. The 3-fold heater is about 200 μm long. Up to 30 mA current is passed through the heater during measurements and the generated Seebeck voltage is recorded by the nanovoltmeter Keithley 2182A. Sourcemeter Keithley 2401 measures the four-probe resistance and Keithley 2400 applies a back gate voltage, V_g, between the highly doped Si substrate and the sample. The leakage current from the back gate should be limited to a few nA up to 100 V for a good quality sample. The measurements have been performed in a vacuum to protect the samples.

4.3.2 Results and Discussion

The four-probe resistance of the two samples was measured while varying V_g and is shown in Fig. 4.13(a). Sample S1 had a smaller resistance of around $6\times10^3\,\Omega$ without application of V_g and changed by about 30% with V_g between -50 V and 50 V. Sample S2 had larger resistance around $4\times10^4\,\Omega$ without back gate doping, which is one order of magnitude higher than that of S1. As V_g was swept from -80 V to 80 V, its resistance varied by one order of magnitude. Both samples exhibited n-type behavior, as the resistance lowered with increasing gate voltages. The electrical conductivity is provided in Fig. 4.13(b), after AFM scans determined the thicknesses of S1 and S2 to be around 25 nm and 150 nm respectively. While S1 had higher resistance than S2,

their conductivity values are similar due to the large difference in thickness.

The Seebeck coefficient of S2 was measured at different V_g and has been plotted in Fig 4.13(c). The negative Seebeck coefficient confirmed the n-type behavior of the samples. The Seebeck voltage detection in the entire measurement range was noisy. When negative V_g was applied, the measured Seebeck voltage became noisier. At large negative values, an offset open voltage was detected even when the heater was off, which should have been close to zero. Similar behaviors have been observed and explained in semiconducting 2D MoS_2 [85]. According to their analysis, when the semiconductor channel resistance became too high, resistive coupling from the back gate to the channel would have caused the offset voltage. The input bias current up to 120 pA from the nanovoltmeter also contributed to the offset and noises, which was mentioned in the case of the 2D MoS_2 [85] and of a Si metal-oxide-semiconductor FET (MOSFET) with high resistance [202]. Due to the noisy signals, although we expected lower Seebeck coefficient with higher electrical conductivity, within the $V_g = 0 - 50$ V range, no significant change in the Seebeck coefficient was observed.

Surprisingly, to the best of my knowledge, there has not been any experimental investigation of the in-plane thermal conductivity of $MoTe_2$ regardless of bulk or few-layer form, but only a cross-plane study on few-layer $MoTe_2$ using TDTR [203], which shows a thermal conductivity of 1.5 $\mathrm{Wm^{-1}K^{-1}}$at 300 K. DFT calculations estimated the in-plane lattice thermal conductivity for monolayer $MoTe_2$ to be around 60 $\mathrm{Wm^{-1}K^{-1}}$at room temperature [204]. HDI was performed to a third sample S3 with 5 V, 5 ms pulses to the heater to extract the in-plane thermal conductivity. S3 was about 25 nm thick. An optical image of the sample as well as a thermoreflectance map is provided in Fig. 4.14. A in-plane thermal conductivity of 9.8 ± 3.7 $\mathrm{Wm^{-1}K^{-1}}$was obtained.

The peak power factor occurs at high positive gate voltage because of the reduction in the resistance. Compared to the intrinsic sample under no back gate bias, the power

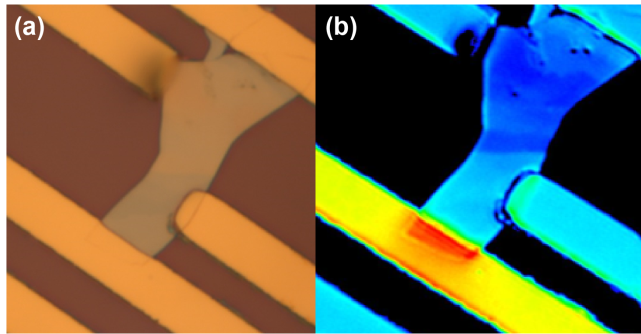

Figure 4.14: (a) Optical image and (b) thermoreflectance image (5 V, 5 ms) of thin 2H-MoTe$_2$ sample S3 at room temperature. The width of the electrodes is 4 μm.

factor improves by 63% at $V_g = 50\,\mathrm{V}$, which could further increase to by 89% at $V_g = 80\,\mathrm{V}$ assuming that the Seebeck coefficient stays almost constant. The peak PFT reaches about 0.04 $\mathrm{Wm^{-1}K^{-1}}$and the zT is about 0.004. Although the samples were annealed in vacuum prior to measurements for a better electrical contact, the electrical conductivity still has room for improvement. Different contact metals and different substrate (hBN) might help to enhance PFT and zT.

Regrettably, both S1 and S2 were burnt due to a malfunctioning shunt box before more measurements were taken and S3 did not have a complete set of electrodes after metal lift-off. These room temperature thermoelectric characterizations of thin 2H-MoTe$_2$ hopefully have opened up dialogues about a more thorough examination of semiconducting TMDs for thermoelectric applications. Much of the research focus on MoTe$_2$ has been on the controlled phase transitions between the 2H, 1T' and T$_\mathrm{d}$ phases for memristor applications [59, 205].

4.4 Cross-Plane Thermoelectric Characterization of Few-Layer WSe_2-Contact Interfaces

WSe_2 has attracted attention both as a thermoelectric device in the in-plane direction and as a thermionic device in the cross-plane direction [206, 207], due to its low thermal conductivities in the two directions [81, 208]. Engineering 2D devices for energy conversion applications, as well as transistors and optoelectronics, requires an understanding of the chemical and electronic interactions at the metal contact/WSe2 interface. Interfaces are important in bulk thermoelectric modules [209, 210] and they carry a even more significant role in the 2D devices, as the device performance at nanoscale is dominated by the interfacial electrical and thermal resistances. Interface chemistry of WSe_2 and a few metal contacts including Au, Ir, Cr, Cu, Ag and Pd has been studied [211–213]. Although Ti contacts have been used in WSe_2 transistors [214, 215], there has been no report on the Ti/WSe_2 interface and its thermoelectric response.

4.4.1 Experimental Setup

The WSe_2 samples for this work were grown on highly oriented pyrolytic graphite (HOPG) substrate by MBE in Dr. McDonnell's lab at UVa. Different contacts of Ti, TiO_x, and Ti/TiO_x were deposited on top of the WSe_2 films and capped with a thin layer of Au. The interface chemistry was characterized using XPS.

A schematic of the Seebeck coefficient measurement setup is shown in Fig. 4.15. The sample consists of metal contact, WSe_2 film and HOPG, structured from top to bottom. Certain areas of the HOPG substrate are exposed for easy placement of probes. For the cross-plane measurement of the Seebeck coefficient, a thermoelectric module was placed beneath the HOPG substrate to provide a vertical temperature gradient across the sample. A set of voltage probe and type K thermocouples (probe A and TC

A) was placed on the metal contact covering the WSe_2 film and the other set (probe B and TC B) was placed on the exposed HOPG region. Here, the Seebeck voltage was measured by a Keithley 2400 source meter and the temperatures signals were converted by a NI 9211 temperature input module from National Instruments. The Seebeck coefficient can then be obtained from the slope of a linear fit of $-\Delta V$ against ΔT using the relation $S = -\Delta V/\Delta T = -(V_{stack} - V_{HOPG})/(T_{stack} - T_{HOPG})$.

The standard 4-point probe geometry was used for resistance measurement by replacing the two pairs of thermocouples with two current probes. By use of this approach, the probe-to-sample contact resistance was eliminated, which, in this case, was orders of magnitude higher than the actual resistance of the sample.

4.4.2 Results and Discussion

The electrical resistance and the Seebeck coefficient of the Au/Ti and Au/TiO_x samples were averaged over measurements at four randomly selected locations across the sample surface, so that the effects from non-uniformity of the HOPG substrate [216] and the film were minimized. The sample properties were monitored over a week to

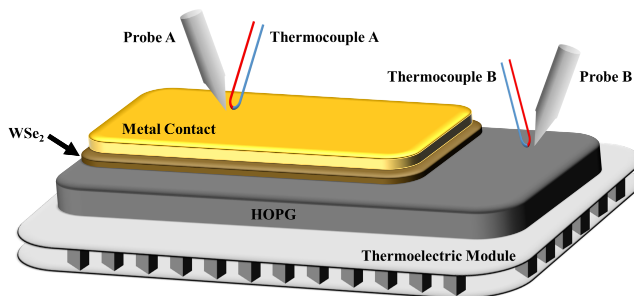

Figure 4.15: A schematic showing the measurement setup for the cross-plane Seebeck coefficient of the WSe_2 sample grown on HOPG by MBE. A thermoelectric module is placed beneath the HOPG substrate to provide the required temperature gradient. Two sets of probe and thermocouple are placed on the exposed HOPG and the metal contact/WSe_2 stack respectively to measure voltage and local temperature.

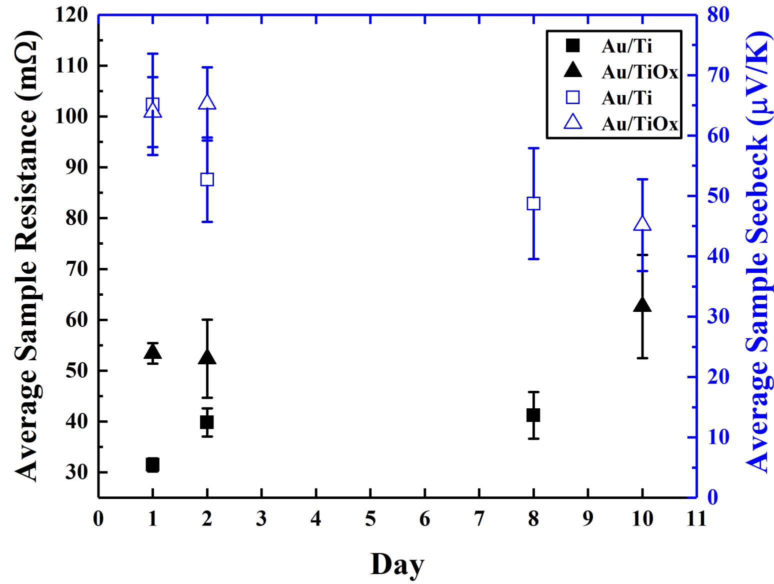

Figure 4.16: Average resistance and average cross-plane Seebeck coefficient of WSe_2 layers capped with Au/Ti and Au/TiO_x, plotted against time. The solid symbols represent the resistance data and the empty symbols are for the Seebeck data.

check for changes in behavior that could occur as a result of the exposure to air and moisture as well as the measurements.

As shown in Figure 4.16, the Au/TiO_x sample has a higher electrical resistance compared to the Au/Ti sample. The TiO_x layer will likely pose a tunneling barrier between the Au and the WSe_2 valence band, which is not present in the case of a Ti interlayer, making it more difficult for the electrons to tunnel from HOPG to Au and increasing the resistance. A speculation of the exact barrier heights is avoided due to the large variability in the band gap of TiO_{2-x} species [217] coupled with the difficulty in determining the exact stoichiometry of these ultra-thin layers. The resistance of the Au/TiO_x sample remains relatively constant with time, while that of the Au/Ti sample increases slightly, indicating that the Ti layer has gradually oxidized over time.

In all cases, the Seebeck coefficient is positive, indicating hole conduction. Since

the WSe_2 films are less than three layers thick, tunneling is expected to be the dominant mechanism for electron transport. The tunneling Seebeck coefficient depends on the effective barrier height, which in turn is a function of material work functions and layer thicknesses [218]. Specifically, the tunneling Seebeck coefficient depends on the logarithmic derivative of the WSe_2 density of states at the Fermi level, which is pinned by the Au layer and hence it is independent of the intermediate (Ti or TiO_x) layers [218]. In the current case, no significant differences between the two samples have been observed. We conclude that there is negligible difference in terms of band alignment between the two interfaces and they exhibit the same effective barrier height. In most samples, the Seebeck coefficient and the resistance exhibit similar trends, where the resistance increases slightly over time but the Seebeck coefficient decreases over time. We note that these changes over time are minor.

We are unable to separate the resistance of the HOPG substrate due to spatial fluctuations of the measured resistance, which results in large error bars. Compare to a metal, HOPG has a low electrical conductivity (2.0×10^6 S/m along the graphene planes and 500 S/m across the layers) and therefore can affect the resistance measurements. Combining these results with the thermal boundary conductance measured by TDTR in Dr. Patrick Hopkins' group at UVa (on the order of 10^7 W/m^{2}K), we can estimate an equivalent interfacial figure of merit, zT, on the order of 10^{-5} for the studied interfaces. Interfacial zT dominated by tunneling current is expected to be very small. While it is not the purpose of this work to make efficient thermionic devices, this result emphasizes that one needs to increase the number of 2D van der Waals layers to about 4-5 layers to suppress the tunneling effects and ensure thermionic transport [219].

The results in this section have been published in *2D Materials* [220].

4.5 Thermoreflectance Imaging for In-Plane Temperature Distribution Analysis in 2D Thermomagnetic Measurement

Besides thermoelectric materials, there has been increasing interest in thermomagnetic materials. The Seebeck effect states that in a conductor a longitudinal Seebeck voltage is produced in the presence of a temperature gradient. When a magnetic field is applied perpendicular to the imposed temperature gradient, a transverse voltage is induced. This is the Nernst effect and is the basis for thermomagnetic energy conversion. With the magnetic field along the z direction, the Nernst voltage can be expressed as

$$V_y = N_{yx} w B \cdot \nabla_x T, \tag{4.1}$$

where N_{yx} is the Nernst coefficient, w the channel width, B the external magnetic field, and $\nabla_x T$ the local temperature gradient at the point of Nernst voltage measurement.

The transverse nature of the Nernst effect decouples the electrical-thermal correlation and avoids the contact resistance problem, providing a potential pathway to surpassing conventional thermoelectric at low temperatures where thermoelectrics are less efficient. Nernst effect in 2D materials is of particular interest, due to their gate tunability and the exotic properties of 2D ferromagnets and antiferromagnets [221, 222].

Accurate determination of temperature distribution across the sample is crucial in the Nernst coefficient measurement of 2D materials. In the case of bulk samples, the sample is bridged between two temperature sensors at the two ends of the sample. The thermal transport is one-dimensional and the temperature gradient is uniform along the material. The temperature gradient is equal to $\nabla T = \frac{\Delta T}{L}$, where ΔT and L are the temperature difference and the distance between the hot and cold ends respectively.

In 2D materials, due to size limitations, conventional thermometers are no longer applicable. We have to use resistive thermometers, the same as in the case of Seebeck coefficient measurements, to read local temperature via resistance changes at the two ends of the sample. Pairs of side contacts are patterned to measure the transverse voltages. A typical electrode geometry is shown in Fig. 4.17(a). However, due to the existence of the substrate, the thermal transport can no longer be taken as one-dimensional as in the bar-shape bulk case. Although suspending flakes can solve this issue, the need for highly sophisticated bridge structures greatly hampers wide applications.

In this work, we systematically evaluate the temperature gradient in Nernst coefficient measurements in 2D materials. With transport and thermoreflectance measurements, the temperature gradient is clearly shown to be non-uniform on 2D film supported by the substrate. The temperature gradient on the end of the channel close to the heater can be twice as large as the value on the far end. Therefore it is inaccurate to assume a constant temperature gradient. Both measurements demonstrate that the temperature gradient along the channel can be well described by a linear function of the distance from the heater. This information will greatly help future studies of the Nernst effect in 2D materials.

This project is in collaboration with Dr. Junxi Duan's group at Beijing Institute of Technology in China. They fabricated the test samples and performed transport measurements. I performed thermoreflectance imaging measurements to capture the temperature distribution along the sample channel.

4.5.1 Methods

The temperature distribution across the sample when the heater is ON is captured with the TR imaging system. The operational principles of the system are explained in detail in Section 2.2.1. During a typical transient measurement, a voltage pulse with a

5 V bias of duration of 5 ms and 30% duty cycle was applied to turn on the heater. The heating on the sample surface reached a steady state by the end of the voltage pulse and a temperature map at this instant was acquired by averaging over hundreds of thermal excitation cycles. The spatial resolution is diffraction-limited and is about 440 nm under the $100\times$ objective and the 530 nm green light. C_{TR} of $-2.5 \times 10^{-4}\,\mathrm{K}^{-1}$ [223] is used for the Au electrodes to extract ΔT.

4.5.2 Results and Discussion

We utilized the thermoreflectance measurements to map the temperature distribution with a submicron resolution. The thermoreflectance imaging technique can provide accurate temperature readings of the Au electrodes on the sample surface. Three samples were fabricated for the thermoreflectance measurements, with one graphite device (GN2) and two bare substrates with gold wires or gold film (EN1, EN2). The thickness of the graphite flakes was chosen to be around 10 nm. Their optical images are presented in Figure 4.17(a), (c) and (e). EN1 has multiple pairs of transverse electrodes in parallel to the heater on a SiO_2 substrate, while EN2 has a square gold film instead. Figure 4.17(b), (d), and (f) show the typical thermoreflectance mappings measured in these three devices. The temperature change ΔT extracted from the variation of the thermoreflectance of the gold electrodes in GN2 and EN1 is presented in Fig. 4.18(a). Note that the ΔT measured in GN2 is different from the one in EN1, due to the different heating powers. In EN2, ΔT is extracted from the variation of the thermoreflectance of the gold film along the middle line, shown in Fig. 4.18(b). Note that the ΔT measured in GN2 is different from the one in EN1, due to the different heating powers.

It is clearly seen that the dependence of ΔT on the distance from the heater is not a linear function. Consequently, the temperature gradient is not a constant but is

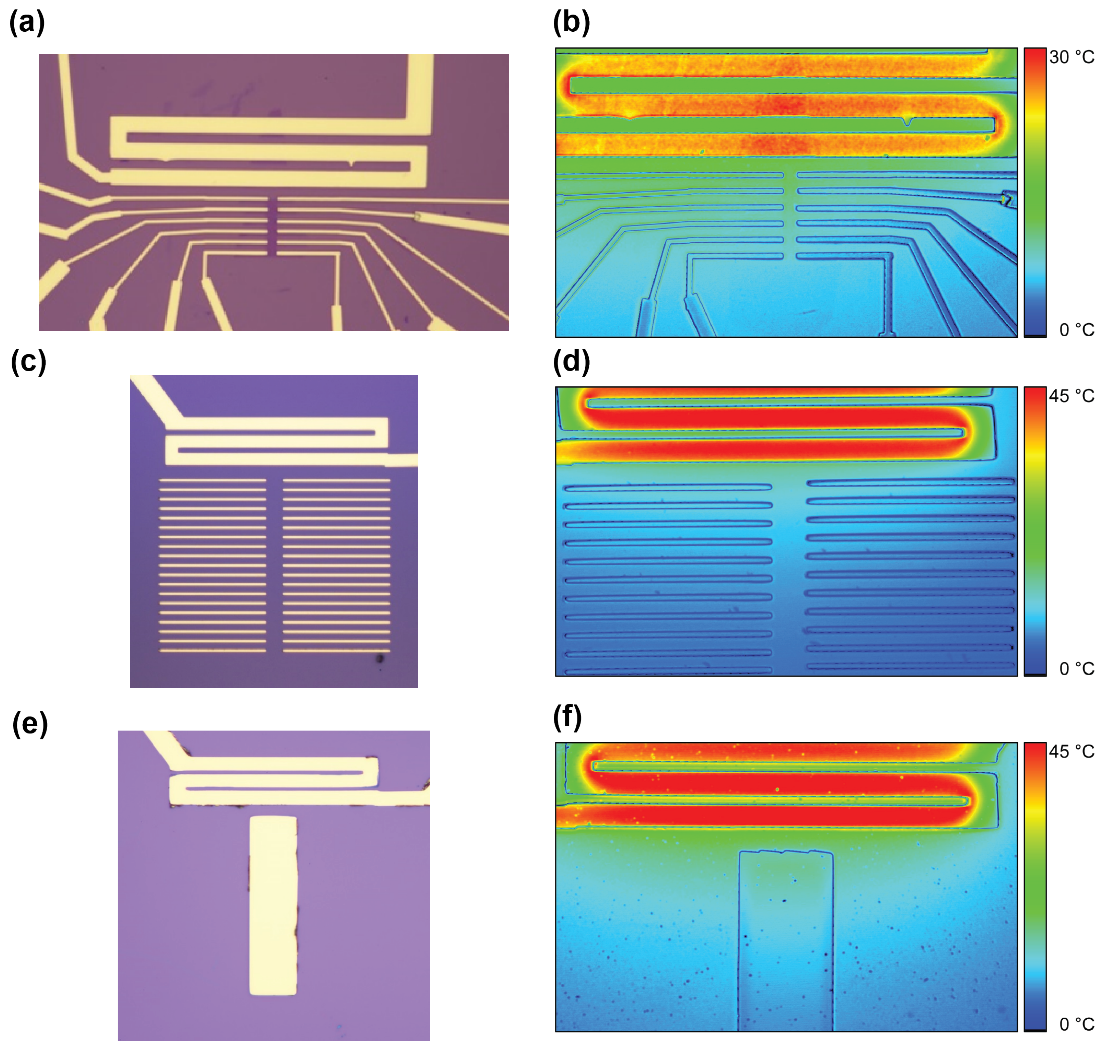

Figure 4.17: Thermoreflectance imaging results. Optical images and the corresponding thermoreflectance images of (a)(b) GN2, (c)(d) EN1 and (e)(f) EN2, respectively. The smallest line width is 1 μm. A bias of 5 V was applied to the heater during thermoreflectance measurements. The colorbar shows the temperature change ΔT across the sample. The variance in the maximum ΔT produced is due to different heater heating powers.

position-dependent. We fitted the data to a parabolic function, $\Delta T = A(d-B)^2 + C$, where A, B, and C are the fitting parameters. The parabolic fittings match all the data quite well. The local temperature gradient is the first derivative of ΔT, and thus a linear function of the distance from the heater. The thermoreflectance measurements confirmed that the temperature gradient linearly depends on the distance from the heater.

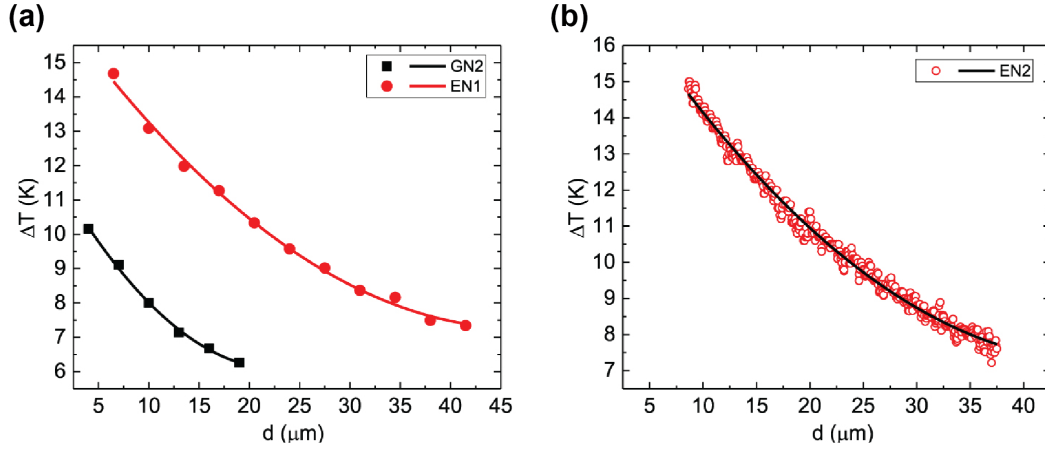

Figure 4.18: (a) Position dependence of the temperature change of the gold electrodes measured in GN2 and EN1. The electrodes in these two devices are separated lines. (b) Position dependence of the temperature change of the gold film in EN2. The solid curves show the parabolic fittings.

As the thermoreflectance results from EN1 and EN2 were similar, the thermal transport is dominated by the substrate.

The thermoreflectance imaging results were corroborated by transport measurements, finite element simulation results and analytical calculations using the generalized Mott formula. The Nernst voltage in several graphite samples similar to GN2 was measured at multiple positions along the channel. The expression in Eqn. 4.1 can be seen as $V_y = k \cdot B$, with the coefficient $k = N_{yx} w \cdot \nabla_x T$ proportional to the local temperature gradient. Instead of being a constant, the coefficient k and thus the temperature gradient have linear dependence on the distance away from the heater. This conclusion holds for different heater currents.

The simulation involves a simple 2D heat transport model with a heater on a substrate, since we have shown that the thermal transport is dominated by the substrate and not the sample or electrodes. A parabolic surface temperature change and a linear temperature gradient have also been observed. We note that the linearity of the temperature gradient is accurate in a certain range. According to our simulation results, the linearity of the temperature gradient maintains well in the range between 10 μm and

40 μm, a typical length scale for 2D devices. This range is actually proportional to the length of the heater. In our presented devices, the length of the heater is 100 μm. This means the range of linearity is roughly $10\%-40\%$ of the heater length. If the size of the sample is larger than the above value, the length of the heater needs to be extended to make sure that the sample fits in the range.

4.5.3 Conclusion

In summary, we systematically evaluated the temperature gradient in the Nernst coefficient measurements of 2D materials. With thermoelectric transport and thermoreflectance measurements, the temperature gradient on a substrate is shown to be position-dependent, suggesting that the long-adopted linear-response assumption is not accurate. Fortunately, the temperature gradient distribution can be well described by a linear function. The experimental results are well captured by simulations based on a simple 2D heat transport model. According to our results, although the local temperature gradient is not a constant, the measurement of the Nernst coefficient within the the standard geometry is still possible, as long as the temperature gradient is corrected considering the linear dependence. Our study provides solutions for accurate measurement of the Nernst coefficient and would be helpful for further studies of the Nernst effect of the 2D materials.

The results in this section have been published in *Journal of Physics D: Applied Physics* [224].

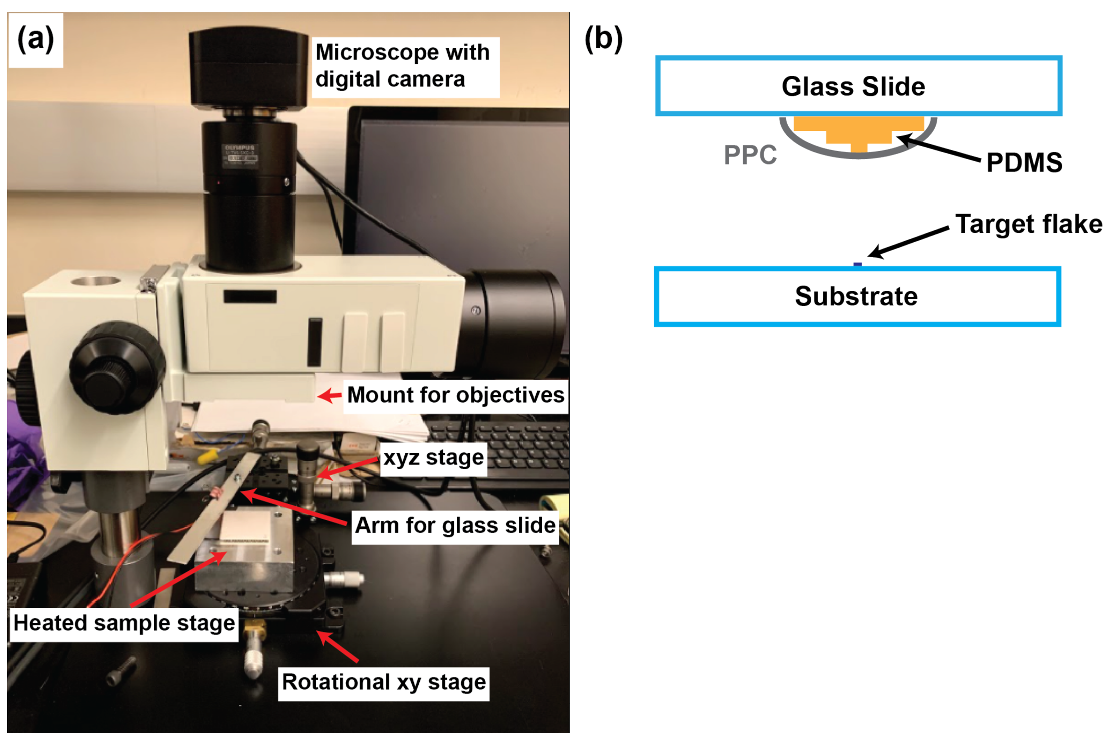

Figure 4.19: (a) The dry transfer setup, which includes a microscope, two micromanipulator stages, and a thermoelectric module to heat up the substrate. (b) A schematic of the PPC/PDMS polymer arrangement for flake pick up.

4.6 Building a Dry Transfer Setup for van der Waals Heterostructures

4.6.1 Experimental Setup

As explained in Section 4.1 at the beginning of this chapter, unique opportunities present in vdW heterostructures for enhanced thermoelectric performance. I have built a simple dry transfer setup following approaches in literature [147] for this purpose.

Figure 4.19(a) shows the entire setup and (b) is a schematic of the PPC/PDMS polymer block. Transparent PPC film is the main component for assembling the layers one by one. It becomes sticky at temperatures above 40 °C to pick up the flakes, and melts at above 110 °C to drop down the entire stack at the desired location. PDMS is a soft, thicker and transparent polymer and can ensure good contact between flake and

PPC. A few layers of PDMS with decreasing sizes are first mounted to a glass slide to form a small hill. Then PPC is attached to cover the PDMS and forms a dome. The shape of the PDMS/PPC stack ensures that only the peak of the structure will be in contact with the substrate and leave the remaining area undisturbed, which reduces the chance of accidentally picking up unwanted debris.

The PDMS block can be reused but PPC films should be made fresh for each use. The PDMS film is prepared using SYLGARD 184 following the manual instructions and is cured on a clean glass slide overnight. 10% PPC solution is prepared by dissolving the powders purchased from Sigma Aldrich into anisole. PPC film is spin-coated (3000 rpm, 60 s) onto a clean Si substrate before use and is baked at 95 °C for 5 min. to dry. After the polymer stack is constructed, the glass slide should be heated for 1 min. to make the PPC conform to the PDMS.

Subsequently, the glass slide with the polymer stack is mounted to the xyz stage with the PPC side facing down. The sample substrate should be fixed to the heated sample stage sitting on the rotational xy stage with double-sided tape. The rotational stage makes it possible to fabricate devices with controlled twist angles and makes alignment easier. The heating is provided by a thermoelectric module and its temperature-current curve should be calibrated beforehand, ideally with a blank substrate mounted. The position of the sample should be adjusted so that the target flake is in the center of the field under the microscope. Then the glass slide is centered and is moved down to pick up the flakes. The steps are repeated until the entire stack is completed. The heterostructure is dropped off by heating the PPC beyond its melting temperature.

4.6.2 Step-by-Step Guide to Construction of hBN/$MoTe_2$ Heterostructure

Here, a step-by-step guide to build and place a hBN/1T'-$MoTe_2$ device onto pre-patterned SiO_2 substrate is provided in Fig. 4.20 as a demonstration of the technique. The adhesion between PPC and $MoTe_2$ is usually weaker than the interaction between $MoTe_2$ and the SiO_2 substrate, so hBN is chosen as a medium to provide stronger adhesion. HBN and 1T' $MoTe_2$ were exfoliated onto two separate SiO_2 substrates and the target flakes were identified under a microscope. Since the dimensions of the electrodes were already set, the flakes needed to be at least $60\times15\ \mu m^2$ to fill the gaps.

The assembly starts from the top so the hBN flake should be picked up first. By changing the focus of the microscope, we would be able to monitor both the PPC film and the substrate as the glass slide was lowered. When the PPC film was within touching distance from the substrate, we would see both surfaces in view, which helped greatly with alignment. The polymers were then slowly dropped onto the substrate. The heating from the stage should help expand the contact area and make the PPC stick to the sample surface. After some time, the PPC stack was slowly moved up. The substrate was kept at 50 °C during the pick-up processes. The flake should now be removed from the substrate and transferred to the film. This 'move down-align-contact-move up' process should be repeated until all desired flakes were picked up. Then the stack could be dropped either at the location of the last flake or onto a new clean substrate, by heating above 110 °C. In our case here, the heterostructure was aligned and placed onto the pre-patterned gold electrodes. The melted PPC should remain on the substrate when the glass slide was moved away and can be cleaned with acetone/isopropanol.

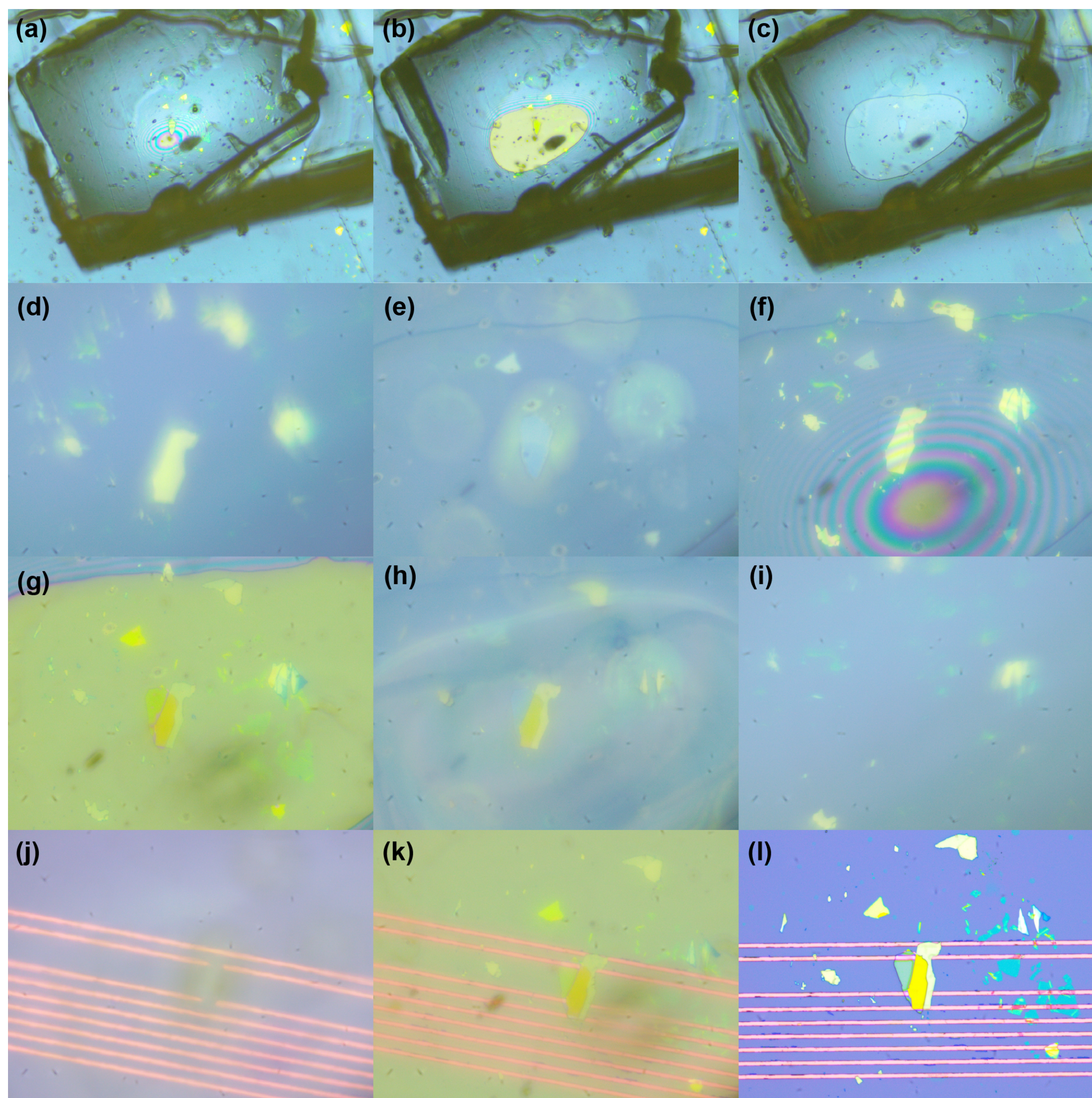

Figure 4.20: Step-by-step demonstration on building a hBN/1T'-$MoTe_2$ device. Magnification is switched between 5× and 20× to better assess the status. The first step is to pick up the hBN flake. (a) PPC film partially in contact with the flake. Edges of the PDMS layers are visible. Some dirt particles on the PDMS are also visible but are not in contact with the sample. (b) PPC film fully covering the flake. (c) PPC film after hBN pick-up with the semi-transparent flake in view. The second step is to pick up the $MoTe_2$ flake. (d) Target $MoTe_2$ flake on the SiO_2 substrate viewed through the multi-layer polymer stack and the glass slide. (e) hBN on PPC, hovering above the $MoTe_2$. (f) Dropping down the hBN to be in partial contact with the $MoTe_2$. (g) hBN and $MoTe_2$ fully in contact. (h) hBN/$MoTe_2$ heterostructure on PPC. (i) Substrate is free of the $MoTe_2$. The last step is to place the stack onto the pre-patterned gold electrodes. (j) Electrodes with shadow of heterostructure hovering right above. (k) Aligning with the pre-patterned electrodes and melting the PPC. (l) hBN/$MoTe_2$ on Au electrodes after acetone/isopropanol cleaning. Some hBN flakes in the vicinity of the target were also transferred.

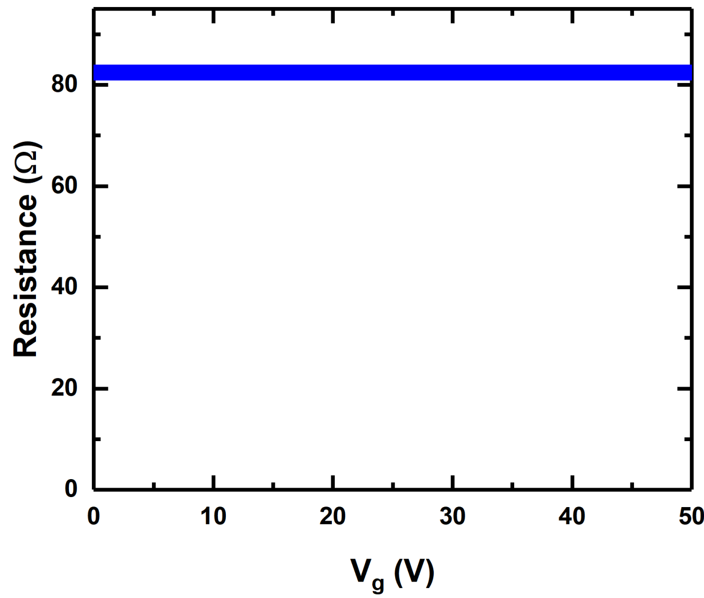

Figure 4.21: Resistance as a function of backgate voltage V_g for the hBN/1T'-$MoTe_2$ heterostructure device.

4.6.3 Results and Conclusion

1T'-$MoTe_2$ is a Weyl semimetal so its resistance should be similar to that of the $NbSe_2$ samples measured in Section 4.2. Four-probe resistance of the sample was measure using AC method with a lock-in amplifier and was about 82 Ω. The value stayed constant with a backgate voltage up to 50 V, as shown in Fig. 4.21. This is expected, since the number of carriers added by the backgate is small compared to the free carriers existing inside the sample. The characterizations mainly serve as a proof that the dry transfer setup can reliably produce clean and high quality samples. This setup paves the way for experimental study of more exciting and sophisticated material systems in our lab.

4.7 Summary

In this chapter, we have investigated thermoelectric transport in various few-layer 2D TMD systems, from metallic $NbSe_2$ to semiconducting 2H-$MoTe_2$ and WSe_2. The measurements for $NbSe_2$ and $MoTe_2$ were in-plane, while that for WSe_2 was cross-plane. In the 4L $NbSe_2$, we first used XPS and STM to show that the MBE-grown samples were Nb-rich, polycrystalline and metallic. Then transport measurements and DFT calculations followed, confirming the metallic nature of the sample. We reported the first thermal conductivity measurement of a few-layer $NbSe_2$ in the low-temperature range. With the help of heat diffusion imaging, we were able to fully evaluate the thermoelectric properties to estimate a zT, when most research on 2D thermoelectric materials reports only PF and replies on others to measure k. Although the zT value was not high in the intrinsic metallic 2D $NbSe_2$ sample, it was still higher than the performance of the bulk samples and other 2D $NbSe_2$ nanosheets. In addition, we demonstrated that the electrical conductivity, the Seebeck coefficient, and the thermal conductivity of 2D samples could be measured all together on a substrate, without having to work on separate designs for the electrical and the thermal transport. In the case of the 2H-$MoTe_2$, the effect of adding charge carriers via an electrostatic gating bias was tested. The resistance change was up to an order of magnitude. However, no obvious change was observed in the Seebeck coefficient. The maximum power factor occurred at high positive backgate voltages when the resistance was smaller and corresponds to an improvement of up to 89% compared to the intrinsic value. With the large channel resistance from the semiconducting samples, noises from the backgate and the instruments affected the Seebeck voltage detection and made the measurements difficult. In the WSe_2, the effects of Ti and TiO_x contacts on the cross-plane thermoelectric transport were discussed. The presence of TiO_x increased the contact resistance but no notable difference in the Seebeck coefficients of the two samples was observed. This

was of great importance on the device level, especially as Ti is an important adhesion layer metal for 2D material contacts but also a gettering metal that easily reacts with other elements.

We also characterized the temperature distribution on 2D samples during thermomagnetic measurement. For thin flakes supported on a substrate, the assumption of a constant temperature gradient, which was commonly adopted in the case of bulk samples, is no longer applicable. With thermoreflectance measurement, transport measurement, and finite-element modeling of the heat conduction equation, it was shown that the temperature distribution could be approximated by a parabolic relation with respect to the distance from the heater, which means the temperature gradient was a linear function of the distance from the heater. This correction is of great importance for future Nernst coefficient measurements. In Section 4.6, the capability of a 2D dry transfer setup that I built was demonstrated with the example of using hBN to move 1T'-$MoTe_2$ onto a pre-patterned substrate.

The results in this chapter add to the knowledge of 2D thermoelectric materials and 2D measurement techniques and should inspire more discussions on using 2D TMD for thermoelectric devices.

Chapter 5

Conclusion and Outlook

This dissertation evaluates the thermoelectric transport properties of Si-based thin films and few-layer 2D materials and discusses the strategies to optimize their performance. It starts with an overview of the development in the field of thin film and 2D thermoelectrics. The experimental work covers a diverse range of topics: a hybrid thermoreflectance-based method to measure the in-plane thermal conductivity of supported thin films, enhancement of thermoelectric performance in Si thin films with holey nanostructures and with surface charge transfer doping from organic molecules F_4TCNQ, thermoelectric transport of few-layer 2D materials for metallic $NbSe_2$ and semiconducting 2H-$MoTe_2$ in the in-plane direction and for WSe_2 with different contact metals in the cross-plane direction, as well as a correction to the temperature distribution in 2D thermomagnetic measurements.

Heat diffusion imaging utilizes the thermoreflectance imaging technique and the heat spreader model, in order to meet the demands for a relatively simple in-plane thermal conductivity measurement method of thin films supported on a substrate. It holds several advantages: it does not require film suspension or fabrication of multiple thermometers; it is a non-intrusive electrical-pump optical-probe method; it measures local temperature directly at the sample surface and is more accurate than thermistor

readings; it has a submicron spatial resolution. The approach was validated using Si thin films with and without holes and its application has been extended to the few-layer limit. It allows us to assess the zT of thin films and few-layer 2D materials without having to change the sample configuration for different measurement techniques and has been substantial in our study of thermoelectric transport in two dimensions.

Si-based thermoelectric materials are attractive due to their cost-effectiveness, industrial compatibility, and high power factor. A nanostructuring strategy, which involves patterning periodic nano-sized holes with spacing smaller than the phonon MFP but larger than the charge carrier MFP, has been proposed to reduce the thermal conductivity of Si thin films. The effectiveness of this strategy was first proved on a holey Si thin film conventionally doped by boron ion implantation. It showed a zT of 0.09 at room temperature, which was more than four times improvement over the highly-doped bulk Si sample thanks to a 16-fold reduction in thermal conductivity, and of exceeding 0.29 at 650 K. Then we employed surface charge transfer doping with organic molecules F_4TCNQ to holey Si thin films with different hole configurations. Compared with conventional doping methods, this doping scheme was expected to improve carrier mobility with less impurity and Coulomb scattering. The holey structure means more surface area and should extend the doping effect to 3D. As a result, the PF and the zT of the organic-holey Si hybrid device improved by 2 orders of magnitude, much larger than the 75% PF improvement observed in Si thin films without holes.

Few-layer 2D TMD materials possess a wide range of electronic properties, from insulating to superconducting, depending on their crystalline structures and the topology of their electronic structure. These properties are usually superior compared to their bulk counterparts and can be tuned by multiple factors, such as thickness and an electrostatic backgate bias. MBE-grown 4L $NbSe_2$ was characterized by STM, in-plane transport measurements, and DFT calculations to confirm its metallic nature.

With the help of heat diffusion imaging, the thermal conductivity of few-layer $NbSe_2$ was first reported in the low-temperature range between 50 K to 200 K. This study adds to our knowledge of 2D thermoelectric materials. In a metallic sample like $NbSe_2$, the charge carriers added via backgate doping would not be enough to significantly alter its behavior. But in a semiconducting sample like 2H-$MoTe_2$, backgate voltages changed its resistance by an order of magnitude and showed an improvement of up to 89% in the maximum room temperature power factor compared with the intrinsic value. The effects of different metal contacts, i.e., Ti and TiO_x, were evaluated for WSe_2 in a cross-plane geometry: resistance was increased in the case of TiO_x although no notable difference was detected in the Seebeck coefficients. Because Ti is an important adhesion layer metal for 2D materials, this research helps us understand the factors that might affect the thermoelectric performance on a device level. Using thermoreflectance measurements, we were able to confirm that for a 2D sample on a substrate, the temperature gradient was a linear function of the distance away from the heater, as opposed to the assumption of constant temperature gradient commonly used in bulk samples. This correction is of great importance to future transport measurement, especially for the Nernst coefficient measurement.

In the research works listed above, various strategies have been implemented to improve the thermoelectric performance of a material and have been shown to be effective, from nanostructuring and surface charge transfer doping for Si thin films to electrostatic gating in 2D materials. The surface doping scheme can probably be tested on other systems with a large surface area, such as nanowires. Although there have been some discussions on applying nanostructuring and surface charge transfer doping to 2D materials, the experimental studies mainly focused on graphene. Future studies should consider expanding the research into other 2D materials, particularly semiconducting TMDs, as TMDs generally have a much smaller thermal conductivity

than graphene and have relatively good electrical properties that can be tuned by gating. The experimental results in this dissertation have deepened our understanding of optimizing the thermoelectric transport in two dimensional systems and hopefully will stimulate exciting new research ideas to follow.

List of Publication

1. **Tianhui Zhu***, Yunhui Wu*, Shuai Li, Farjana F. Tonni, Masahiro Nomura, and Mona Zebarjadi; ****equal contributions***
Enhanced Thermoelectric Performance of Holey Silicon Thin Films using F_4TCNQ Doping, *Materials Today Physics* (2022).
`https://doi.org/10.1016/j.mtphys.2022.100942`

2. **Tianhui Zhu**, Peter M. Litwin, Md Golam Rosul, Devin Jessup, Md Sabbir Akhanda, Farjana F. Tonni, Sergiy Krylyuk, Albert V. Davydov, Petra Reinke, Stephen J. McDonnell and Mona Zebarjadi
Transport Properties of Few-Layer $NbSe_2$: from Electronic Structure to Thermoelectric Properties, *Materials Today Physics* (2022).
`https://doi.org/10.1016/j.mtphys.2022.100789`

3. Qi Feng*, **Tianhui Zhu***, Wei Yuan, Yu Jian, Huimin Peng, Jinrui Zhong, Junxi Duan, Mona Zebarjadi and Yugui Yao; ****equal contributions***
Nernst Coefficient Measurements in Two-dimensional Materials, *Journal of Physics D: Applied Physics* (2022).
`https://doi.org/10.1088/1361-6463/ac923f`

4. **Tianhui Zhu**, David H. Olson, Patrick E. Hopkins, and Mona Zebarjadi
Heat diffusion imaging: In-plane thermal conductivity measurement of thin films in a broad temperature range, *Review of Scientific Instruments* (2020).
`https://doi.org/10.1063/5.0024476`

5. Qin-Yi Li, Qing Hao, **Tianhui Zhu**, Mona Zebarjadi, Koji Takahashi
Nanostructured and Heterostructured 2D Materials for Thermoelectrics, *Engineered Science* (2020).
`https://doi.org/10.30919/es8d1136`

6. Naiming Liu*, **Tianhui Zhu***, Md Golam Rosul, Jon Peters, John E. Bowers, Mona Zebarjadi

*equal contributions

Thermoelectric Properties of Holey Silicon at Elevated Temperatures, *Materials Today Physics* (2020).

`https://doi.org/10.1016/j.mtphys.2020.100224`

7. Keren M. Freedy, **Tianhui Zhu**, David H. Olson, Peter M. Litwin, Patrick E. Hopkins, Mona Zebarjadi, Stephen J. McDonnell

Interface Chemistry and Thermoelectric Characterization of Ti and TiO_x Contacts to MBE-Grown WSe_2, *2D Materials* (2020).

`https://doi.org/10.1088/2053-1583/ab834b`

Appendix A

Summary of Measured Thermoelectric Properties

Sample	S (μV/K)	σ (S/m)	PFT (Wm^{-1}K^{-1})	k (Wm^{-1}K^{-1})	zT	Comment
Plain Si	-	-	-	72	-	100 nm thick, HDI method validation
Holey Si	235	3.1×10^4	0.52	5	0.09	100 nm thick, 100 nm pitch, 55 nm neck, B-doped $3 \times 10^{19} - 1 \times 10^{20}$ cm^{-3}
Holey Si	145	2.3×10^4	0.14	13	0.01	220 nm thick, 300 nm pitch, 120 nm neck, F_4TCNQ-doped
Holey Si	330	255	0.008	26	3×10^{-4}	220 nm thick, 300 nm pitch, 180 nm neck, F_4TCNQ-doped
$NbSe_2$	-12	1.7×10^5	0.007	32 (200 K)	2×10^{-4}	4 layer, MBE-grown
$MoTe_2$	-220	2.5×10^3	0.04	10	4×10^{-3}	25 nm, exfoliated, $V_g = 80$ V

Table A.1: Summary of the room temperature thermoelectric properties of all samples presented in this disseration.

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