Terahertz Sideband Generation based on a Schottky Varactor Diode Array

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A Dissertation Presented to

the faculty of the School of Engineering and Applied Science

University of Virginia

In Partial Fulfillment

of the requirements of the Degree

Doctor of Philosophy

Electrical and Computer Engineering

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July 2013

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Abstract

This work focuses on the design and fabrication of a quasi-optical 1.6THz sideband generator. To create the sideband generator, an array of planar gallium arsenide Schottky diodes are used as varactor mixers. The array is modulated by a 50 GHz lower frequency pump signal to create the desired sideband at 1.55THz. The goal is to create a sub-millimeter sideband generator with conversation losses less than -30 dB, and an output power generation greater than 50 μW at the first lower sideband. This approach varies from other sub-millimeter designs in three key aspects. The most noticeable difference is the use of a quasi-optical coupling of signals. A quasi-optical design eliminates the need for a waveguide and uses a high-resistivity silicon lens to focus the RF power on the sideband generator. Another variation from typical submillimeter sideband generators is the use of an array. The array allows for more power handling capability when compared to a single diode device and creates advantageous boundary conditions which are exploited in the design. The last major variation is the addition of a tuning element in parallel with the diode itself. The tuning element is used to create a parallel resonance circuit within the array design, helps alleviate the effects of parasitics surrounding the anode contact, and eases the fabrication tolerances of the diode design. The added parallel tuning element, in addition with a series tuning element, common to most planar millimeter and submillimeter diode designs, allow the diode to modulate between an open and short circuit. The added phase shift created by the resonance circuits is intended to increase the conversion efficiency of the proposed sideband generator. In addition to increasing the efficiency, the added tuning element simplifies the fabrication process, circuit modeling, and reduces parasitic effects associated with the device geometry.

Acknowledgments

I would like to thank everyone who helped me during my seven years at the University of Virginia. To my adviser, Dr. Robert Weikle, without his guidance, advice, and support throughout the years none of this work would be possible. To all my committee members: Dr. Jeffery Hesler, Dr. Jim Fritz-Gerald, Dr. Scott Barker, and Dr. Art Lichtenberger, all the advice you provided during my studies and research proved invaluable. To my lab-mates: Dr. Ed Douglas, Dr. Haiyong Xu, Bob Benoit, Mike Cybery, Matt Bauwens, Becca Percy, Naser Alijabbari, and Dr. Alex Arsenovic, all the discussions and projects we did together were extremely useful and necessary to the completion of this work. To the Microfabrication lab director Joe Beatrice, thank you for keeping all the tools operational and making sure the lab is always in working order. To Alex Lobo and Harry Wade, your tireless efforts maintaining the tools in the MFL was a major contributor the to success of this work. To Dr. Bascom Deaver and Acar Isin for maintaining the far infrared receiver lab, all the advice, all the machined components, and all the help throughout the years. To all of my friends in Charlottesville, especially Nathalie Nahas, thank you all for the moral support and proof reading. Last, but not least, I would like to thank my mother and father, Khouloud and Aiman Hawasli for always providing me with the best opportunities in life, I wouldn't be where I am today without their endless love and support. Thank you all so very much!

Chapter 1

Introduction

1.1 THz Mixers and Upconverters

1.1.1 Submillimeter sources

The need for tunable sources remains one of the primary concerns for engineers developing submillimeter wave systems. Submillimeter wave tunable sources have uses in radio-astronomy, remote sensing, molecular spectroscopy, and chemical and biological agent detection. However, currently there are limited options for sources that can operate with high power and broad tunability at submillimeter wavelengths.

Figure 1.1 shows a comparison of several different THz sources and their respective power output at various frequencies. There are a select few solid-state sources which can produce significant power at submillimeter wavelengths. Chains of frequency multipliers are frequently used to convert power from a low frequency pump to a much higher frequency. However, the power output of multiplier chains begins to diminish as the frequency approaches 1 THz. Quantum cascade lasers are photonic device capable of producing significant power at submillimeter wavelengths. Much like multipliers, these devices suffer from diminishing power outputs as frequencies decrease towards the millimeter region.

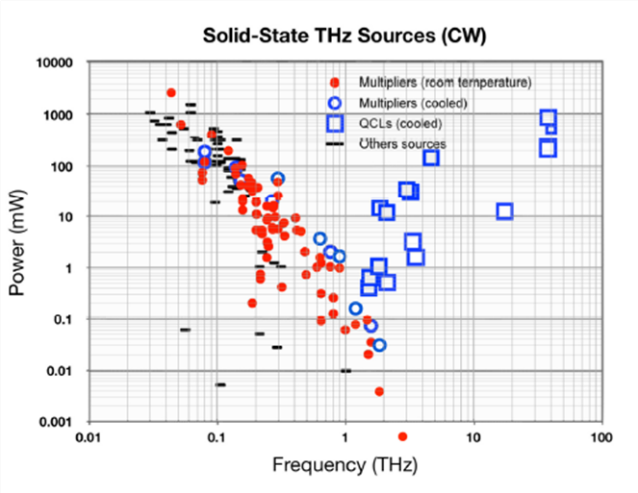


Figure 1.1: Available power sources as a function of frequency and power[1]

There are several high power THz sources which make use of vacuum-tube technology; gyrotons, klystrons, and backward wave oscillators. However, these types of sources tend to be large, difficult to use, and expensive. Another widely used high power source using vacuum tubes is a far-infrared (FIR) laser which can output power levels greater than 100mW at discrete spectral lines, but with little to no tuning bandwidth. The primary advantage of FIR lasers is high power output.

1.1.2 Sideband generation approach to creating a tunable high frequency source

Mixers, downconverters, and upconverters are often employed as modulators and have great utility in millimeter and submillimeter wave applications. Sideband generators are a class of modulators designed to convert power from a single low frequency input to a higher frequency. The manner in which the modulator is pumped determines whether or not it is considered a mixer or upconverter. Figure 1.2a shows the output spectrum of a mixer. In this case the carrier signal (RF) is modulated by a high frequency pump signal (LO). The aim is to convert power from the carrier frequency to a lower intermediate (IF) frequency and the difference frequency between the carrier and modulating

signal.

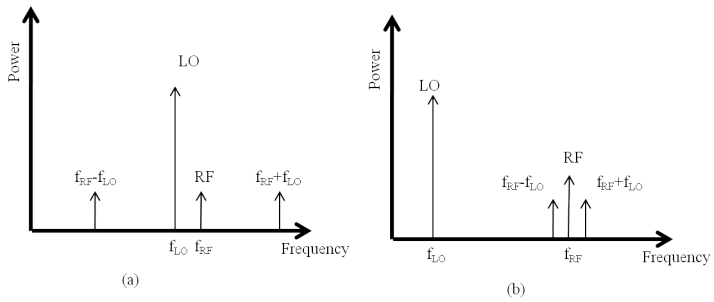


Figure 1.2: a: Frequency spectrum for mixing b: Frequency spectrum for upconversion

Upconversion refers to the opposite process where a high frequency carrier signal (RF) is modulated by a lower frequency pump (LO), producing a high frequency sideband. Figure 1.2b shows the frequency spectrum output of a typical upconverter. The pump is a high power signal that modulates the conductance of a nonlinear device generating sidebands around the low power RF input. The sidebands are generated at the sum and difference frequencies of the carrier and pump. As shown in Figure 1.2b, many sidebands are produced corresponding to multiples of the pump frequency. The goal of sideband generation is to maximize the power converted to a particular desired sideband frequency.

Frequency upconversion using Schottky diodes is another attractive option for producing tunable signals at sub-millimeter wave frequencies for a number of reasons. Upconverters offer a tunability that high power submillimeter sources cannot achieve. In addition, upconverters based on power combining architectures can accommodate power levels much greater than single-device based modulators.

1.1.2.1 Previous submillimeter sideband generators based on planar Schottky diodes

One of the first sideband generators based on Schottky diode technology was developed at the University of Virginia [28]. The sideband generator was designed using a whisker contacted GaAs diode and operated in forward bias as a varistor. Figure 1.3 shows a cross section of the metal whisker and GaAs die. Figure 1.4 shows an SEM image of the whisker in contact with the GaAs

surface. To couple power to the diode, the whisker was placed in a corner cube mount and a FIR laser was used to provide the RF power. The whisker contact design was used to minimize parasitic effects surrounding the actual Schottky contact. The design yielded a conversion loss of 30 dB with a power output of 10.5 μW. However, using a whisker contacted diode made integrating this particular architecture fairly complicated into typical RF integrated circuits.

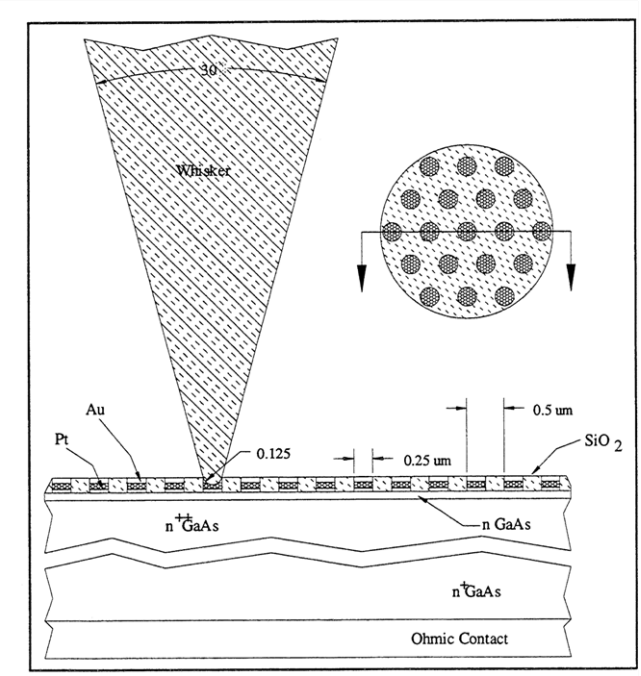


Figure 1.3: Cross section of a whisker contacted planar Schottky diodes used for sideband generation

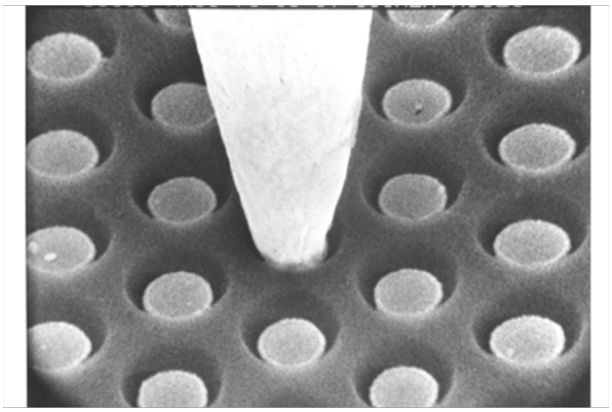


Figure 1.4: A SEM image of a whisker making contact with GaAs substrate

Another sideband generator based on planar Schottky diodes developed in 1998 took advantage of an array of Schottky diodes [26]. Figure 1.5 shows a figure of the array. The array consisted of 36 Schottky diodes and, like the previous design, was operated in forward bias as a varistor. One of the key design features of an array is its ability to spread the incident power over many devices, increasing the overall power handling compared to a single diode design. Figure 1.6 shows a close up image of an unit cell within the array. The Schottky diode geometry is much different than the previously seen whisker contacted diode. A bowtie antenna was used to couple power to the diode and a short length of metal was used to tune the impedance presented to the diode. The array design had a conversion loss of 28 dB and produced about 6 μW of power. The use of planar contacted diodes resulted in a more reliable, easier to fabricate, and a higher yield of devices. However, the design also lead to increased parasitics surrounding the diode which complicate the circuit modeling and overall design of the sideband generator.

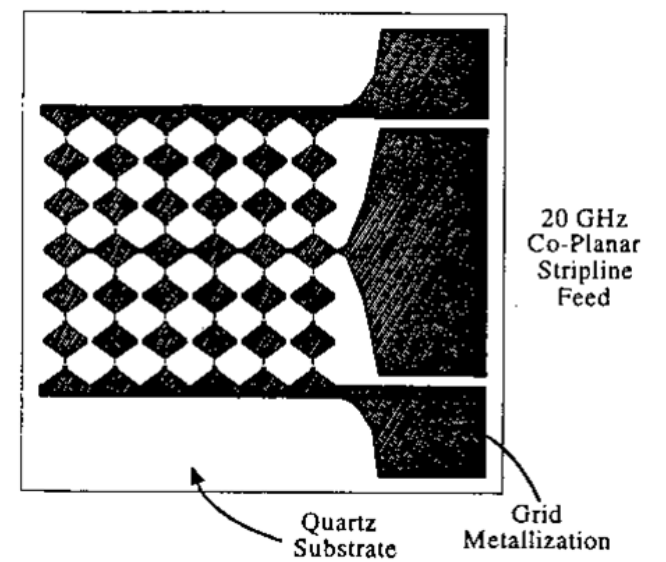


Figure 1.5: A photograph of a previously fabricated sideband generator based on a Schottky diode array

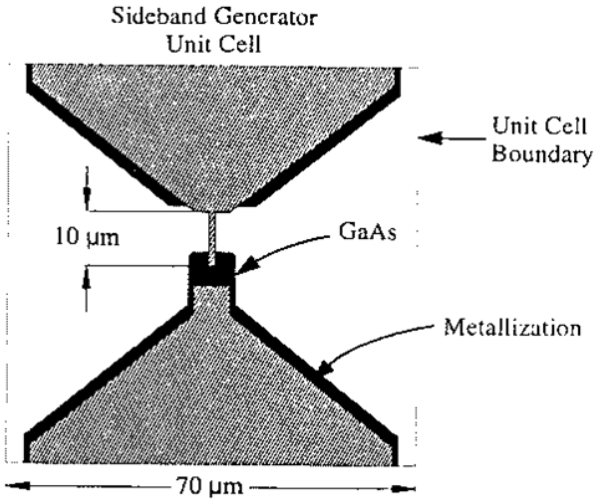


Figure 1.6: An image of a single unit cell within the sideband generator array

A sideband generator design which combined many different techniques was developed in 2002 at UVa. Figure 1.7 shows a cross section of the device. The device used a whisker contacted GaAs

diode. However, unlike the previous design where a corner cube mount was used to couple power to the diode, the whisker was placed inside a waveguide. This design operated in reverse bias as a varactor and had a conversion loss of 14 dB with a power output of 55 μW. The sideband generator took advantage of the low parasitic diode which was a result of having a whisker contact. The integration within a waveguide allowed for external circuitry, such as filters, to be integrated onto the same structure. However, the design did suffer from the unreliability and complexity of having a whisker contacted diode and the power handling was limited to a single element.

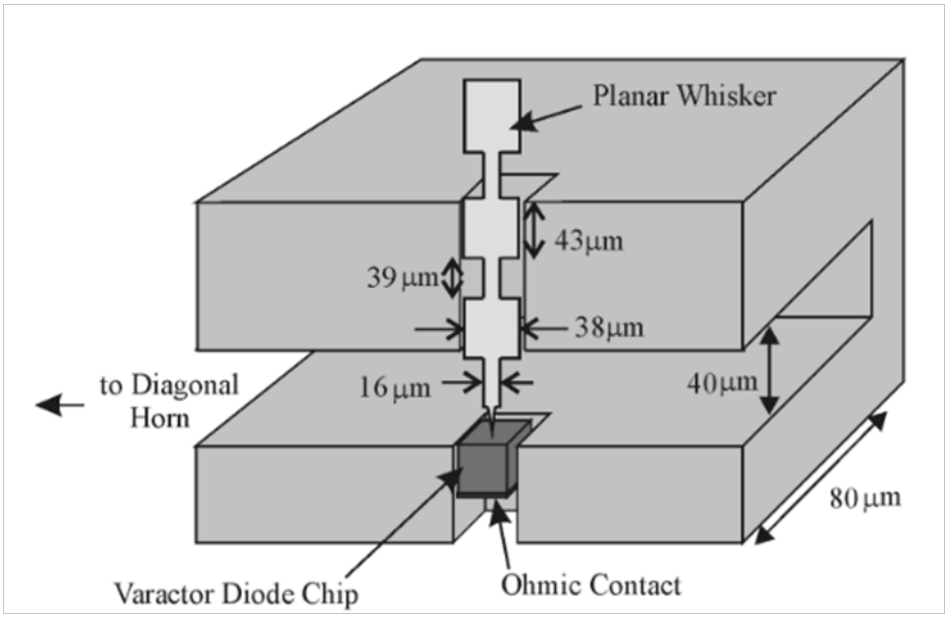


Figure 1.7: A cross section of a sideband generator based on a planar whisker contacted GaAs within a waveguide

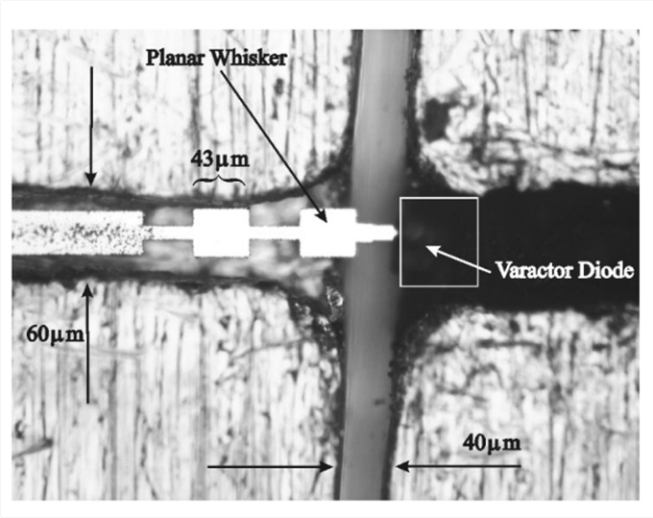
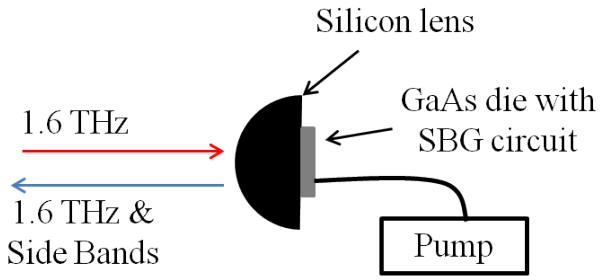


Figure 1.8: A photograph of the device described in Figure 1.7

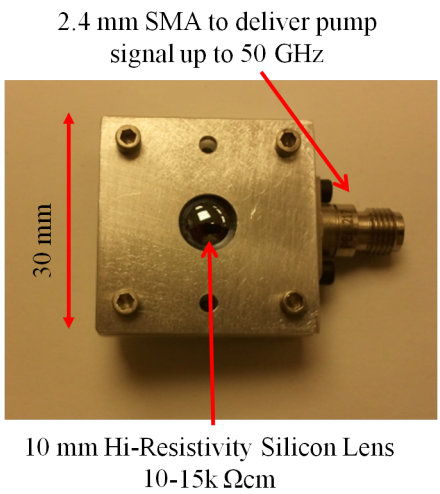
1.2 Project Motivation and Description

In this work, an array of Schottky diodes is investigated for use as a tunable upconverter to create sidebands around a 1.6THz. This work is important to work at the National Ground Intelligence Center (NGIC) in developing scaled radar systems that will employ an upconverter as a tunable submillimeter source. The goal is to create a circuit capable of chirping a 1.6THz carrier with a bandwidth of 50 GHz. Rather than using a static pump frequency, the frequency is ramped over time, which will modulate the output, creating a chirp at 1.6THz.

Figure 1.9a shows the quasi-optical design that will be applied to the upconverter. A silicon lens is used to focus incident radiation onto the array and the sidebands will be reflected back out the lens. The array will be modulated by a pump signal up to 50 GHz. Figure 1.9b shows a photograph of the front side of a packaged sideband generator. This image shows both the dimensions of the housing as well as the exposed part of the silicon lens.



(a)



(b)

Figure 1.9: a: An overview of the quasi-optical design of the SBG. b: A photograph of the final SBG showing the front side of the silicon lens

Figure 1.10 is a photograph of the back side of the sideband generator package showing a GaAs die and a high resistivity silicon piece used to mount the sideband generator into the package. The silicon piece has a Coplanar waveguide transmission line which is used to electrically connect the SMA connector to the sideband generator. The silicon substrate also serves to align the GaAs die to the mechanical center of the lens.

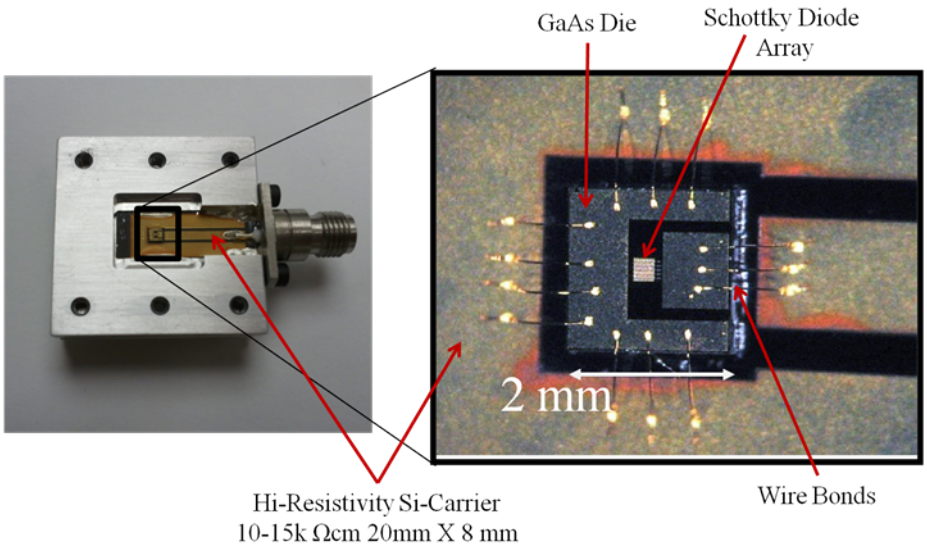


Figure 1.10: A photograph showing the back side of the SBG package and a close up of the GaAs die

Figure 1.11a shows a microscope photograph of a 100 element Schottky diode array. The image shows a bowtie antenna which is used to couple power to the Schottky diodes. A diode is fabricated at the center of each bowtie. Figure 1.11b shows a SEM image of a single unit cell. This figure shows more clearly where the Schottky contact is located and the bowtie formed between the metal and buried ohmic contact. The photograph also shows a tuning element which is added to the design to increase the performance of the sideband generator, reduce parasitic effects surrounding the Schottky contact, and ultimately simplify the fabrication process.

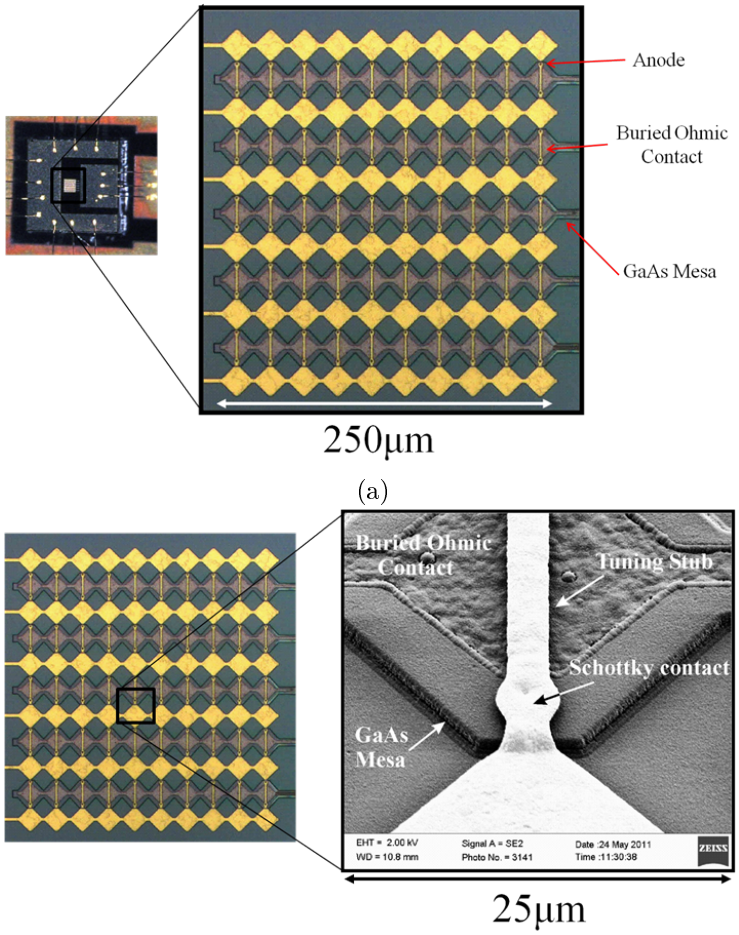


Figure 1.11: a: A microscope image of a 100 element SBG Schottky diode array. b: A SEM image of a unit cell showing the details of the cell and Schottky diode

1.3 Summary

The goal is to create a sideband generator based on an array of planar Schottky diodes which can meet or improve upon results of previously demonstrated sideband generators based on planar Schottky diode technology. This approach to developing a sideband generator based on planar Schottky diodes takes advantages of key design features to improve the performance of the device. The use of an array will increase the power handling of the device as the incident power is spread

over many elements. The array also results in advantageous boundary conditions due to the array's symmetry. These boundary conditions are exploited to create a virtually shorted tuning element. In this case, the tuning element is a microstrip transmission line whose ground plane is a buried ohmic contact of the diode. The integrated tuning element can improve the performance of the device in two ways. First, the integrated tuning element increases the overall phase shift that a single diode can provide, decreasing the sideband conversion loss. The integrated tuning element also reduces the effects of the parasitics surrounding the planar Schottky diode, reducing the fabrication tolerances.

The next chapter provides an overview of millimeter and submillimeter planar Schottky diodes. The chapter discusses the Current-Voltage, Capacitance-Voltage, and series resistance of a Schottky contact as well as how to model the relationships. Chapter 2 also presents the results for diodes centered at 20 GHz and WR1.5 (500 - 750 GHz). Chapter 3 focuses on the design and modeling of the sideband generator array. The chapter builds up the circuit models used to describe the Schottky contact, unit cell, and array performance. Chapter 4 discusses the fabrication process used to create the array. The chapter goes into detail about the specific processes used and the reason why particular processes were chosen. Chapter 5 presents the different methods used to characterize the array. The chapter shows the current-voltage relationships, responsivity measurements, and the phase shifting results which are used to determine the performance of the sideband generator array.

Chapter 2

Millimeter and Submillimeter Schottky Diodes

2.1 Overview of Schottky Diode Fundamentals

The focus of this work is the application of a Schottky diode array for parametric upconversion and sideband generation. The fundamental physics and equivalent models for representing millimeter and submillimeter-wave Schottky diodes have been described extensively in the literature[5]. This chapter will serve to summarize the basic operation and physics of a Schottky diode.

Schottky diodes are employed as mixers, detectors, harmonic generators and parametric devices because of their strong non-linear current-voltage response in forward bias and capacitance-voltage dependance in reverse bias. In typical cases for detection, multipliers, and heterodyne receivers, diodes are used as variable resistors (varistors) being operated in the forward bias region. To create a parametric device such as an upconverter or sideband generator, diodes are operated as a variable capacitor (varactor) in reverse bias. In a commonly employed architecture for sideband generation the diode serves as a voltage dependent reactive load that reflects the incident power with a voltage dependent phase shift.

Figure 2.1 shows a cartoon of a metal to semiconductor contact that forms a Schottky diode. Included in the model is a depletion region and electrically-neutral semiconductor. For a Schottky contact made on n-type semiconductor, the average energy of the semiconductor's electrons is greater than most metals. The energy differences can be determined by comparing the work functions of the two materials. Figure 2.2a illustrates the band structures of the two materials before a contact is made. The difference in the work function of the metal and semiconductor can be compared in 2.2a. To maintain thermal equilibrium, when the metal and semiconductor are brought into contact, electrons transfer form the semiconductor in to the metal to keep the Fermi level constant. Figure 2.2b shows the band structure when the metal and semiconductor are in contact. The difference in the work functions creates an energy barrier and a resulting built in voltage (V_{bi}).

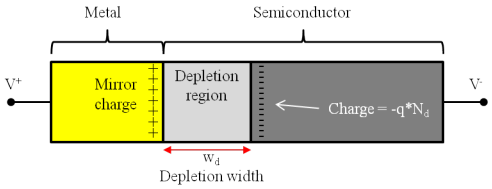


Figure 2.1: Model Displaying the Schottky depletion capacitance

Electrons transferring to the metal deplete the carriers from the semiconductor near the interface creating a region largely devoid of carriers. This region is the "depletion region" and the charge associated with the ionized donors in this region results in a voltage dependent depletion capacitance. The depletion capacitance is a function of substrate doping, work function of the metal creating the Schottky contact, applied bias voltage, and contact area.[2]

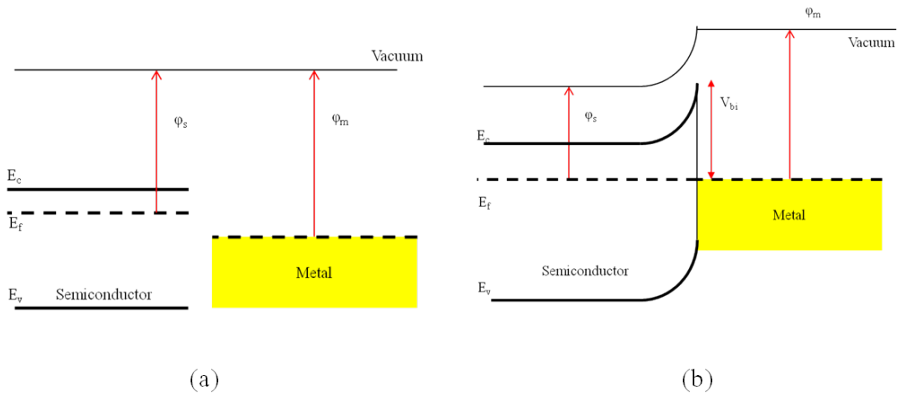


Figure 2.2: (a) Band structure of the doped semiconductor and metal while separated. (b) Band structure of the doped semiconductor and metal after making contact

In addition to the Schottky depletion capacitance, the diode also exhibits a series resistance associated with the motion of electrons through the conductive regions of the device. To accurately model the diode's series resistance, knowledge of the diode and ohmic contact geometry is critical. Figure 2.3 shows a cross section of a planar Schottky diode. The total series resistance (R_s) is composed of three primary components. Each of these three represents losses in a different region along the signal path [2].

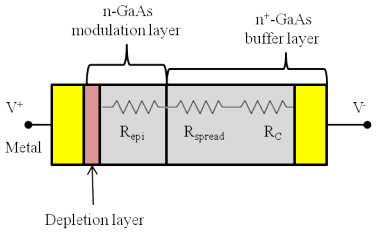


Figure 2.3: A model displaying the regions of the device that contribute to the series resistance

Typically the least significant of the three is the resistance that arises as current flows through any undepleted epi-layer adjacent to the diode's depletion region (Z_{epi}). As current flows from the diode contact it spreads out, resulting in a spreading resistance that is a function of the geometry of the contact (Z_{spread}) [4]. The final component is associated with the specific contact resistance of the ohmic contact. A significant body of research exists on the metallurgy and annealing processes

used to form and minimize the resistance associated with ohmic contacts (Z_C) [3]. The total series resistance of a diode can be written as;

$$R_s(f, V_{bias}) = Z_{epi}(f, V_{bias}) + Z_{spread}(f) + Z_C(f)$$

Figure 2.4 shows the basic circuit model of an intrinsic Schottky diode. The model does not include parasitics associated with the geometry and environment. The model consists of of three fundamental components: a voltage dependent junction capacitance in parallel with a voltage dependent junction resistance and a series resistance. The voltage dependent elements arise due to the potential barrier and depletion layer created at the metal to semiconductor contact. The value of these elements can be varied through the applied bias and are generally treated as independent of frequency. The series resistance is the combination of the three components representing loss in different regions of the semiconductor, as described above. The series resistance is a function of the applied bias as well as frequency.

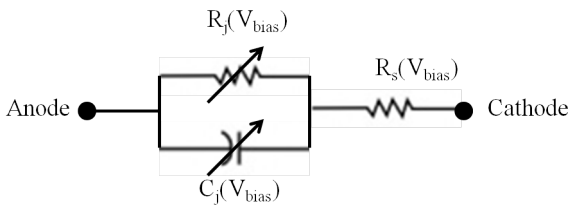


Figure 2.4: Schottky diode equivalent circuit model

2.1.1 Current-Voltage Relationship

The primary transport mechanism for a Schottky contact in forward bias is thermionic emission of majority carriers (electrons) over the junction energy barrier. The forward current is described by the exponential relation:

$$I_d(V, T) = I_S(e^{\frac{qV}{\eta kT}} - 1) \tag{2.1}$$

$$I_S(T) = AA^{**}T^2 e^{\frac{-q\varphi}{kT}} \tag{2.2}$$

Equation 2.1 describes the current voltage relationship of a Schottky barrier where q is the fundamental charge, k is Boltzmann's constant, η is the ideality factor, V the applied external bias voltage and T the absolute temperate in Kelvin. For an ideal diode, η is near unity, however, the ideality factor begins to increase when other transport mechanisms, such as tunneling through the barrier or high-level carrier injection, become important.

Equation 2.2 describes the diode saturation current I_S. The saturation current is a function of; the diode area, the effective Richardson constant A^{**} for <100> n-type GaAs, the barrier height of the metal to semiconductor contact φ , and temperature.

In reverse bias the depletion region adjacent to the metal is depleted of electrons and is highly resistive to current flow. As the reverse bias is increased the width of the depletion layer grows increasing the resistance . However, as the bias increases so does the electric field within the depleted semiconductor. There is a voltage, breakdown voltage, at which the electric field is large enough to accelerate carriers with sufficient energy that collisions produce additions charge carriers. This phenomena, avalanche breakdown, causes a large current to flow abruptly at sufficiently high reverse bias.

$$V_{BD} = 60 \left(\frac{E_G}{1.1}\right)^{\frac{3}{2}} \left(\frac{N_d}{10^{16}}\right)^{\frac{-3}{4}} \tag{2.3}$$

Equation 2.3 is an expression to predict the break down voltage, V_{BD}, for a diode with given doping and epi-layer thickness. The breakdown is a function of $E_g$the bandgap energy and substrate doping level N_d

2.1.2 Capacitance-Voltage Relationship

As discussed earlier when a metal is brought into contact with the semiconductor the difference in energy drives a flow of electrons from the semiconductor into the metal to equalize the Fermi energies on both sides of the junction. This electron motion depletes a certain volume of semiconductor

adjacent to the junction of carriers, and the width of the depletion can be varied with an applied bias.

Equation 2.4 shows the relationship between the depletion width, W_d, and the applied bias. The depletion width is a function of the relative dielectric constant ε, substrate doping N_d, and built-in voltage V_{bi}. Using the depletion width, a first approximation for the diode junction capacitance can be made using the parallel plate capacitance model.

$$W_d(V) = \sqrt{\frac{2\varepsilon}{qN_d}\left(V_{bi} - V - \frac{kT}{q}\right)} \tag{2.4}$$

Equation 2.5 provides an approximation for the diode capacitance as a function of bias voltage, diode area (A), and the effective dielectric constant (ε). However, as the anode size decrease, fringing effects, which are neglected in the parallel plate approximation, become important.

$$C_d(V) = \frac{\varepsilon A}{W_d(V)} \tag{2.5}$$

Equation 2.6 [5] is a parasitic capacitance that can be added to equation 2.5 to correct for the fringing effects. In equation 2.6 $D_{anode}$is the diameter of the Schottky diode.

$$C_{fringe} = \frac{3\varepsilon A}{D_{anode}} \tag{2.6}$$

2.1.3 Series Resistance

As discussed earlier the series resistance generally consists of three parts each representing loss in a different region of the diode. Figure 2.3 shows a diagram of a Schottky diode and highlights the three individual resistances; Z_{epi}, Z_{spread}, and Z_C.

Equation 2.7 represents the loss due to the resistance of any undepleted epi-layer between the depletion region and the n^+GaAs. It is a function of the layer thickness t_{epi}, semi-conductor resistivity ρ_{epi}, diode area A, and bias voltage V. The impedance is a function of frequency and will scale as the depletion width modulates.

$$Z_{epi}(V,f) = \frac{t_{epi}(V)\rho_{epi}(f)}{A} \tag{2.7}$$

Z_{spread} models the impedance of the higher doped buffer layer between the anode and ohmic contact. In order to calculate the Z_{spread} knowledge of the ohmic contact geometry is necessary, specifically the radii of the ohmic contact and anode. This part of the series resistance will also add a positive reactance to due to the length between the anode and ohmic contact and frequency scattering within the semiconductor.

Equation 2.8 describes the spreading resistance within the buffer layer. The spreading resistance is a function of frequency and depends highly on the geometry of the Schottky and ohmic contacts. Within equation 2.8 R_{OC} refers to the radius of the ohmic contact, R_d is the radius of the ohmic contact, and δ is the skin depth.

$$Z_{spread}(f) = \frac{\rho_{epi}(f)}{A} tan^{-1}\left(\frac{R_{OC}}{R_d}\right) + \frac{(1+j)\,\rho_{epi}(f)}{2\pi\delta(f)} ln\left(\frac{R_{OC}}{R_d}\right) \tag{2.8}$$

The final contribution to the series resistance is associated with the ohmic contact itself. This value is specific to the ohmic contact geometry and the metallurgy used to create the ohmic contact. Equation 2.9 predicts the ohmic contact resistance. The ohmic contact resistance is a function of the sheet resistance of the highly doped semiconductor R_{sheet}, the transfer length L_t, and the radius of the ohmic contact.

$$Z_C = \frac{R_{sheet} L_t}{2\pi R_{OC}} \tag{2.9}$$

The sheet resistance can be calculated by knowing the doping level of the buffer layer. The transfer length, however, must be experimentally solved for and will vary for every GaAs die. Further explanation of the transfer length is discussed in chapter 4.

2.2 Planar Schottky diodes

2.2.1 Physical Structure

Planar Schottky diodes were developed in the early 1990's and became very attractive for use at millimeter and submillimeter application. Previous whisker contacted devices were prevalent in early development and application of Schottky diodes. The planar diode structure addressed many of the issues and drawbacks associated with the whisker contacted devices. Planar devices offered a much higher level of compatibility with typical microwave circuits and are much more robust, capable of handling moment and shock. This section will describe the specific issues associated with modeling and designing planar Schottky diodes.

The circuit model shown d in Figure 2.5 strictly refers to the metal semiconductor contact and conduction through the diode epi-layer and buffer layer. The geometry and architecture of a diode that allows it to be interconnected to a circuit however, contribute to parasitic circuit elements that must be accounted for in microwave circuit design. As an example, Figure 2.5 shows an SEM image of a typical planar Schottky diode and an illustration of its cross section. In this example the GaAs mesa is insulated by a layer of silicon dioxide and the buried ohmic contact serves as the cathode contact. A length of metal that makes contact to the anode, known as the finger, overlaps the mesa slightly to create the Schottky contact through an etched via in the SiO_2layer. This section well further elaborate on the parasitics associated with planar Schottky diodes and how they are solved for with computer based models and equivalent circuit designs. To help validate the models two sets of Schottky diodes were designed, fabricated, and measured. One set is designed for characterization around 20 GHz and the other 625 GHz. The same approach will be used to model and characterize the Schottky diodes, despite the differences in operational frequency and physical size. The results will show the validity of this approach to characterize planar Schottky diodes over a wide range of frequencies.

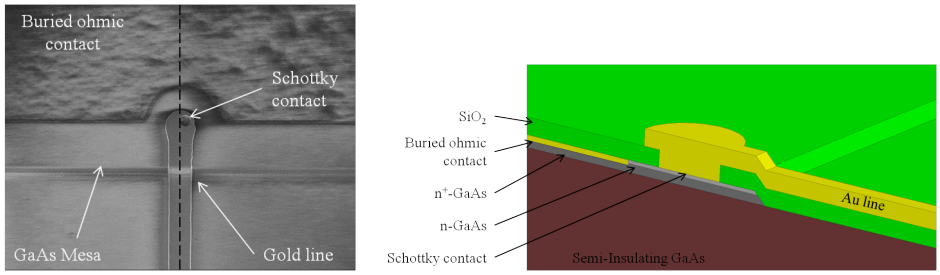


Figure 2.5: Left: A SEM image of a typical planar Schottky diode. Right: An illustration of a cross section taken from the cut line seen in the left SEM

2.2.2 Equivalent Circuit Model

Reactive parasitic circuit elements are always introduced due to the geometry and layout of the device. At sufficiently high frequencies, these parasitic elements seriously impact and degrade the performance of the device. Consequently, it is important to accurately model and characterize these parasitic elements in order to tailor the device geometry to mitigate their impact.

Figure 2.6 shows the layout of a typical planar Schottky diode along with its associated parasitic circuit elements. The finger, which forms the anode contact and creates the Schottky contact, is typically modeled as an inductance, L_f. The finger can also be modeled as a short section of transmission line. However, since typical finger lengths range in the tens of microns, modeling the finger as an inductor is sufficient to accurately characterize the fingers reactance.

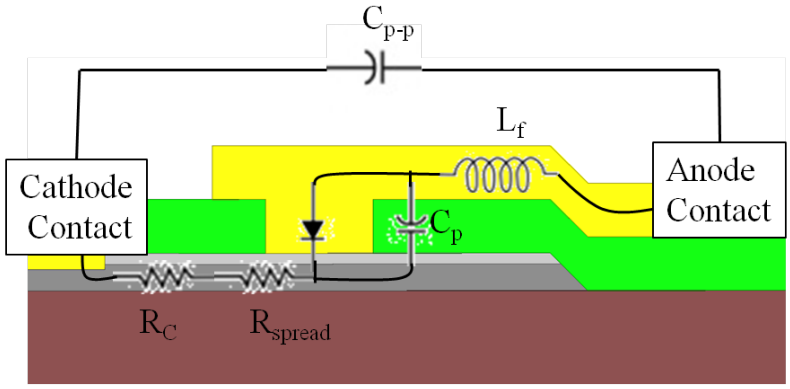


Figure 2.6: An illustration showing the cross section of a planar Schottky diode and its accompanying parasitics

Although series inductance can be detrimental, the finger length and width can also be used as an tuning element to help match or create a resonance with the diode junction capacitance. Lengthening the line or shrinking the width, for example, will constrict current flow and increase the effective inductance of the finger. Using finite element electromagnetic solvers (such as HFSS) the parasitic inductance can be accurately predicted. The finger also introduces a shunting capacitance to the diode's ohmic contact, C_{p-p}. This capacitance is known as the pad-to-pad capacitance and is in parallel with the entire structure. It is typically very small, <1 fF, but its effect on the circuit can be measured.

Another parasitic element resulting from the finger overlapping the mesa is a shunting capacitance directly in parallel with the intrinsic diode model, C_p. This capacitance can range from one femtofarad to 10's of femtofarads. At low frequency operation the impedance of this element is very high, reducing its effect on the circuit. However, as the operation frequency increases, and the impedance of C_p drops, it can begin to shunt out the diode completely. It is this capacitance which severely limits the operation of most planar diode designs at high frequencies.

2.2.3 Integrated Tuning Element

For this research, a goal is to realize an array of planar varactor Schottky diodes to address the power handling and increase the power output of sideband generators. Moreover, one of the objectives of this approach is to reach theoretical limit of conversion loss for a matched, lossless sideband generator, which is 3.92dB[6]. The approach presented here differs from other sideband generator designs in several aspects. One unique element of this design is the incorporation of an extra tuning element to lessen the effects of the parasitic anode capacitance, lessen the effect of parasitic elements surround the diode, and ease the overall fabrication process by requiring a less complex diode geometry.

Typically, Schottky diodes fabricated for use at submillimeter frequencies include required elements, such as gold interconnects, that give rise to added inductances and capacitances. Some of these elements can be considered parasitic, that is, they are undesired because they negatively impact the performance of the device. Others can be used as adjustable tuning elements that may

be tailored to improve the performance of the device. Much work has been done either modifying or developing new diode geometries in an effort to lessen the undesired parasitics while tuning or adjusting certain features to attain a desired impedance. This particular approach invests most of its time and effort into the actual processing and process development of the Schottky diodes.However, the complicated process required to fabricated elaborate Schottky diode geometries results in lower yields and larger variability in the end.

In this work, a shunt transmission line stub is included with the Schottky diode to create an additional tuning element. Figure 2.7 shows the typical planar Schottky diode layout with an added tuning element that extends the length of the finger contact. Figure 2.8 shows the equivalent circuit model for this diode geometry laid over on the device geometry.

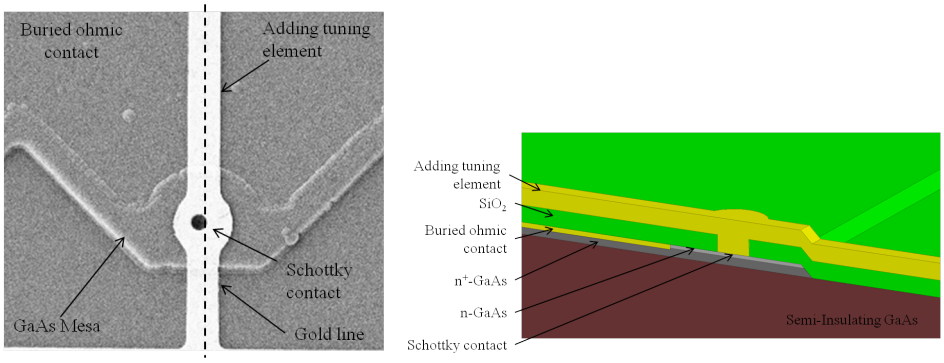


Figure 2.7: Left: A SEM image of a typical planar Schottky diode with an added tuning element. Right: An illustration of a cross section taken from the cut line seen in the left SEM

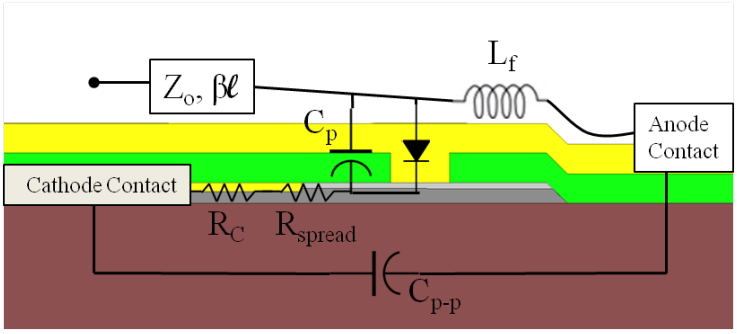


Figure 2.8: An illustration showing the cross section of a planar Schottky diode with the added tuning element and its accompanying parasitics

The tuning element is a microstrip line whose ground plane is formed by the ohmic contact of the diode. The tuning element improves the overall design in many different ways. The most influential is that part of the parasitic capacitance once associated with C_p becomes a part of the distributed capacitance associated with the microstrip line. This change in circuit model effectively lessens the parasitic capacitance C_p without having to alter the geometry of the planar structure, simplifying the fabrication process greatly. Another advantage from the reduction of parasitic C_p is the ability to use larger anode sizes. The increase in anode size will help to lower the series resistance and allow for higher currents. Both these effects will help increase the overall power handling of the device. To create a tuning element to incorporate into an array of Schottky diodes, an approach which makes use of array symmetry is used. The arrayed design creates electrical walls along the horizontal symmetry lines. The electrical wall boundary conditions is exploited to create a virtual RF short. Figure 2.9 shows a picture of a fabricated array while displaying the symmetry lines.

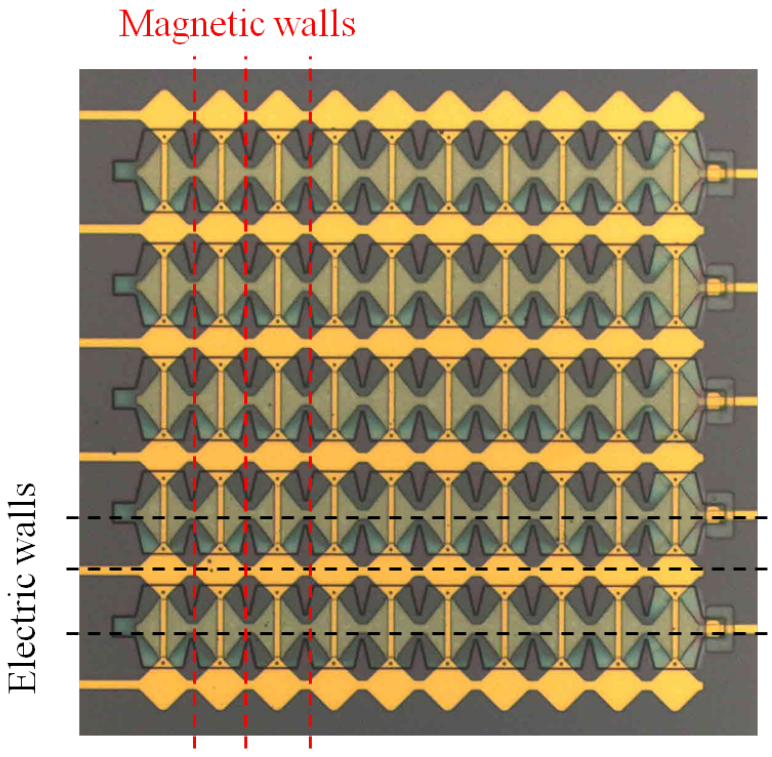


Figure 2.9: Microscope picture of a fabricated array showing the lines of symmetry

2.3 Diode Measurements and Equivalent Circuit Models

To better understand and characterize the Schottky diodes at millimeter and sub-millimeter wavelengths, a set of Schottky diodes designed for microwave on-wafer measurements, were fabricated, and characterized. The data obtained from these devices are used in verifying the intrinsic diode circuit model and surrounding parasitic elements. One of the prototype devices was designed to be characterized at 20 GHz and demonstrates the utility of an added tuning element to extend the reactance variation of the device with a bias. Using a symmetric structure, the tuning element (a section of coplanar waveguide) is terminated in a virtual short under odd mode excitation, thus modeling as a virtual electrical wall. The second set of diodes are intended for measurement and characterization in the WR-1.5 band (500 and 750 GHz). These measurements will be used to evaluate the circuit model for characterizing Schottky diodes and its associated parasitics at microwave frequencies and the suitability of scaling such models to sub-millimeter wave frequencies..

2.3.1 20 GHz Measurements

A low frequency proof-of-concept diode circuit was designed and fabricated to test the planar diode fabrication process, evaluate the validity of the Schottky diode and parasitic models derived from HFSS and DC measurements, and to show the effects of the addition tuning element to resonant with the reactances associated with the planar Schottky diode. Figure 2.10 shows a microscope image of the diode layout. The structure is 2 back-to-back symmetric diode structures which create a virtual short at the symmetry plane when the network is driven with an odd mode excitation. The goal is to realize a device whose admittance can sweep between an open and short circuit as the bias is varied, making use of the series and parallel resonance possible with this circuit topology.

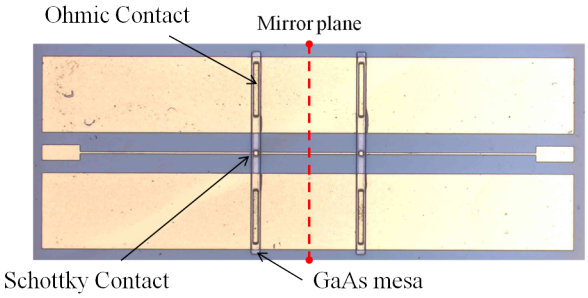


Figure 2.10: A microscope image of the low frequency proof of concept device, two 1-port devices mirrored end to end

To design the proof of concept device, two transmission-line tuning elements are integrated with the Schottky diode. For the specific design presented here, the tuning elements are co-planar waveguide (CPW) transmission lines. All the lines have a characteristic impedance of 90 Ohms with a center conductor width of 8 microns and a gap of 75 microns. The first element is a CPW line feed line to the diode. The second is a short circuited length of CPW in shunt with the diode. To attain an effective short circuit and to allow for biasing the diodes, the device is mirrored end to end. This creates a virtual short under odd mode excitation. Figure 2.10 illustrates the layout of the circuit. The two tuning elements are designed to present the necessary impedance to resonate with the diode's junction capacitance and resulting parasitic elements at a desired frequency. For this example 10 -30 GHz was chosen as a proof-of-concept demonstration, as probes and an on-wafer measurements station were available for this frequency band. The minimum and maximum bias voltages are chosen as the resonant points. The minimum voltage being just above the diode break down voltage and the maximum voltage being below the built-in voltage. The short circuited line in shunt with the diode is tuned to resonate an open circuit at the minimum bias voltage (Vbias = -3V). The second tuning element, the CPW feed line is chosen to create a series reactance the maximum bias voltage (Vbias = +.3V).

To accurately design tuning elements capable of resonating with the diode's impedance and parasitic elements it is necessary to understand the parameters intrinsic to the Schottky contact: the junction capacitance, reverse leakage current, and series resistance. Figure 2.11 shows a SEM image

of the fabricated circuit focused on the GaAs mesa step and Schottky diode. Figure 2.11 also shows the parasitic circuit model associated with such a mesa step. Because the diode is fabricated in the UVa Microfabrication Laboratory, its parameters can be adjusted and optimized for the intended application. The GaAs epi-layer forming the Schottky contact is n-type ($N_d = 3 * 10^{17} cm^{-3}$) with a thickness of 220nm. The anode diameter, which sets the overall diode capacitance and series resistance, is chosen to be 13µm. With the diode acting as a variable capacitor; the diode's area, epi-layer thickness and doping provide for a capacitance swing from ~85fF (-3V bias) to ~350fF (0.3V). The diode series resistance is also a critical parameter and several factors contribute to this component, including the resistivity of the undepleted epi-layer, spreading of current in the highly doped buffer layer, and contact resistance between the cathode and semiconductor. To minimize the series resistance, a low-resistance ohmic contact is fabricated as a semi-circle around the diode contact. In this way, the resistance can be approximated as the spreading resistance between the two concentric circles. In this case, a 6.5µm radius encircled by a 20µm radius results in a series resistance of ~8Ω. The final intrinsic diode parameter is the reverse leakage current associated with the diode junction. For the initial simulations the resistance associated with this reverse leakage was assumed to be very large.

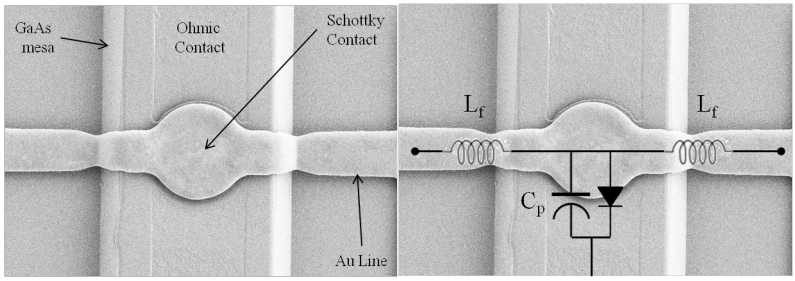


Figure 2.11: Left: A SEM image of the mesa step and Schottky contact Right: the added parasitic model accompanying this planar geometry

With preliminary values selected for the diode model, it is necessary to investigate the parasitic elements associated with the diode's physical geometry. The source of these parasitic components is the surface area of metal overlapping the slightly conductive GaAs and discontinuities in the device geometry. During the fabrication process the GaAs mesa is wet etched creating a nearly

trapezoidal mesa. The mesa is then covered with a thin dielectric layer of silicon dioxide, and the metal is patterned on top of the dielectric (details of the fabrication process will be described in the next section.) Figure 2.12 shows the GaAs mesa with the metal overlap creating the parasitic capacitance near the anode. In addition, the metal trace contacting the anode and discontinuities associated with the mesa give rise to an equivalent two-port network (represented as a T-network) that accounts for external parasitics.

To find approximate values for these parasitic elements, a computer model of the metal step and diode geometry was created in Ansoft's High-Frequency Structure Simulator (HFSS). Figure 2.12 shows the model used for these simulations. HFSS is a full-wave electromagnetic solver that can solve for the impedance matrix of a three dimensional passive structure. The resulting simulated impedance matrix is used to fit values in the T model for the parasitic elements. Figure 2.13 shows the circuit model used to fit to the HFSS results. From the simulations results and fitting, the values of the parasitic elements were calculated to be: L_p~ 25 pH and C_p~ 9 fF.

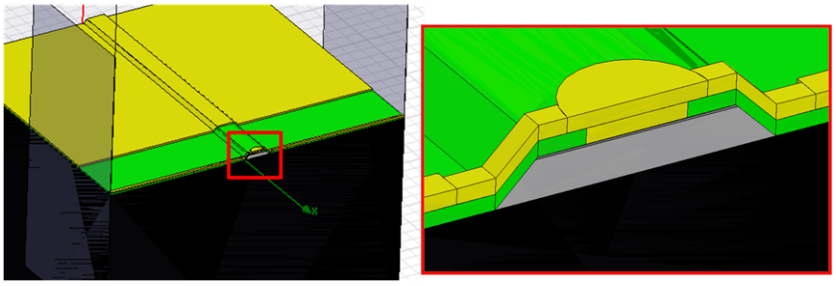


Figure 2.12: The HFSS model used to characterize the GaAs mesa step Schottky parasitic elements

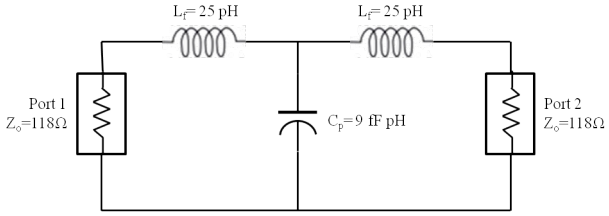


Figure 2.13: The circuit model used to characterize the HFSS drawing seen in Figure 17

With the complete circuit model for the diode and its parasitics determined, the next task is to

incorporate the tuning structures, a through CPW line and a short circuited CPW, and optimize them to resonate at the desired diode bias points. The two bias points were specifically chosen to be -3V and+.3V. At -3V bias the depletion region is approximately 180nm thick, which is nearing the epi layer thickness of 220nm. Consequently, voltages more negative lower than -3V can result in "punch through" and no additional capacitance modulation. A forward bias of 0.3V was chosen as the largest applied voltage because it is just below the diode's "turn on," leaving a ~.2-.3V of margin to account for slight variations due to fabrication.

To optimize the length of the CPW lines, a one port network was created to model the different impedances seen looking into the diode as a function of V_{bias}. With the aid of Agilent's Advanced Design System, the lengths of two lines were tuned to present an open circuit near V_{bias}=-3V and a short circuit at V_{bias}=+.3V. However, due to losses associated with the diode's series resistance and the resistivity of the metal lines, the device will always exhibit some loss due to the nature of plated gold.

During the processing a variety of "back to back" tuned diodes were fabricated with varying lengths of transmission lines. To measure S_{11} of the equivalent one port device, different methods were considered. The most direct is to excite the two-port structure's with signals that are 180^{o} out of phase (Odd Mode). By design the virtual short would create the equivalent one port device at each port. For this case the (S)-matrix for the "Back-to-Back" 2-port structure was measured, and afterward an odd mode result was calculated.

To determine the basic diode parameters, DC measurements were taken of the I-V response of the device. These measurements provided information about the series resistance, reverse leakage current, ideality factor, and built in voltage and allows the computer aided models to be adjusted to more accurately describe the diode. Figure 2.14 shows that values for the parasitics in the ADS model, associated with the mesa step, had to be adjusted to fit the measurements. These measurements demonstrated the utility of the equivalent parasitic T-network in representing the discontinuities near the diode anode. Table 2.1 shows a comparison of the predicted values to the measured and fitted values.

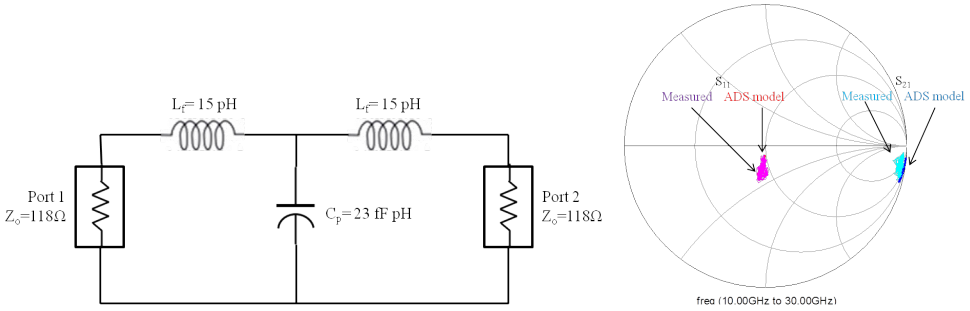


Figure 2.14: Left: The ADS model used to characterize the measured GaAs mesa step Right: The comparison between the ADS model and the measurement results

Device parameters	Simulated values	Measured values
Series resistance (Ω)	8	10
Anode diameter (μm)	13	15.4
Finger inductance L_f (pH)	25	15
Parasitic capacitance C_p (fF)	9	23
Gold conductivity (S/M)	$4.1*10^7$	$3.6*10^6$

Table 2.1: Comparing the simulated results to the measured values

During RF testing the diodes series resistance was measured to be about 10 Ω. To confirm this result the DC IV characteristics were measured beyond the built in voltage. The data was then fit to equation 2.10 using a least squares regression algorithm. The fitted data yielded a series resistance of about 10.2Ω.

$$V_{total}(I_{bias}) = V_{diode}(I_{bias}) + R_s I_{bias} \tag{2.10}$$

In order to determine the anode size, after the processing step which defines the anodes, the sample is put into a Scanning Electron Microscope (SEM). The SEM allows for very detailed photographs at large magnifications, it can be used to make length measurements. The SEM was

used to determine the final anode size after processing. The difference in the anode radius was a result of over etching during processing. The inductances associated with the metal lines over the mesa modeled fairly well compared to the measured results. The larger parasitic capacitance is due to the ideality of the computer aided model. The model assumed the epi-layers had zero conductivity when in reality each layer had a certain conductivity. This simulation setup only accounted for fringing capacitance straight to the ohmic contact metal but ignored any fringing to the doped GaAs. This added stray capacitance is what made the measured value larger. It was also discovered that the platted gold had a much lower conductivity than was used in the simulated models adding additional loss. As a note, the gold conductivity was calculated by fitting the to the remeasured TRL calibration lines.

The left of Figure 2.15 shows the response at 20GHz of the original simulation and the measured device. The increased anode size resulted in and increasing of the diode's junction capacitance and altered the two bias points creating the expected resonances. The added loss from the long, transmission lines can also be seen in the measured results. With the improved circuit model for the parasitic T-network and the Schottky junction, the largest phase shift were obtained at 21.5GHz. The right of Figure 2.15 shows the comparison between the diode without the shorted stub, with the shorted stub, and the measured results. The measured results show the tuning elements are resonating with the junction and parasitic reactances at the bias voltages of +0.3V and -3V.

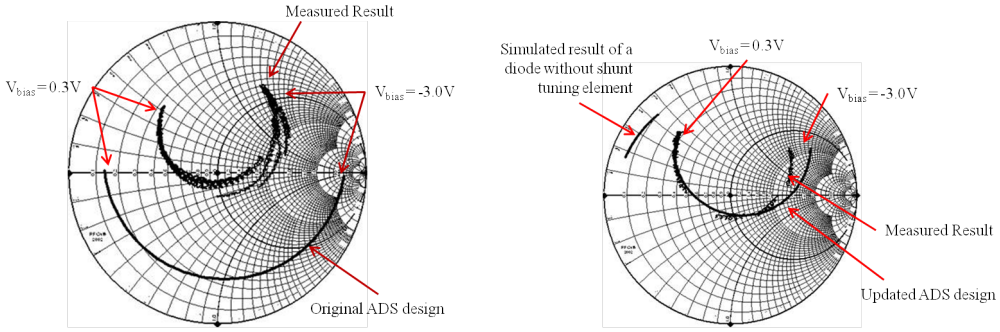


Figure 2.15: Left: Plotted results of the originally designed and measured phase shift at 20 GHz vs bias voltage Right: Plotted results of the updated ADS model, a diode without the shunt tuning element, and measured results centered at 21.5 GHz vs bias voltage

It was shown for this planar diode geometry the addition of tuning elements to the Schottky capacitance can increase the overall phase shift of the circuit and lower the added parasitic effects, allowing better performance for side-band generation. However, accurate and reliable values for the diode parasitic elements must be determined to exploit this approach in designing a sideband generator based on phase modulation. Understanding the precise impedance presented by the diode makes it possible to design the tuning elements, the lengths of CPW transmission lines, to resonate with the known diode reactances.

2.3.2 WR 1.5 Schottky Diode measurement and results

Until recently, direct measurement of the electrical parameters critical for designing Schottky diodes (and other submillimeter-wave components) could not be done and were based on electromagnetic simulation or scaled measurements at microwave frequencies. Over the past year, the development of micromachined probes for on-wafer measurements above 500 GHz has enabled the direct characterization of planar devices in the frequency range for which they are designed [7] equation 2.8. The results here are the first measurements of planar submillimeter-wave Schottky diodes using on-wafer probes in this frequency band. For these measurements, diodes with anode diameters varying from 2 μm to 3.5 μm were designed and fabricated. From the measurements device equivalent circuits are developed and circuit parameters extracted, permitting the establishment of diode models that are based on direct measurement without extrapolation.

Figure 2.16 shows an image of a simple prototype planar Schottky diode designed for this work. The diode is integrated directly into a coplanar transmission line to permit contact with CPW on-wafer probes. The CPW center conductor has a width is 8 μm with a gap of 6 μm giving the line a characteristic impedance of 50 Ω on a GaAs substrate. Anodes with diameters of 2.0μm, 2.5μm, 3.0μm, and 3.5μm were fabricated to allow comparison and assessment of device circuit models and their dependence on anode size.

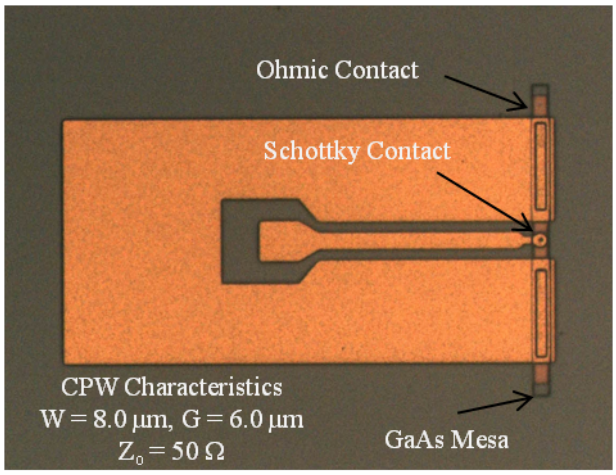


Figure 2.16: Microscope image of a CPW integrated planar Schottky diode (2 μm anode diameter) designed for direct measurement using coplanar micromachined probes

The diodes are fabricated on a semi-insulating GaAs substrate with two epitaxial layers: a highly doped ($5*10^{18}cm^{-3}$) layer 500 nm thick that is employed for the ohmic contact, and a lower doped ($4.5*10^{17}cm^{-3}$) layer,120 nm thick, to form the Schottky contact. The fabrication process consists of five standard steps: (1) formation of the ohmic contacts to the highly doped epilayer, (2) a wet etch to form a device mesa, (3) deposition of a 1μm thick silicon dioxide layer using PECVD to insulate the conductive mesas from the CPW lines, (4) reactive ion etching to define the Schottky contact through the silicon dioxide layer and (5) patterning and deposition of a Ti/Au metal layer to form the diode anode and coplanar lines.

The measurement system used to characterize the submillimeter-wave diodes consists of an Agilent PNA-X N5245A Vector Network Analyzer, a WR-1.5-VNAX frequency extension module manufactured by Virginia Diodes, Inc. and a micromachined on-wafer probe fabricated at the University of Virginia that is capable to applying a DC bias to the device under test. Figure 2.17 shows an image of the probe chip, showing the geometry near the contact tip. The spacing between the probe contacts is 30μm.

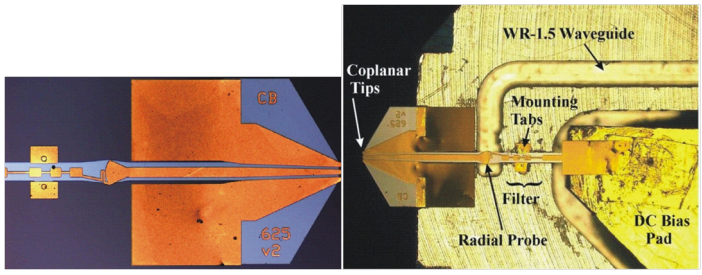


Figure 2.17: Left: An image of the WR-1.5 micromachined probe and Right: An image of the probe mounted to its housing

Initially, the diodes are characterized using their DC current voltage relationship which allows reverse leakage current, ideality factor, and break down voltage to be determined. To determine, R_s, I_o, and η, the forward bias data, 0.0V to 1.0V, is fit using a least square regression algorithm. Several diodes of corresponding anode size are measured and the average taken for each value. Figure 2.18 shows plots of the measured IV characteristics as well as the fitted curves. From this DC characterization the average series resistance for a 2.5μm diameter is 18Ω, the reverse leakage current is 12 nA, and the ideality factor is 1.4. To determine the reverse breakdown voltage Vb, the reverse bias data is used and the point where the current exceeds 500 μA is found to be -4.72 V.

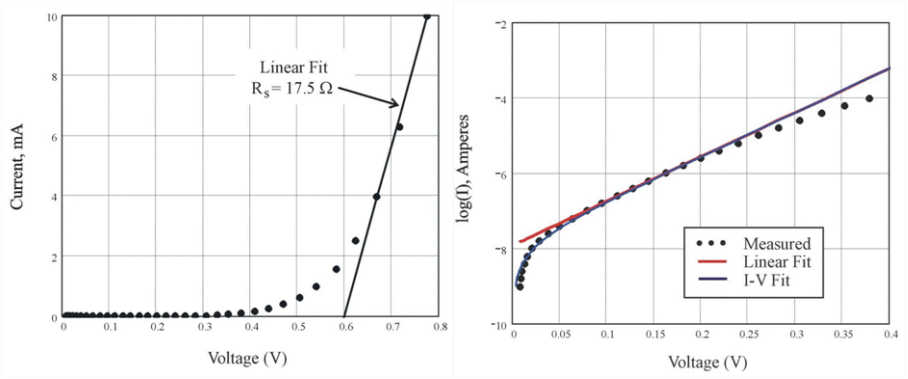


Figure 2.18: Left: Linear Right: logarithmic plots of the measured diode current-voltage characteristic. Also shown are least-squares linear fits to the data to estimate the diode series resistance, reverse saturation current, and ideality factor

To calibrate the system a set of five delay CPW short circuits were fabricated. Figure 2.19 shows

an image of the probe tip contacting one of the shorted calibration standards. With five different standards, the basic one-port error model is over-determined and this permits the characteristics of the CPW lines to be determined during calibration (Zo ~ 50Ω, εeff ~ 4.7.) The delays are in increments of 15 μm (corresponding to 10.12 ps). Figure 2.20 shows a photograph of the fully assembled micromachined coplanar probe fabricated by the University of Virginia and used in this work.

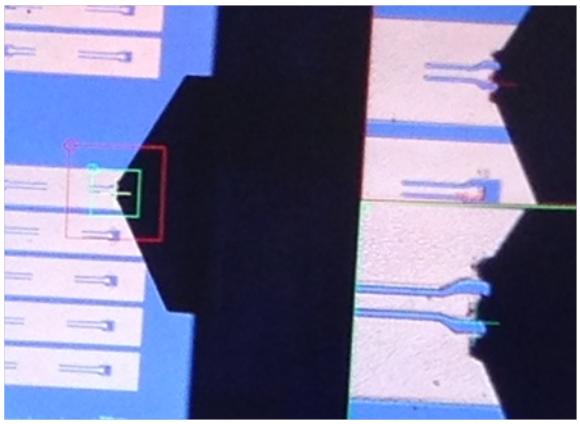


Figure 2.19: Image of the micromachined on-wafer probe contacting one of the delayed short CPW calibration standards at various magnifications

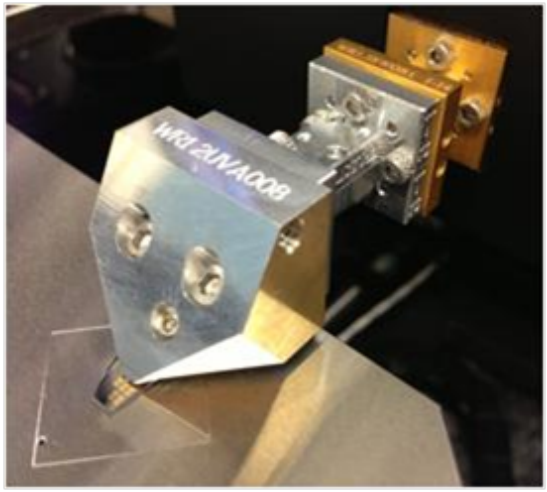


Figure 2.20: Image of a micromachined on-wafer probe contacting a planar Schottky diode.

To characterize the diodes and its equivalent circuit parameters, a model of the device geometry was created in Ansoft's High Frequency Structure Simulator. This permits parasitic elements surrounding the Schottky contact to be found through a least squares fit. The Schottky diode equivalent circuit model is included with its HFSS-derived parasitics to permit simulations with Agilent's ADS software. The results of these simulations are compared to measured data in the WR-1.5 band and the circuit parameters are optimized using a least squares fit to the measurements. Figure 2.21 shows an SEM of the Schottky diode and its basic equivalent circuit model, which includes a CPW transmission line with a series inductance and shunt capacitance representing the reverse-biased Schottky diode.

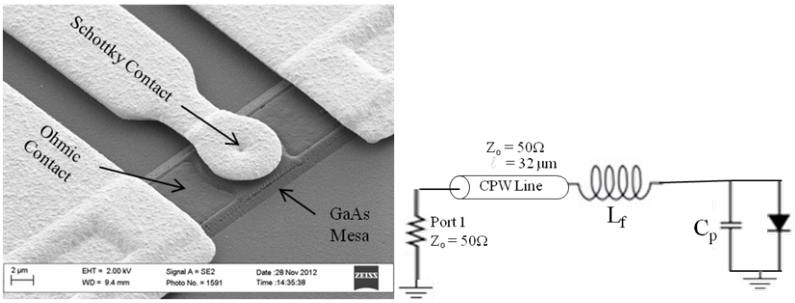


Figure 2.21: Left: A SEM image of the Schottky contact Right: The basic circuit model used to represent the parasitic elements around the Schottky diode

RF measurements of the Schottky diodes under different bias conditions are used to extract the diode parasitics. Figure 2.22 shows the HFSS structure used to model the parasitic elements surrounding the Schottky contact. The impedance of the CPW line has a characteristic impedance of 50Ω and length of 32 μm. The anode diameters vary from 2.0μm to 3.5μm, but the geometry surrounding the contact remains unchanged. Figure 2.22 also shows the equivalent circuit representing the HFSS model and a comparison between the HFSS results and the circuit model, which are in close agreement. The frequency-independent values for the diode parasitics are found by a fit to the HFSS simulation.

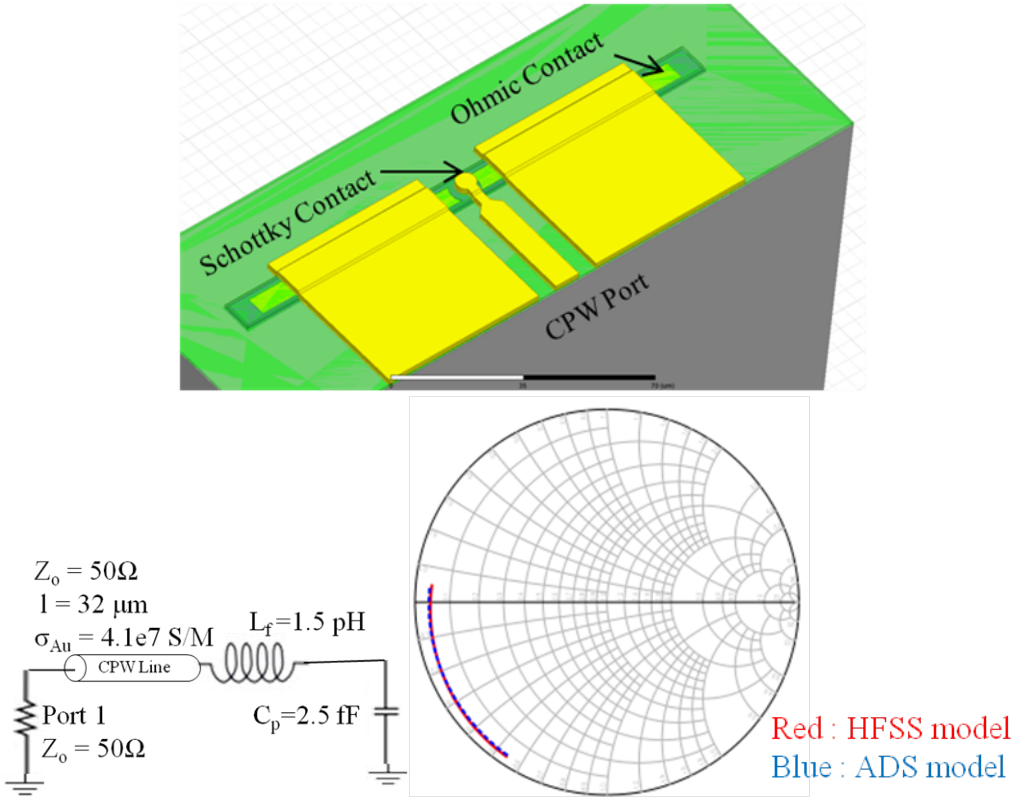


Figure 2.22: Top: HFSS model used to simulate the geometry surrounding the Schottky contact Bottom: Equivalent circuit and comparison of HFSS simulation and the equivalent circuit model from 500 to 750 GHz

With the basic model of Figure 2.22, measured s-parameters in the WR-1.5 band are compared to the circuit model with the Schottky diode included. In reverse bias, the diode is modeled as a series resistance and variable capacitor using the standard C(V) relation with a Cjo= 7.5 fF and Vbi = 0.66V. Measurements are performed at different biases from -4.0V to +0.3V. The series resistance is fixed to the DC value of 18 Ω. And the capacitance is calculated using the diode area, substrate doping, and bias voltage. Figure 2.23 shows the complete circuit as well as results from the circuit simulation compared to the measured s-parameters at different bias voltages and for different anode diameters.

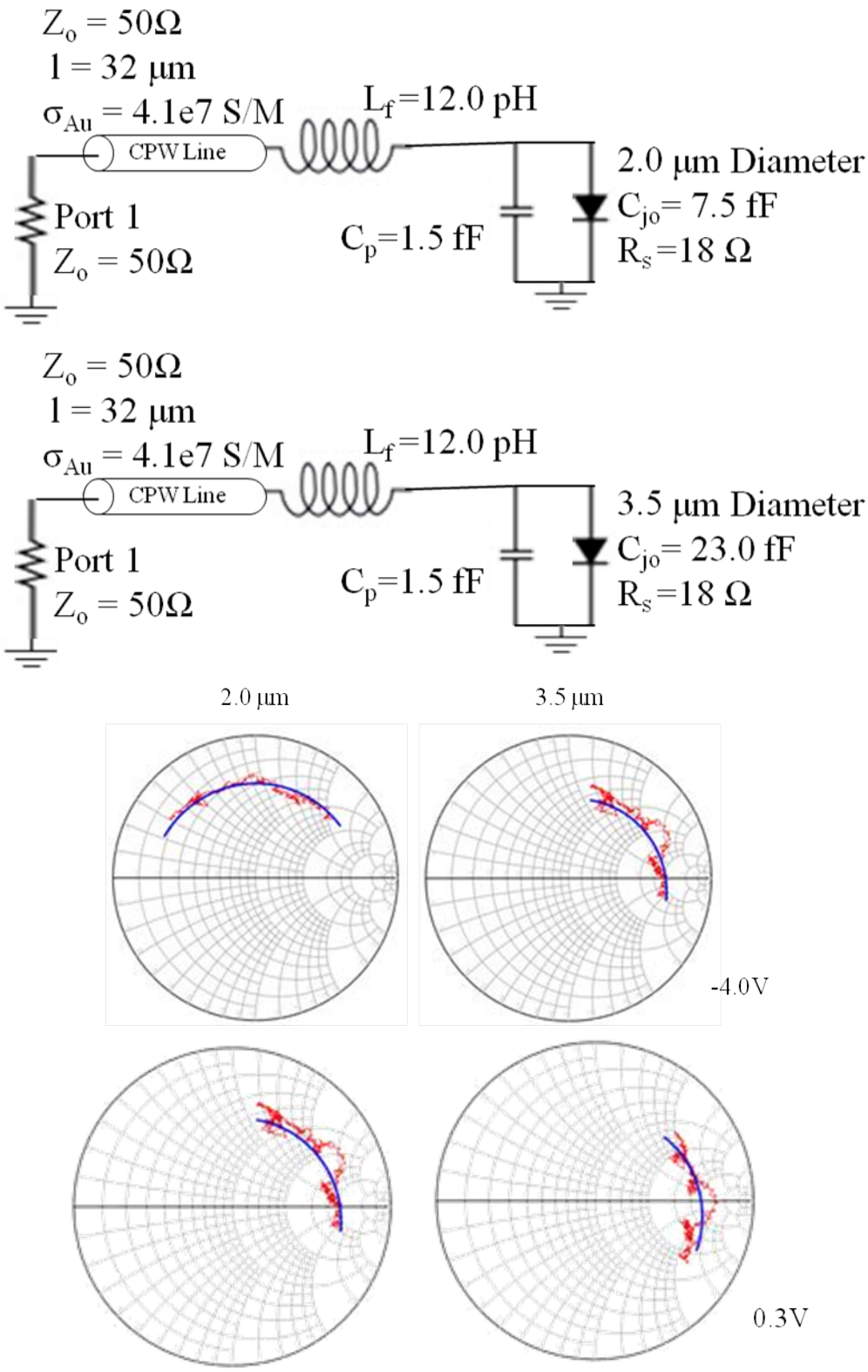


Figure 2.23: Circuit model and parameters used to represent a 2.0µm and 3.5µm diameter diode and comparison of measured s11 for diodes with anode diameter of 2.0µm (left) and 3.5µm (right). The red dots are measured points between 500 – 750 GHz and the blue line is derived from the equivalent circuit model.

Comparing the circuit model in Figure 2.22 to the fitted model of Figure 2.23, it can be noted that the most significant change needed to match the measured and modeled data is an increase in the series inductance Lf over the value extracted from the HFSS simulation. This increase can be attributed to several factors, the most important being the additional inductance associated with the ohmic contact itself. The HFSS simulations are done treating the GaAs epilayers as perfect dielectrics. This permits the 1.5 pH inductance associated with the CPW transition to be determined. However, the additional inductance associated with carrier flow in the device epilayers is not accounted for in this simulation. From the dimensions of the Schottky contact, epilayer doping, and the electron mobility of GaAs, a model for the high frequency series impedance of the diode predicts an added 15 Ω of reactance. This reactance is made of up two parts, the first due to conduction through the top 120 nm epilayer (12 Ω). The impedance associated with this epilayer is a function of frequency and depends on the anode diameter, and the frequency-dependent conductivity of the material. The second contribution is that due to current spreading from the anode to the ohmic contact itself (3 Ω of reactance). The spreading impedance is also a function of frequency and is dependent on the anode diameter, the diameter of the ohmic contact, and the conductivity of the highly doped buffer layer. At 625 GHz, the total reactance of 15 Ω is equivalent to 5 pH of inductance. HFSS was also used to determine inductance associated with the current flow through the length of the mesa. This is done by modeling the highly-doped GaAs layers as conducting. This results in an additional 4 pH of series inductance to the diode model. Adding the previously calculated reactance due to the top epilayer along with the inductance due to the conductive mesa brings the total expected inductance (10.5 pH) into good agreement with the 12 pH extracted from direct on-wafer measurements

With new measurement capabilities being developed for submillimeter wavelengths, it is now possible to directly compare measured results against predicted circuit models at submillimeter wavelengths rather than rely on scaled measurements. In this work, measurements verify that circuit models developed at low frequency for planar diodes can be scaled to higher frequencies. Moreover, direct measurement of devices in this frequency range allows parasitic elements to be extracted and equivalent models based on directly measured parameters to be developed for circuit

design.

Chapter 3

Sideband Generator Design and Simulation

This chapter gives a detailed description of the sideband generator layout, design, and relevant simulations. However, before going into detail about the actual sideband generator design, a brief description of sideband generation is presented. This is done to give the reader an understanding of the methodology used to design and optimize the sideband generator implemented in this work. After the analysis of sideband generation, an ideal case is presented. The ideal sideband generator is simulated using lossless lumped elements. The results from the ideal sideband generator determine the necessary embedding impedance to present to a Schottky diode centered at 1.6THz. The results also offer a starting point from which real circuit components can be derived converting from the ideal to a real case. The remainder of the chapter is devoted to the optimization of the sideband generator array. A brief overview of the physical layout is used to give an idea of how the the final device looks. Then the electromagnetic and equivalent circuit models for a unit cell are shown, along with their results. The components of the sideband generator array are optimized to present the necessary embedding impedance solved before. A non-liner analysis is performed to predict the conversion loss for the final sideband generator circuit.

3.1 Fundamental Limits of Double Sideband Resistive Mixers

To design and optimize a circuit for sideband generation, it is important to understand the conditions to be met to achieve a minimum conversion loss. The simplest case is examined. Figure 3.1 shows a circuit model used to describe an ideal sideband generator. The circuit consists of a RF source connected to an ideal diode. The ideal diode has no parasitics and is driven between two states, a perfect open and perfect short circuit. Another assumption is all the unwanted harmonics are reactivity terminated. Given these assumptions the circuit can be reduced to a three port network, Figure 3.2. In Figure 3.2, port one is the RF signal port, port two is the image port, and port three is the IF port.

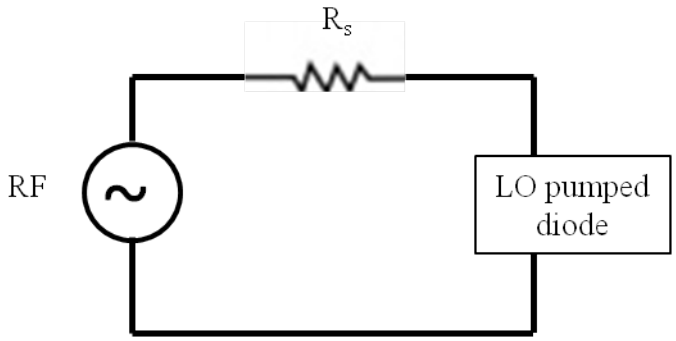


Figure 3.1: Simplest circuit model describing a sideband generator

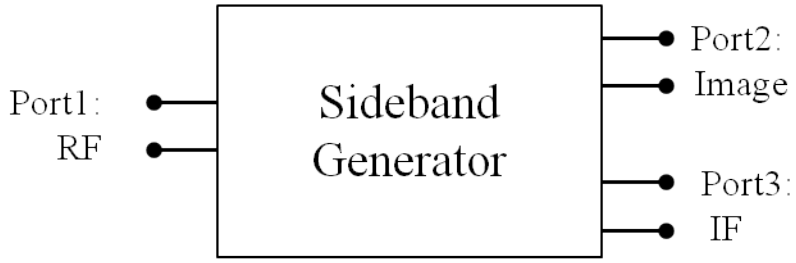


Figure 3.2: A three port network representing the sideband generator circuit in Figure 29

Because the RF and image ports are physically the same, the S-matrix of the sideband generator can be written as;

$$S = \begin{bmatrix} S_{11} & S_{11} & S_{11} \\ S_{11} & S_{22} & S_{11} \\ S_{11} & S_{11} & S_{33} \end{bmatrix} \tag{3.1}$$

Because we are assuming a losses mixer, the following is true;

$$\tilde{S} Y_0 S = Y_0 \tag{3.2}$$

where;

$$Y_0 = \begin{bmatrix} Y_{01} & 0 & 0 \\ 0 & Y_{01} & 0 \\ 0 & 0 & Y_{02} \end{bmatrix} \tag{3.3}$$

Performing the matrix multiplication of (3.2);

$$Y_{01}|S_{11}|^2 + Y_{01}|S_{21}|^2 + Y_{03}|S_{31}|^2 = Y_{01} \tag{3.4}$$

$$Y_{01}S_{11}^* S_{12} + Y_{01}S_{21}^* S_{11} + Y_{03}|S_{31}|^2 = 0 \tag{3.5}$$

$$Y_{01}S_{11}^* S_{13} + Y_{01}S_{21}^* S_{13} + Y_{03}S_{31}^* S_{33} = 0 \tag{3.6}$$

$$2Y_{01}|S_{13}|^2 + Y_{03}|S_{33}|^2 = Y_{03} \tag{3.7}$$

The conversion gain is given by;

$$G = |S_{31}|^2 \frac{Y_{03}}{Y_{01}} \tag{3.8}$$

From reciprocity;

$$Y_{01} \cdot S_{31} = Y_{03} \cdot S_{31} \tag{3.9}$$

Substituting (3.9) into (3.8);

$$G = |S_{13}|^2 \frac{Y_{01}}{Y_{03}} \tag{3.10}$$

And from (3.7);

$$G = \frac{1}{2}(1 - |S_{33}|^2) \tag{3.11}$$

From equation 3.11 it can be seen that a maximum conversion is achieved when the reflection at the IF port is zero. In this ideal case, half the input power is converted to the IF frequency, making the fundamental limit of conversion loss -3dB [6].

This analysis not only calculated the fundamental limits of conversion loss, but also defined a set of conditions that must be met to achieve such results. The analysis assumed a perfect diode. This meant a lossless device which was being switched between a perfect open and short. It also assumed all unwanted harmonics are reactivity terminated to prevent power dissipation at those frequencies.

3.2 Ideal Sideband Generator Circuit

In this section a sideband generator circuit is presented. The goal is to create a circuit, which meets the assumptions made by Kelly's [6] analysis, to approach the fundamental limit of conversion loss. The circuit will employ a perfect diode and two tuning elements. One tuning element is in series and the other in parallel with the diode. This topology was chosen because it offers an opportunity for the diode to resonate with the two elements as a short and open circuit at two different bias voltages. This simple analysis is done to obtain a better understanding of what variables impact the sideband generator circuit and its performance, including substrate doping, series resistance, and anode diameter. In addition, and more importantly, the results will provide an embedding

impedance that can be used as reference when designing a real device.

The simulations are based on the SBG setup seen in Figure 3.3. The SBG is placed on a high-resistivity silicon lens to focus power from a Far Infrared Red (FIR) laser onto the array and to help eliminate substrate moding.

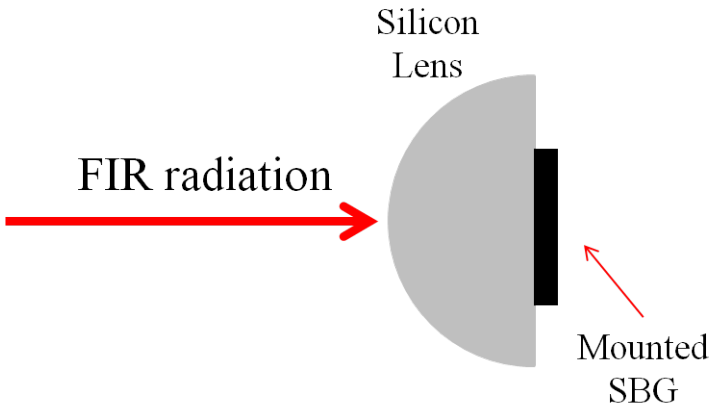


Figure 3.3: Depiction of the SBG die mounted to a hyperhemispherical lens similar to the SBG measurement setups

Figure 3.4 shows a basic circuit to represent the quasi-optical sideband generator design. The circuit is a one port device with three fundamental circuit components. There are two tuning elements and a variable capacitor to represent an ideal losses diode. The port impedance is 104Ω as the array lies on a semi-insulating GaAs substrate with $\varepsilon_r = 13$.

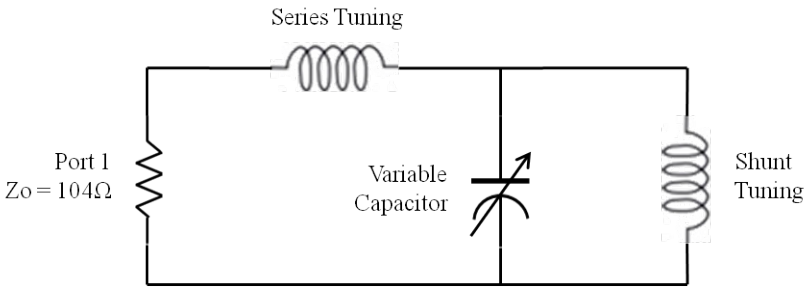


Figure 3.4: Initial ADS simulation to model the quasi-optical design

The left of Figure 3.5 shows the simplified SBG circuit with the optimized circuit elements. The

simulation was done at a single frequency, 1.6THz, while the value of the diode capacitance varied 1 to 3 fF. The right of Figure 3.5 plots the reflection coefficient as a function of the ideal diode capacitance. The goal is to create a circuit which meets the conditions determined by Kelly to achieve the minimum conversion loss of 3 dB, a loss circuit which can switch between an open and short circuit, or vary its phase by 180 degrees, with all un-wanted harmonics terminated reactively. The Smith chart in Figure 3.5 shows the circuit meets these the two conditions. The Smith chart shows the phase of the circuit varies 180 degrees at both ends of the capacitance sweep. However, given this circuit topology all the harmonics will be dissipated in the same 104Ω load.

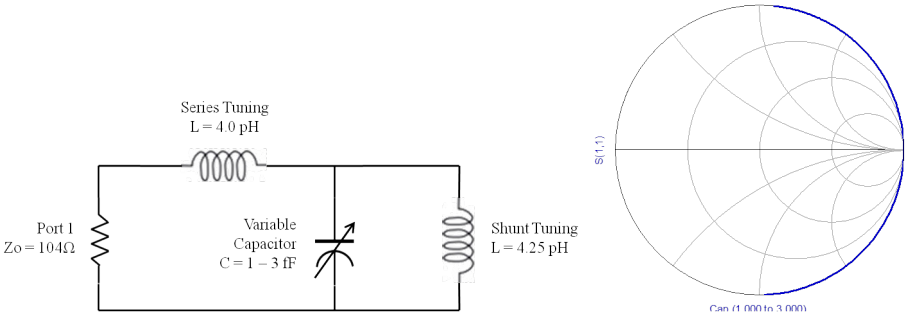


Figure 3.5: Left: The initial ADS quasi-optical simulation with the tuned values Right: is the S_{11}response plotted vs the variable capacitor values

The above simulation only considers the most basic elements required to realize a sideband generator based on parametric upconversion and has been described to illustrate the fundamental consideration needed in the design. However, a proper design and simulation must include a more realistic model for the diode and its parasitics, as well as the circuit architecture surrounding the device. A full wave electromagnetic simulator such as Ansofts's High Frequency Structure Simulator (HFSS) can be used to accurately represent a physical device. The resulting diode model will possess a series and junction resistance as well as parasitic reactances associated with the embedding circuit. Apart from modifying the values in the simplified circuit model above, additional parasitic elements will be added to better model the full wave results.

3.3 Sideband Generator Layout

Figure 3.6 shows the general chip layout for the quasi-optical sideband generator showing the electrical contacts and area occupied by the SBG chip (2x2mm). The array consists of 100 Schottky varactor diodes each within a 25 μm^2 unit cell. The array is fabricated on a semi-insulating gallium arsenide wafer. The device is based on a quasi-optical architecture that eliminates the need for waveguides and allows incident power to be spread over many devices. The admittance the array presents to the submillimeter wave signal will be modulated by a microwave pump signal provided through a 50 Ω transmission line shown in Figure 3.6.

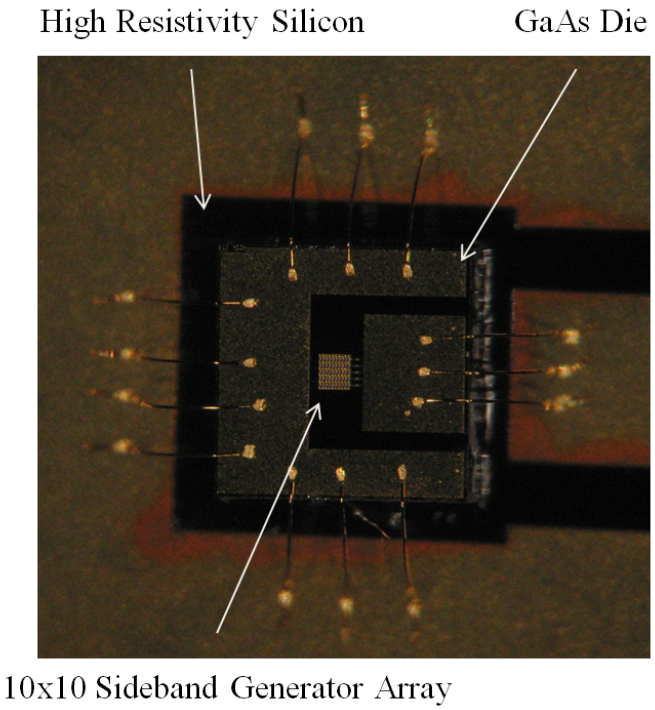


Figure 3.6: A picture of the 1.6 THz Sideband generator array layout

A design goal is to realize a SBG capable of approaching the fundamental limit of conversion loss given by Kelly. To do so, a unit cell geometry as seen in Figure 3.7 is proposed. A bowtie transmission line is used to feed the Schottky diode. One half of the bowtie is plated gold while

the other half is a buried ohmic contact. This bowtie transmission line serves as a series tuning element used in the ideal simulations seen in Figure 3.5. A second tuning element is a microstrip line that extends from the anode contact to the end of the unit cell. Its ground plane is the buried ohmic contact. This microstrip line serves as a shunt tuning element seen in Figure 3.5.

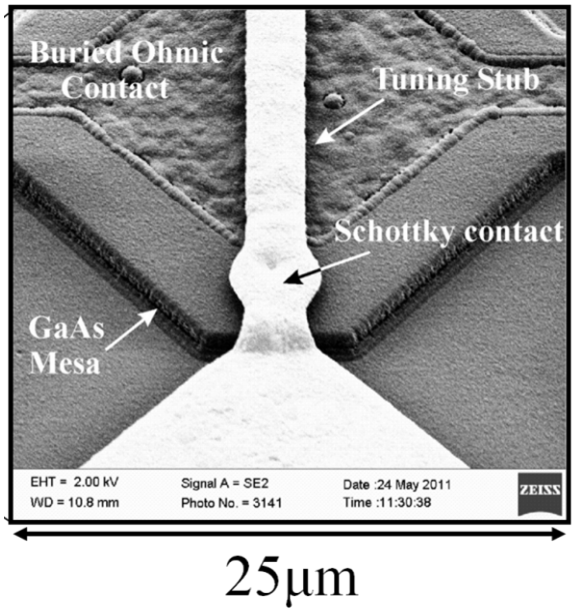


Figure 3.7: A SEM image of a unit cell

Figure 3.8 shows a cross section of a planar Schottky diode layout with an added tuning element that extends the length of the finger contact. Figure 3.9 shows the equivalent circuit model for this diode geometry overlaid on the device geometry. The tuning element is a microstrip line whose ground plane is the ohmic contact of the diode. For this tuning element to create a parallel resonance with the parasitic C_p, it must present an inductive impedance to the diode. There are several ways this tuning stub can be designed as an inductive element. The most direct solution is to terminate the line in a short circuit. However, this obviously would make it impossible to apply a bias voltage to the diode. A second option is to have an open circuited line with a length greater than a quarter wavelength. This may add significant loss considering the required long length of the line. This approach would also reduce the bandwidth of the overall device. The approach taken here

is to exploit the symmetry of the array to create virtual short circuits at the array symmetry planes, Figure 3.10 shows an image of a fabricated array displaying the symmetry lines. By exploiting the virtual shorts inherent in the array, a proper choice of line impedance allows for a shunt inducting tuning element without interfering with application of bias voltage. The tuning stub in addition to the typical finger contact would create a device capable of producing both a series and parallel resonance. With the added tuning elements it becomes possible to create a sideband generator that can approach the optimum theoretical limit of conversion loss.

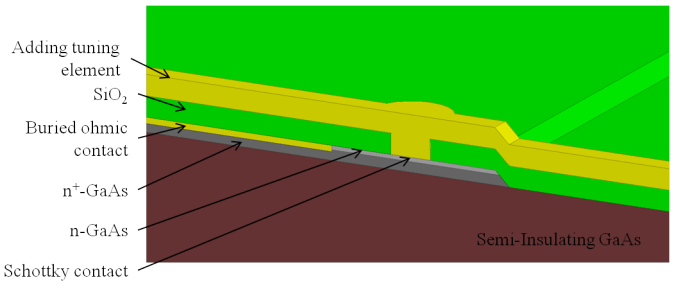


Figure 3.8: An illustration of a cross section taken from Figure 35

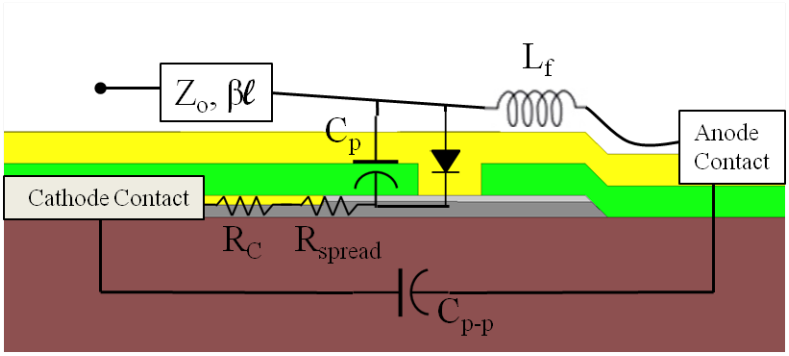


Figure 3.9: An illustration showing the cross section of a planar Schottky diode with the added tuning element and its accompanying parasitics

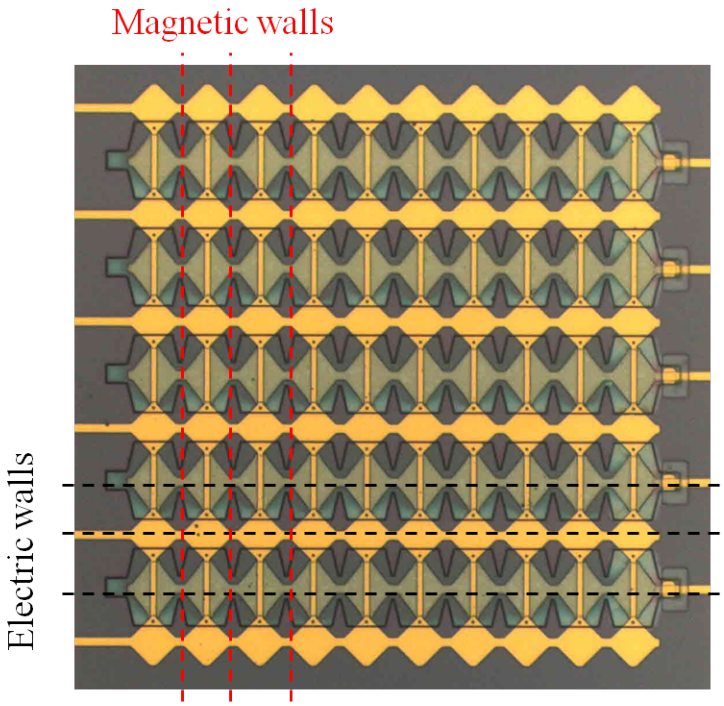


Figure 3.10: Microscope picture of a fabricated array showing the lines of symmetry

3.4 Unit Cell Description

The array unit cell is simulated as a section of waveguide with electric walls on top and bottom and magnetic walls on the sides. The boundary conditions are due to how the unit cells are arrayed. A portion of the waveguide is filled with air, to represent free space, and the remainder filled with dielectric to represent the GaAs substrate. The waveguide is 25x25μm square with a length of 100 μm. Figure 3.11 shows the HFSS model of the unit cell sections . Perfect electrical walls are placed on the walls perpendicular to the wave port's integration lines to maintain the boundary condition arising from symmetry. This setup represents the array as seen by an excitation source. The waveguide boundary conditions allow for the propagation of TEM modes which represent plane waves propagating to and from the array.

Figure 3.11 also shows an equivalent transmission line circuit model that represents the unit cell.

The port impedances of the circuit are the TEM impedances of the respective media, 377Ω for free space and 104Ω for GaAs ($\varepsilon_r \sim 13$). The results of the initial simulation is a step to confirm the proper modeling and to ensure the setup is correct for future simulations involving more complex array architectures.

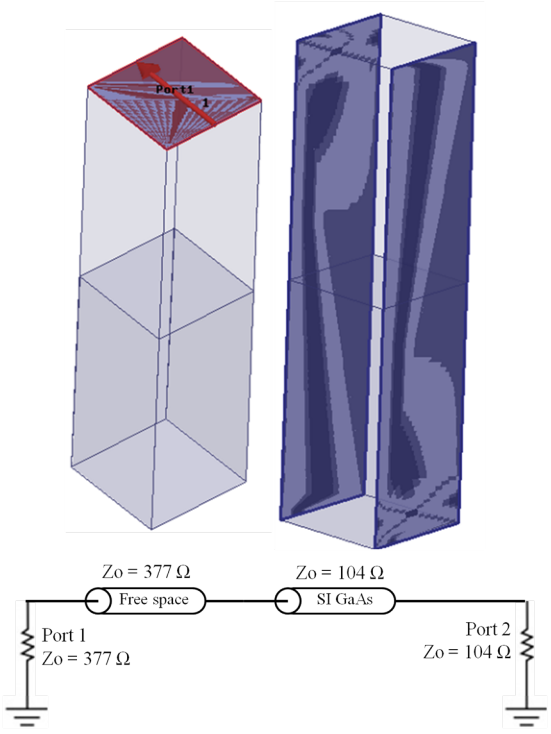


Figure 3.11: HFSS model of the back to back waveguide setup and the accompanying lumped element circuit model

3.4.1 Bowtie Array Design

The array structure is based on the bowtie antenna which has the advantages of being well characterized and can be modeled as a transmission line [24]. Figure 3.12 shows the HFSS model for a short-circuited bowtie antenna lying within a unit cell on a GaAs substrate . The integration line for one of the ports is noted so the orientations of the boundary conditions are known to the reader. Figure 3.12 also shows the circuit model for the HFSS geometry. The bowtie unit cell can

be represented in circuit theory as an equivalent transmission line. With the two arms contacting at the feed point, the antenna behaves as a short-circuited transmission line. Simulations show that with a 45° bowtie, with the specific dimensions of 25 μm^2 on a GaAs substrate, the bowtie equivalent transmission line has a characteristic impedance of 80 Ω and an electrical length of 20 degrees at 1.6 THz.

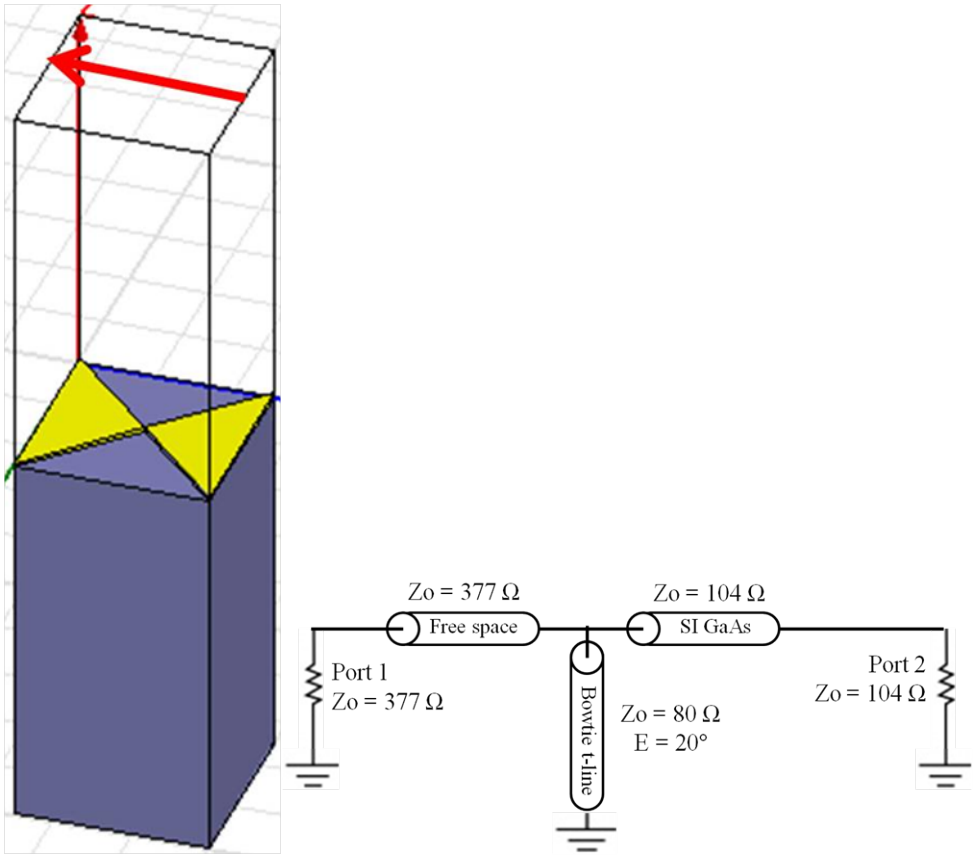


Figure 3.12: HFSS model of a simplified bowtie and accompanying lumped element model

3.4.2 Unit Cell Characterization

After determining the electrical parameters of the bowtie, the geometry of the unit cell is adjusted to account for the diode and to reflect the actual geometry of the full unit cell. Figure 3.13 shows the HFSS model of the bowtie design incorporating a diode. A GaAs mesa in included with an

ohmic contact buried beneath a one micron thick insulating layer of silicon dioxide. Also, a 2μm metal cap is added for alignment tolerances. That metal cap forms the Schottky contact and is somewhat larger than the anode itself. The cap adds considerable capacitance to the diode but is advantageous, from a fabrication perspective, in eliminating issues with tight alignment tolerances.

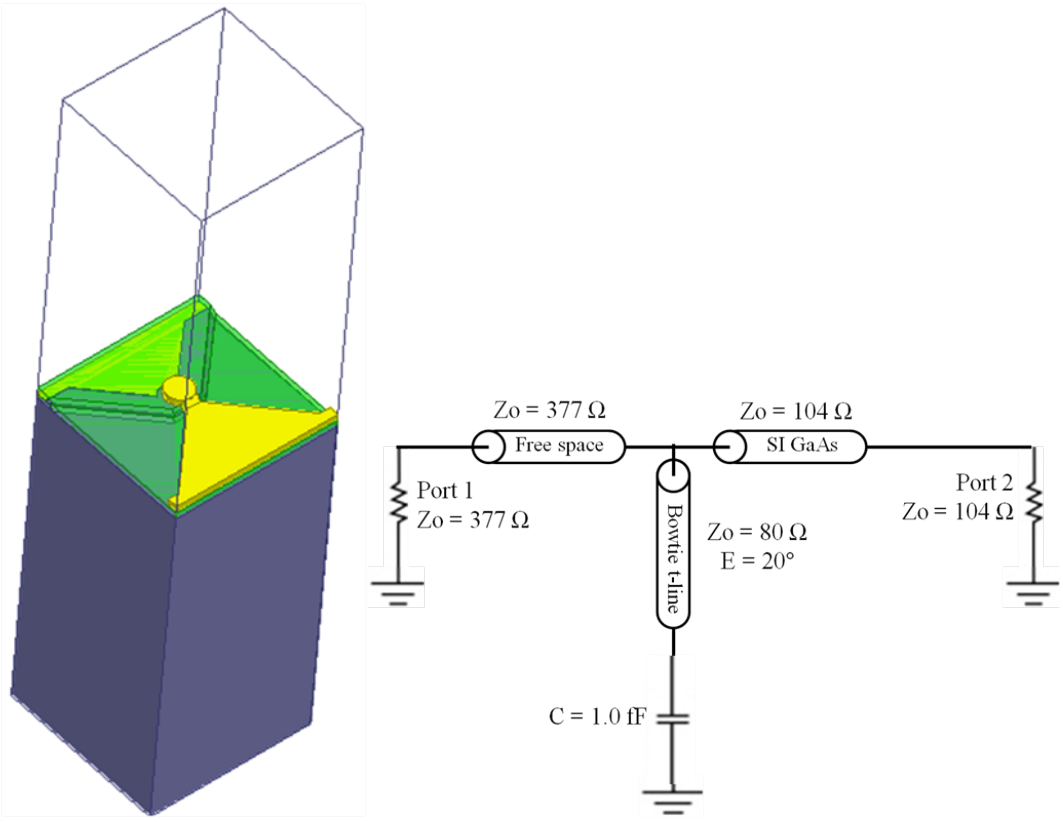


Figure 3.13: HFSS model of a more realistic bowtie design and accompanying lumped element model

Figure 3.13 also shows the circuit diagram which corresponds with the HFSS model. The primary difference, electrically, from the previous circuit of Figure 3.12 is that the bowtie is now capacitively coupled to ground and not physically shorted. The electrical characteristics of the bowtie transmission line are the same, and the value for the parasitic capacitance, C_P, is determined to be approximately 1fF. This parasitic capacitance seems small, but from the ideal sideband generator simulations, the variable capacitance is modulated between 1-3fF. Considering the para-

sitic and diode capacitance are of the same order, the shunting capacitance is significant and can detrimentally affect the overall operation of the sideband generator. However, with the addition of the shunt tuning elements, the effects of C_P can be mitigated and its influence on the circuit minimized.

Once the values for the bowtie transmission line and parasitic shunting capacitance are found, a virtually shorted tuning element is added in parallel with the diode and C_P. The tuning element is a microstrip transmission line with the ohmic contact of the diode serving as the ground plane. The microstrip line is terminated in a virtual short circuit since it extends to the end of the unit cell. Given the array geometric parameters, the microstrip line impedance is ~51Ω with an effective dielectric constant of approximately 3. Also, the added microstrip line reduces the finger to pad capacitance, mitigating its effect on the circuit. This occurs due to a number of factors. The primary factor is the highly conductive GaAs mesa. Because the tuning line begins immediately at the anode contact, a significant portion of the fringing fields formerly associated with C_P are now associated with the distributed capacitance of the microstrip transmission line. This is beneficial to the overall sideband generator operation because it decreases the effects the parasitic C_P had on the circuit performance. Figure 3.14 shows the final HFSS design and its corresponding circuit model.

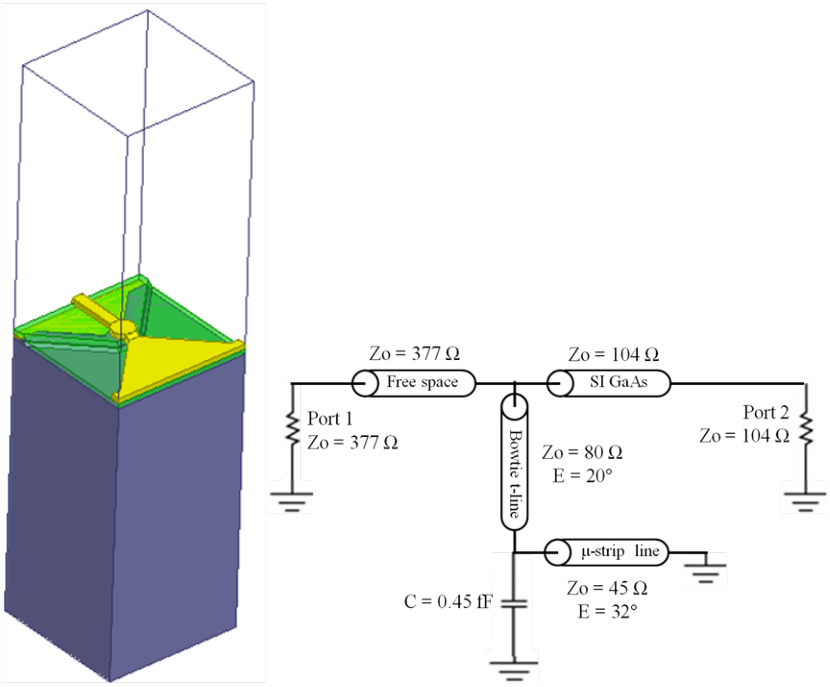


Figure 3.14: HFSS model for the unit cell with accompanying circuit model

Figure 3.15 shows the agreement between the HFSS and ADS model over a frequency range of 1.55THz to 1.65THz. The simulations match quite well over the band showing the validity of the unit cell model to represent the geometric structure seen in Figure 3.14. The values determined by these simulations are not the values used in the final design. For now they simply represent the passive network of an un-optimized HFSS model. At the moment the bowtie angle, length, tuning stub width, and metal thickness were chosen to fit the 25 μm^2 unit cell and leave a 3 μm misalignment tolerance for fabrication. This gives a starting point at which the unit cell can be modified to present the optimum embedding impedance solved for during the ideal sideband generator simulation. Once a model for the Schottky diode is created, the ADS circuit is tuned to present the optimum impedance. When the optimum values for the bowtie transmission line and added tuning element are determined, the HFSS model is modified to create the final optimized design. This is possible because changes in the HFSS model do not directly affect the intrinsic Schottky diode circuit model as HFSS is a linear full wave simulator and does not include the

voltage or field dependencies of a metal to semiconductor contact.

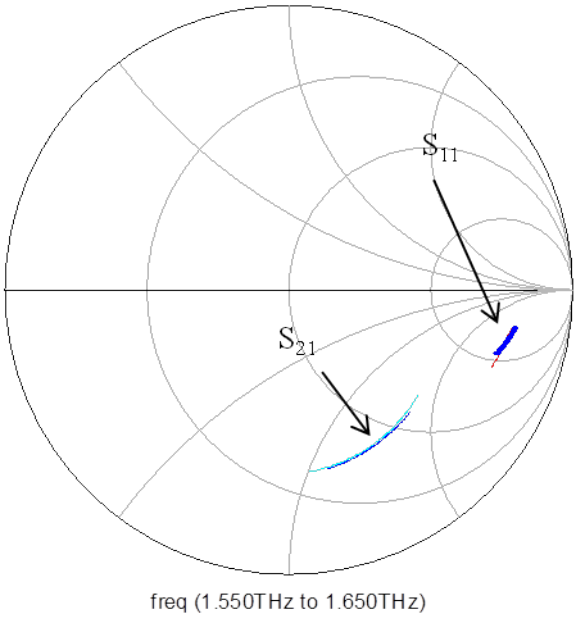


Figure 3.15: A plot comparing the ADS circuit model and the HFSS full wave results from Figure 3.14

3.4.3 Schottky Diode Characterization

The results from the initial simulations, called for a variable capacitor which could vary from 1-3 fF. To create such a device the proper Schottky contact must be designed to realize the necessary capacitance. There are many parameters which can be adjusted when designing a Schottky contact to achieve the desired contact.

When designing a Schottky contact for varactor operation the most important consideration is the non-liner CV relationship. Recalling equations 2.4 and 2.5 the parameters which can be adjusted to vary the capacitance-voltage relationship are the substrate doping N_d, built-in voltage V_{bi}, and Schottky contact area. In this case the metal forming the Schottky contact will be titanium, setting the built-in voltage to 0.68V. Given this built-in voltage, to create a Schottky contact capable of varying its capacitance from 1 to 3 fF, a doping concentration of $N_d = 4.5 * 10^{17}$ and a anode diameter of 1.2 μm is chosen. Table 3.1 plots the CV relationship for a Schottky contact under

these conditions.

Bias voltage (V)	Depletion width (nm)	Junction capacitance (fF)
0.3	33.6	3.87
0.0	45.62	2.85
-2.0	92.1	1.41
-4.0	121.9	1.01

Table 3.1: The depletion width and junction capacitance at varying bias voltages

The series resistance of the Schottky contact has a major influence on the conversion loss of the sideband generator. To properly design tuning element capable with resonating with the diode it is necessary to predict the series resistance as well as the junction capacitance. Using the substrate doping, anode radius, electron mobility, and the diameter of the ohmic contact (9μm), the series resistance for the Schottky contact was estimated; $Z_{epi} = 5.0 + j38.4\Omega$, $Z_{spread} = 6.4 + j1.6\Omega$, and $Z_C = 7.1\Omega$. Adding the three resistances together represents the total series resistance of each diode, $Z_{tot} = 18.5 + j40.0\Omega$.

3.4.4 Unit Cell Optimization for Side-Band Generation

Initial simulations show that optimized unit cells can be designed such that the reflection varies over 180° at the different diode bias points given a lossless device. Figure 3.16 shows the circuit model that represents the sideband generator within a typical measurement setup. The circuit contains a bowtie transmission line, added short circuited tuning stub, and planar varactor diode model. The simulation was done at a fixed frequency of 1.6THz, and the bias voltage on the planar diode was swept from -4V to 0.3V at varying pump frequencies.

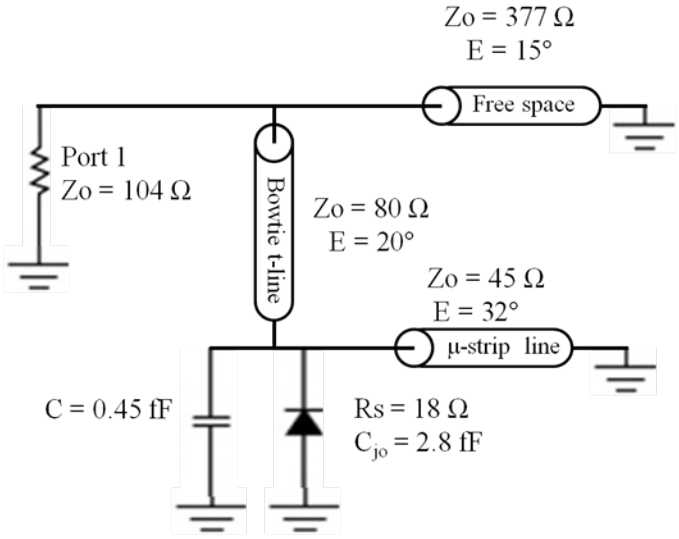


Figure 3.16: Simulation setup to predict the conversion loss

To optimize the unit cell for SBG operation, the goal is to create the largest phase shift between the two bias points. The characteristic impedance, length of the shunt tuning element, bowtie angle, and backshort delay are adjusted to achieve a maximum phase shift from the circuit in Figure 3.16. Figure 3.17 plots the reflection of the optimized circuit as a function of bias voltage. The results show the reflection coefficient varying more than 180 degrees with added loss due to the diode series resistance.

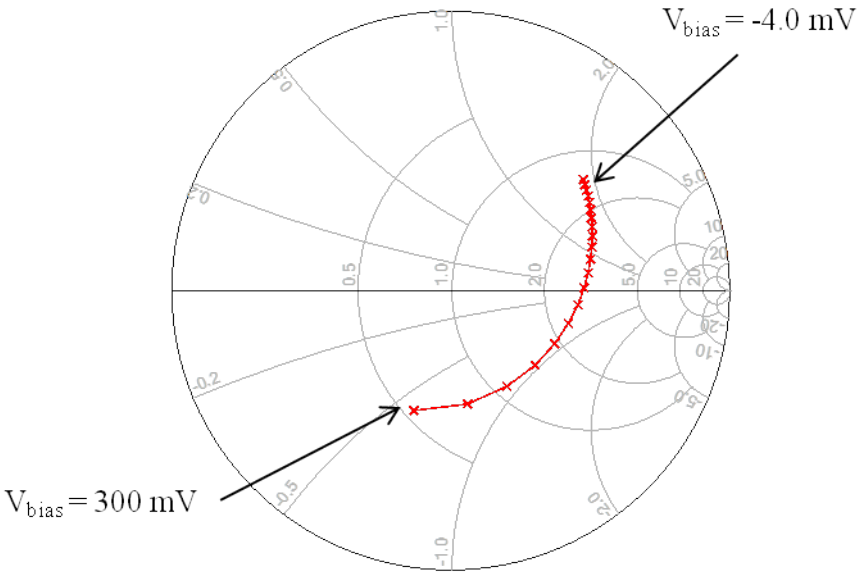


Figure 3.17: Simulation results showing the reflection coefficient of the quasi-optical setup at various bias voltages

To see the utility of the added tuning element a comparison is made between the previously simulated results and a similar circuit design without the tuning element. Figure 3.18 shows the model used to represent the circuit without the added tuning element. In order to make an effective comparison the diode and surrounding parasitic model are identical to the circuit in Figure 3.16. However, in order to minimize the conversion loss for the circuit 3.18, the length of the back short is adjusted to create a maximum phase shift between the two bias points. Figure 3.19 shows a plot of the reflection as a function of bias for the circuit without the added tuning element. From the results the circuit without the tuning element only yields a maximum phase shift of 34 degrees. This simulations shows, for this particular circuit topology, the addition of the tuning element in parallel with the diode can increase the overall phase shift of a single diode. This increase in the phase shift will ultimately result in a lower conversion loss. The next section will show a direct comparison of the non-linear simulation results between the tuned and untuned circuit's conversion loss.

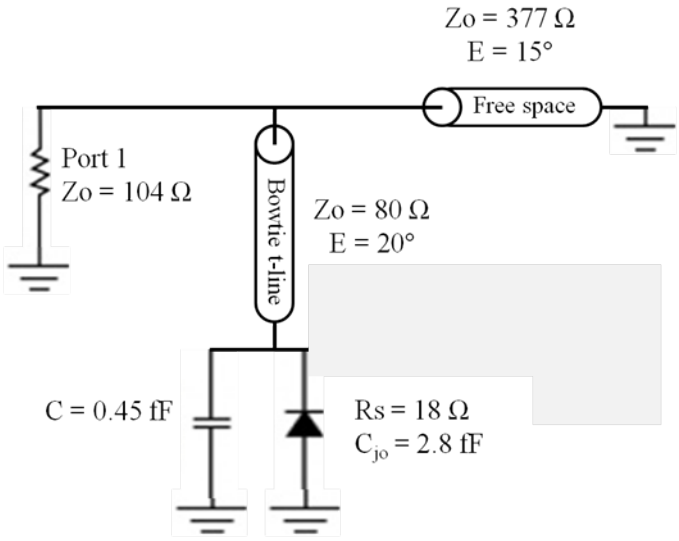


Figure 3.18: Simulation setup to predict the conversion loss without the added tuning element.

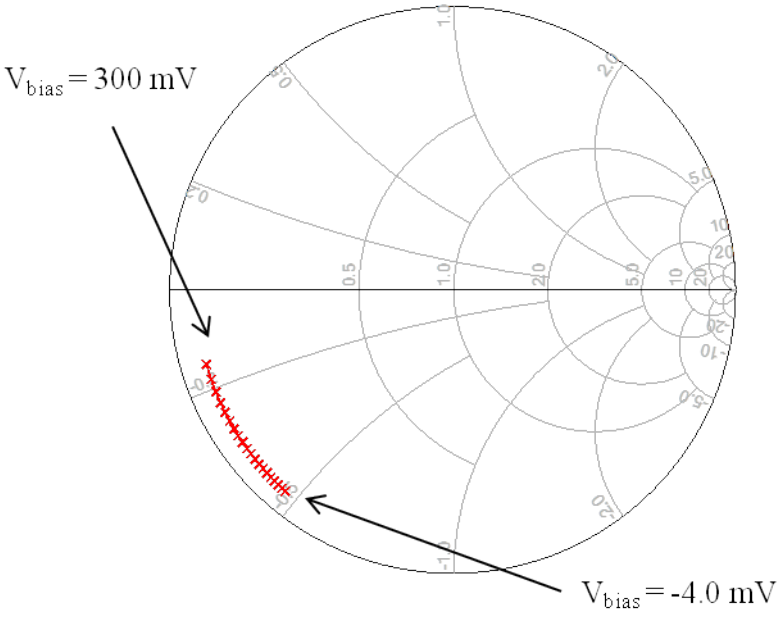


Figure 3.19: Simulation results showing the reflection coefficient of the quasi-optical setup at various bias voltages without the additional tuning element

3.4.5 Non-Linear Simulations and Results

To fully evaluate the circuit performance of the designed sideband generator, a harmonic balance simulation is developed with Agilent's Advanced Design System using the circuit in Figure 3.20. For the simulation, the Schottky diode model is pumped by a sinusoidal source to modulate the diode bias between 0.3 and -4.0V. All harmonics terminated in a 377 Ohm load, mimicking the quasi-optical setup. The model predicts a conversion loss of 8.2 dB.

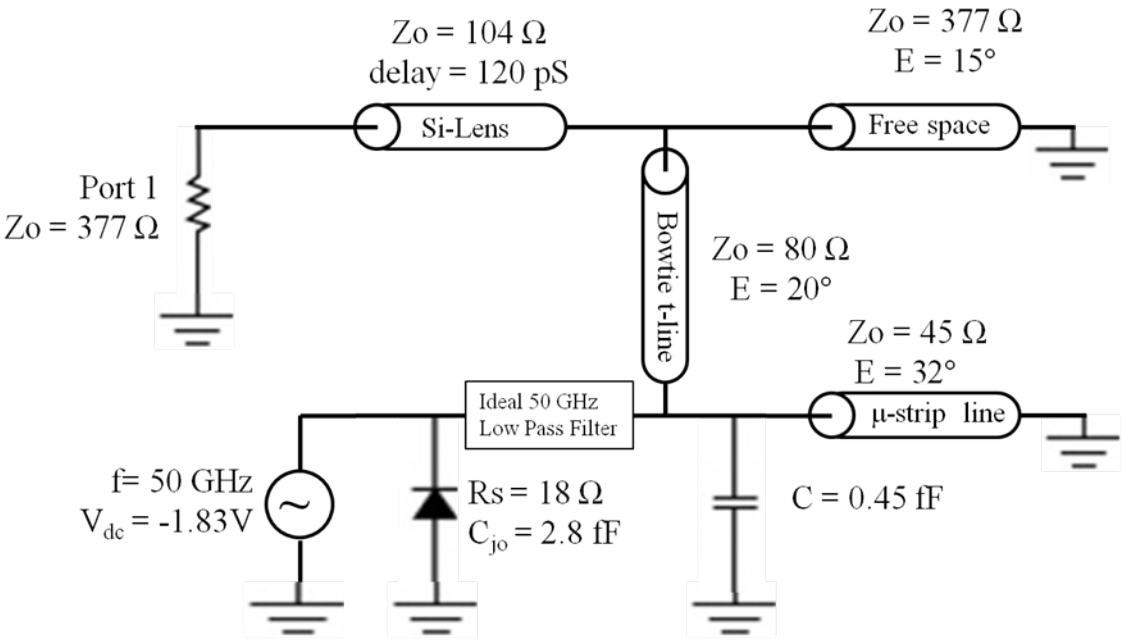


Figure 3.20: ADS Harmonic balance design used to predict the conversion loss of the SBG circuit

To confirm these results, a conversion matrix describing the device is created using the admittance waveform of the pumped device. The matrix is used to predict the currents at each harmonic, given a specific input frequency. The results from the conversion matrix are used to calculate the conversion loss at various harmonic. Each harmonic is terminated the same 377 Ohm a load. The conversion matrix predicts a conversion loss of 7.4 dB from the fundamental 1.6THz to first lower sideband.

It is important to make a comparison between how the circuit performs with and without the

addition of the tuning element in parallel with the diode. In the previous section the results of the phase shift between the two circuits are compared. In this section the same is done with the non-linear harmonic balance simulations. The circuit model in Figure 3.18 is used in the same harmonic balance setup seen in Figure 3.20. This circuit predicts the conversion loss of a unit cell without the added tuning element. From these results, the expected conversion loss for a unit cell without the tuning element is 24 dB. Both this result and the results from the previous section show an improvement in performance of the device with the addition of the added tuning element.

In addition to estimating the conversion loss, another important use for the circuit in 3.20 is to characterize the bandwidth of the circuit. The goal is to create a device that can operate up to 50 GHz. To understand how the pump frequency affects the output of the sideband generator, Figure 3.21 shows the simulated efficiency versus pump frequency. The peak efficiency is at the center of the band (41%) and gives an average of 12% efficiency across the 1-50 GHz range. However, there are several frequencies where the efficiency approaches zero because no pump power is delivered to the diode. This occurs at specific frequencies when the impedance mismatch between the 50Ω generator and diode results in a voltage null.

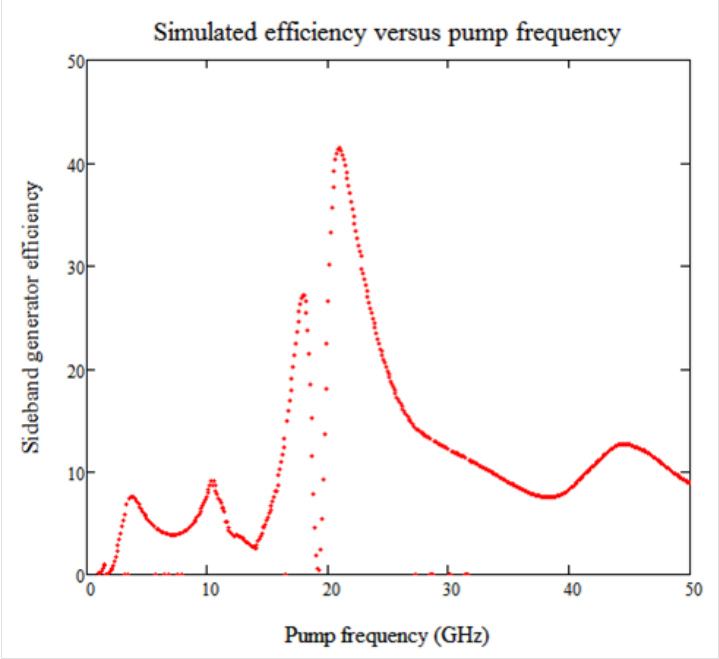


Figure 3.21: Simulated efficiency versus pump frequency

Chapter 4

Schottky Diode Sideband Generator Array Fabrication

4.1 Overview

In this chapter the details of the sideband generator array fabrication process are described. The substrate chosen for this project is a 600 μm thick semi-insulating GaAs substrate with two layers epitaxially grown on the surface. The first is a highly doped "buffer" layer of n-type GaAs, $N_d = 5 * 10^{18} cm^{-3}$, which is used to create an ohmic contact. This layer is kept thin, 500 nm, to simplify the subsequent processing steps. The second epitaxial layer, the modulation layer, is a lower doped n-type GaAs layer, $N_d = 4.5 * 10^{17} cm^{-3}$, which is used to form the Schottky contact. The doping level was chosen to create the diode characteristics and parameters required for the sideband generator based on the design in chapter 3. The thickness of the modulation layer is 120 nm which is larger than the maximum depletion width at -4V of ~100nm. Figure 4.1 shows an illustration of the substrate and the epilayers used for this project.

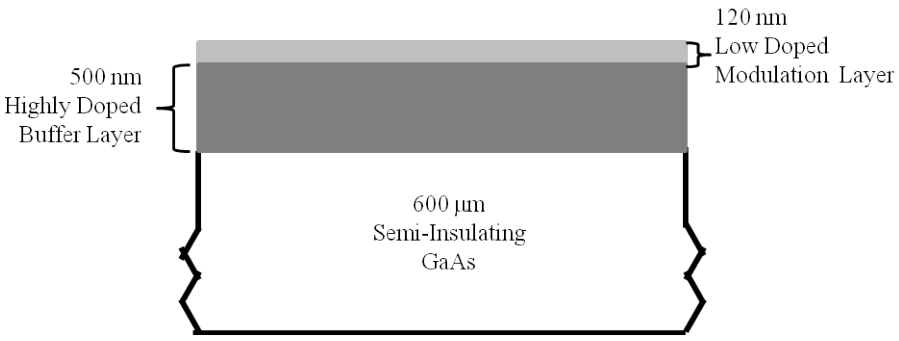


Figure 4.1: Layout of the substrate and epitaxial layers used to fabricate the 1.6 THz sideband generator

Fabrication of the 1.6 THz sideband generator array consists of five basic steps, each with unique processing techniques required to create the final array. The first step is to form the ohmic contacts to the highly doped GaAs buffer layer. A combination of wet and dry etches are used to reveal the highly doped layer. After etching, an ohmic contact metallurgy of Au/Ge-Ni-Au is evaporated onto the exposed epilayer. A rapid thermal anneal (400º C for 60 seconds), RTA, alloys the metal contact creating an ohmic contact.

The second processing step is used to create GaAs mesas, which are the isolated areas where the Schottky and ohmic contacts are formed. A wet etch is used to allow step coverage along the mesa's edge because the etch's isotropic nature creates sloped sidewalls. After the mesas are etched, the substrate is placed into a Plasma-Enhanced Chemical Vapor Deposition (PECVD) chamber to deposit an insulating layer of SiO_2 on the surface.

The third processing step is used to determine the thickness of the SiO_2 film deposited and to etch via holes through the insulating layer. Because precise etch timing is required to accurately define the small anode openings, this mask is useful for determining the exact thickness of the SiO_2 at various regions of the GaAs die. The etch also reveals the cathode contacts common to all the elements in the array. The areas etched during this step are large ($>100\ \mu m^2$) so a wet etch is used.

The fourth processing step defines the anodes for the Schottky diodes. A tri-layer lithography technique is adopted to achieve the small anode dimensions, $<$ 1.2µm diameter. Initially a 2 µm thick polymer, PMMA, is used as a sacrificial layer and helps to planarize the surface. Then a thin

layer of chromium (330 A) is sputtered atop the PMMA surface, followed by a thin photoresist layer, AZ5206, to pattern the anodes. A sequence of dry etches are used to etch the pattern into the chrome, PMMA, and ultimately the SiO_2. However, before the dry etch reaches the SiO_2 GaAs interface (roughly 50 nm remaining) a wet etch is used to remove the final amount of SiO_2 to protect the GaAs surface from the energetic ions of the dry etch.

The final step in the process creates the Schottky contacts, bowtie antennas, and metal interconnects. A seed layer of Ti-Au is deposited over the entire substrate. A fifth mask is used to define the areas which are electroplated onto the seed layer. Roughly 1 μm of gold is electroplated. Afterwards, the resist is removed and the seed layer is wet etched away. Each GaAs die is 17x17 mm and contains 26 arrays. A dicing saw is used to separate each die containing a sideband generator array. The final metal pattern also prints marks to align the dicing saw to ensure each die is symmetric.

4.2 Ohmic Contact Formation

To form the ohmic contacts, the top modulation layer of GaAs must be etch away to reveal the highly doped buffer layer underneath. To accomplish this, a wet etch is first performed to undercut the photoresist slightly. This small undercut will help with the subsequent lift-off process used to deposit the ohmic contact metal stack up. After the wet etch, the majority of the GaAs is etched in a reactive ion etcher, to maintain planarity after the metal deposition.

Once etched, the ohmic contact metal stack up is evaporated over the sample and the excess lifted off. There are a number of metal contacts and annealing times which can be used to create an ohmic contact to GaAs. However, for this work, the well-known Au/Ge-Ni-Au (500Å-250Å-1000Å) stack up is used. Once all the excess metal and resist are removed the sample is annealed. Figure 4.2 shows an SEM image of a finished SBG unit cell and the cut line that will serve as a reference in the fabrication process images to follow.

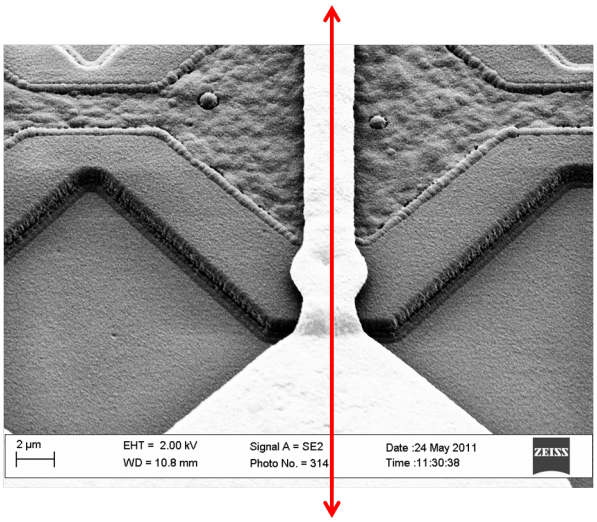


Figure 4.2: SEM image of a SBG unit cell illustrating the cut that will be used to display the ohmic contact process flow

4.2.1 Gallium-Arsenide Ohmic Contact Etch

To reach the highly doped buffer layer a two step etch process is used. The aim is to produce a trench that is the same thickness of the metal to be deposited, a total of roughly 175 nm. The etch depth is important because this surface also serves as the ground plane for the tuning microstrip transmission line. Thus, it must be as planar as possible to insure step coverage while electroplating the transmission line tuning element. Figure 4.3 shows an illustration of the process steps used to create the ohmic contact, referring to the cut line seen in Figure 4.2.

Photoresist (AZ4110 @4000 RPM 30 sec) is patterned with the first mask set to protect the desired areas, Figure 4.3a. A short wet etch is done to aid in the subsequent lift off process. A (1:1:25) ($H_2O_2(30\%) : H_3PO_4(85\%) : DI$) etchant is chosen for this etch because it is very isotropic and insensitive to crystallographic directions. As a result the etch provides a 45˚ slope at each side wall along the ohmic contact edge due to resist undercut. Using a (1:1:25) concentration, an average etch rate of $150\frac{nm}{min}$ is recorded. For the purpose of aiding in lift off, only a 20 sec etch is done to undercut the resist by ~50 nm. The result of this etch can be seen in Figure 4.3b.

The next step is to perform a dry etch to create a trench 175 nm deep. The trench is etched deep enough so the entire ohmic metal stack will rest within, maintaining planarity. A low power BCl_3 dry etch is used to create a trench about ~175 nm deep with vertical side walls. The etch was done at a pressure of 10 mTorr, a power of 20 W, and a BCl_3 flow rate of 20 SCCM. This recipe yields an etch rate of about $100\frac{nm}{min}$ and the etch takes approximately 1.75 minutes. Figure 4.3c shows the unit cell after the RIE is complete.

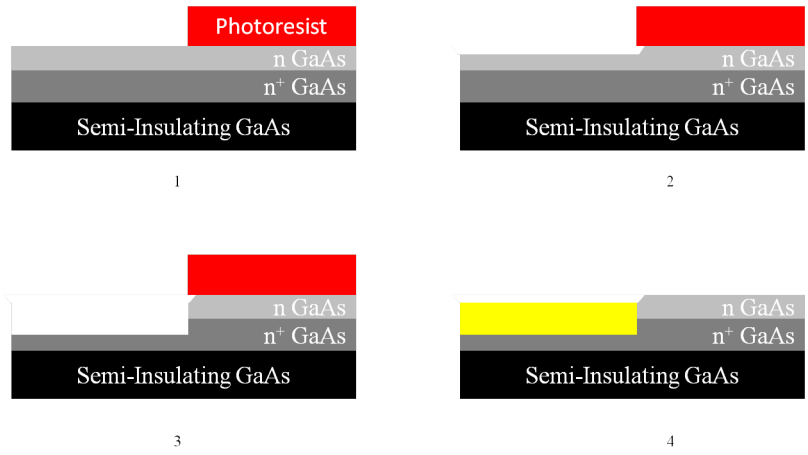


Figure 4.3: Illustration of the ohmic contact formation process flow

4.2.2 Au/Ge-Ni-Au Ohmic Contact Metallization and Annealing

The next step in creating the ohmic contact is to evaporate the correct metal stack-up which is alloyed to form an ohmic contact to the GaAs. As mentioned before there are many different metallurgies which can be used to create ohmic contacts to GaAs. However, for this work the well-understood Au/Ge-Ni-Au metal stack up is used. One of the main reasons for choosing this metallurgy is that the Au/Ge contact has been characterized using existing equipment in the UVa MFL. A mask was created to fabricate many different ohmic contact TLM (transmission line model) structures which were used to characterized the contact resistance after undergoing various annealing conditions. Different time and temperatures were studied and an optimum condition was found, 400°C for 60 sec. Every array fabricated received the same metal evaporation, Au/Ge-Ni-Au

(500Å-250Å-1000Å).

After the metals are evaporated onto the substrate, the excess metal and photoresist is lifted off. A 120° (1:1) NPM:polypropylene glycol solution is used to dissolve the resist. With the aid of the previous wet etch, the lift off process takes no longer than 20 minutes and requires no scrubbing to remove the resist. Care should be taken since the GaAs surface still exposed is what is used to create the Schottky contacts. Once complete the sample should resemble Figure 4.3d.

Before the RTA is performed , an extensive cleaning is done. This ensures no contamination, photoresist, or debris is left behind before the high temperature thermal anneal. During the high temperature anneal most contaminates on the surface; waxes and photoresist, will permanently adhere. Once clean, the RTA is performed to create an ohmic contact.

4.2.3 Au/Ge-Ni-Au Ohmic Contact formation methodology and mechanisms

This method of creating ohmic contacts to GaAs relies on the material properties of the Au/Ge alloy and the fact Ge is an n-type dopant for GaAs. Figure 4.4 shows the phase diagram for the Au/Ge alloy. The Au/Ge concentration used is at the eutectic composition. This is important because it yields the lowest single phase melting temperate possible for the alloy (~320°C). At temperatures above the melting point the entire Au/Ge bulk will entirely melt into one continuous liquid with no single phase, solid Au or Ge, particles present.

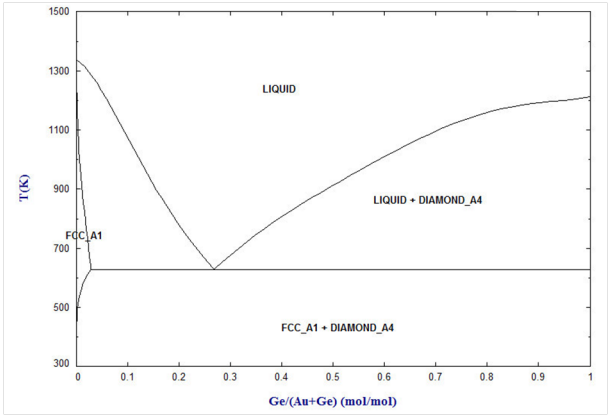


Figure 4.4: Phase Diagram for Au/Ge alloy

During the RTA, as the Au/Ge is in a liquid state, the Ge more easily diffuses into the GaAs. During the 60 second anneal time, sufficient Ge atoms diffuse into the GaAs surface to degenerately dope a very thin layer at the interface of the GaAs. Figure 4.5 shows an illustration of the contact before and after the annealing.

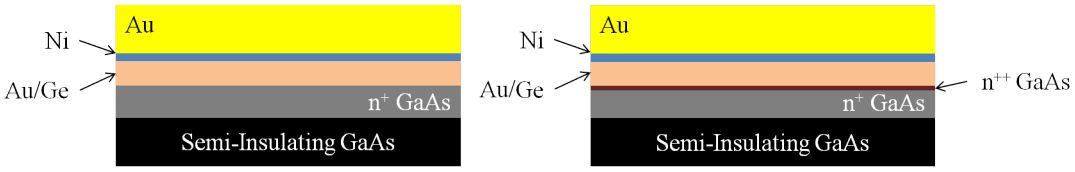


Figure 4.5: Left: Contact before RTA. Right: Contact after RTA

The nickel layer in the stack up plays two important functions. It acts as a wetting agent for the liquid Au/Ge to prevent the liquid from balling up due to surface tension. If the Au/Ge layer balls up or forms single phase regions, the surface of the contact will roughen and result in nonuniform Ge doping across the contact area. The nickel layer also prevents the Ge from diffusing up the metal stack into the top gold layer. This barrier helps increase the diffusion of Ge into the GaAs during the anneal. The top gold contact is used to decrease the contact resistance with the nickel layer and protect it from oxidation. Figure 4.6 shows a microscope image of a 6x6 element array after the ohmic contact formation. The image also highlights a unit cell showing half the bowtie

structure created by the ohmic contact.

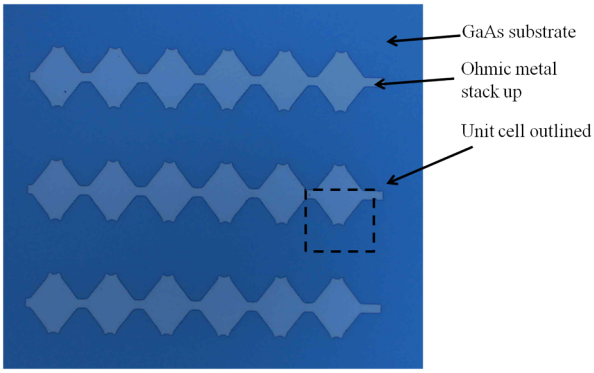


Figure 4.6: A microscope image of a 36 element array after the ohmic contacts have been fabricated

4.2.4 Ohmic contact optimization

Figure 4.7 shows a photograph of the TLM structure. The TLM structure is used to find the optimum annealing conditions for AuGe metallurgy. Figure 4.8 shows a photograph of different GaAs dies, each receiving varying annealing times and temperatures. The TLM test structure consists of metal pads of equal width that are spaced at varying distances. Using a four point probe measurement, the resistance between all the pads is measured and recorded as a function of pad spacing. Measuring the resistance between two pads yields:

$$R_{total} = 2R_C + \frac{R_s}{w}d \tag{4.1}$$

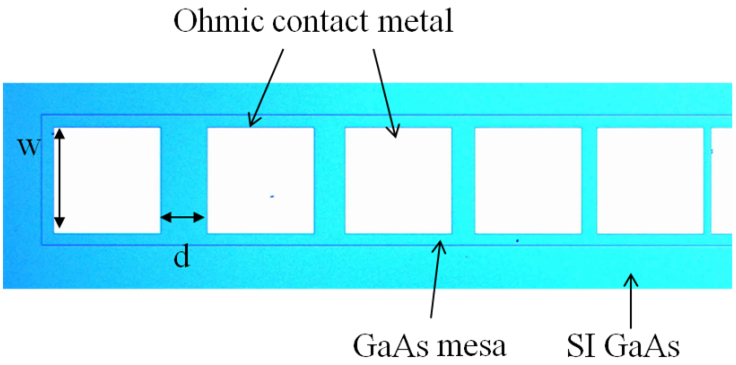


Figure 4.7: A photograph the GaAs ohmic contact test structure

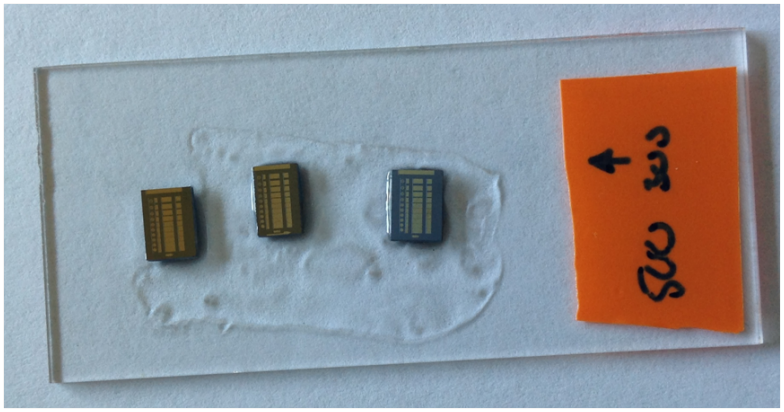


Figure 4.8: A photograph of several GaAs dies which received different annealing times and temperatures

In equation 4.1, R_C represents the resistance associated with the ohmic contact. Since the measurement is done between two pads its value is multiplied by two. R_s is the sheet resistance of the GaAs, w the width of the pads, d the distance between the pads. The function $\frac{R_s}{w}d$ predicts the resistance between the two pads. As different pad spacings are measured, a plot can be created and a line fit to extract the two parameters, R_C and R_s.

Figure 4.9 shows a plot of the measured resistance versus pad spacing for the sample which received an anneal of 400C for 60 seconds. Figure 4.9 also shows the fitted line used to determine the ohmic contact properties. From the line, the contact resistance, R_C, is determined to be 0.585Ω.

The plot in Figure 4.9 also yields another important characteristic of the ohmic contact, the transfer length, L_x. The transfer length represents the length underneath the ohmic contact the current must travel before transferring from the semiconductor to the metal. The transfer length can be determined by solving for the x intercept of the fitted line.

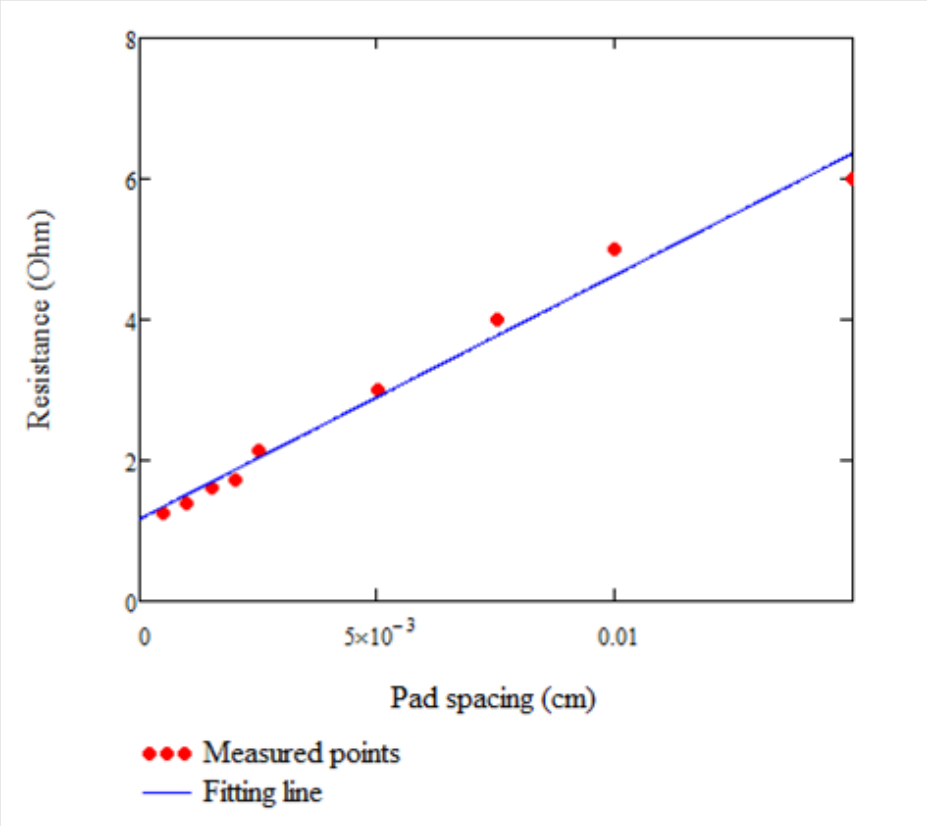


Figure 4.9: Plot of resistance versus pad spacing

However, the figure of merit used to quantify contact resistance is known as specific contact resistance, r_c. To calculate the specific contact resistance the contact resistance R_C, transfer length L_x, and pad width w are used. Equation 4.2 shows the formula used to calculate the specific contact resistance.

$$r_c = \frac{1}{2} R_C w L_x \, \Omega * cm^2 \tag{4.2}$$

To determine the best annealing time and temperature, several different TLM structures were fabricated. Each sample revived a different annealing time and temperature and measurements were done to determine the specific contact resistance of each sample. Figure 4.10 shows a plot of the resulting specific contact resistance as a function of annealing time and temperature. From the results it was determined that 400C for 60 seconds yielded the lowest specific contact resistance and is the annealing conditions used for the entirety of this work.

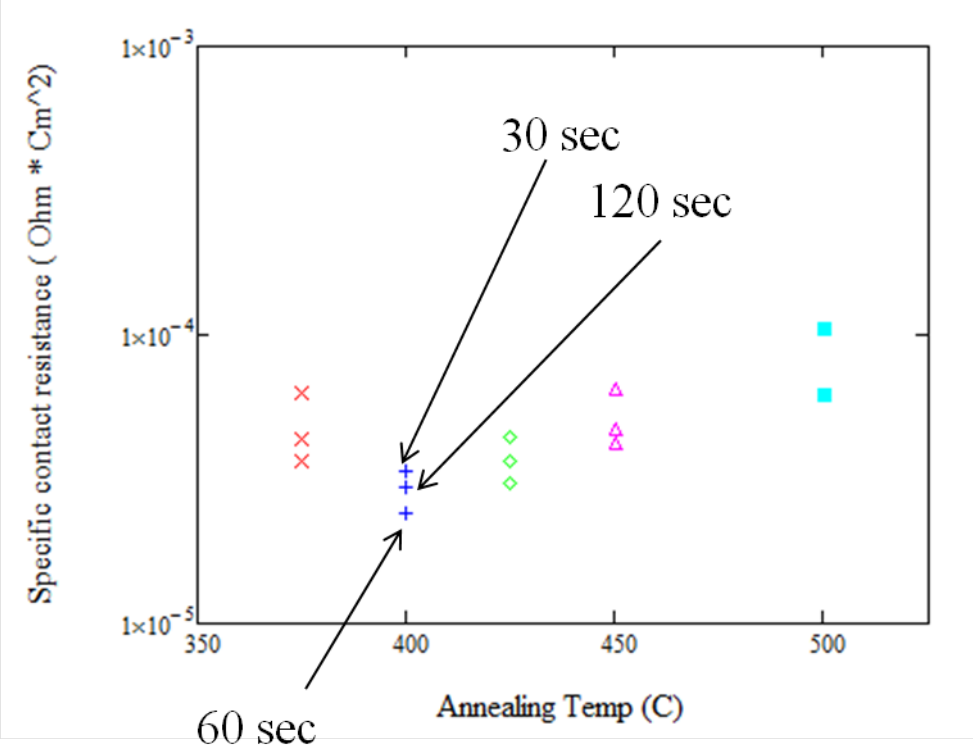


Figure 4.10: A plot of the specific contact resistance versus annealing times and temperatures

4.3 Mesa Etch

The next step in the process is to isolate the device areas by etching away all the undesired epi-layers from GaAs die. The only areas where epi-layers will remain are where the Schottky contacts and n^+GaAs ohmic contact areas. Figure 4.11 shows the two steps necessary to etch the GaAs mesas.

The first step is to pattern photoresist (AZ4110 @4000 RPM 30 sec) with the second mask set. This resist layer serves to protect the areas where the Schottky contact will be made as well as the previously-formed ohmic contacts, Figure 4.11a. To perform the etch, the same (1:1:25) ($H_2O_2(30\%) : H_3PO_4(85\%) : DI$) etchant is used as in the previous ohmic contact formation wet etch. This particular etch was chosen because of its isotropic nature. The etch's isotropy will create side nearly 45^{o} angles walls along all the mesa edges. This is important because the mesa will subsequently be covered by an insulating layer of SiO_2 which supports all the metal bowties and tuning transmission lines.

The goal is to etch down to the semi-insulating substrate, removing the conductive layers from the desired areas. The combined thickness of the two epilayers is 620 nm. To account for variations and uncertainty in the profilometer measurements and epilayer thickness, a target of 700 nm is chosen. The phosphoric based solution averaged about $150\frac{nm}{min}$ which means the 700 nm etch took an average of 4:40 minutes. Figure 4.11b shows the sample just after the etch is complete. Once the die is etched, a four point probe is used to verify the semi-insulating layer is revealed and the photoresist is removed. Figure 4.12 shows a microscope and SEM image of an array after the mesa etch.

Figure 4.11: Illustration of the mesa etching process

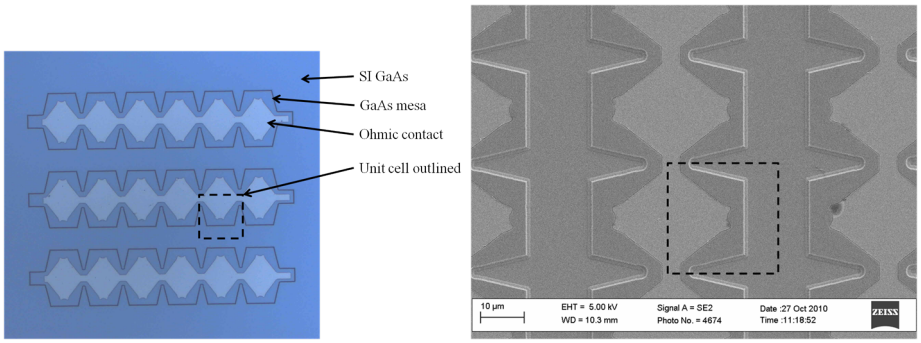


Figure 4.12: Left: Microscope Right: SEM image of a 6x6 element array after the mesa etch.

4.4 Oxide Deposition and Large Area Etch

4.4.1 PECVD

The next step in the process is to deposit an insulating layer of SiO_2. There are a number of ways to deposit an insulating layer on a GaAs substrate; sputtering, evaporation or various form of chemical vapor deposition (CVD). For this work a Plasma Enhanced (PE)CVD is chosen. This is the preferred method for SiO_2 deposition on GaAs because it tends to yield superior film quality, a high deposition rate, and is a low temperature process.

Figure 4.13 shows an illustration of a typical PECVD reactor setup to deposit SiO_2 . The process is done in a low vacuum chamber to eliminate contaminants and to control the pressure during the deposition. Then, much like a typical CVD process, precursor gasses are used to form the final product. However, a PECVD does not solely rely on thermal energy to form the SiO_2 from the precursors. As the name implies an RF generator is used to create a plasma that ionizes the precursors gasses. Figure 4.13 shows the two electrodes within the vacuum chamber. The samples are placed on the grounded platen which is heated. With the precursors ionized by the RF energy, less thermal energy is required to form the SiO_2 on the surface of the sample.

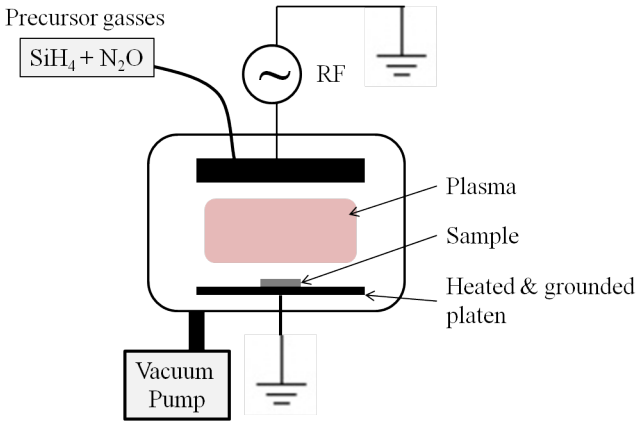


Figure 4.13: An illustration of a PECVD setup to deposit SiO_2

Equation 4.3 shows the desired reaction to transform the precursor gasses, silane and nitrous oxide, into SiO_2. During the deposition, the silane has a flow rate of 108 SCCM and the nitrous oxide 480 SCCM. The chamber pressure is held constant at 800 mTorr. The RF power is 80 W and the platen is heated to 250°C. Under these conditions a SiO_2 film is deposited at $\sim 10\frac{nm}{min}$. The target is to grow 1μm which requires approximately 100 minutes. However, measuring the thickness over an area of $17mm^2$ yields a standard deviation in thickness of 100nm (10%).

$$SiH_4 + 2N_2O \rightarrow SiO_2 + 2N_2 + 2H_2 \tag{4.3}$$

4.4.2 Large area SiO_2 Etch

A third masking step is employed to etch large holes though the SiO_2 to determine the thickness at various locations on the sample. Figure 4.14 shows a diagram of areas that are etched on the GaAs die. Because the holes are not near any critical areas, Buffered Oxide Etchant (BOE) is used to etch through the SiO_2 layer. The etch rate for the PECVD SiO_2 in BOE is roughly $200\frac{nm}{min}$. It takes an average of 5 minutes to etch through the SiO_2 and reach the GaAs surface. Once etched, the depth of each hole is measured and recorded to find the average SiO_2 thickness of each sample. For a sample size of 25 separate depositions, the average SiO_2 thickness is about $1.075\mu m$ with a

standard deviation of 0.142 μm.

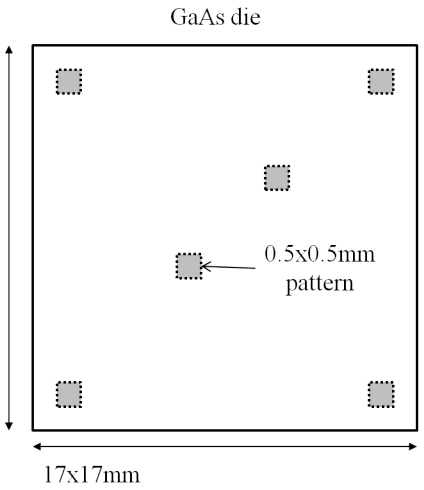


Figure 4.14: A diagram showing the large areas of $SiO_2$to be etched

4.5 Anode Etch

The fourth mask set is designed to carefully etch through the SiO_2 layer and reveal the Schottky contact. To accomplish this, a combination of dry and wet etch techniques are used. First a dry etch is used to remove 950 nm of the 1000 nm of the SiO_2 layer. Using a dry etch ensures an anisotropic etch that keeps the dimensions of the anode the same as the pattern on the mask. 50 nm of SiO_2 is left to prevent the bombarding ions in the dry etch from damaging the GaAs surface and possibly degrading the Schottky diode performance. The final 50 nm is wet etched away using BOE to cleanly reveal the GaAs surface. However, care must be taken as to not over etch the anodes and significantly alter their diameter.

4.5.1 Tri-Layer Process

To accurately define the small 1.0 μm diameter anodes a very thin resist must be used ($< 1\ \mu m$). However, the dry etch used to etch SiO_2 also etches resist with a selectivity of 4:1. Since the SiO_2 layer is a micron thick, a long etch time is required. A more robust method of patterning is used.

A tri-layer lithography process technique is adopted to better define the anode pattern. Figure 4.15 shows the three layers that form the stack up. The first layer is a 2 μm thick Poly(methyl methacrylate) (PMMA) layer. PMMA is an organic based electron beam resist which helps to planarize the surface and reduce the effect the mesas will have on the anode definition. The second layer is a 33 nm thick chromium layer which will ultimately be used to mask the SiO_2 RIE. The final layer is a thin (AZ5206 @ 500 nm) photoresist film which will be used to define the anode pattern into the chromium masking layer.

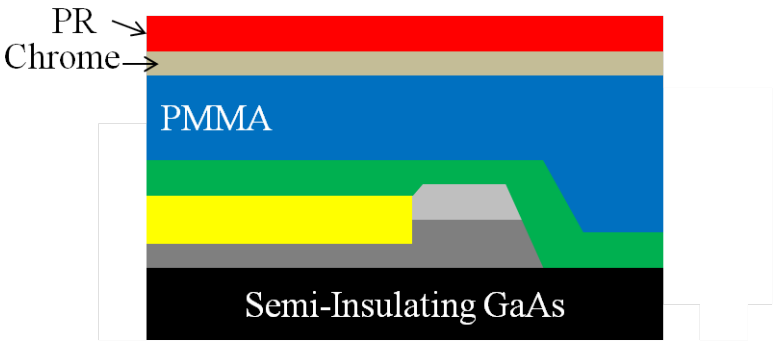


Figure 4.15: Illustration of the tri-layer stack up used

Figure 4.16 shows the steps involved in defining the anodes. After applying the three layers, the process begins by patterning the top most photoresist and revealing the anode areas, Figure 4.16a. Subsequent RIE etches are performed to etch the chromium, PMMA, and SiO_2, Figure 4.16b. The chromium RIE is a Cl_2 based etch which has very good selectivity to photoresist. The next step uses an O_2 RIE to etch the PMMA. The O_2 RIE will etch through the topmost layer of resist leaving only the chrome and PMMA. The chrome layer is then used as the mask and the SiO_2 RIE (CHF_3 = 50SCCM, RF = 80W, P = 10 mTorr) is performed leaving ~50nm of SiO_2 as to not damage the GaAs. A short wet etch (~20 sec) using BOE removes the final 50 nm of SiO_2 and reveal the GaAs surface, Figure 4.16c. With the etching complete the remaining PMMA and chromium is stripped off. Using the same lift-off solution as in the ohmic contact formation the tri-layer is removed, Figure 4.16d.

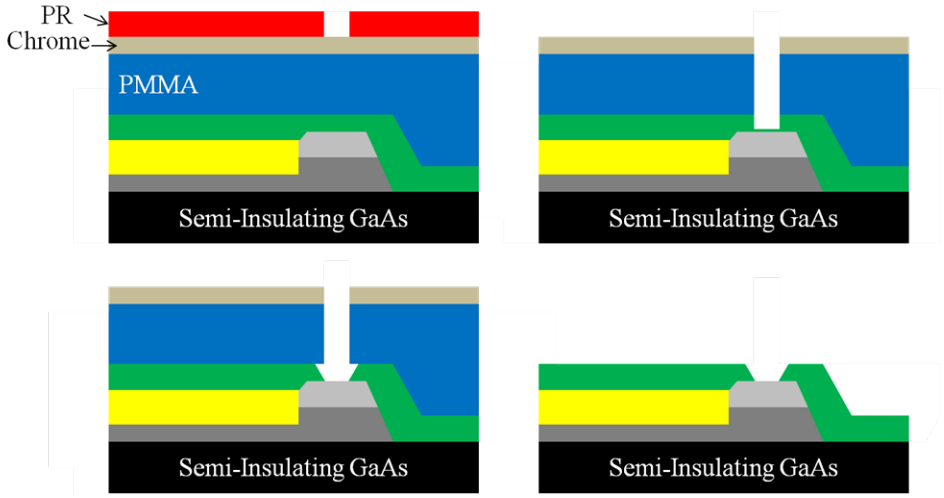


Figure 4.16: An illustration of the process used to etch through the tri-layer and SiO_2

Figure 4.17 is an SEM image showing the etched SiO_2 with the PMMA and chrome masking layer before lift-off. Figure 4.18 shows how the surface of the chrome masking layer looks before the tri-layer lift-off. Figure 4.18 also shows an etched anode after the tri-layer lift-off atop a GaAs mesa.

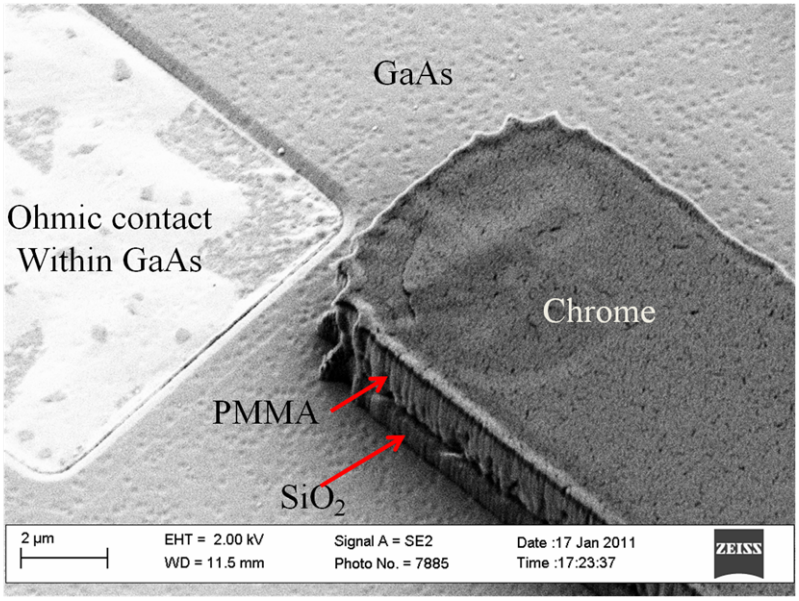


Figure 4.17: SEM image of the tri-layer stack up after all the etch steps

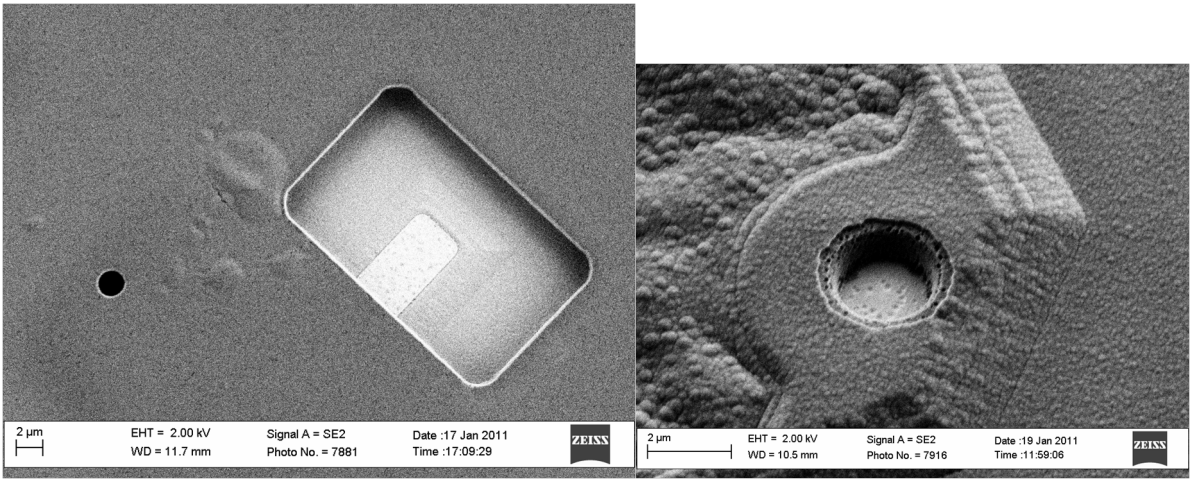


Figure 4.18: Left: SEM image of an anode and ohmic contact connection after the etches but before the tri-layer lift off. Right: A close up of an anode and mesa step after the tri-layer lift off.

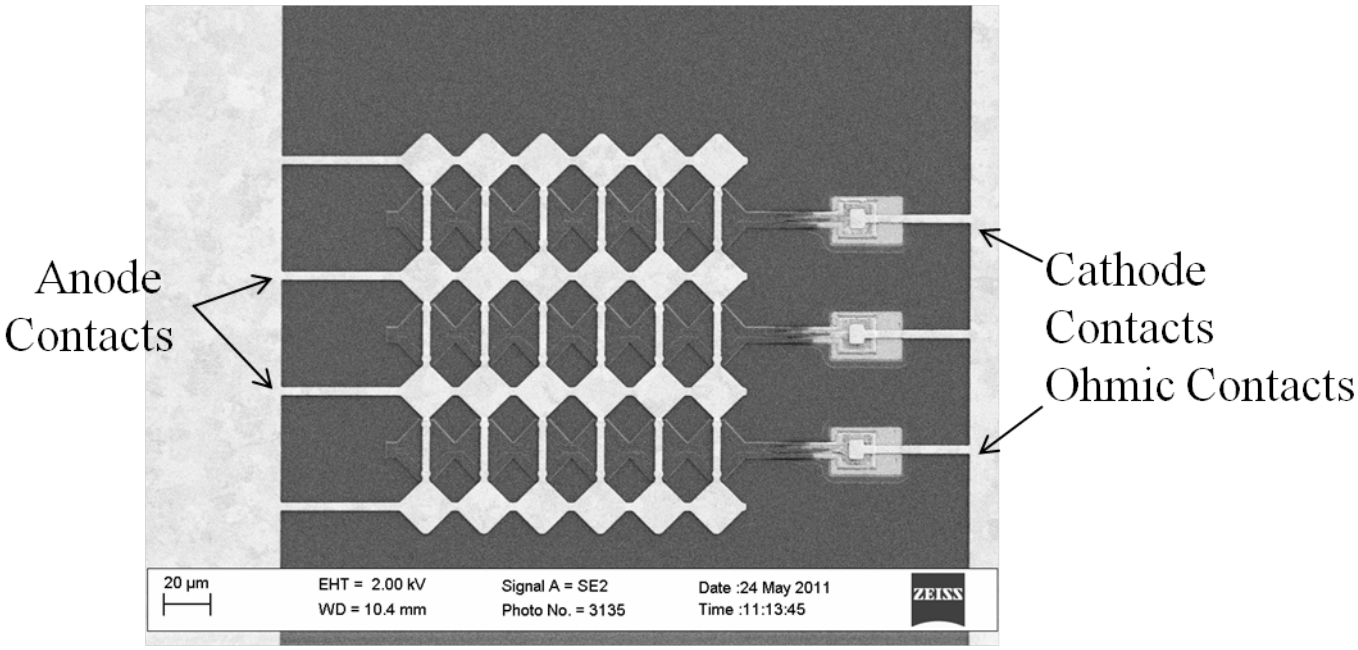
4.5.2 A Note on Etch Rate Lag Within Small Features

It should be noted that when performing a dry etch on areas $<1\ \mu m^2$ the etch rate lags compared to larger areas. After some study, it was determined that the anodes experienced between 10-15% etch rate lag compared to the larger $100\,\mu m^2$ measurement areas. Consequently, it was necessary to add 15% time to each of the three RIE steps for the anodes to open completely.

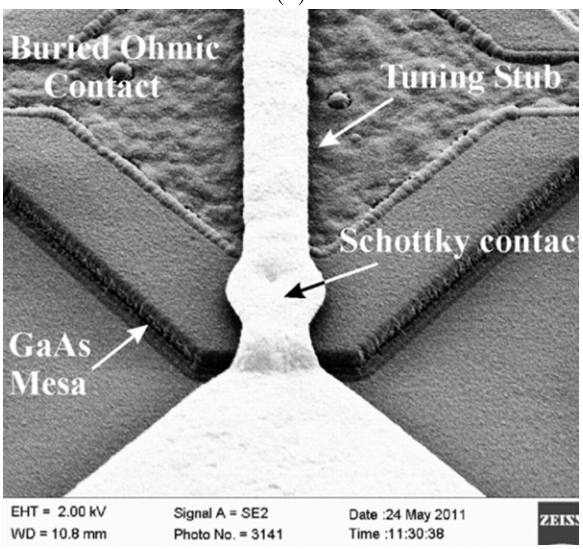
4.6 Final Metallization

The final step in the process is the formation of the Schottky contacts and metal interconnects. For this, a seed layer of titanium (200 A) and gold (1000 A) is deposited over the entire surface. Photoresist (AZ4110 @ 4000 RPM 30 sec) is patterned using a fifth masking layer and the areas which are to be electroplated are revealed. The sample is then placed into a gold electroplating solution and 1μm of gold is plated. The plating was done with a current of 1 to 2 mA and plated about $100\frac{nm}{min}$.

After the plating is completed, the photoresist is removed and the seed layer is etched away. The top layer of gold is removed using HG-400 solution. The 100 nm of gold etched away, on average, in 45 seconds. The 20 nm titanium layer is removed using BOE, taking an average of 20 seconds to etch. Figure 4.19 shows some SEM images of a finished array.



(a)



(b)

Figure 4.19: a: SEM image of a completed 6x6 array b: SEM of a completed unit cell

Chapter 5

Sideband Generator Array Characterization

5.1 Overview of measurements

To characterize the sideband generator array a number of different measurements are performed. These measurements are aimed at determining the s-parameters, conversion loss, and power handling of the array and its equivalent unit cell. The results are also used to make a comparison between the HFSS models, equivalent circuit designs, and Schottky diode characteristics.

The initial measurements are DC current-voltage measurements. Measurements are done on individual diodes as well as the full array. This is important as many of the parameters which govern the array operation depend directly on the intrinsic diode parameters, including reverse saturation current, ideality factor, and series resistance. These results also provide a measure of the number of the diodes within the array that are operational. On the same GaAs die which the arrays are fabricated, several single Schottky diode devices are also fabricated. These individual diodes allow for direct characterization of diodes which are fabricated along with the array.

Following DC characterization, the responsivity of the array as a detector is measured at 1.6 THz.

This measurement demonstrates that the Schottky diodes respond to radiation at 1.6 THz. The measurement also allows the optics of the measurement system to be optimized and an assessment of the power handling of the array. Various bias voltages and back short positions are tested and the results allowed a comparison to the responsivity of similar single-diode Schottky diode detectors.

Following the responsivity measurements, the performance of the array as a phase shifter is measured. Because direct measurements with a vector-network analyzer are not yet possible at 1.6 THz, an interferometric technique is used to determine the phase shift and standing wave ratio as a function of bias voltage. This measurement technique can determine the phase difference of the array's reflection coefficient between two operating points. This result is also compared to the unit cell equivalent circuit models in ADS and HFSS. The data helps to verify and update the circuit models. Finally the updated circuit model is used to predicted a conversion loss to determine the performance of the array.

5.2 Current-voltage relationship

To determine the characteristics of a Schottky diode, DC current-voltage measurements are performed. A Keithley 236 source measurement unit is used to provide a bias current while also detecting the voltage drop across the diode. Four micromanipulators are used to perform a four point measurement to accurately measure the series resistance. During the fabrication process, single-device Schottky diodes were fabricated along with the 100 element diode arrays. The aim is to create an identical Schottky contact, not embedded within an array, to be characterized individually. The results provide a means of measuring the number of the diodes in the array that are functioning through a comparison of I-V curves for single devices and the array. Figures 5.1 and 5.2 show SEM images of the Schottky diode test structures fabricated for DC testing. The geometry of the circuit around the diodes differs from the diodes in the array. However, the two sets of diodes have the same anode size and are expected to respond similar at DC.

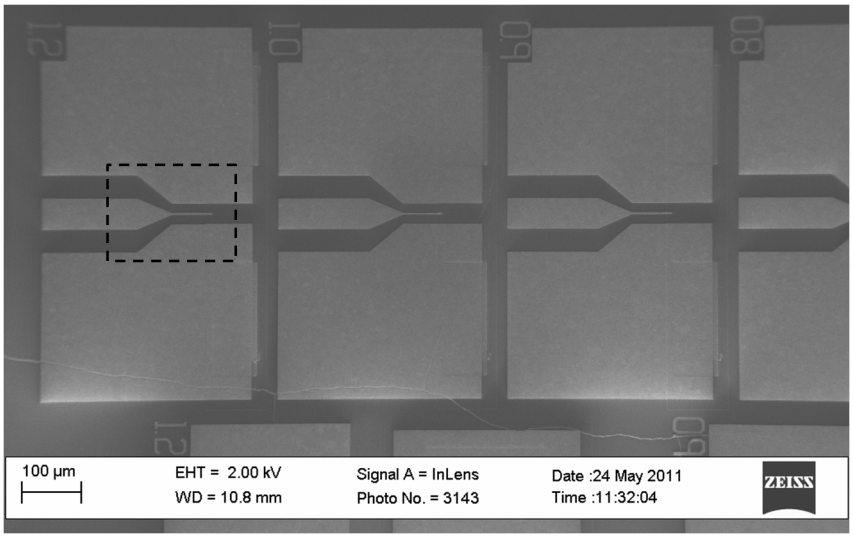


Figure 5.1: A SEM image of the single Schottky diodes intended for DC probing with anodes ranging from 1.2 $\mu m$to 0.8 μmanode diameters.

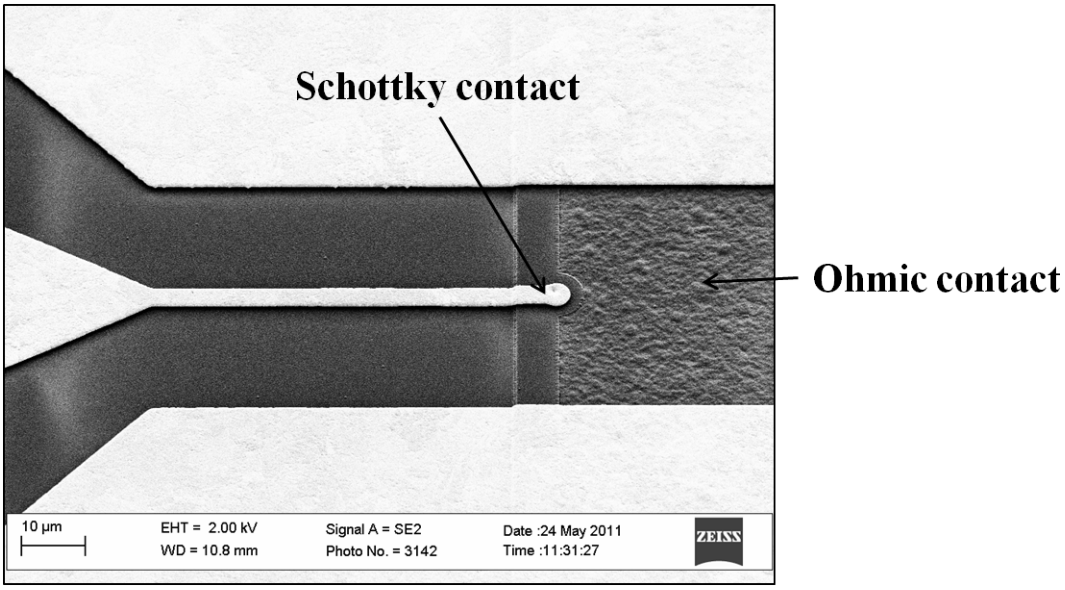


Figure 5.2: A SEM close up of a single Schottky diode. Figure 56 shows the area which is emphasized.

Measuring a single diode will provide the data necessary to determine the DC parameters in-

trinsic to a Schottky contact. The measurement is used to solve for the reverse saturation current I_o , ideality factor η , and series resistance R_s of a single contact. To do so, the measured I-V data is fit to the known forward bias relation, equation 5.1.

$$I(V) = I_{sat} e^{\frac{V}{\eta V_T}} + \frac{V}{R_s} \tag{5.1}$$

The fit is done in Mathcad using a Levenberg-Marquardt regression algorithm to minimize the error. Throughout the GaAs die, diodes are fabricated with varying anode sizes ranging between 0.8 and 1.2 micron diameters. Since the nominal design was for a 1.2 micron diameter anode, the results will be presented for that diameter.

Figure 5.3 is a semi-log plot of the I-V data for a measured device and a fit to equation 5.1. The fitted data results in a reverse saturation current of 2.24 nA, an ideality factor of 1.44, and a series resistance of 58 Ohm.

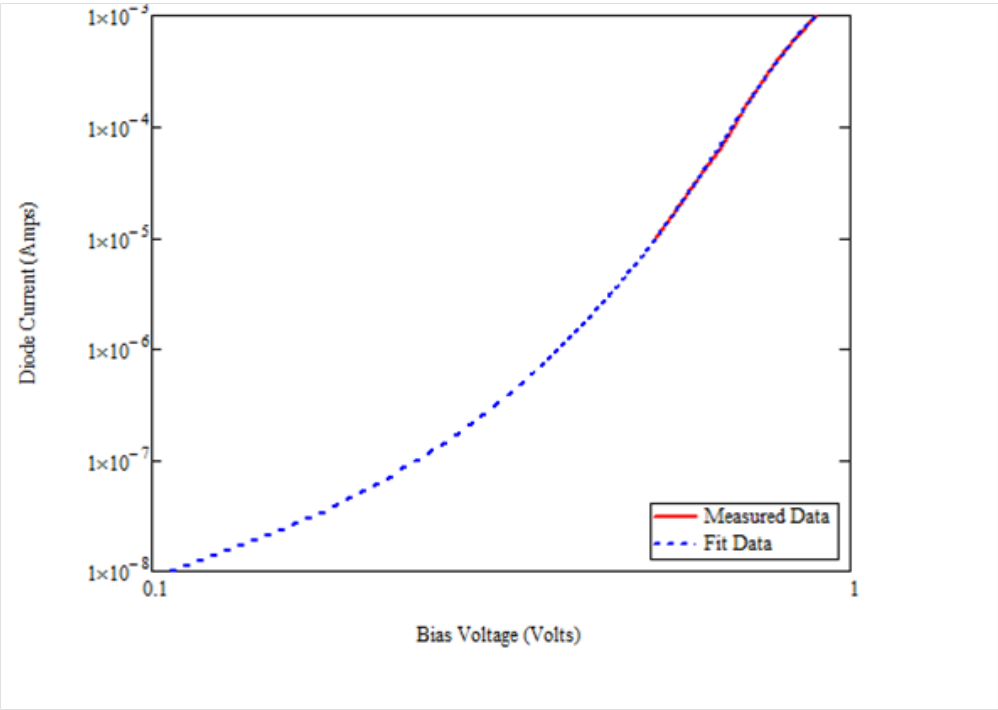


Figure 5.3: Plotting the measured and fitted IV data

A second use for the DC testing is to determine the approximate number of operating diodes within an array. It is possible that during the fabrication process one or more of the anodes may not etch completely due to variations in the lithography or SiO_2 RIE etch rate. However, because all the cells are electrically in parallel with one another, it is difficult to tell if any of the diodes have failed unless they fail as a short circuit.

As a measure of the number of cells that are functioning, the results from individual diode I-V measurements are compared to the I-V measurements of an array with all 100 devices in parallel. Assuming that at a single diode is similar to a diode within the array, it is expected that an array will pull 100 times more current than a single device at the same bias voltage. This assumption is expected to be valid because the anode size and ohmic contact geometry of a single are similar to that of an arrayed device.

Figure 5.4 plots the measured I-V data on a semi-logarithmic scale. The plot shows the results of a single diode (1.2 um diameter) and a 100 element array. The difference between the currents is two decades, as expected for an array containing 100 elements. At high bias levels, the array plot begins to deviate some from the expected scaling, but it is conceivable that this results from differences in series resistance arising from differing geometries of the array and single-element devices.

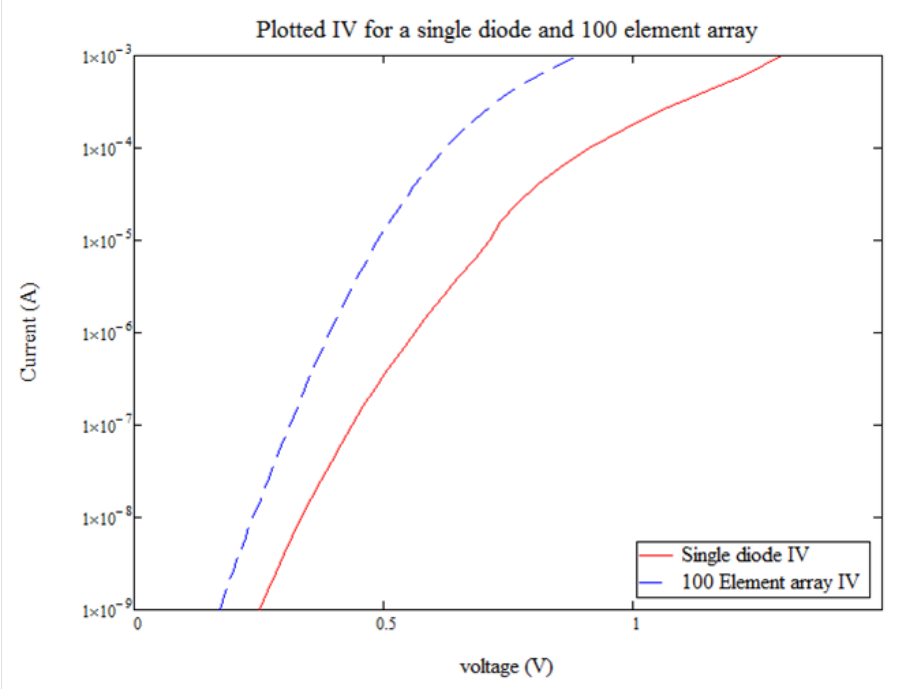


Figure 5.4: A semi-log plot comparing the IV of a single diode and a 100 element array

5.3 Responsivity Measurements

After the DC testing is complete, the focus shifts to RF characterization of the array. The first set of RF measurements are aimed at measuring the voltage responsivity of the array at 1.6 THz. This is done to verify that power at 1.6 THz can be coupled to the diodes and to aid in optical alignment. The responsivity test also provides a measure of the array power-handling capacity.

Figure 5.5 shows the optical setup used to characterize the responsivity. An Edinburgh Photonics FIRL100 laser is used to create a 1.6 THz test signal. The laser is first directed into a Martin-Puplett interferometer. The interferometer is used to rotate the polarization of the laser to ensure the correct polarization illuminates the array. In addition, the interferometer allows for a measurement of the wavelength of the FIR laser. As the roof top mirror in the interferometer translates ~45 microns, the output polarization is rotated 90 degrees. This was confirmed using a millimeter wave power

detector and a wire grid polarizer. As the laser polarization rotates it is possible to observe a drop in detected power as part of the beam begins to reflect off the wire grid.

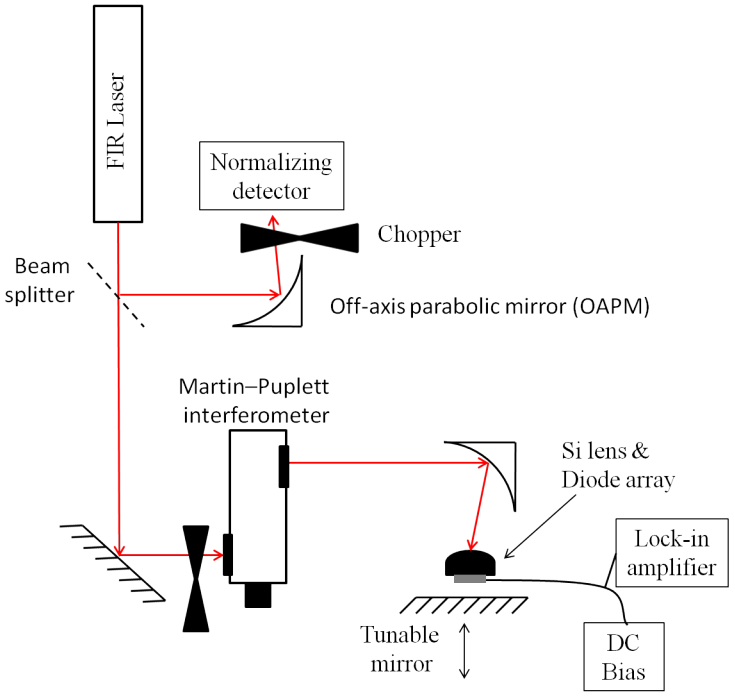


Figure 5.5: A drawing of the optical setup used to characterize the responsivity of the array

Following the Martin-Puplett, an off-axis parabolic mirror (OAPM) is used to focus energy onto a silicon lens which the array is mounted. A moveable mirror is placed as close as possible behind the array, approximately 1.5 - 2.0 mm. This mirror is used to tune the backshort to a desired impedance. However, the absolute distance from the mirror to the array is unknown. Consequently, measurements corresponding to relative distance over 200 microns are done to ensure the backshort is moved an entire wavelength at 1.6 THz.

To perform the measurement, an optical chopper is placed at the input to the Martin-Puplett and a lock-in amplifier is used to record the responsivity data. The chopper was placed early in the beam path to eliminate chopping the room lights to the array. It should be noted that any exposed Schottky diode is sensitive to ambient light in the laboratory. A chopper which shadows the diode from any room light contributes undesired detected power to the measurement. A normalizing

detector was used to monitor the power of the laser and calibrate the power to the array.

The first step to finding the array responsivity is to determine the FIR laser power at the spot which the array is mounted. To do so, a power detector is put at the focus point of the off-axis parabolic mirror. The measured power and recorded normalizing detector voltage are recorded for a number of different laser power levels. Figure 5.6 shows a plot of the data. A linear fit is used to derive a relation to predict the power to the spot as a function of monitored laser power. In this case, equation 5.2 shows the fitted equation. Figure 5.6 shows the agreement between the fitted line and measured values.

$$mWpower(mV) = 1.041 * mV + 1.57mW \tag{5.2}$$

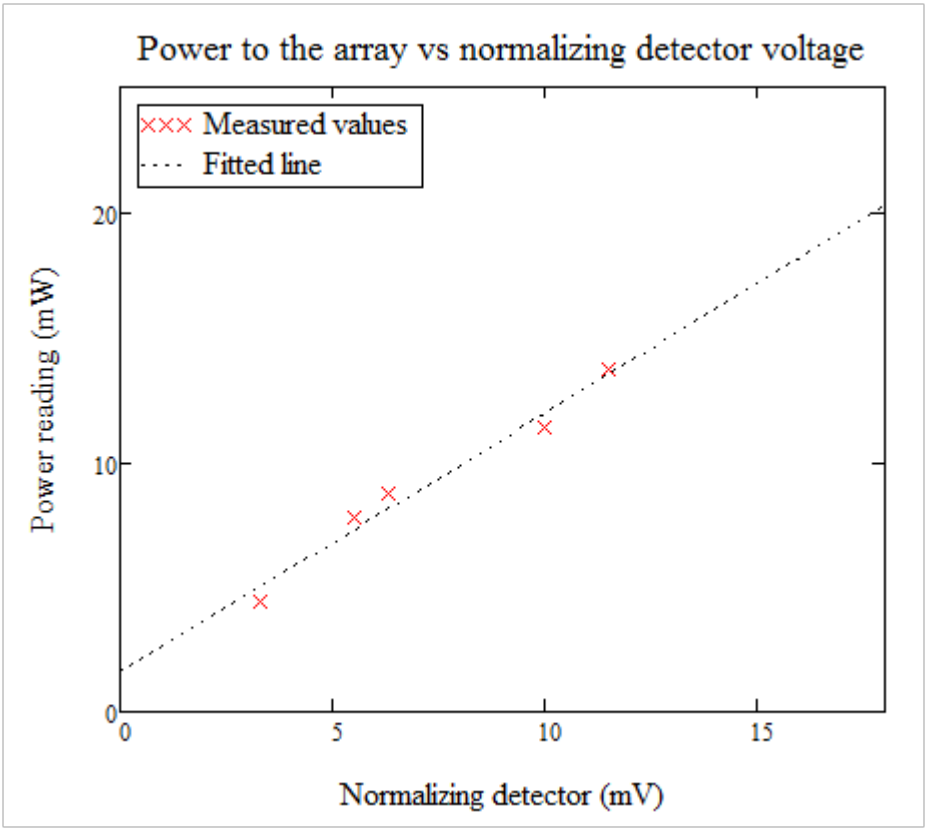


Figure 5.6: A plot showing the power to the array as a function of the normalizing detector and the fitted line to predict the power to the array.

After characterizing the measurement system, the array was aligned to ensure the focused beam was within the area occupied by the array. For this, the array was used as a video detector, as seen in Figure 5.5, and moved on a micrometer stage until the maximum video response is detected using a lock-in amplifier. The the normalizing power detector and DUT lock-in responses are recorded for various backshort mirror positions to find the optimal location for the mirror.

Table 5.1 shows the recorded data from the experiment. The first two columns record the backshort's relative position. The third column is the detected voltage from the array using a lock-in amplifier. Column four is the normalizing detector voltage monitoring the strength of the laser. The final column is the response relative to the normalizing power. These numbers do not

represent a responsivity, but show which backshort mirror positions yield the largest normalized response. Figure 5.7 shows the normalized response as a function of backshort mirror position. The dashed lines represent an electrical distance of 180 degrees, showing a repeating pattern. From this experiment it is possible to determine which backshort position yields the largest responsivity, (80 and 170 degrees).

Having found the best backshort mirror positions, the next step is to record the voltage response for different bias voltages at a fixed backshort position, 170 degrees. Using that data, a few correction factors can be applied to determine the voltage responsivity of the entire array and a single Schottky diode. Using the same setup seen in Figure 5.5, the bias current was adjusted and the response recorded.

Backshort position (um)	Backshort position (degrees)	Array detected voltage (uV)	Normalizing detector voltage (mV)	Normalized power detection
0	0	225.02	6.9	0.032612
10	19.25134	346.9	7.08	0.048997
20	38.50267	315.04	7.15	0.044062
30	57.75401	319.3	6.86	0.046545
40	77.00535	342.05	7.19	0.047573
50	96.25668	369.4	7	0.052771
60	115.508	417.02	7.38	0.056507
70	134.7594	366.03	7.29	0.05021
80	154.0107	378.35	7.01	0.053973
90	173.262	315.95	7.23	0.0437
100	192.5134	259.43	7.11	0.036488
110	211.7647	368	7.29	0.05048
120	231.016	317.1	7.31	0.043379
130	250.2674	342.32	7.24	0.047282
140	269.5187	370.64	7.34	0.050496
150	288.7701	372.26	7.26	0.051275
160	308.0214	408.03	7.34	0.05559
170	327.2727	397.97	7.53	0.052851
180	346.5241	414.3	7.34	0.056444
190	365.7754	198.02	7.54	0.026263
200	385.0267	297.15	7.31	0.04065
210	404.2781	374.36	7.58	0.049388

Table 5.1: Recorded data from the responsivity measurements

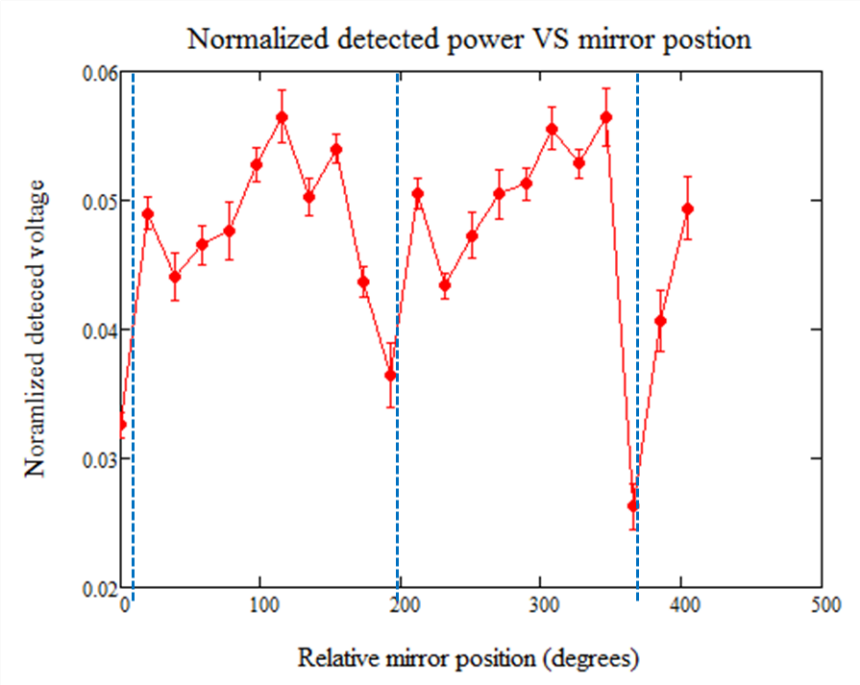


Figure 5.7: A plot of the normalized power detection as a function of back short mirror position.

Figure 5.8 plots the normalized detected voltage as a function of bias current. As expected, at low currents the diodes are poorly matched to the antenna resulting in a low response . However, as the bias current is increased, the diodes are better matched to the array embedding impedance and the response improves. As the current continues to rise, and the operation point approaches the linear region of the I-V curve, the response begins to drop.

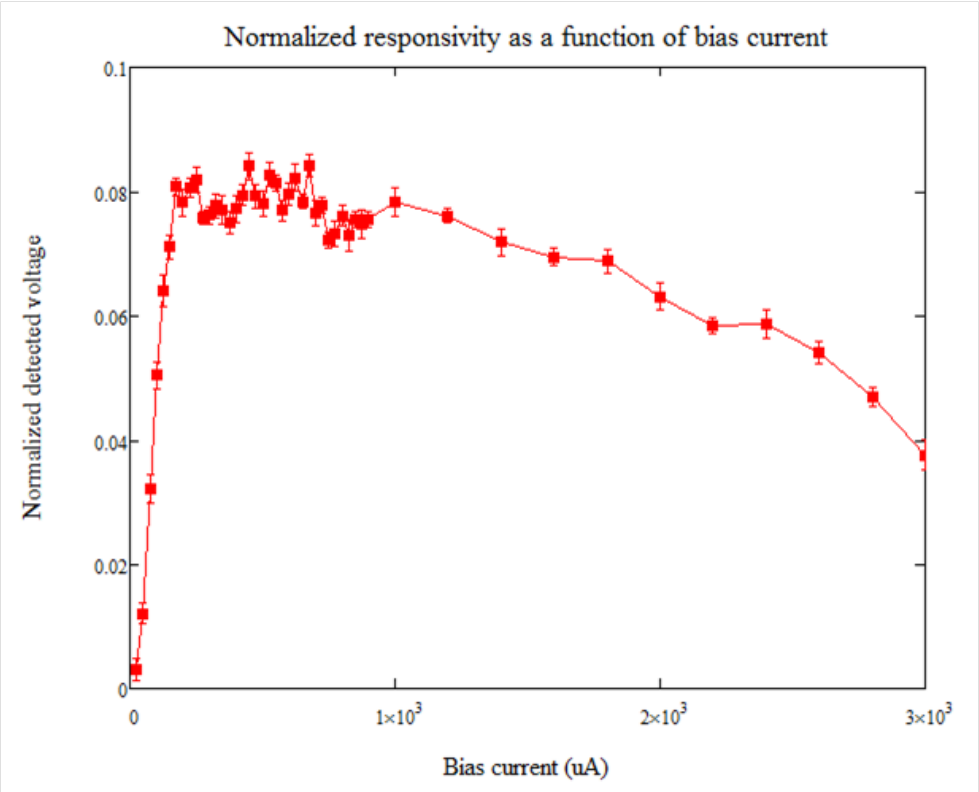


Figure 5.8: A plot showing the normalized responsivity vs bias current

Having found the bias current and mirror position that yield the largest response, it is possible to determine the responsivity of the array. For this calculation, the relationship between the FIR power to the spot and the normalizing voltage response in Figure 5.6 are used. However a few correction factors, noted below, are applied to correct the data.

The first correction accounts for the mismatch between at the silicon lens and free space. As the FIR laser radiation is incident from free space, the silicon interface causes substantial reflection. Using a free-space wave impedance, $Z_o = 377\,\Omega$, and $Z_L = 107\,\Omega$ to represent silicon, the expected transmission coefficient of to silicon is 0.44. The second correction accounts for the spread of the incident power over all the devices within the array. To do this the incident power is divided by 100.

From the plot in Figure 5.8 it is seen that a bias current of 500 uA is expected to yield a

maximum voltage response. Using a bias of 500 uA the corrected responsivity can be calculated. Table 5.2 outlines the steps. Using equation 5.1, the normalizing detector voltage can be converted to a power at the DUT spot. A normalizing detector voltage of 5.21 mW corresponds to power of 6.99 mW at the spot. Applying the two corrections yield a corrected power of 35 uW to each diode. The overall responsivity is found from the detected voltage by dividing by the corrected power. In this case the Schottky diodes measured a responsivity of 16.1 $\frac{V}{W}$ at 1.6 THz.

Bias current	DUT detected voltage	Normalizing voltage	Power to spot	Corrected power	Voltage responsivity
500 µA	0.564 mV	5.21 mV	6.99 mW	35 µW	16.1 V/W

Table 5.2: A table showing the measured responsivity data and calculated result

A final responsivity measurement is done to estimate how much power is needed to saturate the detector. For this measurement, the laser was tuned to produce its maximum power, ~10 mW at the array spot. The array's detected voltage response is monitored as attenuators are placed in the FIR laser path. Figure 5.9 shows detected response as a function of laser power. As the attenuation is removed, the detected power increases linearly, never rolling off. From this it can be concluded that the array remained in the square law region and is capable of handling more than 10 mW of incident power.

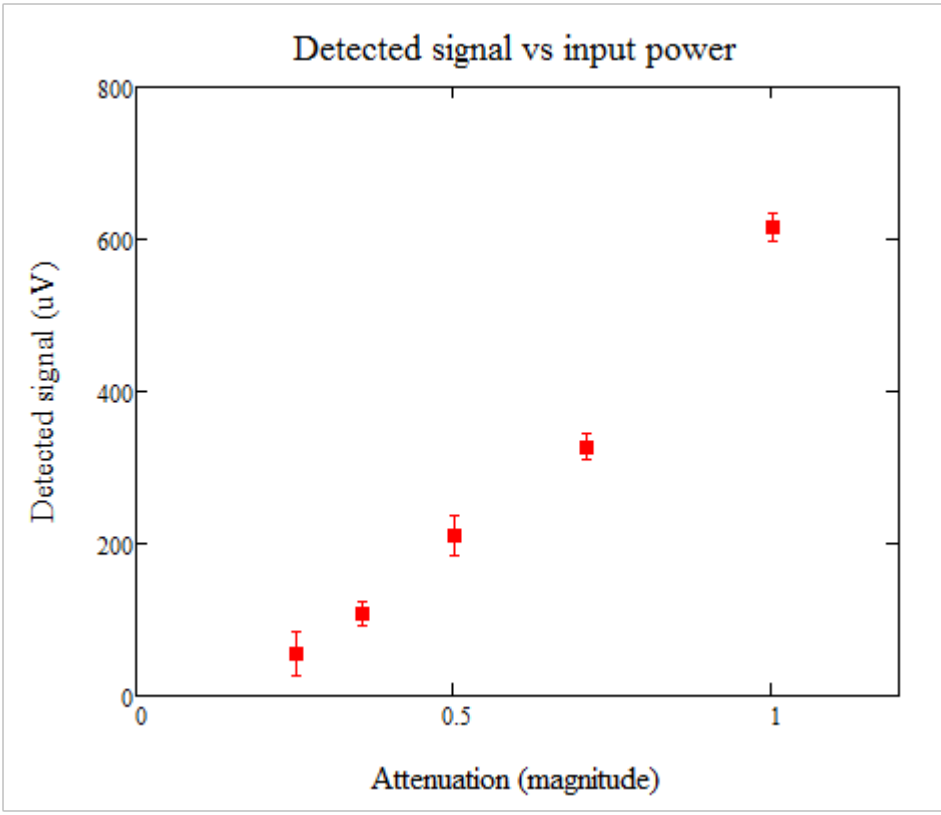


Figure 5.9: A plot showing the response of the array vs input power

To estimate the overall power handling of the device a single diode is considered. From previous measurements done on Schottky diodes with similar anode sizes, 0.8 to 2.0μm diameter, currents exceeding 1 mA is commonly enough to permanently destroy the device. For a titanium contacted GaAs Schottky diode with same anode dimensions to reach currents of 1 mA typically a bias of 1 V is required. For a practical limit of operation, the power must not exceed 1 mW in order to assure a single device is not destroyed. For an array of diodes, as long as the power distribution is equal across all the devices, the practical limit for the sideband generator array with 100 elements is ~100 mW. The FIR laser used for the measurements is capable of producing up to 150 mW at 1.6 THz, however, due to necessary optical components and path length loss, the maximum laser power is never available to the sideband generator array.

5.4 Phase Shift Characterization

Since the sideband generator array is designed to operate as a varactor or parametric upconverter, the ability of the array to produce a large phase shift is critical in determining the overall conversion loss. To characterize the phase shift of the circuit an interferometric technique is employed [25]. Figure 5.10 shows a sketch of the experimental setup. The optics take advantage of constructive and destructive interference in order to determine the relative phase difference between two bias points.

In Figure 5.10 the incident 1.6 THz signal is split using a 1mil think mylar beam splitter. A portion of the beam is reflected towards the interference mirror on a moveable stage. The remaining portion of the signal is focused onto the array. The array is held at a static bias, either at 0.3 V or -4.0 V, as the interference mirror is adjusted in 10 micron increments. The two signals are combined and detected by a GaAs Schottky diode detector mounted in a block with an integrated horn . A chopper and lock-in amplifier are used to detect the signal. As the interference mirror is adjusted, an interference pattern is recorded and repeats ~90 microns corresponding to half wavelengths of 1.6 THz in air. The interference mirror is moved over a total distance of 260 microns in 10 micron increments.

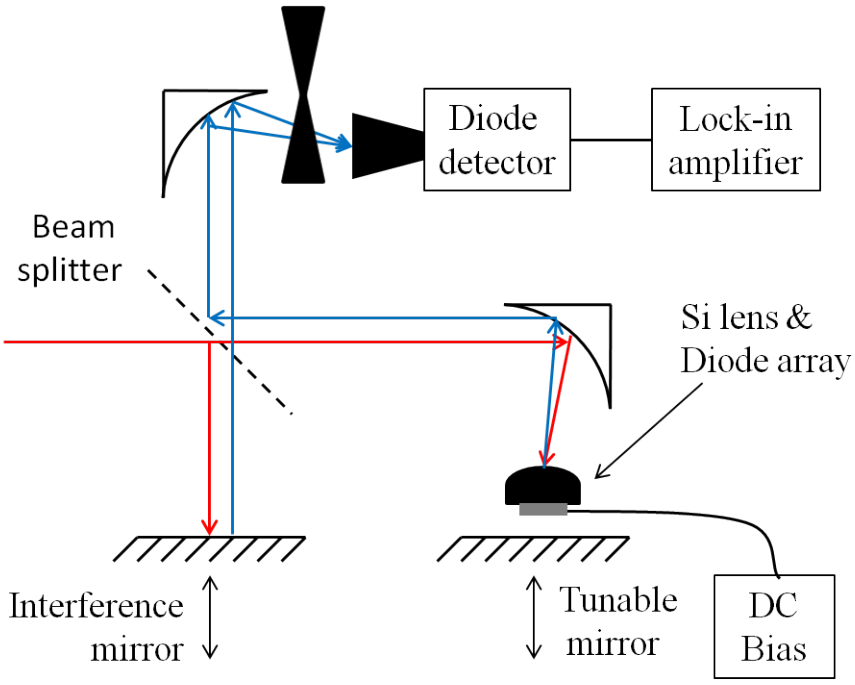


Figure 5.10: A drawing of the optical setup used to characterize the phase shift of the array.

After the data is recorded the interference mirror is adjusted back to its original position and the bias on the array is tuned to the second operating point. The interference mirror is then stepped as in the previous measurement and the voltages from the lock-in amplifier are recorded. This process is then repeated for different steps of the tuning mirror to characterize the phase shift of the array as a function of backshort position.

To interpret the data, a Mathcad program, using a Newtons method algorithm, is used to perform a best fit of a sinusoid, $A*sin(Bx+C)+D$, to each of the measured interference patterns. For each tunable mirror position, the sinusoidal fits of the interference patterns are plotted and compared. The phases, C, are compared to find the phase difference and the amplitudes, A, are compared and recorded. Figure 5.11 shows a plot of the fitted waves at a backshort position of 187 microns at two different bias points.

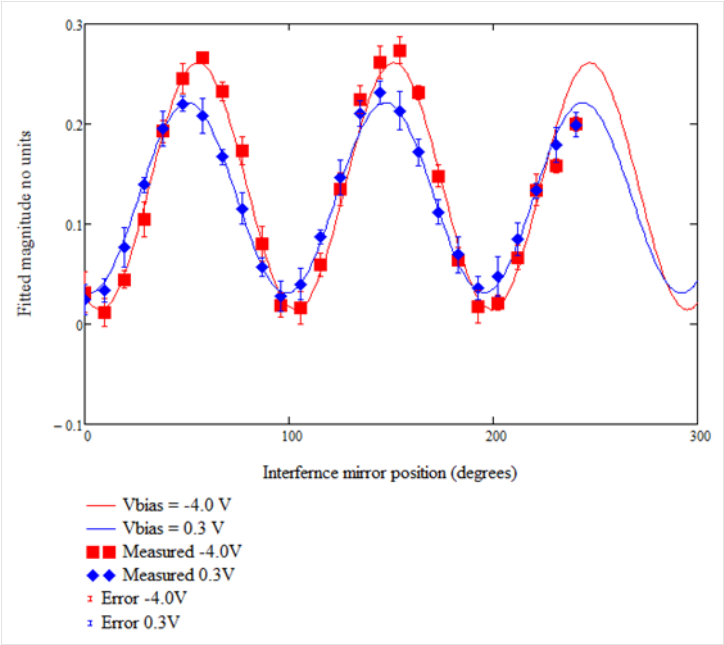


Figure 5.11: A plot comparing the fitted interference patterns at the two operating points

Figure 5.12 shows the phase and magnitude difference recorded as a function of tunable mirror position. The plot shows that for particular backshort positions there is little phase or magnitude difference. However, at repeating intervals of 90 microns, there are tunable mirror positions that yield a maximum 20 degree phase shift with a slight magnitude difference between the two operating points. These results determine which mirror positions will yield the lowest conversion losses.

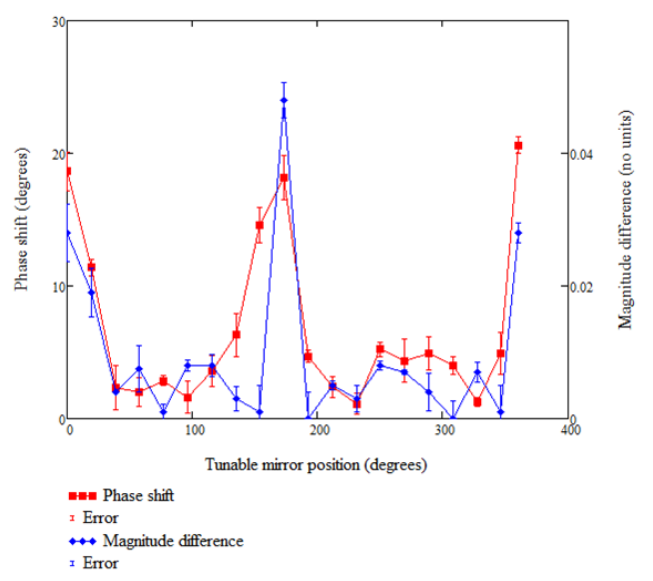


Figure 5.12: A plot showing the phase and magnitude difference between the two operating points as a function of tunable mirror position

The phase shifting results are used to verify the accuracy of the circuit models previously used to characterize and design the unit array cell. Figure 5.13 shows the ADS equivalent circuit model that is used to represent the unit cell. For this simulation the bias on the diode is varied between 0.3V and -4.0V. This is repeated for each backshort mirror position. The phase difference between the two bias points were recorded for each backshort position. Figure 5.14 compares the measured phase shift to the simulated results from Figure 5.13. The phase shift is plotted as a function of the backshort position. The measurement is done with a "relative" mirror position, so a 30 degree offset is added to "synchronize" the phasing of the two results. Both plots share the same resonance pattern and comparable maximum phase shifts of near 20 degrees.

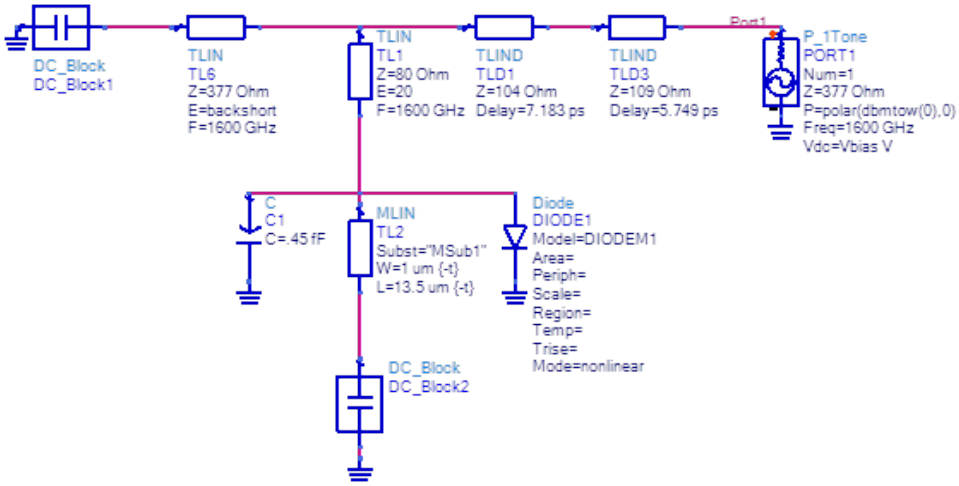


Figure 5.13: The ADS circuit model to describe the phase shift of a unit cell.

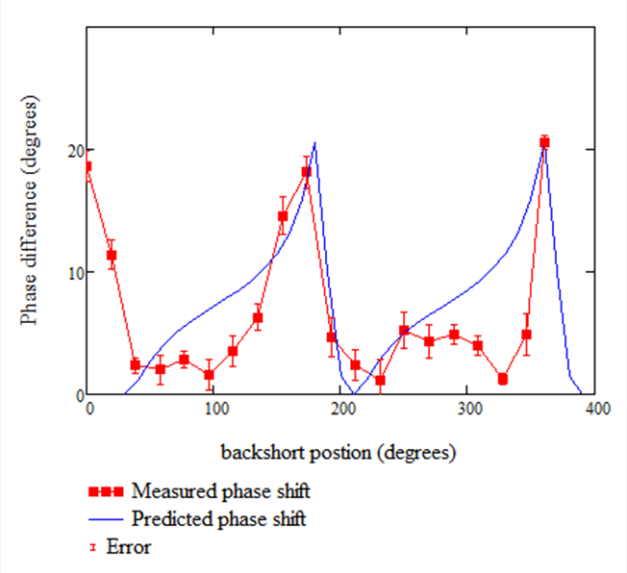


Figure 5.14: A plot comparing the simulated and measured phase shift as a function of backshort position

In order to calculate the conversion loss of the sideband generator array some small adjustments had to be made to the circuit in Figure 5.13. Figure 5.15 shows the circuit model used to predict

the conversion loss. The diode and surround embedding impedance are identical, however, ideal filters and a high frequency pump are added to modulate the diode and terminate the sidebands appropriately. The backshort is adjusted until the circuit results a maximum phase shift between the two bias points.

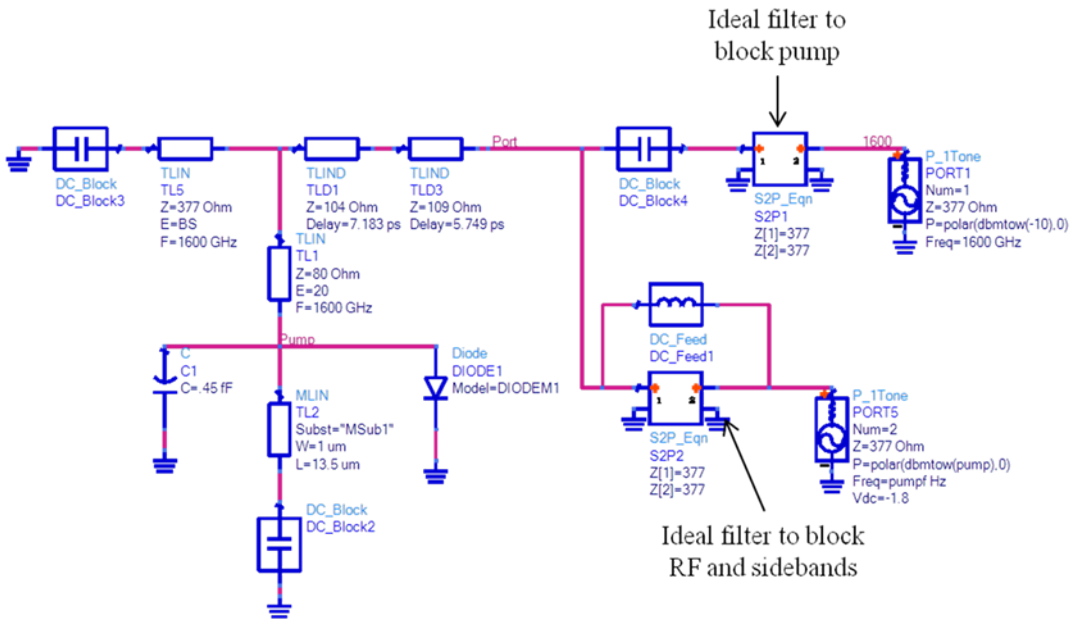


Figure 5.15: The ADS circuit model used to calculate the conversion loss

Figure 5.16 shows the reflection of the model in Figure 5.15 at various bias voltages. The maximum phase shift of the model is 22^{o}. This is in good agreement with the measured phase shift which is 20^{o}. For the simulation the diode is modulated with a 50 GHz sinusoidal pump. Enough available power is provided to modulate the diode between 0.3 and -4.0 V. The circuit in Figure 5.15 predicts a conversion loss of 26 dB.

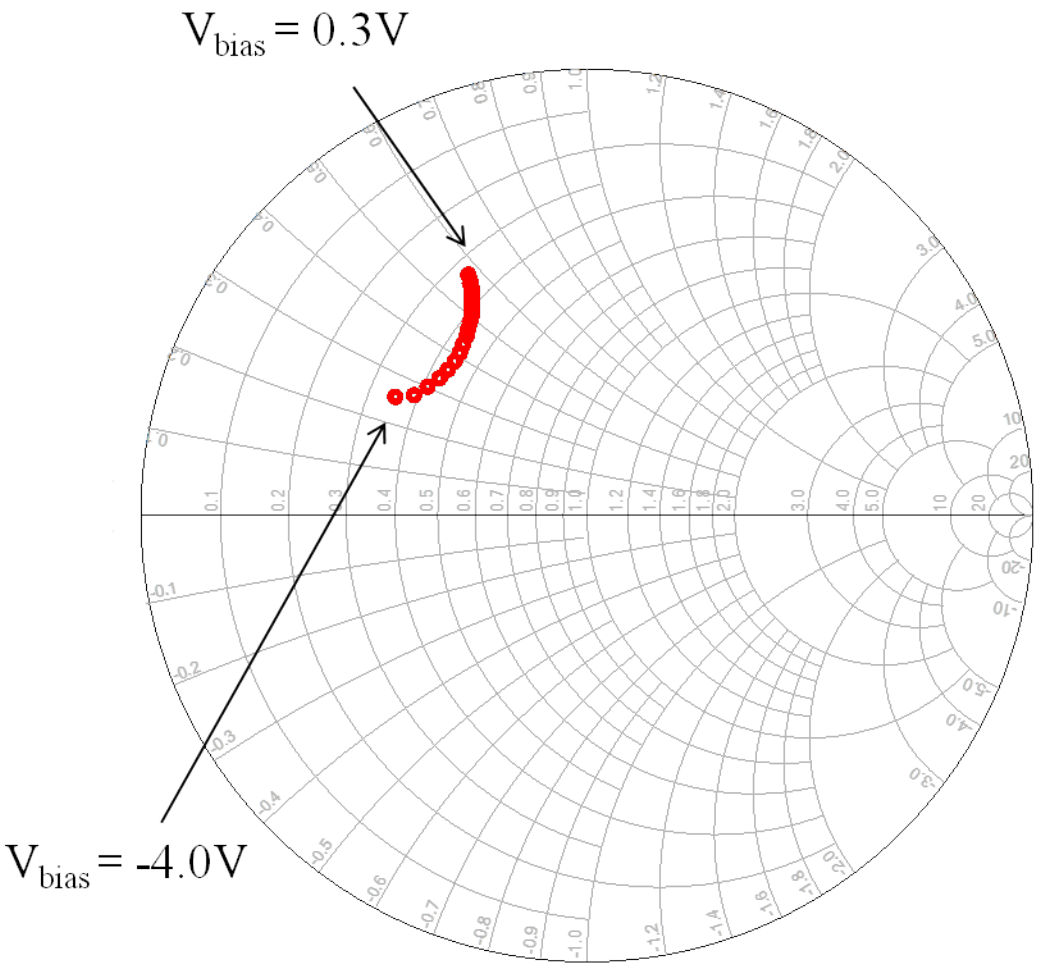


Figure 5.16: The response of the circuit in Figure 5.15 as a function of bias voltage

Chapter 6

Conclusion

The bulk of this research is dedicated to the design, fabrication, and characterization of a 1.6 THz sideband generator based on an array of varactor Schottky diodes. The goal is to meet or exceed the performance of current state-of-the-art technology. In order to accomplish this goal, the Schottky diode array takes advantage of key design features which help simplify the fabrication process, lead to higher efficiencies, and increase the overall power handling. The first design feature is a quasi-optical setup used to eliminate the need for waveguide coupling and helps spread out the incident power over a number of different diodes. The arrayed design also creates advantageous boundary conditions which can be exploited to create specific tuning elements. Another advantage of using an array of Schottky diodes is the ability to extend the power handling of the SBG. Since the available power is distributed among the number of elements in the array, the SBG input power can be increased without the fear of destroying the Schottky diodes. A second design feature which separates this work is the addition of a tuning element in parallel with the anode contact. This additional tuning element increases the performance of the sideband generator in a number of different ways. It was shown that the additional tuning element creates a circuit topology capable of reaching the fundamental limit of conversion loss. More importantly, the additional tuning element reduces the effects of the parasitic capacitance typically associated with planar Schottky diode design with out having to alter the planar diode geometry. This eliminates the need to create

complex diode geometries simplifying the fabrication process and increasing the yield and reliability of the devices greatly.

However, to design such a device, an equal amount of time was spent researching and understanding the planar Schottky diode operation at high frequencies. To do so, two different diode planar Schottky diodes were designed and fabricated. One design is centered at 20 GHz to be probed by commercially available CPW probes. The second set of diode structures were tailored to operate in the WR.1.5 band (500-750 GHz). The higher frequency diodes were designed to be probed by the micromachined on-wafer probe fabricated in house in the UVa Microfabrication lab. The aim was to see if the same modeling and characterization techniques could be used on both the low and high frequency diodes. From the results it was concluded that the same modeling techniques capable of describing the low frequency planar Schottky diode can be scaled to accurately model a similar high frequency Schottky diode. However, as the frequencies being to approach 1 THz, the parasitics within the GaAs mesa and ohmic contact can be realized and their affects can be measured at high frequencies. The time spent researching these high frequency effects is important because the results lead to more accurate models for the Schottky contact in the 1.6 THz sideband generator array design.

To characterize the array a number of different measurement techniques were used. The first was a simple responsivity measurement which showed the power handling of the array. Despite having incident powers approaching 100mW, none of the elements in the array were destroyed, and the same I-V relationship was measured before and after the responsivity measurements. The second measurement was an optical setup which used the array as a phase shifter. This measurement took advantage of a standing wave created between the array and a flat mirror. The measurement setup measured the constructive and destructive interference as a function of the array bias voltage and backshort mirror position. The results from this experiment showed for a particular backshort mirror position a 20 degree phase shift can be observed. Comparing these results to a simulated model for a unit cell showed good agreement. The results also showed the validity of the computer model.

This work has achieved many important results. The first was proving that the scaling technique

used to model low frequency Schottky contacts and the planar diode geometry can be scaled and adapted for their frequency counter parts. However, as the frequency increases past 500 GHz, the parasitic effects of the ohmic contact and GaAs mesa must be taken into account for an accurate design. The second result was the design, fabrication, and measurement of the 1.6 THz sideband generator which took advantage of an arrayed design and additional tuning element in parallel with the anode to outperform previously designed sideband generators. The measurement results from the SBG showed a number of important contributions. The results showed that the quasi-optical and arrayed design allowed for much greater power handling that previously fabricated SBGs centered around 1.6 THz. The more significant result was evidence that showed the additional tuning element in parallel with the Schottky contact helped to alleviate the parasitics associated with planar Schottky diode design. The reduction in the effects of the parasitics allowed for a much simpler fabrication process, reducing the number of mask steps, increasing the yield of the devices, and improving the reliability of the SBG.

There still remains work which can be done to further characterize the performance of the sideband generator array. One method is to use VNA extender heads in a quasi-optical setup to directly measure the S-parameters of the array. This would give a result to directly compare to the HFSS and ADS models used to describe the array. However, the challenge lies in the calibration of the setup. Another important test would be to directly measure the conversion loss of the array. To do so, a characterized 1.6 THz mixer, or downconverter, would be used to directly measure the sidebands produced by the sideband generator array. This measurement will help to characterize the bandwidth, conversion loss, and power handling of the array. Ultimately work will always continue in realm of high frequency Schottky diode characterization. As new devices are designed, and new diode geometries discovered, the need for more accurate models will grow as the need for performance at these higher frequencies increases.

Appendix A: WR1.5 planar Schottky diode process sheet

Planar GaAs Schottky Diode Process Flow

For: 625 GHz planar diodes

Start Date _____ Wafer# _____Mask _____
Wafer Lot _____ Layer type _____

	Process Module #1: Ohmic Contact formation			
	Process	**Description**	**Done**	**Date**
1	Spin Clean	E:Spin&Scrub;TCE/M: Spin&BD, Inspect and rework as necessary		
2	O2 Plasma	200 W, 10 min		
3	HMDS	Spin HMDS 30 sec		
4	Spin Resist	AZ4110, 4000 RPM, 30s		
5	Soft Bake	100 C, 1 min		
6	Edge Bead Exposure	Cont Type _____Exp Time _____ Pwr_____/_____		
7	Develop	AZ400K:DI 1:4, 2 min RDI		
8	Pattern Exposure	Cont Type _____Exp Time _____Pwr_____/_____		
9	Develop	AZ400K:DI 1:4, 1 min RDI		
10	Post-Exposure Bake	130 C, 3 min		
11	Tencor	resist		
12	GaAs etch	H3PO4(85%):H202(30%):DI 1:1:25 (Target 200nm)		
13	Tencor	resist + GaAs		
14	BOE	10:1, PTw, 10 s, RDI 1 min, KW		
15	Surface Clean	NH4OH:H20::1:25, 20 s, fast hard BD		
16	Mount	to evaporator holder		
17	Evaporation	Au/Ge 500 Ang		
		Ni 250 Ang		
		Au 1000 Ang		
18	Resist Liftoff	NMP:Poly-Glycol 1:1 120C		
19	Spin Clean	E:Spin&Scrub; M: Spin&BD, Inspect and rework as necessary		
20	O2 Plasma	200 W, 10 min		

	Process Module #2: Mesa pattern & Etch			
	Process	**Description**	**Done**	**Date**
1	Spin Clean	E:Spin&Scrub;TCE/M: Spin&BD, Inspect and rework as necessary		
2	O2 Plasma	200 W, 10 min		
3	HMDS	Spin HMDS 30 sec		
4	Spin Resist	AZ4110, 4000 RPM, 30s		
5	Soft Bake	100 C, 1 min		
6	Edge Bead Exposure	Cont Type _____Exp Time _____ Pwr_____/_____		
7	Develop	AZ400K:DI 1:4, 2 min RDI		
8	Pattern Exposure	Cont Type _____Exp Time _____Pwr_____/_____		
9	Develop	AZ400K:DI 1:4, 1 min RDI		
10	Post-Exposure Bake	130 C, 3 min		
11	Tencor	resist		
12	GaAs etch	H3PO4(85%):H202(30%):DI 1:1:25 (Target 700nm)		
13	Tencor	resist + GaAs		
15	Resist Strip	Ace spray		
14	O2 Plasma	200 W, 10 min		
15	Solvent Boil Clean	M,TCE,E: 20 s each		
16	RTA	Rapid Thermal Anneal 400C for 60 sec		

	Process Module #3: SiO2 Deposition and Microscope Dot SiO2 thickness Measurements			
	Process	**Description**	**Done**	**Date**
1	Spin Clean	E:Spin&Scrub;TCE/M: Spin&BD, Inspect and rework as necessary		
2	Solvent Boil Clean	M,TCE,E: 20 s each		
3	BOE	10s, RDI 1 min, BD		
4	Surface Clean	NH4OH:H20::1:25, 20 s, fast hard BD		
5	O2 Plasma	200 W, 10 min		
6	PECVD	**RUN ACSCRUB** / SiO2Vart 100 min ~1um		
7	Spin Clean	E:Spin&Scrub;TCE/M: Spin&BD, Inspect and rework as necessary		
8	O2 Plasma	200 W, 10 min		
9	HMDS	Spin HMDS 30 sec		
10	Spin Resist	AZ4210, 4000 RPM, 30s		
11	Soft Bake	100 C, 1 min		
12	Dot Exposure	M-Scope @ full Power w/o filter, 1.5min/Dot 20x		
13	Develop	AZ400K:DI 1:4, 1 min RDI		
14	Post-Exposure Bake	130 C, 3 min		
15	Tencor	resist		
16	BOE	~10 min to completely etch though SiO2		
17	Resist Strip	Ace spray		
18	O2 Plasma	200 W, 10 min		
19	Tencor	SiO2		

	Process Module #4: Anode Etch			
	Process	**Description**	**Done**	**Date**
1	Spin Clean	E:Spin&Scrub;TCE/M: Spin&BD, Inspect and rework as necessary		
5	O2 Plasma	200 W, 10 min		
9	HMDS	Spin HMDS 30 sec		
10	Spin Resist	AZ4210, 4000 RPM, 30s		
11	Soft Bake	100 C, 1 min		
12	Edge Bead Exposure	Cont Type _____Exp Time _____ Pwr_____/_____		
13	Develop	AZ400K:DI 1:4, 2 min RDI		
14	Pattern Exposure	Cont Type _____Exp Time _____Pwr_____/_____		
15	Develop	AZ400K:DI 1:4, 1 min RDI		
16	Post-Exposure Bake	130 C, 3 min		
17	Tencor	resist		
18	RIE Etch	CHF3 160W 0C ~20nm/min Target ~ 950 nm		
19	Tencor	resist + SiO2		
20	BOE	~30sec , RDI 1 min, BD Target ~ Remaining SiO2		
21	Tencor	resist + SiO2		
22	O2 Plasma	100 W, 4 min		
23	Spin Clean	E:Spin&Scrub;TCE/M: Spin&BD, Inspect and rework as necessary		
24	O2 Plasma	200 W, 10 min		

	Process Module #5: Metallization Layer			
	Process	**Description**	**Done**	**Date**
1	Spin Clean	E:Spin&Scrub;TCE/M: Spin&BD, Inspect and rework as necessary		
2	O2 Plasma	200 W, 10 min		
3	Surface Clean	NH4OH:H20::1:25, 20 s, fast hard BD		
4	Seed Layer Evaporation	Ti, 200A Au, 1000 A		
5	Spin Clean	E:Spin&Scrub;TCE/M: Spin&BD, Inspect and rework as necessary		
6	O2 Plasma	200 W, 10 min		
7	HMDS	Spin HMDS 30 sec		
8	Spin Resist	AZ4210, 4000 RPM, 30s		
9	Soft Bake	100 C, 1 min		
10	Edge Bead Exposure	Cont Type _____Exp Time _____ Pwr_____/_____		
11	Develop	AZ400K:DI 1:4, 2 min RDI		
12	Pattern Exposure	Cont Type _____Exp Time _____Pwr_____/_____		
13	u-scope DOT	Expose full power 1:30		
14	Develop	AZ400K:DI 1:4, 1 min RDI		
15	Post-Exposure Bake	130 C, 3 min		
16	O2 Plasma	100 W, 4 min		
17	Tencor	resist		
18	Gold Plate	Start with 1mA Target ~2um top of resist		
19	Resist Strip	Ace spray		
20	O2 Plasma	200 W, 10 min		
21	Spin Clean	E:Spin&Scrub;TCE/M: Spin&BD, Inspect and rework as necessary		
22	Gold Etch	HG-400 ~45 sec for 1000 A		
23	Ti Etch	BOE ~20 sec for 20 A		

Appendix B: 1.6 THz SBG array process sheet

Planar GaAs Schottky Diode Process Flow

For: 1.6 THz SBG array

Start Date _____ **Wafer#** _____ **Mask** _____

Wafer Lot _____ **Layer type** _____

	Process Module #1: Ohmic Contact formation			
	Process	**Description**	**Done**	**Date**
1	Spin Clean	E:Spin&Scrub;TCE/M: Spin&BD, Inspect and rework as necessary		
2	O2 Plasma	200 W, 10 min		
3	HMDS	Spin HMDS 30 sec		
4	Spin Resist	AZ4110, 4000 RPM, 30s		
5	Soft Bake	100 C, 1 min		
6	Edge Bead Exposure	Cont Type _____Exp Time _____ Pwr_____/_____		
7	Develop	AZ400K:DI 1:4, 2 min RDI		
8	Pattern Exposure	Cont Type _____Exp Time _____Pwr_____/_____		
9	Develop	AZ400K:DI 1:4, 1 min RDI		
10	Post-Exposure Bake	130 C, 3 min		
11	Tencor	resist		
12	GaAs wet etch	H3PO4(85%):H202(30%):DI 1:1:25 (Target 50nm)		
13	Tencor	resist + GaAs		
14	GaAs RIE	BCl3= 20 SCCM, RF=20W V=_____ target (200nm)		
15	Tencor	resist + GaAs		
16	BOE	10:1, PTw, 10 s, RDI 1 min, KW		
17	Surface Clean	NH4OH:H20::1:25, 20 s, fast hard BD		
18	Mount	to evaporator holder		
19	Evaporation	Au/Ge 500 Ang		
20		Ni 250 Ang		
21		Au 1000 Ang / Ti 250 Ang		
22	Resist Liftoff	NMP:Poly-Glycol 1:1 120C		
23	Spin Clean	E:Spin&Scrub; M: Spin&BD, Inspect and rework as necessary		
	O2 Plasma	200 W, 10 min		

	Process Module #2: Mesa pattern & Etch			
	Process	**Description**	**Done**	**Date**
1	Spin Clean	E:Spin&Scrub;TCE/M: Spin&BD, Inspect and rework as necessary		
2	O2 Plasma	200 W, 10 min		
3	HMDS	Spin HMDS 30 sec		
4	Spin Resist	AZ4110, 4000 RPM, 30s		
5	Soft Bake	100 C, 1 min		
6	Edge Bead Exposure	Cont Type _____Exp Time _____ Pwr_____/_____		
7	Develop	AZ400K:DI 1:4, 2 min RDI		
8	Pattern Exposure	Cont Type _____Exp Time _____Pwr_____/_____		
9	Develop	AZ400K:DI 1:4, 1 min RDI		
10	Post-Exposure Bake	130 C, 3 min		
11	Tencor	resist		
12	GaAs etch	H3PO4(85%):H202(30%):DI 1:1:25 (Target 700nm)		
13	Tencor	resist + GaAs		
15	Resist Strip	Ace spray		
14	O2 Plasma	200 W, 10 min		
15	Solvent Boil Clean	M,TCE,E: 20 s each		
16	RTA	Rapid Thermal Anneal 400C for 60 sec		

	Process Module #3: SiO2 Deposition and SiO2 thickness Measurements			
	Process	**Description**	**Done**	**Date**
1	Spin Clean	E:Spin&Scrub;TCE/M: Spin&BD, Inspect and rework as necessary		
2	Solvent Boil Clean	M,TCE,E: 20 s each		
3	BOE	10s, RDI 1 min, BD		
4	Surface Clean	NH4OH:H20::1:25, 20 s, fast hard BD		
5	O2 Plasma	200 W, 10 min		
6	PECVD	**RUN ACSCRUB** / SiO2Vart 100 min ~1um		
7	Spin Clean	E:Spin&Scrub;TCE/M: Spin&BD, Inspect and rework as necessary		
8	O2 Plasma	200 W, 10 min		
9	HMDS	Spin HMDS 30 sec		
10	Spin Resist	AZ4210, 4000 RPM, 30s		
11	Soft Bake	100 C, 1 min		
12	Pattern Exposure	Cont Type _____Exp Time _____Pwr_____/_____		
13	Develop	AZ400K:DI 1:4, 1 min RDI		
14	Post-Exposure Bake	130 C, 3 min		
15	Tencor	resist		
16	BOE	~10 min to completely etch though SiO2		
17	Resist Strip	Ace spray		
18	O2 Plasma	200 W, 10 min		
19	Tencor	SiO2		

	Process Module #4: Anode Etch			
	Process	**Description**	**Done**	**Date**
1	Spin Clean	E:Spin&Scrub;TCE/M: Spin&BD, Inspect and rework as necessary		
5	O2 Plasma	200 W, 10 min		
9	HMDS	Spin HMDS 30 sec		
	Spin PMMA	4000 RPM , 30s		
	PMMA bake	100C 1 min --> 130C 1 min -->160C 10min		
	Cr deposition	Reeds sputter tool (~300nm)		
	HMDS	Spin HMDS 30 sec		
10	Spin Resist	AZ5206, 4000 RPM, 30s		
11	Soft Bake	100 C, 1 min		
12	Edge Bead Exposure	Cont Type _____Exp Time _____ Pwr_____/_____		
13	Develop	AZ400K:DI 1:4, 2 min RDI		
14	Pattern Exposure	Cont Type _____Exp Time _____Pwr_____/_____		
15	Develop	AZ400K:DI 1:4, 1 min RDI		
16	Post-Exposure Bake	130 C, 3 min		
17	Tencor	resist		
18	RIE Etch	CHF3 160W 0C ~20nm/min Target ~ 950 nm		
19	Tencor	resist + SiO2		
20	BOE	~30sec , RDI 1 min, BD Target ~ Remaining SiO2		
21	Tencor	resist + SiO2		
22	O2 Plasma	100 W, 4 min		
23	Spin Clean	E:Spin&Scrub;TCE/M: Spin&BD, Inspect and rework as necessary		
24	O2 Plasma	200 W, 10 min		

	Process Module #5: Metallization Layer			
	Process	**Description**	**Done**	**Date**
1	Spin Clean	E:Spin&Scrub;TCE/M: Spin&BD, Inspect and rework as necessary		
2	O2 Plasma	200 W, 10 min		
3	Surface Clean	NH4OH:H20::1:25, 20 s, fast hard BD		
4	Seed Layer Evaporation	Ti, 200A Au, 1000 A		
5	Spin Clean	E:Spin&Scrub;TCE/M: Spin&BD, Inspect and rework as necessary		
6	O2 Plasma	200 W, 10 min		
7	HMDS	Spin HMDS 30 sec		
8	Spin Resist	AZ4210, 4000 RPM, 30s		
9	Soft Bake	100 C, 1 min		
10	Edge Bead Exposure	Cont Type _____Exp Time _____ Pwr_____/_____		
11	Develop	AZ400K:DI 1:4, 2 min RDI		
12	Pattern Exposure	Cont Type _____Exp Time _____Pwr_____/_____		
13	u-scope DOT	Expose full power 1:30		
14	Develop	AZ400K:DI 1:4, 1 min RDI		
15	Post-Exposure Bake	130 C, 3 min		
16	O2 Plasma	100 W, 4 min		
17	Tencor	resist		
18	Gold Plate	Start with 1mA Target ~2um top of resist		
19	Resist Strip	Ace spray		
20	O2 Plasma	200 W, 10 min		
21	Spin Clean	E:Spin&Scrub;TCE/M: Spin&BD, Inspect and rework as necessary		
22	Gold Etch	HG-400 ~45 sec for 1000 A		
23	Ti Etch	BOE ~20 sec for 20 A		

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