High-Speed Integrated Waveguide Photodiodes for Next-Generation Optical Communications

By

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Dedicated

To

My parents

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~"Let all that you do be done with love." – 1 Corinthians 16:14

Abstract

With applications such as cloud computing, social networks, and search, and the coming age of artificial intelligence and the Internet of Things (IoT), data usage is nearly doubling yearly worldwide and current data centers are facing enormous pressure to increase bandwidth and data transmission capacity. Although there have been numerous technological advances in optical communication systems that mitigate pressure on data links, it is predicted that current optical network architectures will not be able to keep up with the rising demand on bandwidth in the near future.

Furthermore, today's computers are not able to process information at the same rate as the rapidly rising demand of data, as the electrical interconnects between memory and processor nodes act as a bottleneck for efficient data transmission. Thus, we need a radical change in technology to fundamentally change the way that our data centers and high-performance computers operate in order to keep up with the ever-increasing data consumption in our society.

A promising solution to this issue is to use integrated photonics to create high-speed, low-power optical transceivers. Moreover, with the emergence of silicon photonics, photonics can be integrated onto the same chip as CMOS electronics to provide high-bandwidth optical interconnects between the CPU and memory units within a high-performance computer. In this work, I demonstrate high-speed integrated waveguide photodiodes for next-generation optical communications in future data centers and supercomputers.

More specifically, I designed and fabricated a 2 μm waveguide integrated photodiode, based on multiple InGaAs/GaAsSb type-II quantum wells, with dark current as low as 1 nA at −1 V, internal responsivity of 0.84 A/W and bandwidth >10 GHz at 2 μm. I also demonstrate ultra-low capacitance MUTC photodiodes on InP with a 44 GHz bandwidth-efficiency product (BEP). And, lastly, I report on the first quantum dot photodiodes heterogeneously integrated on silicon with a record low dark current (0.01 nA), record high 3-dB bandwidth (15 GHz), and a gain-bandwidth product of 240 GHz.

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Chapter 1 – Introduction

With applications such as cloud computing, social networks, search, and the coming age of artificial intelligence and the Internet of Things (IoT), data usage is nearly doubling yearly worldwide and future data centers face enormous pressure to increase bandwidth and data transmission capacity just to keep up. Although there have been numerous technological advances in optical communication systems that mitigate pressure on data links such as wavelength division multiplexing (WDM), dispersion management, and multimode fibers, it is predicted that current optical network architectures will not be able to keep up with the rising demand on bandwidth in the near future [1-1].

Additionally, today's computers are not able to process information at the same rate as the rapidly rising demand of data, as the electrical interconnects between memory and processor nodes act as a bottleneck for efficient data transmission. Furthermore, power consumption in data centers are expected to reach unprecedented levels, as service providers will need to provide over 15 times the amount of power in the next decade than they supplied in 2015 [1-2]. Consequently, a radical change in technology is required to fundamentally change the way that data centers and high-performance computers operate in order to stay up to pace with the ever-increasing data consumption in our society.

A promising solution to this issue is to use integrated photonics to create high-speed, low-power interconnects for next-generation, supercomputers and data centers [1-3]. Moreover, with the emergence of silicon photonics, photonics can be integrated onto the same chip as complementary metal-oxide-semiconductor CMOS electronics in order to act as high-bandwidth optical interconnects for high-performance computing applications. In this work, I demonstrate high-speed integrated waveguide photodiodes for next-generation optical communications links and interconnects.

Firstly, by opening up a new data transmission window at around 2 μm wavelength, optoelectronic devices such as photodetectors can be developed to help extend the channel capacity in future optical communication networks. Therefore, I designed and fabricated a waveguide integrated photodiode (PD), based on multiple InGaAs/GaAsSb type-II quantum wells, capable of high speed and efficient detection at 2 μm. Through optimization of the quantum well layers, I demonstrate a photodiode at 2 μm with dark current (1 nA at −1 V), internal responsivity (0.84 A/W) and bandwidth (>10 GHz).

Next, by using a novel dual-integrated waveguide-depletion layer and SU-8 planarization process, I designed and successfully fabricated ultra-low capacitance integrated waveguide modified uni-traveling carrier (MUTC) photodiodes. It has also been shown that a reduced capacitance can also reduce power consumption and increase the speed of data transmission of an atto-joule optical transceiver [1-4]. MUTC photodiodes a low dark current of 5 nA at -1 V, an ultra-low capacitance of 1.8 fF, an external responsivity of 0.26 A/W for a 5 μm x 7 μm PD, and a 44 GHz bandwidth-efficiency product (BEP) were demonstrated.

Lastly, I report on the first quantum dot (QD) photodiodes heterogeneously integrated on a silicon substrate with record low dark currents (0.01 nA) and record high 3-dB bandwidths (15 GHz), responsivity of 0.34 A/W at -9 V, as well as, avalanche gain up to 45 and a gain-bandwidth product of 240 GHz, which are higher than any quantum dot avalanche photodiode (APD) on silicon. Bit error rate (BER) and excess noise factor measurements were taken, which show a sensitivity of –11 dBm and a noise figure of ~8 at a gain of 5. Open eye diagrams up to 12.5 Gb/s were taken and temperature studies have been done, which exhibit high performance up to 60˚ C, showing that these PDs can be practically used in an uncooled, WDM link for energy-efficient optical interconnects within future supercomputers.

Chapter 2 - Introduction to Integrated Waveguide p-i-n Photodiodes

2.1 Fundamentals of Photodiodes

In order to collect the photogenerated carriers quickly and efficiently, a photodiode needs to be designed with a few figures of merit in mind. These figures of merit include responsivity, dark current, and bandwidth. While there are many different kinds of photodiodes, the p-i-n photodiode has been commonly used in the past because the thickness of the depletion region can be controlled to optimize these figures of merit. Fig. 2-1 shows the energy band structure of a p-i-n diode. An intrinsic, or lightly doped, absorption layer is sandwiched between highly doped p- and n-type contact layers. The p- and n-type contact layers are designed to be transparent for the incoming light so that the electron-hole pairs are generated solely in the depletion region. The photogenerated electron-hole pairs are then separated and swept out of the depletion region by the applied electric field coming from the external voltage as shown in Fig. 2-2 leading to current flow in the external circuit [2-1].

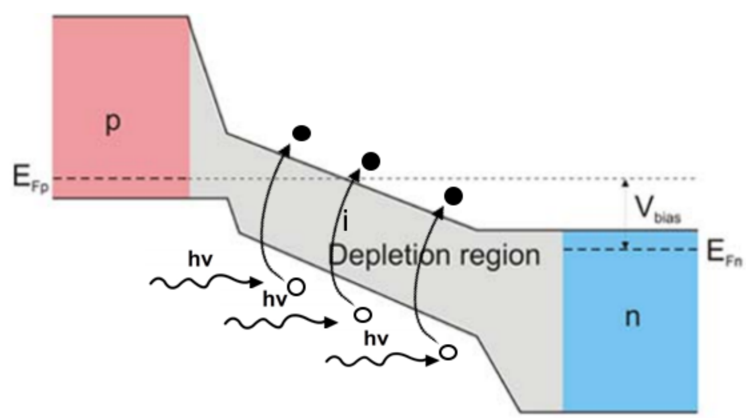


Fig. 2-1. Energy band diagram of a p-i-n photodiode [2-2].

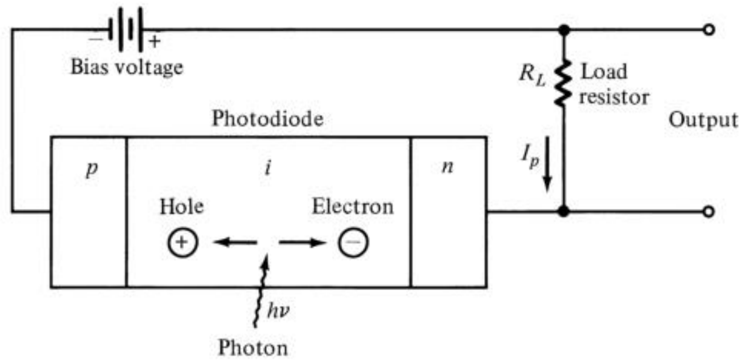


Fig. 2-2. Schematic of a p-i-n photodiode connected to external voltage source and load circuit [2-3].

Responsivity, $\mathcal{R}$, is defined as the output current in Amperes produced by the photodiode per optical power illuminated on the photodiode in Watts. It is a function of the quantum efficiency, η, defined as the number of electron-hole pairs generated in a device and collected by the external circuity for each photon that is absorbed by the device. For example, 100% external quantum efficiency would mean that for each incoming photon absorbed in the photodiode, one corresponding electron-hole pair is collected and injected into the external circuit. Moreover, internal responsivity refers to the amount of current produced by the photodiode under optical illumination minus any losses in between the input optical signal and the photodiode, whereas external responsivity refers to the current produced by the photodiode without accounting for losses outside the photodiode.

Below are the definitions for responsivity and external, and internal, quantum efficiency,

$$\mathcal{R} = \frac{I_{PD}}{P_{opt}} = \eta * \frac{\lambda(\mu m)}{1.24}\ (\frac{A}{W}) \tag{2-1}$$

$$\eta_{ext} = \frac{I_{PD}}{q} * \frac{h\nu}{P_{opt}} \tag{2-2}$$

$$\eta_{int} = \eta_{ext} * (1 - R_0)\left(1 - e^{-\alpha\Gamma L}\right) \tag{2-3}$$

where $\mathcal{R}$ is the responsivity, I_{PD} is the current produced by the photodiode, P_{opt} is the optical power illuminated on the photodiode, η_{ext} is the external quantum efficiency, η_{int} is the internal quantum efficiency, R_0 is the reflection at the air-semiconductor interface, α is the absorption coefficient of the semiconductor material, Γ is the optical confinement factor in the absorption region. L is the length of the absorption region, λ is the wavelength of the input optical signal, h is Planck's constant, q is the elementary charge, and ν is the frequency of the input optical light.

With a high reverse bias applied on the photodiode, avalanche breakdown occurs in the device. Carriers gather enough kinetic energy to bombard and collide into an atom, and causes the atom to ionize and an electron to be freed into the conduction band. This process is called impact ionization, and repeats itself to build up a large number of carriers. This produces gain in the device, as one parent electron creates a large number of electrons to be generated. Gain is also defined as the ratio between the photocurrent when the photodiode is operating under avalanche breakdown and the photocurrent when the device is at unity gain. Unity gain is defined as the responsivity of the photodiode after the device is fully depleted.

Dark current refers to the generated current in a photodiode in the absence of light. Ideally, there is only diffusion current in a photodiode, however, due to thermal effects and crystal lattice imperfections, this is not realistically achievable. More importantly, low dark current is important in order to reduce the noise in a photodiode. The main contributors to dark current are diffusion current, Shockley-Read-Hall generation-recombination current, band-to-band tunneling current, and trap-assisted tunneling current. Generation-recombination current may be decreased by using higher crystal quality and wider bandgap materials, by reducing the number of defects and thermionic ionization of carriers. Also, generation-recombination current caused by surface leakage is a common issue in photodiodes, which can be mitigated by passivating the surface of the device junction area with an insulating material, filling mid-gap traps and eliminating dangling bonds. Additionally, tunneling current can be lowered by using wide band gap materials. Moreover, dark current also experiences multiplication gain when the photodiode is operating under avalanche breakdown and must be factored into the total dark current for photodiodes under high applied voltages.

The frequency response is defined as the response speed of the photodiode to a modulated optical signal. The 3-dB bandwidth is the modulation frequency at which the RF output power extracted from the photodiode at an external load has dropped by 3 dB compared to its value at low frequency. The RF power is defined as the amount of AC power from a photodiode extracted by an external load. It can be expressed as,

$$P_{RF} = \left|I_{(t,f)}\right|^2 R_L \tag{2-4}$$

for a single frequency sinusoidal input signal, where $I_{(t,f)}$ represents the root mean square (RMS) of the AC photocurrent and R_L represents the external circuit load impedance. In p-i-n PDs made out of bulk material, the total RF frequency response of a photodiode is determined by the combination of two factors: the photogenerated carrier transit time through the device and the resistance-capacitance (RC) time constant [2-4].

The transit time can be defined as the amount of time it takes photogenerated carriers to drift through the depletion region and contact regions of the device before being injected into the metal contacts and delivered to the external load. The electron and hole effective mass and mobility play an essential role in the transit time, as well as, the distance they must travel through the device layers before reaching the contacts. The carrier transit time can be expressed as,

$$f_t \approx \frac{3.5v}{2\pi d} \tag{2-5}$$

where v is the effective velocity of the carriers through the depletion region, and d is the thickness of the absorption region.

The RC time constant, on the other hand, is a function of the PD series resistance and external load resistance, as well as, the capacitance of the photodiode. The capacitance can be modeled by a parallel plate capacitor, where the contact regions of the device effectively act as the plates of the capacitor, and the depletion region acts as the dielectric in between the plates, as shown in Fig. 2-3. The total capacitance of a diode is regarded as the sum of the diffusion capacitance and junction capacitance [2-5]. The junction capacitance, also referred to as the depletion layer capacitance, is essentially dependent on the charge variation of the depletion region, while the diffusion capacitance is dependent on the charge concentration in the contact regions. Because the photodiode is reverse-biased, the diffusion capacitance of a p-n junction is negligible in comparison to the junction capacitance of the photodiode, as most of the charge variation lies in the depletion region. The junction capacitance of a reverse-biased photodiode is modeled like a parallel-plate capacitor,

$$C_j = \frac{\varepsilon_0 \varepsilon_r A}{d} \tag{2-6}$$

where ε_0 is the permittivity of free space, ε_r stands for the dielectric constant of the depletion layer material, A is the physical area of the photodiode, d is the distance between the plates [2-5]. The RC-limited 3-dB bandwidth can then be defined as,

$$f_{RC} = \frac{1}{2\pi R_{tot} C_j} \tag{2-7}$$

where R_{tot} is the sum of the series resistance of the photodiode and the external load resistor, and C_j is the photodiode junction capacitance.

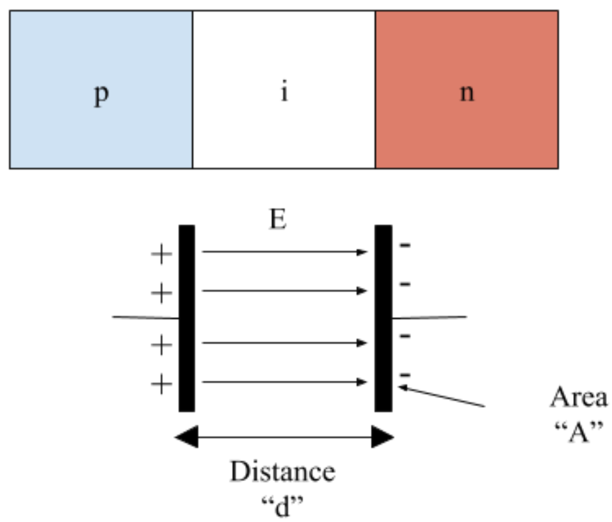


Fig. 2-3. Parallel-plate capacitor model of a p-n junction diode.

The total 3-dB bandwidth of a p-i-n photodiode is expressed in Equation (2-7) [2-2].

$$f_{3dB} = \sqrt{\frac{1}{\frac{1}{f_{RC}^2}+\frac{1}{f_t^2}}} \tag{2-7}$$

2.2 Integrated Waveguide p-i-n Photodiodes

In a vertically-illuminated p-i-n photodiode, the input light is absorbed vertically through the intrinsic absorption region. In order to achieve high responsivity, the thickness of the absorption region should be large. However, the thick absorber increases the transit time limiting the bandwidth. The bandwidth-efficiency product (bandwidth × quantum efficiency) is limited to approximately 20 GHz for top-illuminated p-i-n PDs and 35 GHz for back-illuminated PDs [2-4, 2-5]. Back-illuminated PDs have an higher efficiency than top-illuminated PDs due to reflection of light from the top metal back through the absorption region. Furthermore, the transit time and the RC time constant compete with one another in the total frequency response of the photodiode. For example, a thicker depletion layer produces lower junction capacitance and higher responsivity, but, also a longer carrier transit time, which limits the frequency response. And if the depletion region is too thin, the device capacitance will be large, which results in a large RC time constant, also limiting the total bandwidth. Fig. 2-4 demonstrates the tradeoff between quantum efficiency and transit time bandwidth with $d_{thickness}$, the absorption thickness of a photodiode.

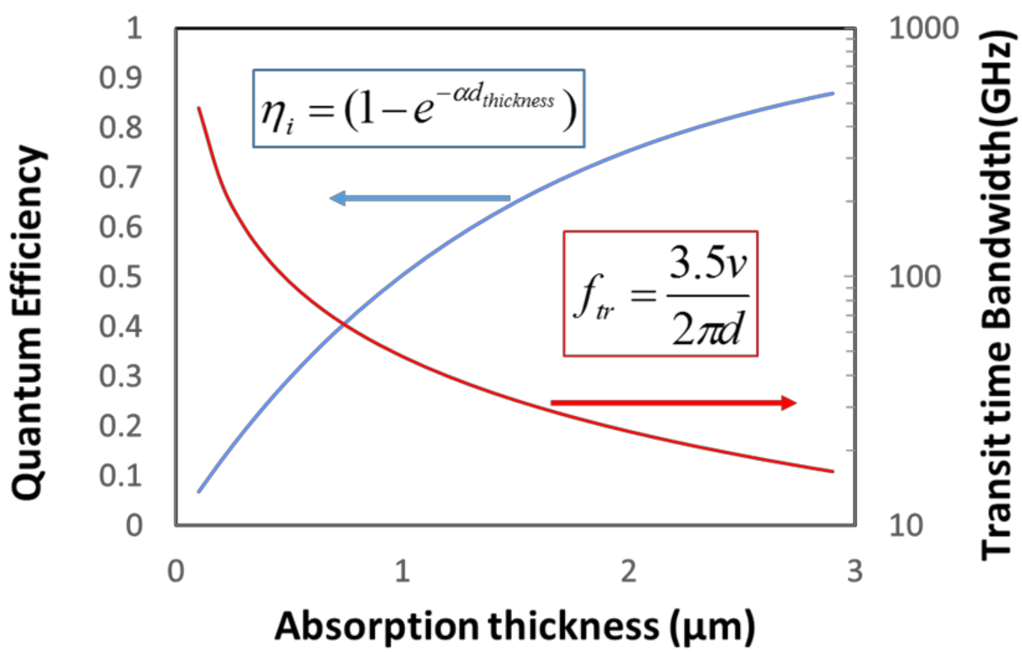


Fig. 2-4. Top-illuminated photodiode internal quantum efficiency, η_{int} and transit time bandwidth, f_{tr}, as a function of absorption region thickness [2-8].

One way to alleviate this constraint is to integrate an optical waveguide with the photodiode to evanescently couple the optical mode into the absorption region. An optical waveguide consists of an optically transparent material at the wavelength of interest, that guides a propagating electromagnetic field. It consists of a core material with an index of refraction, n_1, and two cladding materials that with lower indices of refraction, than the core, n_2 and n_3, to allow for total internal reflection within the core material. When two separate optical waveguides are brought close enough to each other, the evanescent field from the guided mode can excite a propagating mode in the adjacent waveguide. This is precisely what happens in an integrated waveguide photodiode.

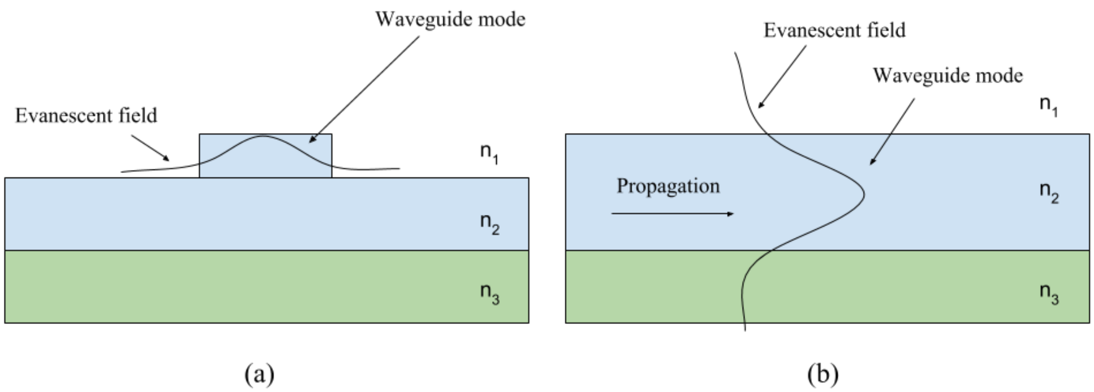


Fig. 2-5. (a) Cross-section schematic of optical rib waveguide. (b) Side-view of optical rib waveguide with electric field of progagating mode.

In an integrated waveguide p-i-n photodiode, light is evanescently coupled from an optical waveguide laterally into the absorption layer, which excites a mode along the optical absorption path oriented perpendicularly to the electric field. This mitigates optical power saturation because the incoming mode is uniformly coupled across the absorption region instead of being concentrated on a specific portion of the absorption region. Furthermore, the carrier transit time and responsivity are decoupled, since the quantum efficiency no longer depends solely on the thickness of the absorption region anymore, but now, also on the length of the absorption region. With this approach, one can design a p-i-n photodiode with a thin absorption region and simultaneously achieve both high quantum efficiency and short carrier transit times by absorbing light across the length of the device instead of through the thickness of the absorption region. However, a PD with a thin absorption region will also have a higher junction capacitance so, the length of the device then must be optimized to maximize quantum efficiency, while also minimizing junction capacitance and carrier transit times. Lastly, another advantage of integrated waveguide photodiodes is their capability of being monolithically integrated into a photonic integrated circuit (PIC).

One design that is to be discussed further in Chapter 3, is the dual-integrated waveguide-depletion layer waveguide p-i-n photodiode. In this new design, a portion of the depletion region simultaneously serves as the optical waveguide of the photodiode. The guided mode is now propagating in this depletion layer-waveguide, and is coupled into the absorption region of the device within a short distance. This allows for high responsivity in smaller area photodiodes, which also relaxes the constraint made by the RC time constant of the device.

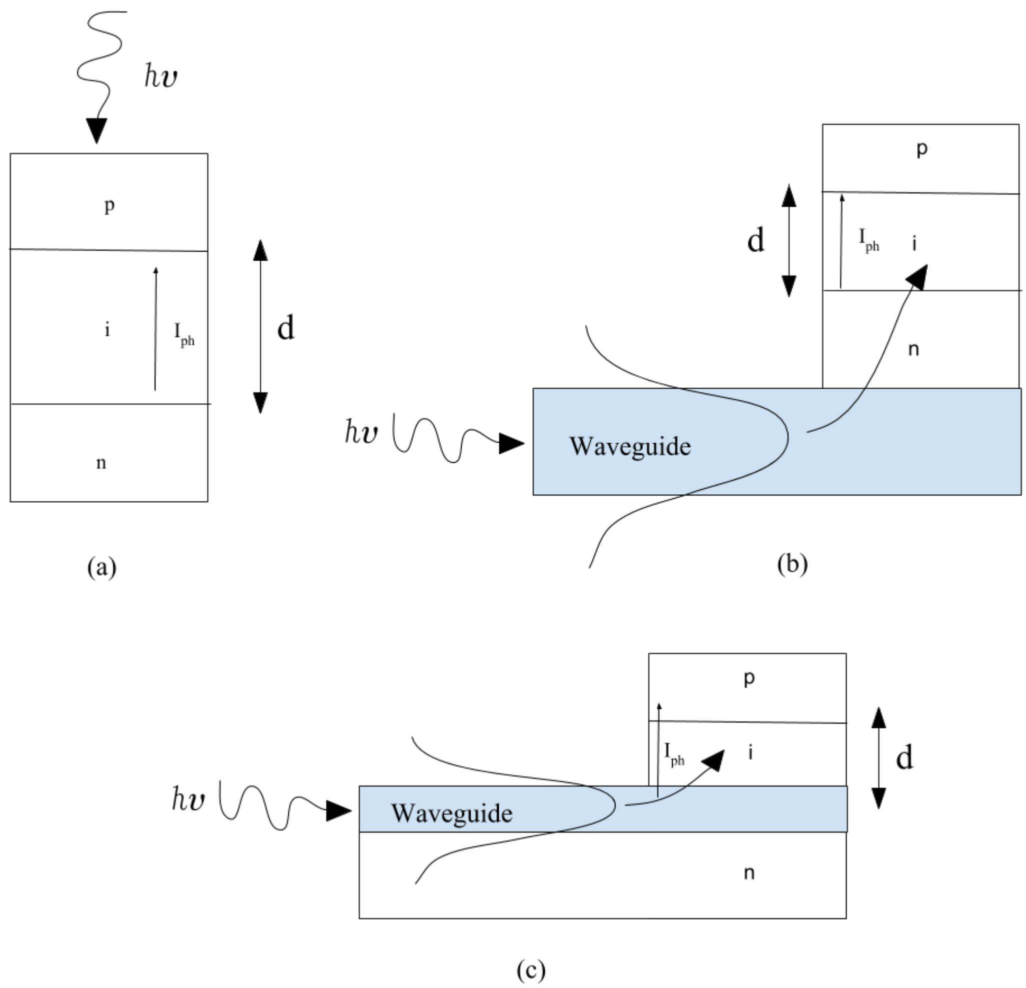


Fig. 2-6. (a) Top-illuminated photodiode. (b) Conventional integrated waveguide photodiode with optical waveguide evanescently coupling light into photodiode absorption region from below. (c) Novel dual-integrated depletion layer-waveguide p-i-n photodiode.

Chapter 3 - Type-II InGaAs/GaAsSb MQW integrated waveguide p-i-n photodiodes for high-speed 2 μm detection

3.1 Introduction

With data demands rising exponentially, fiber-optic communications links are being pushed closer to the Shannon limit, as data channels in the 1310 and 1550 nm transmission windows become fully exploited and approach maximum capacity. Although there have been numerous technological advances in optical communication systems that mitigate pressure on data links such as Erbium-doped fiber amplifiers (EDFA), wavelength division multiplexing (WDM), space division multiplexing, dispersion management, advanced modulation formats with digital signal processing techniques (DSP), and multimode fibers, it is predicted that current network architectures will not be able to keep up with the rising demand on bandwidth in the near future [3-1].

One promising solution to this issue is to utilize the spectral window around 2 μm wavelength, in which optical fibers and optoelectronic devices such as lasers and photodetectors can be developed to support future optical communication networks. Recent developments such as the hollow core photonic bandgap fibers (HC-PBGF) have already been demonstrated to work in WDM transmission with a minimum loss of less than 0.2 dB/km at 2 μm (Fig. 3-1). Since only a small portion of the light actually propagates in silica, the effect of material nonlinearities is insignificant in comparison with standard single mode fibers [3-2]. This can be promising for low latency and high-channel capacity optical data transmission.

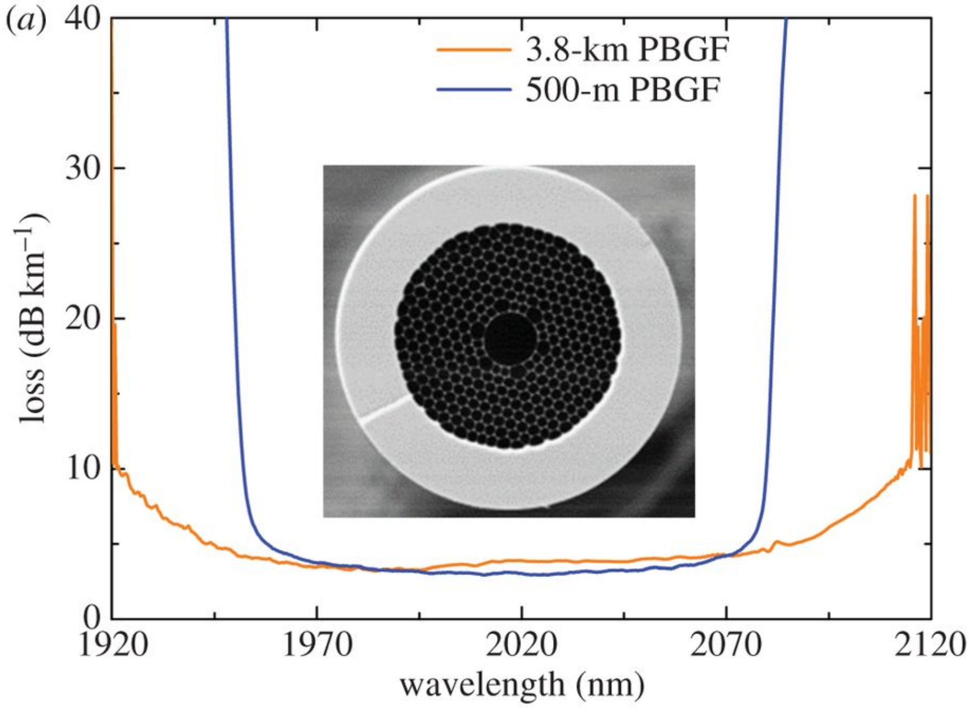


Fig. 3-1. Spectral transmission profiles for two different HC-PBGF designs of 500 m and 3.8 km lengths, respectively. Inset is a photograph of the cross-section of the 3.8 km HC-PBGF [3-3].

Fig. 3-2 shows the transmission spectra of a silica single mode fiber, as well as, different rare earth doped optical amplifiers. Thulium-doped fiber amplifiers (TDFAs) have the advantage of a large gain-bandwidth and low noise, so they can support many channels in an optical transmission link, allowing a sizeable extension in bandwidth capacity. Most of the components required to build photonic integrated circuits and devices (PICs) operating at 2 μm such as semiconductor lasers, optical amplifiers, and arrayed waveguide gratings (AWGs) have already been developed [3-4]. However, to date only a few semiconductor high-speed photodetectors and waveguide photodiodes have been developed extensively for 2 μm [3-5]-[3-8].

Photodetectors for 2 μm are also useful for gas and chemical sensing, LIDAR, and medical applications. This wavelength region offers an "eye safe" platform for coherent LIDAR systems employed by self-driving cars to sense obstacles and avoid collisions [3-9]. Additionally, CO_2 gases in the atmosphere can be sensed at 2 μm, which is helpful in tracking global climate change [3-10]. Also, given that light is absorbed by glucose around 2 μm, detectors can also be used to monitor blood glucose levels in diabetics.

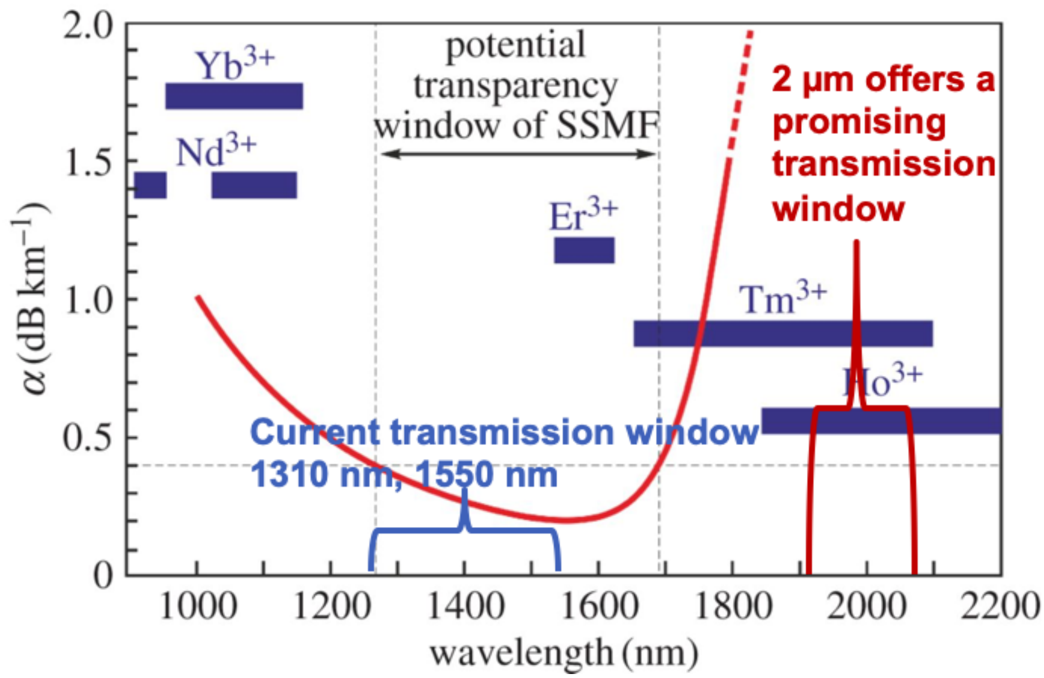


Fig. 3-2. The transmission bandwidth of standard SMF—superposed on which are the amplification bands associated with erbium and other rare earth laser ions incorporated in a silica glass matrix. As can be seen, considerable bandwidth extension would be opened up within the range of 1700–2100 nm with the combination of wide-band Thulium Doped Amplifiers (TDFA) and hollow core photonic bandgap fibers (HC-PBF) [3-3].

Fig. 3-3 shows the different bulk semiconductor materials typically used for active devices in the spectral range from 1.31 μm to 1.6 μm, which is the optical transparency window of silica single mode fibers. However, in order to utilize an optical transmission window at 2 μm, a semiconductor material is needed with a bandgap energy low enough to absorb and emit 2 μm light.

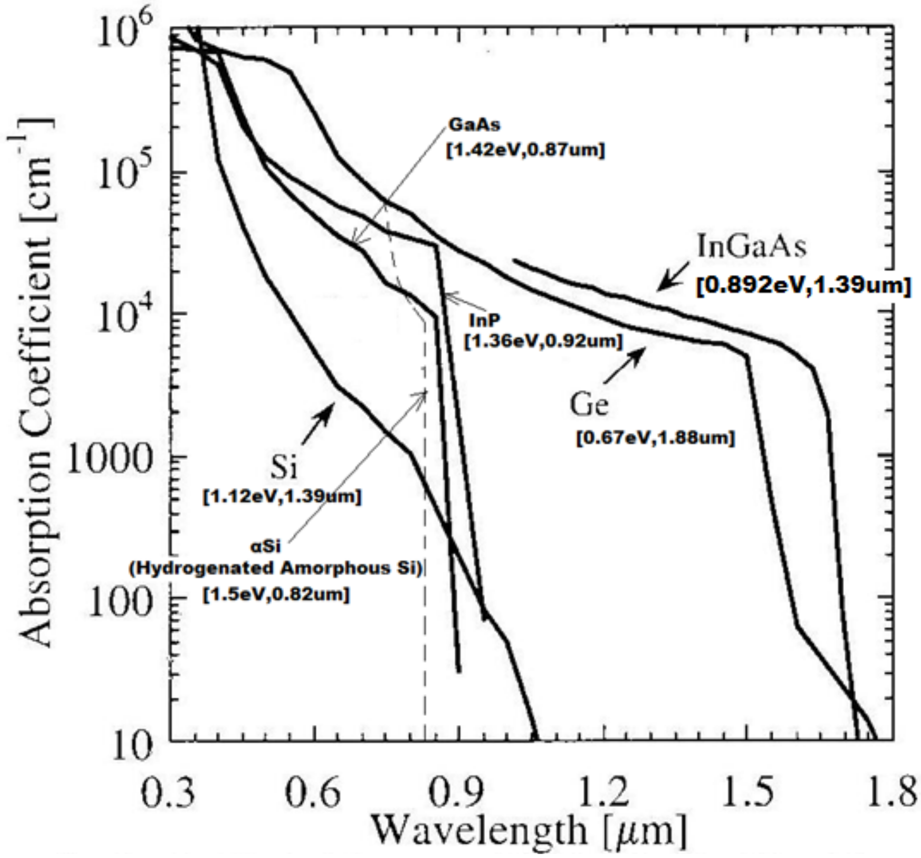


Fig. 3-3. Absorption coefficient of different bulk semiconductor materials versus wavelength of incoming light [3-11].

Silicon provides a viable and promising platform for photonic integrated circuits at 2 μm, especially for passive devices, such as waveguides, which have shown that silicon has low intrinsic absorption at 2 μm, with losses as low as 1 dB/cm [3-12]. Indium phosphide (InP) also provides a mature and well-developed platform for PICs, especially for active devices such as photodiodes, used in current optical telecommunications networks. For example, direct band gap materials grown on InP, for example InGaAs, can be strained to extend the cut-off wavelength past 2 μm, however, the lattice mismatch with InP causes high crystal defect density that leads to high dark currents. A different approach is to use InGaAsN, but it is difficult to grow and still in the early stages of being developed for practical usage [3-13].

Quantum heterostructures such as quantum wells can also be used. Quantum wells have been used in the past to develop lasers, modulators, and detectors, which are able to manipulate light of a longer wavelength than bulk materials. A multiple quantum well (MQW) p-i-n photodiode can be made by using a stack of quantum wells as the absorption region to be sandwiched between p-doped and n-doped contact layers. Type-I AlInGaAs/InGaAs quantum wells have been used in the past, but they still require strained InGaAs [3-14]. GeSn/Ge MQWs on silicon photodiodes have also caught attention for their high-speed detection at 2 μm, but, at the cost of low responsivity [3-15]. Our approach is to use InGaAs/GaAsSb type-II quantum wells as the absorption material for these photodiodes. In this chapter, I will discuss a waveguide integrated p-i-n photodiode (PD) based on multiple InGaAs/GaAsSb type-II quantum wells capable of high speed and efficient detection at 2 μm.

3.2 Type-II InGaAs/GaAsSb Quantum Wells

A study of the band-offsets of InGaAs and GaAsSb shows that the band alignment between InGaAs and GaAsSb is type-II, meaning the electrons and holes are confined in different layers [3-16]-[3-19]. In InGaAs/GaAsSb type-II quantum wells, electrons are confined in the InGaAs wells, while the holes are confined in the GaAsSb wells. In a type-I quantum well, however, the electrons and holes are both confined in the same layer. More specifically, type-I absorption generates an electron-hole pair in the same layer, and in type-II absorption, electrons are generated in one layer, while holes are generated in another. The difference between type-I and type-II band absorption is shown in Fig. 3-4.

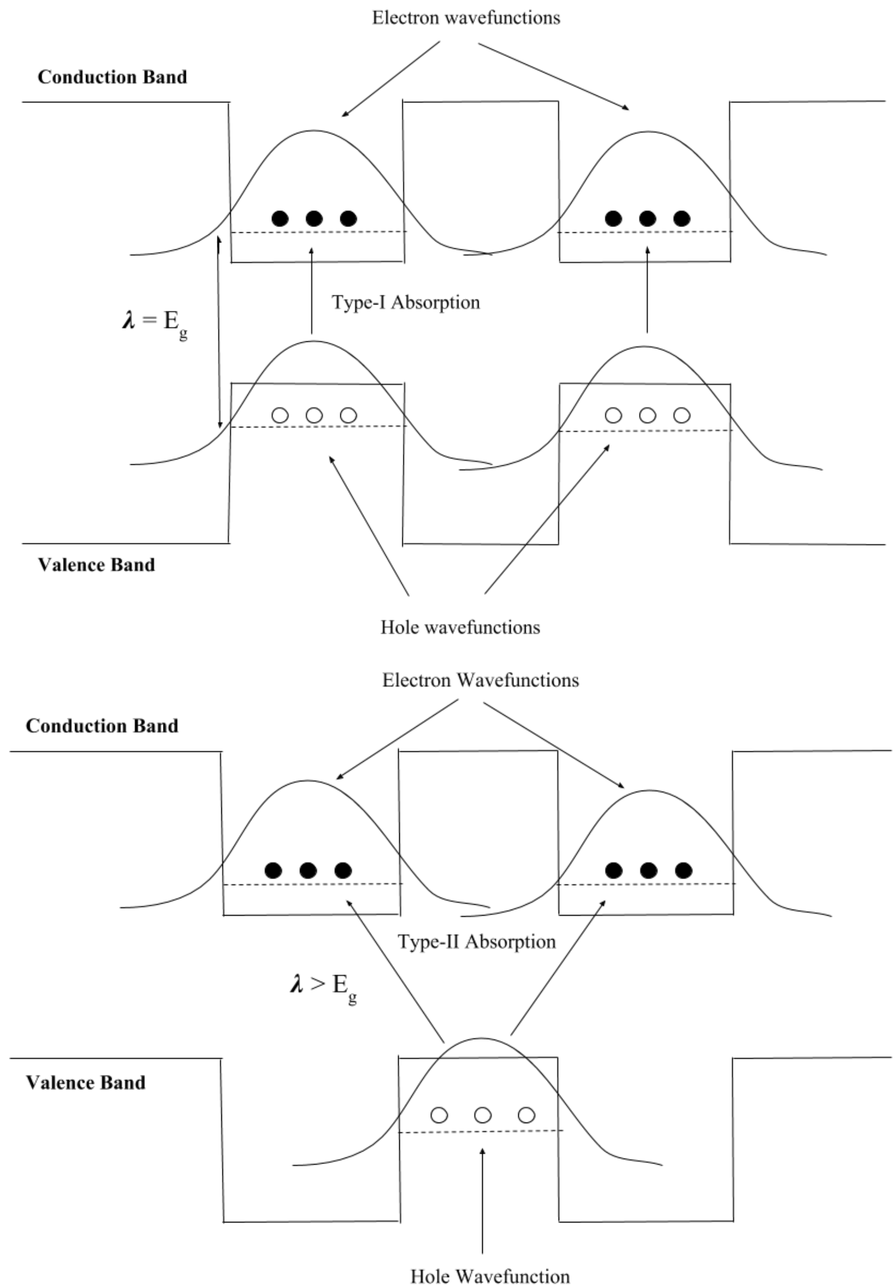


Fig. 3-4. (Top) Type-I absorption. Electron wavefunctions are illustrated directly above the hole wavefunctions. (Bottom) Type-II absorption. Electron wavefunctions are illustrated being diagonally above the hole wavefunctions.

Furthermore, the "spatially indirect" band offset in type-II InGaAs/GaAsSb quantum wells acts as an effective bandgap that is smaller than each individual material, so it is able to absorb light at longer wavelengths than that of either InGaAs or GaAsSb. The absorption of a specific wavelength of light made by this type-II transition is dependent on the wavefunction overlap between the electron wavefunction in the InGaAs well and the hole wavefunction in the GaAsSb well.

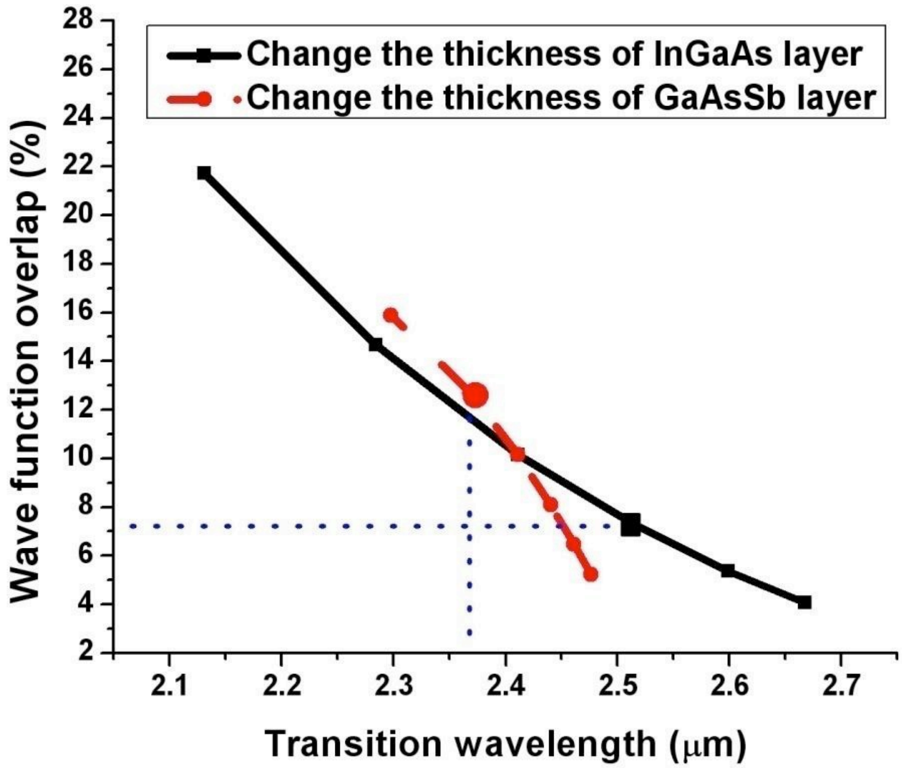


Fig. 3-5. Wavefunction overlap vs transition wavelength as a function of thickness of InGaAs and GaAsSb layers in type-II InGaAs/GaAsSb quantum wells [3-20].

With that said, there exists an inherent tradeoff between wavefunction overlap and cut-off wavelength of absorption. This trade-off can practically be seen in a simulation of wavefunction overlap versus transition wavelength in Fig. 3-5. With proper design, the wavefunction overlap can be properly optimized to maximize absorption at the wavelength desired by choosing the appropriate material thicknesses and compositions. Thinner wells produce a stronger wavefunction overlap between electrons and holes and higher absorption at the transition wavelengths, but at the price of a shorter cut-off wavelength.

The first to demonstrate an InP-based p-i-n photodiode with InGaAs/GaAsSb type-II quantum wells was Rubin Sidhu et. al [3-21]. A p-i-n photodiode with 150 pairs of InGaAs/GaAsSb quantum wells lattice-matched to InP was developed and demonstrated detection with a cut-off wavelength of 2.4 μm. Then, Baile Chen et. al. demonstrated an InGaAs/GaAsSb type-II quantum well photodiode with a cut-off wavelength as long as 3.6 μm [3-20]. Fig. 3-6 shows the spectral response of these photodiodes at different temperatures. These and other examples have shown clear viability of the InGaAs/GaAsSb type-II quantum wells for detection in the short to mid-wave infrared [3-35].

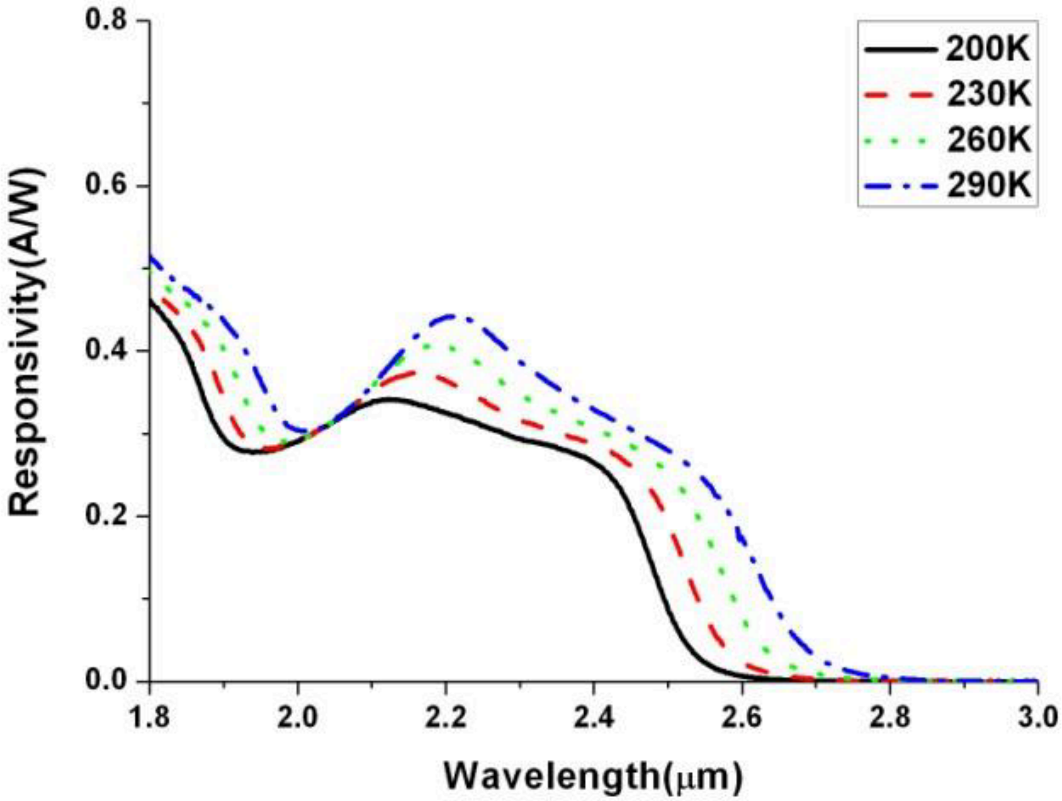


Fig. 3-6. Responsivity versus wavelength as a function of temperature for a p-i-n photodiode with 100 pairs of type-II 7nm $In_{0.53}Ga_{0.47}As$/5nm $GaAs_{0.5}Sb_{0.5}$ MQWs as absorption layer [3-20].

While these photodiodes demonstrated impressive DC performance such as low dark current and high responsivity, the device is not useful for optical communications links without the ability to detect a high-speed optically modulated signal. The thick MQW absorption region in the PDs provided a high responsivity, but, at the expense of slow frequency response. The next section covers the high-speed carrier dynamics of these devices. With a proper understanding of the underlying physics behind carrier transport within the device, a photodiode can be properly designed to detect high-speed optically modulated signals at 2 μm.

3.3 Carrier Escape and Transport Mechanisms

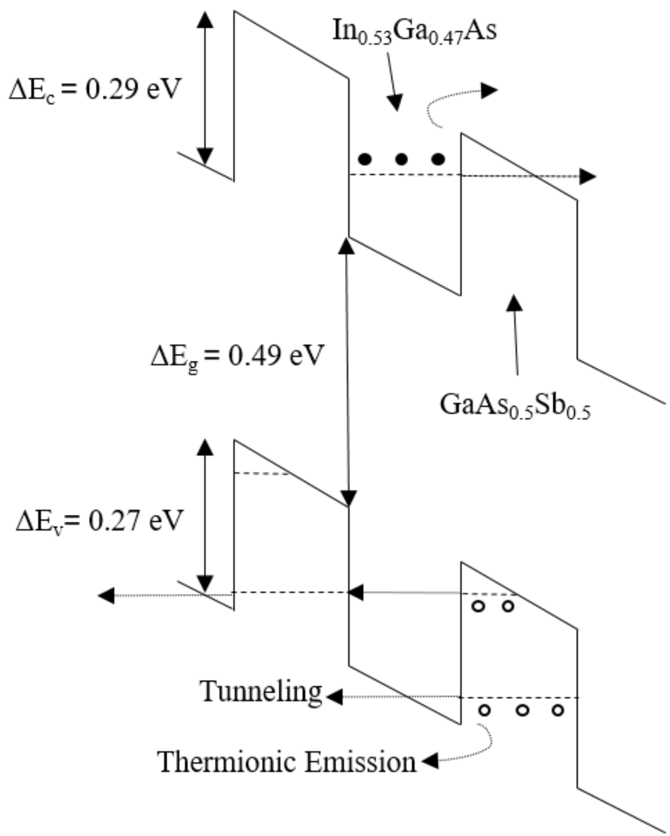


Fig. 3-7. Illustration of the carrier escape mechanisms in quantum wells.

In photodiodes with InGaAs/GaAsSb type-II quantum well absorption regions, the carrier transit time is typically limited by the time it takes for photogenerated carriers to be swept out of the MQWs under the influence of an applied electric field, as illustrated in Fig. 3-7. Generally, there are two primary physical mechanisms in which carriers escape from quantum wells: thermionic emission and phonon-assisted tunneling [3-24]. Thermionic emission is the escape of carriers with a carrier thermal energy higher than the effective barrier height. The thermionic emission time of carriers is given by [3-26]

$$\tau_{therm,i} = \sqrt{\frac{2\pi m_i L_w{}^2}{k_B T}} \exp\left[\frac{\Delta E_b(F)}{k_B T}\right] \quad (3\text{-}1)$$

where m_i stands for effective mass in the wells, L_w represents the well thickness, T is the temperature, k_B is the Boltzmann constant, the subscript i can be e for electrons, hh for heavy holes or lh for light holes, because the effective mass for electrons, heavy holes and light hole can differ [3-25]. $\Delta E_b(F)$ is the effective barrier height and can be expressed as

$$\Delta E_b(F) = E_\Gamma^{Barrier} - E_\Gamma^{Well} - \frac{qFL_w}{2} \tag{3-2}$$

and where F is the electric field, q is electron charge, and $E_\Gamma^{Barrier} - E_\Gamma^{Well}$ is the bulk band discontinuity between the well and barrier for electrons or holes. Tunneling is the escape of carriers through coherent, quantum mechanical tunneling of finite barriers and the time it takes for tunneling can be expressed as [3-25],

$$\tau_{tunnel,i} = \sqrt{\frac{2m_i L_w{}^2}{\pi\hbar}} \exp\left[\frac{2L_b\sqrt{2m_{bi}\Delta E_b(F)}}{\hbar}\right] \tag{3-3}$$

where L_b represents barrier thickness, m_{bi} stands for effective mass in barriers. This includes the tunneling of carriers out of a well into a neighboring well, and tunneling out of a well into continuum. Some carriers directly tunnel from quantum well to quantum well, with the assistance of a phonon, and can be trapped in the wells lower energy state before recombining through a localized defect, effectively reducing the collection efficiency of the device. However, we will only be considering tunneling of carriers into continuum as contributors to the photocurrent [3-22].

The total carrier transit time within the photodiode can be expressed as [3-25]

$$\tau_{transit,i} = n\left(\frac{1}{\tau_{therm,i}} + \frac{1}{\tau_{tunnel,i}}\right)^{-1} + \frac{n(L_w+L_b)+L_D}{v_i} \tag{3-4}$$

where n is the number of wells, L_D is the distance that an electron travels through the collection layer (L_D = 0 for holes), and v_i the carrier drift velocity in MQW layers. Photogenerated carriers average a certain period of time to escape thermionically and through tunneling. If one escape mechanism takes much longer than the other, then it will dominate the total escape time. Short escape times can be achieved by reducing the effective barrier height and thickness of the wells, as well as, the number of quantum wells in the absorber layer. After the carriers escape from the wells, then they drift through the rest of the well and barrier layers, and the collection layer before finally being collected.

In our case, we assume that only the ground well states of electrons and holes are populated by photogenerated carriers because we measure the photodiodes with small optical power illumination at the wavelength used for measurement. We assume that electron-hole pairs are uniformly generated in the absorption region and that once carriers escape from a quantum well they travel through the continuum until reaching the electrode [3-22]. Due to their large effective mass, heavy holes are extremely slow and take a long time to escape from the quantum wells and, therefore, are not considered to contribute to the photocurrent at high-frequencies. More specifically, the transit time of heavy holes is around 10 μs, which is comparable to the recombination time, so many of these carriers will recombine before they transit through the quantum wells to the electrodes and not contribute to the photocurrent, also reducing the collection efficiency of the device [3-25].

Electrons and light holes escape the wells at different rates due to their distinctive effective masses and bound energy levels within the wells. Electrons tunnel faster than light holes due to their smaller effective mass, however, light holes escape through thermionic emission at a faster rate because the effective energy barrier height of light holes is smaller than for electrons. The frequency response associated with the transit time of electrons or holes can be expressed as [3-23]

$$F_i(\omega) = \left| \frac{\sin\left(\frac{\omega \tau_{transit,i}}{2}\right)}{\frac{\omega \tau_{transit,i}}{2}} \right| \tag{3-5}$$

where ω is the angular frequency. The total transit-time-limited frequency response is determined by the sum of the contributions of electrons and holes. Fig. 3-8 shows how the transit-time-limited frequency response of electrons and holes, as well as the total transit-time-limited frequency response, of a type-II p-i-n photodiode would look like with holes that have a longer transit time than electrons. The plot in Fig. 3-8 was calculated using Mathcad, and the material parameters from Reference [3-20].

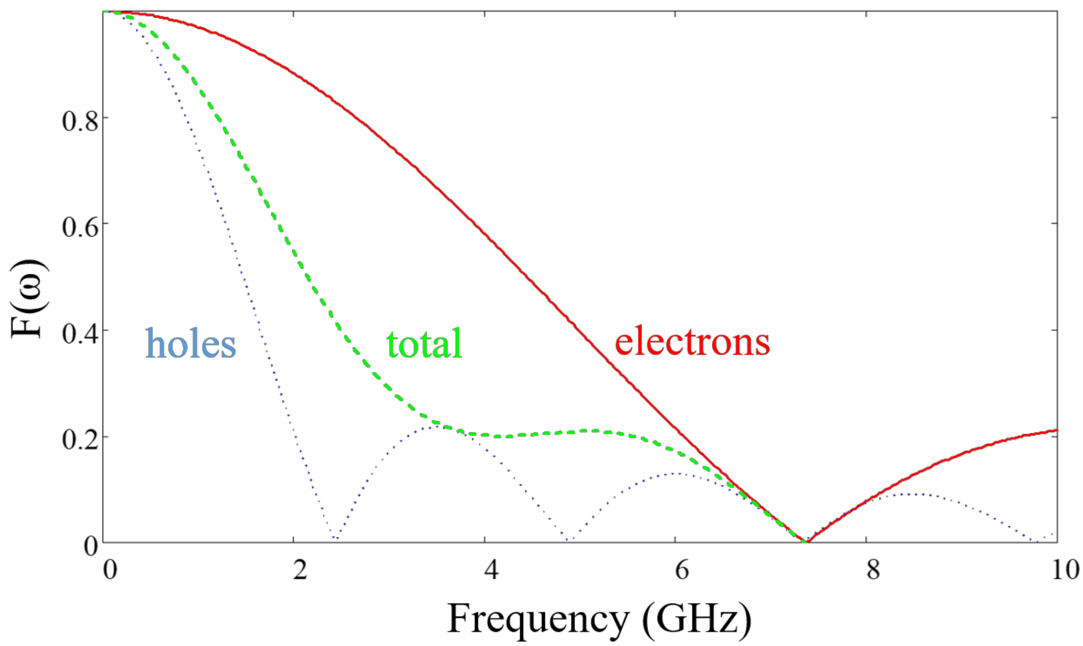


Fig. 3-8. Transit time limited frequency response of a type-II MQW p-i-n photodiode with eighty pairs of 7 nm thick $In_{0.53}Ga_{0.47}As$ and 5 nm thick $GaAs_{0.5}Sb_{0.5}$ type-II quantum wells.

The total frequency response of a p-i-n photodiode can then be expressed as [3-25]

$$H(\omega) = \frac{1}{1+\frac{j\omega\tau_{transit}}{3.5}} \frac{1}{1+j\omega(R_s+R_L)C_j} \tag{3-6}$$

where R_s is the series resistance of the photodiode, R_L is the external load resistance, and C_j is the junction capacitance of the photodiode. This is simply the product of the transit-time-limited transfer function and the RC-time-limited transfer function.

3.4 High-Speed InP-Based p-i-n Photodiodes With InGaAs/GaAsSb Type-II Quantum Wells

3.4.1 Device Design

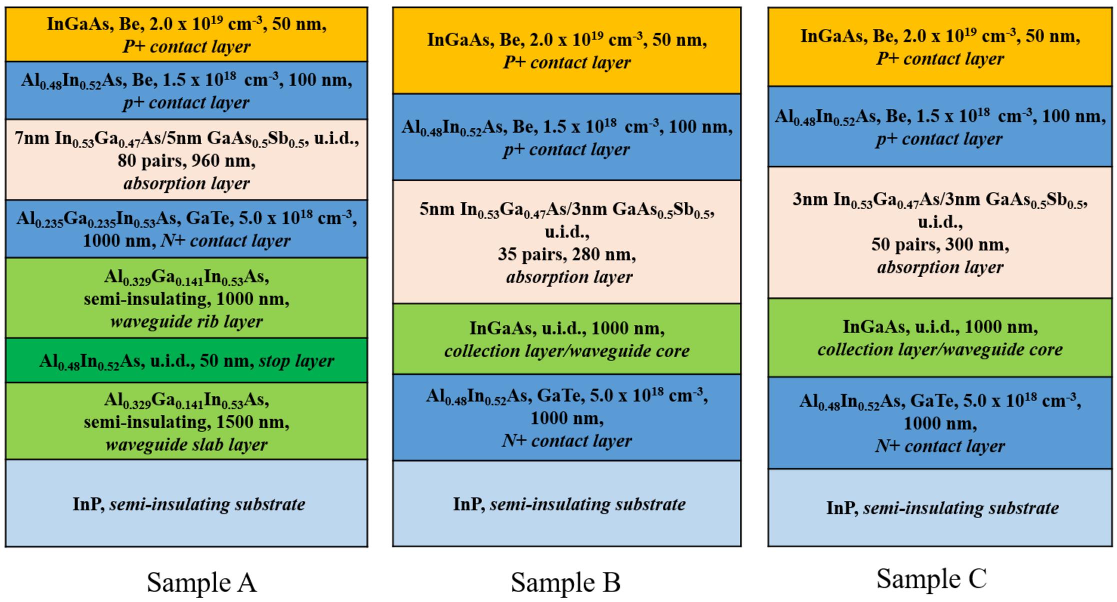


Fig. 3-9. InP-based type-II quantum well photodiodes structures in this study.

I designed three different photodiode structures that are shown in Fig. 3-9. Sample A is a p-i-n photodiode with an integrated rib waveguide on which eighty pairs of 7 nm-thick $In_{0.53}Ga_{0.47}As$ and 5 nm-thick $GaAs_{0.5}Sb_{0.5}$ type-II quantum wells were grown as the absorption layer of the device. Sample B includes 35 pairs of quantum wells with 5 nm-thick InGaAs well layers and 3 nm-thick GaAsSb barrier layers, and Sample C includes 50 pairs of quantum wells with 3 nm-thick InGaAs well layers and 3 nm-thick GaAsSb barrier layers. Samples B and C were designed with thinner quantum well and barrier layers than Sample A in order to increase the absorption efficient at 2 µm by enhancing the wave function overlap of electrons and holes, and, minimize the carrier escape time within the wells [3-22]. The band structure of the quantum wells and electron and hole wave functions were calculated using nextnano, a commercial device simulation software, and those within sample B are plotted in Fig. 3-10. One electron energy level exists in each InGaAs well, two heavy holes states and one light hole state exist in each GaAsSb hole well. In sample C, the InGaAs well is thinner than in Sample B leading to a shorter cut-off wavelength, as can be seen in the absorption coefficients shown in Fig. 3-11, which were calculated using the eight-band k-p method. More information on the software and code can be found in Appendix A.

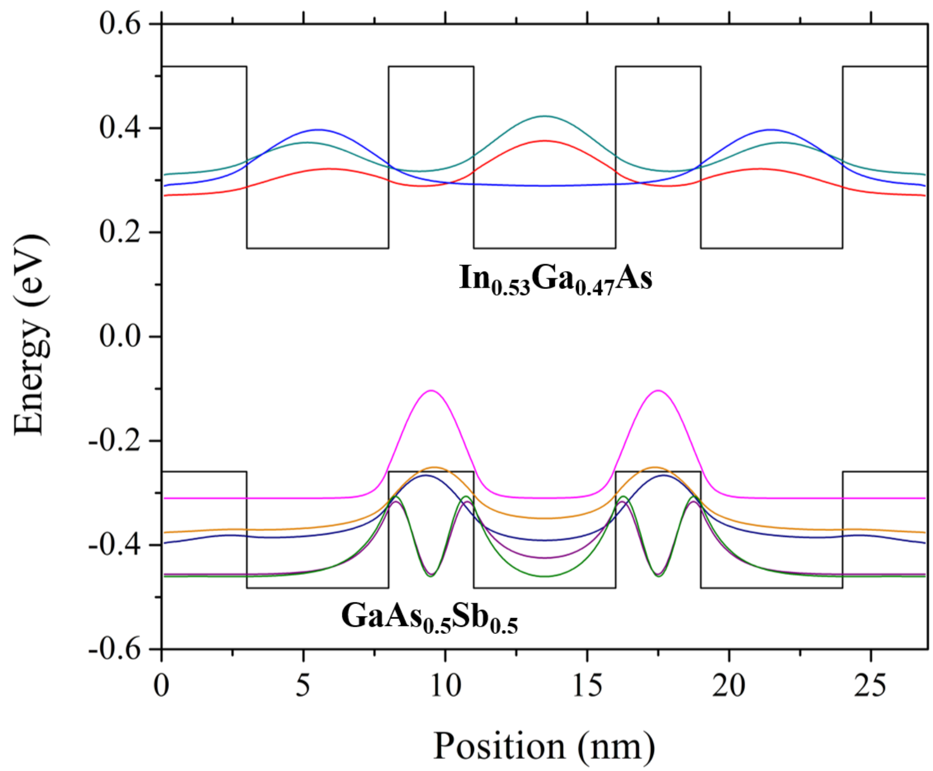


Fig. 3-10. Band structure and wave functions of Sample B. Green, red, and light blue curves represent electron wave functions of each well. Purple curve represents heavy hole wave functions. Orange and dark blue curves represent light hole wave functions in the ground state. Brown and green curves represent light hole wave functions in the second energy level.

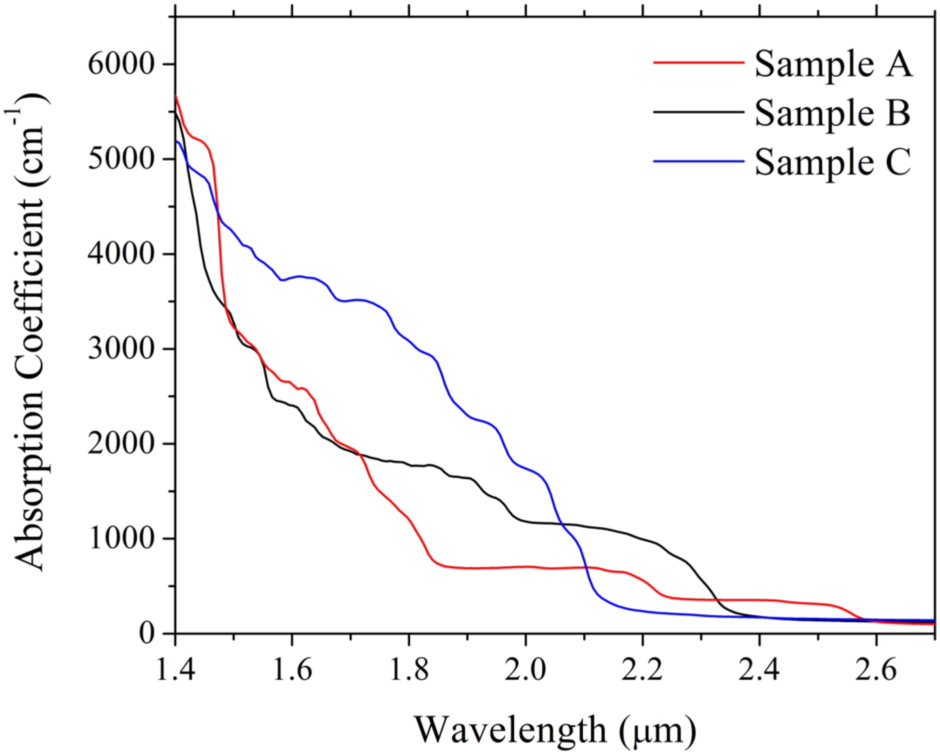


Fig. 3-11. Calculated absorption coefficients of samples A, B, and C.

In Sample A, the multiple quantum-well absorption layer is sandwiched in between highly doped n- and p- contact layers, which have lower indices of refraction in order to serve as optical cladding layers. A 150 nm top InGaAs p-contact layer was subsequently grown in order to reduce contact resistance. The absorber layer is of a higher index of refraction, and is designed to efficiently couple light at 2 μm into the multi-quantum well region. Beneath the n-contact layer, waveguide layers are grown in order to provide an optical interconnect between the photodiode, fibers, and other optical devices.

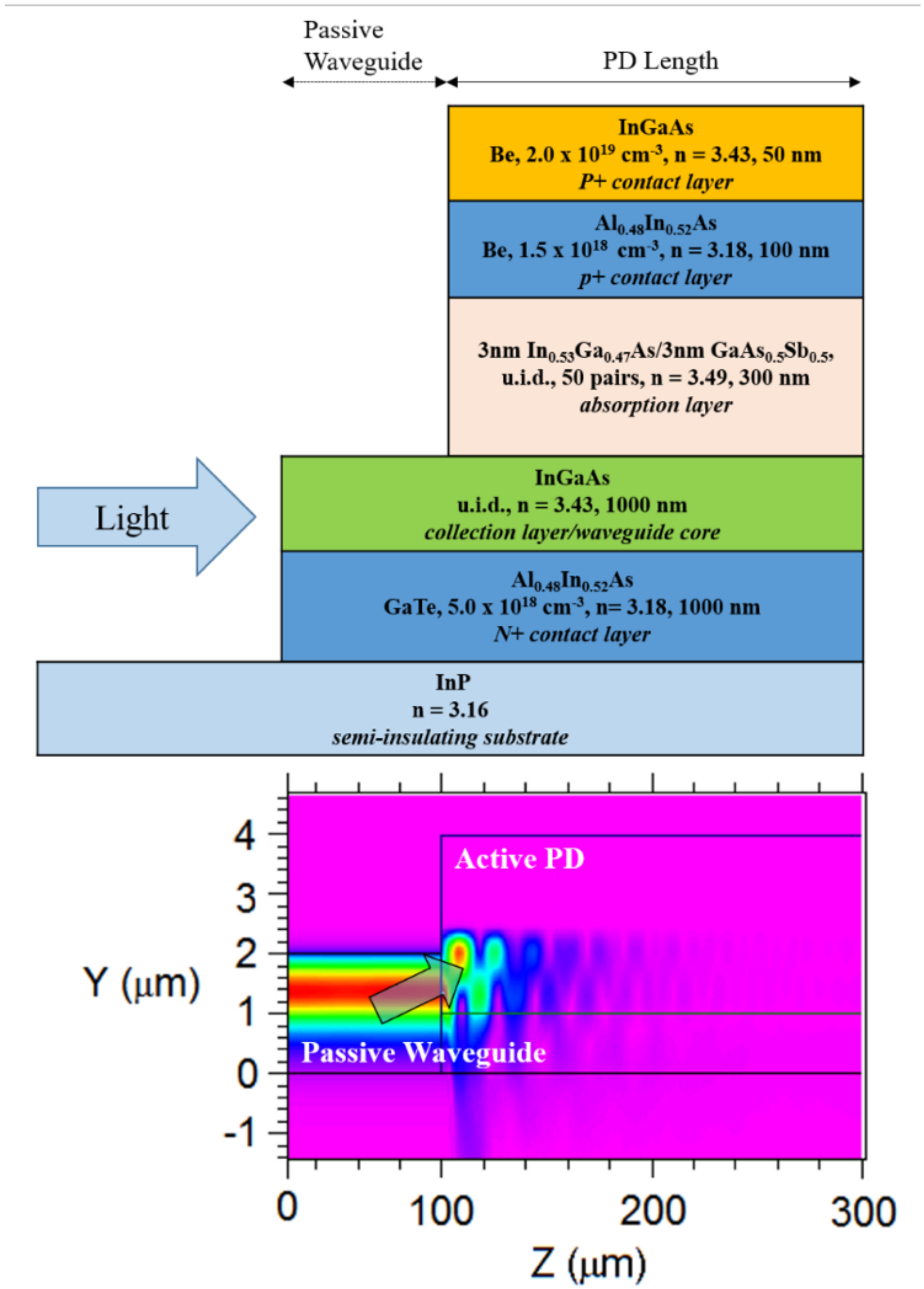


Fig. 3-12. Schematic cross-sectional view of the PD. The light is coupled from the left into the passive waveguide, which couples light into the MQW absorption layer of the photodiode.

Samples B and C are similar to a dual-depletion layer photodiode, with a depleted absorption layer consisting of MQWs and an optically transparent electron collection layer to minimize capacitance while simultaneously maintaining low carrier transit time [3-27], [3-28]. There are two important design changes in samples B and C: optimized quantum well/barrier thicknesses, and the addition of a novel dual-integrated waveguide-depletion layer, which consists of an electron collection layer simultaneously used as a passive waveguide core.

A schematic diagram of the dual-integrated waveguide-depletion layer is shown in Fig. 3-12. Light is fiber-coupled into the passive waveguide section and then guided into the active photodiode region, where it penetrates into the higher refractive index absorption layer. The light is absorbed, generating electron-hole pairs, with the relatively fast electrons then being swept through the collection layer. The n-contact layer is made of a lower index material than the waveguide core layer in order to confine the optical mode within the waveguide core. The InGaAs waveguide core was designed to achieve a balance between the optical confinement factor within the waveguide and coupling loss from an optical fiber. The simulated confinement factor was 0.87 and the coupling loss from a lensed fiber was estimated to be about 7 dB. Since only a small portion of the mode propagates in the n-contact layer, free carrier absorption associated losses in the waveguide are negligible (<2 dB/cm). This is in contrast to designs where a significant portion of the waveguide mode must propagate through the highly-doped contact region and potentially suffer from free-carrier absorption loss [3-7], [3-8].

3.4.2 Device Fabrication

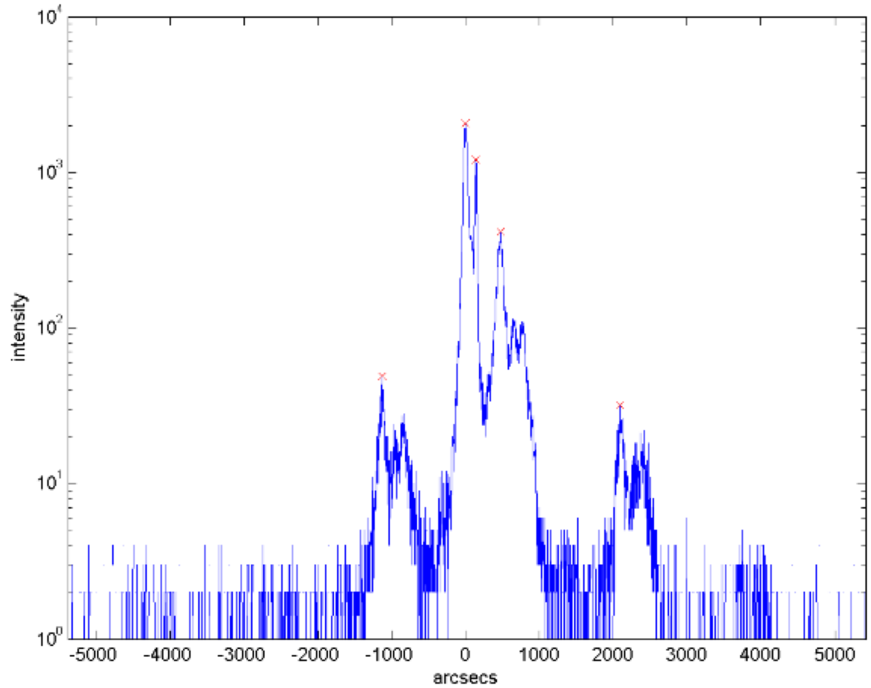


Fig. 3-13. Measured X-ray diffraction (XRD) pattern of the device wafer after growth.

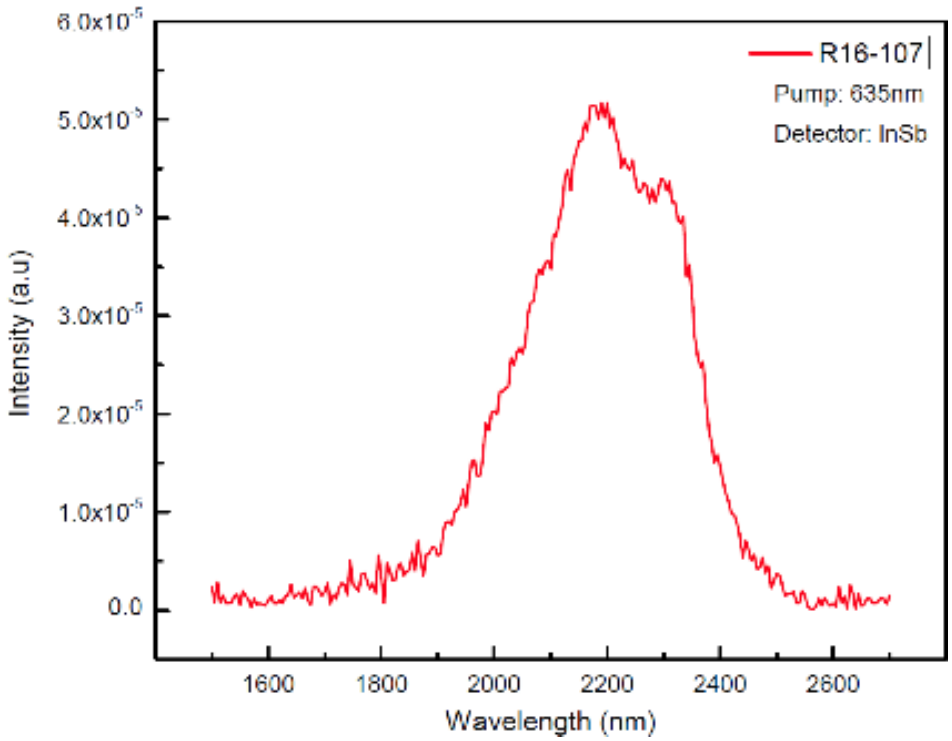


Fig. 3-14. Measured photoluminescence (PL) of the multiple quantum wells.

The photodiode structures described in Fig. 3-9 were grown by molecular beam epitaxy (MBE) on a semi-insulating InP substrate by Professor Balakrishnan's group at the University of New Mexico. In Fig. 3-13, an X-ray diffraction pattern (XRD) of the device wafer for Sample A was measured after growth, revealing the composition of the different layers grown. The peak absorption-edge wavelength of this structure has been measured in the past to be 2.2 μm, as shown in Figure 3-14.

Two different sets of photodiodes were fabricated; a top illuminated mesa structure, and an integrated waveguide double mesa structure. The device fabrication began with definition of different size active mesas using a MJB4 aligner. Standard contact lithography using a 320 nm source was used to define the mesas of the photodiode, which were passivated with SiO_2 using plasma enhanced chemical vapor deposition (PECVD). Ti/Pt/Au was deposited on top of the p-contact layer to provide an ohmic contact, followed by SiO_2 for surface passivation. Wet chemical etching was used to form circular mesas of different sizes for top illumination. Next, the mesas, along with 4 μm-wide, 1 μm-thick input rib waveguides on sample A, and 5 μm-wide, 500 nm thick input rib waveguides on samples B and C, along with double rectangular mesa photodiodes on a separate sample, were etched with an Oxford Instruments Plasmalab-100 chlorine based ICP dry etching machine down to the semi-insulating substrate. Then, Au/AuGe/Pt/Ni was deposited on the n-mesa to provide an ohmic contact, followed by SU-8 as an insulation layer for coplanar waveguide (CPW) probe pads, which act as an RF interface. Finally, a seed layer of Ti/Au was deposited and then electroplated to connect the CPW to the metal contacts. The completed device is shown in Fig. 3-15.

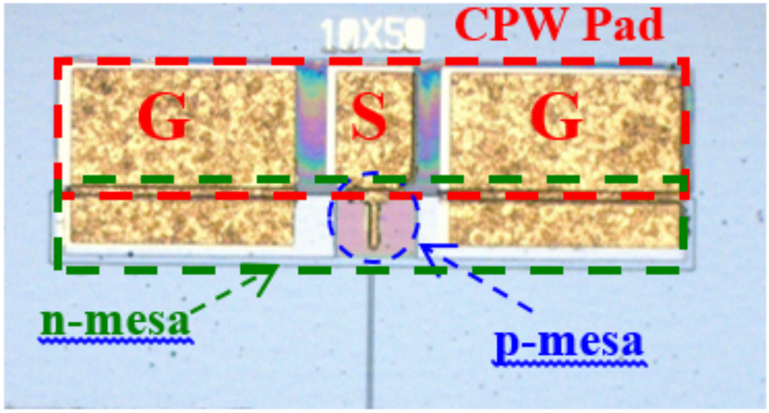


Fig. 3-15. Fabricated photodiode with RF pads integrated.

3.4.3 Results and Discussion

3.4.3.1 DC Measurements and Analysis

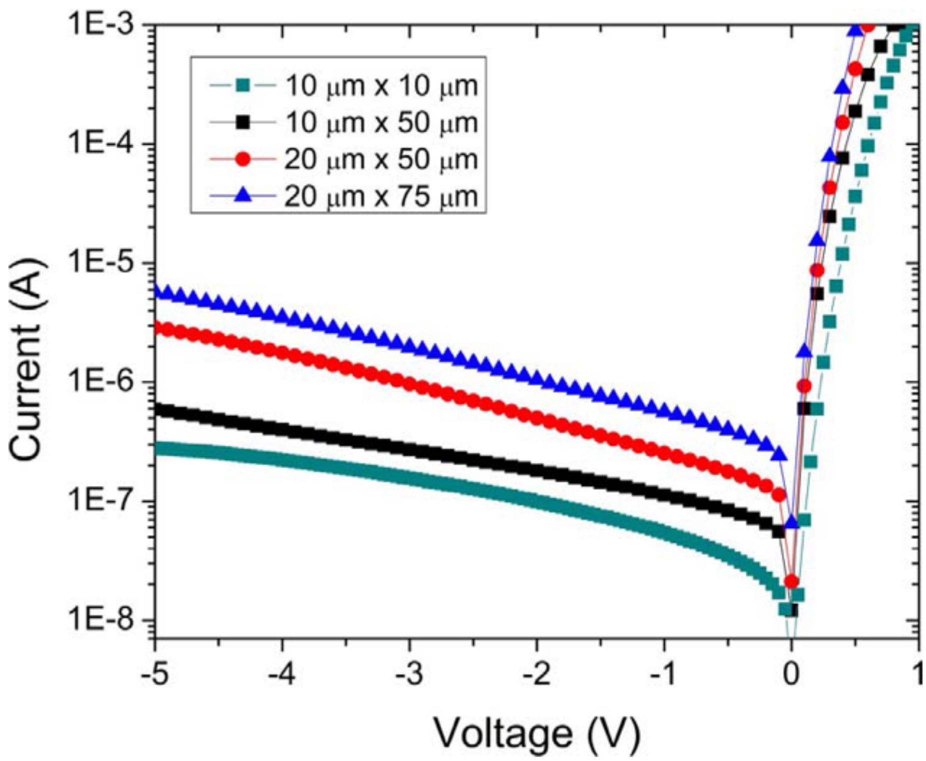


Fig. 3-16. I-V curves measured at room temperature under dark condition of a 10 μm × 10 μm, 10 μm × 50 μm, 20 μm × 50 μm, and 20 μm × 75 μm photodiode (sample A).

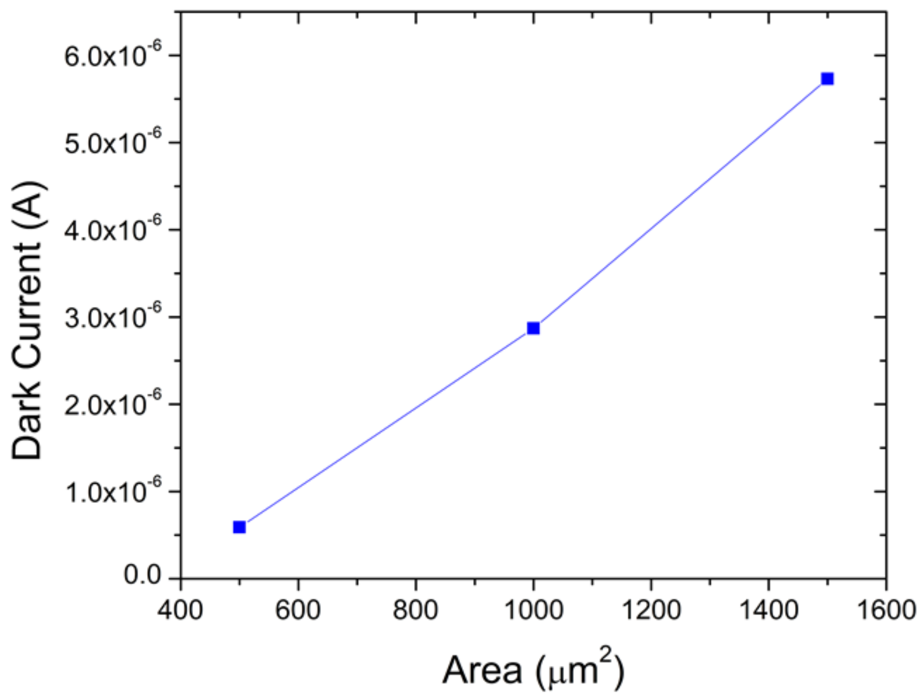


Fig. 3-17. Dark current of photodiodes from sample A versus area at a voltage bias of -2 V.

I-V curves were measured for different photodiode sizes on sample A as shown in Fig. 3-16. The dark current was measured to be less than 100 nA at −2V at room temperature for a 10 μm × 10 μm photodiode. Dark current of PDs on sample A scale linearly with device area, relaying that the current leakage origins from the bulk of the device, as displayed in Fig. 3-17. Due to fluctuations in the aluminum growth rate during molecular beam epitaxy (MBE) transfer, the waveguide layers were grown slightly lattice mismatched to the InP substrate, causing the formation of defects. Because the MQW absorber layer was grown close to the critical layer thickness, threading misfit dislocations propagated through the bulk of the device, and contribute to deep-level defects within the device. This is evident by the wide FWHM of the peaks measured in the XRD graph shown in Figure 3-13, which could potentially be pointing towards multiple Al-compositions very close to each other within the AlGaInAs layers causing defects. With a higher crystal quality and better lattice matching, the defect density can be lowered and the dark current of the device can be further reduced [3-29].

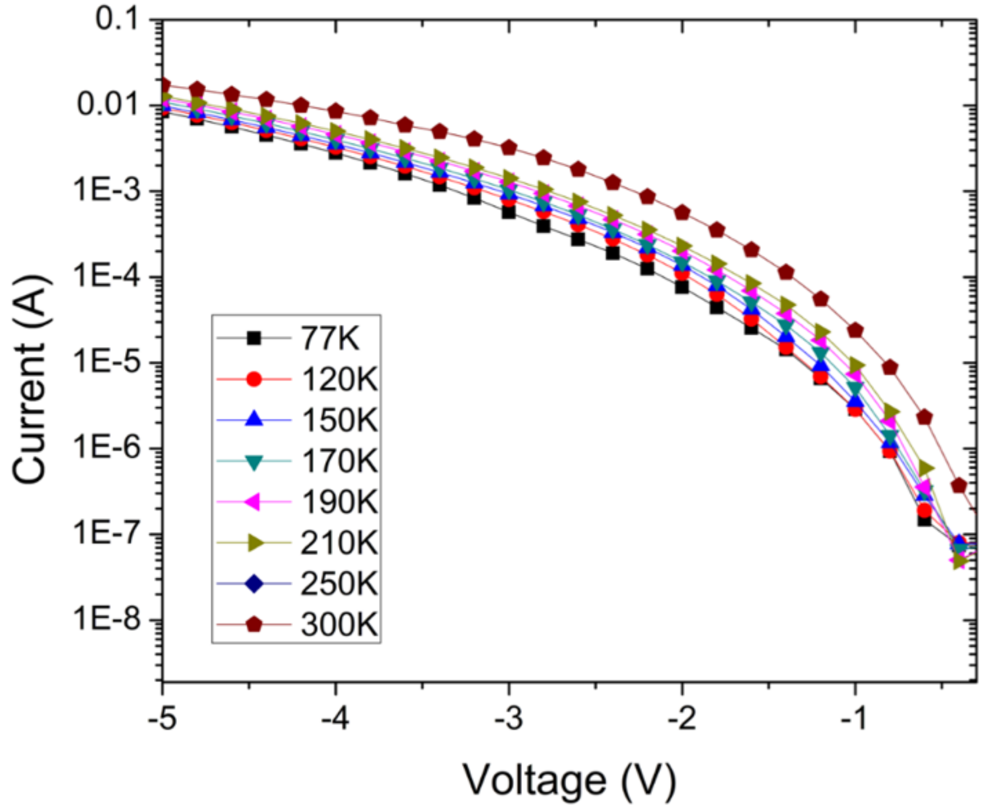


Fig. 3-18. Dark current of a 250 µm diameter photodiode at different temperatures (sample A).

Dark current was measured with variation in temperature (Fig. 3-18) using a Lakeshore cryogenic probe station cooled to 77 K with liquid nitrogen in order to further study the dominant current mechanisms. Below a bias voltage of 1 V, a large change in dark current is observed with increasing temperature, indicating the current in the device can be attributed mostly to thermal generation and recombination of carriers. Above 1 V, the dark current sees a smaller change with increasing temperature, indicating that thermally-independent trap-assisted tunneling of carriers through the quantum well barriers dominates as the main source of current. Trap-assisted tunneling begins to dominate the dark current at a moderately low bias voltage because it is linearly dependent on defect density, which is sufficiently high in these devices [3-30].

The dark current of these devices from Samples B and C were measured to be linearly dependent on the diameter of the mesa, suggesting that they are dominated by surface leakage. The dark currents of 10 μm × 50 μm devices fabricated from the three samples are shown in Fig. 3-19. Samples B and C show significant improvement in dark current due to their thinner MQW absorption regions and improved crystal quality.

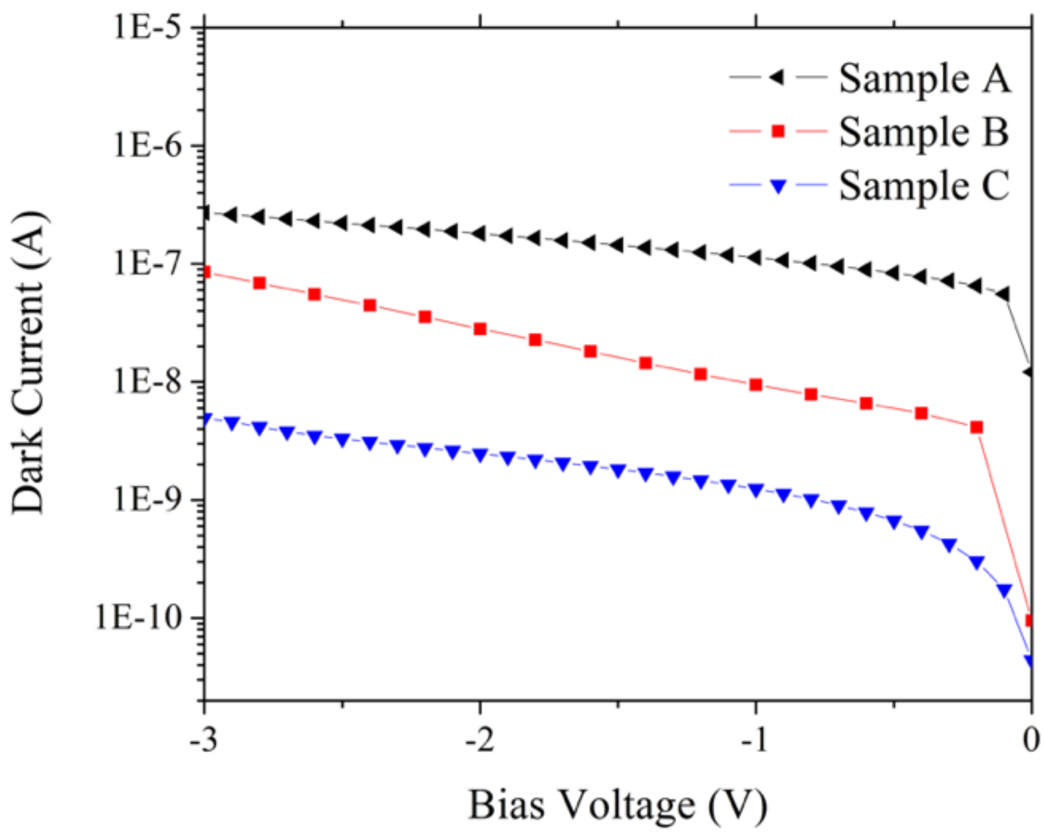


Fig. 3-19. Measured dark currents of 10 μm × 50 μm PDs fabricated from samples A, B, and C versus reverse bias.

In Fig. 3-20, it can be seen that the capacitance of a 100 μm diameter photodiode from sample A is about 0.62 pF, and Fig. 3-21 shows the capacitance versus area of photodiodes from sample A. This value agrees with the calculated capacitance using the parallel plate model described in Equation 2-5. The photodiode becomes fully depleted at about -2 V. The capacitance still decreases slightly with voltage as more charges in the contact regions are depleted and the depletion region widens. Due to this increase in depletion region width, more carriers are generated thermally or optically within the photodiode, and the current increases.

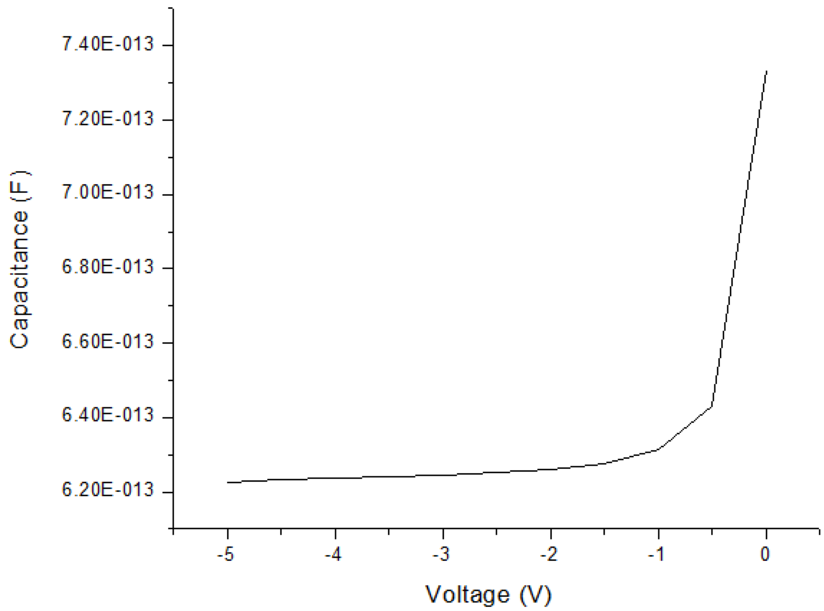


Fig. 3-20. Capacitance versus bias voltage for a 10 µm x 10 µm photodiode from sample A.

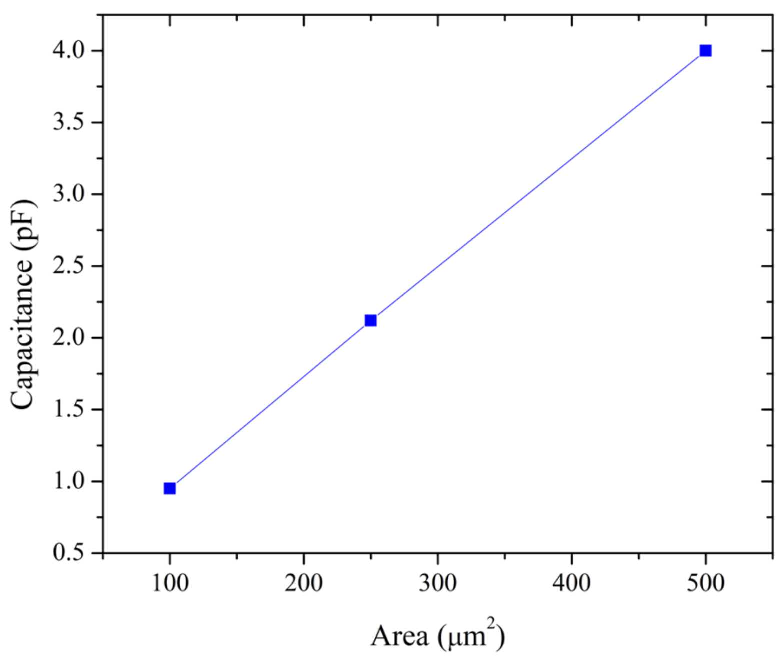


Fig. 3-21. Capacitance versus area of photodiodes of different areas made from sample C.

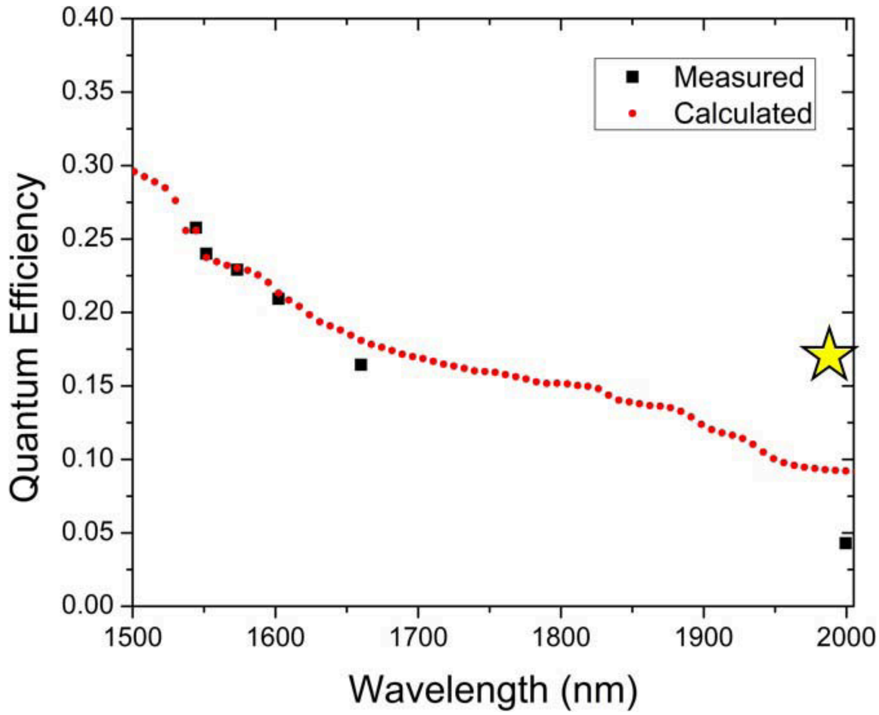


Fig. 3-22. Simulated and measured quantum efficiency of a 500 μm diameter top-illuminated PD as a function of input wavelength. The yellow star represents the measured quantum efficiency for a 200 μm length integrated waveguide photodiode made from sample A.

Top-illuminated photodiodes of sample A with a diameter of 250 μm and anti-reflection coating for 1.55 μm were measured and showed an external responsivity of 0.3 A/W at 1.55 μm and 0.05 A/W at 2 μm. Fig. 3-22 shows the calculated quantum efficiency (QE) of a top-illuminated photodiode, assuming that each photon contributes one electron-hole pair, as well as, the measured QE of a top-illuminated photodiode biased at −5 V as a function of input wavelength. The absorption coefficient used in the calculations is 1000 cm^{-1} at 2 μm and 3000 cm^{-1} at 1.55 μm [3-31]. These numbers were used before the commercial simulation tool, nextnano, was available to use during this study.

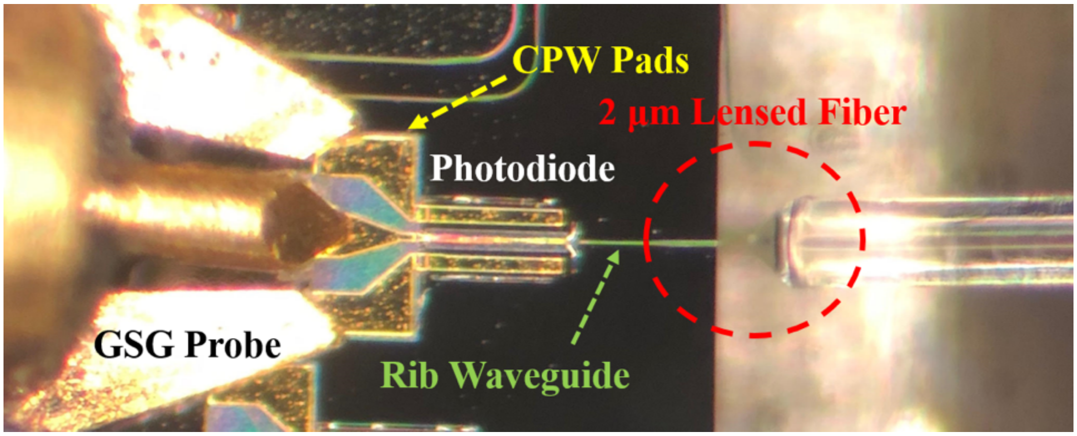


Fig. 3-23. Fabricated photodiode being measured with a microwave ground signal-ground (GSG) probe and optically illuminated by a 2 μm laser through a lensed fiber.

Integrated waveguide photodiodes were also measured, as shown in Fig. 3-23. Fig. 3-24 shows the simulated quantum efficiency of the integrated waveguide photodiode as a function of photodiode length in the ideal case that each photon contributes one electron-hole pair to the photocurrent. The optical simulations which were done in RSoft, a commercial beam propagation software. For a PD length of 400 μm, nearly all of the light at 2 μm is absorbed, relating that theoretically all of the light can be absorbed within a device that is made long enough. Furthermore, the coupling between the waveguide and the device was optimized for 2 μm. For a 20 μm × 100 μm device measured under 7 V reverse bias at room temperature, the external responsivity is 0.15 A/W at 2 μm and 0.23 A/W at 1.55 μm. For a 20 μm × 200 μm waveguide photodiode under 7 V reverse bias measured at room temperature, the external responsivity is 0.27 A/W at 2 μm, which, after excluding 3.5 dB total loss from fiber coupling and reflection at the waveguide facet, corresponds to an internal responsivity of 0.6 A/W. The measured responsivity increases with increasing photodiode length, as predicted in our simulations. We also observe a voltage-dependent responsivity in the PDs as shown in Fig. 3-25. With increasing DC bias, the carrier collection efficiency increases as more carriers have enough energy to escape out of the quantum wells and transit through the absorber to the contacts before recombining. Also, the depletion region of the device widens with bias, also resulting in higher collection of carriers.

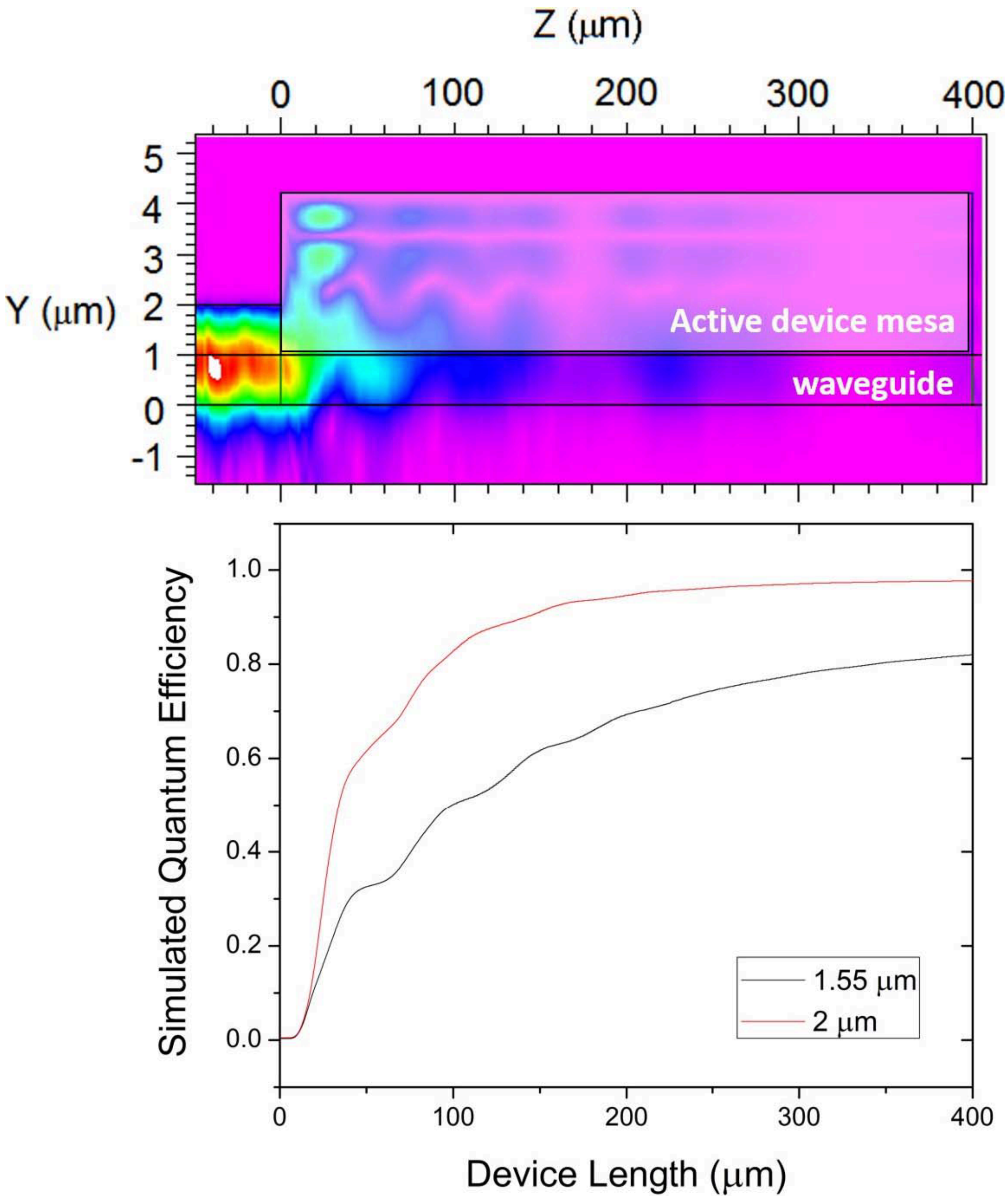


Fig. 3-24. (Top) Optical beam propagation simulations of an evanescently coupled waveguide integrated photodiode from sample A. (Bottom) Simulated internal quantum efficiency as a function of PD length (sample A).

For a 20 µm × 100 µm device on sample A measured under 7 V reverse bias at room temperature, the external responsivity is 0.15 A/W at 2 µm and 0.23 A/W at 1.55 µm. For a 20 µm × 200 µm waveguide photodiode on sample A under 7 V reverse bias measured at room temperature, the external responsivity is 0.27 A/W at 2 µm. The measured responsivity increases with increasing photodiode length, as predicted in our simulations.

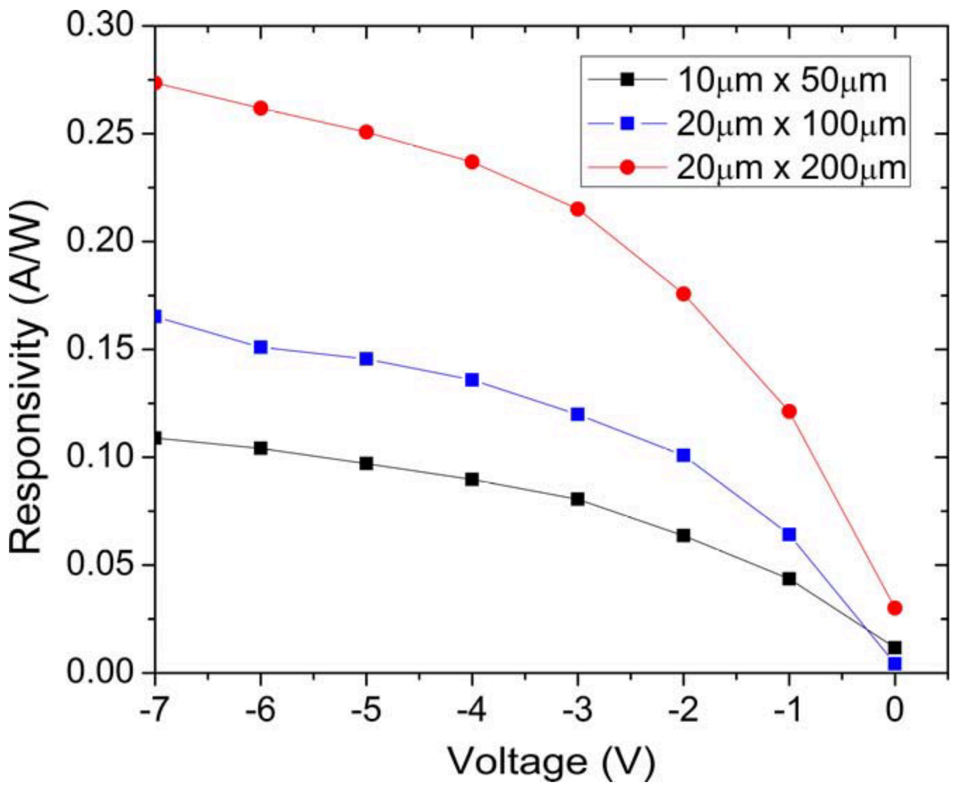


Fig. 3-25. Measured responsivity as a function of voltage at 2 µm wavelength for PDs with different active areas.

The simulated and measured internal maximum responsivity of devices fabricated from all samples are plotted in Fig. 3-26. For a 20 µm × 200 µm device, the maximum internal responsivity observed at 2 µm was 0.6 A/W for sample A, 0.81 A/W for sample B, and 0.84 A/W for sample C. The absorption coefficients from Fig. 3-11 were used in the optical simulations. In order to calculate the internal quantum efficiency from the measured quantum efficiency, we factored in the following loss mechanisms: fiber-chip coupling loss and reflection loss at the waveguide facet, as well as, free-carrier absorption in the waveguide, and carrier collection efficiency within the PD. Losses due to coupling and reflection were calculated to be 3.5 dB for sample A and 7 dB for samples B and C. Reflection losses can be mitigated by adding anti-reflection coating at the edge of the waveguide. The larger fiber coupling loss in devices made from samples B and C are due to a thin input waveguide thickness and can be improved with the integration of a spot-size converter [3-32]. The carrier collection efficiency of the PDs is limited by trapped carriers which recombine in the wells before reaching the contacts and is calculated to be 45% for Sample A and 55% for Samples B and C. These numbers were extracted from comparing top-illuminated responsivity measurements with calculations made using equations (2. 1)-(2.3).

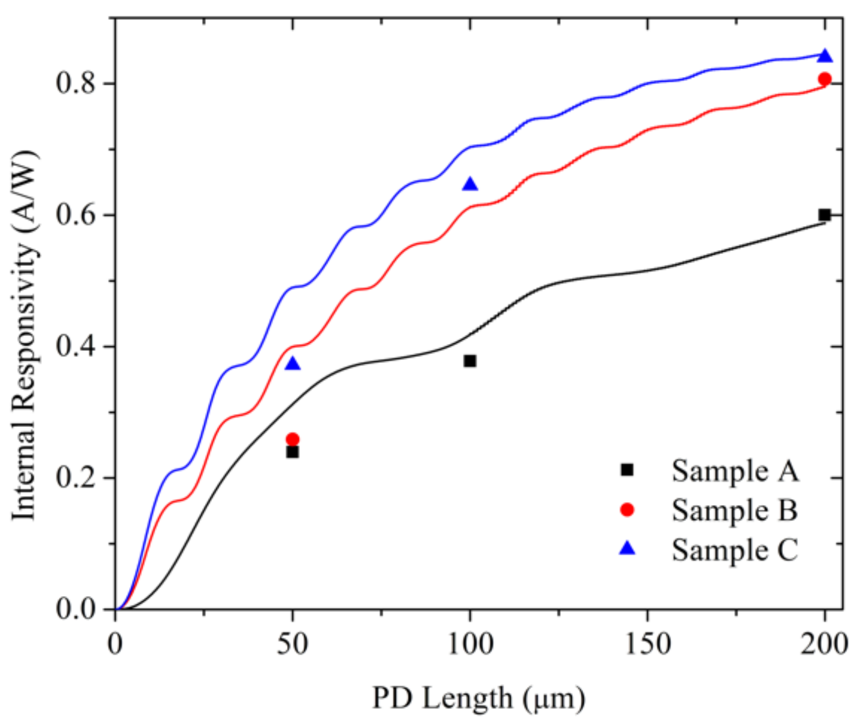


Fig. 3-26. Internal responsivity at 2 μm wavelength versus PD length. Solid curves represent simulated data and markers represent measured data at -5 V.

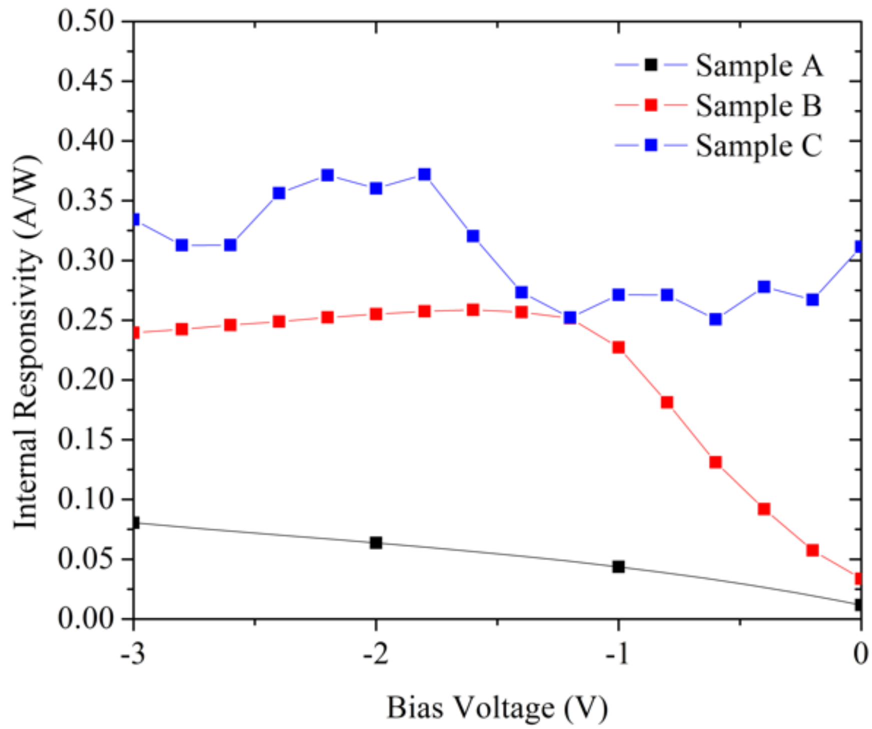


Fig. 3-27. Internal responsivity of 10 µm × 50 µm PDs fabricated from samples A, B, and C versus reverse bias.

The measured responsivity increases with increasing photodiode length, as predicted in our optical simulations. Optical mode beating occurs within the PDs and was optimized in the design of the PDs of samples B and C. In PDs made from sample A, the optical mode must couple through the n-contact layer before reaching the MQW absorption region. In contrast, when using the dual-integrated waveguide-depletion layer design, the optical mode is confined in the waveguide-depletion layer, and then coupled into the directly adjacent MQW absorption region within a shorter distance, enabling smaller devices and lower capacitances at a given responsivity. This can be seen in the rapid increase in internal responsivity of PDs made from samples B and C within the first 20 µm of the PD length, as shown in Fig. 3-26. Even though the PDs fabricated from samples B and C have thinner absorption layers, they achieve a higher internal responsivity than the PDs made from sample A due to the implementation of the dual-integrated waveguide-depletion layer and the increase in absorption coefficient. Furthermore, PDs made from sample C absorb more light at 2 μm than those made from sample B because they have a higher absorption coefficient and more quantum wells in the MQW absorption layer [3-22].

Fig. 3-27 also shows the internal responsivity of 10 μm × 50 μm PDs fabricated from samples A, B, and C versus reverse bias. The responsivity initally increases with applied bias voltage because the depletion region widens and absorbs more light. As a larger bias is applied, the electron and hole wavefunction overlap between the wells increases, which causes an increase of type-II absorption within the device.

3.4.3.2 High-Speed Measurements and Analysis

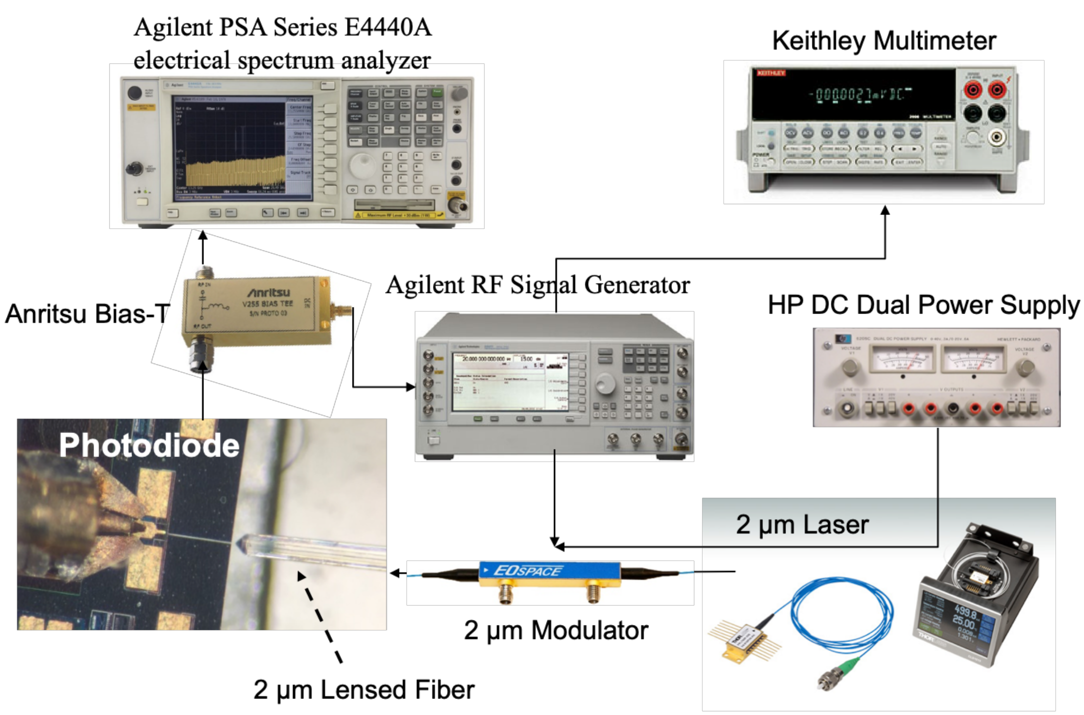


Fig. 3-28. Experiment set-up schematic diagram for frequency response measurements.

To measure the frequency response of the PDs, I used a 2 μm wavelength E-O Space intensity modulator with a 10 GHz bandwidth to modulate a CW optical signal and an Agilent PSA Series E4440A electrical spectrum analyzer to measure the output RF power of the PDs, as shown in the setup schematic in Fig. 3-

28. The measurements revealed a maximum 3-dB bandwidth of 3.5 GHz for a 10 µm × 50 µm PD made from sample A, 4.5 GHz for a 10 µm × 50 µm PD made from Sample B and above 10 GHz for a 10 µm × 50 µm PD made from sample C at -3 V bias with 1.1 mW optical input power (Fig. 3-29 and Fig. 3-30). For a 10 µm × 50 µm PD from sample A, R_s is 33 Ω (extracted from the forward current in the I-V curves from Fig. 3-16) and C_j is 0.1 pF, meaning that the RC-limited 3-dB bandwidth is around 19 GHz, suggesting that the PDs are transit-time limited. PDs from sample B are also transit-time limited, as they are well below the RC-limited bandwidth. However, PDs from sample C are RC-limited as the transit time limited bandwidth is calculated to be 37 GHz, which is nearly double the RC-limited bandwidth. Furthermore, the maximum 3-dB bandwidth of PDs made on sample C can be increased in the future by designing and fabricating smaller active area devices.

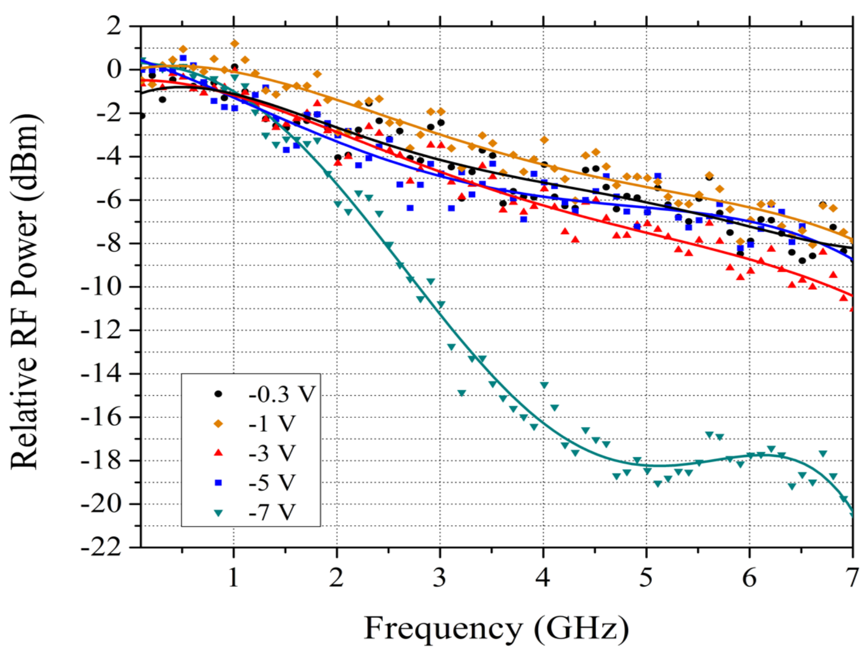


Fig. 3-29. Frequency responses of a 10 µm × 50 µm PD fabricated from sample A under different bias voltages at an average photocurrent of 530 µA. Lines represent averaged data points.

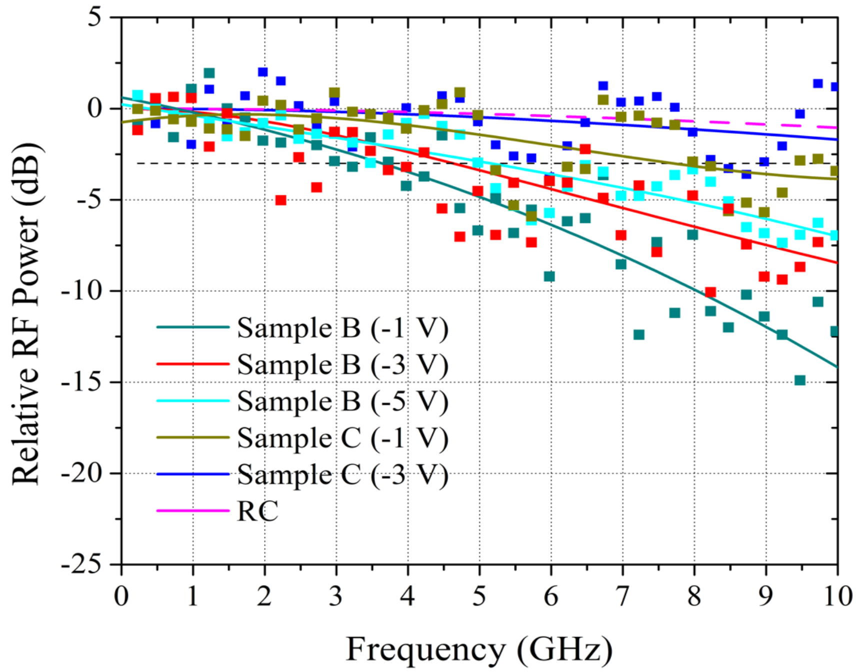


Fig. 3-30. Measured frequency responses of 10 μm × 50 μm PDs fabricated from sample B and C at different bias voltages with 1.1 mW of optical input power. The dots represent measured data and the curves represent calculate data (Eq. (6)) and the RC-limited bandwidth of a 10 μm × 50 μm PD.

We also consider the dependence of an applied electric field across the MQW region [3-31]. These effects can be observed in the bandwidth measurements taken of a 10 μm × 50 μm PD made from Sample A shown in Fig. 3-29. At −7 V, the bandwidth decreased from a maximum of 3.5 GHz (at −1 V) to 2.2 GHz. The bandwidth of these devices vary with applied bias, as the escape time of photogenerated electrons and holes in the wells vary. Light holes transit through the depletion region slower than electrons and limit the carrier transit time at high-frequencies. Therefore, two frequency roll-offs exist, one at low-frequency for light holes, and another one at high-frequency for electrons. The bandwidth in these PDs are lower than the PDs made from Samples B and C because the bound electron and hole energy levels are lower and the effective barrier heights are larger, leading to longer carrier escape times. At low biases, carrier escape is dominated by thermionic emission of carriers above the barriers. Tunneling processes are suppressed due to the heavy effective masses of the electrons and holes. At high biases, carriers escape through the combination of thermionic emission and tunneling [3-33]. With a high applied electric field, the ground state energy levels of electrons and holes are lowered towards the bottom triangular section of the well [3-34]. We see a corresponding decrease in bandwidth with an increase in bias associated with the ground electron and hole energy levels lowering, resulting in longer carrier escape times. At a high enough applied electric field, the energy level will begin to rise again, and the carrier escape time will decrease, increasing the total bandwidth of the PD. This effect can be visualized in Fig. 3-31, which shows the change in the ground state energy level position within a quantum well with a change in applied electric field.

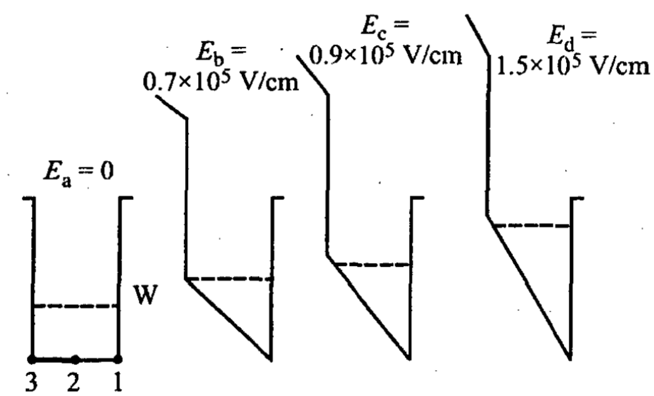


Fig. 3-31. Ground state energy level positon in a quantum well as a function of applied electric field [3-34].

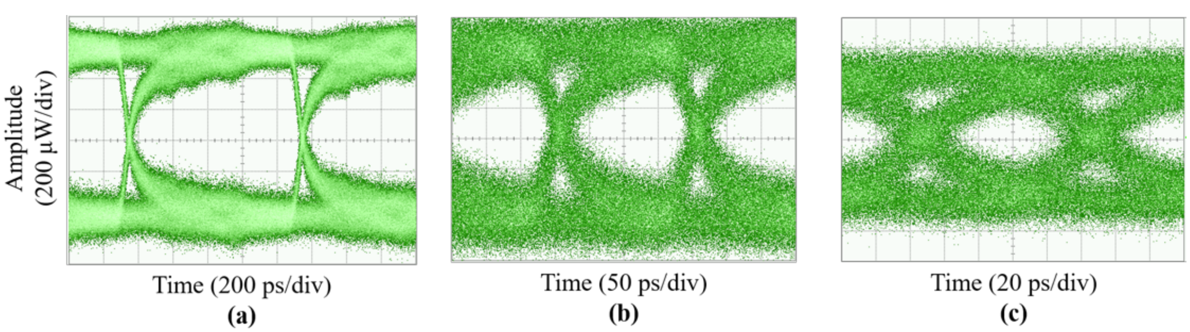


Fig. 3-32. Measured NRZ 16 bit eye pattern at (a) 1 Gb/s, (b) 5 Gb/s, and (c) 10 Gb/s at 2 μm wavelength by a 10 μm × 50 μm PD photodiode made on Sample C biased at −8 V.

Fig. 3-32 shows electrical eye diagrams of a 10 μm × 50 μm PD made from sample C biased at -8 V and operating at 1, 5, and 10 Gbit/s. The non-return-to-zero (NRZ) bit pattern was generated by an Advantest D3186 Pulse Pattern Generator and connected to a RF signal generator and a 2 μm E-O space modulator with 10 GHz bandwidth, which modulates the incoming 3.5-dBm optical signal coming from a Thorlabs 2 μm Fabry-Perot laser diode that, subsequently, generates an optical eye bit pattern that is coupled into the photodiode. After probing the photodiode with a GGB high-speed GSG probe, the output of the PD was amplified by a RF amplifier (Gain = 30 dB, Saturation power = 20 dBm, Bandwidth = 40 GHz, Noise Figure = 6 dB) before electrical eye diagrams were measured using an Agilent Infiniium DCAJ 86100C sampling oscilloscope. A schematic of the experimental setup is shown in Fig. 3-33.

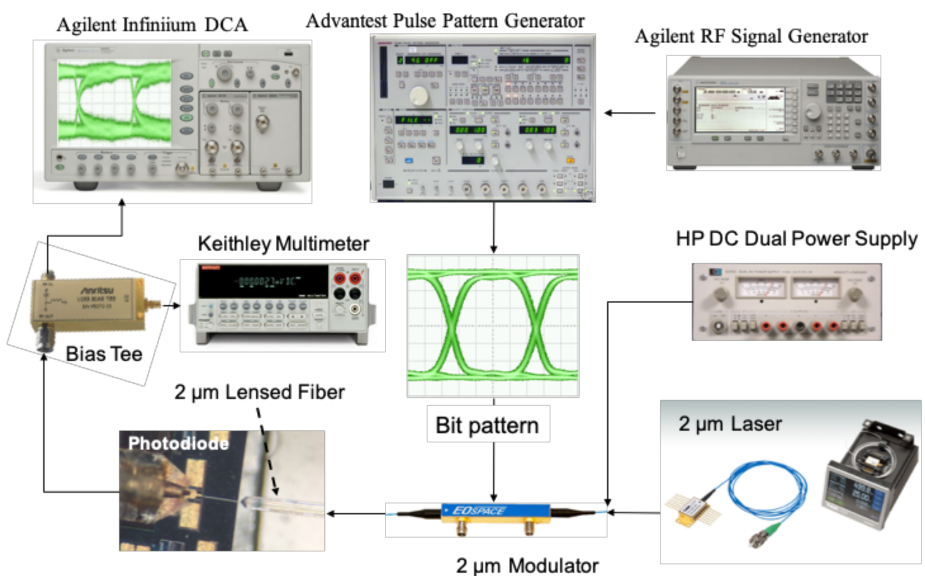


Fig. 3-33. Experiment set-up schematic diagram for eye diagram measurements without amplifier included.

Significant improvement of the eye opening at 10 Gb/s can be expected by calibrating out the losses coming from the RF cables and the optical modulator, and by switching to a low noise amplifier (LNA). Furthermore, with implementation of advanced forward error correction (FEC) coding techniques, we expect that these devices can be used practically at 10 Gbit/s in a 2 μm optical communications system.

Chapter 4 - Ultra-low capacitance MUTC waveguide photodiodes at 1550 nm

4.1 Introduction

High-speed, energy-efficient photodiodes are key components in low-power optical receivers for data communication and processing. According to Miller [4-1], reducing the photodiode capacitance can help enable a ‘receiverless’ system, meaning there is no need for a transimpedance amplifier (TIA) following the photodiode. Because the photodiode capacitance is sufficiently small, the self-induced electric field caused by photogenerated carriers will create a strong enough voltage swing to drive a load CMOS gate with the incorporation of a high load resistor [4-2]. This not only simplifies the system, but reduces the energy consumption per bit of an optical receiver over a hundred fold. We propose to use a modified uni-traveling carrier waveguide photodiode incorporating a novel dual-integrated collection layer-waveguide design, as shown in Figure 4-1, to develop a high-speed integrated waveguide photodiode with low capacitance for energy-efficient optical interconnects.

4.2 Device Design

In selecting the photodiode structure for this particular application, we are looking for a device that can simultaneously achieve low capacitance and high speed. The p-i-n photodiode is commonly used in digital optical communications links for its ability to detect optical signals with high data rates. However, as discussed in Chapter 2, the p-i-n photodiode has an inherent tradeoff between junction capacitance and transit time. Photogenerated electrons and holes travel through the device with their according carrier velocities, which can be calculated by [4-3],

$$v_e(E) = \frac{\mu_e E + \beta v_e^{sat} E^2}{1+\beta E^2} \quad (4\text{-}1)$$

$$v_h(E) = v_h^{sat} \tanh\left(\frac{\mu_h E}{v_h^{sat}}\right) \quad (4\text{-}2)$$

where μ_e is the mobility of electrons in a semiconductor material, E is the electric field strength, v_e^{sat} is the electron saturation velocity and v_h^{sat} is the hole saturation velocity, β is 7.4 x 10^{-10} and γ is 2.5. In semiconductor materials such as InP and GaAs, electrons have a maximum drift velocity at a specific electrical field, called the "overshoot velocity". Fig. 4-1 shows the carrier drift velocity versus applied electric field in InGaAs, which illustrates that the electrons have a faster saturation velocity than holes do. For example, in p-i-n photodiodes with an InGaAs absorber, both electrons and holes must transit through the depletion region, so the total carrier transit time is limited by the slower holes.

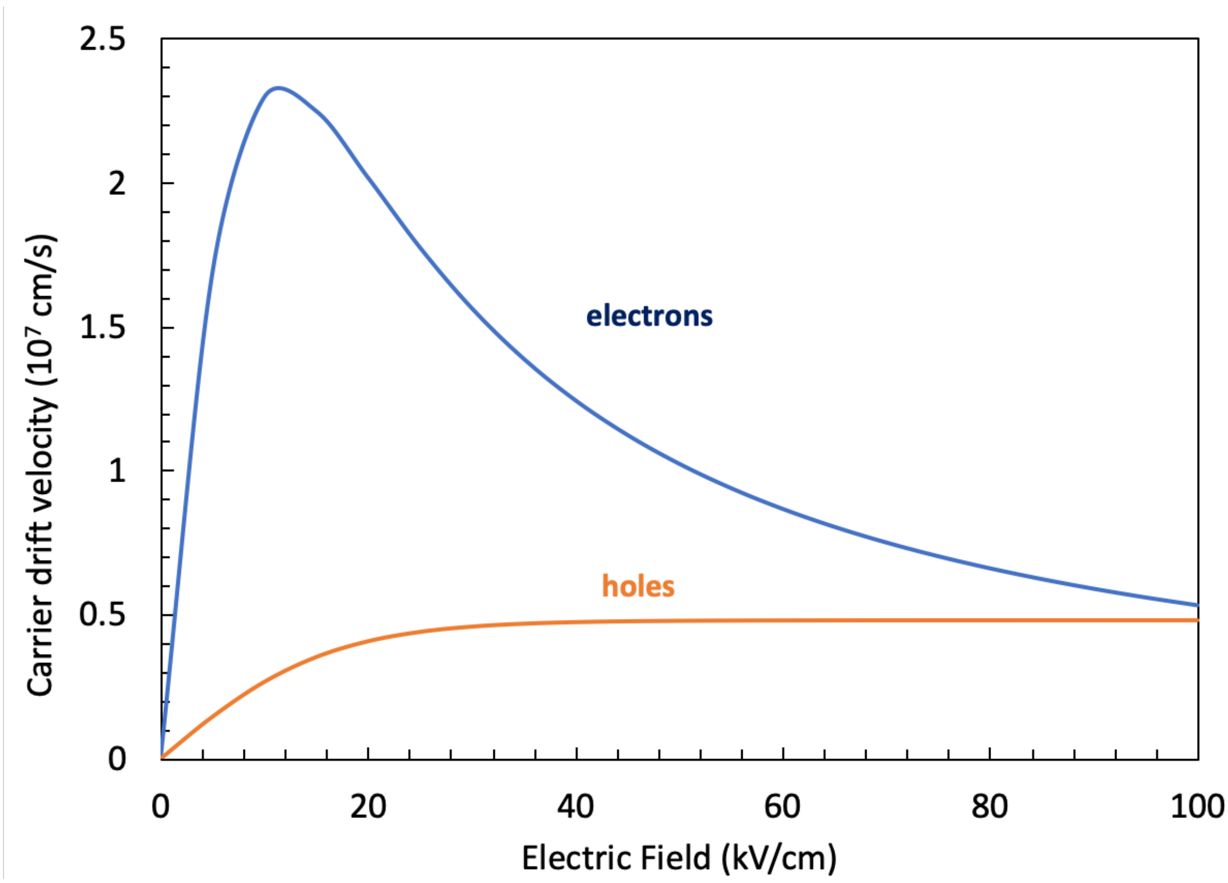


Fig. 4-1. Drift velocity of electrons and holes in InGaAs.

One way to shorten this carrier transit time is to use a uni-traveling carrier (UTC) photodiode structure, in which the electrons are isolated as the primary carrier that transit through the device. The UTC photodiode was discovered by Ishbibashi in 1997 [4-4], and has been a popular alternative for the p-i-n photodiode since. The structure consists of an undepleted absorber and a depleted collection layer. Light is only absorbed in the undepleted absorber, and electrons are injected into the depleted collection layer, then drift until reaching the contact region. The photogenerated holes are collected through the dielectric relaxation time, which is a fast process, determined by the time needed by a semiconductor to return to electrical neutrality after carrier injection or extraction.

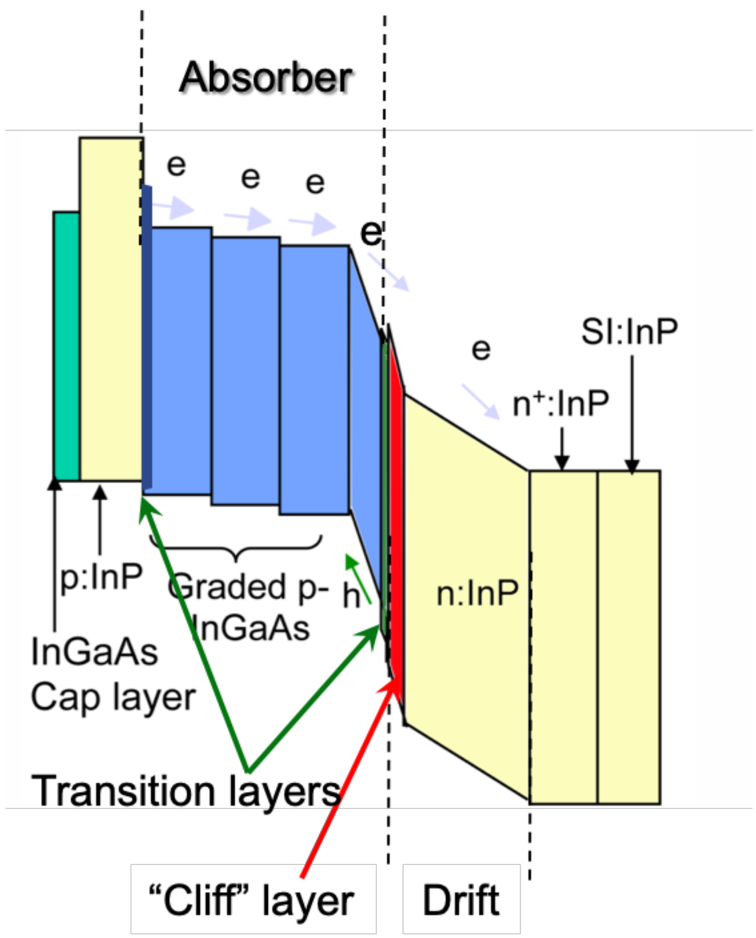


Fig. 4-2. Band diagram of the MUTC photodiode.

The modified uni-traveling carrier, or the MUTC, photodiode is an extended design of the UTC photodiode that includes a depleted absorber in order to increase the optical absorption and reduce the device capacitance, as shown in Fig. 4-1 [4-5]. Therefore, an MUTC structure was selected for its capability to produce photodiodes with low capacitance and a short carrier transit time dominated by electron transit.

Generally, in order to keep the junction capacitance low, the main two device variables to be considered are the depletion region width and device area. However, optimizing these device parameters are nontrivial. Increasing the depletion region width reduces the junction capacitance, but at the price of a longer carrier transit time. Additionally, decreasing the device area also reduces the device capacitance, however, at the cost of a decreased responsivity and higher contact resistance. It also becomes increasingly more challenging to fabricate small devices that are past the limitations of standard microfabrication clean room tools such as the contact aligner.

In the past, waveguide integrated MUTC photodiodes as small as 24 μm^2 have been fabricated and measured by Li et. al [4-6], and have achieved junction capacitances lower than 23 fF with greater than 100 GHz bandwidth. The fabrication process used limited the size of the devices, due to the alignment of the window made on top of the p-mesa needing to be aligned to the center RF pad. Furthermore, the speed of these devices were ultimately limited by the RC time constant, which is dependent on the length of the device.

Fig. 4-2 shows the simulated bandwidth for this device. The bandwidth is limited by the RC time constant for devices greater than 4 μm in diameter. Devices smaller than 4 μm are transit-time limited, which is dependent on the thickness of the collection layer (200 nm in this case). Equation (4-3) is the formula for the frequency response of the photodiode including the RLC time delay and the carrier transit time delay [4-4]. This formula includes the series inductance within the external circuitry, which is intentionally inserted into the circuit in order to create a peaking effect and extend the 3-dB bandwidth of the circuit. R_L represents the load resistance, R_S is the photodiode series resistance, L_{total} is the series inductance of the photodiode, C_{PD} is the junction capacitance, and τ is the carrier transit time.

$$\frac{I(\omega)}{I(0)} = \left(\frac{1}{1-\omega^2 L_{total} C_{PD} + j\omega C_{PD}(R_L + R_S)}\right) \times \left([1-\exp(j\omega\tau)]\frac{2}{\omega^2\tau^2} - \frac{2}{j\omega\tau}\right) \tag{4-3}$$

The inductive peaking effect that occurs in the frequency response at a certain resonant frequency is determined by Equation (4-4) below.

$$\boldsymbol{f_{resonant}} = \sqrt{\boldsymbol{2\pi L_{total} C_{PD}}} \tag{4-4}$$

Choosing the optimum inductance to insert in the circuit can improve the RC-limited 3-dB bandwidth by over 40% [4-7]. Later in this section, we discuss inductive peaking designs that we have incorporated with our photodiodes in order to improve the 3-dB bandwidth of the devices.

Furthermore, downscaling the area of the photodiode in order to minimize capacitance increases the device frequency response, but due to a trade-off in bandwidth-efficiency, these waveguide integrated photodiodes cannot achieve high speed and high efficiency simultaneously. In Li's design, the waveguide is beneath the n-contact layer, and evanescently couples the light into the photodiode, as shown in Fig. 4-4. However, in order to couple and absorb a significant portion of the incoming light from the waveguide, the photodiode must be of a minimum length.

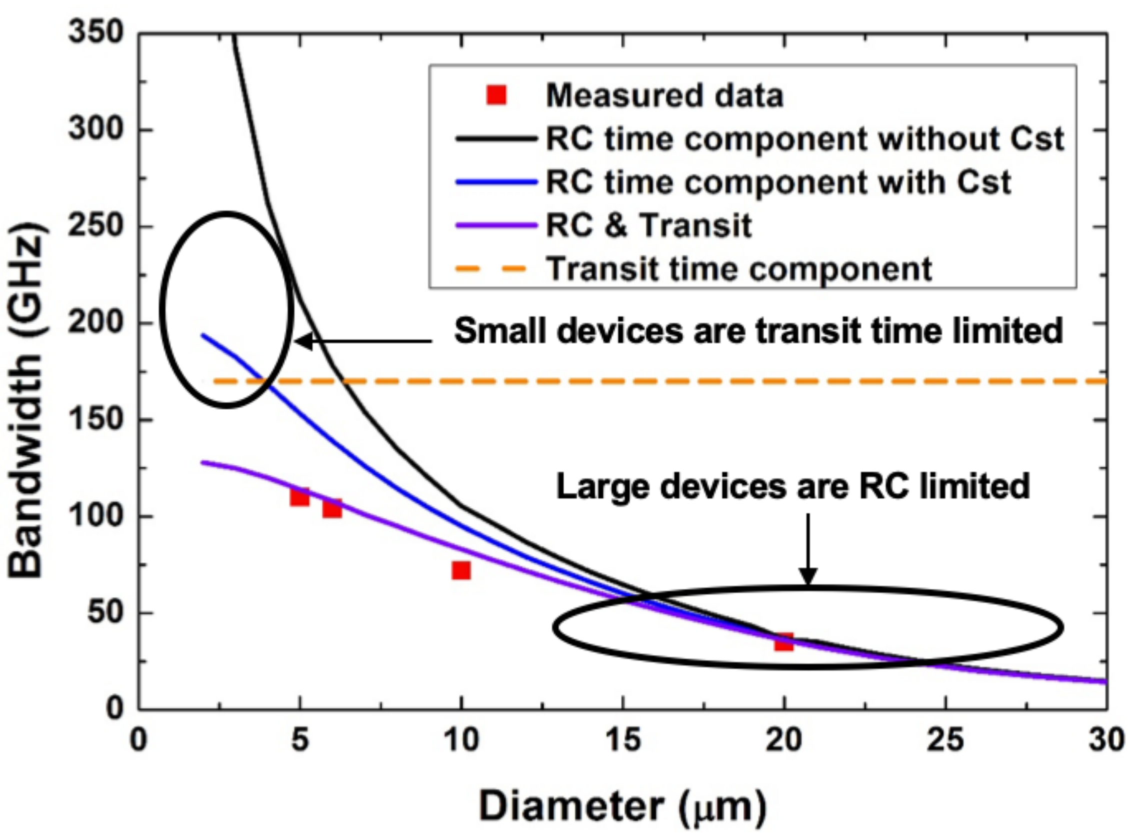


Fig. 4-3. Measured and simulated bandwidths of the MUTC photodiode from [4-6].

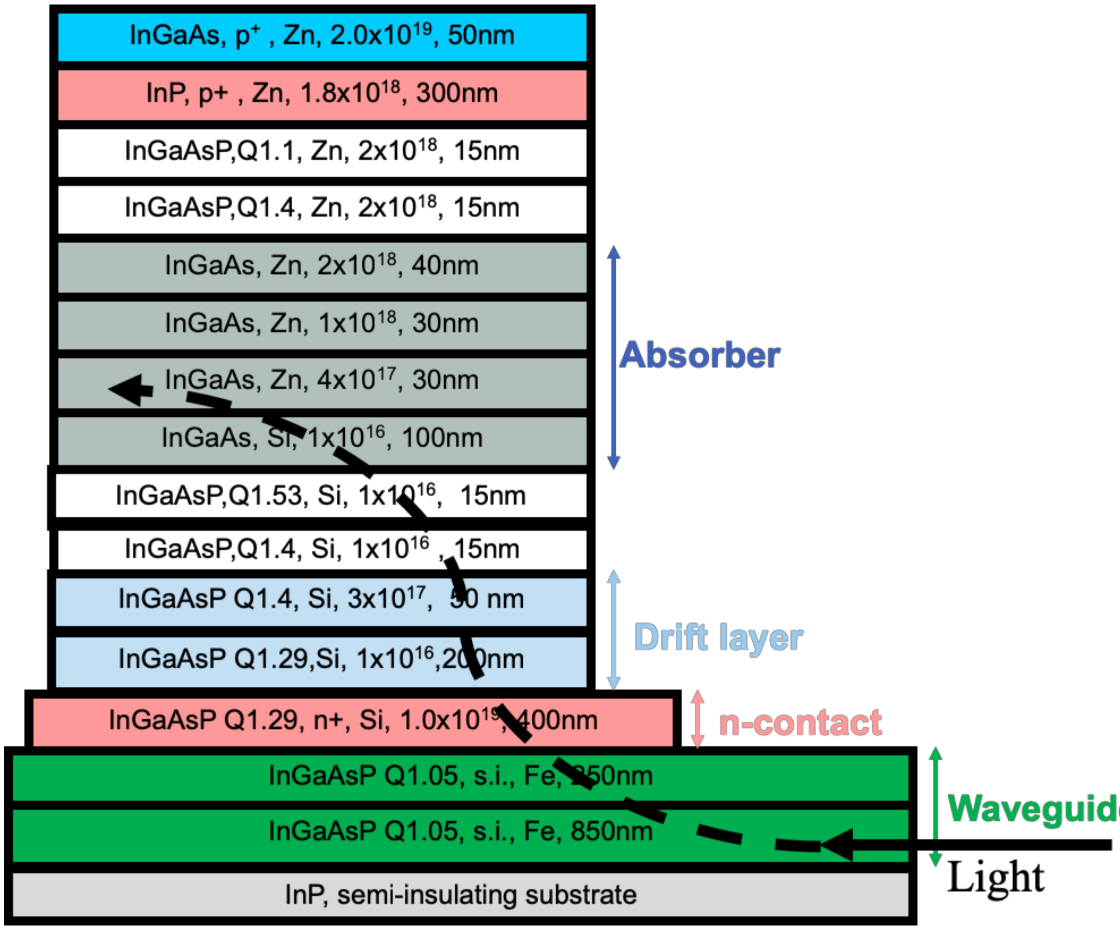


Fig. 4-4. Epitaxial layer design of MUTC photodiode from [4-6].

In order to overcome this limitation, a novel dual-integrated waveguide-depletion layer was utilized to be able to couple light more efficiently into a shorter length photodiode, which allows us to build efficient, ultra-low capacitance MUTC photodiodes. Fig. 4-5 shows the dual-integrated waveguide-depletion layer MUTC photodiode epitaxial layer structure designed.

Light in the passive waveguide section is guided into the active photodiode region, where it penetrates into the higher refractive index absorber layers. The light is absorbed, generating electron-hole pairs, with the electrons then being swept through the drift layer. The n-contact layer is made of a lower index material than the waveguide core layer in order to confine the optical mode within the waveguide core. The drift layer/waveguide core thickness was optimized to achieve a balance between the optical confinement factor within the optical waveguide core and the carrier transit time in the drift layer. Since only a small portion of the mode propagates in the n-contact layer, free carrier absorption associated losses in the waveguide are negligible.

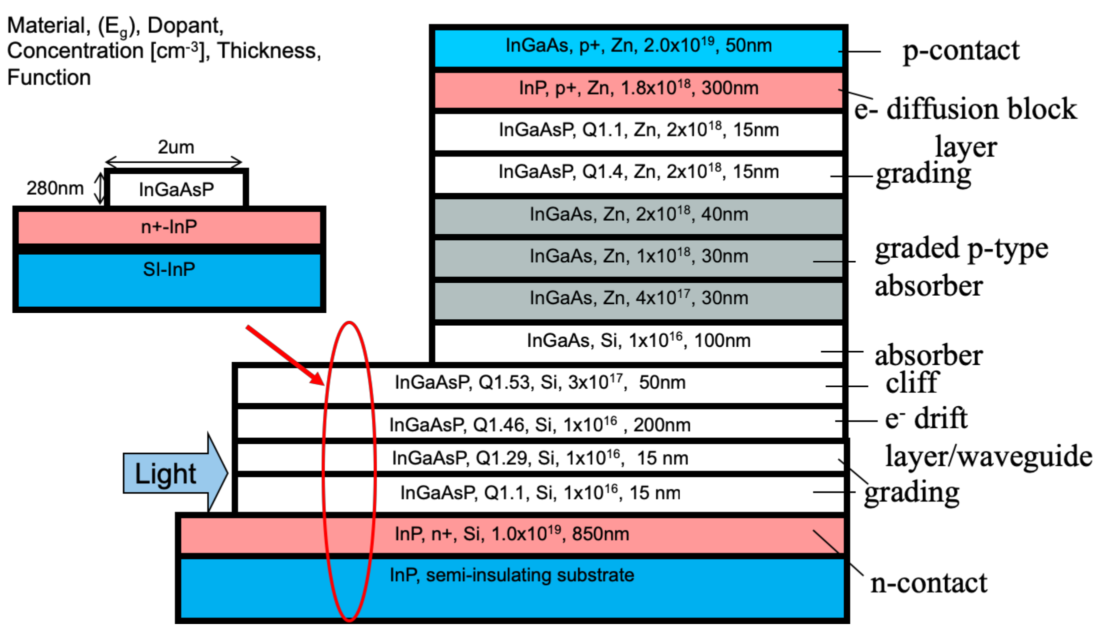


Fig. 4-5. Epitaxial layer design of the dual-integrated waveguide-depletion layer MUTC photodiode.

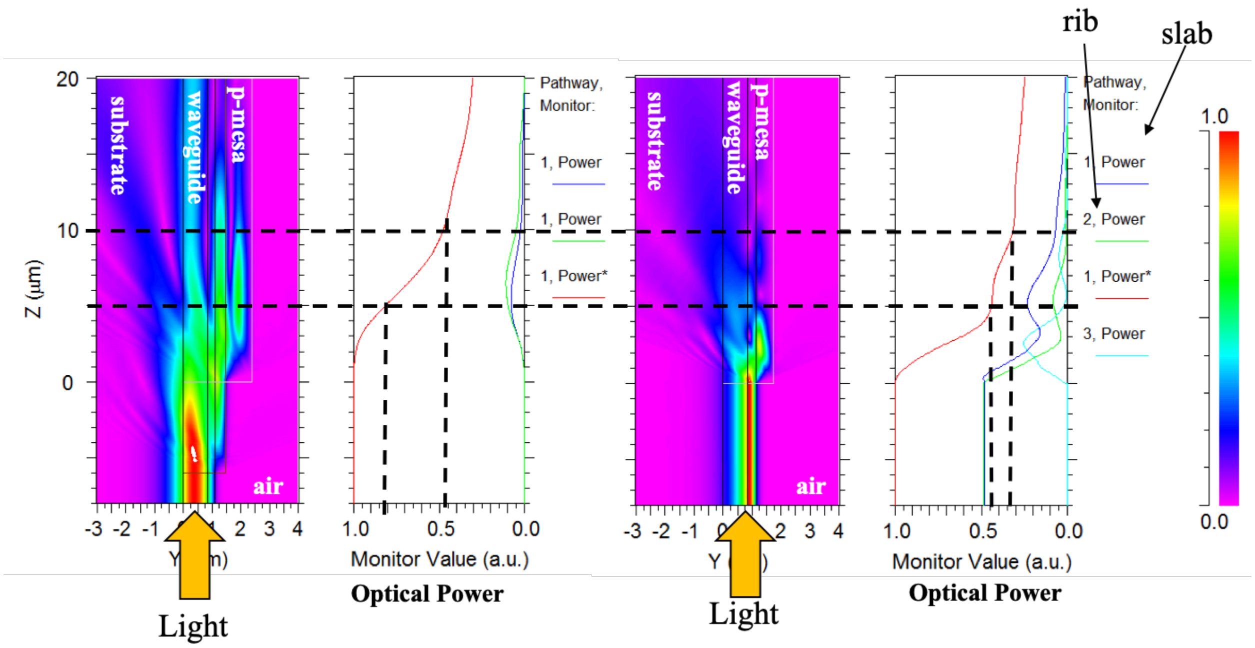


Fig. 4-6. Optical simulations of the MUTC photodiode from [4-6] and the dual-integrated waveguide-depletion layer MUTC photodiode. Red curve represents total power, green curve represents power in waveguide rib, blue curve represents power in waveguide slab, and turquoise curve represents power in absorber.

Optical simulation of the two photodiode designs is shown in Fig. 4-6. As can be seen in Li's photodiode structure, at a device length of 5 µm, less than 20% of the coupled optical mode is absorbed by the photodiode. At a device length of 3 µm, only 5% of the optical signal is absorbed, and nearly no light is absorbed in the device at lengths smaller than 2 µm. Therefore, making devices smaller than 5 µm may not only be challenging to fabricate, but also potentially not able to detect an input optical signal.

However, for the novel dual-integrated waveguide-depletion layer MUTC photodiode design, at a device length of 5 µm, light from the guided optical mode within the waveguide is able to be couple more efficiently in to the absorber. Twice the amount of light is absorbed in the device at length of 5 µm than the previous design, and 8 times the amount light is absorbed in the device at a length of 3 µm. Devices with a length smaller than 3 µm can still absorb a significant portion of light and be able to produce a detectable electrical signal.

Therefore, a newly designed planarization and passivation process was developed and devices as small as 2 µm in diameter were successfully fabricated with reduced device capacitance for potential capability for power reduction and bandwidth increase. More details on the fabrication process are discussed in the Section 4.3. Furthermore, coplanar waveguide (CPW) transmission lines were designed with reduced parasitics and inductive peaking in the frequency response in order to further improve the bandwidth.

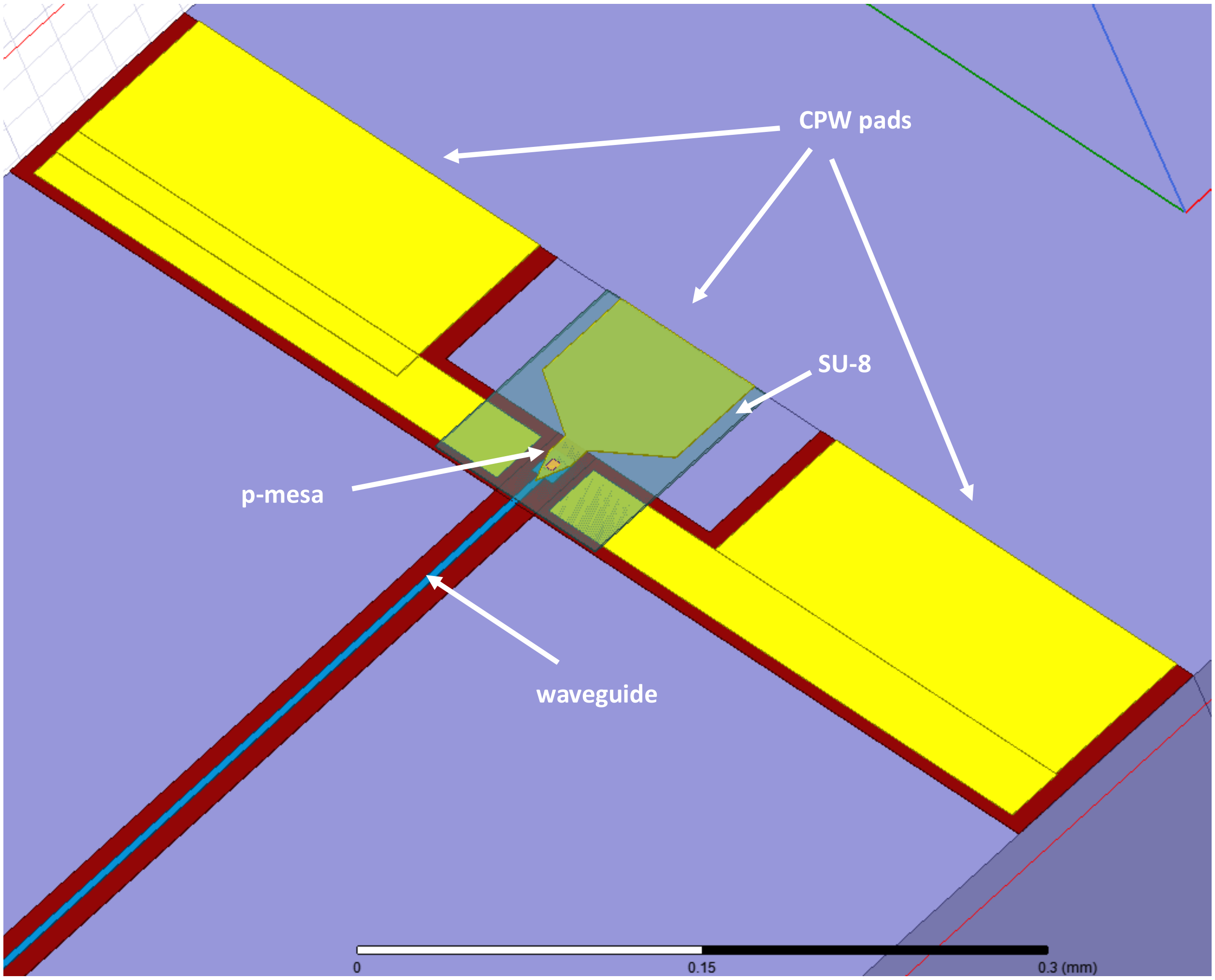


Fig. 4-7. 3-D model of a MUTC photodiode connected to 50 Ω CPW transmission line.

Fig. 4-7 shows a 3-D model of the completed MUTC photodiode passivated with SU-8 and connected to a 50 Ω CPW transmission line and Fig. 4-8 shows the cross section and circuit model of the photodiode with the metal interconnects. There is a stray capacitance in between the CPW signal pad and the n-metal contact, modeled as C_{con}. The area of the n-contact metal pad, as well as, the spacing distance between the metals must be properly designed to account for those additional capacitances.

The transmission line was designed to minimize parasitic capacitances by bringing the CPW signal pad and the n-metal contact closer together, effectively reducing C_{con}, and by reducing the total metal area of the CPW pads. Additionally, the series resistance, modeled as R_s, of the devices depends on the distance in between the n-contact metal and the device mesa. For this reason, it is optimal to bring the n-contact metal as close to the mesa as possible, but at the price of increasing the parasitic capacitance.

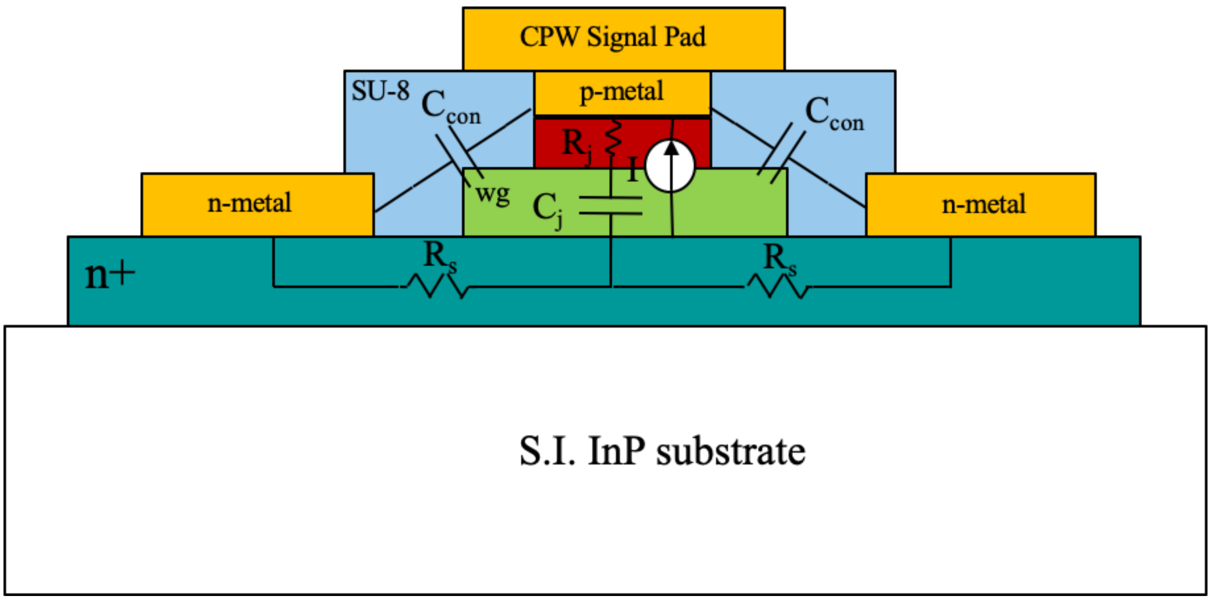


Fig. 4-8. Cross-section with circuit elements of the dual-integrated waveguide-depletion layer MUTC photodiode.

A 1 mm long CPW transmission line was simulated using Ansys HFSS, and the material parameters were input into the software to calculate the exact characteristic impedance of the transmission line. Fig. 4-9 shows the characteristic impedance simulations, which stays around 50 Ω from 0 GHz to 150 GHz.

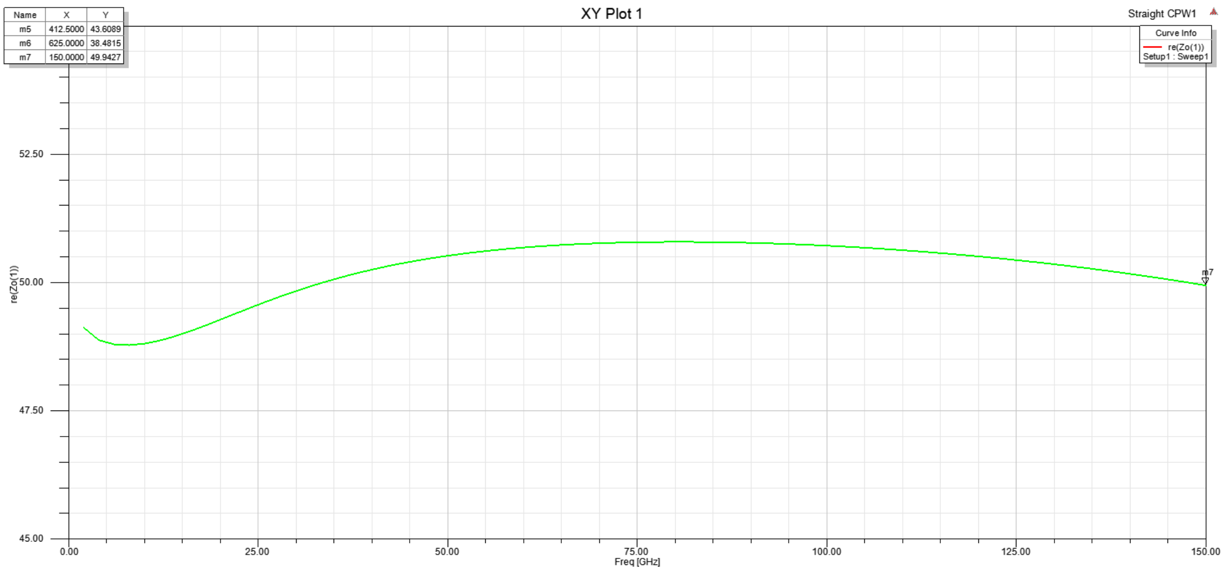


Fig. 4-9. Cross-section of the dual-integrated waveguide-depletion layer MUTC photodiode.

As mentioned before, the n-metal contact length was reduced to 5 µm, in order to keep the area of the metal area close to the CPW center pad as small as possible and, therefore, making C_{con} as small possible. The transmission line length was also shortened in order to reduce ohmic losses, but also kept long enough in order to provide enough skating tolerance for microwave GSG probes. Fig. 4-12 shows an S21 electromagnetic simulation done with Keysight ADS Momentum for the CPW transmission line with a long n-metal end section (Fig. 4-10) and a short n-metal end section (Fig. 4-11). The S21 for the short n-metal end section exhibited less loss above 100 GHz because of reduced parasitic capacitance and resistance.

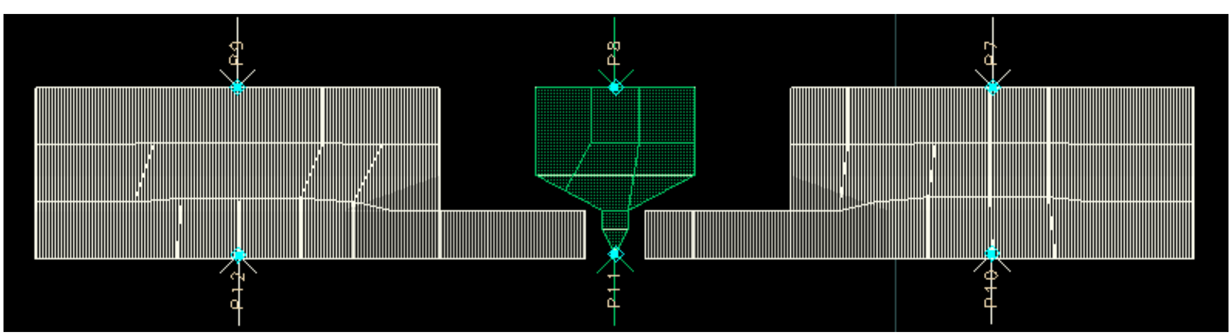


Fig. 4-10. Layout of the 50 Ω CPW with long n-metal end section (taken in Keysight ADS Momentum).

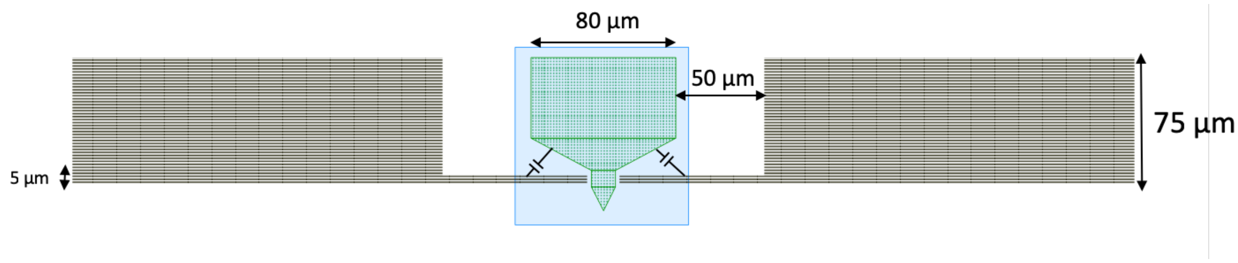


Fig. 4-11. Layout of the 50 Ω CPW with short n-metal end section with dimensions of length and indicated location of parasitic capacitances, C_{con}.

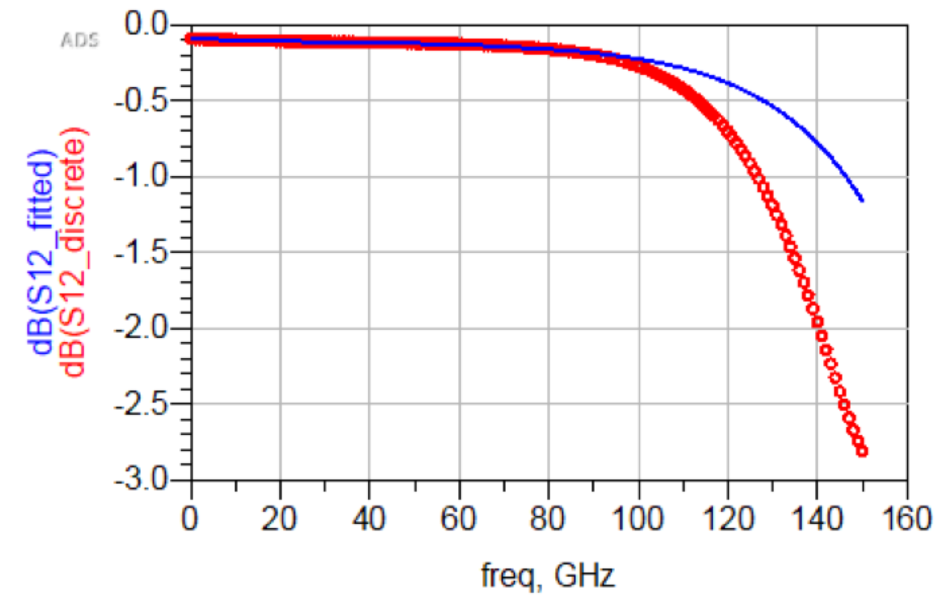


Fig. 4-12. S12 simulation results for the CPW with short n-metal end section (in blue) and long n-metal end section (in red). Lower losses are seen in the CPW with short n-metal end section due to reduced parasitic capacitance.

A circuit (Fig. 4-13) was then simulated with a virtual probe with a 50 Ω characteristic impedance, connected to the designed CPW transmission line that was then connected to a circuit model for a 4 μm x 6 μm photodiode. R_s was chosen to be 6 Ω, C_j was selected to be 13fF, as measured in the photodiodes developed by Li et. al [4-6]. The simulations for the RF output power from the photodiode (Fig. 4-14) show a 125 GHz 3-dB bandwidth, which is 20 GHz higher than the measured 3-dB bandwidth from [4-6], due to reduced parasitic capacitance and losses from the transmission line, not including transit time effects.

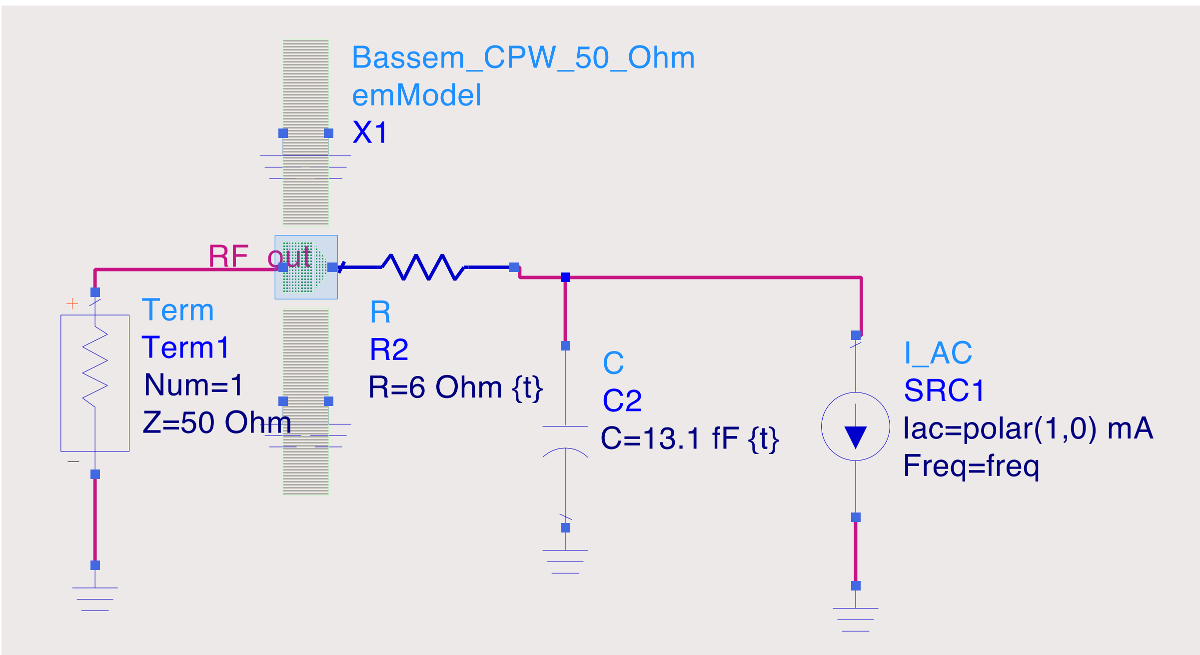


Fig. 4-13. Circuit schematic for a 4 μm x 6 μm photodiode connected to the simulated CPW.

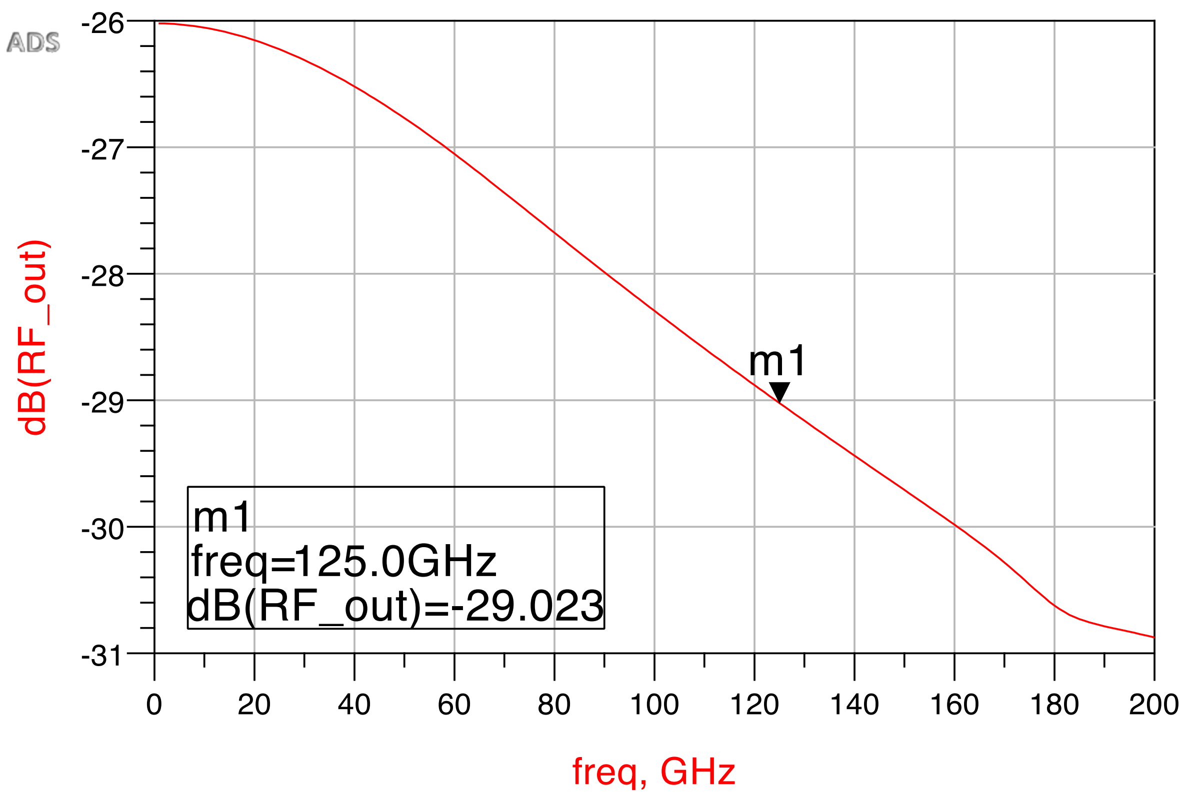


Fig. 4-14. Simulated output frequency response of a 4 µm x 6 µm photodiode connected to the simulated CPW (3-dB marked with marker labeled, m1).

With a device as small as 2 µm in diameter, the maximum 3-dB bandwidth can be limited by the transit time, which is 150 GHz. With the integration of a CPW that utilizes inductive peaking (Fig. 4-15), the bandwidth can be pushed even further, up to 190 GHz (Fig. 4-16). The inductance of the transmission line is largely determined by the area of the rectangular strip in between the probe pads and the p-mesa. More specifically, the inductance can be calculated by [4-7],

$$L_{HTRL} = \frac{\mu_0}{2\pi} l \left(\ln\left(\frac{2l}{R}\right) + \frac{R}{l} - 1 \right) \tag{4-5}$$

where l is the length of the transmission line, μ_0 is the vacuum permeability. R represents the geometric mean of the transmission line cross section and is given by,

$$R = 0.2235(a + b) \quad (4\text{-}6)$$

where a and b are the width and thickness of the transmission line.

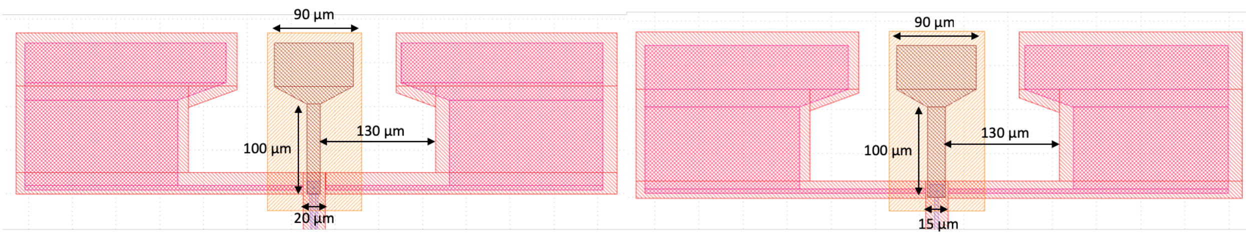


Fig. 4-15. Layout of the high-impedance CPW incorporating two inductive peaking designs.

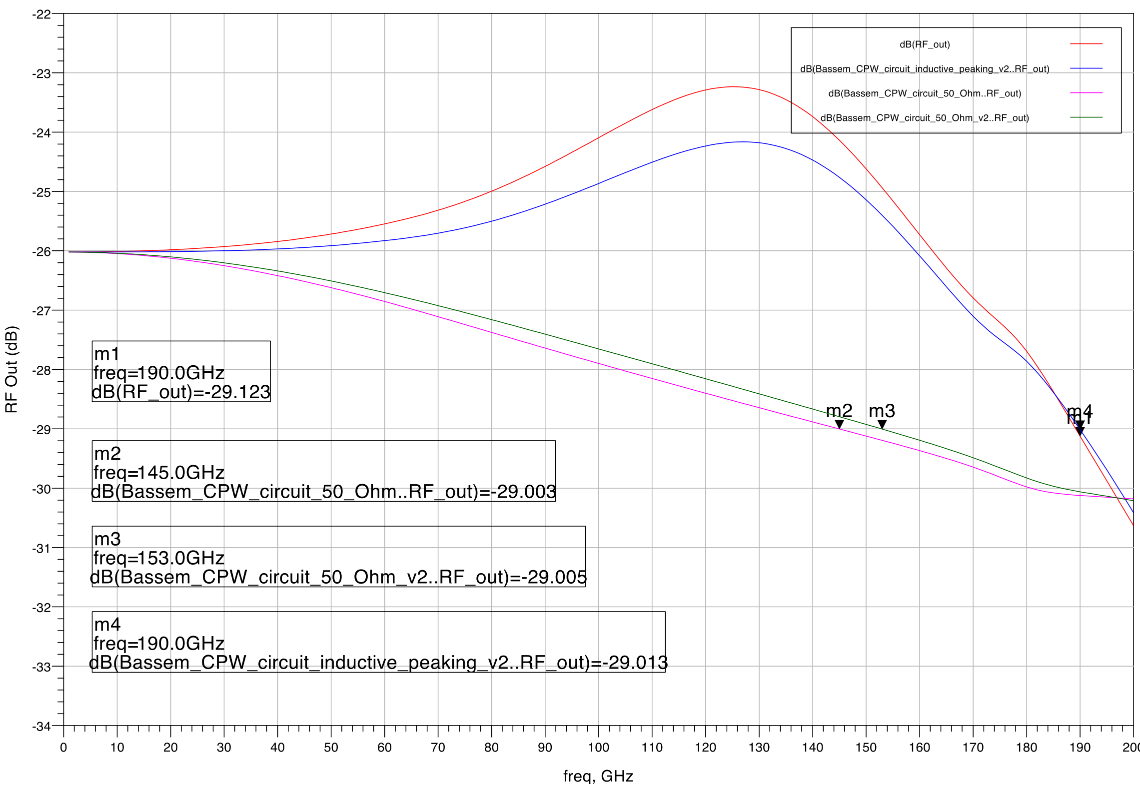


Fig. 4-16. Simulated output frequency response of a 2 μm x 2 μm photodiode connected to a 50 Ω CPW with a short n-metal end section (green curve), long n-metal end section (purple curve), and two different inductive peaking high impedance CPW designs (red and blue). Markers mark the 3-dB bandwidth of each design.

4.3 Device Fabrication Process

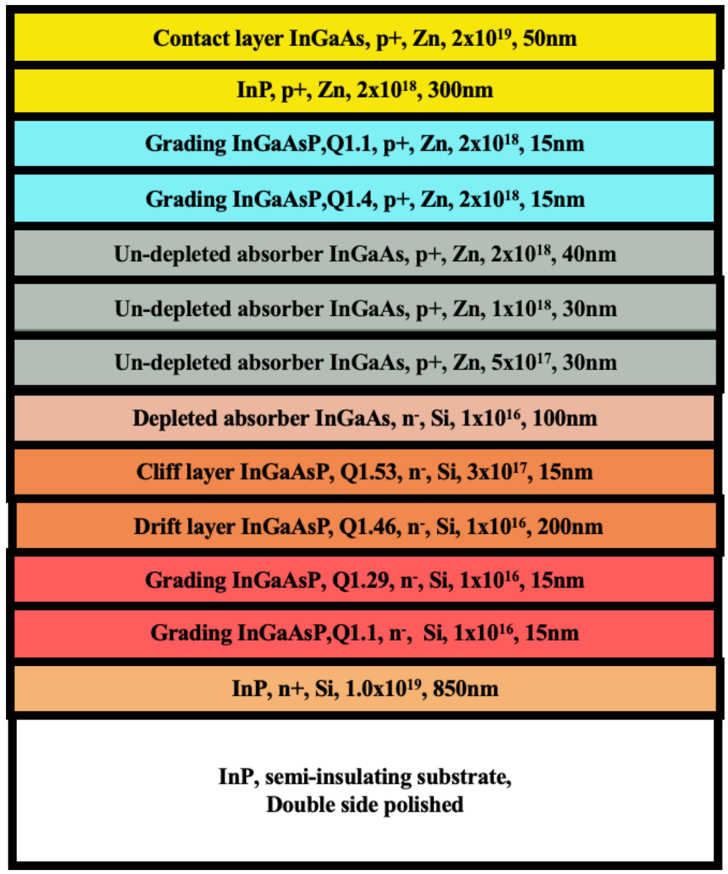


Fig. 4-17. Epitaxial layer structure for the dual-integrated waveguide-depletion layer MUTC photodiode.

Fig. 4-17 shows the epitaxial layer structure for the waveguide MUTC photodiode. The layers were deposited and in situ-doped with zinc (p-type) and silicon (n-type) by metal organic chemical vapor deposition on semi-insulating InP substrate by Landmark. First, a 850 nm-thick heavily doped n-type InP contact layer/waveguide lower cladding layer was deposited followed by a two 15 nm-thick lightly n-doped InGaAsP quaternary layers were to suppress charge accumulation at the heterojunction interfaces and a 200 nm-thick lightly n-doped (1×10^{16} cm^{-3}) charge compensated drift layer. A 50 nm-thick n-doped (3×10^{17} cm^{-3}) InP cliff layer was then used to maintain a high electric field in the depleted absorber [4-9]. The lightly doped layers also serve as the core of the input optical waveguide.

Next, a 100 nm-thick unintentionally doped depleted InGaAs absorber was deposited. Three 50 nm p-type undepleted absorber layers with step grading of 4×10^{17} cm^{-3}, 1×10^{18} cm^{-3}, 2×10^{18} cm^{-3} create a quasi-electric field that aids electron transport. Finally, two 15 nm-thick lightly p-doped InGaAsP quaternary layers were deposited to assist hole collection and block the diffusion of electrons into the p-contact region. The p-type contact was formed using a 300 nm-thick heavily p-doped InP and a 150 nm-thick heavily p-doped InGaAs cap layer.

The fabrication process was designed to have devices as small as 2 µm in diameter to be lithographically defined, etched, and connected to RF pads. The fabrication process that was developed is shown in a step-by-step schematic diagram in Fig. 4-18 and the detailed process recipe sheet can also be found in Appendix B.

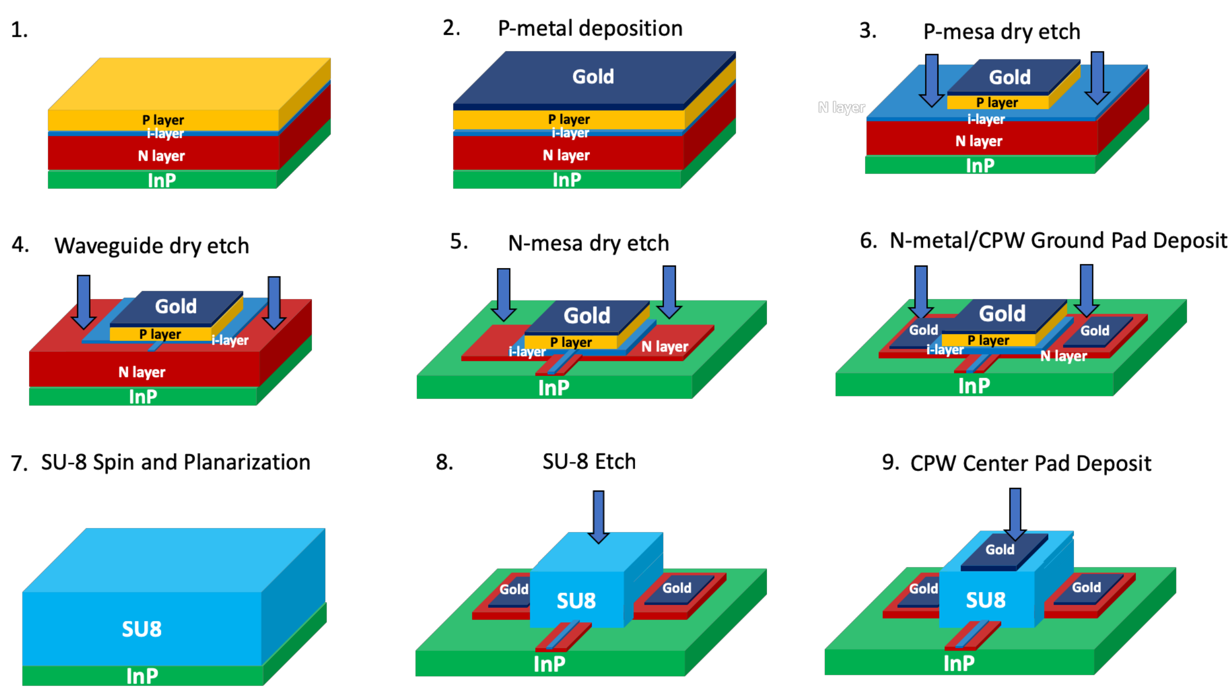


Fig. 4-18. Step by step fabrication process diagram.

The first step was to deposit the p-contact metal on top of the sample using electron beam evaporation. Ti/Pt/Au/Ti was grown, with a thickness totaling 300 nm in order to have a larger tolerance with the SU-8 etch step. Then, silicon dioxide (SiO_2) was deposited as a hard mask for the p-mesa etch. Next, a negative photoresist called NR7-250P was used for its potential to define sub-micron features. The photoresist was deposited and used to pattern the p-mesa. Next, the SiO_2 was etched in an Oxford ICP-RIE dry etching machine using CHF_3. The photoresist was then removed, and the p-contact metal was etched in the ICP-RIE with Cl_2 and N_2, followed by the p-contact layers and the absorber layers.

It is worth noting that if the p-mesa is under-etched, then the waveguide will have contain optically absorbing material, and the light will be absorbed by this material as it propagates through the waveguide. Furthermore, if the p-mesa is over-etched by 100 nm, for example, then the waveguide is also 100 nm thinner, meaning that the optical mode is no longer confined in the drift layer. With that said, it is critical to over-etch the p-mesa less than 50 nm in order to ensure a confined optical mode in the drift layer and minimize waveguide losses. This will be talked about in more detail in Section 4.4.

After the p-mesa was etched, then the waveguide and the n-mesa were etched. Next, Ti/AuGe/Ni/Au was deposited on top of the n-mesa to serve as the n-contact metal, as well as, the RF ground pads. Fig. 4-19 shows a scanning electron micrograph (SEM) photo of a 2 µm diameter p-mesa after the waveguide was etched.

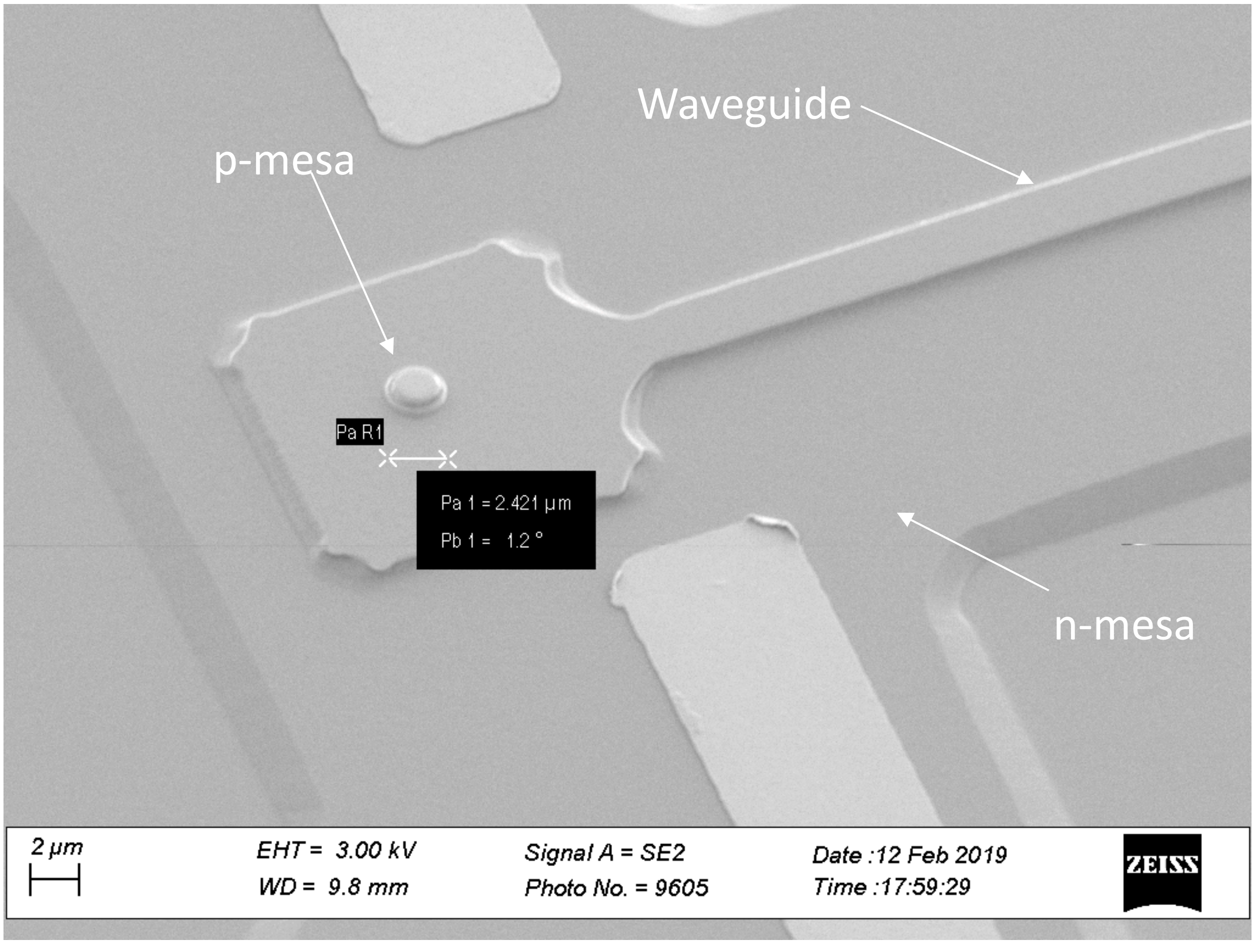


Fig. 4-19. Scanning electron micrograph (SEM) photo of a 2 µm diameter photodiode after the p-mesa, waveguide, and n-mesa etch.

SU-8 was then used to passivate the sidewalls of the device and reduce leakage current, as well as, serve as an insulation pad and interconnect supporting structure for the RF signal pad. The SU-8 also relaxes the alignment tolerance of the subsequent RF signal pad lithography. More specifically, SU-8 5 was selected for its planarization capability on chips with its surface topography. After SU-8 5 was deposited and planarized across the surface of the chip, it was etched until the p-metal was exposed. The etch was done in the Oxford ICP-RIE dry etching machine, using 50 sccm of O_2 and 6 sccm of SF_6, at an RF power of 115 W and a chamber pressure of 20 millitorr.

The height of the SU-8 layer was then checked with a profilometer after each subsequent etch. The etch tolerance is <850 nm, so as long as the SU-8 is etched past the top of the p-metal less than 850 nm total, then the RF signal pad metal can be deposited on top of the p-mesa without shorting the device. This planarization process eliminates the need for an air bridge and its precise and difficult alignment to the p-mesa. Fig. 4-20 and 4-22 show SEM photos of a 10 µm x 100 µm photodiode and a 5 µm x 7 µm with the SU-8 after being etched. As seen, the p-mesa sidewalls are covered with SU-8, so they are passivated, and the p-contact metal is exposed, so it can be interfaced with the RF signal pad.

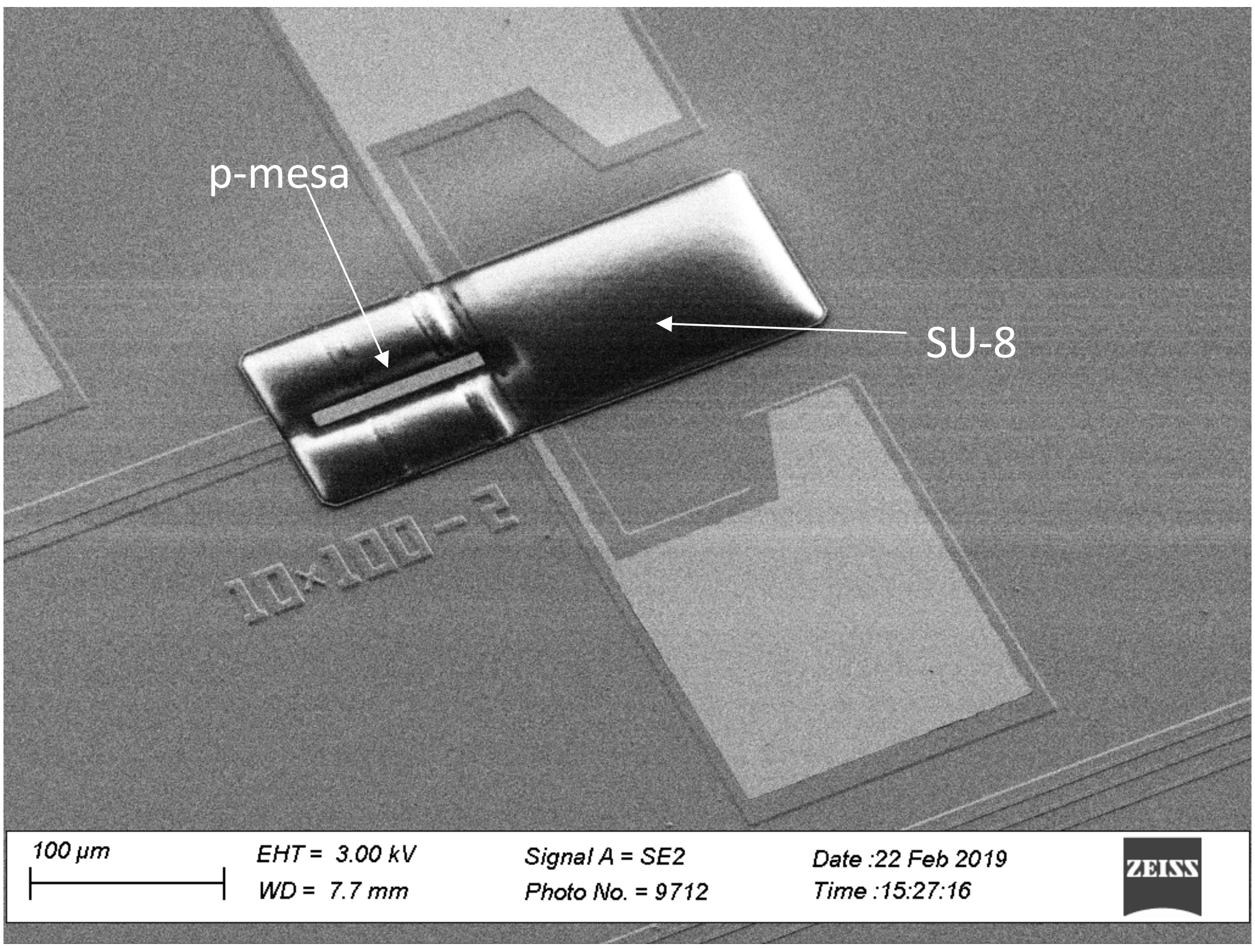


Fig. 4-20. SEM photo of a 10 µm x 100 µm photodiode after the SU-8 etch.

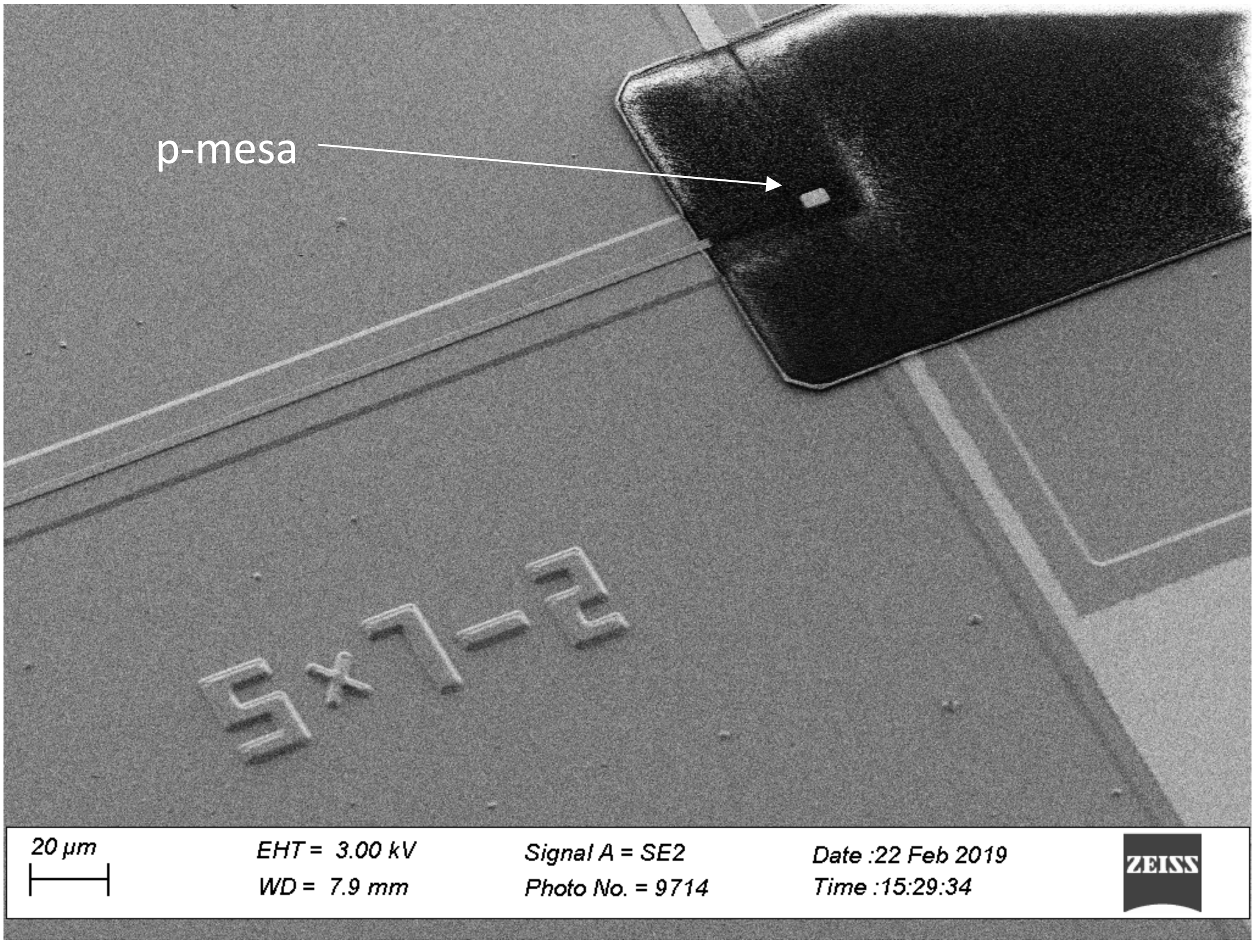


Fig. 4-21. SEM photo of a 5 µm x 7 µm photodiode after the SU-8 etch.

Next, photoresist was deposited in order to open windows for the RF signal pads. Then, 30 nm of Ti and 400 nm of Au was deposited. Afterwards, metal lift-off was used to remove the metals from the areas of the chip covered with photoresist. An SEM photo of a completely fabricated 2 µm diameter photodiode is shown in Fig. 4-22 and Fig. 4-23, and an SEM photo of a completely fabricated 5 µm x 30 µm photodiode is shown in Fig. 4-24. Lastly, the chips were cleaved using a cleaving tool, leaving the waveguide facets cleaved.

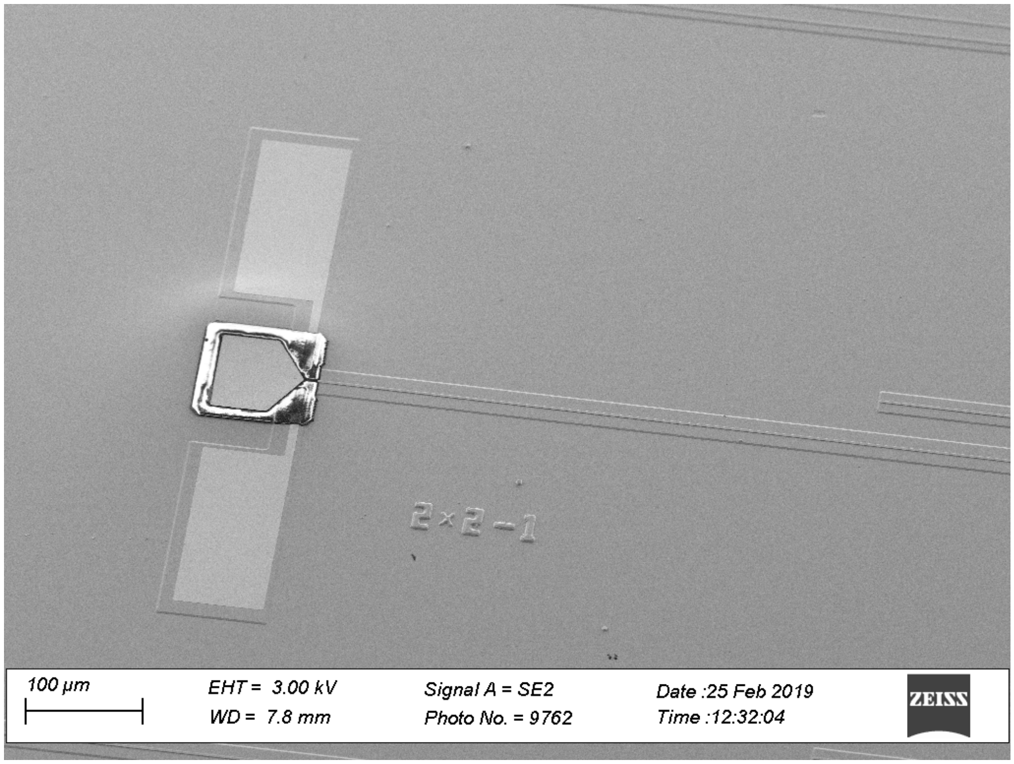


Fig. 4-22. SEM photo of a complete 2 µm diameter photodiode after the SU-8 etch.

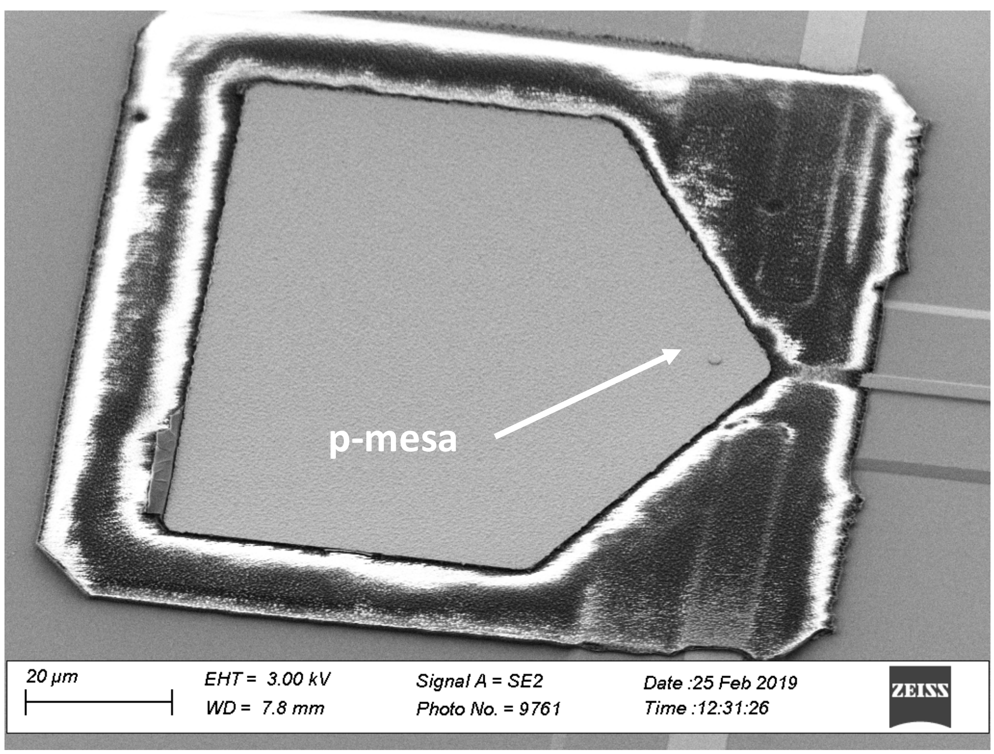


Fig. 4-23. Close-up SEM photo of a complete 2 µm diameter photodiode after the SU-8 etch.

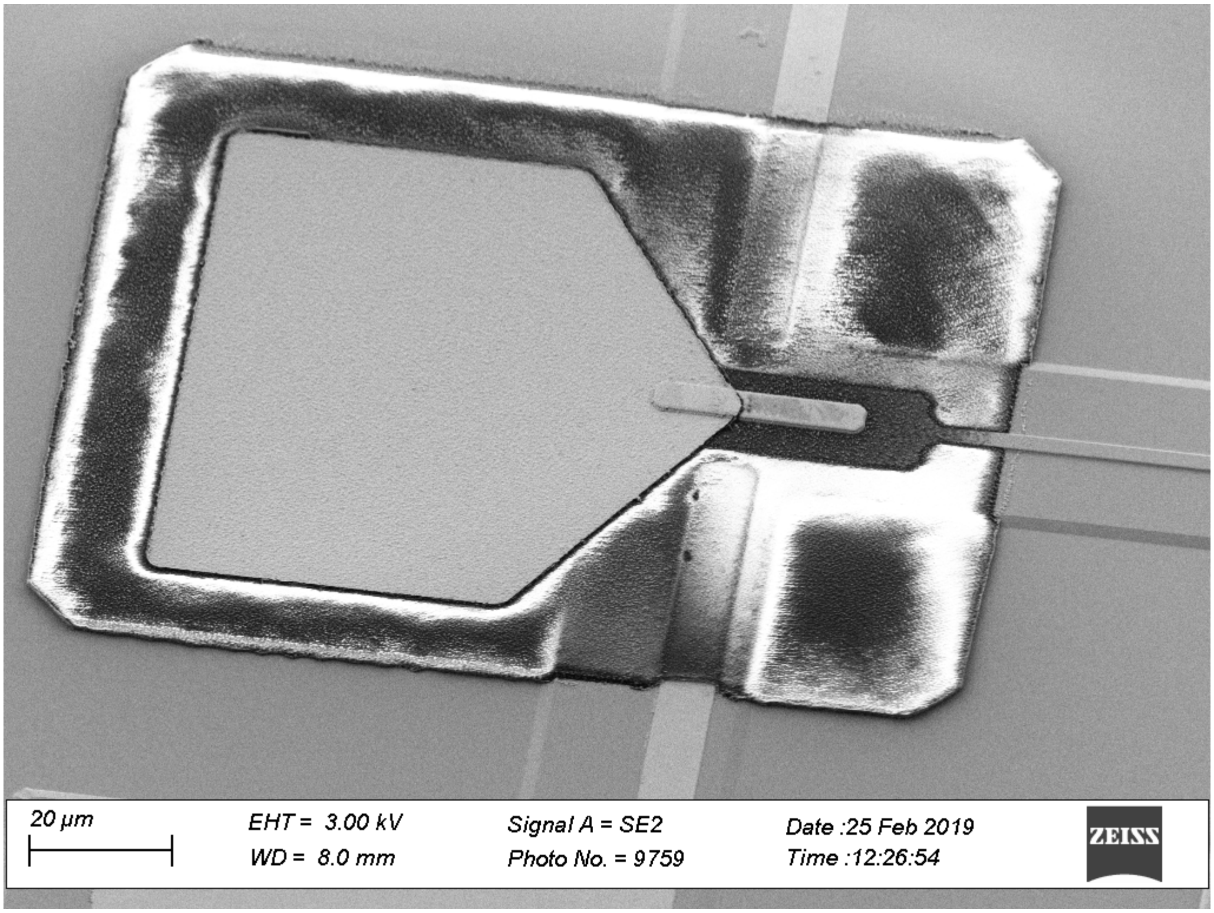


Fig. 4-24. Close-up SEM photo of a complete 5 µm x 30 µm photodiode after the SU-8 etch.

4.4 Device Results

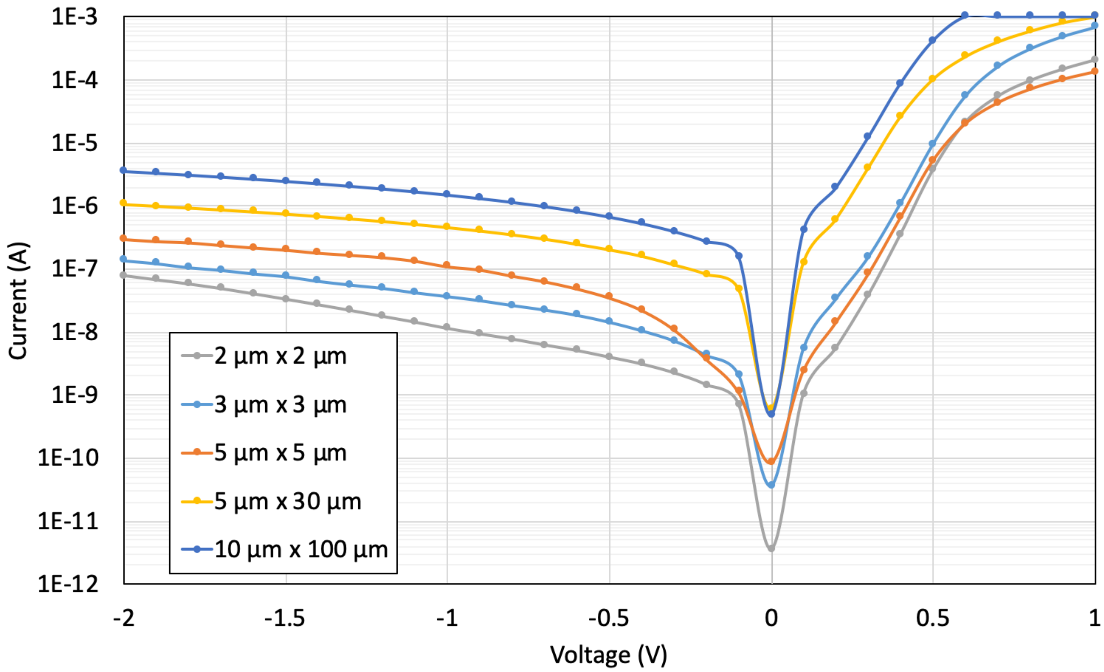


Fig. 4-25. I-V curves for different sized dual-integrated waveguide-depletion layer MUTC photodiodes.

Firstly, I-V curves were taken of the devices by a HP 4156B semiconductor parameter analyzer and are shown in Fig. 4-25. The dark current is as low as 5 nA at -1 V for a 2 µm x 2 µm photodiode. Capacitance-voltage (CV) measurements were also taken with a HP 4275A Multi-Frequency LCR meter. The junction capacitance scales linearly with area as shown in Fig. 4-26, and a junction capacitance as small as 1.8 fF was measured, with an error of less than 5%, for a 3 µm x 3 µm device. This is comparable to other recent work on ultra-low capacitance PDs, such as work from IBM Zurich [4-2], who developed photodiodes with capacitances in the range of 0.3 fF-5.5 fF, as well as work from NTT [4-10], which featured photodiodes with a capacitance < 1 fF, and Ge waveguide PDs with a capacitance of 4-5 fF [4-11, 4-12]. The parasitic capacitance coming from the CPW pads, C_{con}, were measured to be about 1 fF. This verifies that the designs described in Section 4.2 worked, as intended, to lower both device and parasitic capacitances.

The measured capacitance allows for an increase of 3-dB bandwidth by lowering the RC time constant, and a transit time limited bandwidth of 150 GHz can be reached. Even with a large load resistor, a high 3-dB bandwidth can still be maintained. For example, with a 1 kΩ load resistor, the RC-limited 3-dB bandwidth is calculated to be 52 GHz. Also, the energy per bit consumption of an optical receiver would be reduced due to the decreased capacitance. Since the capacitance is smaller, the photogenerated charges in the photodiode produce a large enough voltage swing across the high resistance load resistor to supply a CMOS logic gate, as shown in Fig. 4-27 [4-1].

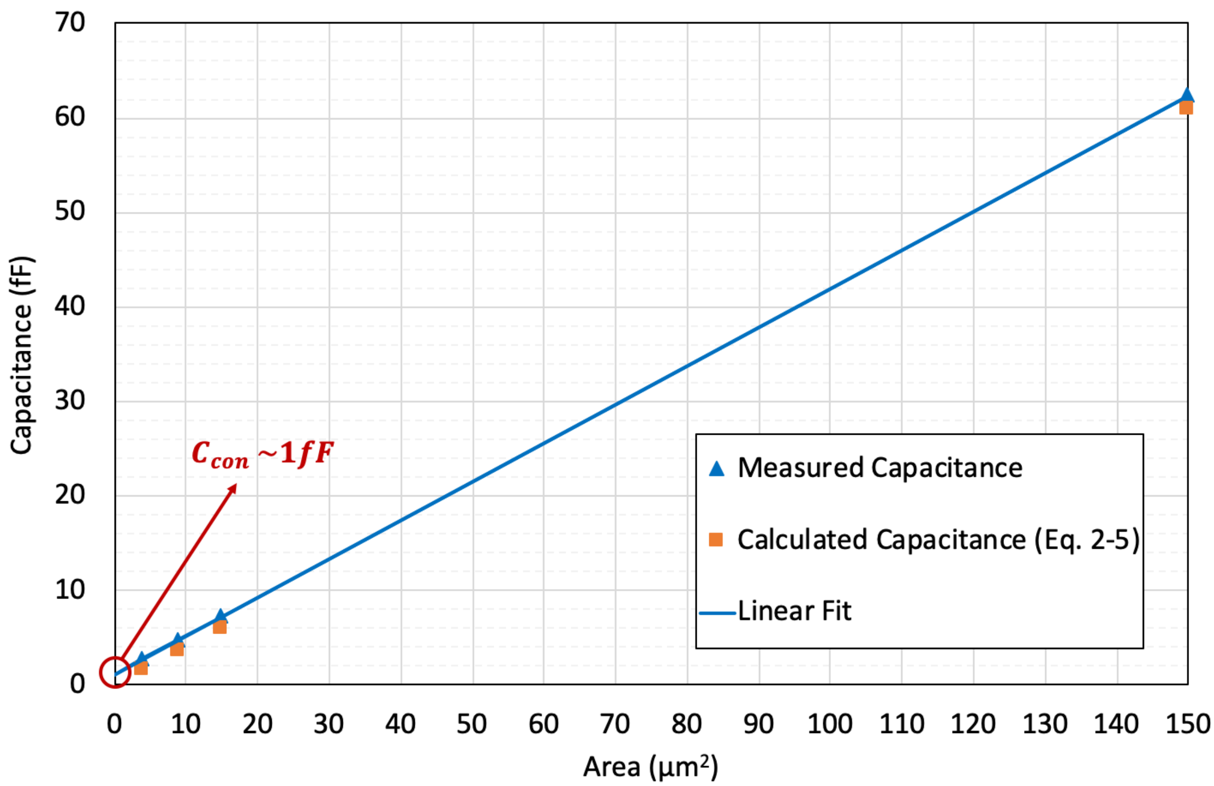


Fig. 4-26. Capacitance of dual-integrated waveguide-depletion layer MUTC photodiodes versus device area at a voltage bias of -1 V. Blue markers represent measured data, blue line represents linear fit of measured data, and orange dots represent calculated capacitance. C_{con} refers to the parasitic capacitance from the CPW pads.

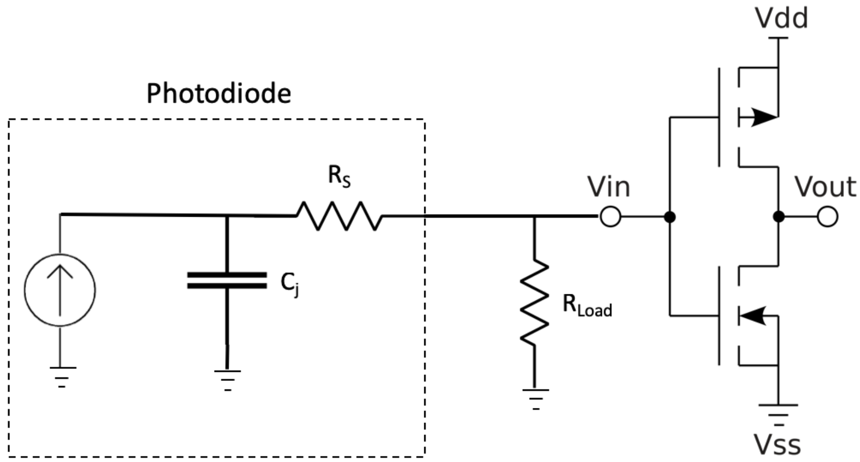


Fig. 4-27. Circuit schematic of photodiodes driving the input of CMOS gate through the voltage drop across a high load resistor, R_{Load}. This method eliminates the need of a transimpedance amplifier at the output of the photodiode.

The external responsivity measured was about 0.26 A/W for a 5 µm x 7 µm PD at -3 V, and 0.46 A/W for a 10 µm x 100 µm PD at -3 V and is shown in Fig. 4-28. Light from a 1550 nm CW laser coupled onto the waveguide facet using a lensed fiber with a 2 µm spot size. The responsivity varied less than 5% with a change in bias. The fiber coupling loss was simulated by Rsoft as about 3 dB, the reflection loss as about 1.5 dB, and the free carrier absorption loss as about 1.6 dB, given the doping concentration of the n-contact region.

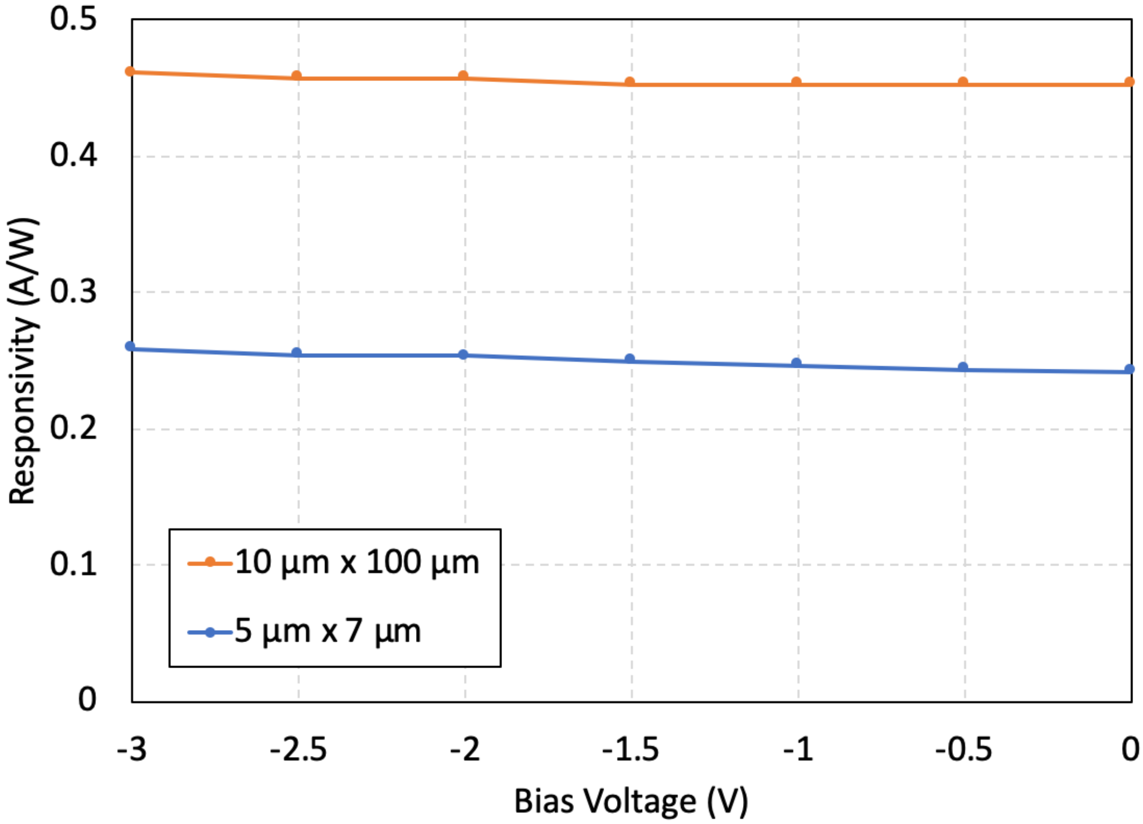


Fig. 4-28. Responsivity at 1550 nm of a 5 µm x 7 µm photodiode and a 10 µm x 100 µm photodiode.

This number does not account for the waveguide loss, hich was too high to measure for a 5 mm long waveguide. The reason for the high waveguide loss is due to over-etching of the p-mesa by 100-150 nm. The waveguide core was too thin, and therefore, the mode was no longer confined and guided in the drift layer. Instead, the mode was guided through the substrate, as can be seen in Fig. 4-29. In Fig. 4-29 (a), the waveguide is simulated with no over etching of the p-mesa, and the optical mode is mostly confined in the drift layer. In Fig. 4-29 (b) and (c), the p-mesa is over-etched by 100 nm and 130 nm, and the optical mode no longer is mostly confined in the drift layer, but rather in the substrate. This then drastically changes the coupling in between the waveguide and the photodiode, as only a small portion of the light is coupled into the absorber of the photodiode. The waveguide loss becomes as high as -20 dB in Fig. 4-29 (c).

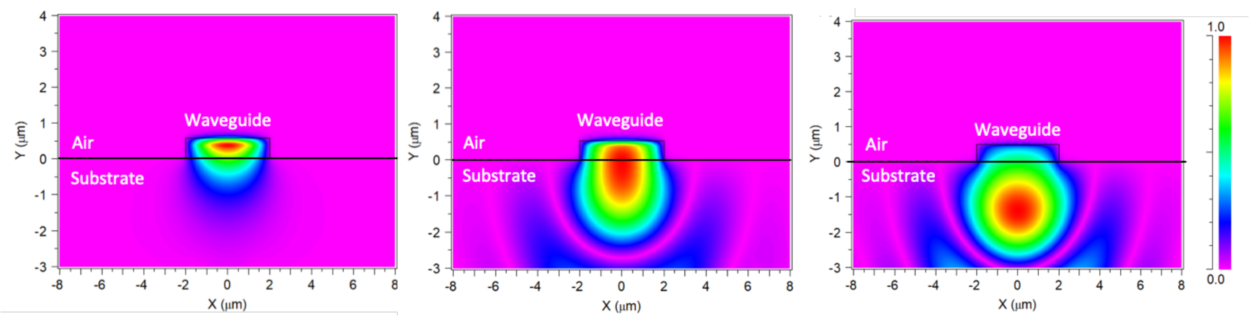


Fig. 4-29. Optical mode confinement for a waveguide after the p-mesa is (a) not over-etched, (b) over-etched by 100 nm, and (c) over-etched by 130 nm.

Fig. 4-30 shows a schematic of the experiment set up for the frequency response measurements. The output frequency response was measured at -1 V for a 5 µm x 30 µm (Fig. 4-30) with a GSG microwave probe, a 1550 nm CW laser amplified by an EDFA and modulated by an E-O Space 1550 nm intensity modulator, and a Rohde & Schwartz electrical spectrum analyzer (ESA). A 45 GHz bandwidth u^2t photodiode was used to calibrate the modulator loss and an Agilent Vector Network Analyzer (VNA) was used to calibrate losses from the RF cables and bias tee. We were limited in measuring the frequency response past 50 GHz by the RF signal generator, which can produce an RF signal only up to 50 GHz.

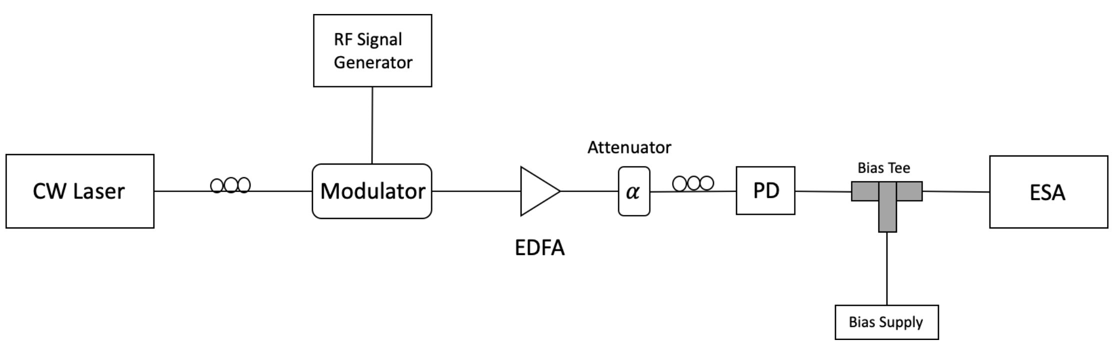


Fig. 4-30. Schematic of the experiment set-up for the frequency response measurements of the MUTC photodiodes.

The RF peak power coming from the ESA was recorded for each measured frequency and a 3-dB bandwidth of around 40 GHz was measured for a 5 µm x 30 µm photodiode, which is close to the expected 3-dB bandwidth of 45.8 GHz with the measured capacitance of a 5 µm x 30 µm of 62 fF, and a series resistance of 6 Ω.

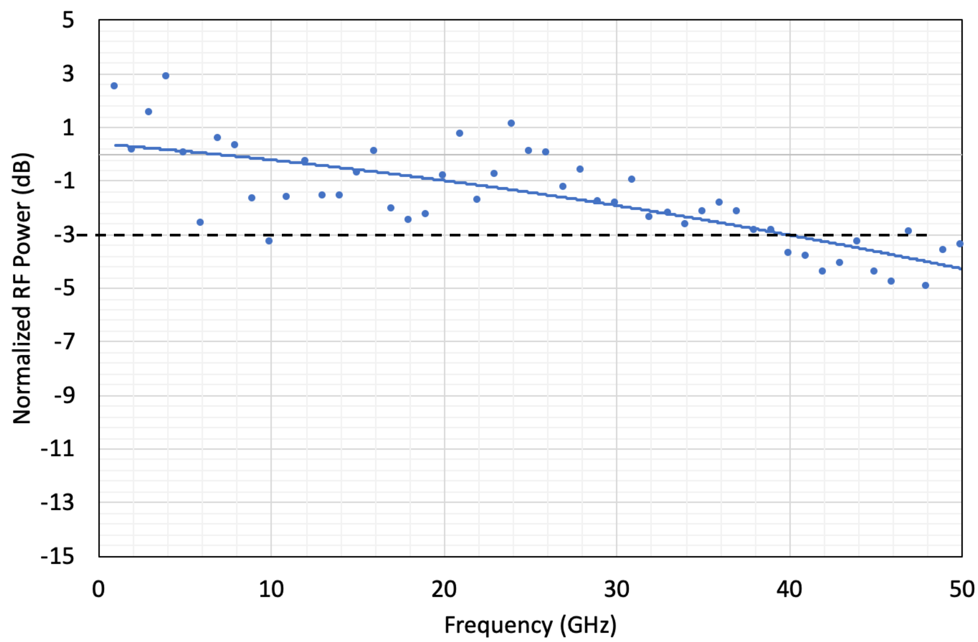


Fig. 4-31. Frequency response of a 5 µm x 30 µm photodiode at -1 V. Dots represent measured data and curves represent averaged data.

The RF frequency response up to 110 GHz was also measured for a 5 µm x 7 µm photodiode and shown in Figure 4-32. These measurements were taken using an optical heterodyne setup. Two 1550 nm lasers with MHz linewidth were mixed together to produce a beat frequency. By adjusting the temperature of one of the lasers, the frequency was swept from DC to 110 GHz.

The RF power was detected using a Rohde-Schwarz power meter with a frequency range from DC to 110 GHz. A 110 GHz bias tee and an 8-inch W-band 1.00 mm semi-rigid coaxial cable were connected to a 110 GHz GSG microwave probe which was then connected to the PD. The losses associated with the bias tee and RF cables were calibrated out with a 110 GHz vector network analyzer (VNA).

After extracting calibrated losses, we measured a maximum 3-dB bandwidth of 85 GHz at -1 V, and a 3-dB bandwidth of 50 GHz at 0 V. This is important to note because it shows that the photodiode is able to produce high speed RF output power at zero-bias, which is advantageous because it simplifies heat sinking, reduces biasing circuit cost, and improves reliability [4-13].

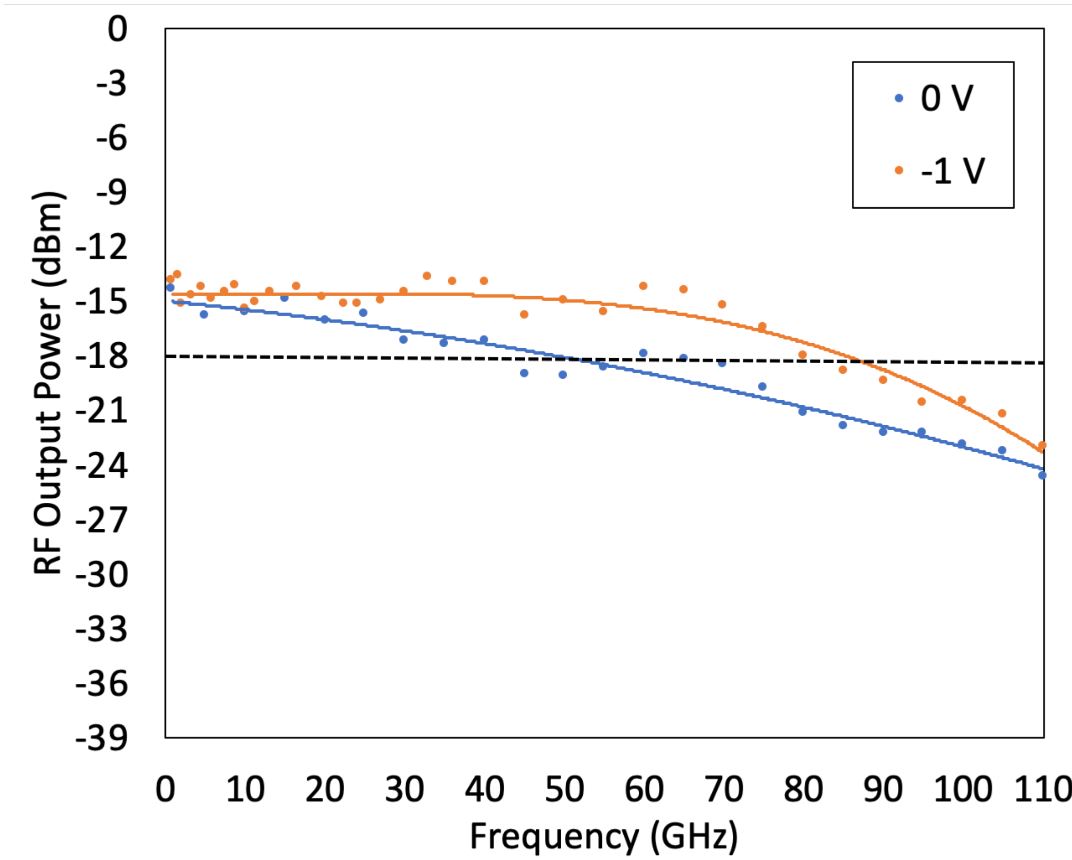


Fig. 4-32. Frequency response of a 5 μm x 7 μm photodiode. Dots represent measured data and curves represent averaged data.

Chapter 5 - High-speed InAs quantum dot waveguide photodiodes heterogeneously integrated on silicon for 1310 nm detection

5.1 Introduction

Future supercomputers and data centers need to be able to keep up with future high-demanding, data-driven applications such as machine learning, virtual reality, and Internet of Things (IoT). More specifically, development of cost-effective integrated photonics with high-volume manufacturability and aggregate bandwidths of many PB/s is necessary for high-speed interconnects in next-generation high-performance computing and fiber-optic communications systems [5-1]. Silicon photonics provides a solution for low-power, high-bandwidth interconnects that are compatible with low cost CMOS electronic processors and memory chips, and has emerged as a new and promising integrated photonic platform in the past decade.

Most silicon PICs typically contain Ge-on-Si photodiodes (PDs) for photodetection in 1310 nm and 1550 nm windows. Silicon-germanium (Si-Ge) p-i-n and avalanche photodiodes have shown significant progress in providing highly sensitive receivers on silicon photonic integrated circuits. However, these PDs often suffer from relatively high dark current and high dislocation densities in comparison to alternatives made from III-V semiconductor materials. Furthermore, to keep power consumption low and enhance high-temperature robustness, avalanche photodiodes (APDs) are integrated on the same chip as the lasers so that the lasers are allowed to operate with smaller output optical power and still be detected with high sensitivity due to the APD's internal gain. But, Si-Ge APDs require high-temperature selective area growth if integrated on the same wafer as lasers made from different materials, complicating the fabrication process and increasing cost [5-2]. Also, due to the indirect bandgap of germanium, Si-Ge lasers are extremely limited in efficiency and have yet to be proven as viable materials to develop lasers on in silicon. Therefore, heterogeneous integration of a direct bandgap material is required to provide a viable gain medium for an efficient laser [5-3].

One way to simplify fabrication cost and complexity is to use the same epitaxial layers for the lasers and the photodiodes. The integration of InAs QDs in GaAs wells as a gain material on silicon has proven to be a promising platform for CMOS-compatible, uncooled on-chip lasers [5-4]. For example, due to the three-dimensional confinement of carriers, QD lasers promise higher temperature stability and lower threshold current densities when compared to quantum well lasers [5-5, 5-6]. In addition, due to the size distribution of the dots, QD lasers have a wide gain bandwidth, which allows for a larger channel count in a WDM link, a particularly attractive feature for comb lasers [5-7].

In this chapter, we report quantum dot (QD) photodiodes heterogeneously integrated on a silicon substrate, made using the same epitaxial layers and fabrication process as that for a recent 1310 nm hybrid QD silicon comb laser with error-free operation for 14-channels [5-8]. These APDs demonstrate an avalanche gain of up to 45 and a gain-bandwidth product of 240 GHz, which are the highest for any quantum dot APDs on silicon. Open eye diagrams up to 12.5 Gb/s were achieved and temperature studies have been done on these APDs, which exhibit high performance up to 60°C, showing that these APDs can be practically used in an uncooled, WDM system on a silicon photonic platform.

5.2 Device Design and Fabrication

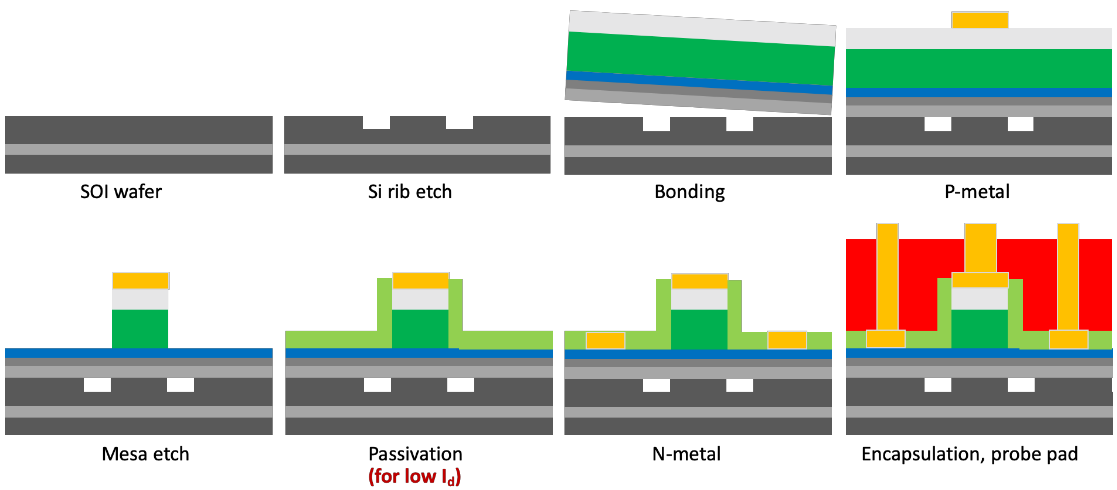
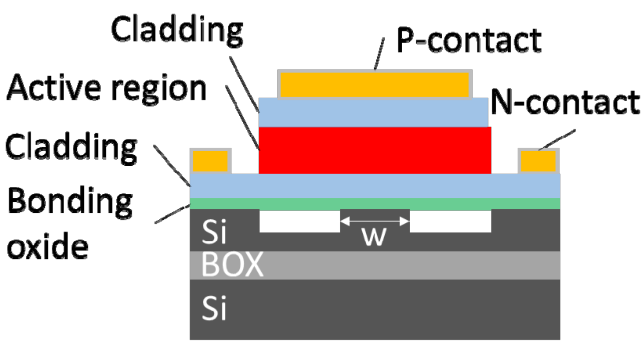


Fig. 5-1. (a) Step-by-step fabrication process of the QD waveguide PDs on silicon.

Fig. 5-1 shows the step by step process taken to fabricate the QD waveguide PDs on silicon. The GaAs QD material was purchased from QD Lasers, Inc. Devices were fabricated on a 100 mm Silicon-on-Insulator (SOI) wafer with a top silicon thickness of 400 nm and a buried oxide thickness of 1000 nm. First, grating couplers and 320 nm thick passive silicon waveguides were etched onto an SOI substrate. Then, a GaAs-based p-i-n epitaxial structure with an active region of 8 layers of InAs QDs, totaling 320 nm in thickness, was bonded directly to the SOI substrate using an O_2 plasma-assisted direct bonding process [5-9].

Next, the Ni/Pd/Au was deposited and then lifted off to define the p-contact. GaAs mesas were made by a mixture of dry etching using $BCl_3/Cl_2/Ar$ and a wet chemistry etching using Citric acid (1 Molar):H_2O_2 (30%), which has a high selectivity to the $Al_{0.4}Ga_{0.6}As$ etch stop layer. Then, the $Al_{0.4}Ga_{0.6}As$ layer was etched in a solution of $K_2Cr_2O_7$:H_3PO_4, which has a high selectivity to the n-GaAs contact layer in the lower cladding. Pd/Ge/Au was deposited followed by lift-off to define the n-contact. Finally, the devices were passivated with 600-nm-thick SiO_2, before vias were formed and probe pad metal was evaporated. Fig. 5-2 shows a cross-section schematic and SEM photo of the device after fabrication. All fabrication steps were carried out at UCSB's nanofabrication facility with Hewlett Packard Labs.



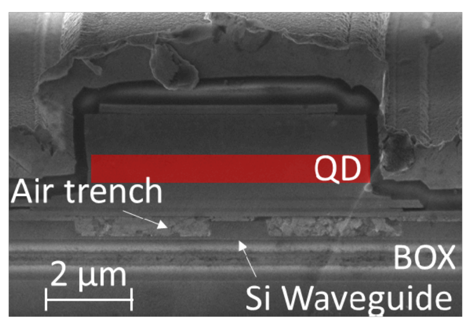


Fig. 5-2. (a) Cross-section schematic of the photodiode. (b) SEM cross-section of the QD waveguide PD on Si.

5.3 Device Results and Discussion

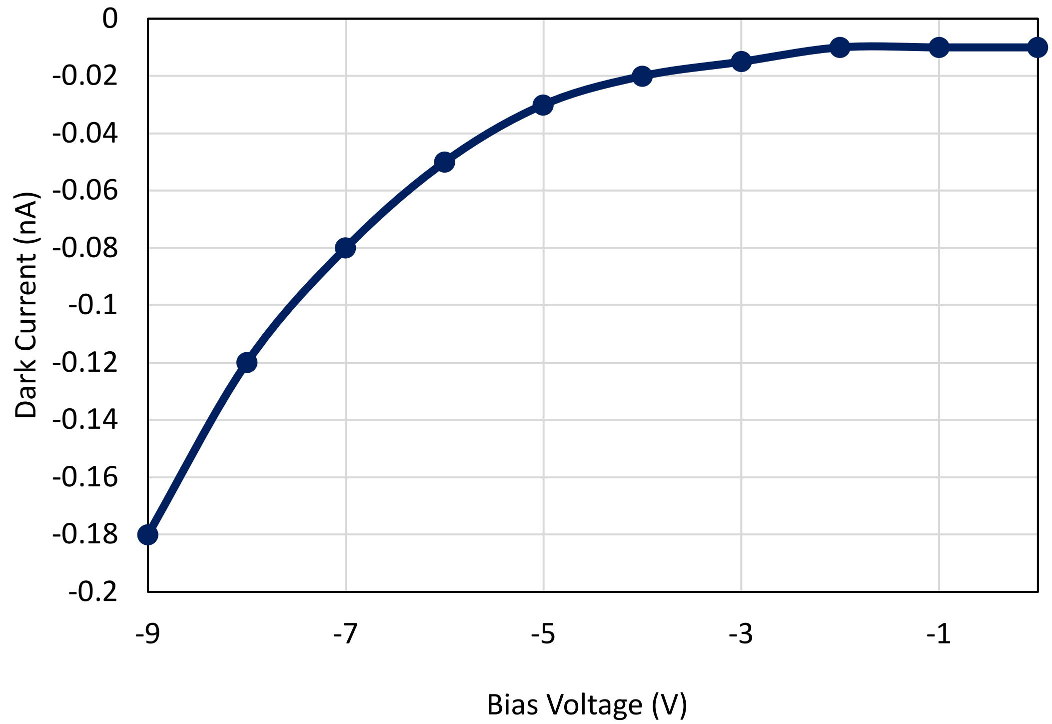


Fig. 5-3. Measured dark current versus bias voltage of an 11 x 60 µm QD on Si waveguide photodiode.

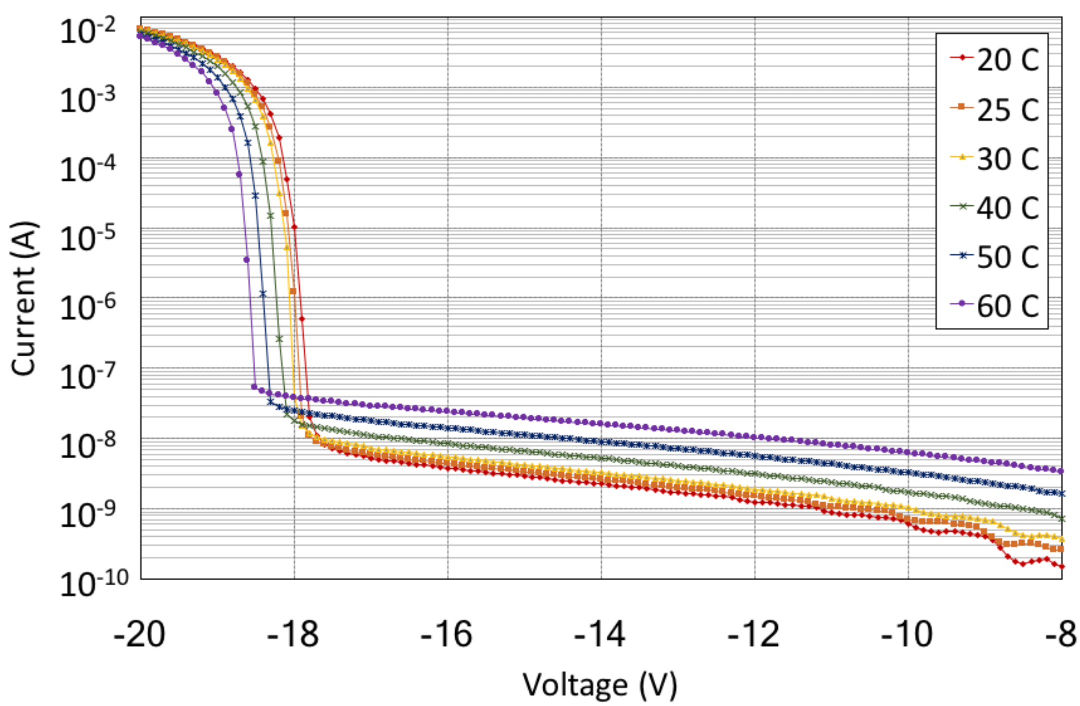


Fig. 5-4. Dark current vs. temperature of an 11 µm × 60 µm device.

Fig. 5-3 shows the dark current measured for an 11 µm x 60 µm PD. A low dark current of 10 pA at -1 V (0.02 pA/µm^2) was demonstrated, which is the lowest dark current reported for any QD PD on Si. This value is three orders of magnitude lower than the lowest ever reported dark current (7 nA at 1 V) in p-i-n Ge-on-Si detectors [5-10]. This can be attributed to the high crystal quality and low dislocation density of the III-V material, as well as, sufficient surface passivation of the PD mesa.

Fig. 5-4 plots the I-V curves of an 11 µm x 60 µm photodiode at different temperatures. The devices were heated using a thermo-electric cooler. The dark current was measured to be 50 µA at a bias near the breakdown voltage. The temperature dependence on the breakdown voltage reveals that impact ionization of free carriers is the primary physical mechanism responsible for the breakdown of the device.

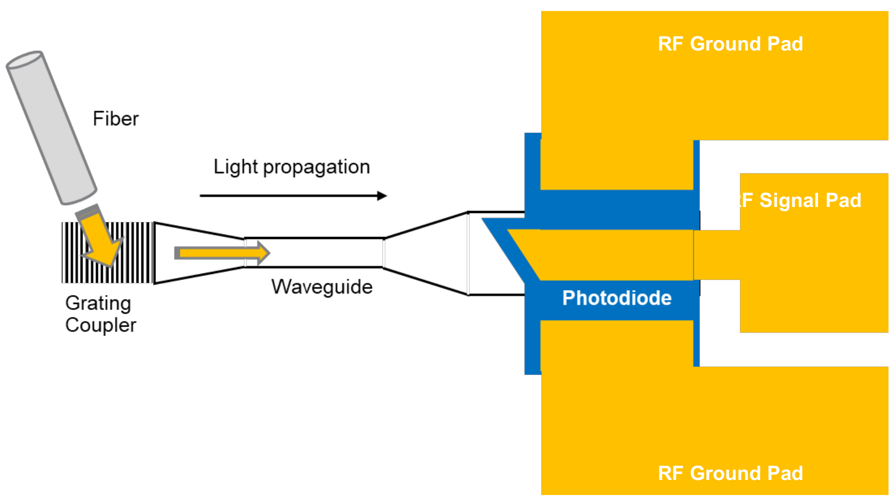


Fig. 5-5. Top-down schematic of the photodiode with a fiber coupled to the input waveguide with a grating coupler.

Fig. 5-5 shows a top-down-view schematic diagram of the PD with a fiber coupling light into an input grating coupler. Light from a 1310 nm laser is coupled from a cleaved fiber into a grating coupler, which then directs the light along a Si waveguide and finally evanescently couples light into the PD above the waveguide.

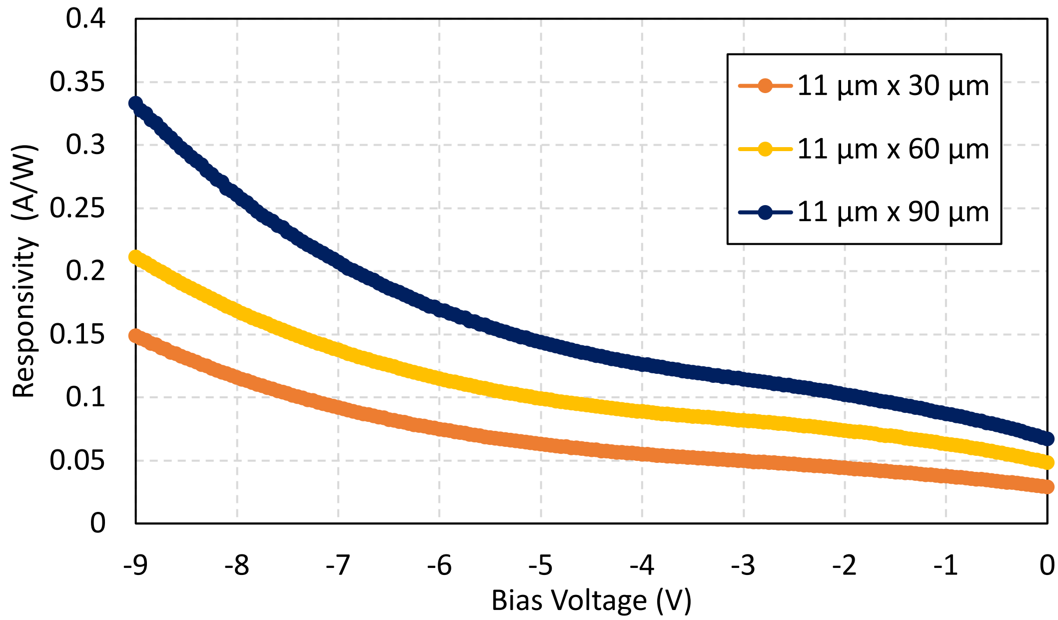


Fig. 5-6. Responsivity at 1310 nm versus voltage bias of QD on Si waveguide PDs of different lengths.

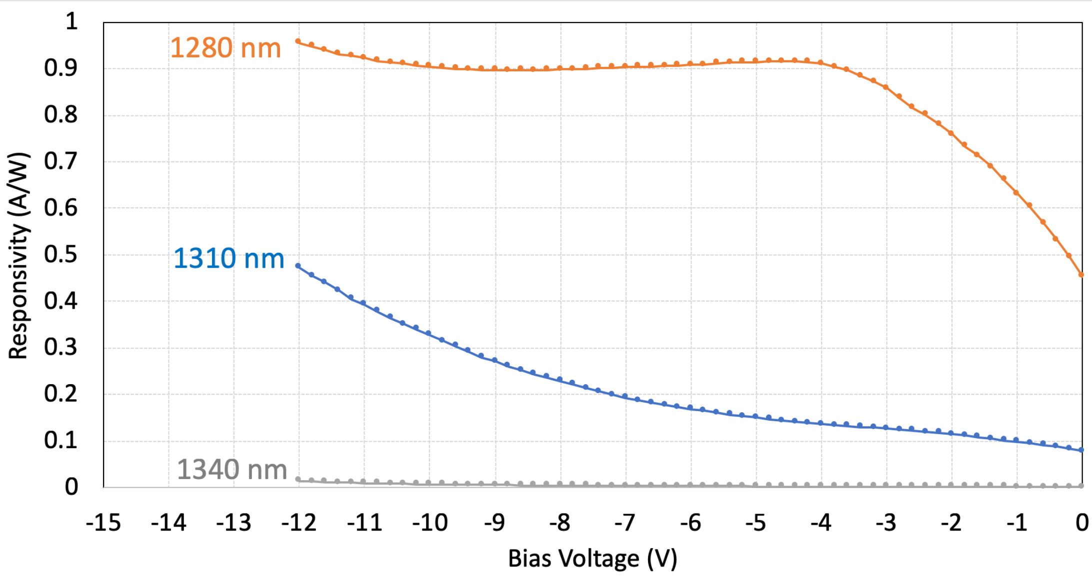


Fig. 5-7. Responsivity of an 11 µm x 90 µm PD at different optical input wavelengths.

The responsivity of 11 µm x 30 µm PD, 11 µm x 60 µm PD, and 11 µm x 90 µm PDs at 1310 nm was measured and is shown in Fig. 5-6. After extracting an estimated loss of 3 dB from fiber coupling and 10 dB from the grating coupler, a responsivity of 0.34 A/W was measured at -9 V for an 11 µm x 90 µm PD.

Fig. 5-7 displays the responsivity with a change in the input optical wavelength. At 1280 nm, unity gain is achieved at -4 V, and avalanche gain begins after -10 V bias voltage.

The spectral response for an 11 µm x 90 µm PD is plotted in Fig. 5-8. Both a wavelength dependence and a bias dependence are seen in the responsivity. The bias dependence on the responsivity at lower biases is due to the quantum confined Stark effect (QCSE), as the electron and hole wavefunctions and energy levels of carriers in the quantum dots shift with an applied electric field [5-11]. However, at higher biases, the bias dependence on the responsivity is due to an increase in gain with applied electric field.

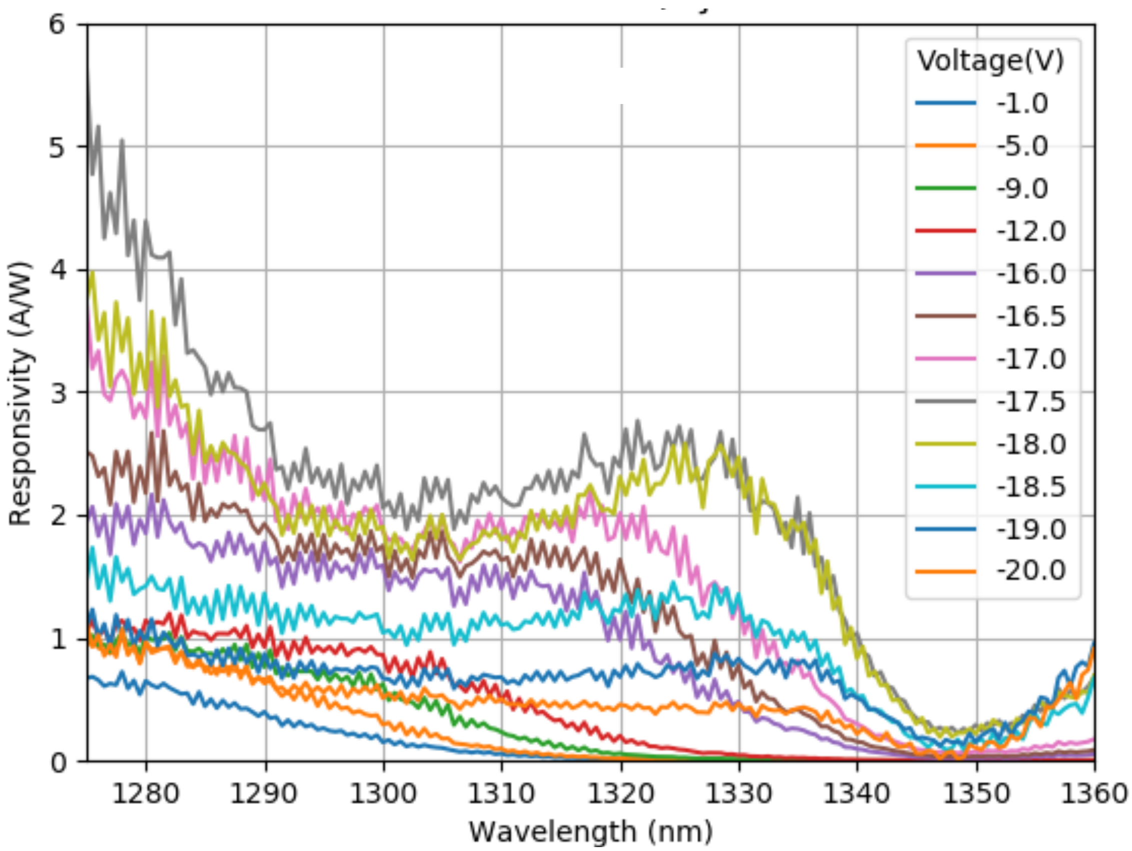


Fig. 5-8. Spectral response versus voltage bias of QD on Si waveguide PDs for a 11 µm x 90 µm PD.

Furthermore, the wavelength dependence on the responsivity at lower biases is simply due to the absorption coefficient of the quantum dot material. At higher biases, it appears that the gain is wavelength dependent, suggesting that the carrier injection and multiplication processes may differ with varying optical input wavelength [5-12]. We believe that avalanche multiplication occurs in the GaAs spacer layers between the QDs [5-13]. However, it also possible that multiplication occurs within the InAs quantum dot material, as suggested in Reference [5-14].

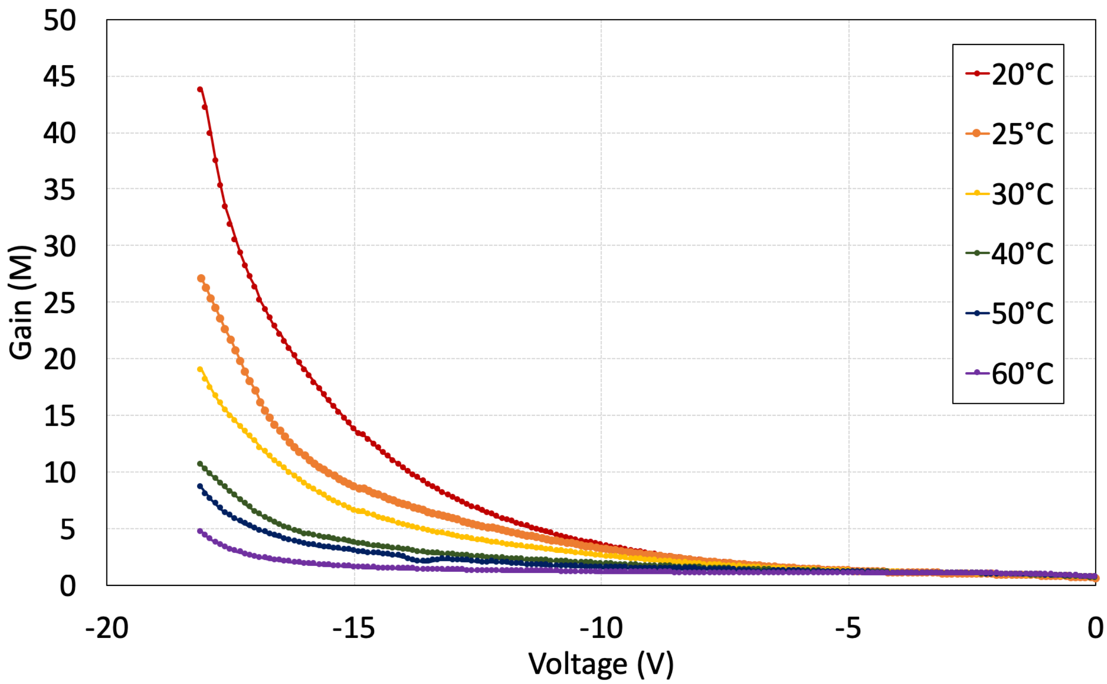


Fig. 5-9. Gain vs. voltage for a 11 μm × 60 μm device at 1310 nm.

The gain of the device at 1310 nm was measured as a function of bias voltage and is shown in Fig. 5-9. The external responsivity at unity gain (at around -4 V) and with 8 dBm optical input power at room temperature is 0.06 A/W, and the maximum external responsivity at room temperature is 2.7 A/W. Temperature dependence on the gain, as well as a decrease in gain at high biases, have been observed and are due to the increase of dark current with temperature and bias. A maximum gain of ~45 was seen at room temperature, with avalanche gain seen up to a stage temperature of 60˚C, displaying the temperature robustness of the devices.

The output frequency response of the PDs was also measured from 0 to -16 V and is plotted in Fig. 5-10 and Fig. 5-11 for an 11 µm x 60 µm PD and an 11 µm x 90 µm PD, respectively. The S21 magnitudes of the PDs were taken at room temperature using an HP lightwave component analyzer (LCA) at an input wavelength of 1300 nm and revealed a maximum 3-dB bandwidth of 8 GHz for a n11 µm x 90 µm PD, 11 GHz for an 11 µm x 60 µm PD, and 15 GHz for an 11 µm x 30 µm PD.

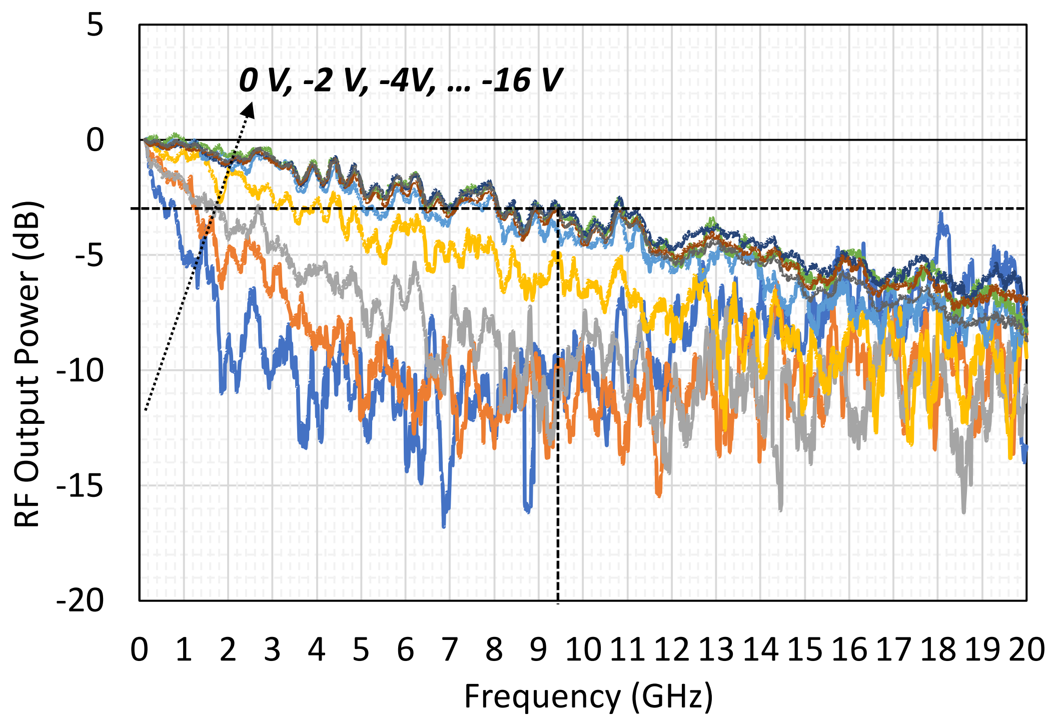


Fig. 5-10. Measured frequency response of an 11 µm × 60 µm APD from 0 to -16 V.

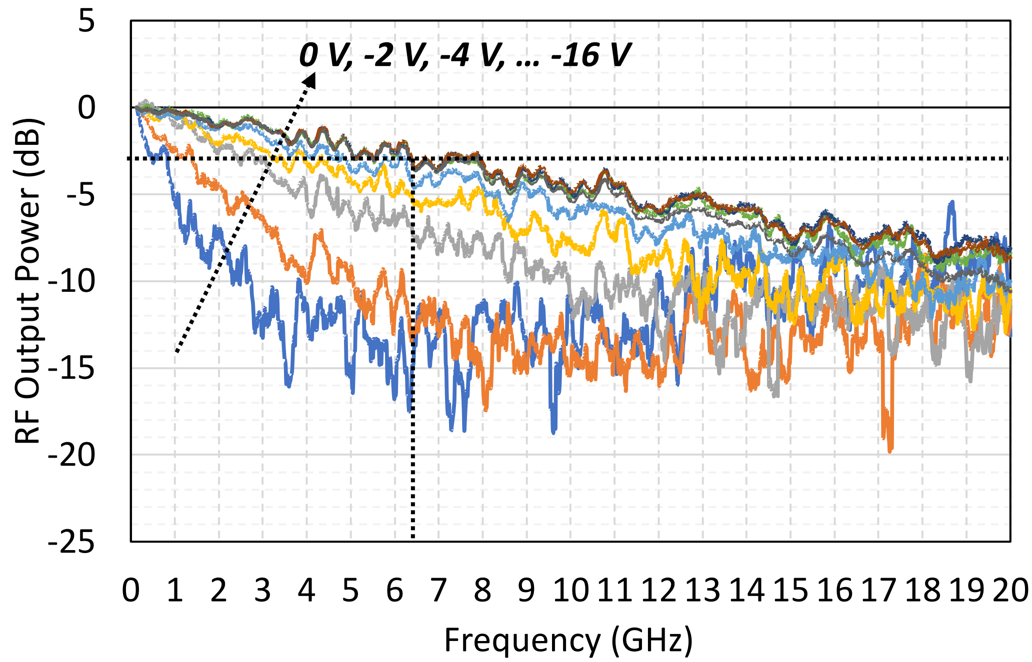


Fig. 5-11. Measured frequency response of an 11 µm × 90 µm PD from 0 to -16 V.

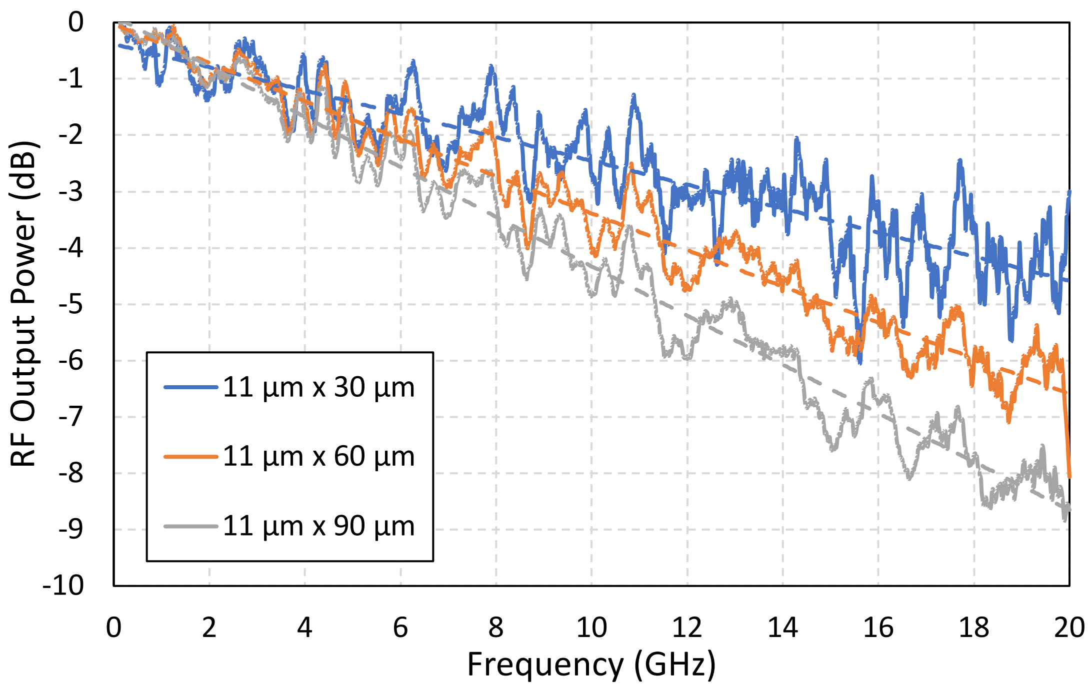


Fig. 5-12. Output frequency response of an 11 µm × 30 µm PD, an 11 µm × 60 µm, and an 11 µm × 90 µm PD measured at -16 V bias voltage (dashed lines are smoothed data).

It can be seen in Fig. 5-10 and Fig. 5-11, that the frequency responses are transit time limited at low biases, and RC limited at high biases, before avalanche gain dominates. At low biases, photogenerated carriers take time to escape from the quantum dots before being collected by the contacts. With an increase in the applied electric field, photogenerated carriers escape from the quantum dots in a shorter period of time [5-15]. With a high enough applied electric field, the frequency response is maximized as it approaches the RC limit of the device.

Fig. 5-12 shows the measured output frequency response with the highest 3-dB bandwidth for three different size PDs. This further illustrates the point that the devices are RC-limited, as the smallest device, which has the lowest capacitance, has the highest 3-dB bandwidth, and the largest device, which has the highest capacitance, has the lowest 3-dB bandwidth.

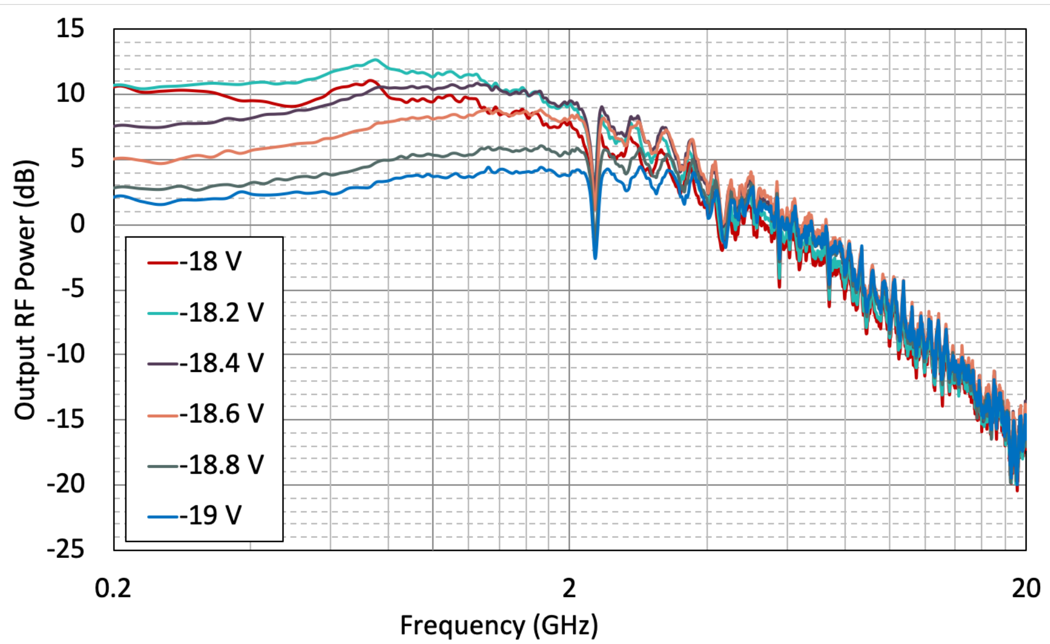


Fig. 5-13. Output frequency responses of a 11 µm × 90 µm PD from -18 V to -19 V.

The frequency response was also measured under bias voltages in which high multiplication gain occurs, as shown in Figure 5-13. An inductive peaking effect was observed, which has been previously explained in other APDs to be caused by impact ionization, which introduces a phase delay between the

AC photocurrent and the applied electric field [5-15].

A maximum gain-bandwidth product (GBP) of 240 GHz was measured at a bias voltage of -18.6 V, as shown in Fig. 5-14. This is higher than most traditional InP-based APDs, which is around 100-200 GHz due to their larger impact ionization coefficient *k* value [5-2]. This number also compares to Ge-on-Si APD counterparts showing higher GBP due to the low *k*-value of Si. But, they often suffer from higher dark currents due to dislocations at the lattice-mismatched Ge/Si interface.

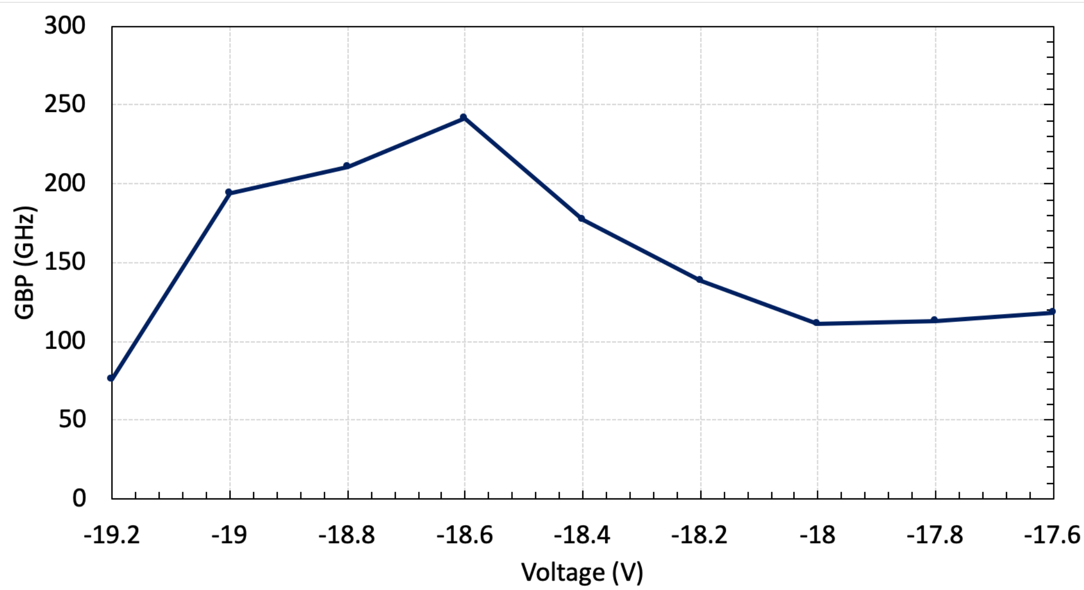


Fig. 5-14. Gain bandwidth product of an 11 μm × 90 μm PD.

These PDs provide enough multiplication gain to produce a sufficiently high signal-to-noise ratio and clear eye diagrams without the need of a transimpedance amplifier (TIA). Fig. 5-15 shows the experiment set-up for eye diagram measurements. A high-speed pseudo-random binary sequence (PRBS) signal was amplified by a 20 dB high-speed power amplifier. Then, a 1310 nm optical signal couples to a PD that is biased through an RF probe and a bias-tee. The output electrical signal is monitored by a DCA86100C sampling scope in the form of an eye diagram.

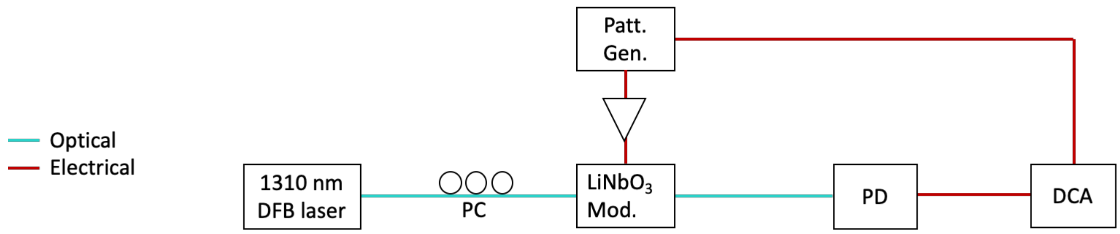


Fig. 5-15. Schematic diagram of experiment set-up for eye diagram measurements.

Figs. 5-16(a)-(c) show the eye diagrams of an 11 μm × 60 μm APD at 5 Gbps, 10 Gbps, and 12.5 Gbps, respectively. At a gain of 40, signal-to-noise ratios greater than 7 dB and 5 dB at 5 Gbps and 10 Gbps were obtained, respectively. We have also obtained open eye diagrams at 12.5 Gbps, as shown in Fig. 5-16(c), where the data rate was limited by the pattern generator.

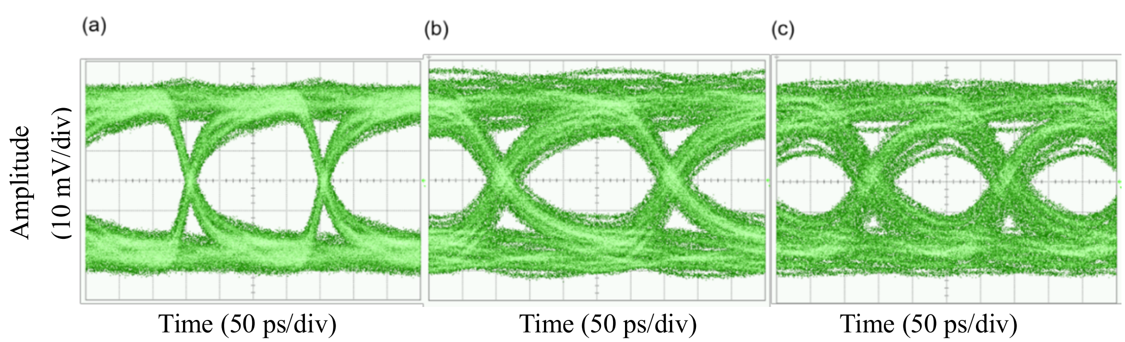


Fig. 5-16. Eye diagrams at a bias voltage of –13 V at (a) 5 Gb/s, (b) 10 Gb/s, and (c) 12.5 Gb/s.

A bit error rate (BER) test was conducted using an Anritsu Bit Error Rate Tester at 10 Gb/s. A schematic of the test set-up for the BER test is illustrated in Fig. 5-17. At a gain of 28, the sensitivity was measured to be approximately -11 dBm at a BER of 1×10^{-12} and -14.6 dBm at a BER of 2.4×10^{-4}, as shown in Fig. 5-18. This sensitivity is a few dB higher than that of a typical Ge-on-Si p-i-n PD [5-16].

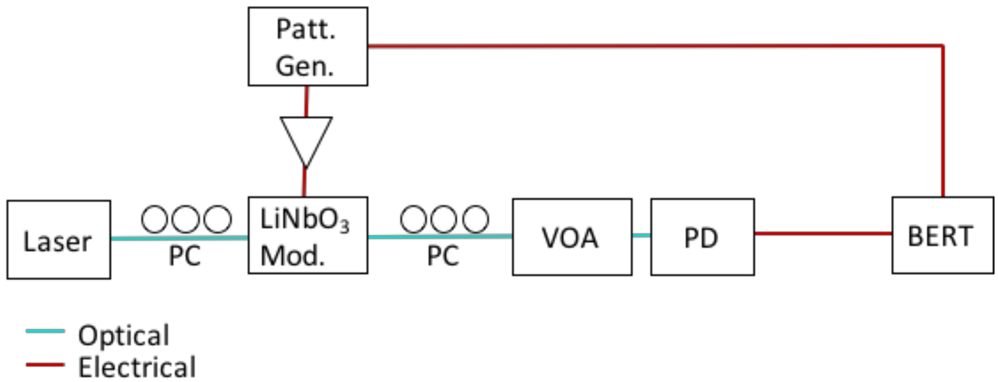


Fig. 5-17. Schematic diagram of experiment set-up for BER measurements.

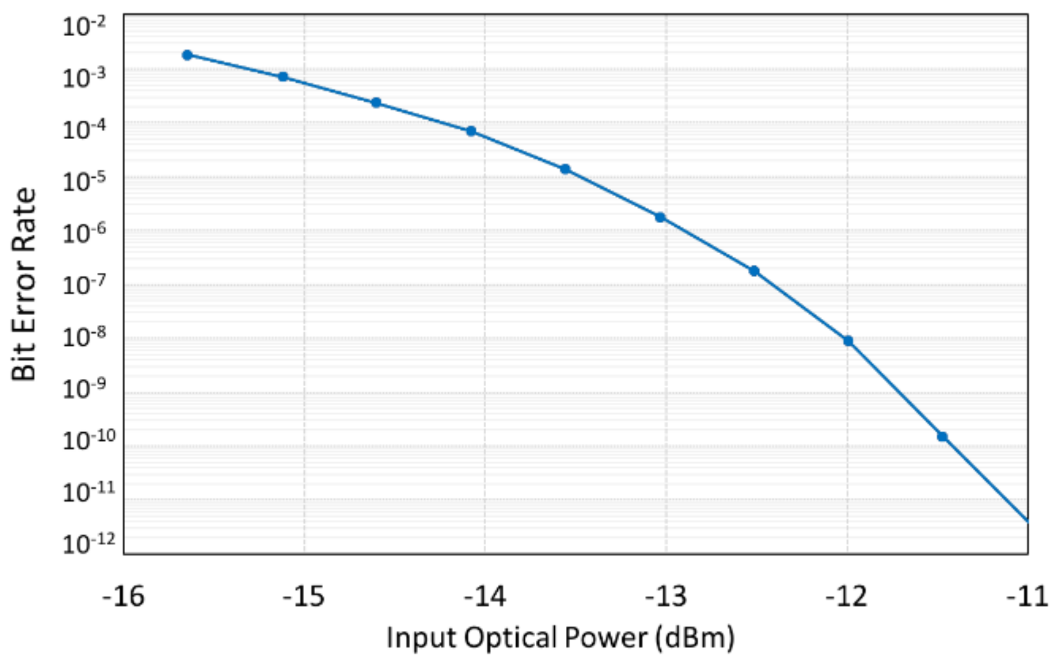


Fig. 5-18. Bit error rate vs. input optical power of a 11 μm × 90 μm PD at a gain of 28.

Lastly, the excess noise factor was measured for an 11 μm x 90 μm PD and is shown in Fig. 5-19. I was unable to extract the *k*-factor since the McIntyre model, which is typically used to determine k factors from measurements of the excess noise, only applies to the case of pure carrier injection [5-17]. This means that only an electron or a hole is injected from the absorption region into the multiplication region of an APD before creating a parent electron-hole pair. However, in these photodiodes, both the absorption and multiplication occur the same region so, both electrons and holes are injected to create parent electron-hole pairs that begin avalanche multiplication processes. Therefore, a different analytical model is needed to analyze the data and extract the *k*-factor.

The excess noise is higher than the case of an APD with pure carrier injection, because the absorption of light inside the multiplication region adds extra gain fluctuations [5-18]. This extra excess noise limits the BER of the photodiode, so it would be advantageous to reduce the excess noise. One way to do so is to create a separate absorption and multiplication region structure, where the photons are absorbed in the absorption region, and only electrons or holes are injected into the multiplication region.

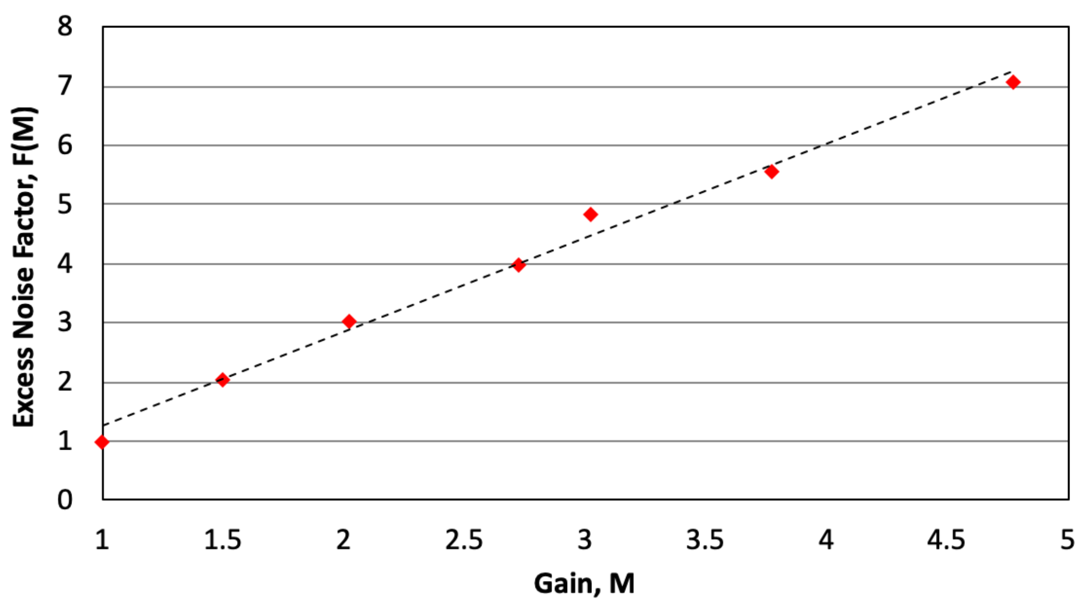


Fig. 5-19. Excess noise factor versus gain of an 11 μm × 90 μm PD.

Chapter 6 - Conclusion and Future Work

6.1 Conclusion

In this dissertation, waveguide-integrated photodiodes (PDs) based on multiple InGaAs/GaAsSb type-II quantum wells (MQW) with capability of efficient high-speed detection at 2 μm have been reported and discussed. Through the modification of the quantum well and barrier thicknesses, and the addition of a novel dual-integrated waveguide-depletion layer, we have designed and fabricated photodiodes with dark current as low as 1 nA at −1 V, maximum internal responsivity of 0.84 A/W and 3-dB bandwidth greater than 10 GHz at 2 μm. Open eye diagrams at 2 μm have also been measured at 1, 5, and 10 Gbit/s. The high-speed carrier dynamics of these photodiodes have been studied and explored for the first time, and reveal that the high-frequency limits in the transit-time-associated frequency response can be attributed to the carrier escape times of light holes in the quantum wells.

High-speed, low-capacitance photodiodes are essential in drastically reducing the power to transport and process high-speed signals down to the attojoule/bit level. By reducing the photodiode capacitance, the photogenerated charges in the photodiode can provide a large enough voltage swing across a high resistance load resistor to directly supply a CMOS logic gate without need of a transimpedance amplifier (TIA) [6-1].

We designed an MUTC photodiode incorporating a novel dual-integrated collection layer-waveguide and a novel fabrication process utilizing planarization SU-8 to produce ultra-low capacitance high-speed integrated waveguide photodiode energy-efficient optical interconnects. Coplanar waveguide RF pads were also designed with minimal parasitic losses and capacitances, in order to minimize any power bottleneck at the interface of the photodiode and an external circuit. We then fabricated and characterized an integrated waveguide MUTC photodiode exhibiting low dark current of 5 nA at -1 V, ultra-low capacitance of 1.8 fF, responsivity of 0.26 A/W, and 3-dB bandwidth of 85 GHz at -1 V, and 50 GHz at zero-bias.

Finally, we demonstrated the first hybrid O-band QD waveguide PDs on silicon. A record low dark current of 0.01 nA at -1 V and record high 3-dB bandwidth of 15 GHz for QD PDs was achieved, as well as, responsivity of 0.34 A/W at -9 V. Avalanche gain was also seen for the first time for any QD photodiode heterogeneously integrated on Si. A maximum gain of up to 45 and a gain bandwidth product of 240 GHz were achieved, which are record high results for any QD APDs on Si. These PDs also achieve a sensitivity of -11 dBm and have demonstrated open eye diagrams up to 12.5 Gb/s and an excess noise factor of ~8 at a gain of 5.

These QD PDs offer a promising alternative to Ge-on-Si counterparts for on-chip monitor PDs and integrated high-speed receivers. They make excellent candidates for p-i-n photodiodes and have shown great potential to be used as avalanche photodiodes (APDs) for WDM links. They also leverage the same epitaxial layers and processing steps as an on-chip laser, which significantly simplifies the processing for a fully integrated transceiver on Si.

6.2 Future Work

6.2.1 Type-II InGaAs/AlGaAsSb MQW Photodiodes Heterogeneously Integrated on Si

Heterogeneous integration offers a valuable platform for active III-V devices on silicon photonic integrated circuits (PICs). In the past, several approaches have been taken for the integration of III-V devices on silicon, including adhesive bonding [6-2], molecular bonding [6-3], and direct growth [6-4]. One advantage of this approach is that it can be used for selective area bonding to integrate multiple different III-V epitaxial layers for different functions on a silicon chip simultaneously. For instance, in [6-3], an InGaAs/InP p-i-n photodetector and a triplexer chip that comprised of an AlInGaAs MQW laser were both bonded on to the same silicon substrate and demonstrated.

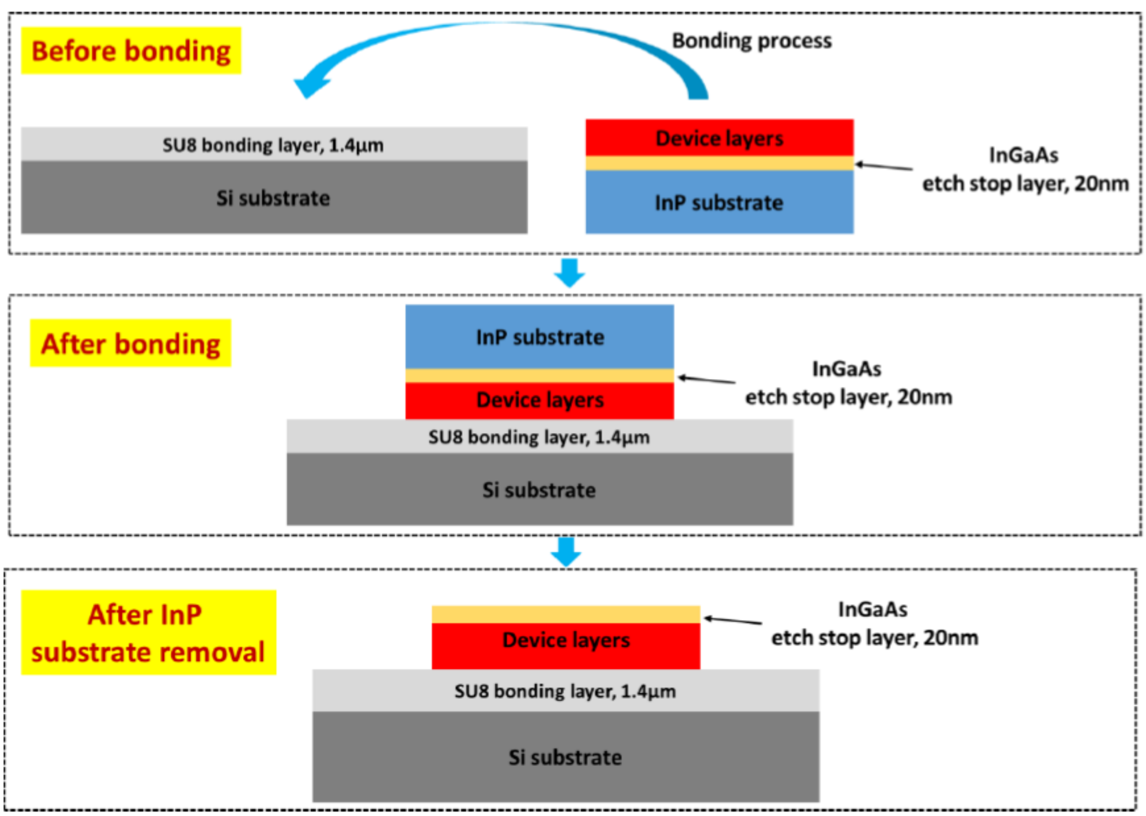


Fig. 6-1. Step-by-step diagram of SU-8 adhesive bonding of III-V on silicon substrate [6-5].

Here, I propose to heterogeneously integrate a Type-II InGaAs/GaAsSb MQW photodiode on silicon, for potential integration with other silicon passive devices and CMOS electrons. We would use an adhesive bonding process based on epoxy-based negative photoresist SU-8 developed in-house in the UVA microfabrication clean room [6-5]. Fig. 6-1 shows a step-by-step diagram of this bonding technique. This approach is particularly attractive because it requires only a low temperature process and can tolerate a considerable amount of surface roughness [6-2]. Before the bonding process, SU-8 is spin coated onto a Si substrate and then soft baked, followed by a 40-minute outgassing, and then cured at 130°C under 10 Psi for 30 min. SU-8 adhesive layers as thin as approximately 260 nm were demonstrated in the past. Fig. 6-2 shows two bonding interfaces of III-V epi stacks on Si that we recently fabricated into fully functional surface normal illuminated PDs for 1.55 µm.

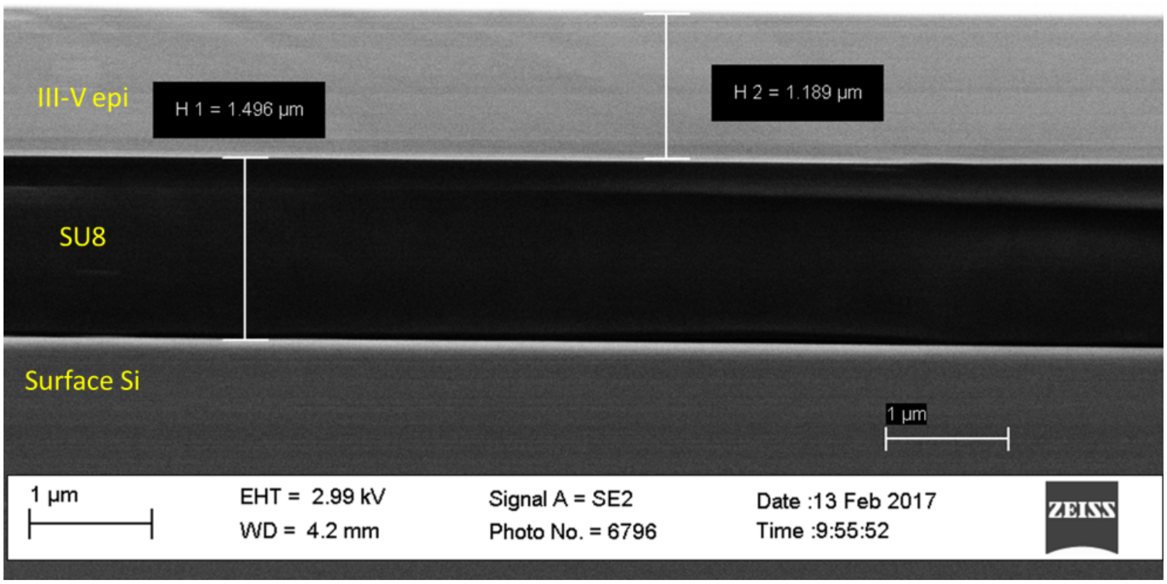


Fig. 6-2. Bonding interface between a Si substrate and III-V chip after bonding with SU-8 [6-5].

Furthermore, to reduce hole escape times we will use quantum well structures with smaller widths and lower barrier heights. Fig. 6-3 shows the band diagrams of lattice-matched InGaAs/GaAsSb MQWs and lattice matched InGaAs/AlGaAsSb MQWs with different Al compositions. By adding Al to the GaAsSb hole wells, a significant reduction in the hole barrier height in the valence band is achieved. For $Al_{0.2}GaAsSb$, preliminary simulations predict a reduction in barrier height of more than 50%. This reduces the effective barrier height for holes, so that photogenerated holes escape from the AlGaAsSb wells quicker than in GaAsSb wells. However, this comes at the expense of an increase in barrier height in the conduction band, which remains to be seen how this will affect the overall carrier transit time of the device. Recently published simulation results suggest that the shortened hole escape time caused by a decrease in the hole barrier height is still slower than the electron escape time with larger electron barrier heights, due to the hole's vastly heavier effective mass [6-6]. This validates the prediction of a larger bandwidth in the device with the use of AlGaAsSb hole wells.

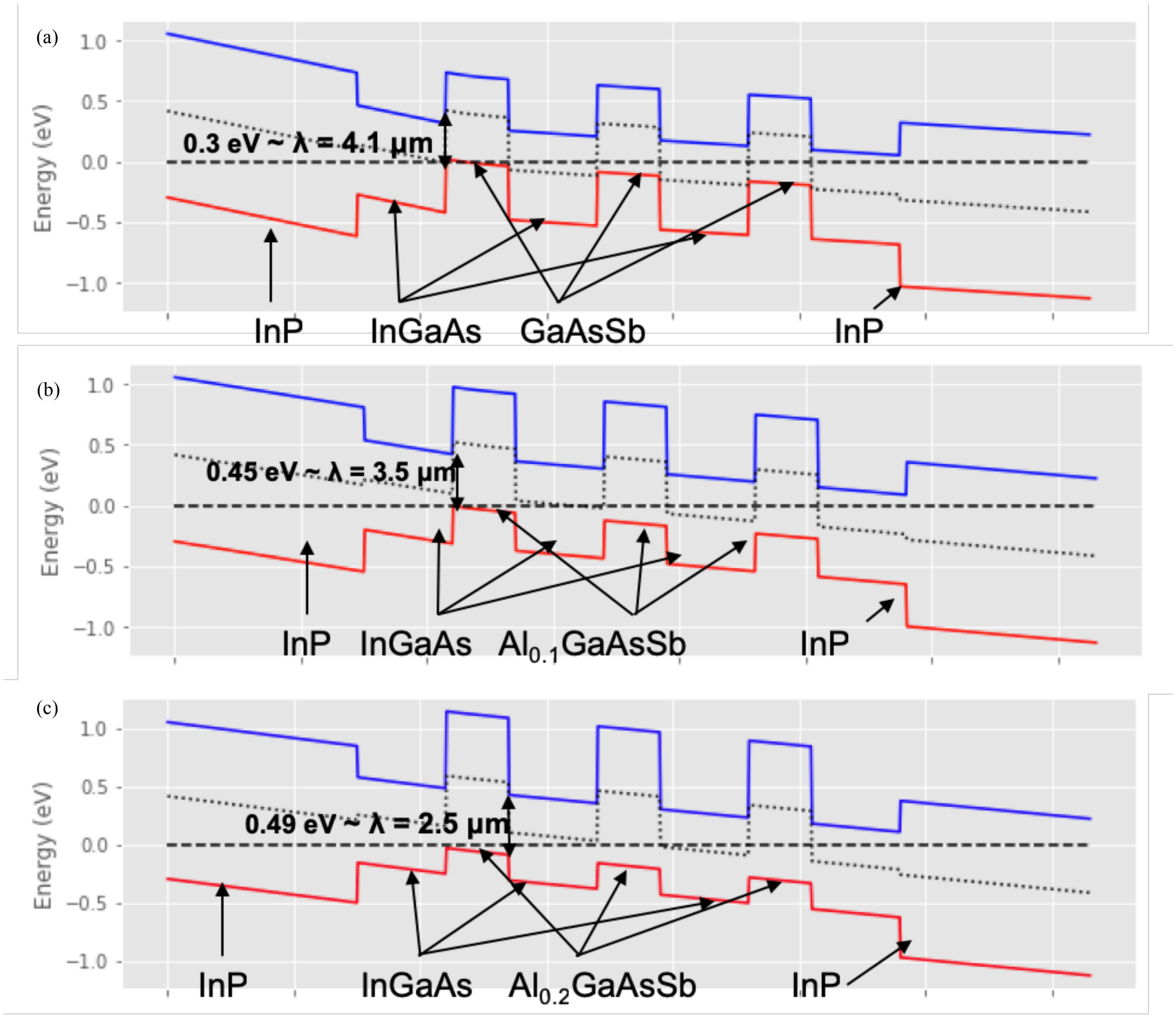


Fig. 6-3. Band diagram of a type-II (a) InGaAs/GaAsSb MQW PD, (b) InGaAs/$Al_{0.1}$GaAsSb MQW PD and (c) InGaAs/$Al_{0.2}$GaAsSb MQW PD.

Fig. 6-4 shows two designs of InGaAs/AlGaAsSb type-II quantum well photodiodes heterogeneously integrated on silicon. Fig. 6-4(a) incorporates a silicon waveguide in order to evanescently couple input light into the photodiode, and Fig. 6-4(b) utilizes the dual-integrated waveguide-depletion layer design from Chapter 3 to couple light into an InGaAs waveguide. In the latter approach, the passive waveguides would be on InP, and the silicon would provide an integration platform with CMOS electronics.

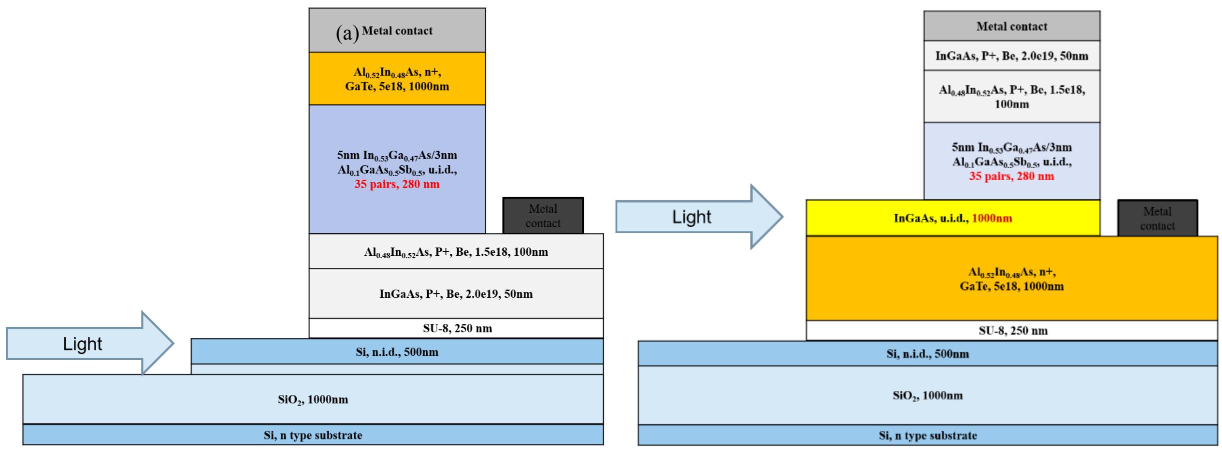


Fig. 6-4 (a) Type II InGaAs/AlGaAsSb MQW photodiode bonded on silicon waveguide, (b) Type II InGaAs/AlGaAsSb
(b)
MQW photodiode with dual-integrated depletion layer-waveguide.

6.2.2 Ultra-low Capacitance MUTC Photodiodes with Improved Waveguides

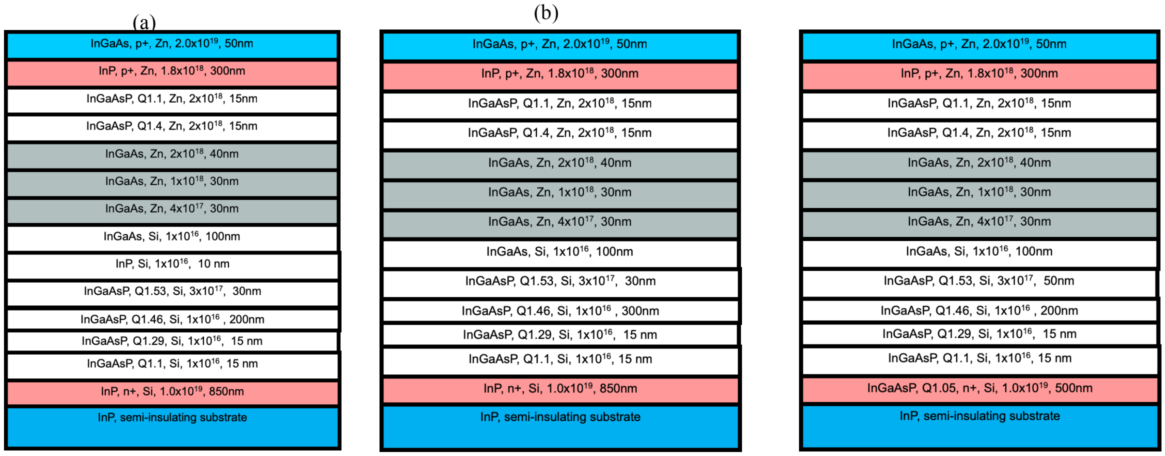
One avenue that needs to be studied to realize the full potential of the ultra-low capacitance MUTC photodiodes demonstrated in Chapter 4 is to refabricate these photodiodes with the proper p-mesa etch depth. As mentioned in Section 4.4, the p-mesa was over etched by 100-150 nm, causing high waveguide losses. The optical mode was no longer mostly confined in the drift layer, but rather, it was guided through the substrate. This drastically reduces the coupling efficiency in between the waveguide and the photodiode, as only a small portion of the light is coupled into the absorber of the photodiode.

In Fig. 6-5, three structures are proposed to help mitigate this issue. Firstly, one way to prevent the p-mesa from being over-etched in the future is to incorporate a etch stop layer, and dry etch partially through the p-mesa and then chemically wet etch the rest of the p-mesa until reaching the stop layer. Fig. 6-5(a) shows a structure that incorporates a InP etch stop layer to be able to stop the p-mesa etch right at the interface of the absorber and the waveguide layers. A 10 nm InP cliff layer was inserted in between the InGaAs depleted absorber and the InGaAsP cliff layer. $H_3PO_4 : H_2O_2 : H_2O$ can be used to wet etch InGaAs and stop at InP. The InP cliff layer will slightly weaken the coupling efficiency, but not significantly. It may also increase the carrier transit time at low applied bias voltages, but with a sufficiently high applied bias voltage, carriers will have enough energy to tunnel through the heterobarrier in between the InGaAs absorber and InP cliff layer quickly.

In addition, the waveguide layers can be made thicker in order to ease the dry etch tolerance. This can be done by either making the drift layer thicker or, by making the n-contact layer high-index, interchanging the substrate to be the lower cladding layer for the waveguide. In the former case, the carrier transit time would be longer, but the bandwidth-efficiency product may still be kept high and the junction capacitance will be further reduced. In Fig. 6-5(b), a design with a thicker drift layer and waveguide is shown.

The structure in Fig. 6-5(c) utilizes a high-index InGaAsP n-contact layer in order to increase the total waveguide thickness, and ease the etch tolerance of the p-mesa. Therefore, we can dry etch partially through the p-mesa and then chemically wet etch the rest of the p-mesa until reaching the stop layer. However, in this design, the optical mode will be slightly pushed down towards the n-contact region, so that the coupling efficiency in between the waveguide and absorber may vary. The photodiode then needs to be slightly longer in order to achieve the same quantum efficiency as the originally intended design. Also, since the optical mode will be partially confined in the n-contact layer, there will be higher free carrier absorption loss in the waveguide. But, as long as the waveguides are kept reasonably short, this may not be a significant issue.

(a) (b)



(c)

Fig. 6-5. Epitaxial layer structure for the dual-integrated waveguide-depletion layer MUTC photodiode (a) with etch stop layer, (b) with thicker drift layer, and (c) with high-index n-contact layer.

After re-fabricating the devices, the high-frequency characteristics of the PD above 50 GHz will need to be measured. This can be done using an optical heterodyne setup using two 1550 nm lasers. S11 and measurements can be done using a Keysight VNA and S21 measurements can be done up to 170 GHz using a VDI frequency extender and a THz VDI power meter in order to measure the photodiodes at frequencies greater than 100 GHz.

6.2.3 SACM and Microring QD APDs heterogeneously integrated on silicon

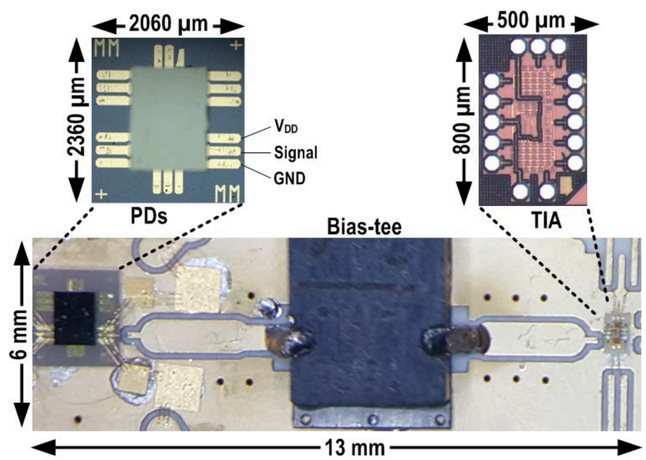


Fig. 6-6. Balanced PDs wire bonded and connected to a TIA [6-7].

One future goal is to decrease the BER and increase the sensitivity of the QD photodiodes. One way to do so, is to wire bond the PD to a TIA with a bandwidth above 15 GHz, as done in a case with balanced photodetectors seen here [6-7]. This TIAs can be supplied by Professor Steve Bowers in the ECE department.

One way to increase the gain and decrease the noise of the QD photodiodes on silicon that were measured in Chapter 5 is to redesign the photodiode as a separate absorption, charge, and multiplication region (SACM) APD. In Fig. 6-7 is shown a SACM structure, wherein the absorption region consists of InAs quantum dots for 1310 nm photodetection, and adjacently lies an $Al_{0.2}Ga_{0.8}As$ charge layer to keep the electric field in the absorption region low so as to not go into avalanche breakdown. Then, adjacent to that is a 100 nm undoped layer of $Al_{0.2}Ga_{0.8}As$ as a multiplication region. So, photons are absorbed and electron-hole pairs are generated inside the QD absorption region, then the photogenerated electrons are injected into the high-field multiplication region and impact ionization begins. This structure should increase gain due to the thick multiplication region. It should also decrease excess noise, and in result, increase sensitivity, since only photogenerated electrons are injected into the multiplication region, which have a higher ionization coefficient than holes in AlGaAs.

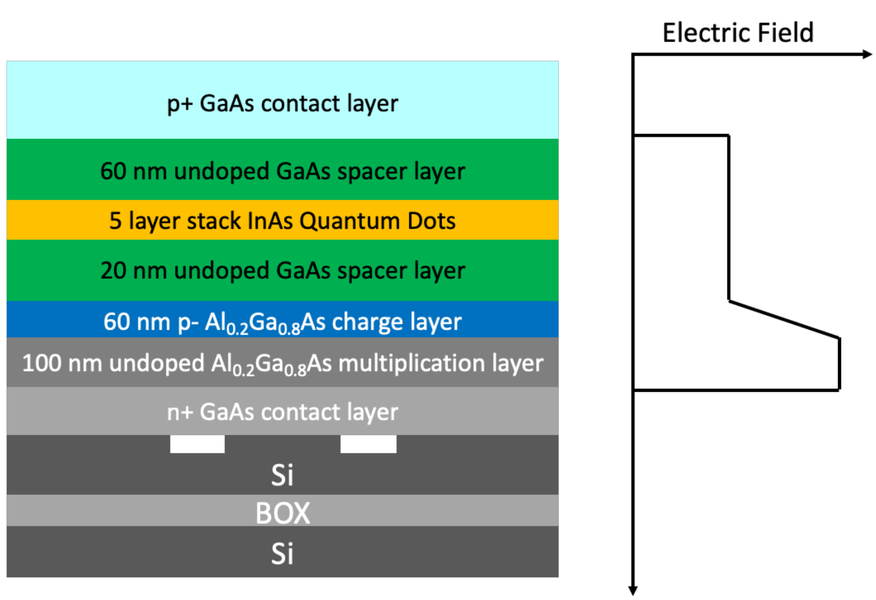


Fig. 6-7. Epitaxial layer structure for the SACM QD APD photodiode heterogeneously integrated on silicon.

Fig. 6-8 shows a model of a microring QD APD, which can be used as a demultiplexer and a photodetector for DWDM (dense wavelength division multiplexing) optical links. In the design, the QD photodiode is shaped bonded on top of and fully, or partially, covering a ring resonator on silicon. The Si ring will couple light from an input bus waveguide and resonate at a specific input wavelength. When the ring resonates, there will be a sharp increase in optical gain, and the light is then coupled into and absorbed by the QD photodiode. Because of the inherent optical gain of the ring resonator, a QD photodiode with a thin absorption region can be designed with short carrier transit time for high-speed operation, while still maintaining high quantum efficiency. The design must also account for the optical losses per roundtrip, as well as, the photon lifetime within the ring. If the photodiode couples a significant amount of the light from the ring, the loss in the ring increases, and the Q-factor decreases which, in turn, decreases the quantum efficiency of the device. Furthermore, if the Q-factor is too high, then the photon lifetime increases, also slowing down the response time of the photodiode.

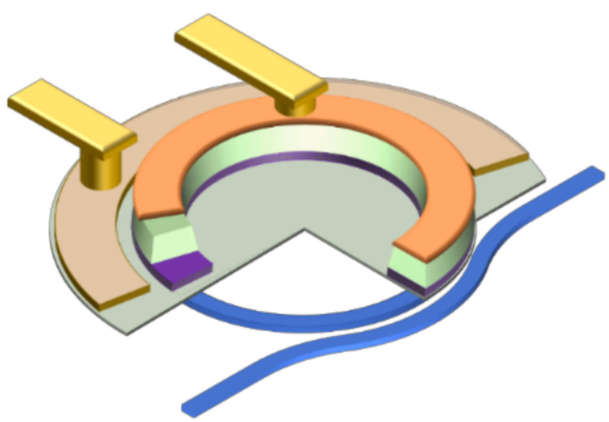


Fig. 6-8. Model of microring QD avalanche photodiode heterogeneously integrated on silicon [6-8].

Appendix A

(MQW Photodiode Fabrication Process for Samples B & C)

1. P-Mesa

1.1 p-metal

- Clean wafer Rinse in Acetone, IPA, DI, nitrogen dry

- O2 plasma Power: 200, Gas: 80, 600sec

- Metal deposition Deposit n metal (rates: 1-2 Ǻ/s)

200Ǻ Ti

300Ǻ Pt

500Ǻ Au

100Ǻ Ti

1.2 Hard mask SiO2

- Clean wafer Rinse in Acetone, IPA, DI

- O2 plasma power: 200, gas: 80, 300 sec

- Filmetrics Film thickness on **Si dummy (with metal)** before deposition:

- PECVD Clean process and then conditional run

Process "SIO2P35T" (TBD):

- Filmetrics **Film thickness on Si dummy (with metal) after deposition:**

- Clean wafer Rinse in Acetone, IPA, DI

- O2 plasma Power: 200, gas: 80, 600sec

- Lithography Spin HMDS, spin resist AZ5214, and **soft bake 100C 2 min**

(40sec, 3000rpm → 1.4~1.6 um) TBD

Exposure **"P-Mesa"**: Align & Expose, hard contact, 376W, 55sec ________

Develop **AZ300MIF 30 sec** (agitate)

Post bake 110C, 50 sec

Alphastep PR thickness (TBD):

- O2 plasma power: 150, gas: 80, 200sec

- SiO2 dry etch Oxford/Trion, Process "Chong_SiO2", and Press: 50, ICP power: 25, RIE power: 70, He press: 3

Rate: 350 nm/600 sec, selectivity SiO2: PR = 1:2.2, time (TBD)

(Use three dummies to monitor the thickness of the SiO_2)

Alphastep PR+SiO2 thickness (TBD):

Alphastep PR+SiO2 thickness (TBD):

Alphastep PR+SiO2 thickness (TBD):

Alphastep PR+SiO2 thickness (TBD):

[- BOE wet etch (If PR thin)]

- Clean wafer Remove PR: Acetone, IPA, DI

- O2 plasma power: 200, gas: 80, 300 sec

- Alphastep SiO2 thickness (TBD): ____________________on Dummy (TBD)

1.3 P Mesa dry etch

- Conditional run Oxford ICP RIE, Process “OPT-InP Etch (Cl2/N2)” 3 min at 50C

with 4 in Si/SiO2 carrier wafer

- ICP RIE dry etch Process “OPT-InP Etch (Cl2/N2)-EP”, wafer on Grease, see laser

monitor

Time ___________________ wafer_____________________ dummy___________________

Time ___________________ wafer_____________________ dummy___________________

Time ___________________ wafer_____________________ dummy___________________

Time ___________________ wafer_____________________ dummy___________________

Time ___________________ wafer_____________________ dummy___________________

Use 4 in Si wafer for cleaning after finish.

-Alphastep SiO2+metal+n-mesa thickness (~ μm): _______________________________

2. Waveguide

2.1 Hard Mask PR

- Lithography Spin HMDS, spin resist AZ5214:soft bake 100C 2 min:

(40sec, 3000rpm → 1.4~1.6 um) TBD

Exposure **“Waveguide”**: Align & Expose, hard contact, 376 W, time: 55sec__

Develop AZ300MIF 30 sec (agitate)

Post bake 110C, 50 sec:

Alphastep PR thickness (TBD):

- O2 plasma power: 150, gas: 80, 200sec

2.2 Waveguide Dry etch

- Conditional run Oxford ICP RIE, Process “OPT-InP Etch (Cl2/N2)” 3 min at 50C

with 4 in Si/SiO2 carrier wafer ____

- ICP RIE dry etch Process “OPT-InP Etch (Cl2/N2)-EP”, wafer die on grease, see laser

monitor

Time __________________ wafer____________________ dummy__________________

Time __________________ wafer____________________ dummy__________________

Time __________________ wafer____________________ dummy__________________

Time __________________ wafer____________________ dummy__________________

Time __________________ wafer____________________ dummy__________________

Use 4 in Si wafer for cleaning after finish.

- Clean wafer Rinse in Acetone, IPA, DI

- O2 plasma Power: 200, gas: 80, 600sec

-Alphastep Waveguide thickness (~ µm): ____

3. Mesa Passivation

3.2 SiO2 Passivation

- Clean wafer Rinse in Acetone, IPA, DI

- O2 plasma power: 200, gas: 80, 300 sec

- Filmetrics Film thickness on **Si dummy (with metal)** before deposition: ________________

- PECVD Clean process and then conditional run

Process “SIO2P35T” (TBD): ________________________________

- Filmetrics **Film thickness on Si dummy (with metal) after deposition:** ______________

- Clean wafer Rinse in Acetone, IPA, DI

- O2 plasma Power: 200, gas: 80, 600sec

- Lithography Spin HMDS, spin resist AZ5214, and **soft bake 100C 2 min**

  (40sec, 3000rpm → 1.4~1.6 um) TBD

  Exposure **"N-Mesa"**: Align & Expose, hard contact, 376W, 55sec _______

  Develop **AZ300MIF 30 sec** (agitate)

  Post bake 110C, 50 sec

- Clean wafer Acetone, IPA, DI, slow bake out 5 min 90C, 5 min 110C

- O2 plasma power: 200, gas: 80, 300 sec

- Alphastep SiO2 thickness (TBD): ____

4. N-Metal

4.1 Open N-contact layer

- Clean wafer Acetone, IPA, DI, nitrogen dry

- O2 plasma power: 200, gas: 80, 300 sec

- Lithography Spin HMDS, spin resist AZ5214, soft bake 100C 2 min

  (40sec, 3000rpm → 1.4~1.6 um) TBD

  Exposure **"N-Metal"**: Align & Expose, hardncontact, 376 W, time: 55sec

  Develop AZ300MIF 30 sec (agitate)

  Post bake 120C, 50 sec

  Alphastep PR thickness (1.5µm thick): ___________________________________

- SiO2 dry etch Trion, Process “Chong_SiO2”, Press: 50, ICP power: 25, RIE power: 70, He press: 3

Rate: 350 nm/600 sec, selectivity SiO2: PR = 1: 2.2, ____________________

- Alphastep PR+SiO2 thickness: _________________________________

- O2 plasma power: 200, gas: 80, 300 sec

4.2 N-contact Etch

- Conditional run Oxford ICP RIE, Process “OPT-InP Etch (Cl2/N2)” 3 min at 50C

with 4 in Si/SiO2 carrier wafer

- ICP RIE dry etch Process “OPT-InP Etch (Cl2/N2)-EP”, wafer die on grease, see laser monitor

Time __________________ wafer____________________ dummy__________________

Time __________________ wafer____________________ dummy__________________

Time __________________ wafer____________________ dummy__________________

Time __________________ wafer____________________ dummy__________________

Time __________________ wafer____________________ dummy__________________

Use 4 in Si wafer for cleaning after finish.

4.2 Deposit metal

- O2 plasma power: 200, gas: 80, 300 sec ___________________________________

- Metal deposition Deposit 200Å Ti (1Å/s), 300Å AuGe (1 Å/s), 800Å Au (1Å/s), 300A Ni (1Å/s)

- Lift-Off Acetone soak + Ultrasonic

5. Via (open P-contact)

- Clean wafer Acetone, IPA, DI,

- O2 plasma power: 200, gas: 80, 300 sec

- Lithography Spin HMDS, spin resist AZ5214: 40sec, 3000rpm, soft bake 100C 2 min:

(40sec, 4000rpm → 1.2~1.4 um) TBD

Exposure **"P-Mesa Open"**: Align & Expose, hard contact, 376 W, 50 sec

Develop AZ300MIF 30 sec (agitate)

Post bake 110C, 50 sec

Alphastep PR thickness: ____

- O2 plasma power: 200, gas: 80, 600 sec

- SiO2 dry etch Trion, Process "Chong_SiO2", Press: 50, ICP power: 25, RIE power: 70, He

press: 3 rate: 350nm/600sec, selectivity SiO2: PR = 1: 2.2, **(TBD)**

___________sec______

- Alphastep PR+SiO2 thickness: ____

- I-V Test Measure I-V characteristics on larger-area PD:

I=1mA @ ______V Idark = ______@ ______V

I=1mA@ ______V Idark = ______@ ______V

I=1mA @ ______V Idark = ______@ ______V

6. SU8

- Clean wafer Acetone, IPA, DI, slow bake out 5 min 90C, 5 min 110C

- O2 plasma power: 200, gas: 80, 300 sec

- Lithography Spin HMDS, bake 15min 90C

Dispense SU8-5, spin 5sec 0-500rpm, 30sec 2000rpm

Edge-bead removal with razor blade

soft bake 2min 90C

Align & Expose, hard contact, 376 W, time: 35 sec

Post-exposure bake (PEB) 2min 90C ____

SU8 Developer 1min, rinse in IPA_________

Step SU8 thickness (2.5μm thick): ____

SU-8 Hard bake for 15-20 min at 120C

6. Pad Metal and Plating

- Clean wafer Acetone, IPA, DI, blow nitrogen
- O2 plasma power: 200, gas: 80, 600 sec
- Lithography Spin HMDS, spin resist AZ5214: 40sec, 3000rpm, soft bake 100C 2 min:

(40sec, 4000rpm → 1.2~1.4 um) TBD

Exposure **"Seed"**: Align & Expose, hard contact, 376 W, time: 55 sec

Develop AZ300MIF 30 sec (agitate)_________Post bake 110C, **10min (tbd)**

Alphastep PR thickness (1.6μm thick): ____________________________________

- O2 plasma power: 200, gas: 80, 300 sec
- Metal deposition Deposit 150Å Ti (1Å/s), 500Å Au (1Å/s),
- O2 plasma power: 200, gas: 80, 300 sec
- Lithography Spin HMDS, spin resist AZ5214: 40sec, 3000rpm

Soft bake 90C 60sec **STOP when BUBBLES APPEAR!**

Exposure **"Plating"**, Align & Expose, hard contact, 376 W, time: 55 sec

Develop AZ300MIF 30 sec (agitate)

Alphastep PR thickness (3.2µm thick): ________________________________

- O2 plasma power: 200, gas: 80, 300 secs

- Plating 25E Technics (ready-to-use), 50C,

Set current: 1mA, V: 0.04V ~ 0.05V, (~0.7µm/10min)

Total plating time~40min for 2.8µm thick plated gold

Time=__________I=____________V=___________Step=______________

Time=__________I=____________V=___________Step=______________

Time=__________I=____________V=___________Step=______________

Time=__________I=____________V=___________Step=______________

[- O2 plasma remove top PR layer, power: 150, gas: 80, ~4 hours 40 min

- Alphastep PR thickness ____

- Seed layer etch Gold etch HG400 to remove Au seed layer

- Lift-Off Acetone soak + Ultrasonic (large Ultrasonic 45 units) 10min

7. Cleaving

- Mount Mount wafer on cleaving tool____

Appendix B

(MUTC Photodiode Fabrication Process)

1. P-Mesa Etch

1.1 P-metal

- Clean wafer Rinse in Acetone, IPA, DI ____ (_)(_)(_)

  slow bake-out 5min 90C, 5min 110C ______________________________ (_)(_)(_)

- O2 plasma power: 200, gas: 80, 600sec ____________________________________ (_)(_)(_)

- Metal deposit Ti: 300-Å (1.0 A/s); ____ spin(_)

  Pt: 500-Å (1.0 A/s); ____ spin(_)

  Au: 2000-Å (1.0 Å/s);____ spin(_)

  Ti: 200- Å (1.0 A/s); ____ spin(_)

- Dektek Si Dummy (~132 nm); ____

1.2 Hard mask SiO_2

- Clean wafer Acetone, IPA, DI, slow bake-out 5min 90C, 5min 110C ______________ (_)(_)(_)

- PECVD process “SIO2P35T” (deposition rate ~ 12.5 nm/min) FUTC 40 min (~ 540 nm)__ (_)(_)(_)

- Filmetrics Film thickness on dummy Si after deposition:

  ____

- Clean wafer Acetone, IPA, DI, slow bake-out 3 min 100C ______________________ (_)(_)(_)

- O_2 plasma power: 200, gas: 80, 600 sec ____________________________________ (_)(_)(_)

- Lithography Spin HMDS, spin resist NR7-250P: 40sec, 1000rpm, soft bake 160C 1 min_______(_)(_)(_)

"Mask 1"

Exposure mask "p-mesa": WEC, Align & Expose, Vac contact, 376W, time: 2 sec ____ (_)(_)(_)

Post exposure bake 100C, 60 sec ____ (_)(_)(_)

Develop in RD 6 for 30 sec (agitate) ____________________________ (_)(_)(_)

Post bake 110C, 2 min _______________________________________ (_)(_)(_)

Dektek PR thickness (~0.6μm thick): __________________________________

____

- SiO2 dry etch Oxford: "JCC CHF3 SiO2 etch" (etch rate ~ 20 nm/min)________ (_)(_)(_)

Calculation(~ 35 min) ____

- Remove Resist O_2 plasma several hours (PR is hardened by the dry etching process) _____ (_)(_)(_)

1.2 P-mesa dry etch

- O2 plasma power: 200, gas: 80, 300 sec __________________________________ (_)(_)(_)

-Dektek SiO2 thickness (~400nm): ______/_______/______on Dummy (0nm): ___________

- Oxford clean Use 4-in Si wafer for chamber cleaning (20 – 50° C) **(critical)** __________________

- Oxford ICP RIE Conditional: "OPT-InP Etch with (Cl2/N2) EP-50C" 3 min at 50° C w/4-in Si carrier wafer

- ICP RIE dry etch "OPT-InP Etch-EP-50C", wafer die w/ L-Grease, see laser monitor

1000 W metal etch

250 W for III-V etch (III-V etch rate 137~150 nm/min; SiO_2 etch rate 20 nm/min)________________________________

____

- SiO2 Filmmetics SiO_2 Dummy thickness (~ 200 nm): ____________________________________

- metal Dektek p-metal thickness (~ 300 nm): ____

- Dektek SiO_2 + metal + p-mesa height (~1.2 to 1.5 µm): ______________________________

- P-mesa height (0.8 µm < x < 1.2 µm): ____

- Mesa wet etch Surface damage layer removal in Bromial acid (2 ~ 3 sec) (lower the dark current by 1 order of magnitute; Do **NOT** over-do since this etch shrinks the mesa size)

2. Waveguide Etch

2.1 Hard Mask PR

- Clean wafer Rinse in Acetone, IPA, DI _______________________________________ (_)(_)(_)

- O2 plasma power: 200, gas: 80, 300 sec _____________________________________ (_)(_)(_)

  - Clean wafer ____ Acetone, IPA, DI, 3 min 100C ____ (_)(_)(_)

- Lithography Spin/Steam HMDS, spin resist AZ5214: 40sec, 3000rpm, soft bake 100C 2 min: (_)(_)(_)

  "Mask 1"
  Exposure mask "Waveguide": WEC, Align & Expose, hard contact, 376W, time: 55 sec (_)(_)(_)

  Develop AZ300MIF 30 sec (agitate) _________(_)(_)(_) Post bake 110C, 50 sec: (_)(_)(_)

  Dektek PR thickness (1.6µm thick): ____

2.2 Waveguide Dry etch

- Oxford clean Use 4-in Si wafer for chamber cleaning (20 – 50° C) **(critical)** ___________________

- Conditional run Oxford ICP RIE, Process "OPT-InP Etch With Epi-50C" (Cl2/N2) 3 min at 50 ˚C _ with 4-in Si carrier wafer ____

- ICP RIE dry etch Process "OPT-InP Etch-EP", wafer die on L-Grease, see laser monitor ___________ (~ 5 min) ____

- Remove PR: O_2 plasma several hours (PR hardened by the dry etch) _______________

3. N-Mesa

3.1 N-mesa dry etch

- Clean wafer Acetone, IPA, DI, slow bake out 3 min 100C ________________________________

- Lithography Spin/Steam HMDS, spin resist AZ5214: 40sec, 3000rpm, soft bake 100C 2 min: (_)(_)(_)

  "Mask 1"
  Exposure mask "N-mesa": Align & Expose, hard contact, 376W, time: 55 sec______ (_)(_)(_)

  Develop AZ300MIF 30 sec (agitate) _________(_)(_)(_) Post bake 110 ˚C, 50 sec: (_)(_)(_)

  Dektek PR thickness (1.6µm thick): ____

- ICP RIE dry etch Process "OPT-InP Etch-EP", wafer die on 3 drops Fomblin oil, see laser monitor ___ (~ 5 min; **Do** over-etch into the S.I. substrate) ________________________________

  - Remove PR: O_2 plasma several hours (PR hardened by the dry etch) ________

  - Dektek: SiO_2 + n-mesa height: ____________________________________

  - I-V test: I > 10^{-9} A @ 1V (low current due to high contact resistance between probe tip and n-mesa).

- O2 plasma power: 200, gas: 80, 300 sec _____________________________________ (_)(_)(_)

  Dektek PR+SiO2 thickness (~1.9µm thick): ________________________________

  ____

4. N-Metal

- Clean wafer Acetone, IPA, DI, slow bake out 3 min 100C _________________________ (_)(_)(_)

- O2 plasma power: 200, gas: 80, 300 sec _____________________________________ (_)(_)(_)

- Lithography Spin/Steam HMDS, spin resist AZ5214: 40sec, 3000rpm, soft bake 100C 2 min: (_)(_)(_)

  "Mask 1"
  Exposure mask "N-metal": WEC, Align & Expose, hard contact, 376W, time: 55 sec _ (_)(_)(_)

Develop AZ300MIF 30 sec (agitate) _________(_)(_)(_) Post bake 110C, 50 sec: (_)(_)(_)

- Dektek PR thickness (1.6µm thick): ____

- O2 plasma power: 200, gas: 80, 600 sec _____________________________________ (_)(_)(_)

4.2 Deposit metal

- Metal deposit AuGe: 300-Å (1.0 A/s);
spin(_) ____ Ni: 200-Å
(1.0 A/s); spin(_) ____ Au: 800-Å
(2.0 Å/s); spin(_)

- Lift-Off Acetone soak + Ultrasonic (small Ultrasonic 20-50 units) 10 min__________ (_)(_)(_)

- I-V Test Measure I-V characteristics on larger-area PD and testing pad:
__ (_______): _____V @ 1mA, _____mA @ -1V; (_______): _____V @ 1mA, _____mA @ -1V

(_______): _____V @ 1mA, _____mA @ -1V; (_______): _____V @ 1mA, _____mA @ -1V

- Clean wafer Acetone, IPA, DI, slow bake out 5 min 90C, 5 min 110C _______________ (_)(_)(_)

- O2 plasma power: 200, gas: 80, 300 sec _____________________________________ (_)(_)(_)

5. SU-8 Spin and Planarization

- Clean wafer Acetone, IPA, DI, blow nitrogen, slow bake out 3 min 100 ˚C ___________ (_)(_)(_)

- O2 plasma power: 200, gas: 80, 600 sec _____________________________________ (_)(_)(_)

- Lithography Spin HMDS, spin resist SU-8: spin 5 sec, 0-500 rpm, 30 sec, 2000 rpm, Edge-bead removal with razor blade, soft bake 90 ˚C 2 min: _____________________________________ (_)(_)(_)

"Mask 2"
Exposure mask "SU-8": WEC, Align & Expose, hard contact, 376W, time: 35 sec____ (_)(_)(_)

Post exposure bake 90C, 2 min ____ (_)(_)(_)

Develop SU-8 Developer 1 min (agitate) _________ ___________________ (_)(_)(_)

Dektek PR thickness (6-7µm thick): ______________________________

- O_2 plasma power: 200, gas: 80, 300 sec ______________________________ (_)(_)(_)

- Oxford clean Use 4-in Si wafer for chamber cleaning (20 – 50° C) **(critical)** ______________

- ICP RIE dry etch __________Process "SU-8 remove 20C", wafer die on L-Grease, see laser monitor

(~ 9 min) ____

6. **CPW Center Pad Metal Deposit**

- O_2 plasma power: 200, gas: 80, 300 sec ______________________________ (_)(_)(_)

- Lithography Spin/Steam HMDS, spin resist AZ5214: 40sec, 3000rpm ____________ (_)(_)(_)

Soft bake 90 ˚C 60 sec min___________/__________/_______________

"Mask 2"

Exposure mask "CPW Center": Align & Expose, hard contact, 376W, time: 55 sec__ (_)(_)(_)

Develop AZ300MIF 30 sec (agitate) _________________________ (_)(_)(_)

Dektek PR thickness (1.6µm thick): ______________________________

- O2 plasma power: 200, gas: 80, 300 sec______________________________ (_)(_)(_)

- Metal deposit Ti: 300-Å (1.0 A/s)

____ (_)

Au: 4000-Å (1.0 Å/s); ____(_)

- Lift-Off Acetone soak + Ultrasonic (large Ultrasonic 45 units) 10 min _________ (_)(_)(_)

7. **Cleaving**

- Mount Mount wafer on cleaving tool_____________________________ (_)(_)(_)

Cleave wafer _______________________________________ (_)(_)(_)

References

[1-1] A. D. Ellis, J. Zhao, and D. Cotter, “Approaching the non-linear Shannon limit,” Journal of Lightwave Technology, vol. 28, no. 4, pp. 423–433, Feb. 15, 2010.

[1-2] A. Andrae, and T. Edler, "On global electricity usage of communication technology: trends to 2030," Challenges, Vol. 6, No. 1, pp. 117-157, (2015).

[1-3] D. A. B. Miller, "Device requirements for optical interconnects to silicon chips," Proceedings of the IEEE, vol. 97, issue 7, pp. 1166-1185, June 10, 2009.

[1-4] D.A.B. Miller, "Attojoule optoelectronics for low-energy information processing and communications," Journal of Lightwave Technology, vol. 35, no. 3, pp. 346-396, February 1, 2017.

[2-1] S. Sze, Physics of Semiconductor Devices, A Wiley-Interscience Publication, 1981.

[2-2] A. Rogalski, M. Kopytko, and P. Martyniuk, "Performance prediction of pin HgCdTe long-wavelength infrared HOT photodiodes," *Applied Optics*, Vol. 57, No. 18, pp. D11-D19, June 2018.

[2-3] G. Keiser, Fundamentals of Optical Detectors, In: Biophotonics, Springer, 2016.

[2-4] K. Kato, S. Hata, K. Kawano and A. Kozen, "Design of Ultrawide-band, High-Sensitivity p-i-n Photodetectors," IEICE Transactions on Electronics, vol. E76-C, no. 2, pp. 214-221, 1993.

[2-5] D. Neaman, Physics of Semiconductor Devices, McGraw-Hill, 2012.

[2-6] K. Kato, “Ultrawide-Band/High-Frequency Photodetectors,“ IEEE Trans. on Microwave Theory and Techniques, vol. 47, no. 7, pp. 1265-1281, 1999.

[2-7] Y.-G. Wey, "100-GHz GaInAs/InP Double Heterostructure p-i-n Photodetectors," Journal of Lightwave Technol., vol. 13, no. 7, pp. 1490-1499, 1995.

[2-8] Q. Li., Over 100 GHz High Power Modified Uni-Travelling-Carrier Photodiodes for Analog Optic Link, (Doctoral dissertation). Retrieved from https://libraetd.lib.virginia.edu/downloads/w66343956?filename=Li_Qinglong_2018_PHD.pdf

[3-1] A. D. Ellis, J. Zhao, and D. Cotter, "Approaching the non-linear Shannon limit," Journal of Lightwave Technology, vol. 28, no. 4, pp. 423–433, Feb. 15, 2010.

[3-2] P. J. Roberts et al., "Ultimate low loss of hollow-core photonic crystal fibres," Optics Express, vol. 13, no. 1, pp. 236–244, Jan. 2005.

[3-3] D. J. Richardson, "New optical fibres for high-capacity optical communications," Philosophical Trans. R. Soc. A, vol. 374, no. 20140441, Nov. 7, 2015.

[3-4] N. Ye et al., "InP-based active and passive components for communication systems at 2 μm," Journal of Lightwave Technology, vol. 33, no. 5, pp. 971–975, Mar. 2015.

[3-5] A. Joshi and D. Becker, "High-speed low-noise p-i-n InGaAs photoreceiver at 2-μm wavelength," IEEE Photonics Technology Letters, vol. 20, no. 8, pp. 551–553, Apr. 2008.

[3-6] E. Ryckeboer et al., "Silicon-on-insulator spectrometers with integrated GaInAsSb photodiodes for wide-band spectroscopy from 1510 to 2300 nm," Opt. Express, vol. 21, no. 5, pp. 6101–6108, Mar. 2013.

[3-7] R. Wang et al., "2 μm wavelength range InP-based type-II quantum well photodiodes heterogeneously integrated on silicon photonic integrated circuits," Opt. Express, vol. 23, no. 20, pp. 26834–26841, Oct. 2015.

[3-8] B. Corbett et al., "High speed AIInGaAs/InGaAs quantum well waveguide photodiode for wavelengths around 2 microns," in Proc. Int. Conf. Indium Phosphide Related Mater., Aug. 2012, pp. 221–224.

[3-9] S. W. Henderson et al., "Coherent laser radar at 2 μm using solid-state lasers," IEEE Trans. Geosci.

Remote Sens., vol. 31, no. 1, pp. 4–15, Jan. 1993.

[3-10] T. F. Refaat et al., "Backscatter 2-μm lidar validation for atmospheric CO2 differential absorption lidar applications," IEEE Trans. Geosci. Remote Sens., vol. 49, no. 1, pp. 572–580, Jan. 2011.

[3-11] E. D. Palik, Handbook of Optical Constant Solids, Academic Press, New York, NY, 1985.

[3-12] F. Gunning, and B. Corbett, "Time to Open the 2-μm Window?," Optics & Photonics News, pp. 42-47, Mar. 2019.

[3-13] H. Fukano, M. Mitsuhara, and Y. Kondo, "Photodiode operating at 2 μm wavelength using InGaAsN layer on InP substrate," LEOS 2008, Acapulco, Mexico, Nov. 2008.

[3-14] S. Xu et. al., "High-speed photo detection at two-micron wavelength: technology enablement by GeSn/Ge multiple-quantum-well photodiodeon 300 mm Si substrate," Optics Express, Vol. 27, No. 4, February 18, 2019.

[3-15] Yang, Hua, et al. "High speed AlInGaAs/InGaAs quantum well waveguide photodiode for wavelengths around 2 microns," 2012 International Conference on Indium Phosphide and Related Materials, IEEE, 2012.

[3-16] H. Takasaki, Y. Kawamura, T. Katayama, A. Yamamoto, and N. Inoue, "Electroluminescence of In0.53Ga0.47As/GaAs0.5Sb0.5 type II multiple quantum well diodes lattice-matched to InP," Journal of Crystal Growth, vol. 227, pp. 294–297, Jul 2001.

[3-17] A. Yamamoto, Y. Kawamura, H. Naito, and N. Inoue, "Optical properties of GaAs0.5Sb0.5 and In0.53Ga0.47As/GaAs0.5Sb0.5 type II single hetero-structures lattice-matched to InP substrates grown by molecular beam epitaxy," Journal of Crystal Growth, vol. 201, pp. 872–876, May 1999.

[3-18] Y. Sugiyama, T. Fujii, Y. Nakata, S. Muto, and E. Miyauchi, "Conduction band Edge Discontinuity of

InGaAs/GaAsSb Heterostructures Lattice-Matched to InP Grown By Molecular-Beam Epitaxy," Journal of Crystal Growth, vol. 95, pp. 363-366, Feb 1989.

[3-19] H. Takasaki, Y. Kawamura, T. Katayama, A. Yamamoto, H. Naito, and N. Inoue, "Photoluminescence properties of In0.53Ga0.47As/GaAs0.5Sb0.5 type II quantum well structures lattice-matched to InP," Applied Surface Science, vol. 159, pp. 528-531, Jun 2000.

[3-20] B. Chen, InP Based Type-II Quantum Wells PIN Photodiodes, (Doctoral dissertation). Retrieved from https://libra2.lib.virginia.edu/downloads/6682x433r?filename=Baile_Chen%27s_final_dissertation.pdf

[3-21] R. Sidhu, Indium Phosphide Based Photodiodes for Mid-wave Infrared Detection, (Doctoral dissertation). Retrieved from https://repositories.lib.utexas.edu/bitstream/handle/2152/2313/sidhur97446.pdf

[3-22] B. Chen, W. Sun, J. C. Campbell, and A. L. Holmes, "Quantum efficiency modeling of PIN photodiodes with InGaAs/GaAsSb quantum wells absorption region," in Proc. Photon. Conf., 2011, pp. 35–36.

[3-23] G. Lucovsky, R. F. Schwarz, and R. B. Emmons, "Transit-time considerations in p-i-n diodes," J. Appl. Phys., vol. 35, no. 3, pp. 622–628, Aug. 1963.

[3-24] M. A. Fox, D. A. Miller, G. Livescu, J. E. Cunningham, and W. Y. Jan, "Quantum well carrier sweep out: Relation to electroabsorption and exciton saturation," IEEE J. Quantum Electron., vol. 27, no. 10, pp. 2281–2295, Oct. 1991.

[3-25] G. Zhou and P. Runge, "Modeling of multiple-quantum-well p-i-n photodiodes," IEEE J. Quantum Electron., vol. 50, no. 4, pp. 220–227, Apr. 2014.

[3-26] D. J. Moss, T. Ido, and H. Sano, "Calculation of photogenerated carrier escape rates from

GaAs/AlxGa1−x As quantum wells," IEEE J. Quantum Electron., vol. 30, no. 4, pp. 1015–1026, Apr. 1994.

[3-27] F. J. Effenberger and A. M. Joshi, "Ultrafast, dual-depletion region, InGaAs/InP p-i-n detector," Journal of Lightwave Technology, vol. 14, no. 8, pp. 1859–1864, Aug. 1996.

[3-28] C. L. Daunt et al., "Sub 10 ps carrier response times in electroabsorption modulators using quantum well offsetting," IEEE J. Quantum Electron., vol. 48, no. 11, pp. 1467–1475, Nov. 2012.

[3-29] W. Chen, B. Chen, J. Yuan, A. L. Holmes, and P. Fay, "Bulk and interfacial deep levels observed in In0.53Ga0.47As/GaAs0.5Sb0.5 multiple quantum well photodiode," Appl. Phys. Lett., vol. 101, no. 5, p. 052107, 2012.

[3-30] B. Chen, J. Yuan, and A. L. Holmes, Jr., "Dark current modeling of InP based SWIR and MWIR InGaAs/GaAsSb type-II MQW photodiodes," Opt. Quantum Electron., vol. 45, no. 3, pp. 271–277, 2012.

[3-31] B. Chen and A. L. Holmes, Jr., "Carrier dynamics in InP-based PIN photodiodes with InGaAs/GaAsSb type-II quantum wells," J. Phys. D, Appl. Phys., vol. 46, no. 31, p. 315103, 2013.

[3-32] A. Umbach, D. Trommer, R. Steingruber, A. Seeger, W. Ebert, and G. Unterborsch, "Ultrafast, high-power 1.55 μm side-illuminated photodetector with integrated spot size converter," in Proc. Opt. Fiber Commun. Conf., vol. 4, Mar. 2000, pp. 117–119.

[3-33] S. Goswami, L. Davis, and P. K. Bhattacharya, "Temporal response of photodiodes with GaAs/AlxGa1xAs (0.1 × 0.3) multiquantum well absorption regions," J. Appl. Phys., vol. 72, no. 10, pp. 4888–4892, Jul. 1992.

[3-34] A. P. Boltaev, N. N. Loiko, M. M. Rzaev, and N. N. Sibeldin, "External electric field effect on energy level positions in a quantum well," Russian Acad. Sci., Lebedev Phys. Inst.,Moscow, Russia, Tech. Rep.

QW/SL.06P, Jun. 2000.

[3-35] H. Inada, K. Miura, Y. Nagai, M. Tsubokura, A. Moto, Y. Iguchi, and Y. Kawamura, "Low dark current SWIR photodiode with InGaAs/GaAsSb type II quantum wells grown on InP substrate," 2009 IEEE International Conference on Indium Phosphide & Related Materials, pp. 149-152, IEEE, 2009.

[4-1] D. A. B. Miller, "Attojoule optoelectronics for low-energy information processing and communications," Journal of Lightwave Technology, vol. 35, no. 3, pp. 346-396, February 1, 2017.

[4-2] K. Nozaki, et al. "Photonic-crystal nano-photodetector with ultrasmall capacitance for on-chip light-to-voltage conversion without an amplifier," Optica, vol. 3, no. 5, 2016.

[4-3] H. Yue, B. S. Marks, C. R. Menyuk, V. J. Urick, and K. J. Williams, "Modeling sources of nonlinearity in a simple pin photodetector," Journal of Lightwave Technology, vol. 32, no. 20, pp. 3710-3720, Oct. 2014.

[4-4] Ishibashi, T., N. Shimizu, S. Kodama, H. Ito, T. Nagatsuma, and T. Furuta. "Uni-traveling-carrier photodiodes," Ultrafast Electronics and Optoelectronics, p. UC3, Optical Society of America, 1997.

[4-5] N. Li, et al., “High-saturation-current charge-compensated InGaAs/InP uni-travelling-carrier photodiode,” The 16th Annual Meeting of the IEEE, Lasers and Electro-Optics Society, pp.790-791, Oct. 2003.

[4-6] Q. Li, K. Sun, K. Li, Q. Yu, P. Runge, W. Ebert, A. Beling, J. C. Campbell, “High-Power Evanescently-coupled Waveguide MUTC Photodiode with >105 GHz bandwidth,” IEEE/OSA J. Lightwave Technol., Vol. 35, No. 21, pp. 4752-4757, November 2017.

[4-7] Q. Li, Over 100 GHz High Power Modified Uni-Travelling-Carrier Photodiodes for Analog Optic Link, (Doctoral dissertation). Retrieved from

https://libraetd.lib.virginia.edu/downloads/w66343956?filename=Li_Qinglong_2018_PHD.pdf

[4-8] Z. Li, H. Pan, H. Chen, A. Beling, and J.C. Campbell, “High-Saturation–current modified uni-traveling-carrier photodiode with cliff layer,” *IEEE J. of Quantum Electronics*, vol.46, no. 5, pp. 626-632, May 2010.

[4-9] B.R. Bennett, R.A. Soref, and J.A. Del Alamo, “Carrier-induced change in refractive index of InP, GaAs and InGaAsP,” IEEE Journal of Quantum Electronics, vol. 26, no. 1, pp. 113-122, January 1990.

[4-10] Y. Baumgartner, C. Caër, M. Seifried, G. Villares, D. Caimi, T. Morf, J. Faist, B. J. Offrein, and L. Czornomaz, "CMOS-Compatible Hybrid III-V/Si Photodiodes Using a Lateral Current Collection Scheme," *2018 European Conference on Optical Communication (ECOC)*, pp. 1-3, 2018.

[4-11] R. Going, T. J. Seok, J. Loo, K. Hsu, and M. C. Wu, “Germanium wrap-around photodetectors on silicon photonics,” *Optics Express*, Vol. 23, pp. 11975–11984, (2015).

[4-12] L. Virot, P. Crozat, J. M. Fedeli, J. M. Hartmann, D. Marris-Morini, E. Cassan, F. Boeuf, and L. Vivien, “Germanium avalanche receiver for low power interconnects,” *Nature Communication*, Vol. 5, p. 4957, (2014).

[4-13] H. Ito, T. Furuta, S. Kodama, and T. Ishibashi, “Zero-bias high-speed and high-output-voltage operation of cascade-twin uni-travelling-carrier photodiode,” Electron. Lett., vol. 36, pp. 2034–2036, Nov. 2000.

[5-1] D. A. B. Miller, "Device requirements for optical interconnects to silicon chips." Proceedings of the IEEE, Vol. 97, Issue 7, pp. 1166-1185, June 10, 2009.

[5-2] D. Dai et al., “Equivalent circuit model of a waveguide-type Ge/Si avalanche photodetector,” Phys. St. Solidi C 7, No. 10, pp. 2532–2535, (2010).

[5-3] D. Liang, J. E. Bowers, “Recent progress in lasers on silicon,” Nature Photonics, Vol. 4, No. 8, p. 511, Aug. 4, 2010.

[5-4] G. Kurczveil et al., “Robust hybrid quantum dot laser for integrated silicon photonics,” Opt. Exp., Vol. 24, No. 14, pp. 16167-16174 (2016).

[5-5] M. Sugawara and M. Usami, “Quantum dot devices handling the heat,” Nat. Photonics 3(1), 30–31 (2009).

[5-6] G. Park, O. B. Shchekin, D. L. Huffaker, and D. G. Deppe, “Low-threshold oxide-confined 1.3-μm quantum-dot laser,” IEEE Photonics Technol. Lett. 12(3), 230–232 (2000).

[5-7] G. Ortner, C. N. Allen, C. Dion, P. Barrios, D. Poitras, D. Dalacu, G. Pakulski, J. Lapointe, P. J. Poole, W. Render, S. Raymond, “External cavity InAs/InP quantum dot laser with a tuning range of 166 nm,” Appl. Phys. Lett., 88(12), 121119 (2006).

[5-8] G. Kurczveil et al., “On-Chip Hybrid silicon Quantum dot Comb Laser with 14 error-Free Channels,” ISLC (Santa Fe, NM, 2018).

[5-9] D. Liang et al., “Highly efficient vertical outgassing channels for low-temperature InP-to-silicon direct wafer bonding on the silicon-on insulator substrate,” J. Vac. Sci. Technol. B, Vol. 26, No. 4, p. 1560 (2008).

[5-10] L. Colace et al., “Low Dark-Current Germanium-on-Silicon Near-Infrared Detectors,” IEEE Photonics Technology Letters, Vol. 19, No. 22, pp. 1813-1815, November 15, 2007.

[5-11] P. Jin, C. M. Li, Z. Y. Zhang, F. Q. Liu, Y. H. Chen, X. L. Ye, B. Xu, and Z. G. Wang, "Quantum-confined Stark effect and built-in dipole moment in self-assembled InAs/GaAs quantum dots," Applied Physics Letters, Vol. 85, No. 14, pp. 2791-2793, October 14, 2004.

[5-12] L. L. Pinel, S. J. Dimler, X. Zhou, S. Abdullah, S. Zhang, C. H. Tan, and J. S. Ng, J, “Effects of carrier injection profile on low noise thin Al0.85Ga0.15As0.56Sb0.44 avalanche photodiodes,” Optics Express, Vol. 26, No. 3, pp. 3568-3576, Feb. 5, 2018.

[5-13] I. Sandall, J. S. Ng, J. P. David, C. H. Tan, T. Wang, and H. Liu, “1300 nm wavelength InAs quantum dot photodetector grown on silicon,” Optics Express, Vol. 20, No. 10, pp. 10446-10452, May 7, 2012.

[5-14] Y. Ma et al., "Enhanced Carrier Multiplication in InAs Quantum Dots for Bulk Avalanche Photodetector Applications,” Adv. O. Mat., vol. 5, no. 5, March 29, 2017.

[5-15] J. E. Bowers, D. Dai, Y. Kang, M. Morse, “High-gain high-sensitivity resonant Ge/Si APD photodetectors,” Infrared Technology and Applications XXXVI 2010, Vol. 7660, p. 76603H, (International Society for Optics and Photonics), May 4, 2010.

[5-16] K. Yu, C.-H. Chen, A. Titriku, A. Shafik, M. Fiorentino, P. Y. Chiang, and S. Palermo, “25 Gb/s hybrid-integrated silicon photonic receiver with microring wavelength stabilization,” Optical Fiber Communication Conference (Optical Society of America), paper W3A–6, March, 22-26, 2015.

[5-17] R. J. McIntyre, “Multiplication noise in uniform avalanche diodes,” IEEE Trans. Electron Devices, Vol. ED-13, pp. 164-168, Jan. 1966.

[5-18] Th. Kirn, D. Schmitz, J. Schwenke, Th Flügel, D. Renker, and H. P. Wirtz, "Wavelength dependence of avalanche photodiode (APD) parameters,” Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment 387, No. 1-2, pp. 202-204, 1997.

[6-1] D. A. B. Miller, "Attojoule optoelectronics for low-energy information processing and communications," Journal of Lightwave Technology, vol. 35, no. 3, pp. 346-396, February 1, 2017.

[6-2] D. Liang, G. Roelkens, R. Baets and J.E. Bowers, '"Hybrid Integrated Platforms for Silicon Photonics," Materials, vol. 3, no. 3, pp. 1782-1802.

[6-3] H. Chang, Y. Kuo, H. Chen, R. Jones, A. Barkai, M.J. Paniccia and J.E. Bowers, '"Integrated Triplexer on Hybrid Silicon Platform," Optical Fiber Communication Conference.

[6-4] K. Sun, D. Jung, C. Sheng, A. Liu, J. E. Bowers, A. Beling, "Low-Dark Current III-V Photodiodes Grown on Silicon Substrate," IEEE Photonics Conference (IPC), October 1-5, 2017.

[6-5] Y. Wang, "Heterogeneously Integrated Photodiodes on Silicon," (Doctoral Dissertation). Retrieved from https://libra2.lib.virginia.edu/downloads/9880vr180?filename=1_Wang_Ye_2017_PHD.pdf

[6-6] Y. Chen, X. Zhao, J. Huang, Z. Deng, C. Cao, Q. Gong, and B. Chen, "Dynamic model and bandwidth characterization of InGaAs/GaAsSb type-II quantum wells PIN photodiodes," Optics Express, Vol. 26, No. 26, pp. 35034-35045, December 24, 2018.

[6-7] R. Costanzo, R., Z. Yang, N. Raduazo, A. Beling, S. M. and Bowers, "A 10 GHz bandwidth balanced photoreceiver with 41 V/W optical conversion gain," 2017 12th European Microwave Integrated Circuits Conference (EuMIC), IEEE, pp. 151-154, October 8-10, 2017.

[6-8] Y. Fan, D. Liang, A. Roshan-Zamir, C. Zhang, B. Wang, M. Fiorentino, R. Beausoleil, and S. Palermo, "A Directly Modulated Quantum Dot Microring Laser Transmitter with Integrated CMOS Driver," *Optical Fiber Communication Conference*, pp. W3E-5. Optical Society of America, March 3-7, 2019.

List of Publications

[1] **B. Tossoun**, J. Morgan, A. Beling, "Ultra-Low Capacitance, High-Speed Integrated Waveguide MUTC Photodiodes on InP," *Integrated Photonics Research, Silicon, and Nano-Photonics 2019,* Burlingame, CA; 30 July-1 August 2019, (2019).

[2] **B. Tossoun**, G. Kurczveil, C. Zhang, A. Descos, X. Zeng, Z. Huang, D. Liang, R. G. Beausoleil, "1310 nm quantum dot waveguide avalanche photodiode heterogeneously integrated on silicon," *European Congress of Integrated Optics 2019*, Ghent, Belgium; 24-26 April 2019, (2019).

[3] **B. Tossoun**, J. Zang, S. J. Addamane, G. Balakrishnan, A. L. Holmes, A. Beling, "InP-based Waveguide-Integrated Photodetectors With InGaAs/GaAsSb Type-II Quantum Wells and 10-GHz Bandwidth at 2 µm", *Journal of Lightwave Technology,* Vol. 36, No. 20, pp. 4981-4987, October 15, 2018.

[4] **B. Tossoun**, S. Addamane, G. Balakrishnan, A. L. Holmes, A. Beling, "High Speed InP-based Type-II Multiple Quantum Well Integrated Waveguide Photodiode at 2.0-µm Wavelength," *Integrated Photonics Research, Silicon, and Nano-Photonics 2018*, Zurich, Switzerland; 2-5 July 2018, July 4, (2018).

[5] **B. Tossoun**, G. Kurczveil, C. Zhang, D. Liang, R. Beausoleil, "High-speed 1310 nm Hybrid Silicon Quantum Dot Photodiodes with Ultra-low Dark Current," *2018 76th Device Research Conference (DRC)*, Santa Barbara, CA, 24-27 June 2018.

[6] Morgan, J. S., Zang, J., Sun, K., **Tossoun, B.**, Campbell, J. C., & Beling, A."Zero-bias Photovaractor with 60 GHz Resonant Network for Optically Modulated Scatterer (OMS) Application,“ *CLEO: Science and Innovations*, Optical Society of America, San Jose, CA, May 12-15 2018.

[7] **B. Tossoun**, R. Stephens, Y. Wang, S. Addamane, G. Balakrishnan, A. Holmes, A. Beling, "High-Speed InP-based p-i-n Photodiodes with InGaAs/GaAsSb Type-II Quantum Wells," *IEEE Photonics Technology Letters*, Volume 30, Issue 4, pp. 399-402, February 15, 2018.

[8] **B. Tossoun**, Y. Wang, S. Addamane, G. Balakrishnan, A. Holmes, A. Beling “High-Speed Type-II InGaAs/GaAsSb Multiple Quantum-Well Integrated Waveguide Photodiodes at 2 μm Wavelength,” *IEEE Photonics Conference 2017*, Orlando, FL; 1-5 October 2017, October 4, (2017).

[9] **B. Tossoun**, Y. Wang, S. Addamane, G. Balakrishnan, A. L. Holmes, A. Beling, “InP-based Multiple Type-II Quantum-Well Integrated Waveguide p-i-n Photodiodes for Mid-Infrared Detection,” Tossoun, B. *et al.*, *IEEE Photonics Summer Topicals Meeting Series 2017*, San Juan, PR; 10-12 July 2017, July 12, (2017).

[10] **B. Tossoun**, D. J. Derickson, S. Srinivasan, J.E Bowers, J. E., “Hybrid silicon mode-locked laser with improved RF power by impedance matching”, *Silicon Photonics X,* 9367-24, San Francisco, CA; 9-11 February 2015, February 10, (2015).