Heterogeneously-Integrated Electronically-Assisted Photonics for RF and mm-Wave Links

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A

Dissertation

Presented to

the faculty of the School of Engineering and Applied Science

University of Virginia

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in partial fulfillment

of the requirements for the degree

Doctor of Philosophy

by

Robert W. Costanzo

May 2021

APPROVAL SHEET

This

Dissertation

is submitted in partial fulfillment of the requirements
for the degree of

Doctor of Philosophy

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Charlottesville, Virginia

Keywords: transimpedance amplifiers, broadband amplifiers, CMOS integrated circuits, photodetectors, photoreceivers, rf photonics, silicon photonics, optical phase-locked loop

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(ABSTRACT)

Electronically-assisted photonics have historically played an essential role in high-speed communications and will continue to do so in the predicted 5G paradigm. While millimeter-wave emitters with beam-forming, massive MIMO, and advanced modulation techniques will likely provide the fronthaul wireless links, photonics provides broadband solutions for long-distance backhaul communications. Optical fiber can be extended even closer to the user, providing additional increases in data rates. Additionally, optical and millimeter-wave frequency synthesis systems utilizing tightly integrated optical and electronic circuits can enable a wide range of applications with high complexity chip-scale solutions.

One of the most important blocks in determining the cost and performance of an optical link is the photoreceiver. Photoreceivers with high bandwidths and low noise can enable high speeds for data transmission and lower minimum detectable signals in the optical link. As silicon PDs are inefficient and III-V material-based electronics can become expensive, heterogeneous integration of III-V PDs and silicon CMOS electronics offers an effective solution. This research presents design, simulation, and measurements of several transimpedance amplifier topologies im-

plemented in several CMOS and BiCMOS platforms. Additionally, heterogeneously integrated photoreceivers based on these electronic circuits and III-V PDs are presented. The integration schemes demonstrate increasing levels of integration and SWaP reduction while simultaneously removing previously encountered bottlenecks in photoreceiver performance. Investigations are presented in both high-speed as well as low-noise application spaces.

Further, integrated silicon photonics (SiP) platforms offer high integration potential for optical and electronic circuits. Germanium-on-silicon (Ge-on-Si) PDs are readily integrated and offer high bandwidths and responsivities. Several PDs and PD arrays are fabricated on a developing SiP platform, along with several other circuits including a Mach-Zehnder delay line interferometer.

Lastly, a solution to radio-over-fiber (RoF) high frequency RF and mm-Wave carrier generation is proposed. For use in coherent receivers, an optical phase-locked loop can improve the phase noise and eliminate long-term temperature drift of the RF beat frequency. An electronics CMOS chip is designed and fabricated to implement the necessary control circuits. Additionally, a SiP chip with phase modulators and the necessary optical components is designed and fabricated. The two chips are heterogeneously integrated on-board to create an optical phase-locked loop. This integration will offer a chip-scale solution with high complexity in order to control and improve the operation of the widely-tunable optical sources used in millimeter-wave frequency synthesis.

This work was supported by the Defense Advanced Research Projects Agency (DARPA) within the Direct On-chip Digital Optical Synthesizer (DODOS) program under award HR0011-15-C-0055, as well as by the Air Force Research Laboratory under agreement FA8650-15-2-5220.

Acknowledgments

As the long road comes to an end and I can finally see the light at the end of the tunnel, I can't help but think back to all those friends and family who have helped me to get where I'm going. First, I want to thank my family. I know that I could not be where I am today had it not been for my father and mother, Robert and Anonglak Costanzo. Despite my jokes and wisecracks, I know you have sacrificed a lot for me and I am truly grateful. Your encouraging words and constant support have been instrumental in completing this degree. I also want to thank my little brother, Joshua, for supporting and challenging me (mostly the latter) along the way. You're a brilliant kid, and maybe one day you'll be acknowledging me in your own dissertation.

Next, I would like to express my gratitude to my advisor, Steven M. Bowers. When Steve began his tenure at UVA, I was entering my first semester of graduate school as his teaching assistant. I never intended to pursue a doctorate degree, but his guidance and energy helped push me into that direction, for which I am glad. I know that I am now a completely different person from when I first started graduate school, personally, intellectually, and professionally. I owe a lot of that to Steve. Thank you for letting me be your first student, and for allowing me to research under you.

I would also like to thank some of the other professors at UVA that have offered me advice and input throughout my time here. For all of his input directly into my research and into my dissertation, I want to thank Andreas Beling, whom I consider a second advisor. As I continued further into an interdisciplinary field, it was invaluable to have his help in addition to Steve's. I also want to thank Mircea Stan, who advised me while I was an undergraduate researcher and convinced me to pursue graduate school in the first place. For all of their help and advice, I would also like to thank the members of my committee: Travis Blalock, Bobby Weikle, Xu Yi, and Olivier Pfister. In addition, I want to thank Terry Tigner for making navigating all the bureaucracy more manageable and personal, and for brightening my days with her stories and charm.

I am also indebted to my fellow graduate students. For the invaluable technical discussions and assistance, I want to thank the members of my IECS family, including Jesse Moody, Pouyan Bassirian, Jay Sheth, Divya Duvvuri, Xiaochuan Shen, Linsheng Zhang, Vinay Iyer, Anjana Dissanayake, and Prerana Singaraju. I want to extend a special thanks to those of you who have become part of my life outside of the lab as well. For their part in my research, I would also like to thank the members of the Optoelectronic Device Group, especially Keye Sun, Zhanyu Yang, Ta-Ching Tzu, and Junyi Gao. Lastly, I have to thank my good friends Brian, Chris, Hector, Kris, and the Seans for letting me vent and bend your ears when things got rough.

To everyone I have mentioned in this acknowledgment, as well as to those who I couldn't quite fit, thank you for everything. I could not have done it without you on my side.

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Chapter 1

Research Overview

1.1 RF Photonics

RF or microwave photonics is an increasingly important technology that continues to enable and improve a wide variety of applications that significantly impact modern daily life. Much of the communication realm is dominated today by fiber optic communications. The benefits and cost-effectiveness of optical fiber has fortified its place in long-distance backhaul communication infrastructure, ever since its deployment in fiber-to-home networks. However, the fronthaul communications primarily occurs in the wireless realm, often in the microwave or millimeter-wave (mmWave) frequency ranges in recent years [1]. First coined in the year 1991, the term "microwave photonics" lies at this interface between photonic and electronic technologies [2]. In recent work, these two fields have merged together into the interdisciplinary topic of microwave photonics, with

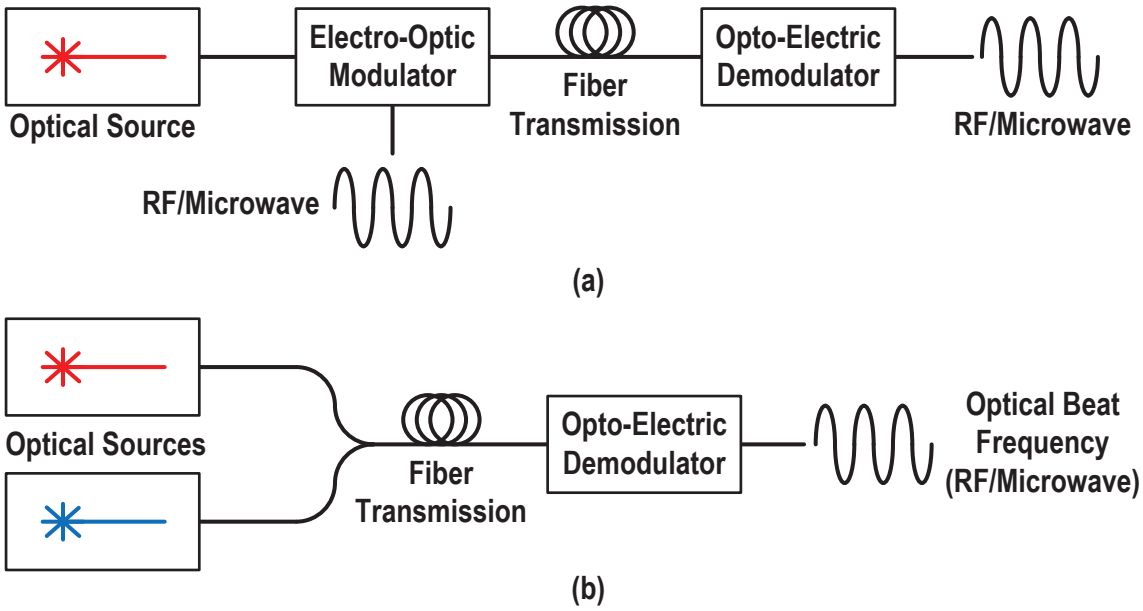


Figure 1.1: Representation of two possible microwave optical links, (a) using an electro-optic modulator to modulate the RF onto the optical carrier and (b) using a heterodyne optical setup to generate an RF beat frequency at the output of the opto-electric converter at the receiver side.

microwave-related issues becoming relevant in optical design and vice versa.

One of the first widespread commercial uses of RF photonics was the distribution of cable television networks through optical fiber [3]. Additionally, photonic links are utilized in server farms for machine-to-machine optical interconnects, allowing high-speed data transmission in a "photonic cloud" [4]. In modern high-speed communication, the communication backhaul is almost exclusively done in optical fiber networks due to several advantages including innately high bandwidths, low losses over long distances, and low susceptibility to electromagnetic interference. While there are many visions as to what the future networks entail, it is evident that microwave photonics will make up a significant portion of it.

Two basic RF photonic links are demonstrated in Figure 1.1. Figure 1.1(a) shows a link based on a single optical source. The frequency (often described in the optical domain by its wavelength) acts as the carrier. At telecommunication standards, this optical source is typically around 1550 nm. Then, the source is modulated via an electro-optic effect, which modulates the desired RF/microwave signal frequency or data onto the optical carrier. This can be done via an external electro-optic modulator immediately following the laser, or by applying the RF signal to an internal tuning mechanism on the laser, such as a drive current or cavity length. Another link shown in Figure 1.1(b) makes use of two lasers at different frequencies and combines their outputs before fiber transmission. The laser outputs can also be routed separately and then combined at the receiver side for the same affect. The two laser frequencies are beat together in the opto-electric conversion by a photodiode, resulting in an output RF frequency. This output frequency is the difference between the frequencies of the two optical sources. This can be highly advantageous as optical sources can have wide tunability and can result in highly tunable RF output frequencies without the need of highly expensive and large electronic equipment. Additionally, the complexity of these links can be significantly increased with multiplexing techniques.

Radio-Over-Fiber Network

Radio-over-fiber (RoF) is a hot topic and one of the most researched applications of microwave photonics for the next generation network. This technology involves the propagation of radio, microwave, or mm-Wave wireless signals through an optical fiber. This is useful for many reasons, and will help provide solutions for achieving untethered wireless access to broadband connectivity [5]. As users demanding access to broadband connections become more and more nomadic,

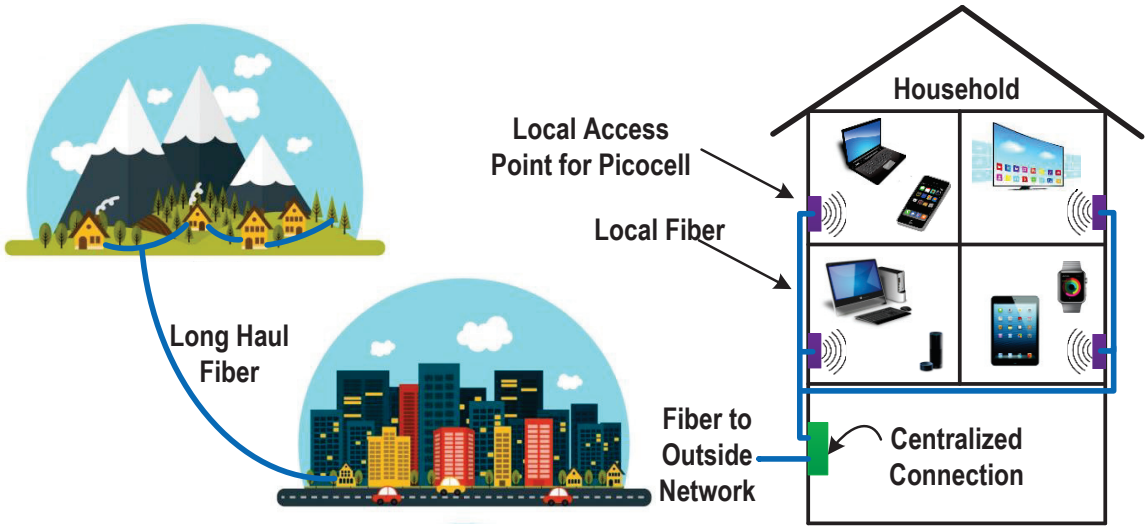


Figure 1.2: Representation of an RoF network extended further towards end user.

making substantial use of handheld personal devices, RoF can assist current and next-generation network designers in achieving improved coverage, capacity, and delivery infrastructure.

A paradigm often proposed for future 5G network communications typically includes radio-over-fiber (RoF) transmissions and antenna remoting for wireless data transmission of optically delivered data [6]. As demand for data-intensive content continues to grow, carrier frequencies will increase to higher RF and mm-Wave frequencies in order to accommodate the necessary increase in bandwidth. However, as atmospheric attenuation typically increases with frequency, wireless access points will suffer from reduced range. One solution to this problem is to extend the optical network closer to the end user with more numerous indoor access points. Optical links can not only provide the backhaul, but can be extended further into the fronthaul. By leveraging the wide tunability of optical sources at a central location and the low loss of optical fiber transmission, the

required microwave or mm-Wave frequency carriers can be generated and sent to the access points via fiber. This removes the need for costly electronics that traditionally generate high frequency carriers. Overall system cost and complexity can be significantly reduced by utilizing a centralized approach, and routing required radio signals wherever needed via optical fiber. This can be in the form of a centralized hub on the premises that accesses the incoming optical fiber from the outside network, processes the data, and transmits it to the local access points within the building. This paradigm is shown in Figure 1.2.

Some significant advantages of RoF networks include highly agile and adaptive control. Because of the highly diversified and numerous access points controlled by the same central processing hub, the network can monitor changing traffic loading conditions across a wider physical area and apply dynamic-channel-allocation [7]. This means individual communication channels can be allocated to traffic-heavy areas to help alleviate the issues of channel reuse. From a commercial standpoint, establishing a far-reaching RoF network can save network providers money in the long run, as this type of network can be considered relatively future proof. This is due to the fact that this kind of network architecture can accommodate many different evolving forms of radio standards and methodologies [8]. Additionally, a lot of the optical infrastructure can be reused despite possible necessary changes in the network architecture.

While the RoF network leverages the advantages of optical communications, none of the communication is possible without the electronics as well. The electronics continue to be crucial in determining the performance of the optical link. On the transmit side, high-speed data drivers are required for the optical modulators. This encodes the electronic data packets onto the optical car-

rier. In order to receive and sense the incoming data, photodiodes convert the optical signal into an electronic one and pass it on to a combination of transimpedance amplifiers, limiting amplifiers, and decision circuitry. The speed of these circuits, collectively called a photoreceiver, directly determine the downlink speeds achievable. As such, an RoF link cannot be designed purely in the optical domain, nor in the electronic domain. A hybrid approach is required to tackle the microwave photonic considerations of the entire system.

One commercial example of a full RoF network technology is developed and sold by the Andrew Corporation [5]. The system is a hybrid fiber radio, and makes use of a distributed antenna system in order to provide the aforementioned benefits of a RoF network. The network is capable of transmitting and receiving radio signals between 800 MHz and 2.5 GHz, allowing it to handle the traffic of both cellular and WiFi applications. As of 2007, the system had been installed at several notable locations, including in Sydney, Australia for the Olympic Games in 2000 and in Germany for the 2006 World Cup [5]. The RoF network can provide solutions for high-density high-traffic use cases.

Antenna Remoting

As mentioned above, the RoF network paradigm almost always entails more numerous antennas and access points distributed throughout the coverage area. With the majority of the signal processing and architecture implementation occurring at the central hub, sometimes referred to as the central “office”, the access points are kept as simple and power efficient as possible. This is because the radio signals can be transmitted between the access point and the central hub via optical fiber. This is especially true at higher frequencies, such as in the mm-Wave frequency range

where atmospheric attenuation is critical and limits the range of the wireless transmission. Therefore, it is necessary to have more widespread access points, and increased power consumption and complexity would only drive up the cost to prohibitive levels.

At the simplest form, a remote access point can be achieved by attaching a photodiode with sufficient bandwidth and an antenna with the correct operating frequency. For example, in Figure 1.3(a), the photonically-driven emitter allows the simplest conversion and transmission of the RF signal in the optical carrier to a wireless signal. This type of emitter has been demonstrated in recent works, even up through 200 GHz [9, 10]. However, the drawback is that this will only function as a downlink. Data can be transmitted to the user, but there is no way to communicate back and forth between the user and central office. As such, additional complexity is required at the remote access point. Shown in Figure 1.3(b), an electro-optic converter must be added to the antenna to modulate received radio signals onto an optical signal for transmission back to the central office. However, this optical source must also be present at the remote access point (RAP). This can be achieved by implementing an optical source at the RAP, or by routing an optical signal from the central office to the RAP to be used specifically for return communications.

While important for communications, antenna remoting is also beneficial to radar and metrological applications. For example, in radar systems, it is useful to sense at higher frequencies, as the relative wavelength determines the resolution of the radar system. For better detection precision, higher mm-Wave frequencies can be used. However, similarly to the problems described in the networking application space, generation of higher frequencies can be difficult or expensive when utilizing purely electronic solutions. As such, photonic-based emitters offer a viable alternative,

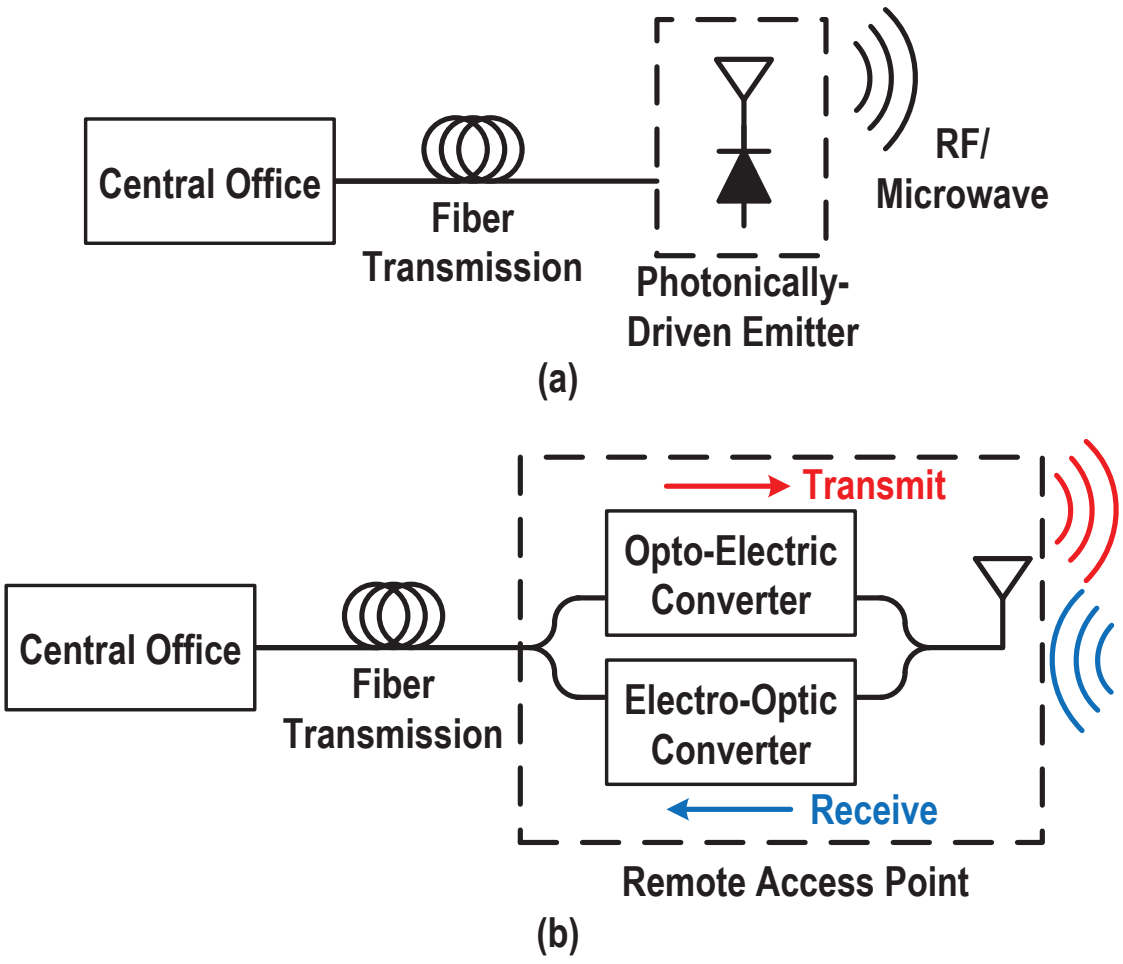


Figure 1.3: Representation of remote antenna, demonstrating a (a) photonically-driven emitter, consisting of only a PD and antenna, and (b) a full remote access point (RAP), consisting of both opto-electric and electro-optic conversion for sending and receiving data between the central office and RAP.

and has been demonstrated [11]. Additionally, the physical scattering of the various access points can be leveraged for benefit. When detecting a stimulus across multiple remote antennas sharing a central processing unit, it is possible to utilize arrival time or phase differences to triangulate the angle of incidence of a wireless signal, much like antenna beamforming [12].

To take one step further, optical beam forming is another field of research prominent in microwave photonics. In a fully electronic implementation of antenna beamforming, a true time-delay (ttd) or electronic phase shift is required. By making use of these delays, and differing the delays between each radiating element (antenna), the constructive interference can cause the radiated signal to propagate in a specific direction. This allows the network to radiate the majority of the energy towards the receiver, gaining benefits in efficiency and sensitivity. However, the beam steering network can combine optical with electronic techniques to create a very agile and adaptive approach. For example, one work presented a "fiber-optic prism true time-delay antenna feed" to create a beam steering architecture [13]. This made use of a tunable laser with an electro-optic modulator being driven by the RF signal. This RF-modulated optical output was split into N paths towards N radiating elements. Each of these N paths consisted of a fibers with different dispersive properties, resulting in different phase delays within each path. The dispersive properties of each fiber also varied with optical wavelength, so the wavelength of the laser could be tuned (without changing the RF signal modulated onto it). This resulted in tuning the delays between each path, tuning the angle of radiation, and thus achieving beam steering, and is shown in Figure 1.4.

Optical Frequency Synthesis

Another major use of RF photonics is the optical-frequency synthesizer (OFS). An OFS system generates a very stable optical frequency by utilizing a lower microwave-frequency reference. These are very valuable in several applications, especially in optical metrology, terahertz spectroscopy, imaging, light-detection and ranging (LiDAR) [14], and in the previously described optical communications. With the generation of very clean, very precise optical signals, the density

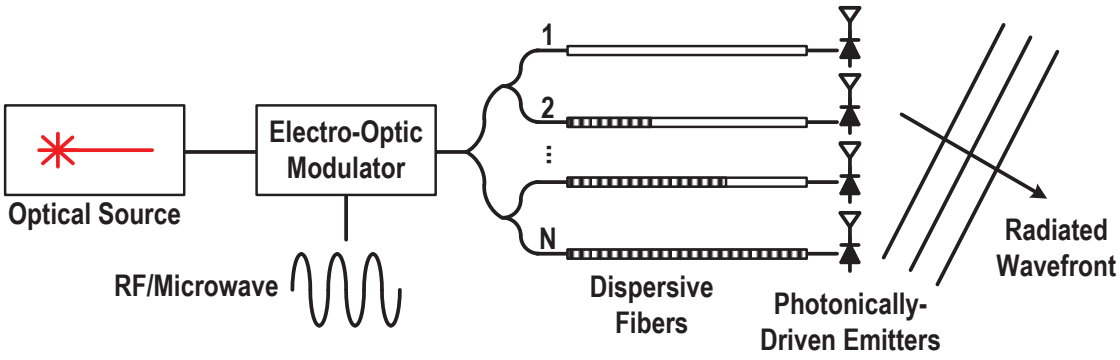


Figure 1.4: Fiber-optic prism true time-delay antenna feed from [13].

of channels on a given optical link can be increased further. However, OFS is often limited to laboratory environments due to the prohibitive physical sizes of current implementations. In order to be utilized in a more widespread manner, complex RF photonic solutions must be reduced in size to chip-scale implementations. This need has given rise to the emerging field of silicon photonics (SiP). In a SiP platform, photonic components and circuits can be designed and fabricated on a silicon chip, lending itself well to incorporation of traditional CMOS devices. As SiP platforms continue to mature and incorporate electronic devices, chip-scale RF photonics will see an an increase in complexity, yield, and cost-effectiveness.

Much of the abilities and technologies available in the electronics domain has been made possible through the advancement in RF and microwave frequency synthesis systems. As a parallel, there is much focus and desire to achieve effective chip-scale optical frequency synthesis to promote similar advancements in the photonic technologies and applications. Making use of both the electronic and photonic components, heterogeneous integration offers a cost-effective solution to this research focus. With advancements in heterogeneous integration, it is possible to create systems

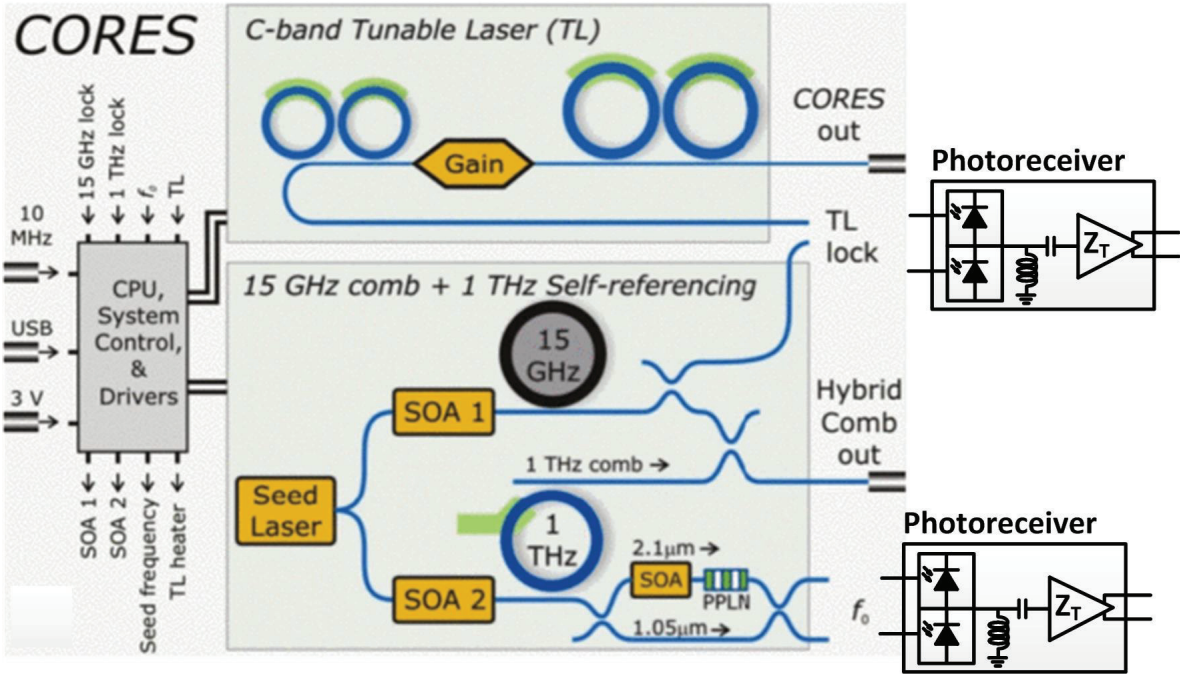
that combine semiconductor lasers, semiconductor optical amplifiers, electro-optic modulators, optical waveguides and couplers, photodiodes, and active electronics such as CMOS or BiCMOS transistors on a chip-scale platform [15]. This system-level multi-domain integration is the primary focus of the DARPA-sponsored DODOS project, described below.

The Direct On-Chip Digital Optical Synthesizer (DODOS) project aimed to promote a technical revolution for photonic systems similar to the one in the microwave domain that was brought about through improved methods of microwave frequency synthesis. According to the Defense Advanced Research Projects Agency, this revolution enabled a new era of technological advancement in many sectors, including modern warfare, civilian capabilities, navigation technologies, satellite and terrestrial communications, and other microwave technologies. The first bench-top demonstration of optical frequency synthesis occurred in the early 2000s [16], and since then many novel solutions have been developed for defense and civilian applications alike. However, the cost, size, and power-consumption has restricted the use of the OFS systems to lab and industrial settings. To increase the applicability, the project aimed to leverage the advancements of heterogeneous integration techniques to combine all the components required for an OFS system. The primary goal was to combine all the optical components including widely tunable lasers, optical combs, and nonlinear devices along with all the necessary control loops integrated on electronic CMOS chips into a small package on the order of 1 cm^3 while consuming under 1 W of dc power to generate a clean, highly tunable 1550 nm light source.

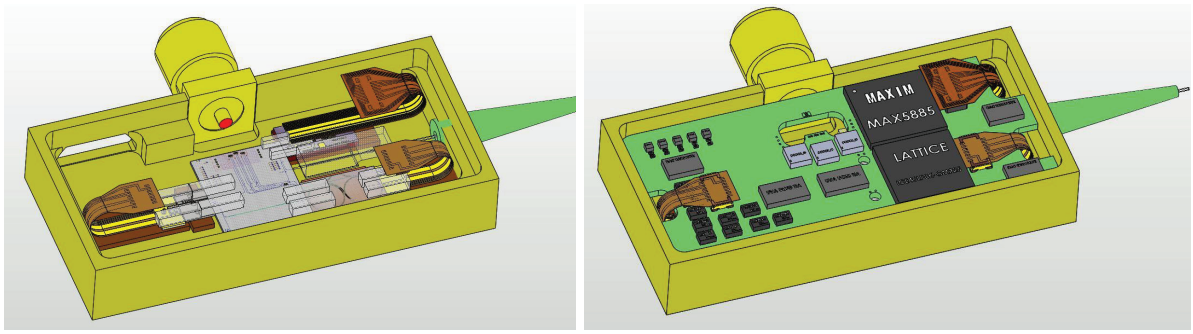
As much of the work in this dissertation was pursued in direct relation to the DODOS project as part of a multi-organization team, the overall system is discussed here briefly to describe the

motivation behind the work. Prior, on-chip widely tunable lasers with tuning ranges of at least 40 nm have suffered from poor linewidths. These linewidths tend to be on the order of hundreds of kHz. This limitation can be attributed to the excessive internal losses of the laser cavities [17]. To address this, an effort to integrate high performance III-V materials and silicon was made, with the III-V absorption losses significantly lower, resulting in laser cavities with higher quality-factors and ultimately cleaner outputs. It is anticipated that the resulting linewidths would be an order of magnitude improved, with linewidths on the order of tens of kHz [18]. Additionally, by making use of improved high-performance optical resonators, the chip-scale optical resonator enabled synthesizer (CORES) was proposed [19] to answer the requirements set forth by the DODOS project.

The overall architecture of the CORES system is shown in Figure 1.5. The system utilizes a single continuous wave laser as a seed laser, used to pump two optical microring resonators. One ring was designed with a free spectral range (FSR), which can also be described as the difference in frequency between two adjacent comb lines, of 15 GHz. One of the optical comb lines from this ring is phase-locked to the laser, and the beat frequency is compared against a 10 MHz RF reference signal. However, in order to phase-lock the optical comb and the laser, several high-bandwidth low-noise photoreceivers are required at various points in the system. In each path, the photoreceiver should be able to detect and amplify up through the FSR of the ring. This necessitates photoreceivers that photodetect up to 15 GHz signals, amplify them into an electrical voltage signal, and pass it on to the following processing electronics. As monolithic platforms are still in their developmental stages, a heterogeneous approach can achieve the required performance metrics by leveraging the advantages of each of the specialized materials for individual functions (laser



(a)



(b)

Figure 1.5: (a) System level architecture for the CORES system from [13]. (b) CAD drawing of the heterogeneously-integrated and assembled package for the OFS system, with cm^3-scale volume.

sources, optical amplification, photodetection, electronic processing, etc.) against the drawbacks of the additional parasitics introduced between components.

In the chip-scale optical resonator enabled synthesizer, all previously-discrete optical components for an OFS system are combined onto a single interposer, resulting in a small, manufacturable,

and reliable chip-scale solution [14]. The Si_3N_4 interposer combines several optical frequency combs for referencing, second-harmonic generation, waveguide photodetectors, and is integrated with CMOS or BiCMOS electronics. With this heterogeneous integration, the package achieves over 1000 times reduction in size and power consumption, and over 100 times reduction in cost compared to the previous bench-top version. Similarly, another OFS system is demonstrated by integrating integrated photonics chips, optical comb chips, and CMOS electronics [15].

Prior Art in Photonic Links

Much work has been done in increasing the integration of photonic and electronic devices, such as in heterogeneously-integrated photonic links and photoreceivers. For example, a 16 Gb/s RoF photonic link was demonstrated operating with a 20 GHz carrier frequency, involving a tightly integrated germanium-on-silicon (Ge-on-Si) photodiode (PD) on a SiP chip and transimpedance amplifier (TIA) on an electronic BiCMOS chip [20]. Another photonic link was demonstrated by also integrating an integrated PD SiP chip and a BiCMOS TIA chip, achieving 28 Gbaud datarate with QPSK modulation [21]. By integrating a Ge-on-Si PD SiP chip with a CMOS TIA, another work was able to show a 20 Gb/s photonic link with an RF bandwidth of 27.5 GHz [22]. Heterogeneously integrating photonic and electronic chips fabricated on separate processes continues to be a highly researched area. This is due to the fact that the individual processes can be tailored to emphasize the desired performance for each side of the microwave photonic interface. Homogeneous integration is still a developing field, and will surely continue to grow. The cost of a monolithic platform can be competitive and internal parasitics would be reduced significantly. However, until the performance of photonic devices on silicon processes are improved significantly, heterogeneous

approaches will continue to provide high-performance and cost-effective solutions.

1.2 Thesis Statement

Heterogeneously-integrated electronically-assisted photonics offers improved solutions for widespread applications in emerging high-speed optical paradigms due to high bandwidths, low noise, and chip-scale complexity, reliability, and cost effectiveness. Additionally, they can satisfy low-noise requirements necessary for power-efficient chip-scale photonic system implementations.

Design techniques to be utilized in this research for achieving the stated goal include designing of high-speed GHz-bandwidth Si CMOS electronics, as well as design of very low-noise electronics in a SiGe BiCMOS processes. Specifically, the circuits designed include several generations of transimpedance amplifiers and phase-locked loops, designing of integrated silicon photonic circuits including photodiode arrays and thermal phase shifters, and designing and implementing integration schemes of electronic and photonic chips in the form of photonic links and optical phase-locked loops. These heterogeneously-integrated electronically assisted photonic systems promise cost-effective and high-performance solutions in chip-scale implementations.

1.3 Research Approach

The presented work primarily focuses on the following research questions:

- **Research Question 1.** What are the current bottlenecks limiting bandwidths in the heterogeneous integration of photonic and electronic chips?

- **Research Question 2.** In what ways can the noise of a heterogeneously integrated photonic/electronic link be minimized?

- **Research Question 3.** How can the co-design methodology for integrating photonic and electronic chips be leveraged to achieve the lowest minimum detectable signal in optical links?

- **Research Question 4.** What are the fundamental limitations for the linewidth of the RF optical beat signal at high RF and mm-Wave frequencies and how far can this be reduced?

To best address the aforementioned research questions, the following primary research thrusts are proposed. The dissertation chapters are also organized as such.

- **Research Thrust 1:** High-Bandwidth CMOS Transimpedance Amplifiers and Photoreceivers

  This research thrust will seek to investigate current bottlenecks in the achievable bandwidths, conversion gains, and noise performances of transimpedance amplifiers. Additionally, the thrust attempts to better understand the necessary co-design for successful integration of the amplifiers and photodetectors to result in high performance photoreceivers with maximum levels of integration.

- **Research Thrust 2:** Low-Noise SiGe Transimpedance Amplifier and Photoreceiver

  This research thrust aims to create a heterogeneously integrated photoreceiver with an emphasis on the noise performance as opposed to the bandwidths. By leveraging the benefits of a SiGe BiCMOS process, the work aims to create a very low noise link still capable of microwave bandwidths. Co-design continues to be crucial as additional loss in packaging and integration will lead to link performance degradation.

- **Research Thrust 3:** RF Photonic Circuits on Silicon Photonics Platform

  This research thrust aims to explore the current state-of-the-art devices and performance achievable on a silicon photonic platform. It will leverage the photonics platform to develop photonic circuits suitable for heterogeneous integration with CMOS electronics chips. The focus of the exploration includes on-chip photodetectors, arrays, and circuits.

- **Research Thrust 4:** Optical Phase-Locked Loop

  Combining the previous research thrusts, the investigation into the optical phase-locked loop will combine electronic CMOS circuitry with optical components from a silicon photonics platform. By heterogeneously integrating these two chips, the research seeks to provide a tightly-packaged chip-scale solution for phase-locking the microwave beat signal generated via optical heterodyne.

1.4 Research Contributions

The research presented in this dissertation has contributed to the field of electronics and photonics, primarily in heterogeneous integration strategies. Additionally, the work merges high performance circuits in both domains to maximize system performances while leveraging the cost-effectiveness and adaptability of heterogeneous integration approaches. The highlights of the work presented in this dissertation are listed below:

- The design, implementation, and fabrication of a novel topology of transimpedance amplifier allowing increased bandwidths, higher gain, and relaxed voltage overhead issues.
- The design, implementation, and measurement of a novel dc-compensating architecture for integration of photodiode and transimpedance amplifier, effectively de-coupling the biasing and improving the circuit use-case adaptability.
- The design, implementation, and measurement of low-noise SiGe transimpedance amplifier integrated with InP-on-Si photodiodes, investigating the low-noise performance achievable while maintaining microwave bandwidths.
- The design, implementation, and measurement of several generations of photoreceivers integrating high-performance photodiodes and the novel transimpedance amplifiers.
- The design and implementation of several optical components and circuits on a new silicon-photonics platform, investigating the achievable metrics for future design.

- The design and implementation of a two-chip optical phase-locked loop solution, involving a CMOS electronics chip and silicon-photonics chip, heterogeneously integrated.

1.5 Complete Publications List

First-Authored Publications

- R. Costanzo, Z. Yang, N. Raduazo, A. Beling and S. M. Bowers, "A 10 GHz bandwidth balanced photoreceiver with 41 V/W optical conversion gain," *2017 12th European Microwave Integrated Circuits Conference (EuMIC)*, Nuremberg, 2017, pp. 151-154.

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Chapter 2

High-Speed Photoreceivers with CMOS Transimpedance Amplifiers

2.1 Introduction

2.1.1 Background, Prior Art, and Application Spaces

The photoreceiver is a critical element in an optical link. A typical photoreceiver consists of a photodiode and a transimpedance amplifier (TIA), which together are responsible for sensing, receiving, and amplifying an incoming optical signal. The photodiode converts an incoming optical signal to an output RF current signal, and the transimpedance amplifier converts the RF current signal into an output RF voltage signal so that subsequent digital circuits can process the signal. This signal could come from a fiber when used in radio-over-fiber links or even an on-chip waveg-

uide when used in chip-scale photonic systems. The metrics that a photoreceiver emphasizes will depend dramatically on what kind of application space it is being used in.

One such application is the radio-over-fiber (RoF) link, used to rapidly transmit dense amounts of data in a mm-Wave communications paradigm often presented in recent discussions of the 5G network. Due to the growing number of internet-connected devices and increasing demands for high definition streaming, high-bandwidth interconnects are required in order to provide fast datarates. One approach to meeting this demand is utilizing high-bandwidth optical fiber communications. Optical fiber communications offer a variety of benefits, including low attenuation and greater transmission distances, making it ideal for long-haul communication. As the demand for high-data content continues to grow, photoreceivers with improved bandwidth and noise performance are desirable for use in optical interconnects, facilitating higher speed machine-to-machine communications such as in server farms and radio-over-fiber (RoF) networks [23, 24]. Communicating in the optical domain provides significant benefits for such applications, the most of which include high intrinsic bandwidths and low attenuation in fiber compared to electrical interconnects that may experience significant loss at higher frequencies. However, benefits of fiber communications can be applied to more localized applications that are closer to the user. For example, photonically driven radiators convert signals from the optical domain to wireless microwave transmission, potentially allowing localized high speed access points for data transmission [25]. Another solution is to develop cheap and compact photoreceivers to expand optical fiber to smaller indoor transmission cells for a RoF network [26, 27]. In order to facilitate higher data transmission rates for an increasing number of users, the RoF and existing fiber network should be extended further to near-user

access points, creating smaller but more numerous "picocells". Inexpensive photoreceivers would enable fiber communications for not only long-haul, but also short-haul local transmissions. High bandwidth, inexpensive photoreceivers are required to implement this highly localized scheme for fiber communication. Optical receivers have other qualities making them well-suited for these dense communication applications such as their high bandwidths and resistance to electromagnetic interference [28].

Another such application is optical frequency synthesis, which enables the synthesis of a precise, clean optical frequency by locking to a clean microwave source [14, 19]. Optical frequency synthesis has found many important uses in a variety of fields. For example, some applications that utilize OFS include optical metrology, terahertz spectroscopy, imaging, and light-detection and ranging (LiDAR) [29, 30]. These systems require the use of high performance microwave TIAs and photoreceivers. In OFS systems, it is crucial to extend the bandwidth of the TIA, as well as the photodiode (PD). With higher TIA and photoreceiver bandwidths, range of synthesizable frequencies is increased and physical sizes of optical combs can be decreased. Photoreceivers used in OFS systems should also present low noise levels to minimize required optical signal levels, lowering the system's overall dc power consumption as optical sources consume significant percentages of system power. Inversely, photoreceivers also play an important role in microwave photonic systems that generate RF and mm-Wave frequencies from optical sources [5, 31]. Reductions in size and power can be achieved in these systems by utilizing tightly integrated photoreceivers, some even utilizing photonic integrated circuits [32, 33, 34]. TIAs can be fabricated in many different processes, but CMOS offers the ability to be directly integrated with subsequent logic circuits in-

expensively. This integration is vital, as challenges faced by OFS systems include the size, cost, and power consumption. These benefits in size, power, and cost are crucial as much of the recent work in OFS systems has targeted high integration with reductions in size and power, moving away from bench-top and towards chip-scale implementations. Much of the recent work on OFS involves moving towards low power, chip-scale implementations [19, 29].

2.2 Considerations for High-Speed Photoreceivers

When designing a photoreceiver, there are three main aspects that will directly determine the performance and achieved metrics. The first is the photodetector, or photodiode (PD). The second is the transimpedance amplifier (TIA). The third is the integration scheme used to combine the two blocks. This section will discuss the three aspects and the associated trade-offs that exist for each.

2.2.1 Photodetectors

The first block in the photoreceiver is the PD. As previously discussed, the photodiode is a critical element at the transition between the optical and the electrical domain. The basic principle of operation for a PD is the internal photoeffect [35]. This effect exists in most semiconductors, but varies in strength. When a semiconductor is illuminated by light, there is an increase in its electrical conductivity. This is because the energy from the photon is absorbed, resulting in the generation of a free electron-hole pair. This pair can now undergo transport effects when subject to an electric field, resulting in electric current. As such, modifications can be made to the semiconductor to

increase its absorption of photon energy, including the implantation of various concentrations of dopant layers.

Additionally, these devices can include internal amplification, in which the free electron-hole pairs can energize and free other electron-hole pairs. PDs with internal amplification are known as avalanche photodiodes (APDs). The amplification leads to an increased responsivity, but is not without cost. The amplification mechanism leads to increased noise added to the signal. These types of PDs excel in applications such as single-photon counting [36].

The amount of output current (known as photocurrent) per unit of input optical power is known as responsivity, and is often reported in amperes/watt (A/W). By increasing the reverse bias voltage applied to the PD junction, the electric field can be strengthened leading to an increase in responsivity. Additionally, the effective capacitance across the PD junction is inversely proportional to the applied reverse bias voltage. This means that a higher reverse bias voltage will lower the effective junction capacitance, which is desirable for high-speed photoreceivers. However, the increased electric field also leads to an increase in the static current flowing through the device even when no optical signal is present. This noise current is known as the dark current. The responsivity, junction capacitance, and dark current are three of the most important metrics for the PD in a high-speed photoreceiver, and can be altered dramatically with various PD designs.

For high-speed photoreceivers, the responsivity directly impacts the transfer function of the photoreceiver. For a fixed input optical power level, PDs with higher responsivities will be able to output a higher RF current signal to the TIA, which is preferable from a signal-to-noise ratio (SNR) perspective (assuming a fixed dark current). A higher SNR for the photoreceiver can allow for sev-

eral trade-offs. First, the optical source in the link no longer needs to provide as much power. As optical sources like lasers tend to dominate the power consumption in photonic systems, this will directly reduce the overall system power consumption dramatically. Alternatively, a higher SNR can also enable the distance of the photonic link to be increased as there is increased margin for attenuation. Lastly, higher SNR values can be utilized in the form of higher modulation schemes, resulting in higher data throughput for the optical link.

Junction capacitance of the PD is also crucial to consider when implementing a high-speed photoreceiver. Most often, the dominant RC time constant that limits the overall bandwidth of the receiver is the time constant associated with the junction capacitance of the PD (C_{PD}) and the input impedance of the TIA. By lowering the effective C_{PD}, the dominant time constant can be lowered, and the first pole of the system pushed out towards higher frequencies. This directly results in an increase of the system bandwidth (unless there is another limiting time constant). A higher bandwidth for the receiver can provide higher data throughput for communication links, or higher tunability ranges for optical frequency synthesis (OFS) systems. C_{PD} can be altered in several ways, including during the material and doping designs, as well as by PD size. PDs with larger total area will have a greater C_{PD} than smaller ones, but may have higher absorption and responsivity.

Dark current is another critical performance metric in the PD. The dark current is a "noise" current that is present even with no input optical signal. This dark current will degrade the SNR by acting as a current noise directly at the input of the TIA. It will be injected into the TIA and amplified to the output. The minimum detectable signal of a PD is the input optical signal required for the

output current signal to rise above the level of the dark current. As such, the amount of dark current directly impacts the optical link's fidelity.

In general, for use in RF photonic circuit design, several models can be used to represent a PD. The model is useful to the designer of the transimpedance amplifier as it allows simulation of the interface between the PD and TIA. Shown in Figure 2.1(a) is the PD model that has been used in the subsequently described works to help during photoreceiver simulations. The values of the components are adjusted to best fit to empirical data recorded for any specific device.

2.2.2 Transimpedance Amplifiers

The transimpedance amplifier (TIA) takes the output current signal from the PD as an input and converts and amplifies it to an output voltage signal. This is useful as many of the subsequent digital or mixed signal circuits sense voltage rather than a current signal. It should be noted that a resistor can provide transimpedance (conversion of a current to a voltage) for a PD. The resistor provides a transimpedance of R, and creates a time constant at the input node of $C_{PD} * R$ which dominates the photoreceiver bandwidth as previously discussed. Additionally, the noise generated at the output of the photoreceiver is independent of the resistor's value [37].

The primary reason that transimpedance amplifiers are used instead of a resistor is that the trade-offs between the bandwidth of the system and the transimpedance gain is improved dramatically. Typically, the input impedance (Z_{in}) of the TIA is designed to be low to minimize the limiting RC time constant. As such, a resistor with an equivalent resistive value (R=Z_{in}) would result in

the same time constant. However, while the transimpedance of the resistor is simply R, the transimpedance of the TIA is much greater than its Z_{in}. In other words, the transimpedance gain (Z_T) of a TIA is greater than its input impedance. This eases the trade-off between the photoreceiver gain and bandwidth.

In designing high-speed photoreceivers, the TIA input impedance is one of the most important design metrics. As discussed above, it will significantly impact the bandwidth of the overall photoreceiver, which directly determines the data transmission rate achievable. To achieve lower input impedance, often the TIA circuit will make use of negative current feedback. This feedback comes at the cost of sacrificing some of the overall transimpedance gain for an increase in photoreceiver bandwidth. Therefore, the TIA input impedance should be considered relative to the C_{PD} to determine and achieve the desired bandwidth.

In addition to the input impedance and bandwidth, the transimpedance gain of the TIA is also critically important. It will determine the SNR of the overall system and affect the required sensitivity of the following processing circuits. There are several ways to increase the gain of the TIA. First, increasing the overall Z_T of the first TIA stage. This will result in the smallest overall system noise figure as more gain at the beginning of the receiver chain will help when referring noise sources back to the input. However, this increase in gain is often achieved by increasing the input or output impedance, and will likely affect the overall system bandwidth negatively. Second, adding additional voltage gain stages after the initial TIA stage can increase the overall transimpedance gain. However, additional devices and circuitry required can negatively impact the bandwidth and noise performance. Therefore, careful consideration must be taken when determining the Z_T required

for a photoreceiver with respect to its trade-offs in bandwidth and noise.

As mentioned above, noise is one other aspect that will play a role in determining the quality of an optical link. The noise of the TIA is typically the dominant source of noise when compared to the dark current provided from a PD. Therefore, the TIA will have the most significant impact on determining the overall system SNR, which will limit the types of data modulation schemes usable with the optical link. This will lead to a limit in the receivable data rate. Additionally, the TIA's noise will contribute to raising the minimum detectable signal level of the input optical signal to the photoreceiver.

2.2.3 Integration Schemes

Another important aspect of photoreceiver design is the integration scheme for the PD and TIA. In the context of this dissertation, heterogeneously integrating a photoreceiver means using a PD and TIA which are fabricated in different processes and are on different chips. While homogeneous integration of photoreceivers has been shown [38, 39, 40] and offers highest levels of integration, heterogeneous integration offers some advantages. One such advantage is being able to maximize the individual performances of the PD and TIA. PDs are often fabricated in III-V semiconductor materials due to their typically higher level of performances. Silicon-based PDs tend to have low efficiency and poor responsivity. While TIAs can be fabricated in III-V processes [26, 27], they are usually more costly to fabricate. Additionally, implementing the TIA on silicon in a CMOS process allows higher levels of circuit complexity, higher yield, and direct integration with the

subsequent processing circuits.

There are several ways to heterogeneously integrate the multiple chips. The most straightforward involves integrating the two chips on a substrate with routes and wirebonds. This is a very flexible and cost-effective method of heterogeneous integration, but may introduce additional parasitics. As previously discussed, the capacitance and impedance of the node between the PD and TIA are critical in determining the bandwidth of the photoreceiver. If the substrate trace is not designed appropriately, it could add some capacitance to this node. Additionally, any signal loss between the two chips due to trace and wirebond loss will result in degradation of the receiver SNR. As such, the devices should be as close as possible to minimize on-substrate losses. The flexibility of this integration method also allows the insertion and use of tertiary circuits or chips. For example, in high-power applications, it is often useful to have a bias-tee between the PD and TIA to provide a return path for the dc photocurrent. However, making a bias-tee with a low enough cutoff frequency can require a physically large and area-expensive inductor. As such, it becomes possible to insert a discrete bias-tee in between the two chips on the interposer as needed.

Another way is to flip-chip the PD and TIA chips together using controlled collapse chip connection (or C4). This method involves depositing solder bumps on the pads of the chips, sandwiching the chips together with their pads aligned, and then reflowing the chips so that the solder bumps form direct connections between the pads of the two chips. This connection method helps minimize the parasitics between the pads, as they reduce the amount of routing required. However, this method is very complicated in comparison, and requires additional alignment shapes and marking layers. The additional area dedicated solely to alignment layers could potentially increase the cost

of a chip prohibitively.

All of the works presented in this dissertation are heterogeneously integrated on an interposer substrate, primarily due to cost (wirebonds vs. flip-chip) and technology availability (separate electronic and optical chips vs. a homogeneously integrated process).

2.3 Photoreceiver with Regulated Cascode (RGC) TIA in 130 nm CMOS

Summary

A 10 GHz bandwidth photoreceiver is demonstrated. The photoreceiver consists of two photodiodes (PD) in a balanced configuration to generate a single-ended input to the transimpedance amplifier (TIA). The PDs achieves a responsivity of 0.48 A/W, and a 15 GHz bandwidth while driving a 50 Ω load under the designed biasing. The regulated cascode TIA is implemented in a 130 nm RF CMOS process. The TIA achieves a transimpedance gain of 39 dBΩ. The complete photoreceiver achieves a conversion gain of 41 V/W across a 10 GHz bandwidth with the TIA consuming 56 mW from a 2 V supply, and the PDs drawing 1.2 mA from +/-5 V supplies. High sensitivity is achieved due to a low noise equivalent power (NEP) of 86 pW/$\sqrt{\text{Hz}}$.

Design

The photoreceiver design is shown in Figure 2.1. The first component is a photodiode, responsible for the conversion of the optical signal power into an RF current signal. This current is input into the transimpedance amplifier (TIA), purposed with converting the current signal into a voltage signal sent to the rest of the processing circuits. Important metrics for the photoreceiver include bandwidth, noise equivalent power (NEP), dc power consumption, and conversion gain. When designing the components for the photoreceiver, an application requiring high sensitivity and bandwidth is targeted. As such, a balanced photodiode configuration is utilized in order to increase the sensitivity of the photoreceiver. A TIA designed and fabricated in 130 nm RF CMOS is integrated on board. The photodiodes and TIA require differing voltage supplies, so a bias-tee is integrated at their interface. The bias-tee provides a dc ground path for the PD, and a short for the ac signal to propagate into the TIA. This is a crucial component in many photoreceivers as the dc current generated by the PD varies with light intensity, potentially changing the dc operating points of the circuitry in the TIA.

The most important characteristics of a photodiode (PD) are the responsivity, bandwidth, and dark current. High bandwidth and low dark currents are prioritized in order to allow the detection of very low input optical powers across a large frequency range.

The photoreceiver utilizes a balanced pair of the InP-based back-illuminated modified uni-traveling carrier (MUTC) photodiode with 15 μm diameter [28]. More specifically, the PDs are charge-compensated MUTCs, which are capable of achieving high output powers due to the implementation of a cliff layer within the fabrication process. This cliff layer can also result in higher

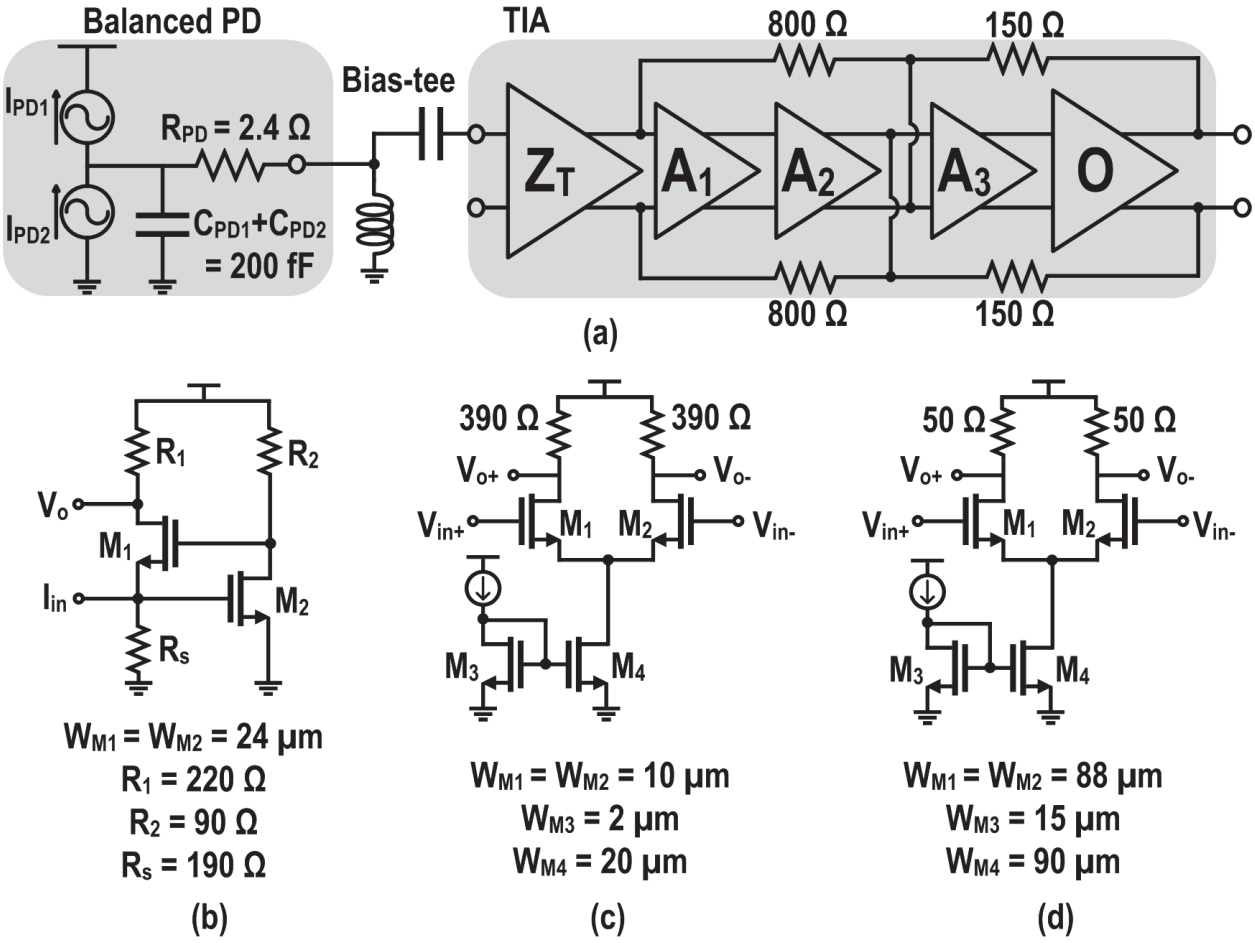

Figure 2.1: (a) Photoreceiver diagram including photodiode model and TIA schematic. (b) Regulated cascode TIA. (c) Voltage amplification stage A_1. Stages A_2 and A_3 are the same structure and thus are not shown, but the active devices are respectively 2x and 4x wider than in A_1. (d) Output buffer stage.

responsivities. The photodiodes are flip chipped onto gold coplanar waveguide (CPW) lines on an AlN substrate. Mounting the devices to the AlN substrate provides the additional benefit of increased heat dissipation.

By operating in a balanced photodiode configuration, the PDs are illuminated with differential signals and can achieve direct summing of their photocurrents, higher sensitivity, lower common mode noise, and can act as key devices in coherent and interferometric detection schemes [41].

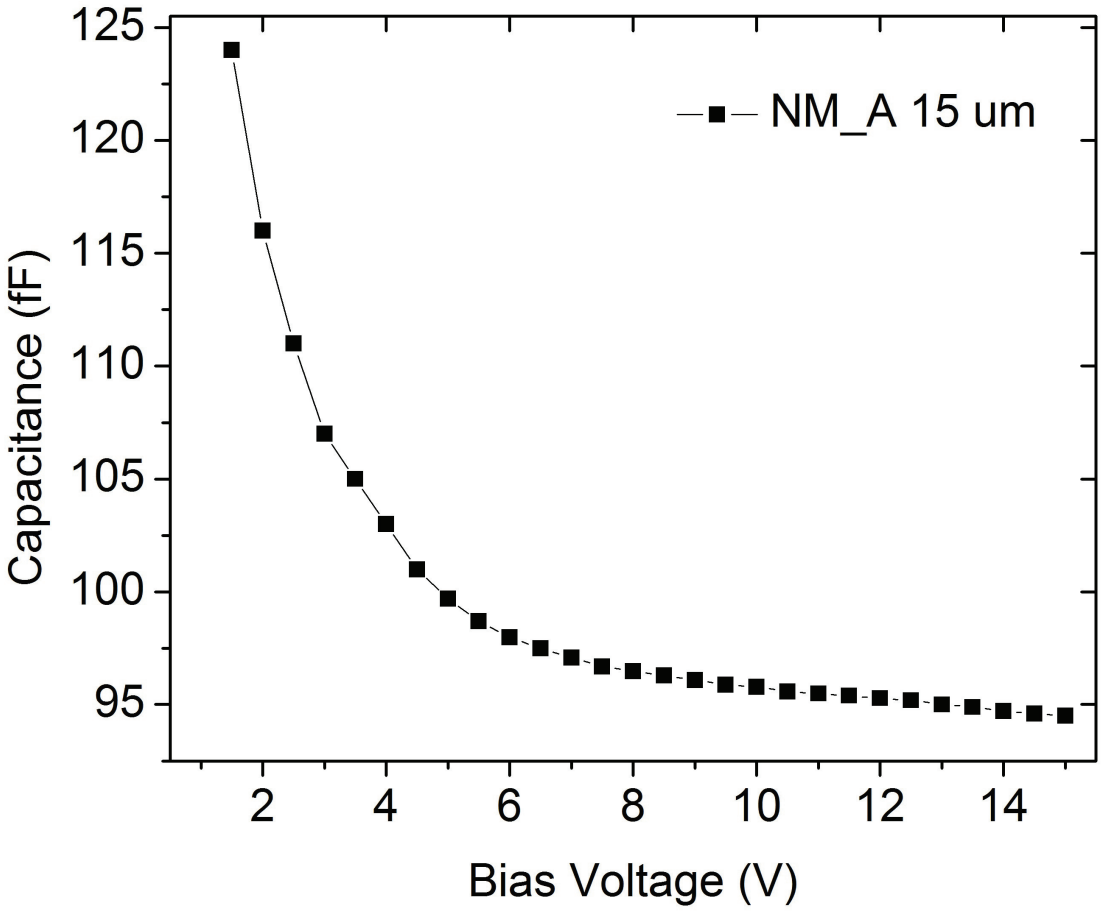

Figure 2.2: C-V curve of the MUTC photodiode.

As it is present in both photodiodes, any common mode signal or noise in the optical domain is rejected and does not appear in the output RF signal. Therefore in a differential detection scheme such as this, a balanced photodiode configuration is quite beneficial in increasing the common mode rejection.

The capacitance-voltage curve for a single MUTC photodiode is shown in Figure 2.2. As higher bias voltages are applied, the effective PD capacitance decreases. Thus, at the cost of additional dc power, the effective bandwidth of the photoreceiver can be increased. Previous measurements

indicate that a 5 V bias is sufficient for a single PD to operate up to a 15 GHz -3 dB bandwidth with a 50 Ω load.

For the desired application, the TIA is optimized to provide a high gain-bandwidth as well as low noise levels to allow the photoreceiver to be sensitive enough for low optical input powers. As the noise equivalent power (NEP) of the TIA is reduced, the overall sensitivity of the photoreceiver improves.

The PD capacitance at the input of the TIA dominates the frequency response. The TIA input impedance is minimized to reduce the RC time constant associated with the node, resulting in a movement of the first pole to higher frequencies. The regulated cascode (RGC) TIA topology, pictured in Figure 2.1, is chosen due to its ability to achieve small input impedances. The RGC small-signal input impedance can be lowered by increasing the gain of the negative feedback branch consisting of M_2 and R_2, a desirable property for maximizing system bandwidth [42]. The RGC low frequency input impedance, Z_{in}, and transimpedance gain, Z_T can be approximated in Eq. (2.1) and Eq. (2.2), respectively:

$$Z_{in} \approx \frac{1}{g_{m1}(1 + g_{m2}R_2)} \tag{2.1}$$

$$Z_T \approx R_1 \tag{2.2}$$

The actual transimpedance is lower than Eq. (2.2) due to the addition of feedback. The 800 Ω and 150 Ω resistors as seen in Figure 2.1, are configured in a negative feedback configuration. In such a configuration, some of the transimpedance gain is exchanged for higher bandwidths.

In order to add the functionality of accepting both differential inputs as well as single-ended inputs, the RGC stage is duplicated. The original RGC circuit drives the positive input of the following differential voltage amplifier while the duplicated circuit drives the negative input. When the input is single-ended, only the original RGC is amplifying the signal, while the duplicate is only providing a similar DC bias point to the negative side of the differential amplifier. In this environment, the first differential voltage amplifier will act as an active balun as well. When the input is differential, the original RGC amplifies the in-phase component of the signal, while the duplicate RGC amplifies the out-of-phase component.

Lastly, output drivers are included to drive 50 Ω loads needed for interfacing with measurement instrumentation. Because the TIA is designed to drive the high-impedance gates of a following stage, simply driving 50 Ω loads without drivers would lead to a substantial drop in gain and bandwidth.

The integration of the PD and TIA is implemented on a Rogers 4350 board, allowing transmission lines to experience a reduced high-frequency dielectric loss compared to traditional FR-4 PCB. All dc biases are applied to the devices using standard headers, and the transmission lines for signal propagation are implemented as 50 Ω conductor-backed coplanar waveguides (CBCPW). Because the balanced PD requires higher supply voltages than the TIA, it is necessary to utilize a surface mounted bias-tee at their interface in order to isolate the dc biases while coupling the ac signal.

The need for a bias-tee between the photodiodes and transimpedance amplifier is typical for a photoreceiver. An external bias-tee is used as the fabrication of a high bandwidth bias-tee in a CMOS process is difficult and expensive, due to area increase and maximum sizes for the required passive components.

The photodiodes, bias-tee, and CMOS chip are fixed to the board with silver epoxy. Connections from the devices to the board are implemented with gold wirebonds. An on-chip supply bypass network is present on the CMOS chip, and additional bypass capacitance is soldered on all the DC supplies on the board.

Due to the need for different supplies for the PDs and TIA, it is important to create a good ac ground reference to enable proper CBCPW and transmission line behavior. Therefore, single layer capacitors (SLC) with high self-resonant frequencies are connected between a shared ground reference and the different voltage supplies (VPD+, VPD-, and VDD). This shared ground reference is used as the return conductors for the transmission lines.

The CPW transmission line is chosen due to its ability to contain the signal fields between the center conductor and the in-plane return conductors. Compared to a 50 Ω microstrip line, the 50 Ω CPW line can be fabricated with a much smaller linewidth, lending to a more space-efficient design. A ground plane is then added underneath the CPW line, resulting in the CBCPW line. Because the distance from the center conductor to the in-plane return conductors is much shorter than the distance to the ground plane on the bottom metal layer, the CBCPW will still act primarily as a CPW. However, with the addition of the bottom ground plane, some of the transmission line losses are reduced and thermal conductivity is increased.

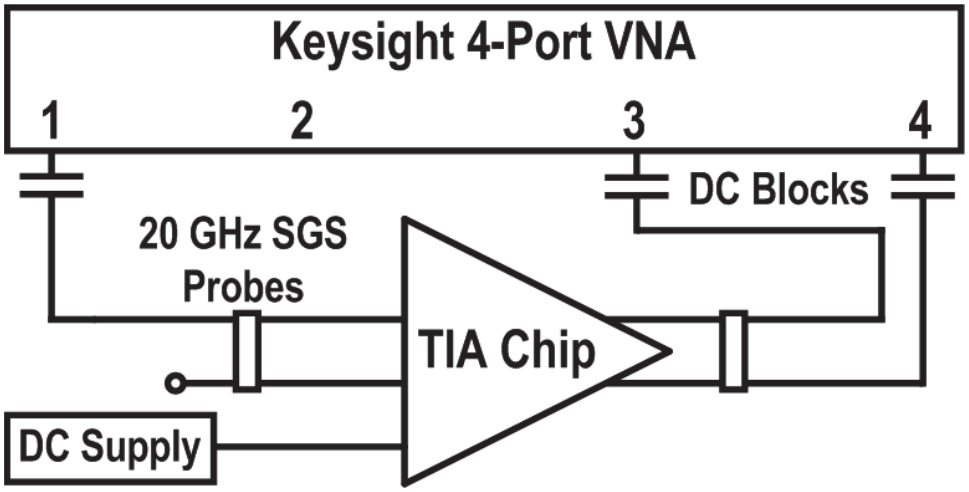

Figure 2.3: Measurement setup used to characterize TIA.

Measurements

The PD and TIA are each measured separately to verify functionality before the overall photoreceiver is measured. Microphotographs of the PD and TIA are shown in Figure 2.7. The total area of the photodiode is 1.25 mm^2 and the area of the CMOS TIA including pads is 0.4 mm^2. It is important to note that the size for the photodiode package includes 4 sets of balanced photodiodes and 2 sets of single-ended photodiodes, as indicated by the 6 sets of CPW outputs on the package. Thus, the size of a single set of balanced PDs is significantly smaller.

The TIA bandwidth and transimpedance gain are measured with the use of a 4-port VNA operating in balanced measurement mode as in Figure 2.3. With the balanced S parameter measurements, the TIA single-ended to differential power gain and transimpedance can be found.

The simulated and measured transimpedances and power gains are plotted in Figure 2.4. The TIA achieves a 39 dBΩ transimpedance and a 9 GHz bandwidth, while providing a 40 Ω input impedance. As the photodiode bandwidths were 15 GHz when driving a 50 Ω load, this input

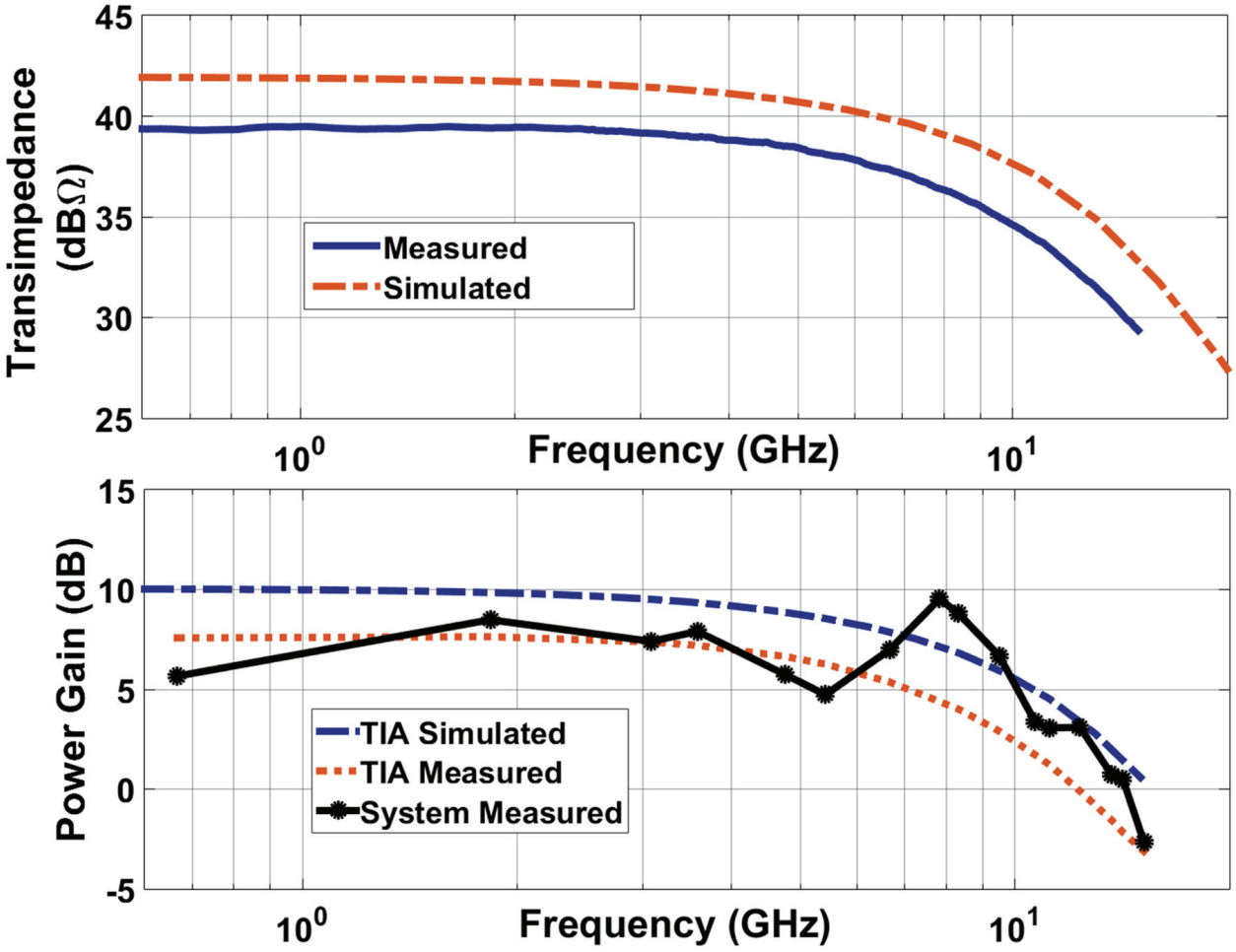

Figure 2.4: Simulated and measured transimpedance of TIA (top) and power gain of TIA and system (bottom).

impedance is sufficiently low for the desired bandwidth. The TIA dissipates 56 mW from a 2 V supply and the output external driver dissipates 39 mW from a 2 V supply. The system power gain plotted in Figure 2.4 is defined from the output of the PD to the output of the TIA to include the effects of the bias-tee and CBCPWs. The rippling and peak of the system gain is most likely due to a slight mismatch between the CBCPW characteristic impedance and the input impedance of the TIA. A CBCPW with a characteristic impedance matching the input impedance of the TIA would have resulted in a maximally flat response. However, the slight mismatch between the 40 Ω input

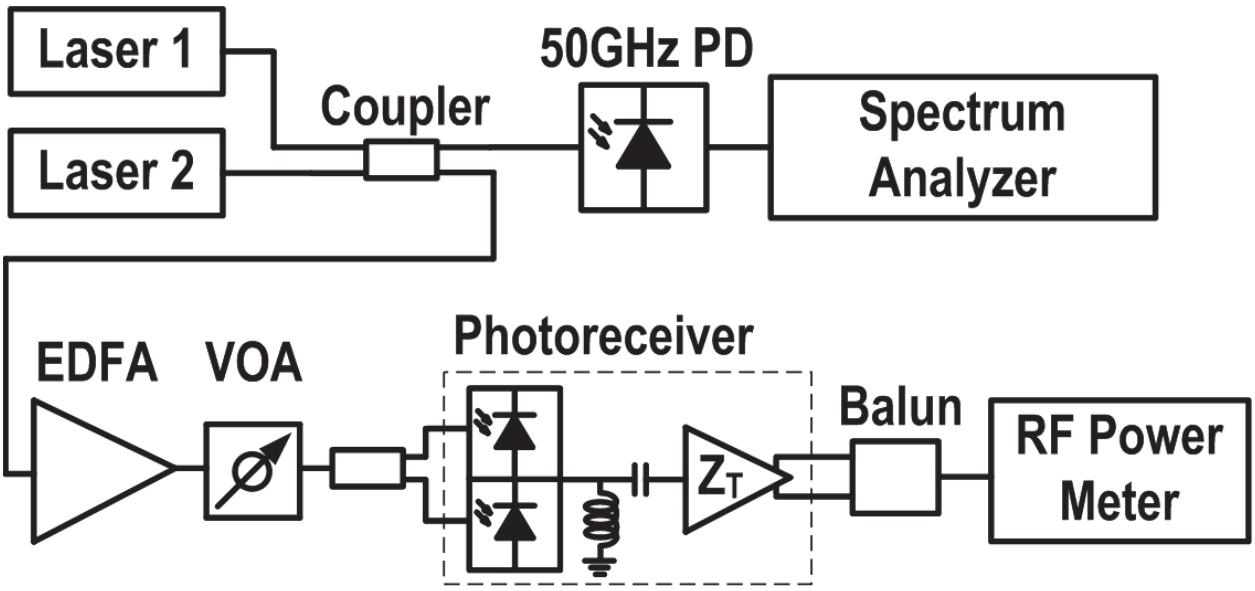

Figure 2.5: Block diagram of measurement setup used to measure system gain and bandwidth.

impedance and the 50 Ω line results in mismatched transmission line effects. The equivalent input noise of the TIA is found to be 39.8 pA/$\sqrt{\text{Hz}}$.

The photodiode C-V curve is characterized with an LCR meter. Based on the performance in Figure 2.2, the bias voltage is chosen to be 5 V across each PD, resulting in a capacitance of 100 fF for each PD. Because a balanced configuration is used, the effective PD capacitance is doubled to 200 fF. At this biasing, the PDs draw 1.2 mA of photocurrent and generate an extremely low 4 nA of dark current, making the TIA the dominant source of the noise in the photoreceiver. The balanced PDs achieve a 0.48 A/W responsivity. However, the anti-reflection coating applied to the PD during fabrication is optimized for an optical wavelength of 1060 nm, but this system is measured at 1550 nm. With the proper coating for 1550 nm, the responsivity could be increased to approximately 0.65 A/W.

The bandwidth and power gain of the photoreceiver is measured in the setup shown in Figure 2.5.

The PD is back-illuminated by the optical signal, generating RF current into the TIA. The optical signal consists of the outputs of laser 1 and 2 coupled together. The frequency of the RF signal generated by the photodiode is the frequency difference between the two lasers. The differential output power of the TIA is measured using a balun and RF power meter. Losses from the following coax cables and balun are measured separately and calibrated out of the measurement. Then, the output voltage and conversion gain are calculated and plotted in Figure 2.6.

The photoreceiver achieves an optical conversion gain of approximately 41 V/W, with a bandwidth of 10 GHz. The photoreceiver bandwidth surpasses that of the TIA alone due to the previously discussed rippling and peaking at 9 GHz, resulting in a bandwidth extension. The slight bandwidth extension may also be attributed to the additional input inductance generated by the wirebonds, potentially resonating out some of the impacts of the pad capacitances which added to the dominating RC time constants at the input node.

To measure noise, the PDs are biased on, but are not illuminated with an optical input signal. The photoreceiver output power is measured with a spectrum analyzer at various frequencies with strictly dark current input. The measurement is plotted in Figure 2.6. From a measured output noise power of -156 dBm, and a conversion gain of 41 V/W, the optical NEP is calculated to be 86 pW/$\sqrt{\text{Hz}}$, indicating that the photoreceiver is capable of detecting low signal powers.

Conclusions

A high sensitivity photoreceiver is demonstrated by integrating an MUTC balanced photodiode with a 130 nm RF CMOS TIA based on the regulated cascode topology. A conversion gain of

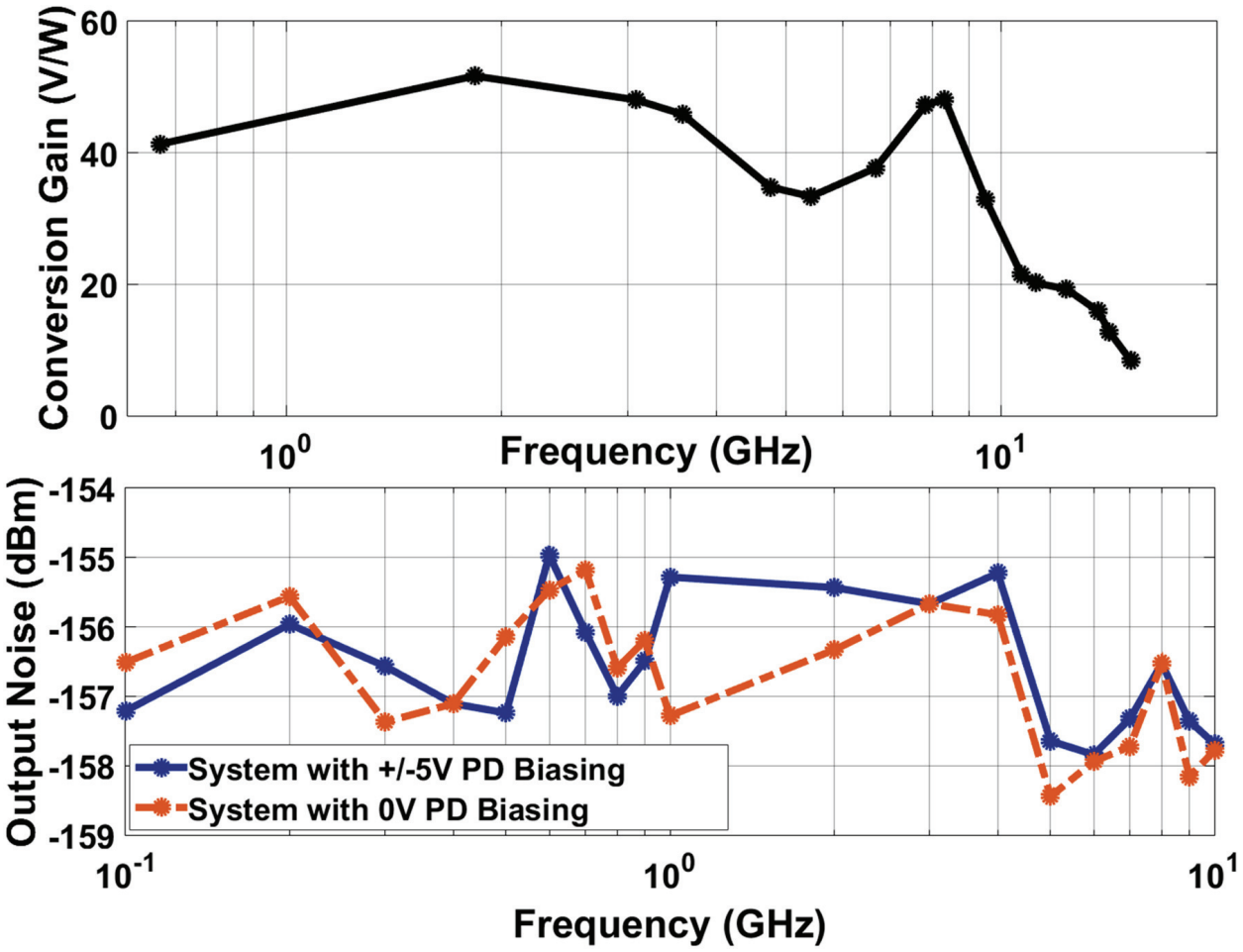

Figure 2.6: Conversion gain of the photoreceiver defined as the output voltage per input optical power (top) and the output noise power for the photoreceiver with PD biasing on and off (bottom).

41 V/W is achieved while consuming 56 mW dc power. Low signal powers can be detected due to a 0 NEP of 86 pW/$\sqrt{\text{Hz}}$. The results are summarized and compared against state-of-the-art photoreceivers in Table 2.1. While many of these photoreceivers utilize HEMT and InGaAs TIAs, results show that even in older technology nodes, CMOS is capable of providing sufficient performance for transimpedance amplification, and is suited well for use in inexpensive localized photoreceivers. To realize a highly localized RoF network, photoreceivers need to be inexpensive, small, and low power, making CMOS an exceptional candidate.

Table 2.1: Comparison of Optical Receiver Front-Ends

Metric	**This Work**	**[26]**	**[27]**	**[41]**
Bandwidth [GHz]	10	7	8	36
Conv. Gain [V/W]	41	1000	157*	35
DC Power [mW]	56	N/A	67	N/A
Area [mm^2]	78	400	N/A	2.96
PD Process	InP MUTC	InGaAs	InP UTC	InP
TIA Process	130 nm CMOS	InGaAs	PHEMT	HEMT

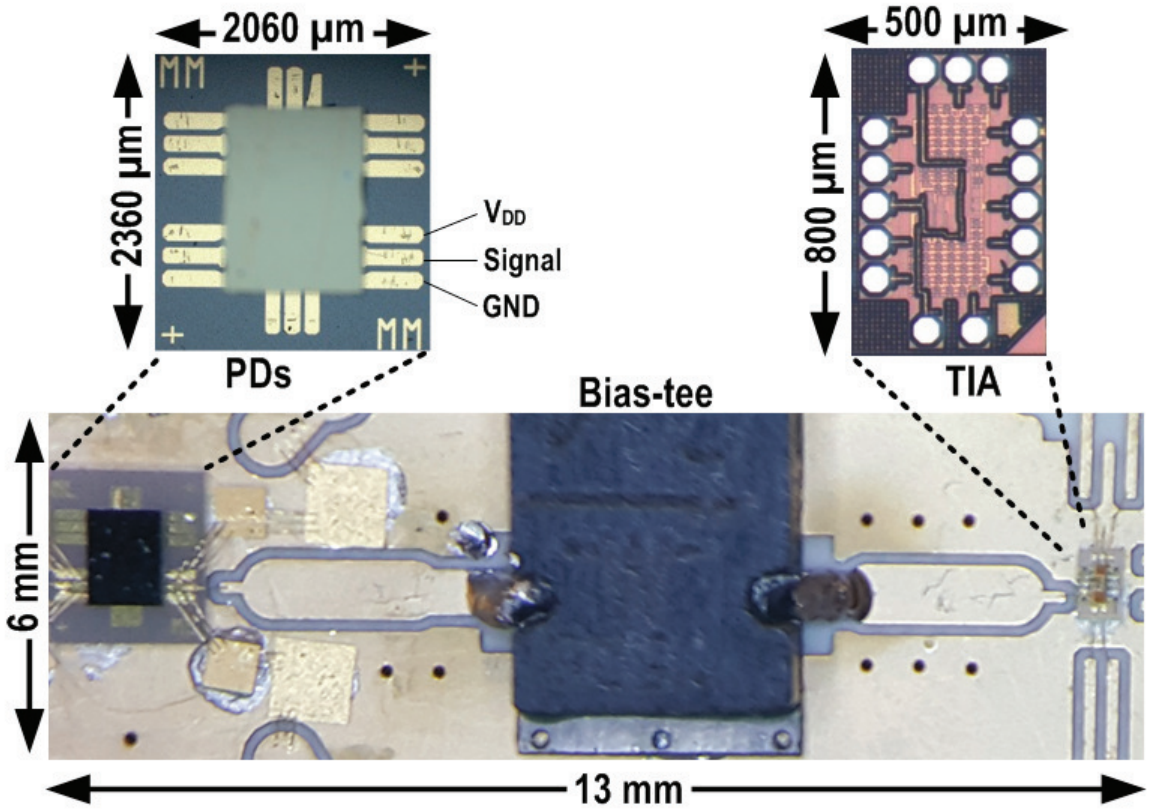

Figure 2.7: MUTC photodiode package with 6 sets of photodiodes and TIA in 130 nm RF CMOS process integrated on gold plated Rogers 4350 board.

2.4 Photoreceiver with Current-Reuse Regulated Cascode TIA in 65 nm CMOS

2.4.1 Current-Reuse Regulated Cascode (CRRGC) TIA

Summary

A transimpedance amplifier (TIA) for use in high bandwidth balanced photoreceivers is designed and demonstrated. The circuit, based on the regulated cascode (RGC) TIA, utilizes the current-reuse strategy to provide performance increases and additional benefits over the traditional RGC TIA. Implemented in a 65 nm general-purpose CMOS process, the current-reuse regulated cascode (CRRGC) TIA achieves a transimpedance of 62 dBΩ across a 3-dB bandwidth of 11 GHz while consuming 10 mW of dc power, with a unity-gain differential output buffer for driving 50 Ω loads consuming 56 mW. High sensitivity is achieved due to a low equivalent input noise of 30 pA/$\sqrt{\text{Hz}}$. The total active area of the TIA, including an active balun and unity gain output driver, is 0.08 mm^2, and 0.25 mm^2 with pads. This work focuses primarily on the design, implementation, and measurement of a novel topology of TIA intended for use in balanced photoreceivers relevant to these OFS applications.

Design

In this work, the TIA is designed for use with a balanced PD. The balanced PDs convert the incoming optical signal into an RF current signal, which the TIA then converts to an RF voltage signal. The balanced configuration is advantageous because the PDs can sum their photocurrents to

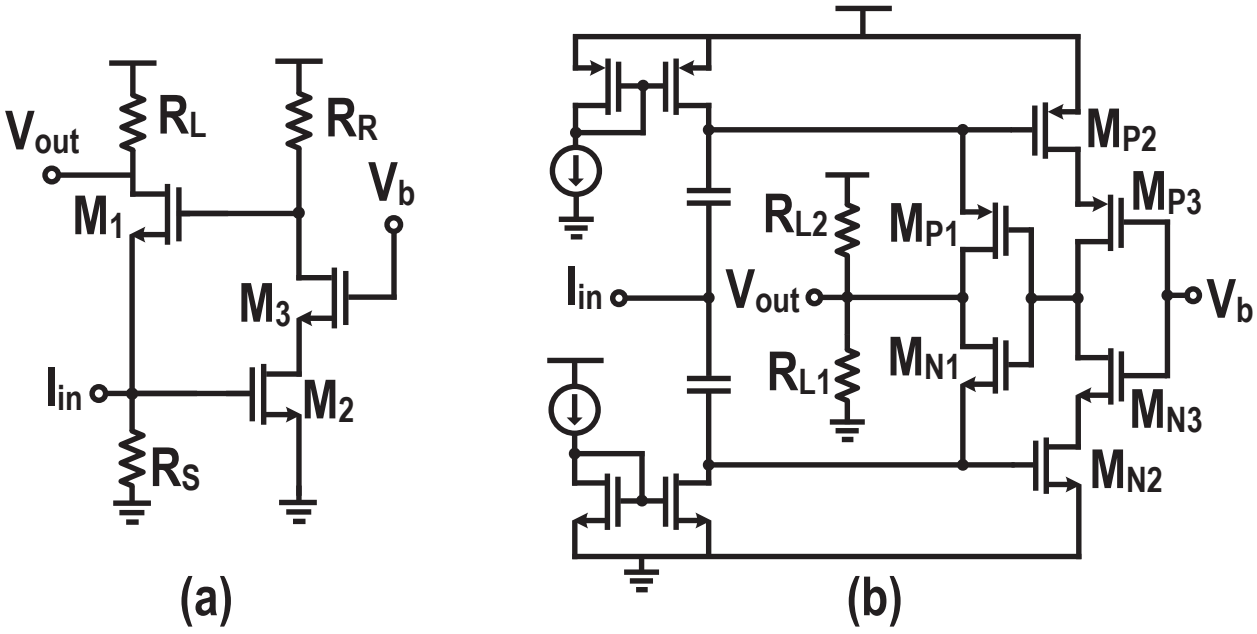

Figure 2.8: (a) Regulated cascode transimpedance amplifier (TIA) with cascode feedback loop. (b) Current-reuse regulated cascode (CRRGC) TIA.

achieve higher sensitivity, as well as reject common mode optical noise [24]. Typically, a bias-tee is required between the two to isolate the dc bias voltages and provide a dc return path for the PD. If the dc currents through the two PDs are mismatched due to fabrication variation or differences in illumination, the bias-tee can provide an alternate dc return path. In OFS applications, important metrics for a TIA include transimpedance gain, bandwidth, and input impedance. The pole created by the RC time constant resulting from the PD capacitance and TIA input impedance is often the limiting factor in the bandwidth of a photoreceiver. Therefore, it is critical to minimize the input impedance of the TIA to help maximize achievable bandwidth.

The conventional regulated cascode (RGC) topology is shown in Figure 2.8(a). The RGC TIA offers low input impedances, necessary for achieving high bandwidths in a photoreceiver [42]. The small input impedance is due to its use of a negative feedback factor [24]. In this work, a current-

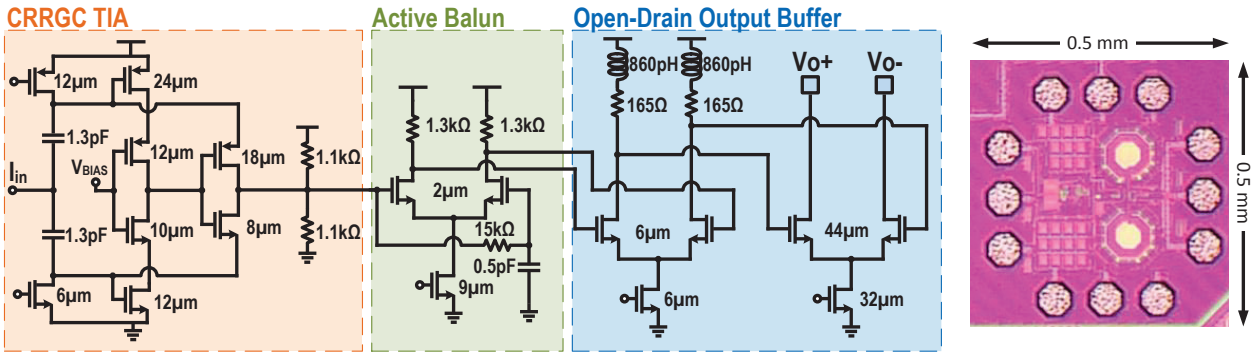

Figure 2.9: *Left*: Full schematic of the implementation of the CRRGC TIA, including active balun and open-drain output buffer. The biasing circuits and references for the current tails are omitted. All devices are minimum length. *Right*: Microphotograph of the CRRGC TIA on a 65 nm GP CMOS chip.

reuse methodology is applied to the RGC TIA to offer improvements in transimpedance performance. The current-reuse regulated cascode (CRRGC) TIA is shown in Figure 2.8(b). Because the input requires routing to two input nodes without shorting the dc components, two ac coupling capacitors are necessary at the input. These input coupling capacitors are sized for a lower cutoff of 30 MHz, but an even lower cutoff can be achieved by using larger capacitors. For the same dc current, the transconductance of the devices and the circuit gain can be improved by mirroring the original circuit with a PMOS implementation [43]. The expressions for the transimpedance and the input impedance of the CRRGC are given in Eq. (2.3) and Eq. (2.4), respectively.

$$Z_T \approx R_{L1}||R_{L2} \tag{2.3}$$

$$Z_{in} \approx \frac{1}{(g_{mn1}+g_{mp1})(1+(g_{mn2}+g_{mp2})(r_{on3}||r_{op3}))} \tag{2.4}$$

The equations are similar to those of the RGC [24], however by adding in the transconductances of the PMOS devices and the cascode feedback loop, the input impedance of the TIA can be further lowered given the same dc current. A reduction in input impedance can also be useful even in systems where high bandwidths are not necessarily required. With a lower TIA input impedance, a photoreceiver can make use of a larger photodiode (larger C_{PD}), typically resulting in a higher responsivity and overall system conversion gain, while achieving the same system bandwidth.

Another benefit that arises from the CRRGC topology is decoupling between the load impedance and voltage overhead. In the RGC circuit, significantly increasing R_L results in voltage overhead issues, limiting the achievable transimpedance. In the CRRGC, high transimpedance values can be achieved as the load resistance is comprised of R_{L1} and R_{L2}, between V_{DD} and ground. The parallel load resistors also serve to assist in dc biasing, as the desired voltage at the output node is approximately half of V_{DD}. Moving to higher transimpedance gain, both from the addition of the PMOS devices as well as increasing the values of the load resistance, is beneficial with regards to noise. With higher gain in the initial stage, the noise impact of subsequent stages, such as the balun and output buffer, is lowered. The additional PMOS devices added to implement the current-reuse technique add noise sources to the circuit, but the additional gain achieved per device helps nullify any increase in equivalent input noise of the TIA [4]. However, this increased

transimpedance will create a larger time-constant, resulting in a direct trade-off with bandwidth. The overall transimpedance limit of this configuration is approximately $r_{op1} \| r_{on1}$, and is reached when R_{L1} and R_{L2} approach open circuits.

The CRRGC topology offers an additional improvement in the form of its voltage handling capability. Because each branch of the TIA from V_{DD} to ground is a stack of four triple-well transistors, the circuit is capable of being supplied by a high voltage source without encountering breakdown. This is a useful trait for use in a balanced photoreceiver as it reduces the number of needed supplies by enabling the TIA to share the higher voltage supply of the photodiodes. This TIA is designed to operate with a 3 V dc supply, which allows 1.5 V across each of the photodiodes in the balanced configuration. Post-layout dc simulations show that the maximum voltage across any two transistor terminals was less than 1.1 V, within safe operating ranges.

The full design of the transimpedance amplifier circuit, as well as the chip microphotograph of the system implemented in a 65 nm GP CMOS process, is shown in Figure 2.9. The first block is the current-reuse regulated cascode TIA. Following the TIA is an active balun, necessary to convert from a single-ended input to differential signals. An RC filter is placed between the two gates to allow the dc voltage to be matched on either side of the balun. Propagating the signal as a differential signal is desirable as it helps to avoid issues involving crosstalk and supply noise. Lastly, the high speed unity gain open-drain output buffer is implemented in order to minimize the impact of directly driving 50 Ω loads at the differential output of the amplifier. Inductors are used at the drains of the pre-driver stage in order to achieve inductive peaking and a bandwidth extension. While omitted from the schematic, approximately 9 pF of on-chip low-Q bypass capacitance is

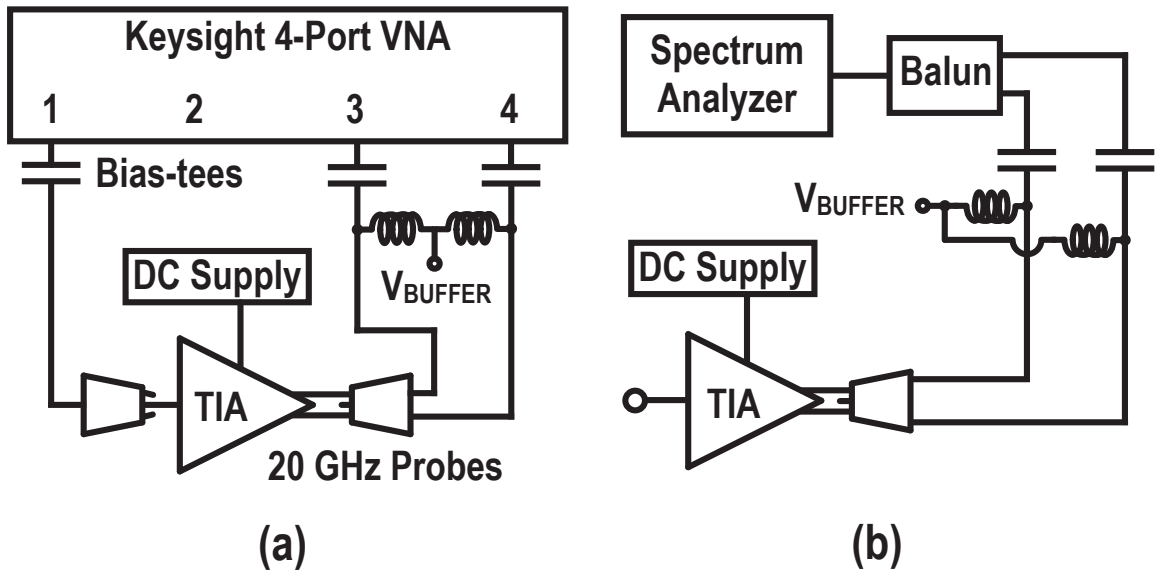

Figure 2.10: (a) Measurement setup for measuring the single-ended to differential gain and bandwidth of the TIA. (b) Measurement setup for measuring the noise of the TIA.

placed between V_{DD} and ground in order to prevent any undesired oscillations. The total active area of the TIA is 0.08 mm^2, and the total area including pads is 0.25 mm^2.

Measurements

The setup for measuring the bandwidth, single-ended to differential transimpedance, and input impedance is depicted in Figure 2.10(a). By utilizing the 4-port VNA in balanced mode, the single-ended to differential transimpedance while driving 50 Ω is calculated using Eq. (2.5), described in [44]:

$$Z_T = Z_O \cdot \frac{S_{21}}{1 - S_{11}} \tag{2.5}$$

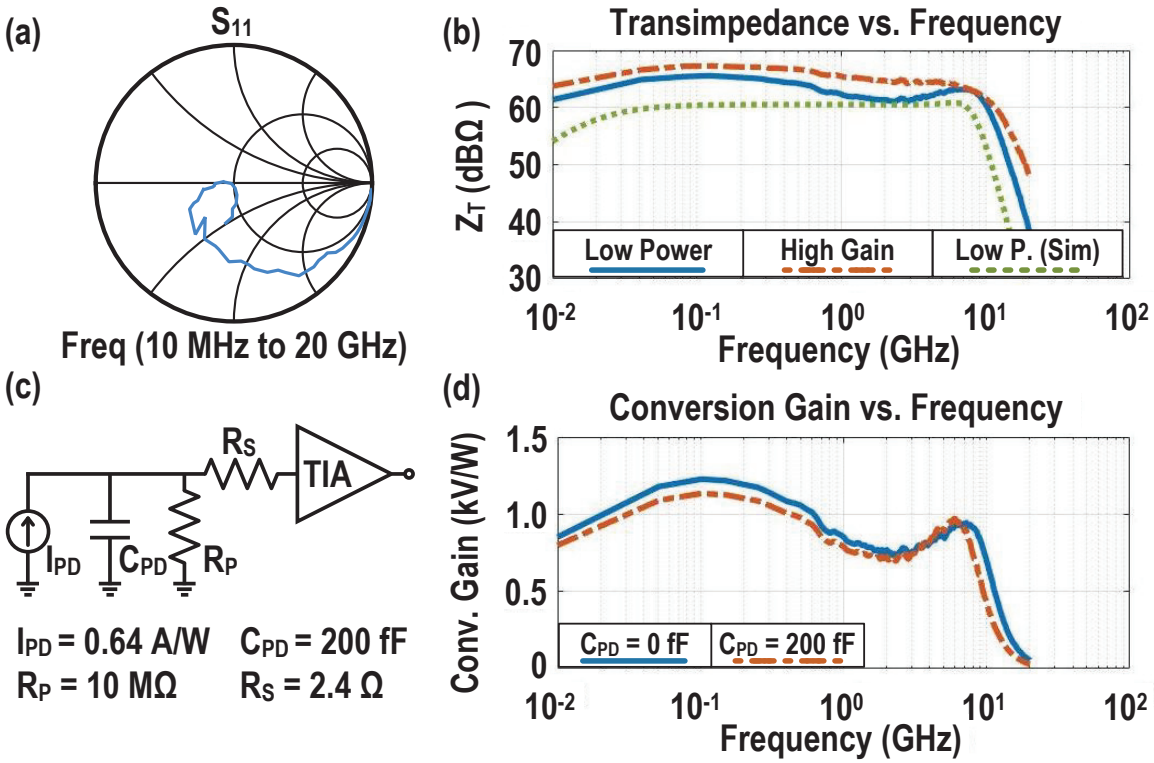

Figure 2.11: (a) Measured S_{11} of the TIA plotted on a Smith chart. (b) Measured transimpedance across frequency at two bias settings: one for low power, and the second optimized for maximum gain, along with simulation of low power. (c) PD model used with TIA measurements to model conversion gain. (d) Conversion gain in low power mode with and without a PD with 200 fF C_{PD} and 0.64 A/W responsivity.

To measure the noise of the circuit, a different measurement setup is required. The setup used is shown in Figure 2.10(b). As the input is a microwave current signal, the concern is the input equivalent current noise. In order to measure current noise, the input of the TIA is left open-circuited [45]. Then, the output power of the TIA is measured using a balun and very low noise floor spectrum analyzer. The output noise power can then be converted into the equivalent input noise by using the measured TIA transimpedance.

The TIA is measured at two bias points, one corresponding to low power and one for maximum gain. In the low power mode, the TIA and buffer consume 10 mW and 56 mW, respectively. In

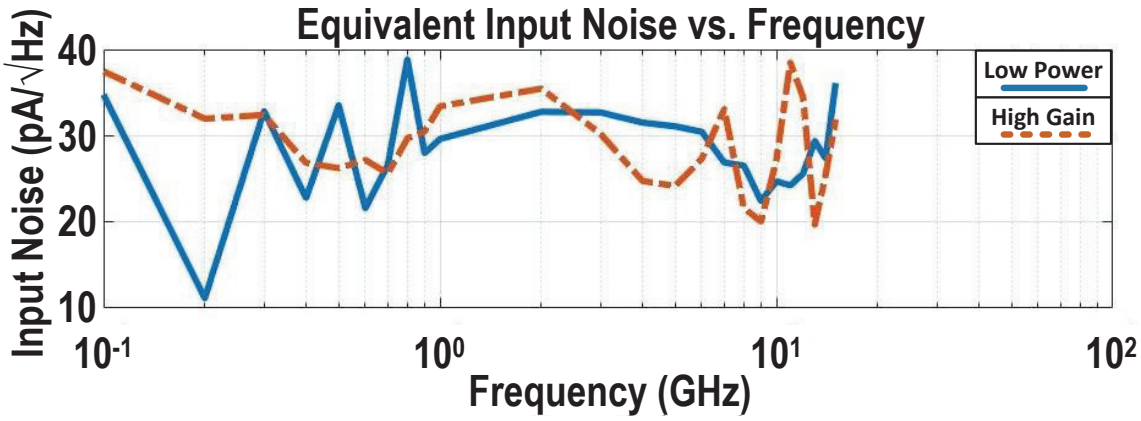

Figure 2.12: Plot of the measured equivalent input noise of the CRRGC TIA. The output noise voltage was measured and referred back to the input via the TIA transimpedance gain.

maximum gain settings, dc power increases to 27 mW and 126 mW, respectively. Measurements of the TIA are plotted in Figure 2.11. S_{11} of the TIA is shown in Figure 2.11(a). The input impedance of the TIA at low frequencies is large and is limited by the ac coupling capacitors. The transimpedance gain Z_T is calculated and plotted in Figure 2.11(b). Z_T is shown for the two bias settings, along with a simulation for the low power setting, which is the primary setting. The TIA achieves 62 dBΩ across a -3 dB bandwidth of 11 GHz. The measured S-parameter data is then combined with a PD model from [24], shown in Figure 2.11(c). The resulting simulations show a conversion gain bandwidth of 9 GHz in Figure 2.11(d). The simulation assumes a PD responsivity of 0.64 A/W and a total PD capacitance of 200 fF. The equivalent input noise of the TIA is measured to be 30 pA/$\sqrt{\text{Hz}}$, plotted in Figure 2.12.

Conclusion

A novel high-speed transimpedance amplifier fabricated in a 65 nm GP CMOS process is demonstrated, capable of achieving a 62 dBΩ transimpedance across a -3 dB bandwidth of 11 GHz. The

equivalent input current noise is measured to be 30 pA/$\sqrt{\text{Hz}}$, and the TIA core consumes 10 mW, with a 56 mW output buffer. The results are compared against performances of other published TIAs in Table 2.2. The CRRGC achieves high transimpedance across a large bandwidth.

Table 2.2: Comparison of CMOS Transimpedance Amplifiers

Metric	**This Work**	**[24]**	**[46]**	**[47]**
Bandwidth [GHz]	11	9	0.55	1.6/17
Transimpedance [dBΩ]	62	39	51-73	85/60
Eq. In. Noise [pA/$\sqrt{\text{Hz}}$]	30	39.8	3.4	N/A
DC Power [mW]	66	56	4.8	0.26*
Output Signal Type	Diff	Diff	Diff	Sing
Total Area [mm^2]	0.25	0.4	0.006†	N/A
CMOS Process	65nm	130nm	65nm	65nm

*Buffer power exempted †Active area only

2.4.2 RGC vs. CRRGC Photoreceivers

Summary

Two photoreceivers, each comprised of a set of InP balanced photodiodes (PD) and one of two CMOS transimpedance amplifiers (TIA) fabricated in a 65 nm general-purpose process, are demonstrated in this paper. The balanced photodiodes achieve a responsivity of 0.65 A/W and a bandwidth of 12 GHz while driving a 50 Ω load. The first photoreceiver uses a 9 GHz bandwidth regulated cascode (RGC) TIA with 59 dBΩ transimpedance, achieving a maximum conversion gain of 1289 V/W and a minimum noise equivalent power (NEP) of 13 pW/$\sqrt{\text{Hz}}$. The second photoreceiver utilizes an 11 GHz bandwidth modified current-reuse regulated cascode (CRRGC) TIA with 63 dBΩ transimpedance gain, resulting in a maximum conversion gain of 2083 V/W and minimum NEP of 13 pW/$\sqrt{\text{Hz}}$.

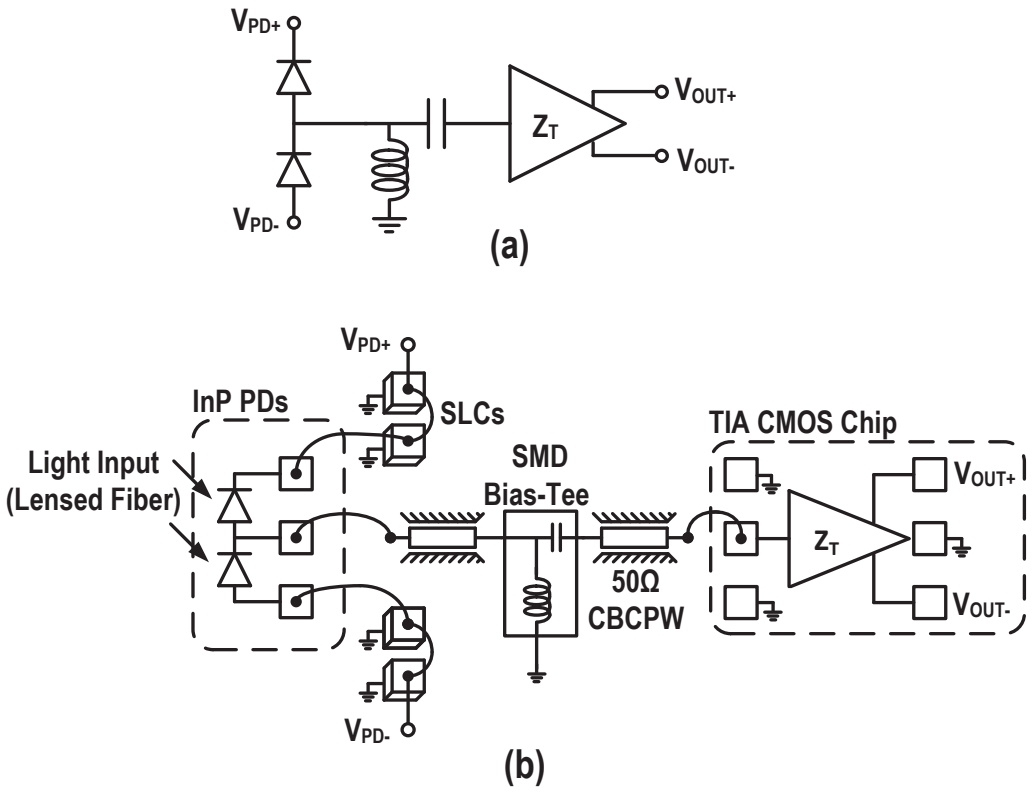

Figure 2.13: (a) A generalized photoreceiver consisting of balanced photodiodes, a bias-tee, and a transimpedance amplifier. (b) A drawing of physical scheme used to implement the photoreceivers. Single-layer capacitors (SLCs) are used in the PD supply lines to create ac shorts for proper transmission line operation. A surface mount device bias-tee is placed between the PDs and TIA, with conductor-backed coplanar waveguides connecting them. Connections from chip to board are made via gold wirebonds.

Design and Fabrication

A photoreceiver consists of a photodiode (PD) and a transimpedance amplifier (TIA). Indium phosphide (InP) PDs have been shown to be suitable candidates for high linearity, high frequency applications, including antenna remoting and RoF [48, 49, 50, 51]. Photodiodes are critical in photonic links, and desirable features such as higher responsivity and lower dark current can increase the link sensitivity [28, 52, 53]. High performance TIAs have been demonstrated in many different

processes, but CMOS offers a cost-effective solution that is readily integrable with any additional digital circuitry required [54, 55, 56, 57]. Ease of integration is critical as much of the effort in today's OFS research is directed towards reductions in size, cost, and power, with an aim in moving from bench-top to chip-scale implementations [19, 29]. This section presents two photoreceivers developed from the integration of a set of InP balanced PDs and a CMOS TIA, intended for use in the OFS application space.

The overall photoreceiver design is shown in Figure 2.13(a). The first component in the photoreceiver is a set of balanced PDs, responsible for converting the incoming optical signals into an RF current signal. The following component is a bias-tee, and the final component is one of the two CMOS TIAs.

The two PDs within the balanced structure are ideally illuminated with an RF beat frequency with an RF phase difference of 180° between the two PDs, resulting in a constructive RF output. When a common mode interferer or noise is illuminated on both PDs, the current draw of the bottom PD will cancel the current draw of the top PD. With the ideal 180° RF phase difference, the current draws will add constructively. The current summation leads to a higher output RF power from the PD [58]. Balanced PDs also provide an added benefit of increased power handling as the two balanced PDs can thermally dissipate more heat than a single PD.

The PDs are based on previously demonstrated charge-compensated modified uni-traveling carrier (CC-MUTC) structures capable of achieving high linearity and common mode rejection ratio (CMRR) for both 1550 nm [53] and 1060 nm bands [58]. The PDs used are 15 μm back-illuminated InP devices fabricated on an InP/InGaAs wafer. The devices are implemented with

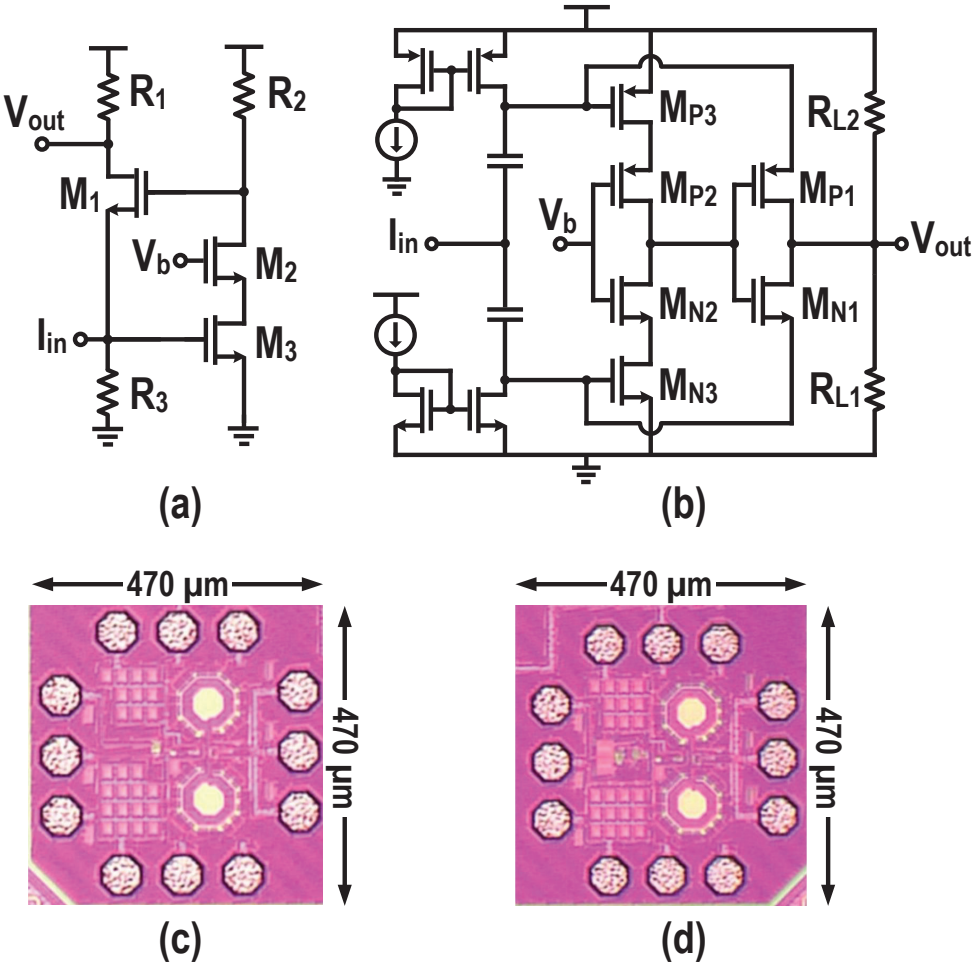

Figure 2.14: (a) Regulated cascode (RGC) transimpedance amplifier (TIA) with cascode feedback loop. (b) Current-reuse regulated cascode (CRRGC) TIA with current mirrors for biasing. (c) A chip microphotograph of the RGC TIA, balun, and output buffer. (d) A chip microphotograph of the CRRGC TIA, balun, and output buffer, both fabricated on a 65 nm GP CMOS process.

a cliff layer, resulting in higher responsivities. The PD chip is then flip-chipped to an aluminum nitride (AlN) substrate with coplanar waveguide (CPW) outputs for connectivity. The substrate also provides benefits in the form of increased heat handling.

The schematics of the TIAs used in the photoreceiver are shown in Figure 2.14(a) and (b). For this work, two photoreceivers are constructed, one with a regulated cascode (RGC) TIA, and one with

a current-reuse regulated cascode (CRRGC) TIA. The RGC TIA offers benefits in high bandwidth due to low input impedance brought about by the use of negative feedback [24, 42]. The CRRGC TIA is based on the RGC TIA, however a current reuse methodology is applied to the TIA to achieve higher feedback gain, lower input impedance, and an improved system noise performance [54]. The following stage is an active balun, converting the RF into a differential signal. Lastly, both TIAs include differential output buffers designed to drive 50 Ω loads. Schematics of these following blocks are presented previously in [54]. The TIAs are fabricated in a general-purpose 65 nm CMOS process, and the chip microphotographs are shown in Figure 2.14(c) and (d).

To achieve the low input impedance that the RGC TIA topology is known for, the circuit utilizes a negative feedback factor [42]. The input signal is amplified and inverted across the M_2 and M_3 path. This causes an effective increase in the small-signal gate-source voltage of M_1, leading to an increase in the transconductance (g_m) of M_1. A higher g_m results in a lower input impedance, as the source impedance of M_1 is inversely proportional. The equations for transimpedance gain and input impedance are shown in Eq. (2.6) and Eq. (2.7):

$$Z_T \approx R_1 \tag{2.6}$$

$$Z_{in} \approx \frac{1}{(g_{m1})(1+(g_{m3})(r_{o2}))} \tag{2.7}$$

where g_m is the FET transconductance and r_o is the FET output impedance. By adding in the PMOS "mirrored" implementation, the effective transconductance of each active device can be effectively increased. This results in a lower input impedance, which is vital in achieving higher bandwidths as the system is typically limited by the RC time constant comprised of the PD capacitance and the TIA input impedance. The equations for the transimpedance and input impedance of the CRRGC topology is shown below in Eq. (2.8) and Eq. (2.9), described in [54]:

$$Z_T \approx R_{L1}||R_{L2} \tag{2.8}$$

$$Z_{in} \approx \frac{1}{(g_{mn1}+g_{mp1})(1+(g_{mn3}+g_{mp3})(r_{on2}||r_{op2}))} \tag{2.9}$$

One advantage that can be seen from Eq. (2.6) and Eq. (2.8) is that the CRRGC TIA relies on a parallel combination of load resistors to determine the transimpedance. In the RGC TIA, when R_1 is significantly increased, the circuit will encounter voltage overhead issues. In the CRRGC TIA, this problem is eliminated. However, due to the input ac-coupling required in the CRRGC TIA, the input capacitor must be made very large in order to present low input impedances at the lower frequencies. The photoreceivers' targeted application space of OFS requires detecting only continuous wave (CW) signal tones, but the input coupling capacitor can result in poor eye

performance and bit-error rate when used in data transmission.

The balanced PDs and the TIA are integrated on a Rogers 4350B board, selected for its low dielectric loss at higher frequencies. The RF signal is generated from the PD, and propagates through a high bandwidth bias-tee, and then inputs to the TIA. These three components are interconnected with 50 Ω conductor-backed coplanar waveguide (CBCPW) transmission lines.

The bias-tee is used with both TIAs. The RGC TIA is dc-coupled, so the bias-tee provides a current return path for the PDs, preventing the photocurrent from significantly changing the biasing of the TIA. The CRRGC TIA is ac-coupled, isolating it's dc path from the PDs. In this scenario, the PDs would have no return path without the bias-tee. In the balanced configuration, the two PDs would ideally both draw the same dc current, resulting in zero dc current on the RF signal path. However, due to mismatch in fabrication or illumination, some dc current will flow into the RF path. Without the bias-tee to provide an alternate dc return path, the mismatch in PD current could lead to significant changes in the voltage at the signal node, resulting in different voltages across each PD and ultimately different responsivities.

In the balanced configuration, each of the PDs uses a different dc supply voltage. Therefore, each of these supplies need to have an ac short to the shared ground plane in order to maintain proper CBCPW operation. To accomplish this, single-layer capacitors (SLC) with high self-resonant frequencies are used as ac shorts between the PD supplies and the shared ground plane. These ac shorts allow a shorter return path for the transmission lines. Ideally the transmission lines would be kept as short as possible to minimize loss and capacitance. A drawing of the physical integration scheme is presented in Figure 2.13(b).

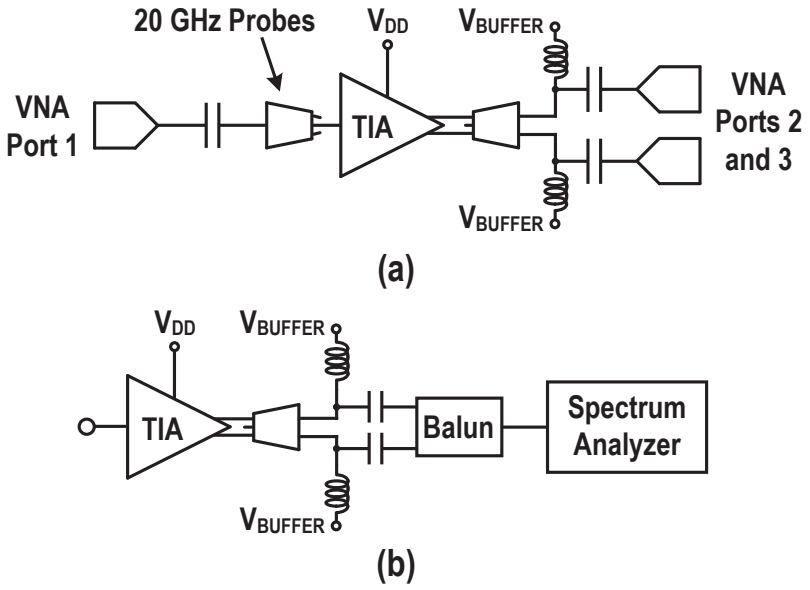

Figure 2.15: (a) Measurement setup for measuring the single-ended to differential gain and bandwidth of the TIA, using a 4-port VNA with ports 2 and 3 operating in mixed mode to capture differential s-parameters. (b) Measurement setup for measuring the noise of the TIA. The input is left open-circuited and the output power due to the noise is measured with a balun and low noise-floor spectrum analyzer.

Measurement Setup

In order to first ensure their individual operations, the performance of the PDs and the TIAs are measured separately. Then, they are integrated on-board and full photoreceiver measurements are conducted.

The two PDs in the balanced configuration are probed individually to verify similar responsivities and bandwidths to ensure that they result in a well-balanced operation. The PDs are each illuminated with the combined outputs of two 1550 nm lasers, generating an RF tone at the difference frequency. The RF frequency is swept by thermally tuning one of the laser's optical frequency,

allowing the measurement of the RF responsivity and bandwidth. This measurement is also conducted across bias voltages. Applying a higher reverse bias across a PD results in a lowering of the PD capacitance, thus achieving a higher bandwidth. A bias voltage of +/- 5 V is selected as the resulting combined C_{PD} of 200 fF should be sufficient for the desired bandwidths.

To measure the standalone operation of the TIA, the chip is wire-bonded to a chip carrier to apply the dc bias. Bondable bypass capacitors are included adjacent to the chip to create clean dc supplies and eliminate oscillations. The input and output RF are contacted using 20 GHz SGS probes. The TIA is then connected to a 4-port vector network analyzer (VNA), as shown in Figure 2.15(a) and the resulting s-parameters are used to calculate the transimpedance gain and bandwidth. The transimpedance can be calculated from Eq. (2.10), described in [44]:

$$Z_T = Z_O \cdot \frac{S_{21}}{1 - S_{11}} \tag{2.10}$$

To measure the noise, the TIA input is left open-circuited and the output power is measured on a low-noise spectrum analyzer at various frequencies [54]. The measurement setup is shown in Figure 2.15(b).

In order to measure the bandwidth of the photoreceiver, the measurement setup depicted in Figure 2.16(a) is used. Each of the PDs in the balanced configuration are reverse biased with 5 V. This means that each PD is exhibiting a capacitance of 100 fF, for a total of 200 fF C_{PD} [24]. Then, one of the PDs is illuminated by the two 1550 nm lasers generating an RF beat frequency via a

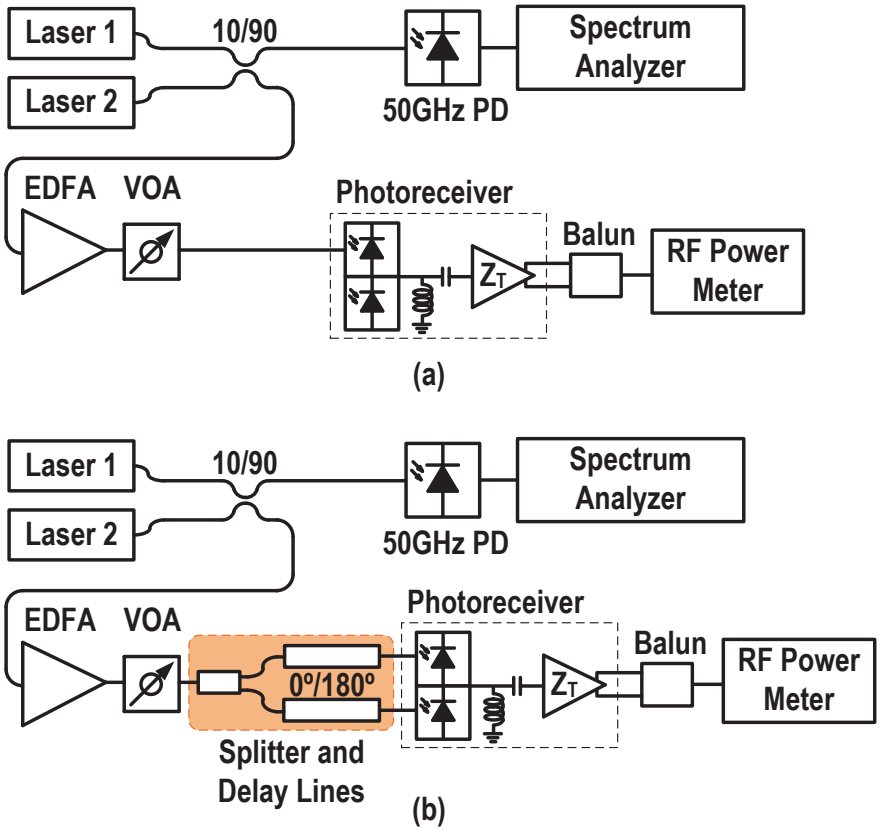

Figure 2.16: (a) Measurement setup for measuring the conversion gain, bandwidth, and (b) common mode rejection ratio of the assembled photoreceivers. Two lasers are beat together to generate an RF beat frequency based on the difference frequency. A tenth of the power is sent to a commercial PD, allowing the beat frequency to be monitored on a spectrum analyzer. The other 90 percent of the power is input into an erbium-doped fiber amplifier (EDFA), a variable optical attenuator (VOA), and split into two paths to be illuminated onto the balanced PDs. The optical delay lines can be tuned to illuminate the PDs with in-phase RF (common mode) or out-of-phase RF (differential).

lensed fiber. The fiber alignment is achieved with a manual 3-axis micropositioner, and adjusted to maintain a fixed photocurrent during the experiment, monitored with a dc source meter. The RF signal is amplified in the TIA, and the power is measured at the output using a balun and spectrum analyzer. One of the lasers is thermally tuned to sweep the generated RF beat frequency. During

the frequency sweep, the optical output powers of both lasers are kept constant and verified to be equal, providing the maximum modulation depth. The 3-dB bandwidth is extracted from the measurement of the output RF power. The lasers used are both Koheras Adjustik E15s from NKT Photonics.

Next, in order to measure the common mode rejection ratio (CMRR) of the photoreceiver, the PDs are biased as before. However, instead of illuminating only one, a fiber array with 250 μm pitch is utilized in order to illuminate both of the balanced PDs. As before, the alignment is done manually with a 3-axis micropositioner. The measurement setup is shown in Figure 2.16(b). The two lasers are combined with a 10/90 2x2 coupler. The 10 percent branch is sent to a commercial PD and spectrum analyzer to monitor the beat frequency. The 90 percent branch is input into an erbium doped fiber amplifier (EDFA) followed by a variable optical attenuator (VOA), which is then input into a 50/50 1x2 coupler to split the light into two paths. Each of these paths contains a mechanically-tunable optical delay line. By adjusting these delay lines, the phase of the RF signals in the paths can be tuned to be 180° apart at various frequencies. By introducing an optical delay corresponding to a 180° phase shift in the RF domain, the balanced photodiodes generate the beat note differentially, maximizing the output RF power from the PDs and the CMRR.

Experimental Results

The PDs utilized in the photoreceiver are similar to those presented in prior work [53]. A 5 V reverse bias is used in the system, corresponding to a PD capacitance (C_{PD}) as low as 100 fF. In the balanced configuration, the effective C_{PD} is the summation of the two device's capacitances, resulting in an effective C_{PD} of 200 fF.

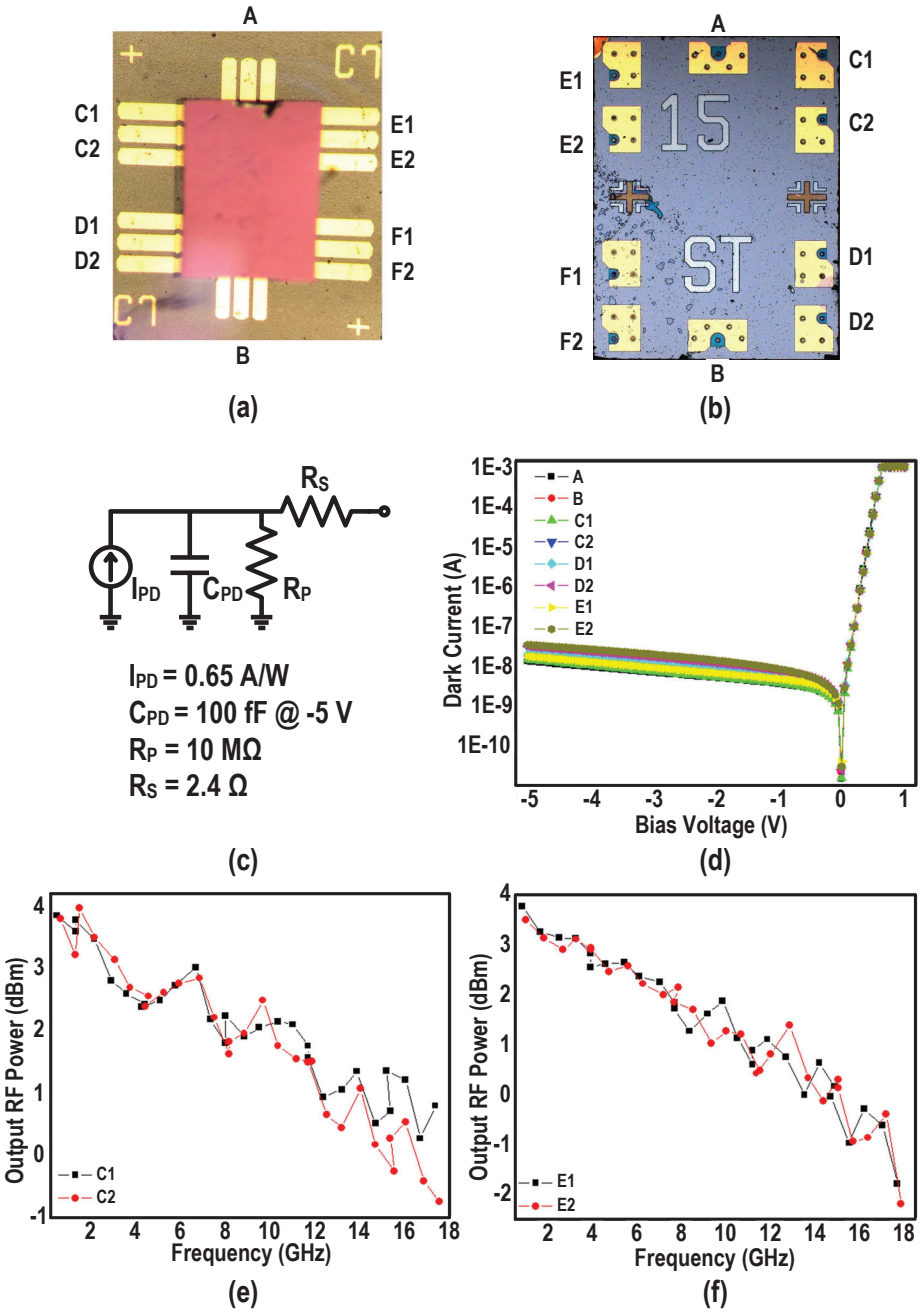

Figure 2.17: (a) Microphotographs of the backside of the PD chip and AlN substrate and of the (b) PD front side. Including the AlN substrate, the chip is 2060 μm x 2360 μm. (c) Model of an individual PD. (d) Measurements of the PD dark current across varying bias voltages. (e) Individual output RF powers of PDs C1 and C2 across varying RF beat frequency. (f) Individual output RF powers of PDs E1 and E2 across varying RF beat frequency.

As seen in Figure 2.17(a) and (b), each PD die consists of two single-ended PDs and four sets of balanced PDs. In order to verify bandwidth and proper balanced operation, the balanced PDs are each measured individually, resulting in the individual PD model in Figure 2.17(c). Figure 2.17(d) shows the dc measurements of the PDs. The dark currents measured at -5 V reverse bias are as low as tens of nanoamps. The PDs comprised of C1 and C2, as well as E1 and E2, are selected for use in the photoreceivers due to the similar RF responses between each set, shown in Figure 2.17(e) and (f). Both sets show bandwidths of 12 GHz and responses that mirror one another closely up through 15 GHz, meaning they are well-balanced and will provide a high CMRR.

The TIA transimpedance gains and frequency responses are shown in Figure 2.18. The S_{11} of the CRRGC TIA and RGC TIA are plotted respectively in Figure 2.18(a) and (b) on 50 Ω Smith charts from 10 MHz to 15 GHz. The input impedance of the CRRGC TIA is high at low frequencies and is limited by the input ac-coupling capacitors. The RGC TIA does not have an input coupling capacitor and maintains a relatively constant input impedance. The transimpedance can be calculated from the measured s-parameters, and is plotted in Figure 2.18(c). The RGC TIA achieves a transimpedance gain of 59.1 dbΩ while the CRRGC TIA achieves 63.2 dbΩ. The equivalent input current noise densities of the TIAs are plotted across frequency in Figure 2.18(d). This is calculated from the measured output noise power and transimpedance. The RGC TIA achieves an equivalent input noise current density of 37 pA/$\sqrt{Hz}$ and the CRRGC TIA achieves 30 pA/$\sqrt{Hz}$. The RGC TIA consumes 68 mW, and the CRRGC TIA consumes 66 mW, including the baluns and output buffers.

The conversion gain of the photoreceiver is measured as the output RF voltage as a function of the

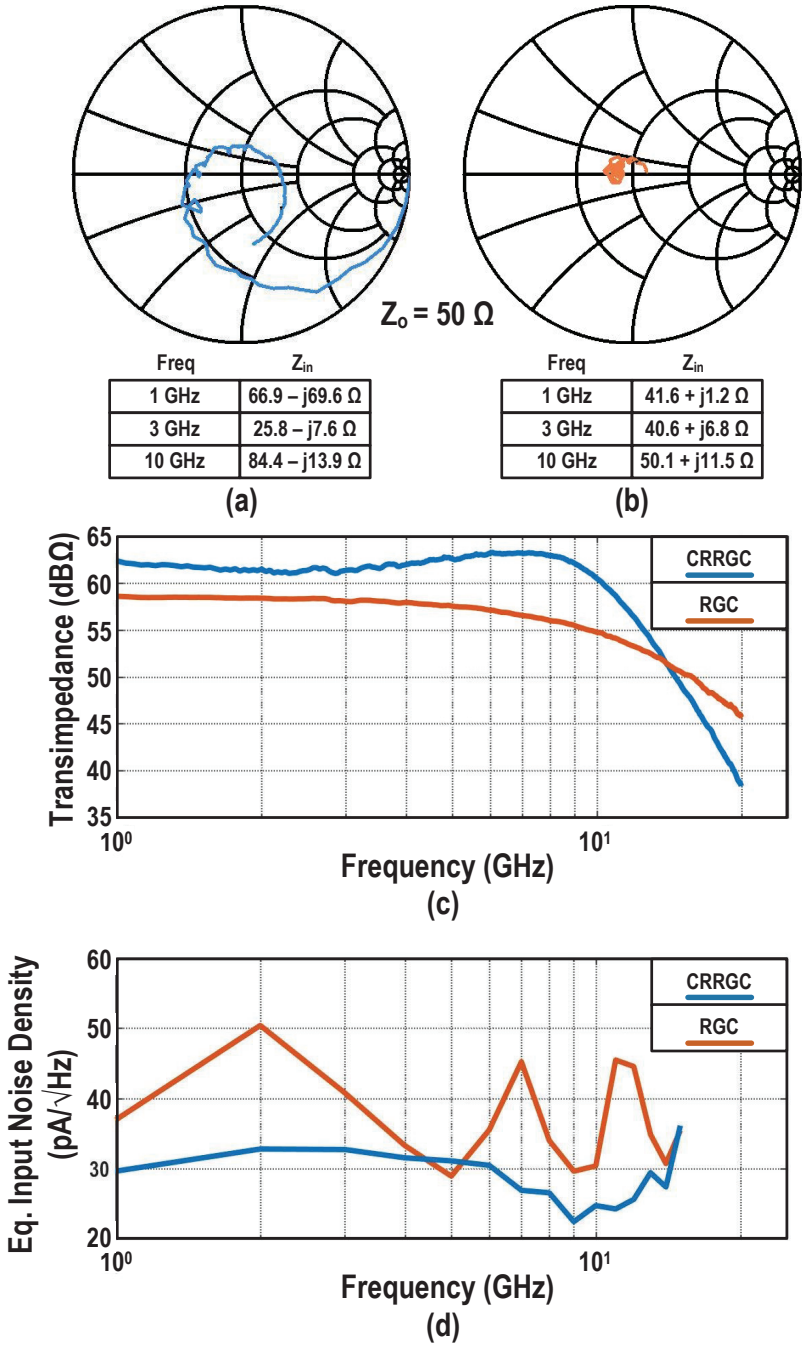

Figure 2.18: (a) Measured S_{11} plotted on a Smith chart from 10 MHz to 15 GHz along with select values of input impedance of the CRRGC TIA and (b) the RGC TIA. (c) Measured transimpedance gain of the CRRGC and RGC TIAs. (d) Measured equivalent input current noise densities of the TIAs.

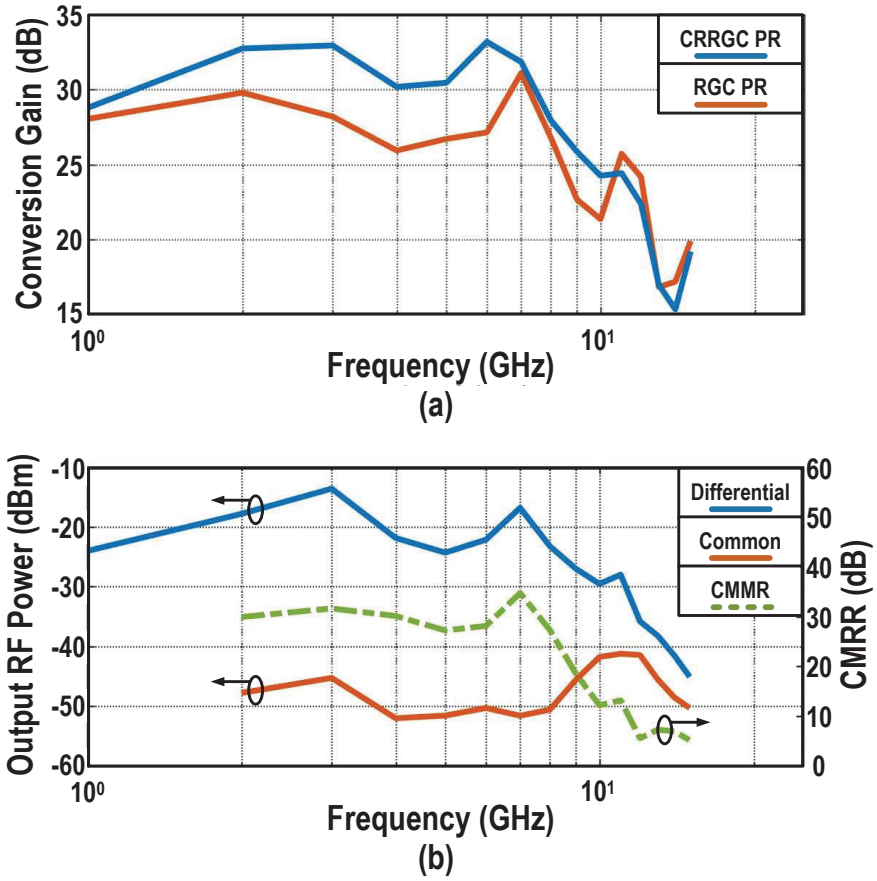

Figure 2.19: (a) The measured conversion gain of the two photoreceivers, defined as the output electrical voltage per input optical power. The conversion gain is shown in dB=10*log10(V/W). (b) The measurement results from the common mode rejection ratio (CMRR) setup. The CMRR is the difference between the differential and common mode curves.

input optical power. The measured photoreceiver conversion gains are plotted in Figure 2.19(a). From the plots, bandwidths of 8 GHz are achieved by both photoreceivers. The RGC-based photoreceiver (RGC PR) achieves a maximum conversion gain of 1289 V/W, while the CRRGC-based photoreceiver (CRRGC PR) achieves 2083 V/W. However, a ripple is observed. While neither the PDs nor TIAs exhibit significant ripple when measured on their own, the integration results in the undesired ripple. This is most likely due to several factors, one of which is mismatch between the

50 Ω transmission lines and the actual input impedance of the TIAs. Another cause is the addition of undesired inductance from the wirebonds, which are kept as short as possible to minimize this impact. This is also evident in the fact that the rippling occurs with a similar frequency response for both photoreceivers. The ripple in the conversion gain is non-ideal for data transmission applications. However in the targeted OFS applications, the signal of interest is a CW signal, and gain flatness is not necessary.

Next, the CMRR is observed. This is done by tuning the optical delay lines in each of the PDs optical paths to create differential and common mode illumination. When the illumination is differential, the balanced PDs undergo maximum current summation and the highest output RF power is achieved. When the illumination is common mode, the balanced PDs have minimum current summation and output the lowest RF power. Both the differential and common mode output RF powers are plotted in Figure 2.19(b). The difference between the two is the CMRR measured at that frequency, and a higher CMRR allows the balanced structure to reject more common mode noise. The CMRR is approximately 30 dB within the bandwidth. The common mode output at the lowest frequencies could not be measured due to the physical length limitations of the optical delay lines.

In order to determine the photoreceiver noise performance, the noise equivalent power (NEP) is calculated from measurements of the photoreceivers output noise power when the PDs are not illuminated. The NEP characterizes the noise performance by providing the minimum signal power needed to match the noise floor of the device. The NEP measured at various frequencies is plotted in Figure 2.20(a). Both photoreceivers achieve a similar minimum NEP of 13 pW/$\sqrt{Hz}$. However,

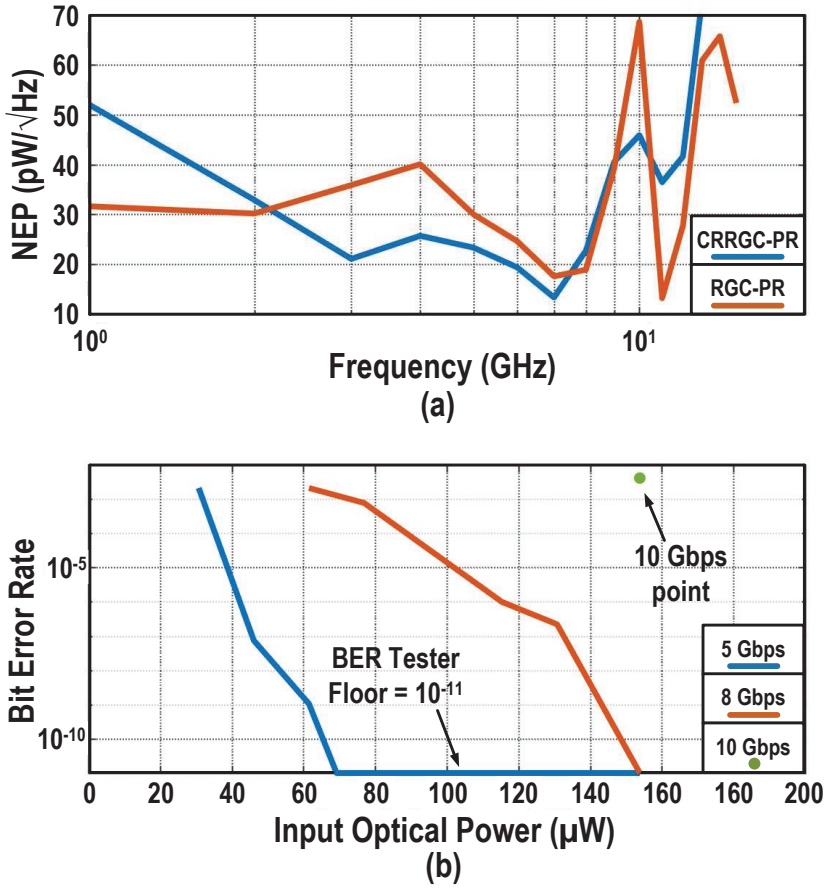

Figure 2.20: (a) Measured results of the photoreceiver noise equivalent power (NEP). The NEP specifies the minimum required input optical power for a signal to rise above the photoreceiver noise floor. (b) Measured bit error rate (BER) curves of the RGC PR for 5 Gbps, 8 Gbps, and 10 Gbps modulation against input optical power. The measurement floor of the BER tester is 10^{-11}.

the NEP of the CRRGC PR is lower than the RGC PR at most frequencies, except at the lowest. This is due to the limitation of the input ac-coupling capacitor that is present in the CRRGC TIA but not the RGC TIA. The ac-coupling capacitor limits the input impedance of the TIA at low frequencies, which can lower gain and increase the input referred NEP.

Lastly, bit-error-rate (BER) and eye diagram measurements were conducted on the photoreceivers. Using a PRBS7 generator to supply the modulation data, the optical input is modulated with an

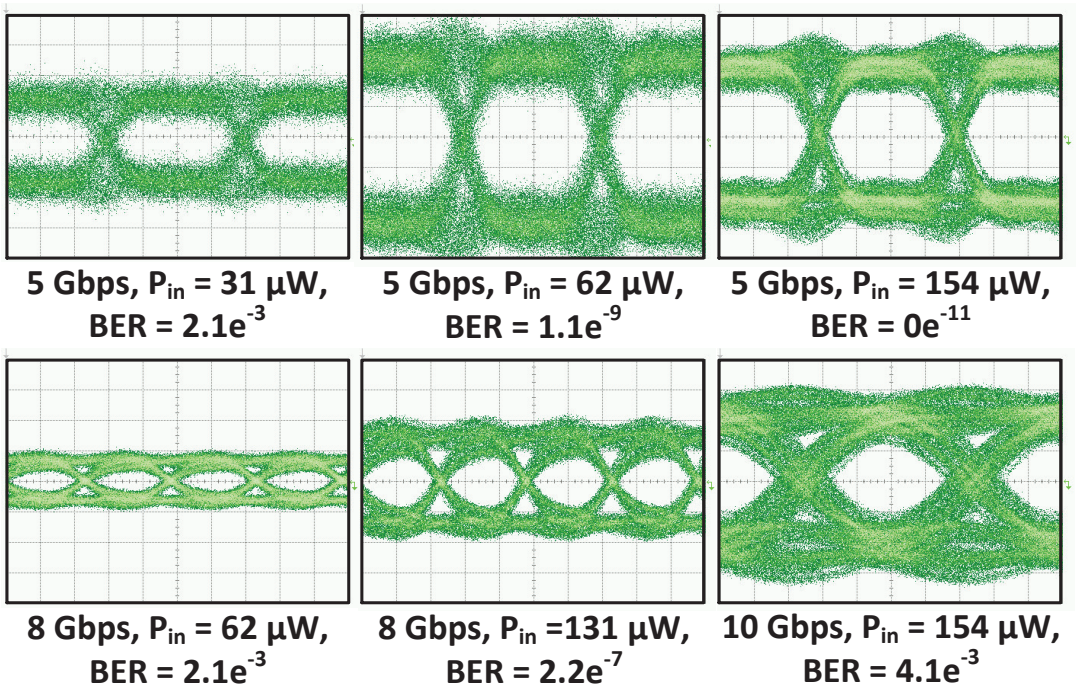

Figure 2.21: Eye diagrams measured from the RGC PR. Eyes are shown at various OOK modulation data rates and optical input powers. The bit error rate (BER) from each eye is also shown.

on-off keying scheme for the BER and eye measurements. The BER curves of the RGC PR are presented in Figure 2.20(b). The curves are measured at data rates of 5 Gbps, 8 Gbps, and 10 Gbps, versus input optical power. The measurement floor of the BER test setup is 10^{-11}, which the photoreceiver surpasses at 5 Gbps with 45 μA photocurrent, correlating to an optical input power of 69 μW, and at 8 Gbps with 100 μA photocurrent or 154 μW input optical power. Only one point is measured at 10 Gbps as any lower input optical power results in an unstable BER, and higher input powers are avoided to prevent damage to the devices. A set of eye diagrams at several data rates and input optical powers for the RGC PR are shown in Figure 2.21 with the eyes open clearly.

The CRRGC PR resulted in poor BER and eyes due to the negative impact of the input coupling capacitors present in the CRRGC TIA on the lowest frequencies, limiting the detection of longer

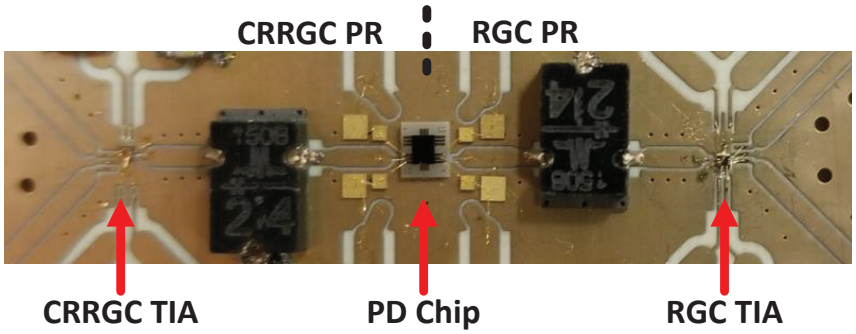

Figure 2.22: A photograph of the assembled photoreceivers. The two photoreceivers were assembled on either side of the PD chip, along with bypass capacitors on the supply lines, and bias-tee chips between the PDs and TIAs.

PRBS signals which are necessary for clear data transmission. However, in an OFS scheme where the signal of interest is a CW tone, clear data transmission is not a priority. A photograph of the photoreceivers is shown in Figure 2.22. Each photoreceiver occupies a 6 mm x 13 mm area.

Conclusions

Two balanced photoreceivers for OFS applications are presented in this paper. Both photoreceivers are based on similar InP balanced photodiode structures, but utilize two different CMOS TIA circuits. The RGC-based photoreceiver achieves a maximum conversion gain of 1289 V/W and a minimum NEP of 13 pW/$\sqrt{Hz}$, while the CRRGC-based photoreceiver achieves 2083 V/W and 13 pW/$\sqrt{Hz}$, respectively. The balanced photodiodes used provide high responsivities of 0.65 A/W and 30 dB of common mode rejection ratio. A comparison against state-of-the-art photoreceivers is presented in Table 2.3. While many photoreceivers utilize HEMT and GaAs TIAs, this work demonstrates high performance with inexpensive CMOS TIAs, allowing direct integration with following locking circuitry in chip-scale OFS systems.

Table 2.3: Comparison of Published Photoreceivers

Metric	**This Work** CRRGC	RGC	**[50]**	**[52]**
Bandwidth [GHz]	8*	8*	7 (26.5-33.5)	10 (49-59)
PD Resp. [A/W]	0.65	0.65	0.55	0.6
Conv. Gain [V/W]	2083	1289	1000	450
DC Power [mW]	68	66	N/A	1023
Area [mm^2]	78	78	400	N/A
Datarate [Gbps]	N/A	10	24	N/A
Bit Error Rate	N/A	$4e^{-3}$	$1e^{-3}$	N/A
PD Process	InP MUTC		InGaAs	InP
TIA Process	65 nm CMOS		N/A	HEMT GaAs

*Includes a 2-dB ripple in passband.

2.5 CRRGC TIA with Input DC Photocurrent-Compensation in 55 nm CMOS

Summary

A transimpedance amplifier (TIA) fabricated in a 55 nm low power CMOS process is presented. The TIA, a current-reuse regulated cascode (CRRGC) topology, includes an active balun and differential output drivers. To maximize integration in high-speed photoreceivers, the TIA also includes dc current compensation, removing the requirement for bias-tees between TIA and photodiode (PD). The TIA achieves a transimpedance gain of 69 dBΩ across a 3-dB bandwidth of 10.7 GHz. Additionally, the TIA demonstrates low-noise performance with an equivalent input noise density of 15 pA/$\sqrt{\mathrm{Hz}}$ in the passband. The dc compensation is capable of providing a fixed bias voltage for a PD while sourcing up to 2.4 mA or sinking up to 1 mA of photocurrent. The TIA, including active balun and dc current compensation, consumes 15.7 mW, while the output buffer consumes

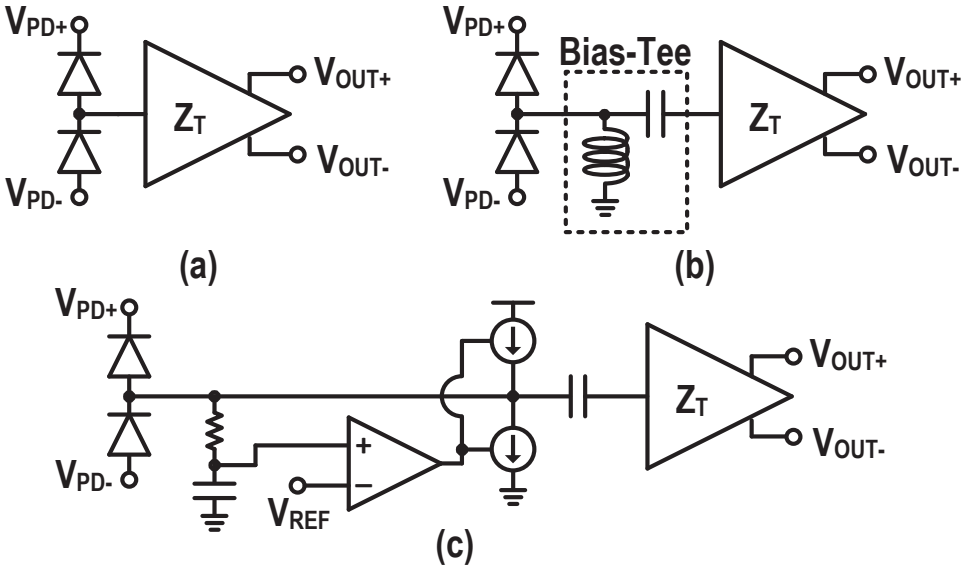

Figure 2.23: Photoreceiver integration schemes where the PD dc current is (a) directly injected into the TIA, (b) isolated from the TIA via a bias-tee, and (c) compensated via proposed feedback and separated from the RF path.

90.7 mW. The total active area of the circuit is 0.07 mm^2, and 0.21 mm^2 with pads.

This work presents the design, simulation, and measurement of a TIA with a new current compensation loop intended for use with balanced photodiodes (PDs) that removes the topology's previous need for a bias-tee during photoreceiver implementation, enabling tighter photoreceiver integration and cost-effectiveness for chip-scale solutions.

Design

When integrating a PD and TIA, several schemes are available, shown in Figure 2.23. In the simplest and smallest scheme, the PD and TIA are directly dc coupled as in Figure 2.23(a). However, in high-power applications, high dc current from the PDs can change the TIA biasing and operation. By inserting a bias-tee, the dc of the PD and TIA are isolated as in the second scheme shown

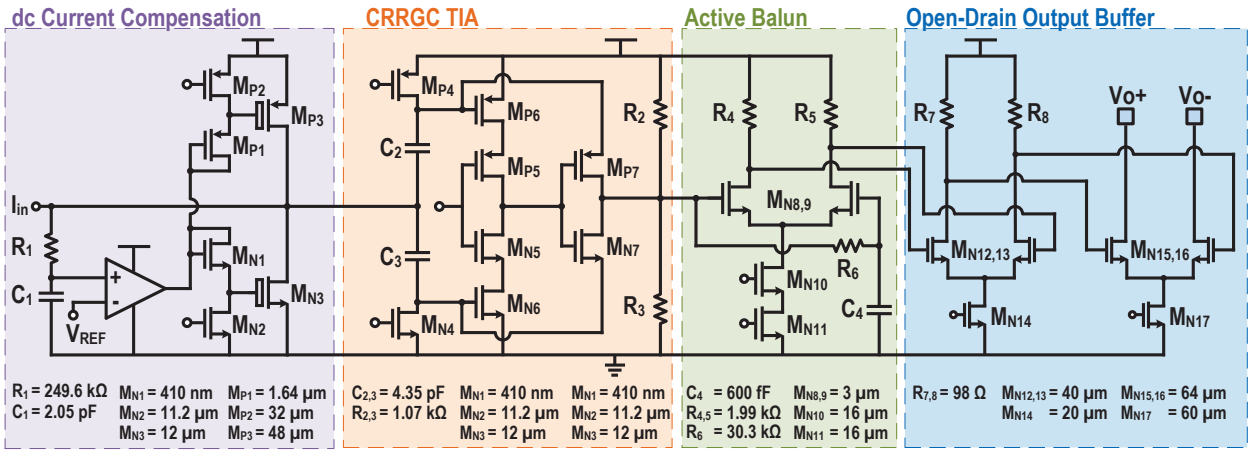

Figure 2.24: Full schematic of the implementation of the CRRGC TIA, including input dc current compensation, active balun and unity-gain open-drain output buffer. The biasing circuits and references for the current tails are omitted. All devices are minimum length unless specified.

in Figure 2.23(b). However, inductors are physically large, especially for lower RF frequencies. A third scheme, shown in Figure 2.23(c), is proposed. The dc and RF components are isolated with a current compensation feedback loop on-chip. The full circuit schematic is shown in Figure 2.24.

The first block in the signal chain is the dc current compensation. As the input current changes, the feedback loop should maintain a constant voltage close to a voltage reference (V_{REF}). This maintains the bias voltage across the PD versus changes in photocurrent that could arise due to illumination or device variation. This constant bias voltage results in uniform PD responsivity and capacitance. Dual-gate 2.5 V transistors are used in much of the compensation to support higher voltage handling for PD biasing. Additionally, the thicker gate oxide reduces the parasitic capacitance added to the input node, which would hinder the overall system bandwidth. The low-pass RC filter at the input of the compensation is designed with a cutoff frequency of approximately 300 kHz. These low frequency (dc) voltage changes are filtered and compensated by the compensation loop, while the high frequency RF signals are passed to the input of the TIA stage.

The schematic of the operational amplifier (op-amp) used in the current compensation loop is shown in Figure 2.25(a). For higher voltage handling, dual-gate 2.5 V devices are used. The inverting input is connected to V_{REF}, and the positive input is connected to the low pass filter. Diode-connected FETs are used at the output of the op-amp to create voltage drop/rise to the gates of the current source/sink devices, preventing a static dc current from flowing through M_{P3} and M_{N3}, thus reducing power consumption and shot noise generated directly at the input. In this configuration, when the voltage of the input changes, M_{P3} will source current or M_{N3} will sink current to compensate and return the node to V_{REF}. Because the TIA topology used has an ac-coupled input, the voltage sensing must occur before the ac-coupling capacitors C_2 and C_3. A dc-coupled TIA could sense at later stages if desired.

The dc current compensation contributes negligible amounts of noise at the input when dc input current is zero. However, the PD dc photocurrent flowing through M_{N3} or M_{P3} will directly contribute shot noise at the input node. The contributed current noise for a FET is directly proportional to dc drain current, shown in Eq. (2.11) from [59]:

$$\overline{i^2} = 2qI_D\Delta f \tag{2.11}$$

Therefore when small optical powers are received at the PD, the receiver must be most sensitive. With a small photocurrent, the noise contribution from the compensation loop is minimal because I_D is small. Inversely, the compensation loop contributes the most noise when optical input powers

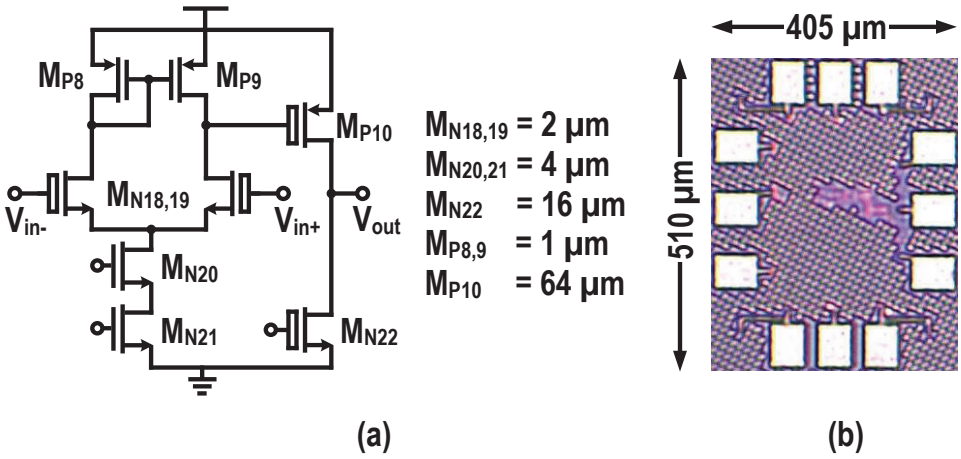

Figure 2.25: (a) Schematic of operational amplifier used in proposed dc compensation loop. (b) Microphotograph of the TIA on a 55 nm LP CMOS chip.

are high, which is when the photoreceiver noise is least critical. This allows the TIA to be suitable in a broader application space.

The next block is the current-reuse regulated cascode (CRRGC) TIA [54], based on the regulated cascode topology [42]. The circuit utilizes an ac-coupled input node, isolating its biasing from the PD and compensation circuitry. Because of its ac-coupled input, the CRRGC previously required a bias-tee between the PD and TIA. Bias-tees are physically large due to the size of the inductor needed to effectively isolate the lowest frequencies. With the addition of the compensation circuitry in this work, the previous need for the bias-tee is removed from the CRRGC, allowing tighter photoreceiver integration for chip-scale applications.

The topology offers a very low input impedance due to its use of negative feedback. The lower input impedance is necessary to maximize the bandwidth of the system by minimizing the RC time constant associated with the typically dominant PD capacitance. The lower input impedance is especially useful as it is now in parallel with the high-impedance dc compensation loop, allowing

the majority of the ac input current to flow to the TIA. Assuming negligible impact from the dc compensation loop, the TIA's transimpedance (Z_T) and input impedance (Z_{in}) can be estimated with Eq. (2.12) and Eq. (2.13), respectively:

$$Z_T \approx R_2||R_3||r_{on7}||r_{op7} \tag{2.12}$$

$$Z_{in} \approx \frac{1}{(g_{mn7}+g_{mp7})(1+(g_{mn6}+g_{mp6})(r_{on5}||r_{op5}))} \tag{2.13}$$

Lastly, the TIA includes an active balun and unity-gain open-drain output buffer to convert the signal from single-ended to differential and drive 50 Ω devices off-chip. A full chip microphotograph is shown in Figure 2.25(b).

Measurements

In order to measure the transimpedance, bandwidth, input impedance, and input current compensation, similar measurement setups from [54] are utilized. The dc connections to the chip are made via aluminum wirebonds, and the RF input and output connections are made with high-frequency GSG and SGS probes, respectively. In order to isolate the vector network analyzer (VNA) from the dc current injected to test the current compensation, the input is then connected to an external bias-tee. The differential outputs are also connected to external bias-tees for similar reasons.

The VNA used is a Keysight N5245A, and the dc sources are Keithley 2400 series source meters. To capture the TIA's single-ended to differential behavior, the VNA is operated in balanced mode, treating ports 2 and 3 as a single differential port during s-parameter measurements. The single-ended-to-differential transimpedance is calculated using Eq. (2.14) from [44]:

$$Z_T = Z_O \cdot \frac{S_{21}}{1 - S_{11}} \tag{2.14}$$

The TIA's simulated and measured S_{11} is shown in Figure 2.26(a). The simulated and measured input impedance agree very well, but a slight mismatch is seen. This mismatch is likely due to inaccuracies in the device models at the highest frequencies. This is also evident in Figure 2.26(b), where the resonant peaking is slightly different in simulation and measurement. The TIA achieves a transimpedance of 69 dBΩ across a 3-dB bandwidth of 10.7 GHz with 2 dB of peaking. The simulated group delay of the TIA is plotted in Figure 2.26(c). Additionally, a PD model of the PD presented in [60] is combined with the measured s-parameters of the TIA to simulate an expected optical conversion gain in Figure 2.26(d), with the photoreceiver model shown in its inset. The conversion gain is simulated with a PD responsivity of 0.64 A/W and the C_{PD} set to 0 fF as well as 200 fF for comparison. The loaded simulated conversion gain is over 1.2 kV/W with a slightly lower effective bandwidth of 9 GHz. The TIA core, including the active balun, consumes 14.5 mW from a 2.7 V supply, and the compensation loop consumes 1.2 mW from a 2 V supply, for a total of 15.7 mW dc power consumption.

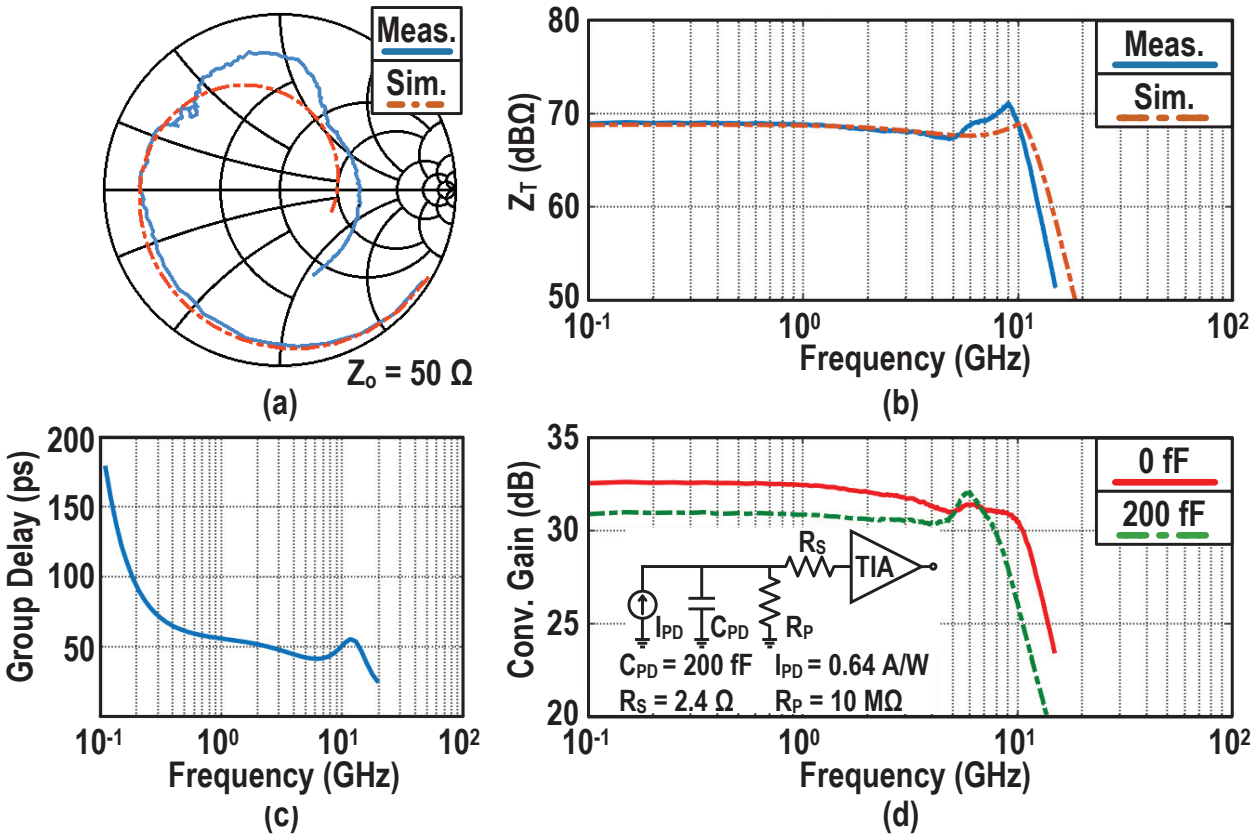

Figure 2.26: (a) Simulated and measured S_{11} of the TIA on a Smith chart up through 15 GHz. (b) Simulated and measured transimpedance gain across frequency. (c) Simulated group delay of the TIA. (d) Simulated optical conversion gain using a PD model with 0 fF and 200 fF C_{PD} and 0.64 A/W responsivity. Shown as dB = 10*log10(V/W). *Inset:* PD model from [60] used with TIA measurements to model optical conversion gain.

To measure the noise of the TIA, the input is left open circuited [45] and the output power of the TIA is measured. Then, the output noise power can be referred back to the input using the TIA's measured transimpedance gain. This shows the equivalent input noise current density. The TIA achieves approximately 15 pA/$\sqrt{\text{Hz}}$ equivalent input noise density measured in the passband, shown in Figure 2.27(a).

To test the current compensation, dc current is supplied to or accepted from the circuit input node using a source meter. A V_{REF} of 1.2 V is applied to the circuit. In Figure 2.27(b), the input node

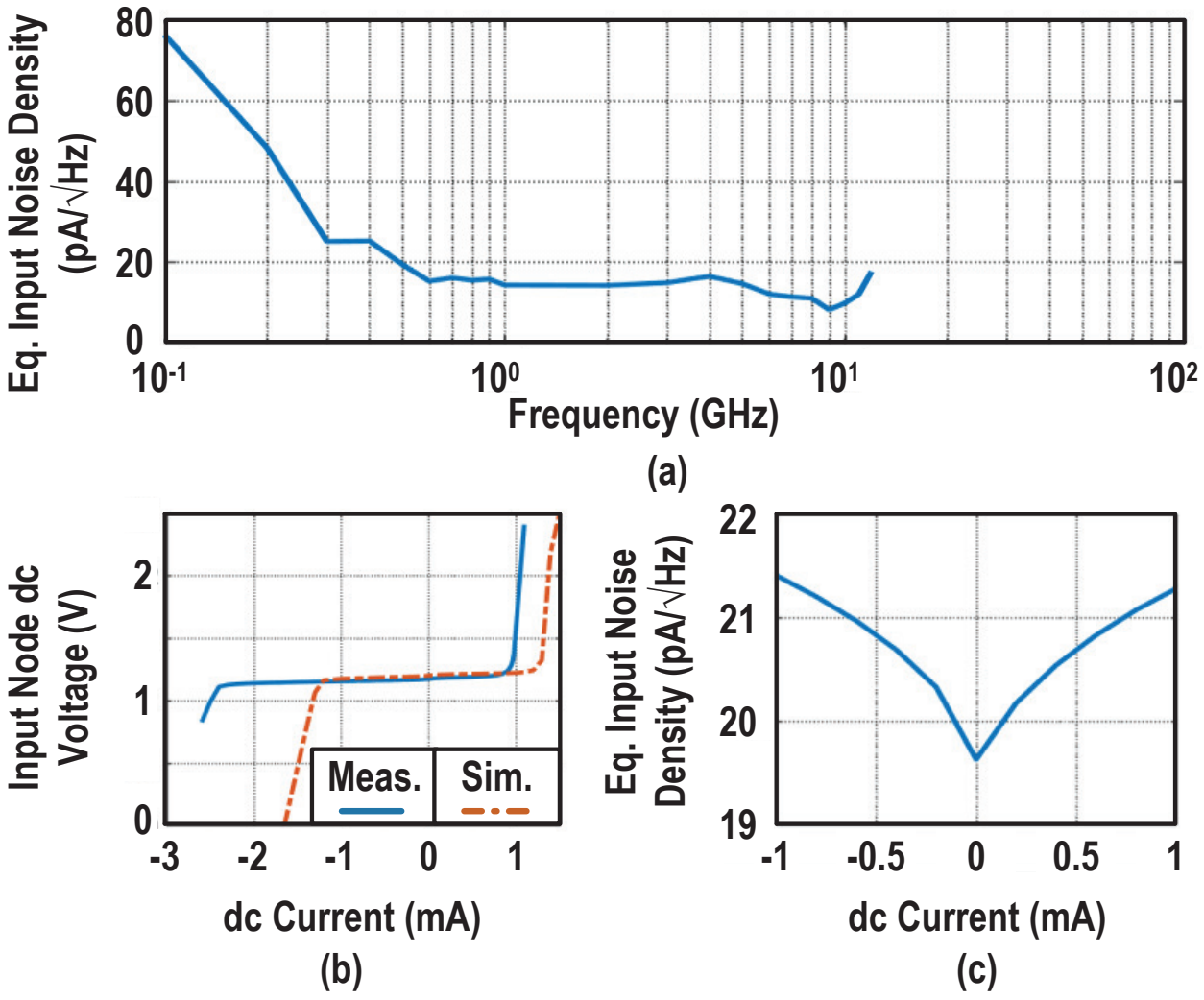

Figure 2.27: (a) Plot of the equivalent input noise of the TIA, measured when compensated dc current is zero. (b) Plot of the simulated and measured TIA input node voltage vs. compensated input dc current. The input node maintains a steady voltage from -2.4 mA to 0.9 mA of input current. (c) Simulated equivalent input noise density of TIA at 500 MHz vs. compensated dc current.

voltage is plotted against the input dc current. The current compensation is capable of keeping the input node's dc voltage fixed at 1.2 V when accepting between -2.4 mA and 0.9 mA of dc input current. Higher currents will saturate the feedback and cause the dc voltage to shift undesirably, causing a change in the bias-voltage of the PD and thus its responsivity and bandwidth. The

compensation is designed and simulated to maintain a steady input voltage while accepting -1.2 mA to 1.2 mA, but a more asymmetric response is seen in measurement, likely due to fabrication-related device variation in M_{P3} and M_{N3}. Additionally, noise simulations at 500 MHz against compensated input dc currents are shown in Figure 2.27(c). As discussed, compensation has little impact on noise.

Conclusion

A 55-nm LP CMOS transimpedance amplifier achieving 69 dBΩ and a bandwidth of 10.7 GHz is demonstrated. The TIA utilizes a current compensation loop at the input in order to remove the need for a bias-tee in high-power applications, enabling higher levels of integration in photoreceiver and photonic systems. When integrated with a PD, the TIA is able to supply up to 2.4 mA or accept up to 0.9 mA from the PD without altering its bias voltage. Table 2.4 presents a comparison of this work against other published TIAs.

Table 2.4: Comparison of CMOS Transimpedance Amplifiers

Metric	**This Work**	**[46]**	**[47]**	**[54]**
Bandwidth [GHz]	10.7	0.55	1.6/17	11
Transimpedance [dBΩ]	69	51-73	85/60	62
Eq. In. Noise [pA/$\sqrt{\text{Hz}}$]	15	3.4	N/A	30
DC Power [mW]	106	4.8	0.26*	66
Input Coupling	DC comp.	DC	DC	AC
Output Signal Type	Diff	Diff	Sing	Diff
Total Area [mm^2]	0.21	0.006†	N/A	0.25
CMOS Process	55nm LP	65nm	65nm	65nm

*Buffer power exempted †Active area only

2.6 Conclusions

Several TIAs were designed, simulated, and fabricated in various silicon CMOS processes. These TIAs were then integrated with UVA-designed photodiodes to create several generations of high-speed photoreceivers. The first generation involved a previously documented and established topology of TIA, called the regulated cascode (RGC), that was fabricated in a 130 nm process. The next generation saw two TIAs fabricated in a 65 nm process: an RGC TIA to act as a baseline, and a novel CRRGC TIA with a current-reuse methodology applied to the original RGC topology. Lastly, the third generation of high-speed TIA and photoreceiver was created by further augmenting the novel CRRGC TIA with dc-compensation circuitry. This final generation resulted in an improvement to the already novel CRRGC TIA, eliminating the topology's ac-coupled limitations. This meant that the TIA could be used in a much broader application space, both for high power and low noise use cases. It should be noted that this is the first design and implementation of this dc-compensated architecture.

2.7 Relevant Publications

First-Authored Publications

- R. Costanzo, Z. Yang, N. Raduazo, A. Beling and S. M. Bowers, "A 10 GHz bandwidth balanced photoreceiver with 41 V/W optical conversion gain," *2017 12th European Microwave Integrated Circuits Conference (EuMIC)*, Nuremberg, 2017, pp. 151-154.

- R. Costanzo and S. M. Bowers, "A current reuse regulated cascode CMOS transimpedance amplifier with 11-GHz bandwidth," in *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 9, pp. 816-818, Sept. 2018.

- R. Costanzo, Z. Yang, A. Beling and S. M. Bowers, "Wideband balanced photoreceivers with InP-based photodiodes and 65 nm CMOS TIAs for use in optical frequency synthesis systems," in *Journal of Lightwave Technology*, vol. 37, no. 23, pp. 5833-5839, 1 Dec., 2019.

- R. Costanzo and S. M. Bowers, "A 10-GHz bandwidth transimpedance amplifier with input dc photocurrent compensation loop," in *IEEE Microwave and Wireless Components Letters*, vol. 30, no. 7, pp. 673-676, July 2020.

Co-Authored Publications

- Z. Yang, R. Costanzo, N. Raduazo, J. Zang, S. M. Bowers, and A. Beling, "Low-noise balanced photoreceiver with 21 V/W optical conversion gain," *Advanced Photonics 2017 (IPR, NOMA, Sensors, Networks, SPPCom, PS)*, OSA Technical Digest (online) (Optical Society of America, 2017), paper IM3A.5.

- J. E. Bowers et al., "Chip-scale optical resonator enabled synthesizer (CORES)," *Government Microcircuit Applications and Critical Technology Conference (GOMACTech)*, Albuquerque, NM, 2019.

Chapter 3

Low-Noise Photoreceiver with BiCMOS Transimpedance Amplifier

3.1 Introduction

Photoreceivers play an important role in many of today's photonic systems, both for optical frequency synthesis (OFS) and high-speed communications. Within an OFS system, photoreceivers can be used to lock an optical source to a clean microwave reference [14, 19]. This allows the generation of a precise optical frequency that can be useful in a variety of applications, including optical metrology, terahertz spectroscopy, imaging, and light-detection and ranging (LiDAR) [29, 30]. By lowering the noise of the photoreceiver, lower power signals can be detected, further lowering the pump power required for the optical source. This results in several benefits, includ-

ing lowering total system power and overall heat generation. Additionally, photoreceivers with microwave frequency bandwidths can enable wider frequency tuning ranges for OFS systems. In the other direction, RF-photonic systems can utilize optical sources for the generation of RF and mm-Wave frequencies, useful in antenna remoting and radio-over-fiber (RoF) networks [5, 10, 31]. Moving towards tightly integrated photoreceivers can allow desirable reductions in size and power for these systems, with some even taking advantage of emerging photonic integrated circuit platforms [32, 33, 34, 61].

Chip-scale OFS systems can also utilize the lower size and power to enable cost-effective and efficient light sources necessary for RoF paradigms typically proposed for 5G networks. These RoF paradigms often extend the optical network to near-user access points and make use of more numerous and widespread power-efficient optical sources [23, 60]. By leveraging the advantages of optical communication and extending its reach within the network, next generation networks can achieve faster data transmissions.

Photoreceivers are often heterogeneously integrated, making use of a PD and TIA/receiver that are fabricated in different processes and are on different chips. This heterogeneous integration allows the PD and TIA performances to be individually maximized. PDs fabricated in III-V processes have significant advantages in terms of device performance, while silicon-based integrated circuits allow increased TIA/receiver complexity along with direct integration with subsequent processing digital circuitry [62, 63]. However, with the recent growth of silicon photonic processes integrating optical and electrical components, there has been growing interest in monolithic solutions as well, offering single-chip solutions capable of minimizing external parasitics [38, 39, 40].

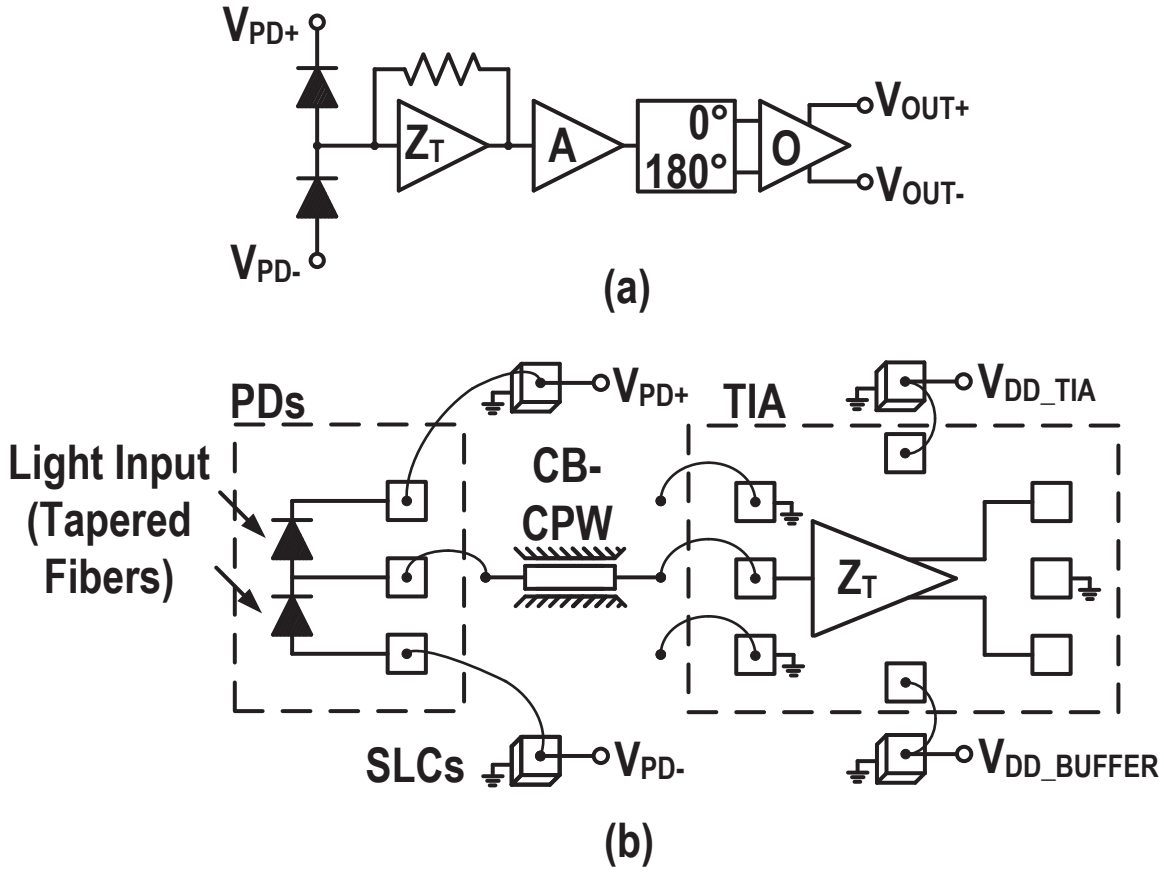

Figure 3.1: (a) A schematic for a photoreceiver consisting of balanced photodiodes directly dc-coupled to the TIA, showing the internal block-level design of the TIA. (b) A depiction of the physical scheme used to integrate the photodiodes and TIA. SLC capacitors are used in the supplies to create clean ac shorts for proper transmission line behavior. A conductor-backed coplanar waveguide (CBCPW) is used to connect the PDs and TIA. All connections from the chips to the integration board is made with aluminum wirebonds.

At the fundamental level, a photoreceiver is comprised of a photodetector, or photodiode (PD), and a transimpedance amplifier (TIA). Photodiodes fabricated in III-V materials such as indium phosphide (InP) are good candidates for high frequency applications like antenna remoting and RoF networks, owing to their high linearity, high bandwidths, and high power handling capabilities [10, 48, 49, 50, 51]. Additionally, these PDs achieve excellent performance in the form of higher responsivities and lower dark currents [28, 52, 53]. Compared to Ge-based PDs, III-V PDs

typically have increased absorption efficiency and lower noise, both critical metrics in establishing a low-power low-noise link. However, one drawback is that Ge-based PDs are more easily integrated onto a silicon process [32, 38, 39, 61].

As for the TIAs, many have been demonstrated in various processes. CMOS processes can offer cost-effective solutions that are readily integrated with subsequent digital circuits [54, 55, 56, 57, 64]. While slightly costlier, BiCMOS processes making use of silicon germanium (SiGe) can provide significantly increased device performances while maintaining ease of integration. Integration is at the forefront of much of today's ongoing research regarding OFS systems as the desire to move from bench-top to chip-scale implementations necessitates reductions in size, cost, and power [19, 29]. This paper presents a low noise photoreceiver with balanced InP-on-silicon PDs and a TIA fabricated on a 130 nm SiGe BiCMOS chip for heterogeneously-integrated OFS systems [65].

3.2 Photoreceiver with Common-Emitter-Based TIA in 130 nm BiCMOS

Summary

A photoreceiver consisting of indium phosphide (InP) balanced photodiodes (PD) on Si_3N_4 waveguides and a transimpedance amplifier (TIA) fabricated in a silicon germanium (SiGe) BiCMOS process is demonstrated. The InP PDs, heterogeneously integrated on a silicon substrate, achieve

external (internal) responsivities of 0.75 (0.9) A/W, bandwidths of 4 GHz, and common mode rejection ratios (CMRR) of greater than 40 dB when illuminated differentially. The TIA achieves 74 dBΩ of transimpedance gain with a 1 dB peak, a bandwidth of 3 GHz, and a low equivalent input noise current density of 7.2 pA/$\sqrt{\text{Hz}}$ when loaded with a C_{PD} of 380 fF. The full photoreceiver achieves high conversion gain of more than 2 kV/W up through 2 GHz, and a low in-band NEP of 8 pW/$\sqrt{\text{Hz}}$. The photoreceiver optical CMRR is measured to be 36 dB.

Design and Fabrication

A photoreceiver consisting of indium phosphide (InP) balanced photodiodes (PD) on Si_3N_4 waveguides and a transimpedance amplifier (TIA) fabricated in a silicon germanium (SiGe) BiCMOS process is demonstrated. The InP PDs, heterogeneously integrated on a silicon substrate, achieve external (internal) responsivities of 0.75 (0.9) A/W, bandwidths of 4 GHz, and common mode rejection ratios (CMRR) of greater than 40 dB when illuminated differentially. The TIA achieves 74 dBΩ of transimpedance gain with a 1 dB peak, a bandwidth of 3 GHz, and a low equivalent input noise current density of 7.2 pA/$\sqrt{\text{Hz}}$ when loaded with a C_{PD} of 380 fF. The full photoreceiver achieves high conversion gain of more than 2 kV/W up through 2 GHz, and a low in-band NEP of 8 pW/$\sqrt{\text{Hz}}$. The photoreceiver optical CMRR is measured to be 36 dB.

The photoreceiver topology with a detailed block-level breakdown is shown in Figure 3.1(a). The first component in the signal chain is the PD, which converts the input optical signal into an RF current signal. The current signal is input into the TIA, which amplifies the signal into an output RF voltage signal. In order to maximize integration and minimize loss, no bias-tee is utilized between the PDs and TIA. The direct dc-coupling allows maximum integration at the cost of some

robustness. The full physical implementation scheme is shown in 3.1(b), and discussed further in this section.

The PDs used in this work are integrated into a balanced structure. The balanced PDs should be illuminated with the same RF beat frequency, but with a 180° RF phase difference. This phase difference can be introduced via additional optical delay lines or discrete electro-optic phase shifters in the PD illumination paths. When illuminated differentially, the photocurrents from each of the PDs will constructively combine into an RF output. Conversely, when a common mode signal such as laser noise or interference is illuminated onto the PDs, the PDs should both see the same photocurrent, effectively canceling it out and preventing the signal from being output to the TIA. This common mode rejection is one benefit of the balanced configuration, along with minimizing the amount of dc current directly input into the TIA [60].

Mismatch in the two balanced devices can cause several issues. One is that the common-mode photocurrent cancellation will be affected negatively, resulting in more of the dc photocurrent flowing into the TIA input, possibly changing its biasing points and altering the performance of the photoreceiver. This mismatch can be corrected by tuning the reverse-bias voltages applied to each PD, compensating the mismatched responsivities and bandwidths.

The PDs are based on previously demonstrated indium phosphide-based InP/InGaAs photodiodes on silicon nitride (Si_3N_4) waveguides [66, 67]. The epitaxial stack and the doping concentrations for the modified uni-travelling carrier (MUTC) PDs are shown in Figure 3.2(a). The InP/InGaAs heterostructure in this work achieves high crystal quality due to good lattice matching. When compared to Ge-based PDs, the InGaAs material provides significantly higher absorption coefficients

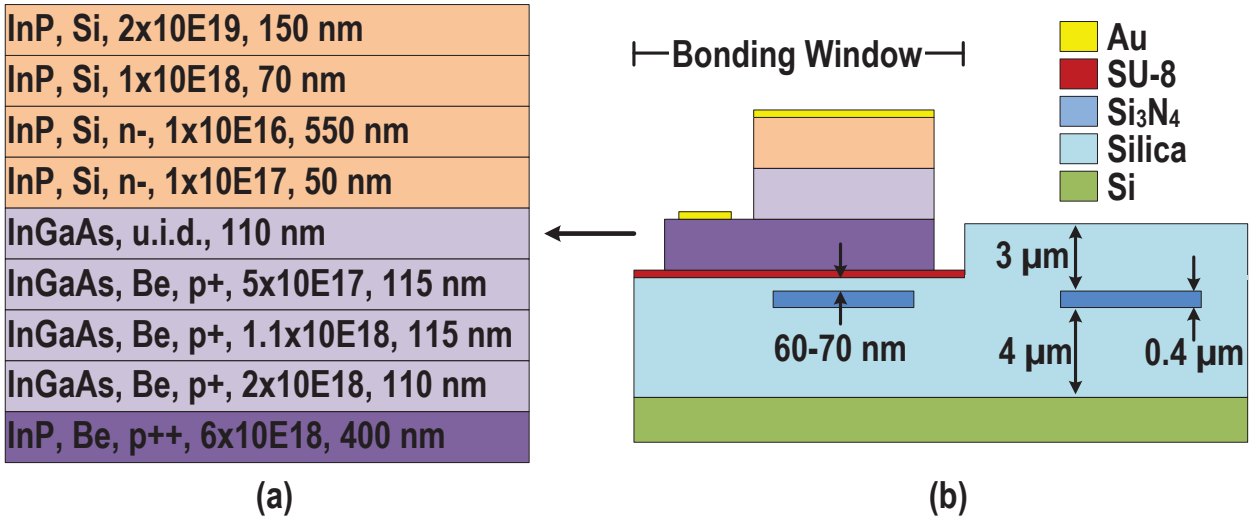

Figure 3.2: (a) Depiction of the PD epitaxial structure along with doping concentrations and (b) the cross-section of the overall chip structure with the PD bonded to the silicon chip.

at wavelengths of 1550 nm and beyond. Also, the bonding process used enables tight integration of high-performance III-V photodiodes and silicon chips, alleviating the disadvantage of III-V integration difficulties. The PDs are heterogeneously integrated via low-temperature bonding to the Si_3N_4 waveguides on a silicon substrate. The optical signals are contained in waveguides with core thicknesses of 400 nm, with upper and lower silica claddings of 3 μm and 4 μm, respectively. Within the bonding windows for PD attach, the top cladding is selectively etched thin to 60-70 nm, allowing efficient evanescent coupling from the waveguide to the PD absorber. The cross-section of the bonded InP-on-Si PDs is shown in Figure 3.2(b).

The TIA is designed and fabricated in a 130 nm silicon germanium (SiGe) BiCMOS process. A SiGe BiCMOS process offers several advantages over silicon CMOS, including access to heterojunction bipolar transistors (HBT). Compared to the metal-oxide-semiconductor field-effect transistor (MOSFET) devices in CMOS processes of similar nodes, HBT transistors provide several

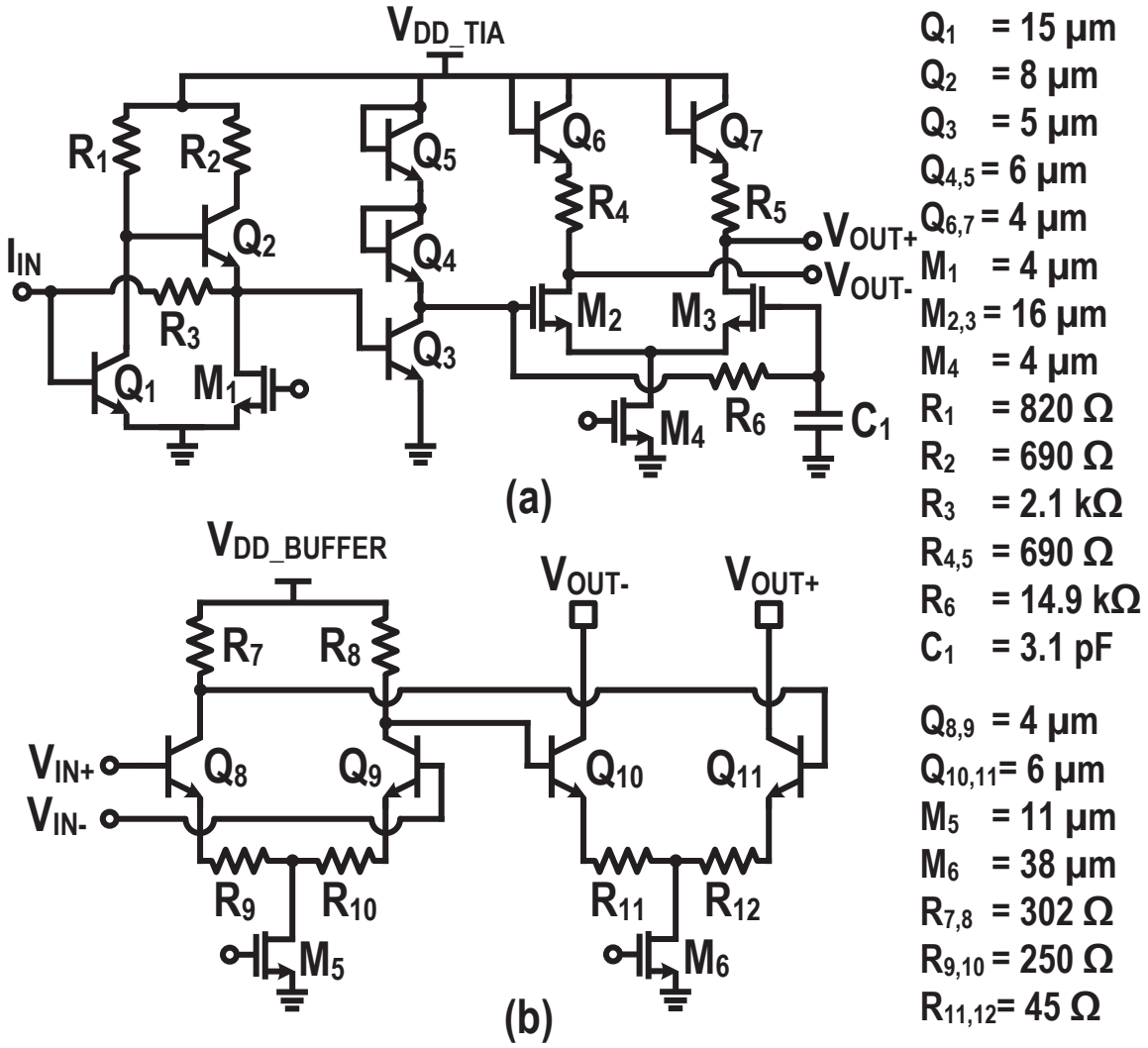

Figure 3.3: (a) Schematic of the TIA, voltage amplifier, and active balun. (b) Schematic of the pre-driver and open-collector stages that comprise the output buffer. Component values are listed, but only widths are shown for the active devices as all are minimum length. Additional on-chip dc biasing circuitry and supply bypass capacitors are omitted.

device-level benefits in the way of higher f_T, higher gain, higher breakdown voltages, and lower input impedances [59]. In this process, the HBT devices reportedly achieve nominal f_T values of 210 GHz. The disadvantages of the SiGe HBT devices include increased power consumption due to base currents and higher static leakage currents, as well as overall process cost.

The schematic of the TIA utilized in this work is shown in Figure 3.3. The TIA chip consists of four stages: the input transimpedance stage, an additional voltage gain and level shifting stage, an active balun, and a differential output driver. The transimpedance stage is a common-emitter amplifier that utilizes a negative feedback resistor. The negative feedback trades some of the gain for a lower input impedance. Lower TIA input impedances are desirable as the RC-time constant from the PD capacitance and the TIA input impedance typically limits the bandwidth of a photoreceiver.

The noise at the base of the HBT device is significantly less than at the collector. Therefore, this topology utilizing a common-emitter device at the input can help reduce total input-referred noise when compared to other topologies with inputs at the collector, such as the regulated gate cascode (or regulated base cascode for HBT devices) [42, 60]. To understand this better, consider the sources of noise in the bipolar transistor. The dominant noise sources include shot noise at the collector, as well as shot noise and flicker noise at the base. These can be expressed in Eq. (3.1) and Eq. (3.2) from [59]:

$$\overline{i_c^2} = 2qI_C\Delta f \tag{3.1}$$

$$\overline{i_b^2} = 2qI_B\Delta f + K_1\frac{I_B^a}{f}\Delta f \tag{3.2}$$

where $\overline{i_c^2}$ is the current noise at the collector, $\overline{i_b^2}$ is the current noise at the base of the transistor, and K_1 and a are device constants. Flicker noise ($K_1 \frac{I_B^a}{f} \Delta f$) is dominant at low frequencies. However, as the lowest frequency of interest in the target application space is 100 MHz, well above where flicker noise is dominant, the flicker noise becomes negligible. This means the dominant noise sources are the shot noise at the collector ($2qI_C\Delta f$), and at the base ($2qI_B\Delta f$). By nature of the transistor, I_C is much higher than I_B, so the current noise of the collector is dominant. Therefore, to minimize the TIA input-referred noise, the RF input should be to the base rather than to the collector.

The following stage is a voltage amplifier, which further increases the overall transimpedance gain of the TIA. While the amplifier provides additional voltage gain, the primary purpose of the amplifier is to allow proper biasing of the subsequent active balun stage. The dc voltage at the output of the TIA stage is too low to provide adequate voltage overhead for the active-balun. While possible to instead use PNP devices to solve the overhead issue, the PNP devices available in this process are primarily for ESD structures and are much slower than the NPN devices, with f_T of 17 GHz. The additional voltage amplifier utilizing an NPN device remedies this issue.

The active balun following the voltage amplifier is comprised of CMOS devices instead of HBT devices. This is due to several reasons. The primary reason is that in order to create a well-balanced balun, the dc biasing of both of the active devices (M_2 and M_3) should be as symmetric as possible. In this topology, an RC filter (R_6 and C_1) is placed between both the positive and negative inputs to a differential amplifier. If the input devices are CMOS FETs, then the input impedances to the gates of M_2 and M_3 are very high. FET gate currents are negligible, resulting

in identical dc voltages at each gate because little current flows across R_6. If the input devices are HBT devices, then the base currents complicate this dc matching. The base current of the right device (where M_3 is in this work) would create a voltage drop across R_6 of the RC filter, and cause a mismatch in base voltages. To solve this issue, the balun instead utilizes CMOS devices, which are still capable of achieving sufficient frequency responses for this circuit. Using FET gates at the input, which have orders of magnitude higher impedance than HBT bases, additionally hardens the circuit against mismatch. Regardless of the mismatch that can be reasonably expected from the fabrication process, the input impedance into the gate of M_3 is on the order of gigaohms, resulting in a negligible current across R_6 and thus matched voltages on both gates of M_2 and M_3.

The balun is much later in the signal chain and follows sufficient amplification, making the noise impact minimal when referred to the input of the TIA. This pattern is seen in the Friis equation [68] shown below in Eq. (3.3):

$$F_{SYS} = F_1 + \frac{(F_2 - 1)}{A_1} + \frac{(F_3 - 1)}{A_1 A_2} + \frac{(F_4 - 1)}{A_1 A_2 A_3} ... \tag{3.3}$$

where the noise factor of a system (F_{SYS}) can be related to the individual noise factors (F_1, F_2 ...) of each block, with block 1 being the first block in the cascade, and so on. The noise contribution of the later blocks in the cascade are divided by the gains (A_1, A_2 ...) of the preceding stages. Therefore, the balun noise performance is of lesser consequence due to the fact that it follows the TIA and voltage amplification stages.

The last block of the TIA chip, shown in Figure 3.3(b), is the unity gain differential output buffer, consisting of a pre-driver stage and an open-collector output stage. This output buffer is necessary in order to drive 50 Ω impedances off-chip, such as measurement equipment. If the TIA were directly integrated with subsequent electronics on-chip, the output driver would not be necessary. The open-collector is utilized because it provides sufficient bandwidth with unity gain and high output impedance. This high impedance makes the output difficult to match to the 50 Ω transmission line and 50 Ω system. However, as long as the characteristic impedance of the transmission lines match with the load impedance, there will be no reflections at the output interface. It is possible to terminate the output of the buffer with on-chip resistors, which would reduce reflections due to mismatches introduced by load and package parasitics, but these issues are negligible up through several gigahertz [37]. Like the balun, the requirements for the noise performance of the output buffer is considerably more relaxed at the end of the system.

The photoreceiver components are integrated on a Rogers 4350B board. This integration scheme is shown in Figure 3.1(b). This material offers several benefits, the most important of which is lower dielectric loss compared to traditional FR-4. This is desirable as the RF signal is bonded down to a trace. The photodiodes are waveguide edge-illuminated on one side of the board. The PD RF output is wirebonded down to a trace and then bonded to the input of the TIA. While possible to directly bond the PDs to the TIA, the two chips are instead bonded to an intermediate trace due to device scarcity. This helps to mitigate the risk of needing to replace both chips in the case where one is damaged from an external event. If the two chips are directly bonded, it would become difficult to replace just one of them as removing wirebonds could damage or contaminate the pads

with residue. The trace is kept as short as possible, while still allowing the wirebonding wedge to physically fit in between the two chips. Further, as the PDs are bonded to a silicon substrate, it may be possible to bond the III-V PDs directly on the silicon electronics chip using this bonding procedure in future work.

As previously mentioned, the PDs and TIA are directly dc-coupled. This means that there is no dc voltage or current isolation between the PDs and TIA provided by an ac-coupling capacitor, a bias-tee such as in [60], or an intermediate compensation circuit such as in [64]. There are several considerations to be cognizant of when dc-coupling the two components. The most important one is that the TIA input is now the sole return path for the PD dc photocurrent. The entirety of the dc photocurrent will now be input directly into the TIA, which can cause the TIA biasing to change significantly, altering its gain, frequency response, and noise characteristics. However, the targeted application space for this photoreceiver involves very low input optical powers. For input optical powers on the order of tens of microwatts, the dc photocurrent from the PDs will be small enough to avoid significant changes to the TIA biasing, and has been taken into account during TIA design. Further, during balanced illumination, the dc photocurrent through both PDs would be similar. When this is the case, only the mismatch in the photocurrents will be input into the TIA.

In addition, the nominal dc voltage at the input of the TIA should be accounted for in the balanced PD biasing. When a bias-tee is used such as in [60], the center pin of the balanced PDs is ground, so a symmetric voltage can be applied. With no bias-tee, the biasing of the PD should be applied such that the center pin voltage is approximately that of the nominal dc voltage at the TIA input

node. In this work, a V_{PD+} of 4.8 V and a V_{PD-} of -3.2 V is applied, resulting in a center pin voltage of 0.8 V, which is the nominal dc voltage of the TIA input node.

Measurement Setup

For optimal balanced performance, both photodiodes in the balanced structure should have similar responsivities and bandwidths. To verify this and select which devices to use from a fabrication run, the photodiodes are independently illuminated and probed. The PD is illuminated with an RF beat frequency created by heterodyning two 1550 nm lasers. The RF beat frequency is the difference between the optical frequencies of the two lasers, whose outputs are combined in a 2x2 coupler. This heterodyne setup allows the RF frequency to be swept while the output RF power of the PD is measured on an RF power meter or electrical spectrum analyzer. Additionally, this measurement can be conducted with various bias voltages applied to the PDs. Higher reverse biasing results in a lower effective photodiode capacitance, which can allow for higher bandwidths. The MUTC PDs are able to relax transit time limitations by using uni-travelling carriers. Compared to PIN PDs with identical capacitances, the MUTC PDs achieve higher bandwidths by utilizing fast electrons as carriers, and not the slower holes. However, the bandwidth is currently limited by the resistance-capacitance component [67]. Therefore, it is important to apply a high enough reverse-bias voltage to reduce the capacitance enough to lower the typically dominant RC time constant created at the PD-TIA interface. For this work, a reverse bias voltage of 4 V is applied to each PD. Based on previous C-V measurements of individual PDs, the estimated C_{PD} for the balanced structure at these applied voltages is 380 fF.

The standalone performance of the TIA is measured by first wirebonding all the supply pads to

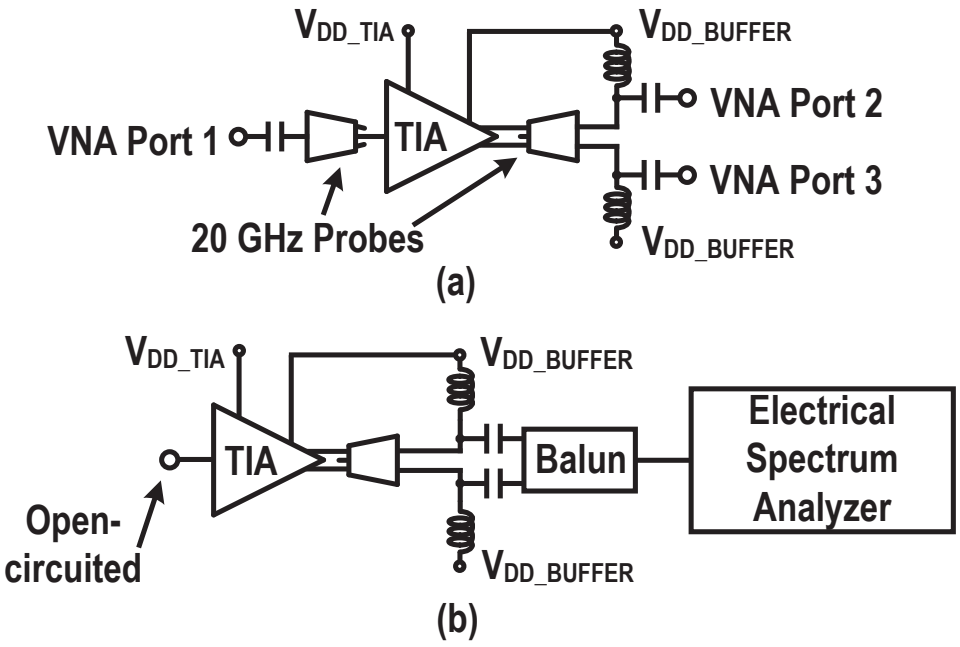

Figure 3.4: (a) Measurement setup used when measuring the single-ended to differential transimpedance gain of the TIA. A 4-port VNA is used, and ports 2 and 3 are operated in balanced mode, allowing capture of differential s-parameters. (b) Measurement setup used when measuring the noise performance of the TIA. The input is open-circuited, and output power is measured with off-chip bias-tees, balun, and low-noise electrical spectrum analyzer. Off-chip component losses are calibrated out of the measurements.

a chip carrier on a separate FR4 breakout board. Additionally, bondable bypass capacitors to ground are epoxied immediately next to the chip. By including these bypass capacitors in the dc supply lines, clean RF grounds are created as close as possible to the chip, reducing the likelihood of undesired oscillations. Then, the RF input and output are probed via GSG and SGS probes, respectively. Because of the open-collector output buffer, bias-tees are used in the setup to provide the bias voltage through the output probe. To measure the gain and bandwidth, a 4-port vector network analyzer (VNA) is utilized, as shown in Figure 3.4(a). The measured s-parameters can be converted to transimpedance gain (and from that, bandwidth) from Eq. (3.4) from [44]:

$$Z_T = Z_O \cdot \frac{S_{21}}{1 - S_{11}} \tag{3.4}$$

where Z_T is the transimpedance gain and Z_O is the characteristic impedance. Then, the TIA noise performance is measured by open-circuiting the input node, while the output power is monitored on a low-noise electrical spectrum analyzer across frequency [54]. The measurement setup for noise is depicted in Figure 3.4(b).

Some important photoreceiver metrics that can significantly impact link performance include bandwidth, conversion gain, and noise. The bandwidth and conversion gain are measured via the setup shown in Figure 3.5(a). The PDs are reverse-biased with 4 V across each. This means a V_{PD+} of 4.8 V and a V_{PD-} of -3.2 V. This asymmetry is to accommodate the nominal dc voltage of the TIA input node around 0.8 V, as discussed previously. The lasers, combined to produce a heterodyne beat frequency, are then illuminated onto one of the PDs. The optical sources used for the heterodyne setup are left free-running. No locking mechanism was used due to availability, but the beat frequency was constantly monitored on the commercial PD and electrical spectrum analyzer. To align the fiber, a 6-axis micropositioner is used to position a tapered fiber at the input edge-coupled waveguide of the PD chip. By monitoring the photocurrent through the PD using a dc source meter, the input optical power can be maintained at a constant value. The output RF power of the TIA is then measured using a differential SGS probe, an RF balun, and an electrical spectrum analyzer. The beat frequency generated in the heterodyne setup is tuned across frequencies via thermally

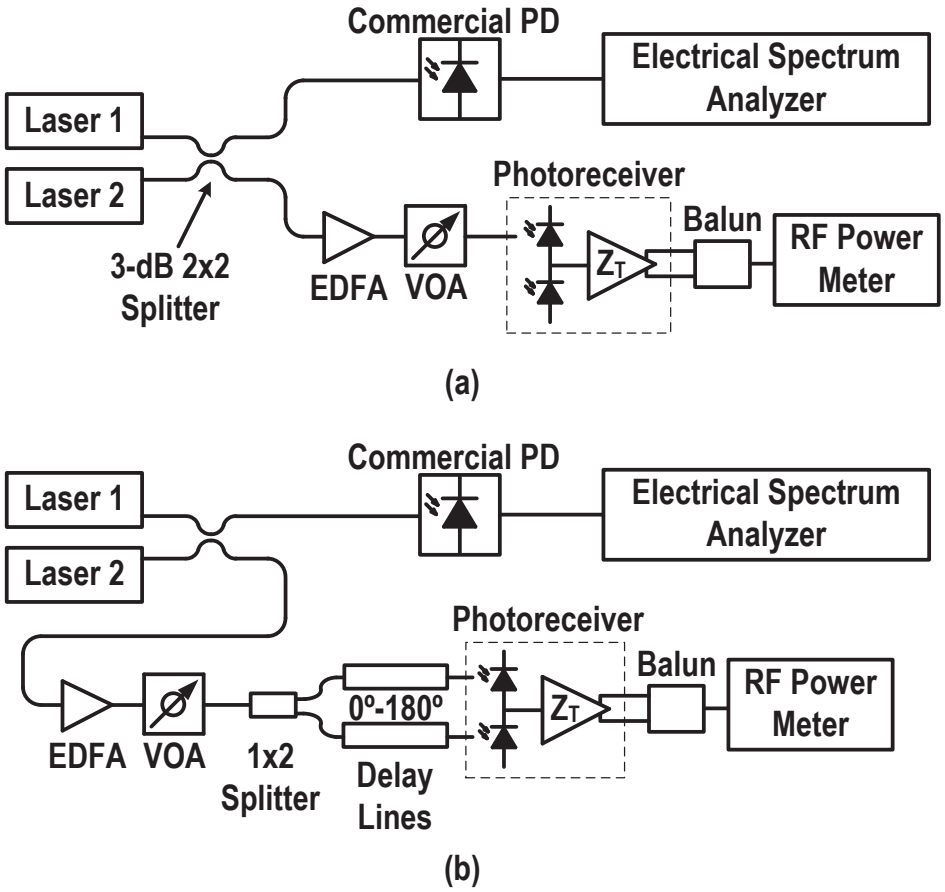

Figure 3.5: (a) Measurement setup used to measure the photoreceiver optical-to-electrical conversion gain and bandwidth. This setup can also be used to measure the noise performance when the optical sources are switched off, leaving the PDs dark. The laser outputs are combined with a 2x2 splitter to create a beat frequency. Some of the power is monitored on a commercial PD and electrical spectrum analyzer to monitor beat frequency. The rest of the power is input to an erbium doped fiber amplifier (EDFA) and variable optical attenuator (VOA) for precise control of optical power. (b) Measurement setup used to measure the photoreceiver common-mode rejection ratio. Delay lines are used to create common-mode or differential illumination, changing the output RF power.

tuning the lasers, and input through an erbium-doped fiber amplifier (EDFA) and variable optical attenuator (VOA) to accurately control the optical power delivered to the photoreceiver. The optical input power is kept constant while sweeping the RF frequency, allowing the 3-dB bandwidth and optical conversion gain to be extracted from the measured output powers of the photoreceiver.

With some modification of the previous design setup to the one shown in Figure 3.5(b), the common mode rejection ratio (CMRR) of the photoreceiver can be evaluated. The TIA itself does not affect the CMRR with respect to the optical input signal, so the photoreceiver should have a similar CMRR to that of the balanced PDs. Instead of illuminating one PD, the optical beat signal is split into two paths, with mechanically-tuned optical delay lines introduced in each. By adjusting the optical delays, the RF delay between the two paths can be changed, allowing the balanced PDs to be illuminated in common-mode or differentially. When there is a full 180° phase shift between the two paths, the PDs are illuminated differentially and will output the maximum RF power to the TIA. When both paths have a 0° phase difference, the PDs cancel their photocurrents and output a minimum RF power to the TIA. The difference between the maximum and minimum output power at a fixed frequency is the CMRR. Additionally, the single tapered fiber is replaced with a tapered fiber array with 127 μm pitch to allow independent simultaneous illumination of both PDs.

To measure the noise of the photoreceiver, all optical illumination is removed. The output electrical power of the photoreceiver is measured while the PDs are biased on but not illuminated. Using the measured output noise of the photoreceiver and the previously measured optical conversion gain, the noise can be referred to the input. This is known as the photoreceiver input noise equivalent power (NEP).

Lastly, to capture eye diagrams and measure bit error rates (BER), the heterodyne setup is replaced with a single laser and an optical modulator. The optical modulator is driven by a pattern generator creating a PRBS7 sequence of bits at various specified bit rates. This modulated optical signal is illuminated onto the photoreceiver. Because the photoreceiver output is differential, the positive

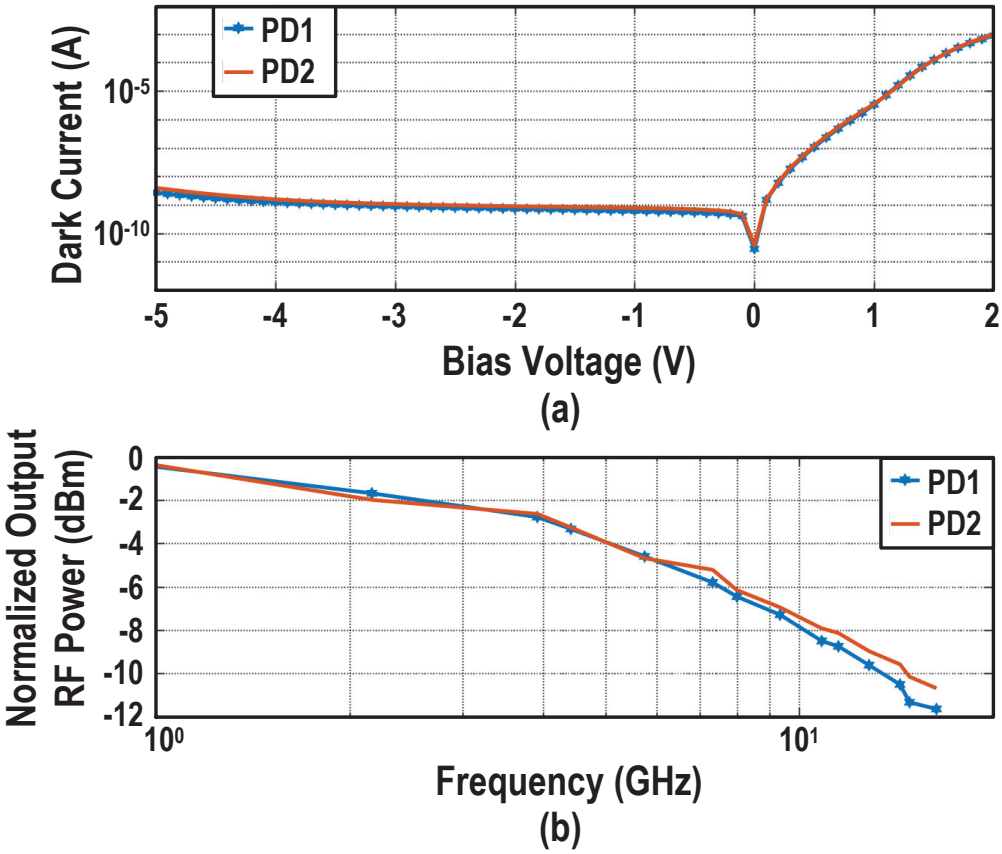

Figure 3.6: (a) Measured dark current versus bias voltage for each of the PDs in the balanced structure. (b) Measured normalized output RF power versus frequency for a fixed optical input power to each PD.

output is given to the BER tester, and the negative output is given to the sampling oscilloscope for eye diagrams. This allows both the eyes and BER to be captured simultaneously, at the cost of 3 dB of signal power in either measurement. The differential outputs of the TIA were verified to be very close to one another in signal power during prior standalone testing.

Experimental Results

The photodiodes used in the photoreceiver presented in this work are from the same process as the photodiodes presented in prior work [66, 67]. A 4 V reverse bias is applied across each of

the PDs to provide sufficient PD performance for the desired bandwidth. The measured results for the photodiodes are shown in Figure 3.6. The independent IV curves of both of the photodiodes are plotted in Figure 3.6(a). The dark current remains on the order of nanoamps out to -4 V of bias. The RF response of the PD is tested by measuring the output RF power across frequency for a fixed input optical power. The result is then normalized to the maximum measured output power at the lowest frequency and plotted in Figure 3.6(b) to show relative output power instead of absolute output power. For a fixed input optical power and biasing of -4 V, the output RF power of each photodiode is measured across frequency. As seen from this frequency response, the PD 3-dB bandwidths are around 4 GHz. Both the IV and RF curves for both of the PDs are very similar, suggesting this pair of PDs will result in excellent balanced performance and high CMRR.

A microphotograph of the TIA used in this photoreceiver is shown in Figure 3.7(a). The total area of the TIA, including pads and bypass capacitors, is 0.16 mm^2. The measured and simulated S_{11} of the TIA is shown in Figure 3.7(b). This shows that the input impedance of the TIA is slightly higher than 50 Ω from 100 MHz to 10 GHz. The measured and simulated transimpedance gain of the TIA is plotted in Figure 3.7(c). The TIA achieves 75 dBΩ of transimpedance and a 3-dB bandwidth of 3 GHz without a PD attached to the input. This does not represent the bandwidth of the entire photoreceiver, as the bandwidth will drop when the input is loaded with a C_{PD}. It should be noted that there is a 1 dB peaking in the measured TIA response. This is an artifact of the way the transimpedance is calculated. At 1 GHz, there is a slight worsening in the TIA match to 50 Ω so the S_{11} of the TIA peaks slightly by about 2 dB around 1 GHz. From eq. (4), a slight increase in S_{11} causes the calculated transimpedance to jump slightly. The output noise of the TIA is measured

with an open-circuited input, and referred back to the input via the measured transimpedance gain. This measured and simulated equivalent input noise current density is shown in Figure 3.7(d). The TIA achieves low equivalent input noise current density, staying around 4 pA/$\sqrt{\text{Hz}}$ through most of the passband. While the measurement is unavailable, the simulations for the TIA group delay is shown in Figure 3.7(e). For most of the passband (up through 2 GHz), the group delay is within 50 ps. The TIA consumes a low dc power of 8 mW, while the output buffer consumes 34 mW, for a total of 42 mW.

The measured conversion gain of the photoreceiver is shown in Figure 3.8(a). The optical-to-electrical conversion gain is defined here as the output electrical RF power per unit of input optical power. The photoreceiver achieves a maximum conversion gain of 10 kV/W, and maintains a high conversion gain over 2 kV/W up through 2 GHz. It should be noted that there is a peaking in the conversion gain. For OFS applications, gain flatness is not necessarily a critical metric and can be calibrated out as the signal of interest is a CW tone. However, for communication applications, variations in gain flatness can lead to distorted eyes and higher bit error rates (BER). The calculated input noise equivalent power (NEP) of the photoreceiver is shown in Figure 3.8(b). This is calculated from the measured output power of the photoreceiver with zero input optical signal, and referred back to the input using the measured conversion gain. The photoreceiver achieves a low input NEP of approximately 8 pW/$\sqrt{\text{Hz}}$ through most of the 2 GHz passband. This demonstrates the minimum input optical power density required to surpass the noise floor of the photoreceiver. By multiplying the NEP by PD responsivity, it is evident that the TIA equivalent input noise current density has increased from 4 pA$\sqrt{\text{Hz}}$ to 7.2 pA$\sqrt{\text{Hz}}$ when loaded with a PD

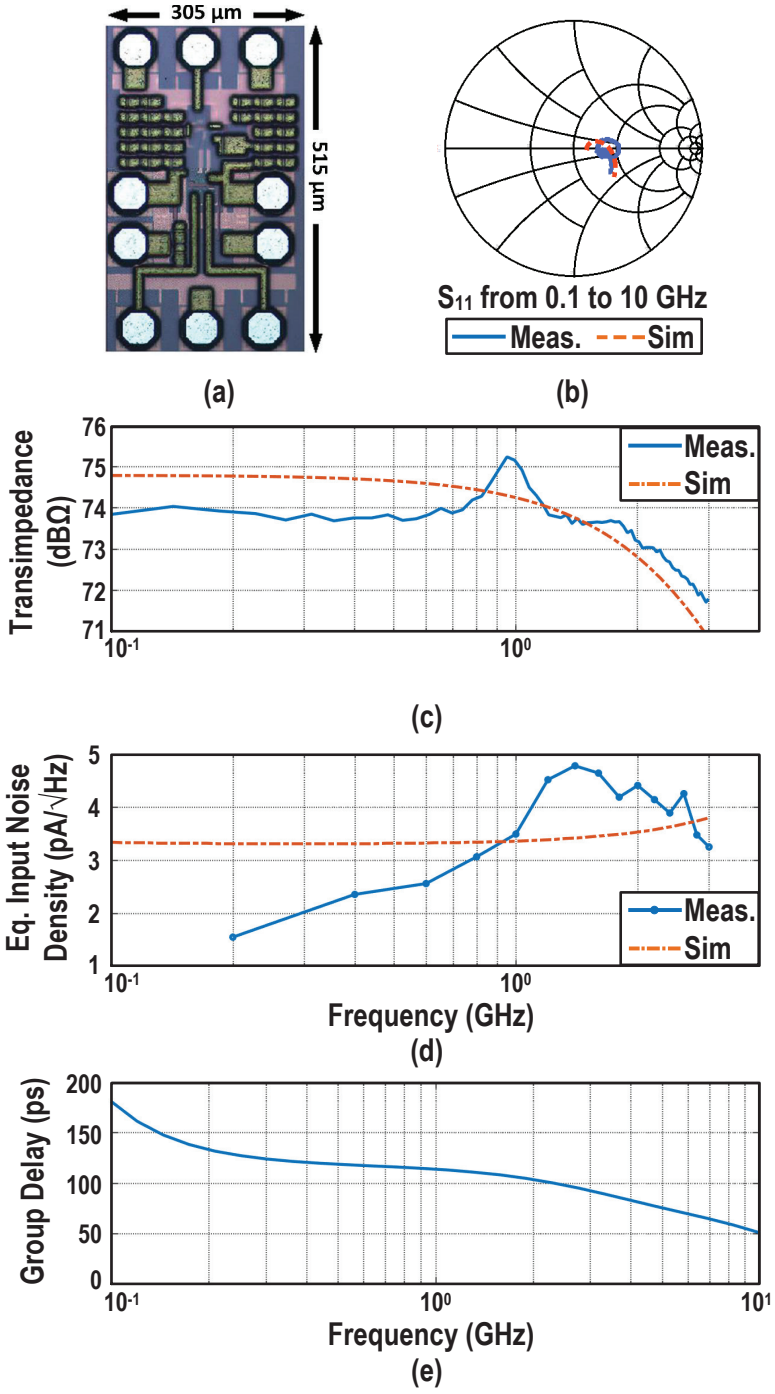

Figure 3.7: (a) Microphotograph of the TIA fabricated on a 130 nm SiGe process. (b) S_{11} of the TIA plotted on a Smith chart from 100 MHz to 10 GHz. (c) Transimpedance gain of the TIA across frequency. (d) Equivalent input noise current density of the TIA. (e) Simulated group delay of the TIA across frequency using layout-extracted models. All simulations include post-layout parasitic extraction.

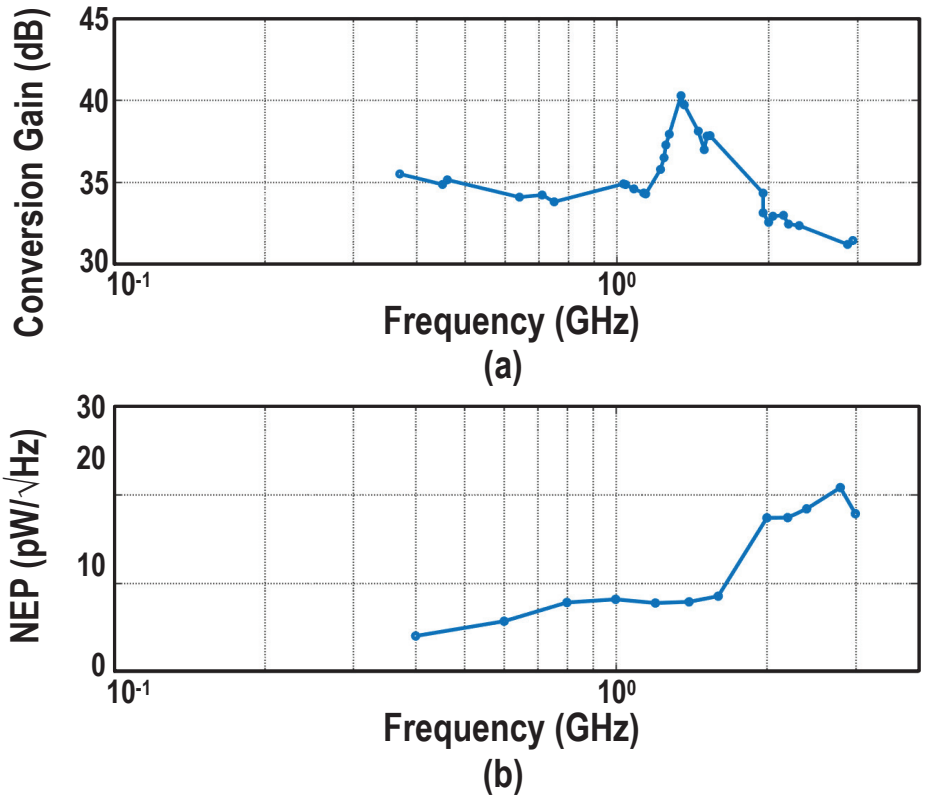

Figure 3.8: (a) Measured conversion gain of the photoreceiver. This is the output electrical RF voltage per unit of input optical power. The conversion gain is represented in dB=10*log10(V/W). (b) Measured input noise equivalent power (NEP), calculated from measured output power with no input optical signal and the optical-to-electrical conversion gain.

capacitance of 380 fF.

The common-mode rejection ratio of the photoreceiver is also measured. This is done by tuning the mechanical delay lines to achieve the maximum (differential illumination) and minimum (common-mode illumination) output RF power at each frequency. Because the delay lines are mechanical, the tunability is limited by the maximum physical length of the delay line. This makes measurement of CMRR at low frequencies difficult, as the delays will be on similar orders of magnitude as the RF wavelength. As such, the photoreceiver's CMRR is measured mostly at the higher frequencies. The CMRR measured is 26 dB at 2 GHz, 30 dB at 2.4 GHz, and 36 dB at 3 GHz.

Eye diagrams sampled from the photoreceiver at several data rates and optical input powers are shown in Figure 3.9(a). The photoreceiver results in clearly open eyes at very low input optical power levels, including 4.4 μW at 1 Gbps, 3.7 μW at 2 Gbps, and 13 μW at both 4 and 5 Gbps. Some distortion and rounding of the eye is present likely due to the peaking in the conversion gain. It is also evident that the higher optical input powers of 56 μW begins to affect the TIA biasing and begins to distort the response further. This is one of the drawbacks of directly dc-coupling the PDs and TIA. However, as the signals of interest for this photoreceiver are very low input powers, this should not be an issue. Additionally, if the PDs were illuminated differentially, most of the dc photocurrents would cancel out, and only the difference current would input to the TIA. Plots of measured BER curves are shown in Figure 3.9(b). The BER is measured at data rates of 1 Gbps, 2 Gbps, and 3 Gbps. The measurement floor of the BER tester is 10^{-8}. It can be seen that the BER can be as low as 10^{-8} with input optical powers as low as 4 μW at 2 Gbps. The input optical powers are back-calculated from the measured PD photocurrents using an estimated internal responsivity of 0.9 A/W [66, 67]. This is to account for the external losses when coupling to the chip input waveguides. The external responsivity is measured as 0.75 A/W, but an internal responsivity of 0.9 A/W is estimated from measurements of similar devices.

A photograph of the photoreceiver is shown in Figure 3.10(a) with a zoomed in view in (b). The total area occupied is 32 mm^2, and can be significantly reduced by dicing off the unused portions of the PD and TIA chips. Additionally, the intermediate trace between the two chips could be removed and the PD directly wirebonded to the TIA. This intermediate trace was left in due to yield issues, as previously discussed.

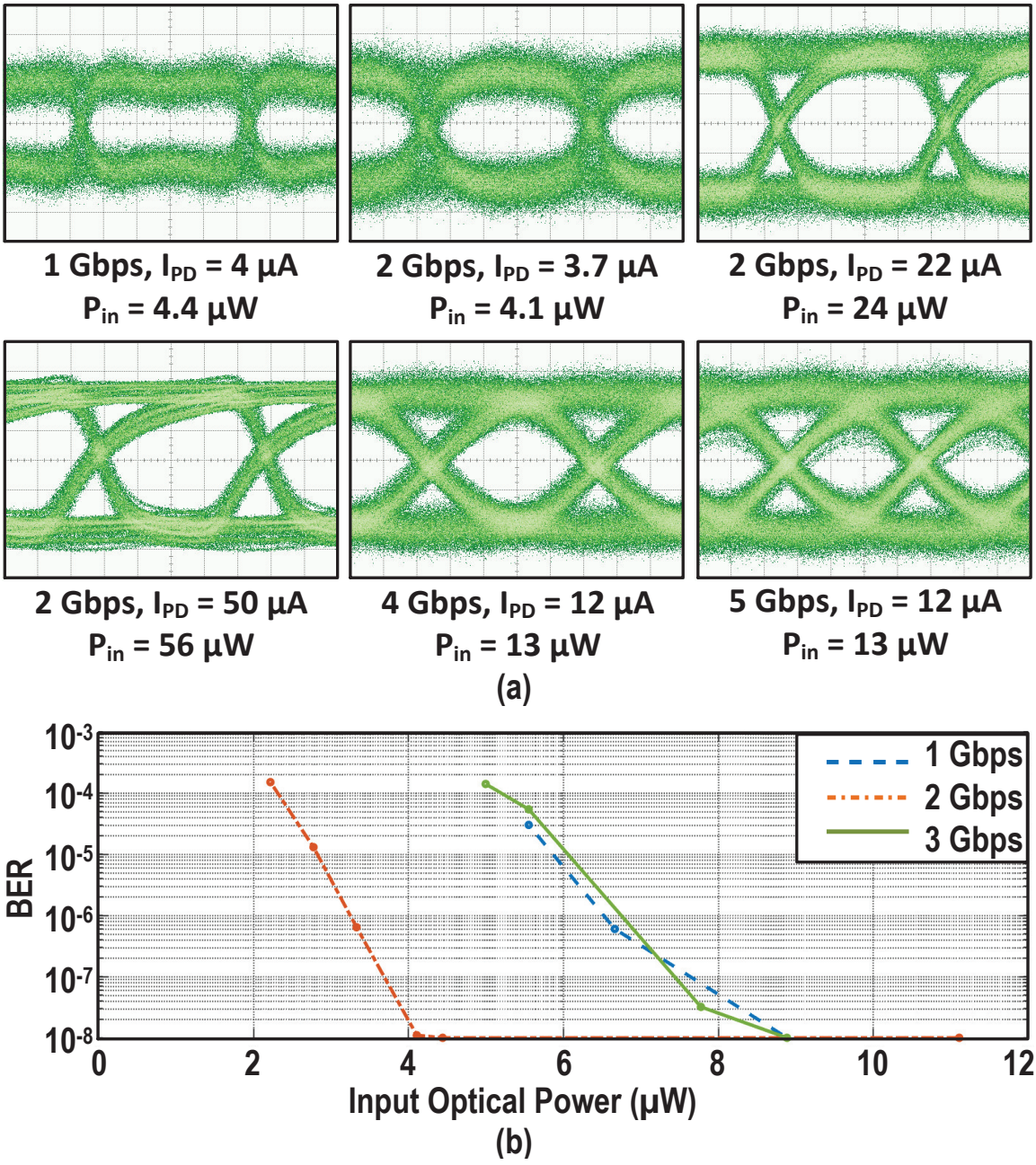

Figure 3.9: (a) Several measured eye diagrams at various data rates and input optical power levels. The input optical powers are calculated from the measured PD photocurrents and an approximate internal responsivity of 0.9 A/W. (b) The BER curves for the photoreceiver at 1, 2, and 3 Gbps data rates across input optical powers. As before, the input optical power is calculated with a responsivity of 0.9 A/W. The floor of the BER tester is 10^{-8}.

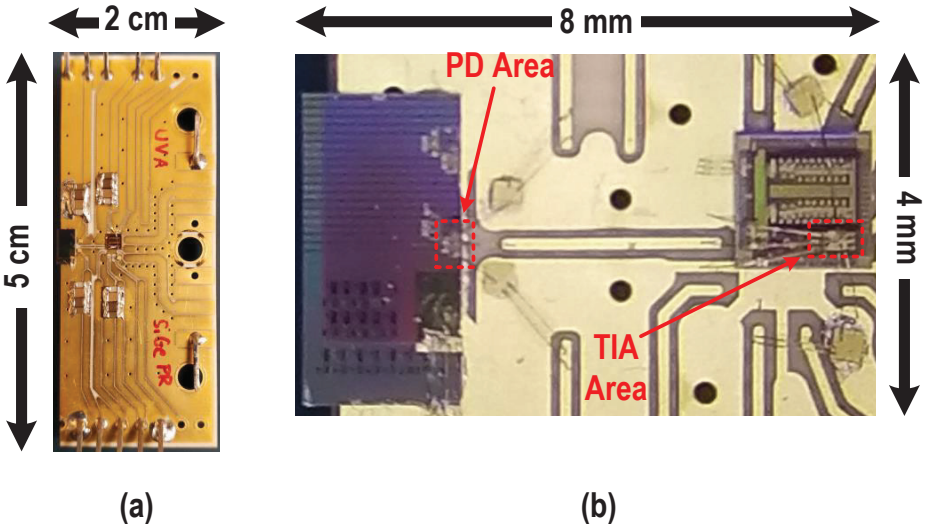

Figure 3.10: Photograph of (a) the integrated photoreceiver board and (b) a zoomed in view, including the InP-on-Si PD chip (left), conductor-backed coplanar waveguide (middle), and SiGe BiCMOS TIA chip (right).

Conclusion

In this work, a low-noise photoreceiver for use in OFS applications is presented. The photoreceiver, consisting of InP-on-Si balanced photodiodes with Si_3N_4 waveguides and a SiGe BiCMOS transimpedance amplifier, achieves a maximum optical-to-electrical conversion gain of 10 kV/W and maintains greater than 2 kV/W up through 2 GHz. Additionally, the photoreceiver exhibits a low input noise equivalent power of approximately 8 pW/$\sqrt{\text{Hz}}$. The photoreceiver, including 50 Ω output drivers, consumes a relatively low dc power of 42 mW. A comparison against other published photoreceivers in literature is presented in Table 3.1. As seen from the table, the InP-based PDs in this work provide very high performance metrics desirable in low-noise links when compared to Ge-based PDs. Additionally, the photoreceiver conversion gain and noise performance is quite competitive. The combination of high conversion gain, low noise, and low dc power makes the photoreceiver a suitable candidate for enabling chip-scale OFS applications.

Table 3.1: Comparison of Published Photoreceivers

Metric	**This** Work	**[38]**	**[39]**	**[40]**	**[69]**	**[70]**	**[71]**	**[72]**
Photodiode								
Responsivity [A/W]	0.9	0.8	0.6	0.32	-	-	0.85	0.45
Dark Current [nA]	10	50	100	-	-	-	-	-
Optical Wavelength [nm]	1550	1550	1550	-	-	-	1550	650
Capacitance [pF]	0.38	-	-	-	1.5	0.7	0.45	1
Single or Balanced	Balanced	Single	Single	Single	Single	Single	Single	Single
Process	InP-on-Si MUTC	Ge PIN	Ge PIN	CMOS APD	Model	Model	External InGaAs PIN†	External Si PIN†
Transimpedance Amplifier								
Trans-impedance [dBΩ]	74	65	-	54	65	72.5	76	79.5
Eq. Input Noise [pA/$\sqrt{\text{Hz}}$]	7.2	28.1	20*	-	9.7*	5	8	-
DC Power [mW]	42	275	-	18$^{\#}$	17	20	19	15
Process	130 nm SiGe BiCMOS	0.25 μm SiGe:C BiCMOS	0.25 μm SiGe:C BiCMOS	130 nm CMOS	0.35 μm RF CMOS	180 nm CMOS*	65 nm RF CMOS	40 nm CMOS*
Photoreceiver								
Bandwidth [GHz]	2	31	13*	2.5	1.9	1	0.7	1.5
Conversion Gain [kV/W]	2	1.4	-	0.16	-	-	5.4	4.2
Integration	Hybrid	Monolithic	Mono.	Mono.	Sims.*	Sims.*	Hybrid.*	Hybrid*

†PD model only. *Estimated from plot. *Simulated only. $^{\#}$Excludes output buffer power.

3.3 TIA Topologies and Observations

When comparing the transimpedance amplifiers presented in chapters 2 and 3 of this dissertation, a few notable design trade-offs can be seen.

The high-speed TIA topologies utilize inputs to the channel of the active devices, as opposed to the low-noise TIA which places the RF input at the base (or gate for FETs). For example, the RGC input is into the FET source. This has several consequences. First, the input impedance can be very low as the already typically small source impedance is divided by the negative feedback factor. In the common-emitter-based TIA, the larger base impedance is divided by the negative feedback factor. Assuming the same negative feedback, it is possible for the prior to have significantly lower input impedances, resulting in higher achievable receiver bandwidths.

In addition to this, there are implications for the noise performance of the TIA as well. The majority of the device noise is present in the channel, with a significantly smaller amount of noise being present at the base (or gate). For an RGC-type TIA, the channel noise is directly at the input of the TIA. For the common-emitter-based TIA, the input is at the base, with all of the channel noise being divided by the gain when referred back to the input. Therefore, for the same transimpedance gain, the base-input (or gate-input) topologies will likely have lesser equivalent input noise densities. However, because they will likely have lower bandwidths as well, the frequency of interest should be considered. If the frequency of interest is significantly higher than the corner frequency, the input-referred noise could end up higher than a TIA with higher bandwidth despite its worse in-band noise performance.

3.4 Conclusions

With a departure from the higher speed photoreceivers researched and presented in chapter 2, a photoreceiver with an emphasis on lower noise is developed. A TIA was designed, fabricated, and measured in a 130 nm SiGe BiCMOS process, allowing use of some HBT BJT devices compared to the CMOS processes used in the previous chapter. This TIA was then combined with a UVA-fabricated InP/InGaAs photodiode on silicon nitride waveguides on a silicon chip. This resulted in a very low noise photoreceiver suitable for low power signal detection in targeted OFS applications. With the higher conversion and lower noise, the photoreceiver can help enable OFS systems that can lower the optical source pump power, which dominates the power consumption of the system.

3.5 Relevant Publications

First-Authored Publications

- R. Costanzo, Q. Yu, X. Shen, J. Gao, A. Beling and S. M. Bowers, "Low-noise balanced photoreceiver with waveguide SiN photodetectors and SiGe TIA," *2020 Conference on Lasers and Electro-Optics (CLEO)*, San Jose, CA, USA, 2020, pp.1-2.

- R. Costanzo, J. Gao, X. Shen, Q. Yu, A. Alabdulwahab, A. Beling and S. M. Bowers, "Low-Noise Balanced Photoreceiver with InP-on-Si Photodiodes and SiGe BiCMOS Transimpedance Amplifier," in *Journal of Lightwave Technology*, revisions submitted Feb. 15, 2021.

Chapter 4

RF Photonic Circuits on Silicon Photonics Platforms

4.1 Introduction

As it continues to grow, silicon photonics (SiP) offers promising solutions for a large range of applications. Much of the recent work focuses on high capacity data communication and optical interconnects. High-bandwidth germanium-on-silicon (Ge-on-Si) PDs have been reported in many works regarding silicon photonics [73, 74, 75, 76, 77, 78, 79, 80, 81, 82]. Many SiP foundries are offering Ge PDs due to their high speeds. For example, epixfab/IMEC's SiP platform has demonstrated a 67 GHz bandwidth Ge PD applied to a 56 Gbps optical link [83]. The IME-ASTAR foundry has demonstrated a Ge PD with 60 GHz of bandwidth with on-chip inductors

to achieve inductive peaking [84]. Owing to the reliability, compactness, and cost-effectiveness of SiP platforms, integrated microwave photonic systems have gained popularity. Integrable PDs capable of achieving high power and high linearity will play a critical role in achieving high RF gain and spur free dynamic range (SFDR) in RF and mm-Wave photonic links. To explore this possibility, we have designed and fabricated several high-power Ge PDs and PD arrays on the AIM SiP platform. In addition, several photonic circuits have been designed, fabricated, and described.

4.2 Germanium-on-Silicon Waveguide Photodiode and Arrays

One of the most important pieces in an RF photonic link is the photodetector. The photodiode (PD) converts the incoming optical signal into an electrical RF signal. Therefore, several configurations were designed and fabricated to test the performance achievable in the process. By arraying PDs within the chip, high linearity and power handling can be achieved at the cost of increased dark current and PD capacitance, or reduced bandwidth.

Several of the designed photodiodes and arrays are shown below in Figure 4.1. In this process, an individual analog germanium PD was fabricated and is shown in Figure 4.1(a). While the process also offers digital and monitor PDs that higher responsivities, the analog has the highest RF bandwidth. This makes it the most appealing for RF photonic links. In order to investigate the trade-off between RF bandwidth, dark current, PD capacitance, and power handling capabilities, PD arrays using the analog PD were also designed and fabricated. In Figure 4.1(b), (c), and (d), the schematic and microphotographs of the 2, 4, and 8-element arrays are shown. The optical inputs

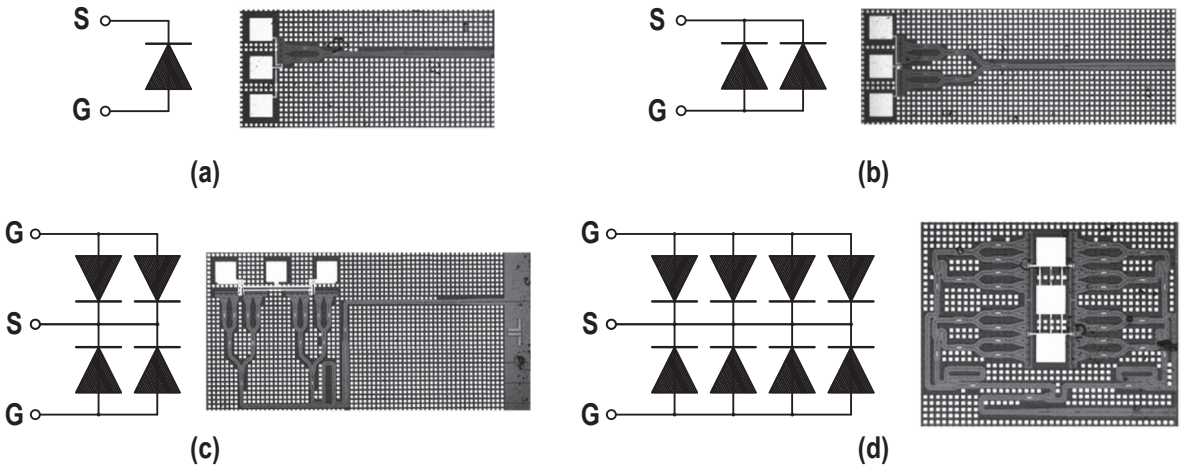

Figure 4.1: Schematic an microphotographs of (a) single analog photodiode, (b) a 2-PD array, (c) a 4-PD array, and (d) an 8-PD array.

are edge-coupled waveguides at the outer edges of the chip, and the RF outputs are ground-signal-ground (GSG) pads. To make these arrays, optical Y-junctions are utilized and additional optical delay lines are added when needed to match all optical delays from the input waveguide to each individual element of the array. The waveguides are implemented in the silicon waveguide layer.

First, the dc characteristics of the PD and arrays are investigated. This is done with zero input optical power. To investigate the dark current or noise current of the photodiodes, the dc current draw is measured as the dc bias voltage on the PD is varied. As the reverse bias voltage is increased, the dark current will increase. The measurements of this dark current I-V curve is plotted in Figure 4.2(a). The individual photodiode exhibits a dark current of hundreds of nanoamps with a bias voltage of -3 V. When arrayed, the dark current increases significantly, with all the arrays exhibiting approximately tens of microamps at the same bias voltage. Thus, the individual device has the best dark current performance.

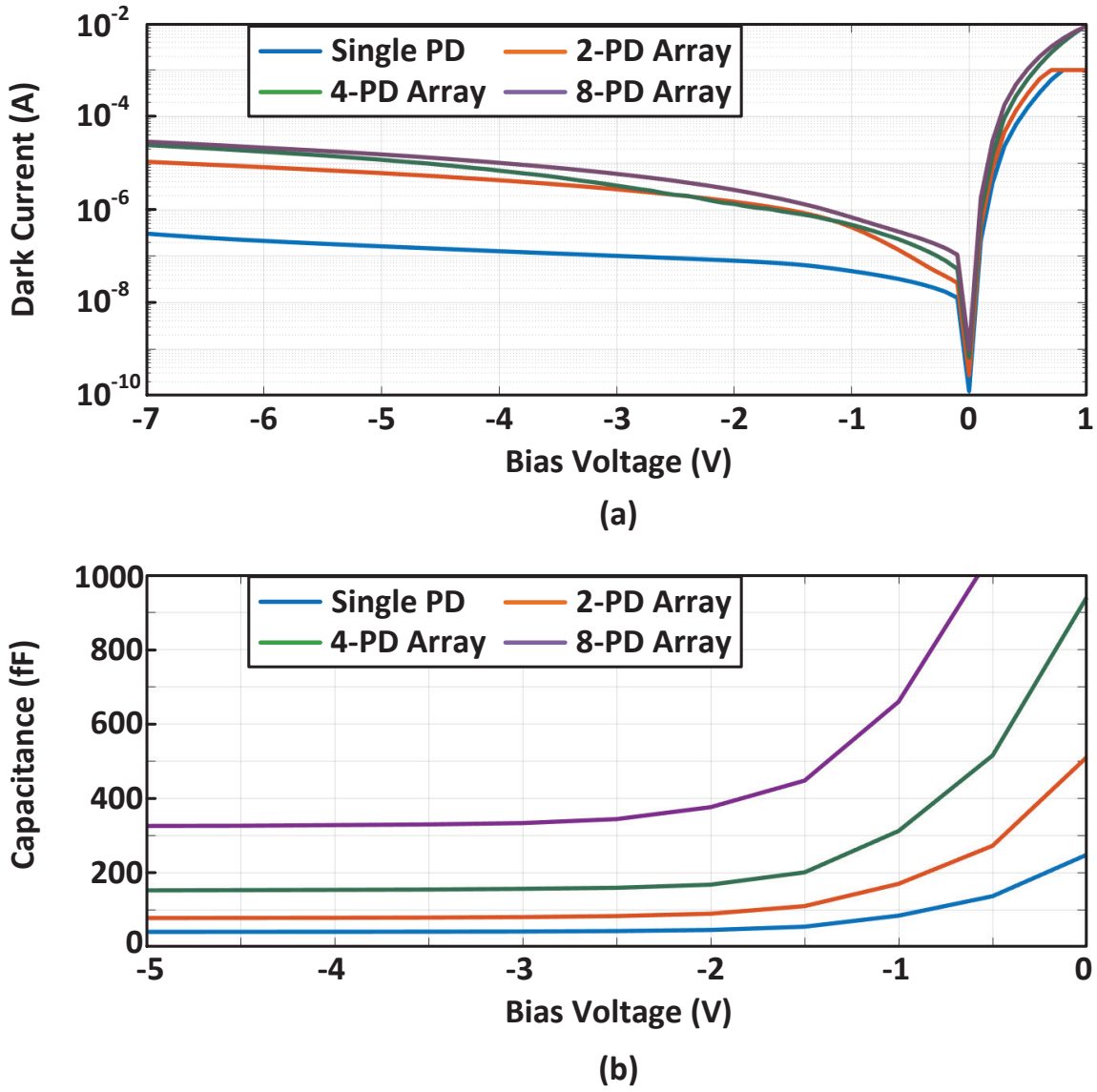

Figure 4.2: Plots of the (a) C-V and (b) I-V curves for the single PD, the 2-PD, 4-PD, and 8-PD arrays.

When the reverse bias of the PD is varied, the PD capacitance changes as well. This capacitance directly impacts and often limits the bandwidth of a microwave photonic link. As the reverse bias is increased and the electric field through the junction increases, the effective capacitance will lower.

The measured capacitance versus voltage (C-V) curve is shown in in Figure 4.2(b). At a reverse bias of 3 V, the individual photodiode shows a low PD capacitance of approximately 40 fF. The 2-PD array exhibits a PD capacitance of about twice that, around 80 fF. This is expected, as an N-element array should have a junction N-times larger than an individual element. This relationship continues when looking at the 4-PD array and 8-PD array C-V curves.

In order to characterize the RF performance of each PD or PD array, an input optical beat signal is edge-coupled into the input waveguides. Then, the output RF power is probed from the GSG pads. The optical beat frequency is then tuned across microwave frequencies to measure the PD or array's RF response. In addition, the optical input power is varied to change the photocurrent output from the PDs, giving an idea of how much power the photodiodes are capable of handling. The photodiodes are biased through an off-chip bias-tee. These PD arrays show a wide variety of bandwidths and power handling. Most importantly, the bandwidths are sufficient for high-speed RF photonic links up through tens of gigahertz. The load seen by each of these PD arrays is 50 Ω from the RF test equipment.

The measured RF responses are plotted in Figure 4.3. In Figure 4.3(a), the single PD achieves the highest bandwidths of about 21 GHz. The highest RF output power achievable was approximately 0 dBm with 7 mA of photocurrent. Going much higher than this photocurrent may damage the individual device. However, when arraying the devices, the photocurrent and optical input powers can be increased as the power handling is spread out across multiple devices. The 2-PD array measurements in Figure 4.3(b) show that the maximum output power achievable was over 6 dBm, with bandwidths of 16 GHz. Further, the 4-PD array achieves an output power of 12 dBm with 30

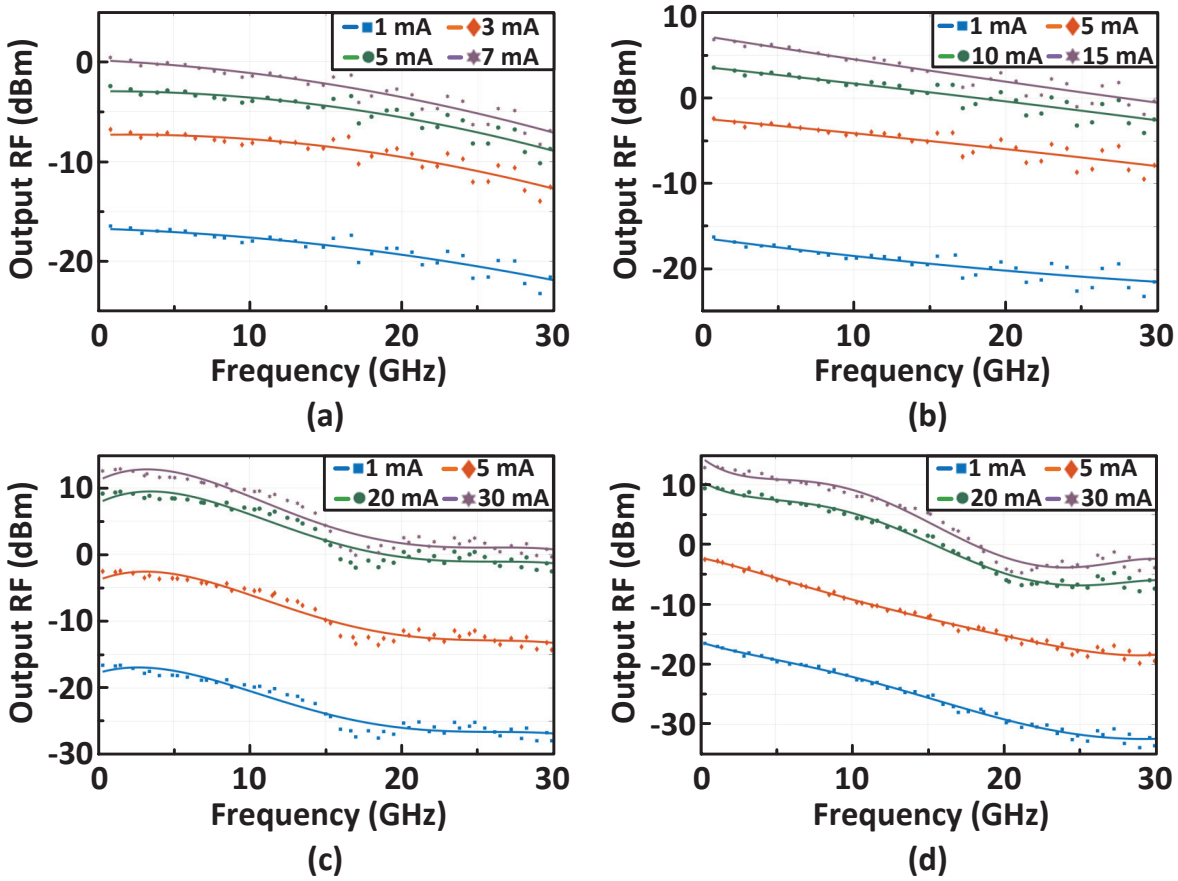

Figure 4.3: Plots of RF responses of the (a) single PD, (b) 2-PD array, (c) 4-PD array, and (d) 8-PD array. Multiple curves are shown for some of the different measured photocurrents, corresponding to different optical input powers.

mA of photocurrent, and a bandwidth of 10 GHz, shown in Figure 4.3(c). Lastly, in Figure 4.3(d), the 8-PD array experiences an 8 GHz bandwidth with similar output powers. These levels of output powers at microwave frequencies are very promising for enabling high fidelity microwave photonic links in a chip-scale solution. More measurements, including power saturation and OIP3, can be found in our published works [32, 61, 85, 86, 87].

4.3 Balanced Photodiodes with Thermo-Optic Phase Shifters

In addition to the photodiode arrays, circuits that utilized thermo-optic phase shifters and 2x2 optical couplers were also designed, implemented, and measured. In this circuit, shown in Figure 4.4(a), two vertical grating couplers were used as opposed to the edge-couplers used in the arrays. While the edge-couplers have a higher coupling efficiency, the vertical couplers were used in order to make use of chip area further from the edge of the chip. The two optical inputs are combined and split via a 2x2 optical coupler. The coupler splits the power into two paths, each with an optical phase shifter. Then the outputs of the phase shifters are recombined and split via another 2x2 optical coupler and sent into a balanced PD structure. Because the balanced structure detects only differential illumination, while rejecting any common-mode illumination, the phase shifters can be used to tune the optical illumination into differential or common-mode.

In order to test the circuit, the I-V performance of the individual PDs is measured. In order to achieve good balanced operation, the I-V curves should be well-matched. As shown in Figure 4.4(b), the dark currents are very close and good balanced performance is expected.

To test the full circuit, one of the phase shifters was grounded and not tuned for simplicity. Instead, only the other phase shifter was tuned via a bias voltage. Additionally, a CW optical signal was only input into one of the vertical couplers. While varying the bias voltage on the phase shifter, the output photocurrent from each of the photodiodes in the balanced structure was measured. This measurement is shown in Figure 4.4(c). This shows that the $V\pi$ and quadrature point of the structure occurs at a phase shifter bias voltage of 4.5 V. Additionally, 5.7 V results in the highest

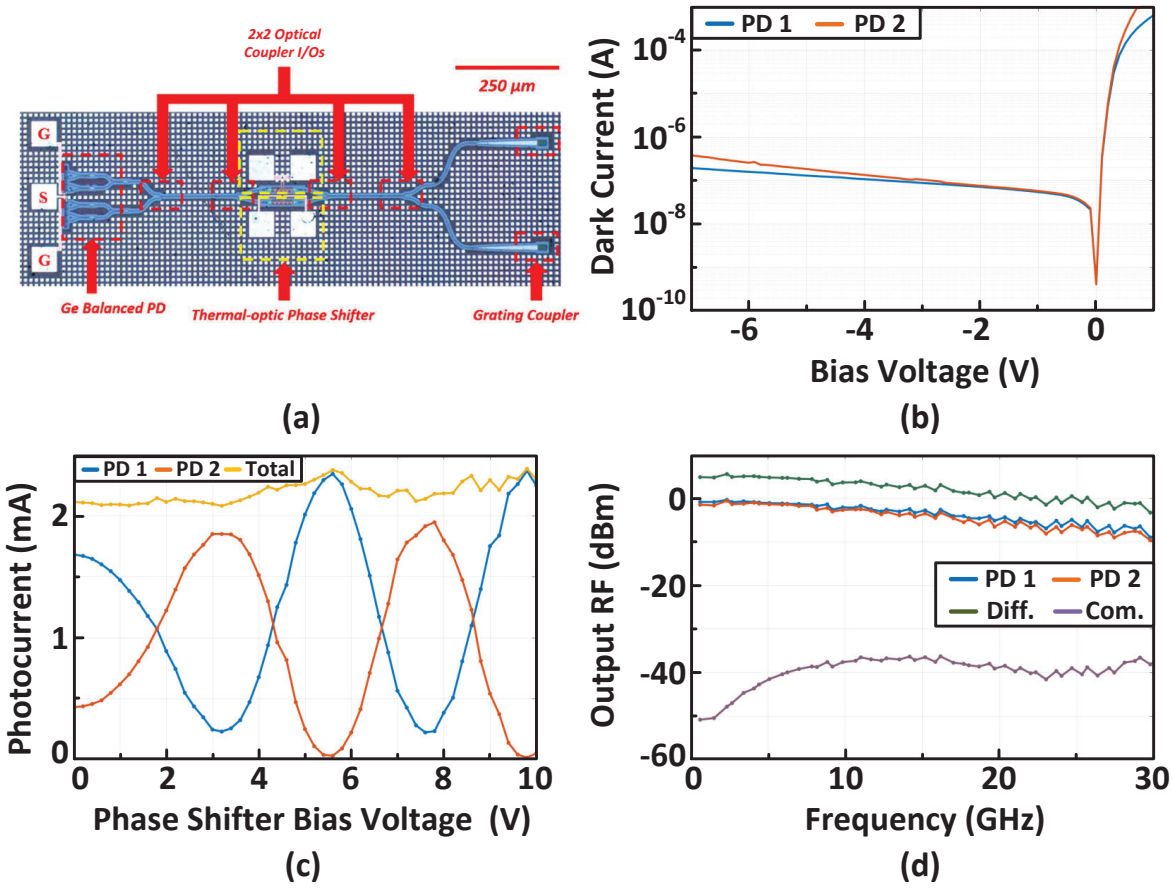

Figure 4.4: (a) Labeled microphotograph of the balanced photodiode structure with integrated thermo-optic phase shifters. (b) Plot of measured I-V curves for the PDs in the balanced structure. (c) Plot of measured photocurrent through each PD as the phase shifter bias is varied. (d) Plot of measured output RF powers for both PDs, as well as for common mode illumination. In addition, the calculated differential mode output power is also plotted.

difference between the two device illuminations. It should be noted that the total photocurrent remains relatively constant, showing the optical signal is being steered between the two devices as the phase shift is altered.

To measure the common mode rejection of the balanced structure, the output RF power is measured at the quadrature point for the common-mode illumination when the two photocurrents cancel each

other. To measure the differential mode, a voltage of 5.7 V is applied to the phase shifter. Then, the output RF power of PD1 is measured. While maintaining the same 5.7 V and phase shift, the grating coupler being illuminated is switched, which causes PD2 to be the primary illuminated device, instead of PD1. The output RF power of PD2 is measured. Lastly, the output powers of PD1 and PD2 are combined to estimate the differential performance. The output powers of the individual PDs, the common-mode output power of the balanced structure, and the estimated differential output power is plotted in Figure 4.4(d). The common-mode rejection ratio (CMRR) is the difference between the differential and common-mode outputs, and is found to be approximately 37 dB over the full 21 GHz bandwidth, suggesting a highly symmetric response. This kind of symmetry and device yield can help enable more complex circuits in the microwave photonic application space.

4.4 Balanced Mach-Zehnder Delay Line Interferometer

To investigate the performance of an on-chip optical link, a balanced Mach-Zehnder delay line interferometer (MZI) for receiving and demodulating phase-modulated signals is designed and investigated. This MZI can be seen in the labeled microphotograph shown in Figure 4.5(a). The circuit consists of input optical vertical grating couplers that are combined and split through a 2x2 coupler. One of the outputs passes directly to the next 2x2 coupler. The other output goes through an RF delay line before the next 2x2 coupler. This delay line in one path acts as a interferometer which can demodulate phase shifted signals into an amplitude signal.

To test it, a tunable CW laser is input into the circuit and the output photocurrent of each PD is

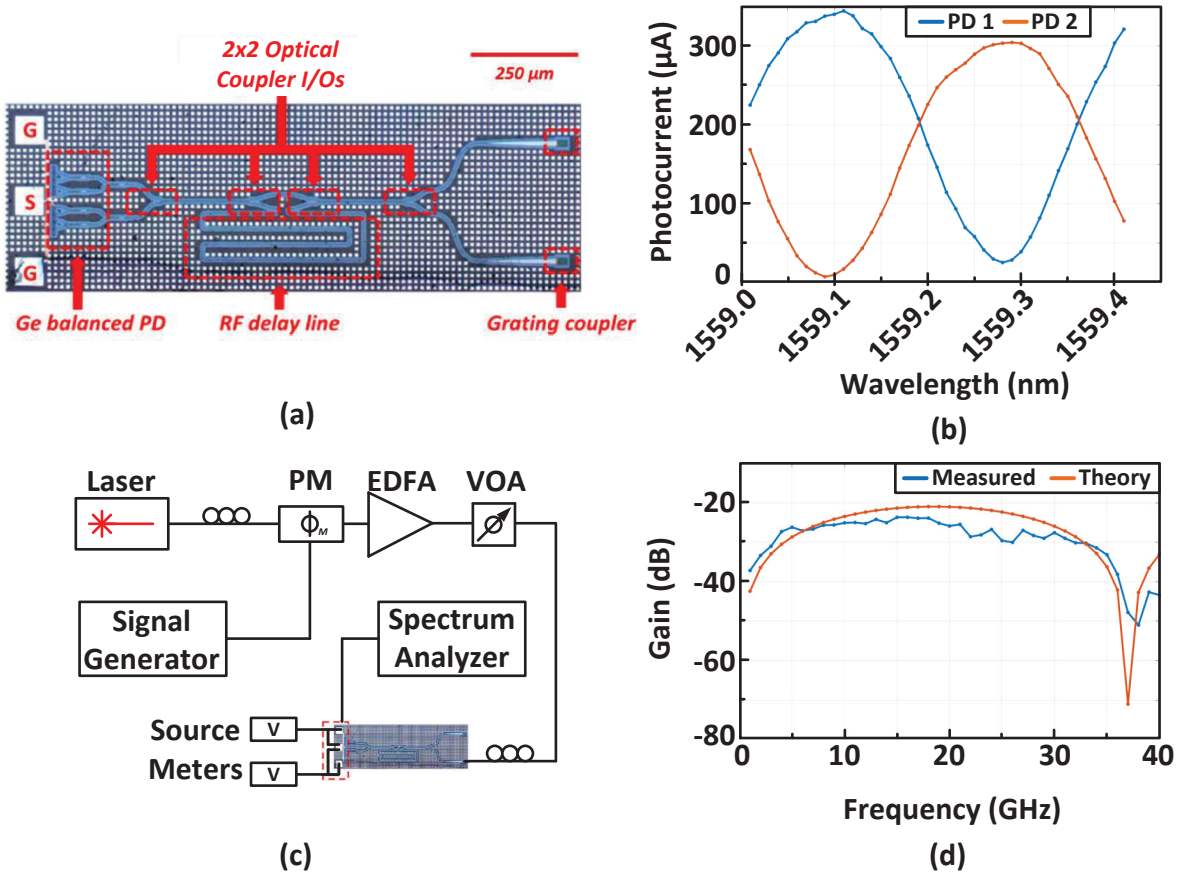

Figure 4.5: (a) Labeled microphotograph of the balanced MZI structure with integrated RF delay line. (b) Plot of measured photocurrent versus input optical wavelength. (c) Test setup used for measuring phase modulated link. (d) Plot of measured link gain versus RF frequency.

measured. The photocurrents are measured across optical wavelength. Figure 4.5(b) shows the plotted measured photocurrents through each PD across input optical wavelength. The two curves cross at approximately 1559.2 nm, which makes it a quadrature point in the phase modulated link.

To test the operation of the MZI in a phase modulated link, a test setup like the one depicted in Figure 4.5(c) is used. A tunable 1550 nm laser is input into a phase modulator (PM), followed by an erbium doped fiber amplifier (EDFA) and variable optical attenuator (VOA) for better precision

over optical power. The actual wavelength of the laser is set to 1559.2 nm, the quadrature point found in the previous measurement. The optical signal is coupled into one of the vertical grating couplers. The balanced photodiodes are biased through a probe with custom bias-tees on-probe, and the RF output is monitored on an electrical spectrum analyzer. The measured gain spectrum of the link is plotted in Figure 4.5(d). From this measurement, the free spectral range (FSR) of the interferometer is found to be 38 GHz, which is beyond the bandwidth of the PD which will cause the response to start dropping quickly. During the design phase, the delay line was meant to create an FSR of about 20 GHz, but the effective index was likely incorrectly estimated. The theoretical gain is plotted as well, with the calculations shown below.

For a phase modulated link operating at its quadrature point, the small signal gain can be calculated using Eq. (4.1) from [53]:

$$g_q = \frac{4\beta^2 I_{dc}^2 sin^2(\pi f \tau) Z_0 Z_{in} \pi^2}{V_\pi^2} |H_{pd}|^2 \tag{4.1}$$

where g_q is the link gain, $\beta = \frac{\varsigma - 1}{\varsigma + 1}$ where ς is the modulator extinction ratio, τ is the phase delay from the delay line, Z_0 is the load at the output, Z_{in} is the input impedance looking into the phase modulator, V_π is the phase modulator's half-wave voltage, and H_{pd} is the frequency response of the photodiode. The values used to estimate the gain are as follows: β = 0.95, V_π = 7 V, Z_0 = 50 Ω, Z_{in} = 50 Ω, $|H_{pd}|^2$ = 0.5, and τ = 25 ps, corresponding to the measured FSR of 38 GHz. The measured link gain follows the theoretical gain very closely.

4.5 Conclusions and Future Work

The work explored the design and measurement of circuits on a developing silicon photonic platform. The first investigation was into the germanium-on-silicon photodetectors, which are critical in determining the performance of potential RF photonic links on chip. Using a variety of PD and PD arrays, on-chip solutions capable of outputting very high RF powers and bandwidths are demonstrated. Output RF powers of up to 12 dBm and bandwidths up to 21 GHz are observed, promising for on-chip microwave links. Additionally, several circuits involving thermo-optic phase shifters and on-chip couplers and delay lines are utilized to create phase modulated links with mm-Wave range FSRs.

4.6 Relevant Publications

Co-Authored Publications

- K. Sun, R. Costanzo, T. Tzu, Q. Yu, S. M. Bowers and A. Beling, "Ge-on-Si waveguide photodiode array for high-power applications," *2018 IEEE Photonics Conference (IPC)*, Reston, VA, 2018, pp. 1-2.

- T. Tzu, K. Sun, R. Costanzo, D. Ayoub, S. M. Bowers and A. Beling, "Foundry-enabled high-power photodetectors for microwave photonics," in *IEEE Journal of Selected Topics in Quantum Electronics*, vol. 25, no. 5, pp. 1-11, Sept.-Oct. 2019.

- K. Sun, T. Tzu, R. Costanzo, Q. Yu, S. M. Bowers and A. Beling, "Ge-on-Si balanced periodic traveling-wave photodetector," *2019 IEEE Photonics Conference (IPC)*, San Antonio, TX, USA, 2019, pp. 1-2.

- K. Sun, R. Costanzo, T. Tzu, S. M. Bowers and A. Beling, "Foundry-Enabled Ge Photodiode Arrays on Si on Insulator with On-Chip Biasing Circuit," *2020 IEEE Photonics Conference (IPC)*, Vancouver, BC, Canada, 2020, pp. 1-2.

- K. Sun, et al., "Germanium Photodiode Arrays on Silicon-On-Insulator with On-Chip Bias Circuit," in *IEEE Photonics Technology Letters*, accepted Mar. 4, 2021.

Chapter 5

Optical Phase-Locked Loop

5.1 Introduction

The phase-locked loop (PLL) is a very important circuit in nearly every piece of modern communication technology. The phase-locked loop is responsible for maintaining clean signals and lowering the frequency and phase noise of a frequency signal, typically from a voltage controlled oscillator of some sort. The most basic block diagram of a PLL is shown below in Figure 5.1.

The first block in the chain is the phase-frequency detector (PFD). This block is responsible for comparing the output signal from the voltage-controlled oscillator against a reference signal. Compared to a traditional phase-detector, the phase-frequency detector is capable of generating its output control signal based on the difference of both the phases and the frequencies of the two signals. Because of this benefit, the PFD is typically used over a standard phase-detector to achieve locking

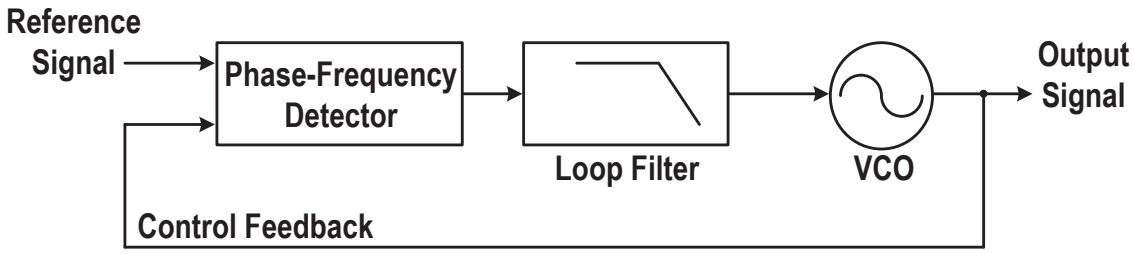

Figure 5.1: Block diagram of a phase-locked loop consisting of a phase-frequency detector, loop filter, and voltage-controlled oscillator.

in the most adverse conditions [88]. While the PFD can output the error signal in a voltage or a current signal, the current output is typically chosen and can be implemented as a charge pump. The PFD with voltage output signal suffers from "backlash", resulting in output spurious frequency signals [88].

To understand the function of the PFD, consider the three possible scenarios concerning the reference and output signal, shown in Figure 5.2. The first case is when the reference signal and the output signal are perfectly matched, with no phase or frequency error between them. This results in a steady-state PFD output signal. However, in case 2, the output signal is "lagging" behind the reference signal. The PFD detects the lagging and outputs a positive PFD correction signal, causing the VCO to speed up and correct to case 1. Conversely, in case 3, the VCO output signal is "leading" the reference signal. This causes the PFD to detect and generate a negative corrective signal instead. It should be noted that the negative/positive error signals can be swapped for leading/lagging scenarios depending on the response of the VCO (also known as K_{VCO}). In other words, a VCO with a positive K_{VCO} will increase its frequency with a positive error signal, and

will decrease its frequency with a negative error signal. A VCO with a negative K_{VCO} simply does the opposite.

The output signal of a current-based PFD is typically generated by a charge pump. The charge pump intakes the previously discussed error signals and either injects or removes current from the PFD output node depending on the configuration and polarity of K_{VCO}. This addition and subtraction of current on the output node changes the voltage of the node into the VCO, which corrects the VCO output signal.

Between the PFD and the VCO is the loop filter. The loop filter serves an important purpose. Utilizing a low-pass response, the loop filter removes the higher frequency products generated by the PFD, and creates a low frequency DC component that is proportional to the error signals output from the PFD. It also smooths out the control signals generated from the PFD and reduces the rippling which can affect the VCO. Additionally, the loop filter also helps with loop stability, preventing the PLL from oscillating and never reaching a locked condition.

The last block of the basic PLL is the voltage-controlled oscillator (VCO). This is an oscillator that outputs a frequency signal, which can be tuned via an input control signal. This input control signal is generated by the aforementioned PFD and loop filter. For the work presented in this work, the VCO is actually a heterodyne setup of two optical lasers, as opposed to a traditional electronic oscillator. This is what is known as an optical phase-locked loop (OPLL), where electronic control loops are applied to optical sources or lasers to generate a stable beat frequency locked to a lower, cleaner microwave reference. This is discussed further in the following section.

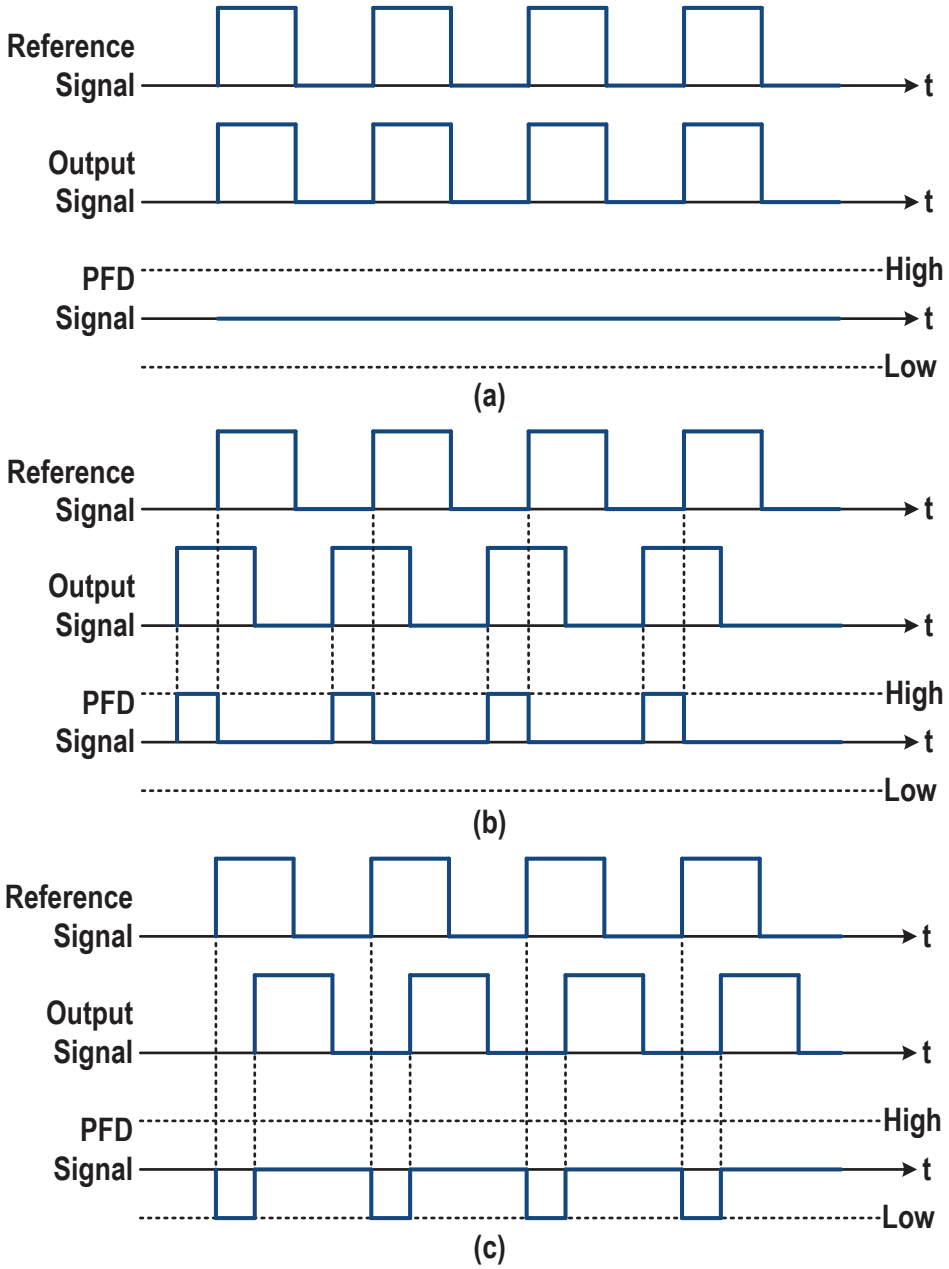

Figure 5.2: Input and output waveforms for the phase-frequency detector in three cases: (a) Case 1, when the reference and VCO output are matched. (b) Case 2, when the reference and VCO output signals are generating a positive phase error signal. (c) Case 3, when the reference and VCO output signals are generating a negative phase error signal.

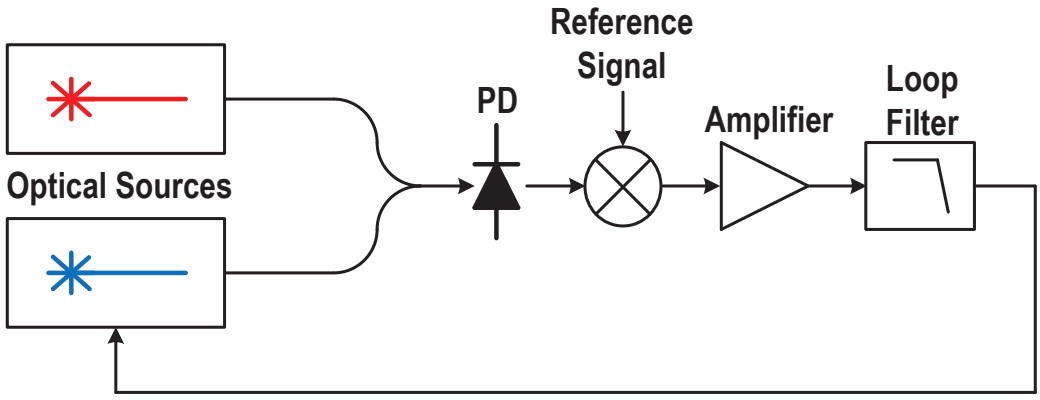

Figure 5.3: Block diagram of basic optical phase-locked loop, used to lock the beat frequency of the two lasers to an RF reference.

The basic approach towards achieving phase coherence between two optical sources in an OPLL is shown in Figure 5.3 [89]. The beat frequency (or difference frequency) between the two optical sources is extracted via the PD. Then, the phase of the beat note is compared to the phase of the reference RF signal, typically supplied from a signal generator. The output voltage, proportional to the difference between the phases of the beat signal and the reference signal, is fed back through a loop filter to one of the lasers acting as a slave laser. This will allow much of the phase difference between the two lasers to be corrected out.

This technique has been explored in bench-top systems for decades. Back in 1989, the beat frequency of two highly stable external cavity GaAlAs lasers was locked, resulting in a very clean beat signals with linewidths of under 3 kHz [90]. In 1992, a heterodyne OPLL was shown to achieve a linewidth of 8 MHz, but was widely tunable from 3 to 18 GHz [91]. This shows one of the strengths of leveraging the wide optical tunability in a heterodyne setup to achieve a wide

tuning range in the microwave domain. In another work presented in 1999, a locking method combining the OPLL technique and the optical injection locking demonstrated an even wider 26 GHz of locking range while achieving a 36 MHz summed linewidth while utilizing semiconductor lasers [92]. Semiconductor lasers are known for having wider linewidths than larger discrete lasers, but are significantly more cost-effective and easily integrated. Therefore, there is much interest in being able to lock them and improve their linewidths using an OPLL control loop. In order to achieve beat frequency locking at higher microwave frequencies, a frequency down-conversion method was presented in 2006 [93]. This allowed the electronic control loop of the OPLL to utilize lower frequency components to achieve locking at higher frequencies while sacrificing some of the phase noise improvement. By combining aspects from much of these works, the work presented in this thesis attempts to achieve a chip-scale OPLL that would enable many new applications and technological progression by no longer being restricted by bench-top implementations.

5.2 Heterogeneously-Integrated Optical Phase-Locked Loop

The primary effort of this work is to create a two-chip heterogeneously integrated solution capable of creating an optical phase-locked loop. This would allow a chip-scale solution that could result in the creation of clean, stable RF beat frequencies generated via optical heterodyning, which would enable low power, low cost, and low size methods of signal generation for applications such as RoF and OFS. The electronic control portion is designed, simulated, and fabricated in a 65 nm general-purpose CMOS process, and the optical control portion is designed and fabricated in a silicon

photonic process. Each of these standalone chips is discussed in more detail in the subsequent sub-sections. Finally, the final close-loop integration schemes for a single and a dual-loop OPLL is discussed.

5.2.1 Electronic Chip Design in 65 nm CMOS

System

The CMOS chip designed is responsible for the electronic control of the OPLL. The overall circuit is shown in Figure 5.4. Both the reference (REF) and the RF signal are biased through 50 Ω resistors. This allows the RF to see 50 Ω termination at the input, rather than the high impedances of the input buffers. This is important as a high impedance termination will severely impact the higher frequency capabilities of the REF and RF sources. The REF is provided from an off-chip CW signal generator and the RF is provided by the photodiode on the silicon photonic chip (discussed in the next sub-section). The RF is input into an RF mixer, which mixes the RF frequency against the input local oscillator (LO) signal, resulting in a lower intermediate frequency (IF) signal, comparable against the frequency of the lower frequency REF signal. The targeted design frequencies are a 28 GHz RF signal, a 27 GHz LO, a resulting IF of about 1 GHz, and a reference frequency of 1 GHz. The inverters at the input attempt to digitize and amplify the input signals for comparison in the subsequent phase-frequency detector.

The PFD compares the down-converted RF signal to the REF signal and outputs error correction signals. The outputs come in the form of UP and DOWN (DN) pulses. Nominally, for a VCO

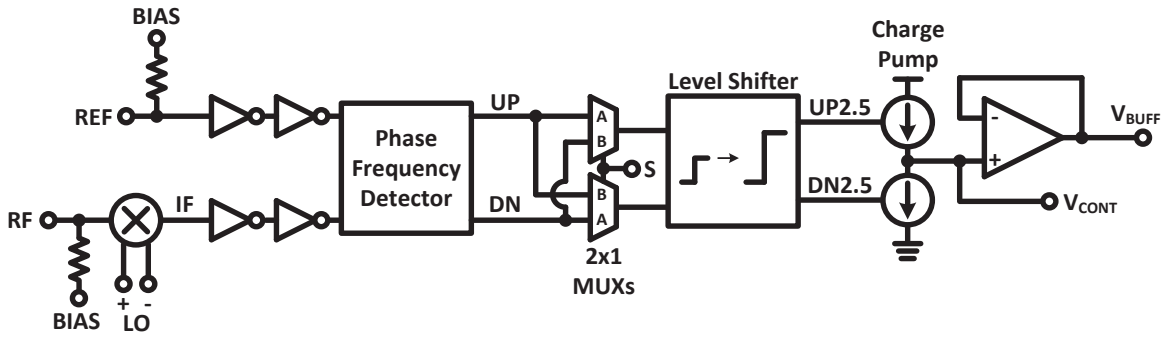

Figure 5.4: System drawing of the electronic control portion of the optical phase-locked loop.

with a positive K_{VCO}, the UP pulses will act as positive error correction signals, and the DN pulses will act as the negative error signals. In the case of a VCO with a negative K_{VCO}, the 2x1 multiplexers (MUXs) can be switched to correct this. If the switch signal (S) is enabled, the UP pulses will switch to acting as negative error correction signals, and the DN pulses will switch to acting as positive error correction signals. This provides more versatility for the OPLL as it can accommodate both negative and positive K_{VCO}.

To increase the tuning range of the OPLL, level shifters are implemented to convert the correction signals from a 1.2 V domain to a 2.5 V domain. This means the error signal to the VCO can range from 0 V to 2.5 V, rather than only to 1.2 V. This level shifted signal is then output to a charge pump. Nominally, when the charge pump receives an UP pulse, it will inject current onto to output V_{CONT} node. When it receives a DN pulse, it will sink current from the output V_{CONT} node, lowering its voltage. The final block is an operational amplifier configured as an output buffer to drive off-chip components such as the laser piezoelectric tuning control. The remaining content of this sub-section will discuss each individual block in more detail.

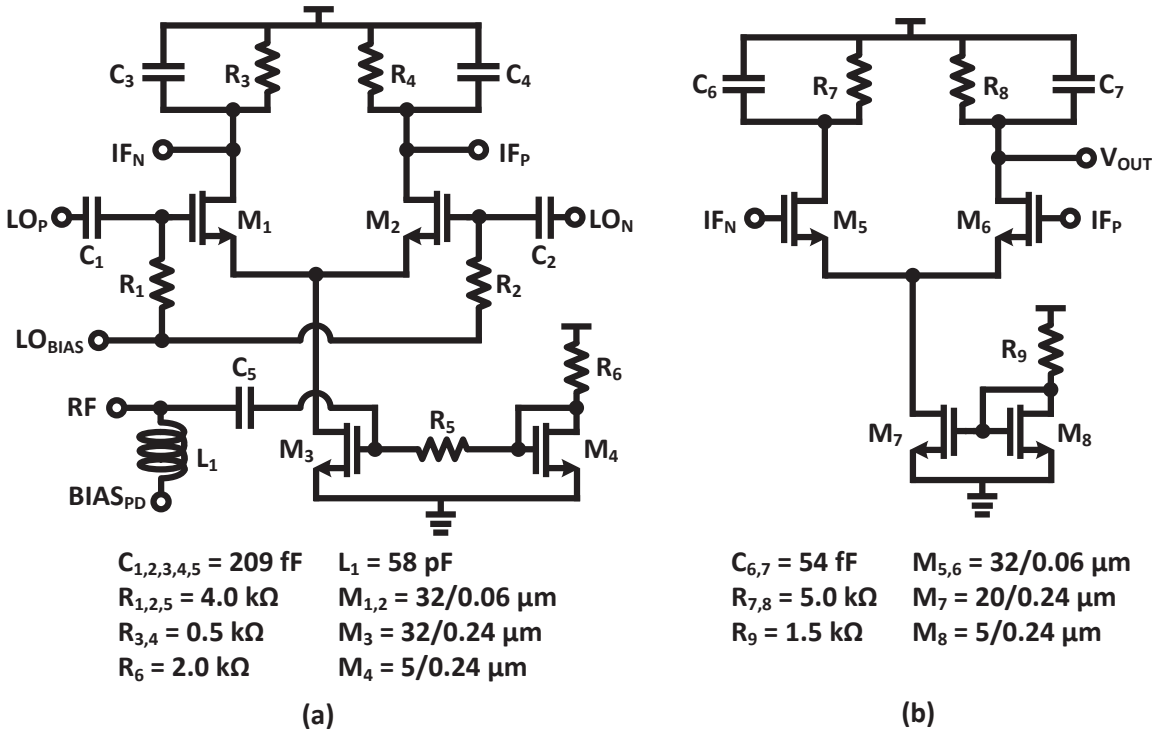

Figure 5.5: Schematic of designed and implemented (a) mixer and (b) balun.

Mixer

The single-balanced mixer utilized in this OPLL design is shown in Figure 5.5(a). The single-ended RF input is passed through to the mixer via an on-chip bias-tee comprised of L_1 and C_5. This is to allow the PD to be biased through the chip directly, removing the need for an off-chip bias-tee between the electronics CMOS and silicon photonic chip. The local oscillator signals are provided from an off-chip signal generator. The single-balanced mixer mixes the the RF signal down to the difference frequency between the RF and LO. Therefore, with a 28 GHz RF signal and a 27 GHz LO signal, the IF frequency should be 1 GHz. This topology results in a differential IF output, but the PFD used compares single-ended inputs. Therefore, a balun shown in Figure 5.5(b)

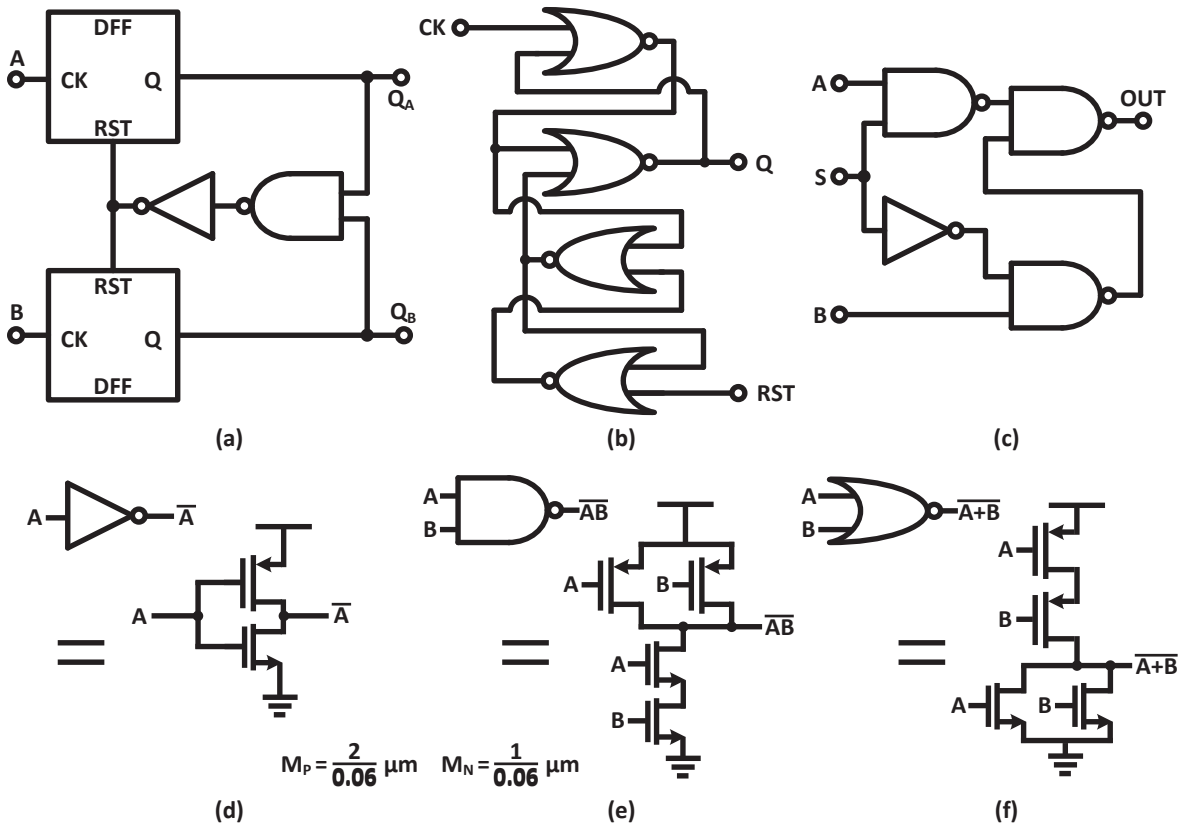

Figure 5.6: Gate-level schematics of designed and implemented (a) phase-frequency detector, (b) D-flip-flops used in the PFD, and (c) 2x1 multiplexer circuit. Additionally, transistor-level schematics are shown for the (d) NOT gate, (e) NAND gate, and (f) NOR gate.

is designed and implemented. This converts the differential input IF to a single-ended IF.

Phase-Frequency Detector

The phase-frequency detector used in this work is shown in Figure 5.6(a). This typical PFD implementation compares the arrival times of both waveforms A and B. It is best to think of these as edge-triggered flip-flops with the latch inputs tied to a logical one [94]. A gate-level schematic of the D flip-flops implemented in this work is shown in Figure 5.6(b). Additionally, the transistor-level schematics for all gates used are shown in Figure 5.6(d)-(f).

To understand the flow of the PFD circuit, begin with the scenario in which both flip-flops are reset, with Q_A and Q_B both at zero. If waveform A is leading and arrives first, Q_A will rise to a one. Then, there is a finite delay before B arrives. This will cause Q_B to rise to a one, but will immediately trigger the AND function that will reset both flip-flops, causing Q_A and Q_B to drop to zero again. This effectively caused a pulse to occur at Q_A. The longer the delay between A and B, the greater the pulse duration created. This pulse is the error correction signal that is sent out to the rest of the PLL circuitry. Similarly, if A is lagging behind B, a pulse is generated instead in Q_B. This is how the phase and frequency difference between a signal of interest and a reference signal is detected.

2x1 Multiplexer

The multiplexer (MUX) utilized in the PLL allows the UP and DN pulses to be swapped as needed depending on the polarity of K_{VCO}. Shown in Figure 5.6(c), the MUX is a straightforward implementation using logic gates. When the select bit (S) is low, A is passed to the OUT port. When the select bit is enabled, B is instead transferred to the OUT port. Using these in the PLL will increase its functionality in a wider variety of use cases.

Level Shifter

The tuning range of the PLL is directly related to the range of the output error control voltage (V_{CONT}). This is multiplied by K_{VCO} to determine the range of frequencies the VCO will be able to produce. Therefore, by converting all of the PFD signals from the 1.2 V domain to a 2.5 V domain, the PLL tuning range can be increased. Additionally, this allows the significantly faster

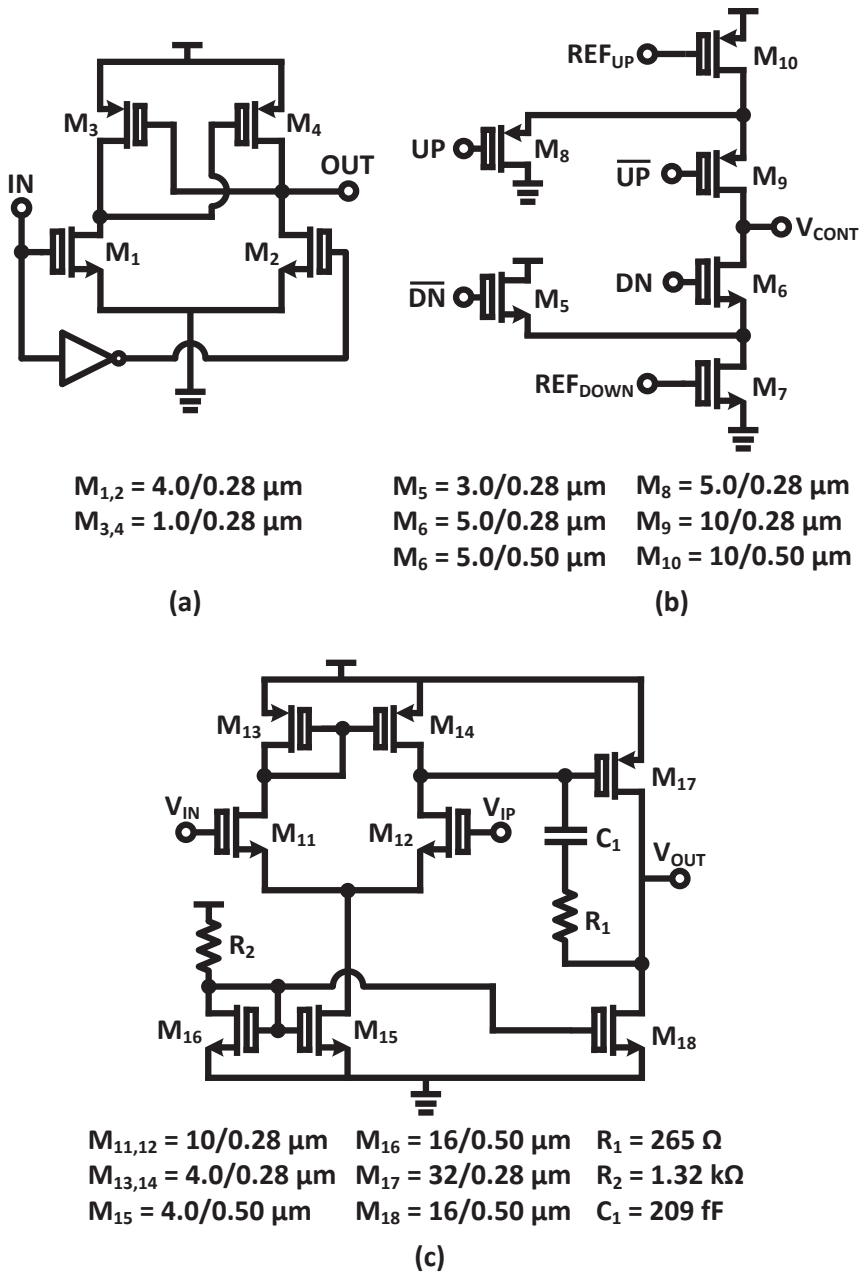

Figure 5.7: Schematics of designed and implemented (a) level shifter for converting 1.2 V signals to 2.5 V signals, (b) differential charge pump, and (c) operational amplifier circuit.

core 1.2 V devices to be used at the beginning stages that process the higher frequency RF signals, only shifting to the slower 2.5 V devices once in the lower IF frequency domain.

The level shifter circuit is shown in Figure 5.7(a). The circuit utilizes a cross-coupled pair to increase the responsiveness of the level shifter. The IN signal is a UP or DN pulse (1.2 V) output from the previously described PFD. When IN goes high, it causes M_1 to pull down the voltage at the gate of M_4, which causes M_4 to pull the OUT node to the 2.5 V supply voltage. Similarly, when IN goes low, it causes M_2 to pull down the OUT node to ground. Therefore, OUT is just a level-shifted 2.5 V version of the 1.2 V IN.

Differential Charge Pump

The differential charge pump is shown in Figure 5.7(b). Compared to a regular charge pump, this topology offers some advantages. Instantaneously cutting off the current that is injected or removed from the output V_{CONT} node, through M_9 and M_6, causes spurs and glitches in a traditional charge pump. However, in this topology, the current is is steered away from V_{CONT}, rather than being turned off and on. For example, M_{10} sources a constant dc current. When an UP pulse is sent to the charge pump, M_9 turns on and sources the same current to the output node. Once the UP pulse ends, M_9 begins turning off while M_8 begins turning off. The current sourced by M_{10} then simply steers from M_9 and is sinked to ground through M_8 instead. A similar function occurs with the DN pulses and M_5, M_6, and M_7. This gentle current steering helps prevent some of the noise glitches associated with hard cutoffs.

Operational Amplifier

Lastly, the operational amplifier (opamp) can be used at the output to drive the high-impedance piezoelectric tuning port of the laser (acting as the VCO), and is shown in Figure 5.7(c). The

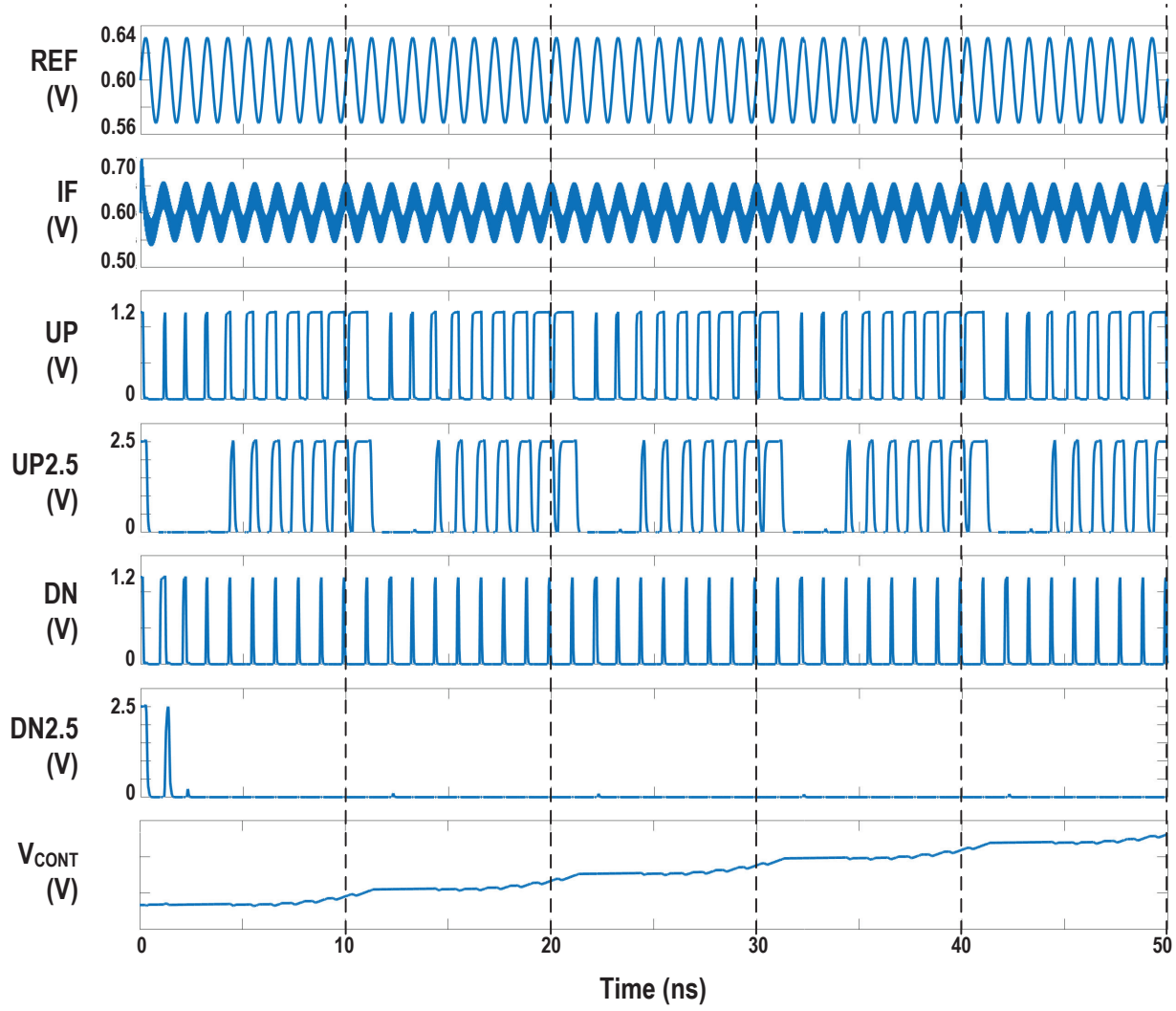

Figure 5.8: Simulated waveforms for the electronic control portion of the optical phase-locked loop. The transient simulation spans from 0 to 50 ns.

opamp is a standard differential amplifier, followed by a RC-compensated output stage to assist with stability.

System-Level Simulations and Results

In this section, layout-extracted simulations are shown to demonstrate the expected chip performance. The simulations shown are for open-loop conditions as a model of the laser is not avail-

able. The transient waveforms from the simulation is shown in Figure 5.8. The names correspond directly to the labels shown on the circuit previously in Figure 5.4.

The simulation is run with the following scenario. The input RF signal is at a frequency of 27.9 GHz and an input power of -20 dBm. This is reasonable as the single PD was capable of outputting at least -7 dBm at 28 GHz during the measurements in chapter 4. The input LO signal is at a frequency of 27 GHz and an input power of 0 dBm (before the off-chip balun). The input REF signal is at a frequency of 1 GHz and an input power of -20 dBm. Additionally, the output at V_{CONT} is driving a 10 nF capacitor.

With the described simulation scenario, the mixer down-converts the 27.9 GHz RF signal down into a 0.9 GHz IF signal through the use of a 27 GHz LO. The 0.9 GHz IF signal is compared to the 1 GHz REF signal. Assuming the PLL is driving a VCO with a positive K_{VCO}, UP pulses are expected to control the VCO to increase the RF frequency until the IF frequency approaches and eventually reaches the same frequency as REF. Inversely, DN pulses are only expected in the opposite case, when the IF frequency is higher than the REF frequency.

When viewing the simulated waveforms for the UP signals, it is evident the circuit is performing as desired. As the frequencies are offset by 100 MHz, we expect to see pulses with steadily increasing pulse duration. Ideally, there would be no DN pulses. Due to glitching during the reset of the D flip-flops, there are spikes in the DN pulses every cycle, called coincident pulses [37]. However, it is the integrated duration of the UP and DN pulses that change the output control voltage V_{CONT}, so the overall control voltage should still be increasing.

Furthermore, this issue is further remedied by the level-shifter. As the 2.5 V devices used in the level-shifter have slower responses, the undesired spikes actually get filtered out during the level-shifting, and never make it to the charge pump. However, some of the quicker desired UP pulses are filtered out as well. Again, as it is the total integration of the pulse durations that impact the control voltage, V_{CONT} should still rise, as desired.

When viewing the simulated V_{CONT} voltage, it is clear that the circuit is performing as desired and is increasing the output control voltage. While not shown here due to space concerns, the circuit also lowers the control voltage as desired when the scenario is changed to include an input RF frequency of 28.1 GHz instead. The simulated combined power consumption from all the supplies is 19.1 mW. The mixer consumes the majority of the power with 18.4 mW.

5.2.2 Optical Chip Design in AIM SiP Process

As the CMOS process used for the electronics chip does not support photonic components, a separate chip is required. The optical portion of the OPLL is fabricated on the silicon photonic (SiP) process explored in chapter 4 of this dissertation. The schematic of the optical circuit is shown in Figure 5.9. The circuit consists of two optical inputs, In_1 and In_2. The two lasers to be used in the heterodyne beat setup are input individually into these two input waveguides. The power from each laser is split into two paths. The top path leads to Out_{D+} and Out_{D-} optical outputs, and the bottom path leads to Out_{Lock} and the photodiode. The bottom path will be used in the locking, and will be discussed first.

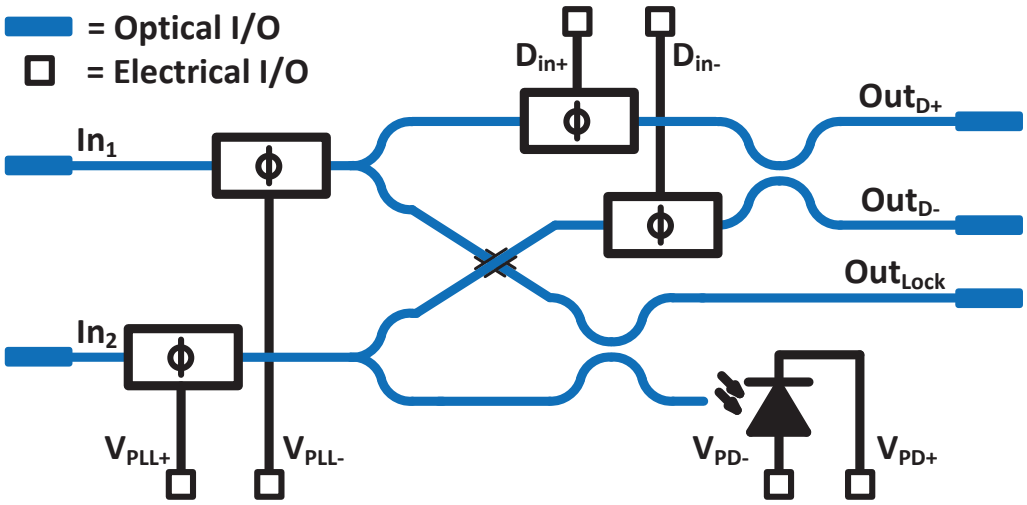

Figure 5.9: Schematic of silicon photonic circuit for OPLL.

The two optical inputs first go through optical phase shifters. In the dual-loop OPLL, the fast error-correction signal can be applied to these phase shifters to correct some of the phase error. In the single-loop OPLL, these phase shifters can be ignored. Following the phase shifters, each of the optical signals are split at Y-junctions.

In the bottom path, the 2x2 coupler combines the two optical signals, passing half of the combined signal to the output Out_{Lock} and half to the photodiode. The photodiode mixes the two optical signals, and generates the RF signal to be passed into the electronics chip for processing. This RF signal is injected into the electronics chip into the mixer and then into the PFD, as discussed in the previous section. Once the electronics compares the beat frequency to a clean reference signal, the error correction signals can be sent back to the laser piezoelectric tuning port (the only tuning port

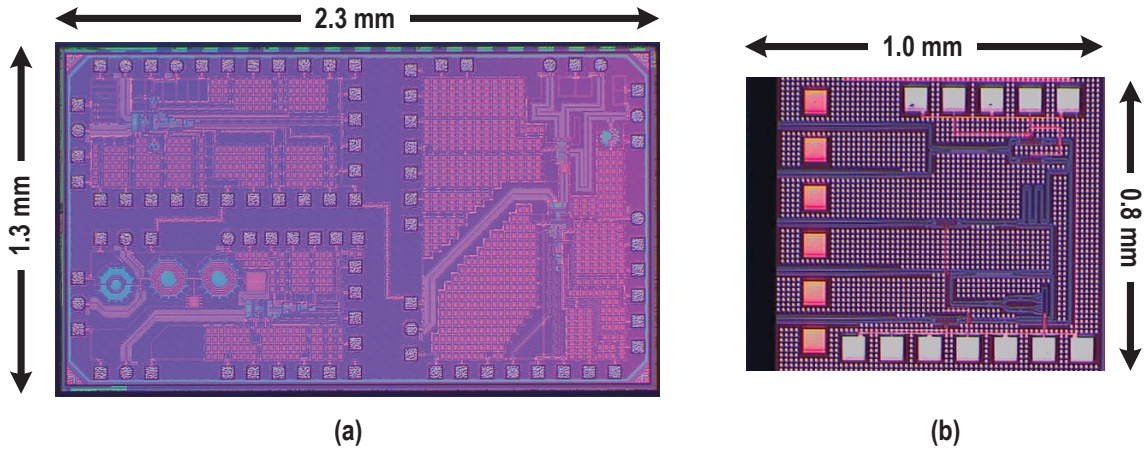

Figure 5.10: Die photo of fabricated (a) CMOS electronics chip and (b) silicon photonics chip.

in the single-loop OPLL configuration) and the phase shifters (V_{PLL+} and V_{PLL-}) on the SiP chip (only used in the dual-loop configuration).

The top path is of interest after the OPLL has been locked. The top path allows data to be phase modulated (D_{in+} and D_{in-}) onto the optical signals, which are now locked and clean, before being output through the output waveguides. This could be to a fiber for an RoF link or even to a photonically-driven emitter.

As the SiP process used is still new and developing, there were no models for simulation at the time of the design and fabrication of the chip. The PD was assumed to perform similarly to the PD structures presented in chapter 4 of this dissertation.

5.3 Integration Schemes

The integration scheme for the heterogeneous integration of the electronics and photonics chip is presented in this section. The electronics chip was designed to be usable in both a single-loop and a dual-loop OPLL. Both schemes are presented in the subsequent subsections. The die photos of both the fabricated silicon CMOS chip and the silicon photonic chip are presented in Figure 5.10(a) and (b), respectively.

Single-Loop OPLL

The proposed single-loop OPLL integration scheme is shown in Figure 5.11(a). Here, the silicon CMOS and photonic chips are heterogeneously integrated, being placed next to each other and required interconnections wirebonded. The LO and REF are supplied from off-chip sources, such as signal generators. The loop filter is included off-chip before going to the piezoelectric tuning port of the slave laser. The required opamps for both loop implementations are already included on the CMOS electronics chip.

Dual-Loop OPLL

Much of the integration scheme is similar to the single-loop architecture. However, there are some differences at the outputs of the electronics control chip. Instead, the immediate output after the first buffer (V_{UNITY}) will go through a loop filter (LF_2) to the phase shifters on the SiP chip. This control loop will correct out the faster errors as the modulation bandwidth of the on-chip phase shifters are much faster than that of the piezoelectric tuning on the laser. Then, the output of the second buffer (V_{OUT}) will act much like in the single-loop scheme and drive the piezoelectric

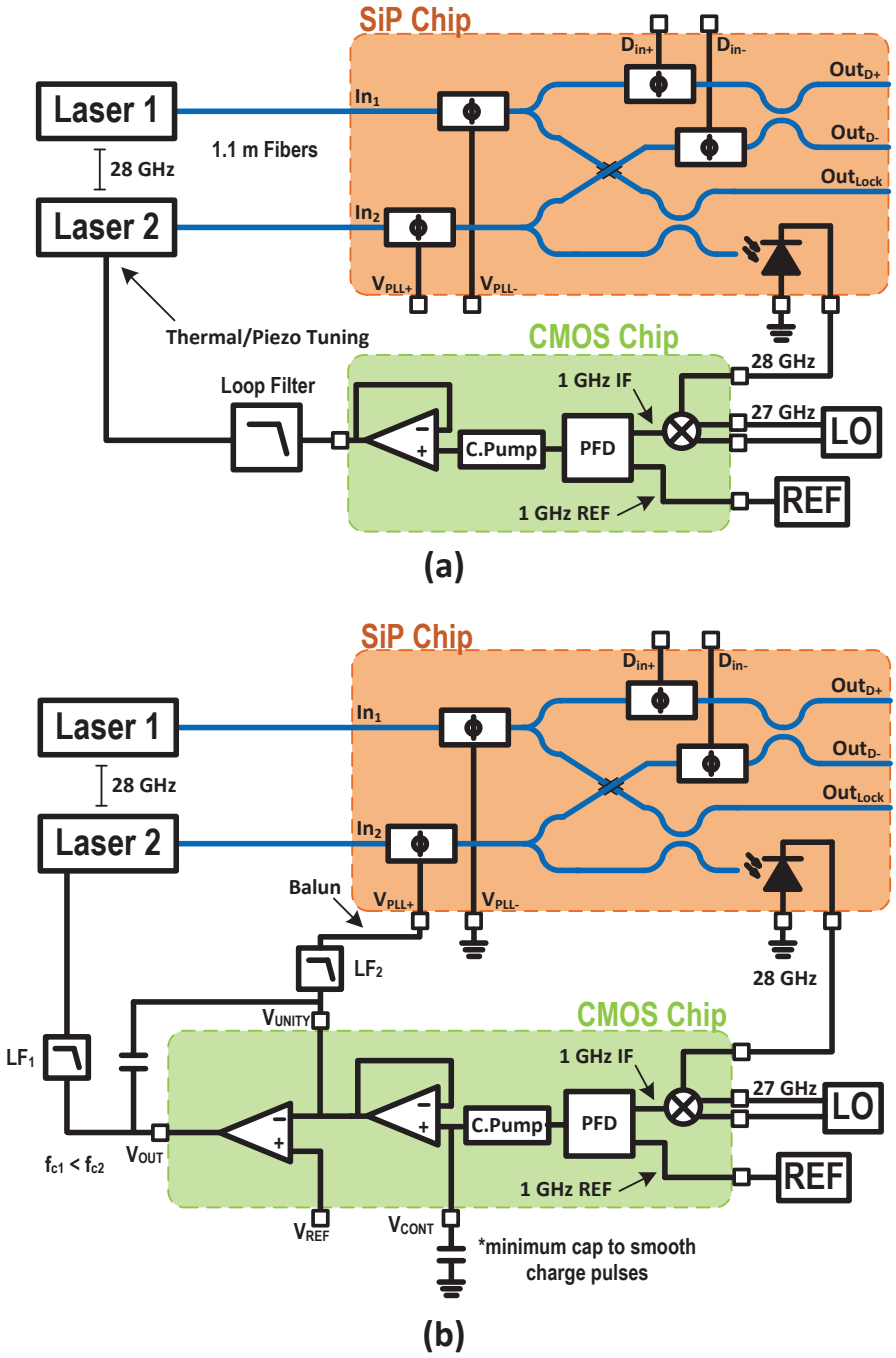

Figure 5.11: OPLL integration scheme for (a) single-loop locking as well as (b) dual-loop locking.

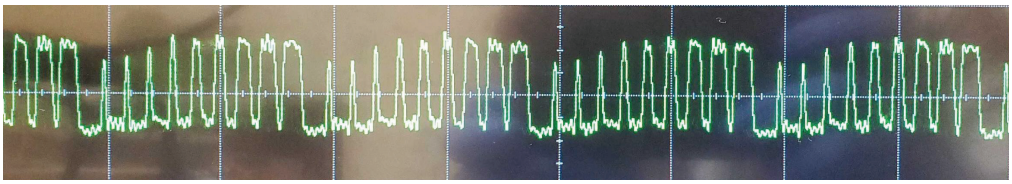

Figure 5.12: Oscilloscope shot of the buffered "UP" signals from the PLL's phase frequency detector.

tuning of the laser. The second opamp will compare the voltage at V_{UNITY} to a reference dc voltage V_{REF}. Over time, it will slowly bring V_{UNITY} back to the nominal voltage of V_{REF}, while passing the integrated correction signal to the laser via the slower loop. This will prevent V_{UNITY} from railing low or high due to long-term, slower drift. The proposed dual-locking scheme would effectively cancel out long-term drift like those due to thermal drift in the lasers via the first loop (LF_1) and additionally cancel out some of the quicker phase noise via the phase shifters as part of the second loop (LF_2). If desired, a balun could be inserted after LF_2 to increase the tuning range on the SiP phase shifters or differentially correct the two lasers, which would help balance the two lasers' input powers.

Measurements

Presently, the electronic PLL chip has been tested open-loop and results have been promising. While the design was for maximum integration, this resulted in having very few observability points. Measurements have shown that the electronic chip functions as desired, and the produced UP pulses are shown in Figure 5.12. The oscilloscope picture shows the UP pulses produced from the PFD when the IF and REF signals are at 0.9 GHz and 1 GHz, respectively. The non-uniform pulse amplitudes is due to the fact that the buffer used to observe this internal node is an open-drain

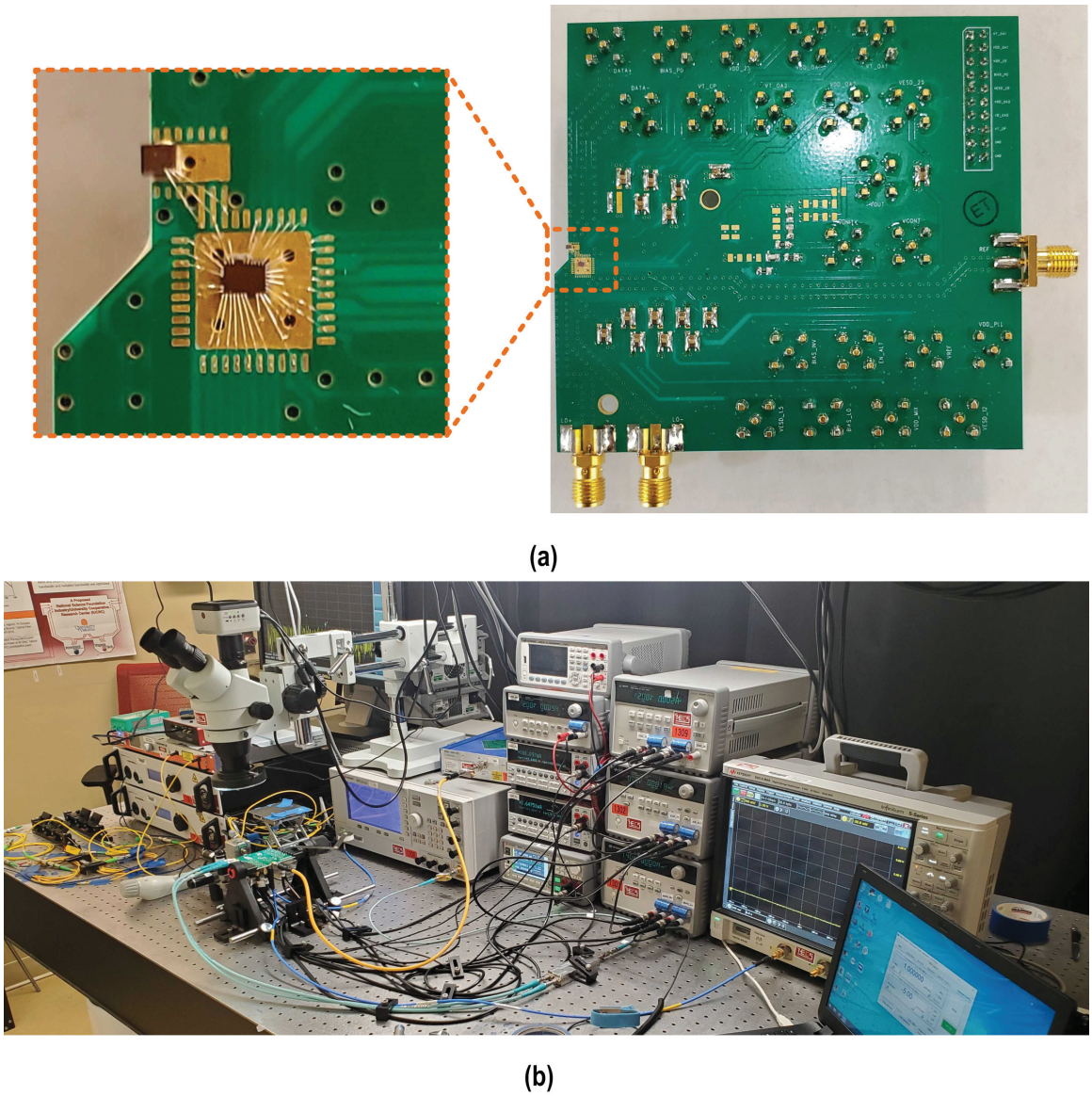

Figure 5.13: Photograph of (a) the CMOS and SiP chip integrated on test board and (b) measurement setup.

output buffer, so a bias-tee is required to bias it properly. This slight distortion is due to the bias-tees lower cutoff corner. While not pictured, it was observed that the V_{CONT} railed high when the IF frequency was lower than the REF frequency, and railed low when the IF frequency was higher than the REF frequency. This is as desired for a positive K_{VCO}.

Additionally, the CMOS and SiP chip were integrated together on board, shown in Figure 5.13(a), and the measurement setup including all the optical and electrical test equipment is shown in Figure 5.13(b). Further testing is ongoing.

5.4 Conclusions and Future Work

The design of a silicon CMOS electronics chip and a silicon photonics chip is presented. Together, these chips can be heterogeneously integrated into an optical phase-locked loop. Additionally, the on-board integration of the two chips has been completed, and full OPLL testing is underway. This OPLL would enable locking of mm-Wave beat frequencies for cleaner frequency signals and more efficient spectrum use for transmissions for RoF. Additionally, this chip-scale OPLL can help create stable frequencies for other OFS-related applications, such as metrology and spectroscopy.

Moving forward, it will be important to test the OPLL's limitations, such as in minimum RF power required for PFD functionality, determining the minimum detectable optical signal required from the lasers. Additionally, testing of the frequency is pertinent, including the range of frequencies that can be locked successfully, as well as the tunable range of synthesizable frequencies. Presently, two very clean fiber lasers are being used in the heterodyne beat, which will result in a very clean beat frequency with thermal drift compensated out by the OPLL loop. However, it may also be interesting to attempt to lock a lower quality laser, such as a semiconductor laser, to a fiber laser to not only compensate the thermal drift, but also to improve the linewidth of an inexpensive laser. This would allow the utilized RoF links to be implemented with higher cost-efficiency.

Chapter 6

Conclusions and Future Directions

6.1 Conclusions from Dissertation Research

Through the work presented in this dissertation, heterogeneous integration is explored as a solution to microwave photonic needs for next generation microwave and mm-Wave photonic links. Several generations of high-speed and low-noise photoreceivers were investigated by combining III-V photodiodes and TIAs from silicon CMOS and silicon germanium BiCMOS processes. The results demonstrate that with proper considerations taken during integration, such as ones regarding required off-chip traces and components as well as on-chip biasing solutions, highly integrated chip-scale solutions can be achieved to satisfy the needs for heterogeneous solutions to RoF and OFS requirements. Then, silicon photonic chips are explored to test and evaluate early opto-electronic components that may be used in future, highly integrated photonic circuits. Additionally, circuits

are designed in this SiP process to be used along with additional electronics designed in a Si CMOS process. When these two chips are integrated, they constitute a potential solution for chip-scale optical phase-locked loops, which have traditionally been implemented in bench-top applications. Overall, these hybrid chip-scale solutions are desirable for implementing more widespread photonic receivers and OFS systems.

6.2 Future Directions

Homogeneously-Integrated RF Photonics

While monolithic approaches are becoming popular, they are still in early stages and still do not provide the same levels of performance with regards to the photonic components. For example, silicon PDs that can be easily integrated within CMOS processes have very low responsivities. Therefore, the work presented here utilizes separate III-V chips for high-performance photodiodes. However, as heterogeneous integration processes continue to improve, it is likely that designers will be able to bond III-V chips directly to silicon CMOS chips. This would result in highly integrated hybrid solutions, with the size and complexity of a single integrated chip.

Additionally, as silicon photonic processes continue to improve, it will become possible to design photonic/electronic circuits in monolithic processes. This typically involves epitaxially growing germanium on the silicon chip. Germanium PDs can provide high performance metrics and can be easily integrated on CMOS processes. Therefore, it will be of high interest to design fully monolithic photoreceivers and OFS solutions for performance comparisons.

Foundry-Enabled High-Complexity Applications

One benefit of highly integrating the photonic and electronic components, whether through a hybrid solution or a monolithic one, is the enabling of higher complexity systems through higher device yields and integration. This could enable massive parallelization of optical channels and directly integrated electronic driver circuits, resulting in novel transmit and receiver architectures for photonically-assisted mm-Wave applications.

6.3 Other Contributions

In addition to the work presented in the previous chapters, contributions were made to other works not presented. Work was contributed towards incredibly wideband photonically-driven emitters, which converted incoming mm-Wave and even sub-Thz optical beat frequencies into electromagnetic radiation via tightly integrating high bandwidth photodiodes and high bandwidth antennas. More information about this work can be found in the following references [9, 10]:

- X. Shen et al., "High-power W-band to G-band photonically-driven electromagnetic emitter with 8.8 dBm EIRP," *2019 International Topical Meeting on Microwave Photonics (MWP)*, Ottawa, ON, Canada, 2019, pp. 1-4.

- X. Shen et al., "High-Power V-band to G-band Photonically-Driven Electromagnetic Emitters," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 2, pp. 1474-1487, Feb. 2021.

Additionally, some work involving ultra-low power wake-up receivers was pursued, including some upcoming publications. This work consisted of wake-up radios that drew very small amounts of dc power on the order of tens of nanowatts to maximize the lifetime of a event-driven system running on a battery. More information can be found in the following reference [95]:

- J. Moody et al., "An 8.3 nW -72 dBm event driven IoE wake up receiver RF front end," *2017 12th European Microwave Integrated Circuits Conference (EuMIC)*, Nuremberg, 2017, pp. 77-80.

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