RF MEMS for Cryogenic Applications

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Abstract

RF MEMS (Radio Frequency Microelectromechanical Systems) has been a rapidly expanding field for the last decade. This expansion is driven by the need for low power, high linearity and high performance devices for wireless, defense, and scientific applications. NASA has a vested interest in RF MEMS switches for signal routing and phase modulation in their next generation of Cosmic Microwave Background (CMB) measurements. Recently detected anisotropies in the polarization of the CMB by the BICEP2 detector have provided insight to the structure and energy of the inflationary period right after the Big Bang and NASA looks to expand on that success with the Beyond Einstein Inflation Probe which will map the polarization of CMB over the entire sky.

This work investigates the fabrication and reliability of RF MEMS devices as possible candidates for phase modulators operating on a satellite platform for CMB measurements at temperatures close to absolute zero. RF MEMS DC-contact series switches have been implemented from $DC - 30\,GHz$ on superconducting Nb microstrip on $5\,\mu m$ silicon-on-insulator (SOI) substrates. The devices were built using a novel fabrication process that uses the device layer of the SOI as the microstrip dielectric. Tunable resonators ($f_c = 16\,GHz$) have been designed and fabricated using the RF MEMS switches to tune f_c in $1\,GHz$ steps. RF performance of the switches and resonators are presented.

The contact resistance (R_C) when the switch is closed is also of interest because variations in R_C could introduce errors into CMB measurements. A closed-cycle cryostat has been modified to measure shifts in R_C as the devices are actuated. Reliability testing of the devices at $4\,K$ show that the devices are currently unreliable for long term operation at cryogenic temperatures, with device lifetimes less that one million contacts. Device failure is in the form of stiction, or a permanently closed switch that will no longer actuate. Charging of the substrate underneath the MEMS switch has been determined as the main cause of stiction at $4\,K$. Results and possible solutions to prolong operation lifetime are discussed.

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Chapter 1

Introduction

Microelectromechanical Systems (MEMS) technology and applications have blossomed over the past two decades. There is already a wide variety of markets into which MEMS have expanded including: sensors (accelerometers, gyroscopes, pressure sensors, etc.), printing (ink jet print heads), video (DLP projectors & TVs), wireless devices (mobile phone cameras, microphones), and scientific/defense applications (phased array radar, radio astronomy detectors)[1]. The branch of MEMS that covers wireless, radar, and radio astronomy applications is typically referred to as radio frequency MEMS (RF MEMS). The RF MEMS field is still young and overcoming various challenges such as packaging and reliability issues[2, 3, 4], however, there is growing demand for RF MEMS components that can push the bounds of what current technology is capable of achieving.

1.1 RF MEMS Technology and Applications

To the microwave engineer, the true excitement over RF MEMS stems from their ability to offer low insertion loss and high isolation while requiring virtually no power - all at a relatively low cost (before packaging)[5]. A variety of microwave circuits, including phase shifters[6], reconfigurable matching networks[7], and tunable filters[8] have all been demonstrated using RF MEMS devices. In addition MEMS fabrication techniques, known as micromachining, have been used to develop a variety of passive microwave components such as planar inductors and transformers, antennas, and guided wave structures[9, 10]. The success of these devices has led to increased interest in using MEMS (and MEMS fabrication techniques) in RF

and microwave systems. This is especially true in the field of radio astronomy where the ability of MEMS to deliver high performance at low power is useful for balloon/space based applications where power is limited by payload size restrictions.

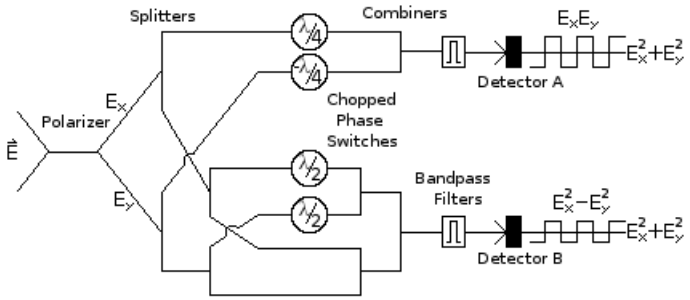


Figure 1.1: Schematic for Beyond Einstein Inflation Probe polarimeter element

1.2 Beyond Einstein Inflation Probe

One such application where RF MEMS can benefit a scientific mission is the Beyond Einstein Inflation Probe; currently under development at NASA[11]. It has the mission of studying the early universe by detecting a very faint signature in the cosmic microwave background (CMB) left over from the Big Bang. Current cosmological models of the early Universe predict a period of rapid inflation of space-time shortly after the Big Bang. It is postulated that during this expansion, gravity waves were excited that would impart a distinctive pattern on the linear polarization of the CMB. If the imprint on the polarization were to be discovered, it would have enormous repercussions on the fields of cosmology and physics by not only confirming inflation of the early Universe, but it would also provide a measurement of the energy scale of this inflation. Detecting a gravity-wave signal in the CMB is technologically challenging because the signal is faint (RMS amplitude of 30 - 100 nK) and will require very sensitive instruments to differentiate this signal from pixel to pixel on a sky map[12]. To achieve the desired sensitivity, NASA engineers have called for a satellite carrying a large antenna array of integrated polarimeters, where each polarimeter (Fig. 1.1) uses low-power,

broad-band switched signal processing on a cold focal plane. After being received by a dual polarization antenna, the polarizations are split so that RF MEMS switches can be used to phase modulate one polarization of the input signal with respect to the other polarization. The polarizations are then recombined so that three Stokes polarization parameters ($I = E_x^2 + E_y^2$, $Q = E_x^2 - E_y^2$, and $U = 2E_xE_y$) can be determined from the output of the square-law detectors. The array will be centered at three frequencies: $100\,GHz$, $200\,GHz$, and $300\,GHz$. This polarimeter design provides multiple levels of rejection against potential systematic errors. For example, the polarized signal is cleanly separated from the unpolarized signal with no mixing between Stokes parameters. This allows for detector calibration from unpolarized sources (i.e. the CMB) without requiring *a priori* knowledge of the polarization of the sky. Also, each polarimeter will be independently phase modulated so there are no common-mode sources of error (e.g a single external modulator such as a rotating half-wave plate). Finally the entire array can be fabricated on a single wafer using micromachining techniques.

1.3 Cryogenic RF MEMS

This work investigates the feasibility of using RF MEMS in phase switches that would be able to handle the switching, performance, and environmental requirements for successful operation of NASA's polarimeter-on-a-chip. A good deal of impressive RF MEMS devices have been developed at lower frequencies[6, 13, 14, 15], however, little work has been carried out at frequencies above W-Band. In addition, only some preliminary studies have been performed on RF MEMS at very low temperatures[16, 17, 18, 19] so this work will break new ground. Previous research presented by Gong et al. on cryogenic RF MEMS switches showing good performance from DC to W-band at temperatures as low as $1.6\,K$[20]. Resent results from Attar et al. show excellent performance of Au RF MEMS switches from DC to $20\,GHz$ on superconducting Nb transmission lines as well as important considerations for

proper thermal grounding of such devices during testing[21].

Building MEMS devices to operate at such low temperatures can be quite challenging. There are many phenomena to account for and obstacles to overcome. As temperatures decrease, structures undergo thermal contraction (as defined by their coefficient of thermal expansion, or CTE), which can lead to unwanted stresses in fixed-fixed beams and increase the pull-down voltage of devices[22]. Dielectrics that cover bias pads to prevent shorting are more likely to hold trapped charge which can cause shifts in pull down voltage and ultimately lead to device failure[23]. Using cantilever beams in DC-contact switches can alleviate the CTE mismatch problem as well as the need to have a dielectric layer over the bias pad.

Changes in material hardness as devices are cooled to low temperatures is another problem that could be encountered. The hardness of materials can increase causing a subsequent increase in the contact resistance of DC-Contact switches, which ultimately leads to more loss than expected within each switch[20, 24]. Contact resistance is hard to model as it is very dependent on the surface roughness of the underside of the cantilever and the region of transmission line under the cantilever contacts[24]. This is because most of the current flow occurs through asperities in the beam and transmission line that are in contact with one another. Often the contact resistance will decrease as the switch is operated through its first tens of cycles because contact forces smooth out the asperities[24]. At cryogenic temperatures, materials such as gold can harden which makes it difficult to flatten out the contacts. Fabricating contacts that are as smooth as possible and cycling the switches at higher temperatures before cryogenic testing to smooth out the contact area should help to ensure that the contact resistance remains low. Another challenge to this research will be to fabricate superconducting circuits out of Niobium. Nb is a great candidate material for these phase shifters as it superconducts at around $9\,K$, while the cryogenic probe station at UVA can reach temperatures below $4\,K$. However, one drawback is the sensitivity of the critical temperature (T_C) for superconduction of Nb (or any superconductor) to stress. Stress can be introduced in a thin film of Nb during deposition[25], resulting in a lower T_C.

Currently, effective ways of lowering stress in evaporated or sputtered thin films is to use low deposition rates and properly prepare samples so that there is no stress induced by defects in the substrate[26].

1.4 Cosmic Microwave Background Measurements

1.4.1 History of the Universe

When the universe began with the Big Bang some 13.7 billion years ago, it was an extremely hot and dense mass of exotic particles. It has been expanding ever since then, becoming cooler and more dilute over the ages. As it cooled, the particles within it combined into progressively more complex structures. When the energy of particles reached $1\,GeV$, quarks combined to make protons and neutrons. Around $1\,MeV$ (comparable to the core of a star) fusion reactions combined the protons and neutrons to make light elements like helium, deuterium, and lithium. 380,000 Years after the Big Bang, left over protons and electrons combined to form neutral hydrogen atoms. This epoch is known as Last Scattering, because neutral hydrogen gas is sufficiently transparent to light that photons ceased to scatter. This is the light that we "see" when we observe the CMB. Since that time atoms have combined into molecules, stars and galaxies, forming the universe as we see it today.

1.4.2 Inflation

The theory of an expanding universe has been well established through red-shift measurements of distant galaxies, however, there is still uncertainty about the earliest moments of cosmic history. The prevailing theory is that right after the Big Bang, the universe underwent a period of rapid inflation and then settled down to the pace that we observe today. Inflation has been used to explain why the geometry of space is Euclidean, why a faint pattern of fluctuations with amplitude almost independent of physical scale is seen in the CMB temperature, and why we do not observe relic particles such as magnetic monopoles[11].

However, to date, the scientific community has no data that measures the scale (or energy) of inflation - only models that show its effects match the scale and structure that we see in the universe today. The simplest theory of inflation predicts that it occurred when the energy of the particles in the universe was about $10^{16}\,GeV$, 12 orders of magnitude above what the Large Hadron Collider at CERN can obtain. The theory also predicts that inflation left behind ripples, or gravitational waves, with an amplitude that depends on the energy scale of inflation. It is these gravitational waves that theoretically left an imprint in the CMB polarization and the accurate detection of them is the next step in not only expanding our knowledge of the early universe, but of our fundamental physics at the highest energies.

1.4.3 CMB Polarization Generation

There are in fact many different phenomena that have affected the polarization of the CMB. At the time of Last Scattering, gravitational waves and density perturbations in the distribution of matter/energy of the universe left an imprint in the CMB. Since then, reionization, gravitational lensing, and polarized foreground emission have also affected the CMB signal. Each of these phenomena have affected the CMB in a different way, but it is easiest to understand how gravitational waves polarized the CMB by comparing them to density perturbations. As photons traveling through space-time in the early universe encountered regions of greater (or lesser) mass/energy, they would be more (or less) likely to be absorbed. Since there are anisotropies (caused by perturbations) in the matter/energy field, the anisotropies were imprinted on the intensity map of CMB radiation. When the universe became transparent at Last Scattering, photons scattered off electrons through Thompson scattering, became polarized, and remained polarized because they were free to travel unimpeded through the universe. Gravitational waves cause similar anisotropies in the CMB, however, anisotropies created by a gravitational wave have different symmetry properties than those created by density perturbations and thus, the two imprints on the CMB polarization can be distinguished[11].

The Epoch of Reionization occurred approximately 200 million years after the Big Bang, when the first stars turned on and generated enough energy to re-ionize some of the neutral hydrogen floating around the universe. This reionization freed electrons that could then scatter CMB photons, further polarizing the CMB. Additionally, the CMB polarization has been affected by matter in between the last scattering surface and the observer. Large concentrations of mass such as galactic clusters can gravitationally deflect photons as they travel past them, in a process called gravitational lensing, which changes both the temperature and polarization anisotropies. Finally, emissions from foreground stars and dust can add to both temperature and polarization anisotropies. Luckily, the effects of reionization, galactic lensing and foreground sources can be subtracted from the CMB data, however, this requires 1) precise measurements of the sky background and 2) precise maps of the known sources of anisotropies. Current scientific missions to detect and map these sources are under development, taking data, or have been completed. Recent results from the BICEP2 experiment potentially confirm the existence of B-modes in the CMB and the next phase of interest to the scientific community will be a full sky map to gain more insight into the origins of our universe[27].

1.4.4 Measuring Polarization

Three numbers are needed in order to completely characterize anisotropies in the CMB: one for the overall intensity (or equivalent temperature T) and two others to characterize the linear polarization (a degree of polarization P and angle α between the direction of polarization and some specified coordinate system). Rather than T, P, and α, it has become customary to use the Stokes parameters $I \propto T$, $Q = P\cos 2\alpha$, and $U = P\sin 2\alpha$. In principle, the fourth Stokes parameter V (which describes the circular polarization component) is needed to completely quantify the polarization, however, the process of Thompson scattering does not generate circular polarization and thus it is not expected to be detected. The Stokes parameters are also commonly defined in terms of an incident plane wave

$E = E_x \cos(kz - \omega t - \varphi_x)\hat{x} + E_y \cos(kz - \omega t - \varphi_y)\hat{y}$ where:

$$\begin{aligned} I &= E_x^2 + E_y^2 \\ Q &= E_x^2 - E_y^2 \\ U &= 2E_x E_y \cos(\varphi_x - \varphi_y) \\ V &= 2E_x E_y \sin(\varphi_x - \varphi_y) \end{aligned} \tag{1.1}$$

Each polarimeter in NASA's array will be able to independently measure the I, Q, and U Stokes parameters in the following way: If we take the upper branch of the polarimeter in Figure 1.1 and zoom in on it we can see that a polarizing element splits the signal and launches voltages in each arm proportional to the electric field amplitudes $V_x = E\cos\alpha\cos(\omega t - \varphi_x)$ and $V_y = E\sin\alpha\cos(\omega t - \varphi_y)$ where $E = \sqrt{E_x^2 + E_y^2}$ and α is the angle between the incident electric field and the x,y-coordinate system of the polarimeter. When the phase switches are off, the detector power is:

$$\begin{aligned} P_{off} &= (V_x + V_y)^2 \\ &= E^2(\cos^2\alpha + \sin^2\alpha) + 2E\cos\alpha\sin\alpha \end{aligned} \tag{1.2}$$

up to an uninteresting phase constant. When the phase switches are on, the 90° phase switch injects a phase delay of $\frac{\pi}{2}$ in the V_x arm while a -90° phase switch injects a delay of $-\frac{\pi}{2}$ in the V_y arm effectively phase shifting V_y by π in relation to V_x. Thus $V_{yon} = E\sin\alpha\cos(\omega t - \varphi_y + \pi) = -E\sin\alpha\cos(\omega t - \varphi_y)$. The detector power with the switches on is:

$$\begin{aligned} P_{on} &= (V_x + V_{yon})^2 \\ &= E^2(\cos^2\alpha + \sin^2\alpha) - 2E\cos\alpha\sin\alpha \end{aligned} \tag{1.3}$$

If the switches are allowed to chop, then the detector produces a slowly varying offset:

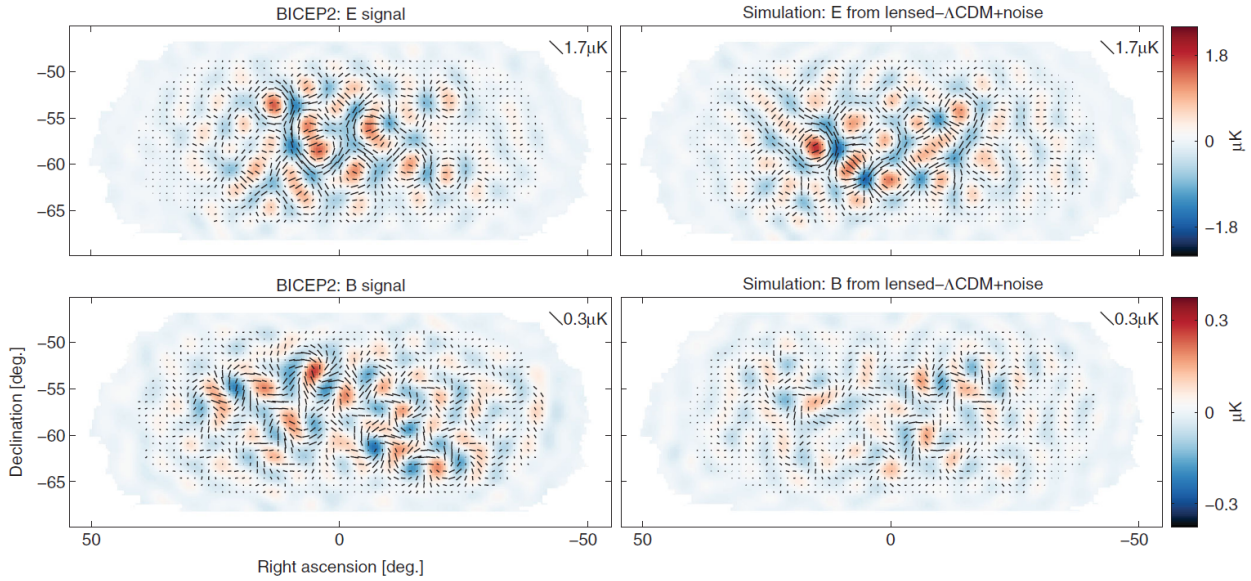
$$\begin{aligned} P_{dc} &= (P_{on} + P_{off})/2 \\ &= E^2(\cos^2\alpha + \sin^2\alpha) \\ &= E^2 \\ &= E_x^2 + E_y^2 \\ &= I \end{aligned} \tag{1.4}$$

plus a rapidly modulated term:

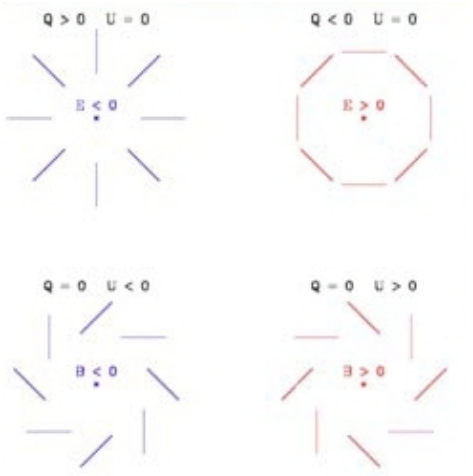
$$\begin{aligned} P_{ac} &= (P_{on} - P_{off})/2 \\ &= 2E^2\cos\alpha\sin\alpha \\ &= 2E_xE_y \\ &= U \end{aligned} \tag{1.5}$$

The beauty of this design is that it has separated the polarized and unpolarized components in a single measurement with a single detector. A similar derivation can be performed for the bottom half of the polarimeter in Figure 1.1 to show that the output from the second detector will be the Stokes I and Q parameters. It should be noted that other designs are possible utilizing different phase shifters, but the objective will still be obtained. For

example, a 180° phase shifter can be used in the V_y arm of the I/U branch instead of the $\pm 90°$ switches. By simultaneously measuring the Stokes I, Q, and U parameters, the polarimeter fully characterizes the linearly-polarized incident electric field and a full sky map can be built from this data.



(a)



(b)

Figure 1.2: (a) BICEP2 intensity map with a polarization plot overlaid showing measured E and B-modes[BICEP2]. (b) A sketch of how E, B, Q, and U are defined. Note how E and B have different properties when reflected across a line going through the centers of the pattern. E-modes have reflective symmetry while the B-modes do not[11].

Polarization maps of the sky plot the polarization of detected light in a manner similar

to the plot of a vector field, however, in a polarization plot instead of arrows, the lines are "rods" that do not point. They are meant to show the angle of polarization with respect to the reference frame of the detector. Polarization maps can be decomposed into two components in a manner analogous to the decomposition of vector maps into a gradient and a curl part. The components are called the E-mode (analog of the gradient) and the B-mode (analog of the curl). Whether or not a polarization field has an E or a B-mode is a property of the pattern of polarization rods around each point on the map and not at the point itself. Thus E and B are not a new set of variables to describe the polarization at a given point, but instead are used to characterize the polarization pattern around the point. It is the B-modes that will enable the detection of anisotropies caused by gravitational waves because the spatial pattern of those anisotropies lacks reflection symmetry and as a result the pattern of polarization rods on the sky created by a gravitational wave will have a B-mode component[11].

1.5 Phase Switches

1.5.1 Phase Switch Motivation and Theory

Phase modulation has played a crucial role in measurements of the CMB temperature anisotropy. A few modulation techniques have been explored including separating incident radiation into orthogonal polarizations, detecting these polarizations independently, and relying on rotation of the instrument with respect to the sky to fully characterize the polarized emission (WMAP [28], BOOMERANG [29]). This technique, though simple, has its drawbacks, which include requiring detailed knowledge of each detector response in order to compare the two detectors. It is also not clear whether modulation by sky rotation alone can provide enough suppression of systematic errors (Gain fluctuations, temperature drifts, and 1/f noise) to separate out the anisotropy from the sky background. Another technique to rotate the plane of polarization with respect to fixed detectors is to add a rotating half-wave

plate in front of the polarizing element (MAXIPOL [30], EBEX [31], SPIDER [32]). When it comes to small arrays, a half-wave plate can be added in front of each element, however, for larger arrays (like the one required to detect gravity waves) the dissipated power from each element becomes too large for the cold stage to properly cool. A solution to this problem is to place a single device, such as a ferrite rotator, in the optics away from the cold stage. However, this means the half-wave plate must operate at warmer ($4\,K$) temperatures where the effects of insertion loss can be three orders of magnitude larger. Furthermore, thermal emission or reflected light associated with an external modulator will produce a common-mode error that will not average down with multiple detectors.

This work contributes to the development of microstrip polarization modulation techniques for the next generation of CMB measurement instruments. The polarimeter-on-a-chip design will incorporate multiple features to suppress systematic errors in order to extract the CMB anisotropy from the background signal. RF switches will be used to achieve polarization modulation within each element in the array by injecting a half or quarter-wave phase delay into one arm of the polarimeter. Each polarimeter is independently modulated so that residual uncertainties will average down as multiple detectors are added. Polarization modulation allows instantaneous measurement of three Stokes parameters (I, Q, U) in each pixel with no information lost, leading to complete characterization of the polarization of the CMB. RF MEMS phase switches dissipate very little power, allowing the entire array to be fabricated on the same wafer as the detector and operate on a single $100\,mK$ stage. This is an important advantage for balloon or space-born instruments. Finally, microfabrication techniques will ultimately allow the entire polarimeter (including the antenna, microstrip, phase delay circuit and detector) to be built without the need for hand fabrication resulting in the entire device being repeatable from pixel to pixel.

1.5.2 Phase Switch Performance

The radiation spectrum of the CMB follows a black body curve which peaks at around 160 GHz but is measurable over a broad band ranging from 30 to 300 GHz[11]. Ideally, any polarization measurement would want a single system that could span this bandwidth, however in practice this is extremely difficult to achieve. Ultimately the CMB band will be broken down into multiple smaller sub-bands over which individual measurements will be taken. Since the cryogenic MEMS phase switches being developed in this research are a new technology, a phased approach is being taken starting with development of 90° and 180° phase switches at 40 GHz. Ultimately phase switches will need to be designed and tested up 300 GHz, however, such work will be beyond the scope of this research. The devices developed in this research will be considered proof-of-concept, and the work of integrating phase shifters into a polarimeter-on-a-chip will also be left for future work.

1.5.3 Insertion and Return Loss

Performance requirements for insertion loss across the band of the phase shifters is dictated by the sensitivity goals of a space-based satellite mission to measure the polarization of the CMB. The B-mode CMB signal strength is expected to be 30 - 100 nK, thus the polarimeter array must be sensitive on the $\sim 15\,nK$ level. The sensitivity ΔT of a radiometer can be shown to be[33]:

$$\Delta T = (T_A + T_{Rec})/\sqrt{B\tau} \tag{1.6}$$

where T_A is the noise temperature of the antenna, T_{Rec} is the noise temperature of the receiver subsystem, B is the bandwidth over which the signal is detected and τ is the integration time over which the measurement is taken. Equation 1.6 holds for a single antenna/receiver system. An array of N detectors can be used to average the signal and increase the sensitivity by a factor of $\sqrt{N}$[34]. Thus for a 3000 element array, each individual polarimeter in the

Beyond Einstein Inflation Probe must have a sensitivity of $\Delta T \sim 1\,\mu K$. This is no easy task and it requires every component of the polarimeter to be as noiseless as possible. Although the exact design for the polarimeters has not been completed, a reasonable estimate for ΔT can still be calculated based on mission specifications from the Primordial Anisotropy Polarization Pathfinder Array (PAPPA)[12]. PAPPA is a balloon-borne experiment designed to test technology for use in the Beyond Einstein Inflation Probe by measuring the CMB over three bands using 32 polarimeters similar to those described in this work (although initial flights have used a half-wave plate instead of MEMS phase switches to accomplish phase modulation). According to Equation 1.6, for a $40\,GHz$ bandwidth centered at $200\,GHz$ and an integration time of $100\,s$ (Two times longer than PAPPA mission specifications), the noise temperature of an individual antenna/polarimeter must be approximately $1.6\,K$ (or better) in order to obtain the desired sensitivity mentioned above.

Equation 1.6 also states that the antenna temperature contributes to part of the sensitivity and needs to be determined in order to limit the noise contribution from the receiver system. To start, the noise temperature of the antenna is governed by the antenna's radiation pattern $R(\theta, \phi)$ and the temperature distribution $T(\theta, \phi)$ that the antenna "sees". Equation 1.7 shows how the antenna noise temperature can be calculated by averaging the temperature distribution weighted by the radiation pattern over all space (in spherical coordinates).

$$T_A = \frac{1}{4\pi} \int_0^{2\pi} \int_0^{\pi} R(\theta, \phi) T(\theta, \phi) sin\theta d\theta d\phi \tag{1.7}$$

On PAPPA, an off-axis primary mirror is used to focus light onto the cryogenic focal plane where an array of corrugated feed horns couple the light onto the polarimeters. The feed horns are highly directional with a coupling efficiency of ~ 0.95 so that the antenna pattern of the polarimeter is almost completely filled. The beamwidth of the Beyond Einstein Inflation Probe will measure a 1° square patch of sky[11], and it is safe to assume that the antenna pattern over that small patch is a constant, $R(\theta, \phi) \sim 0.95$. The temperature distribution of

the sky is roughly a constant $T(\theta, \phi) = 4\,K$. Integrating these values in Equation 1.7 yields $T_A = 72.3\,\mu K$, which overall is a small proportion of the overall noise in the system.

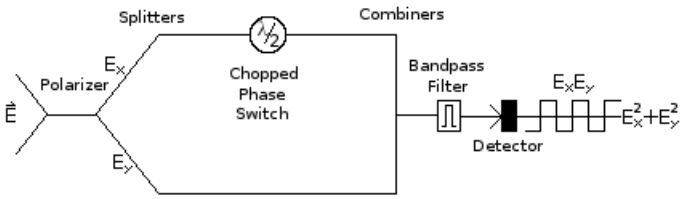


Figure 1.3: Components in one arm of the polarimeter

The receiver chain (Fig. 1.1) is composed of splitters, phase shifters, filters and detectors. If we look at one branch (Fig. 1.3), we can see what will contribute towards the noise measured in a single detector. There are two paths: The $E_{\rm y}$ path, which is composed of two splitters before it rejoins the $E_{\rm x}$ path, composed of two splitters and a phase switch, at the combiner. If we assume the splitters and combiners are matched at each port and evenly split power between ports 2 and 3, then we can treat these two paths as separate cascades of two-port networks and we can use Equation 1.8 to calculate the noise contribution from each branch[35].

$$T_e = T_1 + \frac{T_2}{G_1} + \frac{T_3}{G_1 G_2} + ... + \frac{T_N}{G_1 G_2 ... G_N} \tag{1.8}$$

T_N is the equivalent noise temperature and G_N is the gain of the Nth component in the cascade. For the $E_{\rm Y}$ path, the splitters and combiner are all assumed to be 3-dB couplers. The noise temperature of a passive, two-port network (such as a phase switch, coupler, or filter) can be shown to be[35]:

$$T_e = \frac{1 - G_{21}}{G_{21}} T \tag{1.9}$$

where $G_{21}$is the ratio of power available from the network to power available from the source

and T is the physical temperature of the network. If the network is matched (a safe assumption in this case) then $G_{21} = |S_{21}|^2 = 0.5$ for the couplers. For the E_{y} path, the equivalent noise temperature of each component is $T_{e-coupler} = (1 - 0.5)/0.5 * 100\ mK = 100\ mK$. Using Equation 1.8, $T_{e_y} = 100\ mK + 200\ mK + 400\ mK = 700\ mK$. For the E_{x} path, we have two splitters, the phase shifter, and the combiner. If the insertion loss of the phase shifter is better than $1\ dB$ ($|S_{21}| > 0.794$), then the maximum noise temperature of the phase shifter is $T_{e-phaseshifter} = 42\ mK$ and we can calculate $T_{e_x} = 100\,mK + 200\,mK + 168\,mK + 504\,mK = 0.972\,K$. The combiner will add these two noise sources so that the total noise seen at the input of the filter is $T_{e_y} + T_{e_x} = 1.672\,K$. The maximum equivalent noise temperature of a filter with $-0.5\,dB$ ($|S_{21}| > 0.897$) of ripple in the passband is $T_{e-filter} = 26\,mK$. Again using Equation 1.8 we can finally calculate T_{Rec}:

$$T_{Rec} = (T_{e_y} + T_{e_x}) + \frac{T_{e-filter}}{G_{y+x}} + \frac{T_{e-Detector}}{G_{y+x}G_{filter}} \tag{1.10}$$

where $G_{y+x} = 0.224$ is the total gain of the components before the filter. $T_{e-Detector}$ is the noise temperature of the detector, which is expected to be a microbolometer similar to devices that have flown on PAPPA with a reported noise temperature of $0.4\,\mu K$[12].

Using these values, we see that $T_{Rec} = 1.672\,K + 0.116\,K + 2\,\mu K = 1.782\,K$, which means that each polarimeter has a sensitivity $\Delta T = 0.89\,\mu K$ and the entire array of 3000 elements is sensitive to $\Delta T = 15\,nK$. We can see that the noise contributed from the phase shifter with $1\,dB$ of insertion loss is approximately ${}^{0.168\,K}/_{1.782\,K} \sim 10\%$ of the entire receiver chain. There is little room for additional loss as a phase shifter with $2\,dB$ of insertion loss will decrease the sensitivity by 7%. We must also keep in mind the assumption that the phase shifter was well matched to the rest of the system, a valid assumption if the return loss is kept above $10\,dB$ across the entire band.

1.5.4 Phase Performance

The ability of the polarimeter array to successfully detect B-modes in the CMB is not only limited to the sensitivity of the array, but it is also limited by the accuracy of the phase modulation it can perform. It is an extremely difficult task to design a phase switch that can inject exactly 90° or 180° of phase over the entire bandwidth, however, by taking a second look at the derivations in Section 1.4.4, we can gain an understanding of the bounds we can put on the phase performance that will yield as small an error as possible in the final read-out of the system. This can be done by recalling the voltages launched in each arm of the polarimeter:

$$\begin{aligned} V_x &= E\cos\alpha\cos\beta \\ V_y &= E\sin\alpha\cos\beta \end{aligned} \tag{1.11}$$

where $\beta = \omega t + \phi$. In Section 1.4.4, the phase switch shifted the phase of the V_y arm by π so that $V_{y_{on}} = -E\sin\alpha\cos\beta$. What if the phase error introduced by the phase switch was $\pm 5°$ so that for example $V_y = E\sin\alpha\cos(\beta + \pi + {}^{\pi}/_{36})$ when the phase switch was on? The power measured in the detector when the switch is off would remain the same (Eq. 1.2). However, with the switch on:

$$\begin{aligned} P_{on} &= (V_x + V_{y_{on}})^2 \\ &= E^2(\cos^2\alpha\cos^2\beta + \sin^2\alpha\cos^2(\beta + \frac{37\pi}{36}) && (1.12) \\ &\quad +2\sin\alpha\cos\alpha\cos\beta\cos(\beta + \frac{37\pi}{36})) && (1.13) \end{aligned}$$

For simplicity, we can examine the case when $\beta = n\pi$ for $n = 0, 1, 2, ...$

$$P_{on} = E^2\left(\cos^2\alpha + \sin^2\alpha\cos^2(\frac{\pi}{36}) - 2\sin\alpha\cos\alpha\cos(\frac{\pi}{36})\right) \quad (1.14)$$

$$P_{dc} = (P_{on} + P_{off})/2 = I$$

$$\sim E^2\left(0.9962 + 0.0028\cos^2\alpha + 0.0038\sin\alpha\cos\alpha\right) \quad (1.15)$$

$$P_{ac} = (P_{on} - P_{off})/2 = U$$

$$\sim E^2\left(1.9962\sin\alpha\cos\alpha - 0.0038\sin^2\alpha\right) \quad (1.16)$$

Comparing P_{dc} and P_{ac} to a polarimeter with an ideal phase switch, we can see there is a small error in the measurement of I and U. The angle α is the angle between the incident electric field and the antenna which for a linearly polarized signal will be fixed in time so that the largest deviation P_{dc} and P_{ac} will have from $P_{dc-ideal}$ and $P_{ac-ideal}$ will be $(1-0.9962) \sim 0.5\%$. This correlates to a noise temperature of 1.5 - 5 nK for a 30 - 100 nK signal, thus it can be seen how it is desirable to keep the phase error of the phase switches to $\pm 5^\circ$.

1.6 RF MEMS Switches

It is believed that RF MEMS switches have the performance capabilities necessary to keep the systematic errors of the phase switches below acceptable levels. RF MEMS switches can either be inserted into the phase switch circuits as series or shunt switches and they can be implemented as a direct-contact (DC) or capacitive switch. In the DC configuration, a cantilever is suspended above a transmission line, leaving a gap in the circuit. When a bias is applied to a pad under the cantilever, charge buildup causes electrostatic attraction between the cantilever and the bias pad, pulling the beam down so that the tip contacts the transmission line, closing the circuit. DC contact switches offer high isolation in the open (or up) state and low insertion loss in the closed (or down) state. They can be used in series to switch on or off a particular section of circuit, or they can be used in shunt to switch

in a load. DC contact switches are prone to failure through stiction, where the cantilever sticks to the bias pad permanently, rendering the device inoperable. Capacitive switches are typically implemented by placing a fixed-fixed beam above the transmission line in a shunt configuration. In the up-state, the switch will have a capacitance governed by the area of the beam over the transmission line and the gap separating the beam and the transmission line. A dielectric can be placed over the transmission line to prevent the switch from shorting which will also affect the capacitance. When the switch is pulled down, the gap separation becomes smaller, increasing the capacitance of the switch. A figure of merit of capacitive switches is their capacitance ratio ($\frac{C_{down}}{C_{up}}$), which can reach values typically ranging from (but not limited to) 1 - 100. Capacitive switches are also prone to stiction, however this effect can be mitigated by fabricating posts on the underside of the beam, reducing the area that contacts the transmission line in the down state. Shunt capacitive switches can be used to simply load a transmission line or can even be used modify the capacitance per unit length of a transmission line.

Fixed-free cantilever beams are used in this work because of their low insertion loss and high isolation properties. A dimple can be added to the tip of the beam which acts as a stand-off that will prevent the beam from contacting the actuation pad during switching. This eliminates the need for a dielectric covering the bias pad to prevent electrical shorts and simplifies the fabrication process. The cantilevers can be described by a circuit model, as shown in Figure 1.4. When a voltage is placed between the actuation (or bias) pad and the cantilever, charges of the opposite polarity build up on the cantilever and actuation pad respectively, which causes an attraction between the cantilever and the actuation pad. The cantilever deflects, closing the circuit when the tip of the beam touches the contact transmission line. The parameters of interest in a RF MEMS device are the overall up-state capacitance ($C_{up} = C_1 + \frac{C_2 C_3}{C_2 + C_3}$) and the downstate contact resistance R_C. C_{up} is a measure of how close to an open circuit the MEMS bridge is in the on-state, while R_c is a measure of how close to a short circuit the bridge contact is in the down-state.

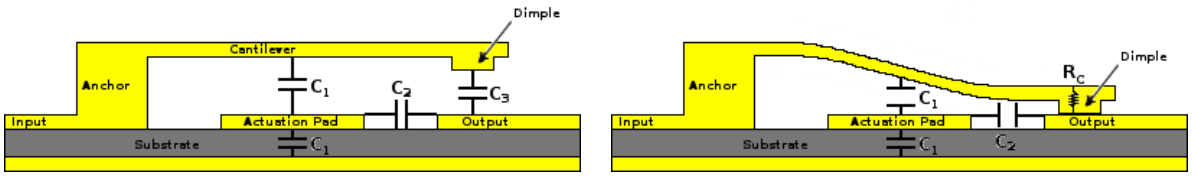


Figure 1.4: Cross-section of the cantilever shows the electrical model.

To first order the beam can be approximated as a parallel plate capacitor, and thus the up-state capacitance is a function of the distance between the cantilever tip and the transmission line the tip will contact when the beam is pulled down. It is also a function of the overlapping area between the tip and transmission line. To achieve the up-state capacitance required for the phase switches, the beam must be relatively high off the substrate, and the tip area overlapping the transmission line must be small.

The last parameters of the beam to be determined are its length and the size of the bias pad needed to pull the beam down. These dimensions govern the pull-down voltage, or the voltage at which the electrostatic force on the beam overcomes its restoring force and pulls the switch to the bias pad. It can be shown that this occurs when the beam is at $\frac{2}{3}$ of the initial height of the beam. A fairly good approximation of the pull-down voltage is found to be[36]:

$$V_P = \sqrt{8k_m g_o^3/(27\epsilon_o LW)} \tag{1.17}$$

where k_m is the spring constant of the beam, L is the length of the bias pad and W is the width of the beam (and bias pad). Often stand-offs, or dimples, are used to prevent the beam from collapsing onto the bias pad. It is important to note that Equation 1.17 is an approximation because it neglects fringing fields at the edges of the cantilever and the actuation pad and often electromechanical simulators are employed to fine tune designs. The spring constant of a fixed-free cantilever with thickness t, width w, and modulus E is shown

in Equation 1.18.

$$k_m = \frac{2EW}{3}\left(\frac{t}{l}\right)^3 \tag{1.18}$$

Another important parameter that is determined by the beam dimensions is the pull-out voltage V_{PO}, also known as the hold-down voltage. This is the voltage at which the restoring force of the beam becomes greater than the force exerted by the electric field applied at the bias pad. When the voltage drops below V_{PO}, the beam is released from the contact and the switch is opened. To estimate V_{PO}, we can assume that the beam is in a pinned configuration with just enough bias so the dimple touches the contact but does not pull the beam down any further. At this point the beam is in equilibrium and the electric force F_e is equal to the restoring force F_k:

$$\frac{1}{2}\frac{dC(g)}{dg}V_{PO}^2 = k_m \Delta g \tag{1.19}$$

where $C(g)$ is the capacitance between the bias pad and the beam as a function of height g, and Δg is the displacement of the beam tip from its initial height before being pulled down. We can treat the cantilever-bias pad system as a parallel plate capacitor thus,

$$C(g) = \frac{\epsilon_o W x}{g} \tag{1.20}$$

where x is the length of the actuation pad underneath the beam. Substituting Equation 1.20 into Equation 1.19 and solving for the hold down voltage yields:

$$V_{PO} = \sqrt{\frac{2k_m}{\epsilon_o W x} g^2 \Delta g} \tag{1.21}$$

Again, Equation 1.21 neglects the fringing fields at the edges of the beam and bias pad and

thus is an approximation of the hold-down voltage. A further approximation can be made when dimples are used; in which case the dimple height defines Δg as the tip displacement of the beam when it is in contact. Since the beam is not flat when pulled down, $g = g(x)$ but we can approximate this as Δg as long as the bias pad is close to the end of the cantilever. In this case Equation 1.21 becomes:

$$V_{PO} = \sqrt{\frac{2k_m}{\epsilon_o W x}\Delta g^3} \tag{1.22}$$

1.7 Focus of This Work

This work has three significant goals. The first is to develop a fabrication process that integrates MEMS fabrication techniques with SOI technology to realize MEMS devices on SOI substrates. A subset of this goal is the fabrication of Nb microstrip lines in place of traditional Au lines. The use of SOI as a microwave substrate is not a new concept[38] and various RF MEMS switches have been built using SOI[39, 40, 41], but this research is (to the best of the Author's knowledge) the first time an RF MEMS switch is implemented on a microstrip transmission line using SOI as dielectric. The second goal will be the characterization of RF MEMS devices fabricated on Au and Nb transmission lines using the new fabrication process to verify that it is capable of producing viable devices. Finally, a study of the reliability of RF MEMS devices at cryogenic ($4\,K$) temperatures and the challenges associated with operating MEMS in such environments will be investigated. To the best of the author's knowledge there is no data on device lifetime and failure mechanisms of RF MEMS switches operating in the liquid helium regime.

Chapter 2

Phase Switch Fabrication

The fabrication of low-loss, reliable RF MEMS switches on superconducting Nb transmission lines requires the integration of an already complex MEMS process[20] with Silicon-on-Insulator (SOI) technology[37]. This would ensure that our devices would be compatible with the 5 μm SOI substrates that NASA uses in their detectors[42] and the Al process was chosen so as to best reduce stress due to a CTE mis-match between the sacrificial layer and the beam[43]. Furthermore, the MEMS process required some changes in order to accommodate Nb (as opposed to Au) transmission lines. This chapter serves to give an overview of the final fabrication process and to highlight the challenges that were encountered building MEMS devices on superconducting circuit lines on top of a SOI substrate. A discussion of solutions to fabrication challenges as well as techniques that did not provide acceptable results are also presented.

2.1 Overview of Fabrication Process

The process steps for the fabrication of MEMS on SOI are outlined in cross-sections in Figure 2.1 and detailed process sheets can be found in Appendix 6.1. SOI is an excellent microwave substrate offering low loss and high isolation, provided the resistivity of the device layer is sufficiently high[44]. Furthermore, the conductivity of Si decreases with temperature leading to carrier freeze-out and resulting in less loss at cryogenic temperatures[45]. High resistivity SOI substrates are readily available and relatively cheap

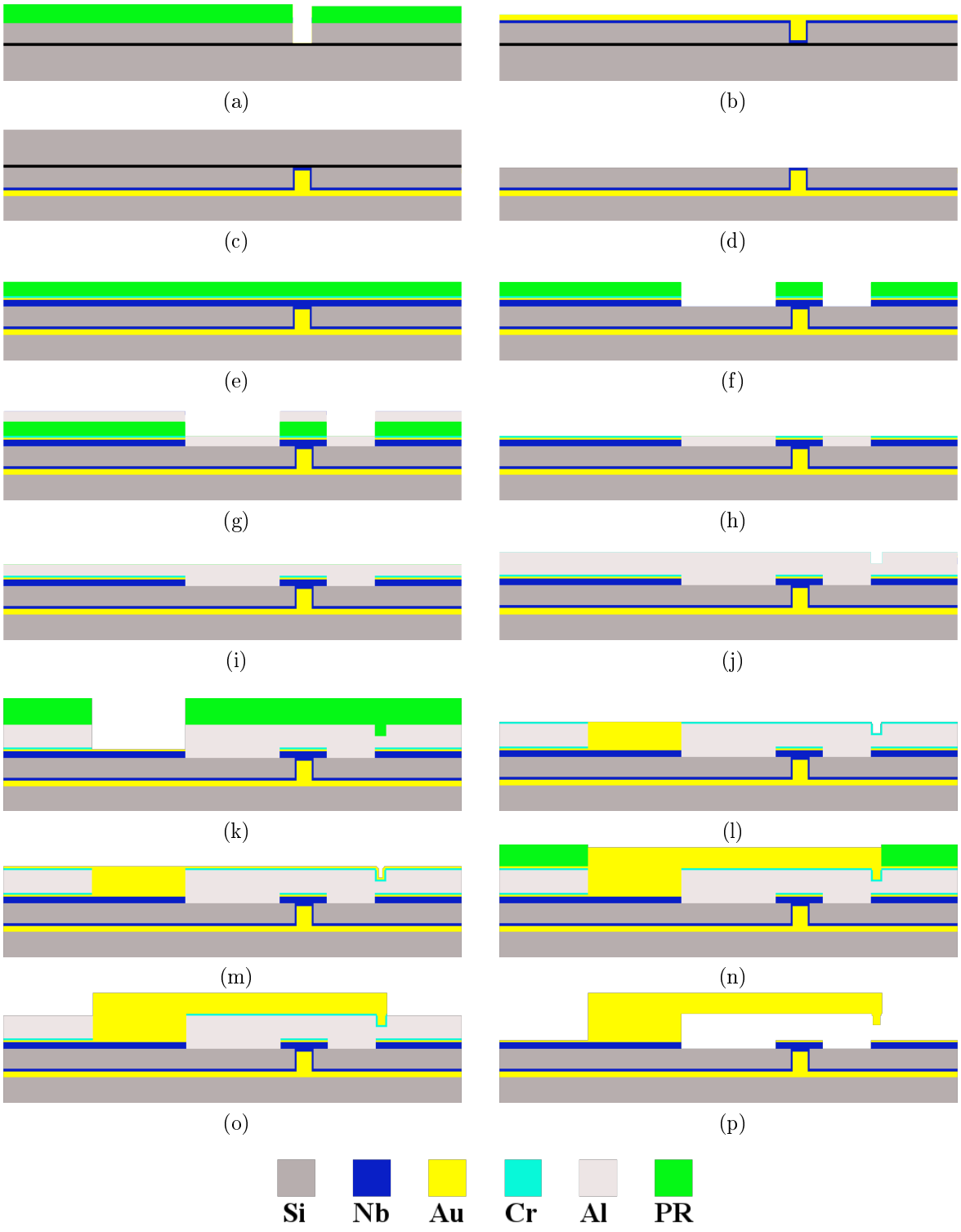


Figure 2.1: SOI fabrication process for RF MEMS Phase Switches

to manufacture, and the substrates used in this research have $\rho > 5\,k\Omega cm$. The fabrication process begins by reactive ion etching (RIE) vias into the Si device layer of a 2-inch SOI wafer (Figure 2.2) and then sputtering a 4000/300 Å Nb/Au ground plane. The Au serves as a seed layer for electroplating 3 μm of Au to form beam-leads for clamping fully released SOI chips into waveguide test blocks and for filling the vias that connect the transmission lines to the substrates. After the beam-lead electroplating (Figure 2.1b), the Nb/Au seed layer is etched away

forming the outline of the beam-lead-plated chips. Next, the SOI is bonded to a 3 inch Si carrier wafer (Figure 2.1c), the handle Si is diced down to about 50 μm and the remaining Si and buried oxide is RIE etched away (Figure 2.1d). Following this is the circuit layer metal deposition consisting of a 4000/300/600 Å stack of Nb/Au/Cr (Figure 2.3). The Cr serves two purposes: first, to provide a diffusion barrier to Al (the sacrificial layer) to keep it from contaminating the Au and the second, to provide an etch-stop for the anchor etch (described below). This metal stack is RIE etched (Figure 2.1f) to form the transmission lines and bias pads and then an 4500 Å Al lift-off step is performed to planarize the sample (Figure 2.1g). The next 6000 Å of Al sacrificial layer is evaporated (Figure 2.1i) and then the wafer is patterned for dimple lift-off. Another 6000 Å of Al is evaporated and lift-off of the resist leaves dimples in the Al layer (see Figure 2.1j). Next the wafer is patterned for

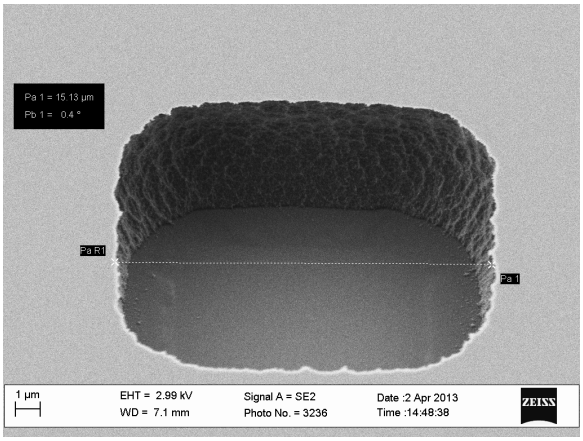
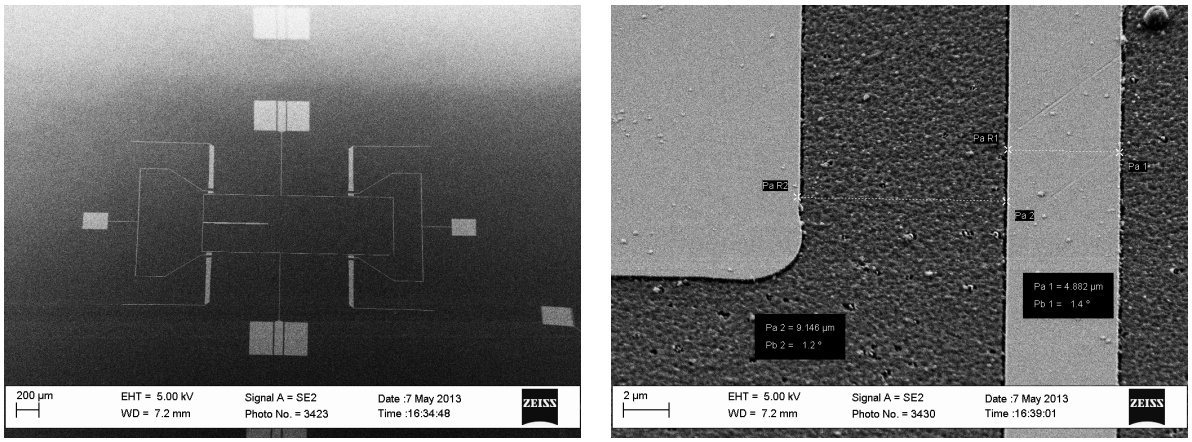


Figure 2.2: Via etched by RIE



(a) (b)

Figure 2.3: Circuit layer liftoff planarization. The light areas are Nb/Au/Cr while the darker areas are Al.

the anchor etch, which consists of Al/Cr RIE followed by a quick Al wet etch to clean up any residuals left from the RIE (Figure 2.1k). The photoresist is stripped and the anchors are electroplated up 1.2 μm so they are planar with the top Al layer. A 500 Å Cr diffusion layer is sputtered and patterned to open up a whole in it to expose the anchor Au (Figure 2.1l). This barrier prevents the diffusion of the Al in the sacrificial layer into the Au beam which will decrease the conductance of the beam lowering device performance[46]. Next, an Au seed layer is sputtered over the sample and the beams are electroplated to their final thickness of 2.2 μm (Figure 2.1o). The Au seed layer is etched away (Figure 2.4) and at

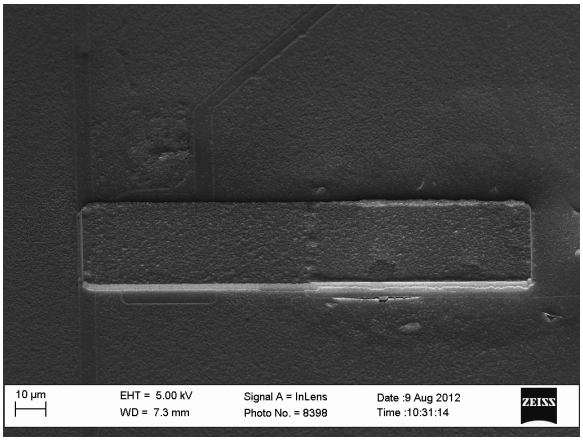
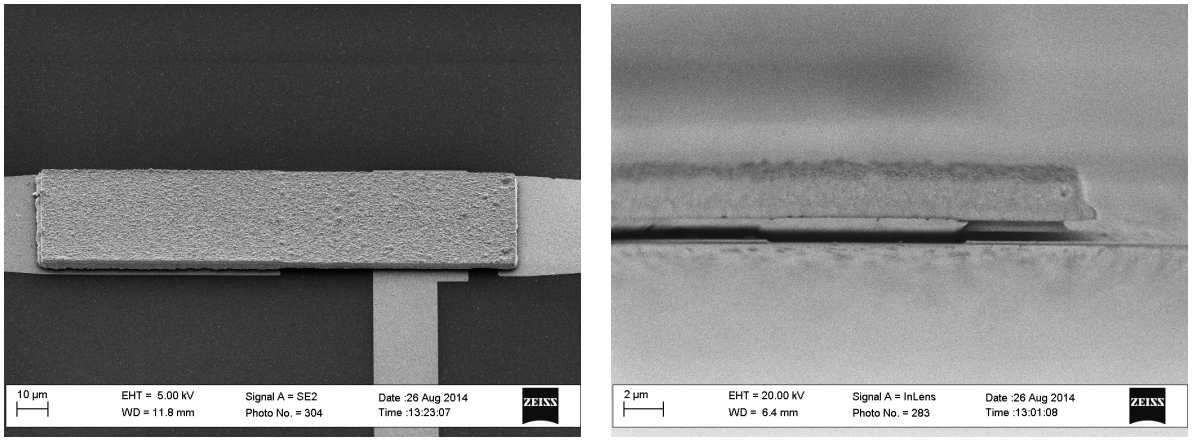


Figure 2.4: Electroplated MEMS beams before sacrificial layer removal.

this point the sample is diced to separate the devices to be probed from devices to be tested in waveguide. The waveguide chips, being processed separately at this point, are patterned with a Cr wet etch followed by an Al/Cr/Si RIE to define the outline of the chips and removed from the carrier. Both the waveguide chips and on-wafer devices have the Cr/Al sacrificial layer removed through a series of wet etches and then are dried in a critical point dryer (CPD) to prevent stiction of the MEMS to the substrate (Figure 2.1p)[47]. After release the devices are plasma cleaned and inspected by SEM to make sure all metal was removed from underneath the beams and that there was no debris left over from the fabrication process that would impede device performance. The development of a fabrication process for microelectronic devices is never straightforward. A brief description of the major challenges that were encountered during development of this process is given in the following sections.



(a) (b)

Figure 2.5: Released MEMS cantilever.

2.2 SOI Adhesion

One of the biggest problems to plague the RF MEMS phase switch fabrication in this research was the bonding of the SOI device layer to its carrier wafer. The MEMS processing on the backside of the SOI involves two lift-off processes and there are multiple lithography steps, all of which were found to attack the adhesion between the epoxy and waferbond used to hold the two wafers together. Unfortunately these steps were necessary to bring the fabrication process to completion and could not simply be removed from the process flow.

Delamination at a polymer-polymer interface can occur for various reasons[48]. In general a polymer is comprised of chains of organic molecules that are interwoven together. The covalent bonds within these molecules combined with the density of the entangled molecule chains is what gives the bulk polymer its strength. When an interface is formed between two polymers these chains become intertwined through diffusion across the interface and in some cases chains can even bond covalently[49]. Small gaps can also form if molecular chains fail to penetrate the material on the opposite side of the interface due to poor solubility in that material, weakening the interface. When the interface is stressed, crazing can occur. Crazing is the formation of micro-cracks formed by stress overcoming Van der Waals forces holding the molecules together. If stressed enough, the crazing can propagate cracks as the intertwined materials pull out from one another or the molecular chains can break (scission). This often occurs at the interface before it can occur in the bulk of the material if the materials at the interface are not as thoroughly bonded. Thus, when chemical solvents that attack polymers (such as NMP) are used to clean photoresist, they will also attack the waferbond-epoxy interface faster than the bulk material, causing the two materials to separate. This process is illustrated in Figure 2.6.

Delamination of the device layer from the carrier would typically occur in later steps but had its origins in the circuit liftoff lithography. Application of LOR photoresist during this step required baking samples at 160 $^{\circ}C$ during which the waferbond underneath the device layer would re-flow. The re-flow would cause wrinkling and stress the Si device layer which

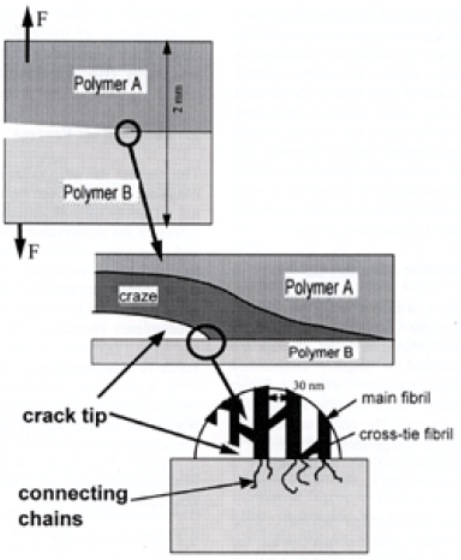


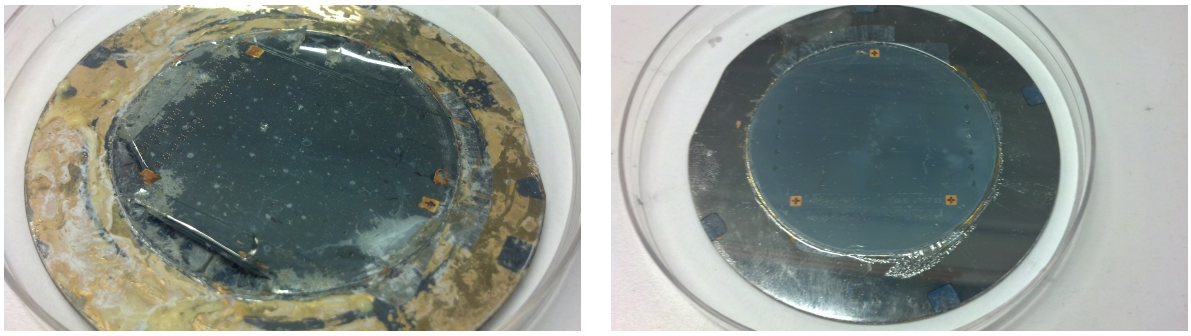
Figure 2.6: Degradation of an interface between two polymers. As the surfaces are separated, molecule chains pull out from each surface or undergo scission as they are attacked by reactive solvents[48].

ultimately would crack after subsequent processing. Solutions such as NMP and photoresist developer would then get into the cracks and further eat away at the waferbond underneath the Si, causing the device layer to crack further and delaminate. According to the process sheets for Waferbond CR-200, the waferbond should be thermally stable up to 220°C provided it is soft baked up to that temperature[50]. It was determined that inadequate soft baking of the waferbond was causing it to re-flow at 160 $^{\circ}C$ and the soft bake temperature was increased to alleviate this problem. The original bake temperature was 200 °C, however, the surface of the hot plate was only reaching 150 °C so the soft bake hot plate temperature was raised to 240 °C.

A second cause of delamination of the device layer would occur during or after the dimple lift-off lithography step and it would usually start underneath the on-wafer circuits. Problems with the dimple lithography step (described in Section 2.1) would often result in the need to repeat that step multiple times. The repeated deposition, baking and stripping of the resist would wreck havoc on the waferbond/epoxy, again resulting in delamination of the device layer. Improvements to the dimple lithography reduced the need to repeat this step multiple

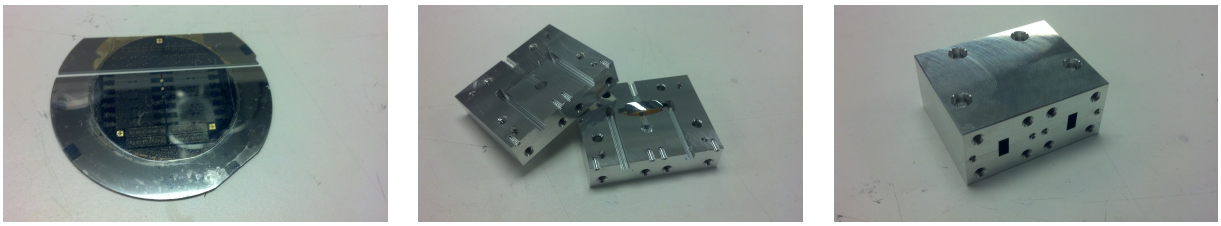
times, which had the added benefit of helping to improve the adhesion between the carrier and device wafers.

However, none of the above mentioned solutions ultimately prevented the SOI from delaminating during the MEMS processing. Eventually the waferbond and epoxy would break apart leading to the destruction of the sample. The first approach to solving this problem was to remove the epoxy from the process by only spinning waferbond on the SOI and pressing it directly to the carrier wafer. The waferbond would need to be soft baked before pressing to remove the solvents in it and although a variety of bake times and temperatures were tried, a solution could not be found that resulted in a completely bonded SOI device layer - air gaps always remained between the SOI device layer and the carrier. The solution then became removing the waferbond from the process and using only epoxy instead. The epoxy is dispensed onto the carrier by syringe into a thick puddle into which the SOI is pressed, filling in any gaps or voids in the SOI. This produced flat, robust extremely well bonded samples that withstood multiple lithography steps, and aggressive cleaning of samples in NMP and ultrasonic acetone agitation. In fact, the samples were so well bonded with the epoxy that the waveguide chips could not be removed by any simple release methods. The entire SOI/Si carrier sample had to be flipped over and bonded to another 4" wafer (using waferbond & epoxy), the 3" carrier diced and thinned down to the epoxy layer holding the SOI, and the epoxy removed by O_2 plasma etching before the waveguide chips could be released from the carrier with a TCE soak. These waveguide chips were designed for use in a cryogenic chamber at NASA, however due to unforeseen challenges in the operation of the on-wafer devices (described in Chapter 3) the RF performance of these devices was never measured.



(a) (b)

Figure 2.7: (a) SOI device layer delaminating from carrier. (b) Bonded wafer ready for dicing at the end of the process flow.



(a) (b) (c)

Figure 2.8: (a) Unreleased SOI waveguide chips on a 3" carrier after the extents etch. The next step in the process would be to bond these to a 4" carrier and remove the 3" one. (b) 5 μm SOI waveguide chips released from a 4" carrier sitting on the waveguide testing block. Built-in stress in the device layer has caused them to bow making them difficult to handle. Redesigning the chips to be smaller for future work would help to make the devices easier to handle. (c) Waveguide block assembled for device testing.

2.3 Al Pillar Removal

Reactive ion etching, also known as dry, or plasma etching because it is carried out in a plasma environment, is often preferred to wet etching for various reasons. Most importantly is the anisotropic nature of a dry etch that can lead to features such as vertical sidewalls and prevent undercutting of material layers. Furthermore the chemical species that are created can be much more reactive in a plasma environment leading to faster etch rates[51]. Generally, RIE etching works by introducing chemical species into a chamber between two parallel plates. A RF bias is placed on the plates causing the molecules in the gas to collide with one another, ionizing them. Since electrons are more mobile than their heavier counterparts they are quickly absorbed by the plates and a DC bias builds in the plasma. If one of the plates is grounded, this bias then accelerates the positively charged species towards that plate where they can chemically react with a sample or physically sputter material from the surface (Figure 2.9). In addition, not all of the molecules in the plasma will necessarily ionize, or the plasma will cause the molecules to dissociate into uncharged chemical species, which can diffuse to the sample surface and perform chemical etching as well. An example of this process can be seen in Al RIE etching. Cl_2 is used to etch Al through the following reaction:

$$4Al + 3Cl_2 \rightarrow 2Al_2Cl_3 \tag{2.1}$$

$Al_2Cl_3$is relatively volatile and can float off the Al surface after the reaction takes place. However, bare Al readily forms a thin oxide of Al_2O_3 which can inhibit the reaction in Equation (2.1) from happening. BCl_3 and Ar are added to the gas mixture to supply B and Ar to enhance the physical sputtering of Al_2O_3. To further aid in this, the RF power can be increased at the start of the etch to help generate more ions and increase the sputter rate of the plasma.

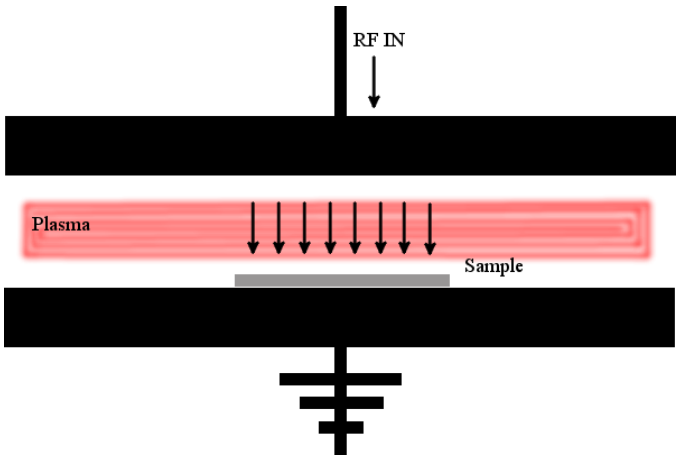
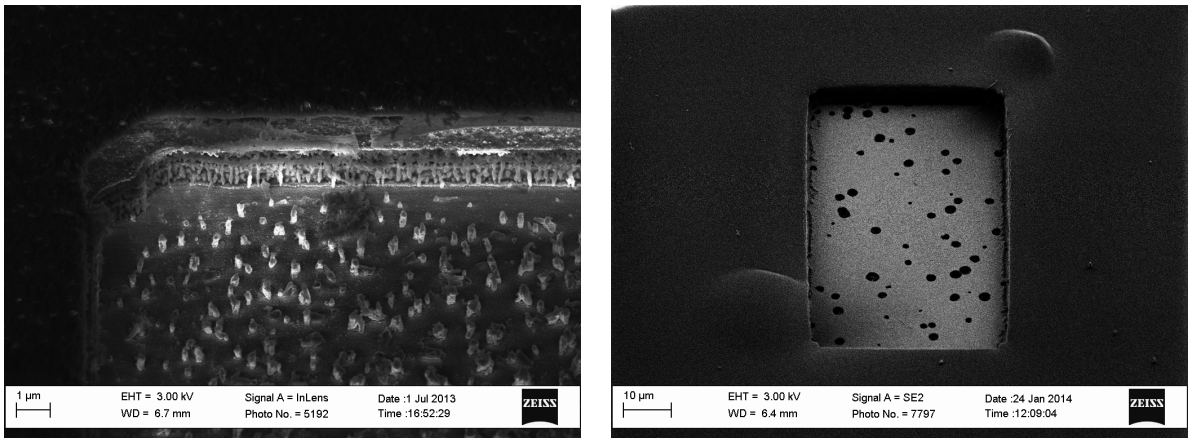


Figure 2.9: Simple layout of RIE Chamber.

Initially, the etch process used to open up the holes for the anchors (Figure 2.1k) involved three RIE etches; one for the Cr diffusion barrier (which was deposited before the Anchor etch), one for the sacrificial Al and one for the Cr etch stop. Upon inspection of the anchors after etching it was found that small pillars of Al remained in the anchor holes. These have to be removed or this Al would cause difficulty with the electroplating of the anchors or it would diffuse into the Au MEMS beams, lowering the conductivity of the Au and thus reducing device performance. It is believed that micromasking of the surface is what led to the pillar formation although it is not entirely clear whether it was unetched Cr or hardened photoresist that was making the pillars. An O_2 plasma could not be used to clean the surface before the Anchor etch because the O_2 would cause a hard oxide to form on the Cr making it resistant to the Cr RIE. Over-etching (by up to 50%) of the top Cr layer to try to remove residual Cr from the diffusion barrier was also unsuccessful at preventing pillar formation. A final alternative; to over-etch the Al Sacrificial layer also proved ineffective as the Cl-based etch would eventually etch through areas of exposed Cr and then begin to sputter away the underlying Au and finally attack the Nb underneath. Ultimately the pillars could removed using a very quick ($10\,s$) wet etch consisting of AZ400K (4:1). The quick etch is long enough to remove the pillars but not cause significant undercutting of the anchor hole sidewalls.

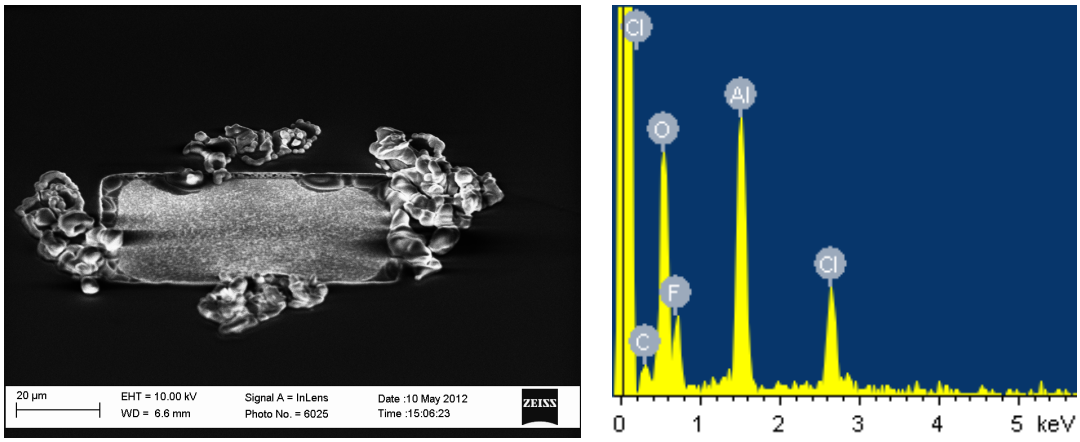


(a) (b)

Figure 2.10: Anchor holes etched by RIE (a) Al pillars remaining on the surface (b) Over-etching causing the Nb and Si to be attacked by the RIE.

2.4 Al_2Cl_3 Contamination During RIE

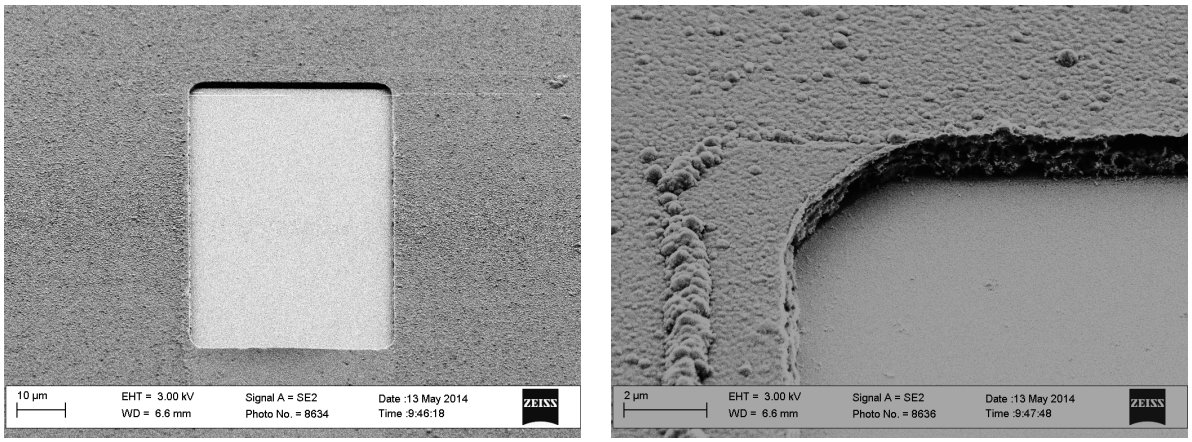
Residual Cl_2 can be left on the sidewalls or in the photoresist after completing the Al and Cr etches for the anchor trenches[51]. This can be problematic when the sample is removed from the chamber and is exposed to water vapor in the atmosphere. The water reacts with the Cl_2 to form HCl which can then etch into the Al or the Cl_2 can react with the Al during subsequent processing leaving Al_2Cl_3 (Figure 2.11). A typical solution to this problem is to expose the sample to a F-based plasma after etching to remove the Cl_2 and passivate the surface with F. Rinsing in deionized water has also been shown to help remove the Cl_2[51], however, in this research it was found that neither method was effective (Figure 2.11). It turns out that an effective solution to removing the Cl_2 was the same as the solution to the Al pillar problem discussed above; immersing the sample in AZ400K (4:1) for 10 s. The active chemical component of AZ400K is potassium borate (BK_3O_3), which when dissolved in water forms a basic solution which can readily neutralize any HCl formed from the Cl_2 residue on the anchor sidewalls. Furthermore, the AZ400K will etch a little bit into the



(a) (b)

Figure 2.11: (a) SEM image of Al_2Cl_3 debris formed after the Anchor RIE. (b) Energy dispersive X-Ray Spectroscopy (EDX) analysis of the debris showing peaks for Al and Cl. An F peak is present because surface passivation with SF_6 was attempted after the Al etch. O and C are present from the photoresist.

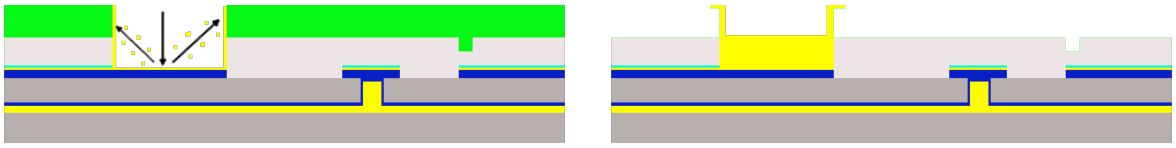
sidewalls, effectively removing any residue that remains leaving a clean sidewall and trench bottom (Figure 2.12).



(a) (b)

Figure 2.12: SEM images showing cleanly etched anchors using Al RIE followed by AZ400K rinse.

2.5 Anchor Electroplating



(a) (b)

Figure 2.13: Diagram showing how (a) back-sputtered Au will redeposit on the sidewall of the etched anchor trench resulting in (b) a lip of Au that remains when the photoresist is removed after electroplating.

Electroplating is a process in which an electric current is used to drive the ions from an electrolyte and deposit them on a surface. In the case of the Technic Au 25ES RTU electroplating bath used in this research the electrolyte contains gold sulfite ($Au_2(SO_3)_3$ or $AuSO_3$) which in solution dissociates into Au^+/Au^{3+} and SO_3^{2-}. When two electrodes are placed into the solution with a potential difference across them, the electric field will attract the sulfite anions to the anode and the Au cations to the cathode where they will deposit. If a sample is placed at the cathode then the Au can be electrodeposited onto the surface of the sample. This thickness of the deposited Au will depend on the plating current and the plating time[52]. A pulsed plating process was used where the polarity of the current was flipped every 500 ms (50% duty cycle). This helps to prevent anion buildup in the region surrounding the cathode to make the plating more effective and can result in a finer grain deposit than conventional DC electroplating[53].

Initially the anchor formation process involved deposition of the top Cr diffusion barrier before completing the anchor etch so the subsequent anchor etch would be through a Cr/Al/Cr stack, after which the anchor would be electroplated. The photoresist from the etch would be left on the wafer to prevent electroplating any Au on the top Cr layer. The photoresist is electrically insulating and Cr is conducting, thus current will only pass through the exposed Au anchor regions and deposit Au there. However, during the Anchor

RIE, back-sputtered Cr and Au deposit on the sidewalls of the resist and cause subsequent plating of Au up the sidewalls. This results in a lip of Au that remains after the photoresist is stripped (Figure 2.13). This lip leads to a weak joint between the beam and the anchor so the process must be modified. Instead of electroplating the anchor separately, the photoresist could be stripped and the Au seed layer for the beam immediately deposited so the anchor can be electroplated at the same time as the beam. However, this results in an inconsistency in the thickness of the beam at the anchor hinge point (Figure 2.14b) and leads to early device failure during reliability testing. This is due to the fact that the weakened hinge does not provide enough mechanical support for the beam to be considered a fixed-free cantilever. This decreases the spring constant of the beam and lowers its restoring force so the beams remain stuck to their contacts after pull-down. To solve this problem, separate electroplating of the anchor and beam were reintroduced to the process flow, however, the photoresist used to mask the anchor etch was stripped after etching so Au would not electroplate on its sidewall during anchor electroplating. This exposes the sacrificial Al layer to the electroplating bath, but fortunately the surface of Al readily forms a very chemically stable oxide (Al_2O_3). Au can not react with the alumina during electroplating because Au is not as electronegative as Al and thus plating only occurs in the bottom of the anchor trench. It should be noted that some back-sputtered Au can remain on the sidewalls of the Al. However, if Au were to plate up and over the sidewall in this case it is not an issue because the Au is now incorporated into the beam during later electroplating steps.

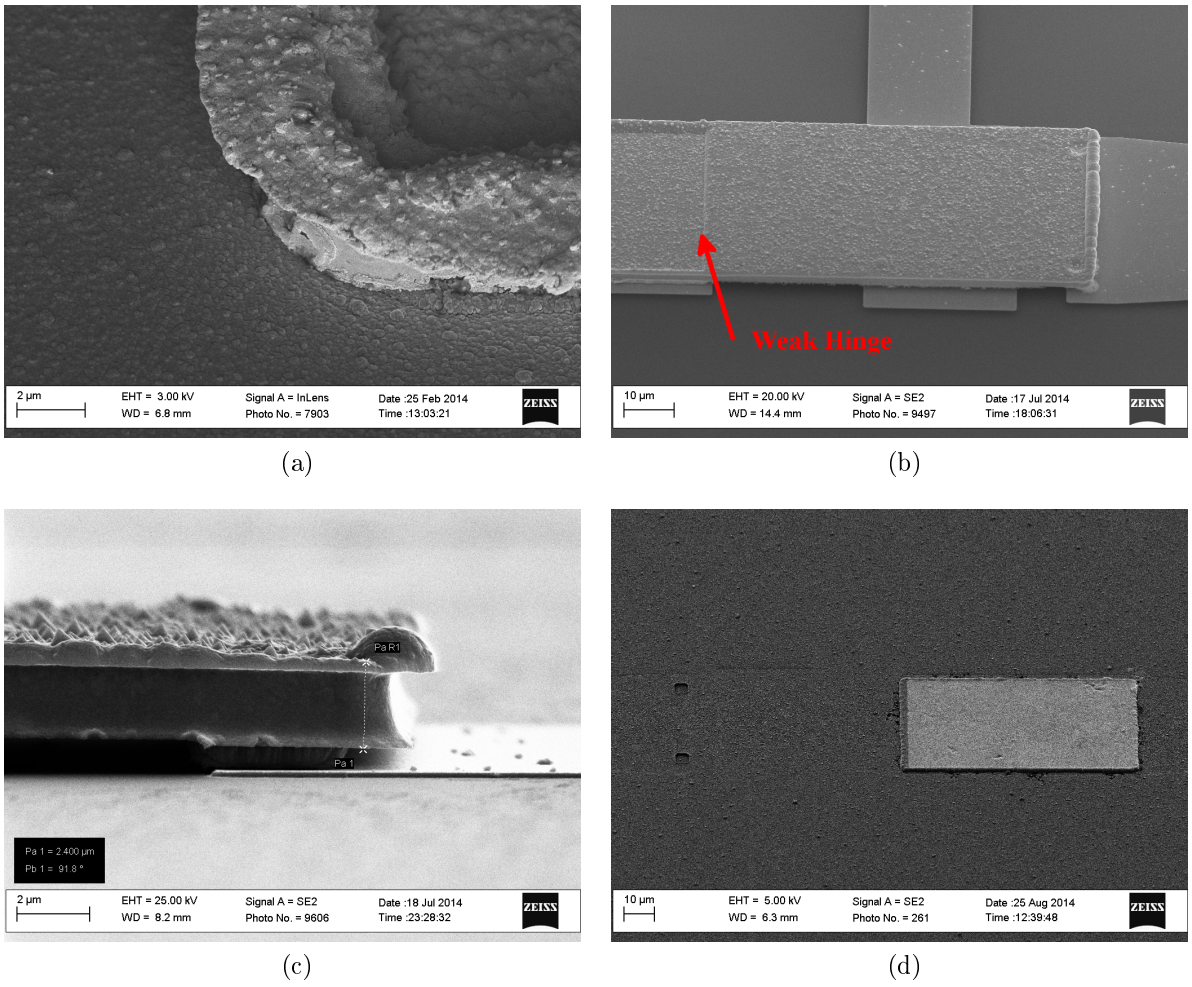


Figure 2.14: Images from the fabrication of the anchors and the beam: (a) Lip formed by electroplating along photoresist sidewalls. (b) Thin hinge-point from electroplating the anchor and beam at the same time. (c) Stuck beam due to a weak hinge. (d) After anchor hole has been etched in top Cr diffusion barrier, the electroplated Au is smooth and planar with the top of the sacrificial layer.

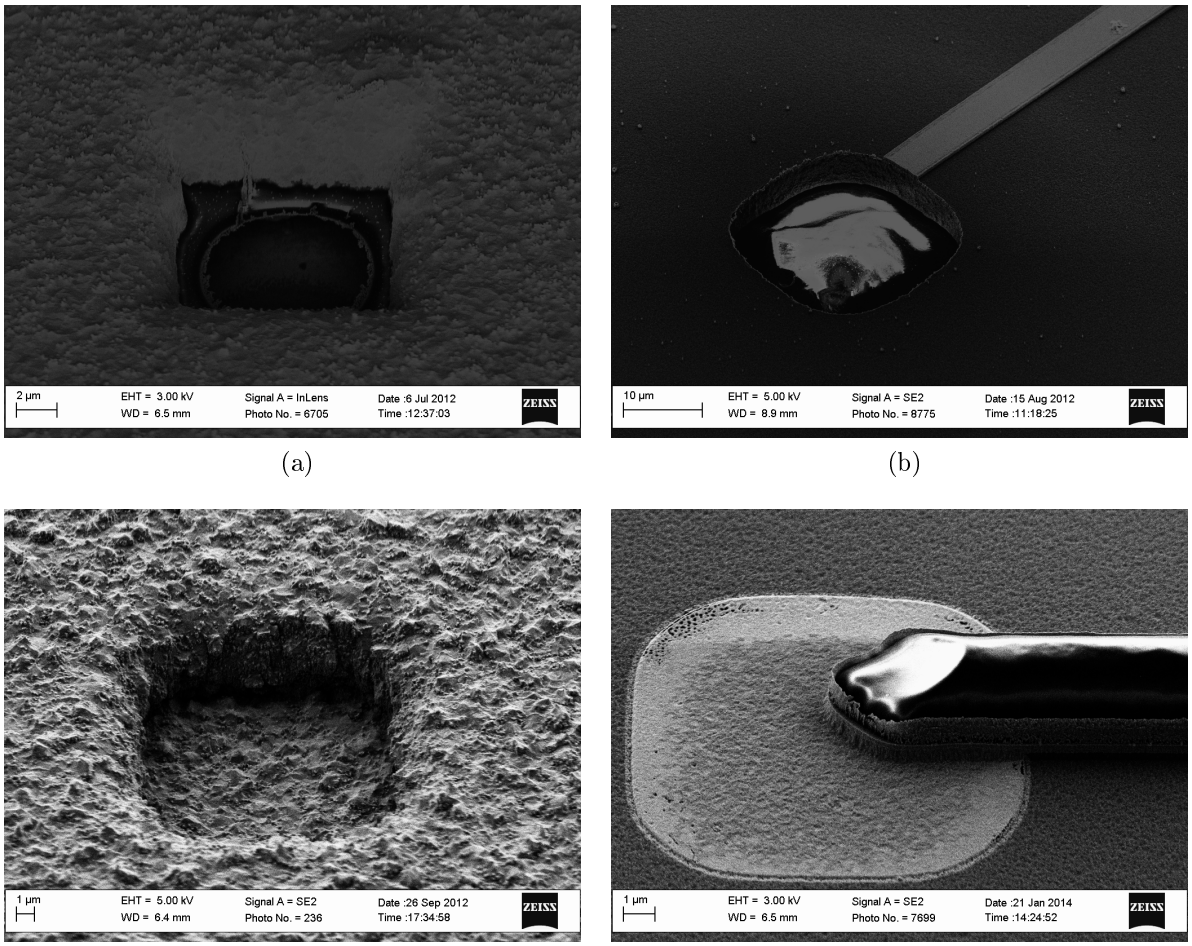
This change means that the Cr diffusion barrier deposition must now occur after the Anchor Etch as described in Section 2.1. This ensures the anchor is planar with the top Al sacrificial layer for the beam electroplating. The top Cr diffusion barrier is deposited and then etched over the anchors so that a continuous Au region constitutes the anchor and the beam. If the Cr layer was not removed over the anchor it could be seriously undercut during the release Cr etch, possibly resulting in detachment of the beam from the anchor. Finally after this etch the beam seed layer is sputtered and the beams are electroplated.

2.6 Via Electroplating

The via electroplating is a crucial step in the process or none of the RF shorts that the phase switches rely on would be properly grounded. This is why the Nb/Au ground plane was sputtered, to conformally coat the sample and insure proper side-wall coverage for the electroplated Au to completely fill the vias. If the side-walls were not covered, then no electrical connection to the bottom of the vias would exist and no Au would plate there. Furthermore, the filling of the vias could be impeded by undeveloped photoresist remaining on the via sidewalls after the beam-lead lithography. The resist remains undeveloped because the intensity of light falls off exponentially with depth z in the resist as:

$$I = I_o e^{-\alpha z} \tag{2.2}$$

where I_o is the intensity at the surface of the resist and alpha is the optical absorption coefficient of the resist[51]. Since the bottom of the vias is $5\,\mu m$ below the surface of the wafer, and there could be up to $4\,\mu m$ of resist above the surface of the wafer, a sample could look fully developed but photoresist could still remain in the vias. Subsequently, the exposure dose for this lithography was tripled as compared to the recommended dose for $4\,\mu m$ of AZ4330 and after hard-baking the resist, a ten minute O_2 plasma clean was performed at $200\,W$ to clean both the wafer surface and the bottoms of the vias.



(a) (b)

(c) (d)

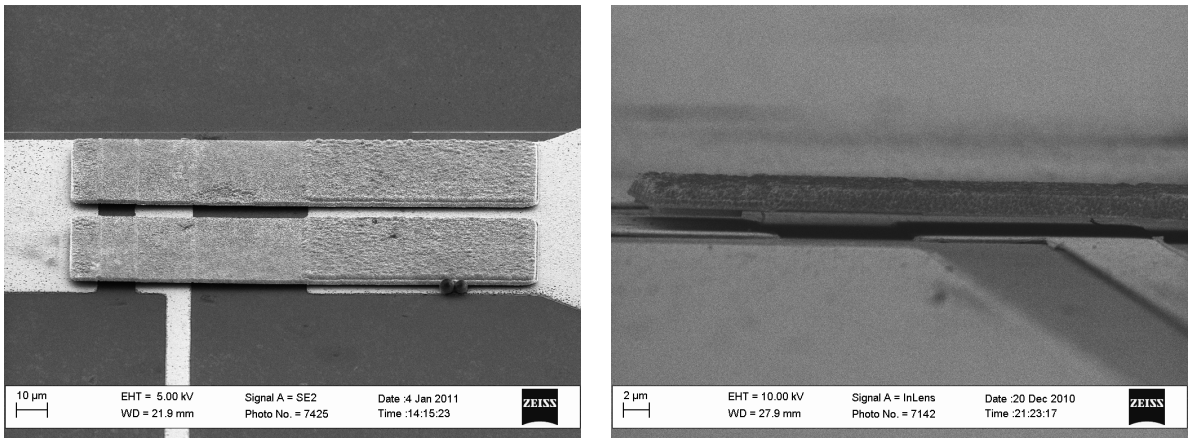
Figure 2.15: SEM micrographs showing (a) improper filling of a via due to residual photoresist, (b) a transmission line ending in an unfilled via, (c) a properly filled via, and (d) a properly shorted transmission line.

2.7 Tungsten Fabrication Process

Early research concentrated on using of W as the sacrificial layer for the MEMS process after previous work in our group found that W acts as an excellent Au-Al diffusion barrier[54, 55]. That work also found Cr was easier to deposit and provided a better etch stop for the anchor RIE[46]. An investigation was launched to determine the plausibility of using W for

the entire sacrificial layer. W has a CTE of $4.5 ppm/K$ which is very close to Au ($14 ppm/K$) and does not diffuse into Au as readily as Al. Furthermore, W is readily etched by H_2O_2, which will not attack Nb or Au making it very compatible as a sacrificial layer. However, our collaborators at NASA determined that the H_2O_2 was incompatible with Mo in their detectors and the W process was abandoned. Detailed process sheets for the process can be found in Appendix 6.2, however, a discussion of the major challenges for using W as a sacrificial layer for MEMS will be discussed below.

2.7.1 W Process Outline



(a) (b)

Figure 2.16: Released MEMS beams fabricated by W Process

The W process follows the same general flow as the Al process discussed above: Circuit layer planarization, anchor and dimple planarization, beam electroplating, and device release. One big difference in how these steps are realized stemmed from the fact that W has a much higher melting point (3422 °C) than Al (660 °C) and thus is more difficult to evaporate. This means that the W is sputtered, which makes it harder to use a lift-off process to define the circuit and dimple layers. The process begins by sputtering a 300 Å Cr etch stop followed by 4000 Å thick W circuit layer and on top of that a trilayer consisting of 1 μm Polymethyl

methacrylate (PMMA), 300 Å sputtered Cr, and 1.4 μm of AZ5214 photoresist. The Cr and PMMA and finally the W are etched by an RIE followed by a quick etch with H_2O_2 for 5 s before sputtering 4000/300 Å Nb/Au into the etched hole. The stack is lifted off and 6000/300 Å W/Cr is sputtered on the planar surface (the Cr layer serves as an etch stop for the dimples later in the process). The anchor hole is opened by patterning the sample using the trilayer stack and a series of Cr/PMMA/Cr/W dry etches followed by a H_2O_2 etch. Next, a Cr RIE removes the layer sitting on top of the PMMA. If this layer isn't removed before electroplating the anchor it is possible that Au could grow everywhere on the sample during plating. After electroplating, the trilayer stack is removed and a third 6000 Å W sacrificial layer (for the dimples) is deposited and etched using the trilayer process. This layer is etched down to the Cr etch stop (mentioned above) and 6000 Å Au is evaporated (then lifted-off) filling the dimple holes and holes above the anchors to planarize the sample. A 300 Å Au seed layer is sputtered and then patterned to electroplate the beams to 2.2 μm thick. This seed layer is etched and the MEMS are released using a W/Cr/W wet etch.

2.7.2 PMMA RIE

In order to successfully lift off the sputtered 4300Å Nb/Au circuit layer a thick photoresist is needed. Such a stack has to have a good selectivity to the W RIE that is used preceding the liftoff. To increase the resistance and thickness of the photoresist, a PMMA/Cr/Photoresist stack is used to pattern all the W layers. Using PMMA has the added advantage that it is easy to remove with acetone. An O_2 based RIE is used to etch the PMMA polymer. Initially, cracks would form during the PMMA RIE that would then leave areas of the W layer exposed to unwanted etching later in the process (Figure 2.17). It was determined that these cracks were caused by heating of the sample during the O_2 RIE. PMMA has a CTE of $\sim 100\, ppm/K$ while W has a CTE of 4.5 ppm/K so when the sample was heated during the RIE, the PMMA would expand more than the W substrate and stress the PMMA causing the cracks. Thus it is very crucial to properly thermally anchor the sample to control the

temperature during the RIE.

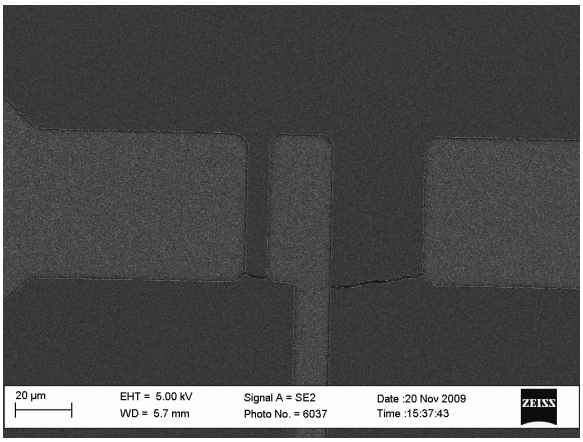
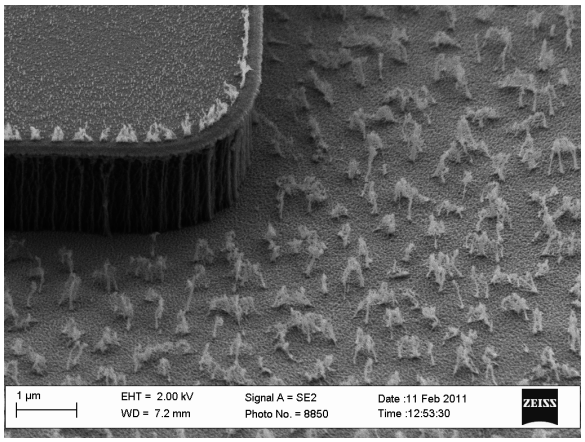


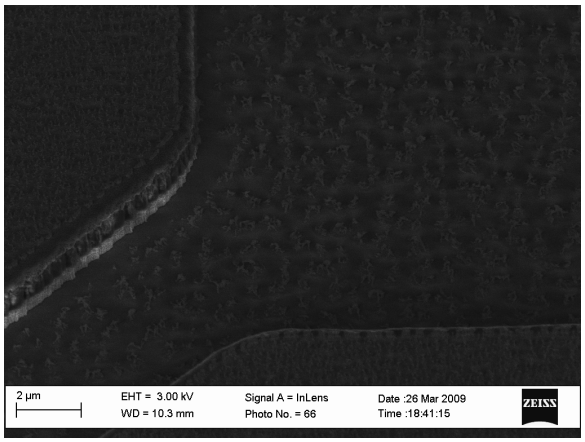
Figure 2.17: PMMA Cracking resulted in etching of the W underneath and deposition of Nb/Au in the etched area.

2.7.3 W H_2O_2 Clean and MIBK Develop.

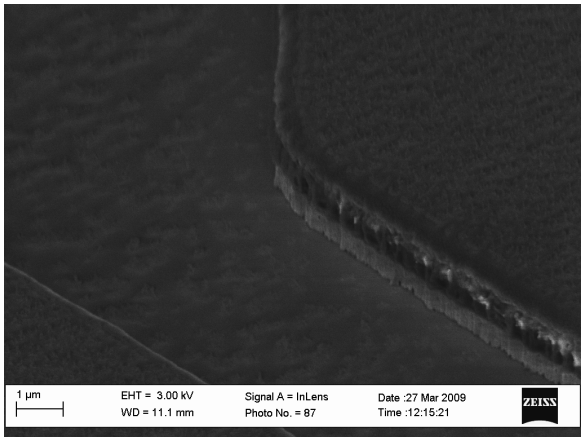
It was found that after completing the PMMA etch, thin pillars of PMMA would remain that would mask the W during the subsequent RIE. Various experiments with the fabrication process were conducted to try to remove the PMMA pillars. First, longer etching of the Cr in the trilayer stack was thought to help remove little bits of Cr that might be micro-masking the PMMA and resulting in the pillars, however, this showed no improvement. Next, varying PMMA RIE process parameters such as increasing the pressure, or adding ICP power to make the etch more isotropic and hopefully remove the pillars from the sides also did not help. Finally Ar was added to the recipe to hopefully help physically sputter away any PMMA that would not etch in the RIE - which also did not help. The ultimate solution was to introduce a 5 sec H_2O_2 wet etch to remove the pillars left in the W after it was dry etched. Sometimes the PMMA debris was too large and the H_2O_2 etch was not long enough to etch away all of the unetched W. It was not a simple matter of extending the etch to fully clean the surface because the sidewalls of the etched trenches could become severely undercut by



(a)



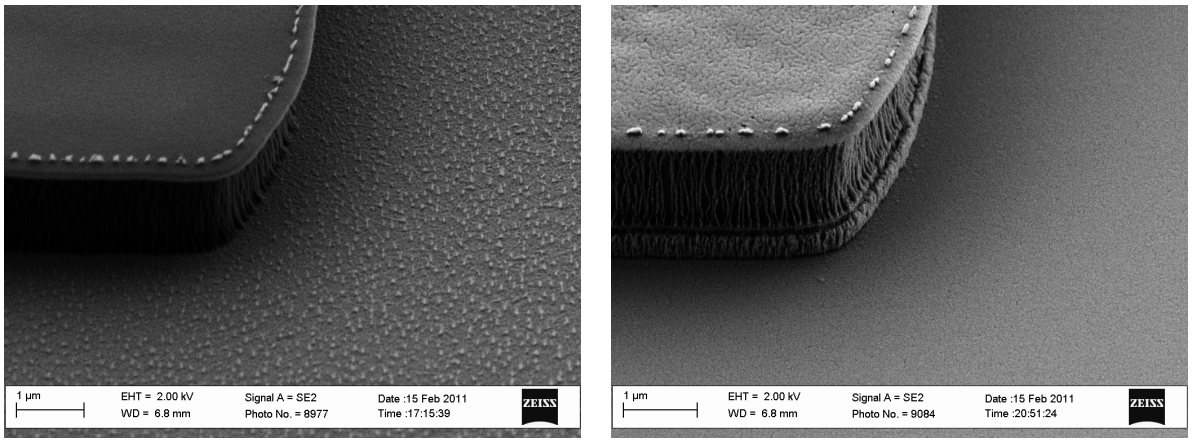
(b)



(c)

Figure 2.18: SEM image of PMMA remaining after RIE (a) W remaining on the bottom of an etched trench after RIE (b) and removal of the pillars after H_2O_2 clean-up (b).

the H_2O_2. An alternative solution was investigated: developing the PMMA after the O_2 RIE in MIBK developer. By quickly developing the PMMA ($15\,s$) and then rinsing it in IPA ($30\,s$) the pillars were significantly reduced and would become sputtered away during the W RIE. By combining the two processes of post PMMA RIE developing and H_2O_2 etching, very smooth trenches were realized for all W patterning.



(a) (b)

Figure 2.19: SEM images of (a) PMMA debris after MIBK development and (b) Smooth trench etched into W.

2.7.4 W Film Stress

During the course of processing samples, cracks would sometimes form in the W films and they would peel up (Figure 2.20). It is believed that the cracks were caused by stress introduced into the films during deposition. Controlling film stress through deposition parameters such as sample temperature, Ar plasma pressure, and RF power are certainly possible, however, the W process was abandoned for the Al process before this issue could be further investigated.

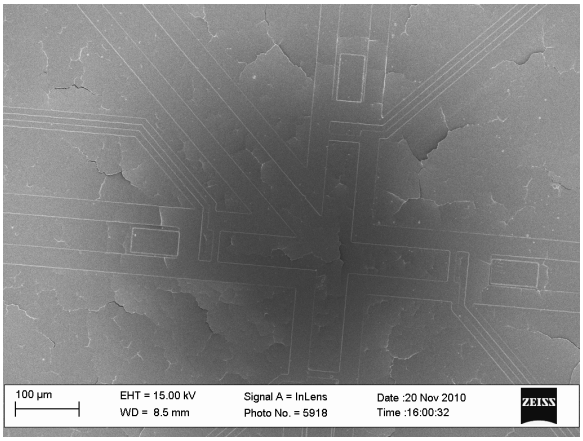


Figure 2.20: SEM image of cracked W film

2.8 Fabrication Process Summary

RF MEMS switches have been fabricated using SOI as a microstrip substrate. The development of the microelectronics fabrication process to realize those switches was not easy or straightforward, and the challenges and solutions presented above attest to that. Keeping the thin, fragile SOI device layer bonded to its carrier wafer using epoxy that won't degrade during processing was the biggest hurdle to overcome. Additional problems that were solved include resputtering of Au and deposition of Cl_2 contamination on the sidewalls of the MEMS anchor and removal of incompletely etched Al films. The formation of good vias with proper electrical connections through the substrate also played a critical role in the fabrication of working devices and an investigation into the use of W as a viable sacrificial layer for MEMS showed promising results. Although currently incomplete, if the W process can be optimized then it may provide a useful tool for the fabrication of MEMS devices in the future.

Chapter 3

RF MEMS: Modeling and Performance

Our research group has already developed a variety of RF MEMS switches and devices [20, 57, 56, 58]. This work draws upon the wealth of prior research and extends our knowledge of RF MEMS to cryogenic temperatures. Some of the switches used in this research were designed by Gong et al. and a thorough description of them operating at $77\,K$ can be found in [20].

3.1 MEMS Switch Design

The switches are modeled using the electromechanical simulator Coventor and a brief discussion of the design methods are presented below. Using Equations 1.17 and 1.18 as a starting point, the height, width, length and thickness of the cantilever that give a required pull-down voltage are found. Coventor is used to determine the tip geometry that results in an up-state capacitance of 1 fF to keep S11 low when the switch is in the up-state. An initial goal restricting $V_P < 25\,V$ is desired by NASA collaborators wanting to keep V_P low due to voltage supply limits on the balloon and satellite platforms on which the devices will potentially fly. Note that a low pull-down voltage is not always practical for an RF MEMS switch. This is because to achieve a low pull-down voltage, the spring constant of the beam is usually reduced, which can have some undesired secondary effects, such as a reduction in restoring force. A lower restoring force means the cantilever has less energy to overcome adhesive forces in the down state leading to an increased chance of device failure through stiction. The switch geometry from [46] is used in this research because it was

already shown to be a reliable switch with a contact force of $\sim 40\,\mu N$. The switch has the dimensions displayed in Figure 3.1 and will yield a pull-down voltage of $\sim 80\,V$ when the beam is $1.2\,\mu m$ above the bias pad. There is one drawback to using this switch at cryogenic temperatures; a CTE mismatch between the Au ($CTE = 14\,ppm/K$) anchor and quartz ($CTE = 0.5\,ppm/K$) substrate which can lead to an increase in pull-down voltage as the temperature decreases. However, it has been shown that this effect on pull-down voltage is greatly reduced on Si ($CTE = 2.6\,ppm/K$) or SiO_2 ($CTE = 4\,ppm/K$) substrates[46] which are used in this research.

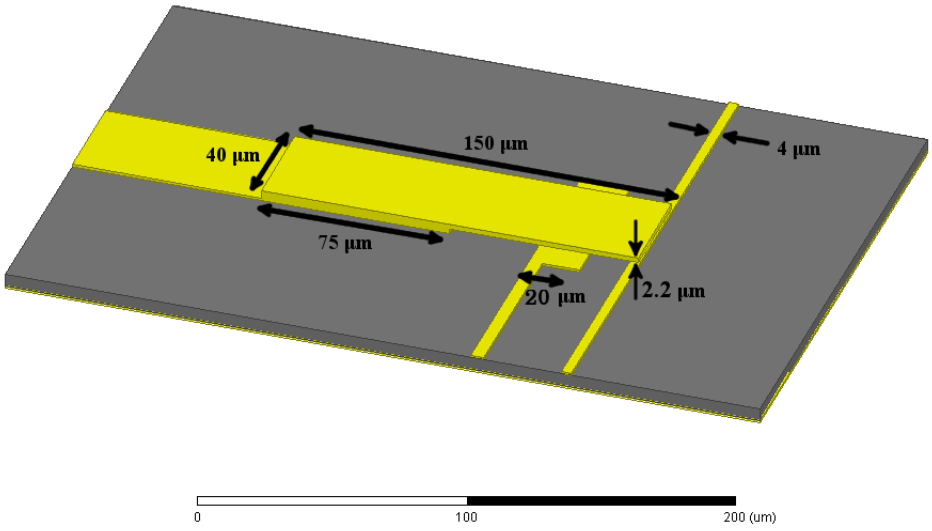


Figure 3.1: Maxwell 3D image of DC-contact shunt switch with dimensions overlaid.

3.2 Phase Switches

Multiple devices were fabricated on $5\,\mu m$ SOI substrates including series DC-contact switches, shunt DC-Contact switches, 180° phase switches and 90° phase switches. At higher frequencies the up-state and parasitic capacitances limit the performance of the series switch so a shunt switch implementation was used in the design of the phase switches. The shunt

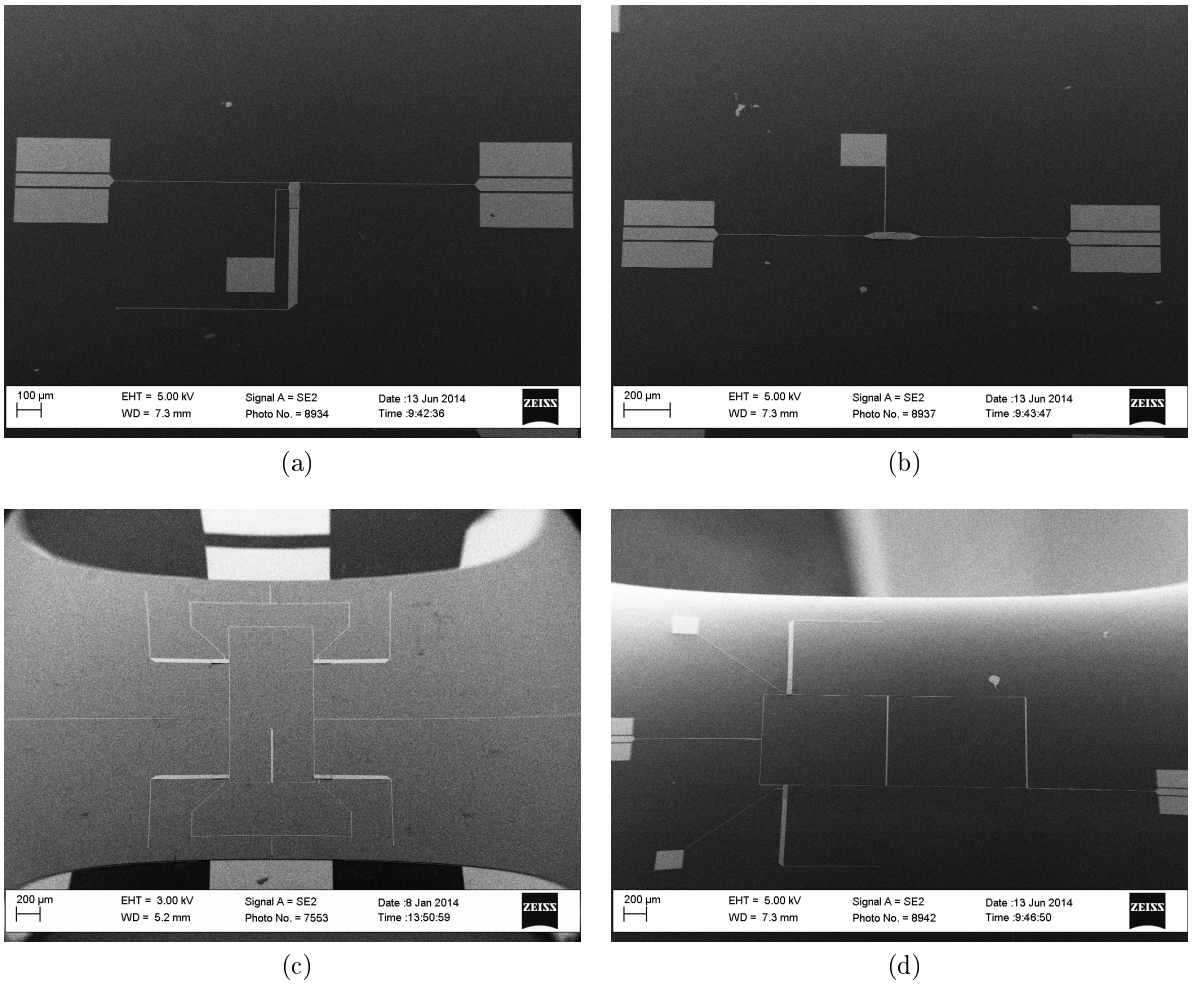


Figure 3.2: SEM images of fabricated RF MEMS devices: (a) Series DC-contact switch (b) Shunt DC-contact switch (c) 90° phase switch (d) 180° phase switch.

configuration works on the principle of impedance transformation; by closing the switch a short to the ground plane (via) is transformed by a series of $\lambda/4$-wave transformers into a virtual open or short at the switch contact depending on how many impedance transformers are used. This enables the phase switches to operate over a 20% fractional bandwidth which can be scaled to higher frequencies. The series switches were intended as a means of determining the range for the pull-down voltage of the other devices and not as an operational RF device and are subsequently not optimized for RF measurements. This can be seen in figure 3.2b where a thin $4\,\mu m\,(50\,\Omega)$ wide transmission tapers out to accommodate the with of the switch. This taper results in an impedance mismatch and poor RF performance.

3.2.1 180° Phase Switch

The phase shift in the 180° circuit is achieved using a simple form of phase modulation; a $\lambda/2$ square[81]. In such a circuit (Figure 3.3), two single-pole single throw (SPST) switches can be used to load two corners of the square with open circuits. This is achieved by placing electrical shorts $\lambda/4$ away from the two corners. The $\lambda/4$ transmission lines transform the short seen at the MEMS switch into open circuits at the branches. Thus keeping one switch open, one switch closed and alternating which switch is open, one can select between the through branch and the 180° branch.

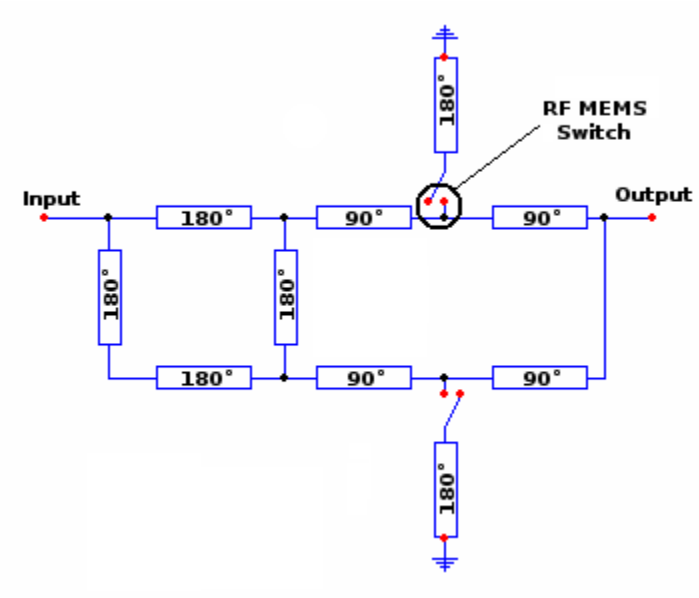


Figure 3.3: *180° circuit schematic*

3.2.2 90° Phase Switch

The 90° phase shift is realized using a loaded-line high-pass/all-pass configuration (Figure 3.4). This design is based on high/low-pass phase shifters which provide improved bandwidth

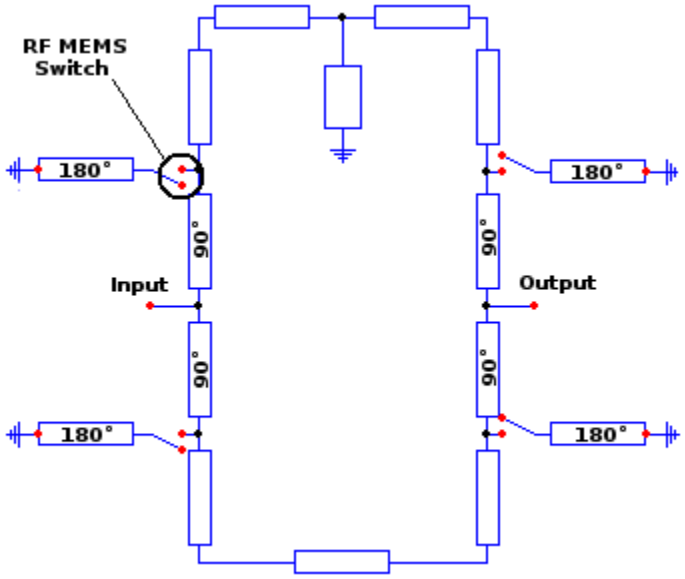
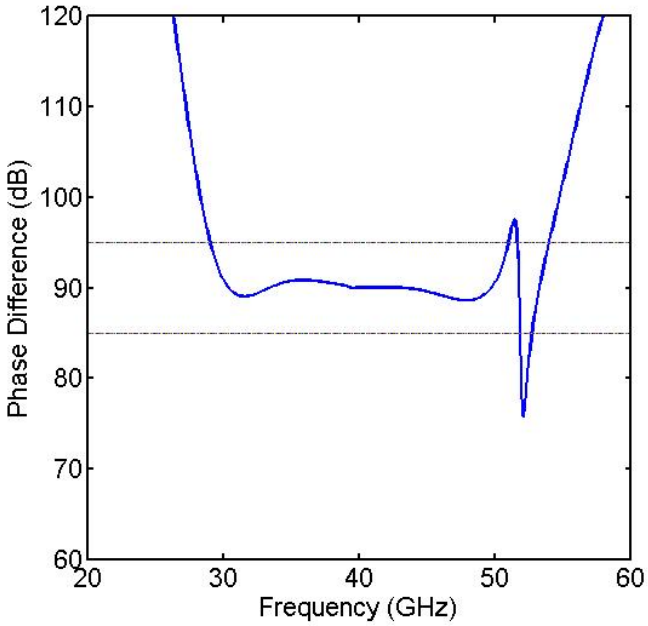


Figure 3.4: *90° Phase Switch Schematic*

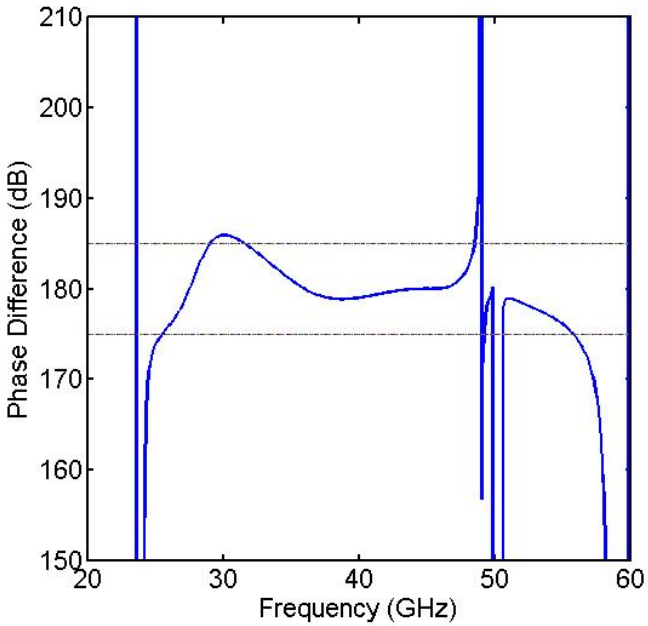
while reducing the overall footprint of the circuit[82]. The high-pass segment is implemented using shorted stub placed at the center of the high-pass branch. Again, SPST MEMS switches are placed 90° away from the transmission line branch points and are transformed to open circuits at the junctions. When both switches on the high-pass side are open, while the all-pass switches are closed, the signal will propagate down the high-pass side. Flipping the switch configuration shuts off the high-pass side and opens the all-pass transmission line. It should be noted that a -90° phase shifter can be implemented by replacing the shorted stub with an open stub, turning the high-pass branch into a low-pass branch. Garver [82] also showed that using the high-pass/low-pass configuration, constant phase difference over an octave or more was possible for $|\Delta\phi| \leq 90°$. For phase differences greater than $\pm 90°$ the bandwidth can be increased by adding more poles to the "filters", however, this would also increase the overall footprint of the phase switch, which is undesirable for large arrays of polarimeters.

3.2.3 Simulation Results

Simulated phase performance at 40 GHz for both the 90° and 180° phase switches are shown in Figure 3.5, while the insertion and return loss are displayed in Figure 3.6. The phase is within ±5° across each band, while the insertion loss remains below 1 dB and return loss below 10 dB. According to the simulations, this performance can be achieved by designing a MEMS contact switch with $C_{up} = 1$ fF and contact resistance of $R_C = 1\,\Omega$ was assumed. The microstrip transmission lines are modeled as perfect conductors on an 5 μm thick SOI substrate. These devices are readily scalable to frequencies as high as 200 GHz without the need to alter the MEMS structure.

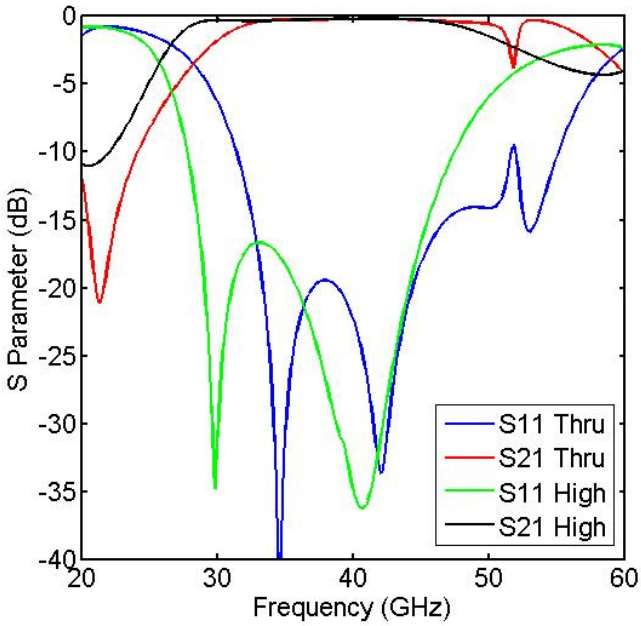


(a)

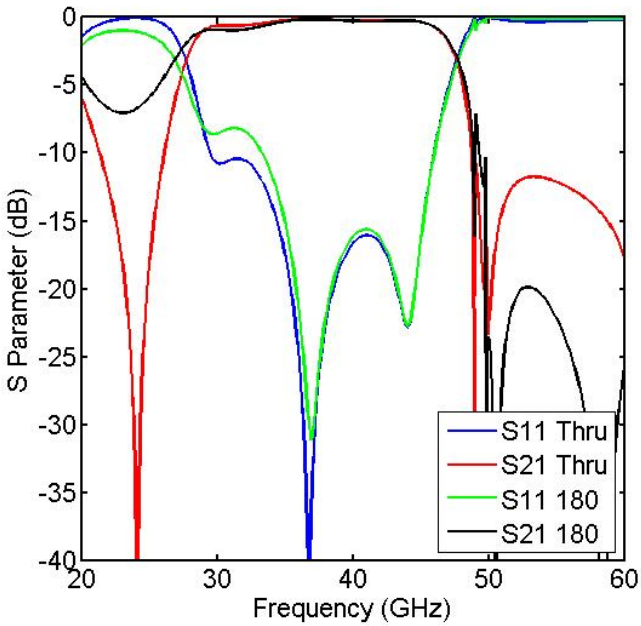


(b)

Figure 3.5: Simulated phase perfofractionalrmance for 90° and 180° phase shifters at 40 GHz.



(a)



(b)

Figure 3.6: Insertion loss and return loss for both signal paths of the 90° and 180° phase shifter at 40 GHz.

3.3 Dielectric Breakdown

Unfortunately there is no available data on the performance of the shunt switches (and as a result, the phase switches) due to dielectric breakdown of the Si device layer during testing. The breakdown field strength of Si is $\sim 3 \times 10^7\, V/m$[60] which, as can be seen in Figure 3.7, is exceeded when there is $100\, V$ between the bias pad and the ground plane (comparable to the pull-down voltage at $4.2\, K$). A potential difference can build here because the anchor of the shunt switches are tied to the ground plane through a via, so when they were biased, they would breakdown before the switch was able to be closed. The series switches would not experience this problem, as long as a floating power supply was used to bias them, so that the ground plane is never referenced to the bias voltage. It should be noted that when a grounded power supply was used to bias the series switches, the Si would also break down because the RF ground was connected to the DC ground, thus establishing an electric field between the bias pad and the ground plane. This is obviously a problematic issue for MEMS switches with high pull-down voltages that are built on microstrip using SOI substrates. Some possible solutions to this problem are to lower the pull-down voltage (if possible) or to use a thin dielectric such as SiO_2 which has a higher breakdown field ($\sim 6 \times 10^8\, V/m$)[62]. Even though the results are less than ideal, the data presented below shows that it is possible to fabricate working RF MEMS switches using a SOI microstrip dielectric.

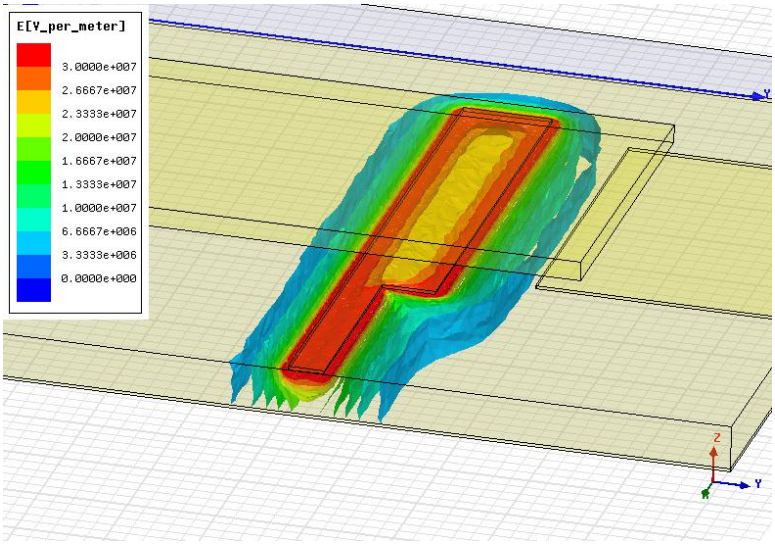


Figure 3.7: Maxwell 3D EM simulation showing the E-Field caused by an $100\,V$ bias.

3.4 RF MEMS Testing

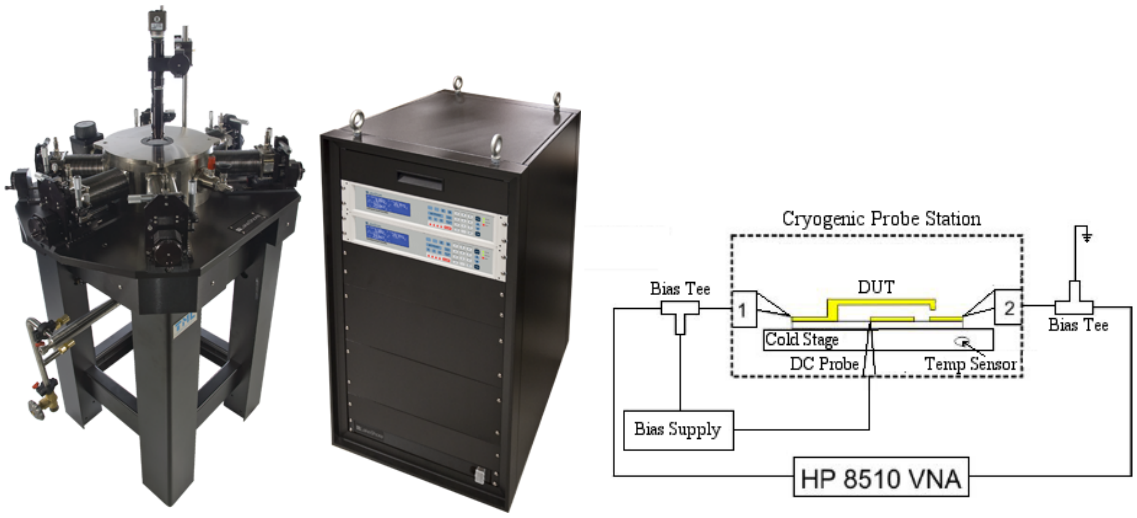


Figure 3.8: Lakeshore CPX probe station (photo: www.lakeshore.com).

The RF MEMS switches fabricated using the SOI-MEMS process described in Chapter 2 were tested in the Lakeshore CPX cryogenic probe station at UVA (Figure 3.8). The probe station has 2 RF ports for measurements up to $67\,GHz$ and four DC probe arms

for biasing. An HP8510 VNA was used for all the RF measurements and either a Keithley 2635A Sourcemeter or Agilent floating power supples for DC biasing. The cold stage can be cooled to $4.2\,K$ using liquid He, or even dropped to $1.6\,K$ by pumping on the He refrigerant to lower its boiling point.

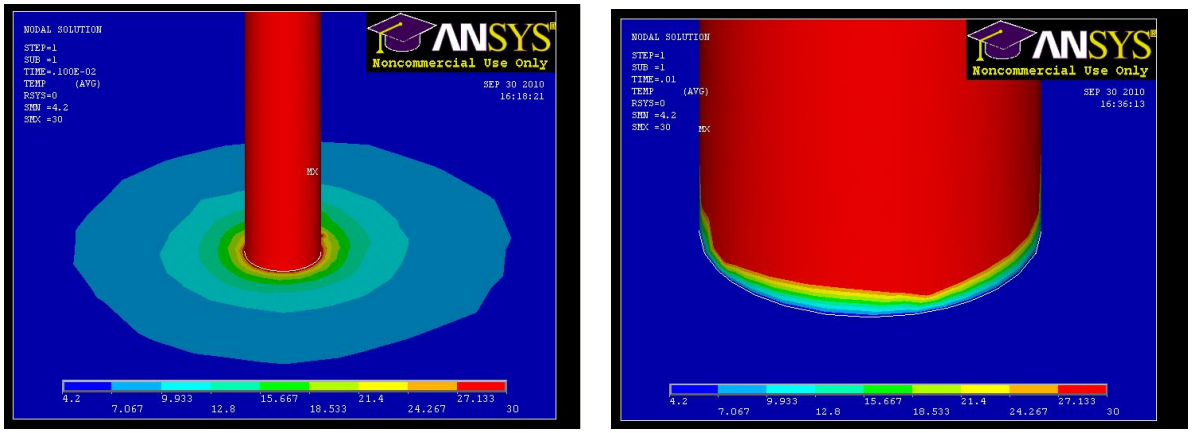
3.4.1 Thermal Considerations

Testing devices at cryogenic temperatures involves a whole new set of testing challenges as opposed to testing at room temperature and there are some important aspects that should be noted. Most importantly is that even though the test stage will reach $4.2\,K$ rather quickly, the geometry of the RF and DC probe arms results in poor conduction of heat from their tips while the CPX cools, resulting in the temperature of the probe arms being higher than the cold stage. Reports in the literature[59] and private discussions with Lakeshore Cryotronics indicate the probe arms will reach as low as $9K$, however, in our system they were never observed to drop lower than $19\,K$. This is very problematic when trying to measure a device based on superconducting Nb, which superconducts at around $9\,K$. When the probe tips are landed to make measurements, they can locally heat the substrate, destroying superconductivity. ANSYS thermal simulations were conducted to study this phenomena and two extremes are shown in Figure 3.9. It should be noted that the geometry involved in the simulations was simplified for convenience and to decrease the convergence time of the simulator. The center conductor of the RF probe is treated as an Au rod $50\,\mu m$ in diameter, and only the center conductor is modeled. In reality there are also two pins for the ground plane spaced $150\,\mu m$ to either side of the center conductor. In Case (a) the rod is treated as a thermal source at a constant $30\,K$ and the Nb substrate is given an initial temperature of $4.2\,K$. The bottom of the substrate (not pictured) is treated as a heat sink at $4.2\,K$. A steady state condition is reached in $\sim 3\,min$ showing that the substrate is locally heated to $T_{CNb} = 9.2\,K$ (or greater) within $\sim 50\,\mu m$ of the landing point. Where the probe lands it will destroy the superconducting state of the Nb within a given radius. This introduces

uncertainty in the RF measurements because the temperature gradient across the substrate surface may be different every time the probe is landed. This means different sections of the transmission line may be superconducting on each contact, thus making calibration of the VNA difficult. This is considered a worst case scenario, and in reality the situation is probably more like Case (b), where the upper end of the probe tip is treated as a heat source at $30\,K$, the probe is allowed to conduct heat, and the initial conditions and loads on the substrate are left the same as Case (a). In this case, the steady state condition shows that a temperature gradient is set up in the probe tip and the substrate is cooled back down to $4.2\,K$ under the probe tip, also in about $3\,min$. This model is limited because it assumes that the probe tip and the substrate are in intimate contact which might not be the case in reality. It also assumes that the surface temperature of the sample is at $4.2\,K$ but since the CPX reads the stage temperature under the sample mount, the actual temperature of the sample could be greater. To try to reduce measurement errors due to local heating, the probe tips were allowed to sit in contact with the sample for at least $5\,min$ before any measurements were taken. This would allow the heat injected into the substrate near the probe tips to dissipate allowing the Nb in that region to return to the superconducting state. A further precaution was to bond samples to the cold stage using silver paint which improves heat conduction away from the sample and into the cold stage[59].

3.4.2 Calibration

The VNA was calibrated using 2-port on-wafer TRL (Thru-Line-Reflect) standards defined during the circuit layer step in the fabrication process. The calibration set consisted of a thru line to define the reference plane of the measurement, shorted lines with a via at the reference plane for the reflect, and a series of line standards ($0.850\,mm$, $1.155\,mm$, $6.255\,mm$) to calibrate over a bandwidth from $50\,MHz$ to $50\,GHz$. The lengths of the lines were determined to be 1/4-wave long at $32.5\,GHz$, $24\,GHz$, and $4.5\,GHz$ respectively, and their electrical lengths were between 20° and 160° longer than the thru line at those



(a) (b)

Figure 3.9: ANSYS thermal simulations of (a) probe tip as a heat source and (b) probe tip as a heat conductor.

frequencies[61]. Figure 3.10 shows a measurement of the thru calibration standard after the VNA has been calibrated at $4.2\,K$. The measurement should read $0\,dB$ across the band for a good calibration. It is believed the errors at lower frequencies are due to poor thermal conduction and local heating of the substrate destroy the superconducting state of the Nb, making the system difficult to calibrate because there is too much loss in the lines above $30\,GHz$ ($> 10\,dB/cm$). To highlight the difficulty in performing a TRL calibration at cryogenic temperatures, a thru line measurement after calibration at room temperature is shown in Figure 3.11. The calibration is much smoother below $30\,GHz$ because the substrate and the probes are at the same temperature, thus there is less errors introduced to the measurement during calibration.

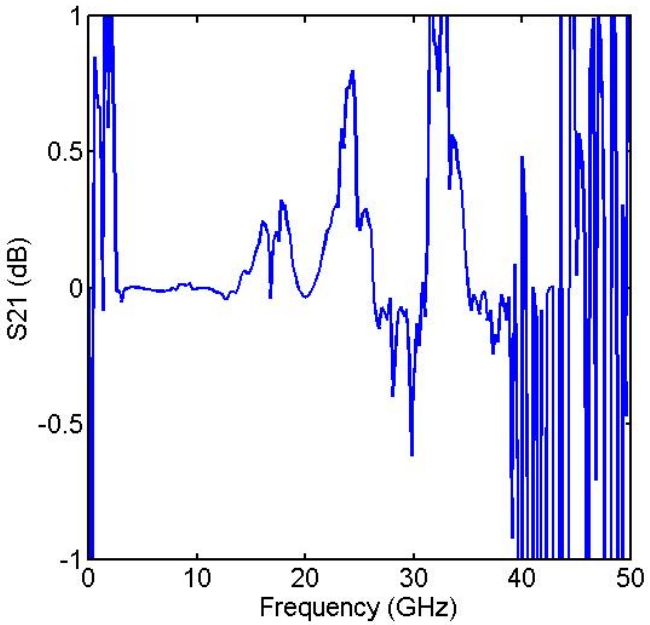


Figure 3.10: Measurement of thru line standard after calibration at 4.2 K. A calibrated thru-line should have zero loss since it has an electrical length of 0°.

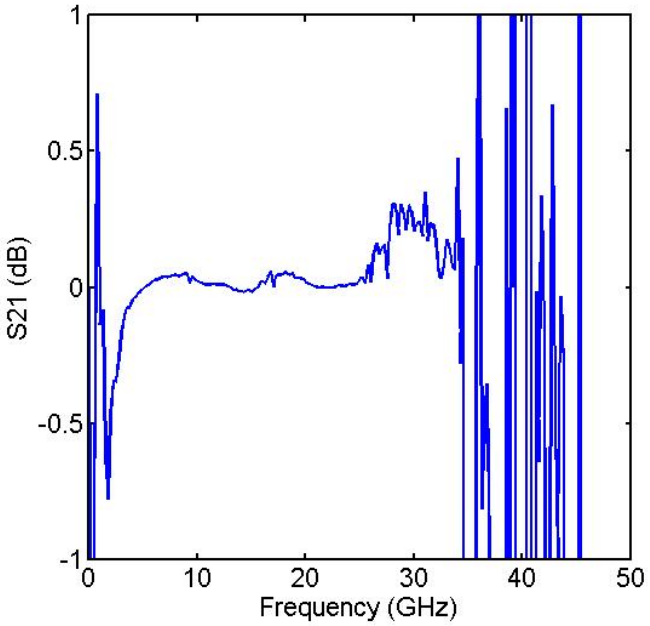


Figure 3.11: Measurement of the thru line standard at 295 K. The measurement shows improvement in the calibration below 30 GHz, and a poor calibration above 30 GHz.

3.4.3 RF MEMS Measurements

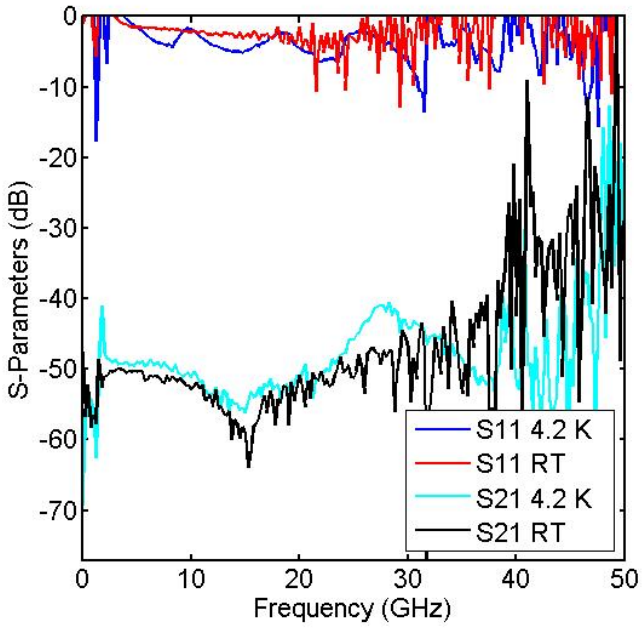


Figure 3.12: Measured S-Parameters of RF MEMS series DC-contact switch at room temperature and 4.2 K. Switch is in the up-state.

RF measurements of an Au MEMS DC-contact series switch fabricated on SOI substrate with Nb transmission line is presented in Figures 3.12 & 3.13. The data presented here shows that the fabrication process is capable of producing working RF MEMS switches on 5 μm SOI substrates. The switch exhibits excellent isolation (S21) in the upstate, and shows an improvement in S21 (vs room temperature) in the downstate when cooled to 4.2 K, however, S21 is still much lower than would be expected for a circuit using a superconducting transmission line. Measurement of the line calibration standard shows that there is loss in the system corresponding to a resistivity of the line material of $1 \times 10^{-8}\,\Omega m$ indicating that the Nb was not superconducting. However loss in the line is not enough by itself to explain why the measured performance is less than ideal. The discrepancy can be explained by the impedance mismatch between the transmission line and the MEMS switch and parasitics associated with the beam itself. As mentioned in Section 3.1 the RF MEMS shunt switches were originally designed to operate in a shunt configuration on a 50Ω transmission line, which

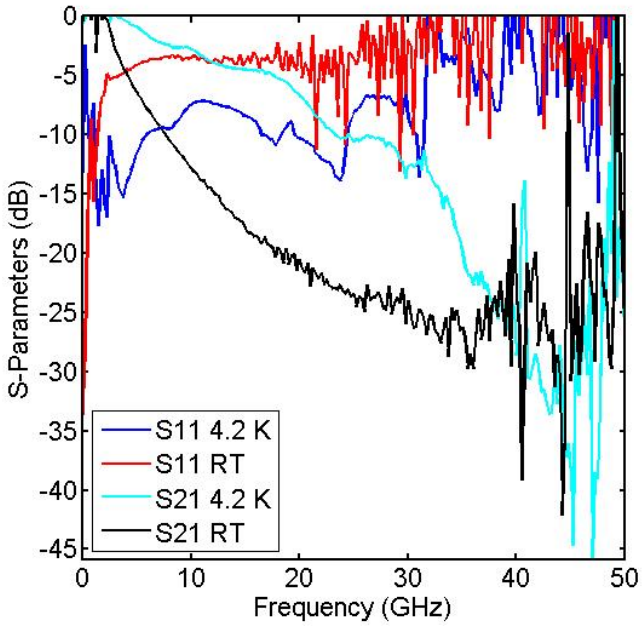


Figure 3.13: Measured S-Parameters of RF MEMS series DC-contact switch at room temperature and 4.2 K. Switch is in the down-state.

corresponds to a $4\mu m$ wide microstrip line on the $5\mu m$ SOI substrate as shown in Figure 3.2a. There were also series switches on the mask layout, which were originally used to determine the pull-down voltage of the switches. However, they also used a $4\ \mu m$ transmission line which meant that the line had to be widened $40\ \mu m$ ($Z_o = 11\ \Omega$) to accommodate for the MEMS switch (Figure 3.2b).

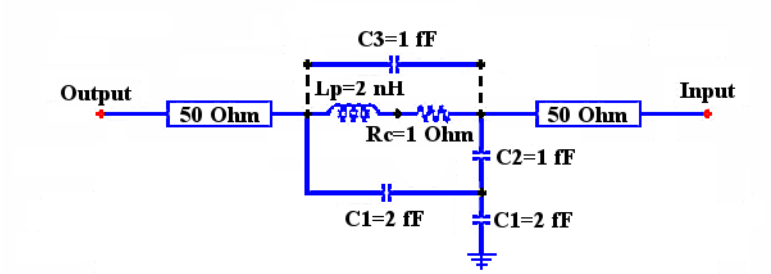


Figure 3.14: Down-state circuit model accounting for parasitics in the MEMS DC-Contact Series Switch. In the up-state, capacitor C3 replaces the series resistor and inductor.

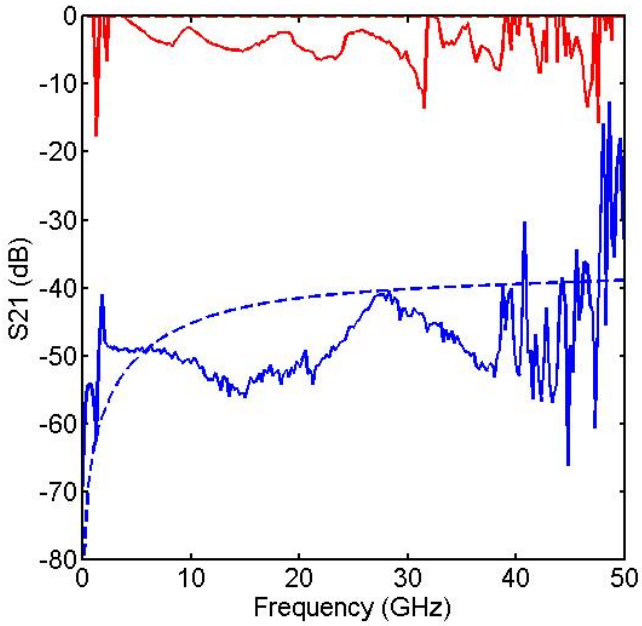


Figure 3.15: Measured (solid) and modeled (dashed) S-Parameters for the up-state of the switch at $4\,K$. The isolation corresponds to an up-state capacitance of better than 1 fF.

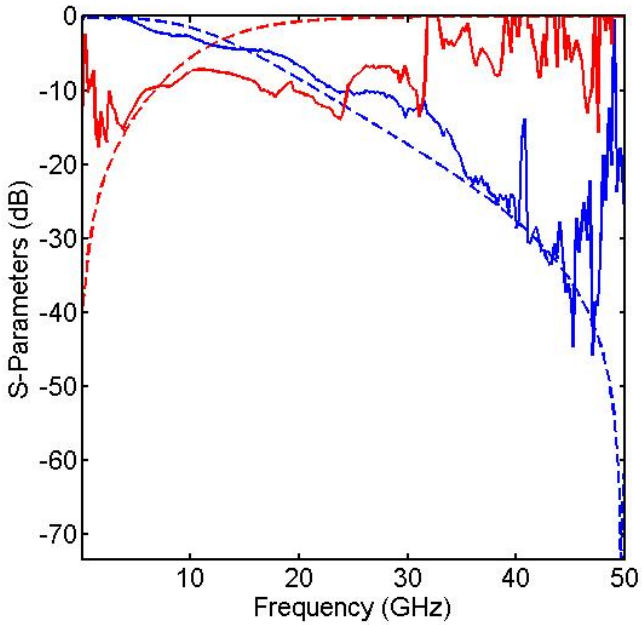


Figure 3.16: Down-state data with impedance mismatch, loss, and parasitics included in the model (dashed) compared to measured (solid) data.

This widening of the transmission line causes the input impedance seen at the switch to decrease; leading to reflection of the input signal and a decrease in measured S21 of the switch. The reflection can be seen in Figure 3.16 as S11 is greater than $-15dB$ above $5GHz$. This mismatch is also not enough to explain the large drop in S21 as frequency increases but the loss can be accounted for when parasitic inductance and capacitance is included in the model (Figure 3.14). The parasitic capacitance values are obtained from Maxwell 3D simulations while the parasitic inductance was fit to the data. Although the series switch exhibits poor RF performance it does demonstrate that it is possible to fabricate working RF MEMS switches on top of a thin SOI microstrip substrate.

3.5 RF MEMS Resonators: Modeling and Results

3.5.1 Motivation

Recent work by Attar et al. shows how lossy Au MEMS switches will affect the performance of superconducting circuits at liquid helium temperatures[59] as well as impressive work with MEMS devices built out of superconducting Nb[63, 64]. This work looks to verify and extend upon this knowledge. It is crucial to gain an understanding of how integrating these MEMS and superconducting technologies will work if RF MEMS are to be used in superconducting circuits for CMB measurements. The biggest questions to be answered are: How will the fabrication process affect the properties of Nb? Will the Nb be able to superconduct? And how will the contact resistance of MEMS affect superconducting device performance? A mask set has been designed with multiple experiments to answer these questions. Four-point probe resistance measurements of Nb test structures (Figure 3.17) were taken as the sample was cooled below the critical temperature of Nb ($9.26\,K$). The room temperature resistance of the structure is estimated to be about $1.14\,\Omega$ show an abrupt drop in the resistance of the structures from $0.25\,\Omega$ to $-0.12\,\Omega$ as the temperature drops below $6\,K$. This verifies that the fabrication process can produce superconducting circuits. Also included on the mask

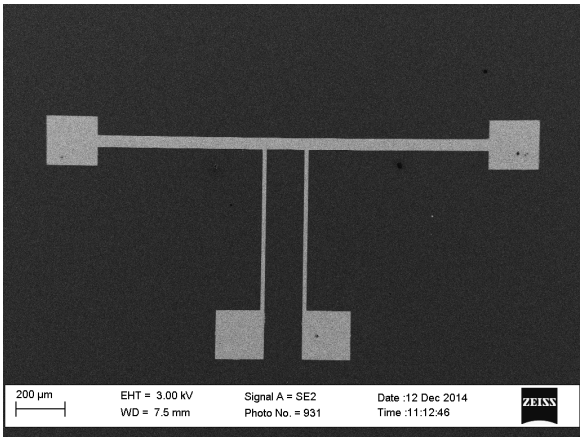


Figure 3.17: SEM image of 4-point probe test structure used to measure the critical temperature of superconduction for the Nb microstrip lines.

are a set of experiments involving tunable microstrip resonators to test how lossy MEMS will affect the performance of the superconducting circuits. Superconducting microstrip resonators have already been developed with quality factors exceeding 5000[65] and are to be used in this research to measure how Au MEMS devices will affect the resonator Q when they are switched on. The high Q of the resonators will allow them to be extremely sensitive to any loss the MEMS switches may introduce into the device.

3.5.2 Tunable Resonator Design and Simulation

A tunable superconducting microstrip gap resonator has been designed to operate at 15 GHz and be tuned by 1 GHz when the switches are operated. A half-wavelength, loaded-line implementation based on work done by Pothier et al.[66] was chosen because of the ease at which MEMS switches can be integrated into the design. The resonators were fabricated on 300 μm high resistivity ($> 5\ k\Omega$) Si substrates (double sided polish) with 1000 Å of SiO_2thermally grown on both sides. The fabrication process was similar to that presented in Section 2, except since SOI was not used, the bonding and thinning steps were unnecessary. This also meant that the ground plane (Nb/Au, 4000/300 Å) had to be sputtered on the backside of the wafer before release. The transmission lines are made of 4000 Å of Nb capped

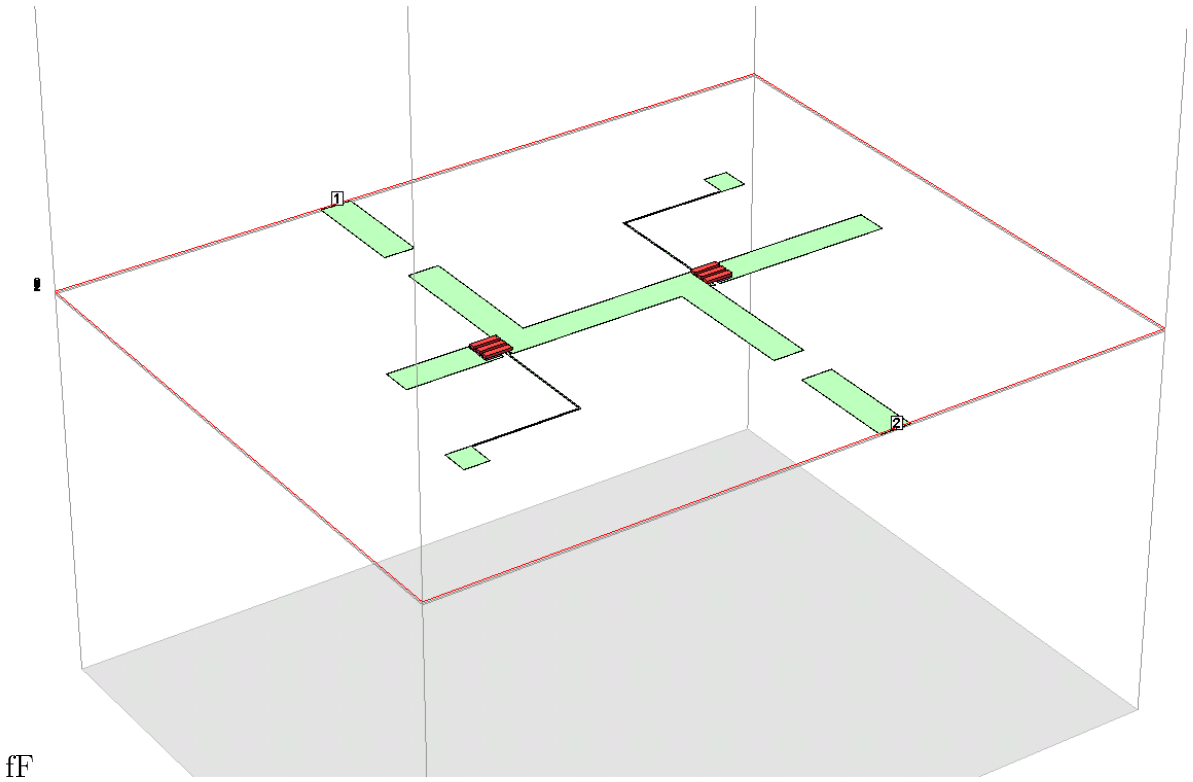


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Figure 3.18: Sonnet image of Tunable Resonator design. Three MEMS switches are utilized in parallel for each stub to minimize reflections at RF frequencies since the transmission lines are wider on the thick Si substrate.

with 300 Å of Au to prevent the Nb from oxidizing. The transmission lines are 240 μm wide have a characteristic impedance of 50 Ω. The central section has a total length of 3.408 mm with two bends, each with an arm 1.032 mm in length extending to a 200 μm gap in the microstrip. A signal will enter one port, couple across the gap and resonate in the central section and then couple to the output port. The gap size is chosen so as to balance the ability to build a resonance by not coupling energy out of the central section, while allowing enough of the signal to cross the gap. If the gap were too big, no signal would couple to the resonator, and if the gap were too small, the two much of the signal would leak out of the output port. Two different loads can be switched in either separately or together enabling the resonator to be tuned to four different frequencies. The longer the stub, the lower the resonance frequency can be shifted. The longer stub is 1.368 mm while the shorter stub is 0.744 mm and they will tune the resonator by 1 GHz. The electromagnetic simulator Sonnet

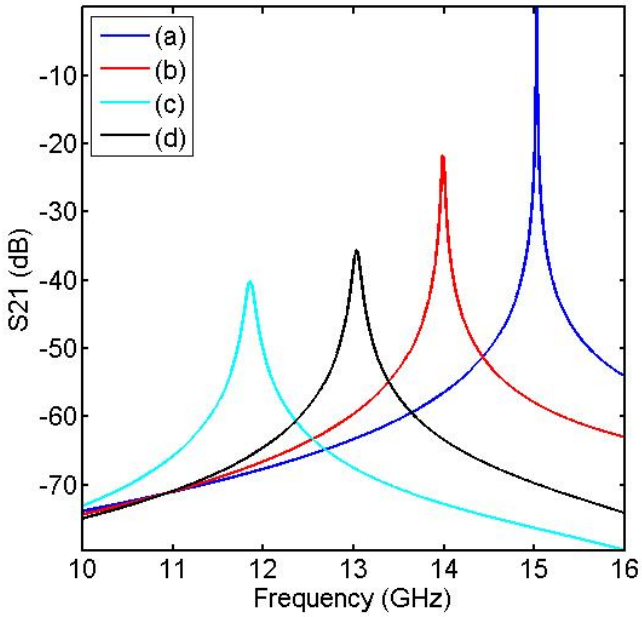


Figure 3.19: ADS simulations of the Tunable Resonator. Case (a) is all switches up - Q = 4291 (15 GHz) (b) one set of switches up (14 GHz), the other down - Q = 501 (c) opposite configuration to (b) - Q = 188 (13 GHz) and (d) all switches down - Q = 127 (12 GHz).

was used to determine the initial dimensions of the resonator and ADS was used to model the RF MEMS switching in the tuning stubs. The ADS simulation results for the four possible resonant states are presented in Figure 3.19. The simulation shows that drop in Q will be observed when the tuning stubs are switched in and the lossy MEMS can have a large impact on the performance of the circuit. The MEMS switches are modeled as shown in Figure 3.14. To model a switch in the up-state, an up-state capacitance of (1 fF) was used, while for a switch in the down-state, R_C (1 Ω) was used. From the simulation results the Q-factor for each switch state can be determined by measuring the full width at half maximum, 3 dB down from the resonance peak. For measured data this means that the Q values reported are approximate since there are fewer data points and the exact 3 dB point may not be able to be determined as precisely as simulated data. We can see from the simulation in Figure 3.19 that the MEMS do indeed reduce the Q of the resonator as the tuning stubs are switched in.

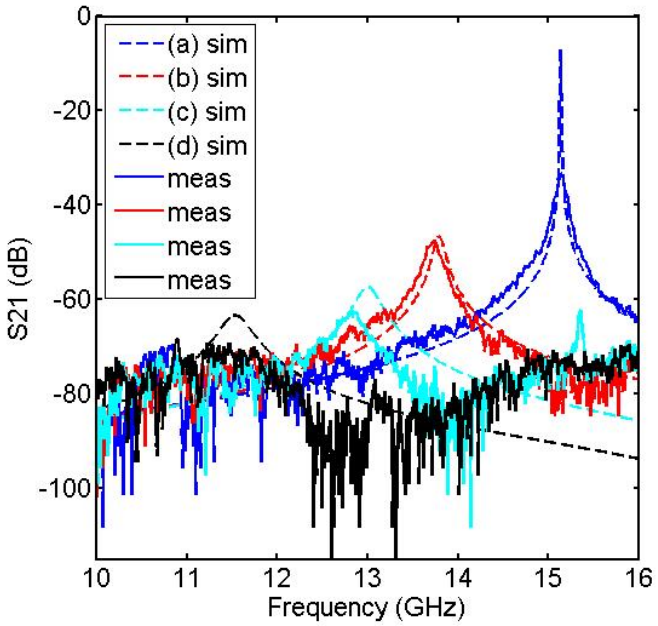


Figure 3.20: ADS models (dotted lines) of the Tunable Resonator with measurements (uncalibrated) overlaid (solid lines). The measured Q values are: 202 ($15\,GHz$), 92 ($14\,GHz$), and 48 ($13\,GHz$), while the resonance at $12\,GHz$ has been damped below the noise floor.

Figure 3.20 shows that the measured resonances are even more lossy than what the original simulations predicted. HFSS models of the resonator (Figure 3.21) show that the microstrip gaps are radiating, causing the reduction in resonator Q. A model of the microstrip gap was built HFSS including radiation (which cannot be modeled in ADS) and the data exported into the ADS circuit model. The measured Q is generally higher for the measured data than simulated, suggesting that the gaps are radiating, just not as much as is predicted by HFSS. There is one notable difference between the data in Figure 3.20 and the simulation in Figure 3.21; the missing peak in the measured data at $12GHz$. An increase in the contact resistance could could be one possible explanation for such a dampening of the resonance. If there was debris underneath any of the 6 switches in the circuit, it would result in a higher contact resistance for the particular resonance that was tuned by that switch, reinforcing how sensitive superconducting circuits are to lossy RF MEMS devices.

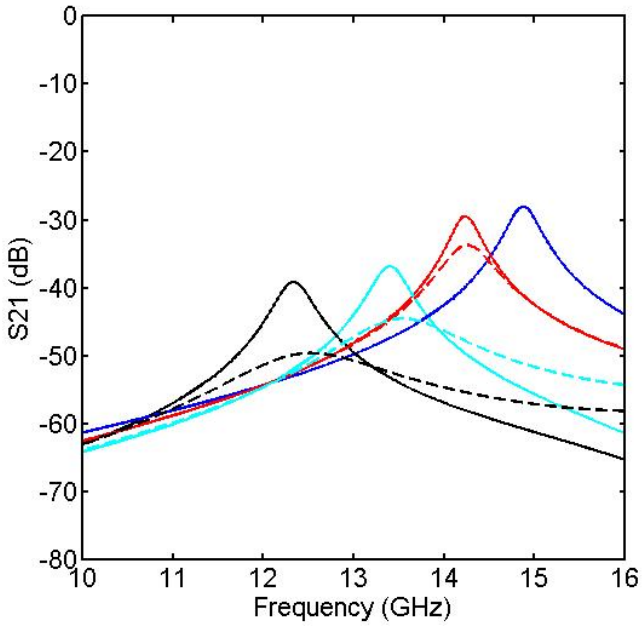


Figure 3.21: HFSS simulation of a microstrip gap resonator showing how a radiating gap (solid lines) degrades the Q to 62 ($15\,GHz$), 57 ($14\,GHz$), 45 ($13\,GHz$), and 36 ($12\,GHz$). The dashed lines are the same simulation with the contact resistance increased to $15\,\Omega$ to demonstrate how the resonance can be damped by a large contact resistance.

Chapter 4

RF MEMS: Cryogenic Reliability Study

Space or balloon based operation of a polarimeter would require the continual switching of MEMS devices for the extent of the scientific mission. The length of such an endeavor could be on the order of years, requiring the the MEMS switches to actuate for an extended period of time and maintain their performance characteristics to prevent the introduction of errors to the CMB measurements. ADS simulations of RF MEMS switches were carried out to better understand how a degradation in contact resistance would affect device performance and are summarized in Figure 4.1. It can be seen that generally the phase switches can be expected to lose 0.15 - 0.25dB just by a 1Ω increase in the contact resistance. This is entirely possible if the dimple contacts on the MEMS device degrade as the switches are actuated, so a cryogenic reliability study was designed and implemented in order to have a better understanding of switch performance over time. Cryogenic operation should be beneficial for MEMS switches due to changes in the mechanical properties of Au as the temperature decreases. The hardness of the Au will increase as temperature decreases, helping to prevent wear[24]. Young's modulus will also increase, helping to stiffen the beam and increase the restoring force, making it less likely to stick to the contacts[46, 67]. Furthermore, the resistance of Au decreases with temperature which will manifest as a decrease in the contact resistance. Other effects can detract from switch operation such as an increase in the pull-down voltage due to a CTE mismatch between the Au and substrate material[46], contamination from condensate within the test chambers on the contacts leading to stiction[24], as well as dielectric charging that will be discussed in this section.

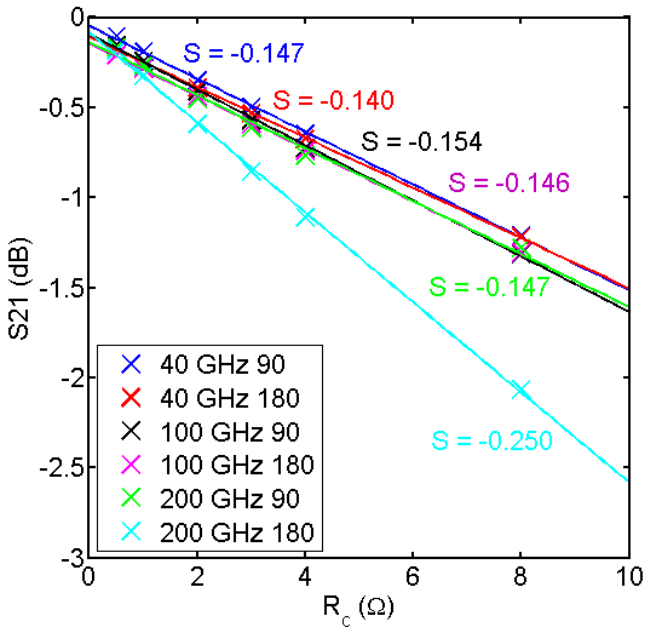


Figure 4.1: Simulated performance of 90° and 180° phase switch designs at $40GHz$, $100GHz$, and $2000\,GHz$ as a function of contact resistance.

Typical failure mechanisms for RF MEMS switches reported in the literature are charging of substrates and dielectrics (used to insulate the beam from the actuation pad), contamination of the contacts causing an increase in contact resistance, plastic deformation of the beam supports[68]. All these scenarios can lead to what is known as stiction - when the MEMS device becomes stuck to the substrate. Stiction can occur for various reasons and is a general catch-all phrase for any time a MEMS beam becomes stuck to the contact/actuation pad. Stiction can occur after the release etch step if the devices are not properly dried using a critical point dryer to instantly vaporize the surrounding medium. Otherwise the capillary force of the liquid as it dries pulls the beam down, causing it to stick. It can be caused by contamination or local heating melting the contacts together[69, 70]. Descriptions of charge injection and contamination failure mechanisms are discussed below.

Charge injection into dielectrics (either a protective dielectric above the bias pad or into an insulating substrate below it) leads to a permanent voltage across a MEMS switch and has been intensely studied[23, 71, 72]. If the voltage becomes greater than the hold-down

voltage of the switch then the switch will become permanently held down to the contact. Furthermore Czarnecki showed that an uneven charge distribution can also cause the switch to close because the E-Field can locally create enough force to collapse the beam or hold it down after it has been actuated[73]. The charge density as a function of time and voltage is:

$$Q = \sum Q^J \left[1 - e^{-t_{ON}/\tau_{ON}}\right] e^{-t_{OFF}/\tau_{OFF}} \tag{4.1}$$

where t_{ON} and t_{OFF} are the applied voltage times, τ is the charge and discharge time constant, and Q^J is the steady state charge:

$$Q^J = Q_o e^{V/V_O} \tag{4.2}$$

Where Q_o and V_o are fitted parameters and J refers to different voltage levels[74]. As can be seen from Equation 4.1 the buildup of charge density can be slowed by modifying the voltage waveform that is sent to the device (ie, on-time, off-time, as well as using positive and negative biasing to balance the charge). Goldsmith also reported that the charging is much greater for positive biases than a negative bias. Once charge is injected into a substrate or dielectric, the only way to remove it is to allow it to bleed out with time constant τ.

When the contacts become contaminated (Hydrocarbons, or water vapor for example) the contaminants at the contact interface can weakly bond the device in the down state. As long as the strain energy density of the beam G is greater than the interface energy density Γ_i then the beam will break loose from the weak bonds and return to its initial up-state. The strain energy density for a cantilever is defined as:

$$G = \frac{stored\ strain\ energy}{contact\ area} = \frac{U_{beam}}{A_c} \tag{4.3}$$

The stored strain energy can be calculated from:

$$U_{beam} = \int_0^L \frac{M^2}{2EI} dx \tag{4.4}$$

where x is the distance from the tip of the beam, $M = Fx$ is the maximum moment of bending of the beam with $F = ky$, k is the spring constant of the beam, y is the maximum deflection of the beam, L is the length of the beam, E is Young's modulus of the beam material and,

$$I = \frac{wt^3}{12} \tag{4.5}$$

is the moment of inertia of the cantilever. Substituting I and k (from Equation 1.18) into Equation 4.4 and integrating yields

$$U_{beam} = \frac{8Ey^2wt^3}{9L^3} \tag{4.6}$$

For an Au beam ($E = 78\,GPa$) with $L = 75\,\mu m$, $w = 40\,\mu m$, $t = 2.2\,\mu m$, and max deflection $y = 0.6\mu m$ we get $G =\sim 200 mJ/m^2$, which is more than enough to overcome $\Gamma_i \leq 50 mJ/m^2$ reported for room temperature operation[75].

4.1 Reliability Test Apparatus

4.1.1 Experiment Design

The reliability study was designed to run over a multiple day span in order to achieve 100 Million switch cycles. Use of a cold cycle cryostat was required in order to keep the switches at $4\,K$ over the course of the test. A Keithley 2700 multimeter (with a 7700 DAQ module) was programmed to take a four-point resistance measurement of ten MEMS switches in the down state when they were actuated by a Keithley 2635A sourcemeter. The chamber would be pumped to below 10^{-4} Torr and then the cryo-cooler would be switched on to bring the

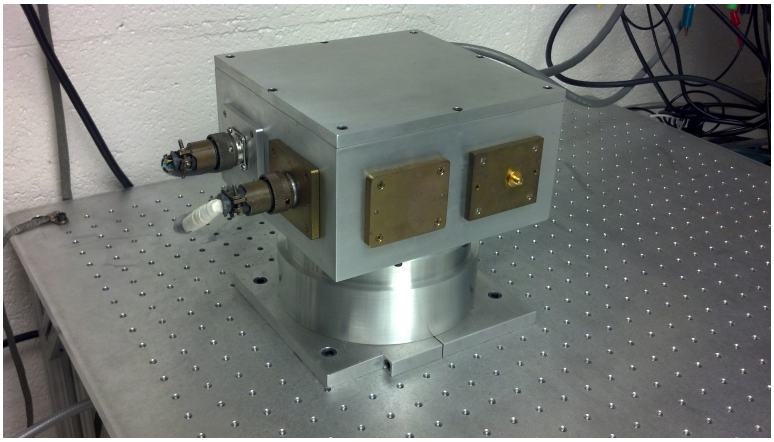


Figure 4.2: Closed Cycle Cryostat

sample to $4.2\,K$[1]. Once cooled, the voltage was ramped to find the pull-down voltage of the switches and make sure they were operating correctly by cycling them above the pull-down voltage five times (typically $80\,V$). The switches were then actuated 100 times, measuring the resistance on each contact after which they were checked for stiction by measuring R_C with $0\,V$ applied bias. Then they would be cycled another one million times, checking for stiction every 100 thousand contacts. This pattern would be repeated for a total of 100 million contacts.

4.1.2 Test Block Design

The fixture to hold the devices was milled out of copper for the best thermal conductivity to help cool the devices to $4\,K$. The block separates into two parts: The lower part has a channel in which the DUT sits while the upper block has a smaller delrin block with pogo pins that clamp down on the DUT to make the requisite electrical connections. A temperature sensing diode was mounted on the side of the bottom block, as close to the DUT as possible, to monitor its temperature over the course of the experiment. Additional temperature sensors were installed on the cold stage ($4\,K$) of the cryostat and the shield stage ($\sim 30\,K$) as well.

[1]Thermal loading of the cold stage from all the wiring was often too much to cool the sample to $4.2\,K$ but the system was routinely able to reach temperatures below $6\,K$.

(a) (b) (c)

Figure 4.3: (a) Test block assembled (b) Pogo pins (c) Sample sitting in the bottom of the block

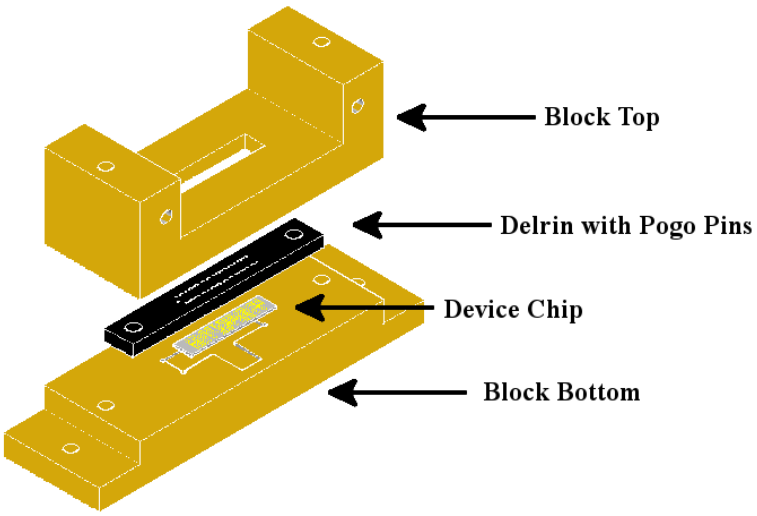


Figure 4.4: 3D Schematic of reliability study test blocks fitting together.

4.1.3 Reliability Study Chip Design

It was desired to have many devices were tested in parallel because the time to complete an experimental run with 100 million contacts would take a relatively long time, however, the more devices that were tested, the more connections to the device chip would be required. More connections would present a higher thermal load to the cold stage while too few devices would be impractical for making generalizations about the reliability of the switches. Ten switches would require 50 feed-through connections (48 for four-point measurements and 2

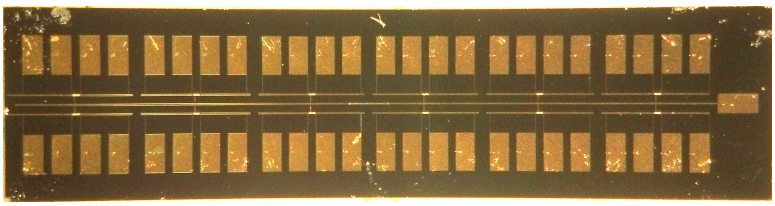


Figure 4.5: Microscope image of the reliability study device chip.

for biasing) which suitably trade off the desire for less connections with the ability to test as many switches as possible. To further reduce the number of inputs, all of the switches were designed to be operated at the same time by the same bias control. However, this meant that if one device failed during testing by contacting the bias line, then none of the switches would actuate. A fail-safe fuse was build into the bias circuit to effectively remove any shorted devices. The fuse was a thinner section of the bias line that would melt when high current flowed through it, thus eliminating any shorted devices from the bias circuit. To reduce the effect a decrease in temperature has on increasing the pull-down voltage, the bias pads were widened under the beam to $30\,\mu m$ (as opposed to $20\,\mu m$ for the RF devices described in Section 3. This decreased their pull-down voltage at room temperature to $50\,V$ while cryogenically they would typically pull-down between $60 - 70\,V$. This variation is due to differences in beam thickness caused by process variation across the wafer during the beam electroplating. The spring constant of the beam scales as the thickness of the beam cubed, thus small differences in the thickness can cause a large variation in the pull-down voltage. These beams also had wider dimples ($4\,\mu m \times 4\,\mu m$) than their RF counterparts ($2\,\mu m \times 2\,\mu m$ to ease the fabrication process.

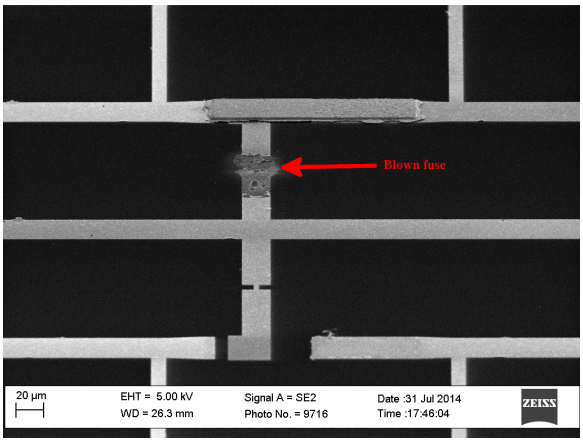


Figure 4.6: Reliability study device chip with a blown fuse due to shorted MEMS switch.

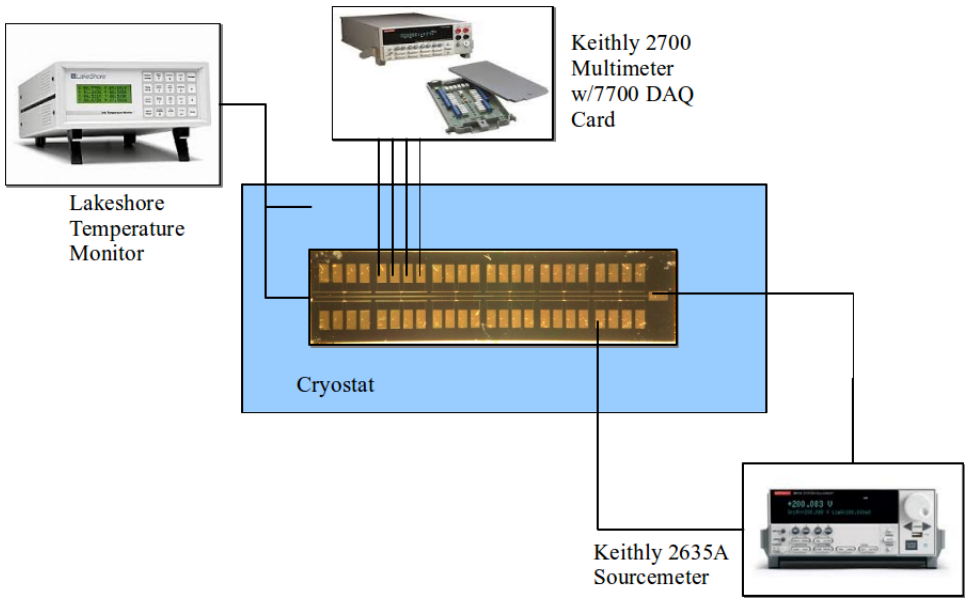


Figure 4.7: Reliability study experimental setup.

4.2 Reliability Study Results

4.2.1 Device Failure

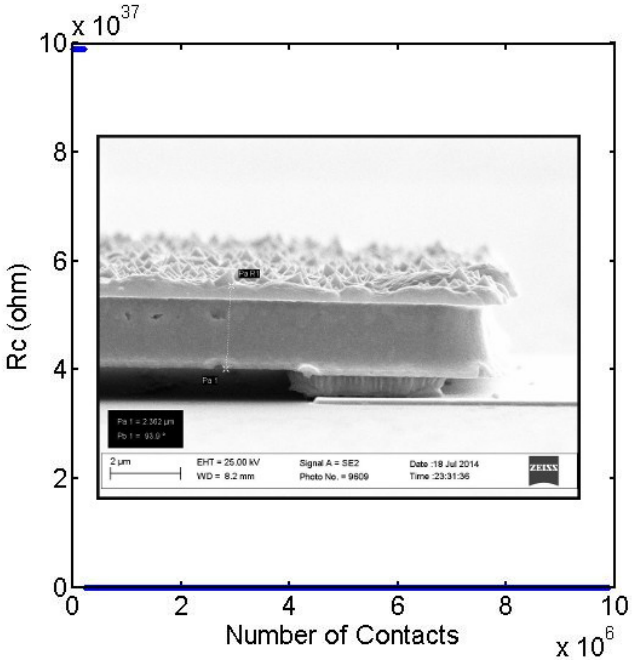
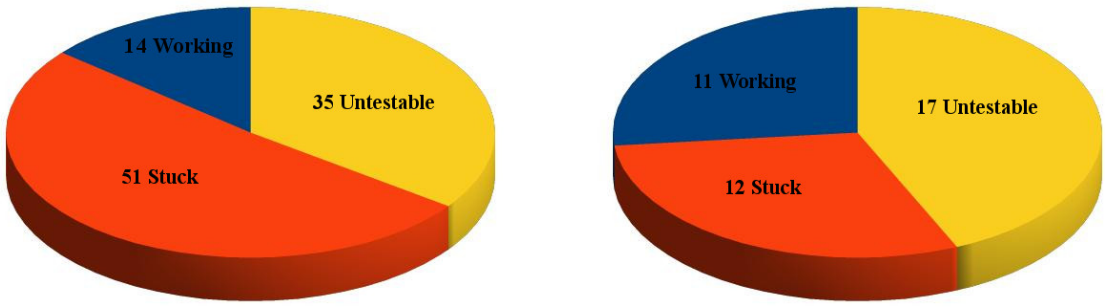


Figure 4.8: Measured contact resistance with $0\,V$ applied bias across the switch. A large R_C implies that the switch is open and operating correctly. This switch is stuck in the closed state after 6 million contacts.

Initial testing resulted in devices failing much earlier than expected. Out of 100 switches tested, very few devices remained operable past a few million contact cycles (6 million was the maximum) and many devices even after their very first contact (Figure 4.9). One further drawback during reliability testing was the loss of electrical connections to some of the switches during cooling. The tolerances for the pogo pin placement was very tight ($\pm 0.5 mil$) and if a pogo pin happened to land on the edge of a contact pad, it could slide off the pad as the system cooled and the delrin the pins were mounted in shrank. To inspect the devices after testing, a DC test probe was used to carefully bend back the beams to inspect the contact dimples. It was determined that the failure mechanism for devices that failed on their first contact was contamination of the contacts and bottom of the beam by thermal grease used to thermally anchor the chip to the test block (Figure 4.11). The application



(a) (b)

Figure 4.9: Testing statistics for 10 samples (100 switches) that were tested. (a) 14 switches were working when testing began, 51 stuck down while finding the V_P before testing began, and 35 were untestable due to poor pogo pin contact. (b) Subset of 30 switches tested after removing grease from the system, increasing device yield.

of too much grease to the underside of the chip as well as to the interface where the block comes together caused grease to seep to the top of the chip. It is believed that vibrations from the vacuum pump and cryo-cooler then spread the grease over the whole sample where it could adhere to the devices. The whole block assembly was disassembled and cleaned with degreaser and organic solvents. When put back together, thermal grease was only applied to the block near the holes for the attachment screws (shown at the edges of the block in Figures 4.3b & 4.3c). Grease was also sparingly applied to the underside of the test chip to keep the surface clean.

Devices that were operating at the beginning of the test had clean contacts and these contacts showed very little signs of wear that could cause stiction (Figure 4.12). Further investigation found that these switches would actually become unstuck after the system was warmed back to room temperature and could be operated again provided grease never reached the contacts. This is atypical of most stiction failure mechanisms, i.e. when a beam becomes stuck, it doesn't have the energy to overcome the bond that is holding it to the contact. Two known phenomena can account for such behavior: A contaminant that is in the liquid or solid phase at $4.2\,K$ which holds the device down and releases it as it returns to the vapor phase when warmed, or dielectric charging of the substrate holding the beam

down until the charge bleeds off and he device is restored.

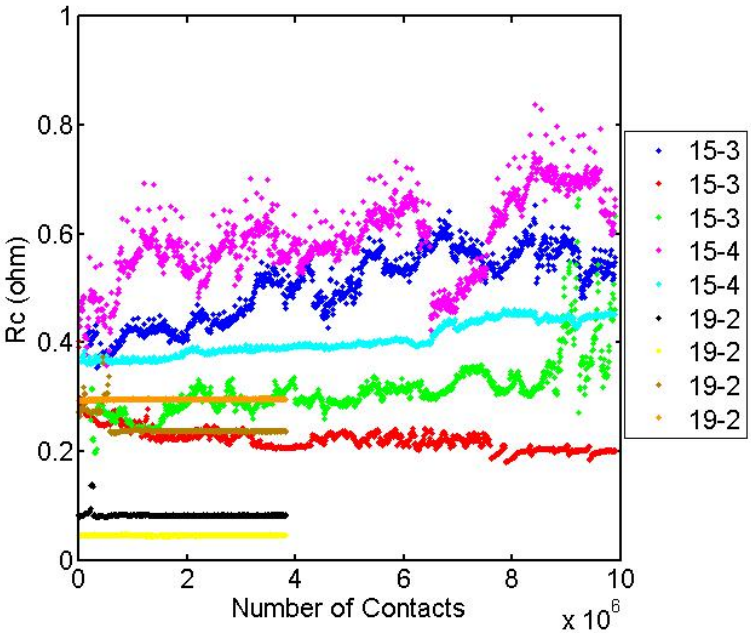
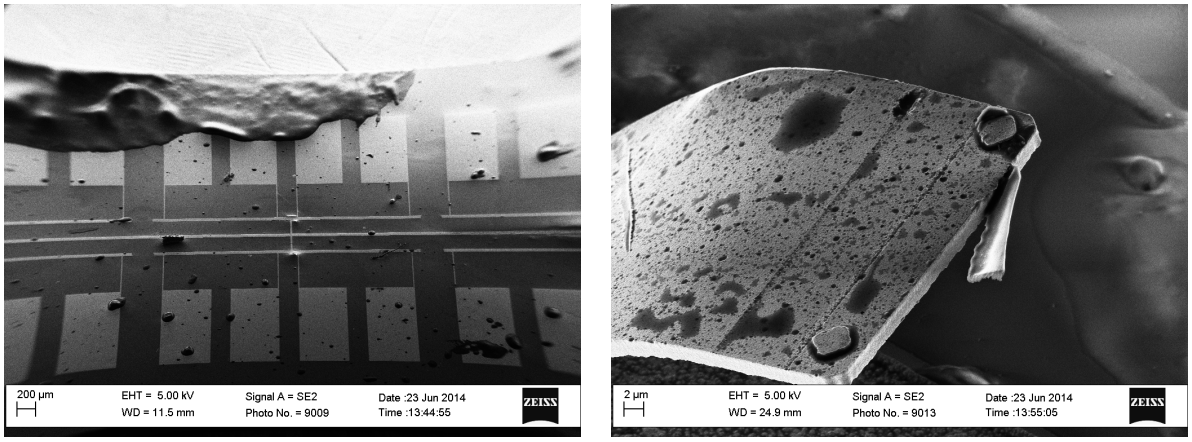


Figure 4.10: Contact resistance of stuck devices show bounds on the consistency of the measurement equipment. The legend indicates Wafer# - Chip#. The test for sample 19-2 was halted early after devices failed.



(a) (b)

Figure 4.11: (a) Thermal grease used to help anchor the test block and the contaminating the test chip. (b) Peeled up beam after testing showing grease covering the contacts.

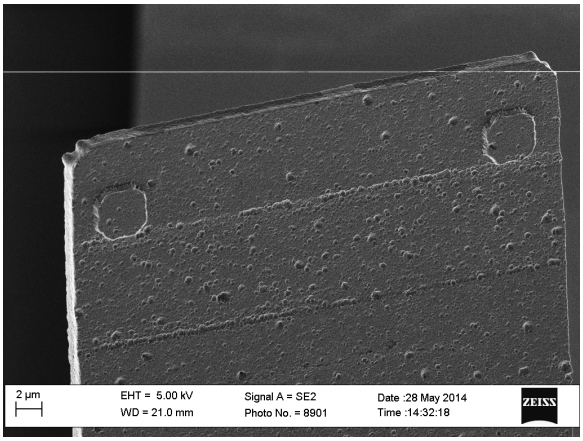


Figure 4.12: Clean dimple contact of a switch that failed after 6 million cycles.

4.2.2 Condensation

The major components of air (nitrogen and oxygen) condense at 77 K and 90 K and freeze at 63 K and 54 K respectively. This means that most of the residual gas (air) in the camber will condense and freeze onto the surface of the cold stage (and the sample) as it cools. Any residual water in the chamber will also freeze on the surface. There are methods for avoiding this condensate such as making sure that a shielding stage (surrounding the sample stage to block thermal radiation) cools below 77 K before the sample stage so most of the gas condenses on the shield first. Unfortunately the closed cycle cryostat used in this research is not presently equipped to do this. Thus the possibility of condensation coating the contacts and leading to stiction failure should be considered. It can be shown that the time required to form a monolayer thick film from a gas (at temperature $T\,(K)$ and pressure $P\,(torr)$) on a completely clean surface is[49]:

$$t_c = \frac{2.85 \times 10^{-8}}{P}\sqrt{MT} \tag{4.7}$$

where M is the molecular weight of the molecule. For the closed cycle cryostat at $P \sim 10^{-5}\ torr$ and $T = 295\ K$ before cooling $t_c = 0.26\ s$ so there is already contamination on the surface before reaching 4 K (where, $t_c = 3.4\ s$). However, this is not an issue for

MEMS operating at room temperature and in fact, operating MEMS in vacuum is preferred to prevent hydrocarbon contamination from reaching the contacts[76]. When cooled, the residual gas in the chamber condenses. If all the gas in the chamber were to condense on the cold stage (not true in reality but it will set an upper bound here) and freeze, the number of gas molecules in the condensate would be equivalent to the number of molecules in the gas before cooling, which can be calculated using the ideal gas law:

$$n = \frac{PV_{chamber}}{RT} \tag{4.8}$$

which for the pumped chamber (dimensions $0.2\,m \times 0.2\,m \times 0.1\,m$) $n = 1.28 \times 10^{-7}\,mol$. The thickness of a frozen layer can be found by dividing the layer's volume by the surface area of the cold stage. Assuming the layer is mostly nitrogen, we can calculate the volume of the condensate V_{solid} using the density of solid nitrogen ($\rho = 500\,kg/m^3$ at $29\,K$[77]) and the ideal gas law:

$$V_{solid} = \frac{Mn}{\rho} = \frac{MPV}{\rho RT} \tag{4.9}$$

at $4\,K$ and $10^{-7}\,torr$ (after cooling). The molecular weight of N_2 is $0.028\,kg/m^3$ so using Equation 4.9, the solid layer is only 2 Å thick across the entire cold stage. This is of course a simplification because the sample chip sits inside the test block which might be at a higher pressure than the surrounding chamber due to outgassing or difficulty pumping out such a small space. In addition, the cantilever beam could shadow the contacts from any gas molecules impinging on the sample (they would hit the top of the beam first) so any molecules that got under the contacts would have to diffuse across the surface, which at $4\,K$ they would have very little energy to do. In any event, if condensed air was keeping devices stuck to the substrate, it should release the devices as soon as the temperature reached above $77\,K$ (when liquid nitrogen evaporates) which was not observed (Table 4.1).

Switch	Temp at Release (K)
28_3-2	244.87
28-3-3	40.92
28-3-10	178.32

Table 4.1

4.2.3 Substrate Charge Trapping

At $4\,K$, any charges injected and trapped in the substrate would have thermal energy $kT = 3 \times 10^{-4}\,eV$ which is orders of magnitude below the energy of some known trap states in SiO_2[78, 79]. Thus at such low temperatures, charges that become trapped in dielectrics are likely to experience long discharge times because the charge carriers don't have the thermal energy to dissipate. This would cause charge to build up even faster than at room temperature leading to early device failures. Modifying the biasing waveform and using bipolar actuation are very effective ways of extending switch lifetime[69]. The Keithley 2635A used to supply voltage for this experiment could only be programmed to output a square wave but could switch back and forth from -80 to $80\,V$, however, this had little effect on increasing the lifetime of devices. It is believed that this is due to differential charging/discharging rates for positive and negative charge carriers in SiO_2 substrates[69]. Changing the substrate from thermally grown SiO_2 to quartz also had little effect on lifetime of the devices.

Figure 4.13: Charging of the substrate causing a voltage to build between the bias and the beam

Switch	# of Contacts	V_P	Switch	# of Contacts	V_P
20_2-5	1	75	28_1-7	1	90
	100	66		100	74
	100000	0		100000	0
20_2-7	1	75	28_1-8	1	200
	100	66		100	200
	100000	0		100100	200
21_2-5	1	60		200000	60
	100	32		200100	13
	100000	0		300000	13
21_2-7	1	60		300100	5
	100	32		400000	4
	100000	0		400100	4
25_2-5	1	75		500000	1
	100	70	28_1-9	1	200
	100000	0		100	200
25_2-7	1	75		100100	200
	100	66		200000	200
	100000	0		200100	200
25_2_10	1	75		300000	0
	100	70	28_2-7	1	80
	100000	68		100	64
	100100	0		100000	0

Table 4.2: Pull-down voltage shift for various devices. A $0\,V$ pull-down implies the switch is stuck. A value of $V_P = 200\,V$ means that the device was initially not actuating (pull-down never reached).

Devices failing due to charging will experience a shift in the pull-down voltage as charge builds up underneath the actuation pad (Figure 4.13). The more charge that builds, the lower the pull-down voltage will become[23, 80]. Measuring a reduction in pull-down voltage during testing would be a confirmation that charging of the dielectric was occurring. This could be accomplished by ramping the bias voltage and measuring the contact resistance, which would measure an open until the pull-down voltage was reached, at which point the voltage would be recorded. This was added to the measurement program after measuring R_C, then again after cycling every 100 thousand cycles. As Table 4.2 shows, the pull-down voltage was significantly lowered as devices were repeatedly biased and they would fail within the first 1 million contacts. It also suggests that devices which were initially not switching

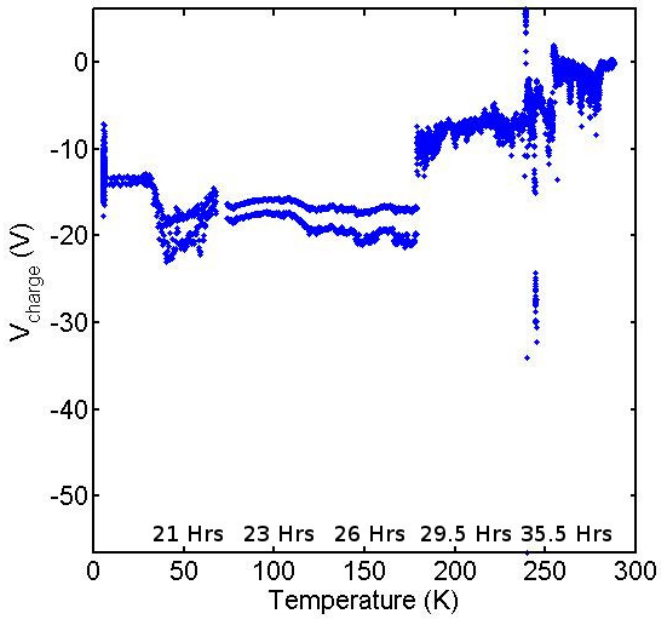


Figure 4.14: Voltage between the bias pad and beam as a function of temperature during testing. It is believed the spikes in the data correspond to vibrations or power surges in the building interfering with data acquisition. The cryostat took 48 hours to warm to 295 K after testing.

because the voltage was never high enough to pull down the beam could eventually be pulled down as charge was injected under the bias pad, as in the case of switch 28_1-8 and 28_1-9.

The testing program was again modified to measure the contact resistance of a new sample (not included in Figure 4.9 or Table 4.2) upon each contact of the beam for 10 thousand contacts with a pull-down voltage of $-80\,V$. After each R_C measurement, the devices were checked for stiction and the voltage due to substrate charge was measured. Four of ten switches were working (three stuck down at the start of the test, and three had bad connections and couldn't be measured) at 6,166 contacts before the cooling compressor overheated (due to an air conditioning issue) and the sample was accidentally warmed to $74K$ before the testing was halted. Even though the devices were working, a shift in the substrate charge voltage was detected over time as the switches were cycled. This shift can be seen at $4K$ in Figure 4.14, where the devices began the test with $-10V$ across them at zero bias and the voltage dropped to $\sim -17\,V$ with subsequent biasing. After halting the test, the devices

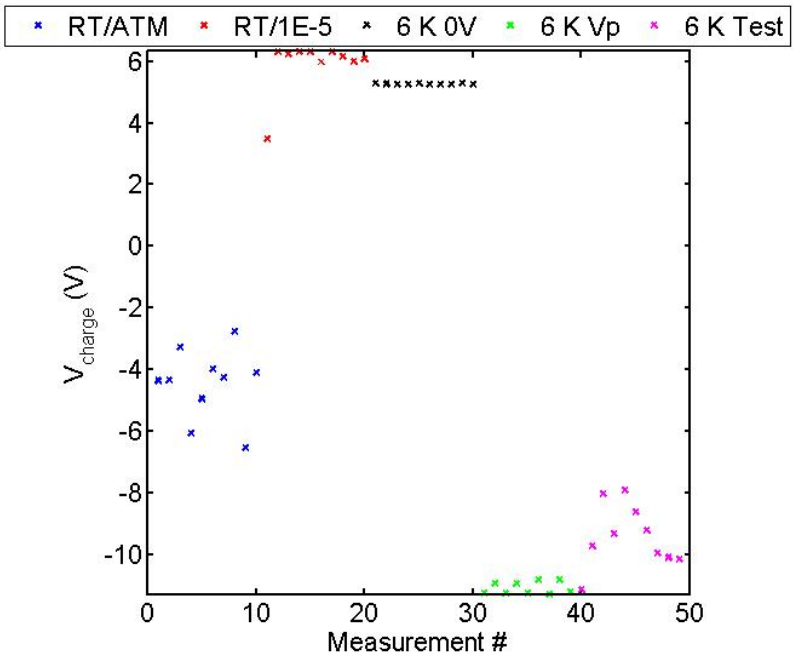


Figure 4.15: First 50 V_{charge} measurements before testing of the devices began. No bias was applied to the devices until Measurement #30 when $V_P = -80\,V$ of the switches was determined. A change in charge level in the substrate corresponding a voltage shift was detected (at Measurement #30).

were monitored for release and allowed to warm to room temperature. During this warming period, trapped charge became mobile and the substrate charge voltage bled off, returning some devices to working condition (Figure 4.14). The sample was then cooled down for more testing, and during this cooling, devices that did not release from the substrate during the previous warming cycle did release when the sample was cooled back down to $4\,K$. It is believed those devices were loosely held to the substrate by contamination and upon cooling, stiffening of the beam caused them to break free from the contact. Additional testing was initiated on all devices, extending the reliability test further by cycling the switches 1000 times before measuring the contact resistance. Three of the switches remained operational out to 500 thousand contacts (Figure 4.17).

Figures 4.16 and 4.17 show that it is possible to have devices that have repeatable drifts in contact resistance. Switches 7 and 9 both have variations in R_C as low as $0.8\,\Omega$ during testing. Switch 10 exhibits a drift in R_C of 5Ω. It is believed that the larger drift of switch 10

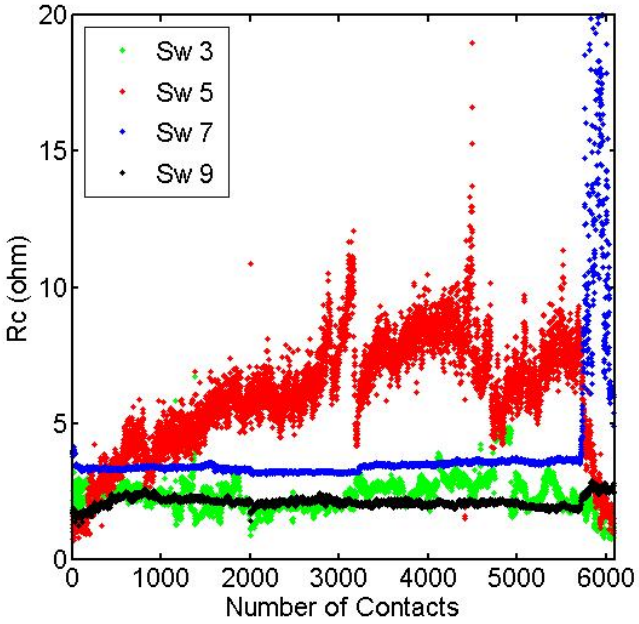


Figure 4.16: Contact resistance of working switches as a function of contact number. The cryostat started warming around 5700 contacts.

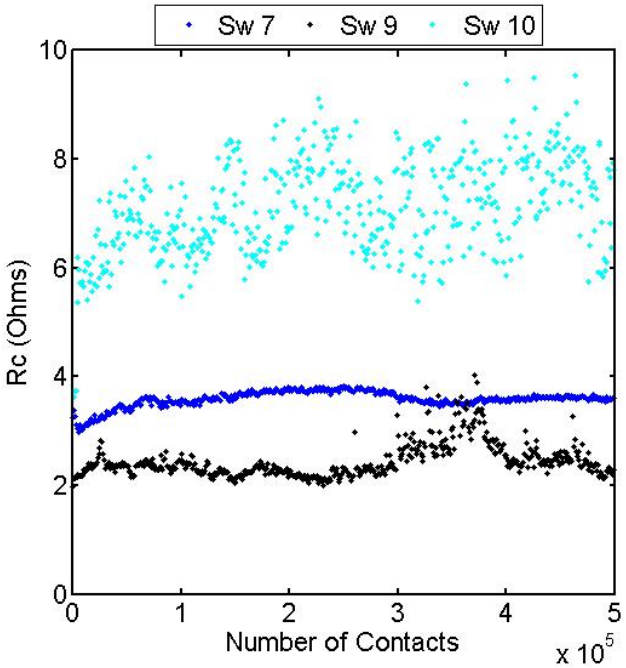


Figure 4.17: Contact resistance of MEMS switches cycled 500,000 times.

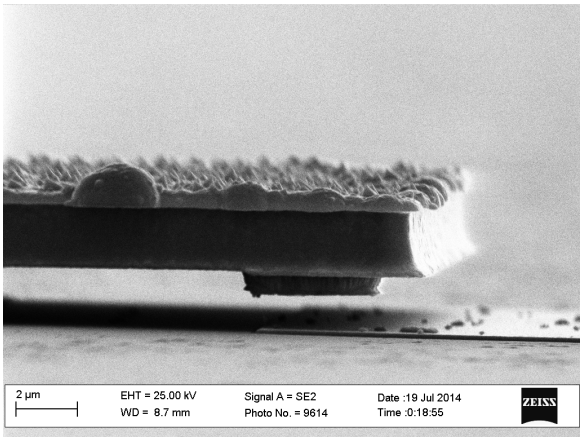


Figure 4.18: Debris particles can be observed underneath a MEMS switch contact.

is caused by some debris underneath the contact, possibly particles of Au left over from the seed layer used to electroplate the beam. When the switch collapses these particles create an inconsistent and less repeatable contact as current can only pass through the particles. The data is encouraging because a shift in R_C of $0.8\,\Omega$ ($5\,\Omega$) corresponds to a decrease in the insertion loss of the switch of $0.12\,dB$ ($0.75\,dB$). This shows that the RF MEMS switches have potential as phase modulators in long-term scientific missions to study the CMB because the increase in insertion loss will only increase the noise temperature of the phase switches to $52\,mK$ ($83\,mK$) and degrade the sensitivity of the overall system to $19\,nK$ ($27\,nK$). The variation of the B-mode polarization could be as low as $30\,nK$ so $5\,\Omega$ looks like the maximum variation in contact resistance that could be tolerated in such a system. Although a positive result, it still demonstrates that there is some work to be done to clean up the fabrication process to try to eliminate debris particles that can cause larger drifts in the contact resistance.

Chapter 5

Conclusions and Future Work

5.1 Summary of Work

This dissertation presents the design, fabrication and measurements of a DC-contact RF MEMS switch fabricated on superconducting transmissions lines and SOI substrates. The cryogenic measurements of the switch show very little DC loss, demonstrating that the fabrication process is capable of producing such structures. The switches were implemented in a microstrip gap resonator which verified that the lossy MEMS will degrade the resonator Q when the tuning stubs are switched into the circuit. Dielectric breakdown of the SOI substrate was found to be an issue for the proper operation of the devices and was solved by the deposition of a thin oxide on the backside of the SOI before MEMS processing. An alternative solution would be the development of a switch with a lower pull-down voltage so that such high fields are not generated during actuation. The reliability of the switches was studied in a cryogenic environment at temperatures close to $4\,K$. Results showed the contact resistance of the switch remains steady over the lifetime of the switch, however, switch lifetimes are severely limited as compared to those found for other devices at higher temperatures. The main failure mechanisms are stiction related and caused by contamination from the fabrication process and substrate charging. A detailed summary of the work presented here is as follows:

- Development of fabrication process for MEMS on SOI substrates and Nb microstrip lines.
  - Integration of Al MEMS process with SOI bonding technology.
    * Weak adhesion of SOI to carrier solved.
    * MEMS Anchor processing optimized.
    * Alternative W Process investigated.
  - Demonstrated working MEMS switches.
  - First time RF MEMS switches have been developed using SOI as microstrip substrate.
  - Substrate dielectric breakdown limits switch V_P.
- Demonstration of loss introduced to superconducting circuits by RF MEMS.
  - Tunable microstrip gap resonators tunable from $12-15\,GHz$ with $\Delta f_c = 1\,GHz$.
  - R_C degrades the resonance Q by at least an order of magnitude.

- Reliability of RF MEMS switches at $4\,K$.
  - 10 Samples tested in total (100 switches).
  - Contact contamination due to thermal and pogo pin contact reduced the yield of measurable operational switches.
  - Dielectric charging was found to be the key cause of early device failure with no devices operating past 6 million contacts.
  - Charge is injected underneath the bias pad and remains there until devices are warmed.
  - Repeatability of RF MEMS contact resistance at $4\,K$.
    * R_C of operating devices ranged between 0 - $10\,\Omega$
    * $\Delta R_C < 5\,\Omega$ was measured out to 500 thousand contacts.
    * ΔR_Cas low as $0.8\,\Omega$ is reported.
    * Debris under the contact is suspected to be the cause of large drifts in R_C.

5.2 Future Work

5.2.1 RF MEMS on SOI substrates

This work opens many avenues for future work in RF MEMS devices at cryogenic temperatures. The testing of phase switches developed in this research was hindered by poor VNA calibration while testing at $4\,K$. An investigation into adhesives for bonding samples to the probe station for more reliable sample cooling could begin with silver paint and extend to other known adhesives with low thermal resistivity.

Dielectric breakdown of the substrate also impeded the testing of RF MEMS phase switches. The deposition of a thin dielectric such as SiO_2 with a higher breakdown strength than Si is one possible method to prevent this problem. Maxwell 3D simulations (Figure

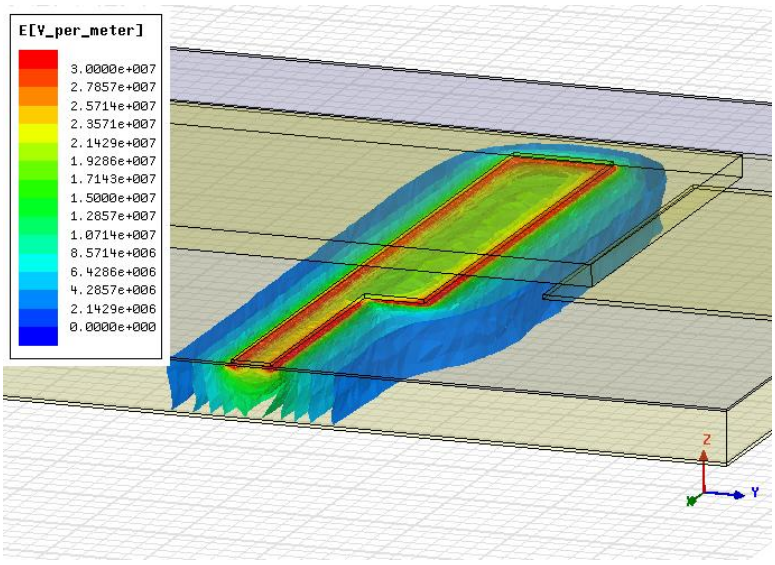


Figure 5.1: Electric field underneath the bias line is reduced in the Si to under $10^7\ V/m$ by the addition of a thin SiO_2 layer.

5.1) show that a 2000 Å SiO_2 layer will reduce the fields in the Si but will not be too thick as to cause a significant reduction in the effective dielectric constant of the substrate[83]. A redesign of the MEMS switch to lower its pull-down voltage would also serve to eliminate substrate breakdown. V_P is dependent on the initial gap height $g_o^{3/2}$, thus reducing the gap is the easiest way to reduce V_P without reducing the spring constant of the beam. However, a reduction in the height of the beam will also increase the up-state capacitance which will decrease the isolation and reduce the RF performance of the switch. The tip of the cantilever can be reduced to compensate for this, since a reduction in area will decrease the up-state capacitance.

5.2.2 RF MEMS Reliability & Repeatability

The 5 Ω drifts in R_C observed during the reliability are believed to be due to Au particles that remain underneath the contacts after fabrication. This contamination issue (Figure 4.18) suggests that there is still some optimization to do on the fabrication process as after device release some debris can be seen on the substrate which could be getting underneath the beam, causing stiction and/or larger drifts in contact resistance. Thermal grease could

also be an issue as it is still used in the system. The grease for holding the sample down could be replaced with silver paste which has been shown to provide better thermal conduction to the sample[59] but is more difficult to remove from the test block.

NASA reports that the mission length of the Beyond Einstein Inflation Probe would be at least one year[11]. Phase switches chopping at a frequency of $1\,kHz$ for a year would need to have a lifetime of over 30 billion contacts. Dielectric charging at cryogenic temperatures remains as a major hurdle to overcome if RF MEMS switches are to be used in CMB studies. The charging results presented here remain mostly qualitative. They demonstrate that charge is building on the substrate and holding the MEMS down but do little to show how that charge builds and what qualities about the substrate can influence charge injection (film stress, film density, trap density, etc). More precise measurements of charging rates and discharging rates as well as an investigation into more advanced actuation waveforms to mitigate charging would be an excellent way to extend this research. Since literature suggests that positive charges build in a dielectric faster than negative ones[69], a potential waveform might actuate the switches at a negative bias for 10 contacts, and then a positive bias for a single contact. Variations on this to find an optimal configuration would be of great benefit to the field. Studies of different dielectrics on device lifetime would also be useful.

Spikes in the voltage across the MEMS device as seen in Figure 4.14 need to be investigated to determine the source of their origin and how to remove them from the measurements. These spikes could be surges in the buildings power system or static charge building from the cold stage that discharges across the MEMS devices. Finally, a more reliable test block design would be of great benefit to further this research. The current block is unreliable at forming a repeatable contact to every device on the test chip when it is loaded into the block. A redesign of the chip with wider contact pads and wider spacing between the pads to account for drifts in the pogo pins would help to alleviate this problem.

Chapter 6

Appendix

6.1 Al-SOI Fabrication Process

- Via Patterning
  - Via Lithography
    - Spin clean new SOI 5 μm SOI wafer with D'Limonene, Reagent Alcohol, and Methanol (DRM Clean)
    - Spin on HMDS 3000 rpm for 30 sec
    - Spin AZ4620 3000 rpm for 30 sec
    - Soft bake at 100 C for 2 min
    - 180 sec exposure at 7 mW/cm^2 in MJB4 aligner
    - 40 sec develop in AZ400K : DI water (1:4)
    - Rinse in DI water for 1 min
    - Blow dry
    - Hard bake at 100 C for 5 min
  - Via Etching
    - Si RIE: 6 min
      - SF_6 = 30 sccm
      - C_4F_8 = 30 sccm
      - RF Power = 40 W

        - ICP Power = 500 W
        - Pressure = 15 mTorr
        - Temperature = 50 C
        - He Backflow = 5 sccm
    - Strip Photoresist
        * Submerge in NMP : Propolyene Glycol (1:1) at 125 C for 10 min
        * Remove from solution and scrub with swab dipped in NMP
        * Rinse in DI for 30 sec
        * Blow dry

- Ground Plane Deposition
    - DRM Clean wafer and load into sputter tool
    - Allow Sputt 3 sputter tool to pump base pressure below 1 x 10^{-7} Torr
    - Ion mill surface for 7 min
    - Nb Deposition (4000 Å)
        * Ar Pressure = 4.20 mTorr
        * Power = 500 W
        * Time = 14:40 min
    - Au Deposition (300 Å)
        * Ar Pressure = 2.70 mTorr
        * Power = 75 W
        * Time = 1:20 min

- Beamlead Definition
    - Beamlead Lithography

    * DRM Clean
    * Spin AZ4330 3000 rpm for 30 sec
    * Soft bake 100 C for 2 min
    * 250 sec exposure at 7 mW/cm^2 in MJB4 Aligner
    * Develop in AZ400K : DI water (1:4) for 25 sec
    * Blow dry
    * Hard bake 5 min at 100 C
    * O_2 Plasma Clean 10 min at 180 W
- Beamlead Electroplating ($\sim 4\,\mu m$)
    * Measure photoresist profile with TENCOR Profilometer
    * Submerge in Technic 25ES Au Electroplating Solution
        · $\pm$20 mA supply current
        · 10 V compliance
        · 0.5 sec step time
        · Time = 1.5 hrs
        · DI rinse for 30 sec
        · Blow dry
- Strip Photoresist
    * Submerge in NMP : Propolyene Glycol (1:1) at 125 C for 10 min
    * Remove from solution and scrub in Ethylene Glycol
    * Rinse in DI for 30 sec
    * Blow dry
- Au Seed Layer Removal
    * HG400 wet etch for 1 min at room temperature

        * DI rinse for 30 sec x 2
    - Nb Layer Removal
        * Nb RIE: 12 min
            · BCl_3 = 40 sccm
            · Cl_2 = 9 sccm
            · RF Power = 80 W
            · Pressure = 50 mTorr
            · Temperature = 50 C
            · He Backflow = 5 sccm
    - Resputtered Au Removal
        * HG400 wet etch for 30 sec at room temperature
        * 30 sec DI rinse x 2

- SOI Bonding
    - Mix Epoxy
        * Epotek 330 (Part a : Part B = 10 : 1)
        * Allow to set under vacuum for at least 30 min
    - DRM clean
    - Dispense 500 μL of mixed epoxy onto carrier
    - Place SOI and carrier into vacuum press and pump for 10 min
    - Press SOI into carrier and heat press to 100 C for 7 min
    - Remove bonded sample from press and swab excess epoxy from edges of SOI using methanol and D'limonene
    - Heat lapping to 100 C

- Press sample in lapping press at 100 C for 1 hr
    - Stack: Glass lapping block/filter paper/sample/silicone/filter paper/glass lapping block

- Handle Thinning
    - Measure total stack height and height of carrier
    - Handle Dicing:
        - Blade Height (mm) = Stack Height - 0.03 +0.450
        - Cut Speed = 3 mm/s
        - Y_{IND} = 0.3 mm
        - Number of cuts = 200
    - Handle RIE: 1 hr
        - O_2 = 2 sccm
        - SF_6 = 20 sccm
        - RF power = 40 W
        - ICP power = 500 W
        - Pressure = 20 mTorr
        - Temperature = 20 C
        - He backflow = 4 sccm
    - O_2 plasma clean at 200 W until epoxy is removed from edge of wafer ($\sim$3 days)
    - Buried Oxide Removal
        - BOE etch at RT for 30 min
        - DI rinse for 30 sec
        - Blow dry

- Circuit Definition
  - Circuit Metal Deposition
    - DRM Clean wafer and load into sputter tool
    - Allow Sputt 3 sputter tool to pump base pressure below 1 x 10^{-7} mTorr
    - Ion mill surface 7 min
      - StandSOI AL MEMS Fabrication Processard Settings
    - Nb Deposition (4000 Å)
      - Ar Pressure = 4.00 mTorr
      - Power = 500 W
      - Time = 14:40 min
    - Au Deposition (300 Å)
      - Ar Pressure = 2.70 mTorr
      - Power = 75 W
      - Time = 1:20 min
    - Cr Deposition (300 Å)
      - Ar Pressure = 2.70 mTorr
      - Power = 150 W
      - Time = 5 min
  - Circuit Lithography
    - DRM Clean
    - Spin LOR 10B 4000 rpm for 45 sec
    - Bake 100 C / 130 C for 30 sec / 30 sec
    - Bake 180 C for 5 min
    - Bake 130 C / 100 C for 30 sec / 30 sec

    * Spin AZ4330 3000 rpm for 30 sec
    * Soft bake 100 C for 2 min
    * Expose at 5 mJ/cm^2 in EVG aligner for 300 sec
    * Develop in AZ400K:DI (1:4) for 2 min
    * 1 min DI rinse followed by 1 min running DI rinse
    * Blow dry
    * Hard bake at 100 C for 2 min
- Circuit Layer RIE
    * Cr RIE: 13 min
        · O_2 = 2 sccm
        · Cl_2 = 60 sccm
        · RF Power = 30 W
        · Pressure = 80 mTorr
        · Temperature = 50 C
        · He Backflow = 5 sccm
    * Au Ion Mill: 5 min
        · Ar = 40 sccm
        · RF Power = 140 W
        · Pressure = 20 mTorr
        · Temperature = 50 C
        · He Backflow = 5 sccm
    * Nb RIE: 12 min
        · BCl_3 = 40 sccm
        · Cl_2 = 9 sccm
        · RF Power = 80 W

        - Pressure = 50 mTorr
        - Temperature = 50 CE
        - He Backflow = 5 sccm
    - Ion mill sample in e-beam evaporator for 45 sec then evaporate 4000 Å Al
    - Circuit Layer Liftoff
        * Acetone ultrasonic at 70 W for 5 min
        * Strip photoresist in NMP / Polyethylene Glycol (1:1) at 125 C for 10 min
        * Scrub in Ethylene Glycol
        * DI rinse
        * Blow dry
        * DRM spin clean

- Sacrificial Layer Deposition
    - Load sample in Turbo Sputt deposition tool and allow to pump at least 3 hrs
    - Deposit Al (6000 Å)
        * Ar Pressure = 10 mTorr
        * RF Power = 43 W
        * Time = 2.5 hrs

- Dimple Layer Definition
    - Dimple Lithography
        * DRM clean
        * Spin AZ5214 4000 rpm for 30 sec
        * Soft bake at 100 C for 2 min
        * Expose at 7 mW/cm^2 in MJB4 aligner for 10 sec

        * Image reversal bake at 100 C for 1:30 min
        * Flood exposure at 7 mW/cm^2 in MJB4 aligner for 20 sec
        * Develop in AZ400K:DI (1:4) for 20 sec
        * DI rinse for 30 sec
        * Blow dry
        * Hard bake at 100 C for 2 min
    - Dimple Liftoff
        * Ion mill sample in e-beam evaporator 45 sec
        * Evaporate Al (6000 Å)
        * Acetone ultrasonic for 10 min
        * Methanol rinse
        * Blow dry
        * DRM clean

- Anchor Definition
    - Anchor Lithography
        * DRM clean
        * Spin AZ5214 1000 rpm for 30 sec
        * Soft bake at 100 C for 2 min
        * Expose at 7 mW/cm^2 in MJB4 aligner for 10 sec
        * Image reversal bake 100 C for 1:30 min
        * Flood exposure at 7 mW/cm^2 for 20 sec
        * Develop in AZ Developer for 20 sec
        * DI rinse for 30 sec
        * Blow dry

    * Hard bake at 100 C for 2 min

- Anchor Etch
    * Al RIE: Surface Oxide Punchthrough: 2 min
        · BCl_3 = 40 sccm
        · Cl_2 = 5 sccm
        · Ar = 4 sccm
        · RF Power = 100 W
        · Pressure = 50 mTorr
        · Temperature = 50 C
        · He Backflow = 5 sccm
    * Al RIE: 15 min
        · BCl_3 = 40 sccm
        · Cl_2 = 5 sccm
        · RF Power = 50 W
        · Pressure = 50 mTorr
        · Temperature = 50 C
        · He Backflow = 5 sccm
    * Cr RIE: 10 min
        · O_2 = 2 sccm
        · Cl_2 = 60 sccm
        · RF Power = 30 W
        · Pressure = 80 mTorr
        · Temperature = 50 C
        · He Backflow = 5 sccm
- Strip resist:

    * NMP:PGlycol (1:1) at 125 C for 10 min
    * Scrub with Ethylene Glycol
    * DI rinse for 30 sec
    * Blow dry
  - Anchor clean
    * AZ400K:DI (1:4) for 10 sec
    * DI rinse 30 sec
    * Blow dry
  - Anchor Electroplating: 1.2 μm
    * Measure anchor profile with TENCOR Profilometer
    * Submerge in Technic 25ES Au Electroplating Solution
      · ± 2 mA supply current
      · 10 V compliance
      · 0.5 sec step time
      · Time $\sim$ 30 min (check rate after the first 5 min)

- Beam Definition
  - Diffusion barrier deposition
    * Cr Depostion (300 Å)
      · Ar Pressure = 2.70 mTorr
      · Power = 150 W
      · Time = 10 min
  - Diffusion barrier etch
    * Anchor Lithography

            - DRM clean
            - Spin AZ5214 4000 rpm for 30 sec
            - Soft bake at 100 C for 2 min
            - Expose at 7 mW/cm^2 in MJB4 aligner for 10 sec
            - Image reversal bake 100 C for 1:30 min
            - Flood exposure at 7 mW/cm^2 for 20 sec
            - Develop in AZ Developer for 20 sec
            - DI rinse for 30 sec
            - Blow dry
            - Hard bake at 100 C for 2 min
        * Cr RIE: 15 min
            - O_2 = 2 sccm
            - Cl_2 = 60 sccm
            - RF Power = 30 W
            - Pressure = 80 mTorr
            - Temperature = 50 C
            - He Backflow = 5 sccm
        * Strip resist in acetone ultrasonic 5 min
            - Rinse with methanol
- Seed Layer Deposition
    * Au Deposition (300 Å)
        - Ar Pressure = 2.70 mTorr
        - Power = 75 W
        - Time = 1:20 min
- Beam Lithography

    * DRM clean
    * Spin AZ5214 1000 rpm for 30 sec
    * Soft bake at 100 C for 2 min
    * Expose at 7 mW/cm^2 in MJB4 aligner for 10 sec
    * Image reversal bake 100 C for 1:30 min
    * Flood exposure at 7 mW/cm^2 for 20 sec
    * Develop in AZ Developer for 20 sec
    * DI rinse for 30 sec
    * Blow dry
    * Hard bake at 100 C for 2 min
- Beam Electroplating: 2.2 μm
    * Measure anchor profile with TENCOR Profilometer
    * Submerge in Technic 25ES Au Electroplating Solution
        · $\pm$3 mA supply current
        · 10 V compliance
        · 0.5 sec step time
        · Time $\sim$30 min (check rate after the first 5 min)
        · DI rinse
        · Blow dry
    * Photoresist strip
        · NMP/PGlycol (1:1) at 125 C for 10 min
        · Scrub with Ethylene Glycol
        · DI Rinse for 30 sec
        · Blow dry
        · O_2 plasma clean at 200 W for 10 min

  - Seed Layer Removal
    * HG 400 (reuse) wet etch for 1 min at RT
    * DI rinse 30 sec x 2
    * Blow dry

- Dice sample to separate on-wafer devices from waveguide chips
- On-Wafer MEMS Device Release (DO NOT BLOW DRY SAMPLE)
  - Cr Removal
    * Transene 1020 Cr etch for 1 min
    * 1% H_2SO_4 for 1 min
    * DI rinse for 1 min
  - Al Removal
    * AZ400K:DI (1:1) for 15 min
    * DI rinse for 1 min
  - Cr Removal
    * Transene 1020 Cr etch for 30 sec
    * 1% H_2SO_4 for 1 min
    * DI rinse for 30 sec
  - Al Clean Up
    * AZ400K:DI (1:1) for 5 min
    * DI rinse for 1 min
  - Cr Clean Up
    * Transene 1020 Cr etch for 30 sec
    * 1% H_2SO_4 for 10 min

        * DI rinse for 30 sec
        * Transfer sample to isopropanol (IPA)
    - Critical Point Dry (CPD)

- Waveguide Device Release Process
    - Mix Epoxy
        * Epotek 330 (Part a : Part B = 10 : 1)
        * Allow to set under vacuum for at least 30 min
    - DRM clean
    - Spin waferbond 200 at 2000 rpm for 30 sec
        * Bake at 120 C for 5 min
        * Bake at 180 C for 5 min
        * Bake at 240 C for 10 min
        * Let sample cool to under 160 C
    - Dispense 500 μL of mixed epoxy onto 4" carrier
    - Place sample and 4" carrier into vacuum press and pump for 10 min
    - Press sample into 4" carrier and heat press to 100 C for 7 min
    - Remove bonded sample from press and swab excess epoxy from edges of sample using methanol and D'limonene
    - Heat lapping press to 100 C
    - Press sample in lapping press at 100 C for 1 hr
        * Stack: Glass lapping block/filter paper/sample/silicone/filter paper/glass lapping block

- Carrier Thinning

- Measure total stack height and height of carrier
- Carrier Dicing:
  - Blade Height (mm) = Stack Height - 0.03 +0.450
  - Cut Speed = 3 mm/s
  - Y_{IND} = 0.3 mm
  - Number of cuts = 300
- Carrier RIE: 1 hr
  - O_2 = 2 sccm
  - SF_6 = 20 sccm
  - RF power = 40 W
  - ICP power = 500 W
  - Pressure = 20 mTorr
  - Temperature = 20 C
  - He backflow = 4 sccm
- O_2 plasma clean at 200 W until epoxy is removed from wafer surface (~ 3 days)

- Strip waferbond in TCE at RT (∼1 day)
- MEMS release (follow steps for On-Wafer MEMS Release)

6.2 W Fabrication Process

- W Deposition
  - DRM clean 2" high-resistivity Si wafer
  - Load sample in Kurt Lesker Sputter tool and pump to $\sim 10^{-6}\,Torr$ range
  - Deposit Cr (300 Å)

        * Power = 300 W
        * Pressure = 300 mTorr
        * Ar flow = 10 mTorr
        * Deposition time = 3:30 min
    - Deposit W (4000 Å)
        * Power = 300 W
        * Pressure = 10 mTorr
        * Ar flow = 10 sccm
        * Deposition time = 30 min

- Circuit Planarization
    - Circuit Lithography
        * PMMA 950A11 Spin
            · 4000 RPM for 45 sec
            · 100 °C for 1 min
            · 130 °C for 1 min
            · 160 °C for 10 min
            · 130 °C for 1 min
            · 100 °C for 1 min
        * Deposit Cr (300 Å) in Kurt Lesker Sputter tool
            · Power = 300 W
            · Pressure = 300 mTorr
            · Ar flow = 10 mTorr
            · Deposition time = 3:30 min
        * Spin AZ5214

        - 4000 RPM for 30 sec
        - Soft bake at 100 C for 2 min
        - Expose at 7 mW/cm^2 in MJB4 aligner for 10 sec
        - Image reversal bake 100 C for 1:30 min
        - Flood exposure at 7 mW/cm^2 for 20 sec
        - Develop in AZ Developer for 20 sec
        - DI rinse for 30 sec
        - Blow dry
        - Hard bake at 100 C for 2 min
- Circuit RIE
    * Cr RIE: 10 min
        - O_2 = 2 sccm
        - Cl_2 = 60 sccm
        - RF Power = 30 W
        - Pressure = 80 mTorr
        - Temperature = -25 C
        - He Backflow = 5 sccm
    * PMMA RIE: 10 min
        - O_2 = 45 sccm
        - RF Power = 150 W
        - Pressure = 30 mTorr
        - Temperature = 20 C
        - He Backflow = 5 sccm
    * Develop PMMA
        - MIBK for 15 sec

        - IPA rinse 30 sec
    * W RIE: 20 min
        - Cl_2 = 30 sccm
        - SF_6 = 10 sccm
        - RF Power = 50 W
        - Pressure = 20 mTorr
        - Temperature = 20 C
        - He Backflow = 5 sccm
    * Cr RIE: 10 min
        - O_2 = 2 sccm
        - Cl_2 = 60 sccm
        - RF Power = 30 W
        - Pressure = 80 mTorr
        - Temperature = 50 C
        - He Backflow = 5 sccm
    * H_2O_2 Wet Etch
        - 5 sec
        - DI rinse 30 sec
- Circuit Deposition
    * Load sample into sputter tool
    * Allow Sputt 3 sputter tool to pump base pressure below 1 x 10^{-7} Torr
    * Ion mill surface for 7 min
    * Nb Deposition (4000 Å)
        - Ar Pressure = 4.20 mTorr
        - Power = 500 W

            - Time = 14:40 min
        * Au Depostion (300 Å)
            - Ar Pressure = 2.70 mTorr
            - Power = 75 W
            - Time = 1:20 min
    - Circuit Liftoff
        * Acetone ultrasonic at 70 W for 10 min
        * Acetone/methanol spin clean

- Anchor Layer Planarization
    - Deposit Cr (300 Å) in Kurt Lesker Sputter tool
        * Power = 300 W
        * Pressure = 300 mTorr
        * Ar flow = 10 mTorr
        * Deposition time = 3:30 min
    - Deposit W (6000 Å) in Kurt Lesker Sputter tool
        * Power = 300 W
        * Pressure = 10 mTorr
        * Ar flow = 10 sccm
        * Deposition time = 30 min
    - Anchor Lithography
        * PMMA 950A11 Spin
            - 4000 RPM for 45 sec
            - 100 °C for 1 min

        - 130 °C for 1 min
        - 160 °C for 10 min
        - 130 °C for 1 min
        - 100 °C for 1 min
    * Deposit Cr (300 Å) in Kurt Lesker Sputter tool
        - Power = 300 W
        - Pressure = 300 mTorr
        - Ar flow = 10 mTorr
        - Deposition time = 3:30 min
    * Spin AZ5214
        - 4000 RPM for 30 sec
        - Soft bake at 100 C for 2 min
        - Expose at 7 mW/cm^2 in MJB4 aligner for 10 sec
        - Image reversal bake 100 C for 1:30 min
        - Flood exposure at 7 mW/cm^2 for 20 sec
        - Develop in AZ Developer for 20 sec
        - DI rinse for 30 sec
        - Blow dry
        - Hard bake at 100 C for 2 min
- Anchor RIE
    * Cr RIE: 10 min
        - O_2 = 2 sccm
        - Cl_2 = 60 sccm
        - RF Power = 30 W
        - Pressure = 80 mTorr

- Temperature = -25 C
- He Backflow = 5 sccm

* PMMA RIE: 10 min
  - O_2 = 45 sccm
  - RF Power = 150 W
  - Pressure = 30 mTorr
  - Temperature = 20 C
  - He Backflow = 5 sccm
* Develop PMMA
  - MIBK for 15 sec
  - IPA rinse 30 sec
* W RIE: 25 min
  - Cl_2 = 30 sccm
  - SF_6 = 10 sccm
  - RF Power = 50 W
  - Pressure = 20 mTorr
  - Temperature = 20 C
  - He Backflow = 5 sccm
* Cr RIE: 10 min
  - O_2 = 2 sccm
  - Cl_2 = 60 sccm
  - RF Power = 30 W
  - Pressure = 80 mTorr
  - Temperature = 50 C
  - He Backflow = 5 sccm

        * H_2O_2 Wet Etch
            · 5 sec
            · DI rinse 30 sec
    - Anchor Electroplating
        * ±2 mA supply current
        * 10 V compliance
        * 0.5 sec step time
        * Time = 20 min
        * DI rinse for 30 sec
        * Blow dry
    - Resist Strip in acetone ultrasonic at 70 W for 10 min
        * Acetone/methanol spin clean

- Dimple Planarization
    - Deposit Cr (300 Å) in Kurt Lesker Sputter tool
        * Power = 300 W
        * Pressure = 300 mTorr
        * Ar flow = 10 mTorr
        * Deposition time = 3:30 min
    - Deposit W (6000 Å) in Kurt Lesker Sputter tool
        * Power = 300 W
        * Pressure = 10 mTorr
        * Ar flow = 10 sccm
        * Deposition time = 40 min

- Dimple Lithography
    - Spin PMMA 950A11
        - 4000 RPM for 45 sec
        - 100 °C for 1 min
        - 130 °C for 1 min
        - 160 °C for 10 min
        - 130 °C for 1 min
        - 100 °C for 1 min
    - Deposit Cr (300 Å) in Kurt Lesker Sputter tool
        - Power = 300 W
        - Pressure = 300 mTorr
        - Ar flow = 10 mTorr
        - Deposition time = 3:30 min
    - Spin AZ5214
        - 4000 RPM for 30 sec
        - Soft bake at 100 C for 2 min
        - Expose at 7 mW/cm^2 in MJB4 aligner for 10 sec
        - Image reversal bake 100 C for 1:30 min
        - Flood exposure at 7 mW/cm^2 for 20 sec
        - Develop in AZ Developer for 20 sec
        - DI rinse for 30 sec
        - Blow dry
        - Hard bake at 100 C for 2 min
- Dimple RIE
    - Cr RIE: 10 min

- O_2 = 2 sccm
- Cl_2 = 60 sccm
- RF Power = 30 W
- Pressure = 80 mTorr
- Temperature = -25 C
- He Backflow = 5 sccm

* PMMA RIE: 10 min
  - O_2 = 45 sccm
  - RF Power = 150 W
  - Pressure = 30 mTorr
  - Temperature = 20 C
  - He Backflow = 5 sccm
* Develop PMMA
  - MIBK for 15 sec
  - IPA rinse 30 sec
* W RIE: 25 min
  - Cl_2 = 30 sccm
  - SF_6 = 10 sccm
  - RF Power = 50 W
  - Pressure = 20 mTorr
  - Temperature = 20 C
  - He Backflow = 5 sccm
* Cr RIE: 10 min
  - O_2 = 2 sccm
  - Cl_2 = 60 sccm

            - RF Power = 30 W
            - Pressure = 80 mTorr
            - Temperature = 50 C
            - He Backflow = 5 sccm
        * H_2O_2 Wet Etch
            - 5 sec
            - DI rinse 30 sec
    - Dimple Lift-off
        * Load evaporator and pump 2 hrs
        * Evaporate 6000 Å Au
        * Acetone ultrasonic at 70 W for 10 min
        * Acetone/methanol spin clean

- Beam Formation
    - Sputter 300 Å Au seed layer
        * Allow Sputt 3 sputter tool to pump base pressure below 1 x 10^{-7} Torr
        * Ion mill surface for 7 min
        * Au Deposition
            - Ar Pressure = 2.70 mTorr
            - Power = 75 W
            - Time = 1:20 min
    - Beam Lithography
        * Spin AZ5214
            - 1000 RPM for 30 sec
            - Soft bake at 100 C for 2 min

· Expose at 7 mW/cm^2 in MJB4 aligner for 10 sec

· Image reversal bake 100 C for 1:30 min

· Flood exposure at 7 mW/cm^2 for 20 sec

· Develop in AZ Developer for 20 secSputter 300 Å Cr

· DI rinse for 30 sec

· Blow dry

· Hard bake at 100 C for 2 min

– Beam Electroplating

* ±5 mA supply current
* 10 V compliance
* 0.5 sec step time
* Time = 50 min
* DI rinse for 30 sec
* Blow dry
* Resist strip: Acetone/methanol spin
* Au Seed Layer Removal

· HG400 wet etch for 1 min at room temperature

· DI rinse for 30 sec x 2

- Ground Plane Deposition

– Load sample into sputter tool backside up

– Allow sputter tool to pump base pressure below 1 x 10^{-7} Torr

– Ion mill surface for 7 min

– Nb Deposition (4000 Å)

* Ar Pressure = 4.20 mTorr

        * Power = 500 W
        * Time = 14:40 min
    - Au Deposition (300 Å)
        * Ar Pressure = 2.70 mTorr
        * Power = 75 W
        * Time = 1:20 min

- MEMS Release
    - H_2O_2 (30%) at 50 °C for 2 min
    - Transene 1020 Cr Etch at RT for 1 min
    - 1% H_2SO_4 for 1 min
    - DI Rinse 1 min
    - H_2O_2 (30%) at 50 °C for 2 min
    - Transene 1020 Cr Etch at RT for 1 min
    - 1% H_2SO_4 for 1 min
    - DI Rinse 1 min
    - H_2O_2 (30%) at 50 °C for 2 min
    - Transene 1020 Cr Etch at RT for 1 min
    - 1% H_2SO_4 for 1 min
    - DI Rinse 1 min
    - Place sample in IPA and transfer to CPD

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