Submillimeter-wave Schottky Diodes Integrated on Micromachined Silicon Probes

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Linli Xie

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This Dissertation
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Author Signature: Linli Xie

This Dissertation has been read and approved by the examining committee:

Advisor: Robert M. Weikle, II

Committee Member: Arthur W. Lichtenberger

Committee Member: N. Scott Barker

Committee Member: Andreas Beling

Committee Member: Steven M. Bowers

Committee Member: James M. Fitz-Gerald

Accepted for the School of Engineering and Applied Science:

Craig H. Benson, School of Engineering and Applied Science

August 2019

Abstract

The submillimeter-wave and terahertz region (300 GHz-3000 GHz) remains one of the the most scientifically useful yet least explored regions of the electromagnetic spectrum. This spectral range is critical for many applications such as remote sensing, radio astronomy, spectroscopy and imaging. However, the measurement infrastructure for developing submillimeter-wave and terahertz devices and materials is often ill-adapted for interfacing to devices for direct in-situ characterization, too large in size, cost-prohibitive, or non-existent. In addressing this issue, the focus of this work is the integration of GaAs Schottky diodes on micromachined on-wafer probes to provide compact, low cost and innovative metrology tools for the submillimeter-wave and terahertz scientific community.

The first part of the thesis focuses on developing a robust fabrication process of heterogeneous integration of Schottky diodes onto silicon substrates. The process aims to simplify the fabrication and improve the yield. The new approach eliminates most thermal processes, including ohmic contact thermal annealing and high-temperature wafer bonding of GaAs epitaxial transfer, that can lead to wafer fracture and delamination. A 160 GHz quadrupler is implemented using the new process to assess its potential.

The second part of the thesis investigates a new approach for on-wafer calibration at submillimeter wavelengths based on GaAs Schottky diodes integrated onto silicon as an electronic standard. Comparison of the error coefficients derived for both one-port and two-port calibration applications, derived using the diode standard are shown to be in good agreement with those obtained from a conventional set of offset short and TRL standards, respectively.

Finally, two implementations of integrating GaAs Schottky diodes onto micromachined

on-wafer probes metrology are described. Probes incorporating diodes for temperature sensing and S-parameters measurement are detailed and designed. The design, fabrication process and measurement plans of these integrated probes are described.

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Chapter 1

Introduction

1.1 Metrology for Submillimeter-wave Spectrum

The submillimeter-wave region (300 GHz-3 THz) is one of the the most scientifically useful yet least explored regions of the electromagnetic spectrum. This region is crucial to remote sensing and radio astronomy, molecular spectroscopy, imaging for medical or security purposes and other applications [17–21]. Unfortunately, the measurement infrastructure for developing submillimeter-wave devices and materials remains limited, too large in size, cost-prohibitive, or non-existent. and is often ill-adapted for direct in-situ characterization.

Among the most important instruments for characterizing RF, microwave and millimeter-wave devices is the vector network analyzer (VNA). The technology of vector network analyzers has been significantly improved since it was first commercially introduced by Hewlett Packard in 1967, the HP 8410. However, it has been less than a decade that VNA measurements of S-parameters have been extended into the terahertz frequency range with external frequency extension modules [22, 23].

Another example of limited measurement infrastructure for terahertz applications is the waveguide and waveguide interfaces. Conceived by Lord Rayleigh in 1897 and rediscovered by G. C. Southworth and W. L. Barrow about fourty years later [24], the past century has witnessed the extensive application of this technology in RF, microwave and millimeter-wave ranges. However, it is found that the measurement precision and accuracy of submillimeter-wave and terahertz range instruments is limited by interconnection quality, repeatability,

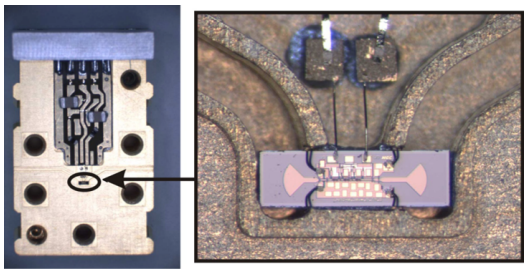
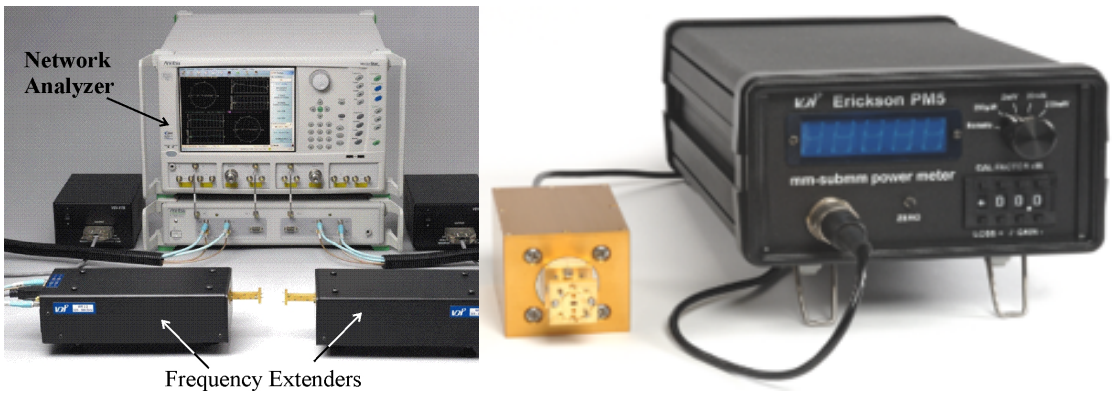


Figure 1.1: An integrated 340 GHz low noise amplifier chip mounted to a waveguide housing for measurement and characterization [1]. The right image is a close-up of the chip mounted to the housing.



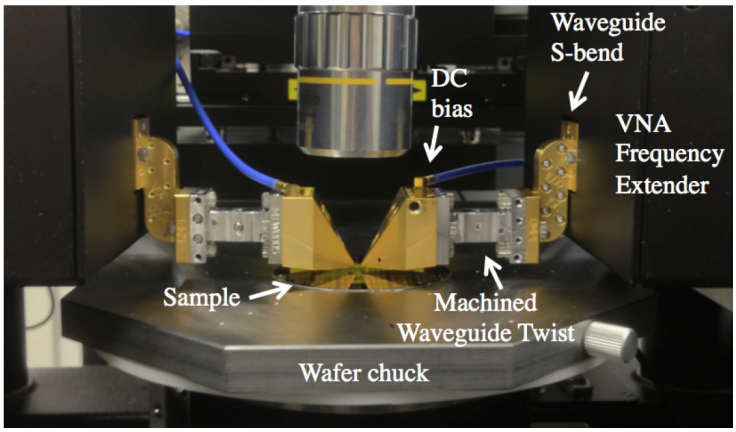
(a) (b)

Figure 1.2: (a) Image of a PNAX vector network analyzer with terahertz frequency extension modules from Virginia Diodes (image courtesy of Agilent, Inc.). (b) Image of a PM5 power meter (image courtesy of Virginia Diodes, Inc.)

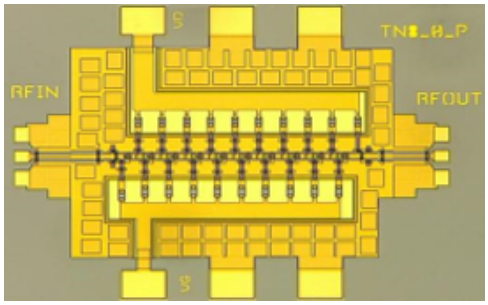
and the lack of traceable standards. Recognition of this issue has led, as a result, to new designs for waveguide flanges [25] and the establishment of a recent IEEE standard P1785 for waveguide interfaces above 100 GHz to at least 1 THz [26, 27].

Figure 1.1 illustrates a common approach to measuring submillimeter-wave and terahertz devices and materials. The device-under-test (DUT) to be characterized is mounted to a test fixture equipped with waveguide flanges that permit interfacing to standard test instrumentation such as a vector network analyzer (Figure 1.2a) or power meter equipped with waveguide flanges (Figure 1.2b).

Mounting of the DUT to a fixture is time-consuming, expensive, and requires de-embedding of the fixture response from the measurement, which is a complex process that limits accuracy and precision. The preferred approach is to measure the DUT *in-situ*, without removing it from its native environment and introducing measurement error due to the



(a)



(b)

Figure 1.3: (a) On-wafer probes interfaced to VNA frequency extenders mounted to large-area positioners (Cascade PA200 probe station [2]. (b) Image of an InP amplifier, developed by Northrup Grumman, that is the first to produce gain at frequencies exceeding 1 THz [3].

fixture. An example is shown in Figure 1.3a, which shows a measurement system equipped with on-wafer probes that permit direct interfacing to planar devices and integrated circuits for characterization on wafer, without need for separating die and mounting them to a housing. The innovation of on-wafer probes developed at the University of Virginia allowed, for the first time, calibrated on-wafer measurement of electronic devices at frequencies over 1 THz and permitted the development and characterization of the world's first terahertz transistor in 2014 (Figure 1.3b) [3].

The prevalent approach for in-situ characterization of submillimeter-wave devices is to measure the device under test (DUT) in-situ with on-wafer probes. However, there is usually considerable overhead associated with this approach. The frequency extender modules that are needed to interface to coplanar on-wafer probes must be mounted to large-area translation stages for positioning and alignment. This places limitations on the number of

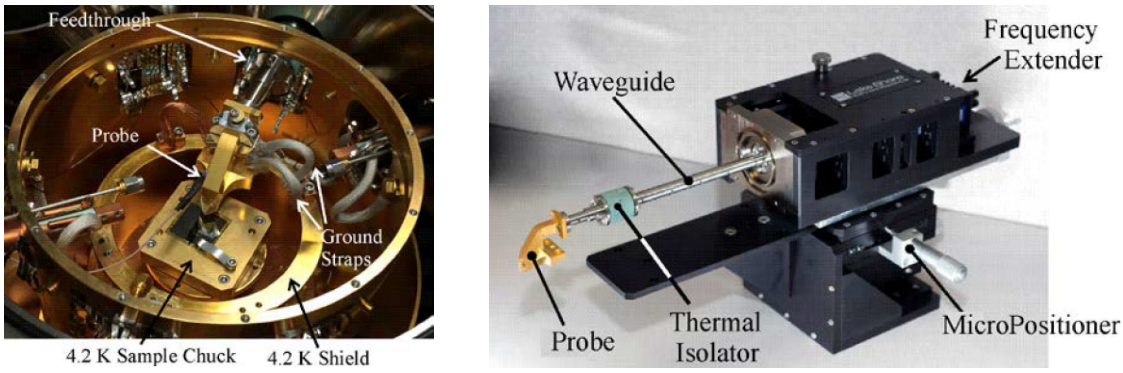


Figure 1.4: Photograph of (a) a cryogenic probe station with feedthroughs for on-wafer probe measurements. (b) Probe feed-through assembly [4, 5].

ports that can be measured practically on a standard probe station, due to the footprint of the extenders and how closely they can be positioned. In addition, measurements of a DUT within a shielded enclosure, such as a vacuum chamber or cryostat, is problematic. Typically, measurement instruments must be placed outside the chamber and be interfaced to the DUT within through hermetically-sealed or thermally-isolated feedthroughs. Thus contributes to system complexity and cost, increases loss, and reduces dynamic range. An example of such as system is shown in Figure 1.4. The submillimeter-wave research community has immediate need for in-situ measurement capabilities as described above, and the work in this dissertation aims to address this issue.

1.2 Micromachined On-Wafer Probes

State-of-the-art micromachining technologies developed at the University of Virginia [6,28,29] has made in-situ on wafer characterization possible up to 1 THz. The SEM image of a WR-1.0 (750-1100 GHz) micromachined probe is shown in Figure 1.5. The micromachined probe is a single, integrated module fabricated from thin (15 μm) micromachined high-resistivity silicon and includes metallized electrical contacts for direct interfacing and physical contact to device under test (DUTs). Figure 1.6 shows a diagram and an example of an on-wafer probe chip for the WR-1.5 band (500–750 GHz) mounted to its housing (a split-block waveguide for interfacing to back-end waveguide-based VNA frequency extenders) [7]. The probe chip protrudes about 500 μm from the housing to permit contact with DUT's on a wafer. As the

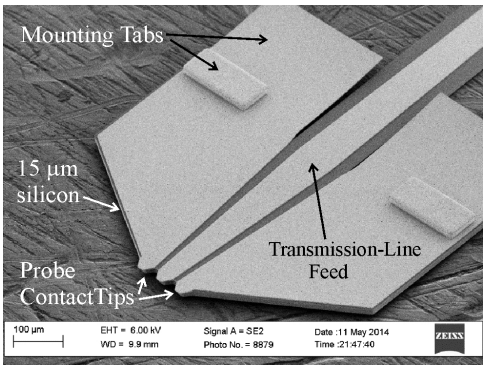
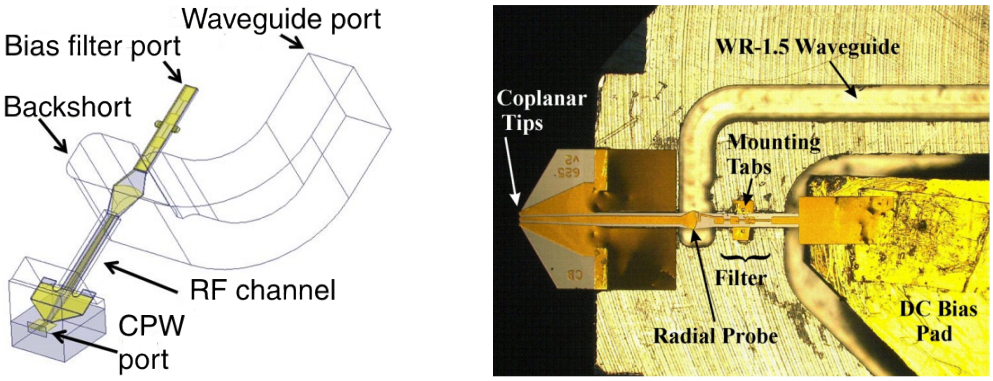


Figure 1.5: Scanning electron micrograph (SEM) of a micromachined on-wafer probe for the WR-1.0 (750-1100 GHz) band on 15 μm thick high-resistivity silicon [6].



(a) Diagram. (b) Photograph.

Figure 1.6: A WR-1.5 micromachined probe mounted to its housing [7].

micromachined probe is compatible with other standard microfabrication processes, it can serve as a foundation for fully-integrated terahertz instruments, including power detectors and frequency multiplier sources based on Schottky diodes.

Design and fabrication of the probe described above is based on micromachining of silicon-on-insulator (SOI) substrates. Because of its well-understood RF properties, low loss, mature processing technology, and mechanical robustness [28], high-resistivity (ρ >10 kΩ-cm), silicon has proven to be an excellent choice for realizing robust terahertz probes and also represents a natural choice as the host support substrate for realizing fully integrated instruments and sensors based on compound semiconductors (e.g., GaAs).

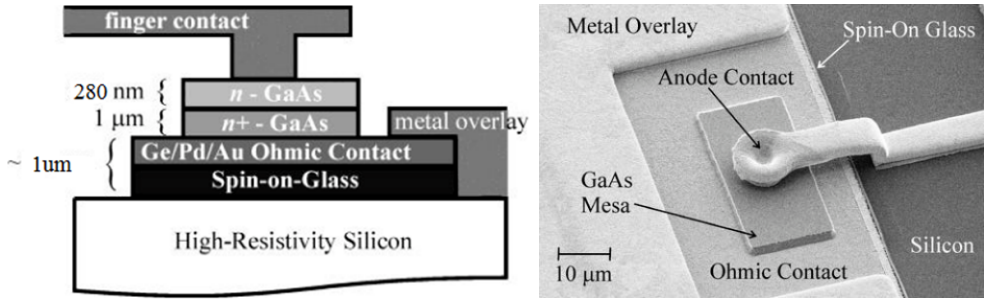
1.3 Heterogeneous Integration of GaAs Diodes onto Si Membranes

Schottky diodes are a critical device technology for applications in the submillimeter-wave spectrum, playing a central role as power detectors, heterodyne receivers, and frequency multipliers. Over the decades, this device has evolved from a single-element whisker-contacted geometry [30–32] to a planar chip with integrated finger contact [33] and finally heterogeneously integrated device bonded to host substrates supporting associated circuitry [34–38].

Heterogeneous integration of III-V semiconductor epitaxy onto silicon has proven an effective approach for realizing novel devices that combine outstanding RF characteristics with a mechanically-robust and low-loss substrate [8, 39, 40]. Integration processes have been shown to provide flexibility in engineering new device geometries and can be exploited to mitigate the electrical parasitics and thermal grounding bottlenecks that frequently limit the performance of terahertz components [13].

GaAs, the primary material used to realize submillimeter-wave Schottky diodes, has a number of severe limitations—its thermal conductivity and mechanical robustness are poor compared to silicon. Moreover, the material is fragile and ill-suited for the direct contact applications such as the on-wafer probes. Fortunately, heterogeneous integration of compound semiconductors onto support substrates, through epitaxial growth or epitaxial transfer, can address this issue. In contrast to epitaxial growth, epitaxial transfer (wafer bonding) is not limited by material issues such as lattice mismatch, coefficient of thermal expansion (CTE) or polarities [41, 42]. Direct bonding can provide high thermal conductivity compared to indirect wafer bonding where an intermediate polymer is placed in between, but this method requires excellent surface cleanness and smoothness of the wafers which limits its applications in many instruments [43].

Recent research at the University of Virginia initiated the development of a heterogeneous integration technology for fabricating GaAs Schottky diodes on silicon [8, 44] and silicon support membranes [9], which is also compatible with the process of micromachining of on-wafer probes. Figure 1.7b shows the diode epitaxy is bonded to a host, high-resistivity



(a) Cross section view.

(b) Scanning electron microscope image.

Figure 1.7: A quasi-vertical GaAs Schottky diode fabricated on a high-resistivity (ρ >10 kΩ-cm) silicon substrate [8].

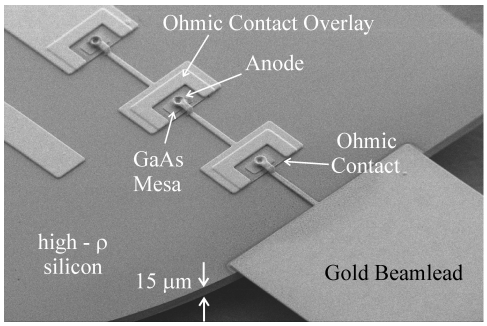


Figure 1.8: Integrated quasi-vertical GaAs Schottky diodes fabricated on a thin (15 μm) silicon membrane with beamleads [9].

silicon substrate that supports both the diode and its associated circuitry. Figure 1.8 shows a GaAs Schottky diode integrated on a high-resistivity silicon substrate and a three-element diode array fabricated on a thin (15 μm) silicon membrane with associated circuitry and beamleads. This initial work serves as the foundation of fully integrated submillimeter-wave and terahertz instruments detailed in this work.

The device shown in Figure 1.7b is a quasi-vertical diode in which ohmic contact lies beneath a GaAs mesa and the anode. As a result, the diode current flows through the bulk GaAs material instead of along the surface, as it does for the more common laterally-oriented planar diodes. Current crowding due to the skin and proximity effects associated with the lateral current flow near the diode surface [13, 45] are understood to increase the RF series resistance of planar diodes. Diode series resistance and parasitic capacitance, critical factors that limit the device's performance at terahertz frequencies, are generally found to be lower for vertically-oriented devices.

Quasi-vertical GaAs Schottky diodes integrated onto silicon can serve as the electronic calibration standard, based on their voltage-dependent impedance. After the RF on-wafer characterization of the diodes to obtain the S-parameters as a function of bias, the diodes can be subsequently used as the standard for electronic calibration. This allows full on-wafer calibration without need for moving or repositioning wafer probes onto the standards' contact pads.

1.4 Electronic Calibration at Submillimeter Wavelengths using Schottky Diodes as On-Wafer Standards

Measurement accuracy, precision and repeatability are of fundamental importance in characterizing the scattering parameters of devices and circuits using vector network analyzers (VNAs). The repeatability associated with interfaces and interconnects between network analyzers and devices-under-test (DUTs) fundamentally limits measurement precision and introduces nonsystematic error that cannot be eliminated through calibration. This issue is particularly important for measurements in the submillimeter-wave spectrum, as small offsets in the mating of interfaces and practical restrictions on mechanical tolerances and can conspire to produce significant electrical discontinuities that are difficult to predict or model.

With the development of wafer probes for the submillimeter-wave region [28,29], interface repeatability has become a more prevalent issue for on-wafer scattering parameter characterization. Misalignment in the positioning and placement of probes onto the contact pads of calibration standards and DUTs can have considerable influence on measurement uncertainty. Variations in the force applied between the probe tips and mating surfaces during such measurements result in uncertainties in contact resistance. Physical displacement of the probe from the measurement reference plane during calibration, due for instance to skating or overdrive, can produce more consequential errors. Such offsets introduce phase error that scales with frequency. Prior work has, in fact, identified phase error associated with positioning misalignment, skating, or overdrive as a major contributor to uncertainty for on-wafer scattering parameter measurements above 500 GHz [46, 47].

Electronically-tunable impedance standards that do not require movement and repositioning between calibration measurements have potential to mitigate the issues noted above, by eliminating uncertainty arising from misalignment or variations in applied contact force that are associated with skating of the probe, bowing of the wafer [10], micrometer backlash and other physical non-idealities of the measurement system. Since their introduction more than two decades ago, electronic calibration techniques have become an important technique for microwave scattering parameter characterization [48–53]. Because they eliminate the requirement for physical connection and re-connection of standards between calibration measurements, electronic standards provide convenience as well as the potential to mitigate measurement uncertainty associated with the electrical repeatability of interfaces.

1.5 On-Wafer Micromachined Probe with Submillimeter-wave Sensors

The micromachining and heterogeneous integration technologies, illustrated in Figure 1.6 and 1.7b, make on-wafer micromachined probes with integrated sensors a feasible approach for submillimeter-wave metrology. Some of the potential applications of this approach are integrated on-wafer probes with single diode temperature sensors, single diode power detectors and six port reflectometer [54] with an ensemble of diode detectors, among other types of instruments.

The report of integrating sensors onto micromachined on-wafer probes (Figure 1.9) was described in [10]. A symmetrical integrated resistive strain sensor pair was used to

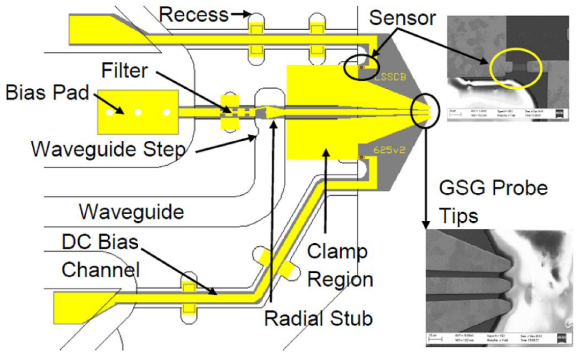
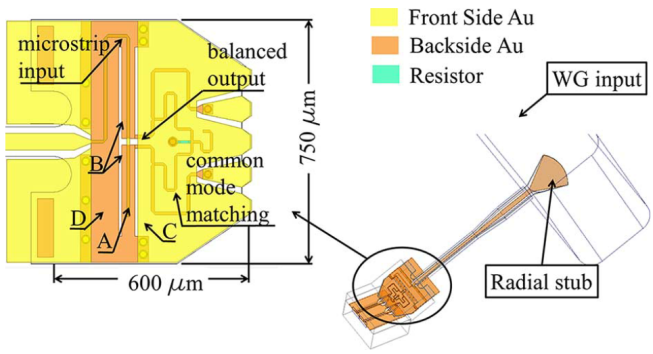
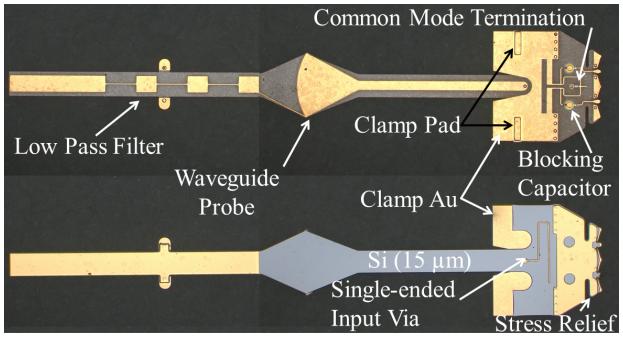


Figure 1.9: In-block view of the WR-1.5 integrated strain sensor probe chip [10].



(a)



(b)

Figure 1.10: Micromachined on-wafer probes with integrated baluns. (a) Full model of the WR-10 balun probe in HFSS [11]. (b) Top side and bottom side geometry of the WR-5.1 micromachined balun probe head. The probe design shown has a ground-signal-ground-signal-ground tip configuration [12].

monitor and control the contact force of a terahertz on-wafer probe to improve measurement repeatability of terahertz probing and enable contact force measurement without modification to the standard probe station. Film resistors [11] and metal-insulator-metal capacitors [12, 55] have also been successfully integrated onto micromachined on-wafer probes (Figure 1.10), enabling circuit design flexibility of more innovative designs to be incorporated onto micromachined on-wafer probes to realize differential probes.

By integrating power detector circuits or diode temperature sensors onto micromachined probes, it is possible to perform direct on-wafer power and S-parameters measurement, as well as temperature measurements. By integrating detectors to form a six port reflectometer (an alternative architecture of VNA), which is then integrated onto a micromachined on-wafer probe, a simple, compact, affordable alternative VNA can be realized.

1.6 Outline of Dissertation

The first chapter introduces the development of one of the technical foundations of the dissertation work, an epitaxy transfer process for heterogeneous integration of submillimeter-wave GaAs Schottky diodes on silicon using SU-8. Previous work and process refinement are discussed. Diodes fabricated using the revised process are characterized by both DC measurement and submillimeter-wave on-wafer characterization.

Chapter 3 discusses the new implementation of an integrated frequency quadrupler, based on previous work. An integrated frequency quadrupler operating at 160 GHz, producing 100 mW of output power, and achieving peak efficiency of 25.5% is described. The quadrupler design is based on prior art and consists of GaAs Schottky diodes with epitaxy transferred to a micromachined silicon carrier forming a heterogeneously-integrated chip. The newly-developed fabrication process described in Chapter 2, which eliminates high temperature annealing and utilizes SU-8 for adhesive bonding, was employed to realize the circuit.

The material presented in Chapter 4 presents the first demonstration of an electronic standard for on-wafer calibration at submillimeter-wave frequencies. The standard is based on the voltage-dependent impedance presented by a GaAs Schottky diode and allows full on-wafer calibration without need for moving or repositioning wafer probes onto contact pads. Both one port and two port on-wafer S-parameter measurement applications are discussed.

Chapter 5 reports the first implementation of heterogenous integration of GaAs Schottky diodes onto micromachined on-wafer probes to realize a temperature sensor. Design and fabrication of the probe, as well as fabrication and measurement of prototype diodes for the temperature sensor are described.

Chapter 6 presents a final example of heterogeneous integration of GaAs Schottky diodes onto micromachined on-wafer probes to realize a sampled line type six port reflectometer. The design of the probe, simulations of its calibration for one port S-parameter measurement, and the fabrication process and measurement plan are described.

The final chapter summaries the contributions and general conclusions as a result of this work. Potential areas of future investigation that stem from the work are also discussed.

Chapter 2

Epitaxy Transfer for Heterogeneous Integration of GaAs Schottky Diodes on Silicon

This chapter is based on the following publication, with some modifications and augmentations.

- **L. Xie** (co-first author), S. Nadri (co-first author), N. Alijabbari, M. E. Cyberey, M. F. Bauwens, A. W. Lichtenberger, N. Scott Barker, and R. M. Weikle, II, "An epitaxy transfer process for heterogeneous integration of submillimeter-wave GaAs Schottky diodes on silicon using SU-8," *IEEE Electron Device Letters*, vol. 38, no. 11, pp. 1-4, Nov. 2017, doi: 10.1109/LED.2017.2756920

This chapter describes an approach for fabricating quasi-vertical submillimeter-wave GaAs Schottky diodes heterogeneously-integrated to high-resistivity silicon substrates. The method described is based on that origianlly developed by Alijabbari [8], but is augmented and modified to improve yield and reliability. Specifically, the revised process eliminates previous processing steps that were prone to result in wafer fracture and delamination. Diodes fabricated with the new process are characterized using S-parameter measurements in the 325−500 GHz range with on-wafer RF probes and exhibit low parasitic capacitance

and series resistance, achieving device characteristics comparable to prior state-of-the-art submillimeter-wave diodes.

2.1 Introduction

Heterogeneous integration of III-V semiconductor epitaxy onto silicon has proven an effective approach for realizing novel devices that combine outstanding RF characteristics with a mechanically-robust and low-loss substrate [8, 39, 40]. Integration processes have been shown to provide flexibility in engineering new device geometries and can be exploited to mitigate the electrical parasitics and thermal grounding bottlenecks that frequently limit the performance of terahertz components [13].

As an example, in [8], an epitaxy transfer method was described that allows formation of quasi-vertical gallium arsenide (GaAs) Schottky diodes on silicon (Si). In contrast to diodes with planar (lateral) geometry in which anode and cathode contacts are formed on the same side of the GaAs, the quasi-vertical configuration incorporates a bottom cathode that serves as a low-resistance ohmic contact and thermal heat sink [56]. Although these devices have exhibited low parasitics at submillimeter-wave frequencies, the integration process used to fabricate quasi-vertical diodes suffers from low-to-modest yields arising from various thermal processes employed.

In general, both epitaxial growth and epitaxial transfer (direct and indirect) methods have been used for the heterogeneous integration of III-V semiconductors on host substrates such as Si, or silicon carbide (SiC) [57, 58]. For high frequency Schottky diodes, GaAs is the preferred material [38]. Epitaxial growth methods of GaAs on Si, as well as direct bonding techniques, are complex [59], impose stringent requirements on the surface cleanliness [60], and are not compatible with quasi-vertical geometries. Indirect bonding addresses these issues by adding an intermediate adhesive layer such as benzocyclobutene (BCB) [61], SU-8 [62], spin-on glasses (SOG) [8], or metals [63].

Both BCB and metal bonding require high processing temperatures of more than 200°C. This aggravates the issues that stem from the mismatch in the coefficient of thermal expansion between GaAs and Si. Previous epitaxial transfer methods based on SU-8 bonding [62]

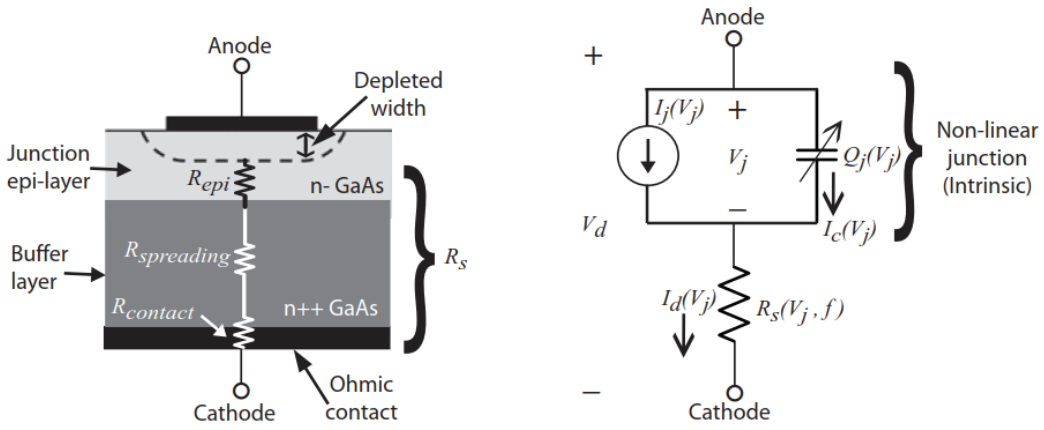
Table 2.1: Specific contact resistance of different ohmic contact metals and processes.

Ohmic contact metal	Process	Specific contact resistance ($\times 10^{-6}$ Ω cm^2)
Ge/Pd/Au [64]	Annealed (450°C 30s)	0.5
Ni/Ge/Au [64]	Annealed (450°C 30s)	0.38
Au/Ni/Au-Ge [65]	Annealed (410°C 115s)	1.05
Pd/In [66]	Annealed (500°C 5s)	0.2
Ti/Ni/Au [67]	Non-alloyed	3
Ni/Ge/Au/Ti/Au [68]	Non-alloyed	0.53
Ti/Pt/Au [69]	Non-alloyed	0.53
Ti/Pd/Au [70]	Non-alloyed	0.005

have been reported, however, these approaches only apply to transparent substrates. Under those conditions, bonding under vacuum and outgassing is not necessary, as curing can be achieved using ultraviolet (UV) light illumination.

Figure 2.1 shows the cross section view and equivalent circuit model of a GaAs Schottky diode [13]. The parasitic series resistance R_s of a Schottky diode can be treated as the sum of three components, R_{epi} (the resistance due to undepleted epi-layer), $R_{spreading}$ (the resistance due to current spreading in the buffer layer) and $R_{contact}$ (the resistance due to semiconductor-ohmic contact). R_{epi} and $R_{spreading}$ are intrinsic parameters of the epi wafers so the primary effort to reduce the parasitic series resistance is to minimize $R_{contact}$. A typical specific contact resistance (renormalized to the area) for Schottky diodes operating in the submillimeter wave region is in the order of 1×10^{-6} Ω cm^2 or smaller to yield a R_s of a few Ohms. Table 2.1 shows this parameter for different metals/processes and the state of art.

In this chapter, a more robust process is described for fabricating quasi-vertical GaAs Schottky diodes on Si. The process employs a low contact resistance ($R_{contact}$) non-alloyed ohmic contact that is characterized by the transmission line model (TLM) method. Furthermore, this work develops an SU-8 bonding process that utilizes low temperature curing, and does not require a transparent substrate. Schottky diodes fabricated using this method are



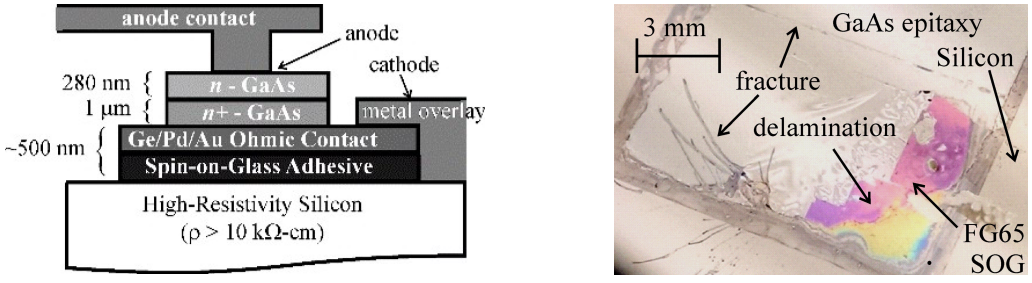
(a) Cross-sectional view. (b) Diode equivalent circuit.

Figure 2.1: Cross section view and equivalent circuit of a GaAs Schottky diode [13].

characterized and compared to previously reported diodes, exhibiting comparable performance with superior yield.

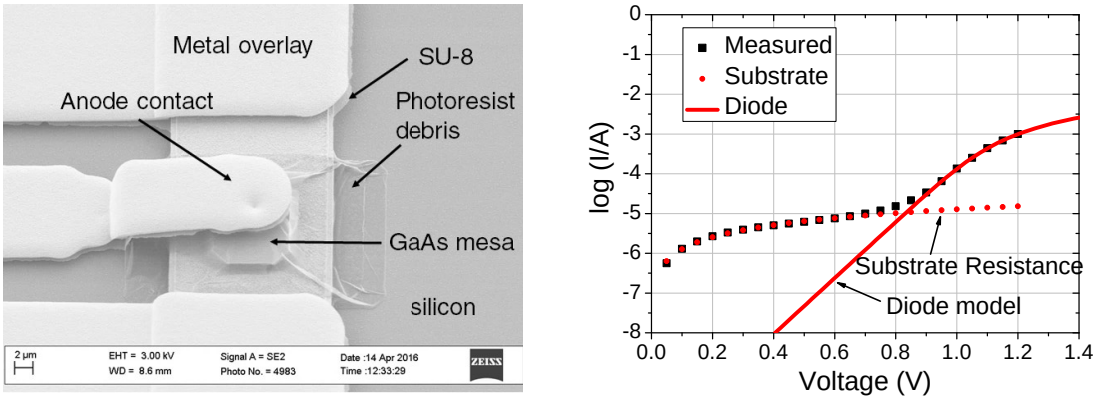
2.2 Quasi-vertical Schottky Diode

The geometry of the quasi-vertical Schottky diode is shown in Figure 2.2a and consists of a top-side anode contact, a mesa of GaAs epitaxy, and a bottom-side ohmic contact bonded to a high-resistivity ($\rho > 10$ $k\Omega$·cm) silicon substrate. The structure of the device allows the ohmic contact to be placed in close proximity to the anode and employs an airbridge anode contact to minimize parasitic capacitance. Frequency multipliers based on this diode geometry have produced high efficiency (30%) and power (80 mW) at an output frequency of 160 GHz [9].



(a) (b)

Figure 2.2: (a) Cartoon illustrating the quasi-vertical Schottky diode geometry. (b) Image illustrating fracturing and delamination of GaAs epitaxy bonded to silicon using Filmtronics FG-65 SOG.



(a) (b)

Figure 2.3: Quasi vertical diodes of under-annealed Ge/Pd/Au/Ti ohmic contact. (a) SEM of the diodes. (b) Measured current-voltage characteristic of a quasi-vertical diode with 3 µm diameter anode.

The original process to fabricate the device illustrated in Figure 2.2a consists of initially forming a patterned, annealed ohmic contact on highly-doped GaAs. This step is followed by a transfer of the epitaxy whereby the ohmic metal contact is bonded to a host silicon substrate using spin-on-glass (Filmtronics FG-65) as an adhesive. Subsequently, most of the GaAs is removed through wet chemical etching, leaving mesas upon which the diodes are formed using standard photolithographic processes.

Surface roughness and vertical relief of the patterned and annealed (335°C for 90s) ohmic contacts, as well as mismatches in the thermal expansion coefficients of Si (2.6 ppm/°C) and GaAs (5.73 ppm/°C) frequently resulted in fracturing or delamination of the thin (∼1 µm) GaAs epitaxy from the silicon substrate. Moreover, the large volume shrinkage associated with curing of spin-on-glasses made these films prone to cracking [71, 72]. Figure 2.2b illustrates these issues and the various failure mechanisms associated with the epitaxial transfer process that frequently limited the usable material and yield of these devices. Figure 2.3 shows the results of under annealing of the original recipe. The quasi vertical diode structure was well formed but it was found to have much higher series resistance than expected (80 Ω as opposed to 2 Ω, measured in [8]) due to under annealing of the ohmic contact metal stacks based on the DC IV characterization.

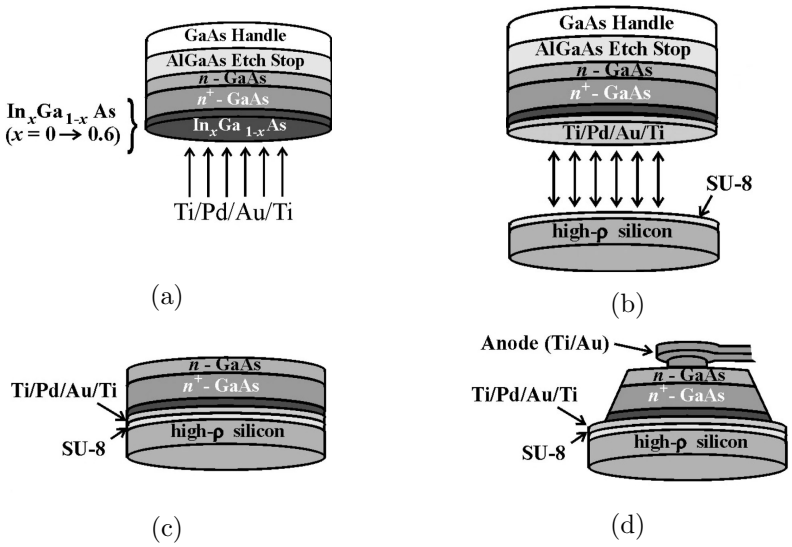


Figure 2.4: Outline of the quasi-vertical Schottky diode fabrication process. (a) Evaporation of Ti (20 nm)/Pd (40 nm)/Au (150 nm)/Ti (20 nm) ohmic contact over the $In_{0.6}Ga_{0.4}As$ cap layer. (b) Bonding of the III-V epitaxy to high-resistivity silicon. (c) Removal of the GaAs handle and AlGaAs etch stop layers. (d) Etching of the device mesa and formation of the Schottky anode contact.

2.2.1 Revised Fabrication Process

To address the issues above, the process has been refined in collaboration with S. Nadri. The detailed fabriaction recipe is provided in Appendix A and B.

The revised process for fabricating quasi-vertical diodes that addresses the issues noted above is summarized in Figure 2.4. See Appdendix A and B and below. The process utilizes epitaxy consisting of a 650 μm semi-insulating GaAs handle with 1 μm AlGaAs etch stop layer, n-GaAs (280 nm, 2×10^{17} cm^{-3}), and n+-GaAs (1 μm, 5×10^{18} cm^{-3}) device layers (Figure 2.4a). In addition, highly doped ($> 10^{19}$ cm^{-3}) InGaAs cap layers [73] are included in the epitaxy to allow the formation of a low resistance ohmic contact using a Ti/Pd/Au/Ti metal stack-up that does not require annealing. This epitaxy, which is commonly used for emitter contacts on HBTs [70], consists of a 50 nm thick graded $In_xGa_{1-x}As$ layer (x=0→0.6) followed by a 40 nm thick $In_{0.6}Ga_{0.4}As$ cap layer. Elimination of the annealing step results in a smooth metal surface. Unlike previous processes involving lithographically formed ohmic contact pads, the metal stack-up Ti/Pd/Au/Ti (20/40/150/20 nm) is evaporated over the entire InGaAs cap layer (Figure 2.4a) and left unpatterned. Consequently, the surface of the GaAs wafer bonded to silicon is planar, eliminating an important contributor for wafer

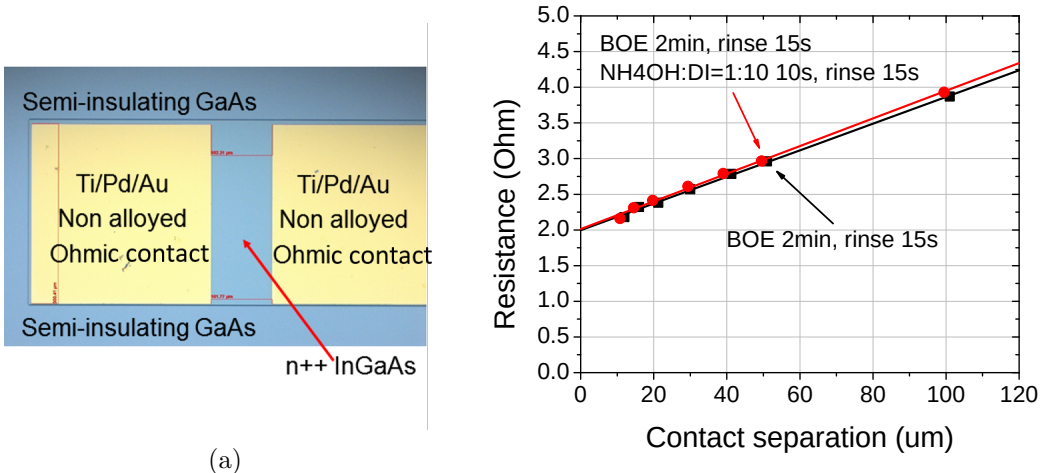
fracture.

The new epi wafers were first characterized using contact resistances measurement, with the well-known TLM method [74]. Si carrier with black wax for handling the InGaAs/GaAs sample was removed because of condensed vapor of black wax during the evaporation would fall onto the sample surface and thus caused contamination. Ti/Pd/Au (20/40/30 nm) stack was evaporated on top of 40 nm $In_xGa_{1-x}As$ ($> 1.0 \times 10^{19}$ cm^{-3}, x=0.6) to form the non-alloyed ohmic contact. The effect of different surface preparations before the metal evaporation was also investigated [75]. Both samples were prepared using oxygen plasma cleaning first, then one sample was prepared with buffered oxide etch (BOE) immersion and a deionized wafer (DI) rinse only, while the other was treated with an extra step of ammonium hydroxide immersion and DI rinse following the BOE and DI treatment. The measured non-alloyed contact resistance (Figure 2.5) on the InGaAs/GaAs epi wafers makes no significant difference and was found to be 8.0×10^{-7} Ω cm^2, comparable with Ge/Pd/Au/Ti annealed ohmic contact (5.0×10^{-7} Ω cm^2) [64]. This specific contact resistance is sufficiently low enough to yield low series resistance for submillimeter-wave applications. Table 2.2 lists the series resistance of some typical diode sizes produced from 5.0-8.0 $\times10^{-7}$ Ω cm^2 specific contact resistance.

In addition to modifying the ohmic contact formation step, the new process revises the wafer bonding step (Figure 2.4b), and replaces SOG with SU-8, a negative epoxy-based photoresist commonly used in MEMS packaging applications to produce high-aspect ratio features [76]. The GaAs epiltaxy layers and the SOI substrate are placed in a wafer press shown in Figure 2.6. The relatively low curing temperature of SU-8 ($100-140°C$) compared to SOG ($\sim 200°C$ or higher), coupled with its relatively lower percent volume shrinkage after cross-linking [76, 77] results in a more robust epitaxy transfer. SU-8 TF6000.5 can achieve 100-300 nm uniform coating, significantly thinner than SOG (> 500 nm). Since the adhesive bonding agent is thermal insulator, decreasing the thickness could improve the

Table 2.2: Typical series resistance of Schottky diodes with 5.0-8.0 $\times10^{-7}$ Ω cm^2 specific contact resistance.

Diameter (μm)	1.8	2.4	3.0	4.0
Series Resistance (Ω)	14.5	5.0	4.2	3.8



(a) (b)

Figure 2.5: Contact resistance measurement test of InGaAs/GaAs epi wafers. (a) Fabricated rectangular array of ohmic contacts. The TLM pattern width was 300 µm. (b) TLM pattern resistance as a function of contact spacing for the Ti/Pd/Au non-alloyed ohmic contact to GaAs with InGaAs cap layers.

thermal handling. SU-8 TF6000.5 has a built-in adhesion promoter and does not require additional coating layers such as OmniCoat or HMDS. The bonding process consists of spin coating the silicon substrate (9700 RPM, 35s), a 1 minute soft bake at 110°C, UV exposure (280 mJ/cm^2), a 40-minute outgas, and curing at 140°C for 40 min. The final adhesive layer of SU-8 is approximately 250 nm thick.

The membrane press for the bonding process consists of an upper and a lower chamber separated by a silicone membrane. In the press, the GaAs wafer is attached to a transparent glass force distribution plate via Apiezon W L-grease and the SOI substrate is placed on the copper heating block. After evacuating the entire press to -27 psi to outgas the SU-8, the GaAs wafer and the SOI substrate are brought into contact and heated to 140 °C to allow the SU-8 crosslink. The upper chamber's pressure is set to -17 psi during the bonding process by injecting nitrogen. Following the curing step, the substrates are allowed to cool by the RTE-110 water chiller through chilled water supply lines. The bonded wafer stack is attached to the transparent glass force distribution plate via L-grease, so it can be slid out and removed while the stack is still warm (about 60-70 °C).

Once bonded to the silicon substrate, the GaAs handle is removed in a nitric acid solution (70% HNO_3 : 30% H_2O_2 : DI = 1 : 6 : 1 at 50°C), followed by a slow citric acid etch

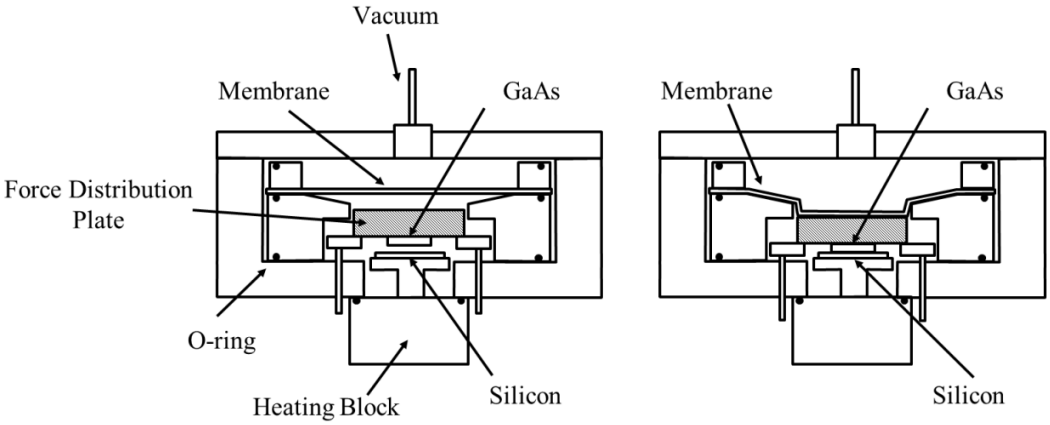


Figure 2.6: (a) Cross section view of the membrane press before bonding GaAs to SOI, (b) view of the press during bonding [14]. The press is designed by Edward Douglas.

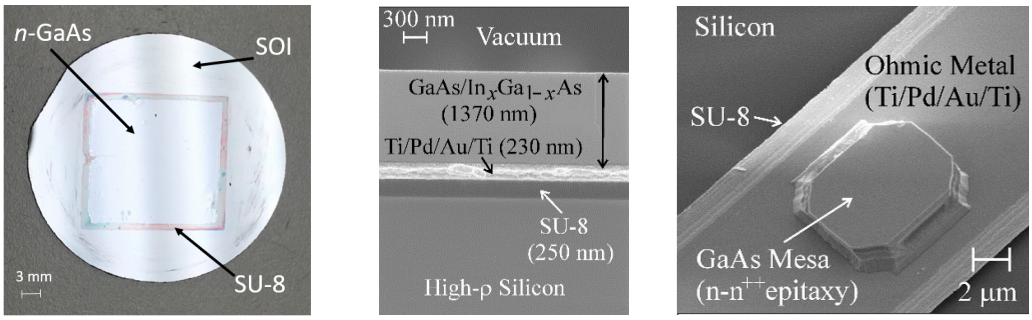


Figure 2.7: (a) Image of the bonded GaAs epitaxy onto a silicon-on-insulator (SOI) wafer. (b) Scanning electron micrograph (SEM) of a cross-section of the bonded GaAs epitaxy, ohmic metal, SU-8 resist, and silicon substrate. (c) SEM showing the GaAs mesa and ohmic metal contact bonded to silicon.

(50% mass $C_6H_8O_7$: 30% $H_2O_2 = 3 : 1$ at 50°C). The exposed AlGaAs etch stop layer is removed in hydrofluoric acid, revealing the GaAs device layer field (Figure 2.4c). Figure 2.7b shows an SEM image of a cross section of the bonded layers and illustrates the uniformity and lack of voids in the SU-8.

After removal of the handle GaAs, the diode mesa areas are defined photolithographically and formed by a sequence of selective etches that stop on the silicon surface. A wet etchant consisting of 98% H_2SO_4 : 30% H_2O_2 : DI $= 1 : 8 : 160$ is used to remove GaAs in the areas between the final device mesas. Following this, the exposed ohmic metal stack is removed using a combination of reactive ion etching (RIE), sputter etching, and wet chemical etching.

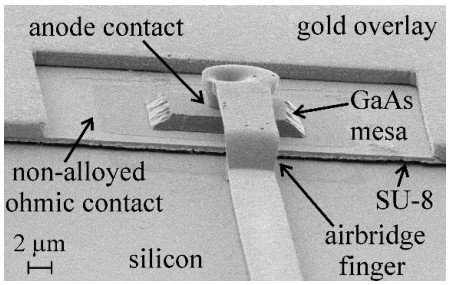


Figure 2.8: SEM of the quasi-vertical diode profile (diameter =3 μm) showing the device mesa, underlying ohmic contact, and anode contact airbridge. A CPW feed to the diode permits on-wafer S-parameter characterization of the device.

The thin Ti layers are removed in a Semigroup 1000-TP RIE tool using etchant gas species CHF_3/SF_6 to achieve anisotropic Ti etch. The process has 20 sccm of SF_6 flow, 5 sccm of CHF_3 flow and 0.7 sccm of N_2, at pressure of 35 mTorr and RF power of 150 W. The Pd is removed with a wet etch (Transene gold etchant TFA:DI=2: 1). Following this, the thick gold layer is removed with an Ar sputter etch (Ar 70 sccm, Pressure 29 mTorr, RF 120 W) in Semigroup 1000-TP RIE tool, followed by a brief potassium iodide wet etch. Once the ohmic metal layers have been removed, the exposed SU-8 adhesive layer is etched using a CF_4 RIE etch (CF_4 30 sccm, Pressure 25 mTorr, RF 100 W) in Semigroup 1000-TP RIE tool. This is followed by a GaAs wet etch 98% H_2SO_4 : 30% H_2O_2 : DI = 1 : 8 : 160 that defines the final device mesa atop an ohmic metal pedestal (Figure 2.7c). The remaining process steps utilize standard lithographic patterning to form the anode, airbridge finger contact, ohmic contact overlay metallization, and other circuit features on the silicon surface (Figure 2.4d). An SEM image of a completed quasi-vertical diode is shown in Figure 2.8.

2.2.2 DC Measurement

A Keithley 236 source measurement unit is used for DC measurement of the quasi-vertical diodes. Estimation of the diode reverse saturation current, ideality factor and series resistance can be found by performing a best-fit to the I-V curve in forward bias, as shown in Figure 2.9. The DC parameters for the nominal 3 μm diameter diodes are listed in Table 2.3. The silicon substrate contributes a leakage resistance of $\sim$ 230 kΩ, which is noticeable in the DC current-voltage characteristic, but is usually inconsequential compared to the typical diode impedance at submillimeter-wave frequencies. The series resistance and ideality

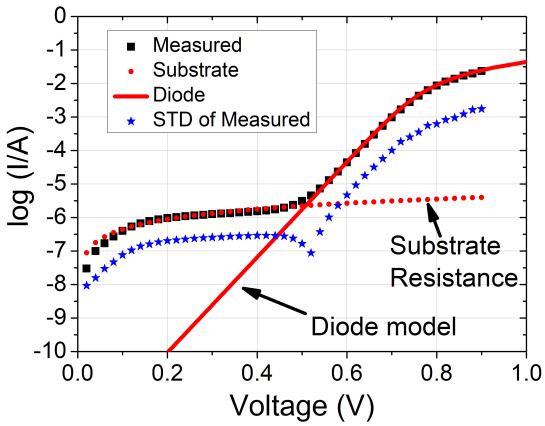


Figure 2.9: Measured average current-voltage characteristic of eight quasi-vertical diodes with 3 µm diameter anode with non-alloyed ohmic contact. The standard deviation (STD) of current-voltage measurements of eight diodes with the same anode size is also plotted.

Table 2.3: Extracted DC parameters and parameters normalized to anode area.

Anode diameter	Ideality factor /STD	Resistance /STD	Saturation current /STD	Normalized Conductance	Normalized Saturation Current
3 µm	1.20/0.02	4.30/0.24 Ω	0.10/0.03 pA	32.9 mS/µm^2	0.014 pA/µm^2

factor extracted from the DC measurements are comparable to those achieved with previous quasi-vertical diodes that utilized annealed contacts [8]. The breakdown voltage is found to be $\sim$ 9.5V from DC measurement under reverse bias.

2.2.3 Submillimeter-wave Measurement

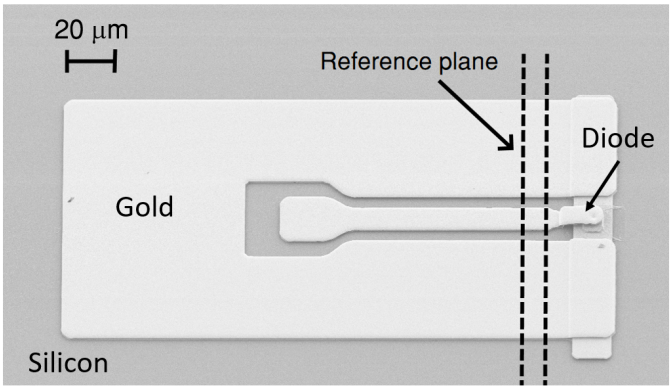


Figure 2.10: Reference plane of the on-wafer S-parameter measurement of the Schottky diodes.

High frequency characterization of the diodes is performed in the WR-2.2 (325−500

GHz) band using an Agilent PNAX vector network analyzer and Cascade Microtech PA200 probe station equipped with WM-570 frequency extenders from Virginia Diodes, Inc. and WR-2.2 on-wafer probes manufactured by Dominion MicroProbes, Inc [28, 44]. An on-wafer calibration is performed using standards fabricated on the same substrate as the diodes. The reference plane for the scattering parameter measurement is set 10 µm from the diode finger (Figure 2.10). Figure 2.11 compares the non-alloyed and annealed ohmic contact diodes [8] on-wafer measurement results.

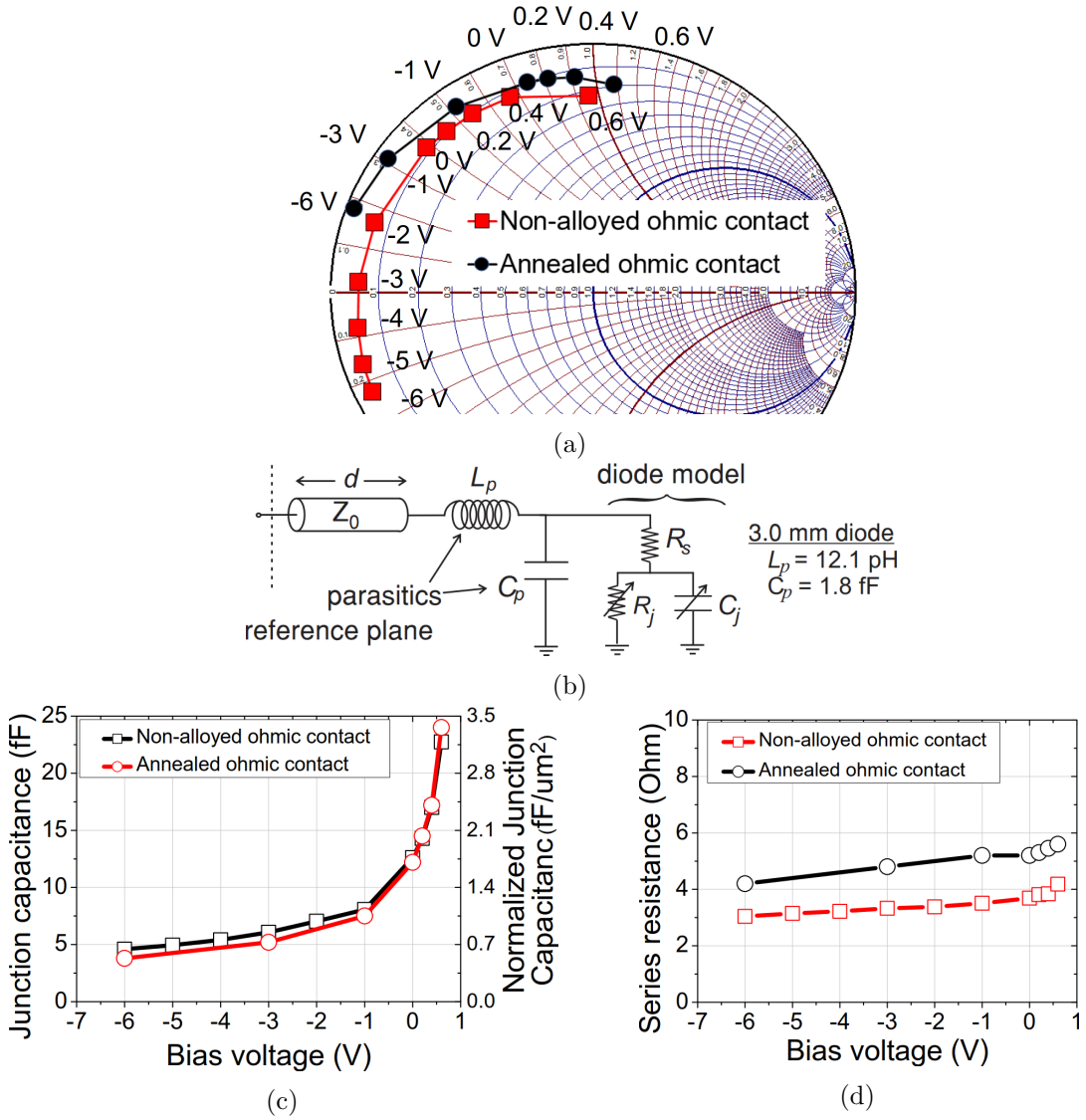


Figure 2.11: WR-2.2 on wafer measurement results. (a) S_{11} vs voltage at 425 GHz. (b) Equivalent circuit model used to represent the non-alloyed ohmic contact diode. (c) Extracted junction capacitance. (d) Extracted series resistance.

Figure 2.11a shows the measured reflection coefficient data taken at midband (425 GHz) as a function of bias voltage. The difference in sweep range vs. bias is due to a difference in the measurement reference plane for this work compared to [8]. Figure 2.11b shows the equivalent circuit model used to extract the junction capacitance and series resistance of the diode. The parasitic pad-to-pad capacitance and finger inductance value are extracted from HFSS model and are found to be comparable to those in [8]. The diode junction capacitance and series resistance, obtained from the S-parameter data, are shown in Figures 2.11c and 2.11d. The extracted junction capacitance for the annealed and unannealed diodes are, as anticipated the same. The normalized zero bias junction capacitance to anode area is 1.78 $fF/\mu m^2$. The series resistance extracted from these measurements indicate approximately 1 Ω lower value than that obtained with annealed ohmic contact diodes fabricated using the process described in [8]. The normalized zero bias series conductance to anode area is 38.4 $mS/\mu m^2$.

2.3 Summary

An improved and robust process for fabricating quasi-vertical GaAs Schottky diodes integrated to silicon has been developed. Thermal processes that lead to wafer fracture and delamination, including ohmic contact annealing and high-temperature wafer bonding, have been eliminated. Ohmic contact metal surface tension issues after thermal annealing have been eliminated. Lower temperature for the wafer bonding and lower percent volumn shrinkage after cross-linking of SU-8 compared to SOG used for wafer bonding agent makes the bonding interface smooth and free of cracks. Diodes fabricated using this new method exhibit excellent RF characteristics in the $325-500$ GHz frequency band.

Chapter 3

Frequency Quadruplers Based on Heterogeneous Integration of GaAs Schottky Diodes with Silicon

This chapter is based the following publication, with some modifications and augmentations.

- S. Nadri (co-first author), **L. Xie** (co-first author), M. Jaffari, N. Alijabbari, M. E. Cyberey, A. W. Lichtenberger, N. Scott Barker, and R. M. Weikle, II, "A 160 GHz frequency quadrupler based on heterogeneous integration of GaAs Schottky diodes onto silicon using SU-8 for epitaxy transfer," *IEEE MTT-S International Microwave Symposium*, Philadelphia, PA, USA, June 2018, pp.769-772, doi: 10.1109/MWSYM.2018.8439536

This chapter describes a new implementation of an integrated frequency quadrupler, based on prior art [8, 9] and documents the first application of the process described in Chapter 2 for implementing a submillimeter-wave integrated circuit. An integrated frequency quadrupler operating at 160 GHz, producing 100 mW of output power, and achieving peak efficiency of 25.5% is described. The quadrupler design is based on prior work, by Alijabbari, and consists of GaAs Schottky diodes with epitaxy transferred to a micromachined silicon carrier forming a heterogeneously-integrated chip. The newly-developed fabrication process that eliminates high temperature annealing and utilizes SU-8 for adhesive bonding was

employed to realize the circuit. This process improves device yield and reliability compared to previous implementations. This work was done in collaboration with S. Nadri.

3.1 Introduction

Sources operating at submillimeter wavelengths are commonly implemented using a chain of frequency multipliers that are based on GaAs Schottky diodes [78, 79]. Although cascading multipliers is a practical solution to generating submillimeter-wave power, a number of issues are associated with this technique; the input stages of a multiplier chain must typically accommodate significant drive power, as the overall efficiency of large chains is often no more than a few percent. Moreover, mismatch between adjacent multipliers can readily perturb earlier stages in a cascade by pulling them from their optimum operating point through loading effects, thus reducing efficiency and output power. Consequently, intermediate matching or isolation networks are frequently inserted between adjacent stages, contributing to loss and system complexity.

A balanced circuit architecture for realizing a "unilateral" multiplier that mitigates the loading effects presented to prior multiplier stages and that addresses a number of the issues outlined above was described in [80]. In 2014, that design concept was extended to develop a monolithic balanced quadrupler operating at 160 GHz and producing 70 mW output power with 29% peak efficiency [9]. In this chapter, a new epitaxy transfer and heterogeneous integration process that utilizes adhesive bonding with SU-8 is described and applied, for the first time, to implement a quadrupler based on the concept first reported in [9]. The new fabrication process addresses a number of issues that limited the device yield in previous monolithic frequency multiplier designs and has resulted in an integrated quadrupler with peak efficiency of 25.5% and maximum output power of 100 mW at 160 GHz.

3.2 Circuit Architecture and Design

The circuit architecture for the balanced quadrupler is depicted in Figure 3.1a. The input feeds a quadrature hybrid coupler that, in turn, drives two balanced frequency doublers. The outputs of these doubler stages are of equal amplitude and out-of-phase. Consequently, they

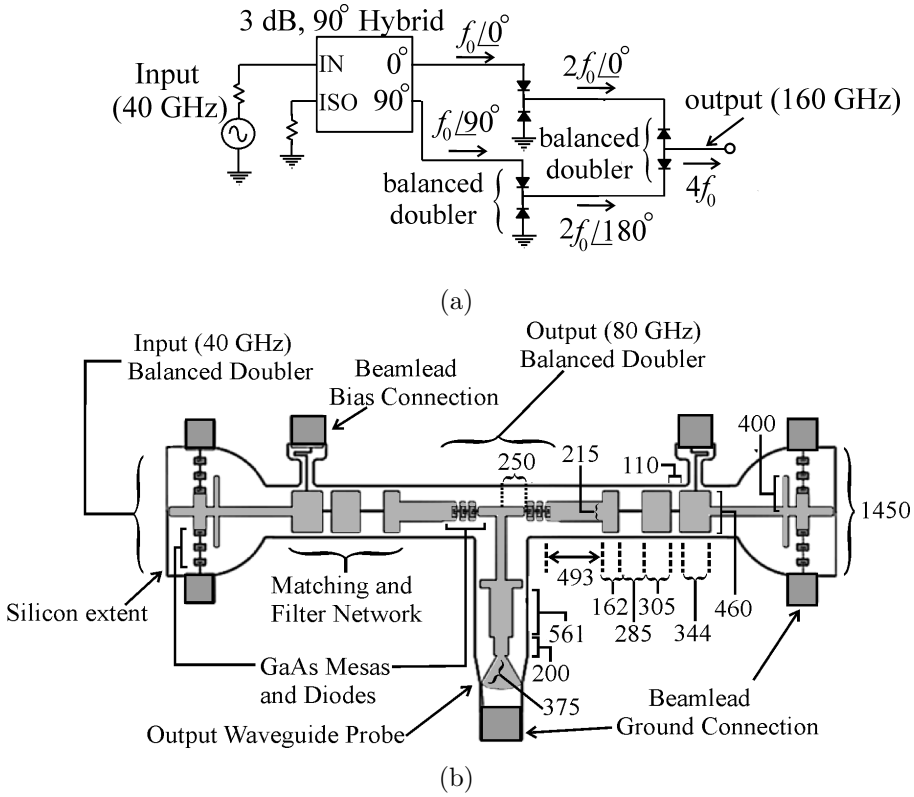


Figure 3.1: (a) Quadrupler circuit architecture and (b) layout of the integrated quadrupler chip. The quadrature hybrid is implemented off-chip (in waveguide) and all dimensions noted are in μm.

can directly drive an output balanced doubler stage, thus producing a frequency quadrupler. Provided the input stages of the multiplier are identical, no power is reflected at the input port. Mismatches associated with the input doublers result in power scattered to the isolation port of the hybrid, which acts as a power dump. The input of the quadrupler is matched over the operating bandwidth of the hybrid coupler, resulting in a unilateral multiplier.

Compared to the original circuit design reported in [9], the suspended substrate stripline (SSTL) to waveguide transisiton at the output of the quadrupler is modified to reduce the mismatch. The comparison of the modified design and original design is shown in Figure 3.2.

Varactor diodes used for the quadrupler design consisted of n-type GaAs epitaxy with modulation layer 280 nm thick and doping concentration of 2×10^{17} cm^{-3} and buffer layer 1 μm thick with doping concentration of 5×10^{18} cm^{-3}. Harmonic balance analysis performed on 9.6 μm and 8 μm diameter varactors fabricated from this new epitaxy, determined the

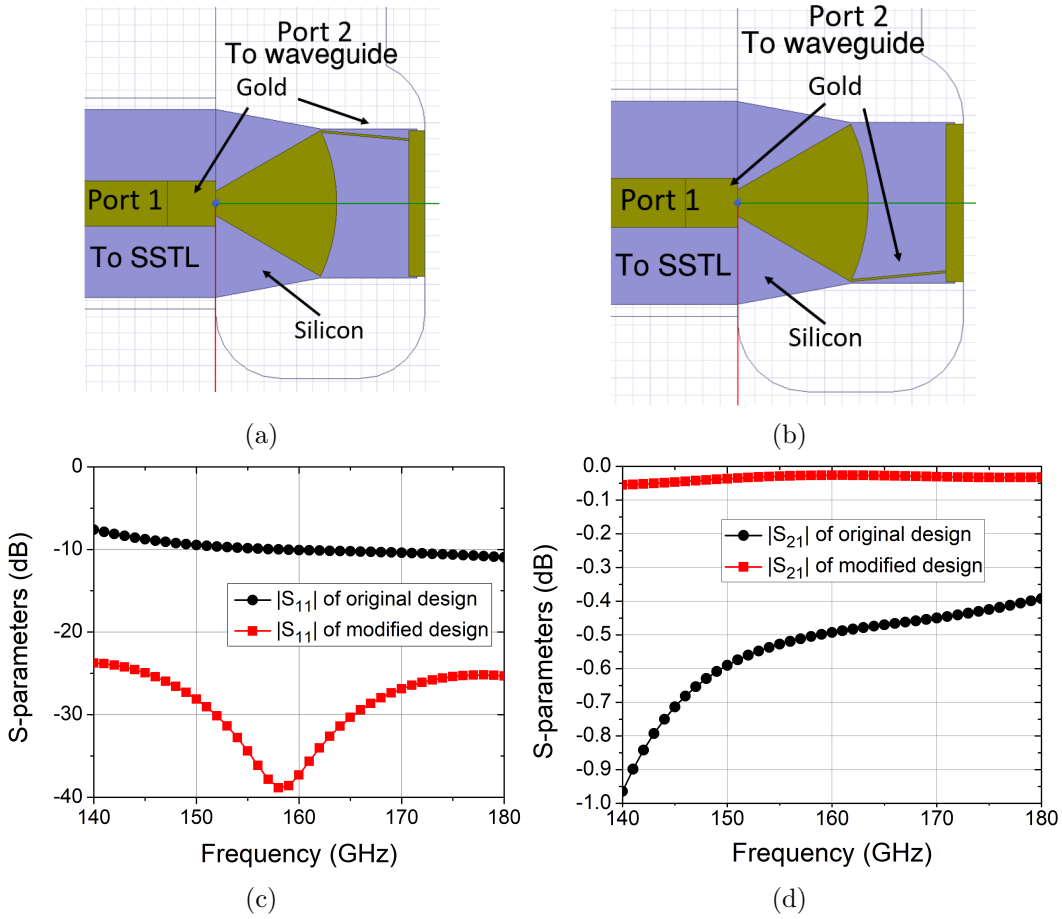


Figure 3.2: (a) Original quadrupler circuit of SSTL-waveguide transistion. (b) Modified quadrupler circuit of SSTL-waveguide transition. (c) Comparison of simulation results of return loss of the original and modified SSTL-waveguide transition. (d) Comparison of simulation results of insertion loss of the original and modified SSTL-waveguide transition.

optimum impedances to be 10.0+j70.3 Ω for the input at 40 GHz and 6.2+j53.0 Ω for the second stage input at 80 GHz. Final design of the quadrupler was accomplished by partitioning the circuit geometry into its three primary sections—an input doubler stage, an output doubler stage, and the intermediate matching network—and simulating each using Ansys HFSS. Scattering parameters obtained were imported into Keysight's ADS to perform harmonic balance analysis on the full quadrupler and to verify its operation.

A layout of the complete integrated quadrupler chip is shown in Figure 3.1b. The circuit incorporates three sets of balanced doublers comprising a total of 18 varactor diodes, and includes intermediate matching and filter networks, an output waveguide probe, and integrated beamleads for biasing. The chip is 7.5 mm from end-to-end and made of 15 μm

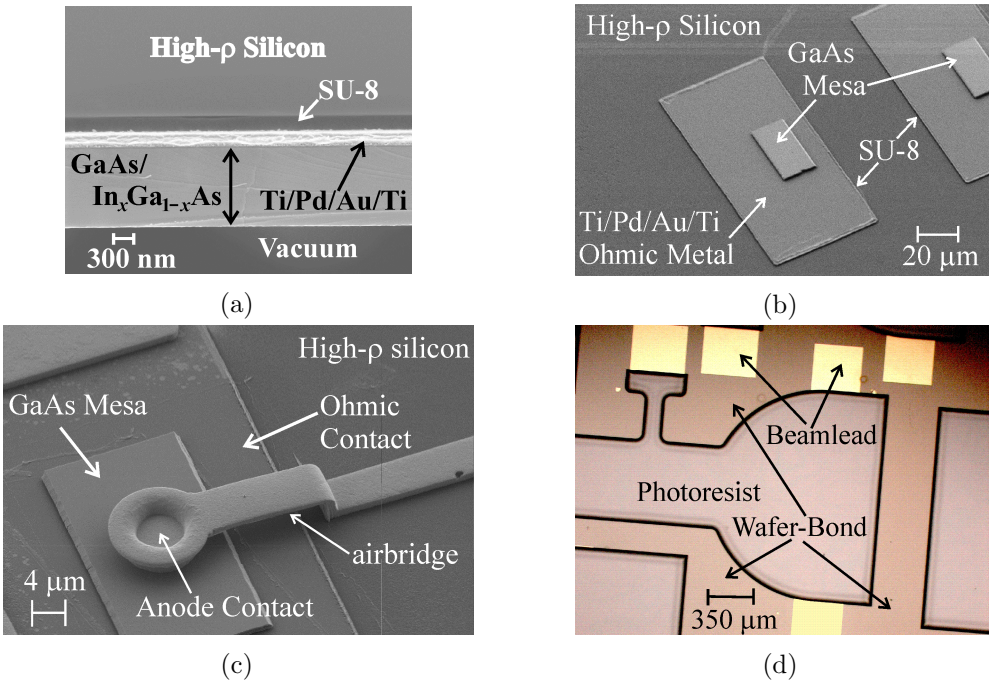


Figure 3.3: Images illustrating steps of the fabrication process. (a) SEM image of the bonded epitaxy. (b) Formation of the GaAs mesas and ohmic metal pedestals, (c) Anode and airbridge structures. (d) Backside lithography used to define the chip geometry.

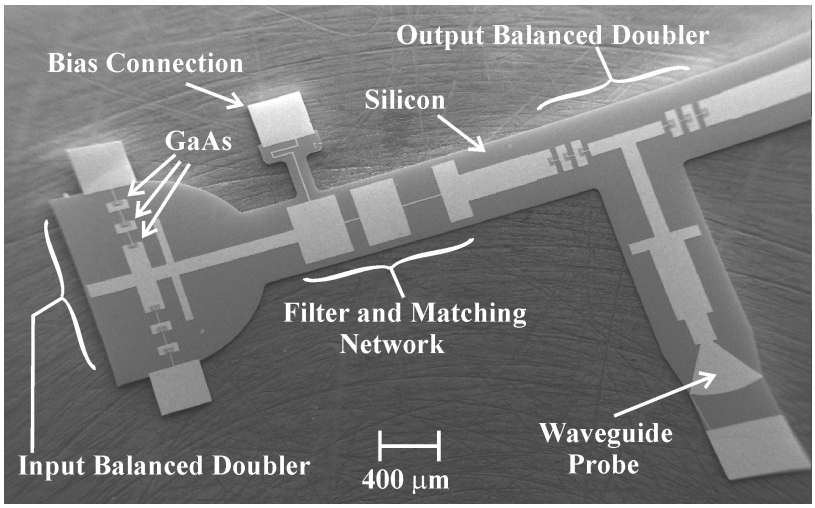
thick, high-resistivity ($\rho > 10$ $k\Omega$·cm) silicon onto which the GaAs varactors have been integrated.

3.3 Fabrication Process

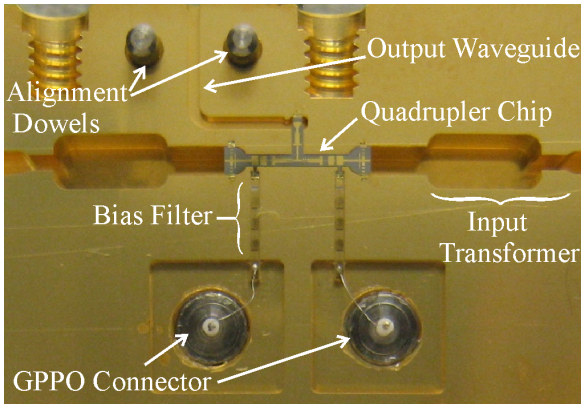
The integrated quadrupler shown in Figure 3.1b was fabricated using the new epitaxy transfer process described in Chapter 2 to integrated GaAs Schottky diodes onto a silicon-on-insulator (SOI) substrate.

The process of forming the diodes are shown in Figures 3.3a-3.3c. Figure 3.3a shows a SEM of the cross-section of the epitaxy after this step and illustrates the quality of the bond. The SU-8 layer between the ohmic metal and high-resistivity silicon layer is uniform (approximately 250 nm thick) with no observable voids.

Figure 3.3b shows the GaAs mesas sitting atop ohmic metal pedestals. Figure 3.3c shows an SEM image of the final diode device structure. For the quadrupler implemented in this work, the diameters of the diodes are nominally 9.6 µm for the input stage doublers



(a)



(b)

Figure 3.4: (a) SEM image of the completed quadrupler chip. (b) The quadrupler chip mounted to its waveguide housing. The quadrature hybrid is not shown.

and 8 μm for the output stage doubler. Once fabrication of the diodes is completed, the silicon carrier to which they are bonded is micromachined to form an integrated chip with geometry tailored to fit the waveguide housing to which it will be affixed. Initially, the surface of the wafer with diode circuitry is attached to a sacrificial carrier using wafer-bond adhesive. Following this, the thick "handle" silicon layer of the SOI is removed through a combination of lapping and plasma etching (SF_6=20 sccm, O_2=2 sccm, pressure=20 mTorr, ICP=500 W, temperature=20°C) in Oxford Instrument Plasmalab System 100 ICP-RIE etch tool. The buried oxide is then removed with a buffered oxide etch. In the final step, backside lithography defines the chip geometry, including integrated beamleads, and a silicon etch forms the final 15 μm thick chips (C_4F_8=40 sccm, SF_6=30 sccm, pressure=15

mTorr, ICP=500 W, RF=40 W, temperature= 0°C). Individual chips are then released by removing the sacrificial carrier with waferbond remover. Figure 3.3d shows an image of the backside lithography prior to release from the sacrificial carrier wafer. An SEM image of the completed quadrupler chips is shown in Figure 3.4a. Figure 3.4b shows a photograph of the chip mounted to its housing. Note that the 40 GHz input quadrature hybrid is implemented in waveguide, but is not shown in Figure 3.4b due to its relatively large size.

3.4 Measurements

Characterization of the quadrupler is done using an Agilent E8257D frequency synthesizer followed by a Spacek Labs SP408-35-26 amplifier with 35 dB gain and 36 to 43 GHz bandwidth. An Erickson PM5 power meter is used to measure the multiplier output power in the WR-5.1 band. The measurement setup is shown in Figure 3.5 and it is the same as the one used in [8] except that the PM1B power meter is replaced with the latest version, PM5. Figure 3.6 shows the input-output power relation for an input frequency of 40 GHz and diode (reverse) bias of 12 V. Peak efficiency of 25.5% occurs for an input of 280 mW. Beyond 280 mW, the multiplier begins saturating and the efficiency drops.

The output power over the full 36—43 GHz operating bandwidth of the Spacek power amplifier is shown in Figure 3.7, for an input power level of 285 mW and bias of 12 V. The power measured at the isolation port of the hybrid coupler, normalized to the available power from the input power amplifier, is also shown and provides a measure of the quality

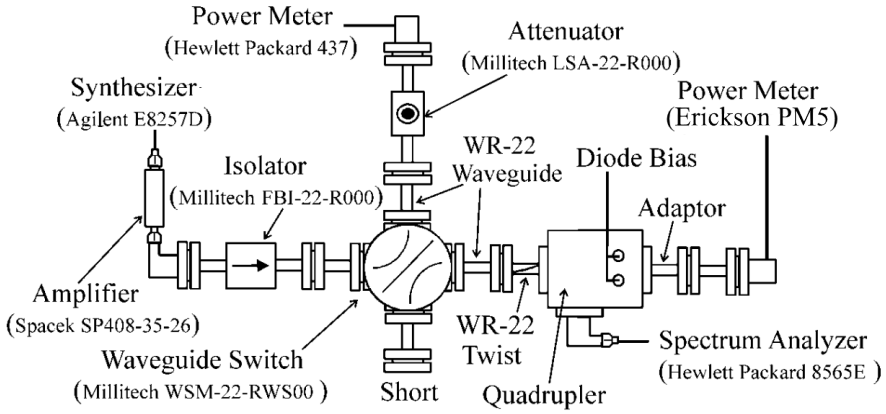


Figure 3.5: Diagram of the quadrupler measurement setup.

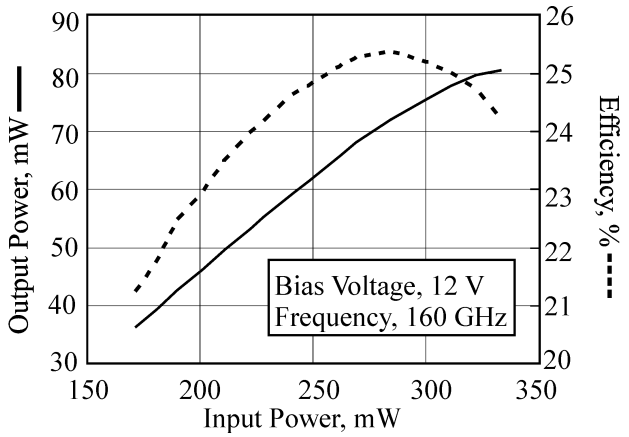


Figure 3.6: Quadrupler output power and efficiency vs. input power.

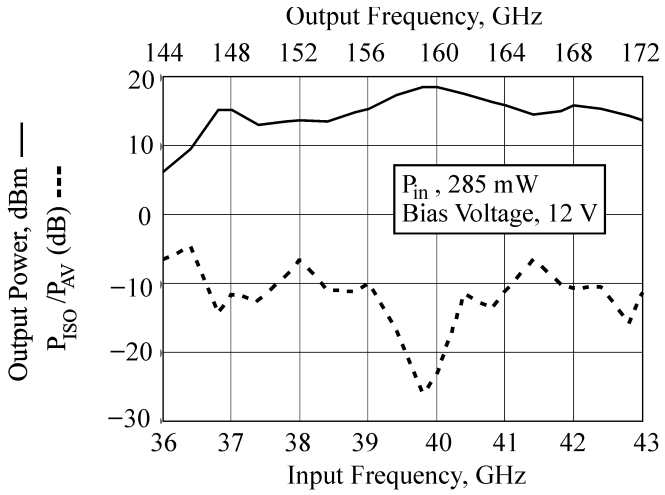


Figure 3.7: Output power and power measured at the isolation port, normalized to available power. vs. frequency.

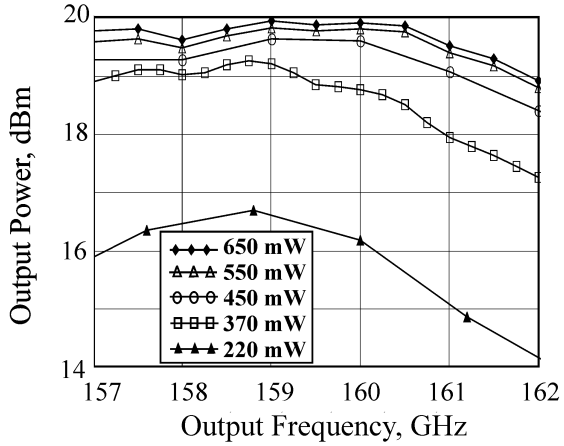


Figure 3.8: Power output vs frequency for different input power levels.

of the input match to the quadrupler. The peak power under these operating condition is 72 mW and the output power is greater than 20 mW over an output bandwidth of 146—176 GHz (16% fractional bandwidth).

Output power of the quadrupler as a function of input power near the design frequency (160 GHz) is shown in Figure 3.8. The saturation characteristic of the multiplier is evident and a maximum output power of 100 mW (20 dBm) was measured at 159 GHz. This output power corresponds to an input power of 650 mW and overall quadrupler efficiency of 15%.

3.5 Simulations and Design Improvements for Future Work

Thermal management considerations are very crucial in the design of frequency multipliers. Elevated diode junction temperature due to inadequate heat sinking is known to degrade performance, accelerate aging effects (for example, due to electromigration, ohmic contact deterioration, or thermally induced stress), and can ultimately lead to device failure [81]. It has been shown in [56] that the addition of an extra beam lead connected to the quadrupler block, for heat sinking, could reduce the maximum temperature by about 20°C. Figure 3.9 and 3.10 shows several implementations of extra beam lead to enhance the thermal handling of the frequency quadrupler.

Other than adding an extra beamlead, increasing the clearance between the edge of ohmic contact and the anchor of the finger air bridge could increase the fabrication yield.

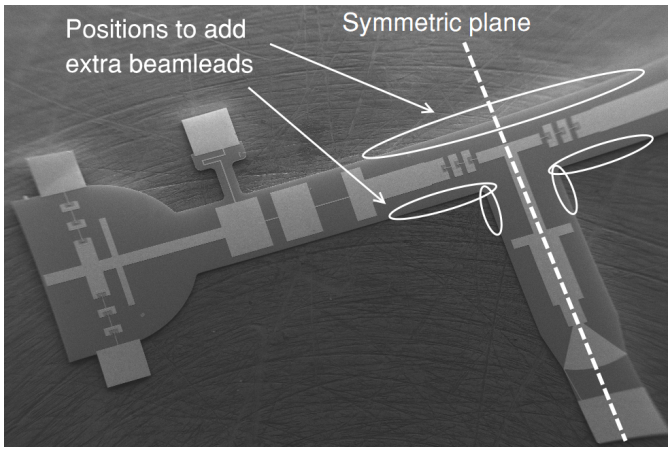
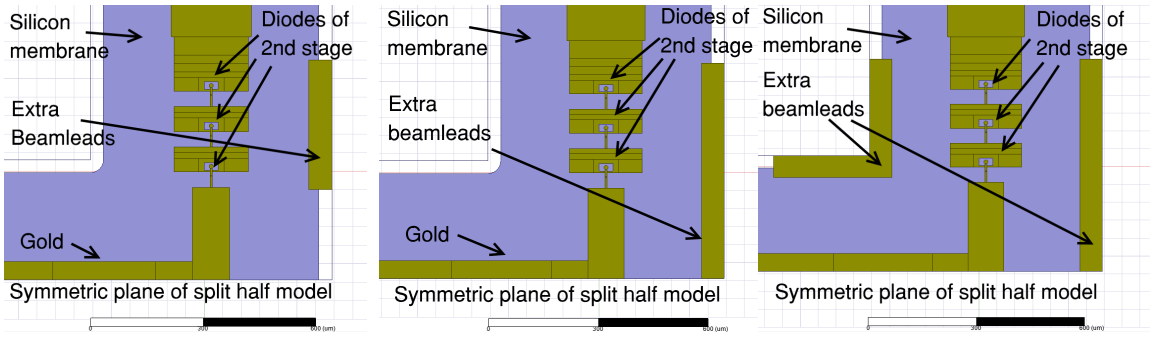


Figure 3.9: Possible positions to add extra beamlead to improve thermal handling of the quadrupler without interfering the electronic performance.



(a) (b) (c)

Figure 3.10: Three options of extra beamlead added to the second stage of the quadrupler for enhanced thermal handling. (a) Option 1: two separate pieces of extra beamlead added to the long side. (b) Option 2: one continuous piece of extra beamlead added to the long side. (c) Option 3: one continuous piece of extra beamlead added to the long side and two more pieces of extra beamlead added close to the output RF channel side.

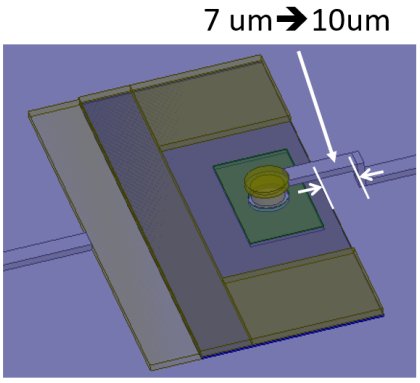


Figure 3.11: Increase the clearance between the edge of ohmic contact and anchor of the finger air bridge to increase the fabrication yield.

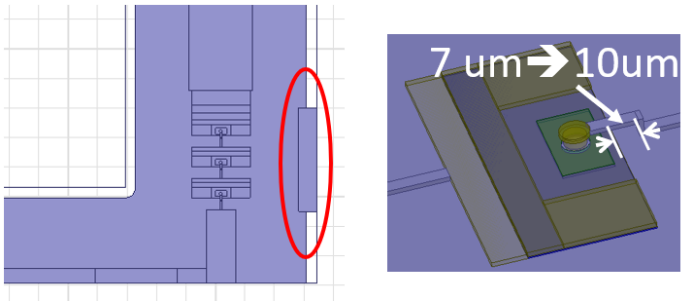


Figure 3.12: Add the beamlead to enhance thermal handling of the quadrupler and increase the clearance between the edge of ohmic contact and anchor of the finger air bridge to increase the fabrication yield.

The modification compared to the orginial design is illustrated in Figure 3.11.

Consider option 1 in Figure 3.10a for example. Adding more clearance between the

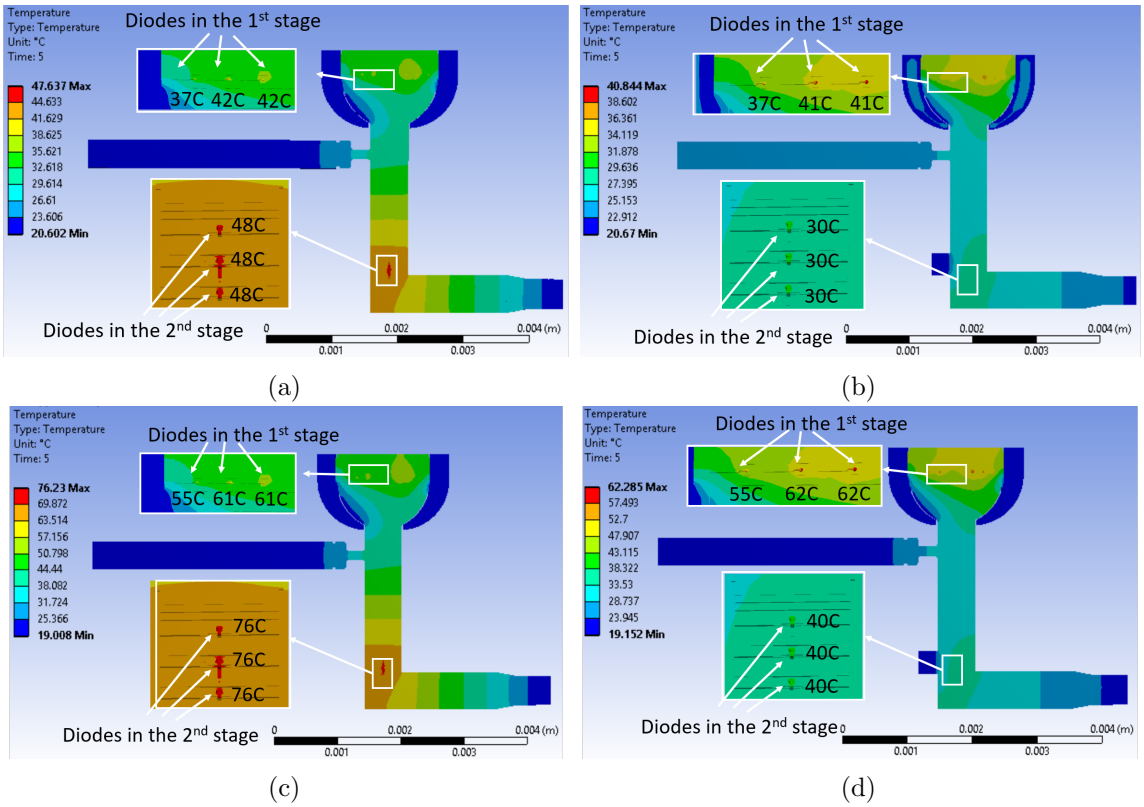


Figure 3.13: Comparison of steady state simulation of the quasi-half split model of quadrupler chip with or without additional beamleads at the second stage and increased air bridge anchor clearance to the ohmic contact pad. (a) 280 mW input power, original design. (b) 280 mW input power, modified design shown in Figure 3.12. (c) 600 mW input power, original design. (b) 600 mW input power, modified design shown in Figure 3.12. Appoximate temperature of anodes in both first stage and second stage of the quadrupler chip are labled.

edge of ohmic contact and the anchor of the finger air bridge, as shown in Figure 3.12. The steady state thermal simulation results using Ansys Thermal Analysis module of the quasi-half quadrupler chip are shown in Figure 3.13, for two different input power level excitation, 280 mW and 600 mW input, corresponding to maximum efficiency (Figure 3.6) and maximum output power (Figure 3.8), respectively. From the simulation, it can be shown that the modified design could lower the temperature of the anodes in the second stage by approximately 18 °C and 36 °C when the quadrupler is driven by 280 mW and 600 mW, respectively. The temperature of anodes of the first stage is about the same before and after adding extra beamleads to the second stage, as expected. The hottest spots were the anodes in the first stage and are the anodes in the second stage after adding extra beamleads.

The ADS and HFSS simulation results of the impedance matching of the intermediate

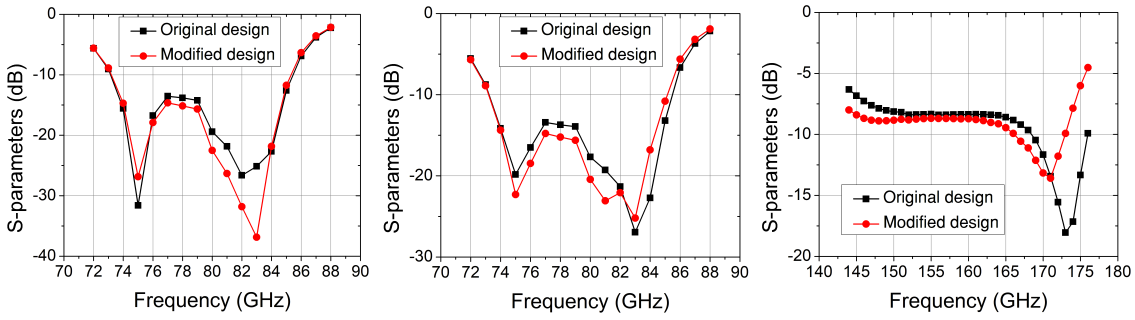


Figure 3.14: Comparison of simulation of impedance matching of the modified design to the original design. (a) Output matching of the first stage. (b) Input matching of the second stage. (c) Output matching of the second stage.

stage and the second stage are shown in Figure 3.14. From the simulation, the modified design has a minor effect on the electrical characteristics of the quadrupler circuit in the working bandwidth. Note that other circuit sections have not been modified yet. It is expected that the optimized modified design could both achieve equivalent impedance matching and enhance the thermal handling.

3.6 Summary

This work has presented a new implementation of an integrated frequency quadrupler, based on prior design [8, 9]. A modified fabrication process based on the new process described in Chapter 2, was adopted to realize the circuit. The new process eliminates high-temperature thermal processes and utilizes SU-8 as an adhesive for epitaxy transfer and heterogeneous integration. This approach has resulted in a more robust and reliable process for developing III-V based submillimeter-wave circuits integrated on silicon membrane carriers. A quadrupler fabricated with the new process has produced an output power of 100 mW at 160 GHz and peak efficiency of 25.5%.

Future work implementations will include adding more heat sink and increasing the fabrication tolerance to the critical points to further increase the yield and enhance the quadrupler's thermal handling. Both thermal and electrical simulation have been carried out to show that the electrical performance of the quadrupler is only slightly changed after the modifications.

Chapter 4

Electronic Calibration for Submillimeter On-Wafer Scattering Parameter Measurements

This chapter is based on the following publications with some modifications and augmentations.

- **L. Xie**, M. F. Bauwens, S. Nadri, M. E. Cyberey, A. Arsenovic, A. W. Lichtenberger, N. Scott Barker, and R. M. Weikle, II, "One port submillimeter-wave on wafer electronic network analyzer calibration with heterogeneously integrated GaAs Schottky diodes onto silicon", *93rd ARFTG Microwave Measurement Conference*, Boston, MA, USA, June 2019, accepted

This chapter describes an approach for on-wafer electronic calibration at submillimeter wavelengths. Quasi-vertical GaAs Schottky diodes integrated onto silicon serve as the electronic calibration standard, based on their voltage-dependent impedance and allows full on-wafer calibration without need for moving or repositioning wafer probes onto the standards' contact pads. The S-parameters of the diode standards are characterized over the WM-570 (325—500 GHz) band as a function of bias and subsequently used as the standard for electronic calibration. Comparisons of the error coefficients for both one port and two port calibration applications, derived using the diode standard are shown to be in good

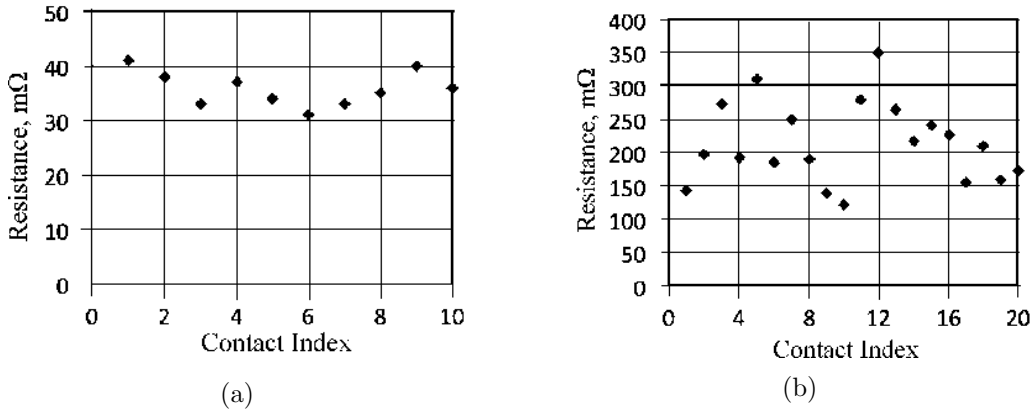
agreement with those obtained from a conventional set of standards. Because the error models and the calibration standards of one port and two port calibrations are different, they will be discussed separately as follows.

The electronic calibration in this work is implemented with the help of an open source, BSD-licensed package for RF/Microwave engineering, Scikit-RF [82]. The electronic calibration figures are plotted using the Matplotlib library [83].

4.1 Introduction

Measurement accuracy, precision and repeatability are of fundamental importance in characterizing the scattering parameters of devices and circuits using vector network analyzers (VNAs). While systematic error in such measurements can be corrected using a variety of well-established methods [84–87], the repeatability associated with interfaces and interconnects between network analyzers and devices-under-test (DUTs) fundamentally limits measurement precision and introduces nonsystematic error that cannot be eliminated through calibration. This issue is particularly important for measurements in the submillimeter-wave spectrum (above 300 GHz), as small offsets in the mating of interfaces and practical restrictions on mechanical tolerances and can conspire to produce significant electrical discontinuities that are difficult to predict or model. Recognition of this issue has led, as a result, to new designs for waveguide flanges [25] and the establishment of a recent IEEE standard for waveguide interfaces above 100 GHz [26, 27].

With the development of wafer probes for the submillimeter-wave region [28, 29], interface repeatability has become a more prevalent issue for on-wafer scattering parameter characterization. Misalignment in the positioning and placement of probes onto the contact pads of calibration standards and DUTs can have considerable influence on measurement uncertainty. Variations in the force applied between the probe tips and mating surfaces during such measurements, for example, result in uncertainties in contact resistance that can range on the order of 10 mΩ to a few 100 mΩ, depending on the conductor material and surface morphology (Figure 4.1). A 61 mΩ (standard deviation in Figure 4.1b) variation of contact resistance corresponds to an insertion loss of 0.005 dB from simulation. While such



(a) (b)

Figure 4.1: Repeated four-point resistance measurements of a nickel-tip micromachined probe contacting (a) gold, and (b) aluminum pads [2].

variations may be relatively minor compared to typical system impedances (50 Ω), they represent a limiting factor on the precision with which low insertion loss devices can be characterized. Physical displacement of the probe from the measurement reference plane during calibration, due for instance to skating or overdrive, can produce more consequential errors. Such offsets introduce phase error that scales with frequency; a 5 μm offset along a coplanar transmission line on silicon, for instance, corresponds to a phase shift of approximately 8° at 500 GHz and 16° at 1 THz. Prior work has, in fact, identified phase error associated with positioning misalignment, skating, or overdrive as a major contributor to uncertainty for on-wafer scattering parameter measurements above 500 GHz [46, 47].

Electronically-tunable impedance standards that do not require movement and repositioning between calibration measurements have potential to mitigate the issues noted above, by eliminating uncertainty arising from misalignment or variations in applied contact force that are associated with skating of the probe, bowing of the wafer [10], micrometer backlash and other physical non-idealities of the measurement system. Electronic calibration methods are well-established and have been common since being introduced by a number of national laboratories, including the National Institute of Standards and Technology (NIST) in the U.S. and the National Physical Laboratory (NPL) in the U.K. [48, 49, 88, 89]. Commercial electronic calibration units are available up to 67 GHz [50,90,91] and a variety of devices have been implemented to realize them, including PIN diodes [51], MEMS switches [52], CMOS transistors [53, 92]. Many of these devices exhibit limitations in operating frequency due to

device parasitics that can render them unsuitable for submillimeter-wave measurements.

In this chapter, one port and two port integrated Schottky diode impedance standards are implemented as electronically-tunable devices for one-port and two-port on-wafer calibration in the WM-570 (or WR-2.2, 325—500 GHz) band, respectively. The scattering parameters of the diode are initially characterized using conventional delayed short circuits [84] (for one-port calibration) or Thru-Line-Reflect (TRL) approach [87] (for two port calibration) to establish an impedance model for the diode standard. Subsequently, ensembles of measurements are performed on both the diode standard (obtained by varying the applied bias) and a set of delayed short circuits or transmission line TRL standards (obtained by moving the probe between different standards). The standard deviation of the error network coefficients derived from these two sets of calibration measurements are computed from these measurements and compared to assess the uncertainty and precision associated with the electronic and delayed coplanar shorts (one port application) or TRL on-wafer standards (two port application).

4.2 Electronic Calibration of One-Port Networks

This section reports on the first demonstration of an electronic standard for on-wafer calibration at submillimeter-wave frequencies. The standard is based on the voltage-dependent impedance presented by a GaAs Schottky diode and allows full on-wafer calibration without need for moving or repositioning wafer probes onto contact pads. Error coefficients derived using the electronic diode standard are compared to those found from a set of conventional coplanar delayed-short circuit standards and the two are found to be in good agreement.

4.2.1 Schottky Diode Calibration Standard

Quasi-Vertical Diode Geometry

A quasi-vertical Schottky diode architecture based on heterogeneous integration was described in Chapter 2 and 3 as a device geometry that could be engineered to mitigate parasitics that limit high-frequency performance. On-wafer measurement of these diodes at submillimeter-wavelengths have demonstrated that they are capable of achieving low series resistance

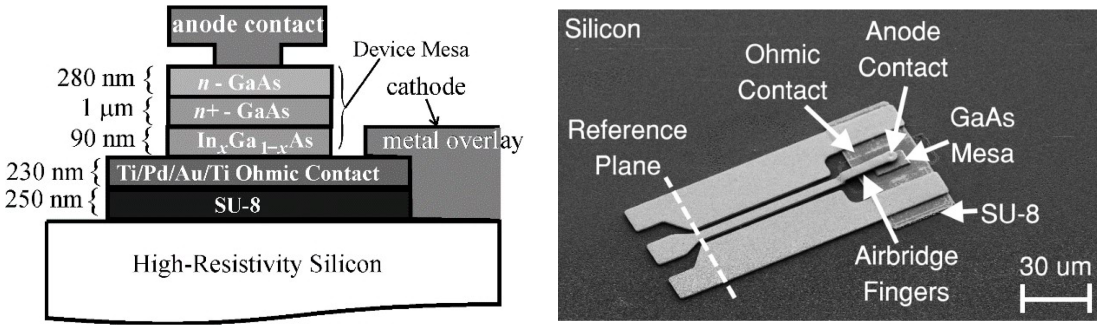


Figure 4.2: (a) Geometry of the quasi-vertical Schottky diode showing the epitaxial layers. (b) Scanning electron micrograph of a coplanar-fed quasi-vertical diode used as an electronic standard.

and shunt parasitic capacitance, making them a suitable technology to realize a tunable impedance standard for applications above 300 GHz [8].

The electronic standard used for the one port calibration is a quasi-vertical Schottky diode fabricated by heterogeneous integration of the device epitaxy onto a high-resistivity silicon substrate. A cartoon of the diode geometry is shown in Figure 4.2a. The device structure consists of an epitaxial mesa that lies upon an ohmic contact pedestal that serves as the cathode of the device and an airbridge finger that contacts the top of the mesa to form the anode. Details of the process used to fabricate this diode architecture have been described previously in Chapter 2.

A coplanar transmission line terminated with the quasi-vertical diode serves as the on-wafer standard investigated in this paper. Figure 4.2b shows an image of the diode standard which consists of landing pads for a wafer probe, a coplanar waveguide (CPW) feed on silicon, and a diode termination. A set of different impedances is presented to the wafer probe contacting the standard by varying the bias voltage of the diode, applied through the probe. DC and RF characterizations of CPW-fed quasi-vertical diodes using both current-voltage and scattering parameter measurements have shown this device structure provides adequately-low parasitic reactance and series resistance to serve as an electronically-tunable submillimeter-wave impedance standard for calibration. A 3 μm diameter device, for instance, exhibits approximately 4 Ω of series resistance, 7.5 pH of series inductance, and 5 fF of shunt capacitance [93].

Scattering Parameter Characterization

The scattering parameters of the diode standard shown in Figure 4.2b were measured as a function of bias voltage over the WM-570 (WR-2.2) frequency band (325—500 GHz) using a Cascade Microtech PA200 probe station equipped with a VNAX WM-570 frequency extender from Virginia Diodes, Inc., and a WR-2.2 band micromachined on-wafer probe [28]. Calibration for these measurements was performed using a set of five coplanar waveguide delayed short-circuits as standards (Figure 4.3a). The coplanar standards were fabricated on a 325 μm thick, high resistivity (>10 kΩ-cm) silicon wafer with 1 μm of electroplated gold metallization. As indicated in Figure 4.2b and Figure 4.3a, the measurement reference plane is placed at the transition between the probe landing pads and CPW feed line. The *ideals* of delay shorts are modeled in Ansys HFSS to establish the response of these standards. A least-squares fitting was applied to solve the over-determined error model in Figure 4.4 to obtain estimates for three error terms and correct the measured data. The error-corrected reflection coefficients of 3 μm and 4 μm diameter diode standards at mid-band (425 GHz) as a function of voltage bias are shown in Figure 4.3b.

4.2.2 Measurement

S-parameter characterization of the diodes as a function of bias permits transfer of the calibration standards from the set of delayed short-circuits (Figure 4.3a) to a new electronic standard consisting of a single, CPW-fed diode (Figure 4.2b). The electronic standard is implemented by using the measured voltage-dependent reflection coefficients of the CPW-fed diode to estimate the calibration coefficients for the same one-port error model used for the primary calibration based on delayed shorts (Figure 4.4). To assess the precision of the electronic calibration approach, the bias voltage of the diodes is swept from -8 V to +0.8 V five separate times with the probe remaining in contact with the CPW pads. A Keithley 236 source measurement unit is used to apply voltage to the diodes through the bias port of the micromachined on-wafer probe, which is not moved or repositioned during acquisition of the S-parameters for the five sets of data. Data are recorded for both 3 μm and 4 μm diameter diode terminations.

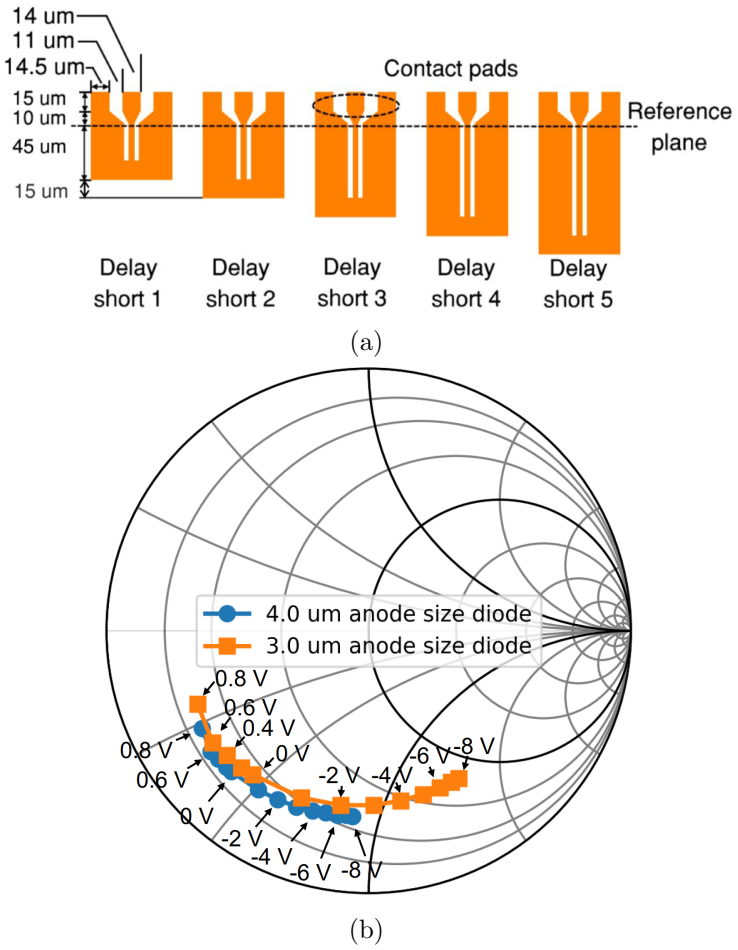


Figure 4.3: (a) Coplanar offset short circuits used as calibration standards. (b) Measured S_{11} of CPW-fed Schottky diodes with different diameters (4.0 µm and 3.0 µm) as a function of bias at 425 GHz. The voltage is swept from -8 V to 0.8 V for each diode.

The three frequency-dependent complex error coefficients for the one-port error model are derived from the measured reflection coefficient using the well-known relation,

$$\Gamma_m = E_{00} + \frac{E_{10}E_{01}\Gamma}{1 - E_{11}\Gamma} \tag{4.1}$$

where E_{00} is the directivity error term, E_{11} is the port match error term, $E_{10}E_{01}$ is the tracking error term, Γ_m is the measured reflection coefficient and Γ is the "true" reflection coefficient presented by the calibration standard or device-under-test. There are $5^5 = 3125$ sets of error coefficients obtained from permutations of the calibration measurements for each diode (five different bias points) from the repeated measurements (five times) described above and are used to generate mean values for the real and imaginary parts of the error

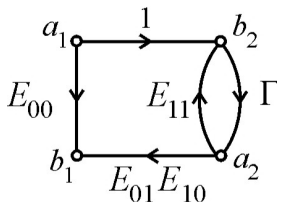


Figure 4.4: Signal flow graph of the one-port error model. Γ represents the "true" reflection coefficient of the device-under-test.

terms as well as their standard deviation, calculated by

$$STD = \sqrt{\frac{1}{N}\sum_{k=1}^{N}|E_k - \bar{E}|^2} \tag{4.2}$$

In (4.3), $N = 3125$, E_k is the error coefficient of interest, and $\bar{E}$ is its (complex) mean. Figures 4.5, 4.6, and 4.7 show the average error coefficients (plotted as magnitude and phase) obtained from the data, for each diode (3 and 4 μm diameter) as well as their standard deviation as computed using (4.3) and expressed in decibels ($20\ \log_{10}|STD|$). For comparison, the one-port error coefficients were also derived using the conventional delayed-short standards shown in Figure 4.3a. Each of the five delayed-short standards was measured, independently, five times by moving and repositioning the probe between measurements. From these data, another 3125 sets of error coefficients were obtained from permutations of the measurements and applying (4.1) and used to generate the mean magnitude and phase, in addition to the standard deviation as described above. The error coefficients derived from the delayed-short measurements are plotted along with those found from the electronic calibration standard in Figures 4.5, 4.6, and 4.7 and are seen to be in good agreement.

The standard deviation of the error coefficients (Figure 4.5c, 4.6c and 4.7c) represent non-systematic error and the uncertainty associated with different independent measurements of a DUT. This parameter is expected to be limited by electrical noise in addition to connection-reconnection repeatability of the measurement system. As the probe is not physically moved for calibration using the electronic diode standard, the uncertainty associated with connection-reconnection is anticipated to be very small and associated largely with the stability of the bias source. It is interesting to note that, although that the probe is moved and repositioned between measurements of the delayed short standards, the standard deviations

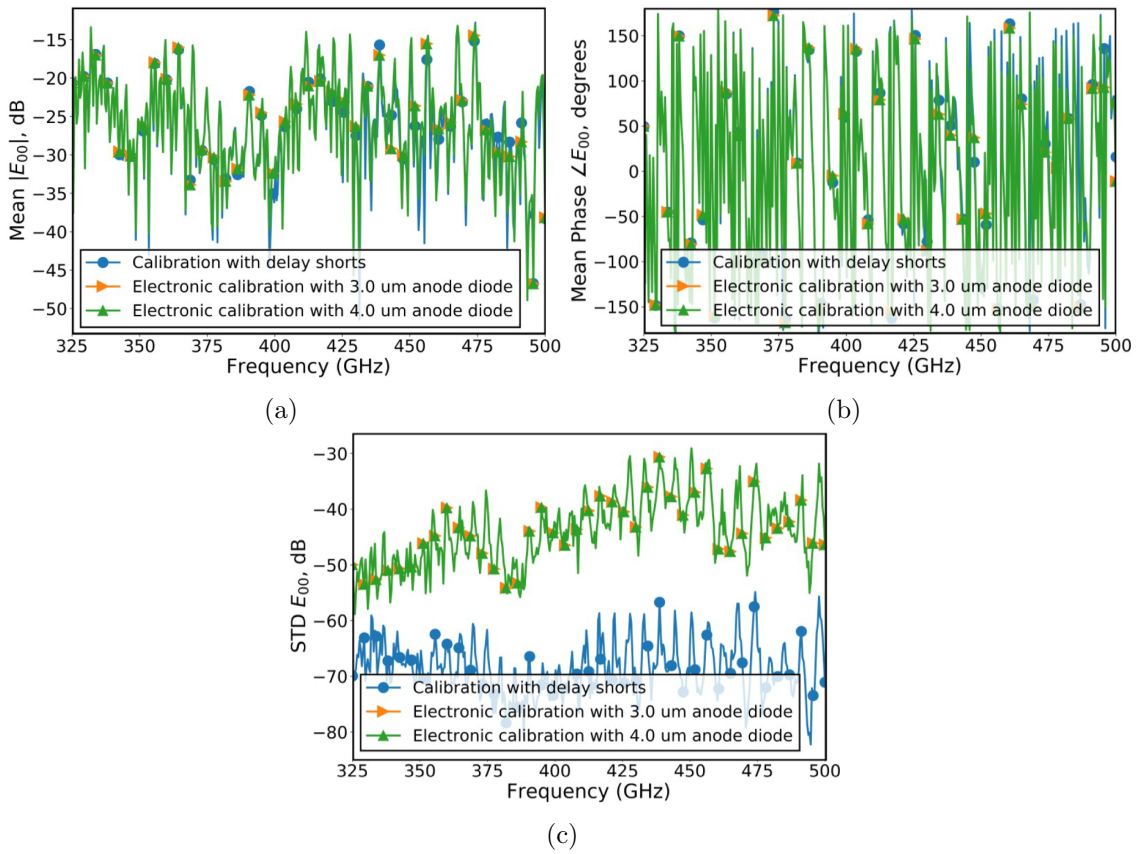


Figure 4.5: (a) Magnitude, (b) phase and (c) standard deviation of the directivity error coefficient (E_{00}) extracted from three sets of calibration standards.

of the error coefficients derived from this set of calibration standards is appreciably lower in comparison to the standard deviation computed from the electronically-tuned standards.

Computer-controlled precision micrometers capable of μm alignment were employed for the on-wafer measurements in this study. Moreover, repositioning of the probes between pads only required lateral translation with the micrometers, perpendicular to the coplanar calibration standards (as seen in Figure 4.3a). Previous studies have shown that positioning error associated with such lateral displacements are not as significant compared to positioning errors parallel to the transmission line standards, which result in phase uncertainty [94]. In addition, the delayed-short standards are designed to be well-spaced on the Smith Chart, while the diode standard sweep with bias spans a smaller region (approximately 90°) due to limited range of junction capacitance modulation versus bias voltage.

It is also interesting to note that the port match error coefficient E_{11} exhibits a distinct

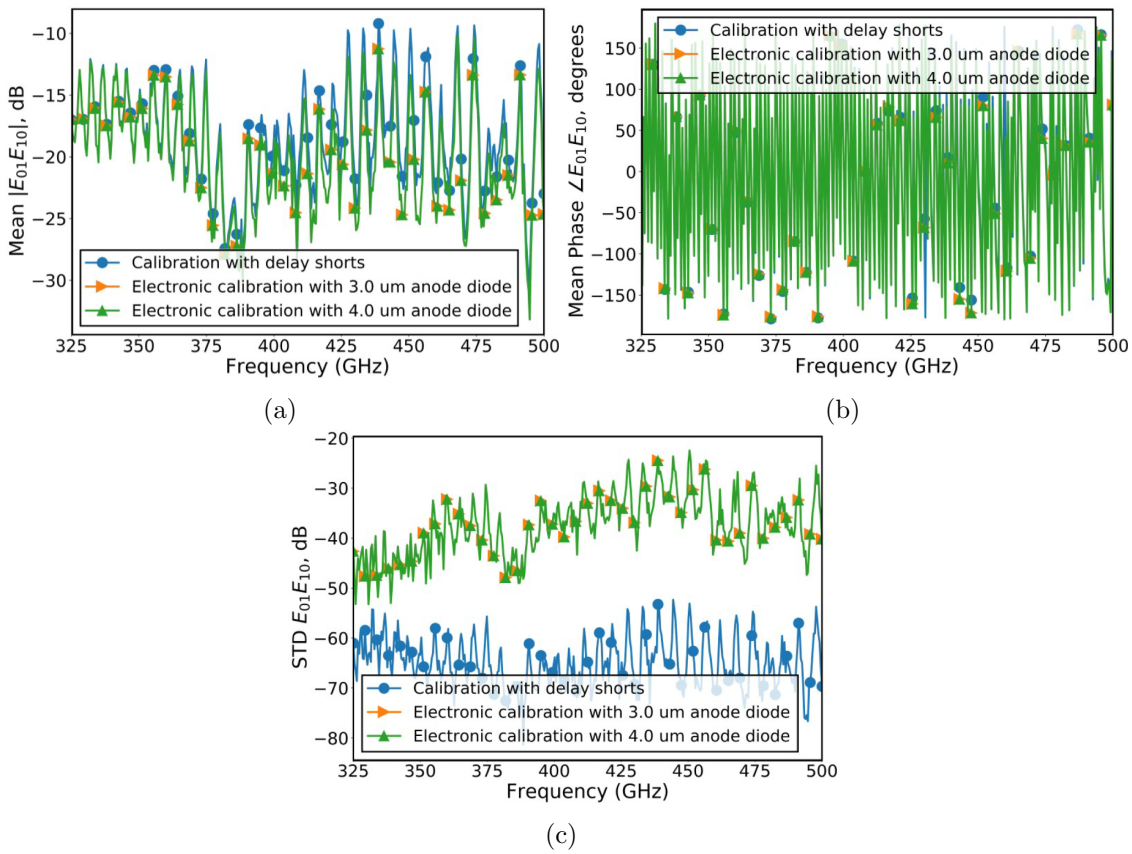


Figure 4.6: (a) Magnitude, (b) phase and (c) standard deviation of the tracking error coefficient ($E_{01}E_{10}$) extracted from three sets of calibration standards.

standing wave pattern (Figure 4.7a). This error term represents the mismatch between the DUT and the port of the measurement system to which it interfaces —in this case, the tips of the on-wafer probe. The scattering parameters measured from the WR-2.2 wafer probe utilizing a two-tier calibration technique [47] [95] are shown in Figure 4.8, showing that the error is primarily associated with the mismatch looking into the probe tip port (S_{22}).

To further illustrate the usefulness of electronic calibration at submillimeter wavelengths using a diode standard, a set of measurements were performed on a 5.6 μm diameter diode and corrected using each of the three sets of error terms derived from the delayed-short, 3 μm and 4 μm diameter diode standards. The mean magnitude and phase of S_{11}, as well as the standard deviation derived from these measurements are shown in Figure 4.9 and are seen to be in good agreement.

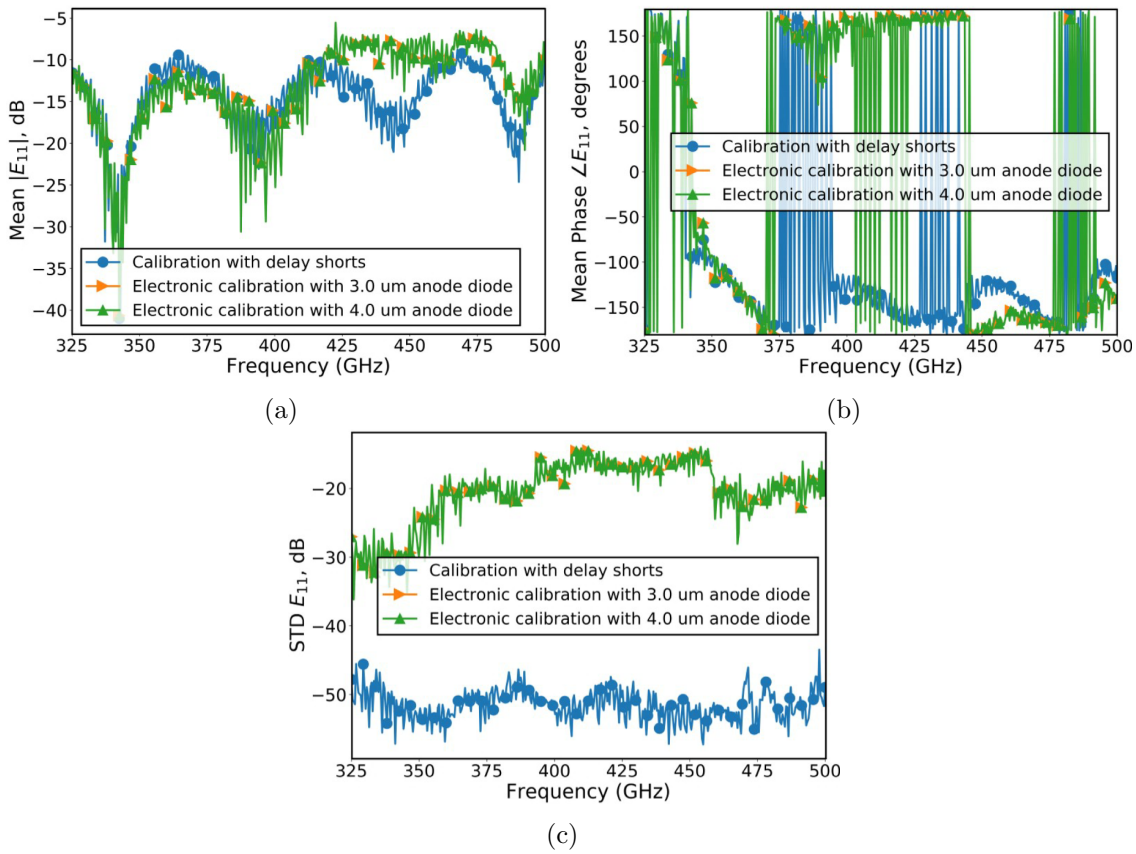


Figure 4.7: (a) Magnitude, (b) phase and (c) standard deviation of the port match error coefficient (E_{11}) extracted from three sets of calibration standards.

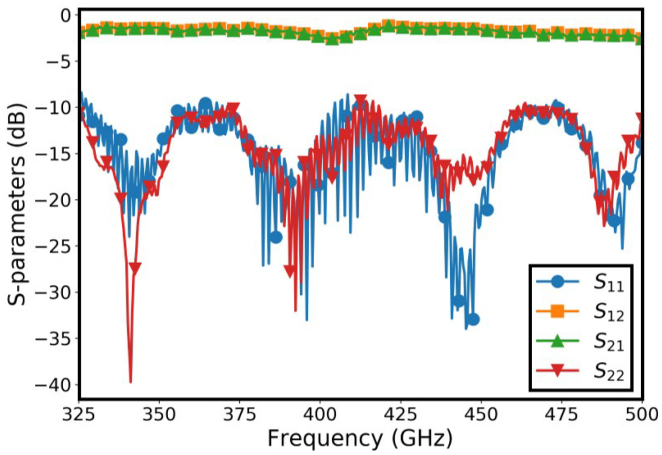


Figure 4.8: Measured scattering parameters (magnitude) of the micromachined WR-2.2 wafer probe.

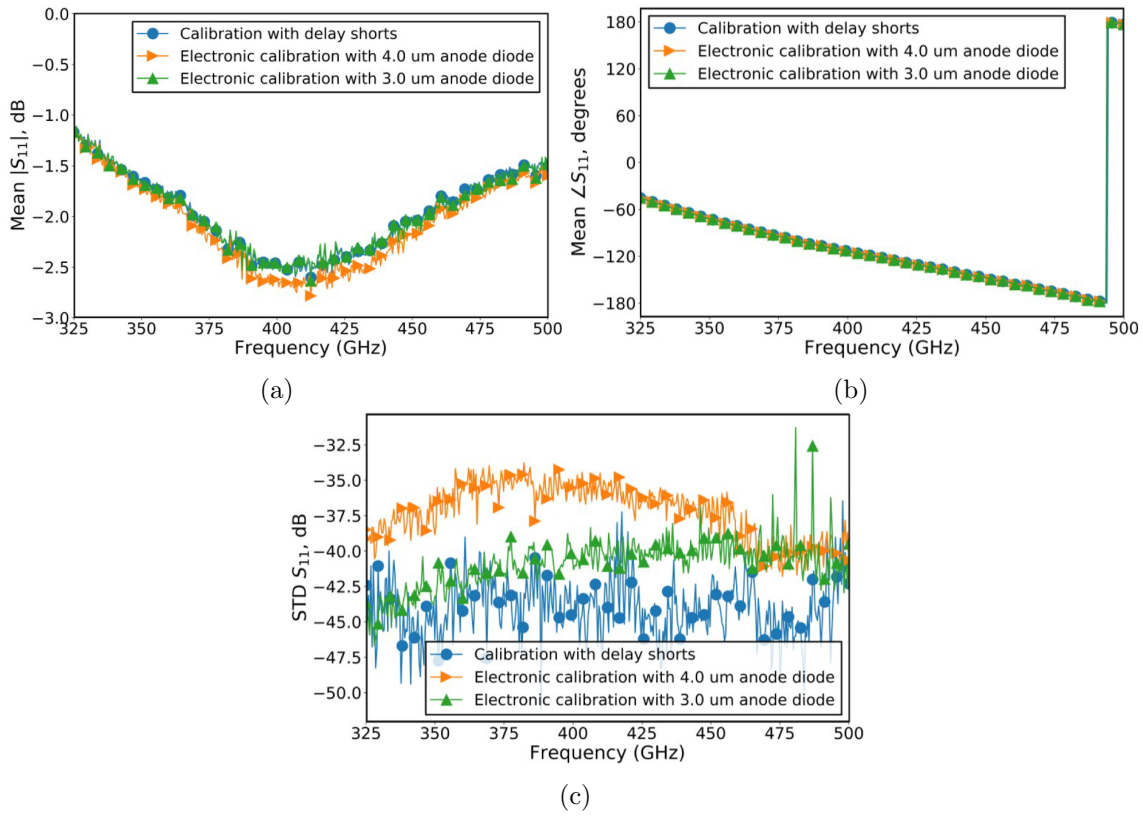
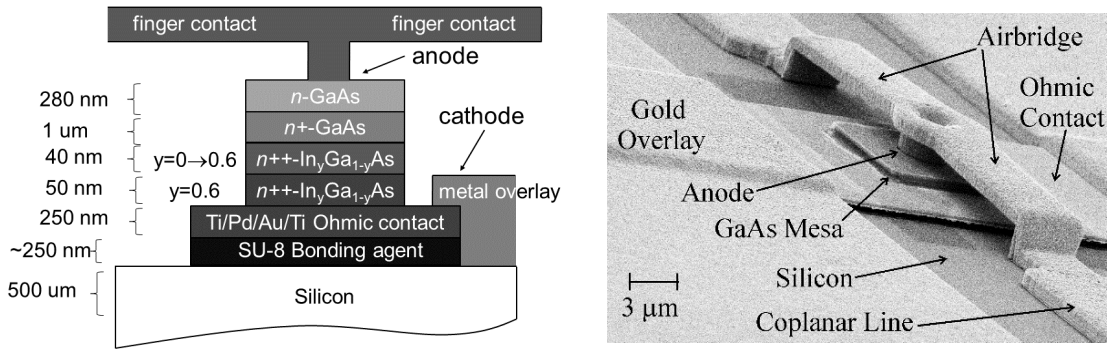


Figure 4.9: Comparison of measurements over the WR-2.2 band of a 5.6 µm diameter diode biased at -4 Volts, corrected using delayed shorts and electronic calibration standards. (a) Mean value of magnitude in dB (b) mean phase in degrees, and (c) standard deviation expressed in dB.

4.3 Electronic Calibration of Two-Port Networks

This section presents an extension of the electronic calibration approach using diodes for two port network analyzer calibrations in the WR-2.2 submillimeter-wave band (325—500 GHz). Quasi-vertical GaAs Schottky diodes integrated onto silicon serve as electronic calibration standard. As before, the diodes are pre-characterized under different bias voltages without lifting and relanding the probe tips to present different impedances for electronic tuning of the calibration standards. An eight term model is used for the two port electronic calibration. Error networks from two port multiline TRL calibration and electronic calibration using Schottky diodes are extracted and compared. Applications of the error networks from multiline TRL calibration and electronic calibration to different on-wafer devices under test (DUTs) are performed to illustrate the versatility of the technique. The electronic calibration



(a) (b)

Figure 4.10: (a) Cartoon showing the diode geometry and epitaxial layers. (b) Scanning electron micrograph of a dual-finger quasi-vertical GaAs Schottky diode shunting a coplanar transmission line.

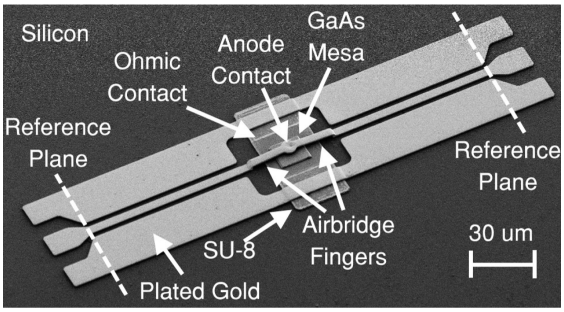


Figure 4.11: SEM images of two-port fed diode (anode diameter=4 µm) for two port electronic calibration of S-parameter measurement.

using quasi-vertical Schottky diodes agrees well with the multiline TRL calibration and shows significant improvement in repeatability due to the elimination of repositioning the probe tips on the landing pads.

4.3.1 Diode Elctronic Calibration Standard

Quasi-Vertical Diode Geometry

Details of the process used to fabricate this diode architecture (Figure 4.10a) have been described previously in Chapter 2. An image of a completed diode with dual airbridge finger anode contacts connecting two coplanar feed lines is shown in Figure 4.10b.

Scattering Parameter Characterization

Two-port scattering parameters of the quasi-vertical diode shunting a coplanar transmission line were measured as a function of voltage bias over the 325—500 GHz frequency range to establish the electronically-tunable calibration standard used in this work. A diode standard with anode diameter of 4 μm was fabricated on a 600 μm thick silicon substrate with 1.8 μm thick electroplated gold used to form the diode and circuit metallization.

A set of TRL standards consisting of a thru, open and short reflect standards for each port, and two delay lines (shown in Figure 4.12) were fabricated on the same substrate as the diode standards and used to perform a two-port calibration with WM-570 (or, WR-2.2) micromachined wafer probes [96]. The commercial software package WinCal XE (from Formfactor) was applied to implement the multiline TRL calibration and subsequently used to characterize the on-wafer diodes that would serve as standards for electronic calibration. The center conductor of the coplanar waveguide standards was 4.2 μm with a gap of 4 μm. To accommodate the probe tip pitch of 25 μm, the contact pads for the wafer probes have center width of 14 μm, a gap width of 11 μm, and are tapered to the CPW line dimensions. The measured S-parameters of the TRL standards are shown in Figure 4.13 and are well separated on the Smith Chart over the full 325—500 GHz band.

A scanning electron micrograph of the diode-based electronic standard is shown in Figure 4.11. The standard incorporates a shunt-connected varactor diode (as described above), two

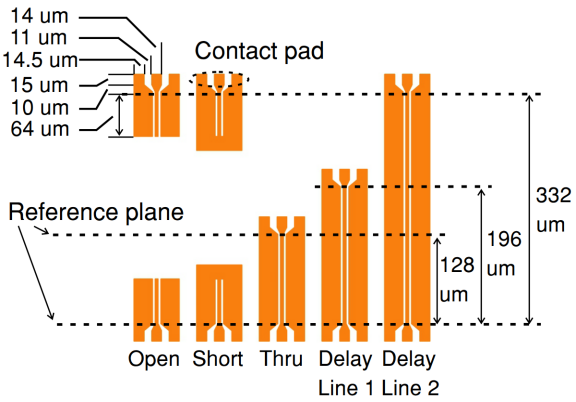
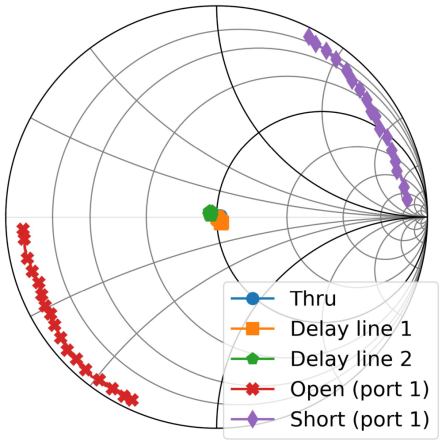
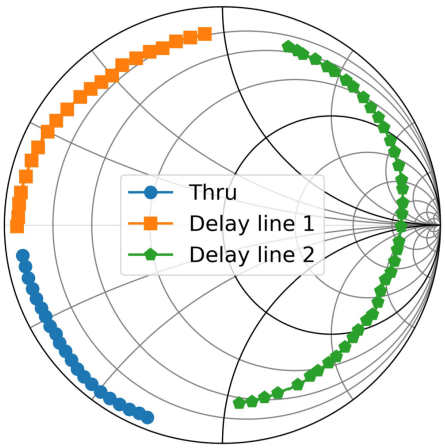


Figure 4.12: TRL calibration kit used for regular two port calibration of S-parameters measurement. The calibration standards are fabricated on the same wafer as the two port diodes and DUTs.



(a)



(b)

Figure 4.13: Measured S-parameters across the WR-2.2 band of the TRL standards used for regular two port calibration: (a) S_{11} (b) S_{21}.

80 µm long 50 Ω coplanar feed lines, and a pair of tapered contact pads to accommodate on-wafer probes. Bias to the diode is applied through the wafer probes and the measurement reference plane is set at the transition between the CPW feed lines and contact pads, as illustrated in Figure 4.11.

Scattering parameters of the diode standard are measured by Keithley 236 source measurement unit, as a function of bias, from -8 V to 0.8 V, over the full WM-570 frequency band (220—325 GHz) and corrected using the two-port error coefficients found from the on-wafer TRL calibration. As a set of 5 measurements are performed on the TRL calibration standards, the ensemble average of the 5 sets of error coefficients generated from these measurements are used to correct the scattering-parameters of the diode standard. Figure

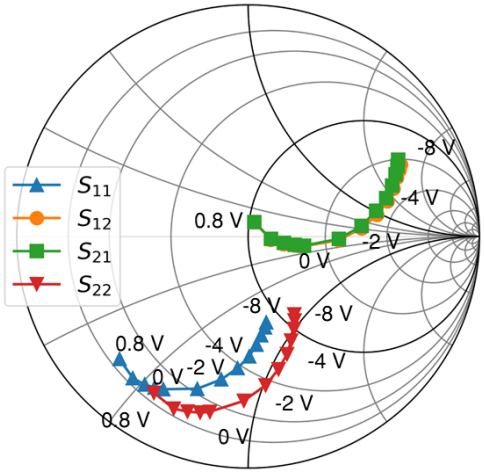


Figure 4.14: Measured S-parameters of the 2 port electronic calibration standard diodes at 425 GHz. The bias voltage is swept from -8 V to 0.8 V.

4.14 shows the resulting error-corrected two-port scattering parameters of the diode standard at center band (425 GHz) as a function of bias voltage. These scattering parameters are subsequently used to represent the diode circuit of Figure 4.11 for electronic on-wafer calibration.

The measurements were performed over WR-2.2 (WM-570) standard waveguide band (325—500 GHz), using a Cascade Microtech PA200 probe station equipped with frequency extenders from Virginia Diodes, Inc., and micromachined on-wafer probes developed previously at the University of Virginia and DMPI, Inc. [28, 29].

4.3.2 Error Model and Coefficients

The eight term error model with switch terms included for the two port calibration is shown in Figure 4.15 [97–99]. The $\{e_{ij}\}$ are the scattering parameters of the error network: e_{00}, e_{11}, $e_{01}e_{10}$ and Γ_{F} are forward directiviy, port match, reflection tracking and switch term respectively; e_{33}, e_{22}, $e_{23}e_{32}$ and Γ_{R} are reverse directiviy, port match, reflection tracking and switch term respectively; and k is the ratio of e_{10} over e_{23}. The general 8-term model is essentially an extension of the one-port algorithm to two-port measurements. The concept was first proposed in [100], and implemented in [99]. One of the 8 error terms can be normalized to yield 7 error terms [101]. Seven or more independent known conditions must be measured to determine the 7 error terms. A known impedance (Z_0) and a port-1 to

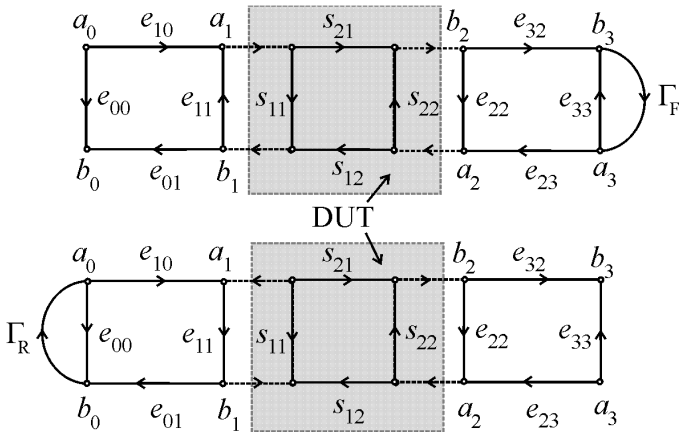


Figure 4.15: Eight term model of two port calibration of S-parameters measurement. The switch terms Γ_F and Γ_R are included too.

port-2 connection are required. Examples of the most common applications of the eight term model of two port calibration are Thru-Reflect-Line (TRL) and Unknown-Thru [102]. Cascade WinCal software is used to apply the multiline TRL calibration for characterizing the diode standards on the wafer for this work.

4.3.3 Implementation of On-Wafer Electronic Calibration

The error networks obtained from the regular calibration using TRL and electronic calibration using the two port diode are compared in terms of mean value (both magnitude and phase) and complex standard deviation, calculated by

$$STD = \sqrt{\frac{1}{N}\sum_{k=1}^{N}|E_k - \bar{E}|^2} \tag{4.3}$$

In (4.3), $N = 5$, E_k is the error coefficient of interest, and $\bar{E}$ is its (complex) mean. For the statistical analysis, all devices on the wafer are measured five times, including the TRL calibration standards for the regular calibration, thus generating five sets of error networks. In order to obtain the error network from electronic calibration using integrated two-port Schottky diode as the calibration standard, the characterized response of the Schottky diode is applied to the corrected data using the five error networks from multiline TRL calibration, and the *raw* (uncorrected) responses are from the corresponding five measurements, thus generating five sets of error networks for the electronic calibration. The comparison of

on-wafer measurements of S_{11} and S_{21} is at reference plane tier 2. The results are shown in Figure 4.16, 4.17 and 4.18 for the forward model and reverse error models, respectively.

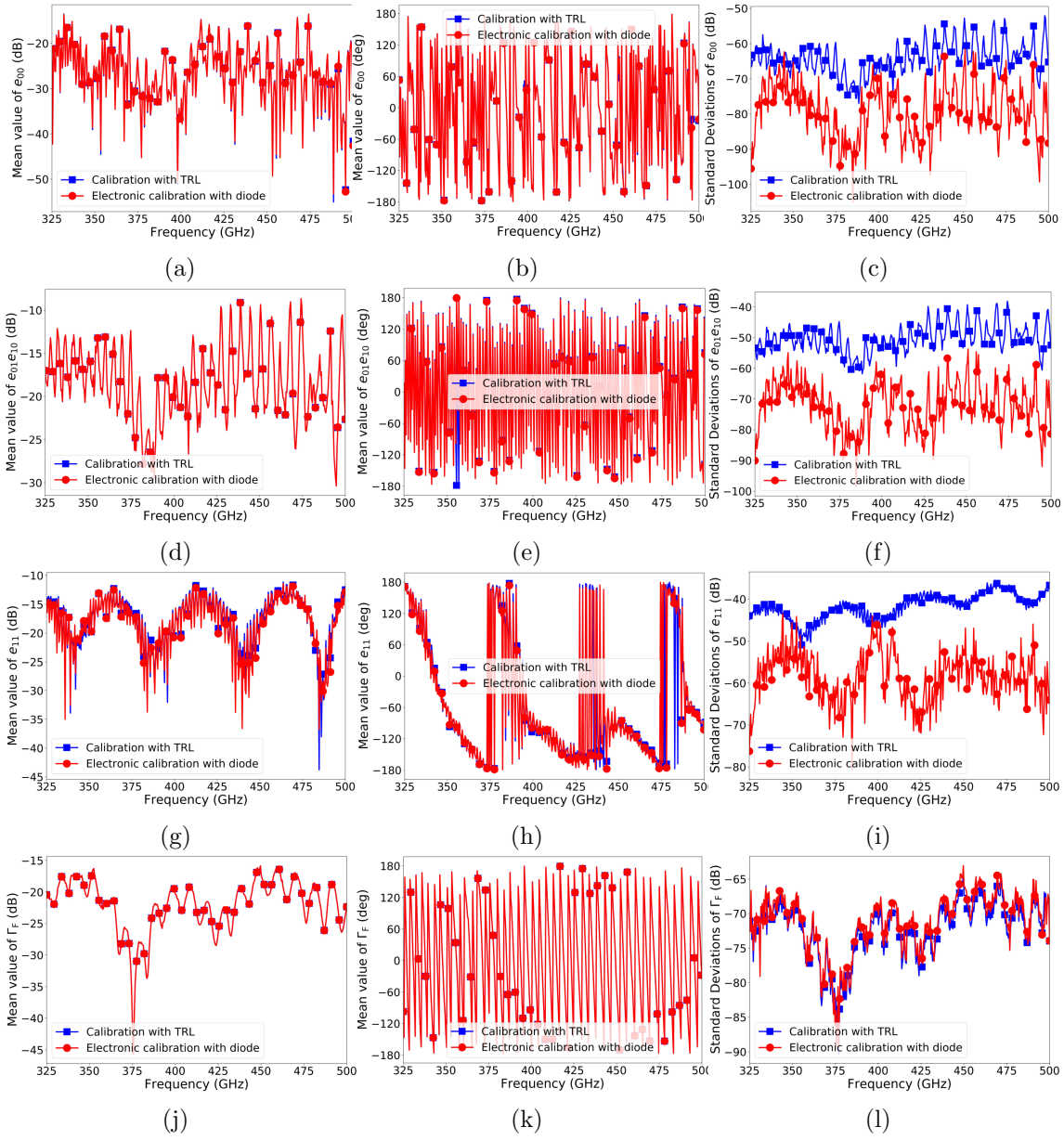


Figure 4.16: Comparison of forward model error terms: e_{00}, $e_{01}e_{10}$, e_{11} and Γ_F of error network from WR-2.2 two port electronic calibration results and TRL calibration. (a) Magnitude of mean value of e_{00} in dB. (b) Phase of mean value of e_{00} in degrees. (c) Complex standard deviation of e_{00} in dB. (d) Magnitude of mean value of $e_{01}e_{10}$ in dB. (e) Phase of mean value of $e_{01}e_{10}$ in degrees. (f) Complex standard deviation of $e_{01}e_{10}$ in dB. (g) Magnitude of mean value of e_{11} in dB. (h) Phase of mean value of e_{11} in degrees. (i) complex standard deviation of e_{11} in dB. (j) Magnitude of mean value of Γ_F in dB. (k) Phase of mean value of Γ_F in degrees. (l) Complex standard deviation of Γ_F in dB.

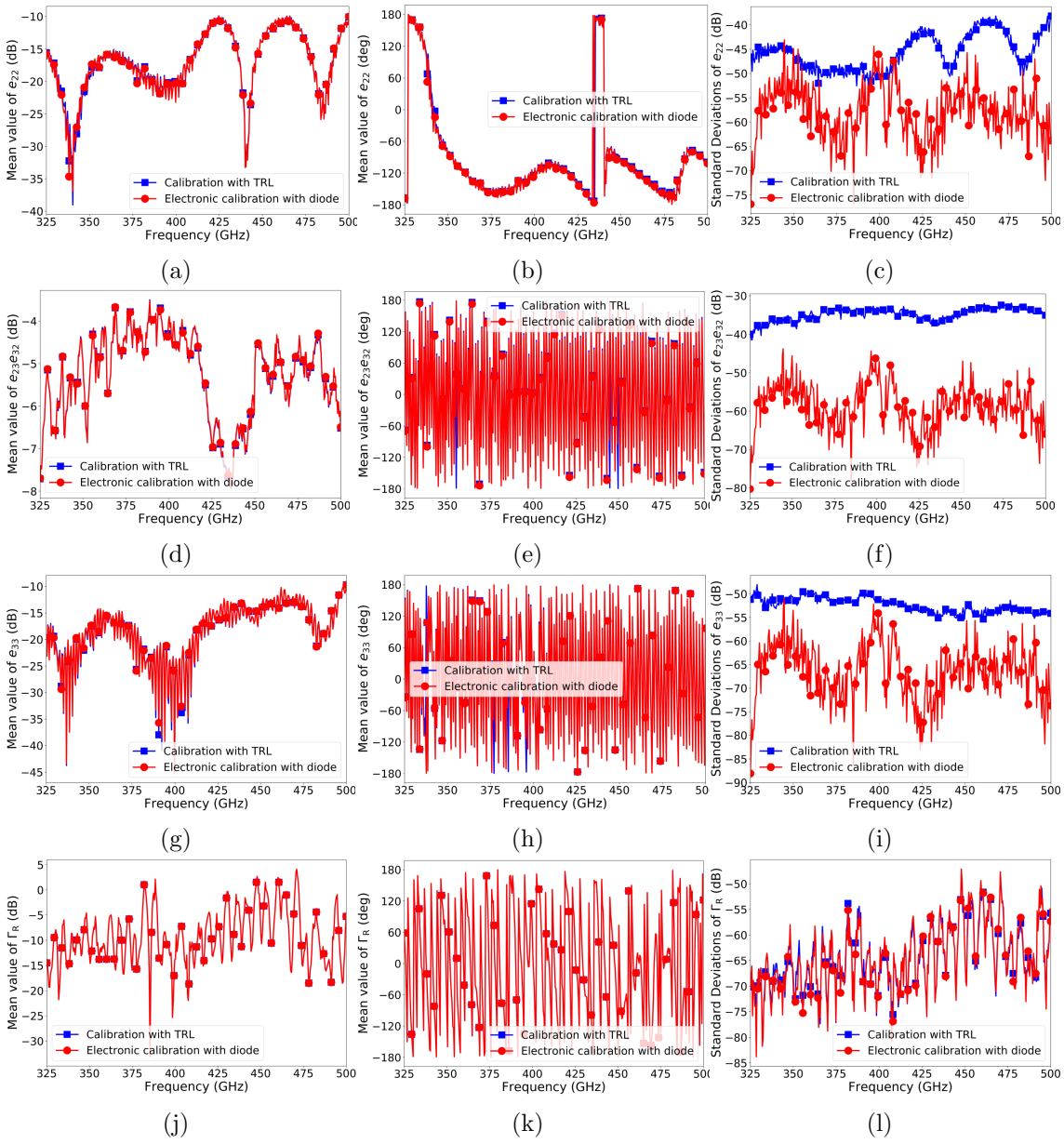
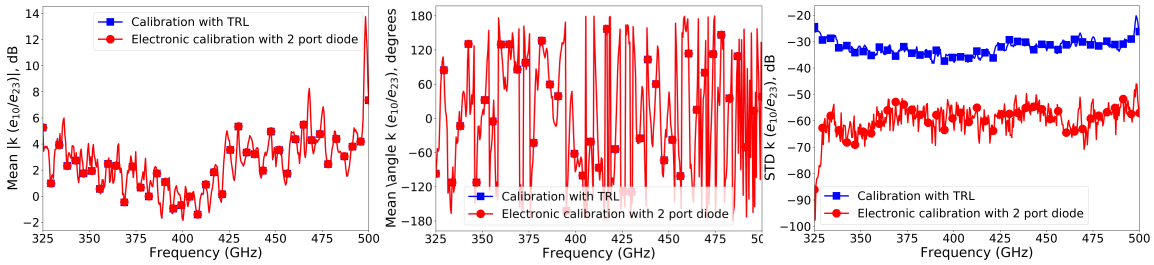


Figure 4.17: Comparison of reverse model error terms: e_{22}, $e_{23}e_{32}$, e_{33} and Γ_R of error network from WR-2.2 two port electronic calibration results and TRL calibration. (a) Magnitude of mean value of e_{22} in dB. (b) Phase of mean value of e_{22} in degrees. (c) Complex standard deviation of e_{22} in dB. (d) Magnitude of mean value of $e_{23}e_{32}$ in dB. (e) Phase of mean value of $e_{23}e_{32}$ in degrees. (f) Complex standard deviation of $e_{23}e_{32}$ in dB. (g) Magnitude of mean value of e_{33} in dB. (h) Phase of mean value of e_{33} in degrees. (i) Complex standard deviation of e_{33} in dB. (j) Magnitude of mean value of Γ_R in dB. (k) Phase of mean value of Γ_R in degrees. (l) Complex standard deviation of Γ_R in dB.

From Figure 4.16, 4.17 and 4.18, all the error network coefficients (directivity, reflection tracking, source match, switch terms of both forward direction and reverse direction and



(a) (b) (c)

Figure 4.18: Comparison of k (e_{10}/e_{23}) error terms from WR-2.2 two port electronic calibration results and TRL calibration. (a) Magnitude of mean value of k in dB. (b) Phase of mean value of k in degrees. (c) Complex standard deviation of k in dB.

k) of the electronic calibration using integrated Schottky diodes agree well with that from multiline TRL calibration in terms of mean value, and the standard deviation is 10-30 dB lower except for the switch terms. The possible reason for the no improvement of switch terms is that the switch terms are due to the internal switch within the VNA, and they are very repeatable compared to the other error terms and the uncertainty of the switch terms are at the same level as the uncertainty of the source unit biasing the diode. In summary, the electronic calibration is seen to be as accurate as a standard TRL calibration. Our data indicates an improvement in precision (repeatability).

The standing wave in e_{11} (Figure 4.16g and Figure 4.16h) are due to the probe shown in Figure 4.8. The high frequency ripple (≈1-2 GHz spacing) is due to the long waveguide between the port interface and the waveguide transition, while the lower frequency ripple is associated with the waveguide transition to probe tip.

4.3.4 Application of On-Wafer Measurement Results of S-parameters

After the error networks are obtained as described previously, they are applied to several on-wafer DUTs respectively to calculate the corrected scattering parameters from the same raw data of the DUT measured from the VNA. The corrected scattering parameters of different DUTs are compared to that from regular calibration using TRL. The DUTs measured include a coplanar Thru and a Schottky diode. Because the DUTs are measured five times, which produces a set of *raw* (uncorrected) data, and there are five sets of error networks for

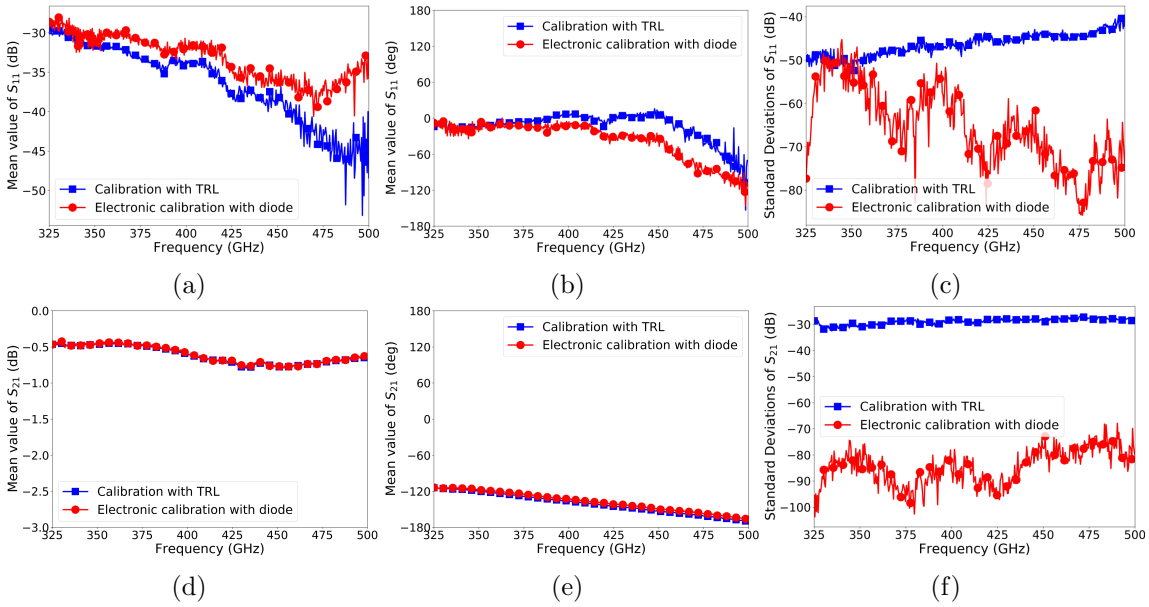


Figure 4.19: Comparison of WR-2.2 two port electronic calibration results and TRL calibration results to a Thru. (a) Magnitude of mean value of S_{11} in dB. (b) Phase of mean value of S_{11} in degrees. (c) Complex standard deviation of S_{11} in dB. (d) Magnitude of mean value of S_{21} in dB. (e) Phase of mean value of S_{21} in degrees. (f) Complex standard deviation of S_{21} in dB.

both TRL calibration using TRL and electronic calibration, the permutation generates five sets of corrected scattering parameters for each of the *raw* data sets.

DUT: Coplanar Thru

The coplanar Thru is part of the multiline TRL calibration kit shown in Figure 4.12. The corrected response of the Thru using the TRL calibration is shown in Figure 4.13. Figure 4.19 shows the comparison of corrected S-parameters using TRL and electronic calibration for one of the five *raw* data of Thru. The mean value of corrected transmission coefficient (S_{21}) of the Thru from electronic calibration using the diode standard agrees well with calibration using TRL and the complex standard deviation from electronic calibration is computed to be about 60 dB lower than that from calibration using TRL. For the reflection coefficient (S_{11}), there's some deviation between the result from calibration using TRL and electronic calibration using diode. This is probably due to the numerical error associated with small numbers near to zero. Only one set of results is shown here but similar results are obtained for other four sets of *raw* data too.

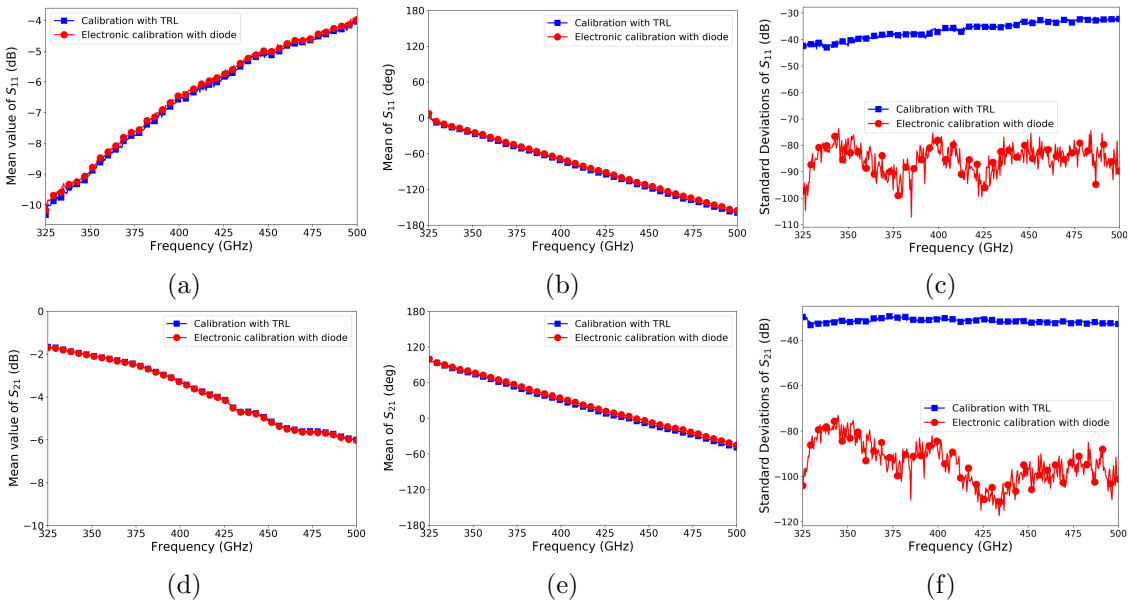


Figure 4.20: Comparison of WR-2.2 two port electronic calibration results and TRL calibration results to a two port diode structure with 4.0 um anode size. (a) Magnitude of mean value of S_{11} in dB. (b) Phase of mean value of S_{11} in degrees. (c) Complex standard deviation of S_{11} in dB. (d) Magnitude of mean value of S_{21} in dB. (e) Phase of mean value of S_{21} in degrees. (f) Complex standard deviation of S_{21} in dB.

DUT: Two-Port Diode

A diode is also used as a DUT to compare the calibration methods. The corrected S-parameters of the two-port diode is shown in Figure 4.14. Figure 4.20 shows the comparison of corrected S-parameters using TRL and electronic calibration using the diode for one of the five *raw* data of the two-port diode. For the purpose of demonstration, only a single bias point at -4V is used as an example for the electronic calibration. The mean value of both corrected transmission coefficient (S_{21}) and corrected reflection coefficient (S_{11}) from electronic calibration using the diode agree well with calibration using TRL and the complex standard deviation from electronic calibration is about 60 dB lower than that from calibration using TRL. Only one set of results is shown here but similar results are obtained for other four sets of *raw* data too.

4.4 Conclusion

This work has demonstrated an approach for electronic calibration of on-wafer measurements at submillimeter-wave frequencies based on integrated Schottky diode standards. The diodes were characterized using a set of conventional coplanar on-wafer standards, allowing propagation of those standards to the diode electronic standard. The error coefficients derived using the electronic standard show good agreement with the coplanar delayed-short standards (for one port calibration case) and coplanar TRL standards (for two port calibration case) over the full WM-570 (325—500 GHz) frequency band.

Future work implementations will include adding tuning elements or additional diodes to increase the coverage of diode standard over a larger portion of the Smith Chart.

Chapter 5

Micromachined Probes with Integrated GaAs Schottky Diodes for On-Wafer Temperature Sensing

This chapter is based partly on the publications (with some modifications and augmentations).

- **L. Xie**, C. M. Moore, M. E. Cyberey, S. Nadri, N. D. Sauber, M. F. Bauwens, A. W. Lichtenberger, N. Scott Barker, R. M. Weikle, II, "Micromachined probes with integrated GaAs Schottky diodes for on-wafer temperature sensing," *International Instrumentation and Measurement Technology Conference*, Houston, TX, USA, May 2018, pp. 1–6, doi: 10.1109/I2MTC.2018.8409690.

This chapter reports a micromachined on-wafer probe integrated with Schottky diode sensors for the first time. The design and fabrication process for implementing an on-wafer probe with integrated diode temperature sensor are described. The sensor consists of a wafer probe fabricated from high-resistivity silicon using micromachining techniques. The temperature sensing element is a GaAs Schottky diode that is integrated onto the probe through an epitaxy transfer process that utilizes SU-8 as a bonding agent. Design of the probe as well as fabrication and measurement of prototype diodes for the temperature sensor are detailed.

5.1 Introduction

On-wafer characterization of cryogenically-cooled millimeter-wave devices, which are critical components used for a variety of heterodyne instruments, presents a significant challenge to test engineers. To collect relevant RF performance data, for example, the sample stage to which devices are affixed typically must reach temperatures below 20 K for low-noise amplifiers [103, 104] and below 5 K for niobium-based superconducting components such as hot electron bolometer (HEB) detectors and semiconductor-insulator-semiconductor (SIS) mixers [105, 106]. Systems for on-wafer metrology of these cryogenic devices, as a result, must carefully balance the requirement of low RF path loss with that of minimum heat load on the devices under test (DUT).

RF frequency cryogenic on-wafer characterization of DUTs has been studied in the past [107, 108]. In more recent work in 2015, Daughton et al, reported the first use of on-wafer probes to measure millimeter-wave cryogenic devices [4] in the WR-5.1 band (140—220 GHz). In that work, an on-wafer probe fabricated from micromachined silicon [109] was incorporated into a cryogenic probe station (Lakeshore model TTP-6), as illustrated in Figure 5.1. Copper braids anchored to the radiation shield of the probe station were used to thermally ground the probe housing, and diode sensors mounted to the probe body monitored the temperature and stability of the assembly. This arrangement permitted on-wafer measurements at temperatures to 9 K, limited by the thermal load associated with the probe contacting the DUT [5].

Practical implementation of systems such as that depicted in Figure 5.1 requires placing temperature sensors some distance from the DUT. Improper thermal grounding of the probe as well as power dissipation in the device can result in elevated temperatures near the DUT, generating thermal gradients and associated errors in temperature measurement. To address this issue, this paper describes a diode-based temperature sensor integrated onto a micromachined probe tip that permits direct monitoring of temperature near a DUT. The temperature sensor is implemented using an epitaxy transfer process in which III-V semiconductor material is heterogeneously integrated onto high-resistivity silicon. Subsequent processing and micromachining of the silicon is used to form the diode temperature sensor

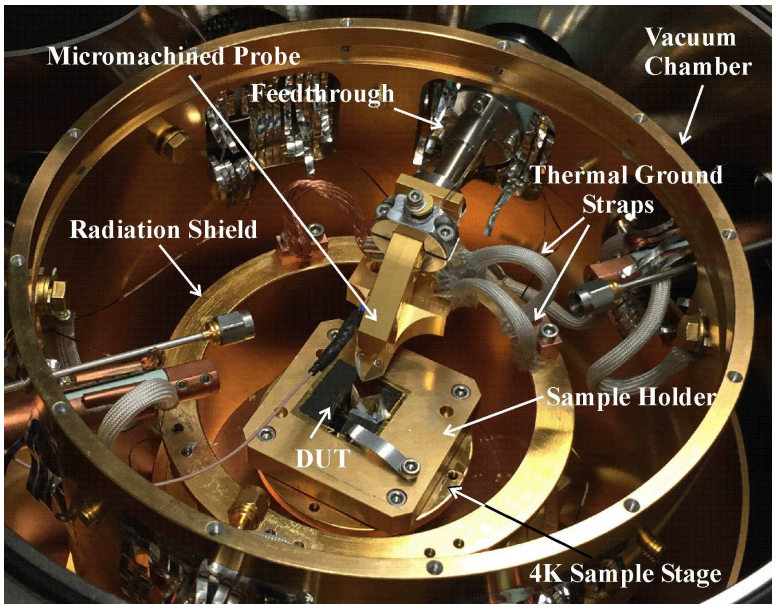


Figure 5.1: Configuration of the Lakeshore TTP-6 cryogenic probe station for on-wafer measurements.

and fully-integrated on-wafer probe chip.

5.2 Low-Temperature Diode Characterization

The prototype quasi-vertical diodes for a proof-of-concept temperature sensor probe were fabricated by the process described in Chapter 2, and characterized at low temperatures cooled down by liquid nitrogen and liquid helium respectively.

5.2.1 Liquid Nitrogen Cooling Measurement

The prototype quasi-vertical diodes were characterized using a Lakeshore TTP-6 cryogenic probe station for the liquid nitrogen cooling measurement. Sample diodes were mounted to the cryostat cold stage using Apiezon N Grease, held in place with a clip, and the cryostat was cooled with liquid nitrogen to 77 K. For this test, the contact pads of the diodes were connected to feedthroughs using DC probes and the diode current-voltage characteristics measured as a function of the temperature of the cold stage. Calibrated silicon thermometers secured directly onto the substrate by a thermally anchored clip were used to measure the

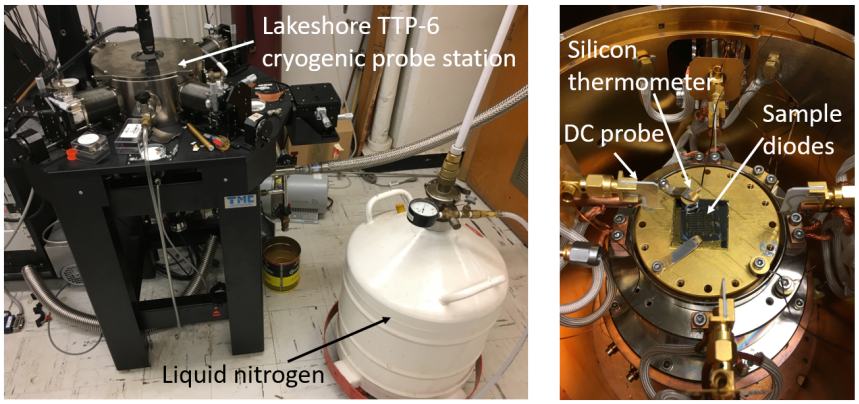
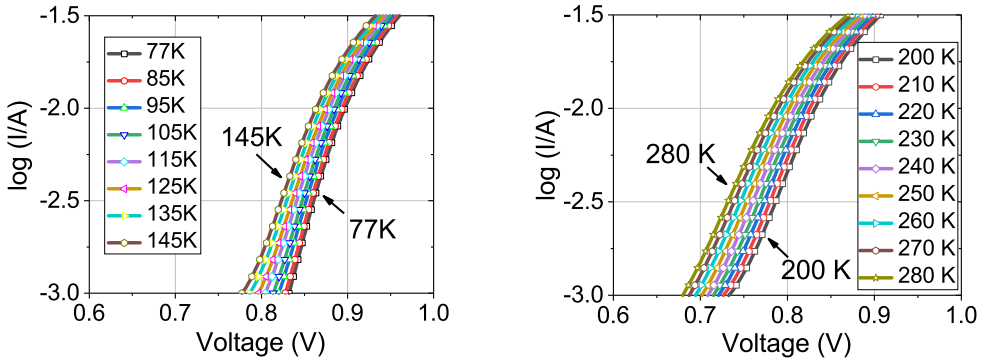


Figure 5.2: Image of the measurement setup for cryogenic characterization of a quasi-vertical diode by liquid nitrogen cooling.

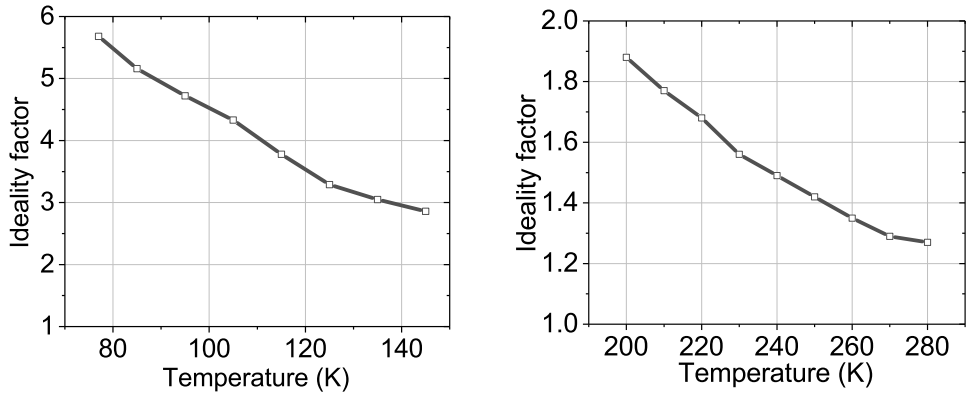


(a) (b)

Figure 5.3: Measured forward voltage-current characteristic of two diodes in two temperature ranges.

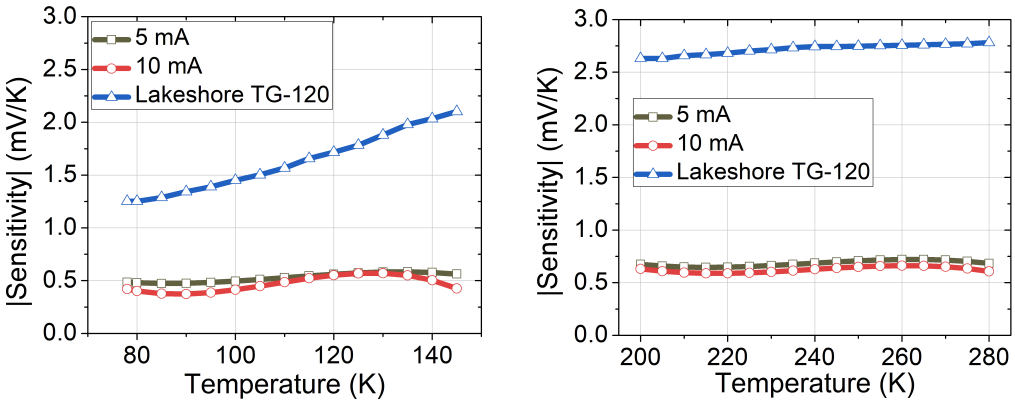
diode temperature. Once temperature was achieved the stage was slowly brought back to room temperate through the use of a heater.

Figure 5.2 shows the measurement setup. Figure 5.3 shows the measured current-voltage characteristics of the heterogeneously-integrated Schottky diodes as a function of temperature and Figure 5.4 the change in diode ideality factor over the corresponding temperature range, which might be explained by [110, 111]. The sensitivity of the GaAs Schottky diodes as a temperature sensor was extracted from these data and is shown in Fig. 5.5 in comparison to a commercial GaAlAs diode. The sensitivity is approximately $0.5-1.0$ mV/K. This is approximately one-quarter that of commercial GaAlAs sensors, which are typically biased at lower bias currents (1 µA) where the sensitivity is higher. Because the quasi-vertical diodes are bonded to silicon, current conduction in the silicon dominates at low bias voltages,



(a) (b)

Figure 5.4: Extracted idealty factor of two diodes at 1mA bias current in two temperature ranges.



(a) (b)

Figure 5.5: Measured sensitivity at different bias current of two diodes in two temperature ranges compared to GaAlAs diodes from Lakeshore Inc. [15].

necessitating the use of higher bias currents (near 1 mA) for the Schottky diodes studied in this work.

5.2.2 Liquid Helium Cooling Measurement

Another sample diode was mounted to the cryostat cold stage using Apiezon N Grease, held in place with a clip, and the cryostat was cooled with liquid helium to 4 K. For this test, the contact pads of the diodes were connected to feedthroughs using DC probes and the diode current-voltage characteristics measured as a function of the temperature of the cold stage. Calibrated silicon thermometers secured directly onto the substrate by a thermally

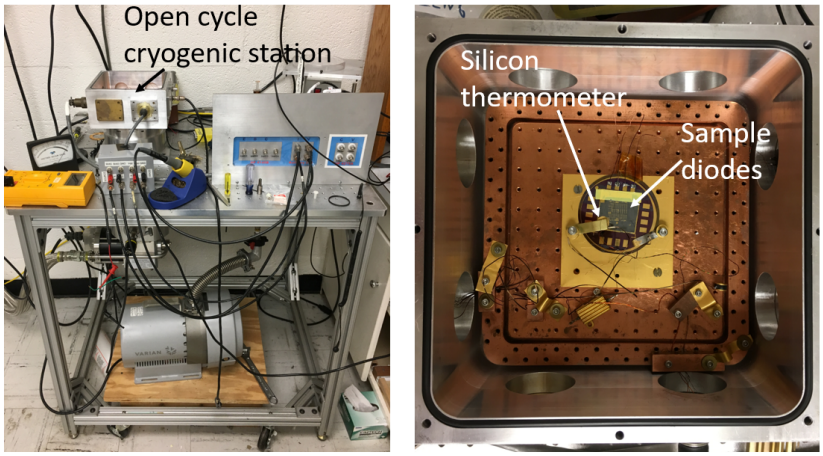


Figure 5.6: Image of the measurement setup for cryogenic characterization of a quasi-vertical diode by liquid nitrogen cooling.

anchored clip were used to measure the diode temperature. Once temperature was achieved the stage was slowly brought back to room temperate through the use of a heater.

The measurement setup and results are shown in Figure 5.6. Figure 5.7a shows the measured current-voltage characteristics of the heterogeneously-integrated Schottky diodes as a function of temperature for the liquid helium cooling and Figure 5.7b shows that when the temperature drops below 30 K, the carriers in the silicon starts to freeze out, presenting the substrate an ideal insulator to the GaAs Schottky diode. In this region, the impedance of the diode device can be viewed as the GaAs diode itself without the presence of the silicon substrate.

The sensitivity of the GaAs Schottky diodes as a temperature sensor was extracted from these data and is shown in Figure 5.8 in comparison to a commercial GaAlAs diode. The sensitivity is approximately 0.2−2.0 mV/K. This is approximately one-quarter that of commercial GaAlAs sensors in the temperature range of 70-300 K, which are typically biased at lower bias currents (1 μA) where the sensitivity is higher. Because the quasi-vertical diodes are bonded to silicon, current conduction in the silicon dominates at low bias voltages, necessitating the use of higher bias currents (near 1 mA) for the Schottky diodes studied in this work. In the temperature range of below 70 K, the sensitivity is significantly lower than that of commercial GaAlAs diode.

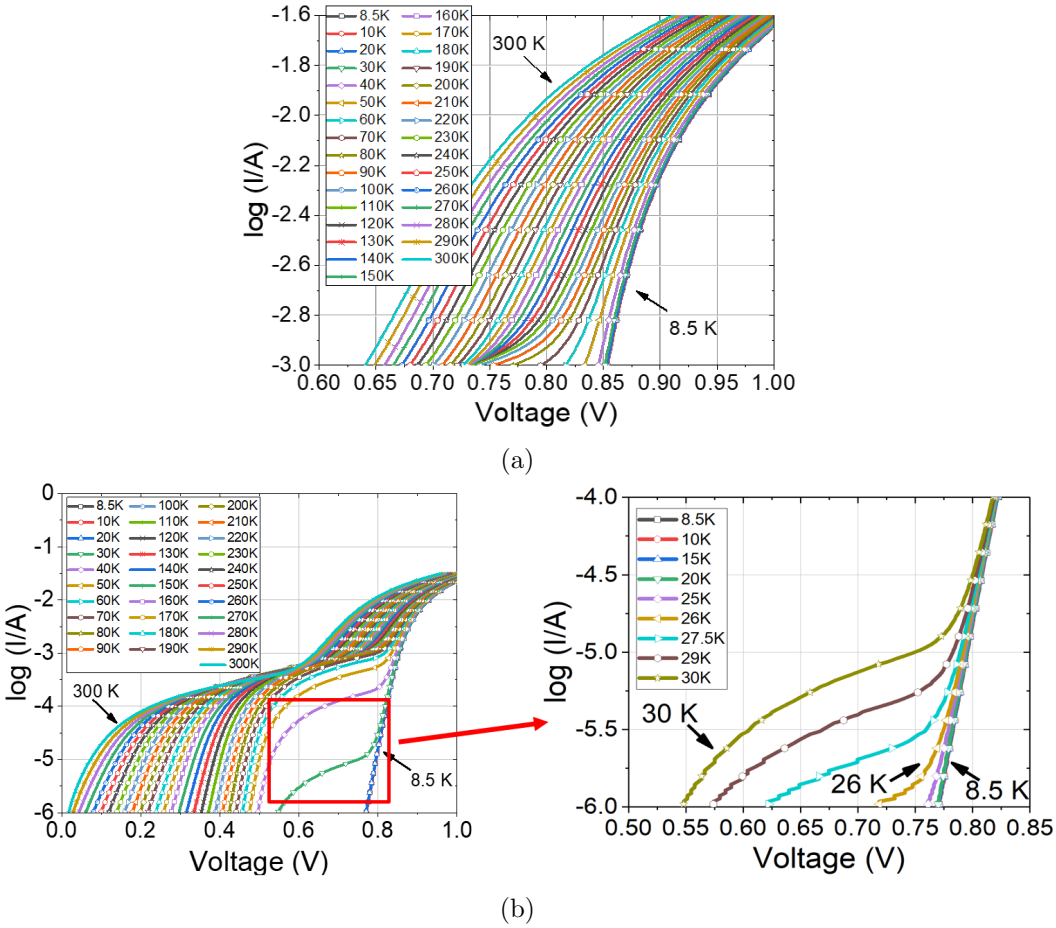


Figure 5.7: Measured voltage-current characteristic of one proof-of-concept diode cooled down in liquid helium. (a) Forward region only (b) Full bias span and zoom in view of the region where carriers freeze out.

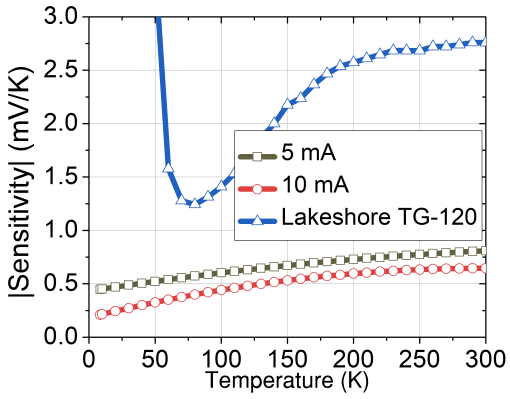


Figure 5.8: Measured sensitivity at different bias current of one proof-of-concept diode cooled down in liquid helium compared to GaAlAs diodes from Lakeshore Inc. [15].

5.3 Temperature Sensor Probe Design

A micromachined on-wafer probe with integrated diode temperature sensor, based on the micromachining and heterogeneous integration processes described above has been designed and processed. Figure 5.9 shows the comparison of chip layout of the proposed temperature sensor probe and the cryogenic micromachined on-wafer probe developed by the University of Virginia and DMPI, Inc. [4], including back-end electrical contacts and alignment and mounting tabs for assembling the probe into its housing. Compard to regular submillimeter-wave and THz micromachined on-wafer probes, the temperature sensor probe removes the transmission lines (MSL or CPW) connecting the probe tips and the waveguide at the back-end of the probe housing. The metalized probe tips do not couple RF signal between on-wafer DUT and the measurement instrument interfacing with waveguide at the back-end of the probe. The probe tips in the temperature sensor probe only provides the path of thermal conduction between the on-wafer DUT and the diode temperature sensor in the probe. The diode is placed near the contact tips where the probe interfaces to the DUT. The area of the back-end beamleads of the temperature sensor probe is enlarged to accommodate the four DC contact pads for the four point sensing IV measurement.

Figure 5.10a shows a finite-element model of the region near the probe tip and illustrates

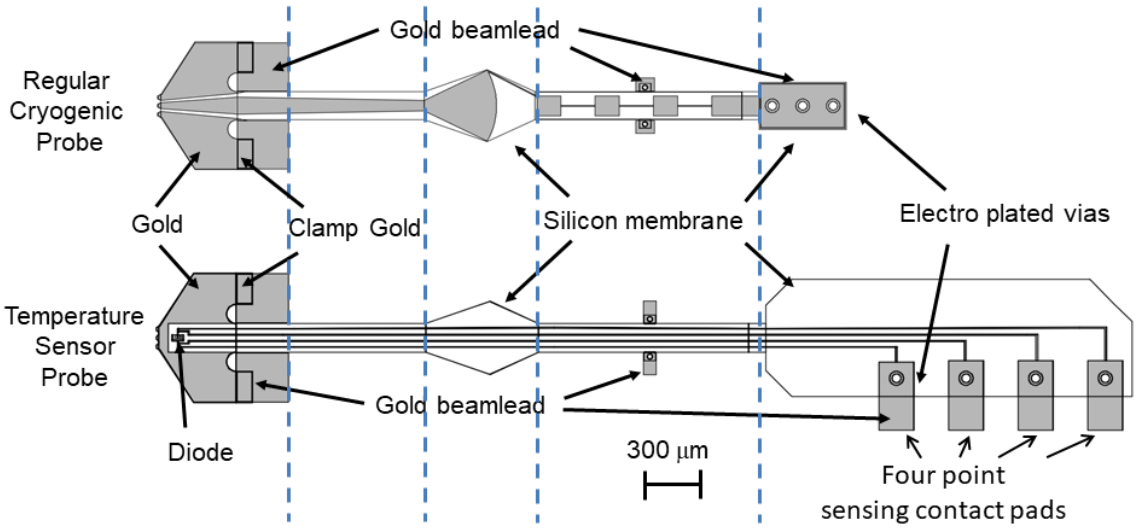


Figure 5.9: Chip layout of two micromachined on-wafer probes. (a) Top: on-wafer probes used in on-wafer S-parameters measurement in cryogenic temperatures up to 77K [4]. (b) Bottom: proposed temperature sensor probes with integrated GaAs Schottky diodes.

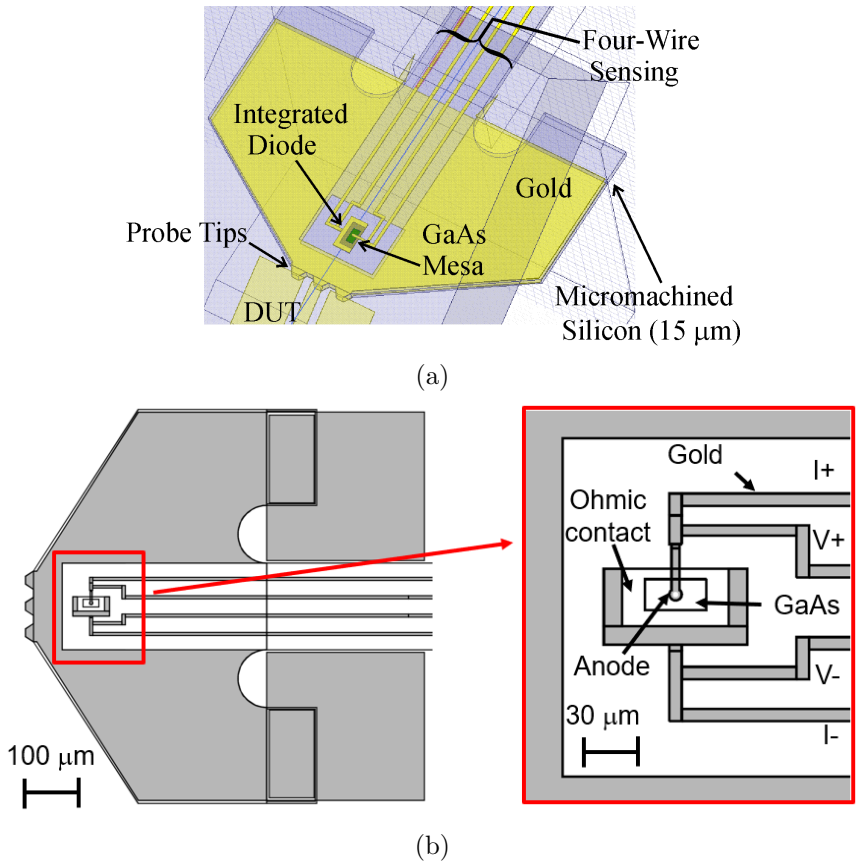
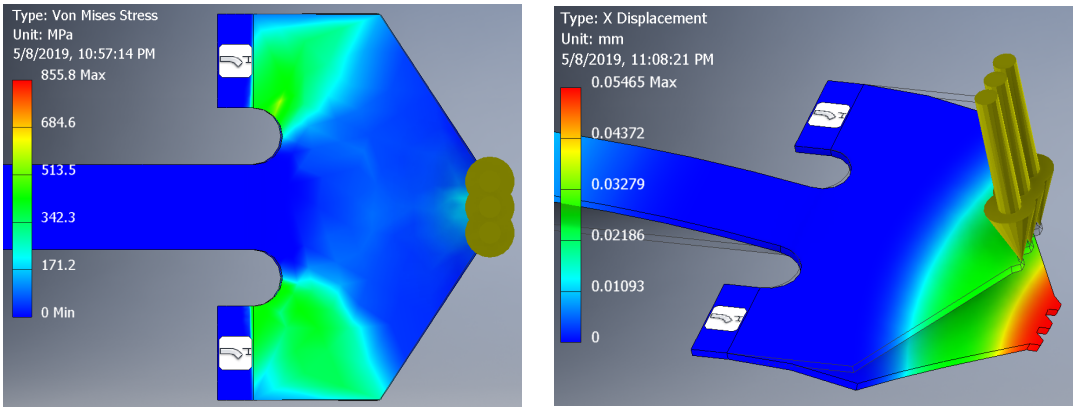


Figure 5.10: Layout of a micromachined wafer probe incorporating a diode temperature sensor. (a) Electromagnetic simulation model showing details of the probe tip, and (b) Zoom in view of the probe tip area.

the location of the diode temperature sensor as well as the sensing circuitry used to measure the diode current-voltage characteristic. The zoom in view of the probe tip area of the temperature sensor probe is shown in Figure 5.10b.

5.3.1 Finite-Element Simulation

The finite element model of the probe chip is simulated using the Autodesk Inventor Mechanical software package to estimate the stress induced in the probe chip with each tip subject to a 10 mN load, corresponding to the typical contact force required for a low-resistance electrical interface [29]. The result of this simulation is shown in Figure 5.11a. To minimize the impact of induced strain on the diode electrical characteristics and mechanical integrity [112], the integrated diode temperature sensor is placed near the probe tip in a region of low induced stress. The largest stress in the silicon (1.1 GPa) occurs in



(a) (b)

Figure 5.11: Mechanical simulation of the temperature-sensor probe induced in the chip when subject to a 10 mN/tip load: (a) stress (b) displacement.

the region where the chip is clamped to its housing. Rounded fillets in these regions are included in the chip design to ensure the stress remains well below the yield strength of silicon (4.5 GPa).

5.4 Temperature Sensor Probe Fabrication

The fabrication process of the temerature sensor probe is similar to that of the 160 GHz frequency quadrupler reimplemented with the revised GaAs epitaxy transfer process described in Chapter 3. The differences are as follows:

- Extra 10 μm thick clamp gold is patterned and electroplated in the clamp region besides the ≈ 2μm thick front side gold [113]. The extra clamp gold is to provide extra gold to fill in the gap between the two halves of the probe block when the probe chip is assembled in the housing.

- An extra lithography step is introduced to expose and develop the photoresist in the via holes for the sacrificial layer step and top metal plating step. This extra exposing via step is to make sure there's no trapped photoresist in the via holes that prevent metalization of the via holes.

- Backside of the SOI device layer is also patterned by lithography and electroplated to provide thermal sink to the temperature sensor probe.

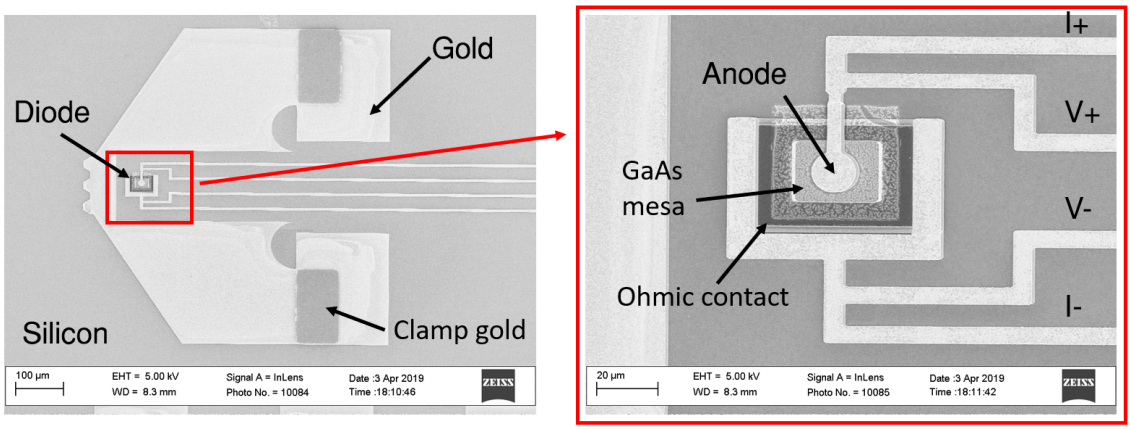


Figure 5.12: SEM of the tip area of temperature sensor probe: front side.

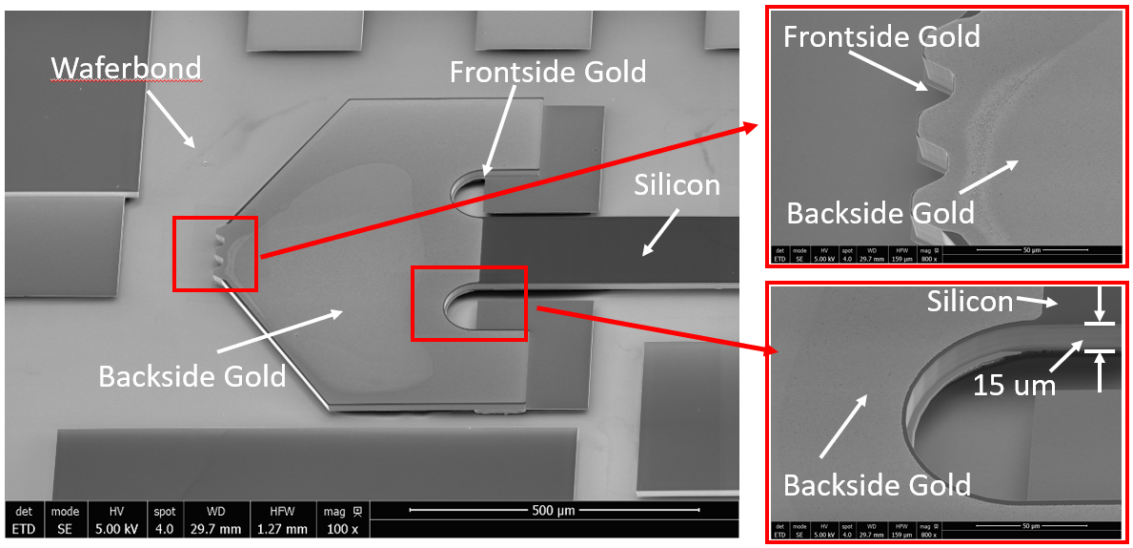


Figure 5.13: SEM of the tip area of temperature sensor probe: back side.

An SEM image of the front side of the probe tip area of the integrated temperature sensor probe before backside processing is shown in Figure 5.12. Then the wafer is flipped and temporarily bonded to a silicon carrier wafer for backside processing. Figure 5.13 shows the SEM images of the backside of the probe tip area right before releasing the chips using waferbond remover. Note that the silicon extents etch is clean, and there's no silicon leftover ("rim") which would act as a possible source of fracture that could then propagate through the chip on the first contact cycle even at low contact force and result in the probe breaking [2].

A Keithley 236 source measurement unit is used for DC measurement of the temperature

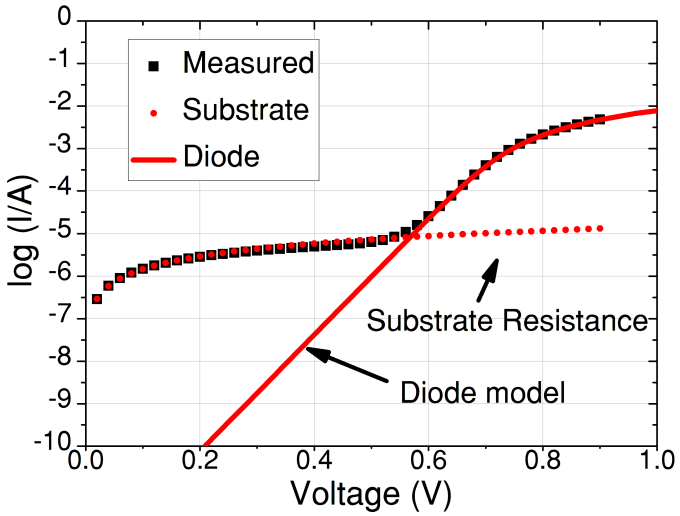


Figure 5.14: Measured room temperature current-voltage characteristic of a quasi-vertical Schottky diode integrated on high-resistivity silicon.

Table 5.1: Extracted DC parameters and parameters normalized to anode area of the temperature sensor probe.

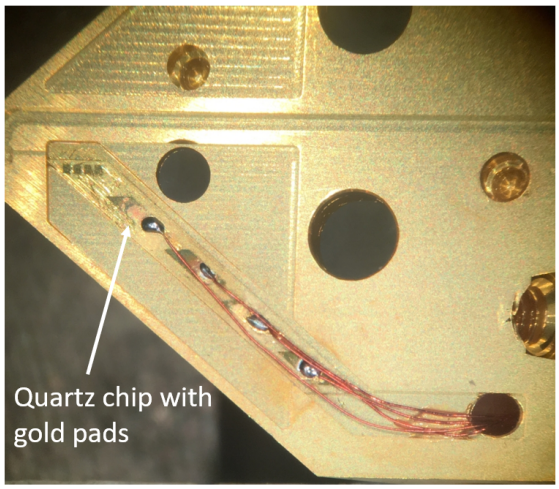
Anode diameter	Ideality factor	Series resistance	Saturation current	Normalized Conductance	Normalized Saturation Current
3 μm	1.27	27.3 Ω	0.1 pA	1.3 mS/μm^2	0.014 pA/μm^2

sensor probe at room temperature. The result is shown in Figure 5.14 and the extracted DC parameters are shown in Table 5.1. The ideality factor and saturation current are consistent with previous runs. The extracted series resistance is larger than expected, possibly due to unexpected inconsitency in the fabrication.

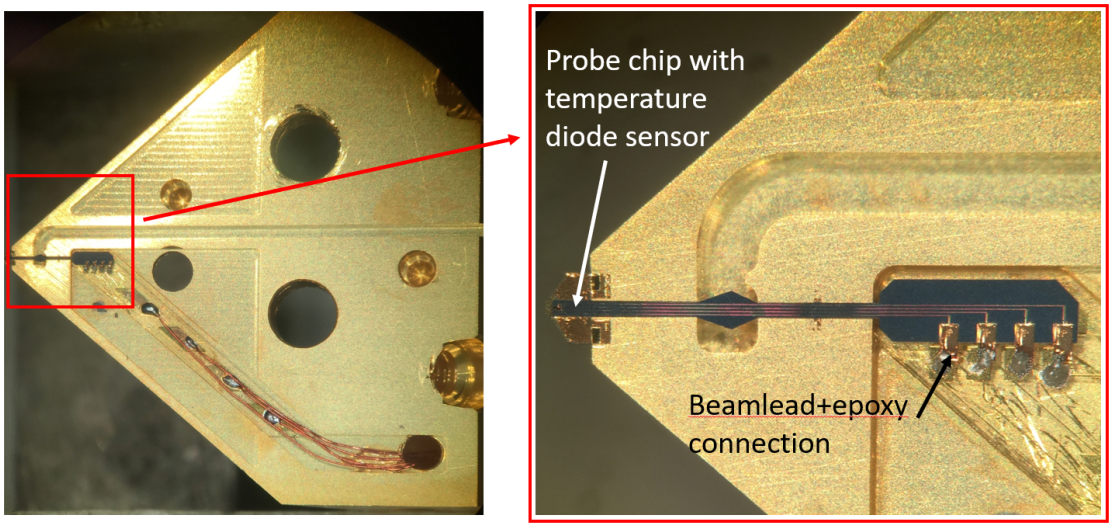
5.5 Proof-of-Concept Temperature Sensor Probe Assembly and Measurement

After the temperature sensor probe chips are released, one of the chips with open-circuited diodes is mounted in the probe housing block for sanity check. Figure 5.15a and Figure 5.15b show the pictures of the assembly consists of the quartz DC bias chip and temperature sensor probe silicon membrane chip into the probe housing.

A proof-of-concept characterization of the diode-open-circuited temperature sensor probe is carried out using a hot plate controlled by Micromanipulator Co. model HSM stage



(a)



(b)

Figure 5.15: Assembling of the probe thermometer into the waveguide housing. (a) Mounting quartz chip into the recess and solder wires onto the gold pads (b) Tacking down the probe chip with integrated diode temperature sensor and strengthened the connection with epoxy.

temperature controller. The temperature sensor probe housing is fixed onto the hot plate by kapton tapes. Current and voltage are measured from 25°C (298.15 K) to 95°C (368.18 K) using a two point sensing setup. Keithely 236 source measurement unit is used for the current-voltage measurement. Figure 5.16 shows the measurement setup.

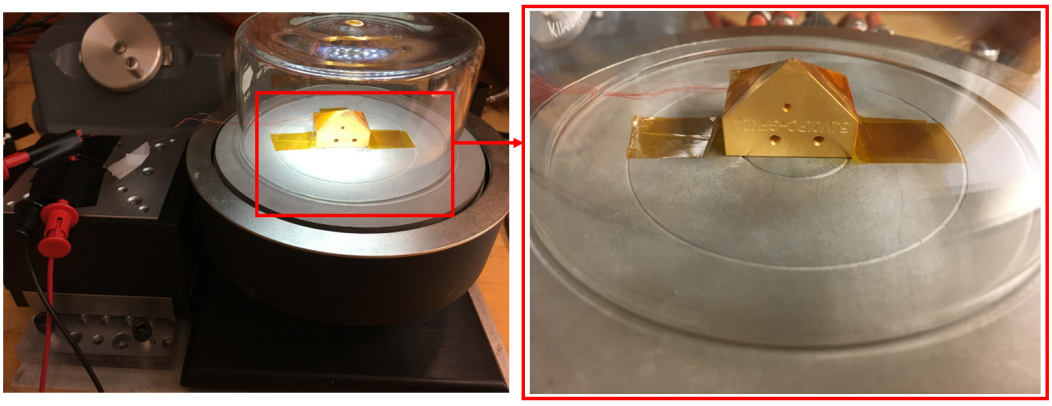


Figure 5.16: Measurement setup of the prototype characterization of the temperature sensor probe.

5.6 Temperature Sensor Probe Measurement Plans

5.6.1 Temperature Measurement

The temperature sensor probe will be characterized both on the hot plate and in the cryogenic probe station. For the heating up measurement using hot plates, the temperature sensor probe will be first characterized the same way as the dummy sample with the diode open circuited, i.e. fixing the probe housing metal surface on the hot plate. Then the temperature sensor probe will be characterized with the probe tips landing on a silicon wafer sitting on the hot plate. This will be the actual operation mode of the temperature sensor probe.

After the heating up measurement, the temperature sensor probe will be cooled down in the cryogenic probe station by liquid nitrogen and liquid helium, respectively. The measurement setup will be similar to that in [4], except that only DC measurements will be carried out to get the temperature of the on-wafer DUT.

5.6.2 Mechanical Properties Characterization

The purpose of mechanical performance evaluation is to ensure that the integrated temperature sensor probe provides repeatable response to a certain contact force as well as measuring the probe contact angle accurately and precisely. The measurement setup is similar to previous work by Chen and Yu [94, 114]. A load cell (Futek FSH0234) is used to measure the contact force generated by the probe contact. A goniometer stage (Newport

481-A) is mounted on the motor-drive stage to change the contact angle by tilting the test substrate.

5.7 Conclusions and Future Work

This work has described the design and fabrication process for implementing an integrated on-wafer temperature sensor that, for the first time, combines a silicon micromachined probe with a heterogeneously-integrated III-V diode thermometer. The prototype diodes fabricated for this study are characterized at cryogenic temperatures from 8.5 K to 300 K. The diodes show comparable performance to commercial GaAlAs thermometers in the 70K-300 K temperature range. A proof-of-concept assembly and measurement of the temperature sensor probe with open-circuited diode is carried out, where the probe housing is in direct contact with the hotplate. Future work will include room temperature measurement and cryogenic measurement of the temperature sensor probe with the probe tips in contact with the on-wafer DUTs.

Chapter 6

Submillimeter-Wave Six Port Reflectometer Integrated onto Micromachined On-Wafer Probes

This chapter presents work of an implementation of integrating GaAs Schottky diodes onto a micromachined on-wafer probe for S-parameters measurements. A sampled-line type six port reflectometer is designed and integrated onto the micromachined on-wafer probe to provide a compact, cost-effective approach for submillimeter wave and terahertz device and circuit S-parameter measurement. The circuit design simulations, calibration simulations, fabrication and measurement plans for a one-port measurement system are discussed. Current approaches of characterizing a DUT within a shielded enclosure such as a vacuum chamber or cryostat requires a feed-through to interface the DUT with the instruments placed outside the chamber. These feed-throughs contribute to system complexity and cost, increase loss and reduce dynamic range. By integrating a six port reflectometer onto a micromachined on-wafer probe, it is possible to implement a low profile network analyzer where the on-wafer DUT, probe, and network analyzer are all enclosed in a dewar, eliminating the need for hermetically-sealed or thermally-isolated feedthroughs.

6.1 Introduction

The terahertz frequency range has been a subject of growing interest for years. Measurement instruments capable of characterizing the performance of systems operating at these high frequencies are crucial for design and assessment. Scattering parameters (S-Parameters) are key figures of merit for such characterization. Current commercial vector network analyzers (VNA), based on four-port architecture can measure S-parameters with a dynamic range larger than 120 dB (Agilent PNA-X (N5245A)), but are expensive. Current approach to terahertz VNA measurement is based on up- and down- converters (frequency extenders) interfaced to a backend VNA. The frequency extenders are bulky, making them unsuitable for measurements in enclosed chambers such as cryogenic dewars.

Six port reflectometers can overcome these shortcomings at a comparable accuracy [115, 116] and much research effort has been devoted to this area [117–120]. The sampled line approach is one of the simplest implementations [121] and has been researched at University of Virginia [122–124] and other institutions. The six-port reflectometer requires no broad band coupler and relies on minimizing loading of the sampling power detectors to the main transmission medium. Amplitude data of coupled power is gathered directly at the frequency of interest via power detectors without any complex heterodyne receivers, greatly reducing the system's complexity. Hence this approach is a promising candidate for terahertz S-parameters measurement compared to current commercial VNA systems.

The quasi-vertical Schottky diode process and micromachining technologies recently developed at the University of Virginia [8,28,29,93] opens a pathway to realize on-wafer probes amenable for integration with sensors for in-situ on-wafer measurements of S-parameters, power, temperature, strain and other physical parameters. A micromachined terahertz on-wafer probe using integrated film resistor strain sensor has been reported [10]. The first integrated GaAs Schottky diode sensors integrated onto micromachined on-wafer probe was describe in Chapter 5. This chapter presents an implementation of integration of GaAs Schottky diode sensors onto a micromachined on-wafer probes as a six port reflectometer. The basic theory of the six port reflectometer will be reviewed in the following section. Afterward the chapter will focus on the sampled line reflectometer structure and its application to

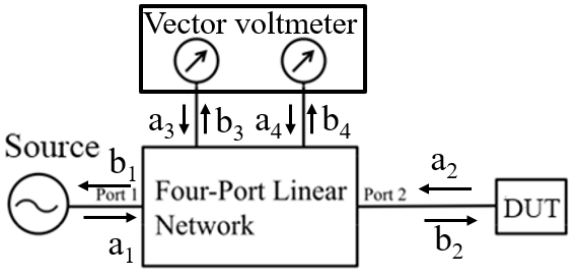


Figure 6.1: Basic structure of a four-port reflectometer.

WR-1.5 on-wafer probing.

6.2 Six-Port Reflectometer Theory

6.2.1 Four and Six-port Reflectometers

Reflection coefficient is defined as the ratio of reflected wave amplitude incident voltage wave to the incident wave amplitude. This parameter is one of the most important figure of merits for characterizing a microwave device or circuit. Reflection coefficient can be measured by commercial vector network analyzers, which are typically based on the four-port reflectometer, which includes vector voltmeter and pair of directional couplers (Figure 6.1).

The reflection coefficient of the DUT, $\Gamma = a_2/b_2$ in Figure 6.1, can be obtained through calibration of the four-port reflectometer, which is essentially a process for finding a_2/b_2 from the measured wave amplitudes at the measurement ports of the vector voltmeter, b_3 and b_4. Assuming that the vector voltmeter is perfectly matched to the directional coupler in the four-port network, then $a_3 = a_4 = 0$. The outputs to the vector voltmeter can be expressed as a linear superposition of the input and output at the DUT port.

$$b_3 = A'a_2 + B'b_2 \tag{6.1}$$

$$b_4 = C'a_2 + D'b_2 \tag{6.2}$$

where A', B', C' and D' are intrinsic parameters of the four port network.

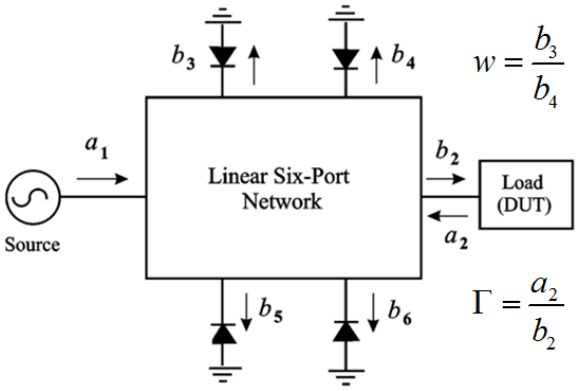


Figure 6.2: Basic structure of a six-port reflectometer.

Deviding (6.1) by (6.2) will yield

$$\frac{b_3}{b_4} = w = \frac{A'\Gamma + B'}{C'\Gamma + D} = \frac{A\Gamma + B}{C\Gamma + 1} \tag{6.3}$$

where $A = A'/D$, $B = B'/D$ and $C = C'/D$. (6.3) is the well-known error model for one port network calibration. Typically three calibration loads (open, short and match) are used to determine A'', B'' and C''. More than three calibrations loads can be used to solve the over-determined equations (6.12) to improve estimation of the calibration coefficients. For submillimeter-wave and terahertz on wafer measurements, implementing a matched load is challenging. Consequently, a set of offset short circuits are common to serve as calibration standards. After the four-port reflectometer is calibrated, the reflection coefficient of the DUT can be obtained from w.

6.2.2 General Six-port Measurements

Another type of network analyzer is based on six-port reflectometer. Figure 6.2 shows the basic diagram of a six-port reflectometer.

There are many different methods of calibrating a six-port refletometer [54, 117–120, 124, 125]. One of the more intuitive approaches to calibration is the "six-port-to-four-port-reduction" method developed by Engen [54]. There are two calibrations steps for a six-port reflectometer to obtain the Γ ($\Gamma = a_2/b_2$) of the device under test (DUT). The first step is a reduction from the six port to an equivalent four port reflectometer ($P \rightarrow w$), i.e. obtaining

the $w = b_3/b_4$ from the measured power coupled to ports 3, 4, 5, and 6. The next step is the conventional four port calibration ($w \rightarrow \Gamma$), to obtain Γ from w. The second step is identical to that for a four-port reflectometer, which was described earlier.

Reduction From Six Port to Four Port

Assuming that the six port network is linear [115], any two output wave amplitudes can be expressed as a linear superposition of two other wave amplitudes.

$$b_5 = \quad Kb_3 + Lb_4 \tag{6.4}$$

$$b_6 = \quad Mb_3 + Nb_4 \tag{6.5}$$

where K, L, M and N are intrinsic parameters of the network.

These expressions (6.5) can be rewritten to describe three circles in the w-plane whose common intersection determines w (Figure 6.3),

$$|w|^2 = \quad \frac{P_3}{P_4} \tag{6.6}$$

$$|w - w_1|^2 = \quad \zeta\frac{P_5}{P_4} \tag{6.7}$$

$$|w - w_2|^2 = \quad \rho\frac{P_6}{P_4} \tag{6.8}$$

where $w = b_3/b_4$, $w_1 = -L/K$, $w_2 = -N/M$, $\zeta = 1/|K|^2$ and $\rho = 1/|M|^2$. w_1, ζ, ρ and complex number w_2 ($\Re(w_2)+i*\Im(w_2)$) are unknowns that can be determined through calibration. These parameters are intrinsic to a given six port network.

If we expand (6.7) and (6.8) and eliminate $|\omega|^2$ from (6.6), we obtain the equation for an elliptic paraboloid.

$$\begin{aligned} &A(\frac{P_3}{P_4})^2 + B(\frac{P_5}{P_4})^2 + C(\frac{P_6}{P_4})^2 + 2D(\frac{P_3}{P_4}\frac{P_5}{P_4}) + 2E(\frac{P_3}{P_4}\frac{P_6}{P_4}) \\ &+ 2F(\frac{P_5}{P_4}\frac{P_6}{P_4}) + 2G(\frac{P_3}{P_4}) + 2H(\frac{P_5}{P_4}) + 2I(\frac{P_6}{P_4}) + J = 0 \end{aligned} \tag{6.9}$$

The coefficients $A, B, \cdots, J$ are related to the six port parameters and can be obtained by fitting a paraboloid in the P_3/P_4-P_5/P_4-P_6/P_4 space. These can be obtained by observing

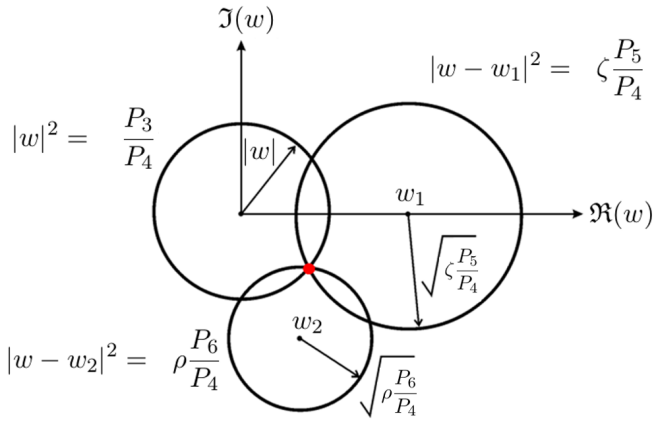


Figure 6.3: The complex value of w is determined by the intersection of these three circles.

the powers in response to sliding short tests where a set of measurements are taken for different sliding short positions. From these, w is obtained by,

$$\Re(w) = \frac{\frac{P_3}{P_4} - \zeta\frac{P_5}{P_4} + |w_1|^2}{2|w_1|} \tag{6.10}$$

$$\Im(w) = \frac{\frac{P_3}{P_4} - \rho\frac{P_6}{P_4} + |w_2|^2 - 2\Re(w)\Re(w_2)}{2\Im(w_2)} \tag{6.11}$$

The general six port reflectometer calibration approach has a sign ambiguity issues which is inherent with power detection because only magnitude information is extracted. We need to check each combination of related terms to choose the correct physical solution. The sampled line type six port reflectometer has no such issue and will be discussed later.

Four Port Calibration

Assuming that the reduced six-port (to an equivalent four port) network is linear, we can obtain Γ from w using the well-known billinear relation:

$$\frac{b_3}{b_4} = w = \frac{A'\Gamma + B'}{C'\Gamma + D} = \frac{A''\Gamma + B''}{C''\Gamma + 1} \tag{6.12}$$

where $A'' = A'/D$, $B'' = B'/D$, $C'' = C'/D$.

At this point, calibration of the network is reduced to the standard four port reflectometer.

6.2.3 Six-port Architectures

Different architectures can be used to realize a six port reflectometer. Engen [16] proposed an architecture based on hybrid couplers to obtain optimal q_i distributions, 120° phase difference from each other, where $q_3 = -B/A$, $q_4 = -F/E$ and $q_5 = -H/G$, and A, B, E, F, G and H come from the following equations describing the six port network:

$$b_3 = Aa_2 + Bb_2 \tag{6.13}$$

$$b_5 = Ea_2 + Fb_2 \tag{6.14}$$

$$b_6 = Ga_2 + Hb_2 \tag{6.15}$$

The circuit layout of Engen's proposed six port reflectometer is shown in Figure 6.4, where the Q and H stand for quadrature hybrid and 180° hybrid, respectively.

Williams [121] proposed another type of six port reflectometer, the sampled line type. The architecture of a sampled line type six port reflectometer is shown in Figure 6.6. In this configuration, power detectors sample the power at discrete points along the transmission line. The sampled line type reflectometer has much simpler structure compared to Engen's design, and the layout is also compatible with transmission lines on micromachined on-wafer probes. Consequently, the sampled line type reflectometer is adopted to be implemented with an integrated six port reflectometer onto micromachined on-wafer probes investigated in this work. The calibration of the sampled line six port reflectometer will be detailed in the following section.

6.2.4 Sampled Line Architecture

If we map $\Gamma = a_2/b_2$ (a circle) in Γ plane to w plane via a bilinear transformation to obtain another circle [54]:

$$|w - R_c|^2 = R^2, \tag{6.16}$$

and substitute R_c and R^2 for w_2 and $\rho P_6/P_4$ respectively, then we obtain an ellipse:

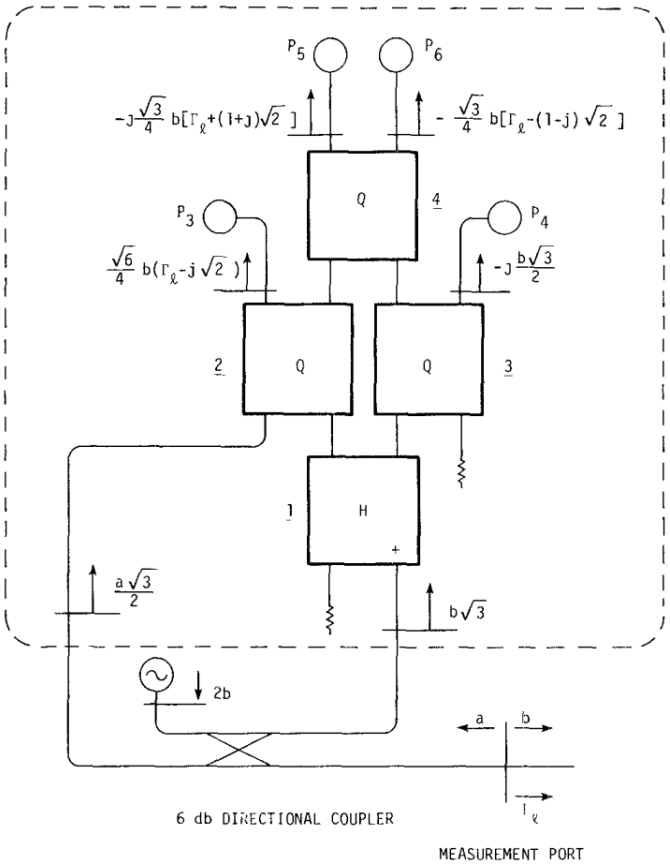
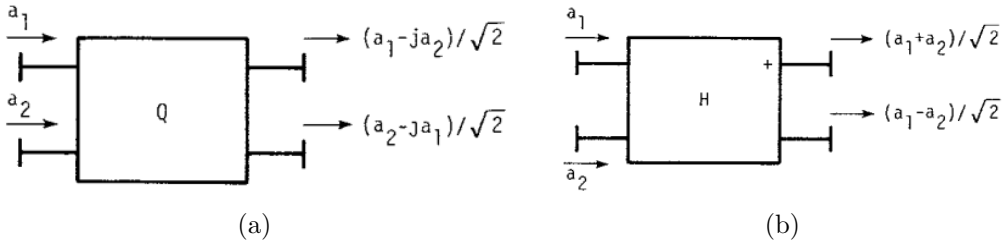


Figure 6.4: Engen's six port architecture based on hybrid couplers [16].

$$A'''(\frac{P_3}{P_4})^2 + 2B'''\frac{P_3P_5}{P_4^2} + C'''(\frac{P_5}{P_4})^2 + 2D'''(\frac{P_3}{P_4}) + 2E'''(\frac{P_5}{P_4}) + F''' = 0 \tag{6.17}$$

The sampled line reflectometer has a very important property that $|\Gamma| > 1$ maps to the upper half of the w plane ($\Im(w) > 0$) and $|\Gamma| < 1$ maps to the lower half of w plane ($\Im(w) < 0$) which is the case of passive DUT (Figure 6.7). That means only five measurements are required to fully determine the all the terms in (6.6-6.8) [126] [127].



(a) (b)

Figure 6.5: The basis modules in Figure 6.4 [16]. (a) Quadruture hybrid. (b) 180 ° hybrid.

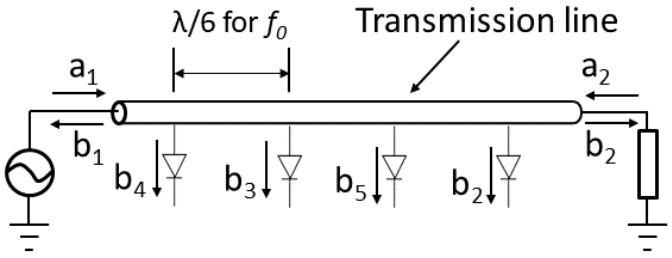


Figure 6.6: Six port circuit sampled line structure.

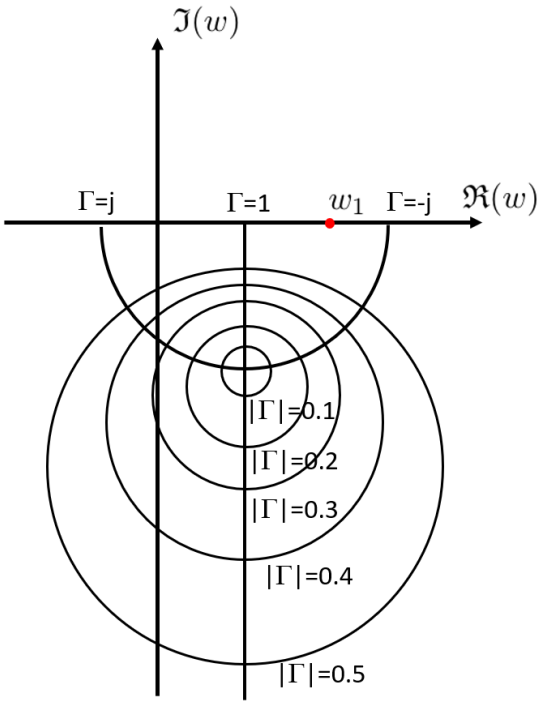


Figure 6.7: Mapping from the Γ plane to the w plane.

Sliding short measurements can be applied to obtain the fitted ellipse curve in the P_3/P_4-P_5/P_4 plane and also the fitted coefficients. For a passive load, i.e. $\Im(w) < 0$,

$$\Re(w) = \frac{\frac{P_3}{P_4} - \zeta\frac{P_5}{P_4} + |w_1|^2}{2|w_1|} \tag{6.18}$$

$$\Im(w) = -\sqrt{w^2 - \Re(w)^2} \tag{6.19}$$

With the complex number w calculated, the usual four port calibration can be applied to get the reflection coefficient Γ. For square law detection, the detected power is proportional

to the detected output voltage. Consequently, the ratio P_i/P_j equals to V_i/V_j (for voltage detection) or I_i/I_j (for current detection), where P is the input power to the detectors, V is the output voltage and I is the output current. The square law detection allows a straightforward measurement of power. Schottky diodes can be used as square law detection and are compatible with heterogeneous integration process onto micromachined on-wafer probes. The background and figures-of-merit of diode detectors will be described in the following section.

6.3 Schottky Diode Detectors

6.3.1 Responsivity and NEP

The responsivity $\mathcal{R}$ is one of the most important figures-of-merit of a detector. The responsivity is defined as the ratio of the output detected voltage (or current) to the input RF power. Hence the current responsivity and voltage responsivity are given by

$$\mathcal{R}_i = \frac{\Delta_i}{P_{RF}} \tag{6.20}$$

$$\mathcal{R}_v = \frac{|\Delta_v|}{P_{RF}} \tag{6.21}$$

Thus, the responsivity is a measure of the sensitivity of the detector. A typical value for intrinsic $\mathfrak{R}_\mathfrak{i}$ of an ideal diode ($\eta = 1$) at room temperature is 20 A/W.

The NEP quantifies the noise power generated by the detector and determines the smallest power that is detectable. The NEP is the input power level that results in a signal-to-noise ratio of unity at the detector output. Consequently, NEP can be found as:

$$\text{NEP} = \frac{i_n}{\mathcal{R}_i} = \frac{v_n}{\mathcal{R}_v} \tag{6.22}$$

Assuming that shot noise is the dominant noise for the detector diode, the rms noise current in a 1 Hz bandwidth can be expressed as

$$i_n = \sqrt{2qI_0} \tag{6.23}$$

Then the NEP becomes

$$\text{NEP} = \frac{i_n}{\mathcal{R}_i} = \sqrt{2qI_0}(\frac{2\eta kT}{q})\, W/\sqrt{Hz} \tag{6.24}$$

It can be found from (6.24) that the typical value of NEP for a diode at room temperature is on the order of 10^{-12} W/$\sqrt{\text{Hz}}$. Smaller NEP yields a lower minimum detectable power for the reflectometer.

6.3.2 Linearity and Dynamic Range

Figure 6.8 shows a typical Δv versus P_{RF} characteristic of a detector diode, where the output voltage can be considered as the voltage drop across a resistor in series with the diode. In the square-law region, the output voltage or current is proportional to the input RF power. As the input RF power increases, the residual terms of the Taylor series expansion of the detected current become more significant. Eventually the input RF power will reaches to a point that the output voltage (or current) can not be viewed as proportional to the input RF power any more, i.e. the output voltage (or current) is not linear with the input RF power. This compression point limits the upper limit of the square-law region. Meanwhile,

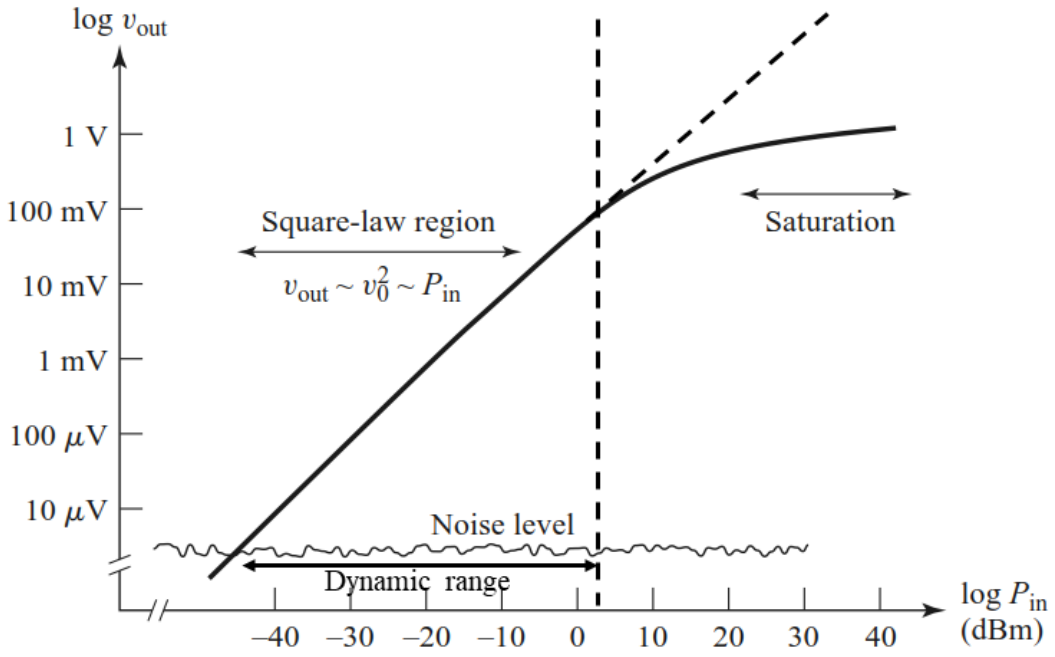


Figure 6.8: IV characteristic of a detector diode.

the minimum detectable input RF power is limited by the NEP of the diode, which sets the lower limit of the square-law region. The range of the square-law region is the dynamic range of the detector diode, which is typically about 50 dB [128]. The derivations of square-law operation will be detailed in the following section.

6.3.3 Square Law Detectors

Figure 6.9 shows an IV characteristic of a detector diode. An RF voltage applied to a biased diode generates a DC response as well as higher harmonics, resulting in an offset current Δi [129].

We can analyze a diode detector mathematically by expanding its I-V characteristic in a Taylor series about the bias voltage V_0,

$$i(V) = i(V_0) + \frac{di}{dV}\Big|_{V_0} + \frac{1}{2}\frac{d^2i}{dV^2}\Big|_{V_0}(V - V_0)^2 \tag{6.25}$$

where the applied voltage is assumed sufficiently small that higher order terms larger than two are omitted. Taking the total voltage across the diode to be the superposition of DC

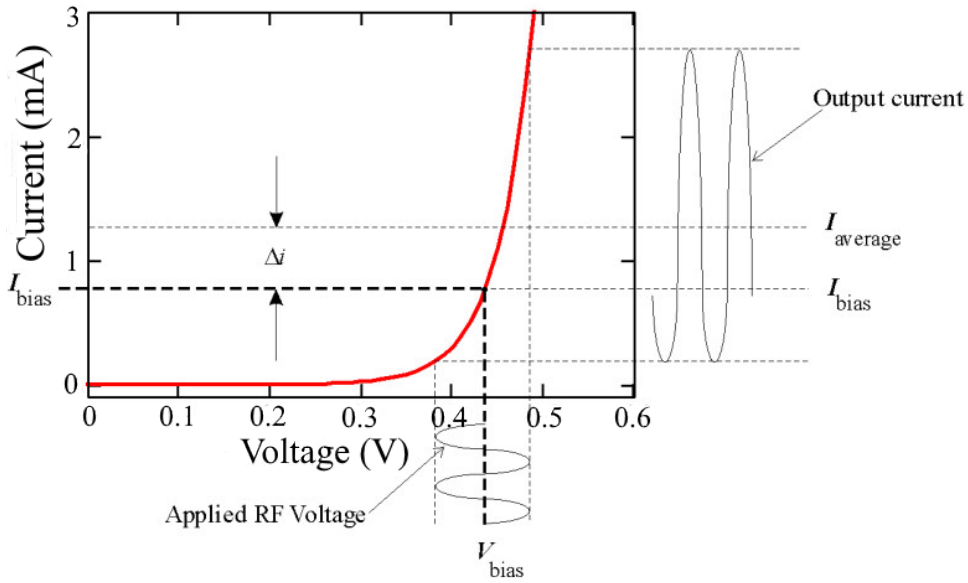


Figure 6.9: An RF voltage applied to a biased diode generates a DC response as well as higher harmonics, resulting in an offset current ΔI.

bias voltage and small signal RF voltage

$$V(t) = V_0 + v_{RF}\cos\omega t \tag{6.26}$$

the current through the diode can be found to be,

$$i(t) = I_0 + \frac{1}{4}\frac{d^2i}{dV^2}\Big|_{V_0} v_{RF}^2 + \frac{di}{dV}\Big|_{V_0} v_{RF}\cos\omega t + \frac{1}{4}\frac{d^2i}{dV^2}\Big|_{V_0} v_{RF}^2\cos 2\omega t \tag{6.27}$$

Taking the time-average of the current (or passing it through a low pass filter), we find the detected (offset) current to be,

$$i = < i(t) > - I_0 = \frac{1}{4}\frac{d^2i}{dV^2}\Big|_{V_0} v_{RF}^2 \tag{6.28}$$

We can find this detected current by recalling the I-V characteristic of a diode,

$$i(V) = I_s[\exp(\frac{qV}{\eta kT}) - 1] \tag{6.29}$$

where I_s is the reverse saturation current, q is the fundamental unit of charge, k is Boltzmann's constant, T is absolute temperature, and η is the diode ideality factor. Taking the second derivative of (2) gives us

$$\frac{d^2i}{dV^2}\Big|_{V_0} = (\frac{q}{\eta kT})^2\exp(\frac{qV_0}{\eta kT}) \approx (\frac{q}{\eta kT})^2 I_0 \tag{6.30}$$

for forward bias. Substitution into equation (1) yields,

$$\Delta i = \frac{1}{4} I_0 (\frac{q v_{RF}}{\eta kT})^2 \tag{6.31}$$

Expression (3) shows us that the detected current, Δi, is proportional to the RF voltage amplitude. As a result, the detector output is proportional to the RF power. Detectors that have this property are known as "square law detectors."

6.4 Integrated Six Port Reflectometer On-Wafer Probe

6.4.1 Circuit Layout

The system block diagram of the proposed WR-1.5 (500—750 GHz) six port reflectometer heterogeneously integrated on micromachined on-wafer probe is depicted in Figure 6.10. The six port reflectometer shown in the dashed square is to be integrated onto the original probe along the primary transmission line, connecting the probe tips to the backend waveguide transition. The standing wave due to the reflection of the DUT on a wafer contacted by the probe, is sampled by four detectors along the primary transmission line. The rectified DC current through Schottky diodes are measured through the low pass filters (LPFs). The complex value of the reflection coefficient at the reference plane on wafer is extracted by calibration of the six port reflectometer. It was found that three diodes uniformly spaced along the line with one-sixth of a wavelength provides good accuracy over an octave of frequency [121]. Therefore the diodes in the integrated six port reflectometer are spaced with one-sixth of a wavelength too. The layout of the full chip of integrated six port reflectometer and the zoom in view of the tip area are shown in Figure 6.11a and 6.11b respectively. Both the electromagnetic simulations and six port reflectometer calibration simulations are

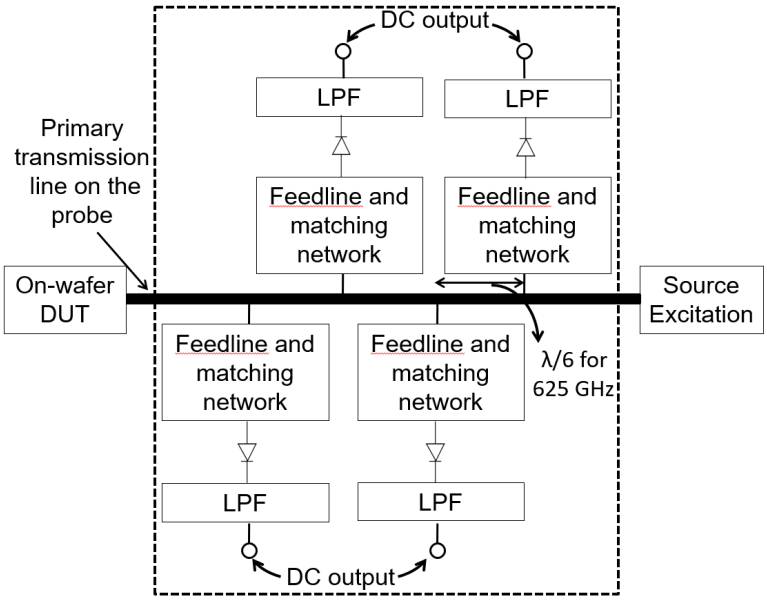


Figure 6.10: Simplified block diagram of the six port reflectometer integrated onto the on-wafer probe.

performed to check the circuit design.

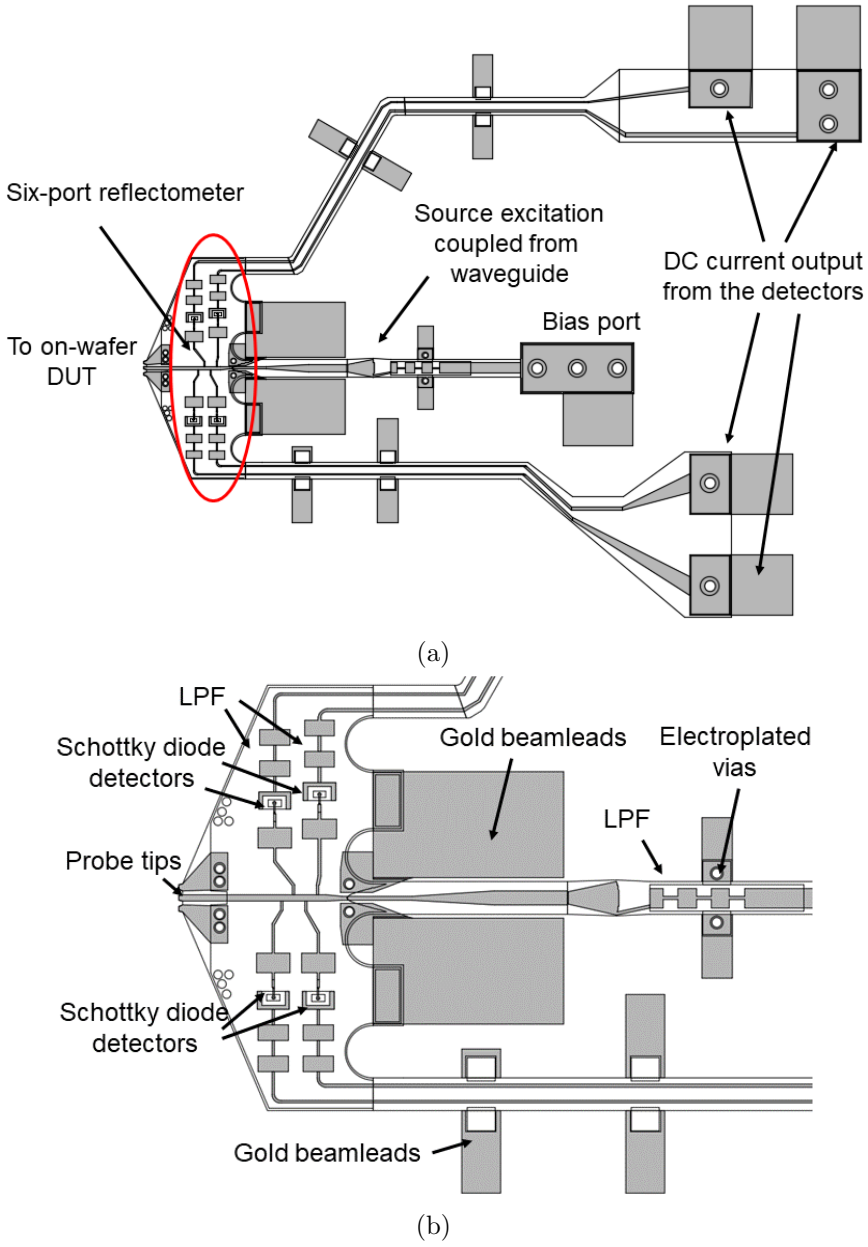


Figure 6.11: Circuit layout of the proposed six port reflectometer integrated onto the on-wafer probe. (a) Full chip. (b) Zoom in view of the probe tip area.

6.4.2 Circuit Design Simulations

Due to the inherently nonlinear property of the detector diodes, combination of two commercial softwares, Ansys's *High Frequency Structure Simulator* (HFSS) and Keysight's *Advanced*

Design System (ADS) are used to simulate the electromagnetic response of the six port reflectometer integrated on an on-wafer probe.

Low insertion loss and high reflection loss are still required to maintain the original probe's RF performance for S-parameters measurement. The key for the sampled line reflectometer to work properly is to make sure the sampling detector circuits present a low loading effect (close to RF open) to transmission line to be sampled [121].

There's a trade off between high coupling to get large enough power to the detector diodes and low coupling to get low loading effect to sustain the original standing wave on the transmission line to be sampled. The power distribution among the diodes should also be as uniform as possible to maximize the dynamic range since the calibration of a six port reflectometer relies on mathematical manipulation of power ratios between each diodes.

The anode size needs to be small enough so that the junction resistance dominates over junction capacitance, namely the diode works as a varistor [130]. 1.2 μm and 1.8 μm anode sizes are chosen as two options considering the limits of equipment available in the microfabrication clean room.

Two common types of power detector schemes are shown in Figure 6.12, depending on how the diode is biased. The current biased type is preferred for integrated six port reflectometer onto micromachined on-wafer probes since it's simpler to realize on the probe structure. The in-situ RF ground of detector diode would be hard to implement for the voltage biased type.

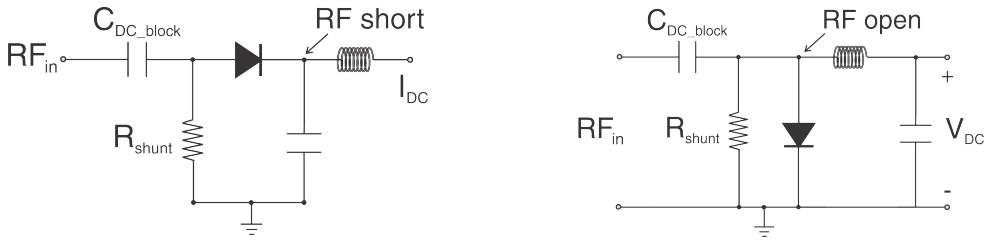
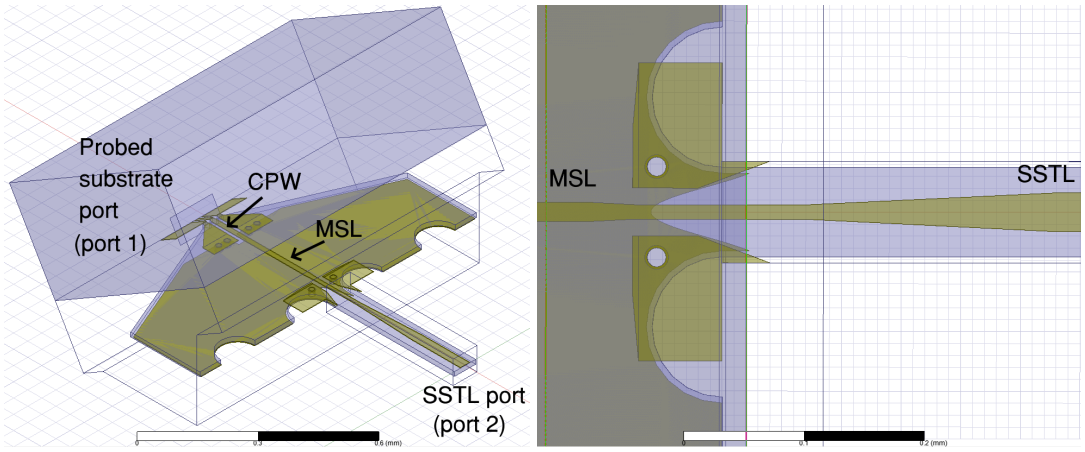


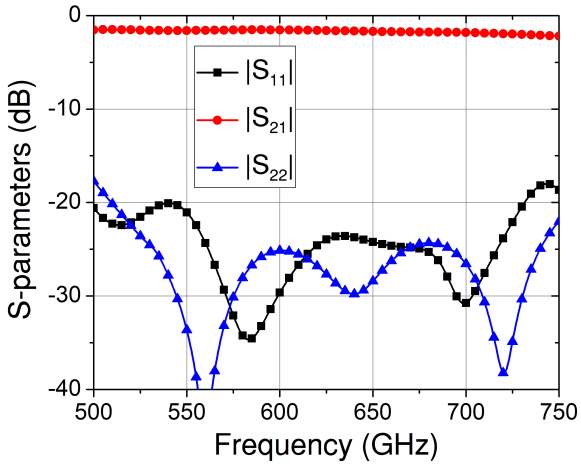
Figure 6.12: Two types of detector circuits. (a) Current detection. (b) Voltage detection.

6.4.3 On-Wafer Probe without Integrated Six Port Reflectometer

There are two types of main transmission lines for the standard micromachined on-wafer probes, based on microstrip line (MSL) and coplanar waveguide (CPW), respectively [114]. For the integrated six port reflectometer onto probes, MSL is preferred to CPW due to relative simplicity to realize the detector circuits in the probe tip area. A cold-via transition of CPW-MSL line is designed with two options based on [131, 132]. The HFSS model and simulation results of two options are shown in Figure 6.13 and 6.14, depending on lithography alignment tolerance. From the simulation results in Figure 6.13c and 6.14c, for both options



(a) (b)



(c)

Figure 6.13: Option 1 of the micromachined on-wafer probe to be integrated with six port reflectometer: tighter lithography alignment tolerance with wider bandwidth. (a) HFSS model of probe tip area. (b) Zoom in view of the MSL to SSTL transition. (c) Simulation results of the S-parameters.

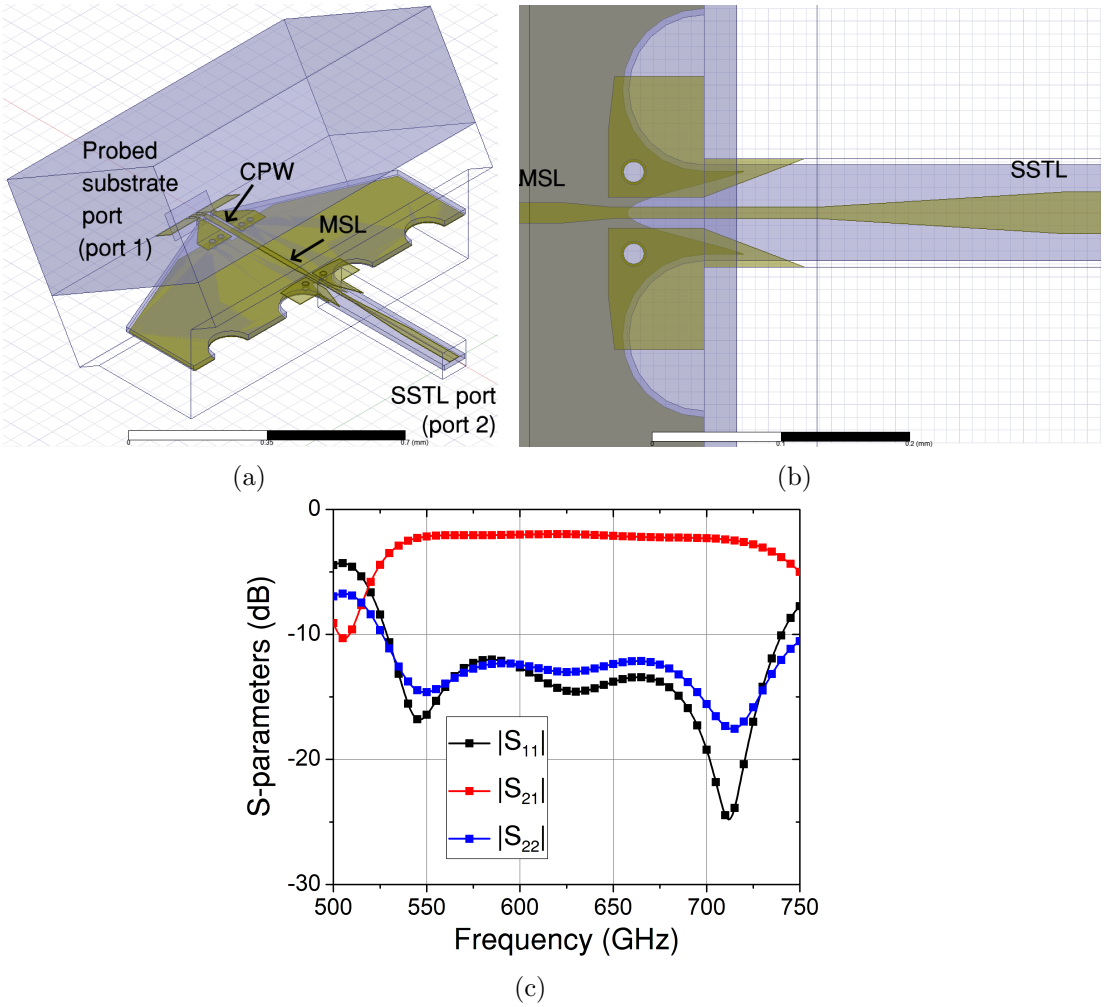
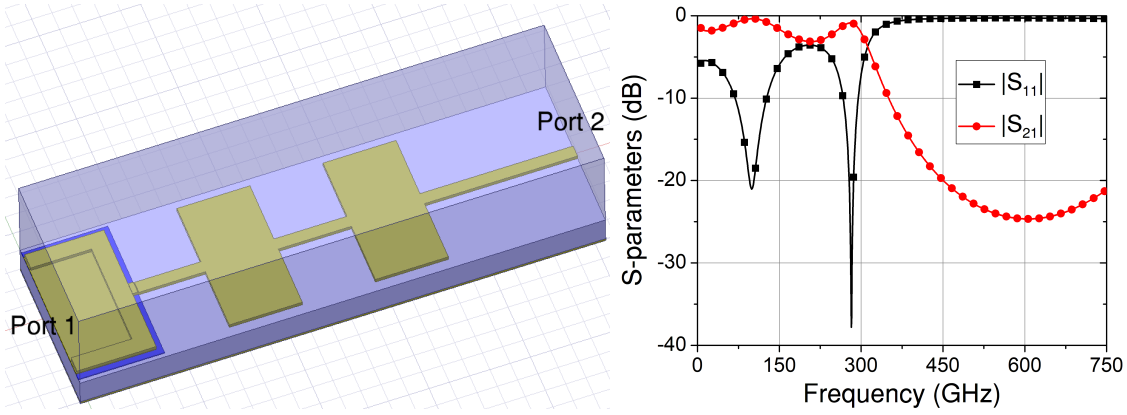


Figure 6.14: Option 2 of the micromachined on-wafer probe to be integrated with six port reflectometer: looser lithography alignment tolerance with narrower bandwidth. (a) HFSS model of probe tip area. (b) Zoom in view of the MSL to SSTL transition. (c) Simulation results of the S-parameters.

of the cold via transition and microstrip line-suspended substrate stripline (MSL-SSTL) transitions, the return loss is larger than 20 dB across the full band and the insertion loss is about 1 dB for option 1 (tighter tolerance of lithographyic alignment). The return loss and insertion loss are about 13 dB and 2 dB respectively for option 2.

6.4.4 Low Pass Filter at the Output

A low pass filter is used to remove unwanted higher frequency component at the detector output. A C-L-C type stepped impedance low pass filter is introduced at the output of the detector to provide an RF short to the diode. The first capacitive component is the ohmic



(a) (b)

Figure 6.15: Low pass filter used in the six port reflectometer probe. (a) HFSS model. (b) Simulation results of the S-parameters.

contact pad of the diode itself. The HFSS model and simulation results are shown in Figure 6.15. The stopband suppression is larger than 20 dB and the insertion loss is less than 1 dB.

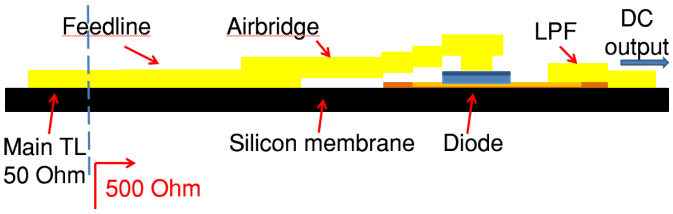
6.4.5 Detector Circuits of the Six Port Reflectomter

In order to minimize the loading effect of the four detector circuits to the primary transmission line, the impedance seen to the direction of the detector circuits from the sampling points should be ideally RF open. The illustration of the reference plane of interest is shown in Figure 6.16a and 6.16b.

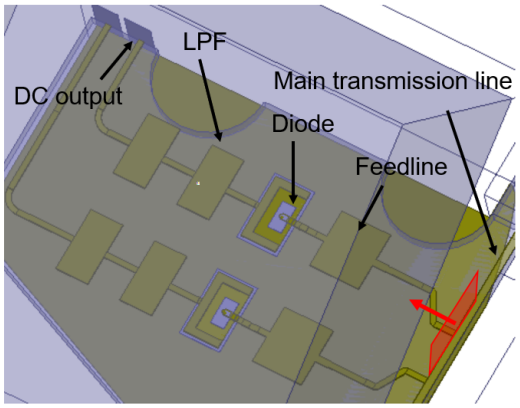
The HFSS model and simulation result of the reflection seen from one of the sampling points on the transmission line to the corresponding detector branch are shown in Figure 6.17a and 6.17b. The magnitude of the reflection coefficient is about 0.9 across a wide bandwidth of 550-705 GHz. A wide bandwidth of 550-705 GHz is achieved.

6.4.6 Six Port Reflectometer Integrated with On-Wafer Probes

Based on the designs of each circuit components in previous subsections, the HFSS model of the full circuit is built and simulated. The model is split in half as in Figure 6.18 for better demonstration. The exciting RF source is fed in from the waveguide port, coupled to the planar circuit on the probe chip and all the way down to the on-wafer DUT through the

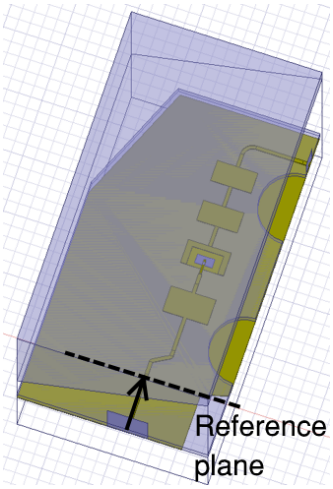


(a)

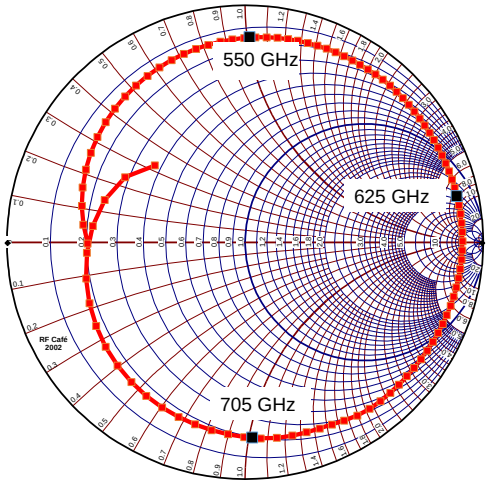


(b)

Figure 6.16: (a) Cross section view of reference plane of embedded impedance of detector circuit to the original main transmission line. (b) Reference plane of two detector circuits on the same side of the main transmission line.



(a)



(b)

Figure 6.17: (a) Single branch of the six port reflectometer of the full circuit model in HFSS. (b) Simulation results of the reflection seen from the sampling point of the single branch to the main transmission line.

probe tip contact pads. The DC output ports serve as both DC output and biasing of the diodes together with the bias port.

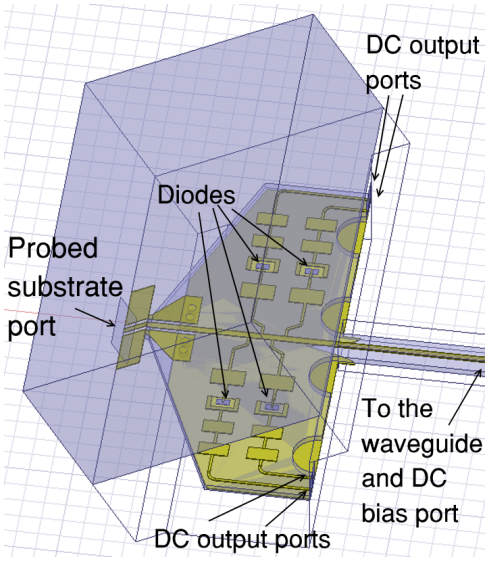
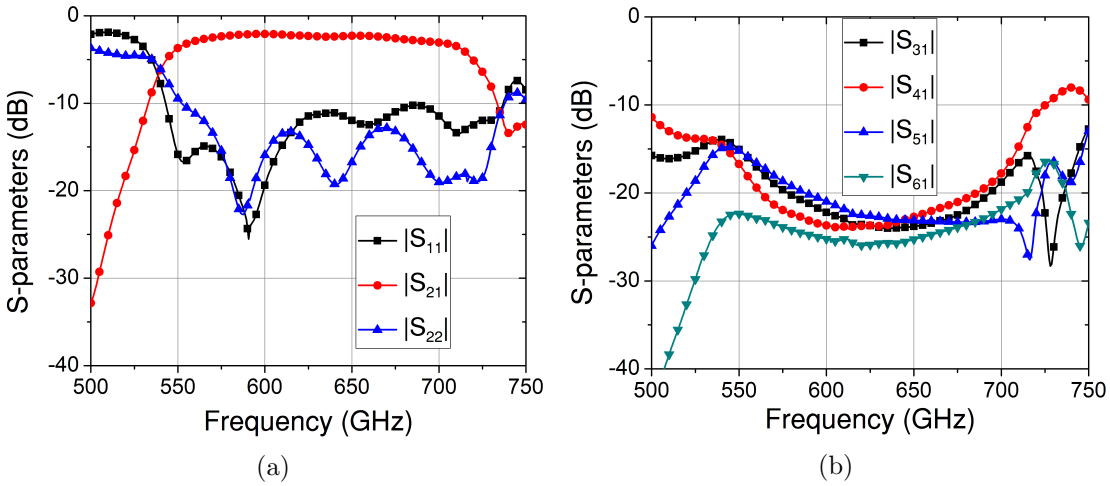


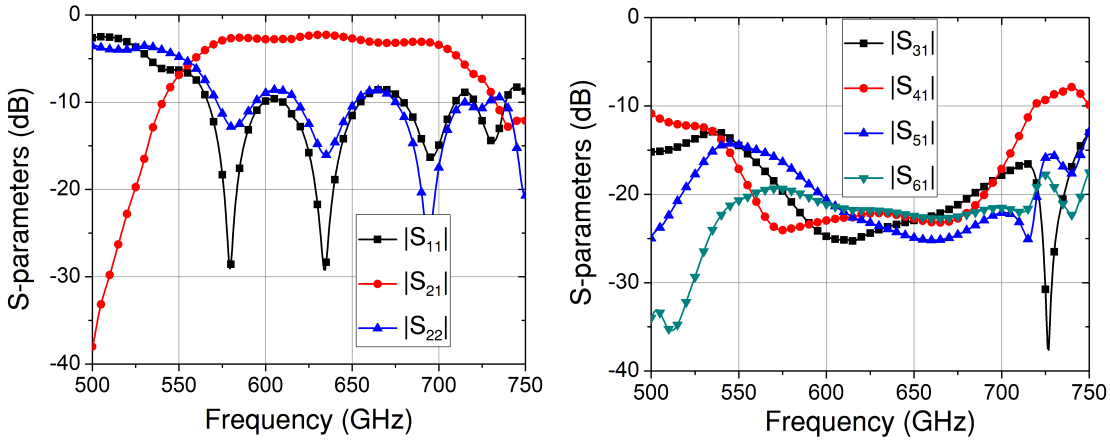
Figure 6.18: Probe tip area part of the full circuit model in HFSS.



(a) (b)

Figure 6.19: Simulation results of option 1 of the full model: (a) ADS simulation results of return loss and insertion loss of the full model with integrated six port reflectometers and (b) ADS simulation results of coupling to the diodes of the full model with integrated six port reflectometers for layout option 1. Port 1 and 2 are SSTL port and CPW port respectively. Port 3-6 are diode ports.

Figure 6.19 and 6.20 show the simulated insertion loss, reflection loss and coupling coefficient from the waveguide to each diode. From the simulation, the reflection is less than -10 dB and the insertion loss is about 2 dB from 560 to 710 GHz. The frequency band where the full circuit has low loss and the power coupling to each diodes is uniformly distributed overlaps with each other (560-710 GHz). This agrees well with that of the loading effect simulation for single detector branch in Figure 6.17, meaning that the detectors do have



(a) (b)

Figure 6.20: Simulation results of option 2 of the full model: (a) ADS simulation results of return loss and insertion loss of the full model with integrated six port reflectometers and (b) ADS simulation results of coupling to the diodes of the full model with integrated six port reflectometers for layout option 2. Port 1 and 2 are SSTL port and CPW port respectively. Port 3-6 are diode ports.

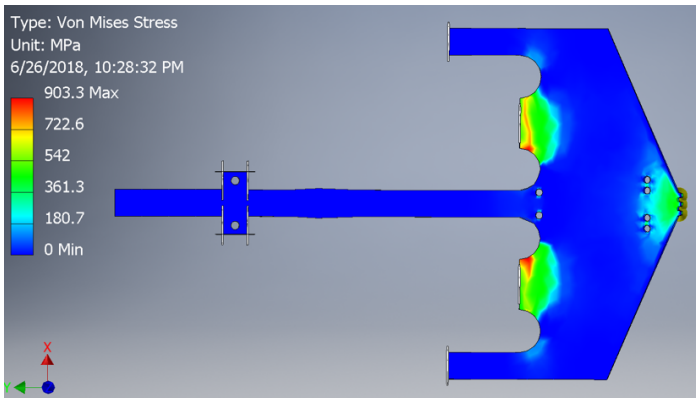
little loading effect at these frequencies to the primary transmission line.

6.4.7 Mechanical Simulation

The finite element model of the probe chip is simulated using the Autodesk Inventor Mechanical software package to estimate the stress induced in the probe chip with each tip subject to a 10 mN load, corresponding to the typical contact force required for a low-resistance electrical interface [29]. The result of this simulation is shown in Figure 6.21. To minimize the impact of induced strain on the diode electrical characteristics and mechanical integrity [112], the integrated diode temperature sensor is placed near the probe tip in a region of low induced stress. The largest stress in the silicon (1.1 GPa) occurs in the region where the chip is clamped to its housing. Rounded fillets in these regions are included in the chip design to ensure the stress remains well below the yield strength of silicon (4.5 GPa).

6.4.8 Six Port Reflectometer Calibration Simulations

Sliding terminations calibration algorithm [54, 126] check is performed to see if the "measurement" accuracy is reasonable. Eighteen predefined offset short circuits and eighteen



(a)

Figure 6.21: (a) Simulated displacement of the tips and (b) Simulated strain distribution profile of the power meter integrated onto WR-1.5 micromachined on-wafer probe. Each tip is applied to 10 mN contact force.

offset open circuits are "measured" first to extract the six port circuit parameters, namely reducing the six port to the four port. Following that, three delay shorts are chosen to serve as the calibration standard for the four port calibration. Then the complex reflection coefficient at the reference plane close to the on-wafer DUT can be retrieved. Different preset load is used to generate known reflections at the DUT port and simulated calibration is carried out to get the "measured" reflections.

The simulated accuracy of the calibration at the center frequency of WR-1.5 band of the six port reflectometer is depicted in Figure 6.22. The error in magnitude and phase of the

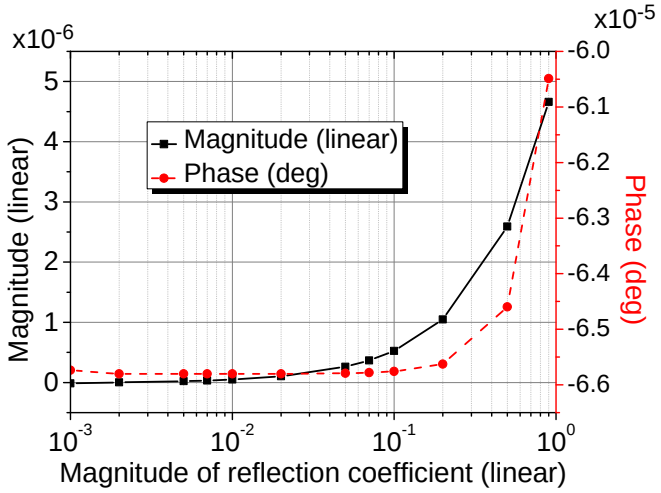


Figure 6.22: Simulated average magnitude and phase measurement errors at 625 GHz.

reflection coefficient are lower than 5×10^{-6} (linear) and 6×10^{-5} (degrees) respectively. Simulation shows that the reflectometer could measure the reflection coefficient with a resolution of 0.01-0.30 dB, depending on $|\Gamma|$.

6.5 Measurement Approach

WR-1.5 frequency extender from VDI Inc. with available power of -25 dBm will be used as the WR-1.5 (500—750 GHz) source. The six port reflectometer is already integrated onto a micromachined on-wafer probe, so there's no need for extra standard on-wafer probes for the measurement. A multimeter or lock-in amplifier will be connected to the output of the six port reflectometer probe to record current readings from each power detector.

6.5.1 Calibration

The six port reflectometer probe will first measure the 18 coplanar offset short circuits and 18 coplanar offset open circuits to perform the calibration for on-wafer measurement. Currents will be measured from each power detectors over the frequency band and for each calibration standard. From Engen's sliding termination method for the six port reflectometer calibration [54], the voltage ratio I_3/I_4 plotted against I_5/I_4 will map out ellipse in the

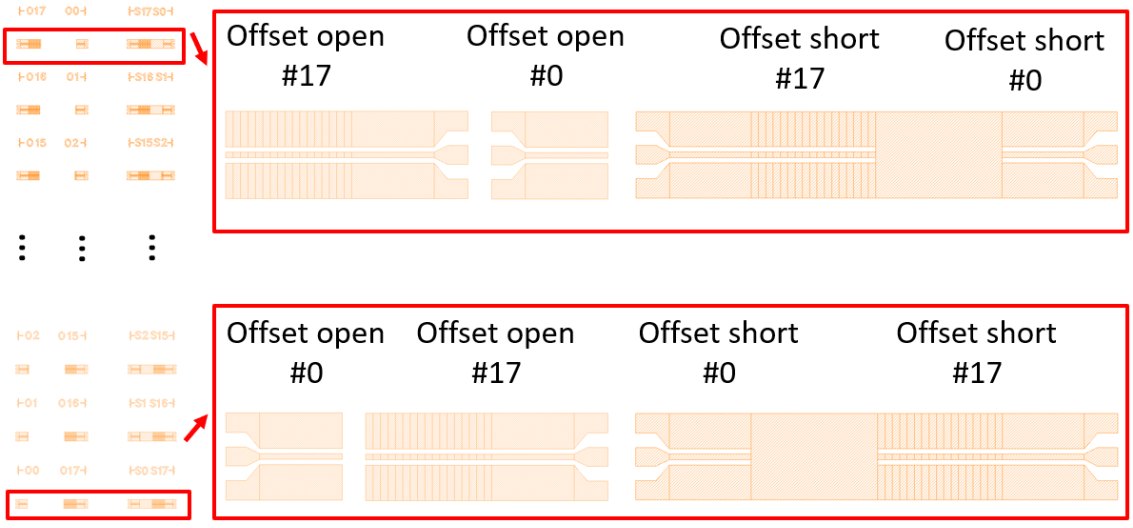


Figure 6.23: Offset coplanar short and open circuits for the six port reflectometer calibration of ellipse fitting.

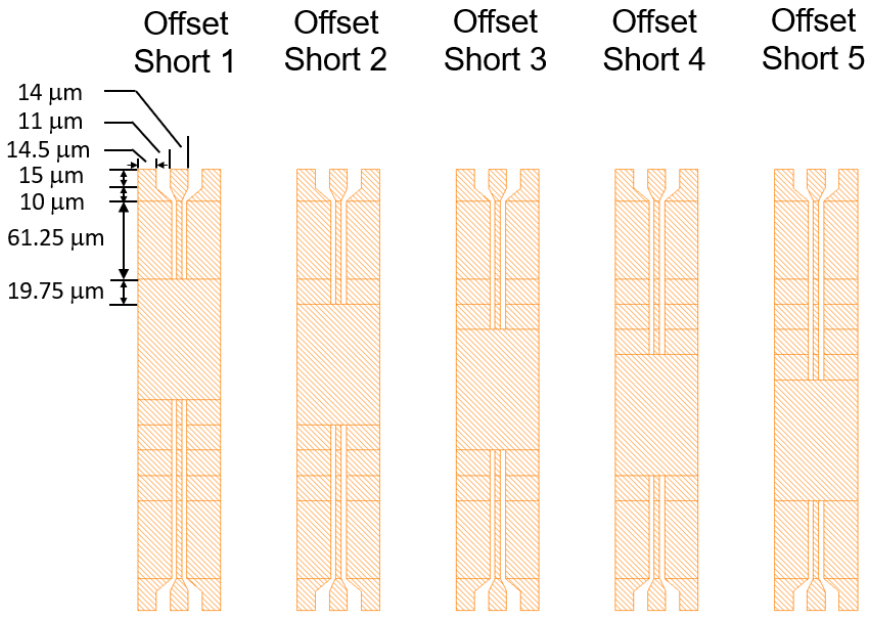


Figure 6.24: Coplanar offset short for the VNA calibration. Another set of calibration standards are incorporated in a back-to-back configuration to save wafer space.

power-plane for each frequency. The fitting of the ellipse will solve for intrinsic parameters of the six port as well as w, which completes the "six-port-to-four-port reduction". A permutation of the offset short circuits and open circuits will be used for the remaining procedure of standard four port calibration to obtain the error networks. Figure 6.23 shows the coplanar offset short-circuits and coplanar open-circuits to be used for the calibration.

6.5.2 Preliminary RF Measurement

After the error networks are obtained, they are applied to several on-wafer DUTs respectively to calculate the corrected scattering parameters from the same raw data of the DUT measured from the VNA. The corrected scattering parameters of different DUTs are compared to that from regular VNA calibration using offset short circuits. The DUTs investigated include the offset short circuits and open circuits used for the calibration of the six port reflectometer (Figure 6.23), offset short circuits VNA calibration standards (Figure 6.24), and mismatched load with open or short termination (Figure 6.25).

(a) (b) (c) (d)

Figure 6.25: Mismatched load DUTs: (a) 65 Ω coplanar open circuit load. (a) 65 Ω coplanar short circuit load. (a) 80 Ω coplanar open circuit load. (d) 80 Ω coplanar short circuit load.

6.5.3 Mechnical Measurements

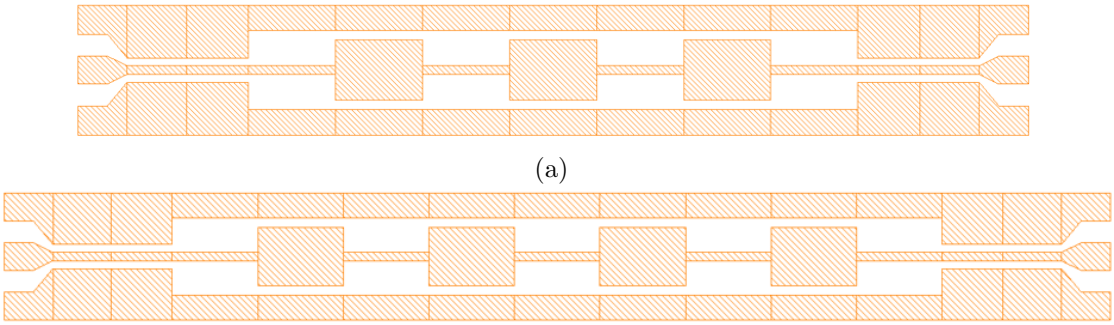
Similar load-cell measurements to the temperature sensor probe in Chapter 5 can be performed to the six port reflectometer probe too. Contact force generated by the probe contact will be measured to evaluate the mechanical properties of integrated six port reflectometer.

6.5.4 Advanced RF Measurement Plans

Some advanced measurement plans include introducing electronic calibration for the six port reflectometer calibration, and performing two port six port reflectometer calibration with and without using electronic calibration.

Based on the work in Chapter 4, integrated Schottky diodes onto silicon can be used as electronic calibration standards for the calibration of six port reflectometer probe. The plan is to replace the 18 offset short circuits and 18 offset open circuits with the diodes standards under different biases.

Previous discussions are focused on one port calibration application. If another six port reflectometer probe chip is assembled and verified through tests, a two port calibration can be setup. Conventional TRL standards will be used to measure the DUTs as a reference to evaluate the performance of the two port calibration of six port reflectometers. Figure 6.26 shows two LPF DUTs designed for the evaluation. Similar to the one port case of six port reflectometer calibration, either the offset shorts/opens or diode electronic calibration standards can be used.



(a)

(b)

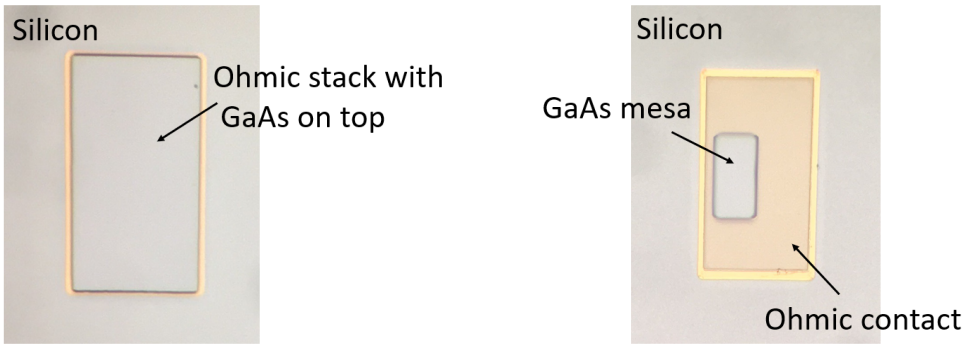
Figure 6.26: Low pass filter DUTs for two port calibration evaluation: (a) Stepped impedance filter of 7th order. (b) Stepped impedance filter of 9th order.

6.6 Fabrication Process

6.6.1 Overview of the Process

The fabrication process of the integrated six port reflectometer on-wafer probe is the same as the temperature sensor probe as described in Chapter 5. The fabrication steps are evaluated to assess potential issues of the actual fabrication run.

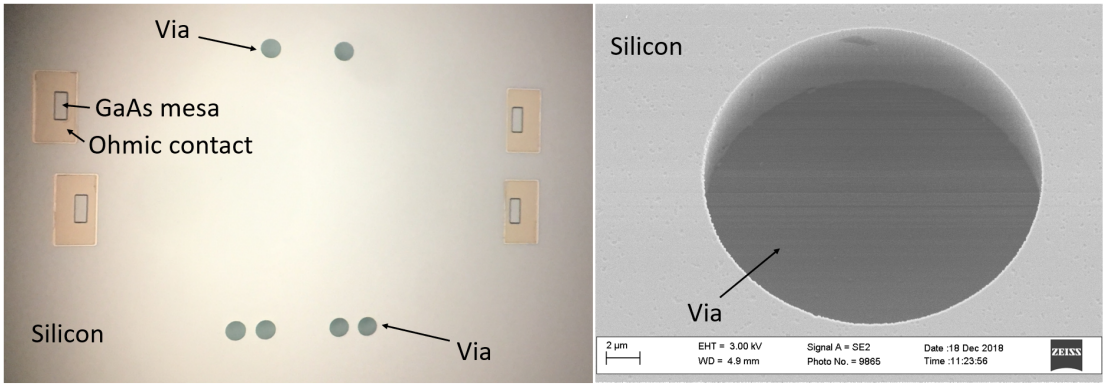
6.6.2 Initial Progress



(a) (b)

Figure 6.27: (a) Ohmic contact stack with unetched GaAs on top. (b) GaAs mesa formed atop ohmic contact stack.

After the GaAs epixtaxy is metalized and bonded to the silicon-on-insulator substrate, the GaAs handle is removed. Lithography and wet etch are performed to form ohmic contact stack and GaAs mesa atop the ohmic stack of the six port reflectometer. The microscope



(a) (b)

Figure 6.28: (a) Vias in the six port reflectometer. (b) SEM pictures of the vias.

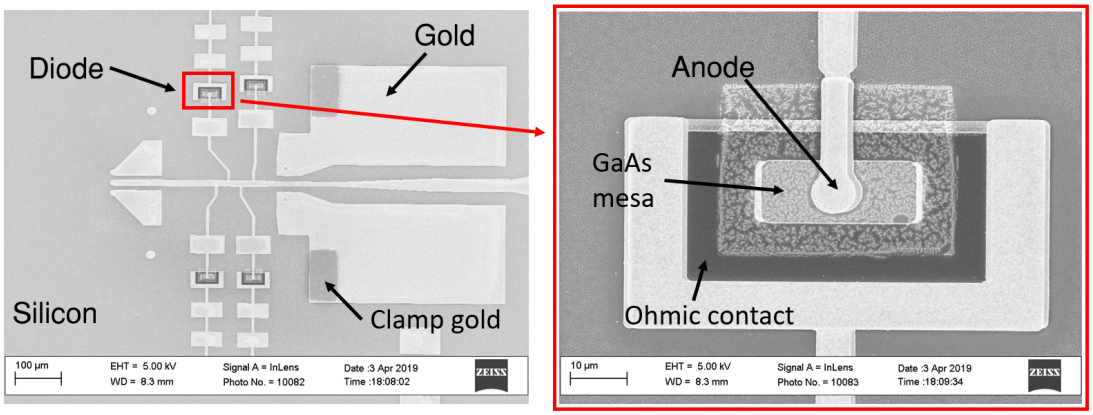


Figure 6.29: SEM of the front side of the six port reflectometer probe before bonding for backisde processing.

images of formed ohmic contact stack and GaAs mesa atop ohmic contact stack are shown in Figure 6.27. Following that is the formation of vias through RIE etch. The microscope image of the six port reflectometer area and zoom in view of SEM image of one of the vias are shown in Figure 6.28.

A test run of a dummy sample for the remaining steps of the six port reflectometer is performed. Figure 6.29 shows the SEM images of the six port reflectometer when all the front side processing is done and the Schottky diodes are formed.

Then the wafer is flipped and temporarily bonded to a silicon carrier wafer for backside processing, including bottom metal patterning and electroplating, and silicon extents etch patterning and RIE etch to define the outline of the silicon membrane chip. Figure 6.30 shows the backside view of one complete six port reflectometer chip prior to the chip release

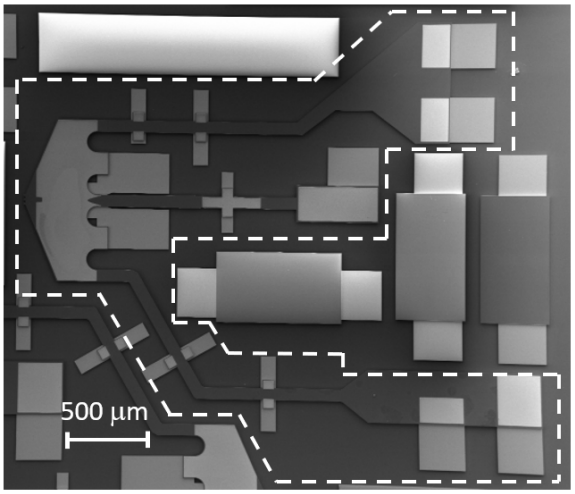


Figure 6.30: The outline of one six port reflectometer probe chip prior to chip release: backside view. The chip is enclosed in the dashed white rectangle.

using waferbond remover. Figure 6.31 shows the SEM images of the backside of the probe tip area right before releasing the chips using waferbond remover. Note that the silicon extents etch is nice and clean, and there's no silicon leftover ("rim") which would act as a source of cracking that will then propagate through the chip on the first contact cycle even at low contact force [2].

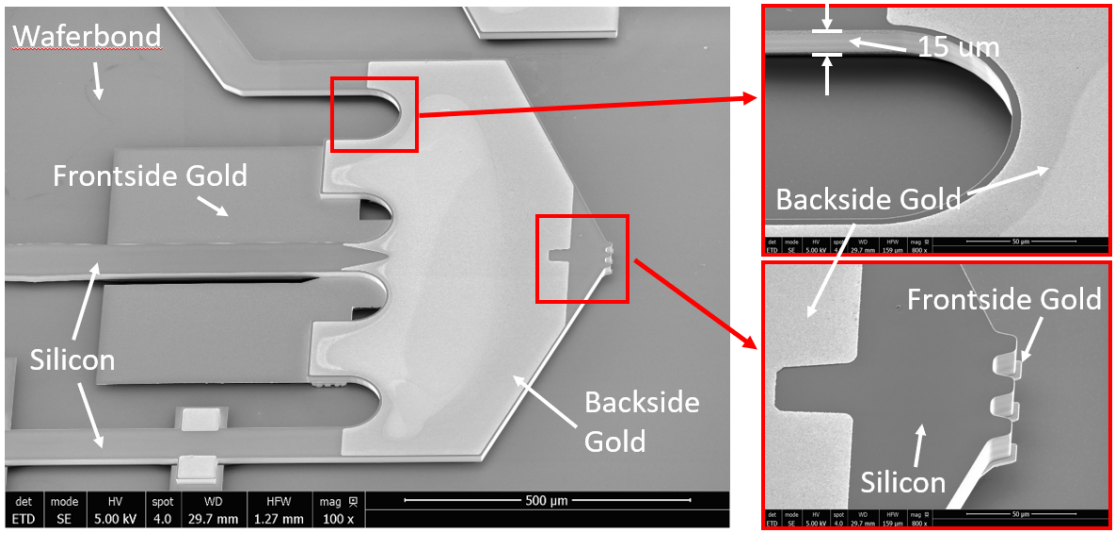


Figure 6.31: SEM of the backside of the six port reflectometer probe chip prior to chip release.

Each step of the six port reflectometer has been evaluated. The device wafer of integrated six port reflectometer is still in process.

6.7 Conclusion

This work has presented the design and fabrication of first six port reflectometer integrated onto micromachined on-wafer probe based on heterogeneous integration of GaAs Schottky diodes onto silicon membrane. The measurement plan is discussed. Future work would be completing the characterization of the six port reflectometer probe and performing the measurements in plan.

Chapter 7

Conclusions and future work

7.1 Conclusions

The focus of this thesis has been to heterogeneous integration of GaAs Schottky diodes onto micromachined on-wafer probes to address the need of compact, low cost and innovative metrology tools for the submillimeter-wave and terahertz community.

First of all, a new fabrication process was developed to simplify and improve the prior process of heterogeneous integration of GaAs Schottky diodes onto silicon, which suffered from low yield issues due to delamination and cracking after the bonding and handle removal of the GaAs epitaxy. The new process eliminated many problematic thermal process steps by replacing the annealed ohmic contact (Ge/Pd/Au/Ti) on n+-GaAs with a non-alloyed ohmic contact on an $n++$ InGaAs cap layer grown epitaxially on top of n+-GaAs. The new process also replaced the high-temperature (200°) wafer bonding using SOG with a new low-temperature (140°) curing wafer bonding using SU-8 as the bonding agent. Both DC characterization and submillimeter-wave on-wafer characterization of diodes fabricated using the new process showed excellent performance. To assess the potential of the new process, a prior art of 160 GHz quadrupler was re-implemented using the new process recipe and obtained comparable performance to the original implementation. Some potential approaches to improve the thermal handling of the quadrupler chip were also investigated.

Secondly, an application of GaAs Schottky diodes integrated onto silicon to electronic calibration for submillimeter-wave and terahertz on-wafer S-parameter measurement was

demonstrated. The standard was based on the voltage-dependent impedance presented by a GaAs Schottky diode integrated on silicon fabricated using the new recipe and allowed full on-wafer calibration without need for moving or repositioning wafer probes onto contact pads. Both one-port and two-port calibration were investigated. Error coefficients derived using the electronic diode standard were compared to those found from a set of conventional coplanar delayed-short circuit standards (for one port application) and those found from a set of conventional multiline TRL coplanar circuit standards (for two port application) respectively, and the two were found to be in good agreement for both cases.

Next, the first heterogeneous integration of GaAs Schottky diodes onto micromachined on-wafer probes for innovative metrology tools was implemented, a temperature sensing probe. The thermometer probe was designed through electrical and mechanical simulations and fabricated in the clean room. The four point sensing current-voltage characterization of the temperature sensor probe chip showed that a functioning GaAs Schottky diode was successfully integrated onto the micromachined probe. Proof-of-concept diodes as temperature sensors were characterized in cryogenic probe station (liquid nitrogen cooling) and closed-cycle cryostat (liquid helium cooling) respectively and showed comparable performance to commercial GaAlAs diode temperature sensors in the range of 70 K-300 K. Proof-of-concept characterization of a thermometer probe with an dummy sample of open-circuited diode sensor was also performed to evaluate the technical challenges of the measurement setup.

Finally, another implementation of heterogeneous integration of GaAs Schottky diodes onto micromachined on-wafer probes was proposed, a six port reflectometer. The circuit design, including electrical and mechanical simulations was discussed in detail. The measurement approach of the integrated six port reflectometer was also planned. The measurement plan consists of mechanical characterization of contact force using load cell, as well as electrical characterization of calibrating the six port reflectometer using conventional coplanar offset shorts/opens and electronic diode standards. Proof-of-concept on-wafer DUTs were designed and fabriacted to evaluate the performance of the integrated six port reflectometer. Critical steps of the fabrication process had been evaluated and chip fabrication is still in progress.

The new contributions of this thesis include:

- The development of a new fabrication process for quasi-vertical Schottky diodes heterogeneously integrated on silicon: diodes with exellent RF performance was realized with much better yield.

- The first demonstration of submillimeter wave on-wafer electronic calibration up to 500 GHz, for both one port and two port S-parameters measurement, using heterogeneous integrated Schottky diodes onto silicon: electronic calibration using integrated Schottky diodes as standard can achieve good agreement of measurement accuracy compared to conventional calibration approaches.

- The first current-voltage characterization of heterogeneous integrated Schottky diodes onto silicon in cryogenic temperatures ranging from 8.5 K to 300 K: integrated Schottky diodes onto silicon could be used as temperature sensors for cryogenic applications and achieved comparable performance to commercial GaAlAs diode sensors from 70 K to 300 K.

- The first implementation of heterogeneous integrated Schottky diodes onto micromachined on-wafer probes for temperature sensing and terahertz on-wafer S-parameters measurement: diode sensors integrated onto on-wafer probes enables the flexibility of miniaturization of metrology tools, which is especially useful when feed-throughs have to be introduced to interface the DUT within a sealed chamber or cryostat and measurement equipment ouside the chamber.

7.2 Future work

Future research related to this dissertation involves evolving the process of heterogeneous integration of Schottky diodes onto silicon. New III-V (gallium nitride etc.) and host substrate materials (silicon carbide or diamond) as well as new bonding agents could be explored to further simplify the process, improve the yield and push the power handling limits. Cold-weld direct bonding offers great thermal handling and is inherently compatible with the current diode process. Process of the RIE and wet etch of the new ohmic contact stack using gold-gold bonding needs to be developed.

Another direction of future work could be optimizing the diodes' impedances across the Smith Chart to get lower uncertainty of S-parameter measurement using diodes as the electronic calibration standard. Adding tuning elements or additional diodes could help to increase the coverage of diode standard over a larger portion of the Smith Chart.

For the temperature sensor probe and the six port reflectometer probe, a thorough and complete characterization is needed to evaluate the performances of the two types of probes with integrated diode sensors. For the temperature sensor probe, both electrical and mechanical measurements could be performed. The temperature sensor probe can be characterized above room temperature on the hot plate, or below freezing point in the cryostat. The mechanical properties of the temperature sensor probe also can be characterized using a load cell. An iterated version of the temperature sensor probe could eventually incorporate the transmission line to measure the in-situ S-parameters and temperatures simultaneously of an on-wafer DUT.

Additionally, for the six port reflectometer probe, conventional calibration using coplanar offset circuits as well as diodes as electronic calibration standards could be investigated. Both one port and two port on-wafer S-parameters measurement using a single six port reflectometer probe and two six port reflectometer probes could be investigated too. Furthermore, future research directions include integrating a source such as frequency multiplier (chain) onto the micromachined on-wafer probe as well as the six port reflectometer to function as an integrated VNA module on chip to realize the miniaturization of VNA for submillimeter wave and THz applications.

Finally, another possible research direction stemming from this research is to integrate diodes loading the transmission lines in the micromachined on-wafer probe to achieve a diode type slug tuner. The junction capacitance modulation of the varactors through varying bias voltage can realize the impedance modulation required for on-wafer load-pull measurement for power amplifiers.

List of Publications

This thesis is based on the following papers:

1. **L. Xie**, M. F. Bauwens, S. Nadri, M. E. Cyberey, A. Arsenovic, A. W. Lichtenberger, N. Scott Barker, and R. M. Weikle, II, "One port submillimeter-wave on wafer electronic network analyzer calibration with heterogeneously integrated GaAs Schottky diodes onto silicon", *93rd ARFTG Microwave Measurement Conference*, Boston, MA, USA, June 2019, accepted

2. S. Nadri (co-first author), **L. Xie** (co-first author), M. Jaffari, N. Alijabbari, M. E. Cyberey, A. W. Lichtenberger, N. Scott Barker, and R. M. Weikle, II, "A 160 GHz frequency quadrupler based on heterogeneous integration of GaAs Schottky diodes onto silicon using SU-8 for epitaxy transfer," *IEEE MTT-S International Microwave Symposium*, Philadelphia, PA, USA, June 2018, pp.769-772, doi: 10.1109/MWSYM.2018.8439536

3. **L. Xie**, C. M. Moore, M. E. Cyberey, S. Nadri, N. D. Sauber, M. F. Bauwens, A. W. Lichtenberger, N. Scott Barker, R. M. Weikle, II, "Micromachined probes with integrated GaAs Schottky diodes for on-wafer temperature sensing," *International Instrumentation and Measurement Technology Conference*, Houston, TX, USA, May 2018, pp. 1–6, doi: 10.1109/I2MTC.2018.8409690.

4. **L. Xie** (co-first author), S. Nadri (co-first author), N. Alijabbari, M. E. Cyberey, M. F. Bauwens, A. W. Lichtenberger, N. Scott Barker, and R. M. Weikle, II, "An epitaxy transfer process for heterogeneous integration of submillimeter-wave GaAs Schottky diodes on silicon using SU-8," *IEEE Electron Device Letters*, vol. 38, no. 11, pp. 1-4, Nov. 2017, doi: 10.1109/LED.2017.2756920

The following publications are not included due to an overlap in contents or the contents are beyond the scope of this thesis.

1. C. Zhang, M. Bauwens, M. E. Cyberey, **L. Xie**, A. W. Lichtenberger, N. Scott Barker and R. M. Weikle, II, "A micromachined differential probe for on-wafer measurements in the WM-1295 (140—220 GHz) band", *IEEE MTT-S International Microwave Symposium*, Boston, MA, USA, June 2019, accepted

2. S. Nadri, **L. Xie**, M. Jafari, M. F. Bauwens, A. Arsenovic, R. M. Weikle, II, "Measurement and extraction of parasitic parameters of quasi-vertical Schottky diodes at submillimeter wavelengths", submitted to *IEEE Microwave and Wireless Components Letters*, March 2019.

3. R. M. Weikle, II, S. Nadri, C. M. Moore, N. D. Sauber, **L. Xie**, M. E. Cyberey, N. Scott Barker, A. W. Lichtenberger, and M. Zebarjadi, "Thermal characterization of quasi-vertical GaAs Schottky diodes integrated on silicon using thermo-reflectance and electrical transient measurements", in *Proc. Additional Conf. (Device Packag., HiTEC, HiTEN, & CICMT)*, Jan. 2019, in publication

4. R. M. Weikle, II, **L. Xie**, S. Nadri, M. Jafari, C. M. Moore, N. Alijabbari, M. E. Cyberey, N. Scott Barker, and A. W. Lichtenberger, "Submillimeter-wave Schottky diodes based on heterogeneous integration of GaAs onto silicon", 2019 United States National Committee of URSI National Radio Science Meeting (USNC-URSI NRSM), University of Colorado at Boulder, CO, USA, Jan. 2019, pp. 1-2, doi: 10.23919/USNC-URSI-NRSM.2019.8713040

5. S. Nadri, C. M. Moore, N. D. Sauber, **L. Xie**, M. E. Cyberey, J. T. Gaskins, A. W. Lichtenberger, N. Scott Barker, P. E. Hopkins, M. Zebarjadi, and R. M. Weikle, II, "Thermal characterization of quasi-vertical GaAs Schottky diodes integrated on silicon", *IEEE Transactions on Electron Devices*, vol. 66, no. 1, pp. 349-356, Jan. 2019, doi: 10.1109/TED.2018.2880915

6. Y. Feng, M. DeJarld, R. M. Weikle, II, **L. Xie**, P. M. Campbell, R. L. Myers-Ward, D. K. Gaskill and N. Scott Barker, "Millimeter-wave detection on basis of graphene photo-

thermoelectric effect", *2018 13th European Microwave Integrated Circuits Conference (EuMIC)*, Madrid, Spain, Sept. 2018, pp. 361-364, doi: 10.23919/EuMIC.2018.8539872

7. A. J. Mercante, S. Shi, P. Yao, **L. Xie**, R. M. Weikle, II and D. W. Prather, "Thin film lithium niobate electro-optic modulator with terahertz operating bandwidth", *Optics Express*, vol. 26, no. 11, pp. 14810-14816 (2018), doi: 10.1364/OE.26.014810

8. Q. Yu, Y. Wang, **L. Xie**, S. Nadri, K. Sun, J. Zang, Q. Li, R. M. Weikle, II, and A. Beling, "High-performance InGaAs/InP photodiodes on silicon using low-temperature wafer-bonding", *in Conference on Lasers and Electro-Optics, OSA Technical Digest (online) (Optical Society of America, 2018)*, San Jose, CA, USA, May 2018, pp. SM2I. 1, doi: 10.1364/CLEO_SI.2018.SM2I.1

9. C. Zhang, M. Bauwens, **L. Xie**, M. E. Cyberey, N. Scott Barker, R. M. Weikle, II and A. W. Lichtenberger, "A micromachined differential probe for on-wafer measurements in the WM-1295 (140—220 GHz) band", *IEEE MTT-S International Microwave Symposium*, Honololu, HI, USA, June 2017, pp. 1088-1090, doi: 10.1109/MWSYM.2017.8058784

10. M. Eller, N. Sauber, A. Arsenovic, S. Nadri, **L. Xie** and R. M. Weikle, II, "A monostatic coded aperture reflectometer for imaging at submillimeter-wavelengths", *IEEE MTT-S International Microwave Symposium*, Honololu, HI, USA, June 2017, pp. 1207-1209, doi: 10.1109/MWSYM.2017.8058820

11. R. M. Weikle, II, H. Li, A. Arsenovic, S. Nadri, **L. Xie**, M. F. Bauwens, N. Alijabbari, N. Scott Barker and A. W. Lichtenberger, "Micromachined interfaces for metrology and packaging applications in the submillimeter-wave band," *Additional Conferences (Device Packaging, HiTEC, HiTEN, & CICMT)*, Jan. 2017, DPC, pp. 1-36, doi: 10.4071/2017DPC-THA3_Presentation2

12. S. Hawasli, S. Nadri, **L. Xie** and R. M. Weikle, II, "An integrated 100-element Schottky varactor diode array for sideband generation at 1.6 THz", *IEEE MTT-S International Microwave Symposium Digest*, San Francisco, CA, June 2016, pp. 1-4, doi: 10.1109/MWSYM.2016.7540263

13. R. M. Weikle, II, C. Zhang, S. Hawasli, S. Nadri, **L. Xie**, N. Scott Barker and A. W. Lichtenberger, "Terahertz diode arrays and differential probes based on heterogeneous integration and silicon micromachining," in *Proc. Additional Conf. (Device Packag., HiTEC, HiTEN, & CICMT)*, Jan. 2016, pp. 924–962, doi: 10.4071/2016DPC-TP36

14. S. Nadri, **L. Xie**, N. Alijabbari, B. Foley, J. Gaskins, P. Hopkins, R. M. Weikle, II, "Steady-state thermal analysis of an integrated 160 GHz balanced quadrupler based on quasi-vertical Schottky diodes", in *Proceedings of Infrared Millimeter and Terahertz Waves (IRMMW-THz)*, pp. 1-2, Aug. 2015, Hongkong, China, doi: 10.1109/IRMMW-THz.2015.7327482

Appendices

Appendix A

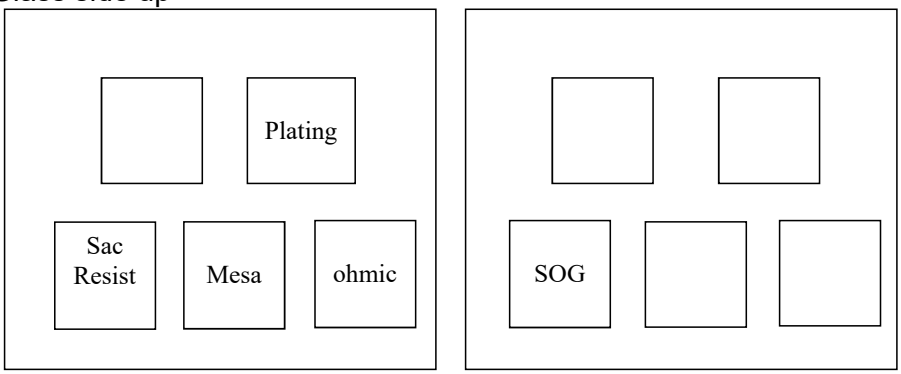
Diodes Fabrication Recipe

Updated: 09/05/2017

Diodes on Mesa with Beam Leads Process Sheet

Masks involved (**the glass side facing up**) for the process:

Glass side up



CPW mask Mirrored and flipped mask

AZ400 K:DI=1:4 for all thickness photoresist development

Non-alloyed ohmic contact_DMBL 01 Chips DMBL01

Name – Module 01: Non-alloyed ohmic contact (Note: 3 hours for 2 samples)				
	Process	**Description**	**Date**	**Done**
0	Mask cleaning	Clean the mask, check the AZ 300T level and the station temp (80C)		
1	No mounting on Si carrier Mark the backside with scalpel	The black wax might vaporize and condense on the sample in the evaporator 78-82C recorded highest temp during evaporation		
2	D'limonene/METH spray	Put the InGaAs/GaAs piece in beakers in sequence Watch for possible black films, redo the bath if see the films, or use AZ400K with swab		
Always use one tweezer and the filter paper to handle the sample to keep from contamination.				
OR use two dedicated clean tweezer to handle the InGaAs piece.				
Use the black anti-static dish or Al foiled dish after the bath.				
3	Spin Clean	TCE/RA/METH with swab, BD		

⚠ Handle with special care

Updated: 09/05/2017

4	Ethelene Glycol swab if not clean yet	Try to avoid AZ400K if possible.		
5	Toothpick	Remove or break the black dots		
6	Redo 3 and 4			
7	NO MARCH	O2 might oxidize n++ InGaAs		
8	Preparation of the evaporator	**The less the mount time the better.**		
		Clean the chamber and fill in the target before surface clean. Change the crystal if previous runs include Cr or the lifetime is low.		
		Wipe the crucible, metal and refilled metal with IPA Remove the clips of the chuck, wipe clean with IPA.		
9	BOE Surface clean with one dedicated clean twizzer	1:10 buffered oxide etchant (BOE), 20 s		
		1:10 NH4OH 20s for better adhesion		
		NO DI rinse might leave residue. DI rinse and fast BD		
10	Load in Evaporator	Use the double sided tape to mount sample on the chuck.		
		Long, single tape so that it's easier to unmount later.		
		Press the tape flat with the cover tape before mount.		
		BD to mount. Knock to check.		
		Put the samples to the inner ring position for lower temperature		
		Use the smaller one to get a better heat sink		
11	Pump Down	Pressure <1.0E-6 torr – Start t=		
12	Deposition	**DO NOT do Ar Ion Mill**	→	
		Compensate the thickness with+20%.		
		Ti 48 nm (480A) for 40 nm, 0.5 A/s	→	
		Cool down for 15-20 minutes		
		Pd 48 nm (480A) for 40 nm, 0.3 A/s		
		Cool down for 15-20 minutes		

Updated: 09/05/2017

		Au, stick to using the shinning one 90 nm (900A)+ 90 nm (900A) for 75nm+75nm, 0.5 A/s	→	
		Cool down for at least 3 hours in between the two Au sessions Overnight cooling is preferred too	→	
		Ti 24 nm (240A) for 20 nm, 0.5 A/s		
13	Unmount the sample from the tape on the chuck **immediatedly**	Use the double-flat tweezer to unmount carefully to avoid cracking		
14	Clean the sample with Ti on top	TCE/RA/METH spin clean with swab		
		Check under the microscope		
15	Inspect using Leica MZ12 and use toothpick if necessary	CLEANLINESS IS CRUCIAL REDUE CLEAN IF NECESSARY		
16	Plasma Clean	O2, 200 W, 10min		

Updated: 09/05/2017

Non-alloyed ohmic contact _DMBL _01 Chips DMBL01

Name – Module 02: SU8 Bonding to SOI **(Note:)**		

Refer to
Bonding GaAs to SOI using Ed's press jig with SU-8 TF6000.5_table format_12182016.docx

Updated: 09/05/2017

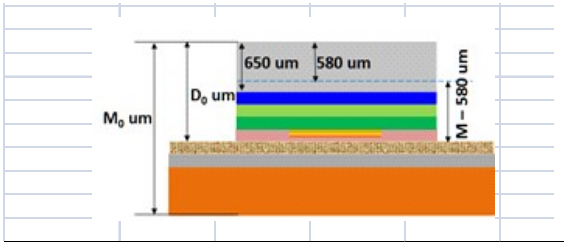
Non-alloyed ohmic contact_DMBL _01 Chips DMBL01

Name–Module 03:SI-GaAs&AlGaAs Removal (Note:)				
	Process	**Description**	**Date**	**Done**
1	Clean the handle of GaAs	TCE to remove L-grease AZEBR and AZ400K to remove rainbow films		
2	Clean the SU8 on the edge of Si carrier	Use the scalpel under LEICA		
3	E-glycol swab clean			
4	Spin Clean	TCE/RA/METH wl swab		
5	**Plasma Clean This is important!**	**March 200 W >10 min until the temp of Nitric:H2O2:DI is ready at 50C**		
6	Fast GaAs Etch (~580 nm, 24 min) **Shake from time to time to get rid of the bubbles**	Etch GaAs in HNO3:H202:H20 (1:6:1) @ 50C 5 min, rotate 180 deg 5 min, rotate 180 deg 5 min, rotate 90 deg **DON'T MEASURE because thinned GaAs will be easily damaged by the Onosoki probe tip.** Soak another 9 min (OR less) but watch for bubbles Take out immediately if see a lot of rapid bubbles		
7	Slow GaAsEtch (stop on AlGaAs, ~70 nm, 1 to 1.5 hours)	**DON'T MEASURE.** Transfer to water beaker for 10 sec then very quickly more to C6H8O7:H202, 3:1 @ 50C Move it to the BOE/HF room It will stop selectively on AlGaAs: **surface turns dark and smooth, wait for another 5 min** t = min		
8	**DI soak and Rinse**	**Keep in citric beaker, prepare HF ahead of time, then quick rinse in 2 water beakers (very quick transfer time)**		
9	Remove AlGaAs	1 min etch in HF, watch for two flashes Should be done in less than 40s BOE or HCl:DI=1:1 didn't work well		
10	Rinse	DI soak for 5min BD		

⚠ **Clean the etchants!**

Updated: 09/05/2017

11	**Spin clean**	**METH only**, with swab, helps to clean the sample		



Updated: 09/05/2017

Non-alloyed ohmic contact_DMBL 01 Chips DMBL01

Name– Module04- Big Mesa Formation: (Note:)				
	Process	**Description**	**Date**	**Done**
1	Spin Clean	TCE/METH Spin, BD		
2	**DO NOT MARCH**			
3	Spin HMDS	2in chuck, filter with a poking hole 4000 RPM 30s Bake 110C 30s		
4	Spin Resist	AZ4330, 3000 RPM, 30s for ~4um thickness Backside clean and edgebead removal with RA/(DI) swab		
5	Soft Bake	**110C, 1 min**		
6	Expose in MJB4	400s using the SODA LIME mask, SOG etch pattern Offset to avoid the damaged area covering the alignment makers		
7	Develop	AZ400K 1:4 ~1 min20s flash+20s		
8	DI	Di soak, rinse and blow dry		
9	Inspect			
10	Hard Bake	110C 1min, 130C 5 min		
11	Tencor the PR	Should be around 4 um		
12	Prepare GaAs and Ti etch	H2SO4:H2O2:DI for GaAs on top of metal field, go straight to BOE for Ti		
13	GaAs big mesa wet etch	H2SO4 (98%): H2O2:DI=2.5 mL:20mL:400 mL Watch for interference pattern Should be done around 3min		
14	DI X2			
15	Ti RIE etch	Semigroup 1min30s~2min CHF3=5 sccm, SF6=20 sccm, N2=0.62 sccm, RF=80W, DC=-300V, press=35 mTorr		
16	Semigroup chamber clean with O2	>10 min		

Updated: 09/05/2017

17	Pd wet etch	Transene TFA:DI=2:1 10s The sample would look like purple films on top of Au surfaces since the TFA attacks Au too		
18	Au dry etch	Semigroup Ar etch of Au Ar sccm, Press 22.7 mTorr, RF 120 W, DC -722V 5min, (2min), 5min, add extra sessions if necessary until see the propagating films of Au		
19	Au wet etch clean	HG800 1~2min		
		Check under microscope		
20	Ti dry etch	Semigroup 1min30s~2min CHF3=5 sccm, SF6=20 sccm, N2=0.62 sccm, RF=80W, DC=-300V, press=35 mTorr		
		Check under microscope and SEM		
21	SU8 etch	Use a 3in plastic petri dish (flat bottom one) for Semigroup etch		
		CF4 23.3 sccm, RF 200W, DC -787 V, Press 26.0 mTorr, 5min, 2min idling, 5min		
		Check under microscope and SEM		

Updated: 09/05/2017

Non-alloyed ohmic contact_DMBL _01 Chips DMBL01

Name– Module05 – Small mesa (Note:)				
22	Etch Mesa	**@Room temp, NOT 50 C** Citric acid:H2O2 :: 5:1 Remove 1.2 um GaAs and stop on SOG ER~340 nm/min Interference pattern appears and stops (**purple↔green→purple**) ~4 mins to start, 5~6 mins to stop **Undercut is NOT wanted**. DI, BD		
22	Leave Mesa Resist on			
23	HMDS Coat	4000 RPM for seconds until see the flash Bake 110C 30s		
24	Resist Coat	AZ4330,3000 rpm,30 sec, 4.2~4.3um		
25	Soft Bake	100C, 1 min		
26	Pattern Exposure	Use DMBL01-L03 **Mask mesa etch Doubler1/Quad1** **EV620 Settings:** Mask Size _4", MaskThk 2.5 um Contact _Hard Vac, Sub Size_2"_ SubThk _1.5 um _, Exp t _**60 sec**_ Separation 60 um Resist Thk_**4.0 um**_		
27	Condition	5 min		
28	Develop	AZ400K 1:4, ~1 min Dev History: L01 →_____ min		
29	Hard Bake	130C, 5 min		
33	Plasma Clean	O2, 200 W, 10 min to burn down the hardened PR		
34	Remove Resist	RA or ACE spray, METH, DI, BD		
35	NMP:Propylene Glycol bath	> 5h @ 100 C with stirring to remove the UV cured resist covering the mesa islands If > 110C, some ohmic patterns got lift off		
36	Plasma clean	O2 150W 5min		

Updated: 09/05/2017

Non-alloyed ohmic contact_DMBL _01 Chips DMBL01

Name– Module06 – Planarizing & Top Metal (Note: finish this in the same day)				
	Process	**Description**	**Date**	**Done**
1	Spin Clean	E/M Spin&BD		
2	Plasma Clean	O2,200 W, 8 min		
3	Spin HMDS	4000 RPM 30s		
4	Spin Resist	AZ4210 4K RPM, 30s, 2.1 um		
5	Backside and Edge bead removal	Use the swab with RA/METH		
6	Soft Bake	**90C 2 min** 100C might cause reflow of sac resist leading to round corner of airbridge		
7	Pattern Exposure	Use DMBL01-L06 **(Sacresist)** **EV620 Settings:** Mask Size _4", MaskThk 2.5 um Contact _Hard Vac, Sub Size_ 2"_ SubThk _1.5 um _, Exp t _**120 sec**_ Separation 60 um Resist Thk_**2.0 um**_		
8	Condition	5 min		
9	Develop	AZ400K **1:4**, 50 sec flash Dev History: L01 →_____ min **Check under 50 X at least for the anode.**		
10	Plasma Clean	O2,150 W, 4 min		
11	Pre-Metal Dep	20 sec BOE, 15 sec NH4OH:DI =>1:20 Blow dry		
12	Ti & Au Metal Dep	No Ar Ion Mill Sputt3: 1.5min (10 nm) Ti and 2min30s (50 nm) Au		
13	Plasma Clean	O2,150 W, 5 min		
14	Spin HMDS	4000 RPM for seconds until see the flash		
15	Spin Resist	AZ4330, 2000 RPM, 30s (5.0 um to cover the sacrificial resist)		

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16	Soft Bake	**90 C, 2 min**		
17	Pattern Exposure*	Use DMBL01-L07 **(Plate)** **EV620 Settings:** Mask Size _4", MaskThk 2.5 um Contact _Hard Vac, Sub Size_2"_ SubThk _1.5 um_, Exp t _**220 sec**_ Separation 60 um Resist Thk_**5.0 um**_		
18	Condition	5 min		
19	Develop	AZ400K **1:4**, 2 min flash Dev History: L01 →_____ min **Check under 50 X at least for the cap and anode.**		
20	Plasma Clean	O2,150 W, 5 min		
21	Electroplate Au	Au 2 um final thick = _____ Iplate= 1mA, 2mA, 3mA 3min each,4mA Vlimit= 5V Typical voltage and current I(mA) 1 2 3 V(V) 0.55 0.60 0.70 T(min) 3 3 6.5 Plated thickness: ~1 um Do multiple plating to get desired thickness		
22	Top Resist Removal	Flood expose sample in MJB4, 200 sec, CP=>CI, CH1, go back to CP when done Develop in 400K:DI :: 1:4		
23	Plasma Clean	O2, 200W, 20 min		
24	Remove Seed Layer	Au → in HG1200, 1min Ti →in BOE, 25s+5s		
25	O2 etch using Semigroup			
26	MARCH clean	200W 10min		
27	Acetone	ACE Spray gently, a thin film residue around the mesa is OK, as long as the surface of the mesa looks clean Microscope and SEM check, IV test.		

Appendix B

Recipe of GaAs Bonding to Silicon

Ver: 12/20/2016

Bonding GaAs to SOI using Ed's Jigg with SU-8 TF6000.5

DMBL 01 **Chips DMBL01**

Name – Module 01: Prepare the SOI wafer (Note:)				
	Process	**Description**	**Date**	**Done**
1	Strip tape	Strip the tape from the SOI wafer		
2	Scratch the edge	Scratch the edges with the surgical blade under LEICA microscope		
3	Spin Clean	ACE/METH,with swab gently towards the edge and stay around the edge for seconds		
		TCE/RA/METH with swab in the litho room		
4	March	200 W, 10 mins		
5	Pretreat	200 C for 5 mins		

DMBL 01 **Chips DMBL01**

Name – Module 02: Spinning SU-8 TF6000.5 onto SOI (Note:)				
	Process	**Description**	**Date**	**Done**
1	Prepare AZEBR in beaker with swab	To clean the spinner and the backside & edge of the SOI later		
2	SU8 types	SU8 TF6000.5 with built-in adhesion promoter for thin films coating (<1um)		
3	Clean the force distribution plate	TCE/RA/METH, heat up on 110C hotplate, wait until stabilized put a dot of L-grease at the center		
4	Coat SU8	Spin coat 1 ml SU8-TF6000.5 on the SOI using micropipette		
		Spin as AZ series resist at **9.7 KRPM for 35sec to get ~250 nm thickness**		
5	Back side & edge bead clean	Clean residual SU-8 from backside and the edge bead with **AZEBR & DI** Avoid splashed DI from the tap		

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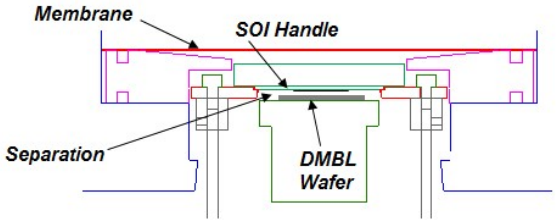
6	Soft bake SOI	**1 min 110C on the force distribution plate** **Avoid rapid cooling down afterwards** **Let it cool for about 10min until slightly warm or close to room temperature**		
7	Double check the InGaAs piece's surface cleanness	NO MARCH		
8	Expose the SOI in MJB3	Handle the mounted SOI on the force distribution plate with caution 280 mJ/cm^2 → **Must Use the quartz filter** labeled "SU8 filter", otherwise the features will get deformed suffering the overexposure **Channel 2 (7mW/cm^2)** **MJB3, 40sec**		
11	Bonding	Set-up mated wafers in Membrane Bonding Jig and Bond at **140C** (130 C to 150 C) for **1 hour 30min using 10 psi difference**		



a. Detail of mechanism for holding DMBL and SOI samples separated during pumping prior to vacuum attach.

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DMBL 01 **Chips DMBL01**

Name–Module 03: Bonding jig (Note:)				
	Process	**Description**	**Date**	**Done**
0	Clean the membrane	Wipe clean with TCE, RA, METH, BD		
1	Open top lid	Open the upper lid		
2	Thermal couple	Check if the thermal couple is in good contact		
3	Clean copper block	Swipe and scrub on filter paper to clean it		
4	Separate the cooling block	Turn the screw in the backside to separate the black-oxidized and shinning cooling block		
5	Separate GaAs and Si	Turn the screw in the front side clockwise to separate the force distributing block and the other one facing towards it. Now the reading should be around "**2**" (See figure 1 below the table)		
6	**Level the stage**	Use the bubble level, adjust the thermocouple if necessary		
7	L grease copper block and GaAs on block	**No need to heat up to 60 C for reflow then cool down because the 65C/95C softbake and exposure already partially cured the SU8.** A little L-grease, GaAs on.		
8	Si on top	Blow dry the carrier+force-distribution-plate with N2 gun from the main clean room, put it on the top of the GaAs sample Now the GaAs sample and the SOI are facing each other.		
9	Thick aluminum	Place the thick aluminum ring and check that the two O rings are **tightly fit in**		
10	Membrane	Place the membrane on top		
11	Thin Al ring	Place it on top of the membrane, make sure the O-ring is **tightly fit in, push hard down**		
12	Put the lid on	No need to tighten the screws		
13	Turn on	Turn on the button between the LED display and the heater, turn on the pump on by plugging in, make sure every valve is OFF		

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14	Set the temp to 30C	Wait until stabilized at 30C		
15	Turn on Upper chamber	Turn on the upper chamber pump S3(the right middle valve) for seconds until **-30 psi**, turn off		
16	Pump lower chamber	Counterclockwise of the left black knob S5 and make the green valve S2 horizontal wait for **40 min for outgassing at 30C**		
17	Contact mode	Turn the screw counterclockwise to bring the force distribution plate and the one facing towards it (NOT the black and silver block!) in contact, until there's a tiny gap between the screw tips		
18	Turn on N2	Now, the left gauge should be **-27 psi** and the right gauge should be **-18~-19 psi**. If needs increasing the pressure for the upper chamber, turn on N2 and off of the cylinder, and SLOWLY open the N2 valve S4 to increase the pressure of the upper chamber If needs adjustment, slowly release the black knob a little bit and turn it off		
19	Set temp to 130 C	Set the temp to be **140 C**, takes around 4+10 mins to ramp up		
20	**Close valves**	**When the temperature reaches 70 C, close all the valves**		
21	When 130 C wait	When the temp reaches **140 C**, wait for **1hour 30 min**		
22	Cool	Turn on the chiller and set the temp to room temp + bring the cooling block in contact		
23	Open the lid	When the temp drops to **70C**, typically all vacuum is lost. Safe to open the lid and take out everything. Be careful of the heat! **Take out the sample no lower than 60C when the L-grease is still liquid!** Slide out the bonded wafer stack from the liquid L-grease		
24	Clean L grease	Clean with the wipe The stack might get stuck, detach with caution		
25	Turn off	Make sure every switch is off and unplug the pump		

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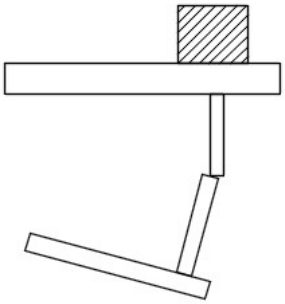

Figure 1

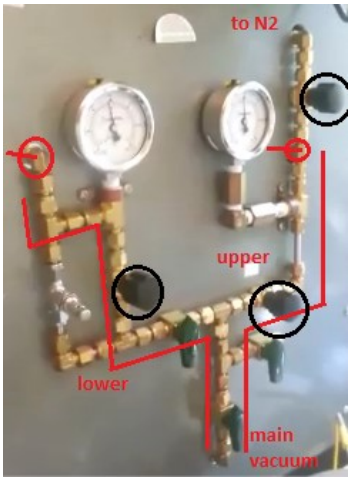

Figure 2

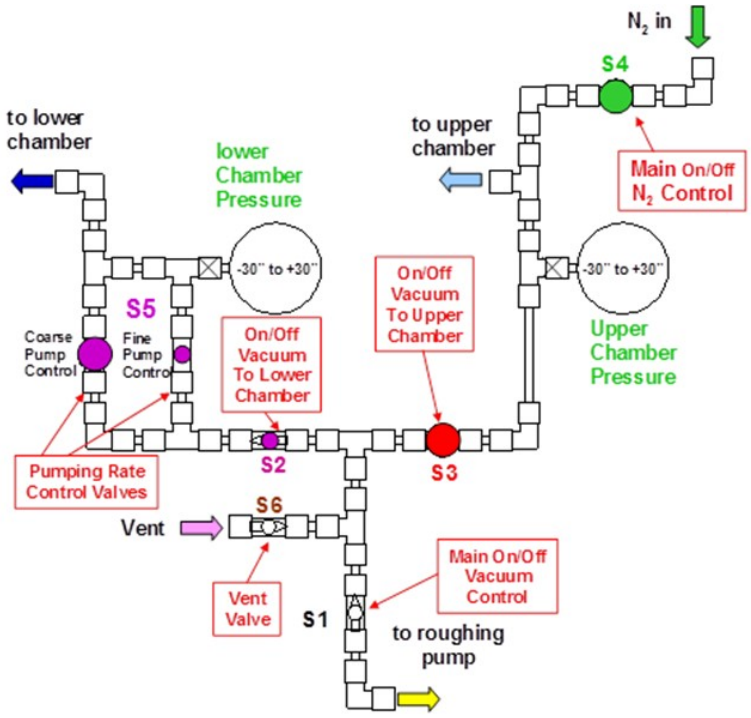

Figure 3. Diagram of Valve Control System

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